OS300 20MHz DUAL TRACE OSCILLOSCOPE Instruction Manual

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Introduction

Section 1

The OS300 is a versatile general purpose dual trace oscilloscope intended for general laboratory, industrial, servicing and educational applications. The full 8 x 10cm rectangular tube provides a bright display against the calibration graticule.

It features two identical input channels with a maximum sensitivity of 2mV/cm and a bandwidth from D.C. to 20MHz. These channels may be displayed separately or together in dual trace mode. Alternatively they can be added or subtracted for sum or difference display. The timebase ranges from 0.2s/cm to 0.5μs/cm and a x 10 expansion facility extends this to 50ns/cm. Independent variable sensitivity and sweep rate controls are provided.

Particular attention has been paid to trigger performance, with D.C. and A.C. coupling available and a bright-line free-run facility to enable trace location in the absence of trigger. An active T.V. synch separator is provided for those working with video waveforms.

The OS300 includes many facilities such as a 1kHz calibrator, a D.C. coupled Z modulation input and a trace rotation control, usually found only on the more expensive instruments.

This compact instrument is readily portable. The internal construction is based largely on a single printed circuit board assembly to provide easy access for maintenance and minimum cost of ownership.

Specification

Section 2

DISPLAY
8 x 10cm rectangular mono-accelerator c.r.t. at 2kV e.h.t. Trace Rotation by front panel preset.

VERTICAL DEFLECTION
Two identical input channels CH1 and CH2.
Bandwidth (–3dB)
d.c. to 20MHz (2Hz to 20MHz on a.c.)
Sensitivity 2mV/cm to 10V/cm in 1–2–5 sequence.
Accuracy ±3%
Variable Sensitivity > 2,5:1 range allows continuous adjustment of sensitivity from 2mV/cm to 25V/cm.
Input Impedance 1MΩ/28pF approx.
Input Coupling DC-GND-AC
Input Protection 400V d.c. or pk a.c.

DISPLAY MODES
Single Trace CH1 or CH2
Dual Trace Chopped or Alternate modes automatically selected by the T.B. switch. Between 0.5μs/cm and 0.2ms/cm the ALTERNATE MODE is selected. Whilst on ranges slower than 0.2ms/cm CHOP MODE is selected. The CHOP frequency is 500kHz.
Add CH1 and CH2 added to give the algebraic sum of the two channels.
Invert CH2 CH2 may be inverted. When used in conjunction with Add mode it gives the algebraic difference of the two channels.
X–Y CH2 input gives Y deflection and CH1 input gives X deflection.
Bandwidth (–3dB) DC to 1MHz with less than 3° phase shift at 50kHz.

HORIZONTAL DEFLECTION
Timebase 0.5μs/cm to 0.2sec/cm, 18 ranges in 1–2–5 sequence
Accuracy ±3%, (to 200ns/cm)
X Expansion x 10 push button gives fastest speed of 50ns/cm. Accuracy ±3% (50ns/cm range ±5%)
Variable Sweep > 2.5:1 allows continuous coverage from 0.5μs/cm to 0.5sec/cm.

TRIGGER
Variable level control with Bright Line ON/OFF facility. With Bright Line on, the timebase free-runs when insufficient signal (20Hz -20MHz) is present or when the selected level is outside the range of the input signal.
Source Internal CH1 or CH2 or External.
Slope + or –.
Coupling DC, AC or TV (active sync. separator with line/frame selected by T.B. switch between 50 and 100μs/cm).
Sensitivity
Internal: DC coupled 2mm to 2MHz, 5mm to 20MHz.
AC coupled 2mm, 10Hz–2MHz.
5mm, 4Hz–20MHz.
External: DC coupled 100mV to 2MHz, 400mV to 20MHz.
AC coupled 100mV, 10Hz to 2MHz,
400mV, 4Hz to 20MHz.
External Input Impedance 100kΩ/10pF approx.
External Input Protection 250V d.c. or pk, a.c.

ADDITIONAL FACILITIES
Calibrator 1V, 2% squarewave at approx. 1kHz.
Ramp Output Approx. +3.5V ramp from 5kΩ.
Z Mod. Input DC coupled, 2V visible mod. sensitivity, +40V cut-off sensitivity, input impedance 10kΩ/10pF approx.
Maximum input 100V d.c. or pk, a.c.

SUPPLY
100V, 120V, 220V and 240V ± 10%
45 to 440Hz approx. 40VA.

SAFETY
Designed for I.E.C.348 Cat. 1.

OPERATING TEMPERATURE RANGE
0 to +50°C (+15 to +35°C for full accuracy)

DIMENSIONS
140 x 305 x 460mm

WEIGHT
6kg approx.

ACCESSORIES SUPPLIED
Handbook P.N. 402011
Mains lead P.N. 402001

OPTIONAL ACCESSORIES
Probe Kit PB12
A passive probe kit with switched X1 and X10 attenuations. X10 attenuation input impedance is 10MΩ/11.5pF.
Probe Kit PB13
A X10 passive probe with 1.5m of cable. Input impedance 10MΩ/11.5pF.
Viewing Hood
P.N. 450609
Trolley
Type TR7. General Purpose.
Protective Carrying Case
P.N. 42610 A strong case which completely encloses the oscilloscope with 3 thicknesses of padding covering the front panel.
Tube Option
Long persistance c.r.t. P7 phosphor.
Rack Mount Kit
P.N. 450070.
Front Cover
P.N. 450240.

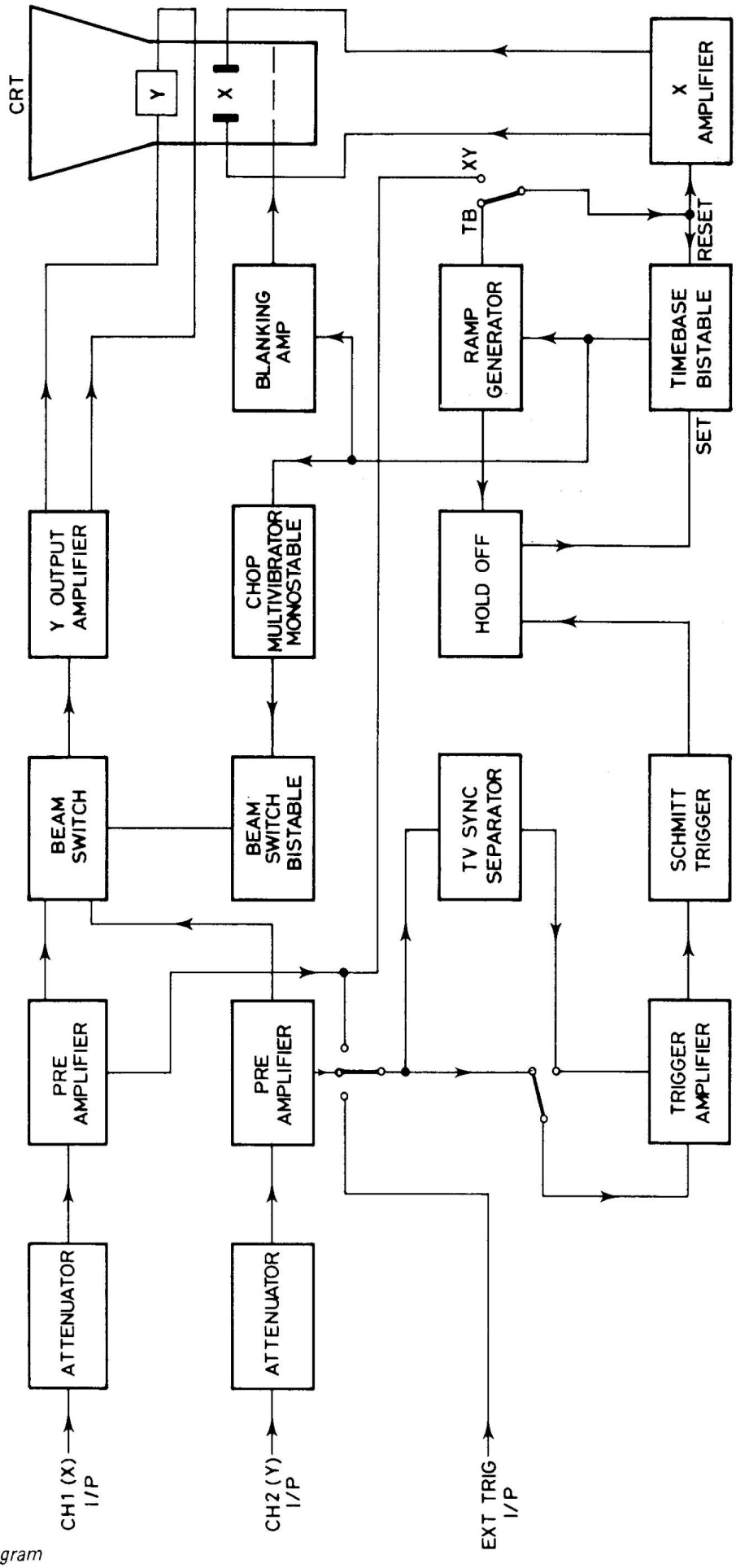

Fig. 1 Block Diagram

The input stage of the pre-amplifier is formed by the f.e.t. source followers, TR201 and TR202, and emitter followers, TR204 and TR203. Unbalance in this stage is corrected by the BAL control potentiometer, R301.

The input stage drives the divider network, RN201. The VOLTS/CM switch second wafer, S201, selects the necessary output, either directly via RN201 on the 2mV or 200mV ranges, or attenuated by 2.5, 5, 10, 25 or 50 times on the subsequent ranges. This network presents a constant output impedance and further attenuation is introduced by the shunt action of the VARIABLE sensitivity control, R217. The resultant signal is amplified by the integrated amplifier, IC301. The amplifier gain is determined by R309 and the preset, R302. The differential output is balanced by the bias through R308 from the preset, R307.

The differential output from IC301 (CH1) or from IC351 (CH2) is selected by the beam switch as the input for the subsequent shunt feedback amplifier stage formed by TR401, TR402. The signal input currents are defined by R316 and R317 and are summed with the Y shift currents defined by R318 and R319 from the CH1 shift control, R315. The corresponding components for channel 2 are R366, R367, R368, R369 and R365. Channel 2 only differs for channel 1 by the addition of the double pole changeover switch, S301, which reverses the output signals from IC351 in the INVERT mode.

The beam switch is formed by the 8 diode gate, D301, D302, D303, D304, D351, D352, D353, D354. The relative control potentials from IC501 allow either the signal current from IC301 and/or IC351 to reach the bases of TR401 and TR402, or divert those currents from the bases.

The outputs from the differential shunt feedback amplifier stage formed by TR401 and TR402, are fed to the gounded emitter amplifier stage, TR403 and TR404. This in turn feeds the differential cascode Y output stage TR405, TR406, TR407 and TR408 to drive the Y deflection plates of the c.r.t.

High frequency compensation of the output amplifier is provided by networks between the emitters of TR403 and TR404 and those of TR405 and TR406. Adjustment of this compensation is by C402 and C405.

4.3 THE TRIGGER CIRCUITS

These circuits are shown in Fig. 5.

The Trigger Source switches, S502 and S503, connect the required trigger signal via the Trigger Coupling switches, S504 and S505, to the trigger buffer amplifier formed by TR601 and TR602. S502 selects the differential CH1 signal via R313 and R314 from IC301 (Fig. 4). S503 selects the equivalent CH2 signal via R363 and R364 from IC351. Where both S502 and S503 are selected, both of the above signals are disconnected and the single-sided input from the EXT TRIG input socket SKC is selected.

When the AC coupling switch, S504, is out, the trigger signals are directly coupled-through, but when this switch is in, AC coupling is introduced via C603 and C604 (C601 on External). TR601 and TR602 form a differential buffer amplifier with the DC balance controlled by the TRIGGER LEVEL control, R602. The differential output from this stage is applied to the comparator, IC602, which has positive feedback applied by R623 to form a Schmitt trigger circuit. The changeover switch, S506, reverses the output from TR601 and TR602 to determine the trigger slope.

When both S504 and S505 are "in" (AC and DC in for TV mode), the junction of R603 and C610 is connected to the −11V supply. D601 and D608 are brought into conduction while D602 and D604 are reverse biased. This diverts the output of the trigger amplifier away from IC602, into TR605, which amplifies the positive tips of the video waveform only. TR605 is prevented from saturation by feeding back the peak detected synch. pulses via TR607 and TR606 to the emitter of TR605. These pulses are amplified by IC601b and applied via R617 and D603 to the Schmitt trigger, IC602. IC601a is used in conjunction with S504 and S505 to disable the synch. separator when AC or DC is selected.

At the fast timebase sweep speeds, S 262a is open and TR603 is cut off. However, at speeds of 100μs/cm and slower, R608 is connected to +11V and TR603 is switched on. This effectively grounds C609 to introduce an RC integrating time constant into the synch. pulse signal time path in the TV mode to separate out frame trigger.

4.4 TIMEBASE GENERATOR AND AMPLIFIER

The square wave trigger output from IC602 is applied (with d.c. bias of zener diode, D605) as the clock to the D type TTL flip-flop, IC501a. A positive-going trigger edge will clock the bistable, driving $\overline{Q}$ low. In the waiting state, $\overline{Q}$ was high (+4.5V), turning on TR261 via R507 and R262, holding the input, and hence the output, of the operational amplifier, IC261 at 0V. This timebase amplifier is connected as a direct voltage follower.

When the trigger signal sends $\overline{Q}$ of IC501a low, the timebase clamp transistor, TR261, is turned off. Part of the constant current generated by TR264 flows through the resistor network, RN272, to charge C263 at a constant rate. The resultant positive-going linear ramp voltage generated at the input of IC261 is buffered by that amplifier to generate the low impedance ramp output.

The timebase range switch, S262, selects the tap point on the network, RN272, to vary the ramp slope in the 1.2.5 sequence over a range of three decades. On all fast sweep ranges, TR262 is biased-off but on ramps 0,5ms/cm and slower, S262c connects R263 to +11V. TR262 is turned on and C264 is effectively connected in parallel with C263 to slow the sweep rate 1000 times.

The constant current into the ramp generator is derived from the current mirror circuit formed by TR262 and TR264. The variable gain control, R261, provides an approximate 3:1 range of variation in this current, R506 provides a preset calibration control on the slow sweep rates, only when S262c is closed.

When the ramp reaches its maximum level the negative bias, introduced by R521 and R519, is overcome and TR503 turns on, driving the reset input of the timebase bistable low. As the bistable switches, $\overline{Q}$ returns high and TR261 conducts to discharge the timing capacitor(s) and the sweep is complete. However, a hold-off action takes place to inhibit trigger signals during sweep and this remains for a short period after a sweep to ensure that the ramp potential is fully reset before the next sweep can be triggered. As the ramp goes positive, D506 conducts to charge C502, reverse biasing D503 and turning on TR502. At the end of sweep when the timebase bistable is reset, $\overline{Q}$ goes low and the D input follows via the action of D508 and R511. The ramp output returns rapidly toward 0V but TR502 remains in conduction for a period determined by C502 and R518. Only when TR502 turns off can R516 and D507 take the D input high for the bistable to respond to the next clock input.

TR501 acts in a way similar to TR262 (described above) to introduce additional hold-off time through C501 on the slower half of the timebase ranges.

The bright line facility causes the timebase to free-run in the absence of trigger signals. The square wave output from the Schmitt trigger, IC602, is coupled via C615 into the peak detector diodes, D606 and D607, to generate a positive-going signal into the –ve input of IC601c driving its output negative. In the absence of such trigger signals for a period determined by C618 with R627 and R626, the output of IC601c goes positive. When TR502 turns off at the end of the hold-off period, D509 conducts to turn on TR504, driving the set input low to initiate another sweep.

This free-run condition is removed as soon as IC601c detects an output from the Schmitt trigger. It can be inhibited also with a positive bias via R625 if the BRIGHT LINE OFF switch, S501, is operated.

The X output amplifier is formed by the shunt feedback stage of TR509/TR511 driving single sided into the amplifier stage, TR513 and TR514. The collector output of this stage drives the X deflection plates of the c.r.t. directly from TR514 and via emitter follower TR515 from TR513. The gain introduced by TR509/TR511 is defined in the x10 magnification mode by the input resistance, R539, and the feedback resistance, R552, with the preset, R553. In this mode the transistor switch, TR512, is biased off. However, in the normal x1 magnification mode S507 is open and the current in R548 turns on TR512, introducing R544 with preset, R511, as additional feedback to reduce the gain of the amplifier accordingly.

The X shift control, R271, introduces an additional bias input via R541 and emitter follower TR506, through the potential divider R569/R545.

4.5. MODE CONTROL CIRCUITS

The display mode is controlled by S261 (Fig. 5) which defines the state of three control lines according to the following table.

Mode	L1	L2	L3	Q IC501b	$\overline{Q}$ IC501b
X-Y	+11V	0	+11V	L	H
CH1	0	+11V	0	H	L
Dual	+11V	+11V	0	Switching	
CH2	+11V	0	0	L	H
Add	0	0	0	H	H

These lines in turn control the function of the beam switch and other necessary signal switching.

Section 4.2 described the signal switching action of the beam switch diodes, D301 to D304 and D351 to D354. These are controlled by the Q and $\overline{Q}$ outputs of the beam switch bistable, IC501b. In the CH1 mode L1 is open, allowing R525 to take the set input of the bistable low, Q is high and $\overline{Q}$ is low, selecting the channel 1 signal for Y display. In the CH2 and X-Y modes, L1 is at +11V and R514 takes the set input high but L2 is open and R524 takes the reset input low to reverse the bistable and select the channel 2 signal.

In the Add mode, both L1 and L2 are open so that both set and reset are applied to the bistable, Q and $\overline{Q}$ are high and both channel signals are added into the shunt feedback stage of the Y amplifier (Fig. 4). In this mode only, L1, L2 and L3 are open, removing the bias through D401, D402 or D403 and defined by R401 and R402 via D405 and D406. This offsets the additional bias introduced by the selection of both channel signals.

Only in the X-Y mode, L3 is held at +11V to turn on the diode gate of D515 and D514, so coupling the channel 1 preamplifier signal of IC301, via TR506 and R547 into the X output amplifier. At the same time D504 conducts to turn off the gain switching transistor, TR512, thereby selecting x 10 X magnification irrespective of the position of S507.

D501 conducts allowing current through R509 to turn on TR261, clamping the ramp generator so that no signal is fed into the X amplifier via R539. Finally, current through R512 turns on TR504, holding the timebase bistable set "on" to provide continuous bright-bright-up of the trace.

In the Dual mode, both L1 and L2 are held at +11V so that the beam switch bistable, IC501, is free of set or reset signals. Thus it can respond to clock signals and as its D input is connected to its Q output its state reverses on each clock input.

On the fast sweep ranges (0.2ms/cm and above), the clock input is derived via emitter follower, TR505, directly from the Q output of the timebase bistable. Thus the beam switch operates in the alternate mode. The Y deflection is switched between channels at the

To aid component location, circuit references have been allocated in the following general pattern.

1	– 99	Components not mounted on printed circuit boards.
100	– 199	Components mounted on the attenuator assemblies.
200	– 299	Pre-amplifier and Ramp Generator components mounted on the daughter board.
300	– 399	Y Pre-amplifier and Beam Switch components mounted on the main board.
400	– 499	Y Amplifier and Y Output Amplifier components mounted on the main board.
500	– 599	Timebase and X Output Amplifier components mounted on the main board.
600	– 699	Trigger circuit components mounted on the main board.
700	– 799	Power supply and Modulation Circuit components on the main board.

4.1 GENERAL

Referring to the block diagram (Fig. 1) signals applied to the CH1 and CH2 input sockets pass into their respective attenuators and amplifiers. The VOLTS/CM switch controls the gain of the pre-amplifier in steps of 1.2.5 sequence to cover the ranges from 2mV/cm to 0.1V/cm and a ÷ 100 attenuator is introduced before the amplifier on the ranges 0.2V/cm to 10V/cm.

The Variable Gain control adjusts the amplifier gain to give 1 to 2.5 times reduction of gain on all settings of the Volts/cm switch. The fast electronic beam switch selects either the CH1 or the CH2 signal to be amplified further and passed to the Y deflection plates of the c.r.t.

A sample of each signal is taken and passed to the trigger switch bank where selection of CH1, CH2 or Ext trig source is made.

The selected signal is amplified and passed to the Schmitt trigger, the output of which clocks the timebase bistable "on". The ramp generator then begins to generate its linear ramp, which, after passing through the X amplifier, is applied to the X deflection plates of the c.r.t. and drives the electron beam linearly across the tube face. A portion of the signal from the ramp generator is fed back to the hold-off circuit, shutting the gate to prevent any further pulses from the Schmitt trigger from reaching the timebase bistable during the ramp period. When the ramp has reached the necessary maximum level, the timebase bistable is reset, and the ramp is quickly returned to its quiescent state. A time-constant in the hold-off circuit retains this signal to inhibit another ramp from being initiated for a short period, until the ramp timing capacitor is discharged fully. Thus a ramp is generated at a rate set by the TIME/CM switch when the trigger signal reaches a pre-determined level. This ramp sweeps the beam across the c.r.t. face, returns and waits for the next input cycle to reach the set trigger point, so producing subsequent ramps. The timebase bistable is connected to a blanking amplifier whose function is to turn on the electron beam during the sweep and blank it off during the fly-back and subsequent waiting period.

At fast sweep rates for a dual trace display, the TIME/CM switch automatically selects the alternate sweep mode of control for the beam switch. At the end of each sweep, the signal from the timebase reverses the state of the beam switch bistable, causing alternate displays of the CH1 and CH2 signal on successive sweeps of the timebase. At slow sweep rates, the chop mode is selected, when the chop multivibrator free runs independently, causing the beam to switch on chop between CH1 and CH2 levels during the sweep.

A signal from the multivibrator also blanks the trace during each switching transitition. With CH1 or CH2 only selected, the beam switch bistable is held to select that channel only. In the X-Y mode, the bistable is held to select CH2 as the Y deflection signal, while an additional switch diverts the output from the CH1 pre-amplifier, to the X output amplifier as the X deflection signal in place of the normal ramp signal. The blanking amplifier is held in the bright-up state. When TV trigger mode is selected, an additional synch. separator circuit is introduced into the signal path leading into the trigger amplifier.

4.2 THE Y AMPLIFIERS AND BEAM SWITCH

These circuits are shown in Fig. 4.

The attenuators and pre-amplifiers of channel 1 are identical to those of channel 2 and accordingly only channel 1 is described.

The input signal is applied to SKA and then to the attenuator via the 3 position slide switch, S101. This allows the input signal to be directly coupled through in the DC position or coupled via C105 in the AC position. In the central GND position, the input signal from SKA is left open circuited while the input to the attenuator is grounded.

On the most sensitive ranges, 2mV/cm to 100mV/cm, the VOLTS/CM switch, S102, couples the signal through directly to the pre-amplifier and the network resistor, RN101c, provides the input impedance. On the remaining ranges, S102 introduces R101a into the signal path to form a 100:1 attenuator with RN101b in parallel with RN101c.

High frequency compensation of the attenuator is provided by C101 and C104 while C102 with C106 allows the input capacitance of the attenuator to be set to equalise that of the unattenuated ranges.

Diodes, D201 and D202 with R207, provide input protection by limiting the input voltage appled to the amplifier to the voltages of zener diode, D203 and the positive supply line.

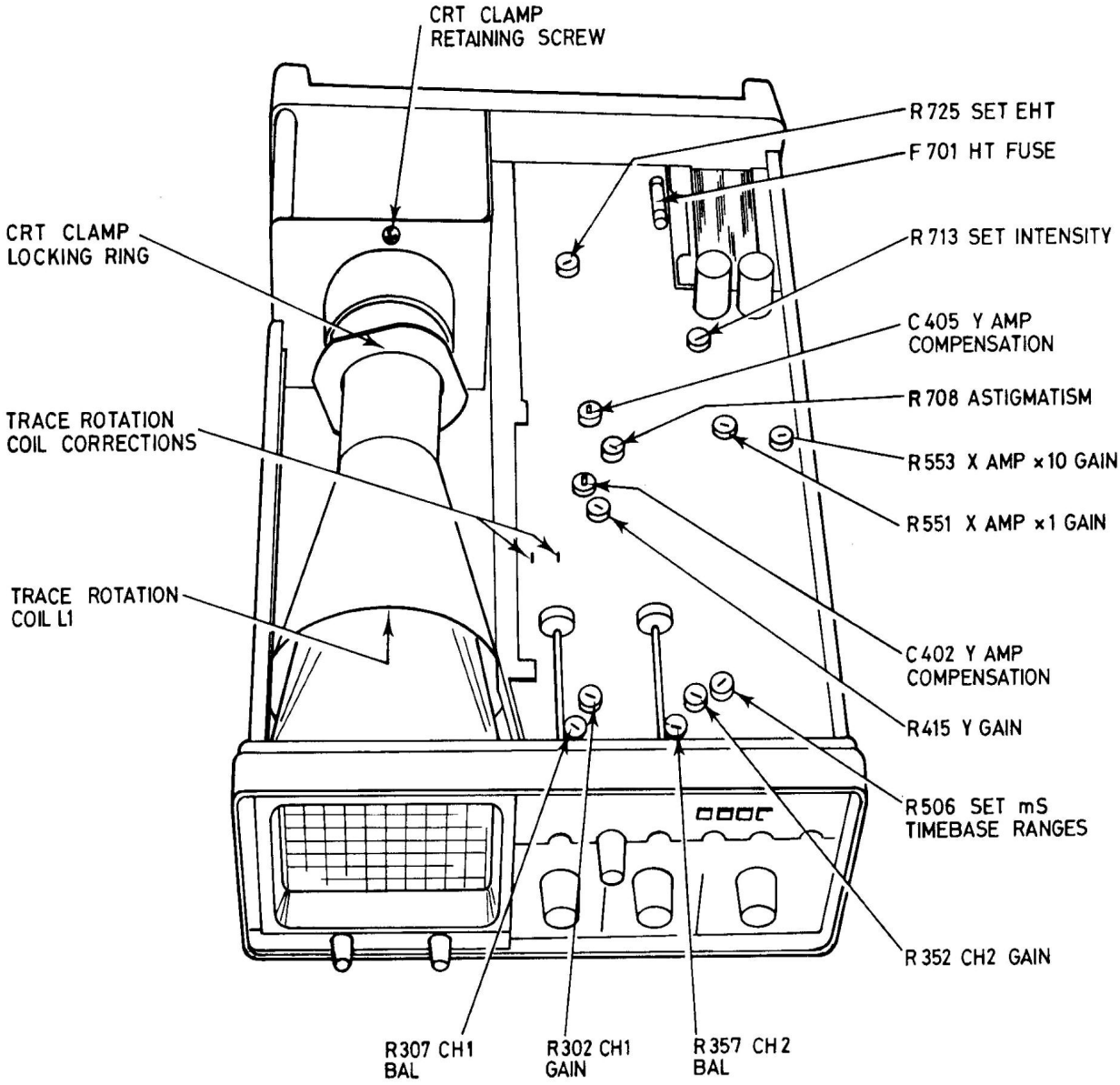

Fig. 2 Internal Assembly – top view

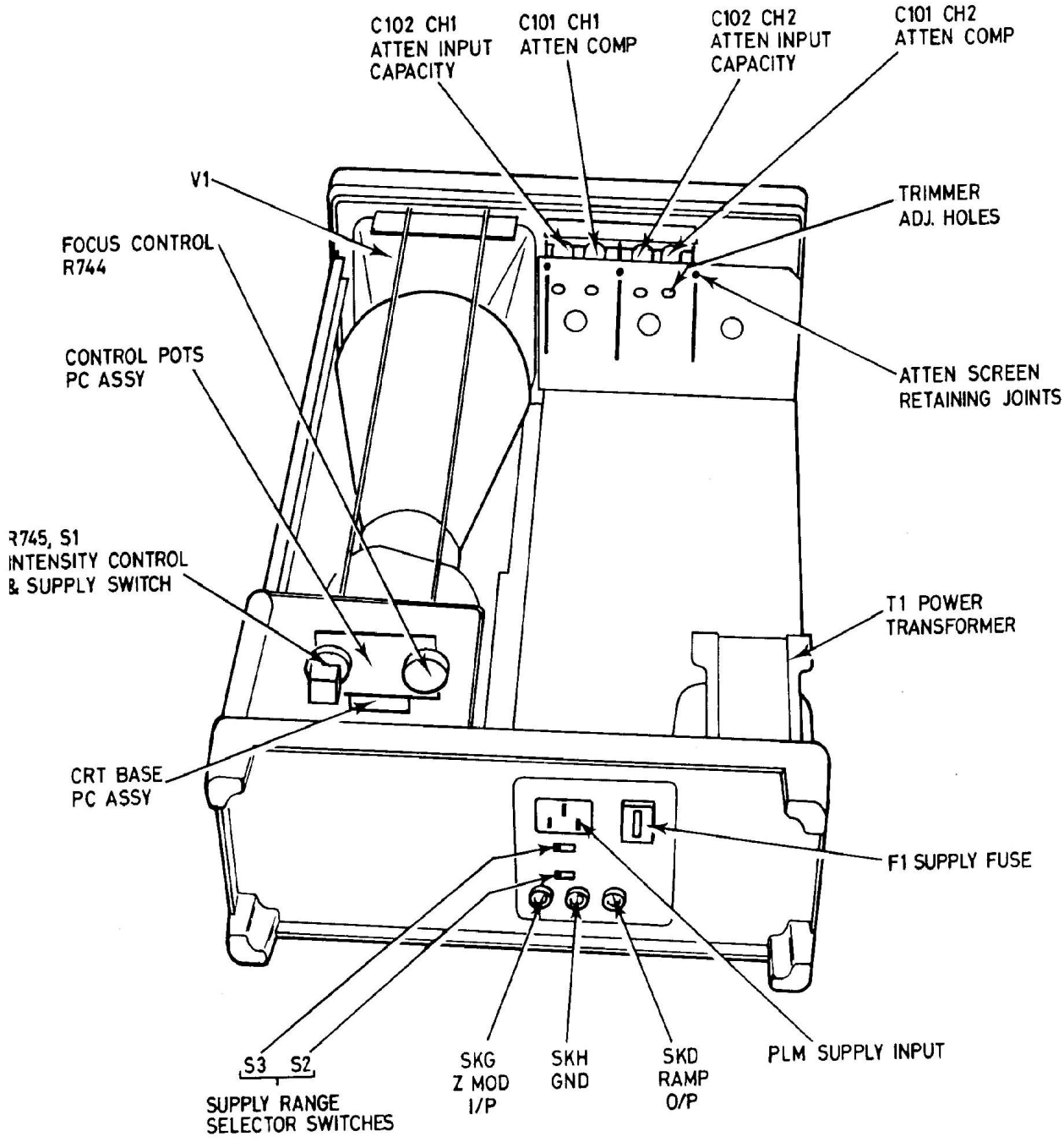

Fig. 3 Internal Assembly – bottom view

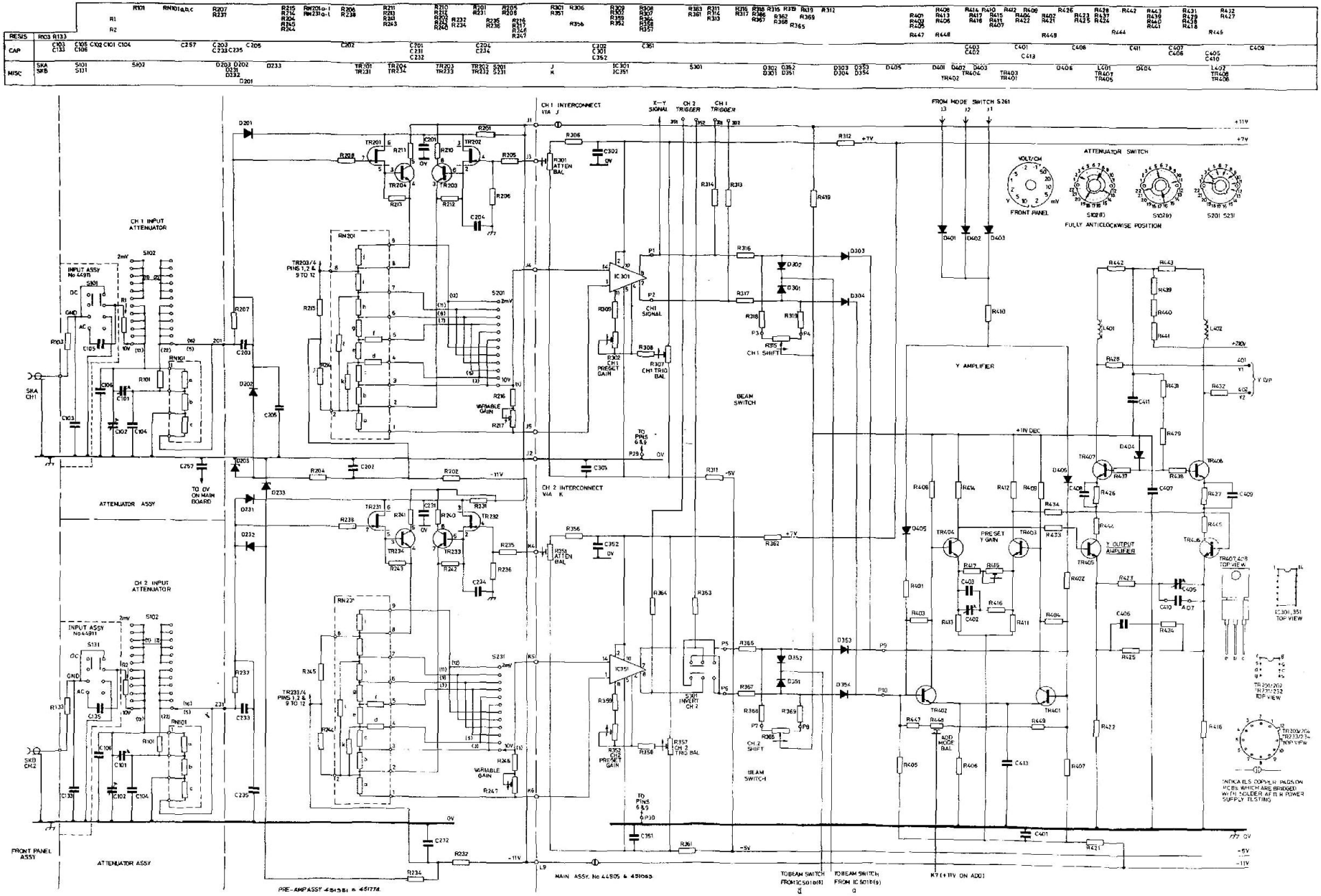

Fig. 4 Y Amplifier Circuit Diagram

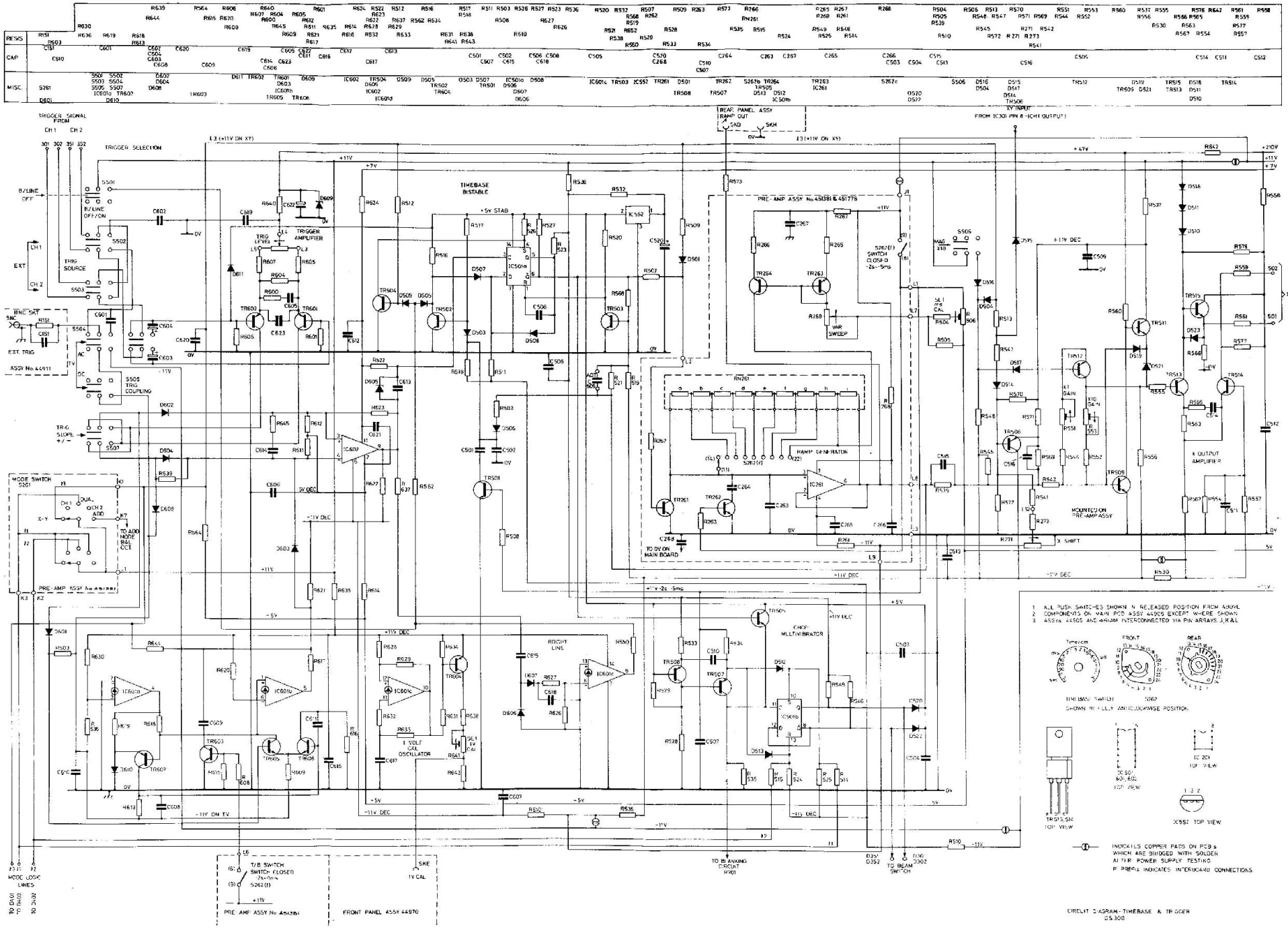

Fig. 5 Timebase and Trigger Circuit Diagram

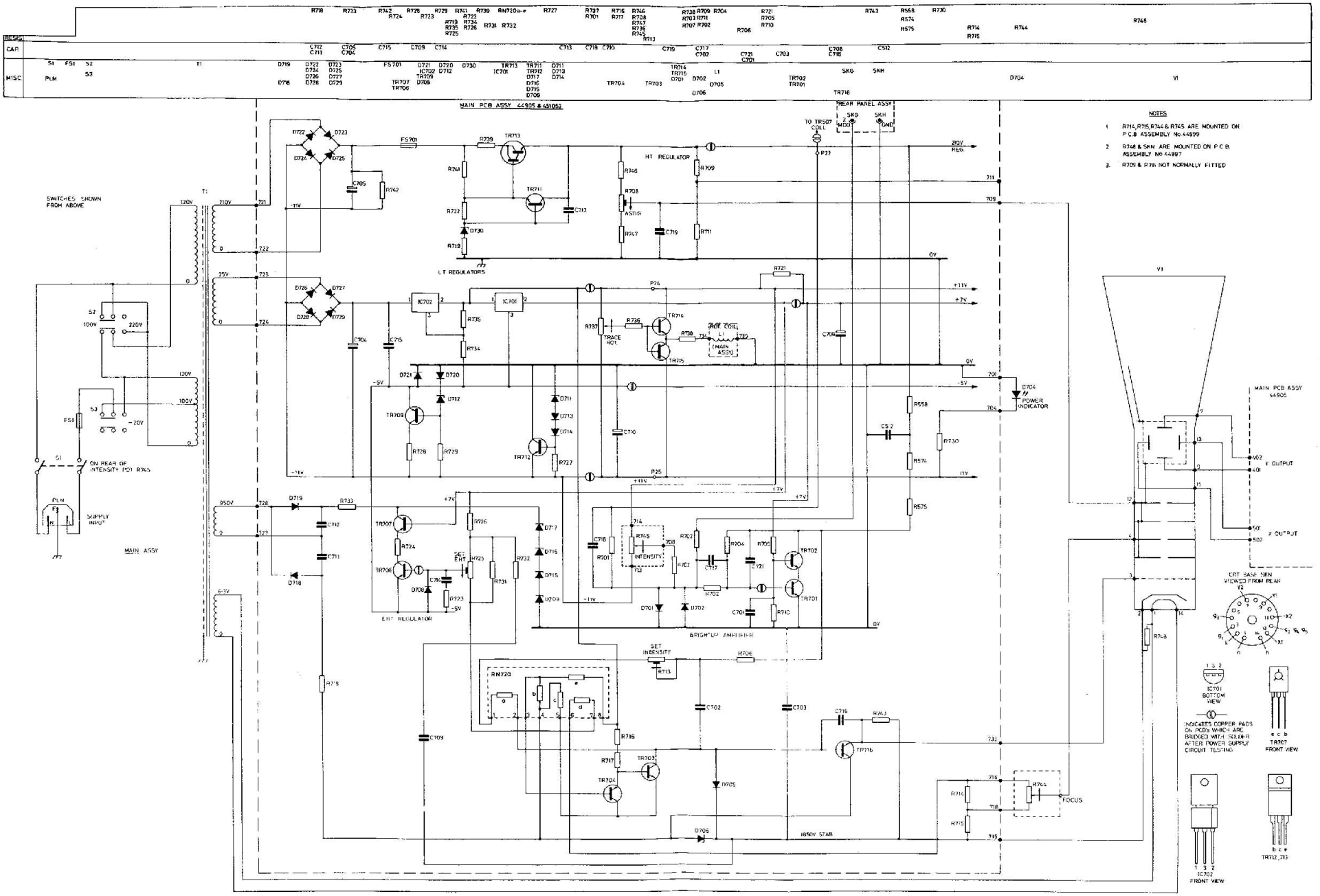

Fig. 6 Power Supply and C.R.T. Circuit Diagrams