

INSTRUCTION MANUAL

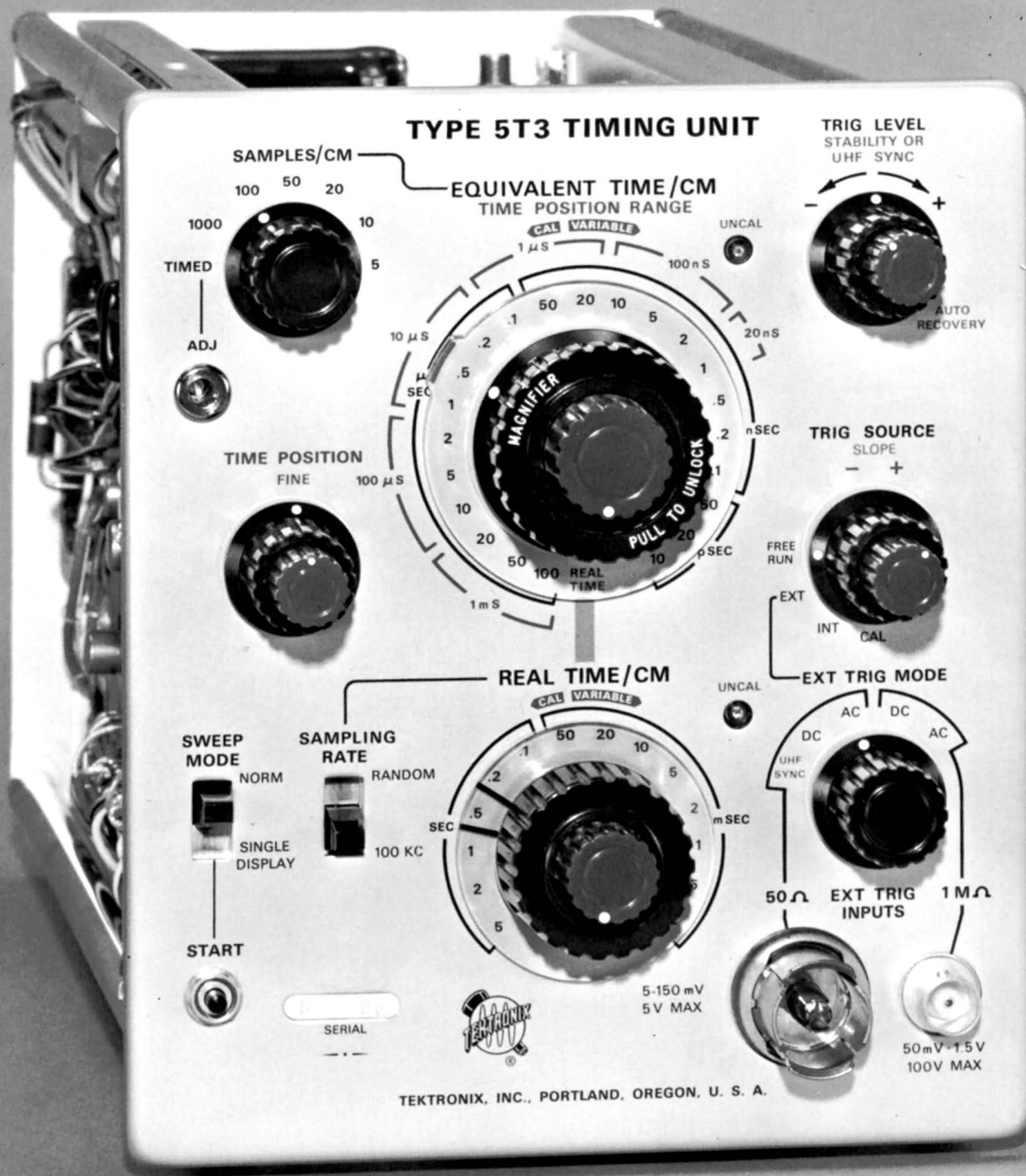
Serial Number 573

TYPE
5T3
TIMING UNIT

Tektronix, Inc.

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070-0470-00

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Type 5T3

SECTION 1

CHARACTERISTICS

General Description

The Type 5T3 Timing Unit is a wide-range time-base plug-in unit for use with the Type 661 Sampling Oscilloscope. Twenty-two calibrated equivalent-time sweep rates and fourteen calibrated real-time sweep rates provide accurate crt displays from 5 seconds per centimeter to 10 picoseconds per centimeter. The equivalent sweep rates faster than 1 nanosecond per centimeter are provided by a direct-reading magnifier. Variable sweep rate controls provide uncalibrated sweep rates between the calibrated steps and extend the fastest equivalent sweep rate to about 4 picoseconds per centimeter.

A Schmitt-type bistable trigger circuit provides triggering from dc to 500 megacycles from either internal or external sources. External triggering may be taken from either a 50 Ω source or a high-impedance source. A synchronizing circuit operated through the 50 Ω external trigger input extends the triggering capability of the Type 5T3 from 500 megacycles to above 5 gigacycles.

This wide range of sweep and triggering rates enables the sampling oscilloscope to display low-frequency signals, as well as repetitive high-frequency signals with risetimes in the picosecond range. In addition to repetitive-sweep displays, a triggered single sweep mode is provided for all sweep rates. In the equivalent-time range, a front-panel control positions the start of the crt "time window" for convenient viewing.

EQUIVALENT-TIME SWEEP

Sweep Rates

100 μ sec/cm to 1 nsec/cm, unmagnified, in 16 calibrated steps. Sequence is 1, 2, 5; accuracy within $\pm 3\%$ ¹. A direct-reading magnifier provides up to 100 \times magnification with no increase in dot spacing. Using the magnifier, the fastest calibrated sweep rate is 10 psec/cm. The magnified display is expanded from the left edge of the screen.

An uncalibrated variable control provides sweep rates between the calibrated steps, increasing the sweep speed up to at least 2.5 times from the calibrated position, and extends the fastest magnified rate to about 4 psec/cm.

Sweep Modes

Repetitive (NORM) or single-display, selected by front-panel switch. START button arms single display circuit. Next trigger starts the sweep.

Display Samples/Cm

5, 10, 20, 50, 100 and 1000 when the oscilloscope magnifier is at $\times 1$ position. With the SAMPLES/CM switch in

the TIMED position, sweep is continuous at a rate adjustable from 0.5 to greater than 5 sec/cm.

Display Time Positioning

1 msec to 20 nsec, depending on the sweep rate and magnification. TIME POSITION and FINE controls delay the start of the display time window over the range indicated on the blue Time Position Range scale. Total width of observable time is equal to the Time Position Range setting plus the time width of one screen diameter.

Blanking

Sweep retrace and interdot blanking internally dc-coupled to oscilloscope blanking circuit.

REAL-TIME SWEEP

Sweep Rates

5 sec/cm to 0.2 msec/cm in 14 calibrated steps. Function only with EQUIVALENT TIME/CM switch at REAL TIME position. Sequence is 1, 2, 5, 10; accuracy within $\pm 3\%$. An uncalibrated variable control provides sweep rates between the calibrated steps, increasing the sweep speed up to at least 2.5 times from the calibrated position, and extends the fastest real-time sweep rate to about 80 μ sec/cm.

Sweep Modes

Repetitive (NORM) or single display. START button arms single display circuit. Next trigger starts the sweep. The same controls are used for both equivalent-time mode and real-time mode.

Sampling Rates

100 KC—A precise clock rate set by an oscillator circuit. Frequency is adjusted to within 1% of 100 kc.

RANDOM—Approximate 80-kc rate frequency-modulated with 60 cps signal. Maximum period between samples is 15 μ sec; minimum period is 10 μ sec. Random rate is provided to break up false sampling displays.

Blanking

Sweep retrace and interdot blanking internally dc-coupled to oscilloscope blanking circuit.

TRIGGERING

Trigger Sources

Internal from sampling plug-in unit or oscilloscope calibrator, and external through 50 Ω or 1 M Ω External Trig-

¹ Excluding slight non-linearity at start of sweep with TIME POSITION and FINE controls fully clockwise.

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ger Inputs. All trigger sources are disconnected in the FREE RUN position of the TRIG SOURCE switch. When the sweep is in free run, the oscilloscope delayed pulse will present a stable display on the crt screen.

Trigger Slope

Positive-going (+) or negative-going (—) from all sources except 50 Ω UHF sync. The UHF synchronizer circuit operates on the positive-going portion of the input waveform in UHF Sync mode.

Trigger Coupling

Dc or ac from all sources except Calibrator and 50 Ω UHF sync. Ac only from these two sources. Internal signal source may be ac-coupled in the sampling unit.

Trigger Characteristics

Internal (from sampling unit with trigger takeoff)

Operating Range—Dc to approximately 500 Mc when dc-coupled.

Signal Requirements— ± 5 mv to ± 150 mv from sampling unit. Input to sampling unit must be large enough to provide this amount of trigger output to the Type 5T3 (e.g., the Type 4S1 must have a 40-mv input to provide 5-mv output).

Calibrator

Operating Range—100 kc to 100 Mc, internally connected to 100-mv oscilloscope calibrator signal.

External 50 Ω Input

Input Impedance—Nominally 50 ohms, regardless of input coupling.

Operating Ranges—Dc to 500 Mc at DC position; approximately 500 kc to 500 Mc at AC position; 500 Mc to 5 Gc at UHF SYNC.

Signal Requirements— ± 5 mv to ± 150 mv. Maximum short-duration overload is ± 5 volts.

External 1 M Ω Input

Input RC (approximate)—1 megohm paralleled by 30 pf.

Operating Range—Dc to 20 Mc at DC position; approximately 160 cps to 20 Mc at AC position.

Signal Requirements— ± 50 mv to ± 1.5 volts. Maximum short-duration overload is ± 100 volts.

Trigger Holdoff Duration

Minimum of 10 μ sec on equivalent Time Position Ranges of 20 nsec, 100 nsec and 1 μ sec; 4 times the Time Position Range switch setting on slower equivalent-time sweep rates.

Minimum of 10 μ sec on all real-time sweep rates.

Equivalent-Time Trigger Jitter

Bistable TD Trigger or Auto Recovery (with pulse input)

Less than or equal to 30 psec of jitter when triggered on a 50-mv pulse applied to the 50 Ω External Trigger Input or applied from the sampling unit to the Type 5T3¹. (Input pulse duration is 2 nsec, risetime is 1 nsec or less and repetition rate is 100 kc.)

Less than or equal to 300 psec of jitter when triggered with a 5-mv pulse of the same shape applied to the External Trigger Input or applied from the sampling unit to the Type 5T3.

Auto Recovery (with sine-wave input)

Less than or equal to 70 psec of jitter at 500 Mc when triggered with a 50-mv signal applied to the 50 Ω External Trigger Input or applied from the sampling unit to the Type 5T3.

Less than or equal to 300 psec of jitter at 500 Mc when triggered with a 5-mv signal applied to the 50 Ω External Trigger Input or applied from the sampling unit to the Type 5T3.

External UHF Sync

Less than or equal to 30 psec of jitter at 2 Gc with a 10-mv signal applied through the 50 Ω External Trigger Input, or 70 psec with a 5-mv signal applied (using the 20-nsec Time Position Range).

Less than or equal to 30 psec of jitter at 5 Gc with a 50-mv signal applied, or 70 psec with a 10-mv signal applied.

Equivalent-Time Display Jitter

Less than or equal to 30 psec on the 20-nsec Time Position Range; 40 psec on the 100 nsec Time Position Range, and 0.02% of the ramp duration on all other Time Position Ranges, when triggered internally with a 50-mv fast-rise signal applied from the sampling unit to the Type 5T3¹ (signal risetime less than 1 nsec).

Real-Time Display Jitter

Less than or equal to 1 μ sec when triggered internally on the 100-mv, 100-kc calibrator waveform.

Less than or equal to 10 μ sec when triggered through the 1 M Ω External Trigger Input from a 200-mv, 1-kc square-wave signal.

MECHANICAL CHARACTERISTICS

Construction

Aluminum-alloy chassis frame and anodized front panel. Epoxy laminate etched-wiring boards.

¹ See Internal Trigger Characteristics.

Dimensions

Height—7 inches; width— $5\frac{7}{8}$ inches; depth— $14\frac{1}{2}$ inches.

Weight

Approximately 7 pounds.

STANDARD ACCESSORIES

- 2 — $50\ \Omega$ $10\times$ T-attenuators with GR connectors (017-0044-00)
- 1 — 10-nsec $50\ \Omega$ coaxial cable with GR connectors (017-0501-00)
- 1 — 18-inch cable with BNC plug on one end and banana plug on other end (012-0090-00)
- 2 — Instruction Manuals (070-0470-00)

SECTION 3

CIRCUIT DESCRIPTION

The Type 5T3 Timing Unit is designed to operate as part of the Tektronix Type 661 Sampling Oscilloscope system. This section of the manual presents a brief description of the basic sampling processes in equivalent-time mode and in real-time mode, then gives more detailed descriptions of the various circuits.

BASIC SAMPLING PROCESSES

Sampling oscilloscopes are designed primarily to be used for viewing high-frequency or fast-rise repetitive waveforms. Most modern sampling systems accomplish this by taking samples from many different cycles of the input signal, then reconstructing the waveform in "equivalent time" on the crt screen.

In addition to equivalent-time sampling, the Type 5T3 incorporates a real-time sampling mode that permits viewing of low-frequency and non-repetitive signals at sweep rates below the practical lower limit of equivalent-time sampling.

Equivalent-Time Mode

The equivalent-time portions of the sampling system are shown in the simplified block diagram in Fig. 3-1. The ver-

tical channel uses an input gate that can take quick samples of the input signal and a memory circuit that remembers the previous sample level until another sample is taken. The horizontal sweep is produced by a staircase voltage that advances one step each time a new sample is to be displayed. In triggered operation, one excursion of the input triggering signal actuates the trigger circuit, which then initiates one cycle of the sampling process to produce one dot of the crt display. Each displayed sample requires a separate triggering event.

The trigger circuit starts the operation of the fast ramp and arms the sweep to start. When the fast ramp run-down voltage becomes equal to the existing staircase feedback voltage, the comparator triggers the regenerator circuit. In turn, the regenerator pulses the sampling circuit and the staircase generator. The sampling circuit then takes a quick sample of the signal level at the input, while the staircase generator advances one step. The sampling memory output is applied to the vertical amplifier and the new staircase output level is applied to the horizontal amplifier. As soon as the sample is taken, a dot is displayed on the crt screen at a level proportional to the input signal level at the moment it was sampled. The dot then remains stationary on the screen until a new sample is taken.

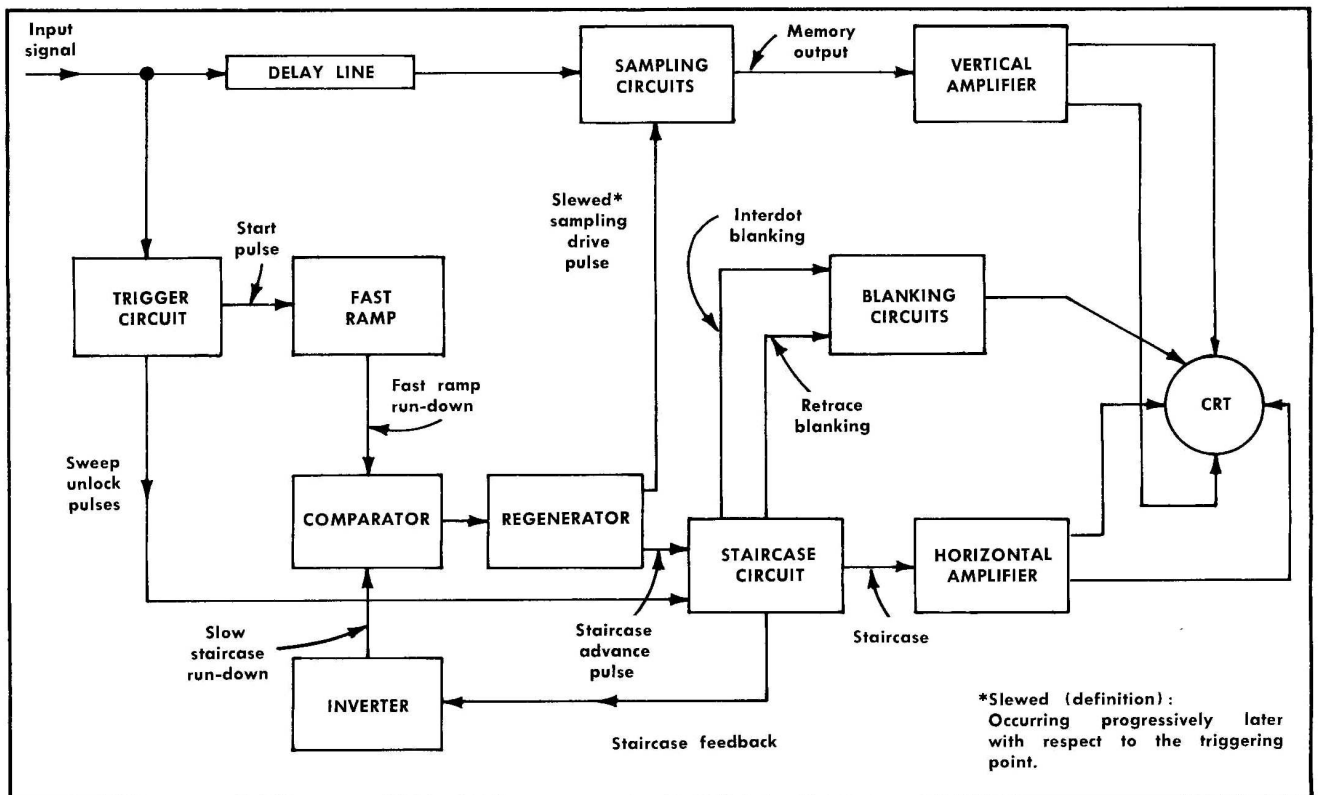


Fig. 3-1. Simplified block diagram of Sampling System with Type 5T3 in equivalent-time mode.

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Each subsequent triggering event initiates the same series of sampling events, but since the staircase feedback voltage moves down one step each time, the fast ramp has to run down slightly farther each time before a comparison pulse is produced. In this way, the sampling event is delayed by successively longer intervals and the samples are taken successively later along the waveform with respect to the triggering point. Each time a sample is taken, the crt is blanked momentarily while the dot position on the crt screen moves horizontally by one increment, and to a new vertical level. Since the sampling channel is an error-sensing circuit, the vertical position of the dot will change only if the input voltage level changes between samples.

Fig. 3-2 illustrates the development of an equivalent-time display from a repetitive square-wave signal. Note that the sampling operation is triggered each time at the same point on the triggering waveform, but that the sample is taken progressively later on the waveform, due to the longer delay between the triggering event and the sampling event. In an equivalent-time display, no two samples are taken on the same cycle of the input waveform; though, if the waveform is of a very high frequency, several cycles may occur between samples, due to the inherent recovery time of the trigger circuit.

Real-Time Mode

Fig. 3-3 is a simplified block diagram showing the system components that function in real-time mode. The sampling operation performed by the sampling unit is identical to that performed in equivalent time, and some of the sweep and triggering functions remain the same. In real-time mode, however, the sampling process and the staircase advance are not initiated by the trigger circuit, but rather by a real-time clock circuit.

In real-time mode, since the waveforms to be viewed are relatively slow moving, samples are taken at a rapid

rate continuously along the waveform, rather than from different cycles of the signal. The crt display is thus made up of a series of dots that actually follows the changes of the input waveform. Only one trigger is required per sweep (as in a conventional non-sampling oscilloscope), rather than one trigger per samples (as in equivalent-time mode).

The real-time clock circuit operates whenever the instrument is set for real-time operation. Each cycle of the clock sends a gate pulse to the staircase generator and a sampling drive pulse through the regenerator to the sampling channel. The dots on the crt screen are produced at a constant rate and the crt display progresses at the selected real-time sweep rate. Thus the sweep rate and the sampling rate determine the dot spacing on the crt screen. For example, a sweep rate of 1 sec/cm and a sampling rate of 100 kc produces a display of 100,000 dots per sweep.

CIRCUIT ANALYSIS

During the following analysis of the various circuits of the Type 5T3, refer to the block diagrams in the text for the general operation of each circuit, and refer to the particular schematic diagram at the rear of this manual for the detailed analysis.

Tunnel Diodes

Since several circuits in the instrument use tunnel diodes as switching devices, the basic operating characteristics of these components are described in general here, rather than in the description of each circuit.

These diodes are specially manufactured to have voltage-current characteristics similar to the 10-ma curve shown in Fig. 3-4. As current through the diode is increased from

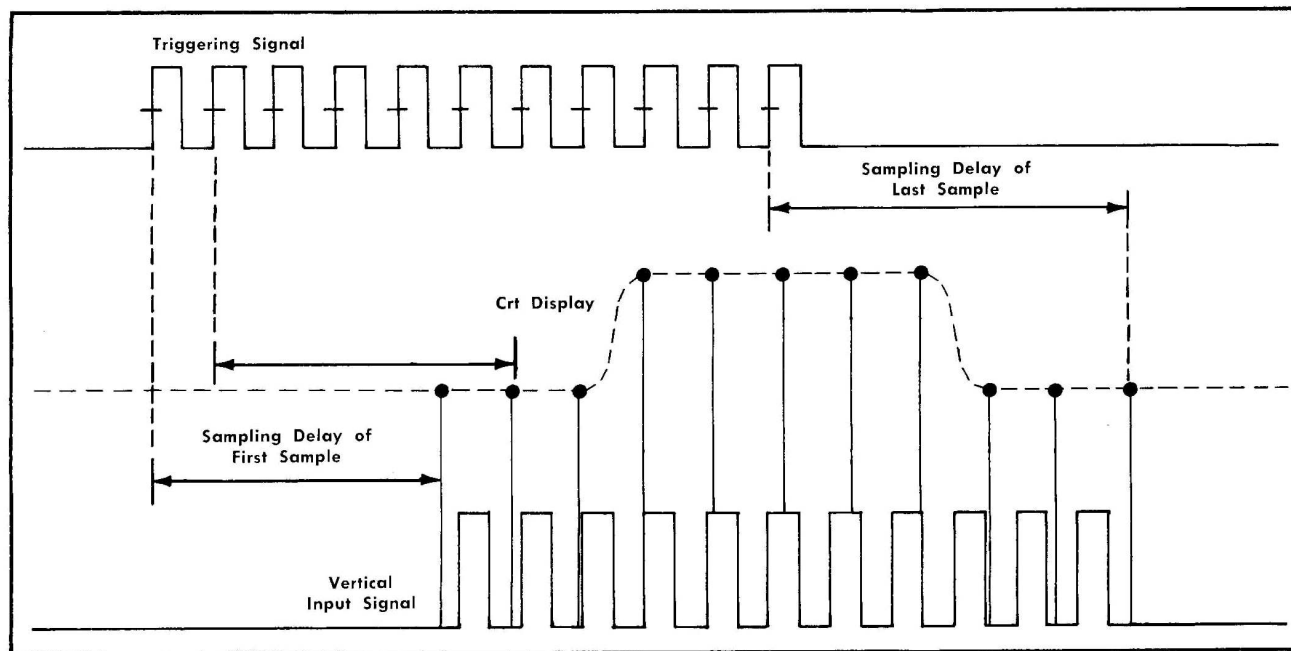


Fig. 3-2. Formation of crt display in equivalent-time mode.

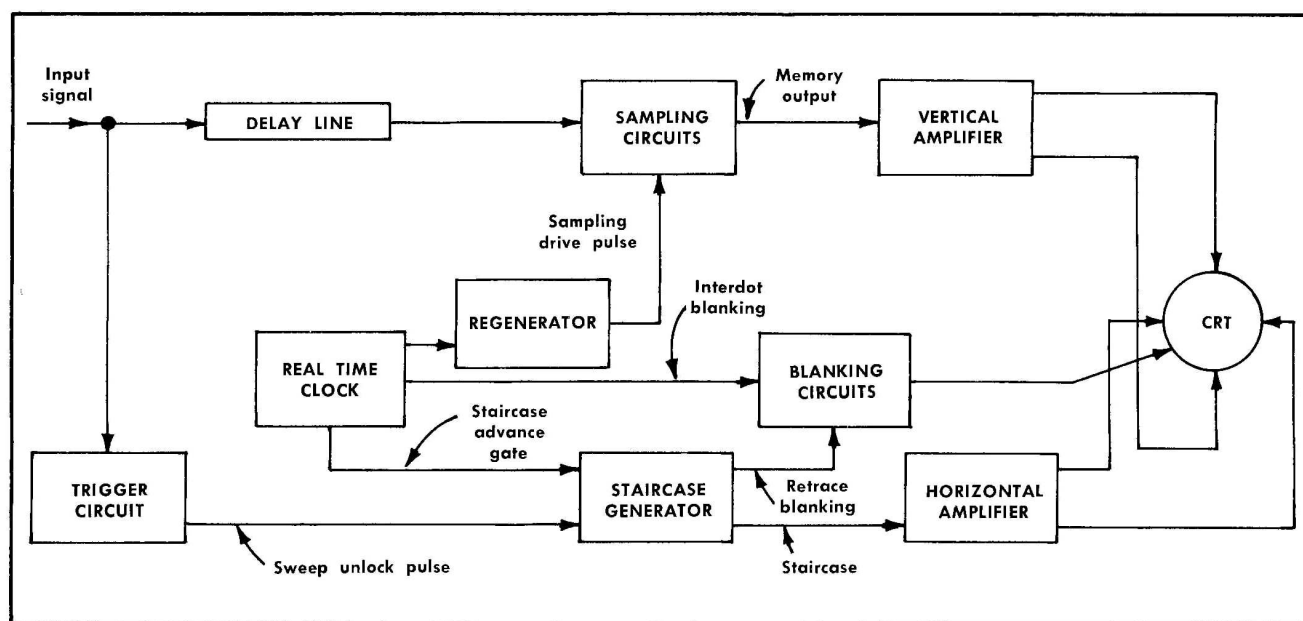


Fig. 3-3. Simplified block diagram of Sampling System with Type 5T3 in real-time mode.

zero to the 10-ma point, the voltage across it increases slowly to about 75-100 millivolts. This is called the low-voltage state of the diode. Any further increase in current then causes an abrupt voltage increase to about 500 millivolts. The diode is then in its high-voltage state. The fast voltage pulse that occurs as the diode switches to its high-voltage state is the pulse that is used as a trigger. Once the diode has switched to its high-voltage state, current through it must be decreased to about 2 ma to make it switch back to the low-voltage state. When it is switched back to the low-voltage state, the transition is also very fast and the resulting voltage pulse may also be used as a trigger or reset pulse.

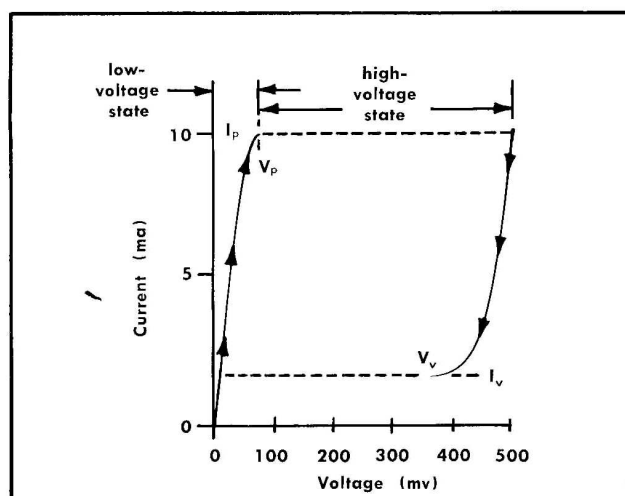


Fig. 3-4. Typical switching characteristics of a 10-ma tunnel diode.

External Trigger Circuit

The external trigger circuit consists of the two external trigger inputs (50 Ω and 1 M Ω), an isolation cathode-follower for the 1 M Ω input and a wide-band external trigger amplifier. Triggering signals that are applied in UHF Sync mode of operation are connected directly to the trigger circuit. All other triggering signals applied to the external trigger inputs are processed by the external trigger amplifier circuit.

50 Ω INPUT

The 50 Ω input circuit presents a constant impedance of 50 ohms at the input connector, regardless of the internal coupling used. The 50 Ω AC or DC positions of the EXT TRIG MODE switch permit triggering from external 50-ohm sources up to a frequency of 500 Mc. The lower frequency limit of the AC position is about 500 kc. In addition to these, a 50 Ω UHF SYNC position of the switch connects the input directly to a monostable tunnel diode in the trigger circuit for synchronizing on input signals up to 5 Gc. In this mode, no trigger isolation amplifiers are used, allowing a great increase in bandwidth but also allowing a considerable amount of external kickout from the tunnel diode.

In the UHF Sync mode, the input is terminated by R187, R183 and R184. In the 50 Ω AC and DC positions, R49 and R57 provide the termination. When the EXT TRIG MODE switch is set to either of the 1 M Ω positions, R53 terminates the 50 Ω input.

1 M Ω INPUT

A high-impedance input circuit is provided at the 1 M Ω AC or DC positions of the EXT TRIG MODE switch for use with low- and intermediate-frequency external triggering signals (up to 20 Mc). Input impedance remains a constant

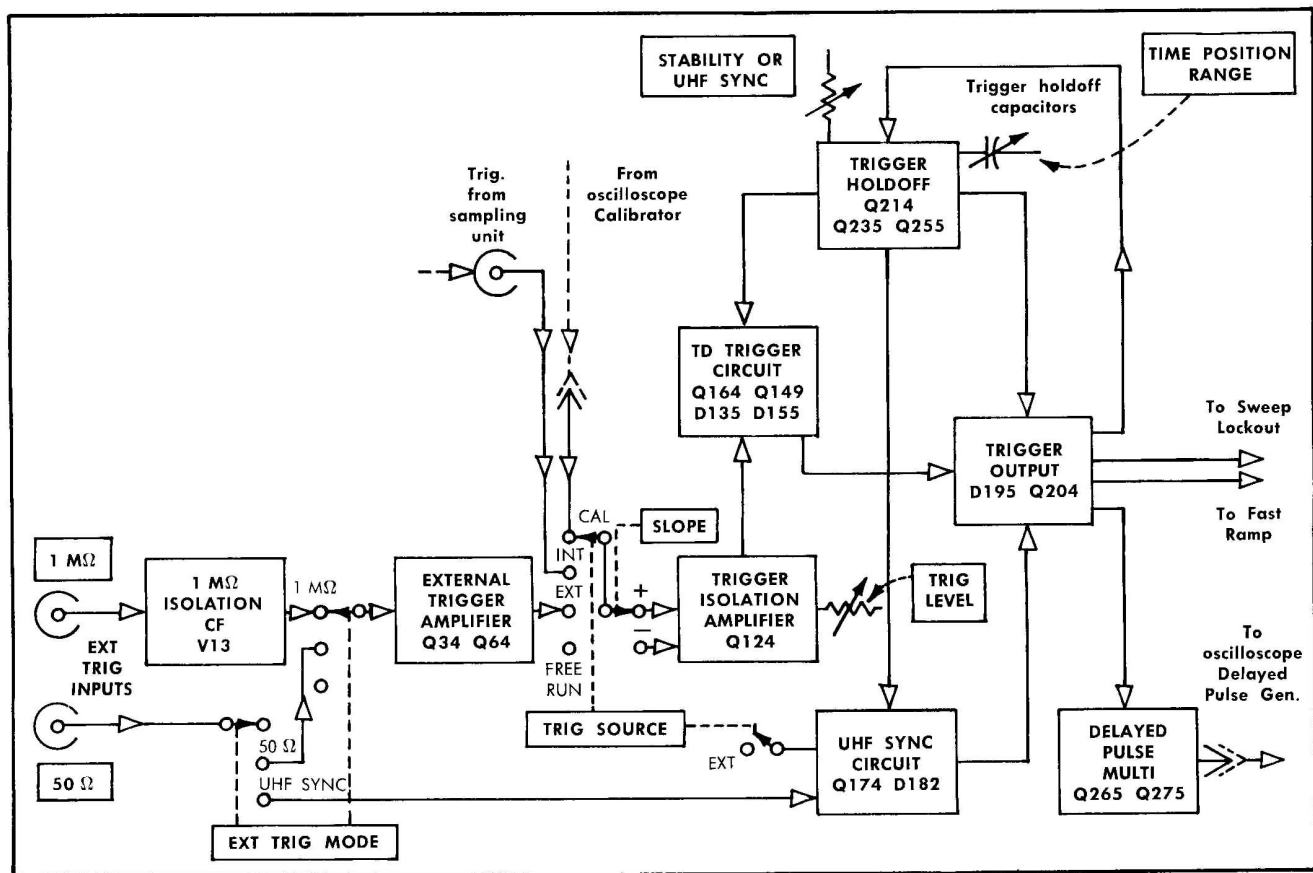


Fig. 3-5. Block diagram of External Trigger Input and Trigger circuits.

1 megohm, set by R5 in the grid circuit of V13. When set to the 1 MΩ AC position, the lower-frequency limit is approximately 160 cps.

1 MΩ ISOLATION CF

In addition to isolating the 1 MΩ input from the trigger circuits, the circuit of cathode-follower V13 also provides an impedance transformation from 1 megohm at the input to about 1 kilohm at its output to the external trigger amplifier. Further impedance transformation is provided by the amplifier circuit.

Input signals of from 50 millivolts to 1½ volts are applied through the 1 MΩ input to the grid of V13. Excessively large signals are clipped by diodes D5 and D7. Gain through the cathode follower is slightly less than one. When the EXT TRIG MODE switch is set to one of the 1 MΩ positions, a 10× attenuator is formed by R15 and R20, providing most of the impedance transformation to 1 kilohm. The 1 MΩ ZERO adjustment (R10) is set so that when there is no signal applied to the 1 MΩ input, the output of the external trigger amplifier to the trigger circuit is zero volts.

EXTERNAL TRIGGER AMPLIFIER

The transistor pair, Q34 and Q64, constitute a wide-band inverter amplifier for the external trigger input circuits. Basic frequency response of the circuit is from dc to 500 Mc with a gain of one.

There are two input paths to the amplifier, one at the base of Q34 and the other at the emitter of Q64. Transistor Q64 is used as a common-base amplifier for high-frequency signals and as a degenerative common-emitter amplifier for low frequencies. Transistor Q34 is used as a simple emitter follower.

When the EXT TRIG MODE switch is set to one of the 1 MΩ positions, the signal is applied from V13 to the base of Q34. The primary of transformer T55 is shorted and the emitter of Q64 is, in effect, terminated in 50 ohms. In this case, only the low-frequency common emitter character of Q64 is used. Thus with a collector load of 50 ohms and an emitter resistance of 50 ohms, a voltage inversion is obtained with a gain of one through the amplifier.

When the EXT TRIG MODE switch is set to one of the 50 Ω positions, V13 is no longer connected to the amplifier. In the 50 Ω DC position, a signal applied to the 50 Ω EXT TRIG INPUT connector passes through the EXT TRIG MODE switch to T55. The high-frequency components of the signal are inverted in the transformer and connected through a coax directly to the emitter of Q64. The low-frequency portion of the signal passes through the primary of T55 to the base of Q34. Fifty-ohm signals applied to the 50 Ω EXT TRIG INPUT connector are thus amplified by a factor of one through one or the other of the two paths. Crossover frequency from low-frequency to high-frequency operation occurs at about 3 Mc.

In the 50 Ω AC position of the EXT TRIG MODE switch, the dc connection to the base of Q34 is disconnected and C45 is tied to ground in parallel with C49. In this position, only the high-frequency information coupled through T55 is applied to Q64, and the low-frequency cutoff is about 500 kc.

TRIGGER SOURCE AND SLOPE SWITCHES

The TRIG SOURCE switch (SW80) is designed to provide a 50-ohm termination for each input triggering signal not connected to the trigger circuit. The three inputs provided to the switch are the oscilloscope calibrator (CAL), internal (INT) from the sampling unit and external (EXT) from the external trigger amplifier or UHF Sync circuit.

The internal connection from the sampling unit is dc-coupled in the Type 5T3, but may be ac-coupled in the sampling unit. In the CAL position of the TRIG SOURCE switch, a 100-mv signal from the oscilloscope calibrator is connected to the trigger circuit. The amplitude of this calibrator signal remains the same, regardless of the amplitude at the calibrator output. The signal is applied through T90 and is ac-coupled only.

The SLOPE switch (SW95) applies input triggering signals to the base and emitter of the trigger isolation amplifier, Q124. In addition, it permits polarity reversal of the voltages connected to the TRIG LEVEL control (shown on the Trigger schematic diagram). In the positive position of the SLOPE switch, signals are applied directly to the emitter of Q124 with no inversion. In this mode, the base of Q124 is held at ground by R99. In the negative polarity (—), however, Q124 is connected to operate as an inverter amplifier. The dc-coupled signal is applied to the base of the transistor and an inverted signal is ac-coupled to the emitter through transformer T97. At high frequencies the dc-coupled signal is shorted to ground through C99 and the primary signal path is through T97. At lower frequencies, the ac-coupling of T97 becomes less effective, while the dc-coupling to the base of Q124 becomes more effective.

Trigger Circuit

The trigger circuit is composed of several smaller circuits—a trigger isolation amplifier, a bistable tunnel-diode trigger circuit, a trigger output tunnel-diode circuit, a monostable tunnel-diode UHF Sync circuit, a trigger holdoff multivibrator, a delayed pulse multivibrator and several switching transistors. Output signals from the trigger circuit are provided for starting the fast ramp circuitry and the staircase generator and for pulsing the delayed pulse generator in the oscilloscope.

When the triggering controls are set for triggered operation, a triggering signal applied to the input isolation amplifier causes the bistable TD circuit to initiate the operation of the rest of the trigger circuit. The bistable TD circuit delivers a pulse to the output tunnel diode which then starts the fast ramp. In addition, the output tunnel diode turns on the transistor in the trigger output circuit, starting the operation of the trigger holdoff and sending an unlock pulse to the sweep gate in the horizontal sweep generator. The trigger holdoff prevents the trigger circuit from operating again until after the holdoff period by cutting off bias current from the bistable TD circuit. At the

end of the holdoff period, current is restored to this circuit making it sensitive to the input triggering signal.

If the UHF Sync mode is used, the UHF Sync tunnel diode synchronizes on the input signal then triggers the output tunnel diode to initiate the output pulses. The hold-off circuit also controls the bias current for the UHF Sync circuit.

TRIGGER ISOLATION AMPLIFIER

When the SLOPE switch is set to +, the trigger isolation amplifier (Q124) operates as a common-base amplifier. Positive-going signals applied to the emitter decrease current through the transistor, decreasing current through the recognition tunnel diode (D135) in the TD trigger circuit. When the SLOPE switch is set to —, the triggering signal is applied to the base of Q124 and the inverted signal is applied to the emitter. The negative-going portion of the triggering signal then decreases current through D135 to arm the trigger circuit.

The TRIG LEVEL control in the emitter circuit of Q124 sets the dc current through the transistor. This determines the input signal level that will cause the trigger circuit to operate. The TRIG LEVEL ZERO adjustment (R120) is set to center the range of the TRIG LEVEL control, and the TRIG BAL control (R103) adjusts the emitter voltage level to zero with no signal applied.

BISTABLE TD TRIGGER AND TRIGGER OUTPUT

Since the bistable tunnel-diode trigger circuit and the trigger output circuit operate so closely as a unit, they will be discussed together here. The bistable tunnel-diode circuit is formed by D135, D155 and Q149. Transistor Q164 is a current switch for this circuit. Output tunnel diode D195 and transistor Q204 form the trigger output circuit. The current source for both circuits is the 19-volt switch (Q214) operated by the holdoff circuit.

All of the current that passes through D135 and D155 also flows through Q164. Since diodes D135 and D155 are connected to a common current source, an increase in current through D135 (caused by a current increase in Q124) is accompanied by a decrease in current through D155. Similarly, a current decrease in D135 is accompanied by a current increase in D155. The STABILITY OR UHF SYNC control (R170) adjusts current through Q164 to set the bias on D135 and D155 for triggered, synchronizing or free-running operation.

In the quiescent state, output tunnel diode D195 is biased near the triggering point by current through R210 (OUTPUT TD BIAS), and output transistor Q204 is not conducting.

Schmitt-Type Triggering. The bistable TD trigger circuit is reset at the completion of each holdoff cycle and if it is set for triggered operation, the circuit is ready to accept another triggering event. At this time, recognition tunnel diode D135 and recovery tunnel diode D155 are both biased in their low-voltage states, with D155 near its switching point and D135 well below its switching point. Transistor Q149, which is connected in shunt with D135, has a saturation characteristic such that its emitter-to-collector impedance is very high when the emitter-to-collector voltage is below 100 mv, and very low when the voltage is greater

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than 100 mv. The base-to-emitter junction is normally forward biased with a quiescent current of approximately 0.5 ma, so that whenever the emitter-to-collector voltage exceeds 100 mv, the transistor will saturate. With D135 in its low state, however, the voltage applied across Q149 is below the 100-mv saturation voltage and the transistor is held out of conduction.

Heater current for V13 and V583 (Horiz. Sweep Generator) flowing through the low-impedance path of D157, R152, R149-R150 and R155 holds the cathode of D155 near +6.2 volts and produces a drop of approximately 250 mv across R149-R150, setting the anode voltage of D147. With both D135 and D155 in the low-voltage state, the anode of D146 is at a less positive voltage than the anode of D147; therefore D146 is reverse biased and D147 is conducting all of the current that passes through R146.

If the input triggering signal causes current to increase through isolation amplifier Q124 (and thus through D135), no switching will occur because the current increase will not raise the bias on D135 above its switching point. When the input voltage excursion causes a current decrease through D135, the resulting current increase through D155 switches D155 to its high-voltage state. The positive-going voltage pulse that appears at the anode of D155 is applied directly to the anode of D135 and through the network of C140, R144 and LR133 to the anode of D135. This raises the level of both the anode and cathode of the tunnel diode, forward biasing D146 and switching current from D147 to D146 and D135. The increased current through D135 biases this diode up near its switching point, but since current is decreasing through Q124, D135 will not switch at this time. The next excursion of the input signal that increases the current through Q124 and D135 (corresponding to a positive-going excursion with the SLOPE switch set to +) causes D135 to switch to its high-voltage state. The resulting negative-going pulse at its cathode is inverted by T135 and applied through C190 and R195 to the anode of D195, the trigger output tunnel diode.

When recognition tunnel diode D135 switches to its high-voltage state, it also applies several hundred millivolts across Q149 and LR133. Initially most of this voltage appears across LR133, but as the field in the inductor begins to break down, more of the voltage appears across Q149. As this transistor saturates, it shorts out D135, automatically resetting the tunnel diode to its low-voltage state.

The positive-going pulse from the bistable TD trigger circuit switches D195 to its high-voltage state. As D195 switches, the positive-going pulse at its anode is sent to the fast ramp circuit and also is applied to the base of Q204, causing the transistor to conduct. As Q204 turns on, it sends a negative gate pulse to the sweep gate circuit and also reverse biases D227 to start the operation of the trigger holdoff circuit. As Q204 becomes saturated, it diverts enough current from Q164 to turn off that transistor. Thus, with the main current source removed from the bistable TD circuit, D135 is held in its low-voltage state, D155 is reset to its low state and D146 is turned off, restoring current through D147.

The holdoff multivibrator turns off Q214 at the halfway point of the holdoff period, causing D195 to reset to its low-voltage state and turn off Q204. Transistor Q164 does not turn on again though, since the current source through

Q214 has been cut off. At the end of the holdoff period when Q214 is turned on again, current is reestablished through Q164 and the bistable TD trigger circuit can again be armed and triggered by the input triggering signal.

Auto Recovery Mode. When the STABILITY OR UHF SYNC control (R170) is switched to the AUTO RECOVERY detent position, C207 is connected to ground, delaying the rearming of D195. With R170 set to this position, current through Q164 sets the bias on D155 slightly above its switching level, so that at the end of each holdoff period, D155 is switched immediately and arms D135 without waiting for a negative excursion of the input signal. If the TRIG LEVEL is set so that D135 is then switched to its high-voltage state, D135 and Q149 will operate as a free-running multivibrator for a few cycles until D195 reaches its triggerable bias level. The repetition rate of this free-running circuit is adjusted by controlling current through D135 with the TRIG LEVEL control. The circuit can thus be adjusted to synchronize on a high-frequency input signal (10-500 Mc) and send a series of small fast triggers to D195.

As the bias on D195 reaches the triggerable level, the first of the small triggers that is able to raise the diode above the switching level switches it to its high-voltage state to produce an output pulse. The normal holdoff interval follows the output pulse, then D155 is reset and D135 and D149 again synchronize on the input triggering signal.

In auto recovery mode, if the TRIG LEVEL is set for triggered operation rather than free run, D135 is rearmed at the end of the holdoff period and is then repeatedly triggered by negative-going excursions of the input signal until one of the triggers is able to switch D195.

Whether free running or triggered, the auto recovery mode operates best on short fast pulses and high-frequency sine waves, but not very well on long pulses or square waves.

Free Run Mode. For triggered operation, R210 (OUTPUT TD BIAS) sets the bias current through D195. However, when the TRIG SOURCE switch is set to FREE RUN position, in addition to disconnecting all triggering sources, the TRIG SOURCE switch also shorts across R210. The resulting increase in bias current causes D195 to be retriggered as soon as the holdoff period has ended, without waiting for a signal from the bistable TD circuit.

UHF SYNC TD CIRCUIT

Diode D182 is the UHF Sync tunnel diode oscillator circuit, capable of synchronizing on input signals from 500 Mc to more than 5 Gc. The tunnel diode receives bias current from the stability control circuit when Q174 is turned on at the end of the holdoff period with the TRIG SOURCE set to EXT. Diode D182, L178 and R179 constitute a free-running oscillator circuit whose frequency is controlled by the adjustable bias current through the STABILITY OR UHF SYNC control. Maximum repetition rate of the circuit is about 50 Mc. The frequency of the oscillator can be adjusted so it will synchronize with a very high-frequency signal applied from the 50 Ω EXT TRIG INPUT through R183, R184 and the capacitance built into the etched-wiring board. In this mode, the OUTPUT TD BIAS control is shorted out, as in FREE RUN mode, and C207 is connected to ground, as in AUTO RECOVERY mode, to retard the recovery of D195. Under these conditions, the series of small fast triggers ap-

plied to the output tunnel diode (D195) causes the diode to switch as soon as one of the small triggers raises the diode above the triggering level following holdoff.

As soon as D195 switches and starts the operation of the holdoff circuit, Q174 is turned off and is held off until after the holdoff period has again ended.

TRIGGER HOLDOFF MULTIVIBRATOR

While Q204 is turned off, prior to receiving a trigger from D195, both transistors in the trigger holdoff circuit (Q235 and Q255) are turned on, holding Q214 in saturation. D227 is conducting current through the path from -100 volts to $+19$ volts. Diodes D228 and D233 are reverse biased, so the voltage on the holdoff capacitors connected to the junction between the diodes is held at about $+12$ volts by current through R230 and R233.

When a trigger is received and D195 turns Q204 on, D227 is reverse biased and the current from the -100 -volt supply turns on D228 and flows into the holdoff capacitors (C230 and capacitors C660, C662 and C664 on the TIME POSITION RANGE switch). The capacitors begin a rundown toward the -100 volts, but when the voltage at the junction between R248 and R249 reaches approximately ground level, D250 turns on and transistor Q255 is turned off. The positive-going voltage at the collector of Q255 then turns off Q235 and Q214. When Q214 turns off, it resets the triggering circuits as described previously and the holdoff period is at its halfway point.

The reset of D195 turns off Q204 and current is reestablished through D227, turning off D228. Current through D233,

which was forward biased when Q235 turned off, allows the holdoff capacitors to begin a runup toward the $+100$ -volt supply. When the voltage at the emitter of Q235 reaches about $+12$ volts, Q235 turns back on, turning on Q255 and Q214 and turning off D233. Q214 then rearms the trigger circuits making them ready for another triggering event.

Minimum duration of the holdoff cycle is slightly longer than $10 \mu\text{sec}$ for all the fast equivalent sweep rates, with only C230 connected to the circuit. For slower sweep rates, larger holdoff capacitors are connected through the TIME POSITION RANGE switch to retard the holdoff rundown and runup. The holdoff interval is always slightly longer than the maximum excursion of the fast ramp.

DELAYED PULSE MULTIVIBRATOR

Normally, transistors Q265 and Q275 in the delayed pulse multivibrator are turned on. In this state, very little current flows into or out of the delayed pulse generator circuit in the oscilloscope. When a trigger pulse is received and D195 turns Q204 on, a voltage pulse is developed across the secondary of T224, sending a drive signal to the delayed pulse multivibrator. The positive portion of the pulse is applied through D263 to the base of Q275, turning off Q275 and Q265 and sending a 15-ma negative-going current pulse to the delayed pulse generator circuit in the oscilloscope. If the bias on the delayed pulse tunnel diode is set correctly, this diode is switched to its high-voltage state, producing the Delayed Pulse output.

When transistors Q275 and Q265 turned off at the beginning of the pulse, C275 began to charge up toward $+19$

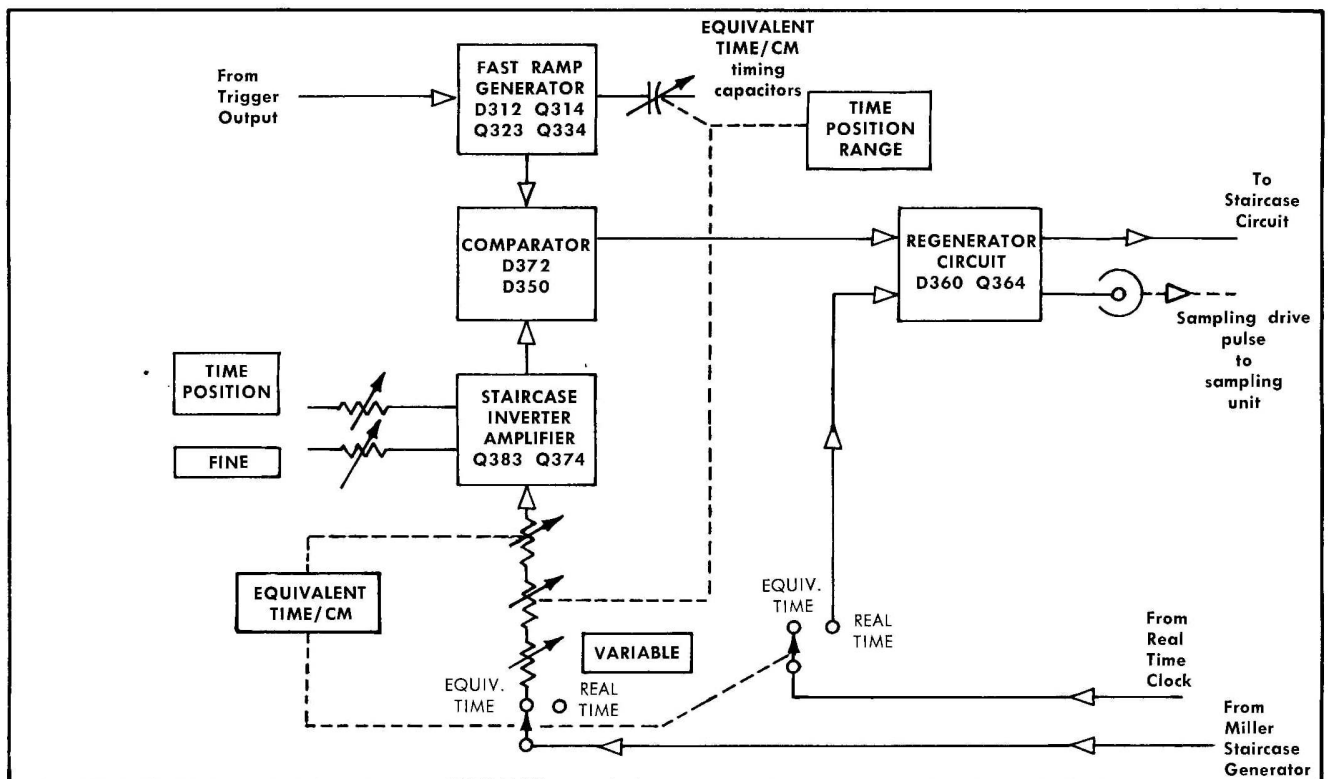


Fig. 3-6. Block diagram of Fast Ramp circuit.

Circuit Description—Type 5T3

volts through R275. When C275 has charged up to approximately 7 volts, D260 turns on and current through R263 turns on Q275, causing the multivibrator to regenerate into saturation. C275 is then discharged through the multivibrator and a positive-going current pulse is sent to the delayed pulse tunnel diode in the oscilloscope to reset it to its low state.

Fast Ramp

The fast ramp diagram includes four main circuits—a staircase inverter amplifier, a fast ramp generator, a comparator and a regenerator.

In equivalent-time mode, these circuits operate to generate the slewed sample drive pulses and the staircase advance pulses that allow the sampling event to progress along the waveform. Feedback voltage from the Miller staircase generator is applied through magnification attenuators to the staircase inverter amplifier. The output of this amplifier is thus an inverter staircase that follows the waveform of the horizontal sweep voltage. Each time the fast ramp generator is triggered, it runs down rapidly until its output voltage is equal to the existing level at the output of the staircase inverter amplifier. When these two voltages become equal, the comparator produces an output pulse that triggers the regenerator circuit. The regenerator then turns on, sending time-oriented pulses to the sampling unit and to the staircase driver circuit to initiate a single sampling event and staircase advance.

In real-time mode, the inverter amplifier is turned off, preventing the comparator from generating output pulses. Clock pulses from the real-time clock circuit then operate the regenerator circuit to pulse the sampling unit. Pulses from the regenerator circuit to the horizontal sweep generator, however, do not advance the staircase, since the staircase driver circuit is disabled in real-time mode.

STAIRCASE INVERTER AMPLIFIER

The staircase inverter amplifier, composed of Q383 and Q374, is an operational amplifier with a gain determined by the ratio of feedback resistor R383 to the input resistor selected by the EQUIVALENT TIME/CM switch. The 52.5-volt staircase voltage is applied to the input through the TIME POSITION RANGE and EQUIVALENT TIME/CM switches. When the Equivalent Time/Cm MAGNIFIER switch is locked to the TIME POSITION RANGE switch, a 1, 2, 5 magnification sequence is obtained for any particular time position range as the switches are turned. This is accomplished by changing the 1-, 2-, 5-step series resistors (R722, R724 and R726) that serve as the input resistors to the inverter amplifier. (These resistors are shown on the Equivalent Time/Cm Switch schematic diagram.) In addition, when the Equivalent Time/Cm MAGNIFIER knob is pulled out and turned clockwise, two attenuators may be connected to the input of the inverter amplifier to change the amplitude of the applied signal. The attenuators consist of R701, R702 and R705 (a 10× attenuator); and R710, R712 and R715 (a 100× attenuator). The greater the attenuation applied to the input of the staircase inverter amplifier (or the smaller the amplification factor), the smaller the staircase inverter output excursion becomes and the less equivalent time there is between samples. This produces the effect of magnifying the display, though the dot density of the display remains

unchanged. The Equivalent Time/Cm VARIABLE control R650 can also change the gain of the amplifier, since it is a series input resistor. On the fastest sweep rates, R669 and R666 provide increased attenuation for further magnification.

The TIME POSITION and FINE controls (R395A and B) determine the dc level at which the output staircase waveform starts. The range of these controls can cause the starting level to move a total of 7.5 volts. By moving the entire staircase waveform up or down, the TIME POSITION controls cause all the samples to be delayed or advanced by the same amount of time, and therefore have the effect of moving the "time window" of the crt screen along the waveform.

The INVERTER DC LEVEL adjustment (R376) adjusts the input level of the amplifier to match the output level of the staircase start, so that no current will flow in the input resistors until the staircase begins its excursion. The TIME POSITION ZERO adjustment (R390) is set so the comparison events begin as soon as the sweep starts.

In equivalent-time mode, when the oscilloscope Horizontal Display switch is set to one of the external or manual sweep positions, the externally applied signal instead of the staircase is applied through the EQUIVALENT TIME/CM switch to produce the comparison voltage. Since the input current to the inverter amplifier is still proportional to the horizontal deflection voltage, the horizontal position of each dot on the crt screen is still referenced to time.

In real-time mode, with the EQUIVALENT TIME/CM switch set to REAL TIME, the input to the staircase inverter amplifier is tied to +19 volts through R720, driving the output down until it is stopped at -19 volts by D385. Since the maximum excursion of the fast ramp generator is about 17 volts, D372 never turns on and D350 never switches. As a result, these circuits are disabled in real-time mode.

FAST RAMP GENERATOR

Before arrival of a trigger from the trigger output circuit, Q314 is operating as a non-saturated clamp transistor with its base at about -0.4 volt and its collector at about -2 volts. Q323 is a common-base amplifier supplying current both to the base of Q314 and to tunnel diode D312. The diode is held in its high state by the current through Q323. Current is drawn by Q314 from the -19-volt supply through D328 and from Q334, the ramp current-source transistor.

When the trigger output tunnel diode switches to its high state, D312 is switched to its low state, quickly turning off Q314 and clamp diode D328. The 7.5 ma of current that Q314 had been drawing from Q334 and R340 (TIMING CURRENT) is switched into the ramp timing capacitors through the comparator circuit. The ramp capacitors (C350 A-K) then begin charging at a linear rate toward -100-volts. The particular rate of the ramp rundown is determined by the capacitor selected by the EQUIVALENT TIME/CM switch. On the fastest sweep rates, the ramp slope is 7.5 volts in 20 nsec, produced by C343 and the inherent capacitance in the circuit.

The ramp voltage continues its rundown until a comparison is made with the staircase inverter output by D372, and the comparator switches.

At the beginning of the fast-ramp operation, when Q314

and D328 turned off, the current that had been flowing through D328 was switched into Q323 and D312, bringing D312 up near its switching point. When D195 in the trigger output circuit returns to its low state halfway through the trigger holdoff period, D312 switches back to its high-voltage state, and Q314 and D328 turn back on.

COMPARATOR

The bias on tunnel diode D350 is determined by the current division between R345 and R347 in series with D350, and is adjusted by R345 (COMP LEVEL) to be very close to its switching point when the fast ramp rundown approaches the staircase inverter level. When D372 becomes forward biased, the additional current through D350 and D372 causes D350 to switch to its high-voltage state, sending an output pulse through T350 to the regenerator.

At the fastest sweep rate there is no arming current for D350, but the increased current through D372 at the time of comparison switches D350 approximately 1 nsec after comparison starts.

REGENERATOR

In equivalent-time mode, the comparison pulse applied through T350 switches D360 to its high state, turning on Q364. As Q364 is turned on, a positive-going pulse is sent to the sampling unit and to the staircase driver in the horizontal sweep generator. D360 resets automatically following the pulse and Q364 turns off.

In real-time mode, the comparator circuit is not operating, and the regenerator circuit is operated by negative-going gate pulses from the real-time clock. Each clock pulse applied through R360 causes D360 to switch to its high state and Q364 to turn on.

Horizontal Sweep Generator

GENERAL

The horizontal sweep circuit includes a sweep lockout, a sweep gate multivibrator, a staircase driver amplifier, a

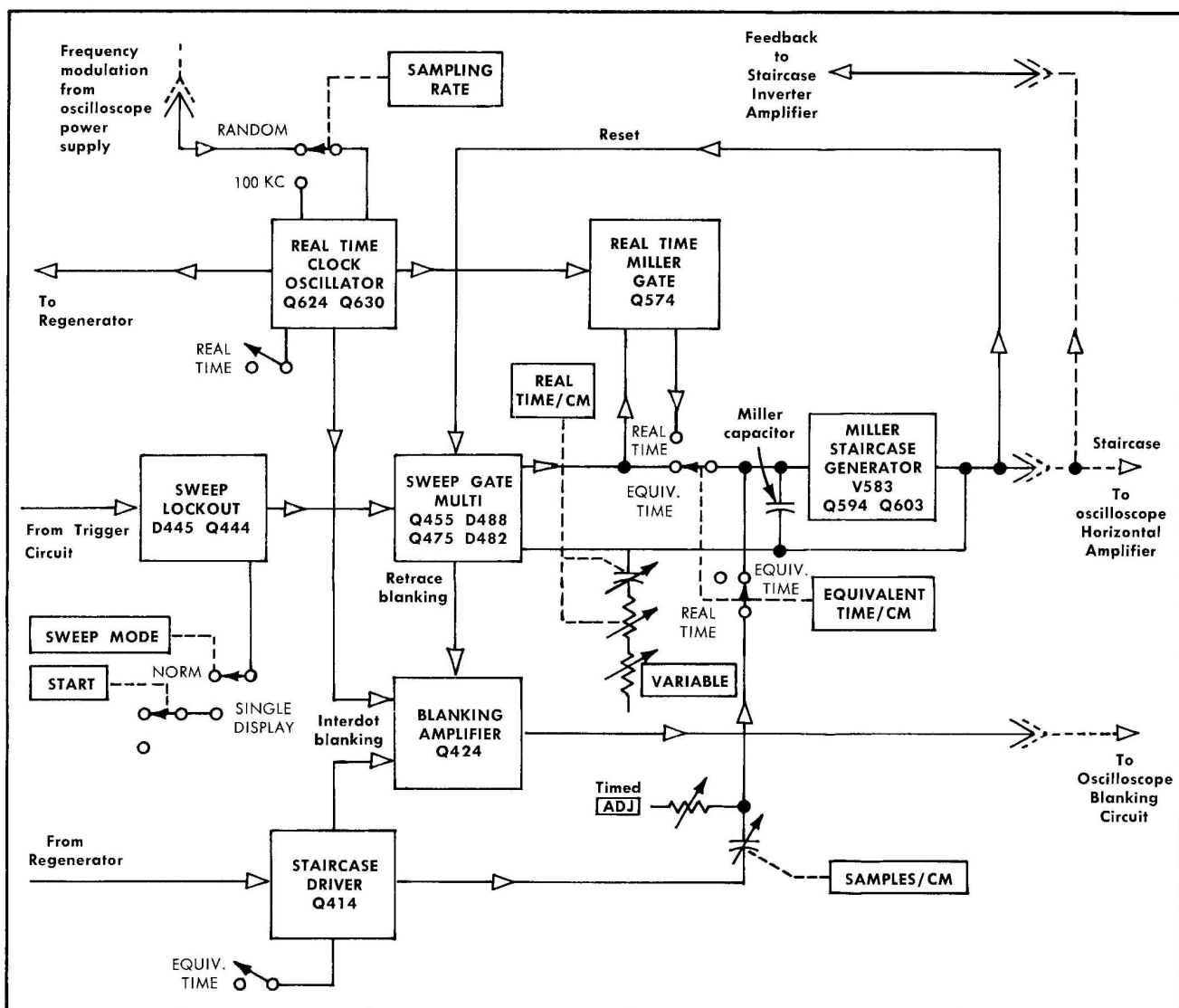


Fig. 3-7. Block diagram of Horizontal Sweep Generator.

Circuit Description—Type 5T3

real-time clock oscillator and gate, a Miller staircase generator and a blanking amplifier. Switching is provided by the Equivalent Time/Cm, the Real Time/Cm, the Time Position Range and the Samples/Cm switches.

Equivalent-Time Mode. Each time the trigger circuit sends a start pulse to the fast ramp circuit to initiate the sampling sequence, it also pulses the sweep lockout in the horizontal sweep circuit. If the sweep gate has been reset, the lockout circuit switches the gate so the sweep starts as soon as the first sample pulse is received. Further trigger pulses applied to the sweep gate through the sweep lockout have no effect until the gate has been reset following completion of the sweep. When triggered, the sweep gate disconnects the Miller staircase capacitors from the discharge path through the disconnect diodes, allowing pulses from the staircase driver to charge up the Miller capacitors.

Following comparison, the regenerator circuit sends a sample drive pulse to the sampling unit and a staircase-advance pulse to the staircase driver at the input to the Miller circuit. The staircase driver in turn sends pulses to the Miller staircase generator and to the blanking amplifier. The amount of charge in the pulses applied to the Miller staircase generator is determined by the capacitors connected into the circuit by the front-panel SAMPLES/CM switch. The step-by-step increase in the charge on the Miller capacitors produces the staircase output voltage.

The staircase output drives the oscilloscope horizontal amplifier for horizontal deflection of the crt beam and also provides the feedback comparison voltage for advancing the sample delay so the sample will be taken later each time with respect to the trigger. When the staircase output reaches a certain value (set by the SWEEP LENGTH control), it resets the sweep gate circuit, causing the Miller capacitors to discharge, and the circuit is ready to start another sweep with the next input trigger pulse.

Real-Time Mode. Whenever the EQUIVALENT TIME/CM switch is set to the REAL TIME position, the real-time clock oscillator operates. Output pulses from the oscillator are sent to the regenerator circuit to strobe the sampling unit, to the Miller circuit to step the staircase, and to the blanking amplifier. The real-time clock gate remains non-conducting while the sample is displayed. When the gate is pulsed by the clock, all the charge that has built up on the real-time capacitors is transferred through the gate to the Miller capacitors, producing an output step. The output of the circuit thus remains a staircase, but the size of each step is proportional to the amount of time elapsed since the previous step. Operation of the sweep lockout, the sweep gate and the blanking amplifier is essentially the same as for equivalent-time operation.

Single Display. When the SWEEP MODE switch is set to SINGLE DISPLAY and the START button pressed, the sweep lockout circuit permits a single trigger pulse to initiate a full sweep of the crt display, but locks out subsequent trigger pulses.

Blanking. During the time that a sample drive pulse is applied to the Miller circuit to step the staircase voltage, a pulse is also applied to the blanking amplifier, causing it to blank the crt while the voltage step is taken. This is called interdot blanking. During retrace of the sweep,

while the sweep gate circuit is being reset, the gate circuit also applies a voltage to the blanking amplifier to blank the crt. This provides retrace blanking.

SWEEP LOCKOUT

Pulses from the collector of Q204 in the trigger circuit are sent through Q444 in the sweep lockout circuit to switch the sweep gate. Quiescently, with the SWEEP MODE switch set to NORM, Q444 is cut off and its collector is at about 6.5 volts. Each negative trigger pulse applied through C440 and R440 to the emitter of Q444 turns the transistor on rapidly, producing a fast 6-volt negative pulse at the collector. The pulse is sent through C446 and R448 to the sweep gate circuit. At the end of each pulse from the trigger circuit, the emitter of Q444 returns to ground and the transistor turns off. The positive-going collector pulse as Q444 turns off is shorted to ground through D448.

A single sweep of the crt is obtained when the SWEEP MODE switch (SW435) is set to SINGLE DISPLAY and the START button (SW430) is pressed. With the SWEEP MODE switch at NORM, the cathode of D445 is connected to ground through R431 and R435 and the diode is normally turned off. When the switch is set to SINGLE DISPLAY, the cathode is connected to a negative voltage from the voltage divider R438, R435 and R431. The diode is still in its low-voltage state, but is biased up near its switching point. The first negative trigger received from the trigger circuit switches D445 to its high-voltage state while Q444 sends the negative pulse to the sweep gate in the usual manner. Following the end of the trigger pulse, however, the emitter of Q444 is held below ground, keeping the transistor turned on. With Q444 turned on, negative pulses cannot be transmitted through the transistor to the sweep gate. As soon as the sweep gate has reset, the sweep is locked out and the staircase output is locked at zero.

In addition to setting the bias on D445, the SWEEP MODE switch in SINGLE DISPLAY position connects a voltage across C430, charging it to approximately 19 volts. If the START button is pressed, the negative side of the capacitor is connected to ground, causing a positive pulse to be applied to the cathode of D445 and the emitter of Q444. The diode switches momentarily to its low-voltage state and Q444 turns off. As soon as C430 has discharged, D445 returns to its triggerable bias point. The next pulse from the trigger circuit turns on Q444, initiating a single sweep of the display, and switches D445 back to its high-voltage state. Releasing the START button again connects C430 to -19 volts. This has no effect on either D445 or Q444, but it allows C430 to recharge, to be ready to initiate another single display.

At the end of the single sweep, the sweep gate resets and is ready to be switched, but with Q444 held in the conducting state, subsequent sweeps are locked out until the START button is pressed again.

SWEEP GATE

The sweep gate circuit (Q455-Q475) is a bistable multivibrator that operates with both transistors turned on during the sweep and both transistors turned off during the retrace. At the end of the retrace period, just prior to a new sweep, the voltage at the base of Q455 returns to a level slightly above ground, holding the transistor in cutoff. With the SWEEP MODE switch set to NORM, negative pulses

are continuously being applied from the sweep lockout circuit to the sweep gate through C446 and R448. The first negative pulse that is able to forward-bias the base-emitter junction of Q455 turns on the transistor, switching the multivibrator. The collector of Q455 goes positive, turning on Q475. The collector of Q475 then goes negative and the regenerative action of the circuit causes both transistors to saturate. The negative voltage at the collector of Q475 reverse-biases D482 and D488, disconnecting the Miller circuit from the sweep gate, allowing the sweep to progress as the staircase capacitors charge.

The output signal from the Miller circuit is applied to the sweep gate circuit through R610, D610, R611 and R612 (SWEEP LENGTH). As the staircase voltage rises, more current is drawn through the sweep length network, diverting current from the base of Q455. R612 is adjusted so when the staircase output voltage reaches 52.5 volts, Q455 will be turned off. The negative step at the collector of Q455 turns on the blanking amplifier transistor and turns off Q475, allowing its collector to go positive. This positive-going collector voltage forward biases D488 and the staircase capacitors begin to discharge. The resulting rise on the grid of V583 operates through the Miller circuit, causing the staircase output voltage to drop quickly to near ground voltage. When the negative-going output forward-biases D482, the diode conducts and a state of clamped equilibrium exists. D488 remains forward biased and conducting current away from the grid of V583 until the sweep gate is triggered and switches again.

When the output voltage drops during the discharge of the staircase capacitor, D610 becomes reverse biased, disconnecting the sweep gate from the staircase output. C611, which had charged up to the staircase voltage, discharges through the SWEEP LENGTH control circuit, setting the hold-off time of the staircase. The current source is restored to the base of Q455 as C611 discharges; however, Q455 is held in cutoff by the current through D455 and R450. The next negative trigger from the sweep lockout will trigger the sweep gate to initiate a new sweep.

STAIRCASE DRIVER

In equivalent-time mode, Q414 serves as a constant-voltage pulse source for driving the samples/cm capacitors and the blanking amplifier. Capacitively-coupled positive pulses are applied from the regenerator circuit to the base of Q414, turning on the transistor and delivering negative pulses through R421 to C560 (SAMPLES/CM). The size of each pulse is set by SAMPLES/CM CAL adjustment R415. The amount of charge applied through D565 to the Miller grid circuit is determined by the particular capacitance value selected by the front-panel SAMPLES/CM switch.

In real-time mode, the emitter current supply for Q414 is disconnected and the circuit is inoperative.

REAL-TIME CLOCK AND MILLER GATE

The real-time clock oscillator consists of a blocking oscillator (Q630) and a transistor that provides current (Q624) to the blocking oscillator. When the SAMPLING RATE switch (SW615) is set to the 100 KC position, Q624 is operated as a 100-kc oscillator. In this mode, sufficient current is supplied from the collector of Q624 during oscillation

peaks to completely charge C632 from +19 volts to below ground. When the emitter voltage of Q630 becomes slightly negative, D635 turns on, forward-biasing the base-emitter junction of Q630. This transistor turns on, starting the blocking oscillator action that produces a large output pulse across each output winding of T635. The blocking oscillator pulses are sent to the regenerator circuit, the blanking amplifier (Q424) and the real-time Miller gate (Q574). When the backswing has ended, C632 is charged back up to +19 volts.

When Q574 is momentarily saturated by the blocking oscillator pulse, the charge on the real-time timing capacitors is transferred to the Miller capacitor C495, causing the staircase output to make a step.

In the RANDOM POSITION of the SAMPLING RATE switch, Q624 is connected as a dc current source that can charge C632 from +19 volts to a point slightly below ground in about 12.5 μ sec. This current to C632 is frequency-modulated by 60 cps hum from the oscilloscope heater circuit. Thus the oscillation period of Q630 in random mode varies by about $\pm 5\%$. The purpose of the modulation is to break up false displays that might occur as a result of viewing signals that are multiples of 100 kc.

MILLER STAIRCASE GENERATOR

In equivalent-time mode, the negative output pulses from the staircase driver circuit are sent through R421, C560, D565 and R570 to the Miller capacitors (C493 and C495) and the grid of V583. The amount of the charge delivered to the capacitors is determined by the value of C560.

When the sweep gate circuit is holding off the sweep, the energy of the stepping pulses is sent through D488 and dissipated. As soon as the sweep gate has switched and disconnected D482 (the discharge path), the pulse energy starts to charge up the Miller capacitors. In this mode (equivalent-time), Q574 is shorted out by the EQUIVALENT TIME/CM switch. The voltage on the grid of V583 begins to drop and the voltage on the cathode follows. An amplified positive signal is produced at the collector of Q594 and coupled to the output. This signal, applied to the output side of the Miller capacitors keeps the grid of the tube nearly stationary and each energy pulse applied to the grid appears as a charge on C493 and C495.

The staircase voltage output, which runs from zero to 52.5 volts, is sent through the EQUIVALENT TIME/CM switch to the staircase inverter amplifier, to the sweep gate to reset the gate, and to the oscilloscope horizontal amplifier to produce the horizontal deflection of the crt beam.

When enough pulses have been received to raise the charge on the Miller capacitors to the required staircase amplitude, the sweep gate is switched, causing the disconnect diodes to discharge the Miller capacitors, and the staircase recovers to produce another sweep.

During positive excursions, the output emitter follower, Q603, is turned on to provide the necessary current at the output. During reset, D597 turns on to reset the base of the staircase near zero volts. R585 (STAIRCASE ZERO) adjusts the output level so the staircase does start at zero volts.

In real-time operation, the real-time timing capacitors C488, C486, C490 and C493 are used to produce a ramp

Circuit Description—Type 5T3

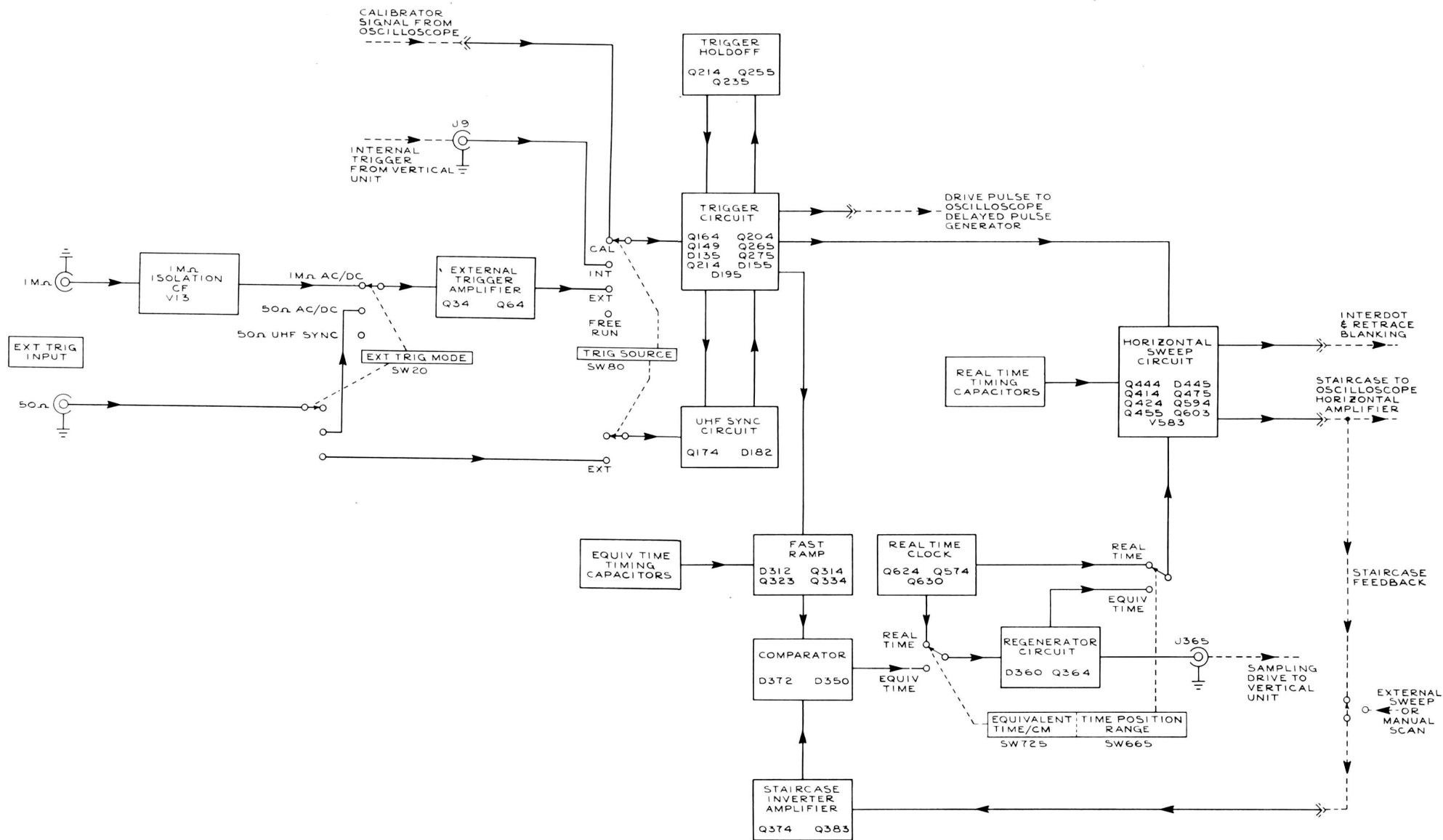
sawtooth waveform at the emitter of Q574. In this mode, Q574 is not shorted out, but is gated on by the blocking oscillator pulses from the real-time clock. The particular combination of capacitors and resistors selected by the REAL TIME/CM switch then produces a linear ramp as the capacitors charge from the —100-volt supply. When Q574 is pulsed on, the charge is transferred to C495 to produce the real-time staircase step. Each step made in real-time mode is proportional to the real time elapsed between the previous sample and the new one.

BLANKING AMPLIFIER

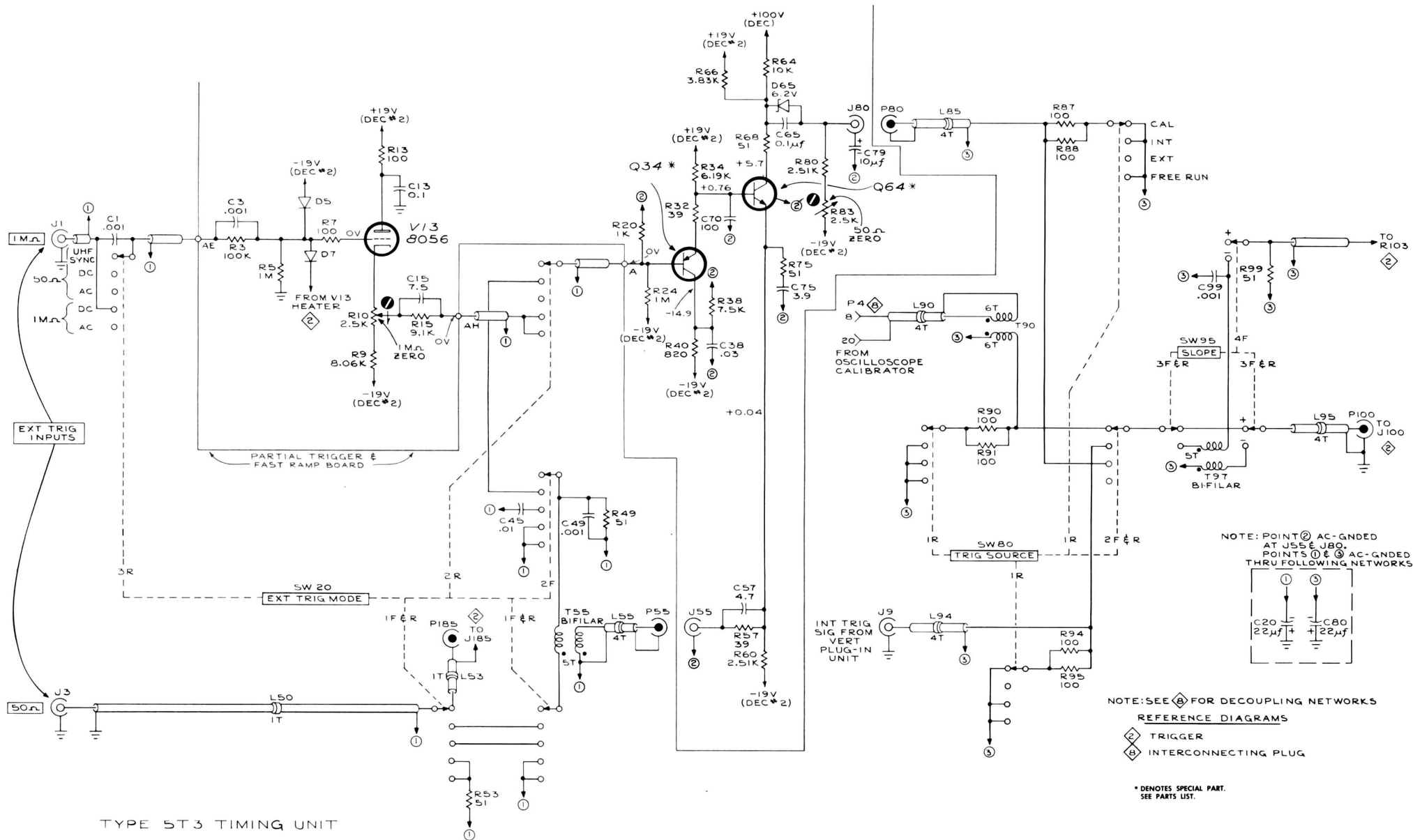
The blanking amplifier (Q424) is driven by the staircase driver, the real-time clock and the sweep gate to provide blanking signals to the oscilloscope. The collector of Q455 in the sweep gate circuit is connected through R457 to the base of Q424, and one winding of T635 in the real-

time clock is connected through D458 and R458 to the base of the transistor. While the staircase is being generated, the voltage applied to Q424 from the sweep gate circuit is set slightly positive so the blanking amplifier will be turned off except when a negative pulse is applied from the staircase driver (through R420 and C420) or from the real-time clock. During retrace, while the Miller capacitor is being discharged and the horizontal deflection voltage is returning the crt beam to the left side of the screen, the negative voltage from the sweep gate keeps Q424 turned on.

The collector circuit of Q424 is completed in the oscilloscope, so that whenever the transistor is turned on, current through it produces blanking of the crt. Thus, no sample dot is displayed on the screen while the dot position is changing or while the beam is retracing to the left side of the crt.

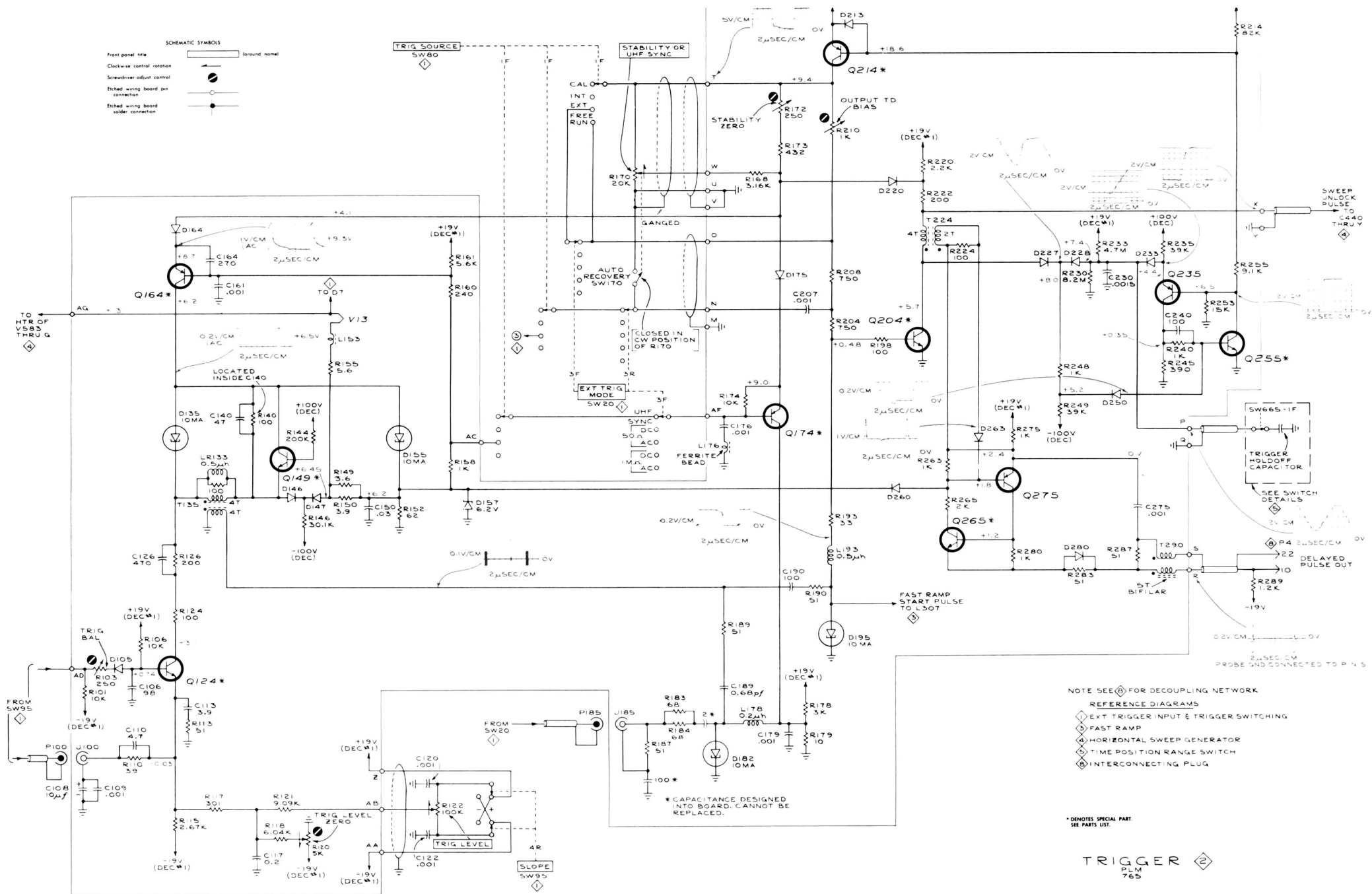


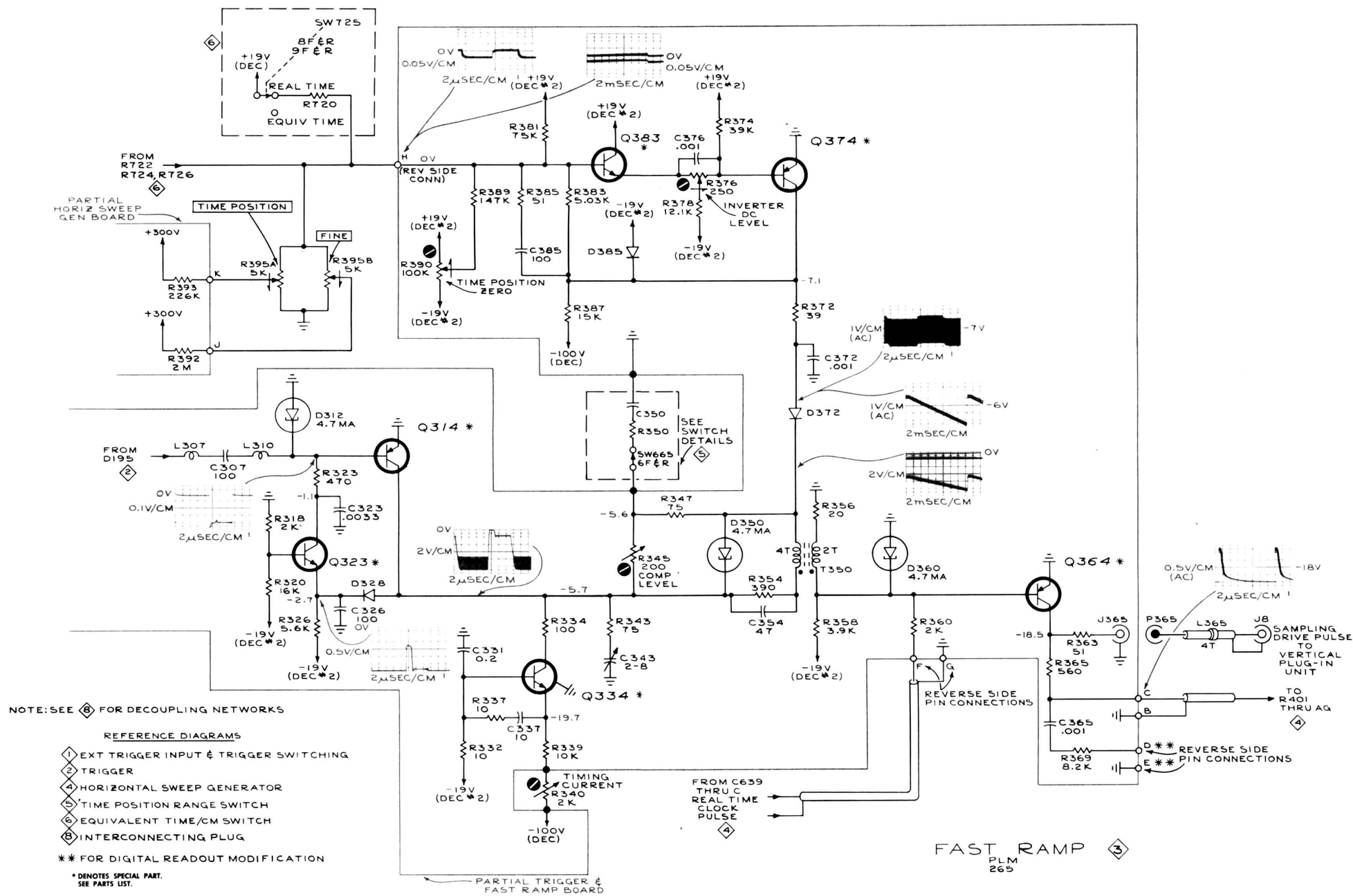
BLOCK DIAGRAM



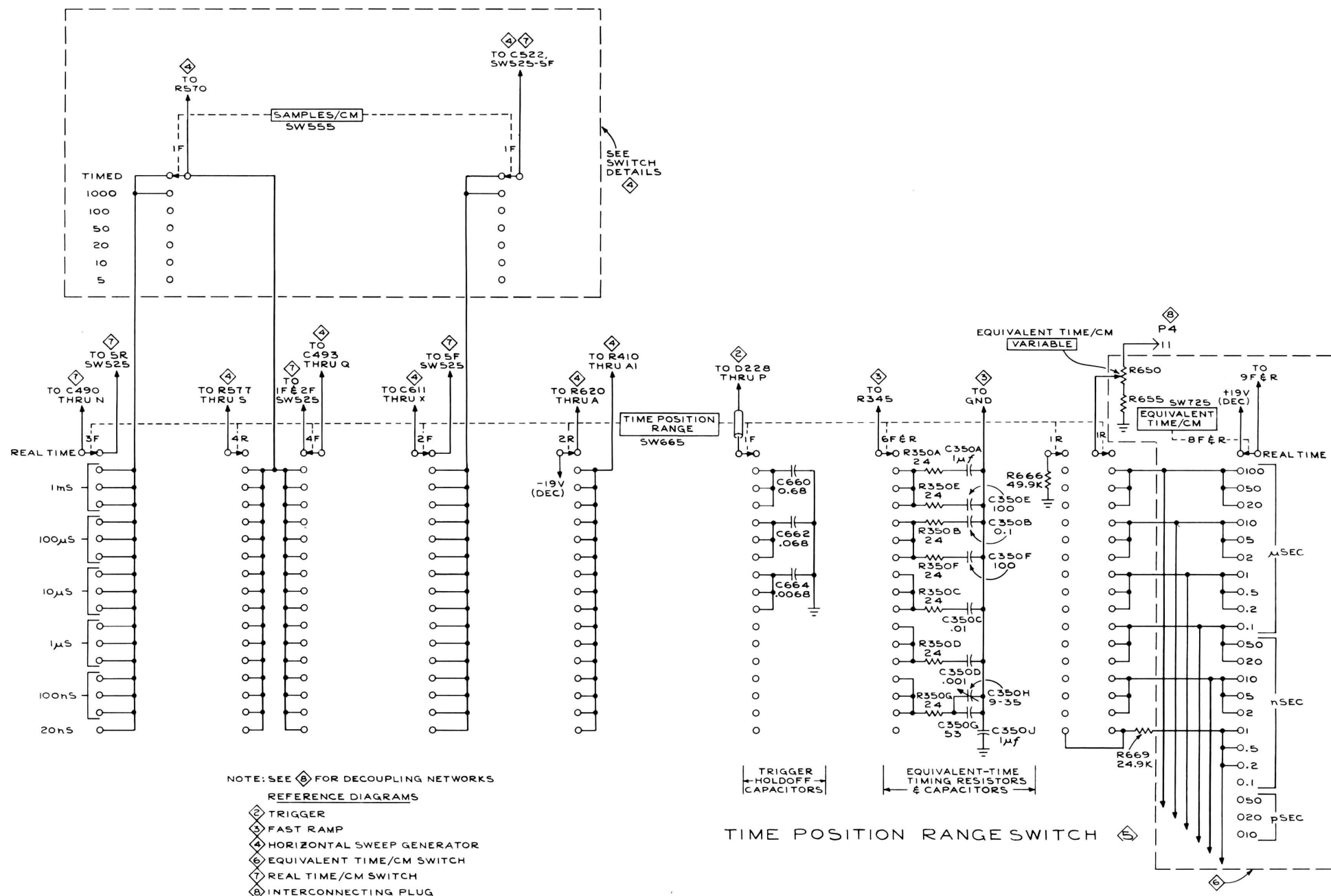
EXT TRIGGER INPUT & TRIGGER SWITCHING ①

PLM
265

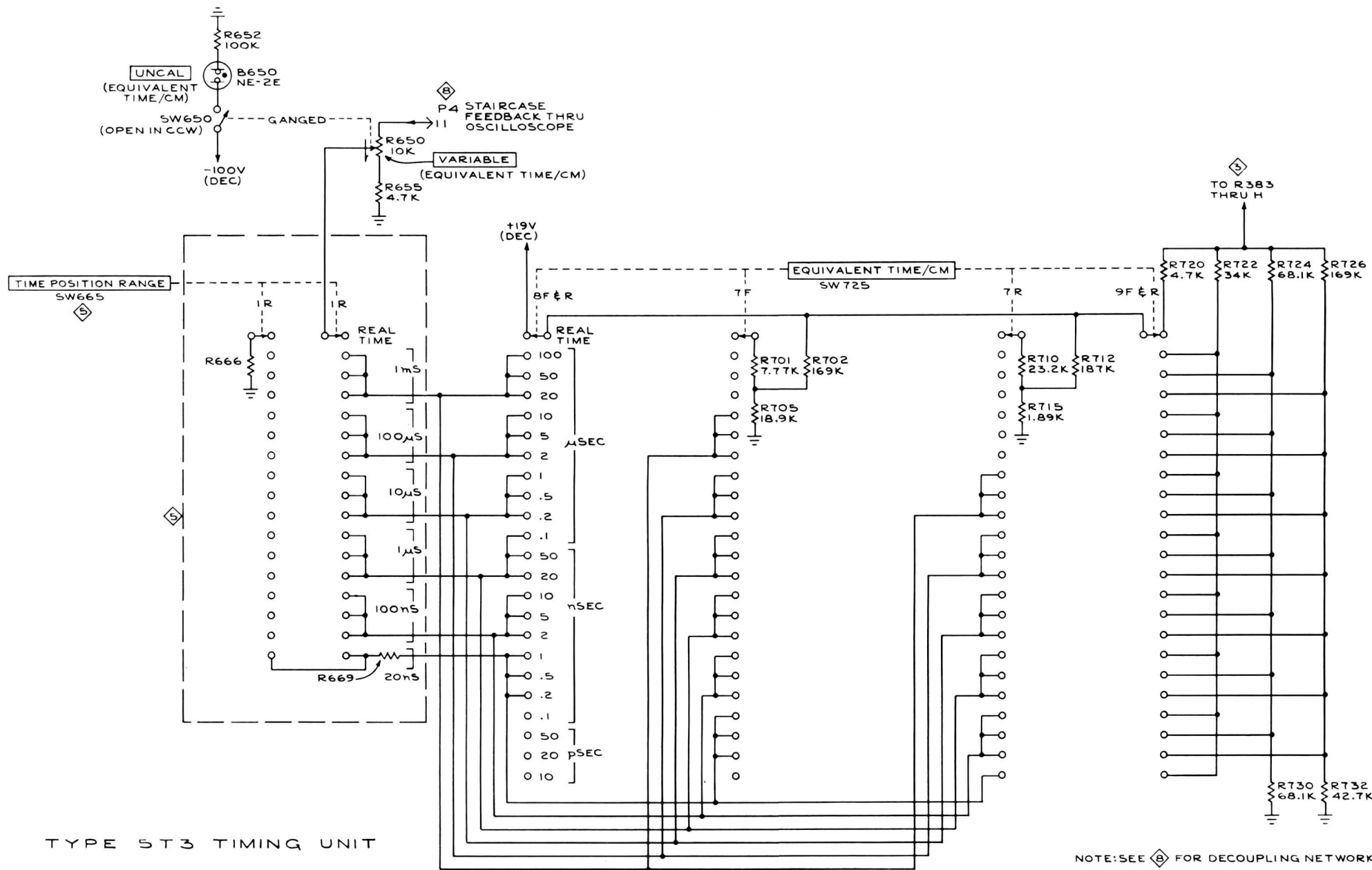




TYPE 5T3 TIMING UNIT



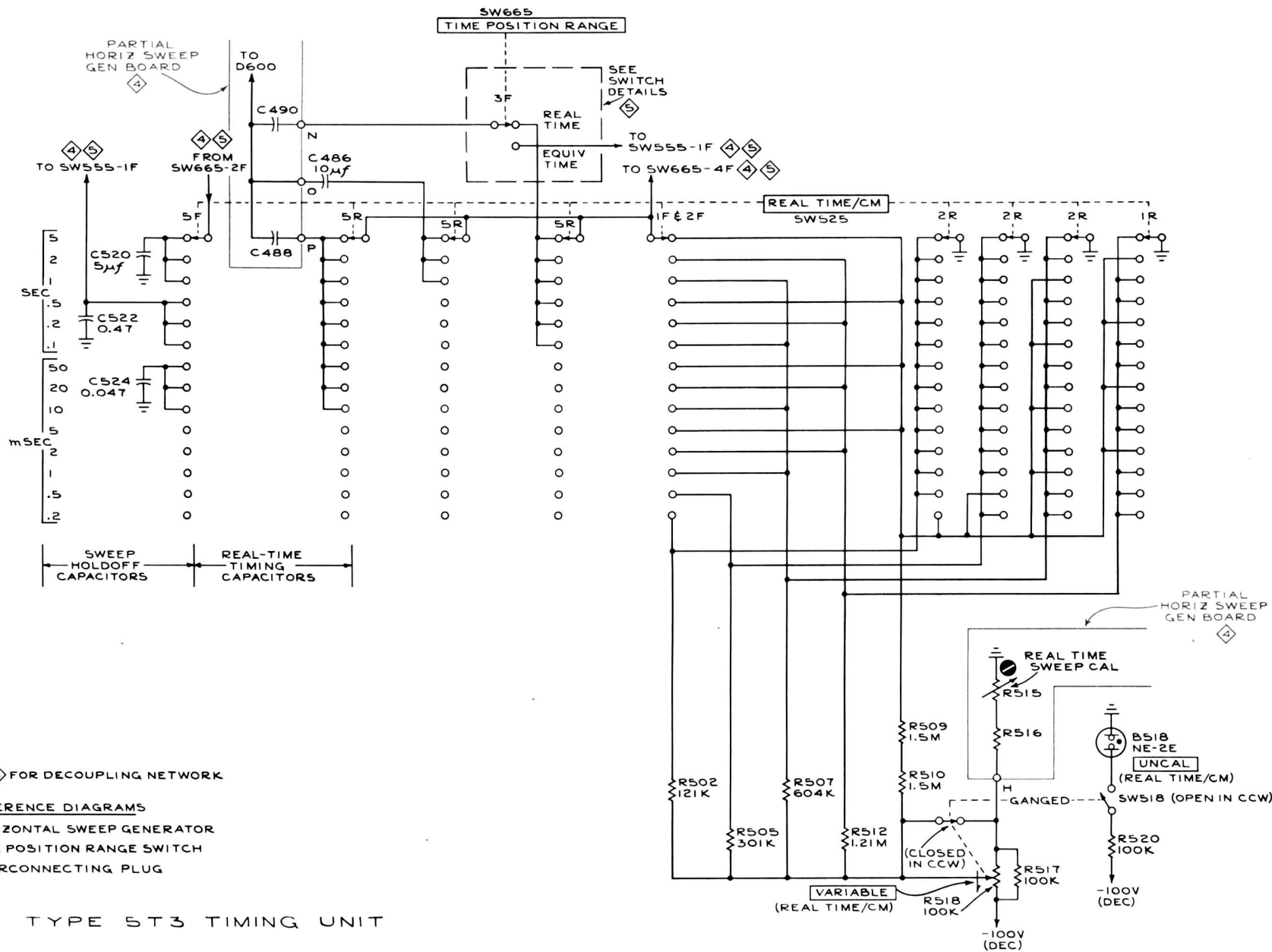
TYPE ST3 TIMING UNIT



NOTE: SEE \diamond B FOR DECOUPLING NETWORK
REFERENCE DIAGRAMS

- \diamond FAST RAMP
- \diamond TIME POSITION RANGE SWITCH
- \diamond INTERCONNECTING PLUG

EQUIVALENT TIME/CM SWITCH \diamond E



REAL TIME/CM SWITCH ⑦
PLM
365

INTERCONNECTING PLUG 
PLM
365