TEKTRONIX®

485/R485

OSCILLOSCOPE

SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97005

Serial Number _____

070-1193-00

473

The 485 Portable Oscilloscope.

SPECIFICATION

Introduction

The 485/R485 is a general-purpose, environmentalized, high-performance, portable, wide-band oscilloscope which has a dual-channel vertical amplifier with selectable input impedance (DC to 350 MHz bandwidth with 50 Ω input impedance; DC to 250 MHz bandwidth with 1 MΩ input impedance). The 485 has a 1 ns sweep rate, stable triggering to bandwidth limits and calibrated X-Y capabilities. Delayed sweep has calibrated delay time, can be triggered after delay and can be displayed with the intensified main sweep in an alternate sweep switching display. Additional features are X10, X100 probe scale factor readout, 8 div X10 div graticule area, small spot size and high writing rate. A 20 MHz bandwidth limiter, 1 MHz and 1 kHz fast-rise calibrator and autofocus are also included. The 50 Ω input is automatically disconnected from excessive voltages. An external trigger view feature is also provided. The 485-1 and 485-2 have no external trigger view. The 485-2 has only 50 Ω vertical input impedance.

ELECTRICAL CHARACTERISTICS

VERTICAL DEFLECTION SYSTEM (2 identical channels)

Selectable Input Impedance

50 Ω within 0.5%. VSWR ≤1.25:1 on 5 mV/div and 10 mV/div, 1.15:1 from 20 mV to 5 V/div to 350 MHz.

1 MΩ within 1% paralleled by approximately 20 pF.

Bandwidth[1] and Risetime[2] (VARIABLE gain CALIBRATED[3]) From 50 Ω Terminated Source −15°C to +35°C

From 50 Ω terminated source −15°C to +35°C.

50 Ω DC to at least 350 MHz, 1 ns

1 MΩ DC to at least 250 MHz, 1.4 ns

[1] Bandwidth (BW) measured at −3 dB down.

[2] Risetime calculated from 0.35/BW. From +35°C to +55°C, BW is 300 MHz for 50 Ω and 200 MHz for 1 MΩ.

[3] See Fig. 1-1 for effect of VARIABLE gain control.

Input Coupling Selection

AC; DC; GND (provides zero reference, precharges coupling capacitor, disconnects 50 Ω load in 50 Ω mode).

Lower −3 dB Point (AC coupling from 50 Ω source)

50 Ω input, 1 kHz or less.

1 MΩ input 1X, 10 Hz or less.

Deflection Factor

5 mV/div to 5 V/div in 10 calibrated steps (1-2-5 sequence), accurate within 2%. Uncalibrated, continuously variable between steps to at least 12.5 V/div. Lights at edge of knob skirts indicate correct deflection factor for 1X, 10X and 100X probes.

Gain can be recalibrated at front panel. 1 MΩ BAL is available at bottom panel to eliminate step attenuator shift above 10 mV/div, in the 1 MΩ mode.

Display Modes

Channel 1; Alternate; Chopped (approximately 1 MHz rate); Added; X-Y (CH 1 −Y and CH 2 −X); Channel 2 (+Up or Inverted).

Internal Trigger Source

Normal (displayed signal), Channel 1 or Channel 2 signal.

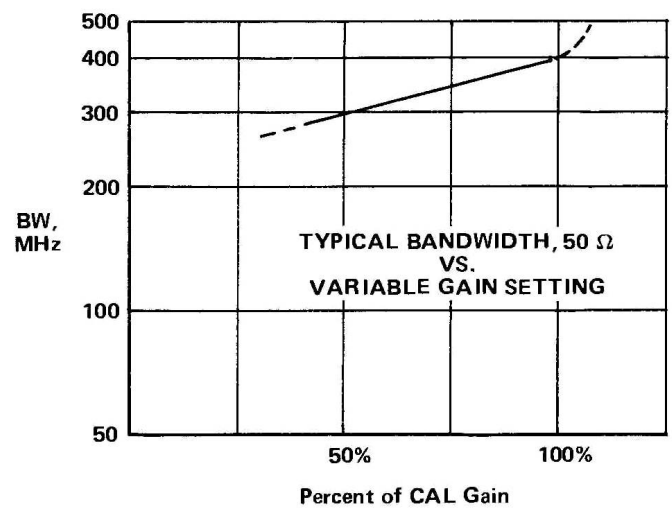

Fig. 1-1. Typical Bandwidth, 50 Ω vs. Variable Gain Setting

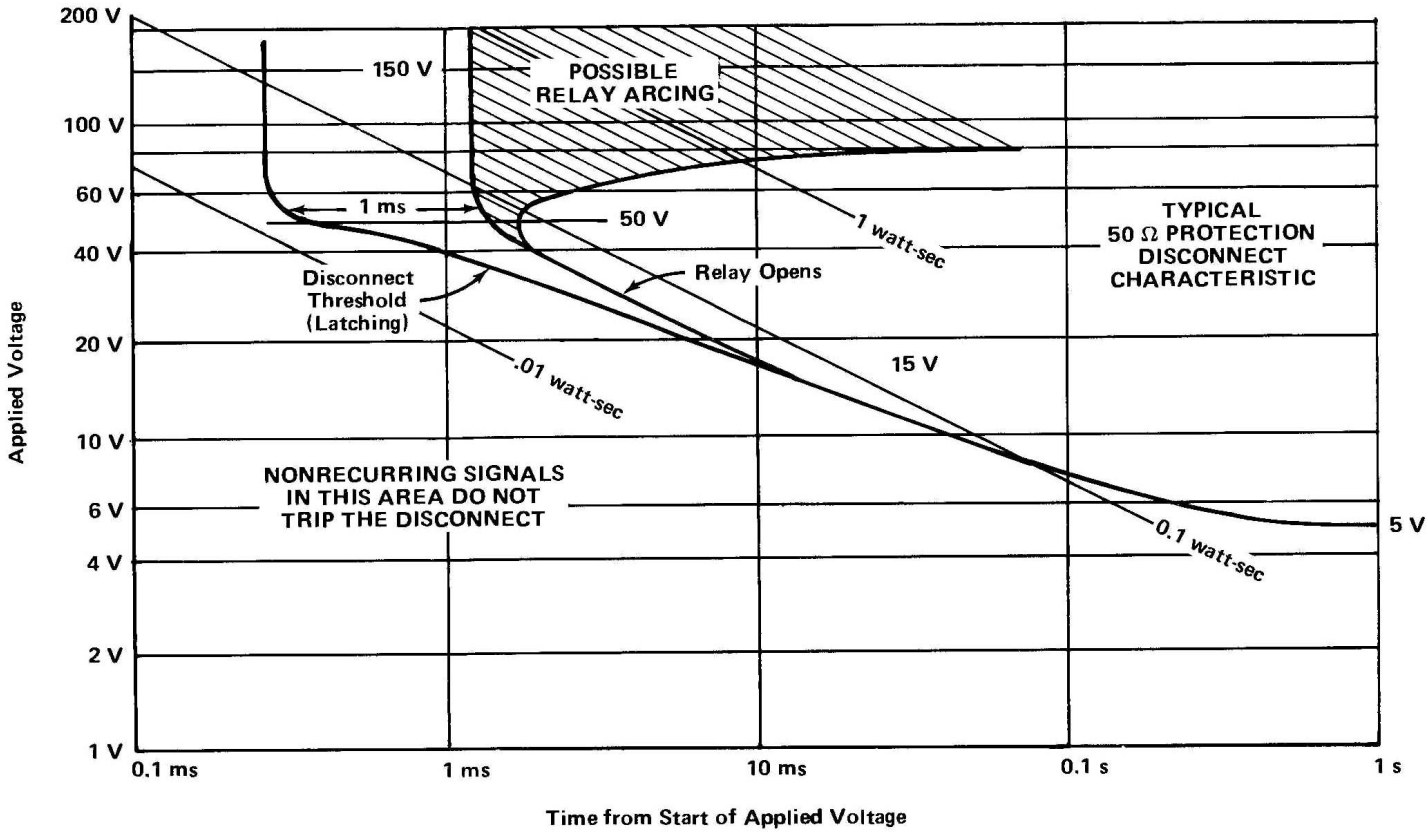

Fig. 1-2. Typical 50 Ω Protection Disconnect Characteristic.

50 Ω Protection

Internal detection circuitry automatically disconnects excessive signals of up to 50 V. The disconnected condition is indicated, and has manual reset.

Maximum Input Voltage

50 Ω Disconnect occurs for voltages that exceed approximately 5 V RMS continuous or 0.1 watt-second for instantaneous voltages of 5 V to 50 V.

Repeated application of voltages in excess of 50 volts and greater than 0.1 watt-second will cause deterioration of K1S1 relay contacts, due to arcing. Signals in excess of 150 volts will damage the instrument.

1 MΩ-DC coupled 250 V (DC + peak AC), 500 V P-P to 1 kHz. AC coupled 500 V (DC + peak AC), 500 V P-P to 1 kHz.

Common Mode Rejection

Added Mode with Channel 2 inverted. At least 10:1 at 50 MHz for 8-division signal after adjusting CH 2 gain for best CMR at 50 kHz and 20 mV/div.

Bandwidth Limiter

Limits to approximately 20 MHz the Vertical Amplifier and Internal Trigger signals.

Channel Isolation

At least 30:1 at 350 MHz.

A Ext Trigger Display (R485 and 485 only)

Momentary pushbutton in VERT MODE area enables display of EXT A Trigger when A source is in EXT position. Deflection factor is approximately 50 mV/div. Risetime is approximately 1.5 ns. Delay match to CH 1 or CH 2 input is within 0.5 ns at 50% amplitude. Triggering level is within 0.5 div of center-screen.

Probe Power

Two 4-pin connectors at the rear of the instrument provide power suitable for optional active probes such as the P6201.

PROBE PERFORMANCE

(Probes are Optional Accessories)

Type		Atten.	Input Impedance	Lower –3 dB point (maximum)	Bandwidth with 485 (minimum)	Temperature Range for this Bandwidth Specification
For Use With 50 Ω Input						
P6056	010-6056-03 – 6 ft. 010-6056-05 – 9 ft.	10X	500 Ω 1 pF	200 Hz	350 MHz	
P6057	010-6057-03 – 6 ft. 010-6057-05 – 9 ft.	100X	5 kΩ 1 pF	20 Hz	350 MHz	–15°C to +35°C
P6201 (FET Probe)	010-6201-01 – 6 ft.	1X Plug- 10X On 100X	100 kΩ 3 pF 1 MΩ <1.5 pF 1 MΩ <1.5 pF	10 Hz 1 Hz 10 Hz	330 MHz	0°C to +35°C
For Use With 1 MΩ Input						
P6053A	010-6053-01 – 3 1/2 ft. 010-6053-03 – 6 ft. 010-6053-05 – 9 ft.	10X	1 MΩ 9.5 pF 1 MΩ 12 pF 1 MΩ 13.5 pF	1 Hz	250 MHz 250 MHz 200 MHz	–15°C to +35°C

A and B TRIGGERING

A Trigger Mode

NORMAL.

Sweep runs only when triggered.

AUTOMATIC.

Sweep free-runs in the absence of a triggering signal and for signals below 20 Hz.

SINGLE SWEEP.

Sweep runs one time on the first triggering event after pressing the reset selector.

B Trigger Mode

B RUNS AFTER DELAY TIME.

Starts automatically at the end of the delay time.

B TRIGGERABLE AFTER DELAY TIME.

Runs when triggered. The B (delayed) sweep runs once, in each of these modes, following the A sweep delay time.

Time Base A and B Trigger Sensitivity

Trigger Mode	To 50 MHz	At 350 MHz
DC Int	0.3 div	1.5 div
DC Ext	20 mV	100 mV
AC	Signals below 16 Hz are attenuated.	
LF Reject	Signals below 16 kHz are attenuated.	
HF Reject	Signals below 16 Hz and above 50 kHz are attenuated.	

Level and Slope

Internal, permits selection of triggering point at any level on the positive and negative slope of the displayed waveform. External, level is adjustable through at least ±0.5 V for either polarity (±5 V for EXT ÷10).

A Source

Internal, Line, External, External ÷10.

B Source

B runs after Delay Time, Internal, External, External ÷10.

External Inputs

1 MΩ paralleled by approximately 20 pF. Maximum input voltage 500 V (DC + peak AC), 500 V P-P to 1 kHz.

Jitter

Less than 0.1 ns at 350 MHz and 1 ns/div.

HORIZONTAL DEFLECTION

Time Base A and B

1 ns/div to 0.5 s/div in 27 calibrated steps (1-2-5 sequence). Uncalibrated, A is continuously variable between steps and to at least 1.25 s/div.

Time Base A and B Sweep Accuracy (Center 8 screen divisions)

Sweep Rate	+15°C to +35°C	−15°C to +55°C
1 ns/div to 20 ns/div	±3%	±5%
50 ns/div to 0.1 s/div	±2%	±4%
0.2 s/div to 0.5 s/div	±3%	±5%

Display Modes

A, A INTENsified during B delayed, ALTernate display of A INTEN and B (delayed sweep). Only A sweep is displayed for A sweep rates of 1, 2 and 5 ns/div.

Minimum Sweep Holdoff (A Trigger Holdoff in Norm detent)

A Time Setting	
1 ns/div to 0.1 μs/div	Less than 0.4 μs.
0.2 μs/div	Less than 1.0 μs.
0.5 μs/div to 0.5 s/div	Less than 2 times the A TIME/DIV setting.

A Trigger Holdoff

Adjustable control permits a stable presentation of repetitive complex waveforms. The control covers at least the time of one full sweep for sweeps faster than 0.2 s/div.

B Ends A

The A sweep is reset at the end of the B sweep to allow the fastest possible sweep repetition rate for increased trace intensity in the delayed sweep mode.

CALIBRATED SWEEP DELAY

Delay Time Range

0 to 9.9 times the Delay Time/Div settings of 10 ns/div to 0.5 s/div.

Differential Delay Time Accuracy (+15°C to +35°C)

Exclude the first (above 0.0) 1.0 turn or the first 40 ns of the DELAY dial.

DELAY TIME Setting	
10 ns/div and 20 ns/div	± (1% of measurement +0.2% of full scale[3])
50 ns/div to 1 ms/div	± (0.5% of measurement +0.1% of full scale)
2 ms/div to 0.5 s/div	± (1% of measurement +0.1% of full scale)

[3] Full scale is 10X the Delay Time/Div Setting.

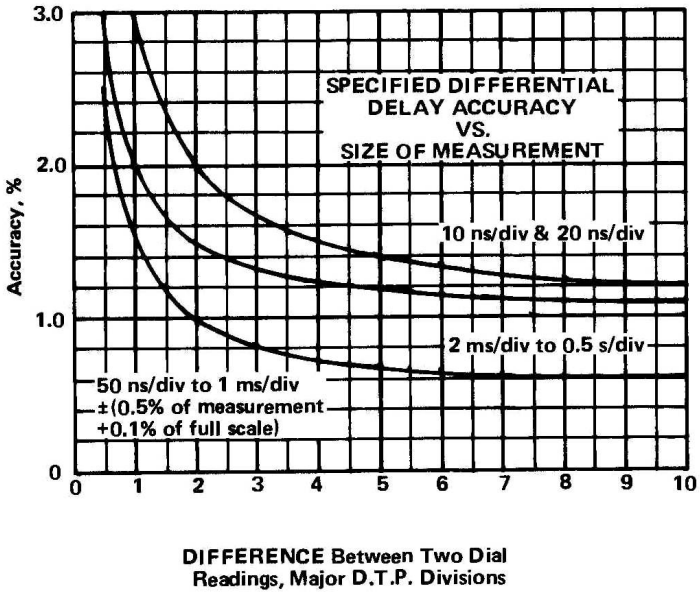

Fig. 1-3. Specified Differential Delay Accuracy vs. Size of Measurement.

Jitter

Less than 0.005% (one part in 20,000) of full scale plus 0.2 ns. (Wrap-around cover must be in place.)

X-Y

Full Sensitivity

(CH 1 Vert, CH 2 Horizontal.) 5 mV/div to 5 V/div in 10 calibrated steps (1-2-5 sequence) accurate within 2%. Gain can be recalibrated at front panel.

Y Performance

Identical to CH 1. See Vertical Deflection.

X-Axis Bandwidth

DC to 4 MHz (with 10 div reference signal).

X-Y Phase Match (Full BW and BW Limit)

Within 3° to 4 MHz.

X-Gain Match to CH 2

+15°C to +35°C: 1%

−15°C to +55°C: 3%

CRT

TEKTRONIX CRT

4-inch rectangular tube; 8X 10 divisions (0.8 cm/div) display area. P31 phosphor normally supplied; P11 optional without extra charge. 21 kV accelerating potential.

Photographic Writing Speed

At least 3 div/ns for standard P31 phosphor; at least 6 div/ns for optional P11 phosphor (with the TEKTRONIX C-31-R Camera and POLAROID 10,000 ASA film).

Auto Focus

Automatically maintains beam focus for all intensity settings. (Intensified zone and EXT Z axis are not auto-focused).

Graticule

Internal, no parallax. Variable edge-lighting. Markings for measurement of risetime. Graticule is dark with illumination off.

Beam Finder

Limits display within graticule area.

External Z-Axis

Risetime 15 ns. Input R 500 Ω. +0.2 V (DC to 20 MHz) blanks trace of average intensity. +2 V (DC to 2 MHz) blanks maximum intensity trace.

Beam Current Limit

Automatically limits the average beam current to protect the CRT phosphor. (Limits average current to 20 μA for sweep rates faster than 50 ms/div; 5 μA for 50 ms/div and slower sweep rates and for X-Y. Backup system shuts down power supply if average current reaches approximately 30 μA.)

CALIBRATOR

Two-Frequency Fast-Rise Calibrator

Accuracies	+15°C to +35°C	−15°C to +55°C
5 V amplitude to 1 MΩ load	0.5%	1%
0.5 V amplitude to 50 Ω ±0.5% load	1%	1.5%
50 mA amplitude to optional BNC accessory current loop	1%	1.5%
Selectable Frequency of 1 MHz and 1 kHz	0.25%	0.5%

Output Resistance

450 Ω

Risetime

Positive edge into 50 Ω, less than 1 ns. Overshoot and ringing less than 2% into 50 Ω at 1 GHz bandwidth.

1 kHz Duty Cycle

49.8% to 50.2%

OTHER CHARACTERISTICS

Signal Outputs

Positive gates from both time bases (approximately 4 V), and a positive-going Sawtooth from Time Base A (approximately 10 V). Gates and Sawtooth are approximately 0.5 V amplitude into 50 Ω.

Power Requirement

Two-position line voltage selector 115 V (90 V to 136 V) and 230 V (180 V to 272 V) 48 to 440 Hz. 60 watts maximum at 115 V and 60 Hz. 0.9 A maximum at 115 V and 60 Hz. Line fuse: 3 A fast.

Cooling

Quiet, filtered, forced-air ventilation. Fan speed increases smoothly with increasing ambient temperature.

ENVIRONMENTAL CHARACTERISTICS

Ambient Temperature

Operating: −15°C to +55°C

Storage: −35°C to +75°C

Altitude

Operating: to 15,000 feet. Maximum allowable ambient temperature decreased by 1°C per 1000 feet from 5,000 to 15,000 feet.

Nonoperating: to 50,000 feet.

Vibration[5]

Operating: 15 minutes along each of the three axis, 0.025 inch peak-to-peak displacement (4 g's at 55 Hz) 10 to 55 to 10 Hz in 1-minute cycles.

Shock[5]

Operating and Nonoperating: 30 g's, one half sine, 11-ms duration, 2 shocks per axis in each direction for a total of 12 shocks.

Electromagnetic Interference

(With 485 EMI modification option 4). Meets interference requirements of MIL-1-618D: power line conducted, 150 kHz to 25 MHz; radiated, 150 kHz to GHz.

Humidity

Operating and Storage: 5 cycles (120 hours) to 95% relative humidity referenced to MIL-E-16400F (par. 4.5.9 through 4.5.9.5.1, class 4).

Dimensions and Weight

Height: 6 and 9/16 inches.

Width: (with handle) 12 inches.

Depth (including panel cover): 18 and 1/2 inches.

Depth (handle extended): 20 and 5/8 inches.

Net weight (without accessory case and panel cover): 21 pounds.

Net weight (with panel cover, accessory case and accessories): 24 pounds.

Domestic shipping weight: 31 pounds.

Export-packed weight: 42 pounds.

[5] R485 strapped to table, not mounted in rack.

CIRCUIT DESCRIPTION

Introduction

This section describes the electrical operation and relationship of the circuits in the Type 485. The theory of operation for circuits that are used only in this instrument are described in detail in this discussion. Circuits that are commonly used in the electronics industry are not described in detail.

50 Ω ATTENUATOR

Two identical attenuators, one for each vertical channel, are used to select the desired vertical sensitivity of the 485. Each attenuator is an integral unit containing various 50 Ω attenuators, input overload protection circuitry and, where applicable, a 1 megohm attenuator and 1 megohm buffer amplifier.

The 50 Ω attenuator is comprised of a delay line, DL410, and four 50 Ω attenuator sections. The ÷ 2 and ÷ 2.5 50 Ω attenuator sections are shared by a 1 MΩ buffer amplifier. The two ÷ 10 attenuator sections are used only in the 50 Ω mode. The delay line equalizes the delay differences between the 1 MΩ buffer amplifier and the 50 Ω mode. R127 provides termination for the 1 MΩ buffer amplifier when the instrument is operating in the 50 Ω mode.

1 MEGOHM BUFFER AMPLIFIER

The 1 megohm buffer amplifier provides a high input impedance and unity gain when terminated in 50 Ω. It is connected to the input through relay K1S1 only in the 1 megohm mode and when the RESET light is on.

C33 and R33 provide input current limiting. CR33 clamps negative transients in excess of 9.6 V to protect FET Q34. The gate to drain junction of Q34 gives clamping for positive-going overloads. The high frequency signal path goes from the input FET to Q40, an emitter follower. R53 sets the high frequency gain. Q60 drives Q62; CR62 balances out the base-emitter voltage of Q62 and temperature compensates it to keep the standing current in Q62 independent of temperature. Q62 current drives the output for positive signal swings. Q60 also drives Q70, which pulls the output negative through R69 and serves as reverse termination at high frequencies. CR64 and CR65 work as expanders for high amplitude signals. R55 and C55 are high frequency adjustments which affect the first five nanoseconds of the transient response. L56 and L71 are integral parts of the circuit board providing high frequency peaking. Q50 is a low impedance drive for the low frequency feedback path.

Low frequency feedback is accomplished by U48, which compares the voltage levels at the base of Q40 and the output, J70. C46 matches the time constant of C77 and R75 with the time constant of R42 and parallel combination of C46 and C47. C48 sets the bandwidth of U48.

50 Ω OVERLOAD PROTECTION

In the 50 Ω mode, K1 is closed by U80, which routes the signal to the 50 Ω attenuator. 50 Ω input protection is provided by an RMS detecting circuit in U80. R84 and R107 attenuate the input signal 100X for U80. C86, C87, and R87 integrate a signal proportional to the RMS value of the signal at pin 3 of U80. When an overload is detected, K1 is de-energized, removing the signal from the 50 Ω attenuator section and applying it to the input of the 1 megohm buffer amplifier. U80 also lights DS96, the RESET light. To reset, S125B is switched to the 1 megohm position, causing the scope to be in the 1 megohm mode. Return to the 50 Ω mode is then accomplished by pushing S125B (50 Ω/1 megohm mode switch) again.

VERTICAL PREAMPLIFIER

CH 2 is identical to CH 1 except that CH 2 has a polarity switch. Only CH 2 will be described here. The CH 2 signal is received from the CH 2 attenuator through J300. Diode bridge CR301, CR302, CR303, and CR304 protects the input from large signals that occur too fast for the input protection relay to react. T305 is a balun, providing a push-pull signal to U310 at high frequencies. The 50 Ω input termination consists of R308, R305, and R309. R308 is adjusted to give 50 Ω DC resistance at input connector J1. CH 2 offset control R306 adjusts the voltage at the input connector J1 to zero in the absence of an input signal. Either R310 or R312 is selected by the POLARITY switch S310, allowing the variable control to be balanced in both invert and normal modes. The output leads of U310 (pins 5, 6, 8, and 9) are crossed over so that the polarity of the signal can be inverted. R90, the variable control, and the resistor network R317, R319, R325, R326, R327, and R328 determine the ratio of currents in pin 11 and pin 12, hence the ratio of currents in transistors connected to pins 6 and 8 to the current in transistors connected to pins 5 and 9. Varying this ratio controls the gain of U310[1]. At all sensitivities other than 5 mV/div, pins 11 and 12 of U350 are shorted together by S95. Thus half the signal current in U350 is lost through R367 and R368. In 5 mV/div, S95 contacts open, causing all of the signal current to flow in the transistors connected to pins 5 and 9, doubling the gain

[1] Gilbert, Barrie, A New Wide-Band Amplifier Technique, IEEE Journal of Solid Stete Circuits, Vol SC-3 number 4, December, 1968, P353.

of U350. Other S95 contacts (shown on schematic 4) close to maintain the voltage at outer collectors pins 5 and 9 of U350. R355, R356, and R357 are low frequency (thermal) transient response compensations. The CH 2 gain control R358 is used to allow the CH 2 gain control (front-panel) to be centered in its range.

SIGNAL CHANNEL SWITCH

Signal from U350 is connected to pins 13 and 1 of U430 and exits U430 at pins 16 and 14. The signal then continues on to and is terminated by the trigger channel switch U530, diminished slightly in bandwidth by the energy extracted by U430.

A push-pull position control signal is injected between U430 and U530 through R376 and R386.

If no current flows through Q436, pin 12 is 0.3 V higher than pin 11 and U430 is on. Under this condition, the amplified signal leaves pins 5 and 9 on 100 Ω EC board transmission lines, joins with the signal from channel 1 and enters the A Ext Trigger relay K410 on 50 Ω EC board transmission lines.

Instruments without the A Ext Trigger option contain jumper wires in place of the relay. The A Ext Trigger signal is injected by the relay at this location, which is considered to be the interface between the preamplifier and the main vertical amplifier. A RLC network consisting of C407, L409, R407, etc. provides some boost to compensate for delay line losses at high frequencies.

The signal next passes into the delay line DL410 which delays the vertical signal 75 ns so that the sweep may start before presentation of the triggering signal.

INTERNAL TRIGGER AMPLIFIER

Signals looped through U430 continue to trigger channel switch U530 and are terminated in R528 and R529 which are the collector loads for U350. If no current flows in Q538, voltage divider R534 and R535 holds pin 12 of U530 above pin 11 and the CH 2 trigger signal amplified in U530 appears between pins 5 and 9 of U530. Trigger channel switch U530 is turned off when Q538 conducts 4 mA, pulling pin 12 down to 9.8 V (0.3 V below pin 11). Signal current in this case is shorted out by the connection between pins 6 and 8. In either case, the total current in U530 is unchanged so that the voltage on pins 5 and 9 of U510 remains unchanged at +12 V.

Q544 and Q546 provide small additional gain for the trigger signal. RT551 temperature compensates the gain of stages U310 through Q564. Q552 and Q556 select the bandwidth of the trigger signal.

In the full bandwidth mode Q556 is on and Q552 is off. Filter L559, R559, R557, and C557 provides a constant impedance at all frequencies as the collector load of Q556 and thus full bandwidth. In the 20 MHz mode Q552 is on, Q556 is off, and high frequencies are attenuated by C557. Since the bandwidth filter in the vertical amplifier is a two-pole filter, the 3 dB point of the trigger's single pole filter is slightly less than 20 MHz. The low frequency phase shift of the two filters is identical, however, so that phase match may occur in X-Y operation of the scope.

Signals at the collector of Q556 are buffered by emitter follower Q564 and sent to A and B trigger amplifiers via J568 and J566 respectively. CR562 matches the base emitter junction of Q564, and R560 is adjusted so that the zero signal voltage at Q564's emitter is zero. R562 pulls away the collector current of Q556 or Q552.

Q572 and Q576 buffer the trigger signal, which becomes the X signal in X-Y mode. C572 is part of the filter which matches the delay of the vertical delay line DL410.

Trace Separation

Trace separation circuitry injects a positioning signal at the main vertical interface during the operation of B sweep in the ALTernate sweep mode.

Q440, Q456, Q444, and Q454 provide the push-pull trace separation signal through R440 and R456. R458 and C458 ensure that the output impedance of the trace separation circuitry is 100 Ω at all frequencies.

MAIN VERTICAL AMPLIFIER

The signal received from delay line DL410 is terminated and T coil peaked by the inductance of pins 1, 13, 14, and 16 of U620. The required additional inductance L621 and L625 is achieved in the leads to pins 16 and 14 which are lengths of run on the etched circuit board. This inductance plus C621 and C625, made from 3 layers of etched circuit board, and R621 and R625 form the forward termination of the delay line. The same method of termination and peaking is used in each stage using the 151-0078 integrated circuit.[2] The network attached to pins 2 and 3 of U620, provides delay line and thermal transient response compensation. The gain of the main vertical amplifier is adjusted by R629. Vertical amplifier gain is temperature-compensated by RT644.

[2] **Addis, John "Three Technologies On One Chip Make A Broadband Amplifier", Electronics, June 5, 1972, Pg. 103.**

The network connected between U650 and U660 is the bandwidth limiter network. The network provides a constant impedance of 50 Ω per side at all frequencies looking from pins 4 and 10 of U660. In the full bandwidth mode, signal from pins 5 and 9 of U650 loops through U660 and is terminated in the bandwidth limit network. In the 20 MHz mode, the signal is obtained from pins 6 and 8 of U650. In passing through the bandwidth limit network signals above 20 MHz are attenuated at 12 dB/octave.

U660 is an FT doubler configuration with the input T coil peaked. Bias for the inner set of bases is set by R672 and R673. The output transistors are high voltage devices which drive the CRT's distributed deflection structure.

In the event of a loss of a CRT termination resistor, the long tail current through R657 pulls pins 2, 8, and 3 of U660 down. When the +27 V supply goes below 25 V, Q686 turns on, turning on Q688 which shorts the 25 V supply. The loss of the +25 V supply will shut down the power supply inverter. See inverter current limiting.

SCALE FACTOR READOUT

Scale factor readout control circuitry is in U80. With a 1X probe or with an non-readout coded connector connected to the input connector code ring surrounding J1, pin 11 of U80 is connected to +5 V through R81. The voltage at pin 11 is sensed by U80 and pin 10 is pulled down, lighting the X1 light emitting diode (LED), CR99. 11 kΩ to ground from the code ring shuts off CR99, and turns on CR98, the X10 LED. A 6.8 kΩ from the code ring to ground will shut off the X10 LED and light CR97, the X100 LED. A short circuit on the code ring provides trace ID which pulls down pin 7 of U80, shifts the trace upward one-fourth of a division, and shuts off the scale factor light. The trace ID signal goes to R289 on CH 1 and R389 on CH 2 to provide trace shift in the vertical pre-amplifiers.

VERTICAL MODE CONTROL

U1535B controls the vertical logic (diagram 3) via two control leads from pins 8 and 9. These leads also are connected via Q1590 and Q1594 to the trigger logic (diagram 4) when the trigger is NORM. The trigger logic is independent of U1535B when CH 1 or CH 2 triggers are called up.

U1535B is controlled by the mode switch in CH 1, CH 2, ADD, or X-Y. In the ALT or CHOP mode, the IC's control the input to pin 7 of U1535B to cause it to either alternate on command from A GATE or to CHOP. When the HORIZ is in ALT, and the vertical in ALT, U1535B changes state only every other A GATE. Note that A GATE is the signal that activates U1535 in ALT and the signal from U1530B pin 6 only allows every other A GATE through. U1535A output is A GATE 2, and U1535B is A GATE 4.

In the CHOP mode, U1585 is on and U1535B changes state every time U1585 makes an output. While U1585 is making an output a signal from U1585 pin 4 blanks to prevent displaying the switching from CH 1 and CH 2 and back.

Z AXIS

U1560 output drives the Z AXIS amplifier. U1560 is controlled by the A and B GATES, the A-B control via pin 15, the INTENsity controls and the EXT Z AXIS.

The circuit consisting of Q1566 and Q1568 disconnects the B INTENSITY control during X-Y or when A=1, 2, or 5 ns.

A TRIGGER AMPLIFIER

The Source Switch SW700 selects one of the four modes which the 485 will trigger on: INT, LINE, EXT, or EXT ÷ 10. Signals above approximately 1 MHz, except in HF REJ are coupled through C705. R705 and R709 form a 1 MΩ input resistance and a loss pad to compensate for the loss across C705, matching high frequency and low frequency gains. R708 protects Q712A input by limiting current when CR711 or Q712A is forward biased. Q712A and Q712B form a source follower with the source voltage very close to zero. The source follower drives Q716, an emitter follower, which drives U730. The balun coil T719 produces a differential signal. U730, U738, and U740 are cascode amplifiers. The slope switch SW720, switches the collectors of U740 to give selection of the triggering slope.

A EXT TRIGGER IDENTIFY

The A EXT TRIG IDENTIFY function is driven by the emitters of U730; this allows U830 to be coupled to the trigger signal and the level control. The center line crossing point of the A EXT TRIG signal corresponds to the trigger point of the sweep for timing information.

When the EXT TRIGGER IDENTIFY switch is pushed, U830 is turned on and its collectors are connected to the vertical delay line via relay K410. VR838 and VR839 provide DC level shift.

The cables between J842 and J843 and relay K10 have a time delay so that the EXT trigger signal will be displayed with the same time position as signals arriving through CH 1 or CH 2 input.

A TRIGGER GENERATOR

The trigger amplifier drives a Schmitt Trigger circuit based around CR751 and a constant resistance load. This circuit provides a standardized output pulse that is time related to the trigger event. This standardized pulse and a holdoff signal drive a two tunnel diode circuit to provide stable triggering from DC to at least 350 MHz with very low trigger jitter.

CR762 is the arming tunnel diode and CR772 is the output tunnel diode. After CR762 is fully armed and CR772 is partially armed (at the end of holdoff), a pulse from CR751 causes CR762 to go to its high state. This increases the current through R764 to fully arm CR772, which goes to its high state when the same pulse that fired CR762 is received through the short delay line. The output of CR772 drives differential pair Q792 and Q794. When CR772 is in its high state pin 1 of U780 is high, turning on the light DS781 (TRIG'D). Q792 provides the A GATE through emitter follower Q810. The output of Q794 couples to a differential pair Q802 and Q804, which provide the sweep gates.

When the sweep is completed, a positive signal from A sweep turns on Q816 and Q822 to provide a signal to pin 16 if U780. This initiates the holdoff portion of U780 and pin 17 goes positive. Pin 17 stays positive as determined by timing R's and C's on the timing switch to pin 8. The holdoff signal on pin 17 of U780 drives Q768 and Q778. Q768 and Q778 gate the current to CR762 and CR772. When Q768 and Q778 are off, CR762 and CR772 are receiving the appropriate current as set by R765 (A arming T.D.) and R775 (A output T.D.). When Q768 and Q778 are on they reset CR762 and CR772 to their low states.

In AUTO TRIG pin 19 of U780 is grounded. The trigger signals must recur at least every 50 ms, which is the lowest rate the circuit will provide a triggered sweep in AUTO MODE. The timing of the AUTO MODE is determined by the time constant of R787 and C787.

In SINGLE SWEEP mode +5.5 V is applied to pin 12 of U780. There will be only one sweep for each time U780 is armed by pushing the RESET switch. The sweep will fire when a trigger signal is received while or after the RESET switch is depressed. The READY light on pin 11 of U780 indicates when the sweep is armed.

B TRIGGER GENERATOR

Is similar to A Trigger Generator except it has RUNS AFTER DELAY TIME mode that disconnects the trigger amplifier. In addition, it uses A Trigger Gate and delay pickoff gate as hold-off.

In the triggerable mode, the B Trigger Generator triggers only after receiving both the delay pickoff and A Gate signals. Delay pickoff gate drives comparator Q1092 and Q1096. Both A Gate and delay pickoff gate are required to drive Q1082. The output of Q1074 provides arming current for CR1062 and CR1104. When the triggering signal causes CR1052 to go to its high state, CR1062 is properly armed, and will fire arming CR1104, which fires approximately 1.5 ns after CR1062.

In B RUNS AFTER DELAY TIME mode, the trigger amplifier is turned off via R1038 and enough current is flowing in the base of Q1068 so that it is in saturation. This saturation routes enough current to CR1104 to turn it on when A Gate and delay pickoff gate arrive.

In both cases when CR1104 goes to its high state, comparator Q1106 and Q1110 changes state giving a B GATE out thru Q1114. Q1106 is connected to comparator Q1121 and Q1124 which changes state, giving plus and minus sweep gate out.

In A 1, 2, and 5 ns, B is in B RUNS AFTER DELAY TIME. In addition in 1 and 2 ns the voltage to which C1121 charges is varied by the HORIZONTAL POSITION control. This gives a time position to these two sweep speeds when using the HORIZONTAL POSITION control.

A and B SWEEPS

A and B sweep generators each produce, upon receipt of a gate, a negative going sweep of 1.0 V/div of horizontal excursion, starting at +13 V.

In A Sweep, Q884 and Q888 are the miller amplifier. Timing resistors R873 and R1409 to R1422 return to +50 V in calibrated settings. The values of the timing resistors and capacitors C877 to C882, C1404 and C1405, at various sweep speeds may be determined on the Timing Switch and Generator schematics. Q892 compares the sweep output to +13 V and sends the error signal to the miller input via R866 and Q854. Receipt of a + gate at TP851 turns off Q854, allowing the sweep to run. CR867 must not conduct during baseline, so Q866 sinks the higher timing currents. Q934 turns on at the end of the sweep, producing a + going stop pulse that terminates the sweep gate. Q856 and Q858 feed a current to the miller input at the end of the gate to prevent large negative voltages and long recovery times at low timing currents. R863 affects linearity at 10 and 20 ns/div.

The Delay Comparator Q902 enables B Sweep when the sweep voltage becomes less than the voltage on the Delay Time position control, where U910 is a voltage follower.

Q908 disables B Sweep in A HORIZ DISPLAY mode and Q914 introduces an offset at 10 and 20 ns/div. Switch A9 opens when A Sweep speed is 1, 2, or 5 ns/div to start B Sweep with minimum delay, since the B Sweep Generator produces these speeds regardless of the HORIZ DISPLAY mode.

B Sweep generator is similar to A except that the maximum output rate is 5 times faster. The sequence of timing components is different from A Sweep. Q1238 prevents large positive voltages that would occur at the miller input after the end of the sweep but before the end of the gate.

For A Sweep speed settings of 10 ns/div or slower, A HORIZ DISPLAY mode displays A Sweep. B HORIZ DISPLAY mode displays B, ALT, INTEN, and INTEN (A) function. However, when A Sweep speed is set at 1, 2, or 5 ns/div the Horizontal system displays B Sweep which has been gated on by A trigger. Switch A9 is open so that the Delay Time Position control is effectively set to zero. At A = 5 ns/div, the displayed B Sweep is positioned horizontally in the amplifier. At A = 1 or 2 ns/div, the POSITION control is disconnected from the Horizontal Amplifier via switches B19 and B20. The POSITION control is connected to a variable delay circuit Q1102 which time-positions B Gate for about 30 ns after A Gate.

HORIZONTAL AMPLIFIER

The A sweep or B sweep may be selected by saturating Q1312 or Q1318 respectively. This is done by the horizontal control logic level at N4. If N4 is below –5 V, Q1336 is off and Q1338 saturates. This allows the node R1313, R1314 to go up and turns off Q1318 and saturates Q1312. The output of A sweep generator has been selected. Q1338 being saturated also shunts to ground any signal from B sweep generator that might be present in ALTernate mode. If N4 is –3 V, B sweep is selected as Q1336 saturates, turning off Q1338 and pulling down on R1314, saturating Q1318 and turning Q1312 off. CR1311 will shunt any signal from A sweep.

A +1 V at N4 will turn Q1342 on which turns off Q1358, disconnecting A and B sweeps and saturating Q1356, selecting the X signal for X-Y.

In A = 1, 2, or 5 ns, B18 closes and Q1331 turns on, saturating Q1322, a 2X magnifier. To provide offset to enable viewing at sweep start, in 5 ns B22 closes and offset through R1327 is provided. In 1 and 2 ns, the base of Q1328 is moved and a current from Q1328 through Q1331 and the base collector of Q1332 is inserted to provide offset.

Q1362 and Q1364 compose a HI gain amplifier. The feedback R is R1364 and R1366. The input resistance in B sweep is R1321 and R1322. If A sweep is selected the input resistance is R1307 and R1308.

By selecting B sweep and adjusting R1366, the horizontal gain is set. Then by selecting A sweep and adjusting R1308, A sweep may be calibrated. Both adjustments are done in 0.1 ms/div. To get A and B sweep to start at the same point on screen, R1325 (B REGISTER) provides some offset current for positioning B sweep relative to A sweep. This is done in ALT horizontal mode. Q1378 and R1368 provide a constant current for the operational amplifier Q1362, Q1364. Q1366 is saturated in Beam Finder by S600B. This cuts the feedback resistor value by 2/3 and Rf/RI is reduced. C1364 provides linearity control for 1, 2, and 5 ns/div.

Q1372 and Q1374 are a paraphase amplifier to provide a differential signal to the horizontal amplifier. C1372, C1374, R1372, and R1374 provides thermal compensation for Q1372 and Q1374. Since the horizontal is symmetrical, we will deal with one half only. Q1172 provides isolation between the CRT capacitance and the input amplifier Q1154. Q1172 and Q1174 provide the current path to drive the deflection plate. Q1192 is an emitter follower to provide feedback to Q1154. By using active feedback the actual feedback resistance may be lowered without sacrificing gain. This is accomplished by utilizing the impedance of Q1192, emitter to base, and the divider circuit of R1177 and R1178. CR1156 provides a –5 V reference for Q1154 and CR1152. CR1153 limits the voltage swing to keep either half of the horizontal from saturating. This allows the horizontal to be very linear.

HORIZONTAL CONTROL

This circuit is activated by the HORIZ DISPLAY controls. Several output signals are derived; B disable, horizontal control, A-B control autofocus, trace separation and vertical control drive.

The basic circuit consists of U1535A which is controlled by the HORIZ DISPLAY. The HORIZ DISPLAY switch is overridden when B sweep is used in A = 1, 2, or 5 ns or is X-Y. A truth table is shown on the diagram 12.

The main function of U1535 is to provide a HORIZ CONTROL signal to the horizontal B preamplifier. With the X-Y control of Q1520 (which saturates in X-Y), this signal on pin N4 has 3 levels. In the ALT mode, U1535 switches from one state to another each time the A GATE goes negative. U1530C inverts the A GATE to get the positive edge required by U1535A. (It is important to maintain correct timing with the sweep control since switching must

occur during holdoff.) Pin 5 of U1535A alternates from HI to LO and the sweep switches from A to B and back again. When B is called up and pin 5 is HI, the Z AXIS IC will be in the B mode via pin 15 signal and the B intensity control will function and Autofocus control is also provided. Also, the trace separation signal will be LO, causing the trace separation control to function. This is via control of U1530B. All inputs must be HI to get LO outputs, and this only occurs in ALT when B is called up. The output of U1530B also drives the vertical logic when the HORIZ DISPLAY is in ALT. B disable is controlled by A, the X-Y signal, and switch SWA2 (which is closed when A = 1, 2, or 5 ns).

POWER INVERTER/REGULATOR

General

The Power Inverter/Regulator circuit provides the operating power for this instrument from a line voltage source or DC voltage source. This circuit also includes the Line Voltage Selector switch to allow for selection of a 115 V or 230 V nominal operating voltage. Fig. 3-1 shows a block diagram of the Power Inverter/Regulator circuit. A schematic is shown on diagram 14 at the rear of this manual.

Line Filter

The purpose of the Line Filter is to prevent the instrument from injecting power supply frequency interference into the power line, or power-line interference from entering the instrument. L1812 and L1813 provide both common-mode and differential filtering. R1812 and R1813 are damping resistors. C1812 and C1813 are common-mode filters and C1814 is a differential filter. R1811 discharges C1814 when the power switch is off.

Line Input Circuit

Thermal cutout S1802 provides thermal protection for this instrument. If the temperature exceeds a safe operating level, S1802 opens to interrupt the applied power. When the temperature returns to a safe operating level, S1802 automatically closes to re-apply the power.

CR1821 contains the main power rectifiers for the Line Input circuit. C1822 and C1823 are the line-storage capacitors. With S1803 in the 115 V position, the circuit acts as a full-wave voltage doubler so that the voltage across the series combination of C1822 and C1823 will be the peak-to-peak value of the line voltage. In the 230 V position, CR1821 acts as a full-wave bridge rectifier. Therefore the voltage developed across C1822 and C1823 will be approximately the same for either 115 V or 230 V operation.

RT1821 and RT1822 are thermistors which limit the charging currents during turn on. When the POWER switch is turned off, the Line Stop circuit stops the Inverter and C1822 and C1823 discharge thru R1822 and R1823.

WARNING

Because the discharge is slow, dangerous potentials will exist across capacitors C1822, C1823, and other connected components for several minutes after the POWER switch is turned off. The presence of voltage in the circuit is indicated by relaxation oscillator R1824, C1824, and DS1824. Neon bulb DS1824 blinks until the potential drops to approximately 100 V.

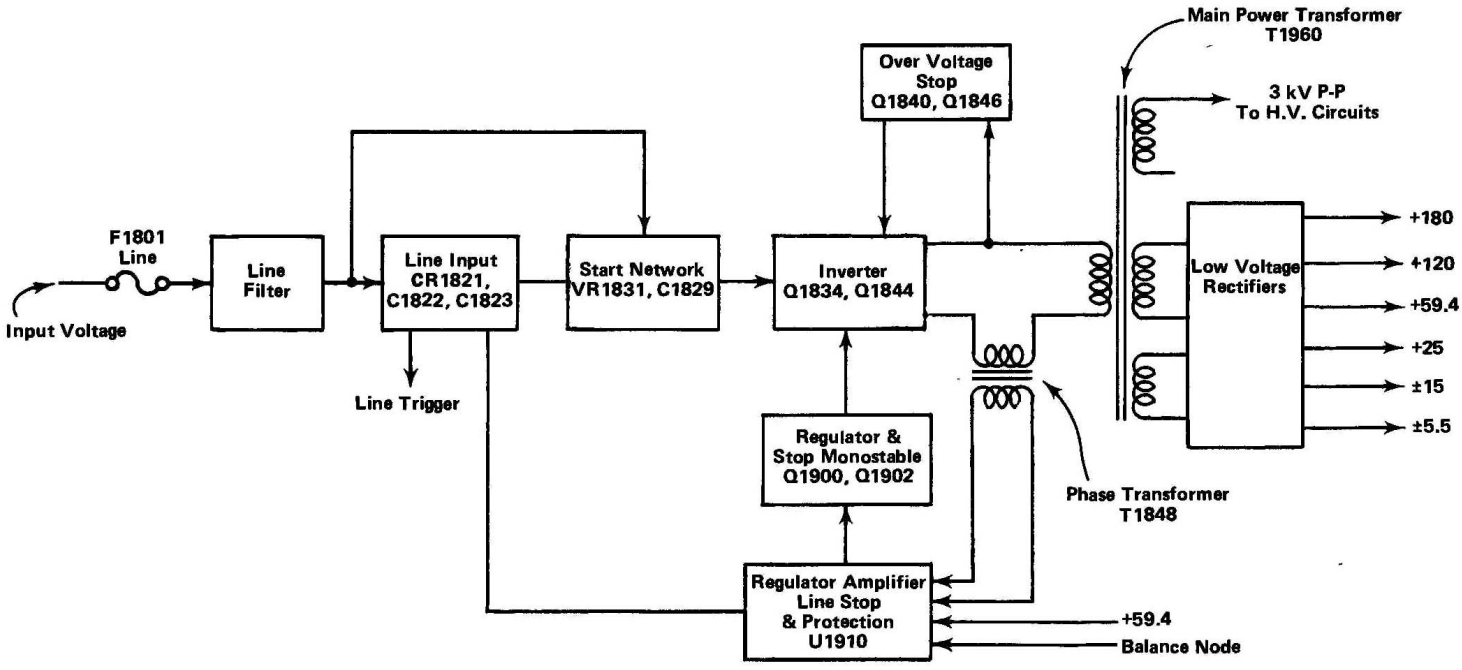

Fig. 3-1. Block diagram of power inverter/regulator circuit.

DS1801 and DS1802 are line voltage transient protectors. With S1803 in the 115 V position, only DS1801 is connected across the line. If a peak voltage surge in excess of approximately 230 V is present on the line, DS1801 will break down and conduct sufficient current to open the line fuse F1801. In the 230 V position, DS1801 and DS1802 are in series across the line to protect against voltage surges exceeding 460 V.

Transformer T1801 provides a sample of the line voltage for triggering at line frequencies. It also provides a signal to the Line Stop circuit to indicate the presence of line voltage at the input to this circuit. T1825, C1825, and C1827 provide common-mode filtering. C1826 and L1825 act as a differential filter.

Start Network

Resistive divider R1828 and R1829 is connected between the input line and the negative side of C1823. When the line voltage goes positive, C1829 charges. At the same time CR1842 conducts, charging C1835, and CR1843 conducts to charge C1848. When the voltage on C1829 reaches approximately 32 V, VR1831 conducts, discharging C1829 thru the base of Q1844. As Q1844 turns on, C1835 discharges thru L1835 to start the Inverter. After operation has begun, CR1842 discharges C1829 with each cycle of the Inverter. This disables the start network.

Inverter

Refer to the simplified schematic shown in Fig. 3-2. Once the Inverter has been started by the Start Network, the Inverter is self-oscillating. Feedback necessary for oscillation is provided by base-drive transformer T1831. The series-resonant circuit, consisting of L1835 and C1835, has a nominal resonant frequency of about 25 kilohertz. To provide regulation of the voltages induced in the secondary circuit, the action of regulator transistor Q1900 varies the frequency of oscillation on the low side of resonance by holding both Q1834 and Q1844 off for a time during each half cycle as determined by the Regulator circuit (see Inverter Regulator for a more detailed discussion of regulation).

Transistors Q1834 and Q1844 are a switching pair, where only one transistor can conduct at a time. The direction of current flow in the feedback winding of T1831 determines which transistor will conduct. Transistors Q1834 and Q1844 change states every half cycle. The switching action provides a square-wave voltage at the emitter of Q1834, which has a peak-to-peak voltage about equal to the DC voltage from the Line Input circuit. This square-wave voltage supplies the drive necessary to maintain oscillation in the resonant circuit. When both Q1834 and Q1844 are being held off by Q1900, resonant circuit current flows through CR1834 or CR1844. The resonant circuit current drives the primary of the power transformer T1960 and thus supplies power to the Secondary circuit.

In normal operation, the sequence of events during one cycle of operation is as follows:

1. Assume the current in the resonant circuit is at 0 ampere and beginning to increase in the direction to cause conduction in CR1834. At the time the current reaches 0 ampere, regulator transistor Q1900 is turned on by the Inverter Control circuit. The Regulator transistor holds both Q1834 and Q1844 off for a controlled amount of time. During this time, resonant circuit current flows through CR1834.

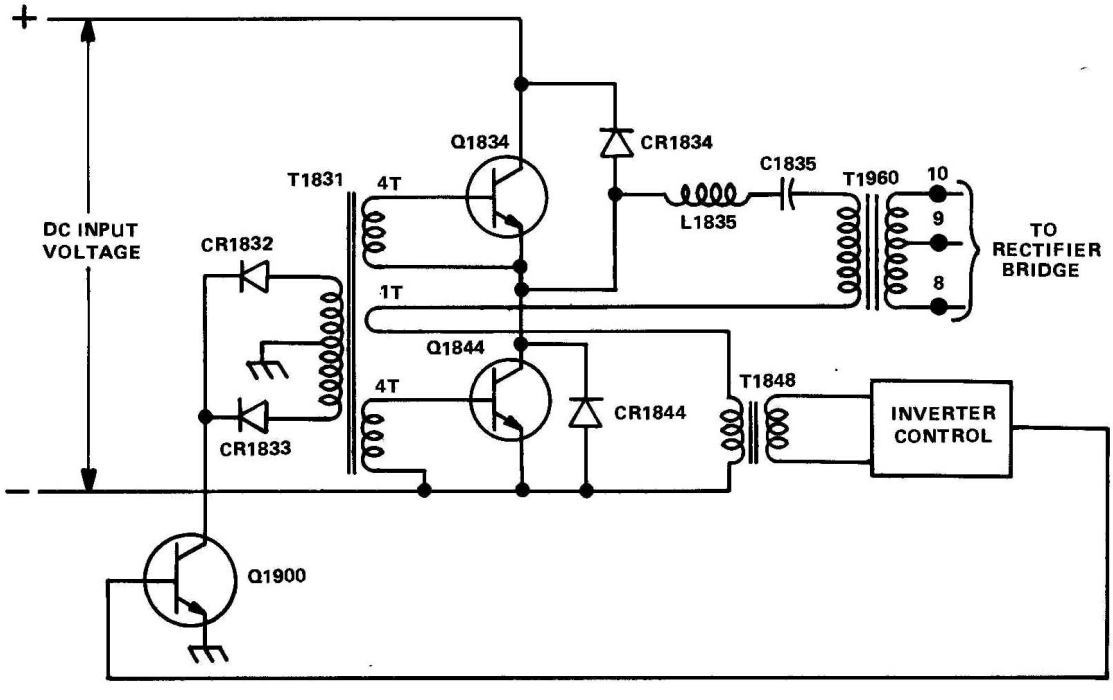

Fig. 3-2. Simplified schematic of inverter.

2. At a controlled time after the resonant circuit current passes through 0 ampere, regulator transistor Q1900 is turned off by the Inverter Control circuit. When Q1900 is turned off, the direction of current flow in the feedback winding T1831 is such that it induces a voltage in the base windings of T1831, which turns on Q1844 and holds off Q1834. Transistor Q1844 conducts while the resonant circuit current builds up to a maximum and falls off toward 0 ampere.

3. When the resonant circuit current reaches 0 ampere and begins to increase in the opposite direction, regulator transistor Q1900 is again turned on by the Inverter Control circuit. This holds both Q1834 and Q1844 off for a controlled amount of time. While Q1900 is on, resonant circuit current flows through CR1844.

4. When Q1900 is turned off by the Inverter Control circuit, the direction of current flow in the feedback winding of T1831 is such that the induced voltage in the base windings of T1831 turns on Q1834 and holds off Q1844. Transistor Q1834 conducts as the resonant circuit current increases to maximum and falls off toward 0 ampere.

5. When the resonant circuit current reaches 0 ampere and begins to increase in the opposite direction the cycle begins to repeat.

Inverter Regulator

The Inverter Regulator circuit schematic is located in diagram 14 at the rear of this manual. The purpose of the Inverter Regulator is to maintain constant voltages at the semi-regulated supply outputs. This is accomplished by varying the inverter frequency. The nominal resonant frequency of L1835 and C1835 is 28 kHz. Regulation is achieved by operating on the low side of resonance, in the range of 20 to 28 kHz. At the lowest line voltage and highest load, the Inverter will operate at a frequency close to resonance. If either the line voltage is increased or the load is reduced, the inverter frequency will decrease.

Power and phase information to the regulator circuit is provided by current transformer T1848. CR1931, CR1932, CR1933, and CR1934, are connected as a bridge rectifier to deliver both positive and negative voltages. The +7.5 V at pin 6 of U1910 is internally shunt regulated. The −2 V at pin 7 is unregulated. VR1945 provides a stable reference for the sensing divider string consisting of R1940, R1941, R1942, and R1944.

U1910 contains the regulator circuit consisting of a voltage amplifier and a variable pulse width monostable multivibrator. Pin 15 (normally near ground potential) is the input to the voltage amplifier. The charging ramp of the monostable is available at pin 12. Inputs that trigger the start of the monostable appear at pins 10 and 11. The output at pin 9 drives the regulator transistor Q1900. Circuit operation is as follows: In the stable state of the multivibrator, pin 9 will be near ground, holding Q1900 off. As the inverter current goes thru zero, either pin 10 or pin 11 will go positive depending on polarity. This positive pulse sets the multivibrator into its unstable state. During the unstable state, pin 9 will be positive holding Q1900 on. The duration of the unstable state is determined by the voltage sensed at pin 15. If the voltage is low, the duration will be short. As the voltage increases, the duration becomes longer.

The monostable pulse width controls the inverter frequency by the fact that when Q1900 is on, both Q1834 and Q1844 are off. Power delivered to T1960 varies with inverter frequency because the impedance of the series resonant circuit L1835 and C1835 varies with frequency.

Inverter Current Limiting Circuit

U1910 also contains the Inverter Current Limiting circuit. Circuit operation is similar to voltage regulation except that the pulse width of the multivibrator is varied so that the inverter current never exceeds a safe level. The current limit circuit takes over control of the multivibrator during the turn on surge or whenever an overload on a semi-regulated supply causes the inverter current to reach the limit value. R1926 is the current sensing resistor. Voltage at TP1926 will be the negative rectified inverter current to a scale of approximately 0.7 V/ampere. The current sense input at pin 13 will normally be held positive by R1922. During current limit, the negative voltage at TP1926 pulls pin 13 toward ground. Multivibrator pulse width then increases until the current limits at a value which holds pin 13 near ground. If the circuit remains in current limit for more than approximately 30 ms, pin 8 will go positive, tripping the stop monostable, which stops the Inverter. (See protection circuit description.)

Overvoltage Stop Circuit

Q1840 and Q1846 provide a circuit to stop the Inverter whenever the voltage across the primary of T1960 exceeds a safe level. This circuit will be active whenever the connector between the Inverter and power board is removed or the normal regulating path thru Q1900 and T1831 is inoperative. CR1848 charges C1848 to the peak of the voltages across T1960. If this voltage exceeds a safe level, VR1846 will conduct turning on Q1846. C1848 will then discharge thru R1846 into the base of Q1840. When Q1840 is on, Q1844 will be held off stopping the Inverter. The Inverter cannot restart until CR1843 has charged C1848 to the breakdown voltage of VR1831.

Line Stop Circuit and Surge Limiting

The Line Stop Circuit stops the Inverter when the POWER switch is turned off or the AC line voltage falls below a minimum value. This circuit function is necessary to limit the turn-on surge current and thereby protect the POWER switch, Line Fuse, and Line Rectifier Bridge.

When the instrument is first turned on, thermistors RT1821 and RT1822 have a value of approximately

5 ohms. Line current charging C1822 and C1823 is limited by the thermistors. As the instrument continues to operate, the thermistors heat and drop in resistance. When the instrument is turned off, the Line Stop circuit stops the Inverter, leaving C1822 and C1823 charged. The line storage capacitors now discharge through R1822 and R1823 at a rate approximately equal to the thermal recovery of the thermistors. This rate ensures enough thermistor resistance to limit surge current whenever the instrument is turned back on.

A simplified schematic of the Line Stop circuit is shown in Fig. 3-3. Line Trigger transformer T1801 generates a ground referenced Line Frequency signal of approximately 1 V peak-to-peak. This signal is biased to +0.4 V by R1916 and R1917. Under normal operation, C1918 charges toward +7.5 V through R1918 until a positive going signal from T1801 turns Q1 on discharging C1918. This repeats each line cycle. When the POWER switch is turned off, Q1 stays off allowing C1918 to charge. When the voltage at pin 3 of U1910 reaches approximately +0.7 V the inverter control circuit inside U1910 allows pin 8 to go positive, triggering the stop monostable, which stops the Inverter. For trouble-shooting at low line voltage, the line stop circuit may be disabled by grounding the Line Stop test point TP1918. (L.S.).

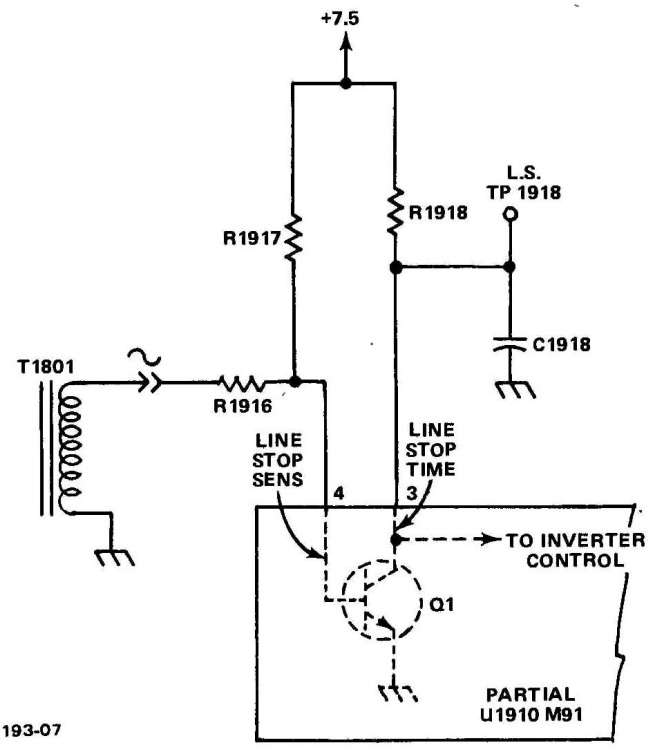

Fig. 3-3. Line stop circuit.

Procedure for Converting the 485 to DC Operation

Read the circuit description entitled Line Stop Circuit and Surge Limiting before proceeding.

1. Set the LINE VOLTAGE SELECTOR switch (rear panel) to 230 V.

2. Check that the DC source voltage range is within 220 V to 350 V DC limits.

3. For DC operation the Line Stop Circuit must be disabled while the instrument is running. Two methods are possible, depending upon the current available from the DC source. The object is to prevent high surge currents, which can occur during hot turn on when the thermistors are low in value and the line storage capacitors are discharged.

a. If the instantaneous current available from the DC source is limited to 30 A or less, connect a jumper from the Line Stop test point (TP1918) to ground. Circuit board holes for this purpose are provided in the rear corner of the power board. This jumper must be removed whenever the instrument is operated on AC.

b. If the DC source is not current limited, an auxiliary switch must be provided to stop the 485 Inverter BEFORE the power is turned off. Stopping the Inverter will prevent rapid discharge of the line storage capacitors. A schematic showing the auxiliary switch is shown in Fig. 3-4A. When operating with the auxiliary switch, always move the switch to the off position BEFORE turning off the power. When turning the instrument on, move the auxiliary switch to the on position BEFORE turning the power on.

4. Check polarity of the power source. The line side (black) must be connected to the positive. The neutral side (white) must be connected to the negative. The safety ground must be connected to earth potential. Proper polarity at the 485 plug is shown in Fig. 3-4B.

LOW VOLTAGE SUPPLIES

± 15 V Supply

The plus and minus 15 V supplies are generated by the same winding on T1960. The center tap (pin 9) is connected to ground. The voltage at pins 8 and 10 is a square wave, swinging positive and negative with a peak value of 15.7 V and a risetime of approximately 2 μs. Each supply is rectified full wave and filtered with a pi section filter.

±5.5 V Supply

The plus and minus 5.5 V supplies are identical to the 15 V supplies except the transformer voltage is 6.2 V peak.

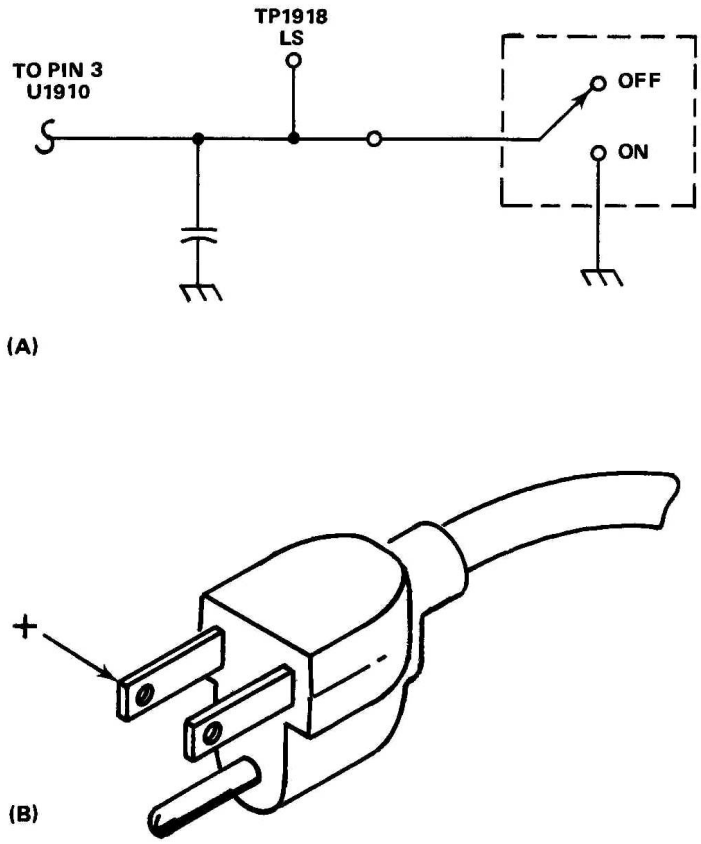

Fig. 3-4. (A) Schematic showing auxiliary switch for disabling line stop circuit, (B) power plug polarity for DC operation.

+59.4 V and +120 V Supplies

The 59.4 and 120 V supplies are similar to the 15 V supplies except for the output connection, which ties the negative rectified voltage to ground. This elevates the transformer center tap to the peak AC voltage on one side of the winding, which is 59.4 V. The 120 V supply is generated by the full rectified voltage on the transformer.

+180 V Supply

The 180 V supply is formed by a voltage doubler which rectifies the 59.4 V peak AC swing and adds it on the 120 V supply.

+25 V Supply

The 25 V supply is formed by a voltage doubler, which rectifies the 12.4 V AC peak-to-peak swing on the 5.5 V winding and adds it on to the 15 V supply.

+50 V Supply

The 50 V supply is regulated from 59.4 V by Q2046. A temperature-compensated reference is provided by VR2042. The reference voltage is compared to a sample of the 50 V output at U2042 which acts as an inverting amplifier. If the +50 V goes negative, the output of U2042 goes positive. CR2042 is short circuit protection for U2042.

+9 V Supply

The 9 V supply is re-regulated from the +15 V supply by Q2056. A 9 V reference is provided by a divider from the +50 V supply. U2052 is an inverting amplifier which drives Q2056 directly.

+5 V Supply

The +5 V supply is essentially identical to the +9 V supply except for the value of the output voltage.

−9 V and −5 V Supplies

The −9 V and −5 V supplies are essentially identical to +9 V and +5 V supplies except that the driving amplifiers are ground referenced.

POWER SUPPLY PROTECTION CIRCUIT

The power supply protection circuit provides fault protection for the inverter, low voltage, and high voltage power circuits. Fig. 3-5 shows a simplified block diagram of the protection circuit. A schematic of this circuit is shown on diagram 14 at the rear of this manual.

Power supply protection is accomplished by operating the Inverter in a pulse mode. When a fault is present, the Inverter will come on for a short period of time, then shut off for a longer period of time. The cycle repeats until the fault is removed. Approximate timing of the duty cycle is shown in Fig. 3-6.

Stop Monostable

Q1900 and Q1902 form a monostable multivibrator which acts to stop the Inverter when a fault is detected by U1910. During the start period T1831 supplies current to charge C1901 and C1904 thru CR1901 and CR1904. At the same time T1848 supplies power to U1910. As U1910 becomes active, pin 8 acts as a current sink, holding Q1902 off. Pin 8 of U1910 will remain at ground during the start period and sampling period. If a fault exists at the end of the sampling period, pin 8 of U1910 stops conducting, allowing Q1901 and Q1902 to turn on. When these transistors turn on, the voltage on all secondaries of T1831 will go to zero, stopping the Inverter. Once triggered on, the stop monostable will stay on while C1901 discharges through R1902 into the base of Q1902. If U1910 is removed from its socket or is otherwise nonfunctional, the stop monostable will stop the Inverter after the first few cycles of operation. In this mode, the duty cycle will be much shorter because C1901 will not have sufficient time to charge.

Balance Node

The Balance Node provides short circuit protection for all semi-regulated and regulated DC voltages. It also provides over current protection for the H.V. winding of T1960 and beam current protection for the CRT. Pin 2 of U1910 is the input to the voltage balance amplifier. If the voltage at pin 2 of U1910 is more positive than +200 mV or

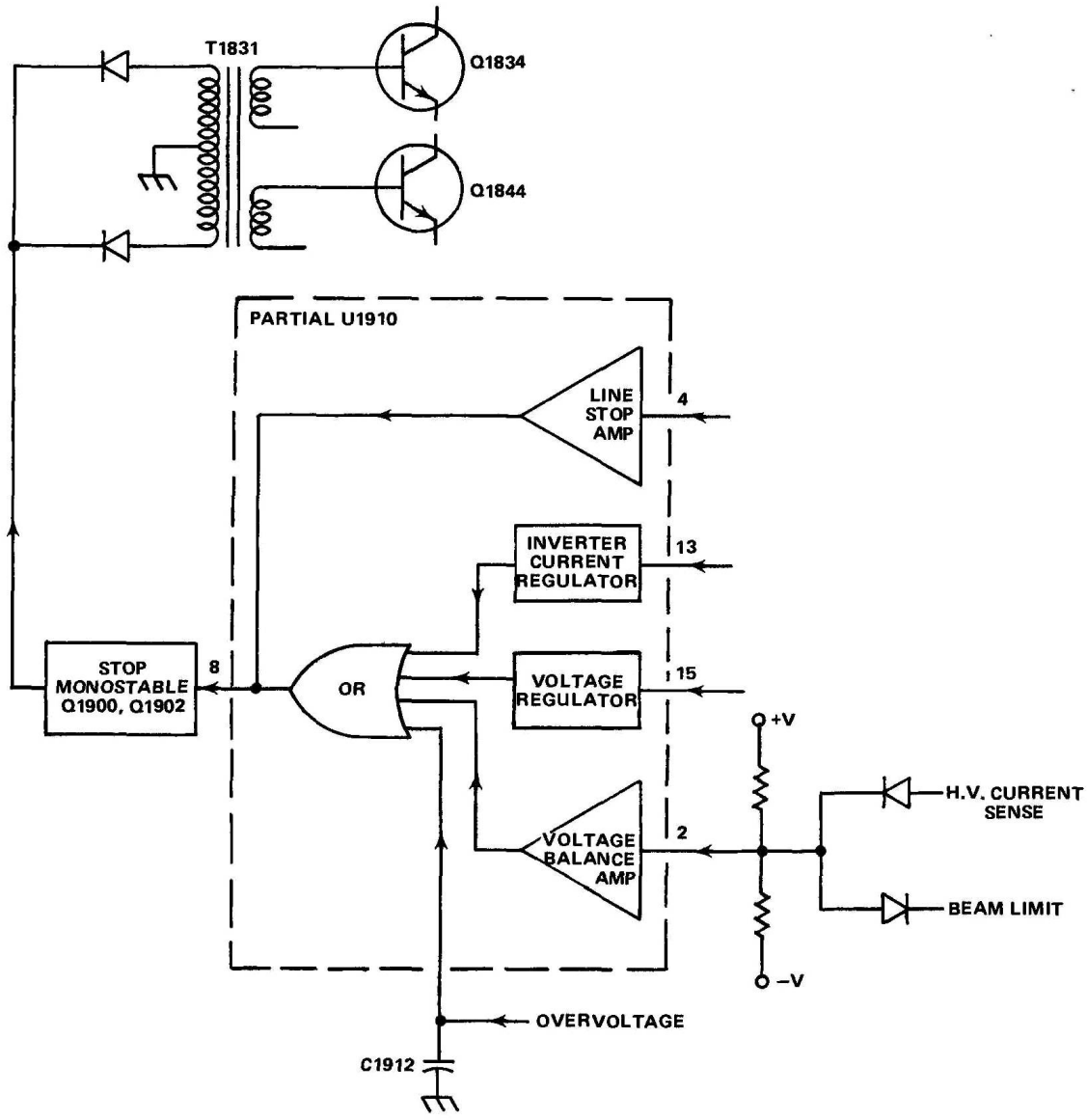

Fig. 3-5. Simplified block diagram of power supply protection circuit.

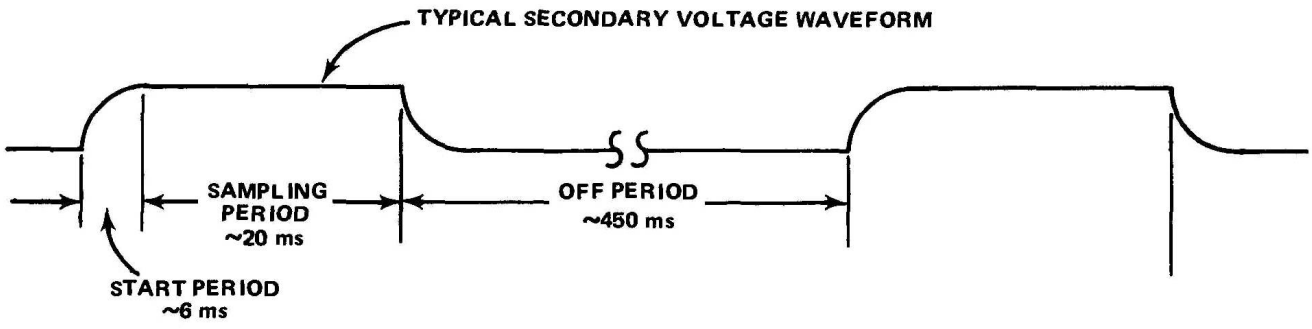

Fig. 3-6. Protection circuit duty cycle.

more negative than —200 mV, the output will generate an error to stop the Inverter. Under normal operating conditions, current from positive supplies to the Balance Node will equal current to the negative supplies, allowing pin 2 to operate near ground, typically within 50 mV. If any supply is shorted the currents will be unbalanced, causing the voltage at pin 2 to shift into the error region. Shorting a positive supply moves the Balance Node negative, and vice versa.

TP1958 (HV) is the high voltage current sense point. Normally the signal at TP1958 does not have sufficient amplitude to cause conduction in CR1958 and therefore has no effect on the Balance Node. If excessive current is drawn from the cathode multiplier or the H.V. winding in T1960, the amplitude at TP1958 will increase causing CR1958 to conduct, producing an error which stops the Inverter. The DC level at TP1953 (LIM) will normally be at +15 V when the intensity controls are off. As the intensity is increased, CRT beam current will increase, causing TP1959 to move toward ground. If TP1959 goes more negative than —.7 V, CR1959 will conduct, causing an error at the Balance Node, which stops the Inverter. This will only occur when the normal beam limit circuit is inoperative.

Overcurrent Protection

Pin 13 of U1910 is the input to the Inverter Current Regulator circuit. If a semi-regulated supply is shorted, the regulator circuit allows the inverter current to increase to the limit value and remain there throughout the sampling period. At the end of the sampling period, pin 8 of U1910 will go positive, stopping the Inverter.

Low Line Voltage Protection

If the line voltage drops significantly below the minimum specified value, the Inverter will not maintain the correct voltages at the semi-regulated supply outputs. When this occurs, an error will be generated by the voltage regulator, which will cause pin 8 of U1910 to go positive, stopping the Inverter. The Line Stop Circuit will also stop the Inverter if the line voltage is low (see Line Stop Circuit Description).

Sampling Period Timer and Overvoltage Protection

When an error is present at the input to the OR circuit, (see Fig. 3-5) a current is generated which charges C1912 thru pin 1 of U1910. The time it takes pin 1 to reach +0.7 V determines the sampling period. When pin 1 reaches +0.7 V, pin 8 of U1910 will go positive, stopping the Inverter. Over-voltage on the +120 V supply will cause VR1912 to conduct, charging C1912 which stops the Inverter.

CRT CIRCUIT

General

The CRT Circuit produces the high voltage potentials and provides the control circuits necessary for the operation of the cathode-ray tube (CRT). This circuit also includes the Z-Axis amplifier and the Auto-Focus amplifier. Fig. 3-7 shows a detailed block diagram of the CRT circuit. A schematic of this circuit is shown on diagram 13 in the rear of this manual.

Filament Voltage

Filament voltage for the CRT heaters is provided by a separate winding on T1960. The filament voltage is elevated to cathode potential through R1687 and decoupled by C1687. Short circuit protection is provided by DS1687.

High Voltage Supplies

A semi-regulated voltage for operation of the high voltage supplies is provided by the high voltage winding of T1960. One end of T1960 is connected to ground through the high voltage current sensing resistor R2094. A 3 kV peak-to-peak square wave is generated and provides the power necessary to operate the Anode Supply, Cathode Supply, and DC Restorer Circuits.

Anode Supply. The Anode Supply consists of 6X multiplier assembly U1600.

Cathode Supply. The CRT cathode voltage (—2950) is generated by a 2X multiplier consisting of CR1601, CR1602, C1601, and C1603. R1611 and C1611 provide high frequency filtering. R1612 and C1612 provide high frequency filtering and an AC coupling path for the cathode regulator.

Cathode Regulator. The cathode regulator maintains the cathode at —2950 V and reduces AC ripple. U1624 is a non-inverting preamplifier and Q1614 and Q1618 form an inverting output amplifier. A DC change at U1624 input sensed by R1624B and R1642C (thick film resistors) starts the regulator action. If the voltage at U1624 input goes positive, the output at TP1614 goes negative. This causes the voltage on C1601 to increase during the positive voltage cycle of T1960. Note that the voltage on C1601 is the difference between the positive voltage on T1960 and the voltage at TP1614.

During the negative half of T1960 voltage cycle, the increased voltage on C1601 increases the voltage at the output of the cathode multiplier, thus correcting the original error. R1633 and C1633 provide a low impedance

coupling path for AC changes to the input of U1624. The output correction is AC coupled through C1612 directly to the cathode. CR1618, CR1621, CR1626, and CR1627 provide short-circuit protection.

Grid DC Restorer. The purpose of the DC restorer circuit is to elevate the output of the Z-Axis amplifier to a potential more negative than the cathode, thereby allowing the grid to control the beam current of the CRT. The circuits are short-circuit protected by R1685, DS1684, and DS1685; R1668, DS1668, and DS1669.

The DC Restorer is current driven from the square wave at the high voltage winding through R1603, R1604, R1605, and R1606. When T1960 goes positive, CR1660 conducts at the grid bias voltage potential. This clamping action establishes the positive swing of the DC Restorer drive. On the negative swing of T1960, CR1663 conducts at the voltage established by the Z-Axis output. This clamping action establishes the negative swing of the DC Restorer drive. The AC swing of the DC Restorer drive is coupled from the low voltage section to the high voltage section by C1663. On the positive swing of the DC Restorer drive, the high voltage end of C1663 is clamped to the cathode voltage by CR1666. During the negative swing of the DC Restorer drive, CR1664 charges C1664 to a voltage more negative than the cathode by an amount equal to the difference between the grid bias setting and the voltage at the output of the Z-Axis amplifier. Fast AC-coupling between the Z-Axis and the CRT grid is provided by C1684. A slower AC path is by way of R1684 and C1664.

Focus DC Restorer. The operation of the Focus DC Restorer circuit is similar to the operation of the Grid DC Restorer. The AC swing of the DC Restorer drive is coupled from the low voltage circuit to the high voltage circuit by C1651. The positive swing will be established when CR1656 clamps at the Focus DC Restorer level voltage. This voltage is approximately 173 V. The negative swing is established when CR1652 clamps at the output voltage of the Auto-Focus amplifier. During the positive swing of the Focus DC Restorer drive, the high voltage end of C1651 is clamped to the focus pot voltage by CR1646. During the negative swing of the Focus DC Restorer drive, CR1651 charges C1652 and thereby establishes the proper level at

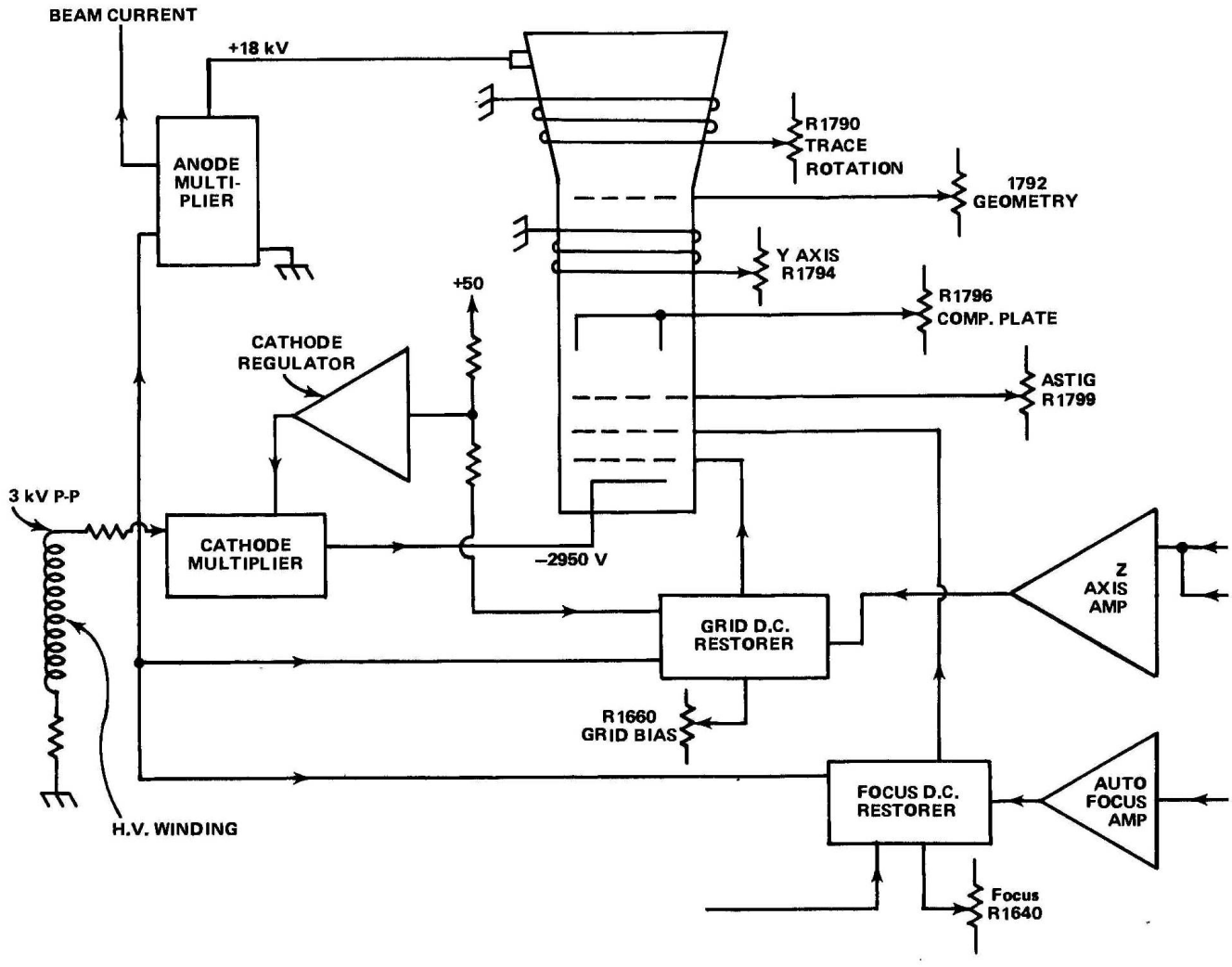

Fig. 3-7. CRT circuit block diagram.

the focus electrode. The focus pot R1640 is set for optimum focus at low intensity level.

Beam Current Limit

The amplifier consisting of Q1544, Q1546, and Q1548 controls the voltage to the INTENSITY and B INTENSITY controls.

For sweep speeds of 50 ms/div and slower and X-Y, the current in resistor R1536, about 5 μA, pulls the base of Q1544 up to about +6 V. All three transistors are saturated. The average beam current of the CRT post-accelerator is available at the low-voltage end of the high voltage multiplier and is also connected to the base of Q1544. When the beam current is zero, the 5 μA current of R1536 flows into the base of the saturated Q1544. When due to high intensity, the average beam current exceeds the 5 μA value, the voltage at Q1544 base decreases at a rate determined by the net discharge current delivered to C1537. As this voltage goes negative, the transistors Q1544, Q1546, and Q1548 come out of saturation, and into the control range, when the input base voltage has dropped to +4 V. In the linear range the three-stage amplifier gain is about −5 V. Input voltages of +4 V and +1 V result in output voltages of −15 V and 0 V respectively.

The positive going voltage at the intensity controls (Q1548C) gives reduced Z-Axis drive and less beam current. In the linear range of the amplifier the output voltage stabilizes at a voltage resulting in the 5 μA average beam current.

The beam current limit becomes 20 μA if the additional 15 μA current of R1534 is not pulled away by closed A1 contact on S1420 (sweep 50 ms/div and slower) or by X-Y switch closure. Diodes CR1532, CR1534, and CR1535 are involved in this switching.

The time response to an overcurrent is in two parts: A delay for the input to charge to a voltage where the output transistor comes out of saturation, followed by a linear response time constant. Initial delay is 10 ms for maximum beam current and increases for smaller over-currents. The linear response time constant is 10 ms.

Power Supply Shutdown Caused by Excessive Beam Current

If, due to some failure, the control loop is unable to keep the average beam current within either the 5 μA or 20 μA limit, the voltage at the amplifier input discharges below the +1 V level. As the voltage reaches about +0.5 V the Q1546 collector voltage is approximately −0.9 V, and operates the power supply shutdown by connection through diode CR1959.

To prevent shutdown being signaled during the first 200 ms of instrument turn-on, C1538 (thru R1538) provides a delay to compensate for charging currents in the CRT post-accelerator supply. Diode CR1533 biases the 15 μA network so that this current is connected to the Q1544 base before it can drop to the +0.5 V shutdown voltage level. Thus, the higher beam current, (approximately 28 μA) is always required to trip shutdown.

In troubleshooting the instrument it may become necessary to disable the beam limit or beam shutdown loops. This can be done by grounding TP1544 at the collector of Q1544.

CRT CONTROL CIRCUITS

The ASTIG adjustment R1799, which is used in conjunction with the FOCUS adjustment R1640 to obtain a well defined display, varies the positive level on the astigmatism grid. Geometry adjustment R1792 varies the positive potential on the mesh to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field around the CRT. Y Axis Align adjustment R1794 controls the current through L1794, which affects the CRT beam after vertical deflection, but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. TRACE ROTATION adjustment R1790 controls current through L1790 and affects both the vertical and horizontal rotation of the beam.

R1796 adjust the voltage on the compensation plates to the average vertical deflection plate structure potential. If this adjustment is not precise, proper focusing can not be achieved by the focus control.

AUTO-FOCUS CIRCUIT

The Auto-Focus circuit provides an output voltage that keeps the display focused for all settings of INTENSITY control. To do this, it amplifies the intensity control voltages in a non-linear fashion and gates the B INTENSITY function.

U1710 provides gating, limiting and part of the shaping of the auto-focus. Gating is of the B INTENSITY current pin 1, by the A-B control function pin 15. In ALTernate sweep operation the A-B control switches from −0.1 V to +0.9 V at the end of A sweep (A display), steering the B INTENSITY current to the output, pin 8. The sweep holdoff time, a minimum of 300 ns, is used for the amplifier that follows to settle to the new focus voltage for

the subsequent A sweep (B display). The first segment of non-linear shaping is done in U1710 by the biasing, which gives no output for an INTENSITY control setting between ground and −3.8 V. No change in Focus voltage is required over this low-intensity range.

The MAX Focus adjustment is used to set the limiting in this stage to coincide with maximum Z limiting. The resistor, pot, and diode network between pin 8 of U1710 and the base of Q1716 serve to provide the last two segment of non-linear shaping and focus gain setting. At the low-intensity condition, the base of Q1716 is at +10 V and CR1710 is conducting. At higher intensity, as current passes into pin 8 of U1710, the voltage drops and CR1710 disconnects as the voltage reaches +8.5 V. When the maximum (limit value) current into pin 8 is reached, this voltage is typically +5 V. The Focus Gain adjustment provides for optimizing the high intensity focus.

The Auto-Focus amplifier provides a stablized voltage gain of about +35 from the Focus Gain control to the output at Q1728 collector. At maximum intensity level, this output voltage can be adjusted from about zero to +70 V and is typically in the +20 V to +50 V range, after proper Focus Gain adjustment.

The network at the base of Q1736 causes its conduction to be proportional to the amplitude and frequency of the Auto-Focus output voltage. This arrangement permits the power transistors Q1728 and Q1732 to operate at a minimum power level consistent with the displacement current output required.

A DC-Restorer network provides for coupling the output of the Auto-Focus amplifier to the focus electrode of the CRT. This consists of four diodes, six capacitors and four resistors including C1651 and C1681. The low-intensity focus is controlled by the high voltage focus pot, which is located for operator adjustment at the rear of the instrument.

CALIBRATOR

Q2106, Q2112, and associated circuitry compose an emitter coupled multivibrator. The frequency of operation, 1 kHz or 1 MHz, is selectable from the front panel by switch S2105. R2109 and R2112 are the current sources for the emitter coupled multivibrator. Accurate 50% duty cycle is obtained by close match of these resistors. R2106 and R2111 are used to protect Q2106 and Q2112 from damage if they are plugged in with power on. C2111 is a speed up capacitor.

Q2114 and Q2124 compose a current mode switch. When Q2124 is on, CR2133 is off and the calibrator voltage (at J2134) is virtually zero. When Q2114 turns on, the current in Q2124 is diverted through Q2114 and the calibrator output voltage is determined solely by the current through R2131 and R2132. R2133 keeps the output impedance at 450 Ω when CR2133 is off. R2124 damps the resonant circuit created by the inductance of CR2133 and the collector capacitance of Q2124. Schottky diodes, CR2124, and CR2133, are used for low capacitance fast switching. CR2124 keeps Q2124 from saturation.

Risetime of the calibrator is less than 1 ns only when terminated in a 50 Ω load. The negative-going edge is not suitable for checking amplifier transient response.

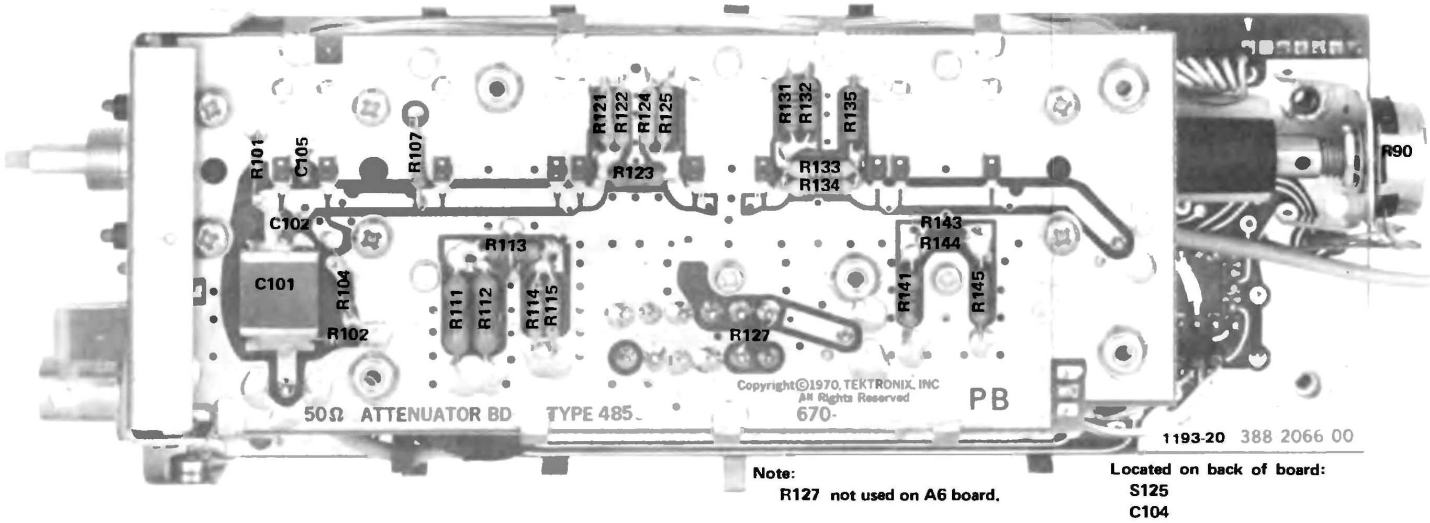

Fig. 8-1. A5 & A6 50 Ω Attenuator board.

FIG. 8-2B

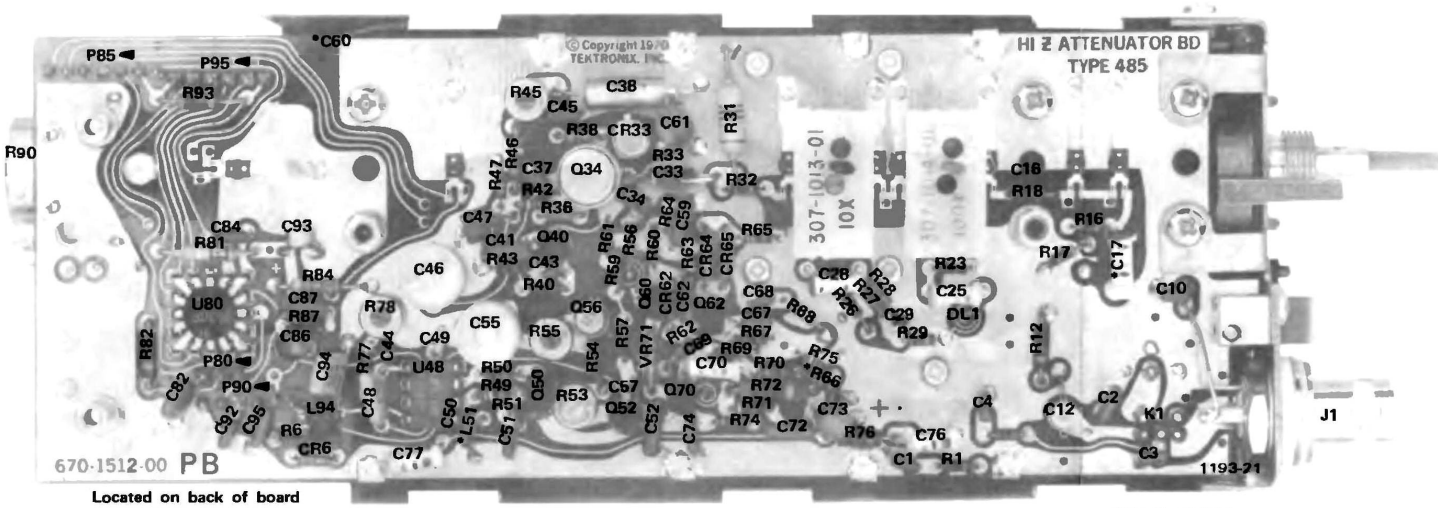

Fig. 8-2A. A3 Hi Z Attenuator board (485 & 485-1 only).

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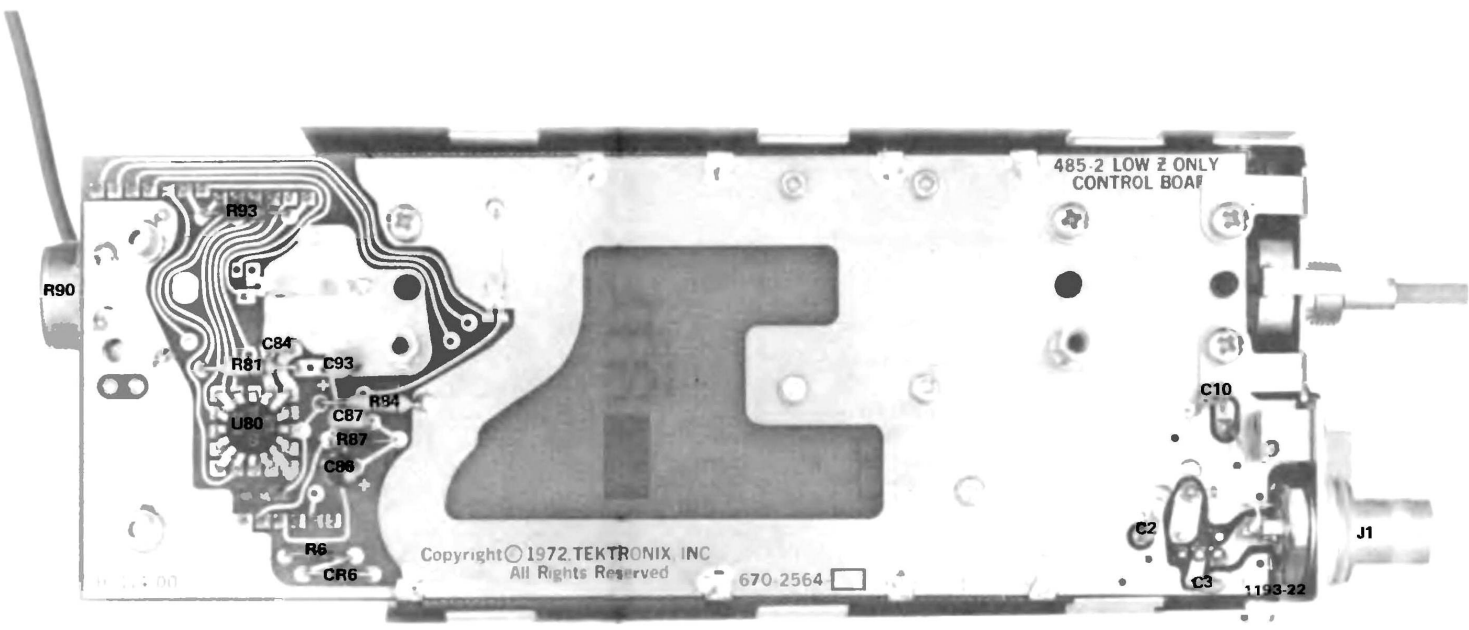
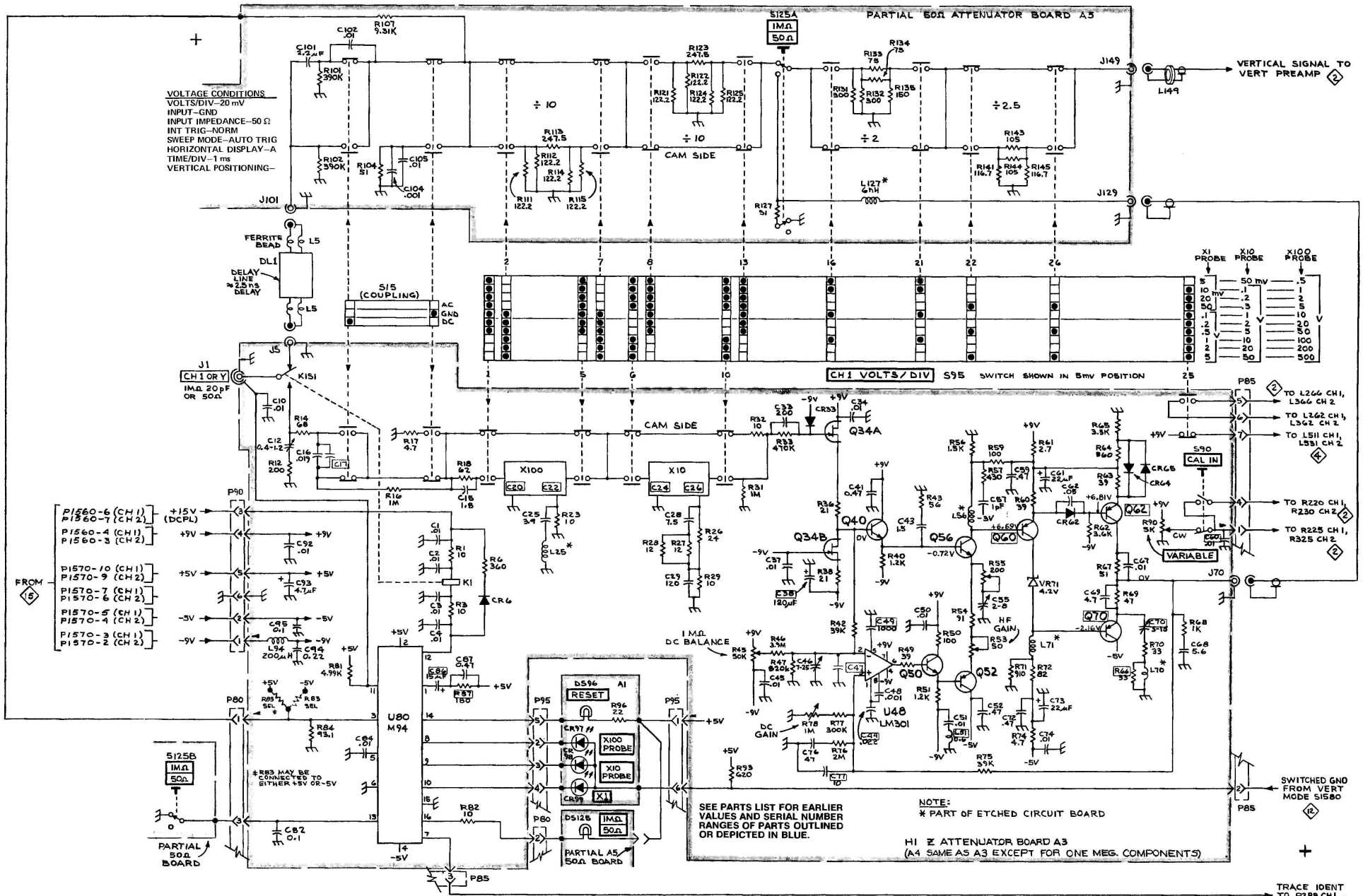


Fig. 8-2B. A4 Low Z Control board (485-2 only).



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CH 1 ATTENUATORS (1)
(CH 2 IDENTICAL)

EKP

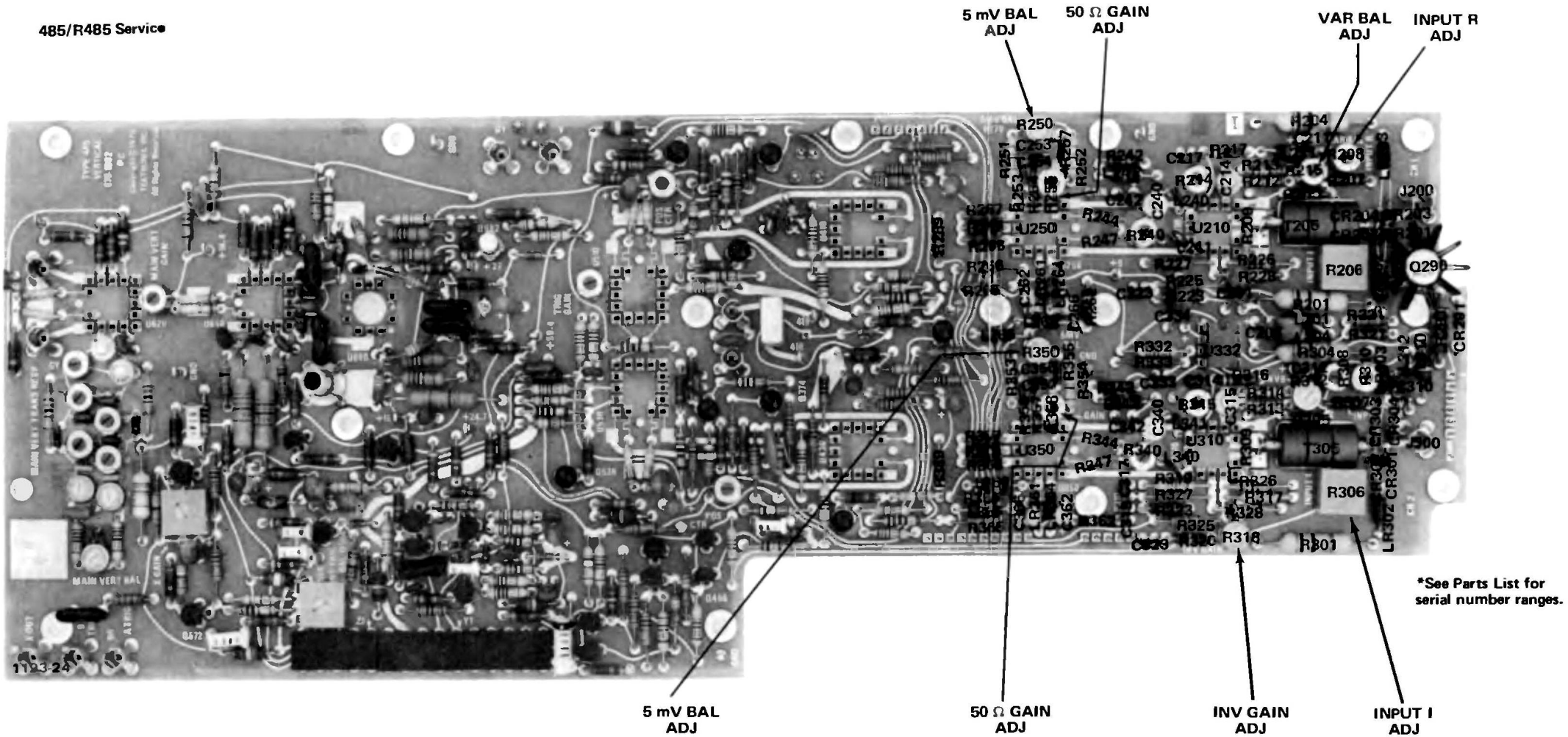
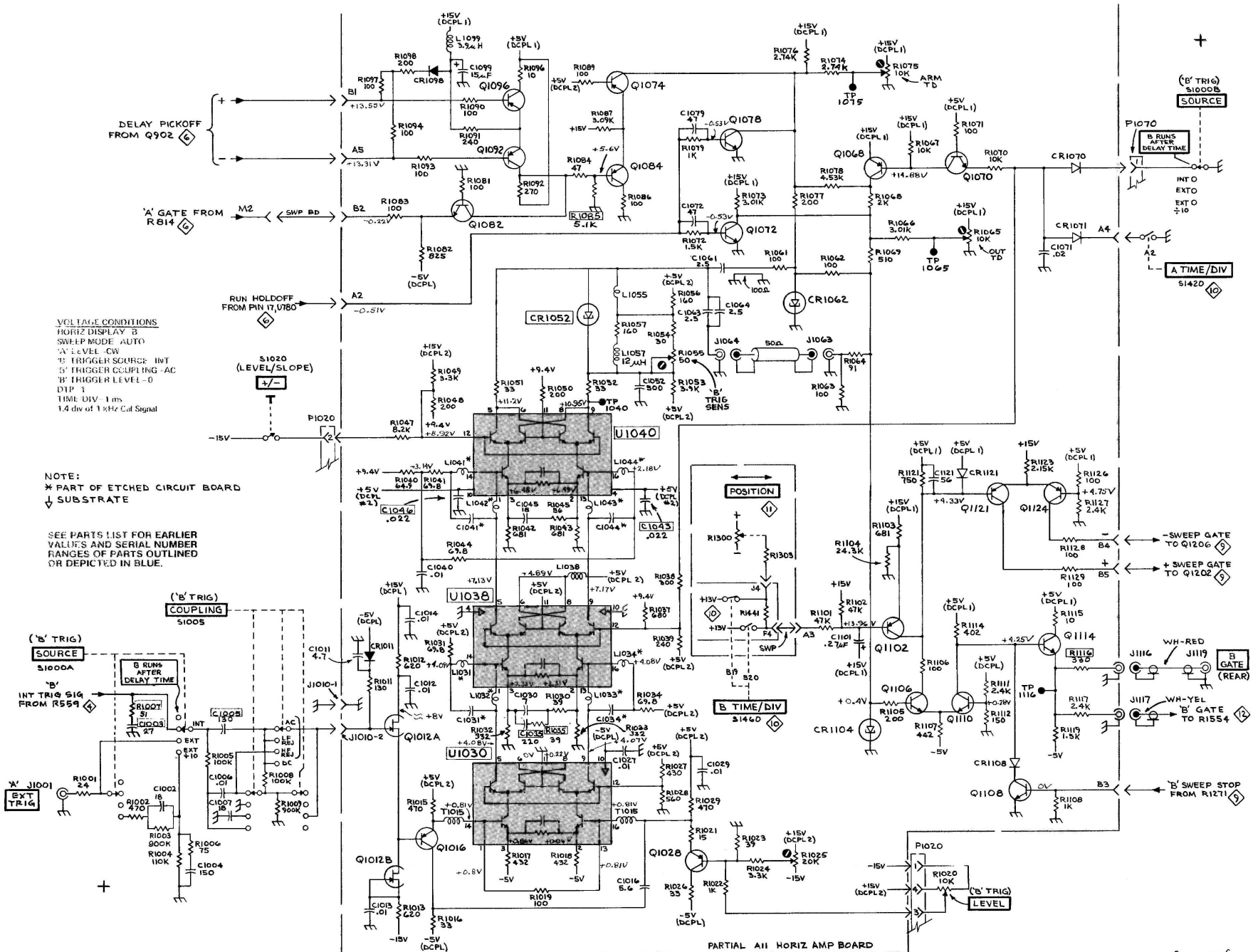


Fig. 8-3. A7 Partial Vertical Amplifier board.



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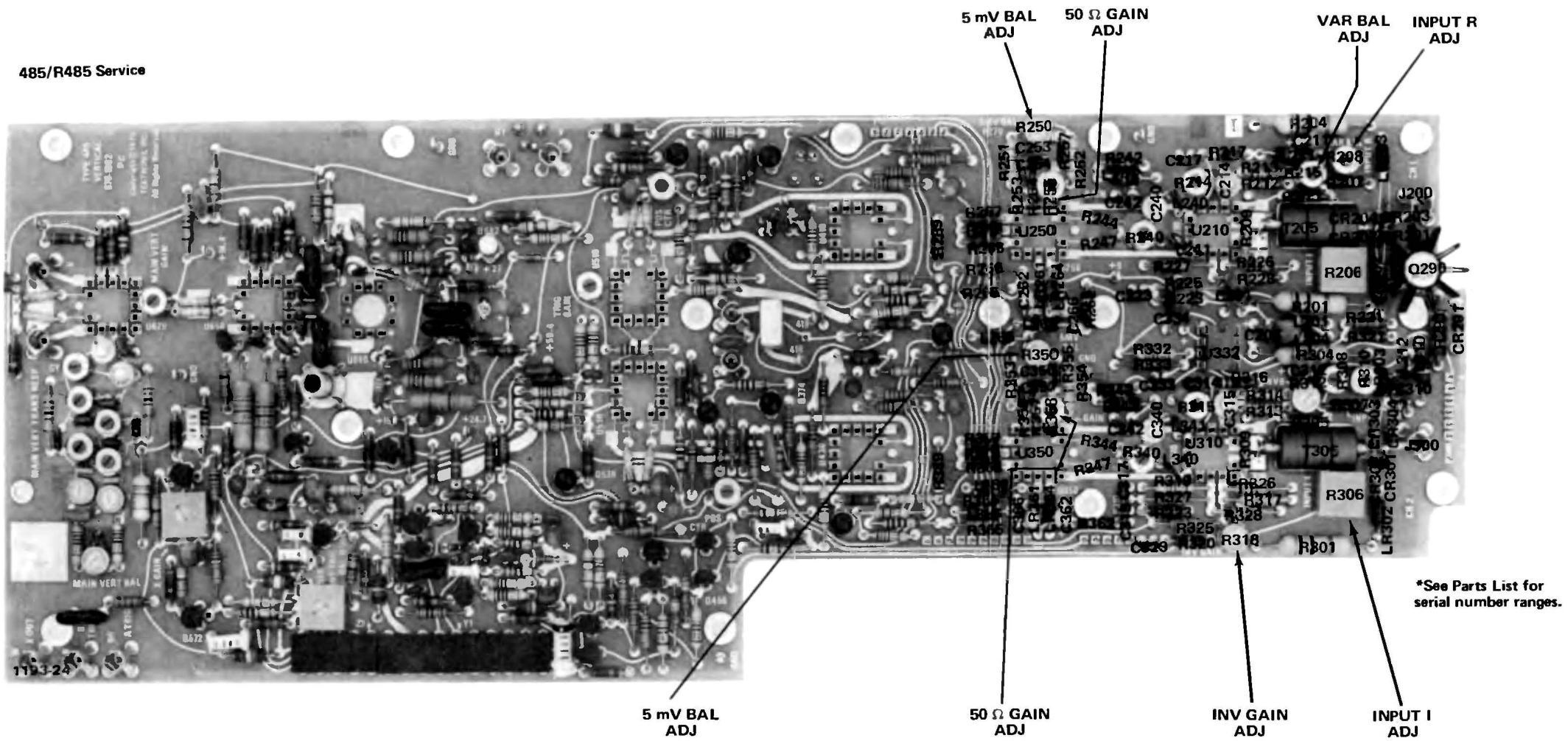
B TRIGGER GENERATOR 8

mgf 773



*See Parts List for serial number ranges.

Fig. 8-3. A7 Partial Vertical Amplifier board.

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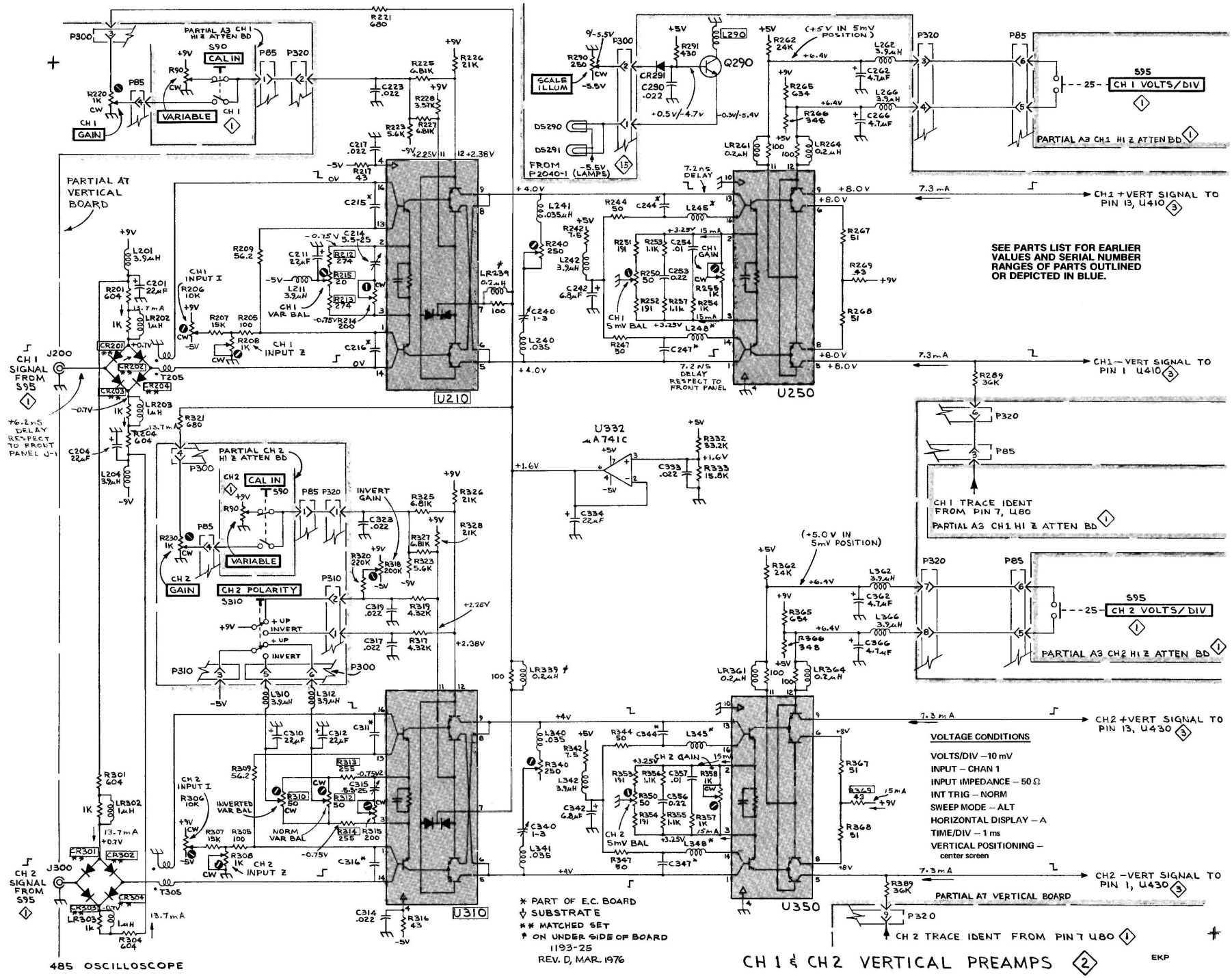
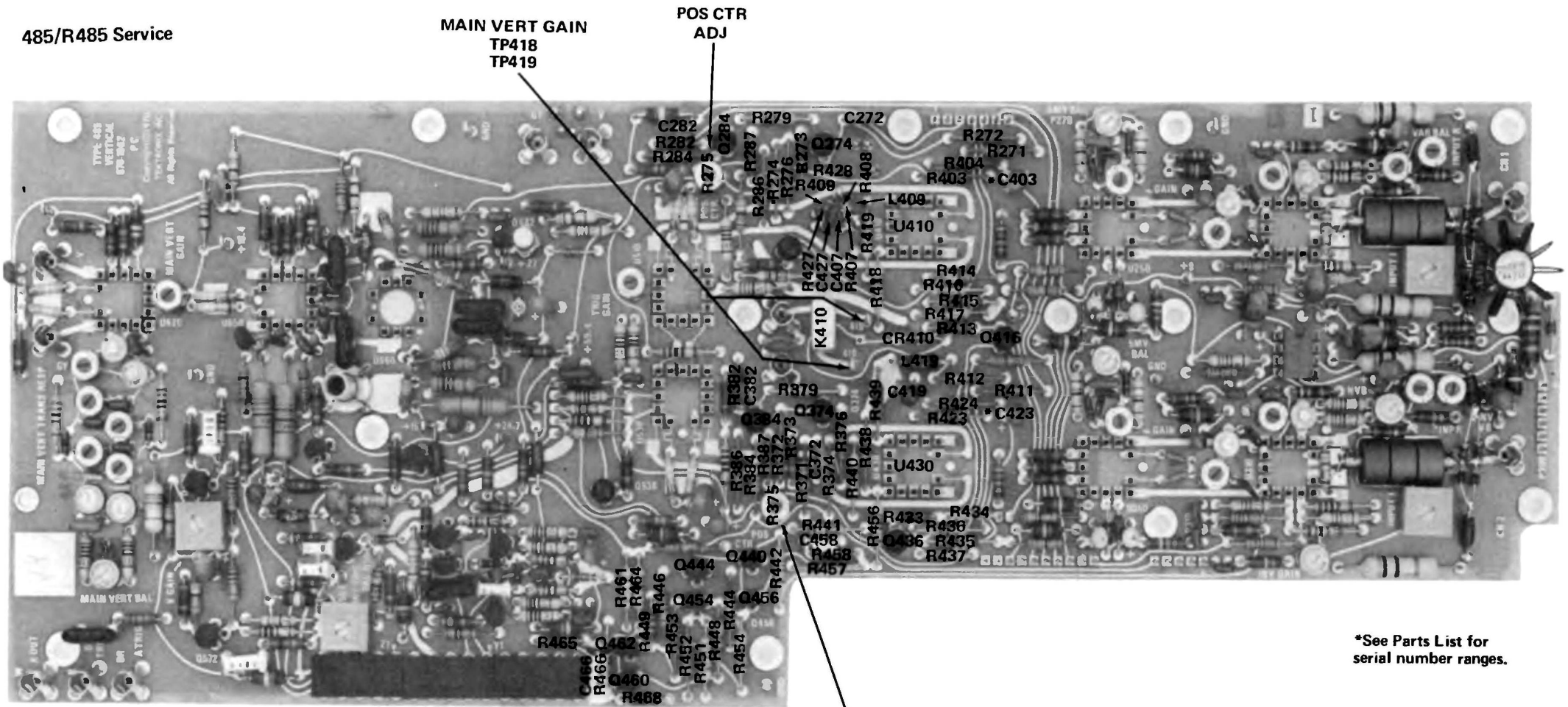
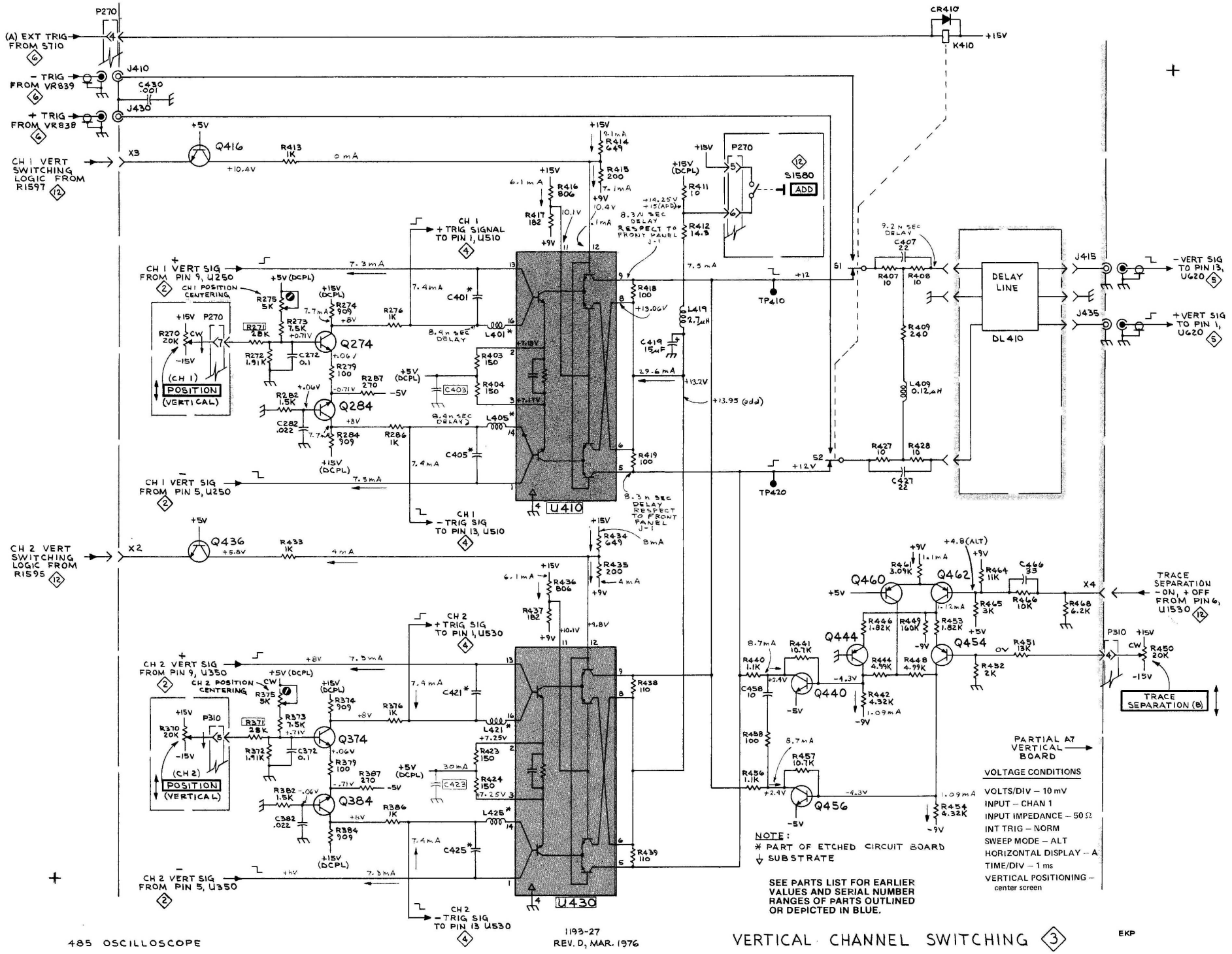

PARTIAL AT VERTICAL BOARD
PARTIAL A3 CH1 HI Z ATTEN BD
PARTIAL A3 CH2 HI Z ATTEN BD
CH1 GAIN
CH1 VARIABLE
CH1 CAL IN
CH1 VOLTS/DIV
CH2 GAIN
CH2 VARIABLE
CH2 CAL IN
CH2 VOLTS/DIV
CH1 INPUT I
CH1 INPUT Z
CH2 INPUT I
CH2 INPUT Z
CH1 VAR BAL
CH1 5mV BAL
CH2 POLARITY
INVERTED VAR BAL
NORM VAR BAL
CH2 5mV BAL
SCALE ILLUM
FROM P2040-1 (LAMPS)
CH1 SIGNAL FROM S95
CH2 SIGNAL FROM S95
CH1 +VERT SIGNAL TO PIN 13, U410
CH1 –VERT SIGNAL TO PIN 1 U410
CH2 +VERT SIGNAL TO PIN 13, U430
CH2 –VERT SIGNAL TO PIN 1, U430
CH1 TRACE IDENT FROM PIN 7, U80
CH2 TRACE IDENT FROM PIN 7 U80
U210
U250
U310
U350
U332
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.
VOLTAGE CONDITIONS
VOLTS/DIV – 10 mV
INPUT – CHAN 1
INPUT IMPEDANCE – 50 Ω
INT TRIG – NORM
SWEEP MODE – ALT
HORIZONTAL DISPLAY – A
TIME/DIV – 1 ms
VERTICAL POSITIONING – center screen
* PART OF E.C. BOARD
⏚ SUBSTRATE
** MATCHED SET
# ON UNDER SIDE OF BOARD
1193-25
REV. D, MAR. 1976
485 OSCILLOSCOPE
CH 1 & CH 2 VERTICAL PREAMPS
EKP



*See Parts List for serial number ranges.

REV. C, SEPT 1974

Fig. 8-4. A7 Partial Vertical amplifier board.



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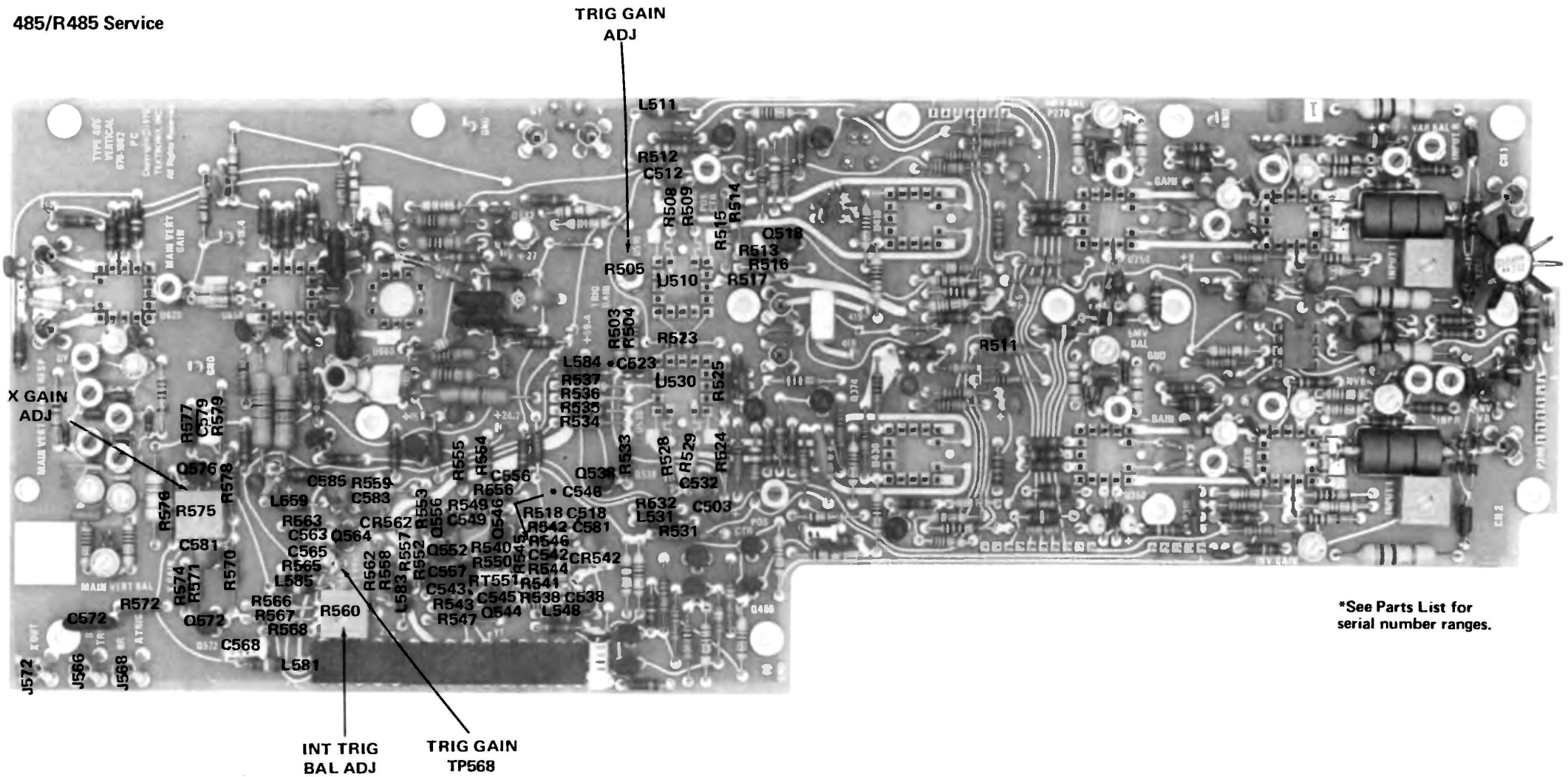
REV. D, MAR. 1976

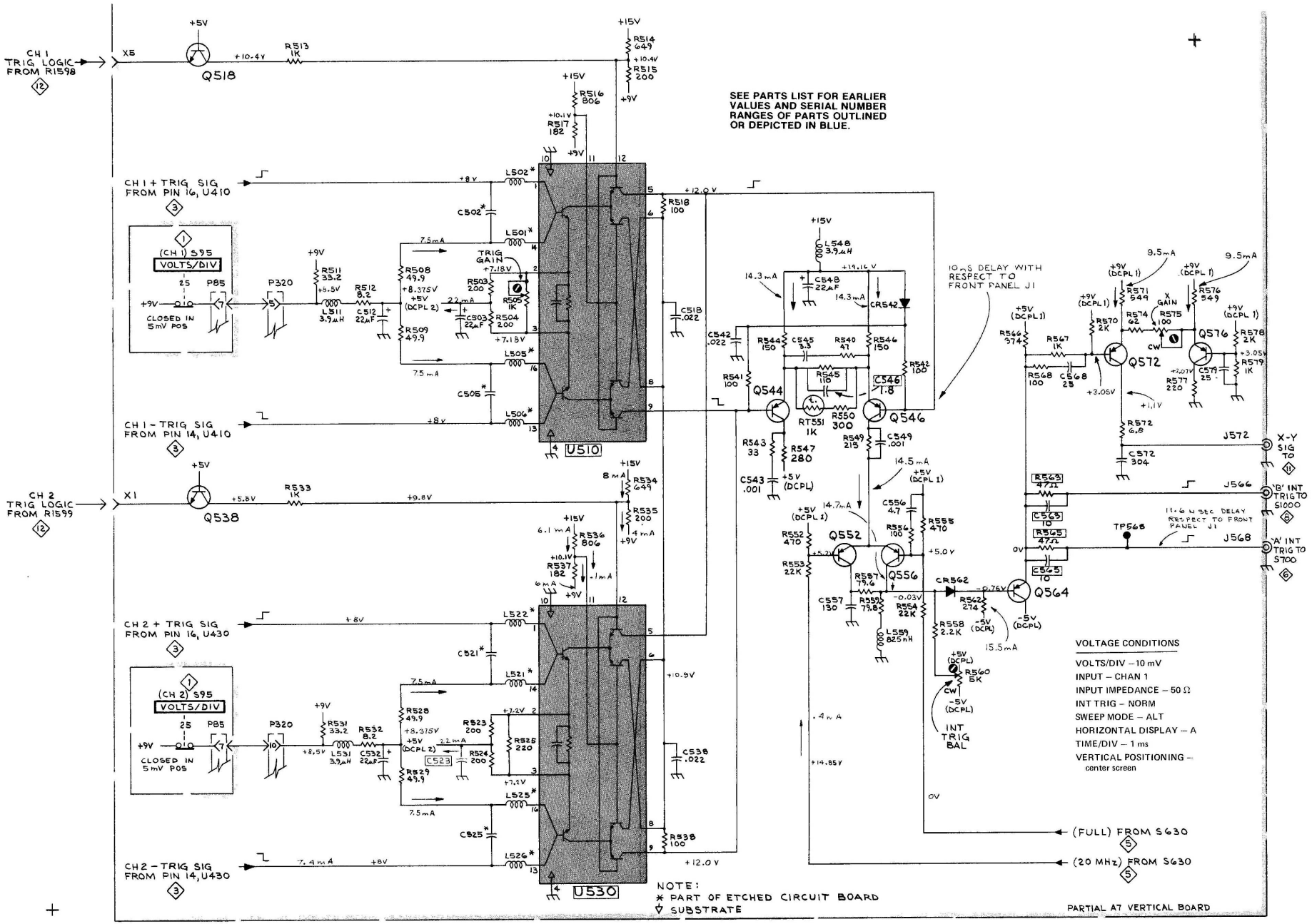
VERTICAL CHANNEL SWITCHING 3

EKP



*See Parts List for serial number ranges.

Fig. 8-5. A7 Partial Vertical amplifier board.


SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.
CH 1 TRIG LOGIC FROM R1598
CH 1 + TRIG SIG FROM PIN 16, U410
CH 1 - TRIG SIG FROM PIN 14, U410
CH 2 TRIG LOGIC FROM R1599
CH 2 + TRIG SIG FROM PIN 14, U430
CH 2 - TRIG SIG FROM PIN 14, U430
(CH 1) S95 VOLTS/DIV
(CH 2) S95 VOLTS/DIV
CLOSED IN 5mV POS
TRIG GAIN
U510
U530
Q518
Q538
Q544
Q546
Q552
Q556
Q564
Q572
Q576
RT551 1K
CR542
CR562
10mS DELAY WITH RESPECT TO FRONT PANEL J1
11.6 mSEC DELAY RESPECT TO FRONT PANEL J1
X GAIN
INT TRIG BAL
J572 X-Y SIG TO J1
J566 'B' INT TRIG TO S1000
J568 'A' INT TRIG TO S700
TP568
VOLTAGE CONDITIONS
VOLTS/DIV – 10 mV
INPUT – CHAN 1
INPUT IMPEDANCE – 50 Ω
INT TRIG – NORM
SWEEP MODE – ALT
HORIZONTAL DISPLAY – A
TIME/DIV – 1 ms
VERTICAL POSITIONING – center screen
(FULL) FROM S630
(20 MHz) FROM S630
NOTE:
* PART OF ETCHED CIRCUIT BOARD
◊ SUBSTRATE
PARTIAL A7 VERTICAL BOARD

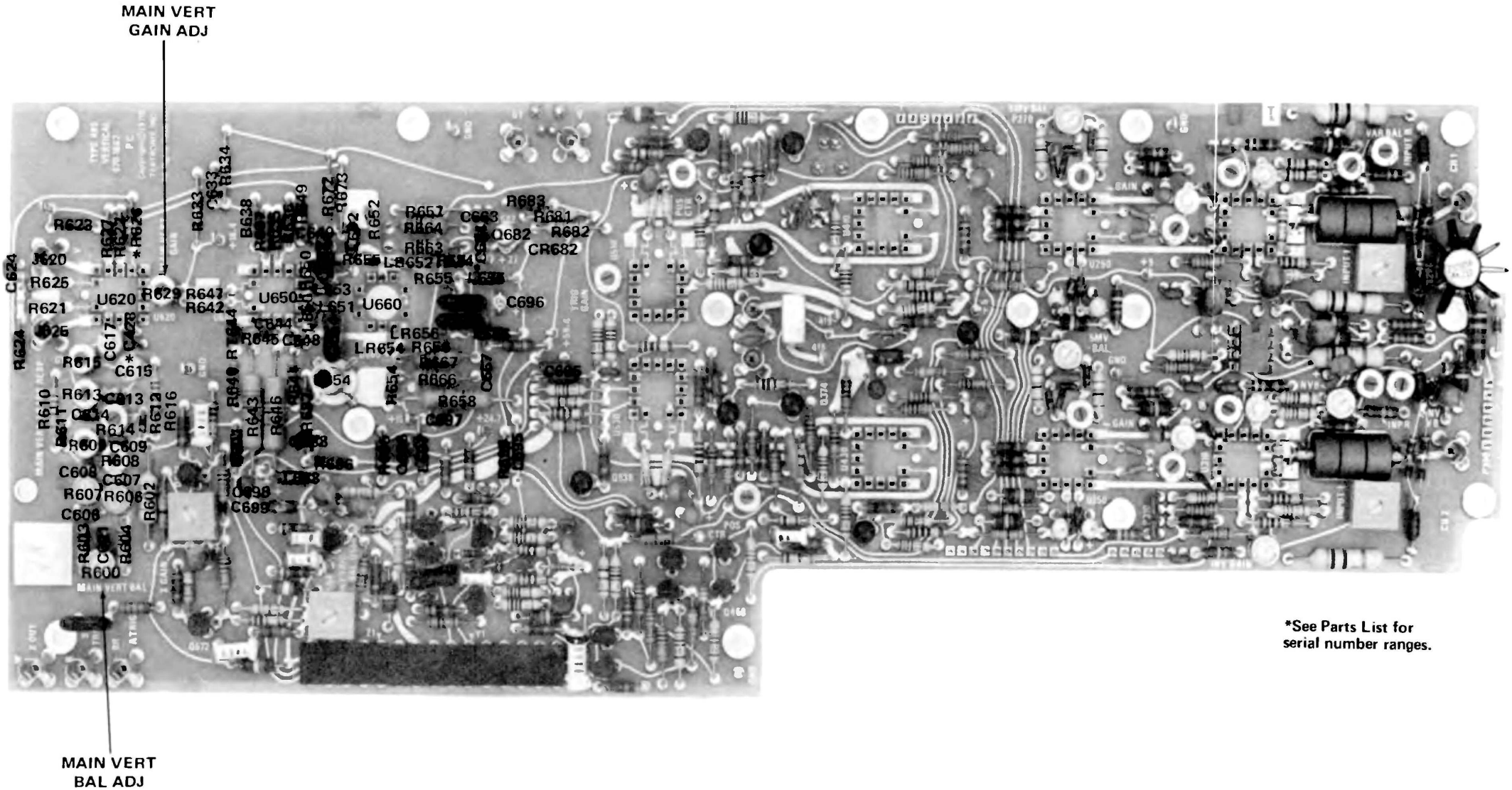
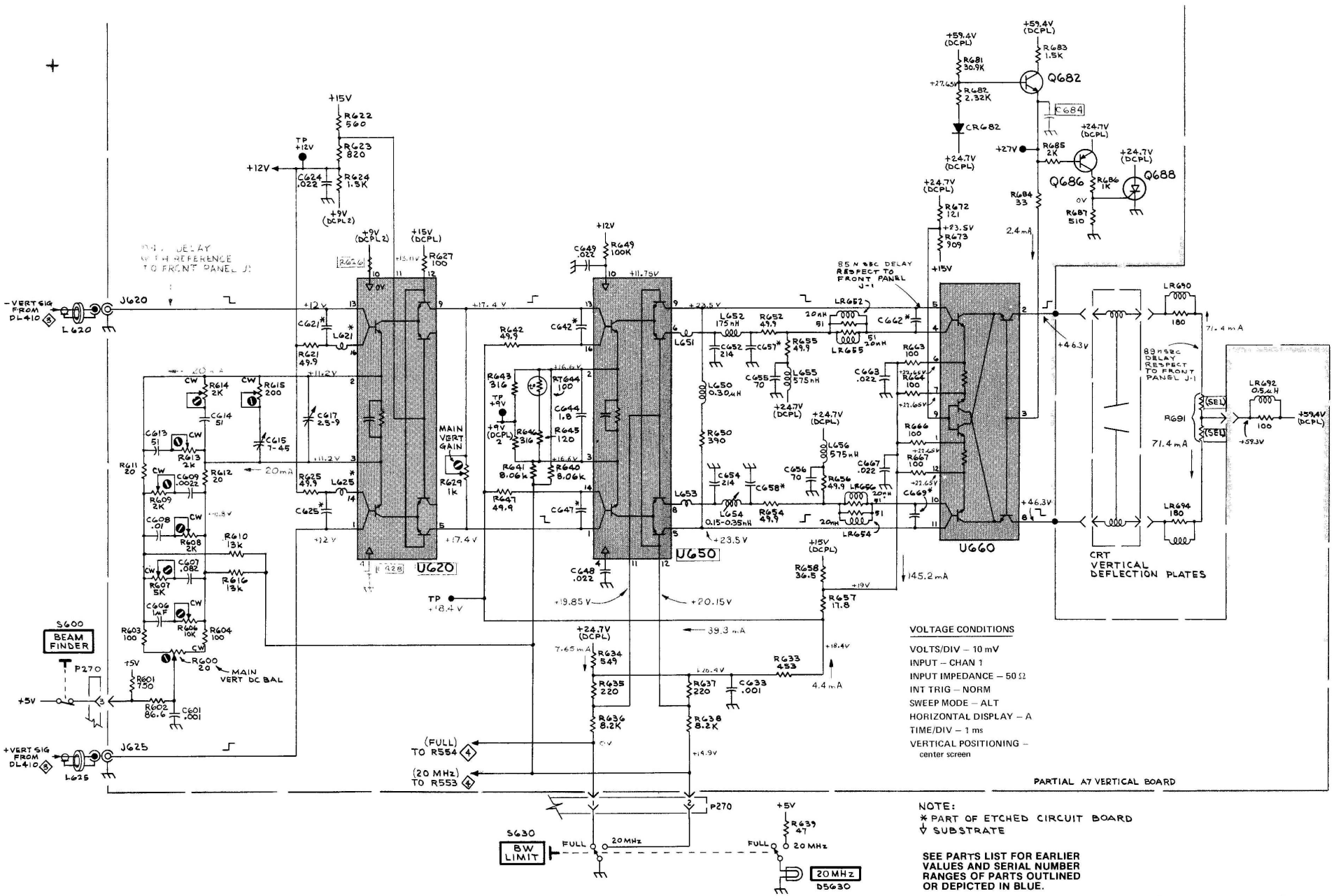


Fig. 8-6. A7 Partial Vertical amplifier board.



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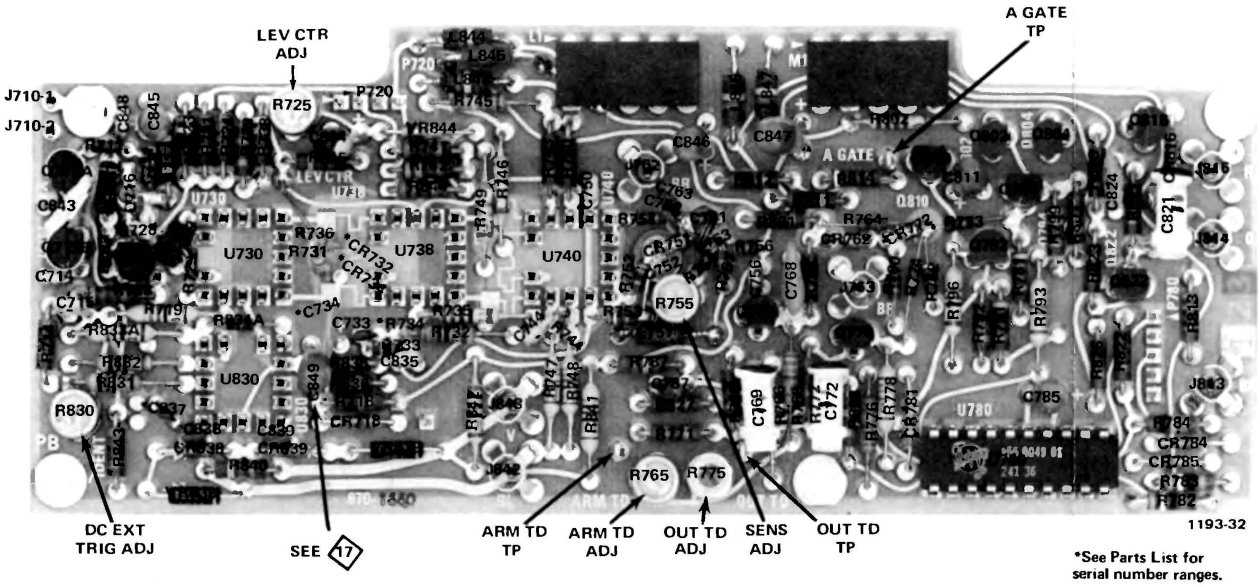
1193-31

VERTICAL AMPLIFIER (5)

mgf
773

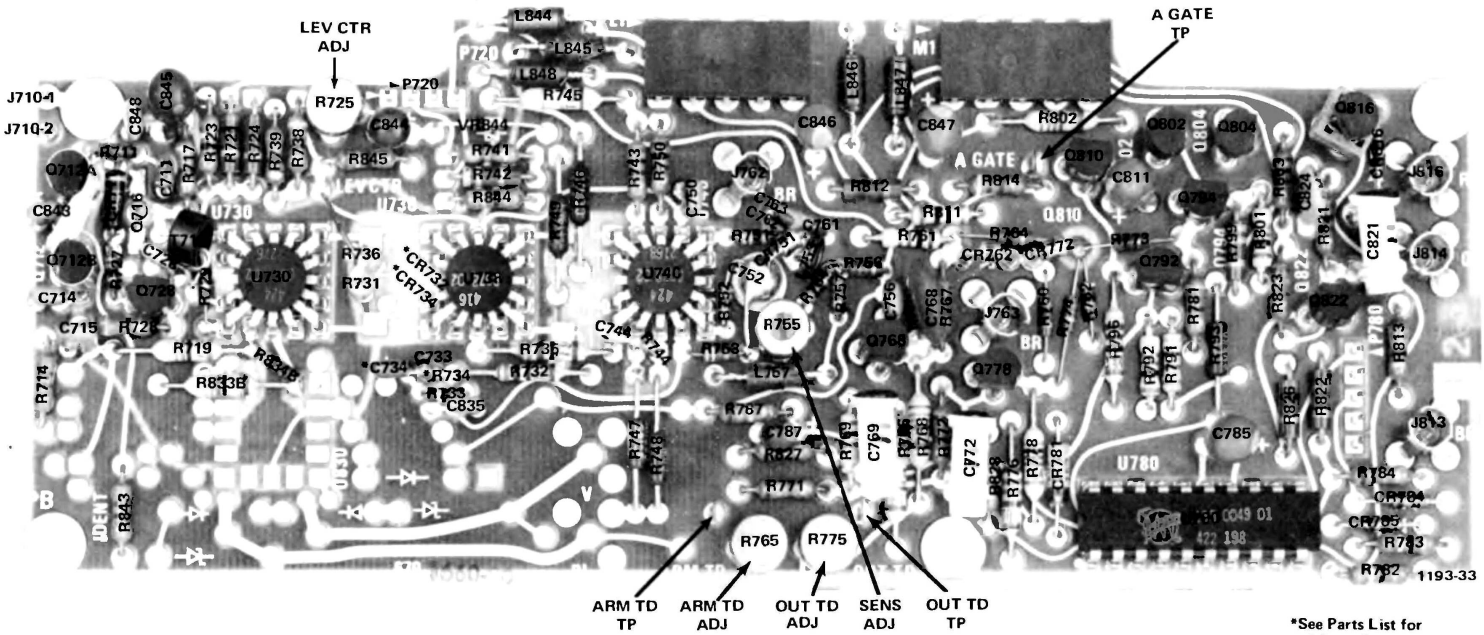
FIG. 8-7B



*See Parts List for serial number ranges.

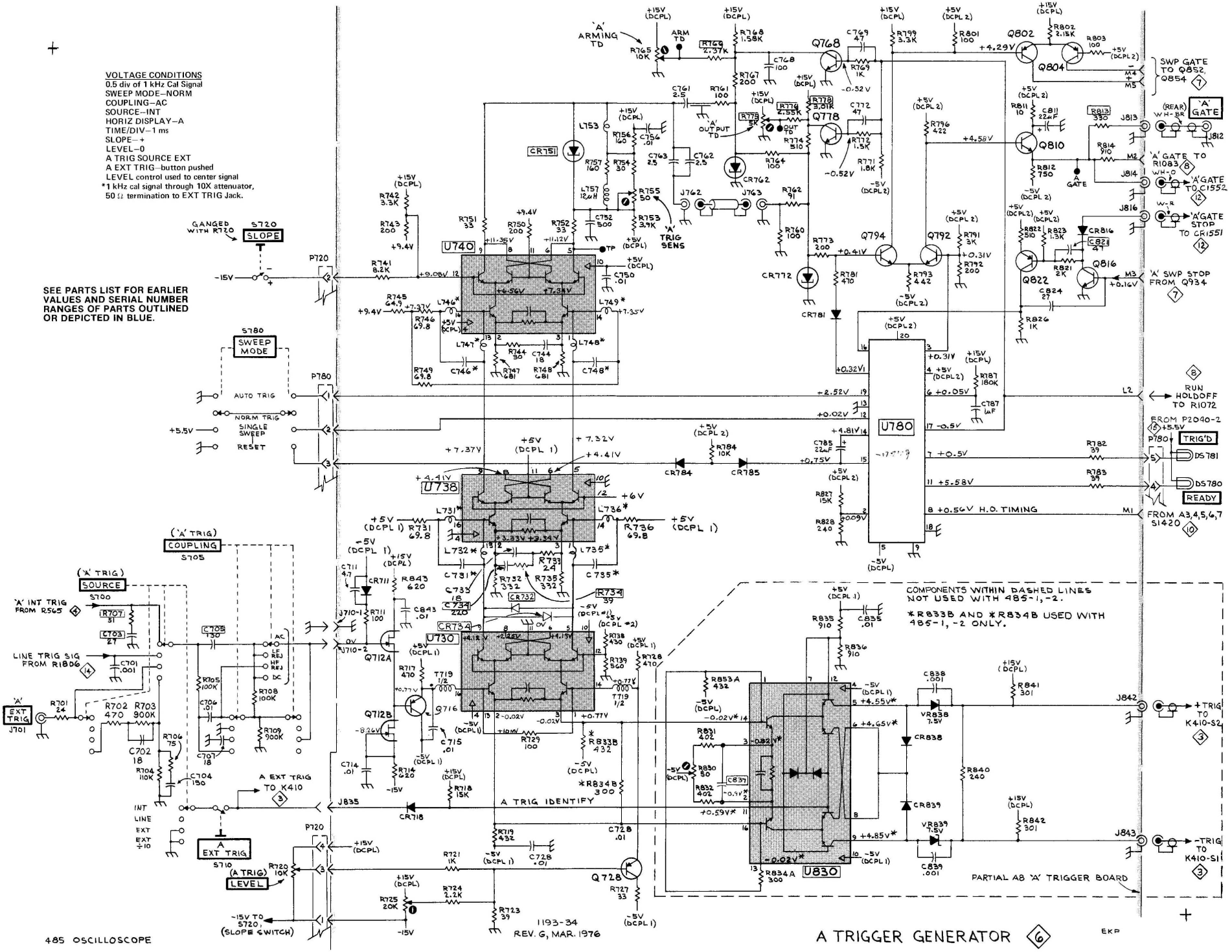
REV. D, AUG. 1975

Fig. 8-7A. A8 A Trigger board (485 only).



*See Parts List for serial number ranges.

Fig. 8-7B. A9 A Trigger board (485-1,-2 only).


VOLTAGE CONDITIONS
0.5 div of 1 kHz Cal Signal
SWEEP MODE—NORM
COUPLING—AC
SOURCE—INT
HORIZ DISPLAY—A
TIME/DIV—1 ms
SLOPE—+
LEVEL—0
A TRIG SOURCE EXT
A EXT TRIG—button pushed
LEVEL control used to center signal
*1 kHz cal signal through 10X attenuator, 50 Ω termination to EXT TRIG Jack.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.
'A' ARMING TD
ARM TD
'A' OUTPUT TD
'A' TRIG SENS
GANGED WITH R720
S720 SLOPE
S780 SWEEP MODE
AUTO TRIG
NORM TRIG
SINGLE SWEEP
RESET
('A' TRIG) COUPLING S705
('A' TRIG) SOURCE S700
'A' INT TRIG FROM R565
LINE TRIG SIG FROM R1806
'A' EXT TRIG J701
INT
LINE
EXT
EXT ÷10
A EXT TRIG S710
('A' TRIG) LEVEL
A EXT TRIG TO K410
-15V TO S720 (SLOPE SWITCH)
U740
U738
U730
U780
U830
A TRIG IDENTIFY
COMPONENTS WITHIN DASHED LINES NOT USED WITH 485-1, -2.
*R833B AND *R834B USED WITH 485-1, -2 ONLY.
PARTIAL A8 'A' TRIGGER BOARD
SWP GATE TO Q852, Q854
'A' GATE
'A' GATE TO R1083
'A' GATE TO C1552
'A' GATE STOP TO CR1551
'A' SWP STOP FROM Q934
RUN HOLDOFF TO R1072
FROM P2040-2 +5.5V
TRIG'D
DS781
DS780
READY
FROM A3,4,5,6,7 S1420
+TRIG TO K410-S2
-TRIG TO K410-S1
1193-34
REV. G, MAR. 1976
485 OSCILLOSCOPE
A TRIGGER GENERATOR 6
EKP

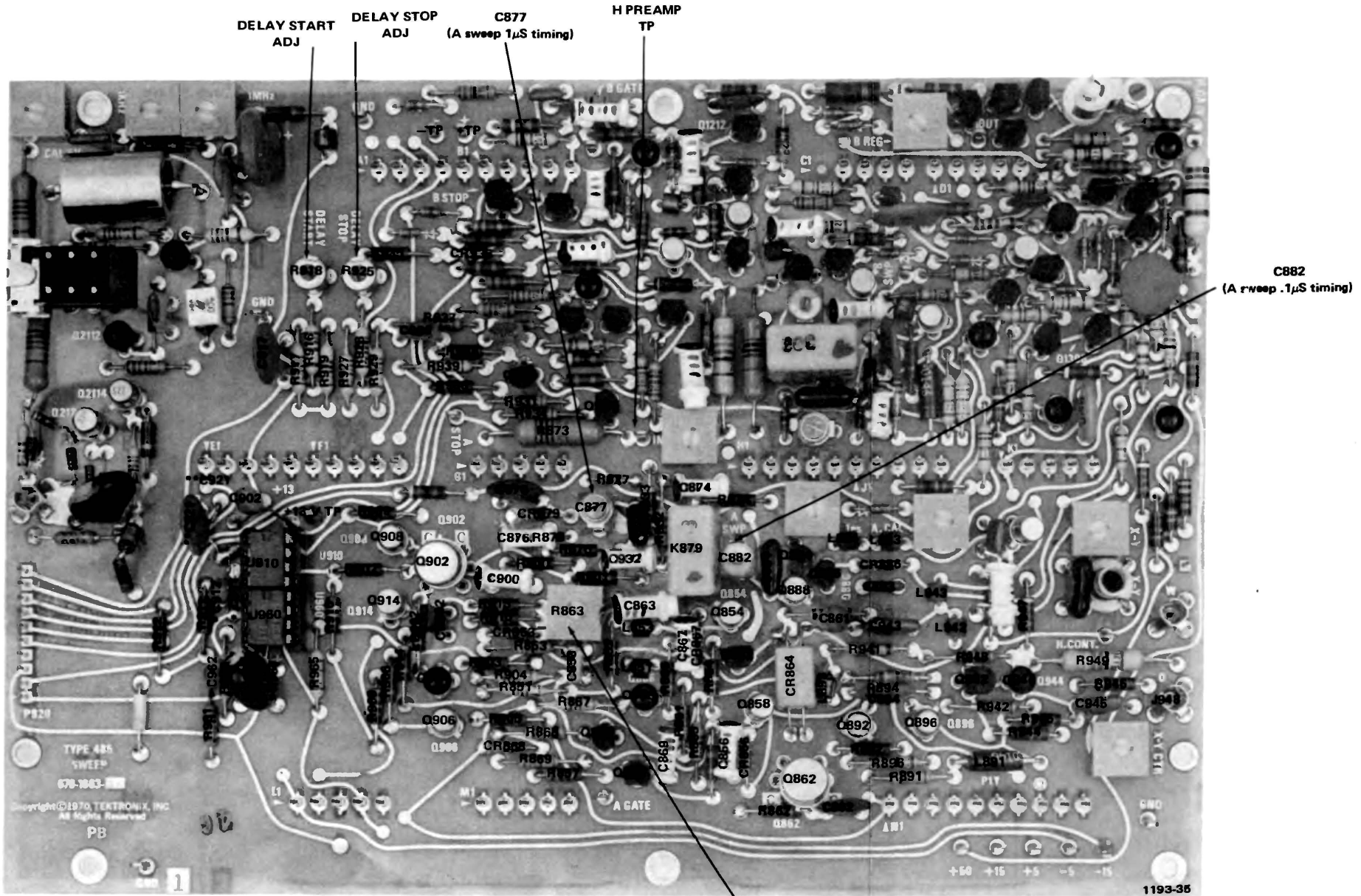
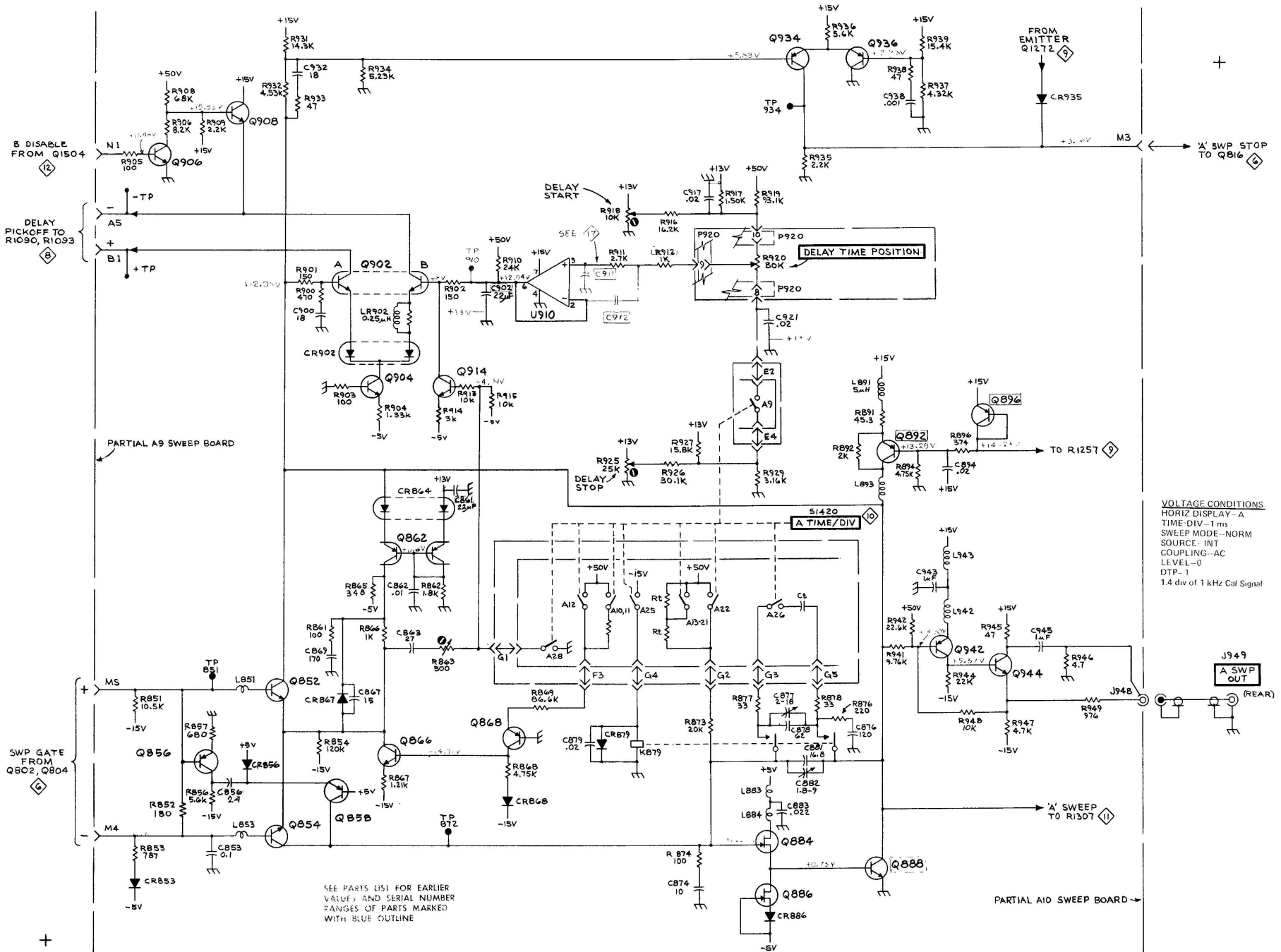


Fig. 8-8. A10 Partial Sweep board.



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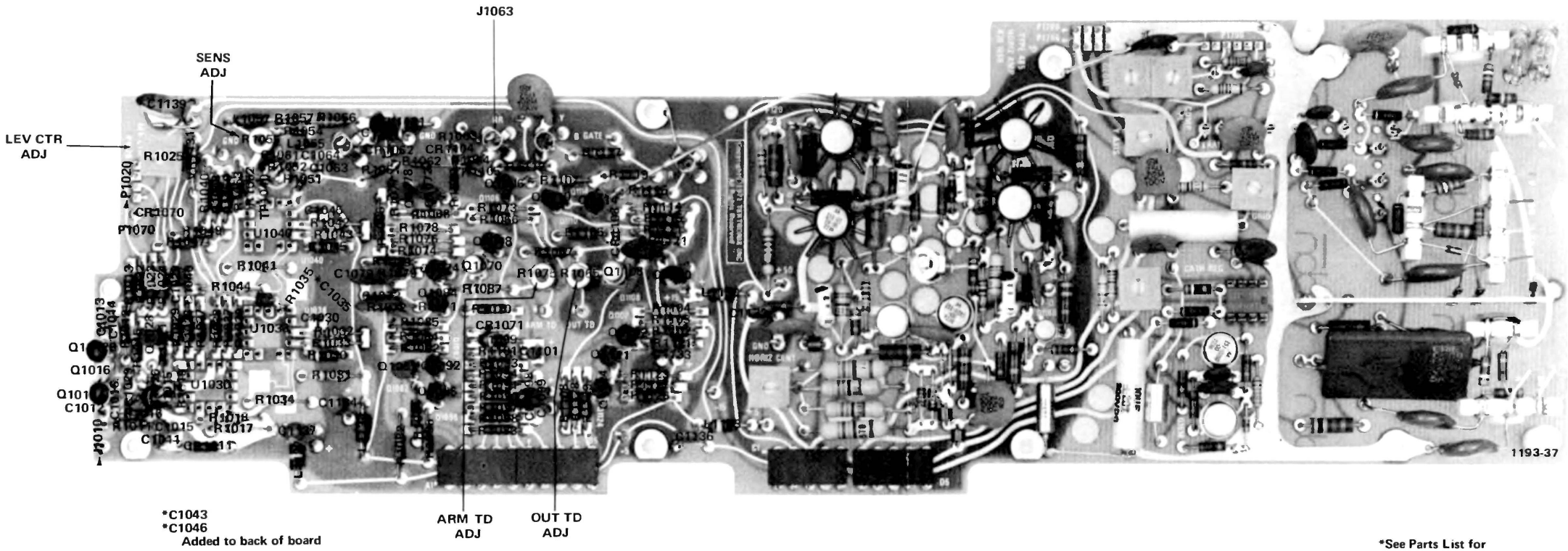
1193-36

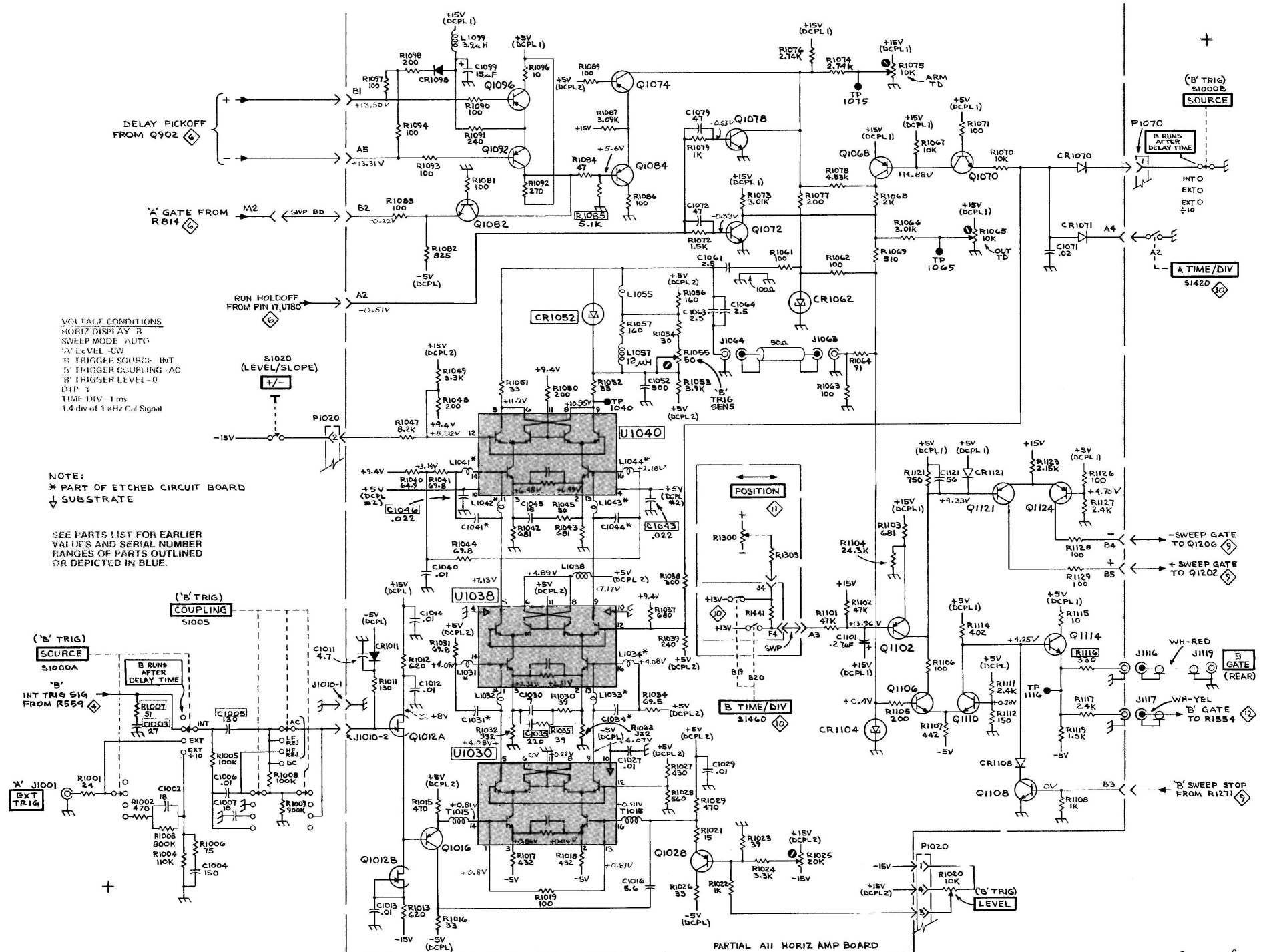
A TIME-BASE GENERATOR 7

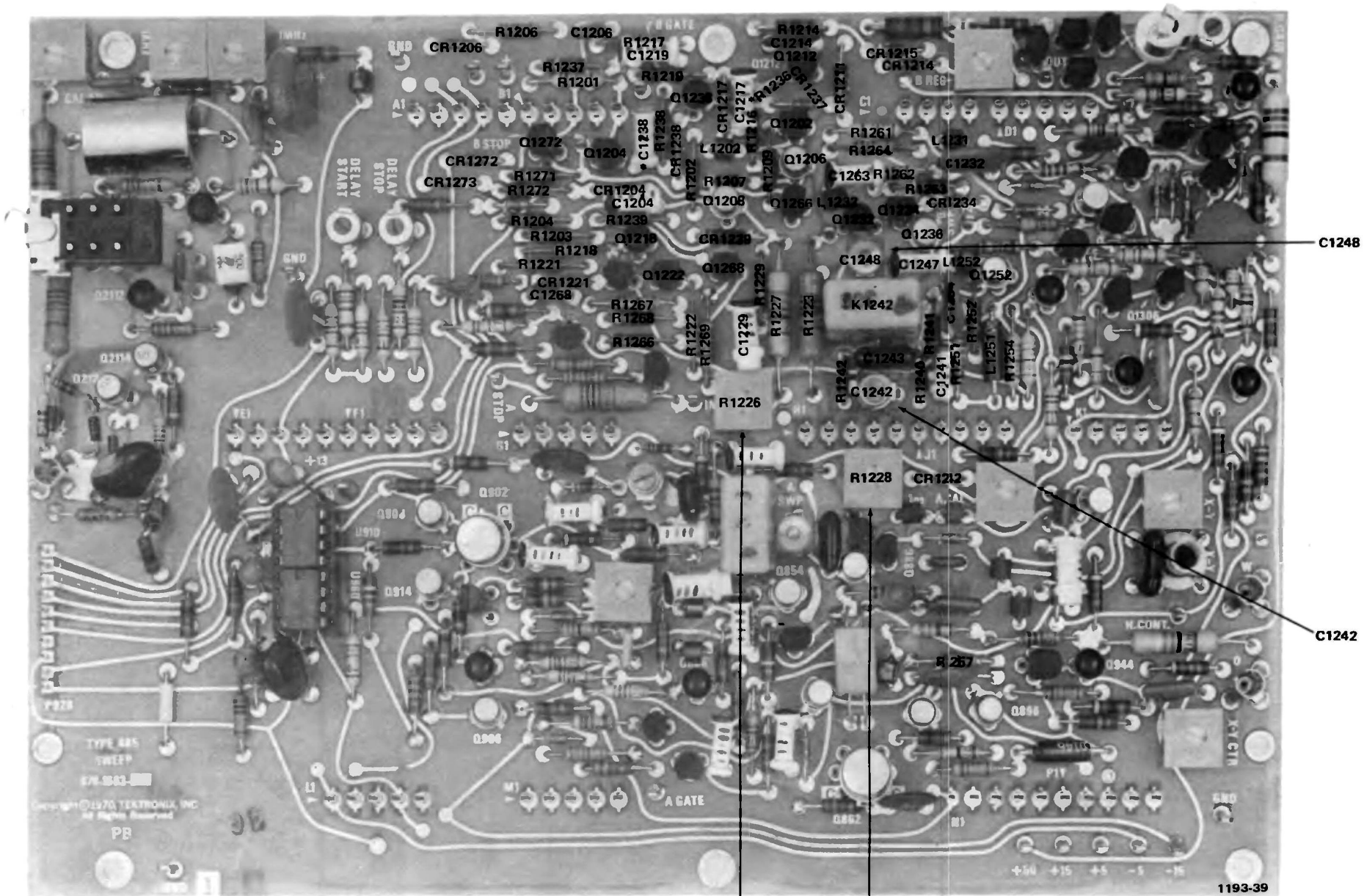
mgf 773



*See Parts List for serial number ranges.

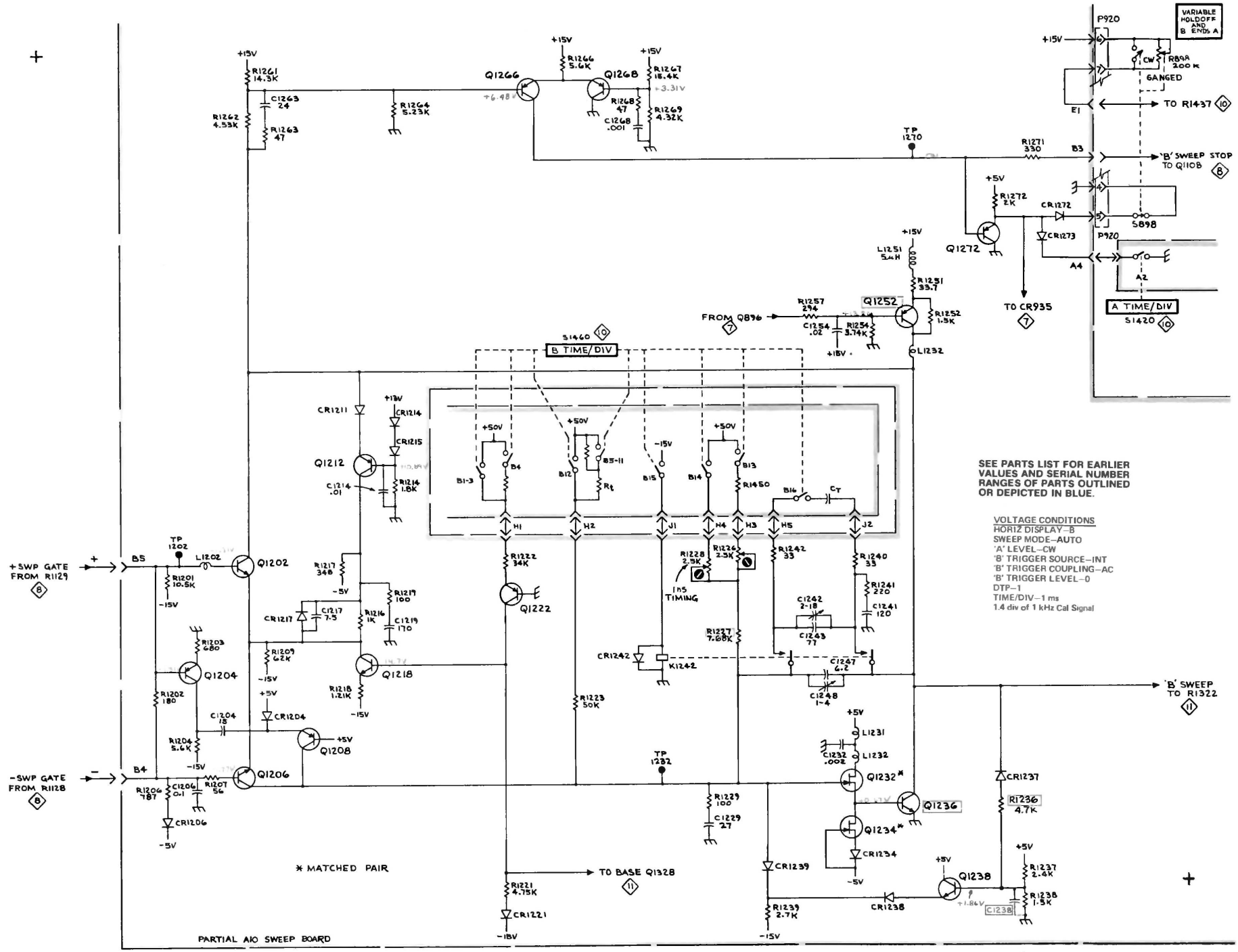
Fig. 8-9. A11 Partial Horizontal amplifier board.


VOLTAGE CONDITIONS
HORIZ DISPLAY B
SWEEP MODE AUTO
'A' LEVEL -CW
'B' TRIGGER SOURCE INT
'B' TRIGGER COUPLING -AC
'B' TRIGGER LEVEL -0
DTP 1
TIME DIV-1 ms
1.4 div of 1 kHz Cal Signal
NOTE:
* PART OF ETCHED CIRCUIT BOARD
↓ SUBSTRATE
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.
DELAY PICKOFF FROM Q902
'A' GATE FROM R814
RUN HOLDOFF FROM PIN 17, U180
S1020 (LEVEL/SLOPE)
('B' TRIG) COUPLING S1005
('B' TRIG) SOURCE S1000A
'B' INT TRIG SIG FROM R559
'A' J1001 EXT TRIG
B RUNS AFTER DELAY TIME
U1040
U1038
U1030
POSITION
B TIME/DIV S1460
A TIME/DIV S1420
('B' TRIG) S1000B SOURCE
P1070
INTO EXT
EXT ÷10
-SWEEP GATE TO Q1206
+SWEEP GATE TO Q1202
B GATE (REAR)
'B' GATE TO R1554
'B' SWEEP STOP FROM R1271
('B' TRIG) LEVEL
P1020
PARTIAL A11 HORIZ AMP BOARD
485 OSCILLOSCOPE
1193-3B
REV. E, MAR. 1976
B TRIGGER GENERATOR
mgf
773



*See Parts List for serial number ranges.

Fig. 8-10. A10 Partial Sweep board.



485 OSCILLOSCOPE

1193-40
REV.D, MAR. 1976

B TIME BASE GENERATOR 9

EKP

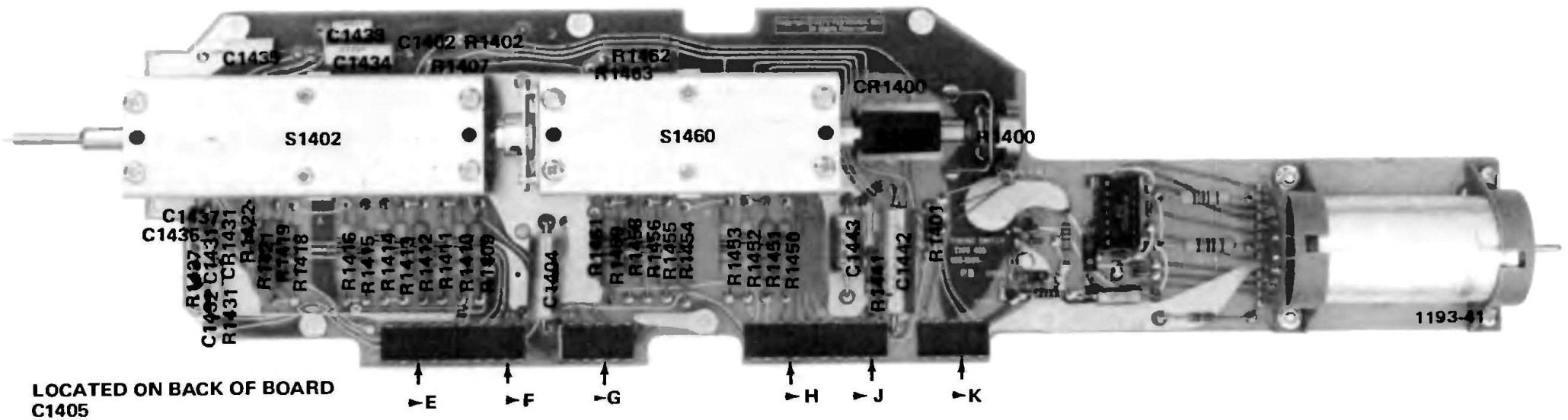


Fig. 8-11. A12 Partial Timing switch board.

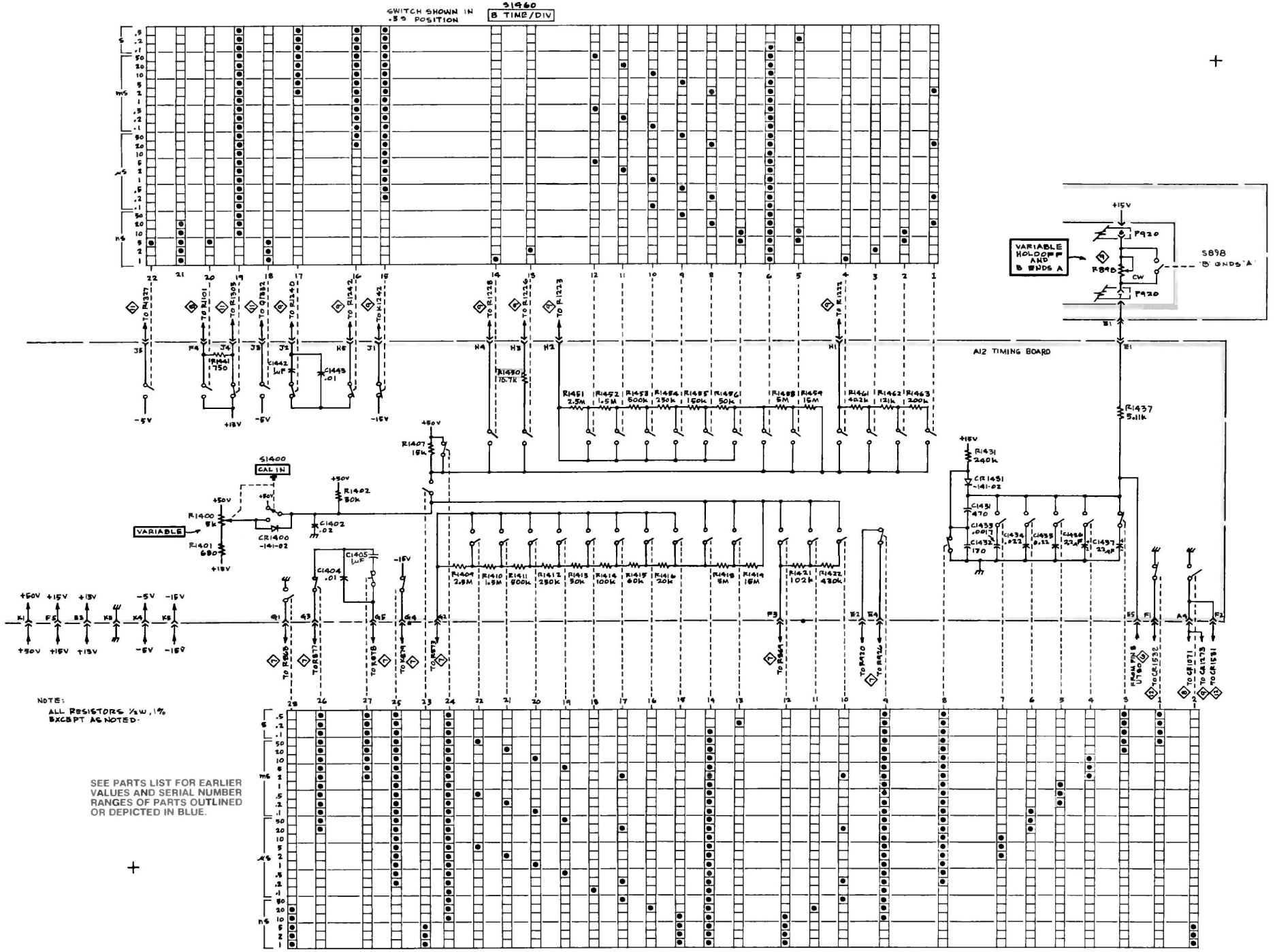

S1460
B TIME/DIV
SWITCH SHOWN IN .5 S POSITION
VARIABLE HOLDOFF A ENDS B ENDS A
S898
A12 TIMING BOARD
S1400
CAL IN
VARIABLE
NOTE:
ALL RESISTORS ½W, 1% EXCEPT AS NOTED.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.
SWITCH SHOWN IN .5S POSITION
A TIME/DIV AND DELAY TIME
S1420

Fig. 8-13 ➡

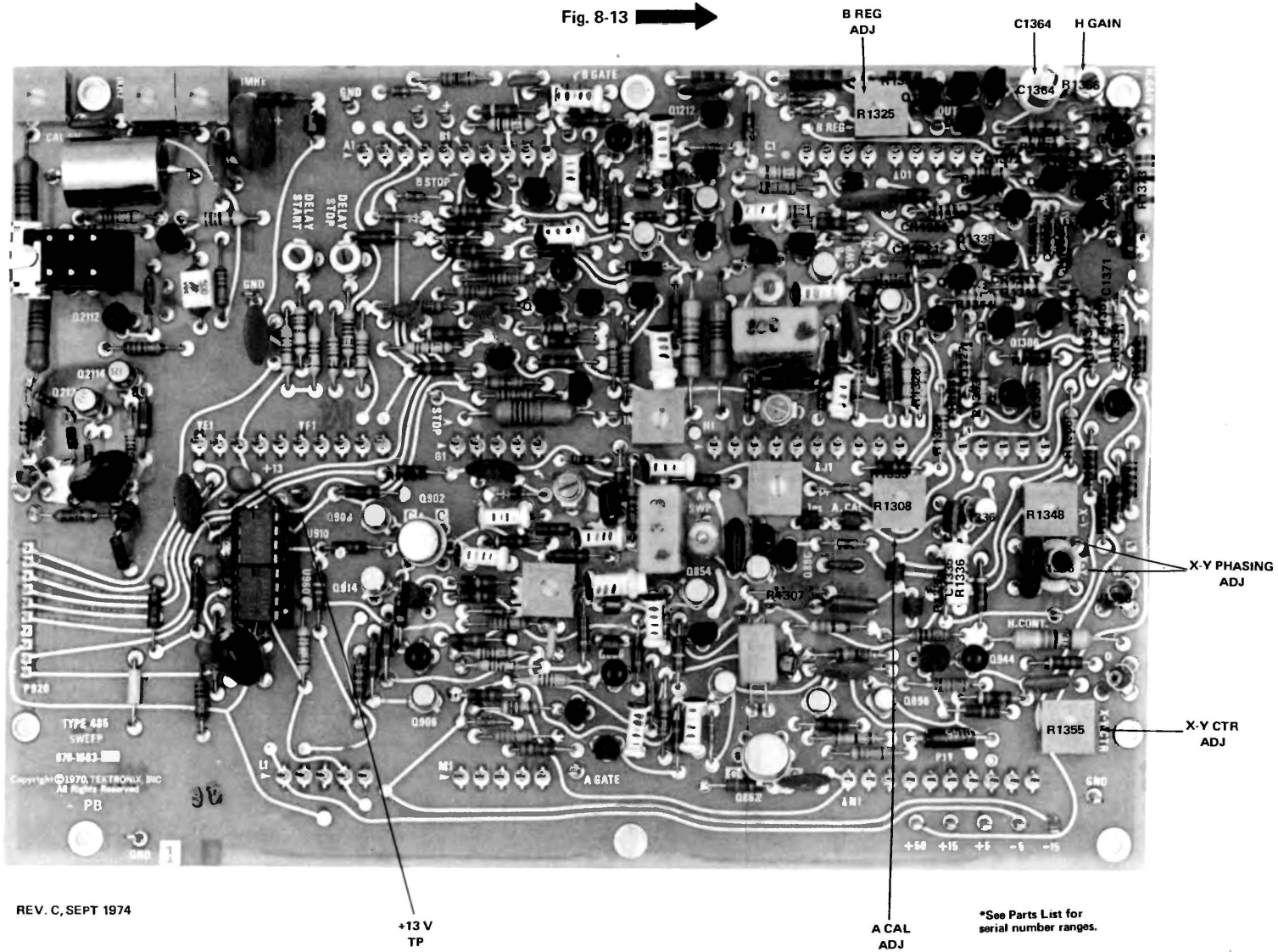


Fig. 8-12. A10 Partial Sweep board.

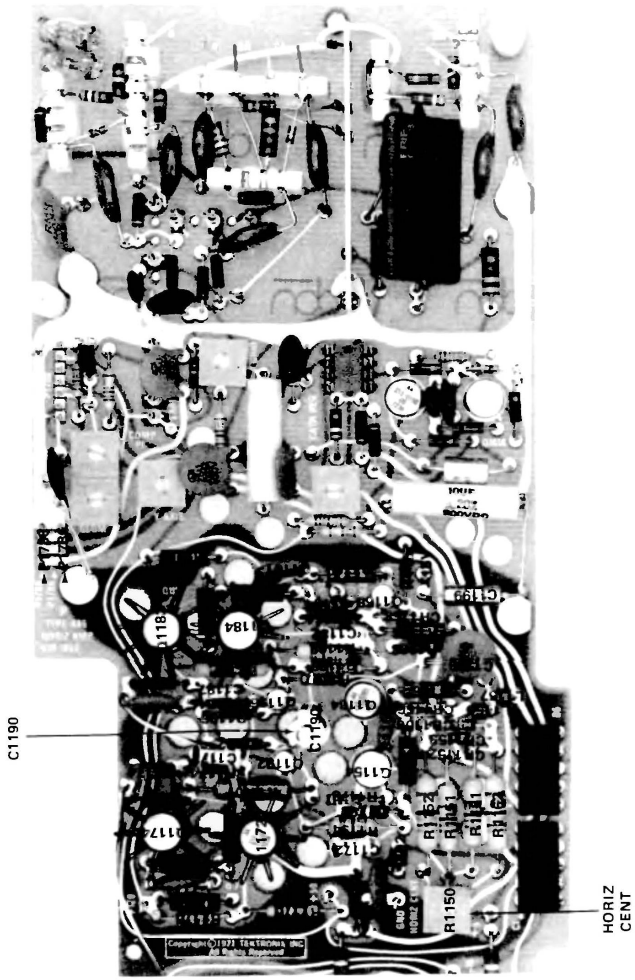
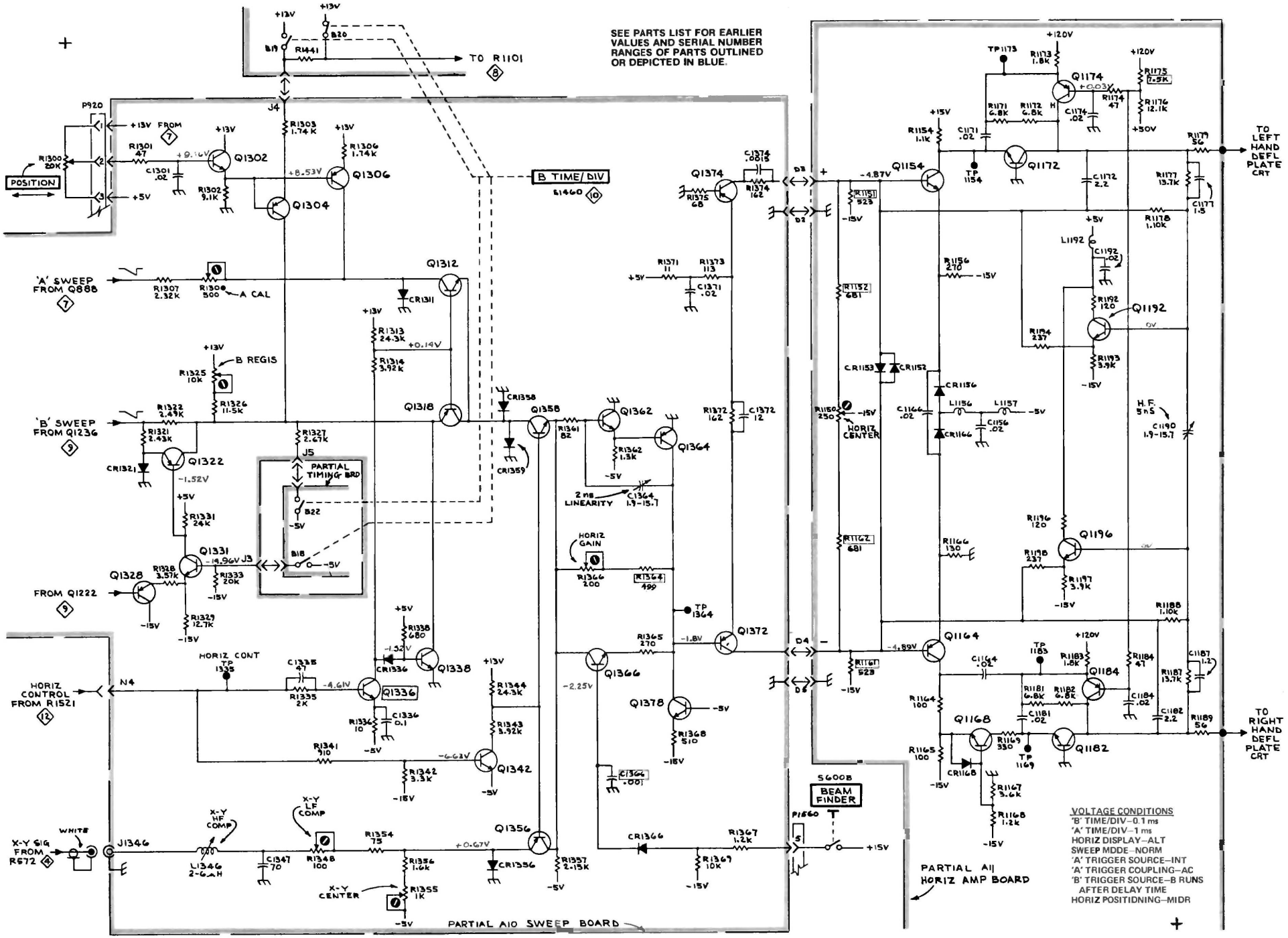
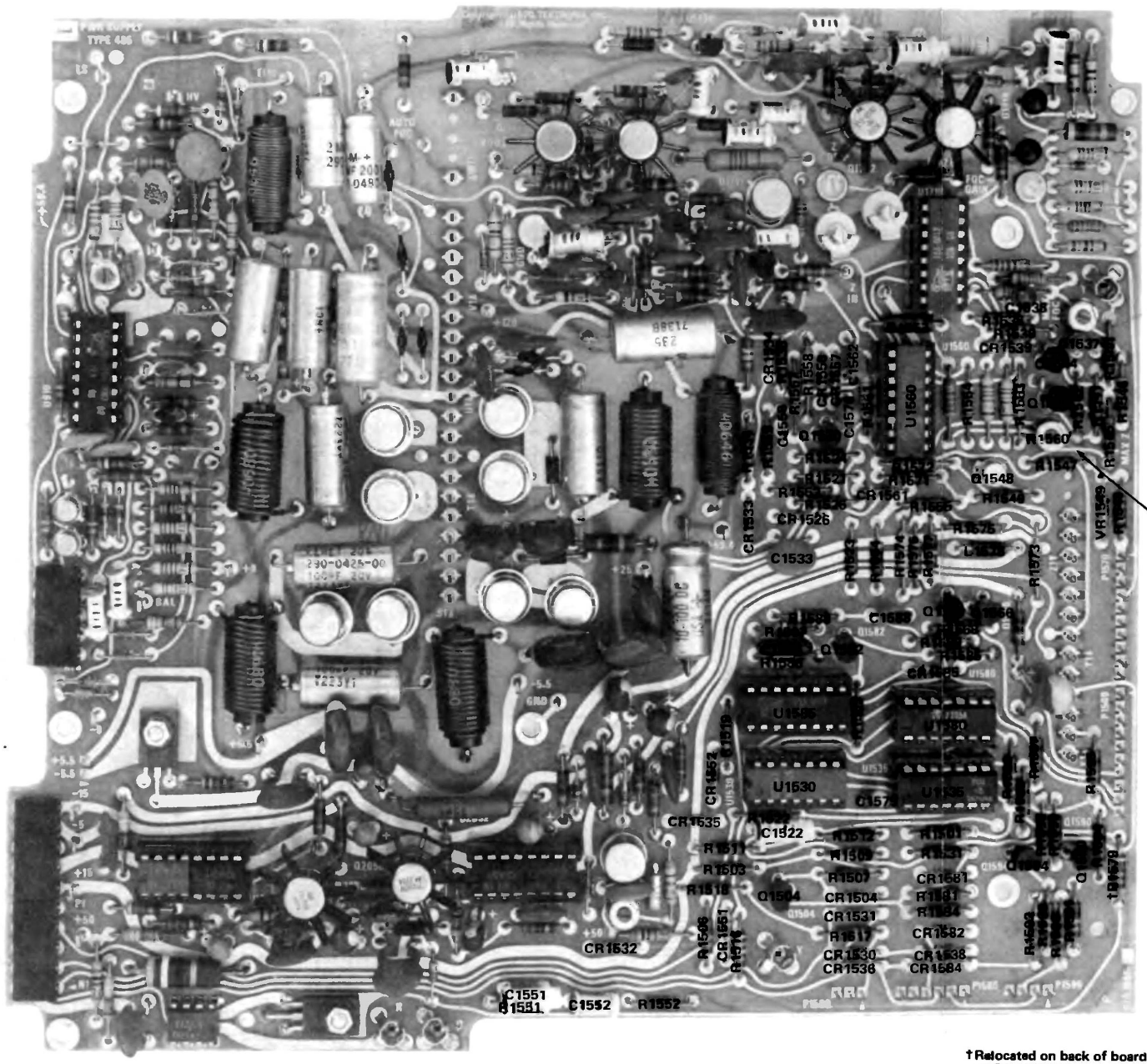


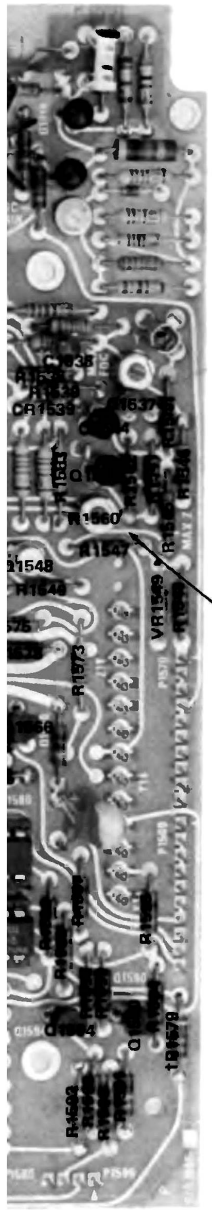
Fig. 8-13. A11 Partial Horizontal amplifier board.



HORIZONTAL AMPLIFIER 11 mgf



†Relocated on back of board at SN B140000-up



Relocated on back of board at SN B140000-up

Fig. 8-14. A13 Partial Power supply board.

REV. B, SEPT 1974

CR1534 IN SHORT CIRCUIT CAUSES
NOTE: INTENSITY CONTROL INOPERATIVE
IN 50 ms, 0,1, 02, 05 s AND X-Y MODE

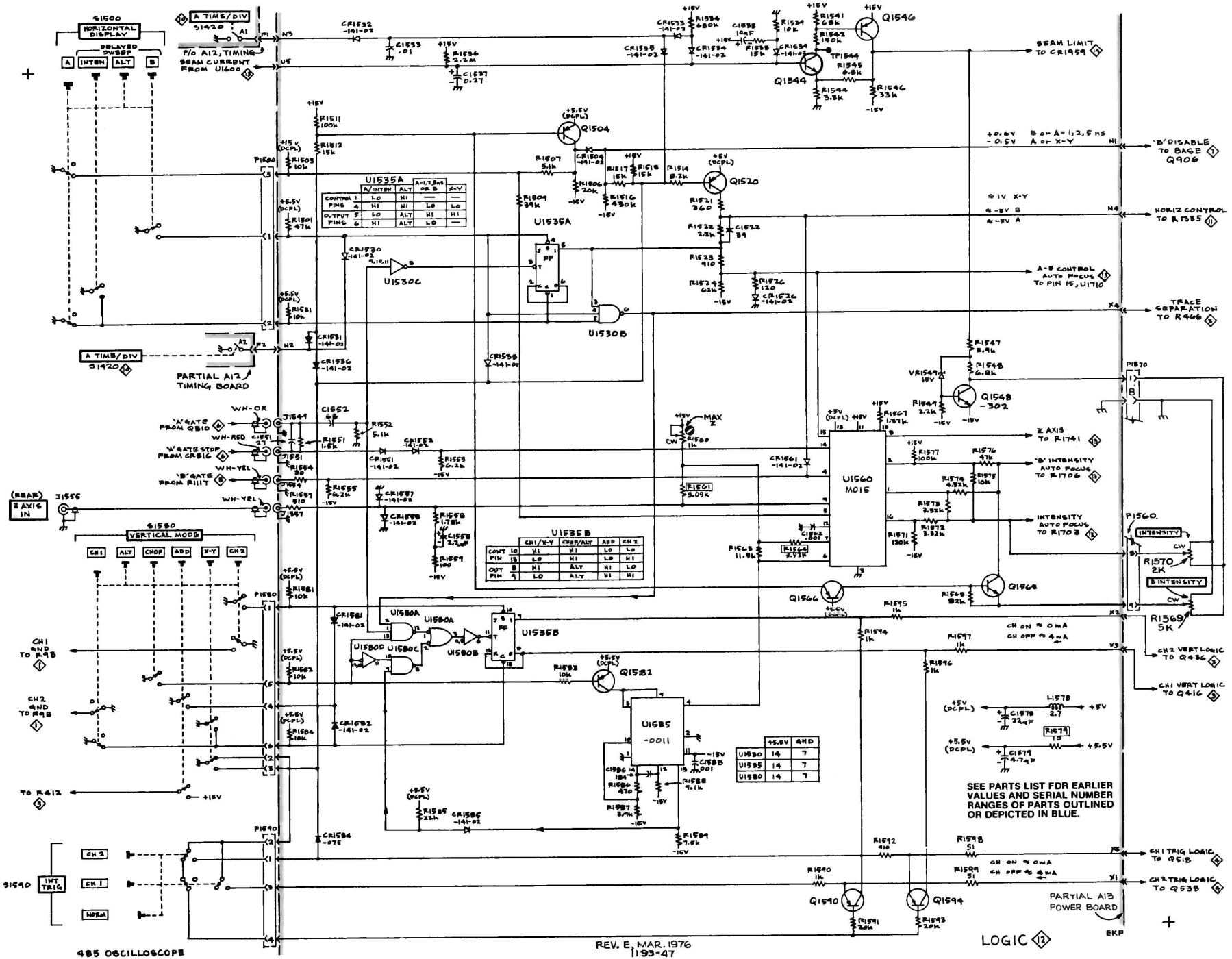


FIG. 8-16

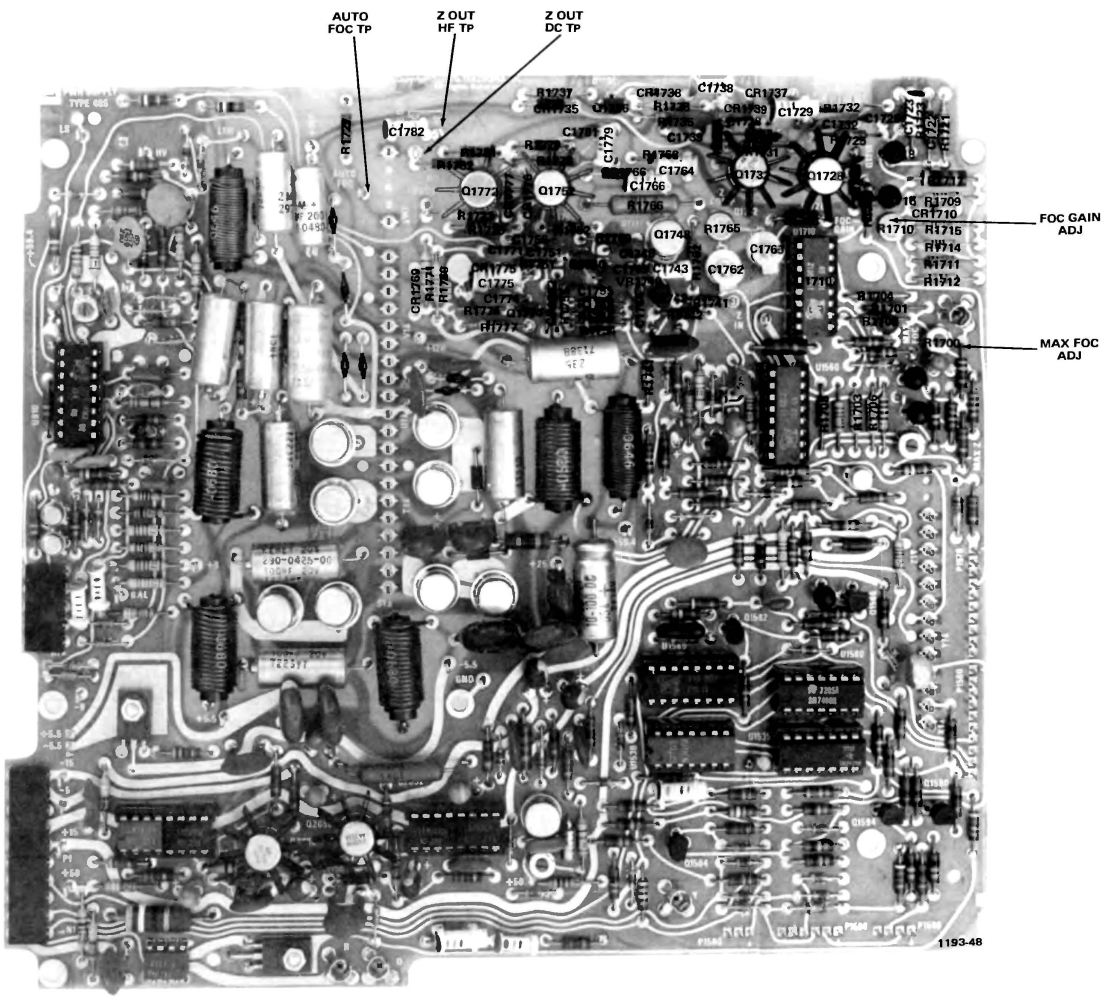


Fig. 8-15. A13 Partial Power Supply board.

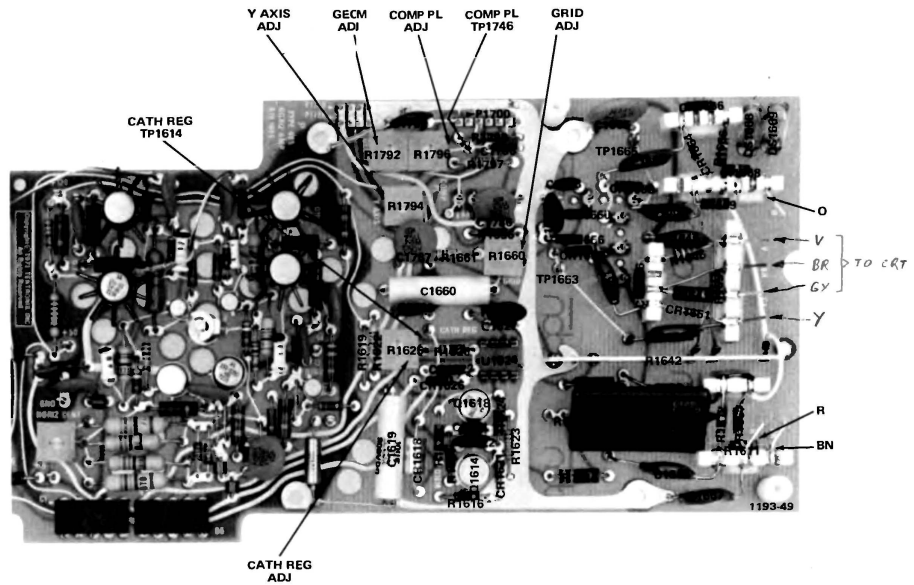


FIG. 8-16. A11 Partial Horizontal amplifier board.

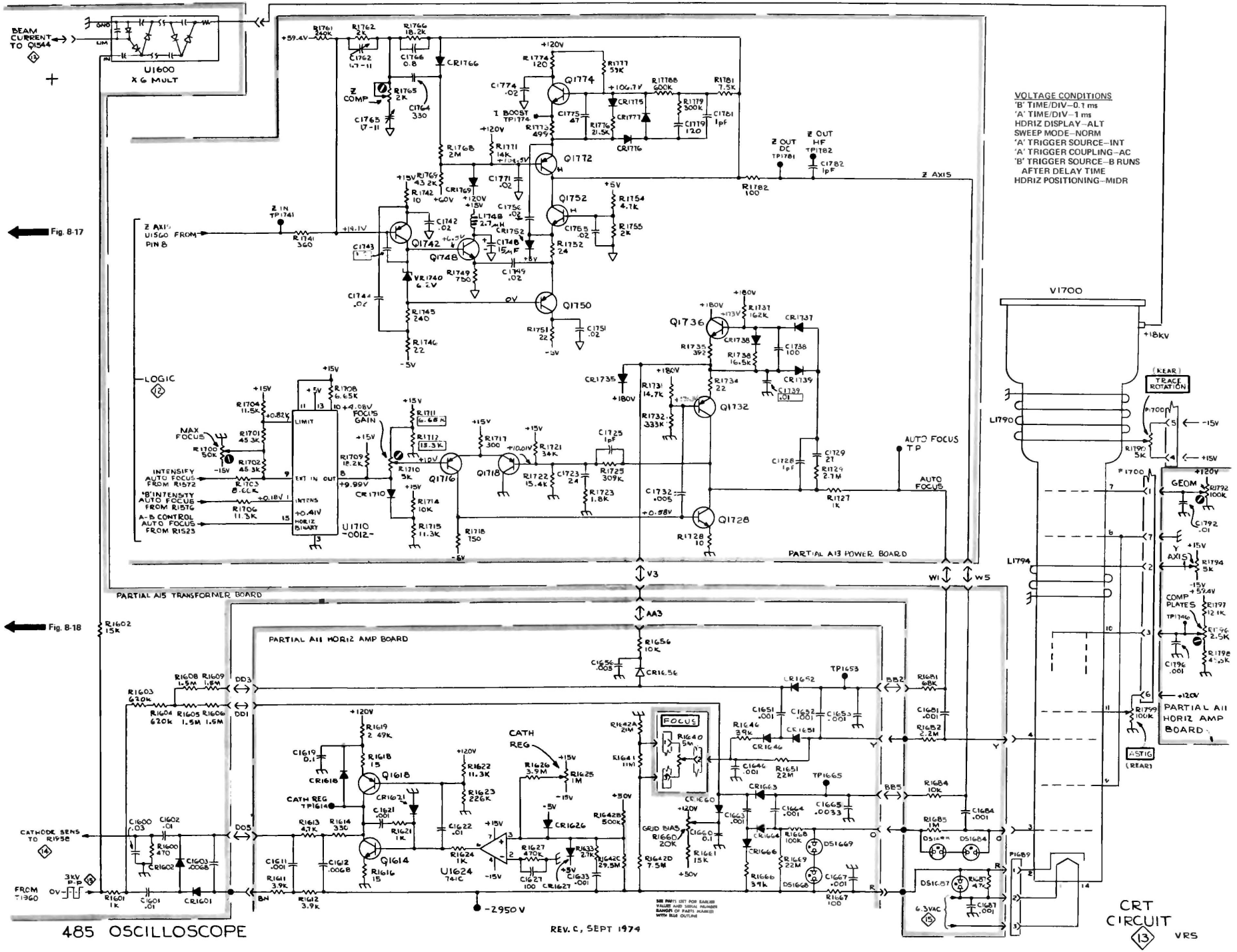
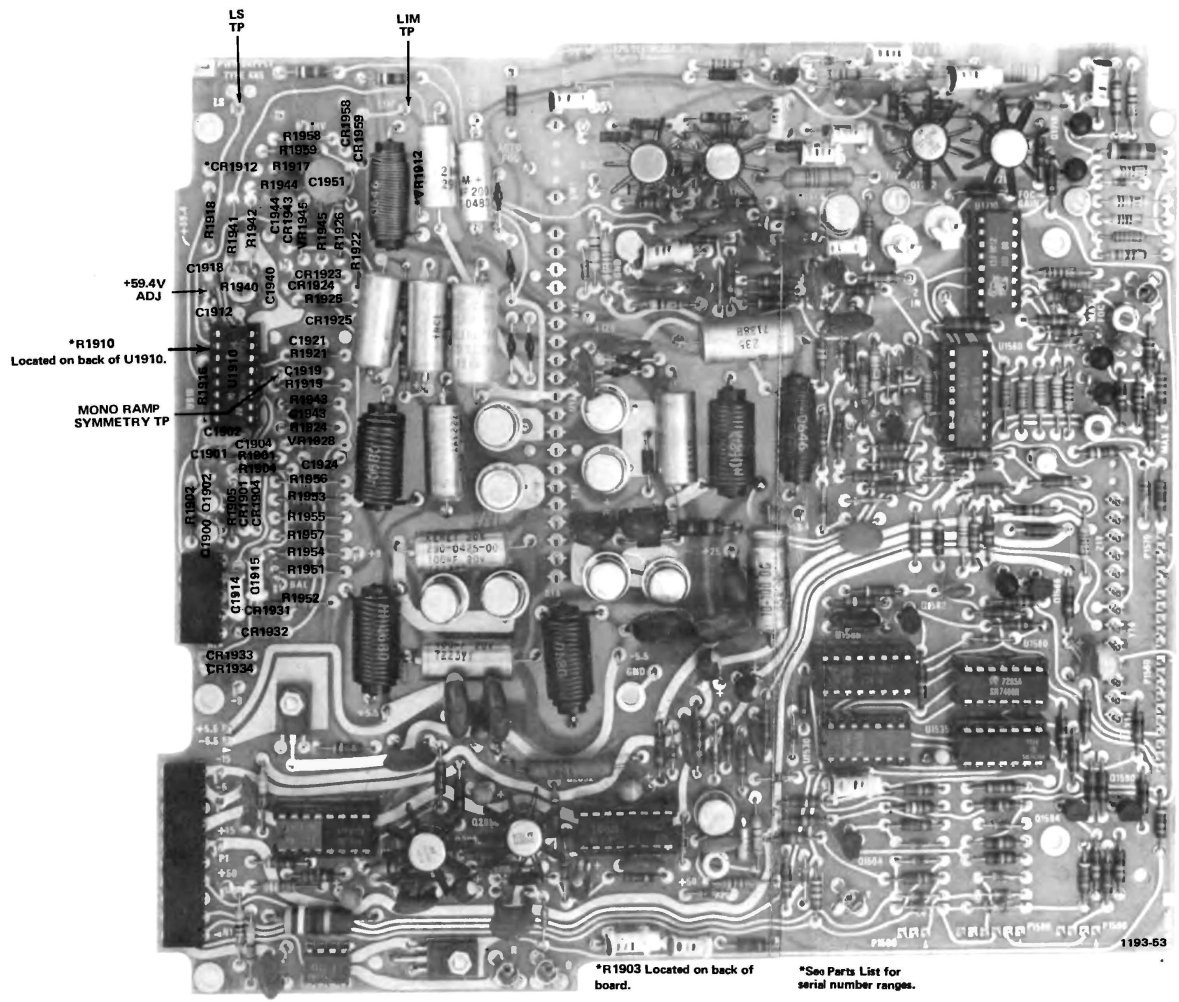

VOLTAGE CONDITIONS
'B' TIME/DIV–0.1 ms
'A' TIME/DIV–1 ms
HDRIZ DISPLAY–ALT
SWEEP MODE–NORM
'A' TRIGGER SOURCE–INT
'A' TRIGGER COUPLING–AC
'B' TRIGGER SOURCE–B RUNS AFTER DELAY TIME
HDRIZ POSITIONING–MIDR
BEAM CURRENT TO Q1544
U1600 X G MULT
Z COMP
Z BOOST TP1774
Q1774
Q1772
Q1752
Q1742
Q1748
Q1750
Z OUT DC TP1781
Z OUT HF TP1782
Z AXIS
Z IN TP1741
Z AXIS FROM U1560 PIN 8
Fig. 8-17
LOGIC
MAX FOCUS
INTENSITY AUTO FOCUS FROM R1572
'B' INTENSITY AUTO FOCUS FROM R1576
A-B CONTROL AUTO FOCUS FROM R1523
U1710 -0012-
FOCUS GAIN
Q1716
Q1718
Q1736
Q1732
Q1728
AUTO FOCUS TP
AUTO FOCUS
PARTIAL A13 POWER BOARD
PARTIAL A15 TRANSFORMER BOARD
V1700
+18kv
(REAR) TRACE ROTATION
L1790
L1794
GEOM
Y AXIS
COMP PLATES
PARTIAL A11 HORIZ AMP BOARD
ASTIG (REAR)
Fig. 8-18
PARTIAL A11 HORIZ AMP BOARD
CATH REG
FOCUS
GRID BIAS
U1624 741C
-2950 V
CATHODE SENS TO R1958
FROM T1960
3KV P-P
CRT CIRCUIT
13 VRS
485 OSCILLOSCOPE
REV. C, SEPT 1974

FIG. 8-20 & 8-21



*R1903 Located on back of board.

*See Parts List for serial number ranges.

Fig. 8-19. A13 Partial Power Supply board.

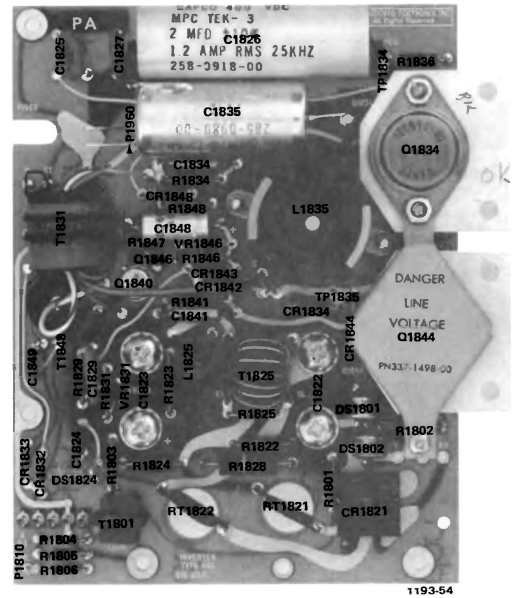


Fig. 8-20. A14 Inverter board.

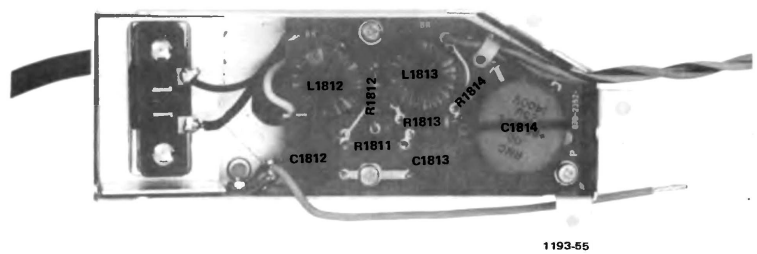
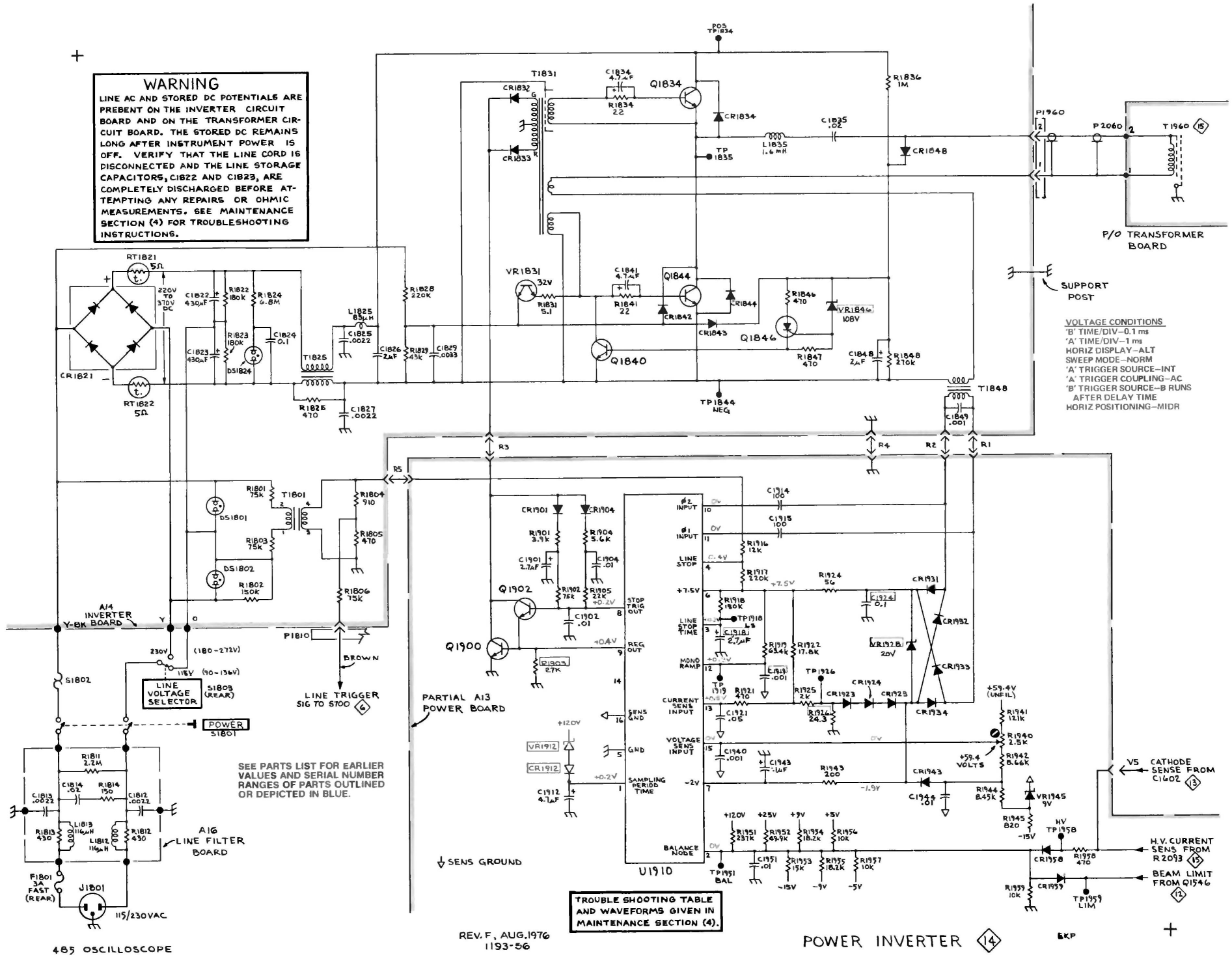
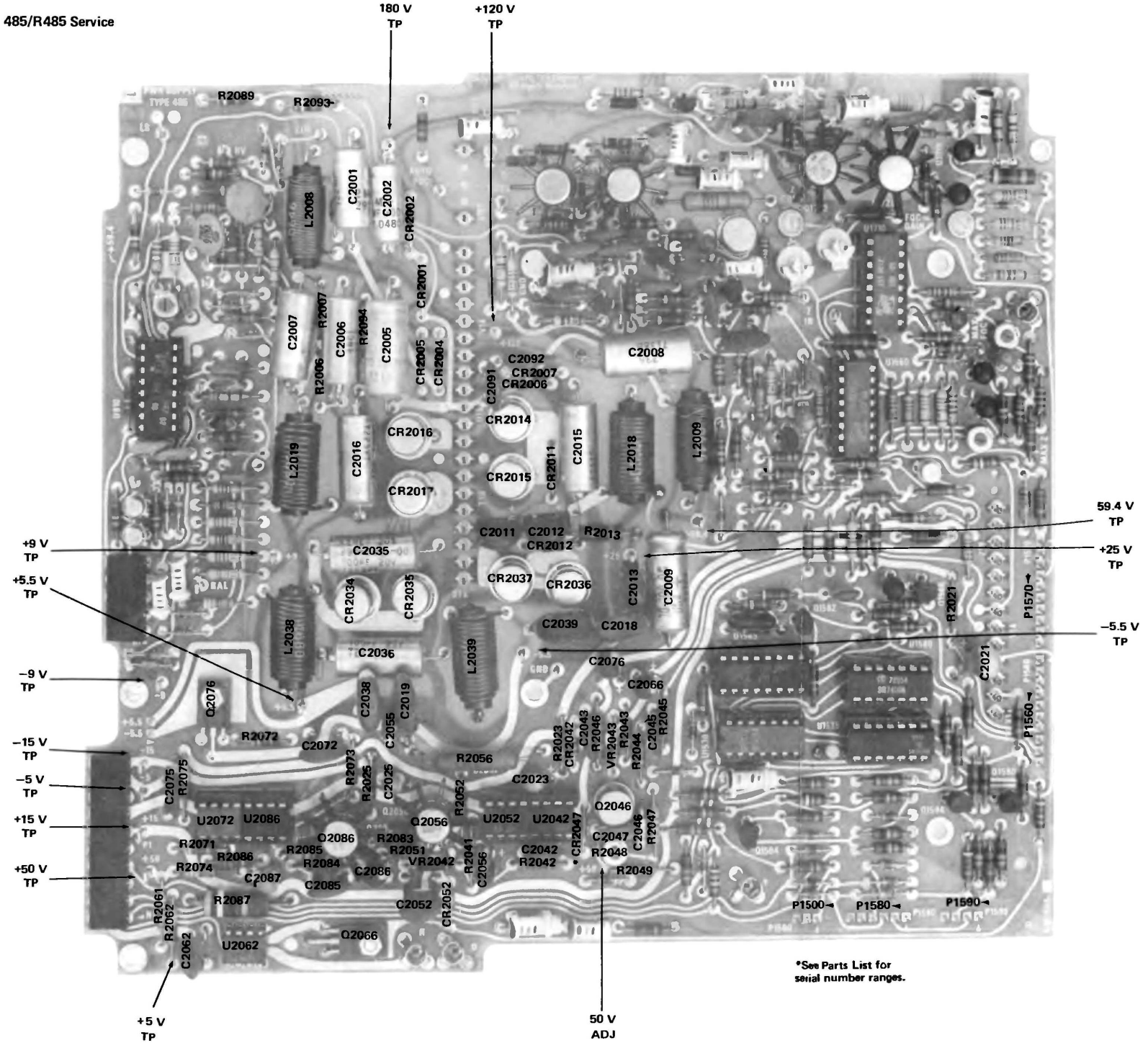


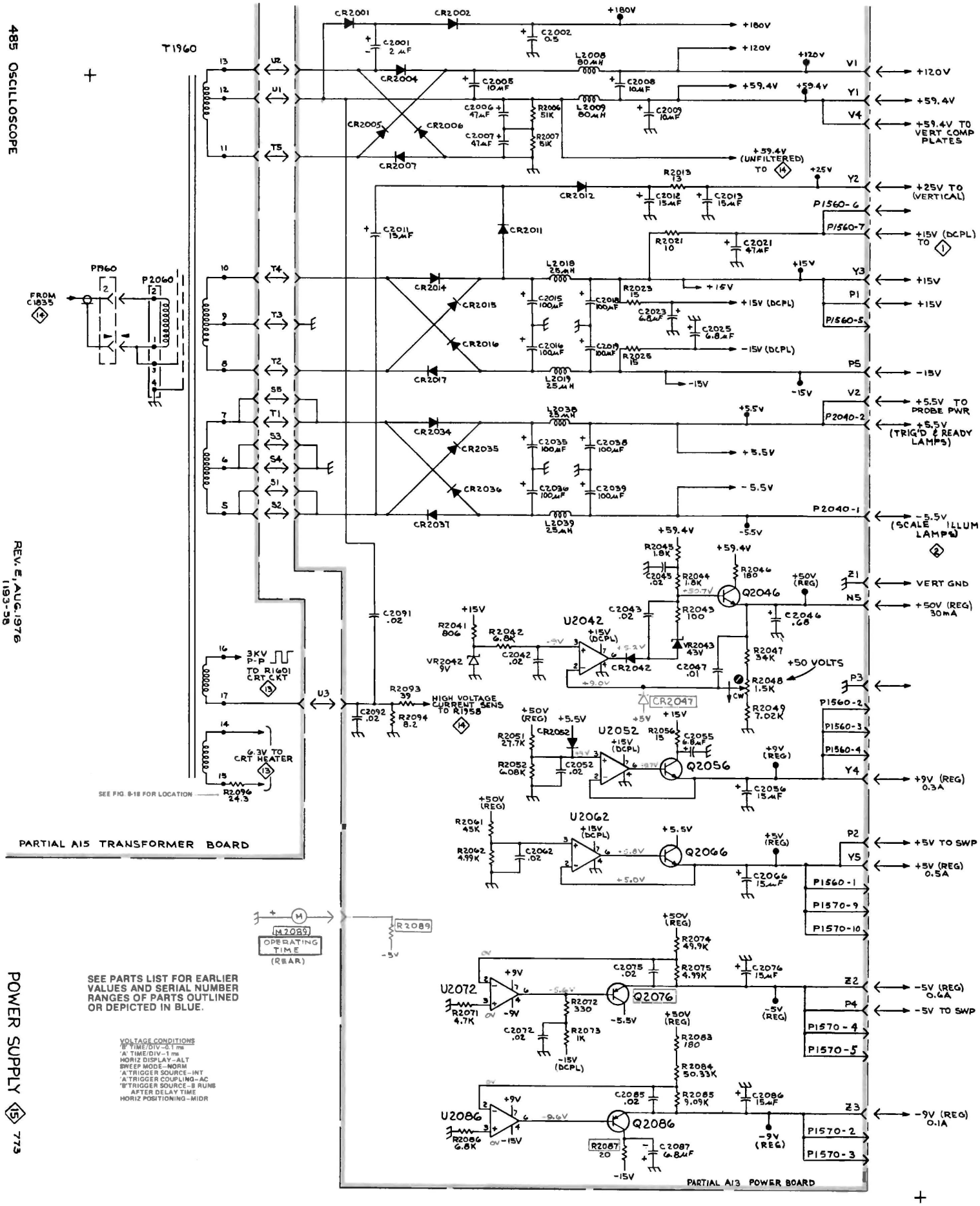
Fig. 8-21. A16 Line Filter board.


WARNING
LINE AC AND STORED DC POTENTIALS ARE PREBENT ON THE INVERTER CIRCUIT BOARD AND ON THE TRANSFORMER CIRCUIT BOARD. THE STORED DC REMAINS LONG AFTER INSTRUMENT POWER IS OFF. VERIFY THAT THE LINE CORD IS DISCONNECTED AND THE LINE STORAGE CAPACITORS, C1822 AND C1823, ARE COMPLETELY DISCHARGED BEFORE ATTEMPTING ANY REPAIRS OR OHMIC MEASUREMENTS. SEE MAINTENANCE SECTION (4) FOR TROUBLESHOOTING INSTRUCTIONS.
P/O TRANSFORMER BOARD
SUPPORT POST
VOLTAGE CONDITIONS
'B' TIME/DIV—0.1 ms
'A' TIME/DIV—1 ms
HORIZ DISPLAY—ALT
SWEEP MODE—NORM
'A' TRIGGER SOURCE—INT
'A' TRIGGER COUPLING—AC
'B' TRIGGER SOURCE—B RUNS AFTER DELAY TIME
HORIZ POSITIONING—MIDR
A14 INVERTER Y-BK BOARD
PARTIAL A13 POWER BOARD
A1G LINE FILTER BOARD
LINE VOLTAGE SELECTOR
POWER S1801
LINE TRIGGER SIG TO ST00
BROWN
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.
TROUBLE SHOOTING TABLE AND WAVEFORMS GIVEN IN MAINTENANCE SECTION (4).
SENS GROUND
115/230VAC
485 OSCILLOSCOPE
REV. F, AUG. 1976
1193-56
POWER INVERTER
V5 CATHODE SENS FROM C1602
H.V. CURRENT SENS FROM R2093
BEAM LIMIT FROM Q1546
U1910



REV. B. SEPT 1974

Fig. 8-22. A13 Partial Power supply board.



SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN BLUE.

VOLTAGE CONDITIONS
'B' TIME/DIV-0.1 ms
'A' TIME/DIV-1 ms
HORIZ DISPLAY-ALT
SWEEP MODE-NORM
'A' TRIGGER SOURCE-INT
'A' TRIGGER COUPLING-AC
'B' TRIGGER SOURCE-B RUNS AFTER DELAY TIME
HORIZ POSITIONING-MIDR

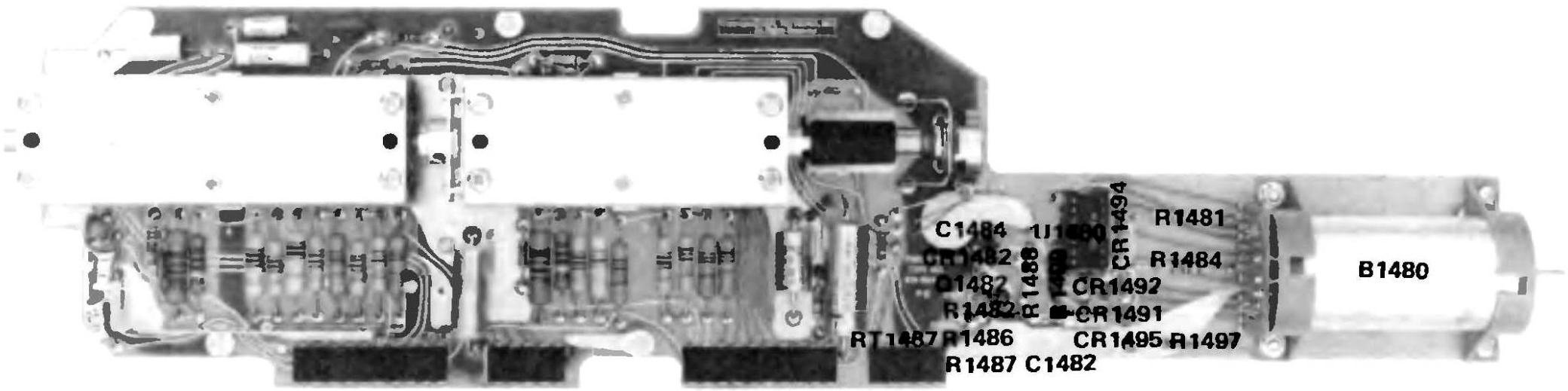


Fig. 8-23. A12 Partial Timing switch board.

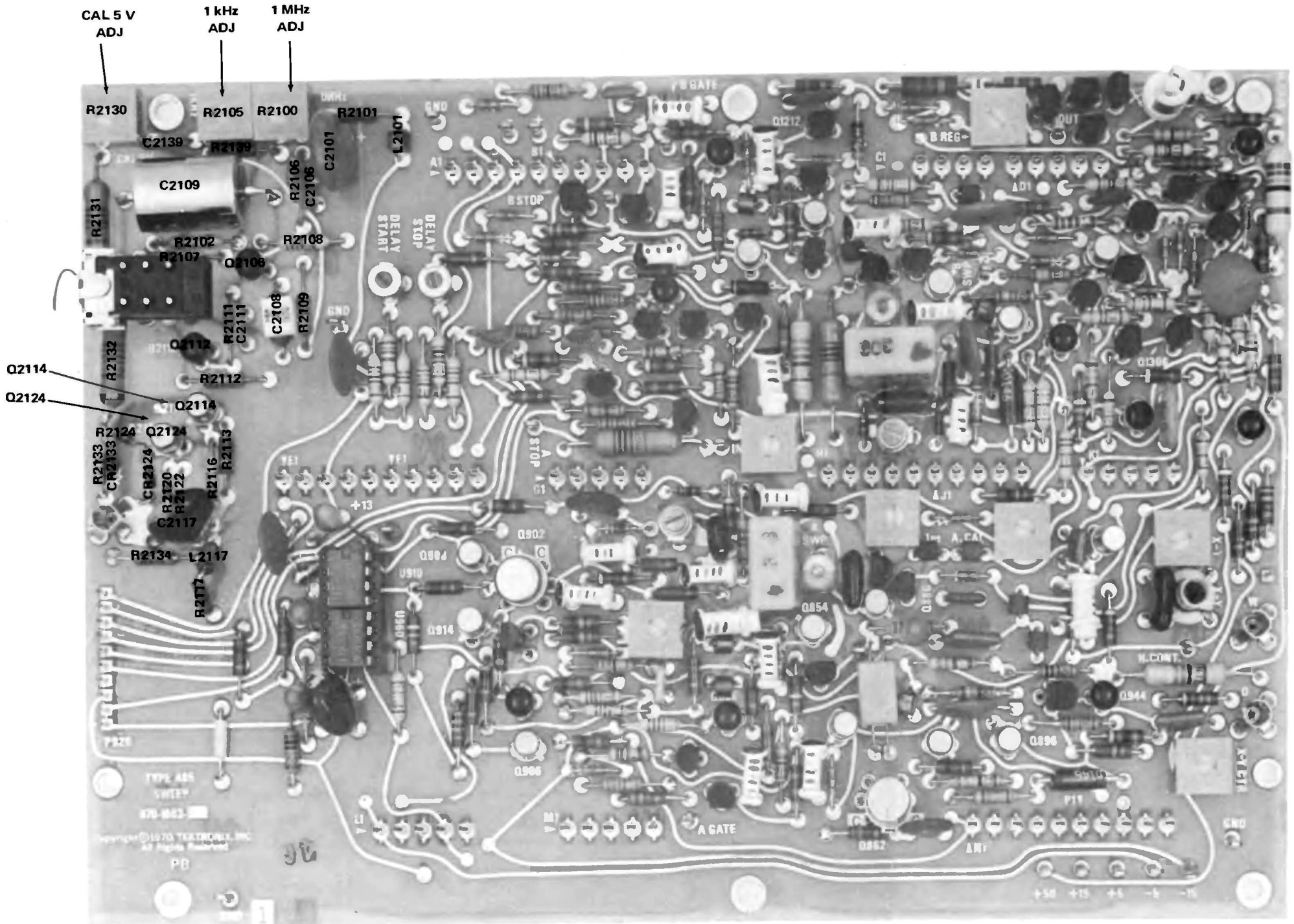
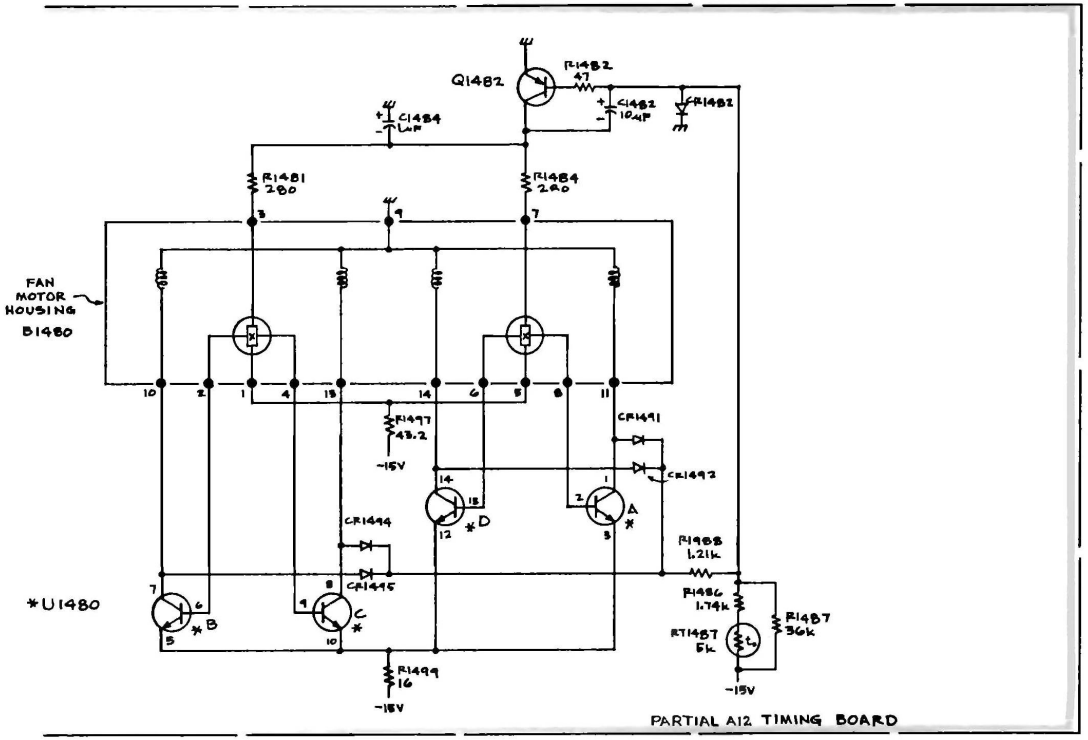
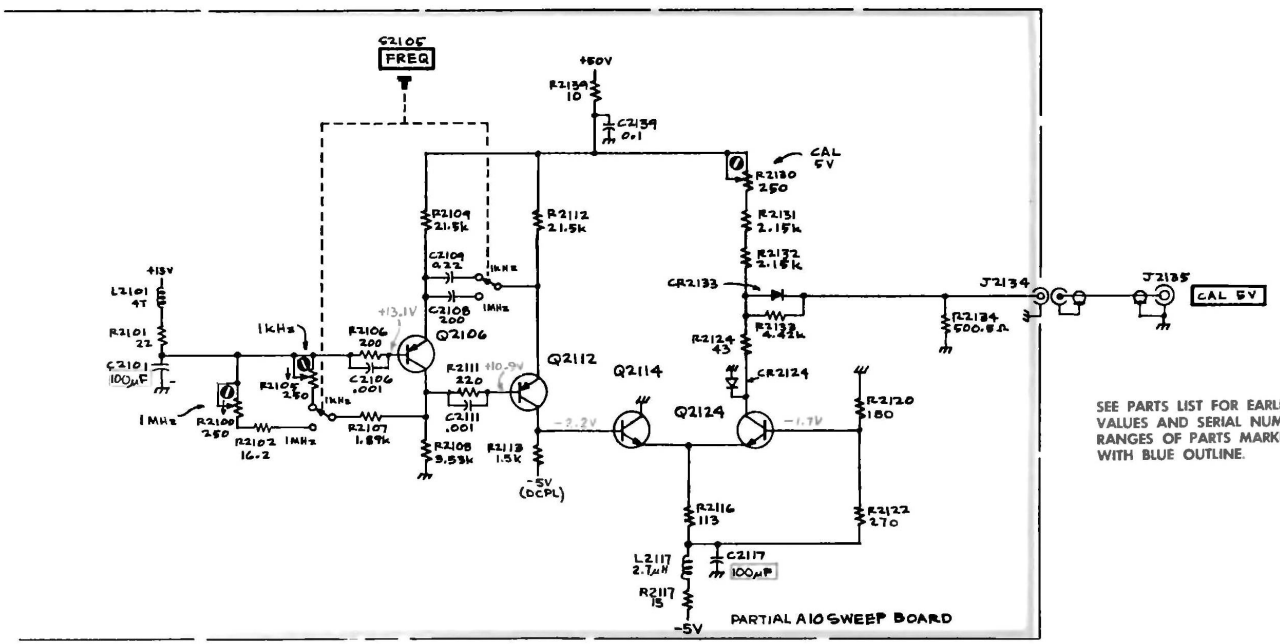
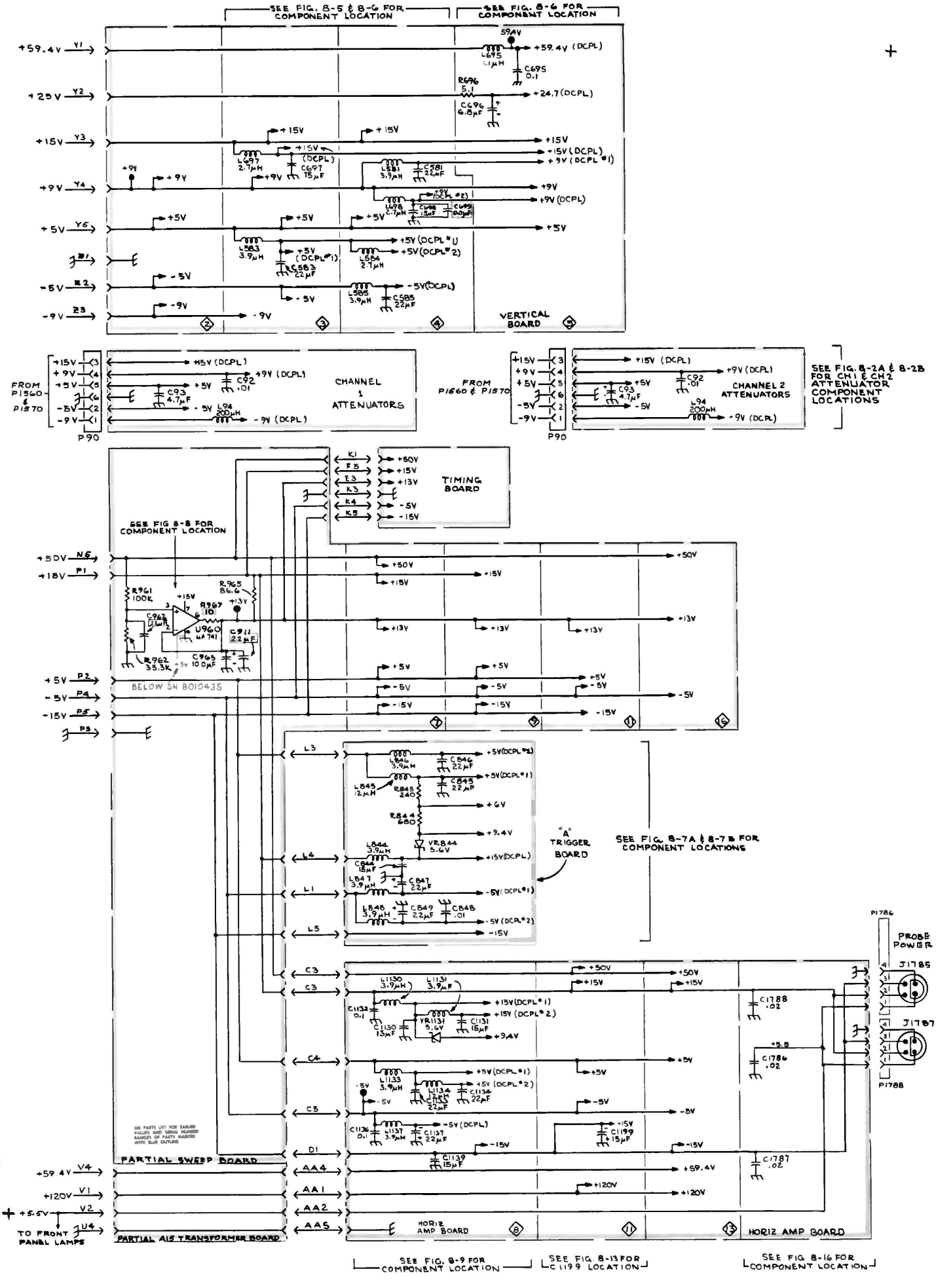


Fig. 8-24. A10 Partial Sweep board.





SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.



REV. E AUG. 1973
1163-62
EKP