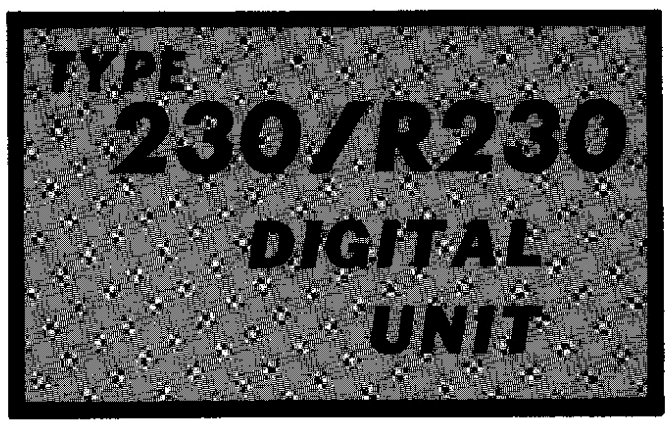
INSTRUCTION MANUAL

Serial Number _____



Tektronix, Inc.
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070-0635-00

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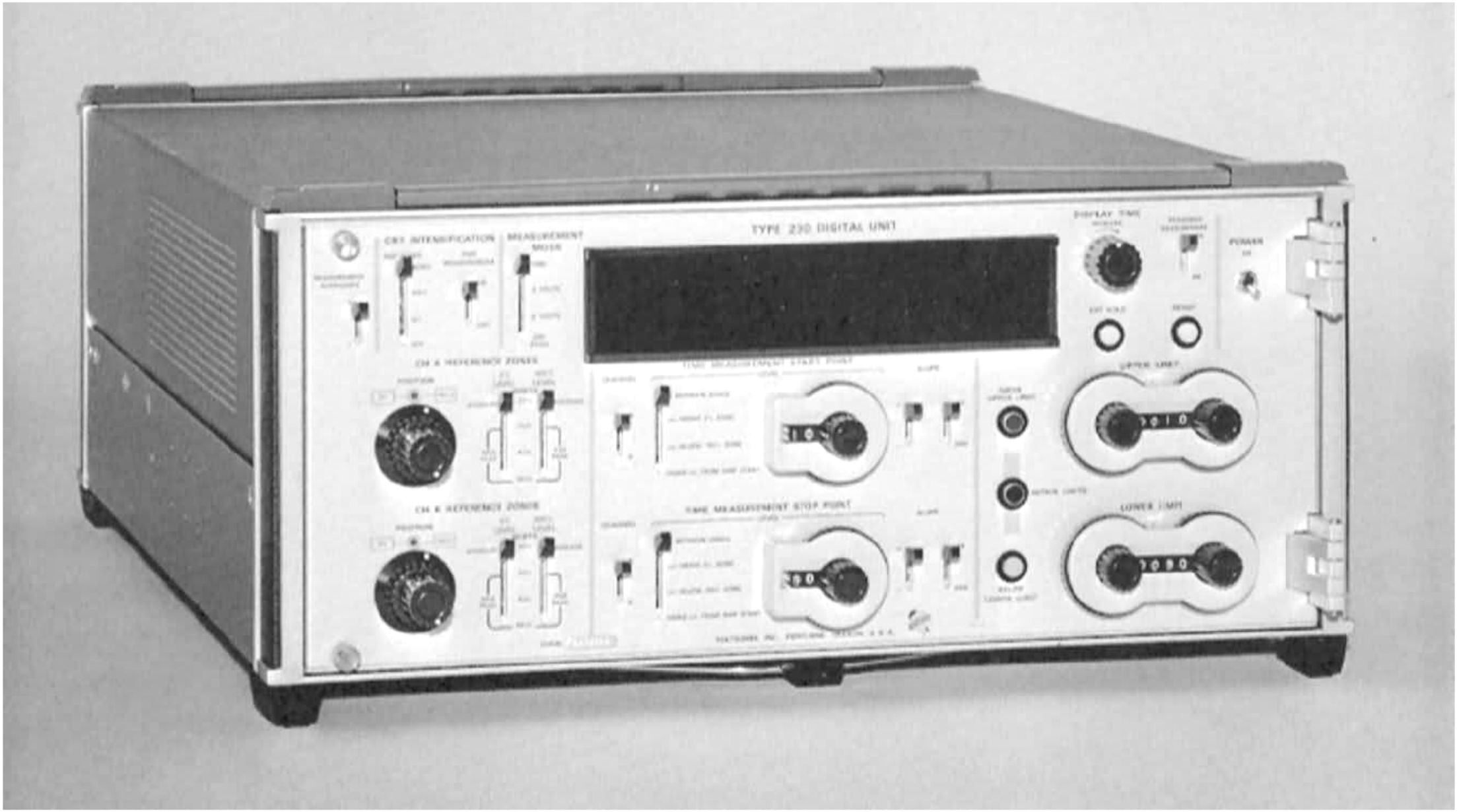

TYPE 230 DIGITAL UNIT
CRT INTENSIFICATION
MEASUREMENT MODE
CH A REFERENCE ZONES
CH B REFERENCE ZONES
TIME MEASUREMENT START POINT
TIME MEASUREMENT STOP POINT
DISPLAY TIME
POWER
UPPER LIMIT
LOWER LIMIT
3010
3080

SECTION 1
CHARACTERISTICS

General Information

The Type 230/R230 Digital Unit is designed for use with the Tektronix Type 568 Oscilloscope as part of a digital readout system for making automatic digital measurements of voltage, time between percentage points, and time between pulses on one or two waveforms. All functions of the Type 230 are programmable, making the instrument appropriate for applications requiring a variety of measurements that can be changed in rapid sequence. The Type 230 may also be operated from the front panel controls, although the functions of the instrument are limited as compared to those available with external programming. The Type 230 provides front panel readouts including + or —, unit of measure, and a 4-digit numerical readout. Go-no-go limits are also indicated. Rear panel connectors provide inputs for external programming, and binary-coded-decimal outputs of the front panel information.

The instrument is designed to operate over an ambient temperature range of 0° C to +60° C. Performance specifications given in this section apply over this temperature range after a 5-minute warmup period, provided the instrument has been calibrated at +25° C ±5° C. Additional information describing some characteristics and features is also included where needed in this portion of the manual. Characteristics given under Operational Information are not specifications in themselves and are not necessarily checked in the performance check or calibration procedure.

Information given in this instruction manual applies to both the Type 230 and Type R230 unless otherwise specified. The Type R230 is electrically identical to the Type 230, but is equipped with front panel pull handles and slide-out tracks for rackmounting in a standard 19-inch rack. Rackmounting instructions, a mechanical parts list and a dimensional drawing of the Type R230 are provided in Section 8.

Thoughout the text, each plug-in circuit card is referred to either by the circuit number of the plug (which constitutes the edge of the card) or by the circuit number of the jack into which the card is plugged. For example, the Buffer may be referred to either as P5 or J5. When reading the text, consider that these plug and jack circuit numbers are interchangeable.

OPERATING CHARACTERISTICS

Characteristics	Operating Information	
Input	External from a Tektronix Type 568 Oscilloscope.	
Units of Measure[1]		
Volts	Readout in millivolts (MV) and volts (V).	
Time	Readout in nanoseconds (NS), microseconds (μS), milliseconds (MS), and seconds (S).	
Numerical Range[1]	Readout from —3999 to +3999.	
Display Time[1]	Variable from 0.01 second to 10 seconds,	
Preset Limits Range[1]		
Upper	From —3999 to +3999	
Lower	From —3999 to +3999	
	Externally Programmed	Front Panel Operation
Time Measurement Start and Stop Point Range		
% Between Zones	0% to 159%	0% to 99%
Vertical Millimeters Offset	0 mm to 159 mm above or below the reference zone	0 mm to 99 mm above the 0% zone, 0 mm to 99 mm below the 100% zone.
	No more than 80 mm of offset is usable, since only 80 mm of vertical display is available.	
Horizontal Millimeters Offset	1 mm to 159 mm from sweep start. No more than 105 mm is usable.	1 mm to 99 mm from sweep start.

ELECTRICAL CHARACTERISTICS

Characteristics	Performance Specification
Zone Generators, Ch A and Ch B, 0% and 100%, P1 and P2.	
Zone Position	Horizontal increments of 0.5 major division from sweep start.
Accuracy	Within 1 minor division of position programmed.
Zone Width	0.3 cm, 2 cm, 4 cm or 10 cm (to end of sweep) from start of zone.

[1]**Digital readout from Nixie tubes on Type 230. All references to major or minor divisions of display refer to Analog readout from Type 568 CRT. Nixie Trademark Burroughs Corporation.**

Characteristics	Performance Specification
Accuracy	Within 1 mm when programmed for 0.3 cm width; within 10% when programmed for 2 cm or 4 cm width.
Memories, Ch A and Ch B, 0% and 100%, P3 and P4.	
Memory Output Level	−0.6 V to +5.4 V.
Accuracy	Within 6 mV of input voltage.
Leak Down	30 mV or less in 10 seconds.
Peak Charge Time	15 μs of zone or peak signal time.
Buffer, P5	
Ch A and Ch B Signal Gain	0.5 V/div output for 1.0 V/div input.
Output Level	+2.15 V ±0.10 V output for +10.0 V DC input.
5 V RAMP	
Gain	0.5 V/div ±0.5% for 5 V/div input; adjustable to 0.5 V/div ±0.2%.
Linearity	Within 1% of input linearity.
DC Level	0.0 V ±20 mV for 0.0 V input; adjustable to 0.0 V ±1 mV.
50 V RAMP	
Gain	Adjustable to give proper zone position at 9th graticule line.[2]
VOLTMETER RAMP	Adjustable, 5 mV/μs, 2.5 mV/μs, and 10 mV/μs.
Linearity	Within 0.25%.
Comparators, P6 and P7	
Signal Input Range	At least −1.0 V to +5.0 V.
Offset Voltage Out	±50 mV to ±4.95 V.
Accuracy	Within 0.25% ±2 mV of programmed offset.
Offset Tracking Accuracy	Within 1 mV of input reference, from +0.15 V to +4.15 V.
% Offset Gain	0% to 99% of voltage difference between 0% and 100% memory levels.
Accuracy	Within 0.25% ±2 mV of programmed voltage.
External Control	
Plus Trigger (J204-Pin 29)	Positive step of 4 volts or more, having a ristime of 1 microsecond or less.
Minus Trigger (J204-Pin 30)	Negative step of 4 volts or more, having a negative-going risetime of 1 microsecond or less.

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Performance Specification
Ambient Temperature Range	
Operating	0° C to +60° C
Non-operating	−40° C to +65° C
Maximum Altitude	
Operating	15,000 feet
Non-operating	50,000 feet
Vibration (Operating)	Performs within specifications after being vibrated for 15 minutes along each axis at frequencies from 10 c/s to 50 c/s and accelerations up to 1.9 g.
Shock (Non-operating)	Performs within specifications after being subjected to guillotine type shocks of 30 g's one-half sine, 11 millisecond duration. One shock each direction along each axis (total of 6 shocks).
Transportation (Non-operating) Vibration	Performs within specifications after transportation package has been vibrated for 1 hour at accelerations up to 1 g.
Drop Test	Performs within specifications after transportation package has been dropped from a height of 30 inches on one corner, on each edge radiating from that corner and on each flat side of the package.

[2]Model 1 not independently adjustable.

MECHANICAL CHARACTERISTICS

Characteristics	Description
Construction	
Chassis and cabinet	Aluminum alloy
Front panel	Anodized aluminum alloy
Circuit cards	Epoxy laminate with etched wiring
Approximate Dimensions	
Type 230	
Height	8 inches, including feet
Width	16⅞ inches
Depth	22 inches, including knobs and rear-panel feet
Type R230	
Height	7 inches
Width	16⅞ inches; fits into a standard 19 inch rack
Depth	22¾ inches, including handles and rear-panel feet
Connectors	
Input, programming and readout (rear panel)	Microribbon type 36-terminal jacks (total of 6)
Ventilation	Forced filtered air; overheat protection by means of thermal relay.

POWER SOURCE ELECTRICAL REQUIREMENTS

Characteristic	AC RMS Operating Range	Operational Information
Line Voltage		Power connection changed by means of rear-panel line-selector assembly; normally set for 115 VAC. Medium operating range when shipped from the factory.
Low		
100 VAC Nominal	90 volts to 110 volts	
200 VAC Nominal	180 volts to 220 volts	
Medium		
115 VAC Nominal	104 volts to 126 volts	
230 VAC Nominal	208 volts to 252 volts	
High		
124 VAC Nominal	112 volts to 136 volts	
248 VAC Nominal	224 volts to 272 volts	
Line Frequency	48 to 66 Hz	
Power Consumption		130 W maximum

SECTION 3
TYPE 230 PROGRAMMING INSTRUCTIONS

General Information

The 230 has a total of 105 programming inputs available at the external connections located at the rear of the instrument. There are also 52 readout lines available. The characteristics of the external program input lines are as follows:

TRUE

For a TRUE indication, the program inputs are particularly adapted to saturated transistor collector inputs, and will easily function with ground closures by relays. To ensure that no feedback or "sneak path" occurs, a series diode should be inserted at each program input in use. The ideal logic level which constitutes a logical ONE is ground; the most positive level which constitutes a logical ONE is +2 volts.

FALSE

To program a ZERO (FALSE), any program line may be left open. If a line is held at a specific level when programmed FALSE, the holding level must be more positive than +6 volts to constitute a logical ZERO. Pullup on any program line should not exceed +12 volts. A line providing +12 volts at 350 mA is available at J204 pin 23.

Jacks J201, J202, and J203 are located on the Type 230 rear panel for external program inputs. Jack J204 contains program inputs, Type 230 power supply voltages for external use, and controlling outputs from the Type 230. Jack J301 provides measurement results or readout to external devices. Jack J101 provides the necessary interconnections from the Type 230 to the Type 568 and vice-versa. (For physical location of the jacks see Fig. 3-1).

Program Common Lines

Pins 17, 18, 35, and 36 of J201, J202, and J203 are program common outputs. J204 pin 17 is also a program common output. All of the 13 program common lines join at the Type 230 front panel MEASUREMENT MODE switch. Only when the MEASUREMENT MODE switch is in the EXT PROG position will the program common lines enable the external program inputs.

Effective with serial number B13050 and above, all Type 230/R230 instruments are equipped with keyed rear panel connectors. This change is to prevent damage to the instrument. The cables used on instruments serial numbered below B130540 will not fit modified instruments, but keyed cables will fit unmodified instruments. Keyed cables for modified Type 230/R230 are available under the following Tektronix part numbers:

Cables for J201-J202-J203-J301	012-0131-00
Cable for J204	012-0131-01
Cable for J101	012-0119-01

EXTERNAL PROGRAM LINES

Table 3-1 lists all of the 105 external program inputs. Since some of the lines provide a program function in either TRUE or FALSE condition, each line will be examined in each condition. Special notations are provided where combinations of lines program an additional function.

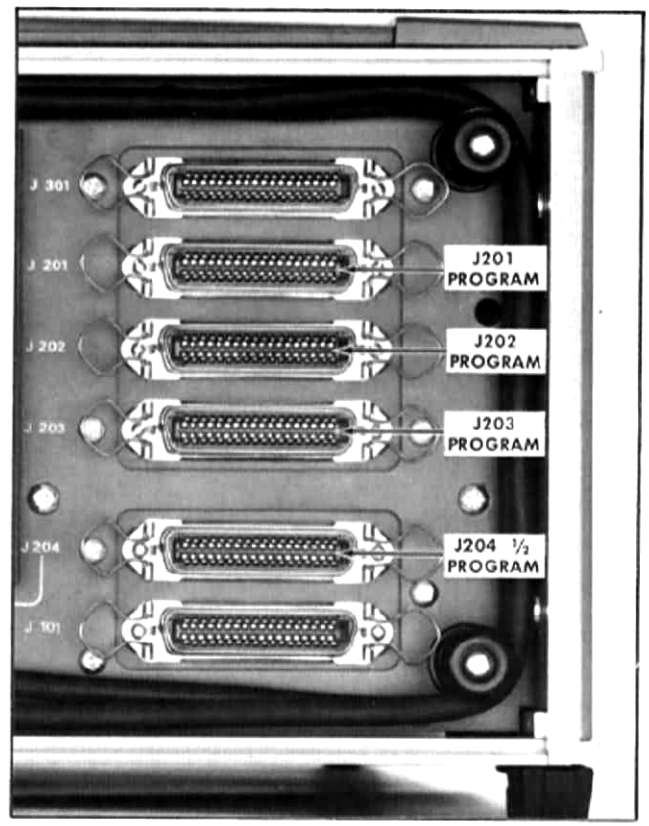


Fig. 3-1. Type 230 external connectors.

TABLE 3-1
External Program Inputs

TITLE	PIN NO. (J201)	TRUE	FALSE
A 0% POSITION 8	1	Provides 8 cm position command to the A 0% Zone Generator.	No program
A 0% POSITION 4	2	Provides 4 cm position command to the A 0% Zone Generator.	No program

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J201)	TRUE	FALSE
A 0% POSITION 2	3	Provides 2 cm position command to the A 0% Zone Generator.	No program
A 0% POSITION 1	4	Provides 1 cm position command to the A 0% Zone Generator.	No program
A 0% POSITION .5	5	Provides .5 cm position command to the A 0% Zone Generator.	No program

NOTE

Although only 9.5 cm of zone position may be programmed from the front panel, externally the zone can be programmed to 15.5 cm. Any programmed position of 12 (8 cm +4 cm) through 15.5 cm (8 cm + 4 cm + 2 cm + 1 cm + .5 cm) will Cause the previous memory information to be retained subsequent measurement. If the zone position is programmed past the sweep end and before position 12, measurement cycles will no longer occur since the memories cannot assume a charge.

A 0% WIDTH 4 cm	6	Shifts the A 0% Memory from AVERAGE to PEAK; zone width changes to 4 cm.	Programs the A 0% memory to AVERAGE; zone width is .3 cm.
A 0% WIDTH 2 cm	7	Shifts the A 0% Memory from AVERAGE to PEAK; zone width changes to 2 cm.	Programs the A 0% memory to AVERAGE; zone width is .3 cm.

NOTE

If both 4 cm and 2 cm are programmed TRUE, the remainder of the sweep intensifies from the start position of the zone. If either one of the two are programmed TRUE, the sweep is intensified from the programmed zone position for the programmed width or to the end of the sweep, whichever occurs first.

VOLTS	8	Programs the Type 230 to a voltage measurement mode, disables the horizontal decimals and units plug-in common lines; enables the vertical decimals and units plug-in common lines.	Programs the Type 230 to a time measurement mode; enables the horizontal decimals and units plug-in common lines; disables the vertical decimals and units plug-in lines.
A 100% POSITION 8	9	The position and width programs for the A 100% zone perform the same function as the position and width program lines for the A 0% zone.	
A 100% POSITION 4	10		
A 100% POSITION 2	11		
A 100% POSITION 1	12		
A 100% POSITION .5	13		
A 100% WIDTH 4 cm	14		
A 100% WIDTH 2 cm	15		
A CHOP	16	Enables A chopper drive for external chopper synchronization.	
B 0% POSITION 8	19	The position and width programs for the B 0% and B 100% zones perform the same function as the position and width program lines for the A 0% and A 100% zones.	
B 0% POSITION 4	20		
B 0% POSITION 2	21		
B 0% POSITION 1	22		
B 0% POSITION .5	23		
B 0% WIDTH 4 cm	24		
B 0% WIDTH 2 cm	25		
MEASURE AVERAGE	26	Programs a readout equal to the average value of eight consecutive measurements. Used for noisy signals to reduce error.	Programs the readout to indicate the value of one measurement.

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J201)	TRUE	FALSE
B 100% POSITION 8	27	See B 0% POSITION for B 100% position and width characteristics.	
B 100% POSITION 4	28		
B 100% POSITION 2	29		
B 100% POSITION 1	30		
B 100% POSITION .5	31		
B 100% WIDTH 4 cm	32		
B 100% WIDTH 2 cm	33		
B CHOP	34	Enables B chopper drive for external chopper synchronization.	

TITLE	PIN NO. (J202)	TRUE	FALSE
(START) B CHANNEL	1	Start point on B channel.	Start point on A channel.
(START) HORIZONTAL mm	2	Start Comparator fires at OFFSET mm from sweep start. (Independent of signal).	Start comparator fires as a function of the signal.
(START) % BETWEEN	3	Start Comparator fires at the signal level expressed as percentage.	Start comparator fires on the signal level in offset mm vertically displaced from the memory.
(START) mm BELOW	4	Start Comparator fires at the amount of programmed start offset below the selected reference zone.	Start Comparator fires at the amount of programmed start offset above the selected reference zone.
(START) OFFSET 100	5	References the Start Comparator offset from the 100% zone.	References the Start Comparator offset from the 0% zone.
(START) MINUS SLOPE	6	Start Comparator fires on a minus slope of the analog display.	Start Comparator fires on a plus slope of the analog display.
(START) SECOND SLOPE	7	Start Comparator fires on a 2nd slope of the analog display (either plus or minus 2nd slope as programmed).	Start Comparator fires on a 1st slope of the analog display (either plus or minus 1st slope as programmed).
COUNTER RESET INHIBIT	8	Programs the Type 230 counter to accumulate a series of measurements without resetting or clearing the previous measurement information. Additive readout will still occur at the end of each measurement.	Normal operation
(START) OFFSET 80	9	Start Comparator fires at one of three references: a. Signal—offset mm or offset % may be selected. b. Voltmeter ramp—offset mm or offset % may be selected. c. Sweep ramp (Horizontal mm)—only offset mm may be used.	No program

NOTE

OFFSET program lines are additive. It is possible to program 159 increments (% or mm) through the external programming inputs. Since the Type 230 is not designed to measure out-of-graticule information, no more than a maximum of 80 mm would be useful. The offset percentage above 100% is useful for the measurement of overshoot. Although the sum of the offset lines is greater than 159, the first decade of the offset is constructed to provide no more than nine.

(START) OFFSET 40	10	Programs 40% or 40 mm	No program
(START) OFFSET 20	11	Programs 20% or 20 mm	No program
(START) OFFSET 10	12	Programs 10% or 10 mm	No program

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J202)	TRUE	FALSE
(START) OFFSET 8	13	Programs 8% or 8 mm	No program
(START) OFFSET 4	14	Programs 4% or 4 mm	No program
(START) OFFSET 2	15	Programs 2% or 2 mm	No program
(START) OFFSET 1	16	Programs 1% or 1 mm	No program
(STOP) B CHANNEL	19	Pins 19 through 25 perform the same programming functions that pins 1 through 7 perform, with the exception that pins 19 through 25 control the Stop Comparator.	
(STOP) HORIZONTAL mm	20		
(STOP) % BETWEEN	21		
(STOP) mm BELOW	22		
(STOP) OFFSET 100	23		
(STOP) MINUS SLOPE	24		
(STOP) SECOND SLOPE	25		
EXTERNAL SCALE	26	Disables internal scaling (See J204)	Enables internal scaling

NOTE

If EXT SCALE is TRUE, the front panel readout will not indicate the correct scaling for the measurement. Programming of the decimals and units externally is required.

(STOP) OFFSET 80	27	Pins 27 through 34 program functions identical to those of pins 9 through 16, with the exception that pins 27 through 34 program the Stop Comparator.
(STOP) OFFSET 40	28	
(STOP) OFFSET 20	29	
(STOP) OFFSET 10	30	
(STOP) OFFSET 8	31	
(STOP) OFFSET 4	32	
(STOP) OFFSET 2	33	
(STOP) OFFSET 1	34	

TITLE	PIN NO. (J203)	TRUE	FALSE
EXTERNAL HORIZONTAL ÷ 2	1	Divides readout by two (See J204).	Programs normal clock rate.
UPPER MINUS	2	Programs the upper limit level to be a negative number.	Programs the upper limit level to be a positive number.
UPPER LIMIT 2000	3	Programs the upper limit level to an algebraic value of 2000.	No program
UPPER LIMIT 1000	4	Programs 1000	No program
UPPER LIMIT 800	5	Programs 800	No program
UPPER LIMIT 400	6	Programs 400	No program
UPPER LIMIT 200	7	Programs 200	No program
UPPER LIMIT 100	8	Programs 100	No program
UPPER LIMIT 80	9	Programs 80	No program
UPPER LIMIT 40	10	Programs 40	No program
UPPER LIMIT 20	11	Programs 20	No program
UPPER LIMIT 10	12	Programs 10	No program
UPPER LIMIT 8	13	Programs 8	No program
UPPER LIMIT 4	14	Programs 4	No program
UPPER LIMIT 2	15	Programs 2	No program
UPPER LIMIT 1	16	Programs 1	No program

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J203)	TRUE	FALSE

NOTE

The limit level inputs are additive so that a limit of + or — 3999 may be programmed. Care must be taken to avoid programming any decade of either the upper or lower limits to a value greater than 9. For example, the combination of 800 plus 100 is permissible, but the combination of 800 plus 200, 800 plus 400, or any combination totalling over 900 will result in an erroneous limit readout.

EXTERNAL HORIZONTAL ÷ 5	19	Multiplies readout by two; shifts readout decimal to left one place. (See J204).	Programs normal count and decimal position.
LOWER MINUS	20	Programs the lower limit level to be a negative number.	Programs a positive number.
LOWER LIMIT 2000	21	Programs the lower limit level to lower an algebraic value of 2000.	No program
LOWER LIMIT 1000	22	Programs 1000	No program
LOWER LIMIT 800	23	Programs 800	No program
LOWER LIMIT 400	24	Programs 400	No program
LOWER LIMIT 200	25	Programs 200	No program
LOWER LIMIT 100	26	Programs 100	No program
LOWER LIMIT 80	27	Programs 80	No program
LOWER LIMIT 40	28	Programs 40	No program
LOWER LIMIT 20	29	Programs 20	No program
LOWER LIMIT 10	30	Programs 10	No program
LOWER LIMIT 8	31	Programs 8	No program
LOWER LIMIT 4	32	Programs 4	No program
LOWER LIMIT 2	33	Programs 2	No program
LOWER LIMIT 1	34	Programs 1	No program

NOTE

The limit level circuits are constructed to be sensitive to polarity differences as well as differences in absolute value. This means that it is possible and sometimes desirable to program a +0000 or a —0000. It should be noted that the circuit views a + 0000 as being greater in algebraic value than a — 0000. Any count that occurs without a polarity sign is treated as plus, and if the Type 230 is in a cumulative measurement mode (average-of-eight; counter reset inhibit) the counter adds all numbers arithmetically regardless of polarity. When this mode is present, enough jitter may be present to cause the equipment to indicate a readout of ±. The limit circuit sees ± as —, so the entire readout will be meaningless for that measurement.

TITLE	PIN NO. (J204)	TRUE	FALSE
DECIMAL 2	1	Programs the 2nd readout decimal from the left to light.	When DECIMAL 2, DECIMAL 3, and DECIMAL 4 are all FALSE, the fifth decimal light from the left will be programmed ON (except as noted below).
DECIMAL 3	2	Programs the 3rd readout decimal from the left to light.	
DECIMAL 4	3	Programs the 4th readout decimal from the left to light.	

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J204)	TRUE	FALSE
		NOTE Scaling the readout of the Type 230 by external programming is done by programming the decimal and units nixies with the following exceptions, variations, or conditions: When EXT SCALE is FALSE, the vertical and horizontal plug-ins in the Type 568 control the scaling of the readout, but do not forbid or inhibit additional scaling from the external program inputs. In most cases additional scaling would not be desired, but if attenuators were placed between the vertical input and the signal source the external scaling could be used to compensate the readout. When EXT SCALE is TRUE, internal scaling is disabled. Without some external scaling provided, the readout will indicate an accumulation of measurement without any decimals or units to indicate magnitude of measurement. EXT ÷ 5 is used to multiply the readout by two. This enables the programmer to compensate for a change in a plug-in attenuator or sweep range. EXT ÷ 5 also shifts the decimal one place to the left when TRUE. In order to compensate for this characteristic, programming the decimal point position should be adjusted if necessary to provide the correct decimal readout. EXT ÷ 2 divides the readout by two, so scaling should also compensate for the division if needed. The decimal scaling of the Type 230 has an inhibiting function so that no two decimals may appear. The units scaling has no inhibiting function, and it is possible for all units to be energized at once. The operator should note this when programming the instrument and avoid programming multiple unit lines unless so specified by the program.	
NIXIE 'v'	4	Programs front panel readout nixie 'v' ON	No program
NIXIE 's'	5	Programs front panel readout nixie 's' ON	No program
NIXIE 'm'	6	Programs front panel readout nixie 'm' ON	No program
NIXIE 'μ'	7	Programs front panel readout nixie 'μ' ON	No program
NIXIE 'N'	8	Programs front panel readout nixie 'N' ON	No program
		NOTE If either units or decimals are to be programmed externally, EXT SCALE should be programmed TRUE to prevent multiple display of units or decimals.	
HIGH SPEED PROGRAM	9	Reduces time between measurements.	Normal measurement speed.
A CHOP[1]	15	Enables A chopper drive for external chopper synchronization.	Disables A chopper drive.
B CHOP[1]	16	Enables B chopper drive for external chopper synchronization.	Disables B chopper drive.

The remainder of J204 is composed of external control outputs. Jacks J101, J301, and the remainder of J204 will be discussed after the programming instructions.

FIRST-TIME PROGRAMMING

Since the majority of the external functions are controllable from the front panel of the Type 230, an easy way to set up the first program is to "front-panel program" the instrument to perform a desired measurement. After determining that the measurement succeeds on a front panel basis, the operator can then proceed with externally programming the Type 230. Table 3-2 lists all front panel functions and their external program counterparts. This will allow the operator to cross-reference a front panel setup to an external program.

TABLE 3-2

Program Line Equivalents of Front Panel Settings

FRONT PANEL	CORRESPONDING PROGRAM LINE
MEASUREMENT AVERAGING 1:8	MEASURE AVERAGE: J201-26
CRT INTENSIFICATION	No External Counterparts

[1]This line used only on instruments SN 360 and up.

TABLE 3-2 *(cont)*

FRONT PANEL	CORRESPONDING PROGRAM LINE
MEASUREMENT MODE:	
TIME	VOLTS FALSE: J201-8
A VOLTS	VOLTS: J201-8. B CHANNEL FALSE: J202-1
B VOLTS	VOLTS: J201-8. B CHANNEL: J202-1
EXT PROG	No Counterpart

NOTE

Offset is used in External Program Volts, but not in Front Panel Volts.

DISPLAY TIME	No Counterpart
TRIGGERED MEASUREMENT	No Counterpart
CH A REFERENCE ZONES	
POSITION 0%	A 0% Position 8, 4, 2, 1, .5: J201-1, 2, 3, 4, 5
POSITION 100%	A 100% Position 8, 4, 2, 1,.5: J201-9, 10, 11, 12, 13
0% LEVEL	
AVERAGE .3 cm	No Program: J201-6, 7 FALSE
NEG PEAK 2 cm	A 0% Width 2 cm: J201-7
NEG PEAK 4 cm	A 0% Width 4 cm: J201-6
NEG PEAK 10 cm	A 0% Width 2 cm, 4 cm: J201-7, 6
100% LEVEL	
AVERAGE .3 cm	No Program: J201-14, 15 FALSE
POS PEAK 2 cm	A 100% Width 2 cm: J201-15
POS PEAK 4 cm	A 100% Width 4 cm: J201-14
POS PEAK 10 cm	A 100% Width 2 cm, 4 cm: J201-15, 14
CH B REFERENCE ZONES	
POSITION 0%	B 0% Position 8, 4, 2, 1, .5: J201-19, 20, 21, 22, 23
POSITION 100%	B 100% Position 8, 4, 2, 1, .5: J201-27, 28, 29, 30, 31
0% LEVEL	
AVERAGE .3 cm	No Program: J201-24, 25 FALSE
NEG PEAK 2 cm	B 0% Width 2 cm: J201-25
NEG PEAK 4 cm	B 0% Width 4 cm: J201-24
NEG PEAK 10 cm	B 0% Width 2 cm, 4 cm: J201-25, 24
100% LEVEL	
AVERAGE .3 cm	No Program: J201-32, 33 FALSE
POS PEAK 2 cm	B 100% Width 2 cm: J201-33
POS PEAK 4 cm	B 100% Width 4 cm: J201-32
POS PEAK 10 cm	B 100% Width 2 cm, 4 cm: J201-33, 32
TIME MEASUREMENT START POINT	
CHANNEL	
A	B CHANNEL FALSE: J202-1
B	B CHANNEL: J202-1
LEVEL	
% BETWEEN ZONES	% BETWEEN: J202-3
mm ABOVE 0% ZONE	mm BELOW FALSE: J202-4
mm BELOW 100% ZONE	mm BELOW: J202-4 (OFFSET from 100% zone)
HORIZ mm FROM SWP START	HORIZ mm: J202-2 (normally first plus slope)
OFFSET DIALS (0-99)	OFFSET 80 through 1: J202-9 through 16
SLOPE +	MINUS SLOPE FALSE: J202-6
—	MINUS SLOPE: J202-6
1st	2nd SLOPE FALSE: J202-7
2nd	2nd SLOPE: J202-7

TABLE 3-2 *(cont)*

FRONT PANEL		CORRESPONDING PROGRAM LINE
TIME MEASUREMENT STOP POINT		
CHANNEL		
A		B CHANNEL FALSE: J202-19
B		B CHANNEL: J202-19
LEVEL		
% BETWEEN ZONES		% BETWEEN: J202-21
mm ABOVE 0% ZONE		mm BELOW FALSE: J202-22
mm BELOW 100% ZONE		mm BELOW: J202-22
HORIZ mm FROM SWP START		HORIZ mm: J202-20
OFFSET DIALS (0-99)		OFFSET 80 through 1: J202-27 through 34
SLOPE	+	MINUS SLOPE FALSE: J202-24
	—	MINUS SLOPE: J202-24
	1st	2nd SLOPE FALSE: J202-25
	2nd	2nd SLOPE: J202-25
UPPER LIMIT DIALS		UPPER MINUS and UPPER 2000 through 1: J203-2 through 16
LOWER LIMIT DIALS		LOWER MINUS and LOWER 2000 through 1: J203-20 through 34

NOTE

Whenever the Type 230 is operated with the MEASUREMENT MODE switch in the EXT PROG position, it is advisable to position the TRIGGERED MEASUREMENT switch ON. This will help in preventing lockup of the measurement cycle. When the TRIGGERED MEASUREMENT switch is ON, a plus or minus trigger must be applied through rear-panel jack J204 to initiate a measurement. This trigger must be synchronized with the programming device so that a change in program does not occur until after PRINT COMMAND from the Type 230 moves high and returns low, signifying the end of measurement and readiness for a new program.

SAMPLE PROGRAMS

The following pages show a group of example programs to aid the operator in first-time programming of the Type 230. All of the program input lines have been conveniently arranged in an 8-4-2-1 order. Each four-bit (line) segment is called a character. Since there are 105 bits (lines) programmable, there are 27 characters in the program chart below (Notice that the 27th character has only one bit; bit eight). The entire group of characters is called a word. In addition to the three program examples mentioned above, a blank program chart is included for convenient reproduction (see Fig. 3-7). The blank program is arranged in the same fashion as the example program charts. The character number is at the far left of the chart. Moving right, the eight, four, two, and one bits are tabulated. The two columns to the right of the bit spaces are for the programs, two to each worksheet. At the far right the program input lines appear in the same order as the bits. For example, if the operator did not wish to program the other three bits in character 6 TRUE, he would write 0001 in the program space adjacent to Character 6. Moving to the right at the Character 6 level, the program input line corresponding to Character 6, Bit 1 is Jack J201, pin 26.

Example Program One (See Fig. 3-4)

The first example deals with a voltage measurement of channel A information. Refer to Fig. 3-2 for a pictorial representation of the information to be measured. The Type 568 vertical plug-in has been set to display about 6 divisions of signal vertical deflection on channel A only. The Type 568 horizontal plug-in has been triggered on the plus slope of the signal, and the TIME/DIV has been set to cause the display as shown in Fig. 3-2. Since the display rises from 0% to 100% amplitude from the fifth to the seventh division, the program input may be only concerned with the 5th to 7th division area. The program for this measurement is as follows: (See example program chart No. 1, Fig. 3-3).

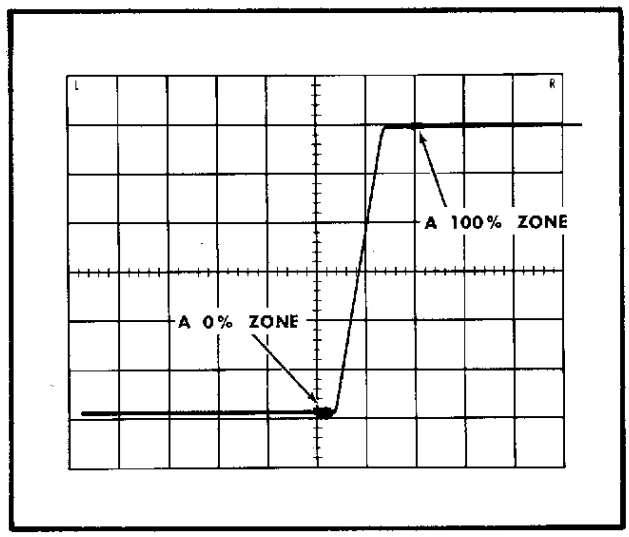


Fig. 3-2. Information to be measured in Example Program 1.

Character 1:	0101	This places the A 0% zone and the start of measurement at the fifth graticule division.
Character 2:	0001	Since we wish the memories to charge to average, bits 4 and 2 are FALSE. A voltage measurement is desired, so bit 1 is TRUE.

CHARACTER	8	4	2	1	PROGRAM 1	PROGRAM 2	J201 PINS 8	4	2	1
1	A 0% POS. 8	4	2	1	0101	0001	1	2	3	4
2	A 0% POS. .5	A 0% Wid. 4 cm	2 cm	VOLTS	0001	0000	5	6	7	8
3	A 100% POS. 8	4	2	1	0111	0101	9	10	11	12
4	A 100% POS. .5	A 100% Wid. 4 cm	2 cm	A CHOP	0000	0000	13	14	15	16
5	B 0% POS. 8	4	2	1	0000	0000	19	20	21	22
6	B 0% POS. .5	B 0% Wid. 4 cm	2 cm	MEASURE AVE.	0000	0000	23	24	25	26
7	B 100% POS. 8	4	2	1	0000	0000	27	28	29	30
8	B 100% POS. .5	B 100% Wid. 4 cm	2 cm	B CHOP	0000	0000	31	32	33	34
							J202			
9	(START) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0000	0010	1	2	3	4
10	(START) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	COUNTER RESET INHIBIT	0000	0000	5	6	7	8
11	(START) OFFSET 80	40	20	10	0000	0001	9	10	11	12
12	OFFSET 8	4	2	1	0000	0000	13	14	15	16
13	(STOP) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0000	1001	19	20	21	22
14	(STOP) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	EXT SCALE	1000	1100	23	24	25	26
15	(STOP) OFFSET 80	40	20	10	0000	0001	27	28	29	30
16	(STOP) OFFSET 8	4	2	1	0000	0101	31	32	33	34
							J203			
17	EXT HORIZ ÷ 2	UPPER MINUS	UPPER LIMIT 2000	1000	0000	0000	1	2	3	4
18	800	400	200	100	0110	0011	5	6	7	8
19	80	40	20	10	0011	1000	9	10	11	12
20	8	4	2	1	0000	0101	13	14	15	16
21	EXT HORIZ ÷ 5	LOWER MINUS	LOWER LIMIT 2000	1000	0000	0000	19	20	21	22
22	800	400	200	100	0101	0011	23	24	25	26
23	80	40	20	10	0111	0001	27	28	29	30
24	8	4	2	1	0000	0101	31	32	33	34
							J204			
25	PROG DEC 2	3	4	NIXIE 'V'	0000	0000	1	2	3	4
26	NIXIE S	NIXIE M	NIXIE 'μ'	NIXIE 'N'	0000	0000	5	6	7	8
27	HIGH SPEED PGM		A CHOP[2]	B CHOP[2]	0000	0000	9		15	16

NOTE: GROUND CLOSURE OF A PROGRAM LINE CONSTITUTES A LOGICAL ONE (TRUE); ANY OPEN LINE IS A LOGICAL ZERO (FALSE).

[2]Below SN 360 these bits are not used.

Fig. 3-3. Example Programs 1 and 2.

Character 3:	0111	Character 3, Bits 4, 2, and 1 position the A 100% Zone at the 7th display cm; the A 100% memory charges to the average value of the signal during the ZONE.
Character 4:	0000	No program desired.
Character 5:	0000	No Program.
Character 6:	0000	No program desired. (Bit 1, MEASURE AVERAGE is usually used for an unstable display. Since no problem exists, Bit 1 is left FALSE).
Character 7:	0000	No program. Characters 5 and 7 are programmed 0000 to allow the B memories to charge and discharge with each measurement cycle of the instrument. If more than ten centimeters of zone position is programmed, and a memory is not allowed to charge on a previous cycle, the measurement cycle may lock up.
Character 8:	0000	No program desired.
Character 9:	0000	Programming Bit 8 FALSE causes the Start Comparator to fire on the A channel information. The other three bits concern time measurement programming.
Character 10:	0000	No program desired.
Character 11:	0000	No program desired.
Character 12:	0000	No program desired.
Character 13:	0000	Programming Bit 8 FALSE causes the stop comparator to fire on the A channel information. The other three bits concern time measurement programming.
Character 14:	1000	Bit 8 is programmed TRUE to fire the stop Comparator at the offset % from the 100% zone. Bit 1 is programmed FALSE to enable plug-in commons and allow the plug-ins to control the readout decimals and units.
Character 15:	0000	No program desired.
Character 16:	0000	No program desired.
Character 17:	0000	Programming Bit 4 FALSE causes the upper limit level to be a positive number.
Character 18:	0110	Since the display is to read out approximately +06.00 V, assume that a tolerance of ±5% is imposed on the measurement. The sum of Character 18, Bits 4 and 2; Character 19, Bits 2 and 1 equals 0630. +0630 is the maximum value of measurement that may occur without an indication of above upper limit level.
Character 19:	0011	
Character 20:	0000	
Character 21:	0000	Programming Bit 4 FALSE causes the lower limit level to be a positive number.
Character 22:	0101	Note the explanation for Characters 18, 19, and 20. The desired measurement should not exceed 5% from + 06.00 V, so the lower limit level is programmed to + 0570.
Character 23:	0111	
Character 24:	0000	
Character 25:	0000	No program desired.
Character 26:	0000	No program desired.
Character 27:	0000	No program desired.

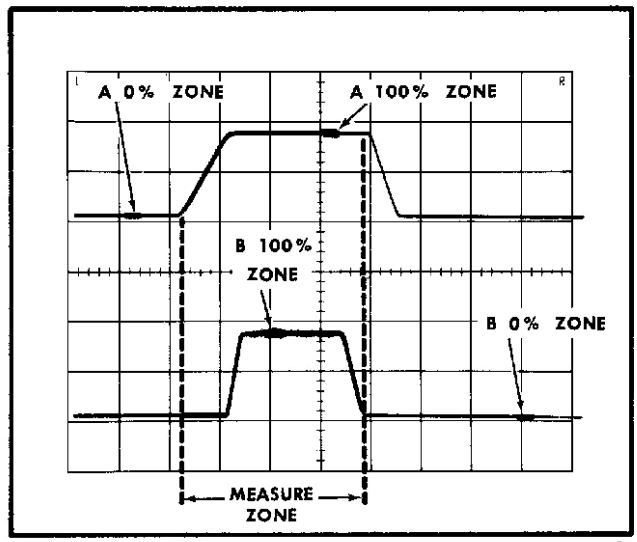


Fig. 3-4. Measurement information included in Example Program 2.

Example Program Two

The second example shows how to set up a time measurement program. In addition to this explanation, the second column of sample program chart No. 1 (Fig. 3-3) shows the program setup. Refer also to Fig. 3-4 for a photograph of the signal being measured. This program is a time measurement between two events; one on channel A, the other on channel B. The Type 568 vertical plug-in is set at A and B with the Type 568 display as shown in Fig. 3-4. The Type 568 horizontal plug-in is set for 100 dots per division to display the events shown in Fig. 3-4. The objective of this measurement is to measure the time difference between 10% up on the A channel event to 15 mm down from the top of the B channel event. In other words, we wish to measure from the start of the A channel event to the end of the B channel event. Note that the A channel event begins its rise at the 2nd centimeter of display, and begins to fall at about 6.5 cm of display. The B channel event begins its rise at the 3 cm point, and starts to fall at the 5 cm point. This information should be used for programming zone positioning. The program word by characters is as follows:

Character 1:	0001	Bit 1 is TRUE to place the A 0% zone at the first cm of display on the A trace.
Character 2:	0000	No program desired.
Character 3:	0101	Bits 4 and 1 are TRUE to place the A 100% zone at the fifth cm of display on the A trace.
Character 4:	0000	No program desired.
Character 5:	1001	Bits 8 and 1 position the B 0% zone at the ninth cm of display on the B trace.

Character 6:	0000	No program desired.
Character 7:	0100	Bit 4 positions the B 100% zone at the fourth cm of the B trace.
Character 8:	0000	No program desired.
Character 9:	0010	Bit 8 FALSE fires the start comparison on the A channel; Bit 2 TRUE places the comparison at a percentage of the position between zones as determined by OFFSET (characters 11 and 12).
Character 10:	0000	Bits 4 and 2 FALSE cause the start comparison point to occur on the first plus slope.
Character 11:	0001	Bit 1 TRUE causes the start comparison to occur at 10% above the 0% zone.
Character 12:	0000	No program desired.
Character 13:	1001	Bit 8 TRUE selects B channel for the stop comparison point, Bit 1 TRUE places the stop comparison point at Offset mm below the reference zone.
Character 14:	1100	Bit 8 TRUE selects the 100% zone as the stop offset reference; Bit 4 TRUE and Bit 2 FALSE selects the first minus slope for the stop comparison point.
Character 15:	0001	Character 15, Bit 1 and Character 16, Bits 4 and 1 TRUE make a sum of 15 mm offset which causes the stop comparison point to occur 15 mm down the first minus slope.
Character 16:	0101	
Character 17:	0000	Bit 4 FALSE causes a plus upper limit.
Character 18:	0011	Assuming a tolerance of plus or minus 10% for this measurement, the TRUE bits in characters 18, 19, and 20 sum up to an upper limit level of +0385, since the approximate length of the desired measurement is 350 microseconds (100 dots/cm, 3.5 cm, and therefore 350 dots).
Character 19:	1000	
Character 20:	0101	
Character 21:	0000	Bit 4 FALSE selects a positive lower limit level.
Character 22:	0011	The TRUE bits in Characters 22, 23, and 24 sum the lower limit level to +0315, which equals the desired measurement minus the 10% tolerance.
Character 23:	0001	
Character 24:	0101	
Character 25:	0000	No program desired for characters 25, 26 and 27 since external scaling is not used for this measurement. Although an equivalent-time sampling plug-in unit is being used for this measurement, no need for speedup of the sweep is indicated in this program.
Character 26:	0000	
Character 27:	0000	

Example Program Three

The third example program illustrates how a pair of consecutive measurements may be made to determine the exact time of a peak amplitude occurrence. Referring to Fig. 3-5, a pulse-type signal is shown with its peak occurring at about the fifth cm of display. The time (horizontal mm) from the sweep start to the 90% point on the rise of the signal is measured on the first program. The time from the sweep start to the 90% point on the fall of the signal is measured on the second program. By accumulating the count from both measurements and dividing them by two, the time position of the peak from the start of the sweep may be determined. The second measurement is pictured in Fig. 3-5b. The external program is shown in example program number three (Fig. 3-6). An explanation of the measurement programs by character follows:

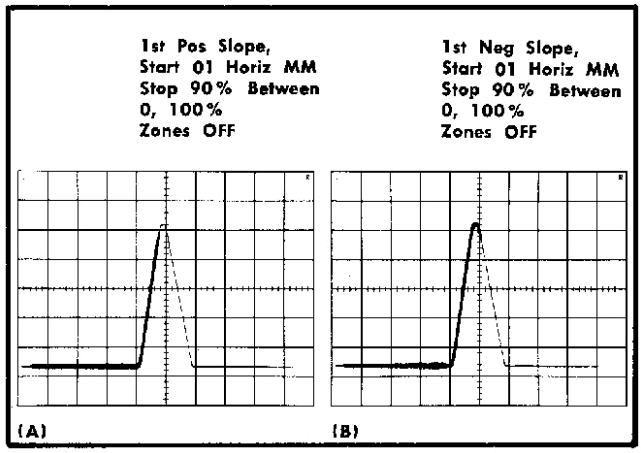


Fig. 3-5. Measurement information included in (A) Example Program 3 and (B) Example Program 4.

Character 1:	0000	No program desired.
Character 2:	1000	A 0% (Average) zone positioned at the .5 cm point on the display.
Character 3:	0001	Characters 3 and 4 program the A 100% memory to charge to the maximum positive peak of the display from the 1.5 cm position to the end of the sweep.
Character 4:	1110	
Character 5:	0000	No program desired.
Character 6:	0000	No program desired.
Character 7:	0000	No program desired.
Character 8:	0000	No program desired.
Character 9:	0100	Selects start comparison on Horizontal mm from sweep start.
Character 10:	0000	Selects start comparison at first plus slope of the signal.
Character 11:	0000	No program desired.
Character 12:	0001	Programs 1 mm from sweep start.
Character 13:	0010	Selects stop comparison point on A channel and % between the zones.
Character 14:	0001	Selects stop point at the first plus slope; disables internal scaling.
Character 15:	1001	Selects stop point to 90% level.
Character 16:	0000	No program desired.

CHARACTER	8	4	2	1	PROGRAM	PROGRAM	8	4	2	1
							J201 PINS			
1	A 0% POS. 8	4	2	1			1	2	3	4
2	A 0% POS..5	A 0% Wid. 4 cm	2 cm	VOLTS			5	6	7	8
3	A 100% POS. 8	4	2	1			9	10	11	12
4	A 100% POS. .5	A 100% Wid. 4 cm	2 cm	A CHOP			13	14	15	16
5	B 0% POS. 8	4	2	1			19	20	21	22
6	B 0% POS. .5	B 0% Wid. 4 cm	2 cm	MEASURE AVE.			23	24	25	26
7	B 100% POS. 8	4	2	1			27	28	29	30
8	B 100% POS. .5	B 100% Wid. 4 cm	2 cm	B CHOP			31	32	33	34
							J202			
9	(START) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW			1	2	3	4
10	(START) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	COUNTER RESET INHIBIT			5	6	7	8
11	(START) OFFSET 80	40	20	10			9	10	11	12
12	OFFSET 8	4	2	1			13	14	15	16
13	(STOP) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW			19	20	21	22
14	(STOP) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	EXT SCALE			23	24	25	26
15	(STOP) OFFSET 80	40	20	10			27	28	29	30
16	(STOP) OFFSET 8	4	2	1			31	32	33	34
							J203			
17	EXT HORIZ ÷ 2	UPPER MINUS	UPPER LIMIT 2000	1000			1	2	3	4
18	800	400	200	100			5	6	7	8
19	80	40	20	10			9	10	11	12
20	8	4	2	1			13	14	15	16
21	EXT HORIZ ÷ 5	LOWER MINUS	LOWER LIMIT 2000	1000			19	20	21	22
22	800	400	200	100			23	24	25	26
23	80	40	20	10			27	28	29	30
24	8	4	2	1			31	32	33	34
							J204			
25	PROG DEC 2	3	4	NIXIE 'V'			1	2	3	4
26	NIXIE S	NIXIE M	NIXIE 'μ'	NIXIE 'N'			5	6	7	8
27	HIGH SPEED PGM		A CHOP[3]	B CHOP[3]			9		15	16

NOTE: GROUND CLOSURE OF A PROGRAM LINE CONSTITUTES A LOGICAL ONE (TRUE); ANY OPEN LINE IS A LOGICAL ZERO (FALSE).

[3]These bits are not used on instruments below SN 360.

Fig. 3-6. Example Programs 3 and 4.

CHARACTER	8	4	2	1	PROGRAM 3	PROGRAM 4	J201 PINS 8	4	2	1
1	A 0% POS. 8	4	2	1	0000	1100	1	2	3	4
2	A 0% POS. .5	A 0% Wid. 4 cm	2 cm	VOLTS	1000	1000	5	6	7	8
3	A 100% POS. 8	4	2	1	0001	1100	9	10	11	12
4	A 100% POS. .5	A 100% Wid. 4 cm	2 cm	A CHOP	1110	1110	13	14	15	16
5	B 0% POS. 8	4	2	1	0000	1100	19	20	21	22
6	B 0% POS. .5	B 0% Wid. 4 cm	2 cm	MEASURE AVE.	0000	0000	23	24	25	26
7	B 100% POS. 8	4	2	1	0000	1100	27	28	29	30
8	B 100% POS. .5	B 100% Wid. 4 cm	2 cm	B CHOP	0000	0000	31	32	33	34
							J202			
9	(START) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0100	0100	1	2	3	4
10	(START) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	COUNTER RESET INHIBIT	0000	0001	5	6	7	8
11	(START) OFFSET 80	40	20	10	0000	0000	9	10	11	12
12	OFFSET 8	4	2	1	0001	0001	13	14	15	16
13	(STOP) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0010	0010	19	20	21	22
14	(STOP) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	EXT SCALE	0001	0101	23	24	25	26
15	(STOP) OFFSET 80	40	20	10	1001	1001	27	28	29	30
16	(STOP) OFFSET 8	4	2	1	0000	0000	31	32	33	34
							J203			
17	EXT HORIZ ÷ 2	UPPER MINUS	UPPER LIMIT 2000	1000	1011	1000	1	2	3	4
18	800	400	200	100	1001	0101	5	6	7	8
19	80	40	20	10	1001	0000	9	10	11	12
20	8	4	2	1	1001	0000	13	14	15	16
21	EXT HORIZ ÷ 5	LOWER MINUS	LOWER LIMIT 2000	1000	0000	0000	19	20	21	22
22	800	400	200	100	0000	0100	23	24	25	26
23	80	40	20	10	0000	1000	27	28	29	30
24	8	4	2	1	0000	0000	31	32	33	34
							J204			
25	PROG DEC 2	3	4	NIXIE 'V'	0000	0000	1	2	3	4
26	NIXIE 5	NIXIE M	NIXIE 'μ'	NIXIE 'N'	0000	1010	5	6	7	8
27	HIGH SPEED PGM		A CHOP[1]	B CHOP[1]	0000	0000	9		15	16

NOTE: GROUND CLOSURE OF A PROGRAM LINE CONSTITUTES A LOGICAL ONE (TRUE); ANY OPEN LINE IS A LOGICAL ZERO (FALSE).

[1]These bits are not used on instruments below SN 360.

Fig. 3-7. Blank External Program worksheet.

Character 17:	1011	Divides the count (readout) by two so that the accumulation of the two measurements will read out the actual time to the amplitude peak; plus upper limit level. Care must be taken that the horizontal plug-in is not set in a ÷ 5 sweep rate function or erroneous readout will occur.
Character 18:	1001	Characters 17, 18, 19, and 20 are programmed for an Upper Limit level of +3999 so that no out-of-limits indication will occur on the first section of this measurement series.
Character 19:	1001	See character 18.
Character 20:	1001	See character 18.
Character 21:	0000	Characters 21, 22, 23, and 24 are programmed for +0000 so that only when the count reaches some negative value will the Lower Limit Level indicate an out-of-limits condition.
Character 22:	0000	
Character 23:	0000	
Character 24:	0000	See Character 21.
Character 25:	0000	No scaling of the readout is needed until the end of the second measurement.
Character 26:	0000	See Character 25.
Character 27:	0000	No program desired.

Since the two measurements are so alike, only the characters that differ will be listed for explanation. Assuming that the distance from sweep start to the peak of the waveform is about +490 μs and the tolerance is ±2%, the limit levels and scaling program will be set accordingly.

Character 1:	1100	Characters 1, 3, 5, and 7 are programmed to the 12 cm position to cause both A and B Memories to remain charged. This is possible since the peak amplitude to be "remembered" is the same in both words of the program. Keeping both of the memories charged allows the Type 230 to make both measurements on only one memory charging sweep, thus saving cycle time.
Character 3:	1100	
Character 5:	1100	
Character 7:	1100	
Character 10:	0001	Counter Reset Inhibit is TRUE to allow accumulation of the two measurements.
Character 14:	0101	Selects first minus slope for start point; still inhibits internal scaling.
Character 18:	0101	Characters 18, 19, and 20 form the upper limit level for the measurement, a total of +0500.
Character 19:	0000	
Character 20:	0000	
Character 22:	0100	The sum of the TRUE bits in characters 22, 23, and 24 form the lower limit level for this measurement, a total of +0480.
Character 23:	1000	
Character 24:	0000	
Character 25:	0000	The fifth decimal lamp from the right will illuminate.
Character 26:	1010	Lights the μ and s symbols in the units nixie.

The total readout should be +0490 μs.

EXTERNAL PROGRAMMING

The external programming functions may be easily checked for proper performance by any programming device which will provide the proper logic levels to the Type 230 (See the first page of the programming instructions). The need may arise to check the programming performance of the Type 230 when there is no programming device readily available. A substitute for an automatic programmer may be constructed with 105 SPST switches connected to program common on one side. The remaining pole of each switch should be connected through an inexpensive diode to a programming input. Closure of any switch will activate a single program function, and any proper measurement program can be set up readily.

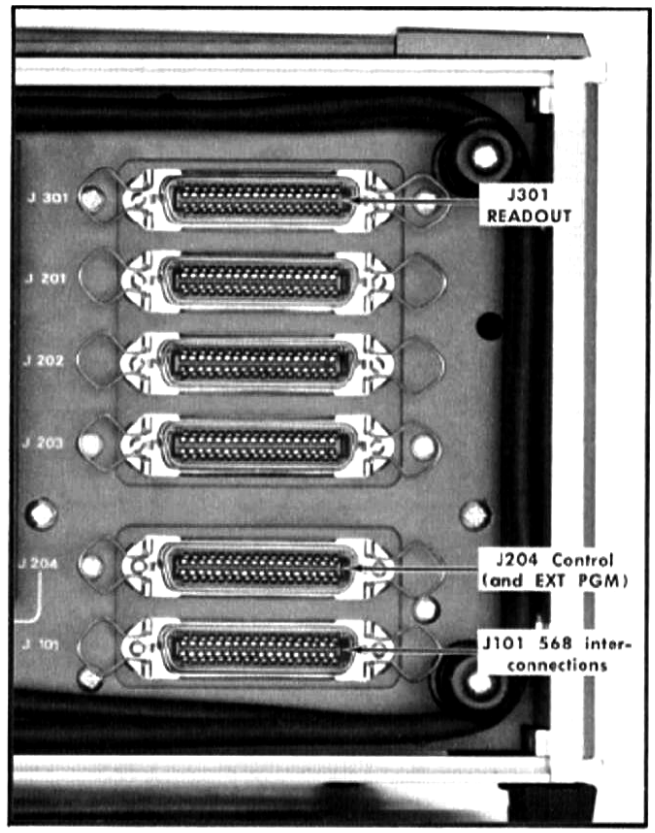


Fig. 3-8. Type 230 external connectors.

Type 230 Control Outputs

As was mentioned earlier in this text, J204 (See Fig. 3-1 or Fig. 3-8 for J204 location) is used for some external program inputs (pins 1 through 9). The majority of the remainder of the pins on J204 are used for external control outputs from the Type 230 for controlling external devices. Fig. 3-9 illustrates the connectors of J204. The following list by pin number explains the purpose of each line.

J204 Pin 17 As mentioned earlier, this is a program ground enabled by the MEASUREMENT MODE switch on the front panel.

Pin 18 Ground to the Type 230 chassis.

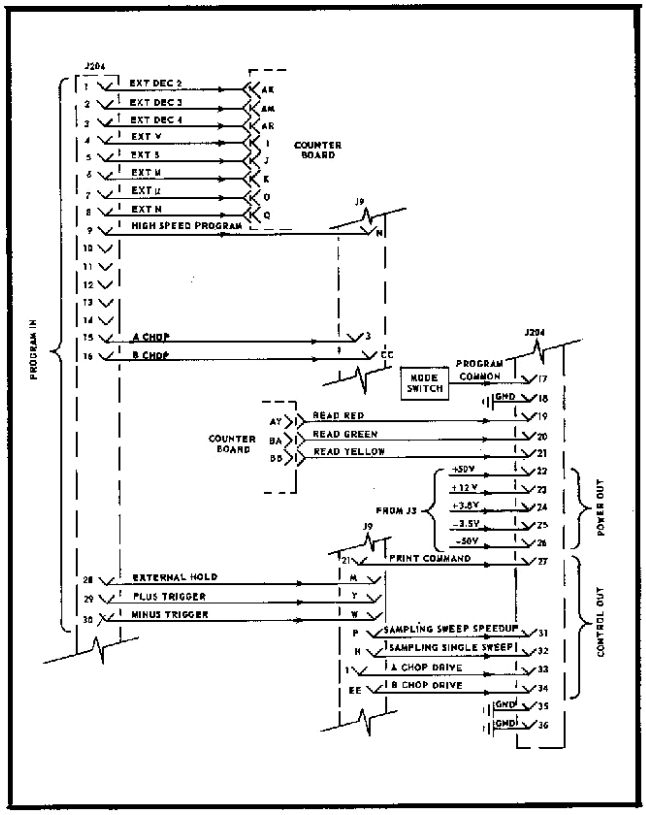


Fig. 3-9. J204 wiring diagram.

Pin 19 READ RED: This output from the Limit Lamp Driver circuitry on the Counter and Readout board is low when the measurement exceeds the Upper Limit Level. This and the outputs from pins 20 and 21 can be used to control an external device which would stop further measurements by the Type 230 on a device under test.

Pin 20 READ GREEN: Indicates the measurement is within limits. See J204 pin 19.

Pin 21 READ YELLOW: Indicates that the measurement has exceeded the Lower Limit level. See J204 pin 19.

Pin 22 +50 volts (±1% at 50 mA maximum) available for powering external controlling units.

Pin 23 +12 volts (±1% at 350 mA maximum; see pin 22.

Pin 24 +3.8 volts (±1% at 200 mA maximum); see pin 22.

Pin 25 —3.5 volts (±1% at 200 mA maximum); see pin 22.

Pin 26 —50 volts (±1% at 25 mA maximum); see pin 22.

Pin 27 PRINT COMMAND: This line is used to signal an external device that a measurement has been completed and the measurement information has been shifted into the storage registers of the Type 230. Normally, the PRINT COMMAND negative step will occur 150 µs after the storage registers are set.

Pin 28 EXTERNAL HOLD: This line is essentially a control input to the Type 230. When EXTERNAL HOLD is TRUE, it keeps the storage registers from resetting. EXTERNAL HOLD, in conjunction with the readout section (J301), may be used to stop the measurement cycles when an out-of-limits situation occurs.

Pin 29 PLUS TRIGGER: Used to synchronize the speed and occurrence of measurement cycles with some external source.

Pin 30 MINUS TRIGGER: See pin 29.

Pin 31 SWEEP SPEEDUP: This line is a control from the Type 230 to the Type 568 horizontal plug-in unit to speed up the repetition rate of measurement cycles by decreasing the total sweep time.

Pin 32 SWEEP RESET (SINGLE SWEEP): This line is a control from the Type 230 to the Type 568 horizontal plug-in unit (Type 3T5 or 3T6) to speed up the repetition rate of measurement cycles by resetting the sweep when the memories are charged or the measurement is complete[5]. With a Type 3T4 plug-in unit, this line causes the unit to permit only one measurement cycle for each triggering pulse.

Pin 33 A CHOP DRIVE: Provides a synchronizing signal to an external signal chopper for the Type 568 vertical plug-in A channel input.

Pin 34 B CHOP DRIVE: Same as pin 33 except for B channel.

Pins 35 and 36 Chassis ground.

Readout Connector J301

Jack J301 (See Fig. 3-8 for physical location of J301) provides an external readout of measurement information from the Type 230 to an external recording device. Fig. 3-10 is a wiring diagram of the Type 230 internal connections to J301. On each line in use, the descriptive label indicates the function of the individual line when TRUE. For example, READ PLUS at J301, pin 1 comes from pin AH on the Counter and Readout board. When TRUE, READ PLUS indicates that the measurement is positive. With the exception of open pins 17 and 18, pins 1 through 29 are information outputs from the Counter and Readout section of the Type 230. Pin 31 (PRINT COMMAND) provides an indication to an external receiver that the measurement is complete and may be recorded.

J301 Pin 30 EXTERNAL HOLD: This line permits an external recorder to prevent clearing the measurement data in the registers.

Signal Connector J101

Jack J101 provides interconnection between the Type 230 and the Type 568 (See Fig. 3-9 for the physical location of J101). Fig. 3-8 shows the internal connections from J101 to

[5]Does not apply to Synchronizer Circuit Card Series F, Model 1 and 2.

SECTION 4
CIRCUIT DESCRIPTION

Introduction

The Type 230 Digital Unit is a programmable time and voltage measurement unit. External program connectors on the rear panel provide for interconnections to a programming device. Front panel controls, switches, and readouts permit manual control of most programmable functions. The signal processing circuitry of the unit is contained on 11 plug-in circuit cards and one circuit board. This section of the manual describes the operation of the Type 230; first in block diagram terms and then on an individual circuit card basis.

On the block diagram level, overall descriptions are given of instrument operation when making time measurements and when making voltage measurements. Block diagrams are included within the text to show the difference between the two modes of operation. An overall block diagram, located in the Diagrams section, shows the relationship between the major circuits of the instrument.

Following the block diagram description, this section contains a description of each circuit in the Type 230. In general, where a circuit functions as an analog or linear device, a conventional circuit description is given. If a circuit performs a logic function, a logic description is given. In the Type 230, the activated logic state is provided by a low voltage level (0 to +2 volts) and corresponds to the true logic state or a logical one. The non-activated logic state is provided by a high voltage level (+6 to +12 volts) and corresponds to the false logic state or a logical zero. Any logic line that is not connected to a low logic level automatically assumes the false (high) state. The "high" and "low" convention will be used as a general rule in this description.

Block diagrams, logic diagrams, and waveform illustrations are included within the text to support and clarify the description. Overall logic diagrams of some of the more complex circuit cards are included in the Diagrams section. Complete circuit card diagrams are also included in the Diagrams section. The circuit diagrams should be referred to for electrical values and those circuit elements not given on the logic diagrams.

BLOCK DIAGRAM DESCRIPTION

Time Measurements

The usual way to measure time with an oscilloscope is to count the horizontal divisions on the CRT between the measurement limits. This distance multiplied by the sweep rate equals the elapsed time. With the Type 230, the elapsed time between two points on a waveform display is measured with a counter and presented as a digital readout. To make a time measurement, the Type 230 needs specific information from the vertical amplifier and the time-base plug-in units. The required information is applied via an interconnecting cable from the Type 568 Oscilloscope and includes the following:

1. Horizontal sweep waveform
2. Sweep gate waveform
3. Clock pulses
4. Unit of measure (ns, μs, etc.)
5. Decimal point position information
6. Signal to be measured

Figure 4-1 shows the time relationship between a typical signal and the horizontal waveform. The intensified 0% and 100% zones (points A and B on the signal waveform) can be moved to any of 20 positions on the display by turning the 0% and 100% controls on the front panel (0.5 cm zone movement between switch positions). In the description that follows, the 0% intensified zone of the CRT is set for the most negative point of the signal, and the 100% zone is set for the most positive point.

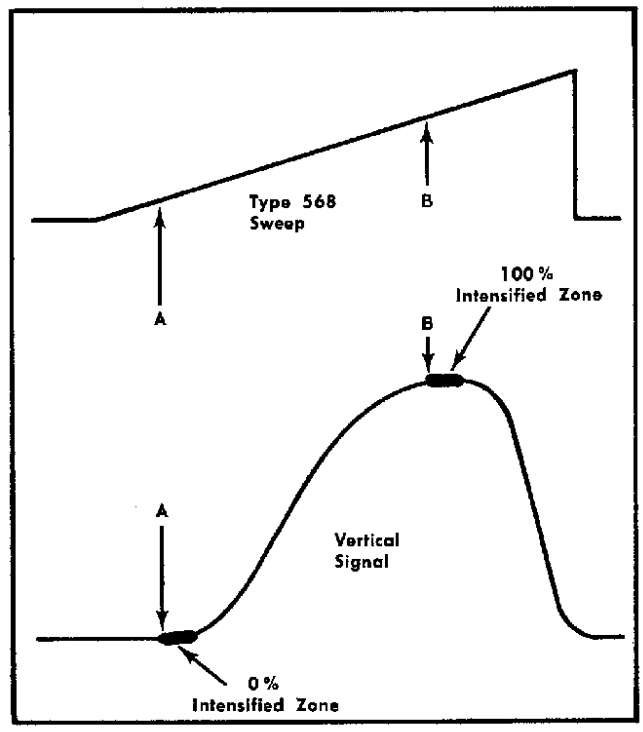


Fig. 4-1. Time relationship of Type 568 sweep, signal, and intensified zones.

The horizontal sweep, after passing through a buffer stage, is applied to the 0% and 100% zone generator circuits (see Fig. 4-2). The horizontal sweep voltage is combined with the voltage from each zone generator circuit to form gate pulses that are delayed a preset amount of time from the sweep start. These gate pulses are applied to memory circuits.

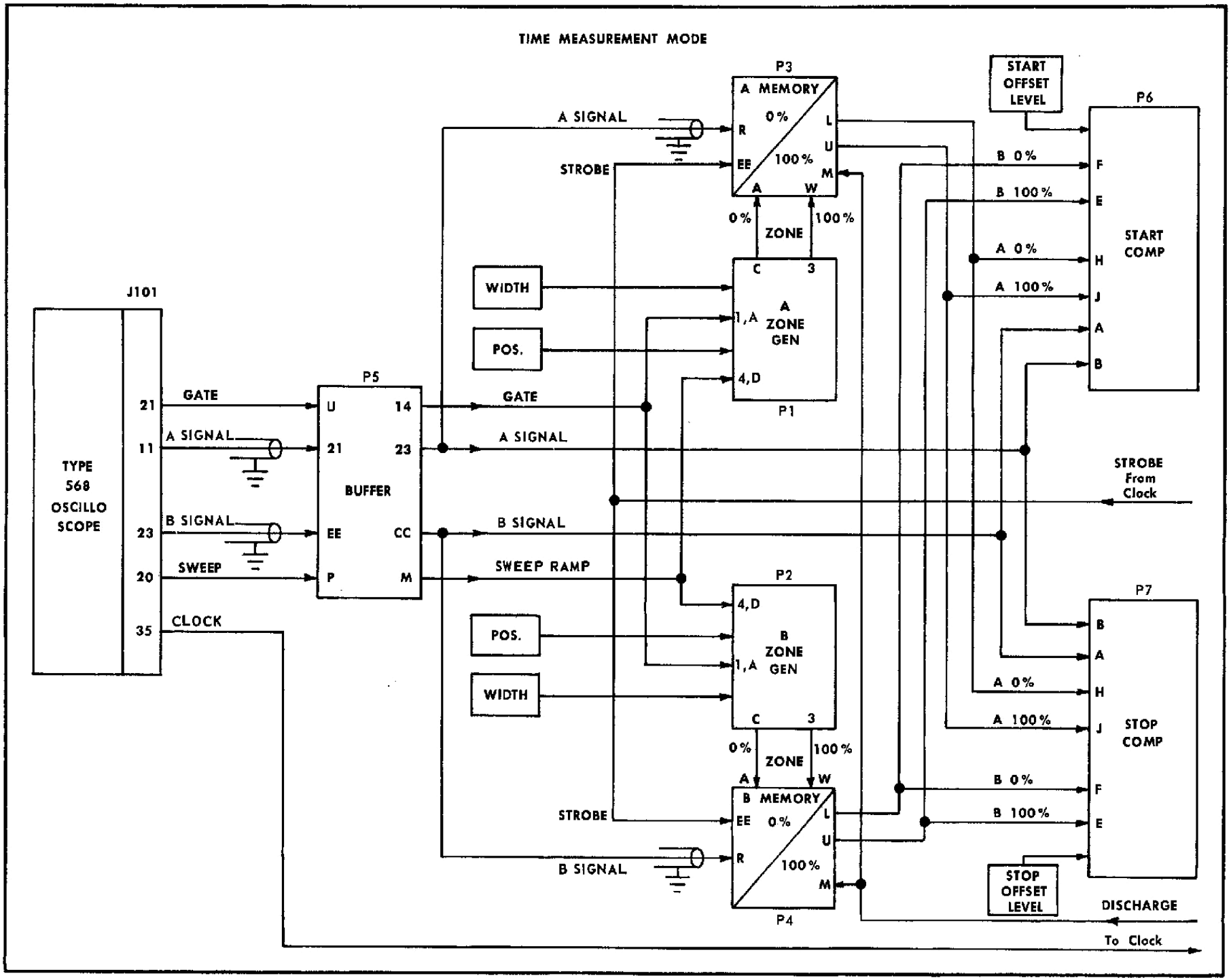


Fig. 4-2. Block diagram showing signal flow to start and stop comparators, time measurement mode.

There are two memory circuit cards, one for Channel A and one for Channel B. The use of two memory circuits provides the Type 230 with the capability of starting a measurement on one trace of a dual-trace display and ending the measurement on the other trace. For example, the time difference between pulses on two different signal lines can be measured.

When the 0% gate pulse is generated as previously explained, the 0% memory samples the vertical signal voltage at point A of Figure 4-1. This sample is stored in the 0% memory circuit. The output of the 0% memory circuit is applied to one input on each of two differential comparator circuits (the start and stop comparators). Each memory circuit takes a sample of the vertical signal and its output automatically adjusts to the signal voltage with every sweep.

When the horizontal sweep reaches point B in Figure 4-1, the sweep voltage and the voltage from the 100% zone generator combine to form a gate pulse that activates the 100% memory circuit. The 100% memory circuit samples the vertical signal at point B and stores it. The output of the 100% memory circuit is applied to a second input of the differential comparator circuits.

Each comparator needs two inputs:

1. A pre-selected DC voltage level that sets the point of comparison (start or stop point of measurement).

2. The signal from the vertical amplifier plug-in or the sweep waveform. (The START SLOPE and STOP SLOPE switches on the front panel are set to the polarity of the waveform slope being measured, plus or minus slope, and 1st slope or 2nd slope. In programmed operation, the selections are made by programming inputs).

The DC voltage level referred to in (1) above can be a percentage of the voltage between the two memories, a voltage offset from either of the memories, or a selected DC offset voltage referenced to ground as in the case of "Horiz mm" offset. The signal in (2) above can be from either the A Channel or B Channel of the vertical plug-in unit.

Figure 4-3 shows the comparators and the time relationship between the reference and signal voltage. To illustrate the operation, the instrument is set to make a 10% to 90% time measurement as follows:

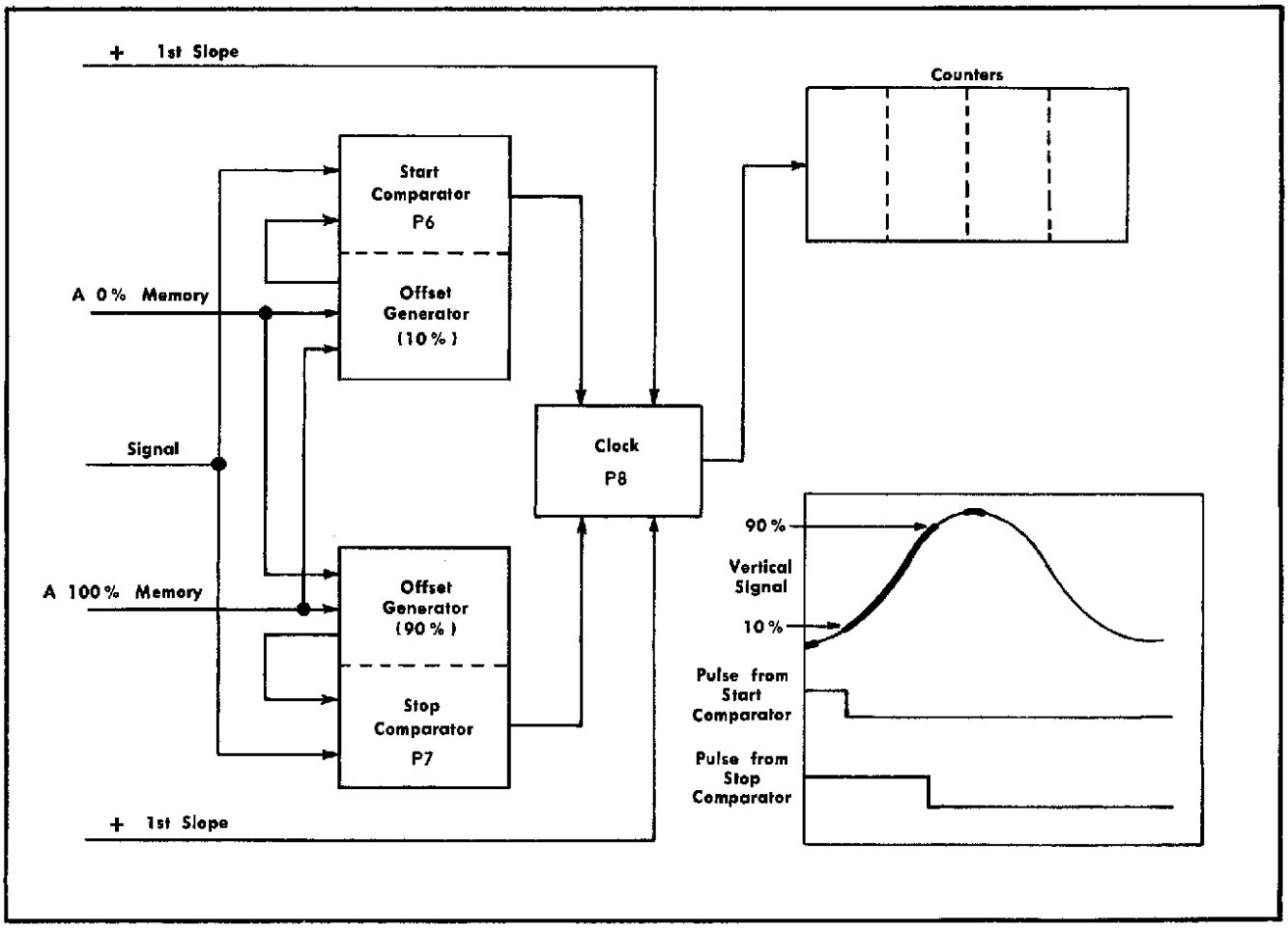


Fig. 4-3. Block diagram showing start and stop comparator pulse generation.

1. Both the 0% and 100% memory levels are applied to the offset generator (mounted on the Start Comparator circuit card) whose output is a voltage level selected to be 10% of the voltage between the 0% and 100% memory levels. This 10% voltage is applied to one side of the start comparator.

2. In an identical manner to that explained above, a 90% voltage level is generated by the offset generator on the Stop Comparator circuit card and is applied to one side of the stop comparator.

The other input of each differential comparator receives the vertical signal from the buffer stage. When the vertical signal rises to 10% of its amplitude, the start comparator switches and sends a pulse to the clock gate, allowing clock pulses to pass to a counter. When the signal voltage reaches 90% of its amplitude, the stop comparator fires and ends the pulse to the clock gate. Thus between the firing of the start comparator and the firing of the stop comparator, clock pulses are passed to the counters. As a result, the number shown on the readout is the time between the 10% and 90% voltage points of the vertical signal.

Voltage Measurements

Figure 4-4 shows the connections to the comparators when making voltage measurements. For simplification, only one signal, one zone generator and one memory are shown. Note that the front panel START and STOP functions are not used when making voltage measurements.

When making voltage measurements, the reference voltages for the comparators are the memory outputs (derived from the vertical signal). The other input to the differential comparators is a voltmeter ramp voltage generated on the Buffer circuit card. As the voltmeter ramp voltage rises through the 0% memory voltage the start comparator fires. This sends a pulse to the clock gate and gates a 1 MHz clock (generated on the Clock circuit card) to the counters. When the voltmeter ramp voltage rises through the 100% memory voltage, the stop comparator fires and sends a pulse to the counter. The voltage between the 0% and 100% levels is equal to the number of 1 MHz clock pulses times the voltmeter ramp rate of rise.

There are three linear voltmeter ramps generated on the Buffer circuit card. The voltmeter ramp applied to the comparators for a particular measurement is determined by the setting of the volts/div switch of the vertical plug-in unit. The rate of rise for the voltmeter ramp for a particular setting of the volts/div switch is as follows: (a) 2.5 mV/μs for any "2" setting of the volts/div switch (÷5), (b) 5 mV/μs in any "1" setting of the volts/div switch (÷1), and (c) 10 mV/μs in any "5" setting of the volts/div circuitry (÷2). Likewise, the position of the decimal point and the unit of measure are determined by the input attenuator switching of the vertical plug-in unit (volts/div).

The foregoing discussion briefly outlines the two basic operating modes of the Type 230. The functions of the synchronizer, counter, and limit comparator circuits are basically the same for both modes of operation. The synchro-

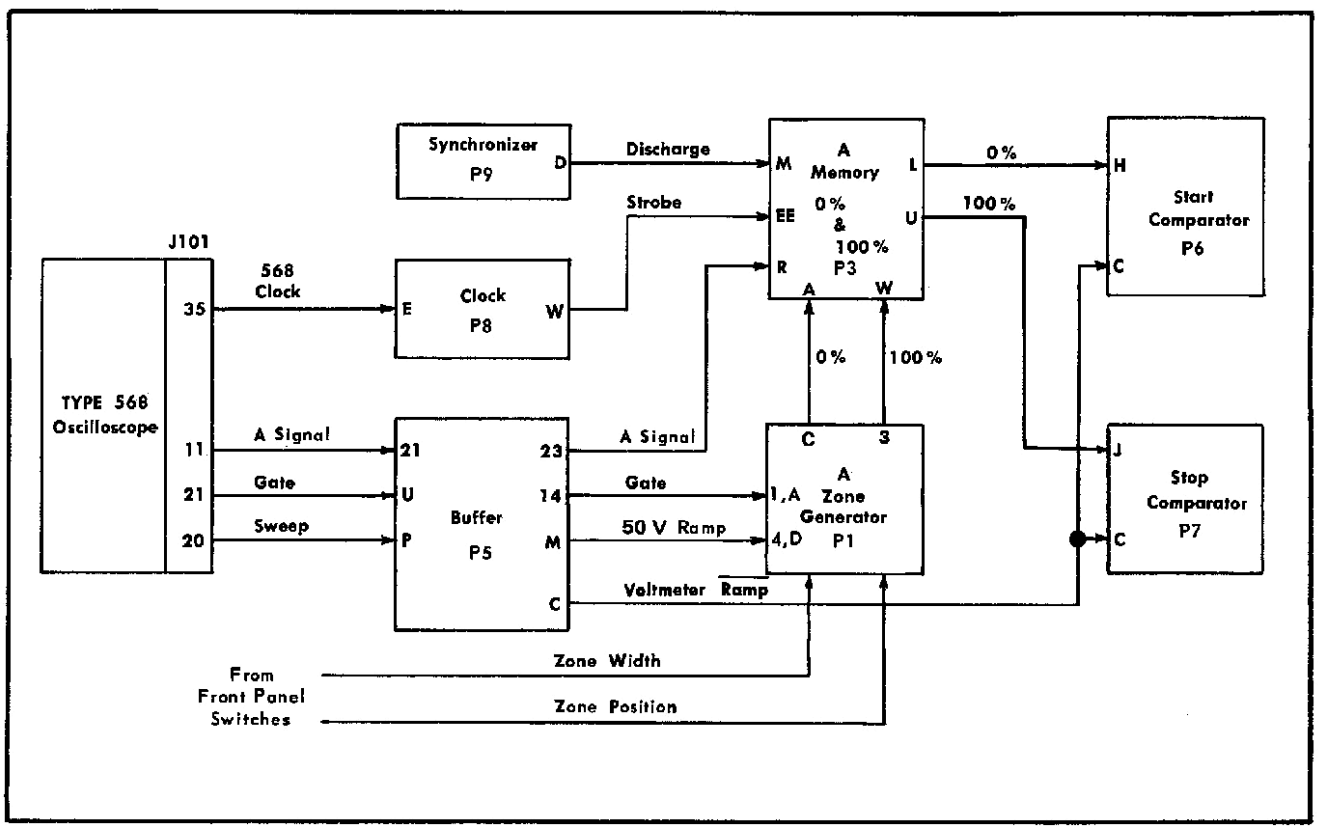


Fig. 4-4. Block diagram of signal flow to the start and stop comparator circuits, volts mode.

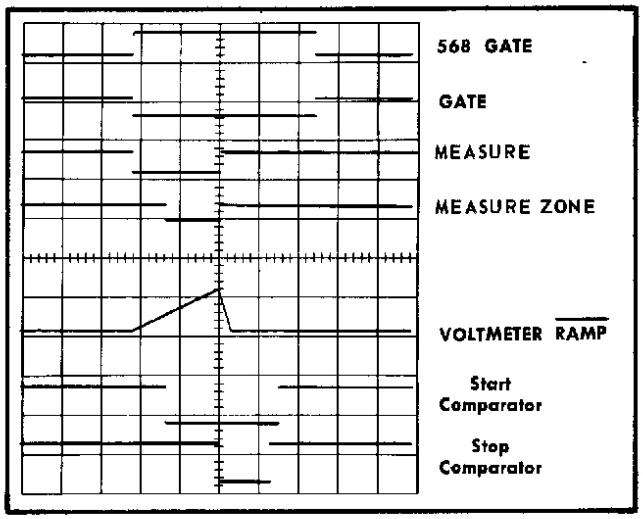


Fig. 4-5. Waveform diagram showing major signals used in volts mode.

nizer is the heart of the whole system in that it directs the system to perform all of its functions in their proper sequence. The synchronizer is comprised of a delay generator, logic gates, and flip-flops. The delay generator generates the DELAY pulse which starts the measurement cycle. Other pulses derived from the DELAY pulse discharge the memories, reset the clock and counters, and tell the circuitry when to measure (see Fig. 4-5). The counter counts and stores the gated clock pulses (digitized measurement) from the clock circuit. The limit comparators take the binary information from the register and compare it with preset limits (either front-panel or externally programmed) and read out the comparison results.

A detailed analysis of the operation of the various circuits in the Type 230 is given in the following circuit card descriptions. Refer to the end of Section 3 for a definition of terms.

CIRCUIT ANALYSIS

BUFFER CIRCUIT CARD

The Buffer circuit card provides the interface between external equipment and the circuits within the Type 230 proper. Circuits on the Buffer circuit card are presently comprised of gating circuits, a ramp generator circuit, and two operational amplifiers. The Buffer circuit card has been kept uncomplicated for easy re-design if future external equipment changes cause interface problems.

GATE and GATE Generator Circuit. The signal on connector P5 pin U (see Fig. 4-6) is actually the plus gate from the time base plug-in unit. Throughout this description this particular signal is referred to as the 568 GATE since it arrives via the Type 568. The 568 GATE goes high at the start of the sweep, then goes low as the sweep ends.

From P5 pin U the 568 GATE is applied to transistor Q611. The inverted output at the collector of Q611, now called SWEEP GATE, is applied to two circuits; to the Zone Generator circuit card via P5 pin W, and to the base of transistor Q613. The SWEEP GATE output from the collector of Q613 is applied to pin 6 of three-input NAND gate M614. When the 568 GATE goes high at the start of a sweep, the output of M614 pin 5 goes low, causing flipflop M618 to toggle. The output on M618 pin 5 goes low and starts the GATE pulse. Simultaneously, the output on M618 pin 7 goes high and generates the GATE pulse. The high GATE signal, through capacitor C621, resets flipflop M620 and the resulting high output on M620 pin 4 starts the voltmeter ramp generator (transistors Q652, Q663, Q666 and associated circuitry).

The high output of M620 pin 4 is also applied to M614 pin 7 and holds the output of M614 pin 5 low. Thus the 568 GATE cannot end GATE and GATE until the VOLTMETER RAMP is ended.

The MEASURE signal on P5 pin K goes low at the start of the measure sweep. When MEASURE goes high, M620 switches and the resulting low output on M620 pin 4 biases Q652 into conduction and ends the VOLTMETER RAMP. As VOLTMETER RAMP goes low, transistor Q617 is biased into conduction and applies a low to M614 pin 8. The 568 GATE goes low at the end of the sweep. With all three of its inputs low, M614 pin 5 applies a high to M618 pin 6. Flipflop M618 sets, ending GATE and GATE. If for some reason MEASURE does not go high, the VOLTMETER RAMP continues to run up until the current through resistor R625 switches M620. In this case, capacitor C624 speeds up the switching process. The switching of M620 ends VOLTMETER RAMP as previously explained.

Voltmeter Ramp Generator. The voltmeter ramp generator is an integrating Miller run-up circuit comprised of transistors Q663 and Q666 and associated circuitry. The rate of linear rise is controlled by capacitor C665 and resistor R661 in series with variable resistor R660. Operation of the voltmeter ramp generator is as follows:

The output of M620 pin 4 is coupled to the base of inhibitor transistor Q652. Transistor Q652 forms a current shunt through diode D653 to prevent the generation of a VOLTMETER RAMP until GATE goes high and resets M620. With M620 reset by GATE as previously explained, the output of M620 pin 4 goes high and reverse biases Q652. Diode D653 is now reverse biased. Timing current from resistor R660 is allowed to flow into timing capacitor C665 and the VOLTMETER RAMP starts to run up.

Transistor Q663 and Q666 form an operational amplifier. As the current through R660 is diverted into C665, the voltage at the base of Q663 tries to go negative; the voltage at Q663 collector goes positive, decreasing the current through Q666. As the current through Q666 decreases, Q666 emitter goes positive and applies degenerative feedback to the base of Q663. The result is a linear voltage ramp at the emitter of Q666. The VOLTMETER RAMP thus generated is used by the start and stop comparators when making voltage measurements.

The rate of rise of the VOLTMETER RAMP can be changed by enabling either VERT ÷ 1 or VERT ÷2 (P5 pins B and A respectively). As an example, grounding pin A reverse biases transistor Q632, and thereby reverse biases diode D633. With D633 reverse biased, additional current through R634 and R635 is made available for charging timing capacitor C665. Since programming pins A and B simultaneously is not permitted, three choices of ramp rise are available. The three ramps correspond to the "1", "2" and "5" positions of the Volts/Div switch on the vertical plug-in

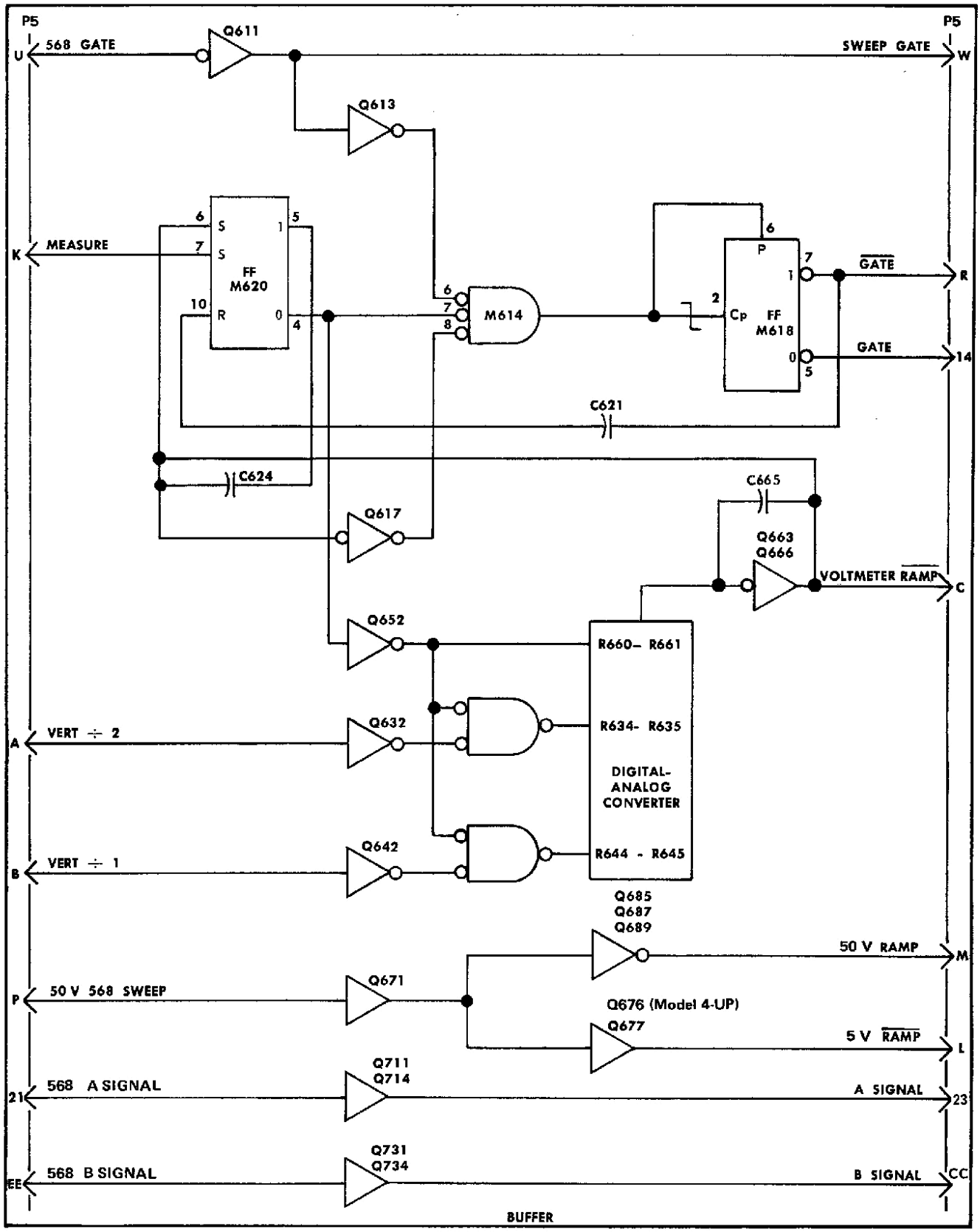


Fig. 4-6. Buffer circuits logic diagram.

unit and are enabled by connecting one of two common lines (A ÷ 1, 2, 5 COMMON or B ÷ 1, 2, 5 COMMON) to P5 pin A or B or leaving both open. Selection of the proper VOLTMETER RAMP can best be understood by looking at a composite of all the circuits related to the voltmeter ramp generator as shown on the simplified voltmeter ramp function foldout diagram in the Diagrams section of this manual. The common line selected by the vertical plug-in unit Volts/Div switch is provided from the CRT Intensification card (P10) in the Type 230, and its logic level depends on the state of NAND gates Q123 and Q113 as controlled by the front-panel MEASUREMENT MODE switch.

When the MEASUREMENT MODE switch is set to B VOLTS, P10 pin 12 (B SIGNAL) on the CRT intensification card is grounded through D524 and the switch, and P10 pin 9 is held low by current through D2051 on the Clock card when P8 pin 7 is grounded through D521 and the MEASUREMENT MODE switch. This results in a low on the B ÷ 1, 2, 5 COMMON line which is then connected by the Channel B Volts/Div switch of the vertical plug-in unit to select the proper VOLTMETER RAMP for the Volts/Div setting. When the Channel B Volts/Div switch is set to one of the "2" positions, P5 pins A and B are both open and the VOLTMETER RAMP rate is 2.5 mV/μs. When the switch is set to one of the "1" positions, P5 pin B (÷1) is held low and the ramp is 5 mV/μs. When the switch is set to one of the "5" positions, P5 pin A (÷2) is held low and the ramp rate is 10 mV/μs.

When the MEASUREMENT MODE switch is set to A VOLTS, P10 pin 9 (VOLTS) is held low by the connection to P8 pin M, but P10 pin 12 (B SIGNAL) is not connected and is therefore high. This results in a low on the A ÷ 1, 2, 5 COMMON line which selects the proper VOLTMETER RAMP to correspond with the deflection factor set by the Channel A Volts/Div switch.

If the MEASUREMENT MODE switch is set to TIME P10 pin 9 is high, causing both ÷ 1, 2, 5 COMMON lines to be high and no lows applied to P5 pin A or B. This is true regardless of the logic level on P10 pin 12, since inhibitor Q103 on the CRT Intensification card applies a low to the inputs of NAND gates Q113 and Q123. In this measurement mode the VOLTMETER RAMP runs in the ÷5 mode during each sweep (when the 568 GATE is low) but the ramp is disconnected in the Type 230 and is not used.

50 V Ramp Inverter (Models 1, 2, 3). The inverter circuit consisting of transistors Q671, Q685, Q687 and Q689 forms a buffer and inverting operational amplifier circuit with a gain of approximately —1. The input is the positive-going 568 SWEEP (50 volts) on P5 pin P. The output is a negative-going 50-volt ramp which is applied to the Zone Generator Circuit card for use in deriving the ZONE pulses.

In operation, the 568 SWEEP ramp is applied through diode D671 to the base of emitter follower Q671. The voltage at the junction of emitter resistors R670 and R672 rises, increasing the conduction through Q687. As the current through Q687 increases, the voltage drop across resistor R685 increases and in turn lowers the base voltage of Q685. Since Q685 is another emitter follower, decreasing its base voltage causes a corresponding decrease in its emitter voltage. Feedback resistor R683 applies negative feedback to the base of Q687 and ensures a linear output, which is taken as 50V RAMP from P5 pin M.

Note that the output of emitter follower Q671 has a voltage divider circuit in its emitter. The voltage at the junction of emitter resistor R672 and R673 is tapped off and applied to the base of transistor Q677, another emitter follower. The output of Q677 is a positive-going ramp of five volts amplitude, the DC level of which is adjustable by resistor R675. This 5V RAMP is applied through P5 pin L to the Start and Stop Comparator circuit cards. On the Comparator cards, the ramp is used as one input to a comparator when offsetting the start or stop point from the sweep start in making time measurements (HORIZ mm FROM SWEEP START).

50 V RAMP Inverter (Model 4-up). In operation, the 568 SWEEP is applied through SW671 and D671 to the base of emitter-follower Q671. A portion of the voltage rise at the emitter of Q671 is taken off at the junction of R672 and R673 and coupled through emitter-followers Q676 and Q677 (see Buffer diagram) to the output at P5 pin L. This positive-going 5V RAMP output is adjusted by R670 (5V RAMP GAIN) to 5 volts for use as a comparison ramp in the start and stop comparators while making time measurements in HORIZ mm FROM SWEEP START mode. Switch SW 671 at the input is used while adjusting the amplitude and DC level of the 5V RAMP output.

The input 568 SWEEP ramp signal is also taken directly from the emitter of Q671 and inverted by Q687, then applied through emitter-follower Q685 to the output at P5 pin M as 50V RAMP, a negative-going ramp to be used by the zone generators. Negative feedback from the output to the base of Q687 ensures a linear output of the ramp. The amplitude of 50V RAMP is adjusted by R680 (50V RAMP GAIN) for proper zone positioning across the CRT.

Vertical Signal Buffers. The vertical signal inputs at P5 pins 21 and EE are applied to two identical operational amplifier circuits, each having an overall gain of 0.5. Since the circuits are identical, only the amplifier for Channel A is described.

The input signal on P5 pin 21 is applied to a voltage divider consisting of resistor R702 in series with the series parallel combination of resistors R704, R705, and R709. The resistance of the series-parallel network is equal to that of R702. The input signal is thus attenuated by one half and is applied to the base of emitter follower Q711. Resistor R716, the emitter load resistor of Q711, is long-tailed to transistor Q714 which functions as an impedance transformer to match a high impedance input to a low impedance output. The attenuation of the input signal is necessary to make the signal levels compatible with the input capabilities of the integrated-circuit comparator on the Start and Stop Comparator circuit cards.

ZONE GENERATOR CIRCUIT CARDS

The two Zone Generator circuit cards generate the time and width-variable 0% and 100% zone memory-gate pulses. The time locations of the four zones are indicated by trace brightening on the Type 568 CRT. The operator has an option of twenty zone positions and four zone widths, all controllable from the front panel or programmable at the appropriate program inputs. The zone positions are variable in 0.5 cm steps; the widths available are 0.3 cm, 2 cm, 4 cm, and 10 cm.

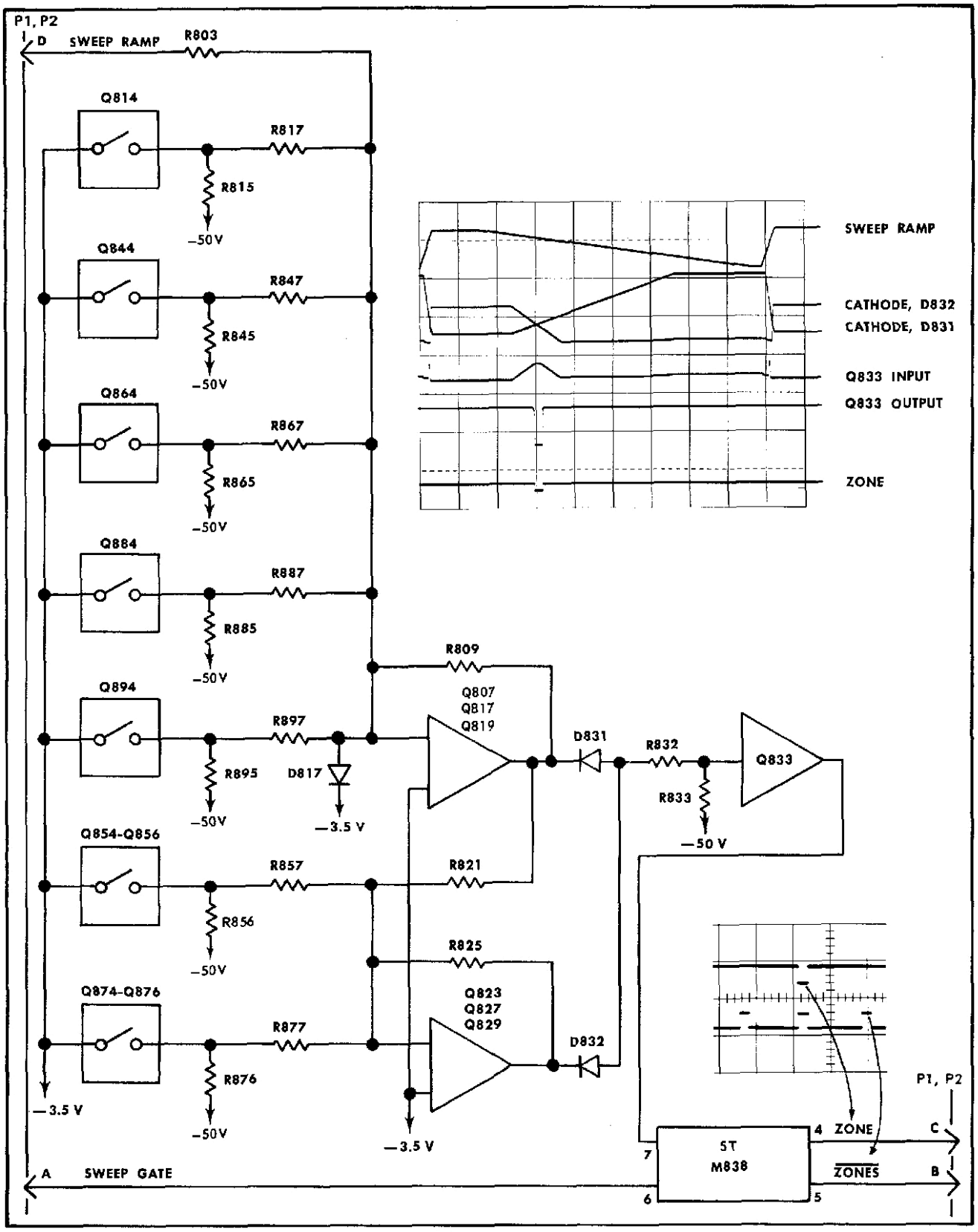


Fig. 4-7. Block diagram showing zone generation.

The intensified memory zones are generated by two identical Zone Generator circuit cards; the "A" Zone Generator circuit card and the "B" Zone Generator circuit card. Each of the two Zone Generator cards contains two zone generator circuits which are identical except for the circuit numbers assigned. Since the four zone generator circuits are alike, only the "A" 0% zone generator is described.

Each zone generator circuit can be further divided into three circuits: the positioning circuit, the width circuit, and the squaring circuit. In the following description, the zone positioning circuitry is explained, then the width circuitry, and finally the generation of the zone pulse by the squaring circuit.

The inputs to the zone generators (see circuit diagram) are the SWEEP GATE pulse and the 50 V RAMP from the Buffer circuit card, and position and width logic inputs controllable from either the front-panel REFERENCE ZONES switches or from the programming connectors. The outputs of each zone generator are (1) ZONE, (2) $\overline{\text{ZONE}}$, (3) AVERAGE, and (4) $\overline{\text{TWELVE}}$. The $\overline{\text{ZONE}}$ output on pin B is applied to the Synchronizer circuit card. The ZONE, AVERAGE, and $\overline{\text{TWELVE}}$ outputs are applied to the Memory circuit cards.

Positioning Circuit

In operation, zone positioning is controlled by applying low levels to the bases of transistors Q814, Q844, Q864, Q884, and Q894. These transistors control the current into the input of an inverting operational amplifier consisting of transistors Q807, Q817, and Q819 and associated circuitry. The current control transistors and operational amplifiers actually make up a digital-to-analog converter, the analog output being taken from the emitter of Q807.

The 50 V RAMP which starts at approximately +50 volts, is applied through R803 to the base of Q817. At the start of the sweep the base of Q817 is clamped at about —3.0 volts by D817. Assuming that all the current control transistors are cut off due to highs on their inputs, the voltage on the emitter of Q807 is about 0 volts. Transistor Q819 is near cutoff due to the conduction of Q817. These are the conditions at the start of the sweep when all the zone positioning inputs are high (positioned at start of sweep).

As the 50 V RAMP starts running down, the decreasing voltage results in decreasing current flow through R803. Clamp diode D817 starts giving up its current to compensate for the decrease in current through R803. With all the current control transistors cut off, D817 soon runs out of current. Transistor Q817 now starts to give up its base current, with the result that its collector current decreases and its collector voltage starts to rise. The rise in Q817 collector voltage increases the drive to Q807 base. Emitter-follower Q807 increases its conduction and the ramp output as its emitter starts to rise (see Fig. 4-7). As the ramp output of Q807 rises, increasing current flow through R809 applies a feedback voltage to the base of Q817 which keeps Q817 from being immediately cut off. Eventually the voltage at the collector of Q817 reaches about +12 volts and Q807 is saturated. With no further increase in feedback available through R809, Q817 is cut off by the falling 50 V RAMP. The voltage at the base of Q817 reaches about —8 volts by the time the sweep ends.

For purpose of further explanation, assume that a low is applied to pin Y or W. (Zone position: 4th centimeter from sweep start). Transistor Q884 saturates and takes all the current flowing through resistor R885. This current is subtracted from the total available at the base of Q817. Diode D817 now conducts harder and makes up most of the current difference necessary to hold Q817 base voltage at —3.5 volts. The increased current flow through D817 increases the voltage drop across the diode slightly and Q817 increases its conduction to the point where the voltage on the emitter of Q807 rests at about —3.5 volts. These are the conditions at the start of the sweep.

As the 50 V RAMP starts running down, the circuit operates as previously explained except that now D817 does not run out of current as soon. The 50 V RAMP must run down much farther before D817 is reverse biased and Q817 starts giving up its base current. The increased distance the 50 V RAMP must run down before the Q807 emitter starts rising represents 4 cm of zone position displacement on the CRT trace. Switching the current control transistors on and off changes the amount of current which D817 must pass and changes the zone position.

When externally programming the Type 230, it is possible to program both the 4 cm and 8 cm position inputs. This is detected by circuit connected to the base of Q899, and Q899 is turned off. The $\overline{\text{TWELVE}}$ signal output of Q899 is applied to pin 27 and thence to the memories. The use of this signal will be described in the memory circuit description.

Width Circuitry

The width circuitry consists of Q823, Q827, Q829, Q833, Q854, Q856, Q874, Q876, D831, and D832. Transistors Q823, Q827, and Q829 form another inverting operational amplifier; Q833 operates as an inverter. For purposes of explanation, assume that the width inputs (pins R, U, M, and N) are high (the zone width is 0.3 cm). Assume also that one or more of the position inputs is low.

At the start of the sweep the voltage at the base of Q827 is resting at about —3.6 volts. Q829 is conducting, which biases Q827 to a collector current of about 1 mA. The conduction of Q827 biases Q823 to where it also passes about 1 mA and the voltage on Q823 emitter is about +2 volts. The voltage at the junction of diodes D831 and D832 is about —2 volts, that at the base of Q833 about —4 volts. Diode D831 is forward biased and conducting; D832 is reverse biased.

When the 50 V RAMP starts running down, nothing happens in the width circuit until D817 runs out of current and the ramp out of Q807 starts running up as previously explained. At the point where Q807 ramp starts to run up, two things start to happen; the forward bias on D831 starts to decrease and the voltage on the base of Q827 tries to move positive. As the base voltage of Q827 starts to rise, Q827 increases its conduction and decreases the bias on Q823 base. Transistor Q823 decreases conduction, Q823 emitter voltage starts to fall, and the falling emitter voltage is coupled through R825 to Q827 base where it opposes the rising ramp voltage.

As the ramp output of Q807 continues to rise the current through D831 decreases toward zero. The voltage at the

base of Q833 starts positive and Q833 is biased into conduction. The rising ramp voltage of Q833 base quickly drives the transistor into saturation and its collector voltage bottoms out at about —3.5 volts. This is the start of the ZONE pulse.

Meanwhile, the ramp voltage on Q823 emitter is running down. When the ramp output of Q823 emitter falls to the point where D832 becomes forward biased, the conduction of D832 starts pulling the Q833 base negative again. Transistor Q833 collector voltage rises rapidly to about +2 volts as Q833 is driven into cutoff. This is the end of the zone pulse. The waveform output of Q833 collector is that of an inverted, truncated triangle whose leading edge is generated from the Q807 emitter ramp and whose trailing edge is generated from the Q823 emitter ramp (see Fig. 4-7).

The zone width is increased from 0.3 cm to 2 cm by applying a low to either pin R or U. A low at either of these inputs biases transistor Q854 into conduction. The conduction of Q854 biases Q856 into cutoff and the current through R856 is now diverted through R857 to R821 and the base of Q827. Transistor Q827 decreases conduction, its collector voltage rises, and the resting voltage at Q823 now emitter rises. Since the negative-going ramp output of Q823 now starts from a higher positive level the time between the point where D831 is reverse biased and the point where D832 becomes forward biased is increased. Transistor Q833 remains in conduction for a period equal to 2 cm of CRT trace.

Note the values of R876 and R856 in the 4 cm and 2 cm width circuits respectively. It can be seen that if 4 cm width is programmed instead of 2 cm, the resting point of Q823 emitter is moved more positive and Q823 emitter ramp must run down from the higher level. The output pulse from Q833 is now 4 cm wide instead of 2 cm. With both the 2 cm and the 4 cm WIDTH inputs low, the resting potential to Q823 emitter is so high that D832 never becomes forward biased before the sweep ends. Once the ZONE pulse moves low, it does not return to the high level until the end of the SWEEP GATE Pulse. Before leaving the width circuits, the function of AND gate diodes D855 and D875 should be noted. If neither the 2 cm width circuit nor the 4 cm width circuit is receiving a low input, both D855 and D875 are reverse biased and the AVERAGE signal output on pin P is low. If either or both of the two width circuits are receiving a low, the corresponding diode(s) is forward biased and the AVERAGE signal is high. The AVERAGE signal output on pin P is used to signal the memory whether an average charge or a peak charge is to be made. This will be discussed again in the Memory circuit card description.

Squaring Circuit

Integrated circuit M838 is used as a Schmitt circuit whose purpose is to square up the pulse output of Q833. Between sweeps the SWEEP GATE input on pin A is high and inhibits M838. At the start of the sweep, pin A goes low and M838 is enabled. When Q833 collector voltage goes negative at the start of a ZONE pulse as previously explained, the circuitry inside M838 changes state. The ZONE output on pin B goes high, the ZONE output on pin C goes low. Switching action is rapid and the pulse shows a square shape. At the end of the negative pulse from Q833, M838 resets. If 10 cm zone width is programmed, M838 is reset by the end of SWEEP GATE. Thus M838 is reset by either the end of the negative pulse from Q833 or the end of SWEEP GATE,whichever occurs first.

MEMORY CIRCUIT CARDS

The Type 230 contains two Memory circuit cards, one for Channel A and one for Channel B. The two cards are identical; each contains a 0% memory circuit and a 100% memory circuit.

The inputs to each Memory circuit card (see circuit diagram) are the 0% ZONE, 100% ZONE, AVERAGE, and TWELVE signals from the Synchronizer circuit card, the signal output of the vertical plug-in unit received via the Buffer circuit card, and the STROBE signal from the Clock circuit card. The outputs from each of the two cards are memory voltage levels corresponding to the signal voltage at the intensified zones and signals that indicate when the memories are properly charged. The memory voltage levels are applied to the Start and Stop Comparator circuit cards for use as one of the reference voltages in each of the two comparators. The memory status signals are sent to the Synchonizer circuit card where they enable a measurement sweep if the memories are properly charged.

0% Memory Circuit

For purposes of explanation, assume that the AVERAGE, TWELVE, and STROBE signals are low, that DISCHARGE AND 0% ZONE are high, and that there is a signal present at pin R. Assume also that flipflop M1022 is in the reset state, providing a low state of 0% CHARGED, indicating to the synchronizer that the 0% memory is charged (see Fig. 4-8). Under these conditions the high 0% ZONE signal on NAND gate M1012 pin 7 causes a low on M1012 pin 5. The low on M1012 pin 5 biases transistor Q1015 off, Q1015 collector voltage rises and biases Q1018 off. The high DISCHARGE signal on NAND gate M1020B pin 9 causes its output to go low, biasing transistors Q1031 and Q1036 off. The high 0% ZONE signal from pin A to NAND gates M1040A pin 8 and M1040B pin 9 cause both inputs to NAND gate M1042B (pins 9 and 10) to be low. The output of M1042B goes high and biases transistor Q1046 off. Turning off Q1046 biases transistor Q1053 off also. At this point diodes D1062, D1063, D1065, and D1066 are all reverse biased. The charge on memory capacitor C1063 cannot change under these circumstances.

When the Synchronizer circuit starts a measurement cycle, the memory DISCHARGE pulse is generated by the DELAY pulse and GATE. The negative-going DISCHARGE pulse is applied to M1020B pin 9 and the output of M1020B goes high (TWELVE, the other input, is low). The high output of M1020B sets flipflop M1022, causing the output on M1022 pin 5 to go high and the output on pin 4 (Model 4-up) to go low. The high output from M1022 pin 5 goes to the Synchronizer card to indicate that the 0% memory is not charged. In Memory Model 4-up, M1022 Pin 4 is connected to M1040A pin 7. The low at pin 7 enables M1040A to act when 0% ZONE moves low. The high output at M1022 pin 5 also is applied to pin 7 of AND/NAND gate M1026, causing the output at M1026 pin 4 to go high and the output at pin 5 to go low. The low at M1026 pin 5 turns off Q1043, which enables Q1057. The high signal from M1020B pins 4 and 5 is also applied to Q1031, biasing it into con-

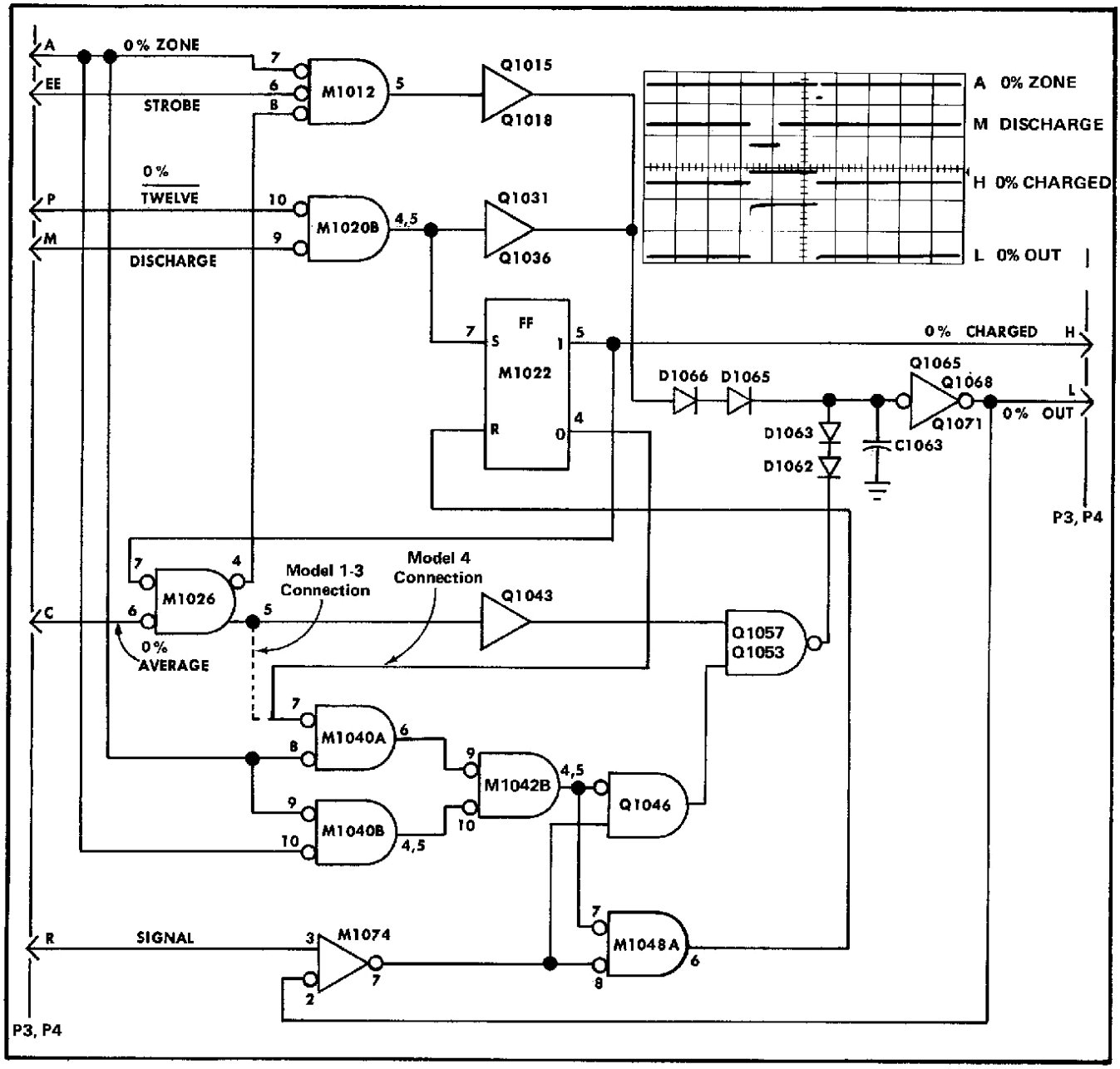


Fig. 4-8. 0% memory circuit logic diagram.

duction. The conduction of Q1031 turns on Q1036, which completes a current path for memory capacitor C1063 through D1065, D1066, and Q1036. Capacitor C1063 now charges to about +6 volts. This is considered to be the discharged state of C1063. As the DISCHARGE pulse ends and again goes high, Q1036 cuts off, disconnecting the discharge path for C1063.

The 0% memory circuit now waits until the 0% ZONE pulse from the Zone generator circuit moves low. The low 0% ZONE pulse is applied to NAND gate M1040B pin 9 and to NAND GATE M1040A pin 8. Since the input to M1040A pin 7 is receiving a low from M1022 pin 4 (Model 4-up), the output at M1040A pin 6 goes high. The high output of M1040A is applied to M1042B pin 9 causing the output at M1024B pins 4 and 5 to go low. The low output from M1042B is connected to M1048A pin 7, permitting M1074 to control the gate via the pin 8 input. The low output of M1042B also is applied to the base of Q1046, and enables the transistor. Thus, the 0% ZONE pulse has enabled the memory charging circuit. Whether the charge in C1063 gets changed or not is now dependent upon the output of the differential comparator, M1074. The low output of M1042B enables input pin 7 of NAND gate M1048A, allowing M1074 to control the gate.

NOTE

In Memory circuit cards Models 1, 2, and 3, pin 7 of M1040A is connected to pin 5 of M1026 instead of M1022 pin 4 as in Model 4 and up. The earlier configuration caused the state of M1040A to be dependent upon the condition of the AVERAGE signal. Models 4-up are no longer dependent upon this condition.

The signal input on pin R is applied to the inverting input (pin 3) of M1074. The memory output is applied via resistor R1073 to the non-inverting input (pin 2). Now, if the voltage across C1063 is greater than the signal voltage, the output of M1074 goes positive and turns on Q1046 through resistor R1046. The conduction of Q1046 biases Q1053 into conduction, closing the charge path from −3.5 volts through Q1057, Q1053, D1062, D1063 and R1063. High current through this path very quickly reduces the positive charge in C1063 and the memory output follows the change in C1063 voltage. When the voltage across C1063 reaches the signal input voltage, M1074 pin 7 immediately goes low and cuts off Q1046. The voltage across C1063 is now a close approximation of the signal voltage at this instant (the beginning of the 0% ZONE). The low output of M1074 pin 7 activates NAND gate M1048A, M1048A resets flipflop M1022, and M1022 sends a signal (via pin H) to the Synchronizer circuit that the 0% memory is charged.

Switching M1022 also applies a low to M1026 pin 7. The output on M1026 pin goes high (AVERAGE is assumed to be low). The output of M1026 pin 4 is applied through resistor R1011 to M1012 pin 8. Since both 0% ZONE and STROBE are already low, the output of M1012 pin 5 goes high after about 1 microsecond of delay caused by R1011 and C1011. The high output from M1012 pin 5 biases on transistors Q1015 and Q1018. A small amount of current now flows through the path consisting of R1063, D1065, D1066, Q1018, and R1018, pulling the voltage on C1063 positive.

In Model 4-up, pin 4 output of M1022 goes high, and after about 1 microsecond of delay caused by R1041 and C1041, M1040A pin 7 goes high and output pin 6 goes low, enabling pin 9 of NAND gate M1042B. The high output on M1026 pin 5 is applied through R1042 to the base of Q1043, causing Q1043 to conduct and Q1057 to cut off.

In Models 1-3, the high output of M1026 pin 5 is applied through R1041 to M1040A pin 7 and to Q1043 base. After about one microsecond delay caused by R1041 and C1041, Q1043 is biased into conduction and cuts off Q1057. The high also causes that output of M1040A pin 6 to go low, enabling M1042B pin 9. Since both 0% ZONE and STROBE are low, the output of M1040B is high and causes the output of M1042B to be low. The output of M1042B is applied as enabling bias to Q1046 base.

As the current through Q1018 pulls the voltage on C1063 positive, the 0% memory output voltage rises also (all models). When the 0% memory output voltage equals the signal voltage, M1074 switches and its output on M1074 pin 7 goes high. The high from M1074 pin 7 is applied to Q1046 emitter and Q1046 now conducts and biases Q1053 on. The conduction of Q1053 through R1059 starts pulling the voltage on C1063 slowly negative again. Differential comparator M1074 now switches rapidly back and forth, constantly balancing the voltage on C1063 with the signal voltage. Flipflop M1022 continues to send a 0% memory charged signal to the synchronizer, since it does not set again until DISCHARGE occurs.

At the end of the 0% ZONE pulse, M1012 pin 7 goes high, M1012 pin 5 goes low, transistor Q1015 turns off, and the path from C1063 to the +50-volt supply opens. The input to M1040B pin 9 and M1040A pin 8 goes high and both NAND gates deliver low outputs. NAND gate M1042B now delivers a high on its output pins 4 and 5 and applies cutoff bias to the base of Q1046. Turning off Q1046 biases Q1053 off also, opening the path from C1063 to the −50-volt supply. Memory capacitor C1063 is now disconnected from any charge or discharge path and retains its charge until the DISCHARGE pulse or another 0% ZONE pulse occurs.

At the start of the foregoing description it was assumed that STROBE remained low. The assumption was made in order to simplify the explanation. In actual practice, the only time that STROBE remains low is when the Type 3B2 is used as the horizontal plug-in unit. At clock rates of 100 kHz and below, as in equivalent-time sampling, the STROBE pulse is delayed for about two microseconds following each clock pulse, then is low for a period of about six microseconds.

Strobing the memories with 6 μs pulses provides for better averaging. Without strobing, it would be possible for the memories to contain a voltage representing a noise spike or misplaced sample at the time ZONE goes high. With strobing, the memory voltage is permitted to move 10 mV during each 6 μs strobe pulse, thus averaging out misplaced samples or noise spikes. The fact that STROBE is switching between high and low does not invalidate the foregoing explanation; the action is merely broken up into 6 μs periods as the STROBE pulses switch NAND gates M1012 and M1040B.

Likewise in the description it was assumed that $\overline{\text{TWELVE}}$ was low. This is always so in front-panel operation. With $\overline{\text{TWELVE}}$ low, the memories are discharged at the beginning of each memory sweep. However, when making programmed measurements, it is frequently advantageous to discharge the memories, charge them during the zones, then make a whole series of voltage and time measurements before again discharging the memories. This saves the time normally spent on first discharging, then charging, the memories on separate memory sweeps for each measurement. As an example, after making a memory charging sweep, it is possible to program a measurement series consisting of A volts, B volts, A risetime, B risetime, Time between A and B, and so on.

When programming the $\overline{\text{TWELVE}}$ function, certain other program inputs and conditions are required also. These are as follows:

1. The Type 230 must be set for triggered measurement and must receive a trigger from the readout equipment or other source.

2. The time-base unit must be synchronized with the Type 230. This can be accomplished by programming HIGH SPEED.

3. The series of measurements must be made on a repetitive input waveform (or waveforms when using both A and B channels).

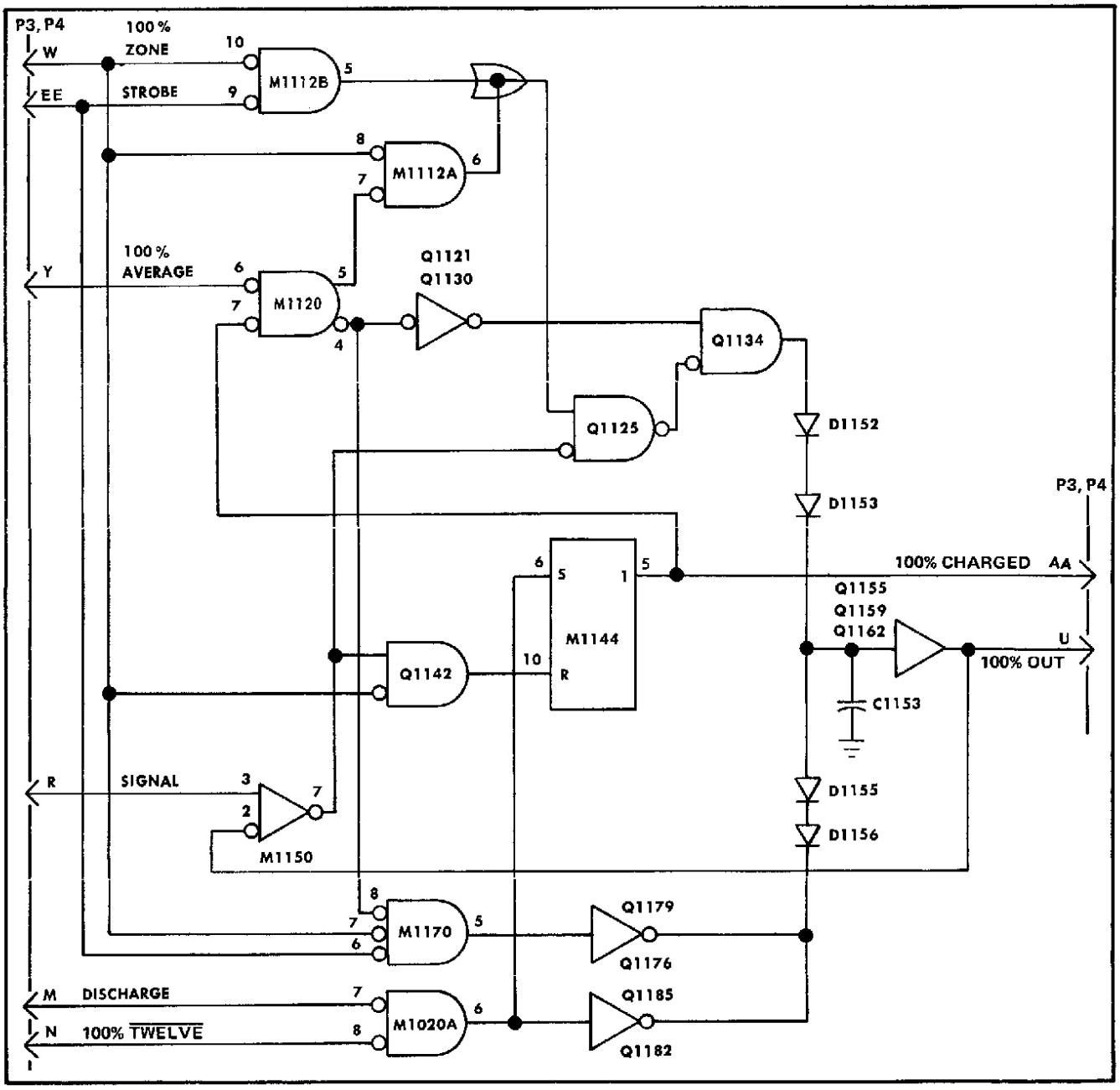


Fig. 4-9. 100% memory circuit logic diagram.

4. The first measurement in the series should be made before TWELVE is programmed.

5. The vertical sensitivity, offset, trace position and signal must remain the same throughout the measurement series. For further information concerning the programming of the TWELVE function, see the Programming section of this manual.

Operation of the Type 230 in any of the peak modes causes AVERAGE to go high. The 0% memory changes its operation as explained in the following paragraphs.

The high AVERAGE signal applied to M1026 pin 6 causes a high output at M1026 pin 4. The high from M1026 pin 4 to M1012 pin 8 inhibits M1012, turning off Q1015 and Q1018. Current flow through Q1036 provides discharge current for C1063 during DISCHARGE time.

In Models 1 through 3, the high AVERAGE signal applied to M1026 pin 6 causes the output of M1026 pin 5 to go low, enabling M1040A pin 7. The other input, M1040A pin 8, is activated by the now widened 0% ZONE pulse (ZONE is widened because of the uncertainty as to where the peak signal actually occurs). The low output of M1026 pin 5

also biases Q1043 and Q1057 into conduction, providing additional current to charge C1063 at a faster rate.

In Model 4-up, the low output at M1022 pin 4 enables pin 7 of M1040A. The other input, M1040A pin 8, is activated by the now widened 0% ZONE pulse (ZONE is widened because of the uncertainty as to where the peak signal actually occurs). The high AVERAGE signal applied to M1026 pin 6 causes the output of M1026 to go low, turning off transistor Q1043 and enabling the base of Q1057.

The 0% memory circuit (all models) is now able to follow rapid negative increases in signal level, but since Q1018 is biased off, positive-going excursions of the signal are ignored. The 0% memory circuit output now represents the most negative peak that occurs during the low state of 0% ZONE.

100% Memory Circuit

The 100% memory circuit is similar in operation to the 0% memory circuit except that where the 0% memory capacitor is discharged positively to +6 volts and charged to +2 volts (with the trace centered), the 100% memory capacitor is discharged to —2 volts and charged to +2 volts. The reason for the circuit differences between the two memories is that 0% memory must charge quickly in the negative direction while the 100% memory must charge positive rapidly, when in peak mode.

For purposes of explanation, assume that 100% AVERAGE, STROBE, and $\overline{\text{TWELVE}}$ are low (see circuit diagram). Assume also that the 100% ZONE and DISCHARGE inputs are high and that a signal is applied to pin R. Under these conditions the high 100% ZONE signal on NAND gate M1112B pin 10 causes a low on M1112B pin 5. The low on M1112B pin 5 is applied through a phantom OR gate (see Fig. 4-9) to the base of transistor Q1125, biasing it off. Turning off Q1125 biases off transistor Q1134 and thereby reverse biases diodes D1152 and D1153. The high 100% DISCHARGE signal on NAND gate M1020A pin 7 causes a low output on M1020A pin 6, biasing off transistors Q1182 and Q1185. Diodes D1155 and D1156 are consequently reverse biased by the path through resistor R1178 to +50 volts. With D1152, D1153, D1155, and D1156 all reverse biased, the charge on memory capacitor C1153 cannot change.

The negative-going DISCHARGE pulse is applied to M1020A pin 7. The 100% $\overline{\text{TWELVE}}$ signal at M1020A pin 8 is also low, so the output on C1020A pin 6 goes high. The high output of M1020A pin 6 sets flipflop M1144 and the output on M1144 pin 5 goes high. The high output of M1144 pin 5 is applied to the Synchronizer card and signals that the 100% memory is not charged. The high signal from M1020A also biases Q1182 and Q1185 into conduction, discharging C1153 to —2 volts. This is the discharged state of the 100% memory capacitor. As the DISCHARGE pulse ends and again goes high, M1020A pin 6 goes low, cutting off Q1182 and Q1185 and disconnecting the discharge path for C1153.

The 100% memory circuit now waits until the 100% ZONE pulse from the Zone generator circuit card arrives at pin W. The negative-going 100% ZONE pulse is applied to NAND gate M1112B pin 10. With both inputs low, M1112B pin 5 goes high and turns on transistors Q1125 and Q1134. The high output of flipflop M1144 pin 5 causes AND/NAND gate M1120 pin 4 to go high and turn on transistors Q1121 and Q1130. The current flow through Q1134 and Q1130 forward biases D1152 and D1153 and applies a heavy charge current to C1153. As the voltage across C1153 quickly goes positive, the operational amplifier consisting of Q1155, Q1159 and Q1162 follows the change and delivers a positive-going signal to differential comparator M1150 pin 2. When the memory output voltage equals the signal voltage, M1150 switches and applies a high to Q1125 emitter, cutting it off. The high output of M1150 pin 7 is also applied to Q1152 emitter. With 100% ZONE low, Q1142 turns on and switches flipflop M1144 via M1144 pin 10. The output M1144 pin 5 goes low, signaling the Synchronizer card that the 100% memory is charged. The voltage in C1153 is now a close approximation of the signal voltage at this instant (the beginning of the 100% ZONE).

Switching M1144 also applies a low to M1120 pin 7. The output on M1120 pin 4 goes low and turns off transistors Q1121 and Q1130, opening the high-current charge path to C1153. The low output on M1120 pin 4 is also applied to M1170 pin 8. The input to M1170 pin 7 is the 100% ZONE pulse, the input to pin 6 is the STROBE signal. The output of M1170 pin 5 now goes high and low at the STROBE rate, turning Q1176 and Q1179 off and on. Turning the two transistors off and on starts removing the charge from C1153. When the charge on C1153 falls slightly below the signal level, M1150 switches and turns Q1125 back on. Turning on Q1125 again biases Q1134 back into conduction and starts recharging C1153. The charging current is turned off and on in accordance with the STROBE signal applied to M112B pin 9. When the charge in C1153 again exceeds the signal voltage, M1150 once again switches and starts the discharge process. The switching of M1150 is very rapid and the charge on C1153 is held very close to the signal level for the duration of the 100% ZONE pulse.

Operation of the Type 230 in any of the peak modes causes AVERAGE to go high as previously explained. The 100% memory changes its operation as explained in the following paragraphs.

The high AVERAGE signal applied to M1120 pin 6 causes a high output at M1120 pin 4. The high from M1120 pin 4 to Q1121 base turns on Q1121 and Q1130. The conduction of Q1121 and Q1130 provides additional current through Q1134 to charge C1153. The high from M1120 pin 4 is also applied to M1170 pin 8. The output on M1170 pin 5 goes low and biases Q1176 and Q1179 off, opening the discharge path for C1153. With the charge path controlled by the operation of M1150, M1120, M1112B, Q1121, Q1130, Q1125, and Q1134, the memory circuit is now able to follow rapid increases in signal level. However, with Q1176 and Q1182 cut off, decreases in signal level are ignored. The memory circuit output now represents the highest peak that occurs during the 100% ZONE pulse. As in the case of the 0% memory, the 100% ZONE pulse is widened because of the uncertainty as to where the peak signal actually occurs.

Operation of the 100% memory circuit with $\overline{\text{TWELVE}}$ programmed high is similar to the operation of the 0% Memory circuit with similar programming. The $\overline{\text{TWELVE}}$ signal is programmed high before the second measurement and causes the output of M1020A pin 6 to remain low, disabling the path for the DISCHARGE signal.

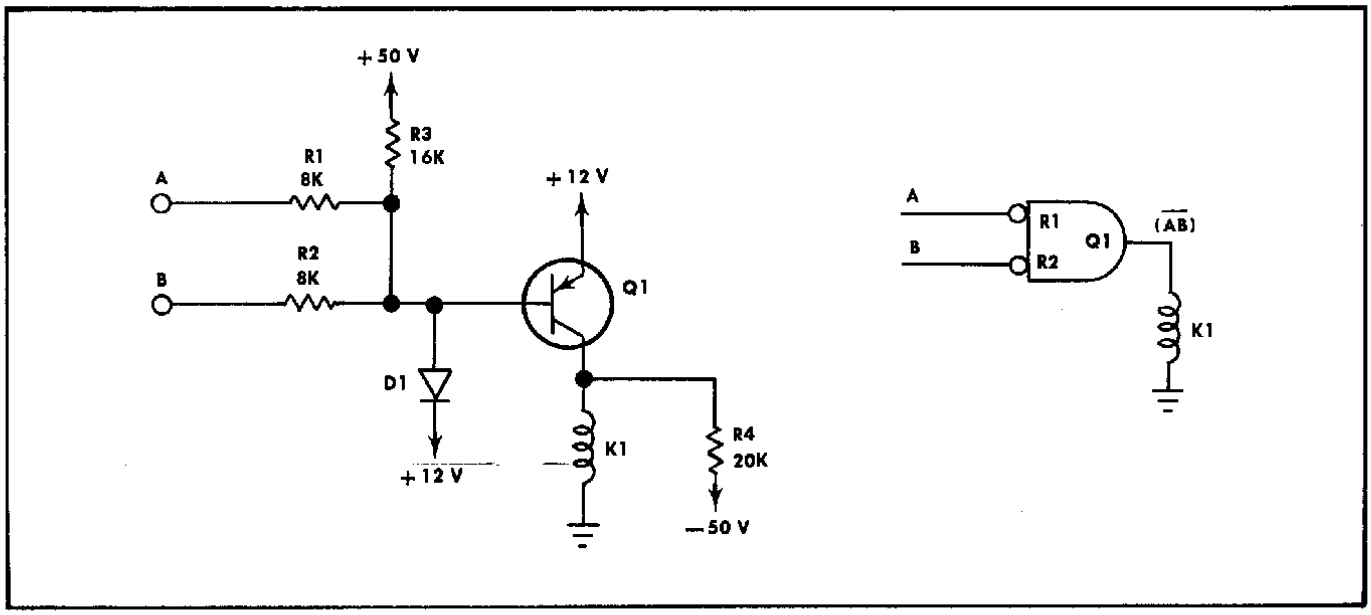


Fig. 4-10. Basic RTL circuit and logic symbol.

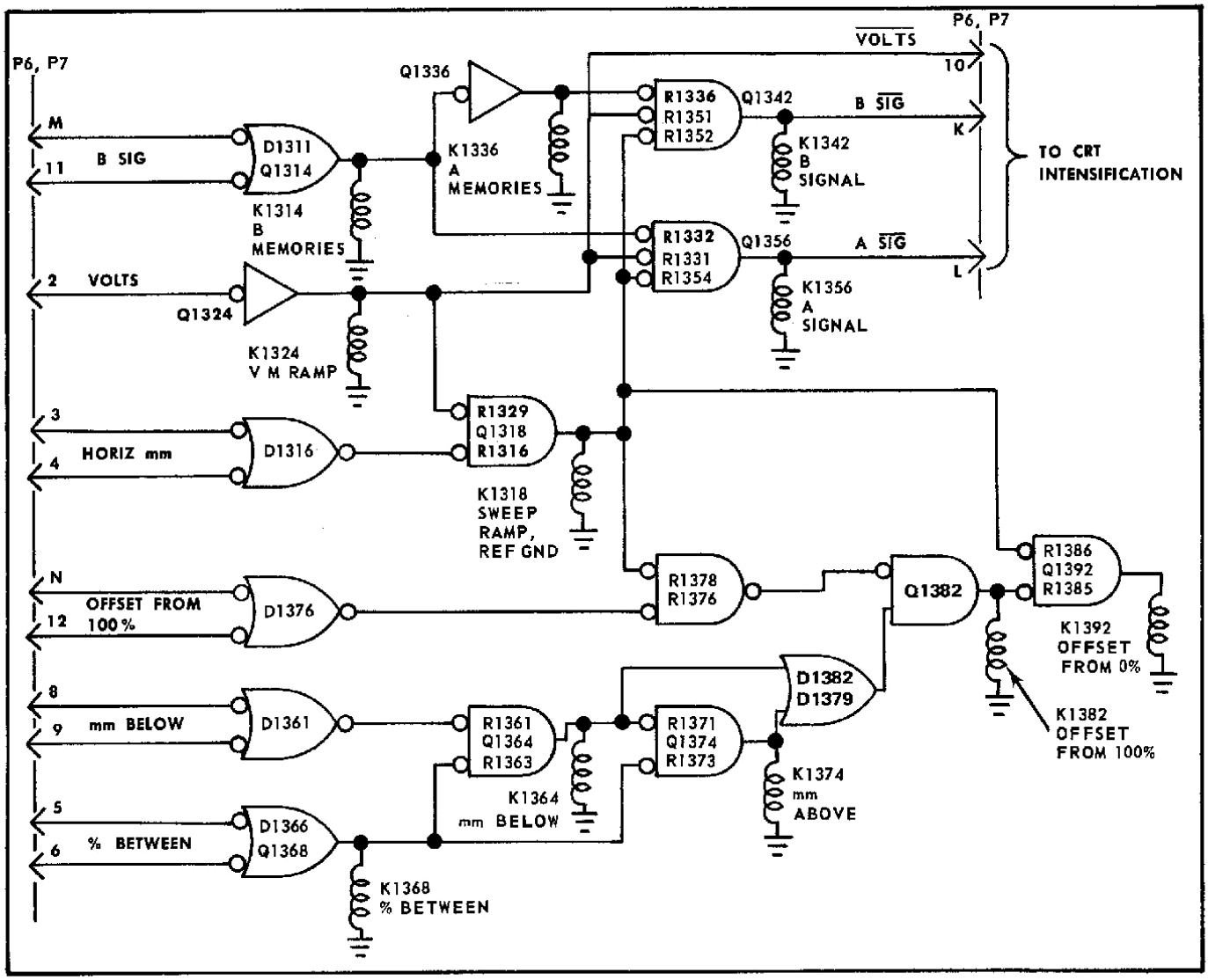


Fig. 4-11. Comparator function logic diagram.

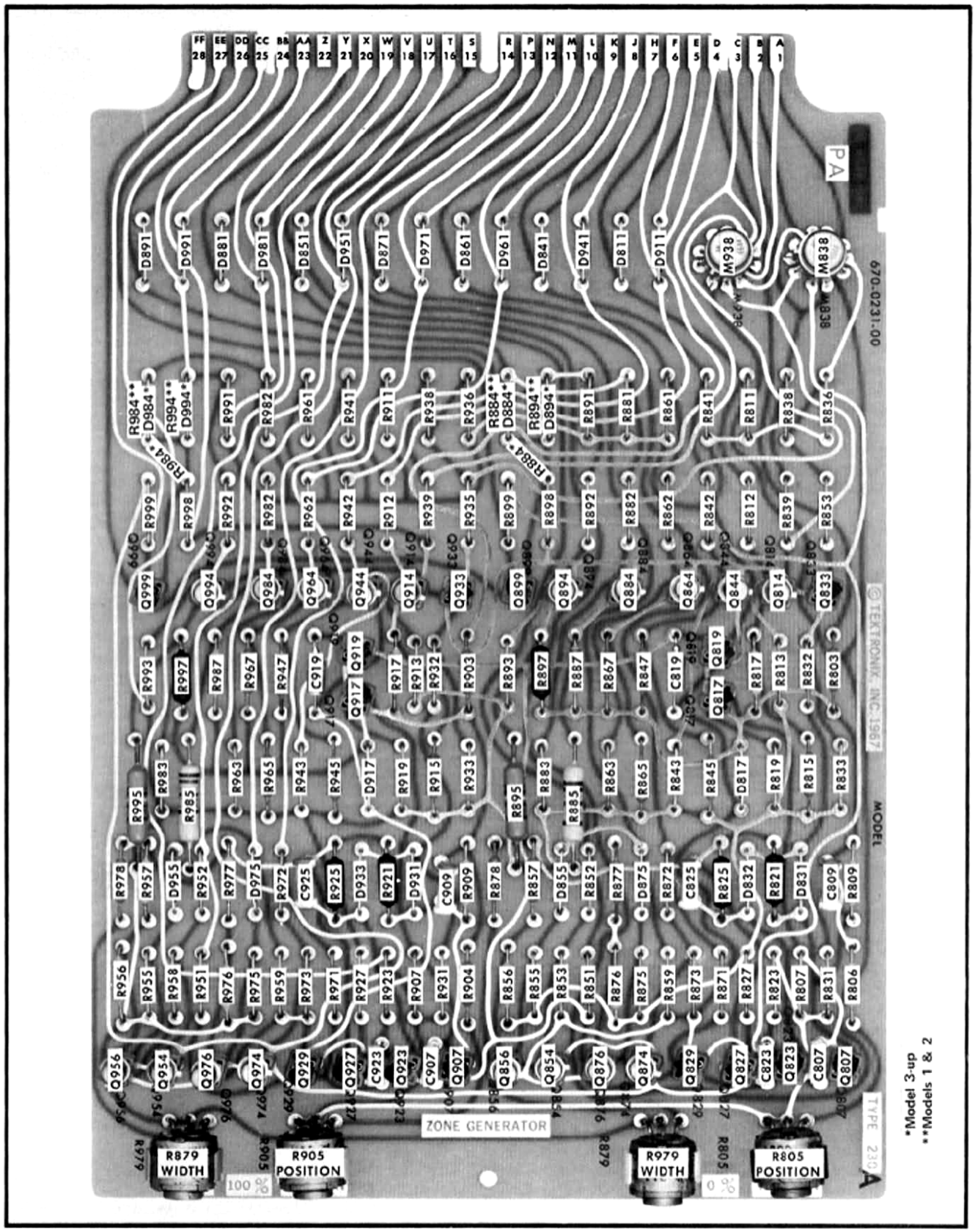


Fig. 5-8. Component locations on the Ch A or Ch B Zone Generator card.

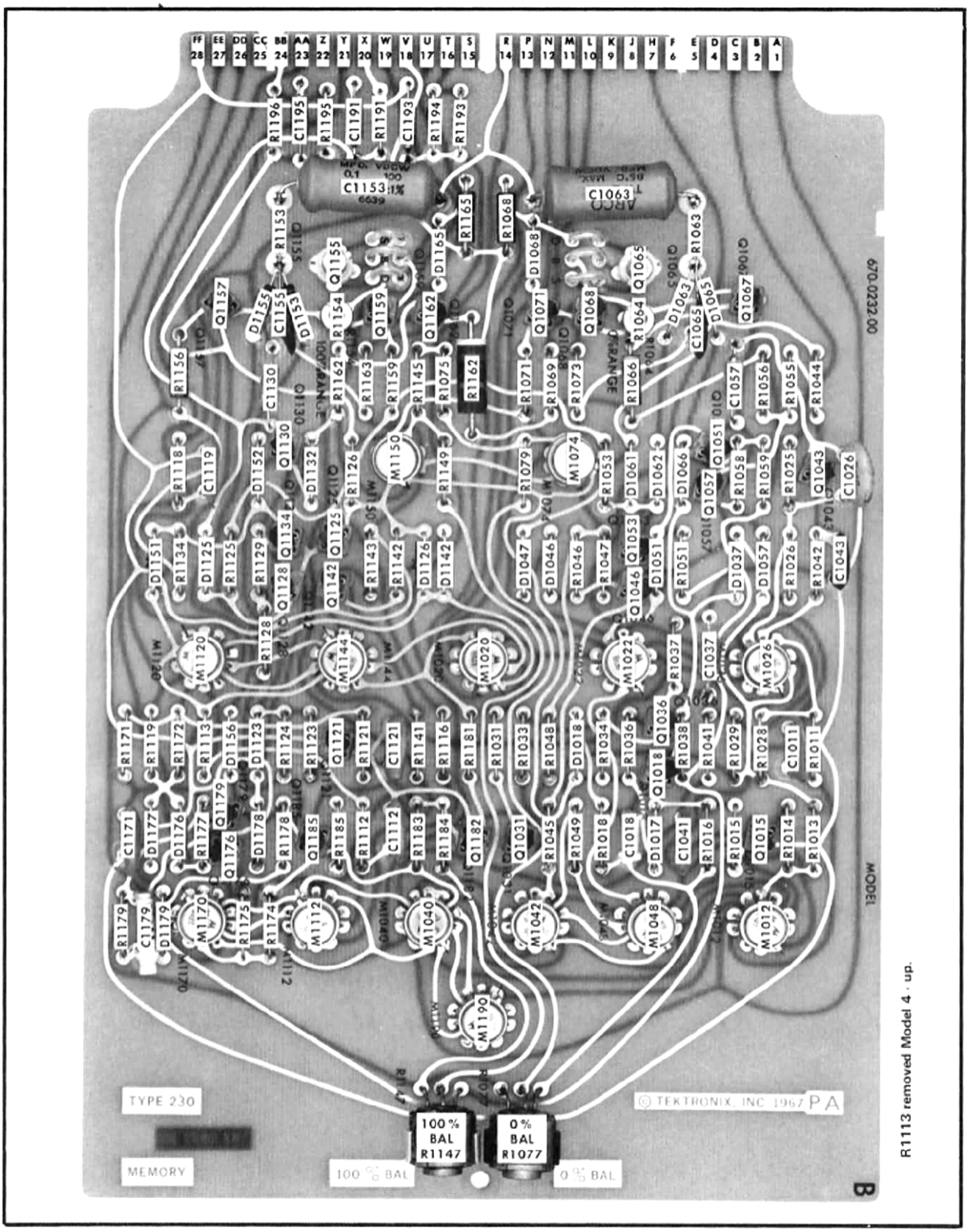


Fig. 5-9. Component locations on the Ch A or Ch B Memory card.

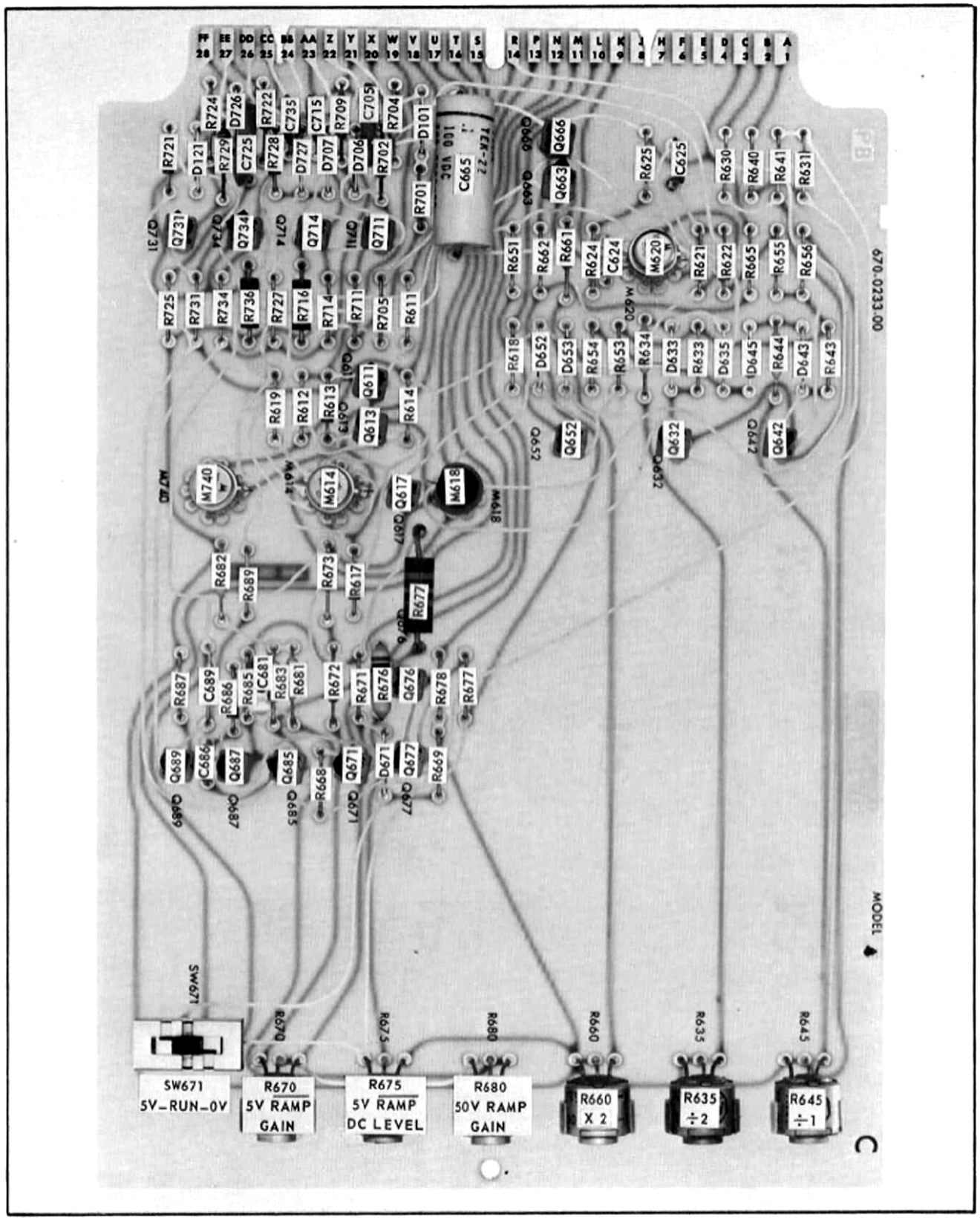


Fig. 5-10. Component locations on the Buffer card (Model 4-up).

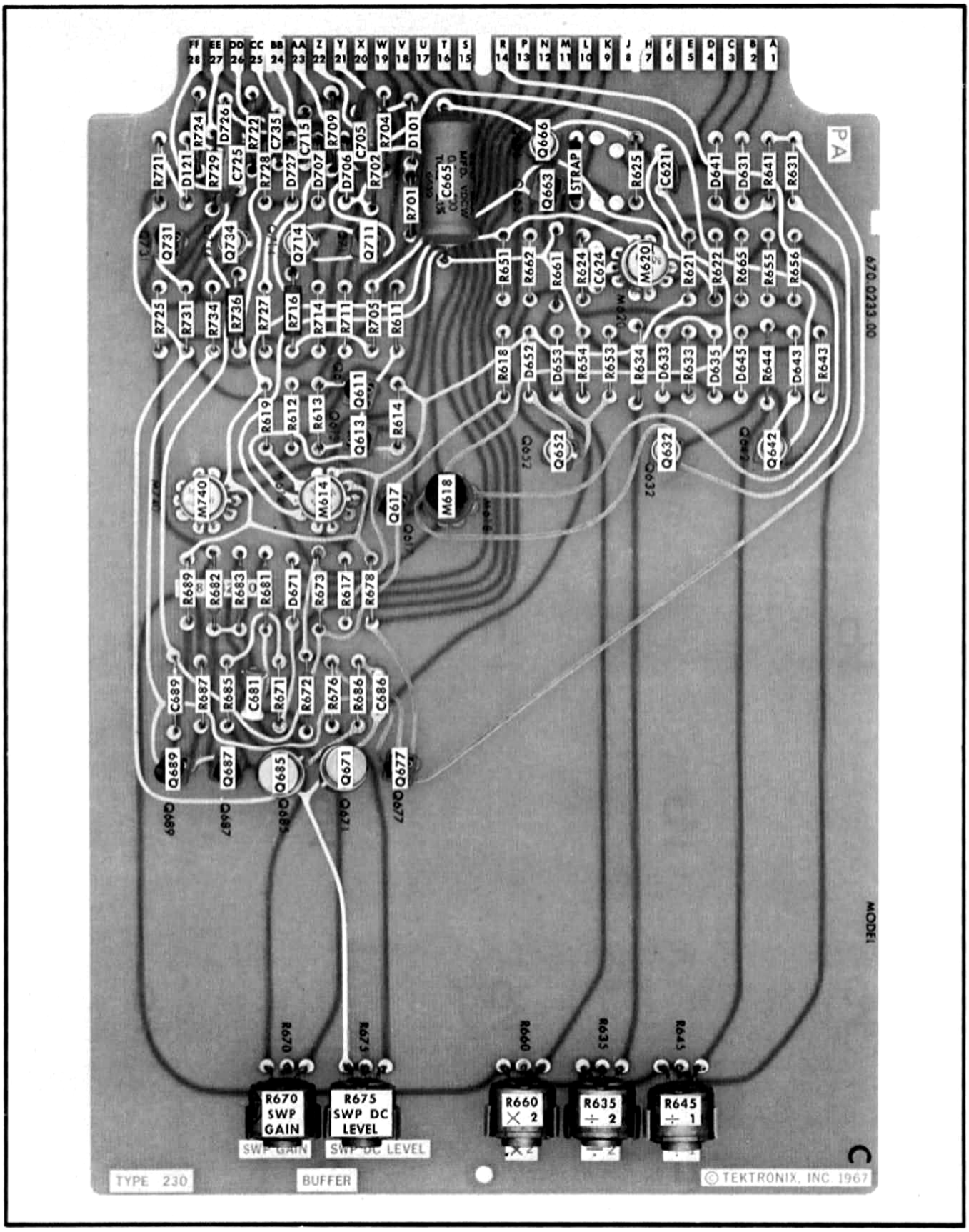


Fig. 5-11. Component locations on the Buffer card (Models 1-3).

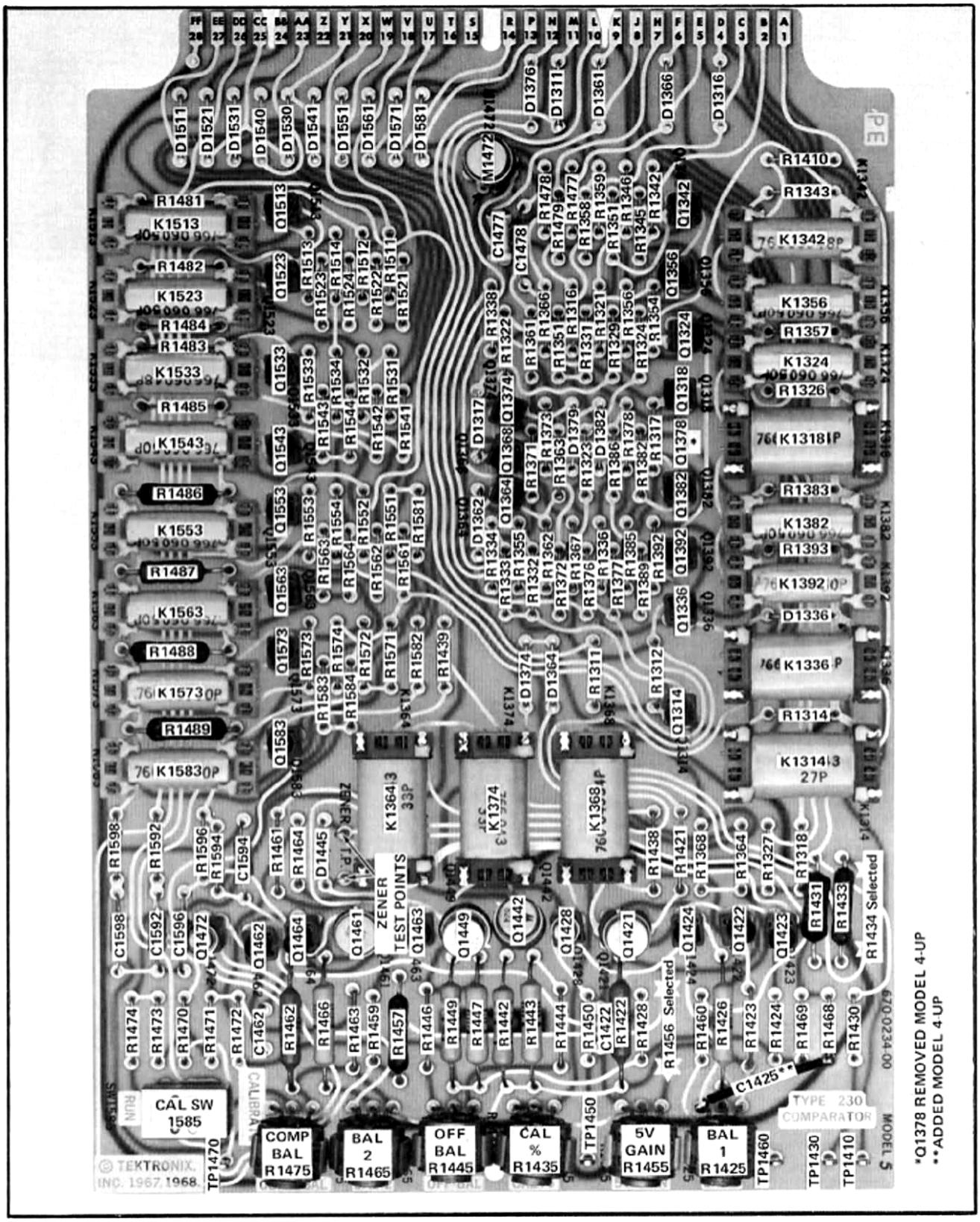


Fig. 5-12. Component locations on the Start or Stop Comparator card.

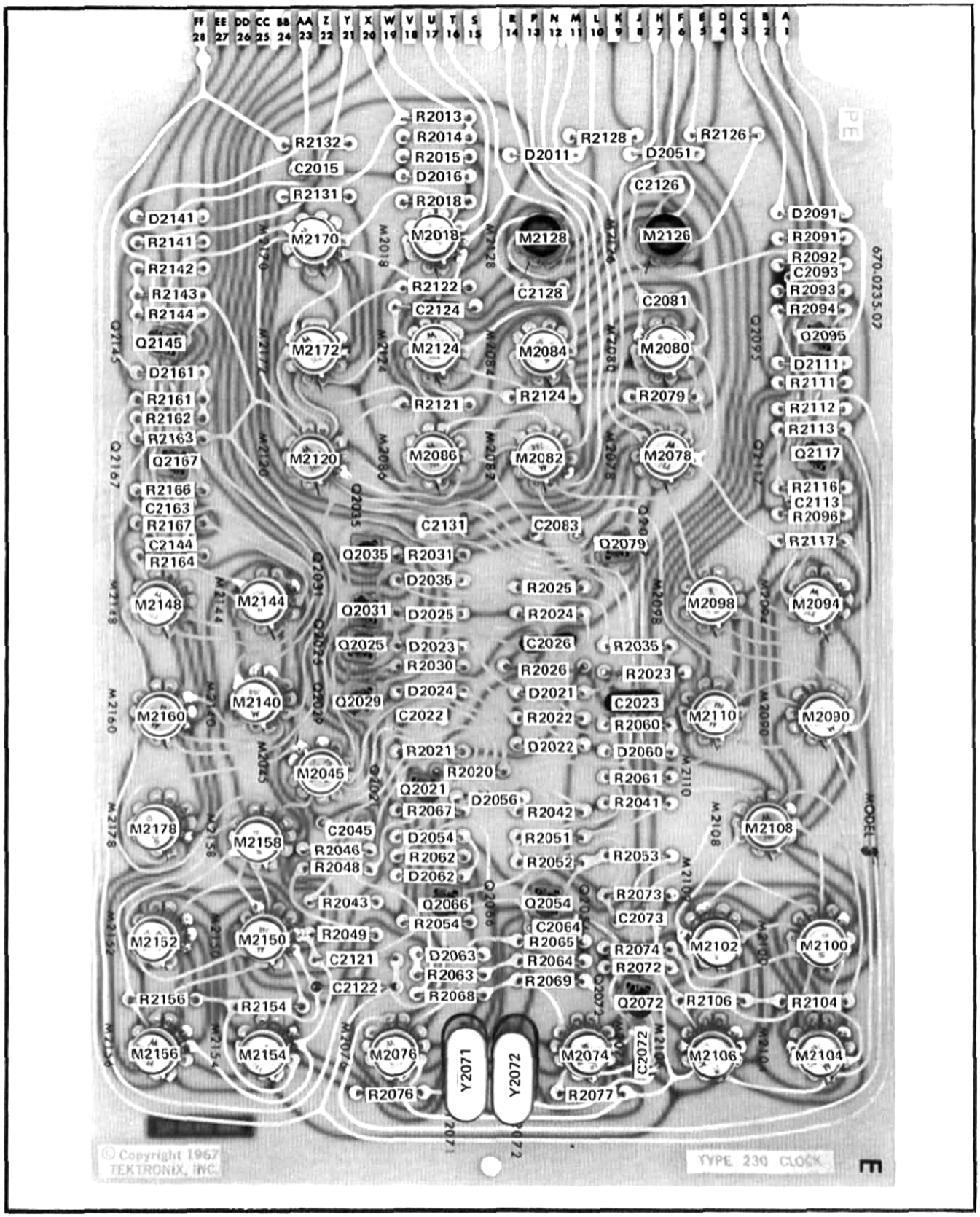


Fig. 5-13. Component locations on the Clock Card (Model 3-up).

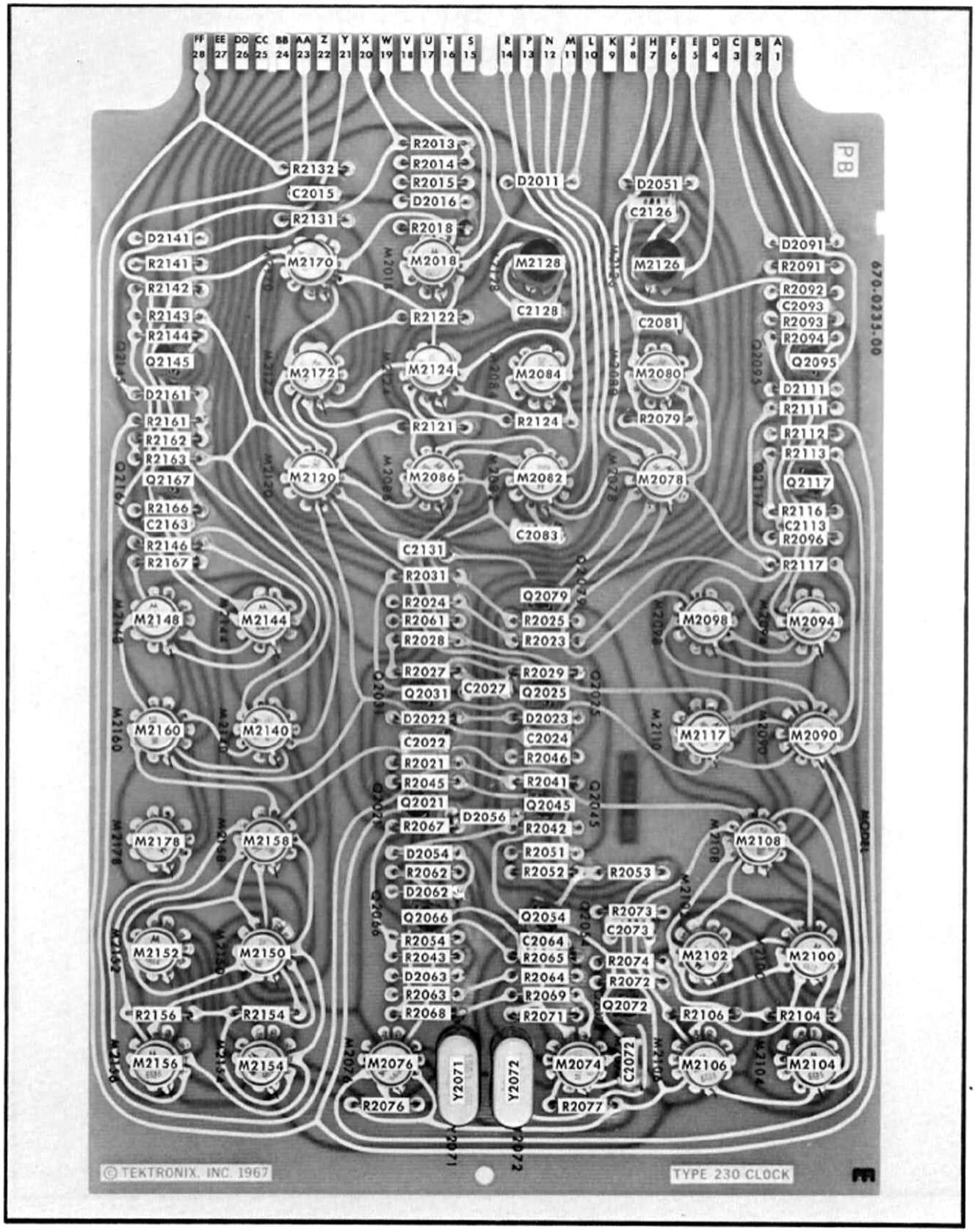


Fig. 5-14. Component locations on the Clock Card (Model 1 and 2).

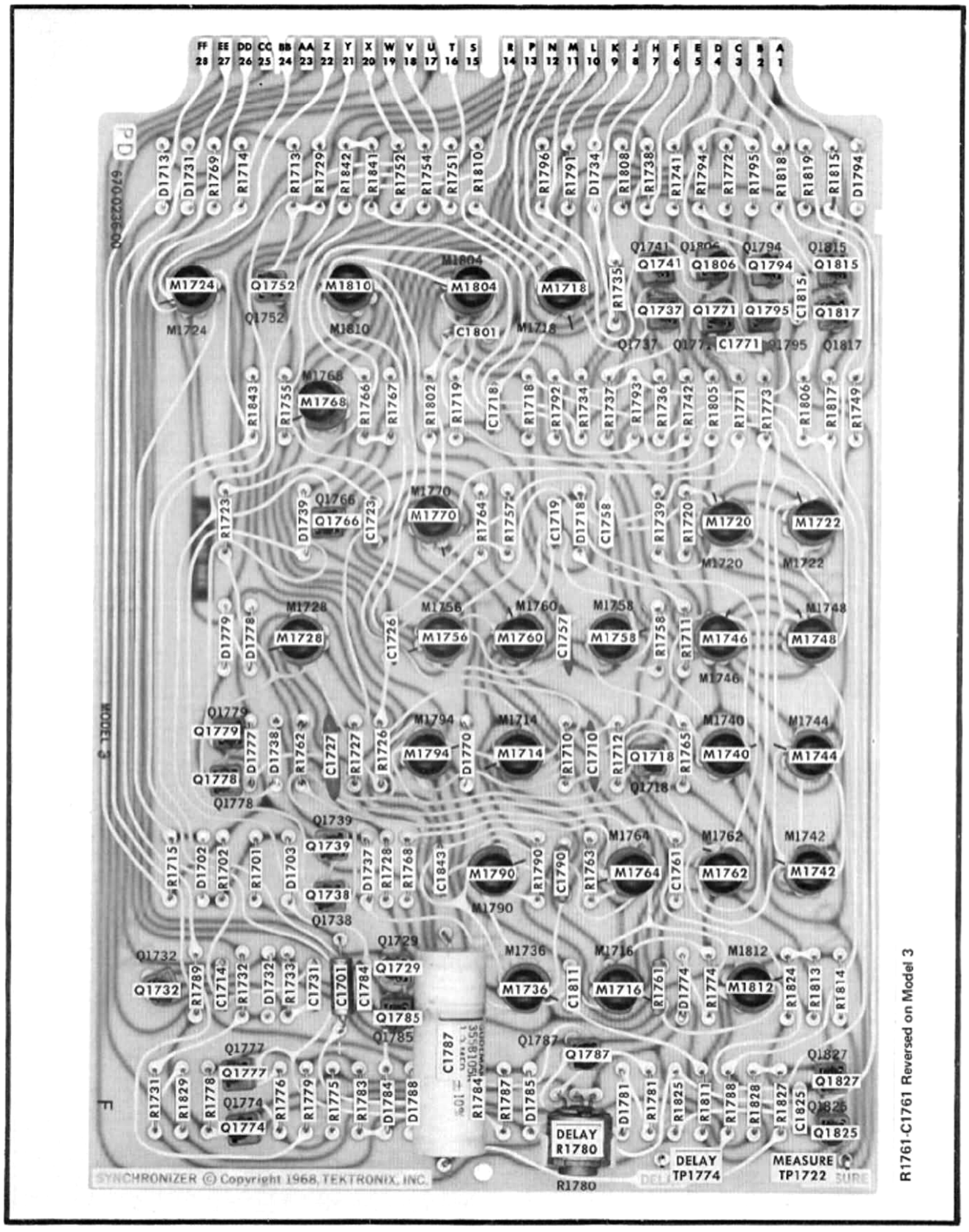


Fig. 5-15. Component locations on the Synchronizer card (Model 3-up).

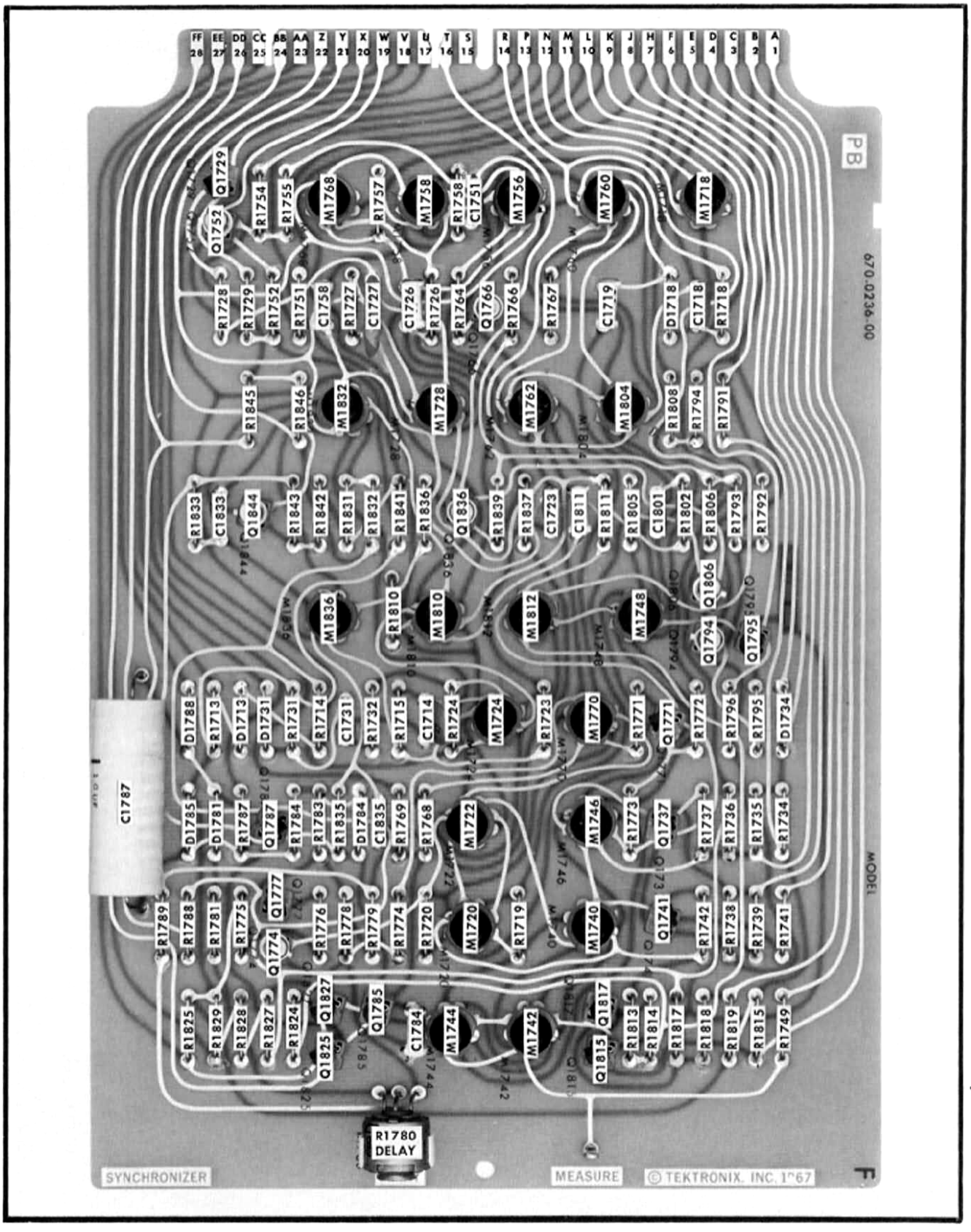


Fig. 5-16. Component locations on the Synchronizer card (Model 1 and 2).

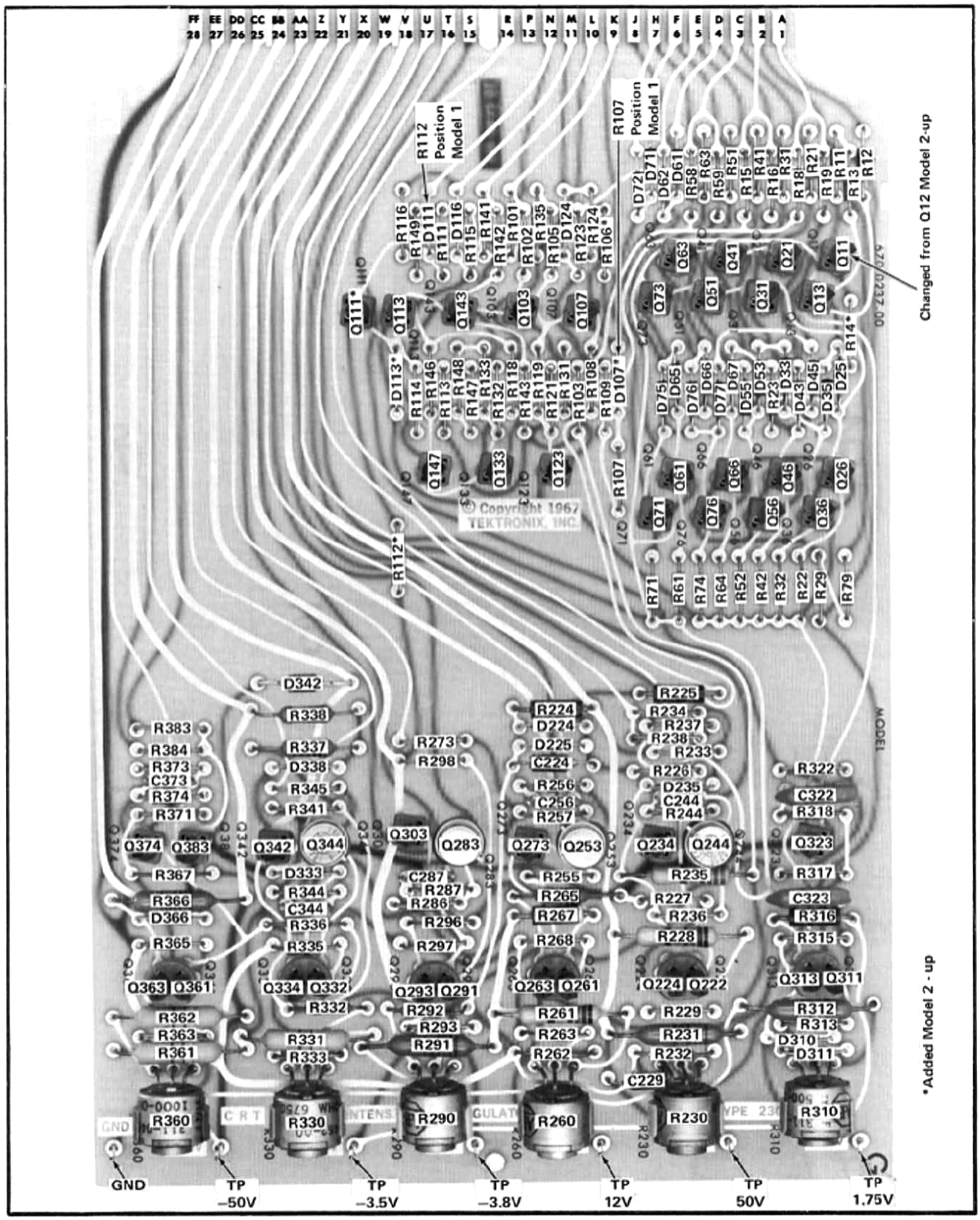


Fig. 5-17. Component locations on the CRT INTEN/Regulator card.

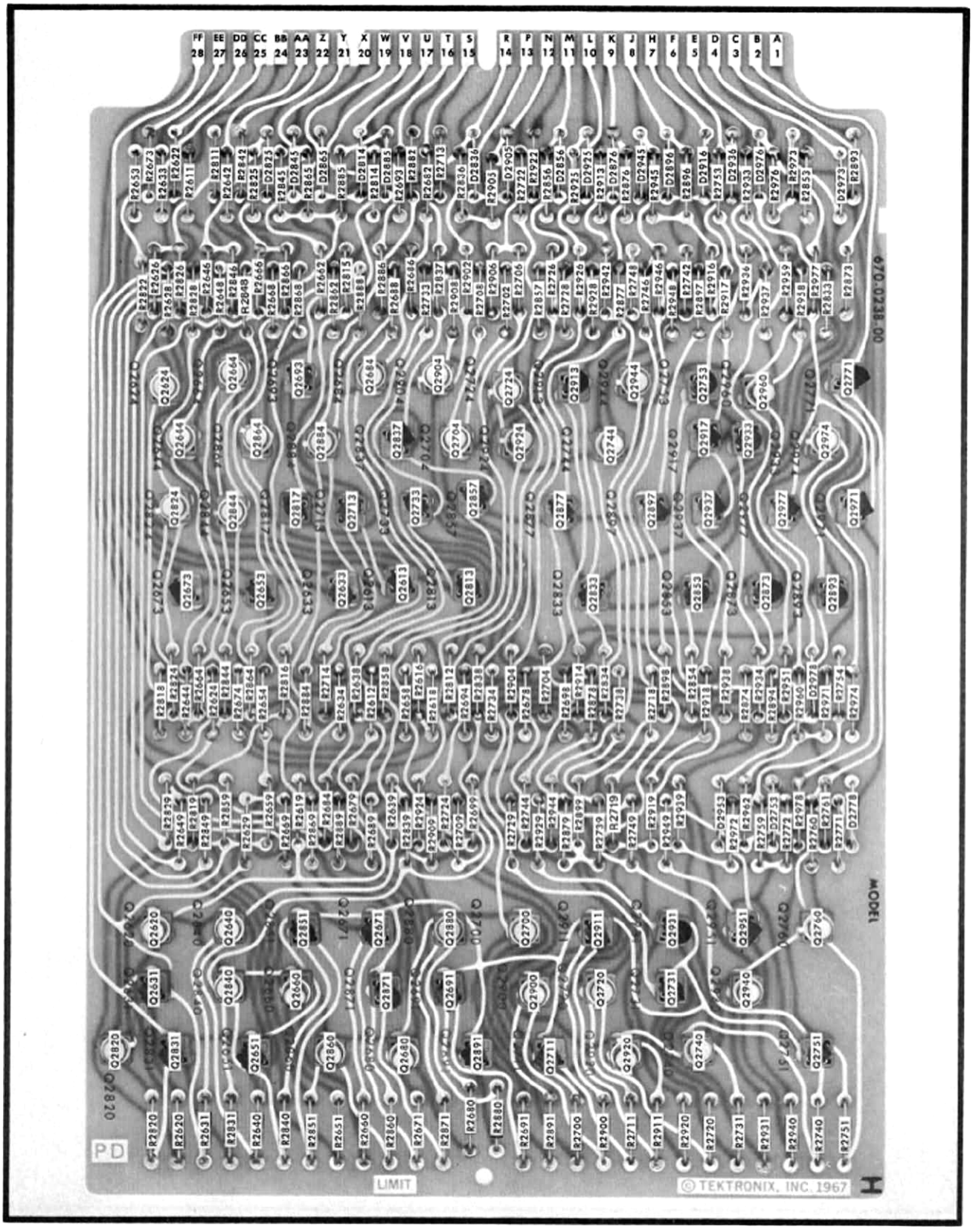


Fig. 5-18. Component locations on the Limit card (Model 1).

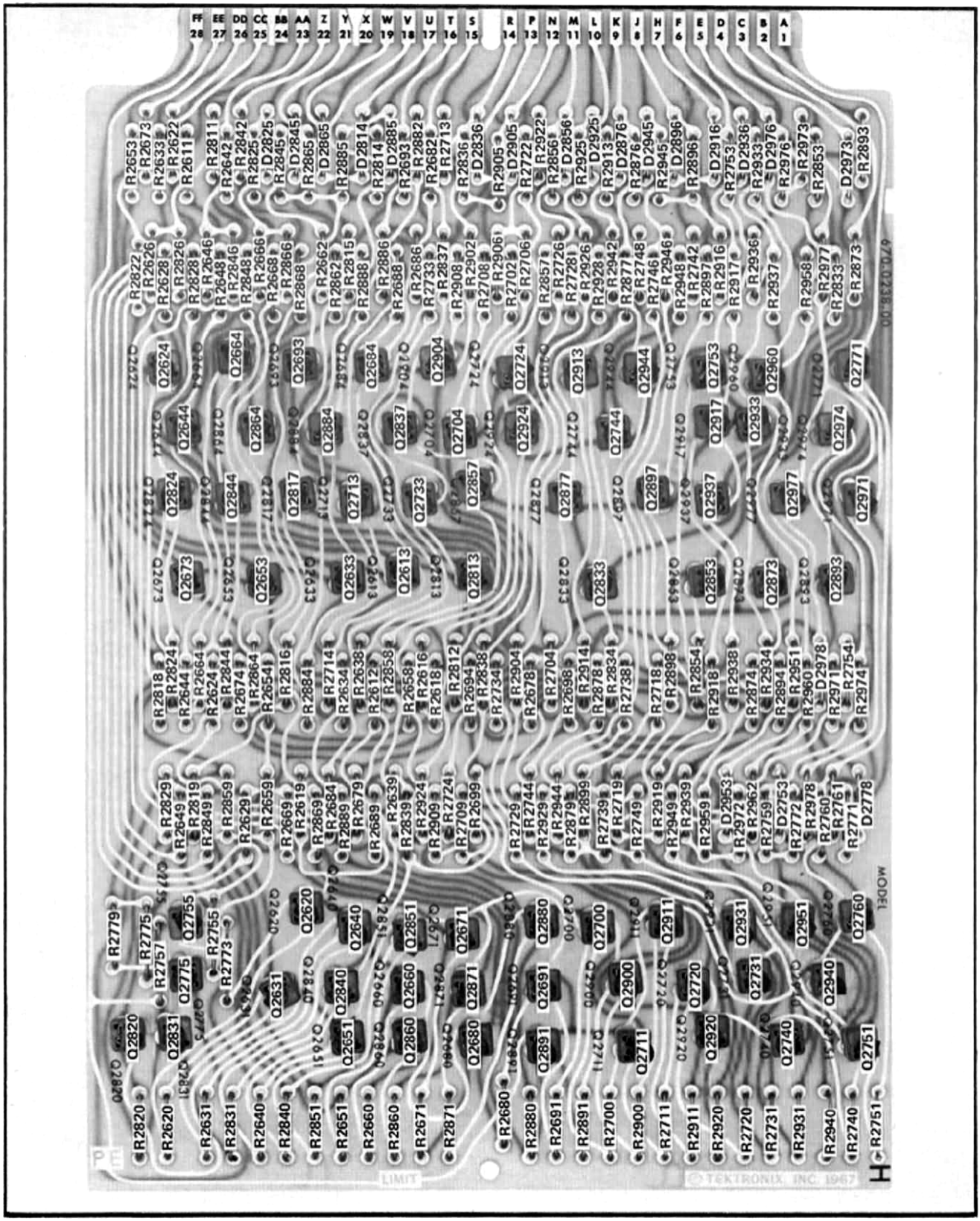


Fig. 5-19. Component locations on the Limit card (Model 2-up).

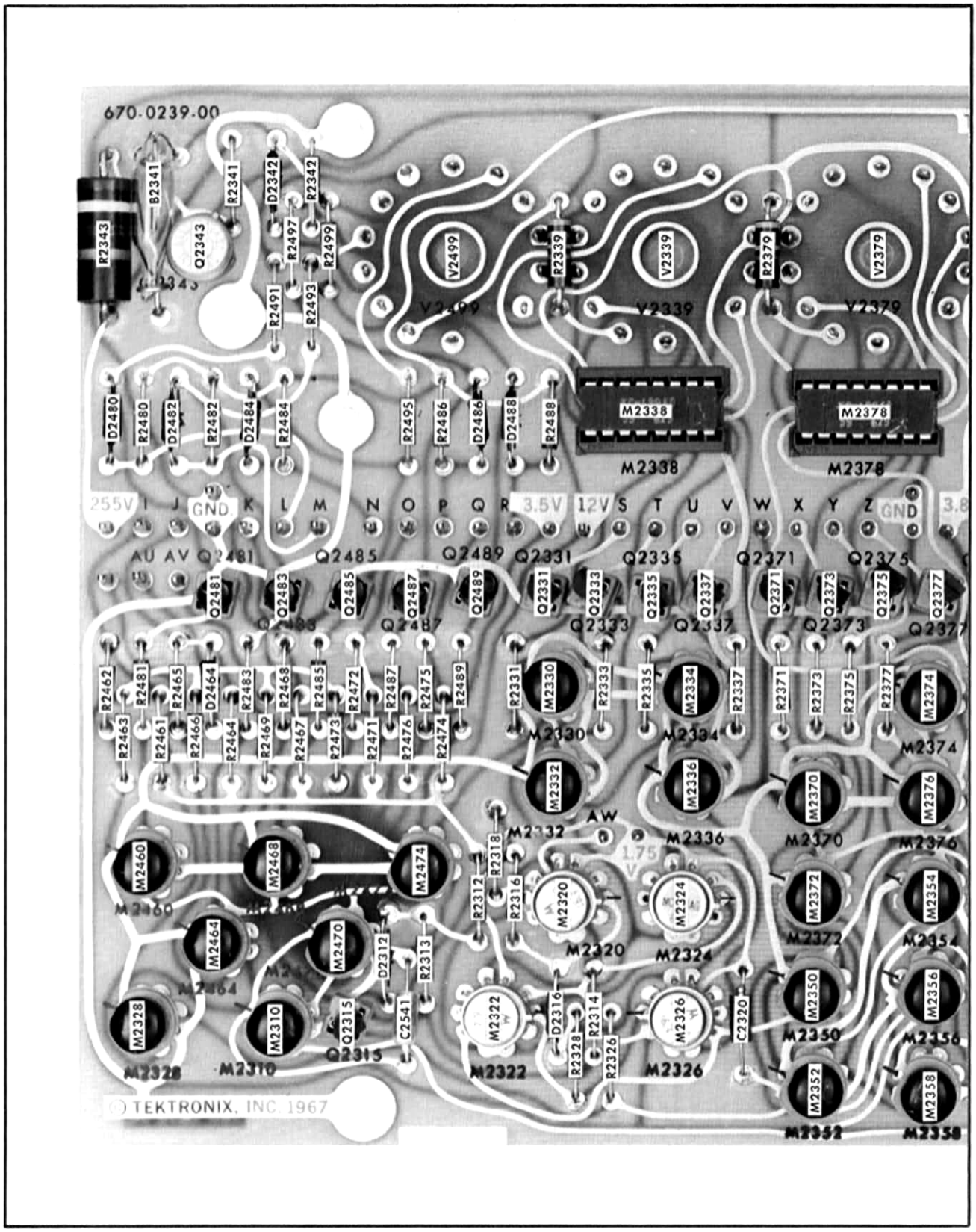


Fig. 5-20. (A and B) Pin connection locations on the Counter circuit board.

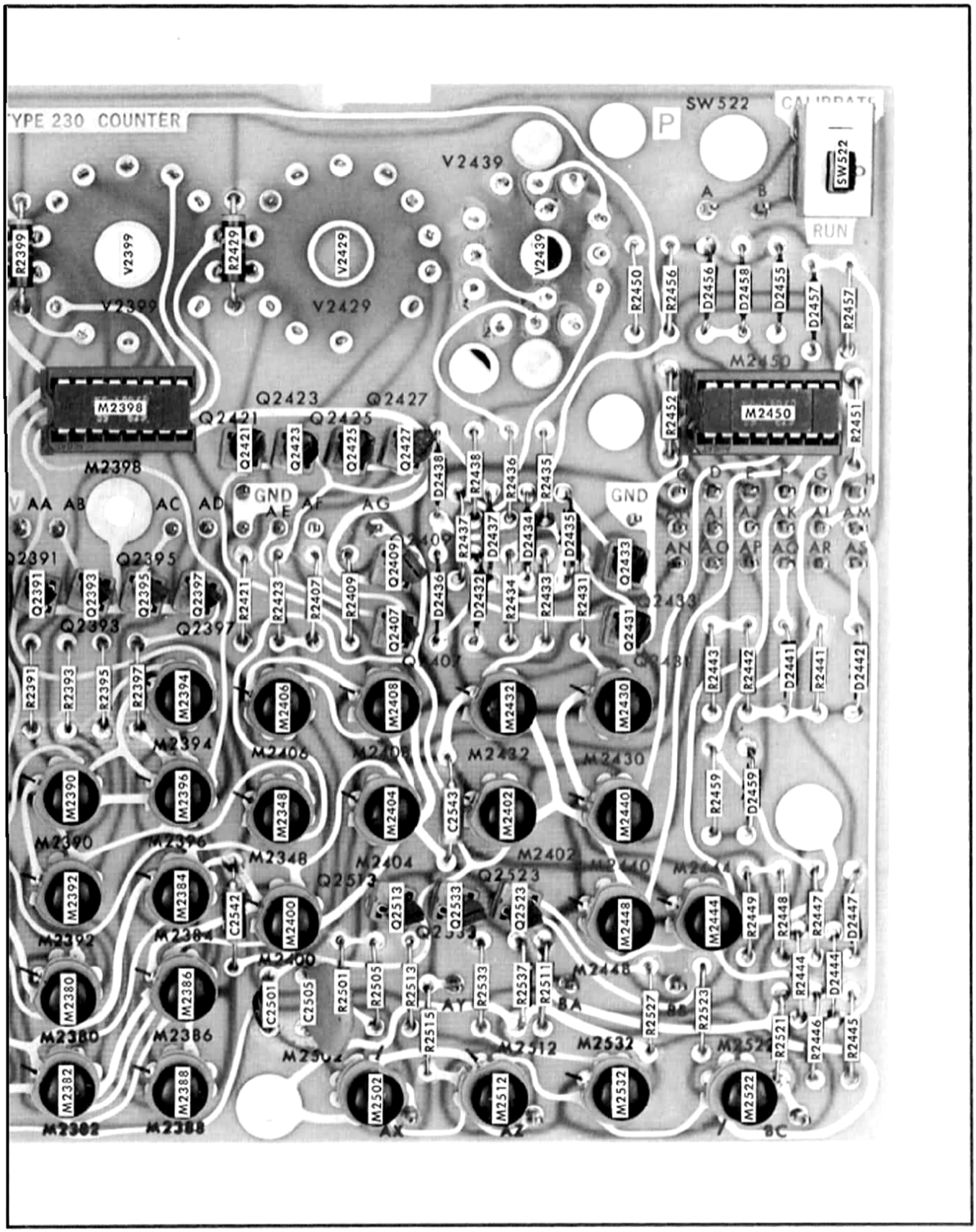

TYPE 230 COUNTER
SW522
CALIBRATE
RUN
P
V2439
V2429
V2399
M2398
M2450
Q2421
Q2423
Q2425
Q2427
Q2391
Q2393
Q2395
Q2397
Q2407
Q2431
Q2433
Q2513
Q2523
GND
M2394
M2406
M2408
M2432
M2430
M2390
M2396
M2348
M2404
M2402
M2440
M2392
M2384
M2400
M2448
M2444
M2380
M2386
M2502
M2512
M2532
M2522
M2382
M2388

Fig. 5-208.

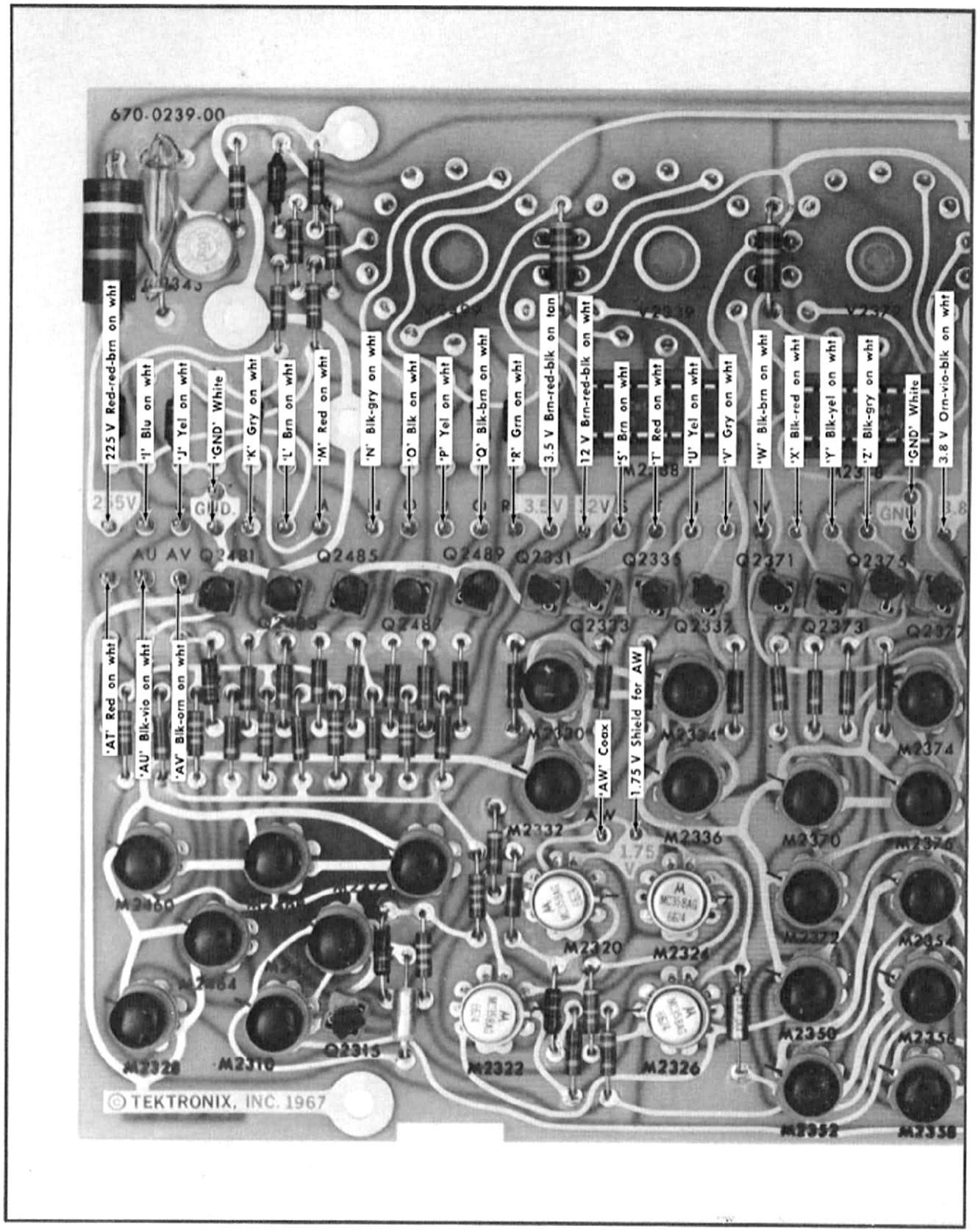
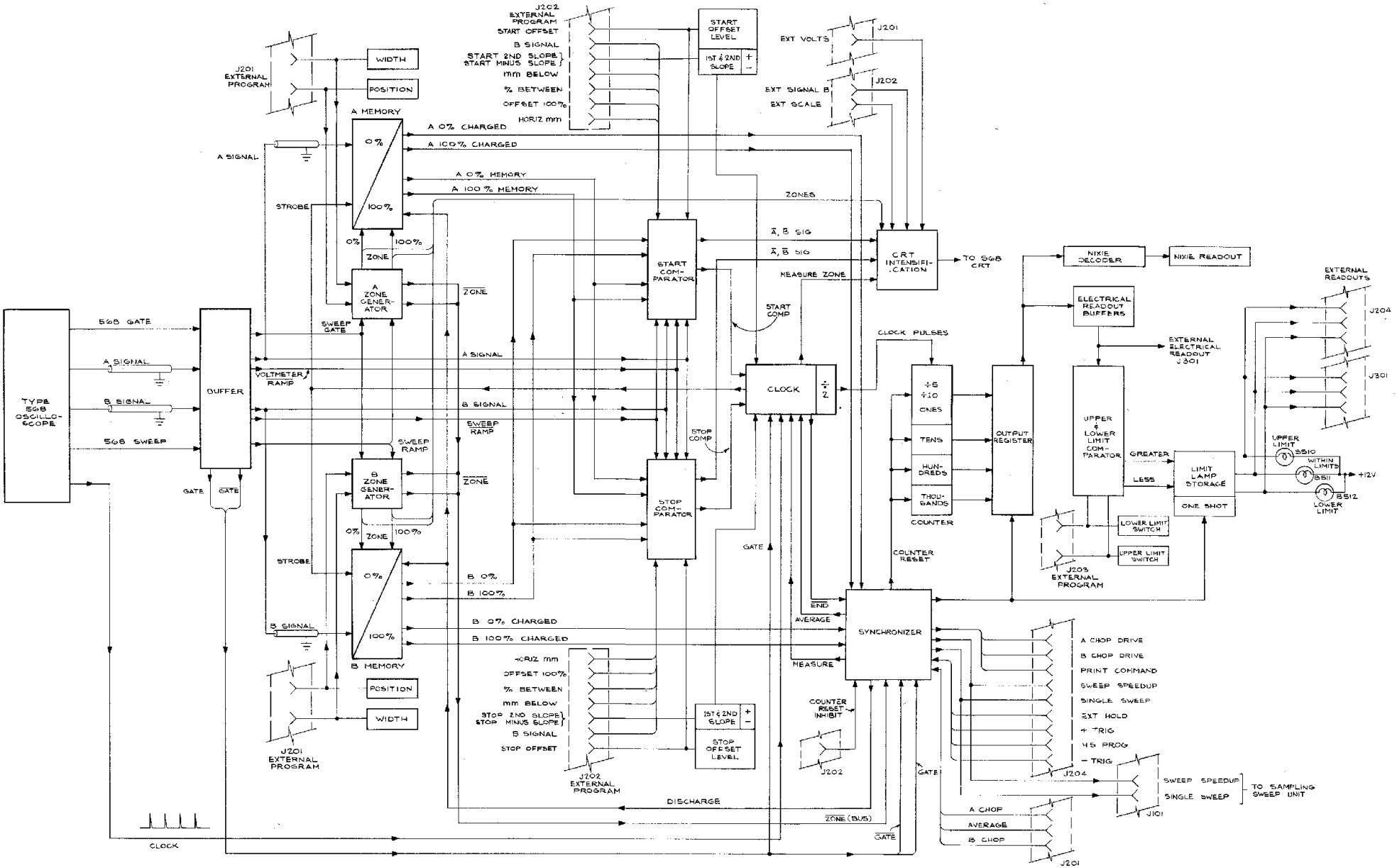


Fig. 5-21. 1A and B1 Pin connection locations on the Counter circuit card board.



TYPE 230 DIGITAL UNIT

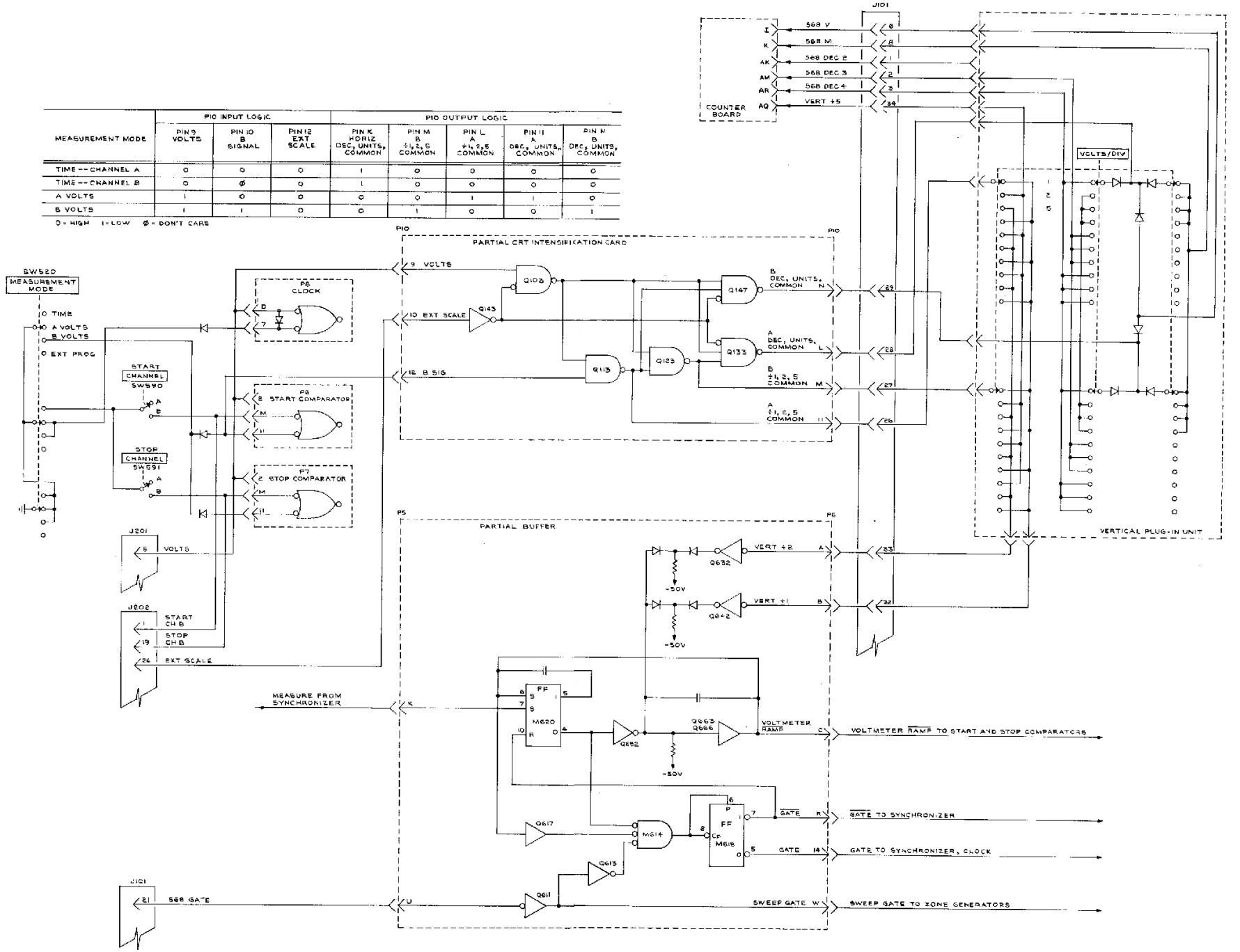
A3

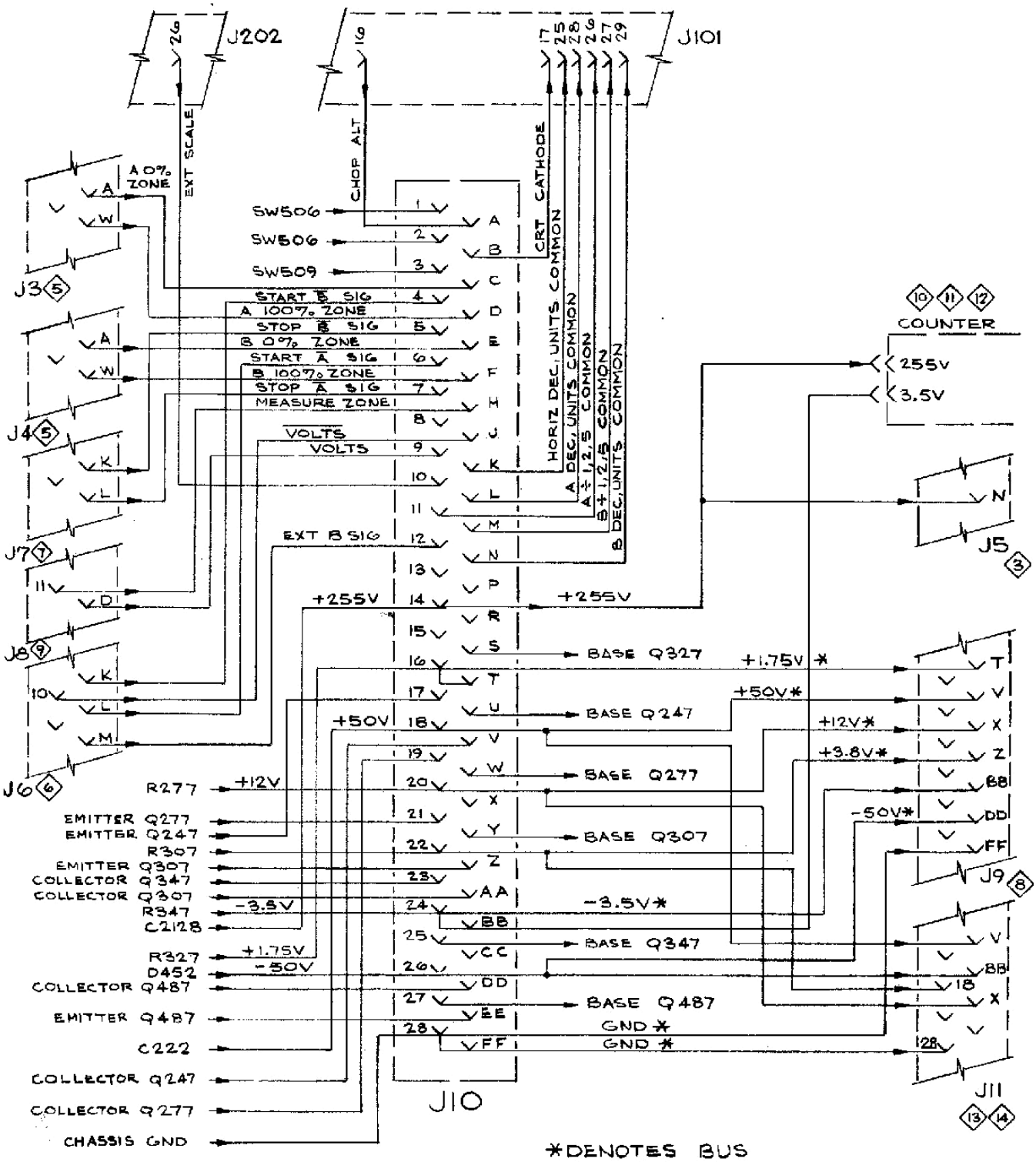
667

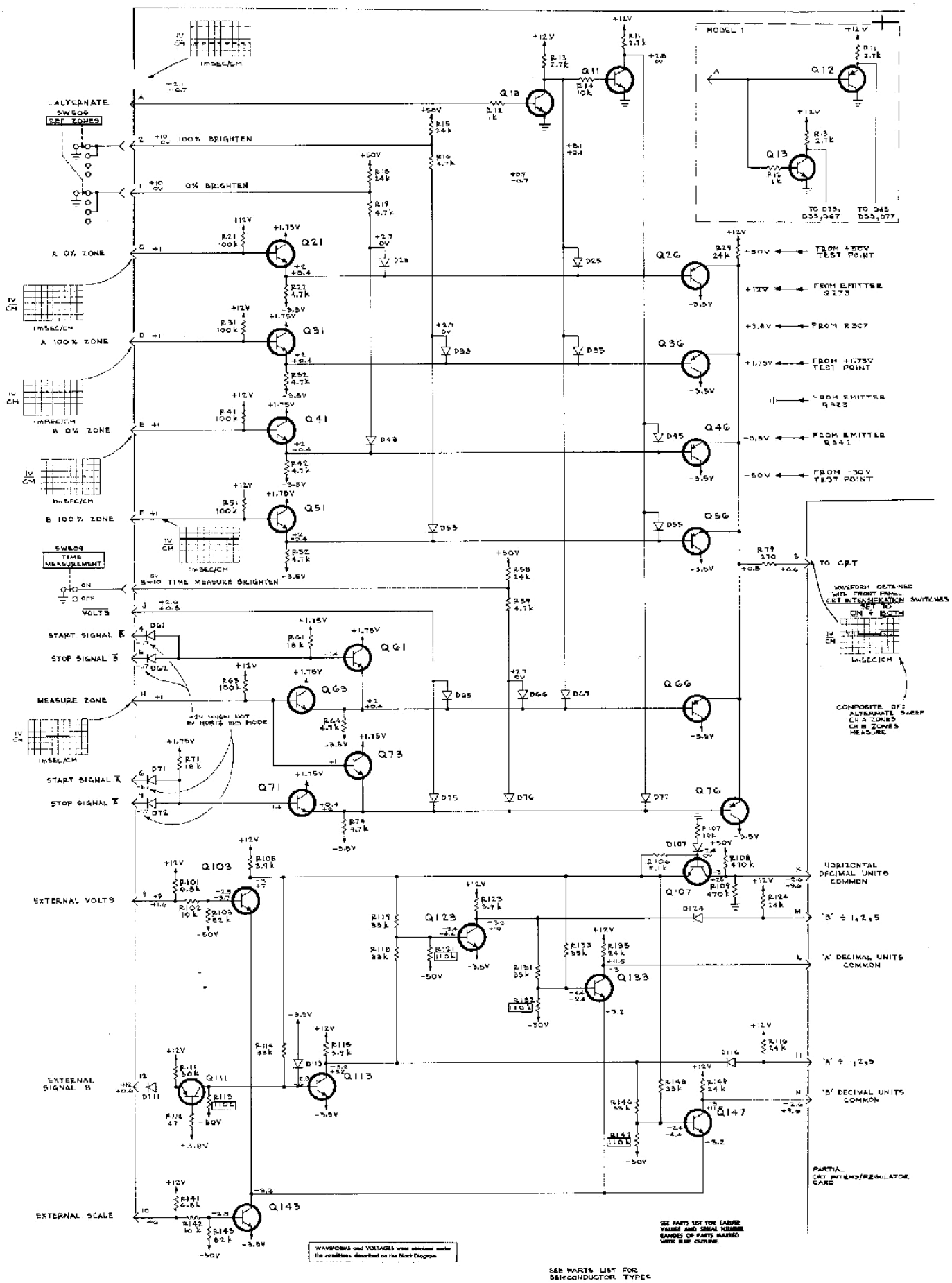
BLOCK DIAGRAM

MEASUREMENT MODE	P10 INPUT LOGIC			P10 OUTPUT LOGIC				
	PIN 9 VOLTS	PIN 10 B SIGNAL	PIN 12 EXT SCALE	PIN K HORIZ DEC, UNITS, COMMON	PIN M B ±1, 2, 5 COMMON	PIN L A ±1, 2, 5 COMMON	PIN H A DEC, UNITS, COMMON	PIN N B DEC, UNITS, COMMON
TIME -- CHANNEL A	0	0	0	1	0	0	0	0
TIME -- CHANNEL B	0	Ø	0	1	0	0	0	0
A VOLTS	1	Ø	0	0	0	1	1	0
B VOLTS	1	1	0	0	1	0	0	1

0 = HIGH 1 = LOW Ø = DON'T CARE



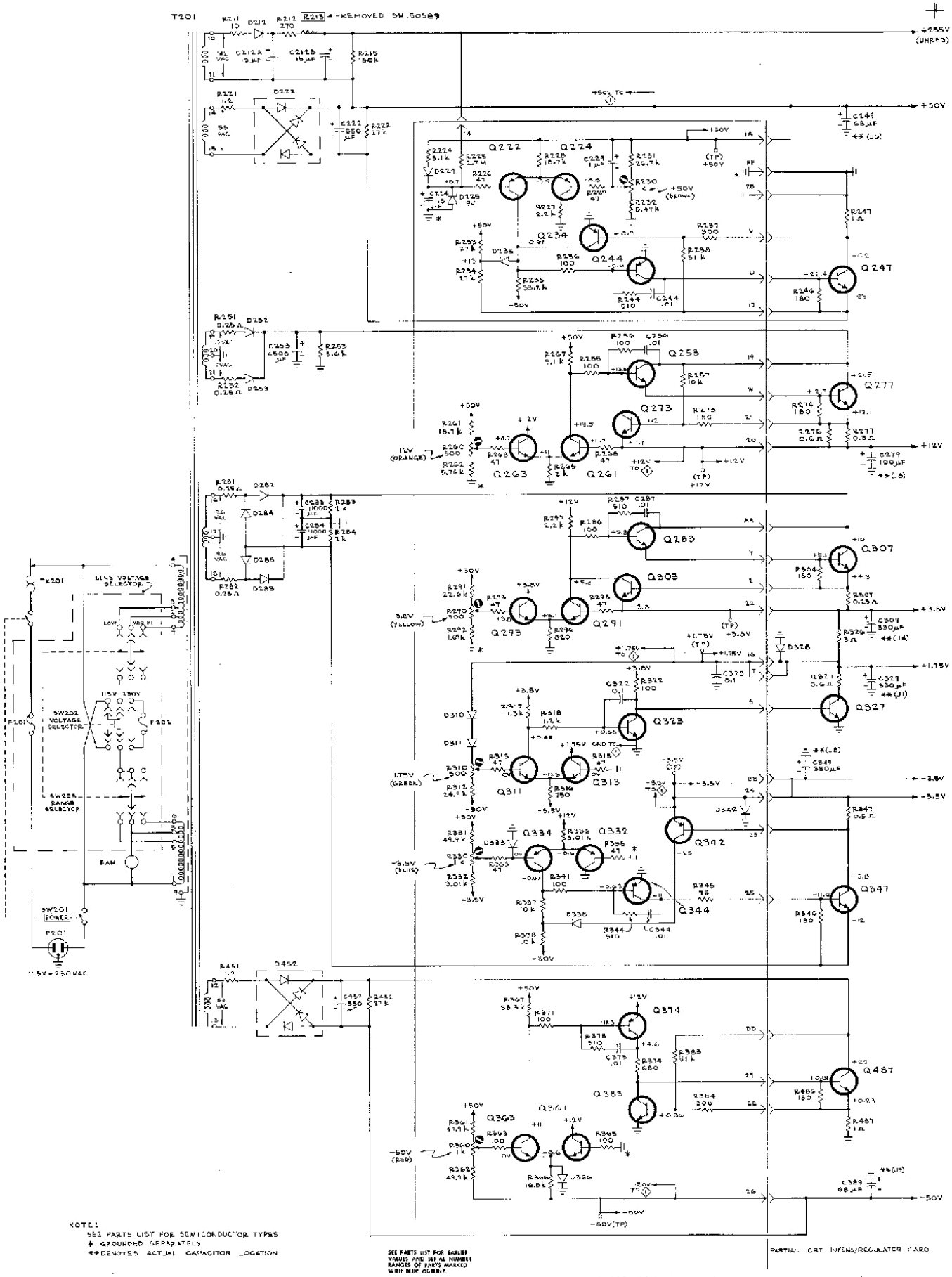

J202
J101
EXT SCALE
CHOP ALT
CRT CATHODE
HORIZ DEC. UNITS COMMON
A DEC. UNITS COMMON
A ÷ 1,2,5 COMMON
B ÷ 1,2,5 COMMON
B DEC. UNITS COMMON
A 0% ZONE
J3
J4
J6
J7
J8
SW506
SW506
SW509
START B SIG
A 100% ZONE
STOP B SIG
B 0% ZONE
START A SIG
B 100% ZONE
STOP A SIG
MEASURE ZONE
VOLTS
VOLTS
EXT B SIG
+255V
+255V
BASE Q327
BASE Q247
BASE Q277
BASE Q307
BASE Q347
BASE Q487
GND *
GND *
COUNTER
255V
3.5V
J5
J9
J11
+1.75V *
+50V*
+12V*
+3.8V*
-50V*
-3.5V*
R277
+12V
EMITTER Q277
EMITTER Q247
R307
EMITTER Q307
COLLECTOR Q347
COLLECTOR Q307
R347
C2128
-3.5V
R327
+1.75V
D452
-50V
COLLECTOR Q487
EMITTER Q487
C222
COLLECTOR Q247
COLLECTOR Q277
CHASSIS GND
J10
*DENOTES BUS



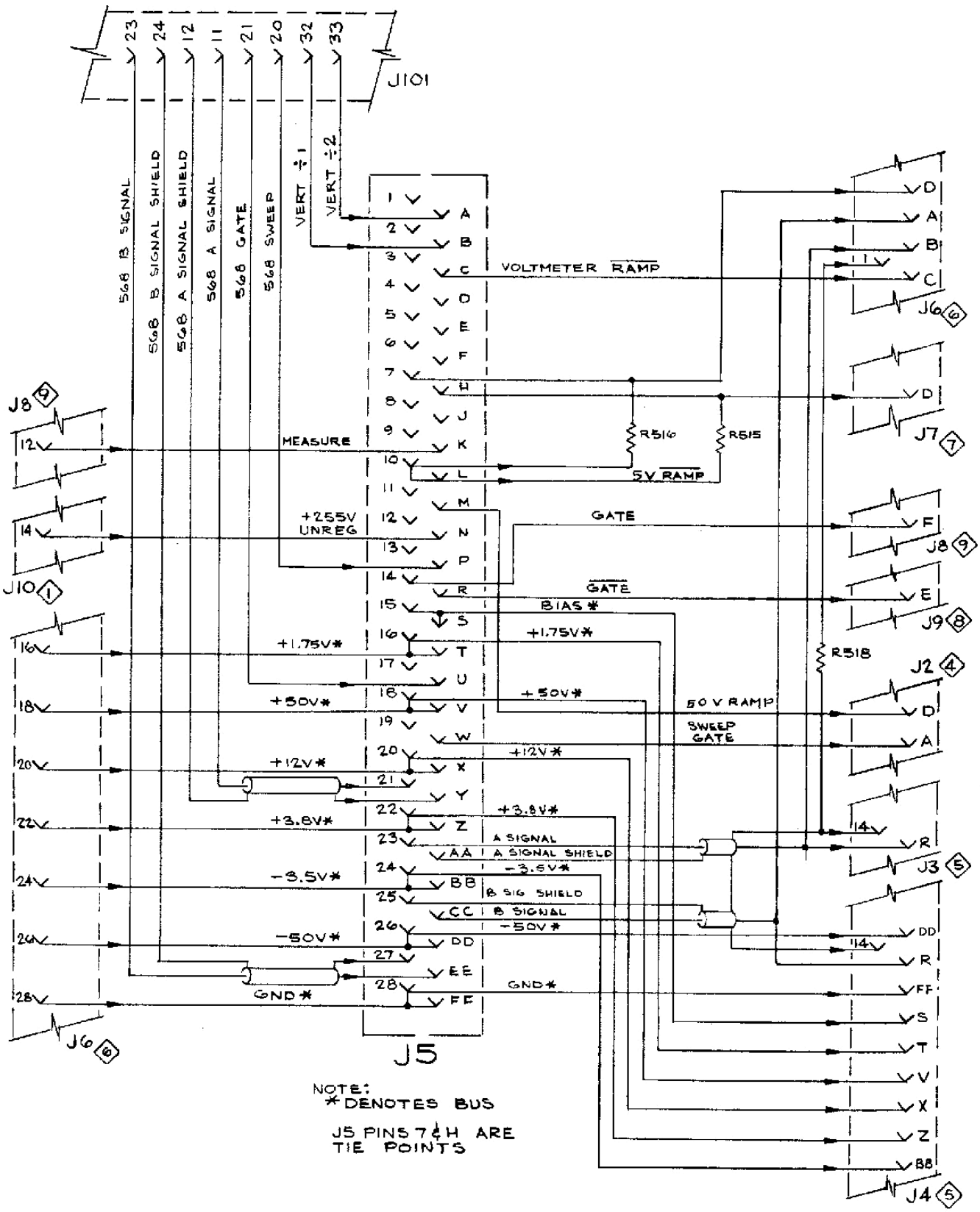
TYPE 230 DIGITAL

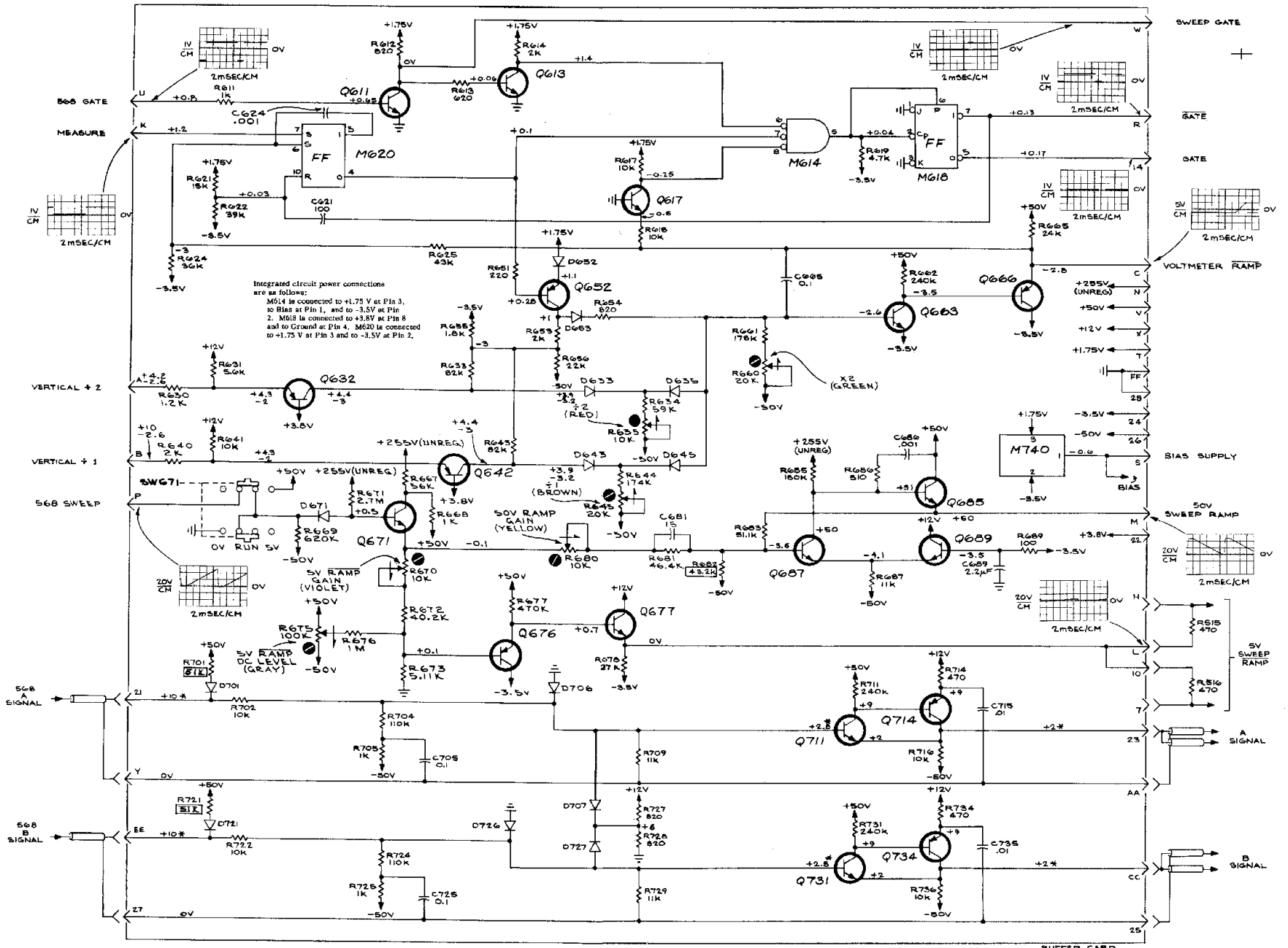
CRT INTENSIFICATION
PIC (PARTIAL)
SERIES G, MODEL 1-UP

869



NOTE:
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
* GROUNDED SEPARATELY
** DENOTES ACTUAL CAPACITOR LOCATION


J101
23
24
12
11
21
20
32
33
568 B SIGNAL
568 B SIGNAL SHIELD
568 A SIGNAL SHIELD
568 A SIGNAL
568 GATE
568 SWEEP
VERT ÷1
VERT ÷2
J5
A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
W
X
Y
Z
AA
BB
CC
DD
EE
FF
VOLTMETER RAMP
R516
R515
5V RAMP
MEASURE
+255V UNREG
GATE
GATE
BIAS *
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
50 V RAMP
SWEEP GATE
A SIGNAL
A SIGNAL SHIELD
B SIG SHIELD
B SIGNAL
R518
J8 9
J10 1
J6 6
J7 7
J9 8
J2 4
J3 5
J4 5
NOTE:
*DENOTES BUS
J5 PINS 7 & H ARE TIE POINTS

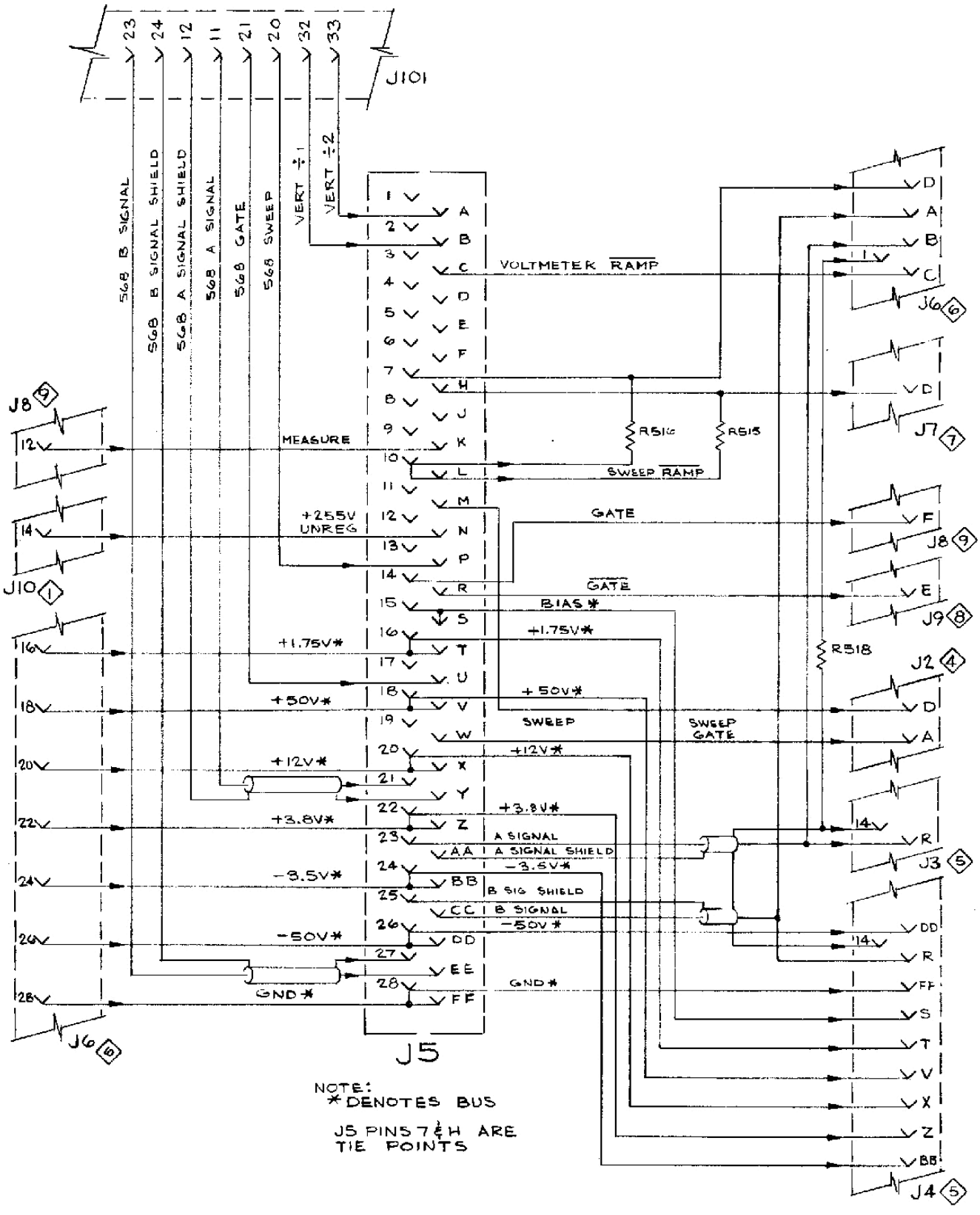


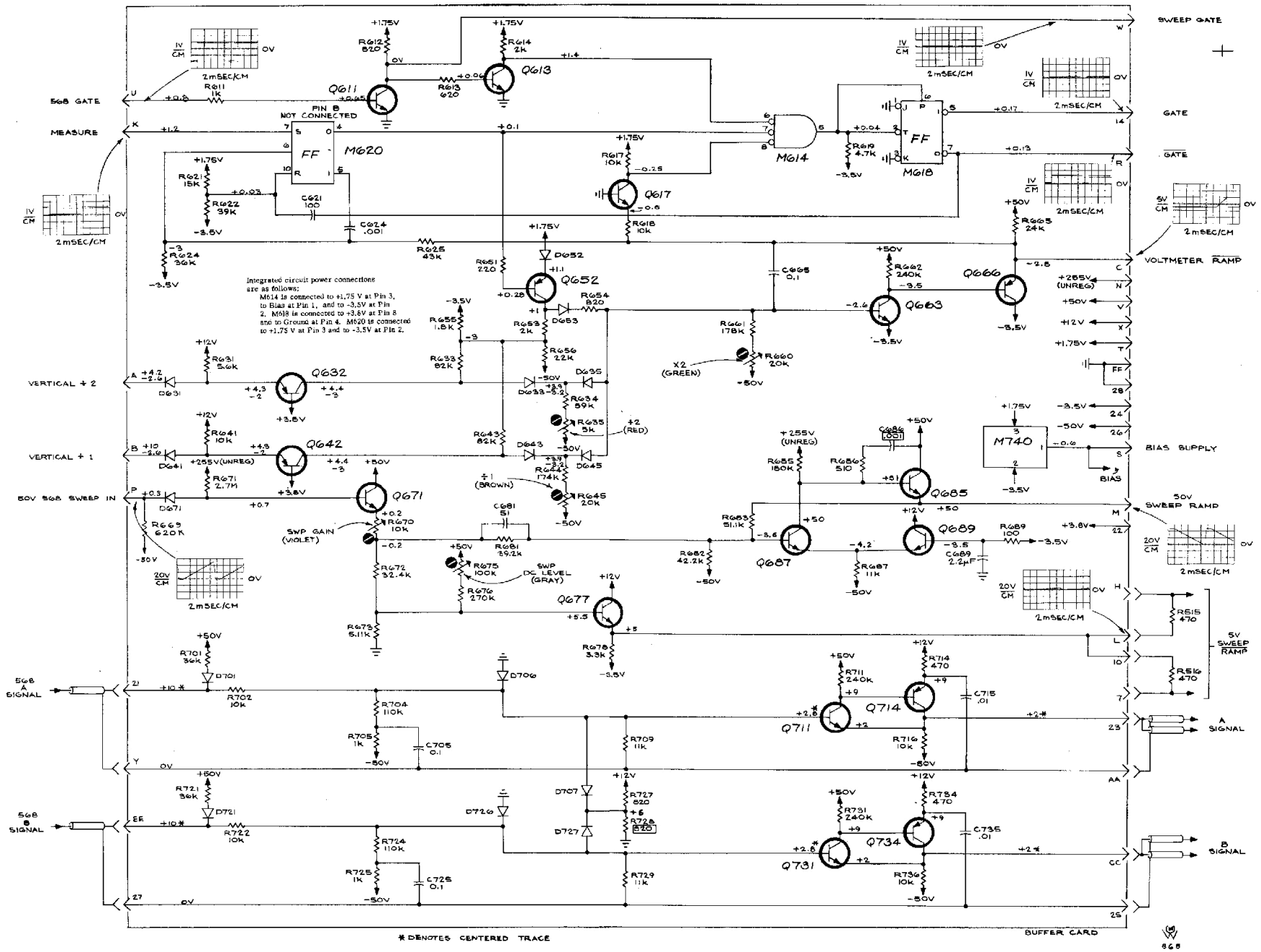
TYPE 230 DIGITAL UNIT

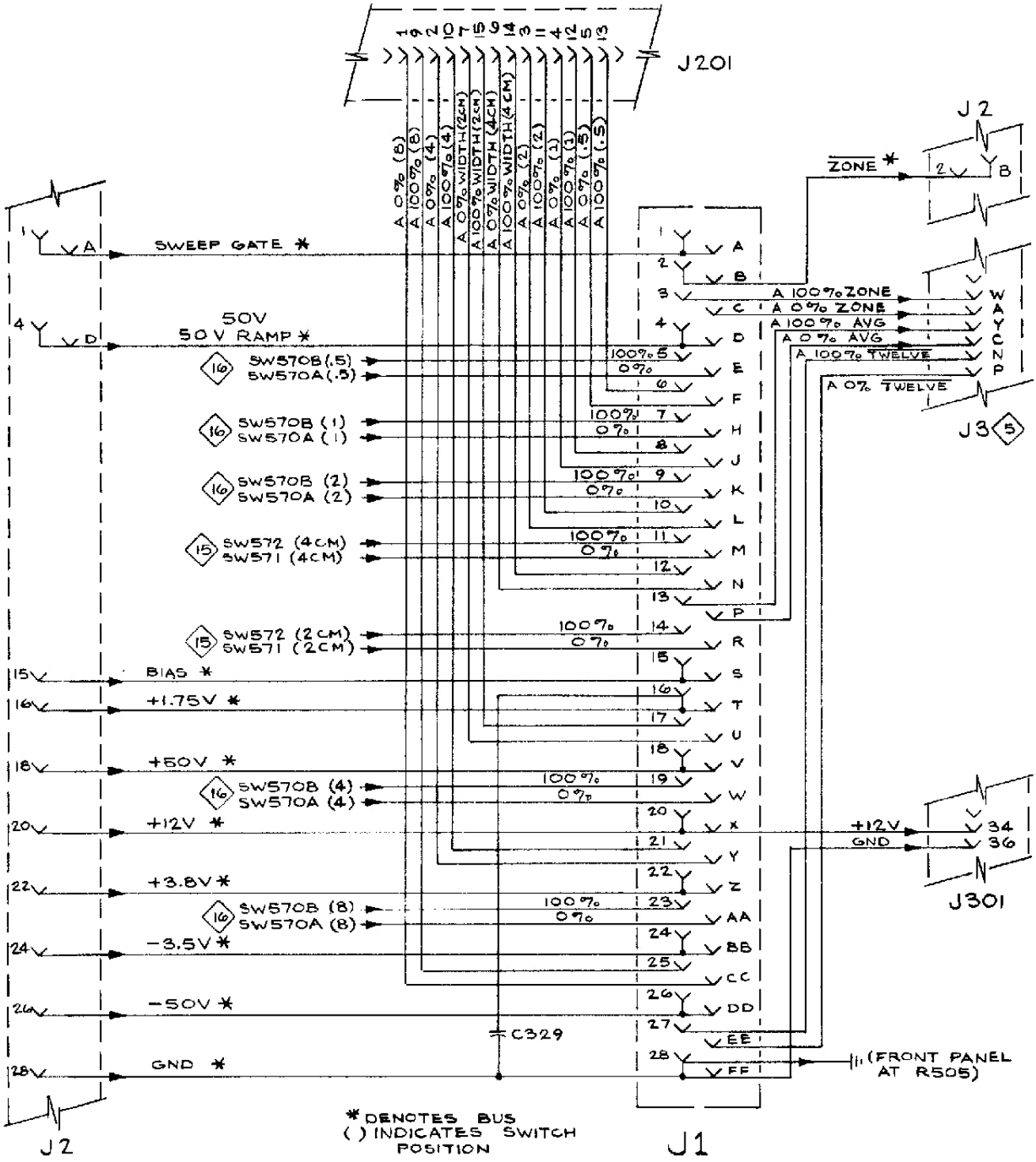
P5 – BUFFER 3

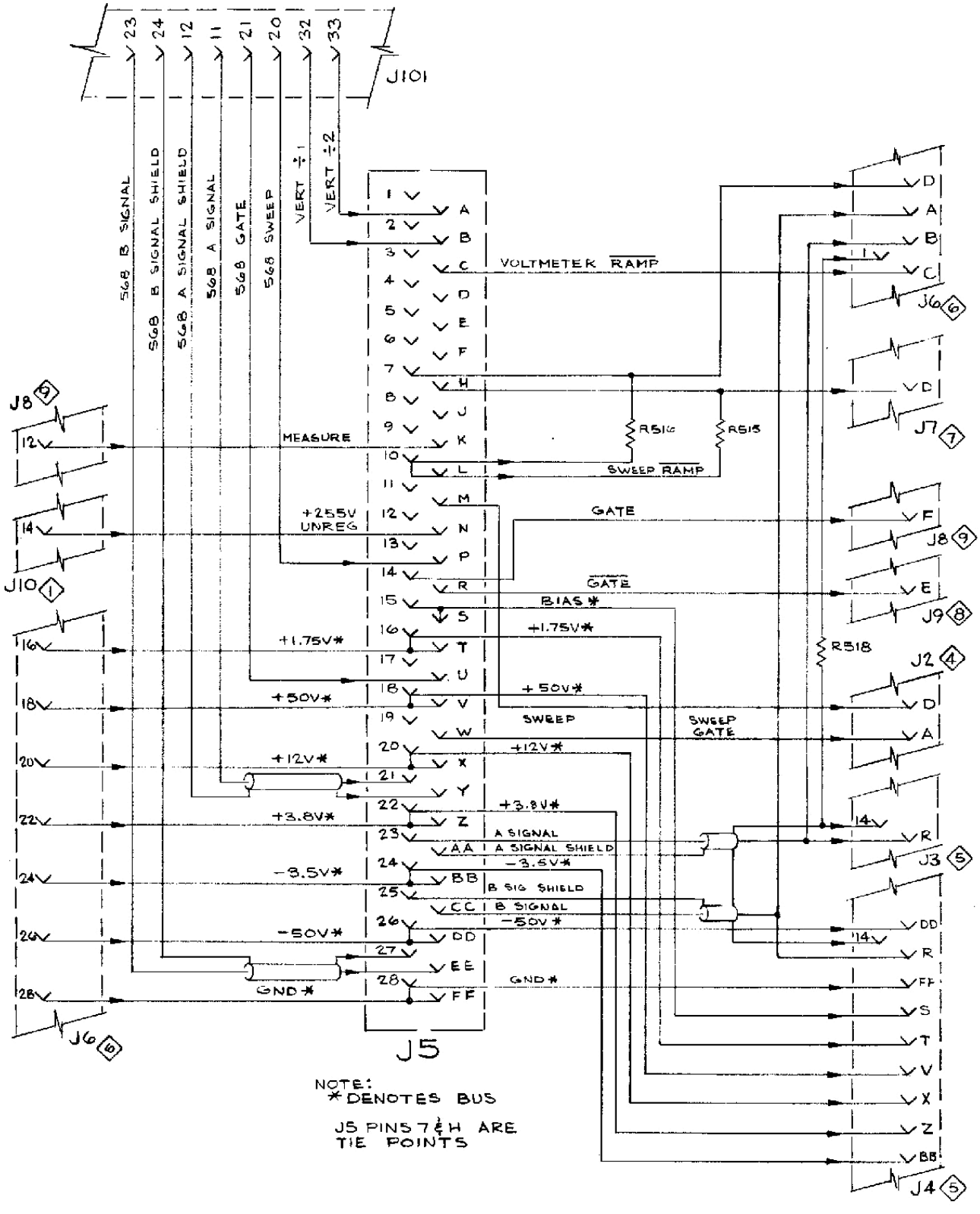
(SERIES C, MODEL 4 - UP)

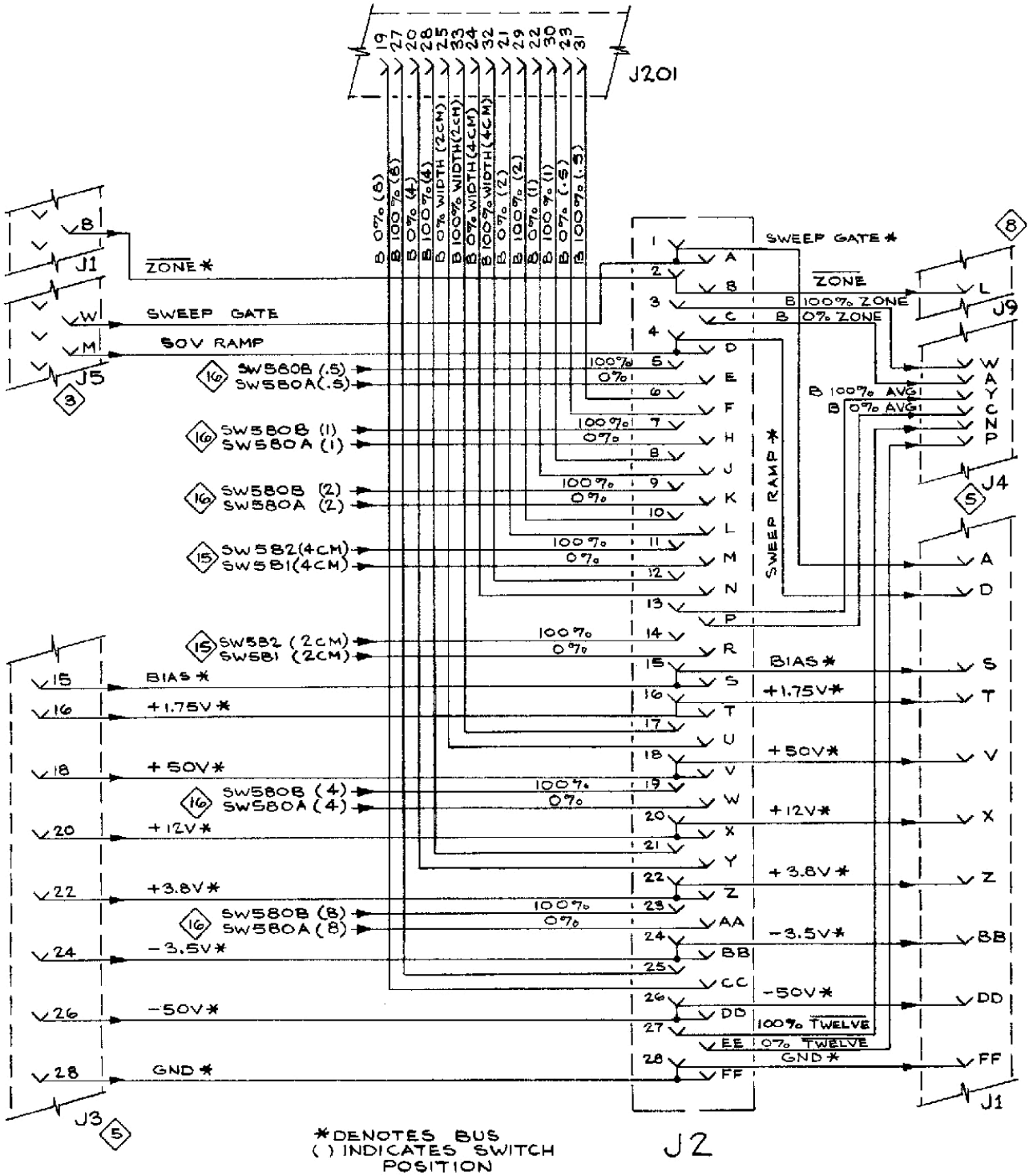
969


J101
23
24
12
11
21
20
32
33
568 B SIGNAL
568 B SIGNAL SHIELD
568 A SIGNAL SHIELD
568 A SIGNAL
568 GATE
568 SWEEP
VERT ÷1
VERT ÷2
VOLTMETER RAMP
MEASURE
+255V UNREG
GATE
BIAS *
+1.75V*
+50V*
SWEEP
+12V*
+3.8V*
A SIGNAL
A SIGNAL SHIELD
-3.5V*
B SIG SHIELD
B SIGNAL
-50V*
GND*
SWEEP RAMP
R516
R515
R518
SWEEP GATE
J8
J10
J6
J5
J7
J9
J2
J3
J4
NOTE:
*DENOTES BUS
J5 PINS 7 & H ARE TIE POINTS


SWEEP GATE
GATE
GATE
VOLTMETER RAMP
BIAS SUPPLY
BIAS
50V SWEEP RAMP
5V SWEEP RAMP
A SIGNAL
B SIGNAL
BUFFER CARD
568 GATE
MEASURE
VERTICAL + 2
VERTICAL + 1
50V 568 SWEEP IN
568 A SIGNAL
568 B SIGNAL
PIN B NOT CONNECTED
FF M620
M614
FF M618
M740
Q611
Q613
Q617
Q632
Q642
Q671
Q652
Q663
Q666
Q685
Q687
Q689
Q677
Q711
Q714
Q731
Q734
SWP GAIN (VIOLET)
SWP DC LEVEL (GRAY)
X2 (GREEN)
÷1 (BROWN)
+2 (RED)
Integrated circuit power connections are as follows;
M614 is connected to +1.75 V at Pin 3, to Bias at Pin 1, and to -3.5V at Pin 2. M618 is connected to +3.8V at Pin 8 and to Ground at Pin 4. M620 is connected to +1.75 V at Pin 3 and to -3.5V at Pin 2.
* DENOTES CENTERED TRACE
VOLTAGES and WAVEFORMS were obtained under conditions given on Block Diagram.
TYPE 230 DIGITAL UNIT
P5 — BUFFER 3
(SERIES C, MODELS 1, 2, 3)


J201
A 0% (8)
A 100% (8)
A 0% (4)
A 100% (4)
A 0% WIDTH (2CM)
A 100% WIDTH (2CM)
A 0% WIDTH (4CM)
A 100% WIDTH (4CM)
A 0% (2)
A 100% (2)
A 0% (1)
A 100% (1)
A 0% (.5)
A 100% (.5)
J2
SWEEP GATE *
50V
50 V RAMP *
SW570B (.5)
SW570A (.5)
SW570B (1)
SW570A (1)
SW570B (2)
SW570A (2)
SW572 (4CM)
SW571 (4CM)
SW572 (2CM)
SW571 (2CM)
BIAS *
+1.75V *
+50V *
SW570B (4)
SW570A (4)
+12V *
+3.8V *
SW570B (8)
SW570A (8)
-3.5V *
-50V *
GND *
C329
100% 5
0%
100% 7
0%
100% 9
0%
100% 11
0%
100% 14
0%
100% 19
0%
100% 23
0%
J1
ZONE *
J2
A 100% ZONE
A 0% ZONE
A 100% AVG
A 0% AVG
A 100% TWELVE
A 0% TWELVE
J3
+12V
GND
J301
(FRONT PANEL AT R505)
* DENOTES BUS
( ) INDICATES SWITCH POSITION


J101
23
24
12
11
21
20
32
33
568 B SIGNAL
568 B SIGNAL SHIELD
568 A SIGNAL SHIELD
568 A SIGNAL
568 GATE
568 SWEEP
VERT ÷1
VERT ÷2
VOLTMETER RAMP
MEASURE
+255V UNREG
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
GATE
BIAS*
SWEEP
SWEEP GATE
SWEEP RAMP
A SIGNAL
A SIGNAL SHIELD
B SIG SHIELD
B SIGNAL
R518
J5
J10
J8
J6
J7
J9
J2
J3
J4
NOTE:
*DENOTES BUS
J5 PINS 7 & H ARE TIE POINTS


J201
19 27 20 28 25 33 24 32 21 29 22 30 23 31
B 0% (.5)
B 100% (.5)
B 0% (1)
B 100% (1)
B 0% (2)
B 100% (2)
B 0% WIDTH (4CM)
B 100% WIDTH (4CM)
B 0% WIDTH (2CM)
B 100% WIDTH (2CM)
B 0% (4)
B 100% (4)
B 0% (8)
B 100% (8)
J1
J5
J3
J4
J9
J2
ZONE *
SWEEP GATE
50V RAMP
SW580B (.5)
SW580A (.5)
SW580B (1)
SW580A (1)
SW580B (2)
SW580A (2)
SW582 (4CM)
SW581 (4CM)
SW582 (2CM)
SW581 (2CM)
SW580B (4)
SW580A (4)
SW580B (8)
SW580A (8)
100%
0%
BIAS *
+1.75V *
+50V *
+12V *
+3.8V *
-3.5V *
-50V *
GND *
SWEEP GATE *
SWEEP RAMP *
ZONE
B 100% ZONE
B 0% ZONE
B 100% AVG1
B 0% AVG1
100% TWELVE
0% TWELVE
*DENOTES BUS
( ) INDICATES SWITCH POSITION

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

TEXT CORRECTION

Section 6 Performance Check

Page 6-1 EQUIPMENT REQUIRED

REPLACE: items 1, 2 and 3 with the following:

1. Type 568 oscilloscope with sampling and sampling sweep units, such as Type 3S5 (with two Sampling Heads) and Type 3T5.

2. Interconnecting cable, Tektronix Part Number 012-0119-01 (Included as standard accessory with the Type 230).

Page 6-1 Control Settings

ADD: the following controls after SLOPE:

TIME MEASUREMENT STOP POINT	
CHANNEL	A
LEVEL	HORIZ mm FROM SWP START
Offset dials	1 and 0

Page 6-2

REPLACE: the control settings in column 1 with the following:

Sampling Sweep Unit	
Samples/Sweep	1000
Time/Div	(100 ns)
Decade	7
Multiplier	1
Delay	1000
Program Selector	Int
Trigger	
Sensitivity	fully cw
Recovery Time	fully cw
Mode	+, Int
Horiz Pos	Centered
Sampling Unit	
Mode	Ch A
Channels A and B	
Units/Div	100
Cal/Variable	Cal
Invert	Pushed In (normal)
DC Offset Dials	0-0
Normal/Smooth	Normal

TEXT CORRECTION

Section 1 Characteristics

Page 1-3

ADD: the following information to the end of the present text:

Characteristic		Performance Requirement	
J 101 From Type 568		True	False
Pin	Indicates		
1	Decimal 2	≤ +2 V, ≤ 2.8 mA	≥ +6 V, ≥ 0.0 mA
2	Decimal 3	≤ +2 V, ≤ 3 mA	≥ +6 V, ≥ -0.15 mA
3	Decimal 4		
4	Not Used		
5	Not Used		
6	Letter V	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≥ -0.15 mA
7	Letter m		
9	Letter μ		
10	Letter n	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≥ -0.15 mA
11	Ch A Signal In	1 V/div ±3% at +10 V center screen. Z_{in} ≥ 10 kΩ	
12	A Signal Shield		
13	not used		
14	3T4 Speed up	≥ +1 V at ≤ 2.5 mA	≥ -11 V at 68 kΩ ±10%
15	3T4 Single Sweep		
16	Chop/Alternate	≥ -1.0 V low to ≥ 1.0 V high, ≤ 1 kΩ	
17	CRT Intensity(output)	≥ +0.8 V at 270 Ω ±10%	≤ 0.2 V at 270 Ω ±10%
18	Ground		
19	Ground		
20	Sweep	5 V/div ±3% starting at 0 V ±0.5 V	
21	Sweep Gate	≥ +1.0 V at 3 kΩ ±5%	≥ -0.5 V at 3 kΩ ±5%
22	10 MHz	≥ -9.3 V, 0.17 mA	≤ -3.1 V, 0.06 mA
23	Ch B Signal In	1 V/div ±3% +10 V center screen. Z_{in} ≥ 10 kΩ	
24	B Signal Shield		
25	Horiz Decimal Units, Common	≥ -.25 V at ≤ 5 mA	≥ +23 V at 235 kΩ ±10%
26	A ÷ 1,2,5	≥ -2.5 V at ≤ 5 mA	+12 V at 24 kΩ ±10%
27	B ÷ 1,2,5		
28	A Decimal Units Common	≥ -3.0 V at ≤ 5 mA	+12 V at 24 kΩ ±10%
29	B Decimal Units Common		
30	Horiz ÷ 2	≤ +2 V, ≤ 2.4 mA	≥ +6 V, ≤ 0.5 mA
31	Horiz ÷ 5	≤ +2 V, ≤ 0.4 mA	≥ +6 V, 0.0 mA
32	Vert ÷ 1	≤ +2 V, ≤ 2.4 mA	≥ +6 V, 0.0 mA
33	Vert ÷ 2	≤ +2 V, ≤ 1.4 mA	≥ +6 V, 0.0 mA
34	Vert ÷ 5	≤ +2 V, ≤ 5.5 mA	≥ +6 V, 0.0 mA
35	Sweep Clock Risetime/Falltime Frequency Pulse Width Amplitude	 ≤ 150 ns ≤ 1 MHz 0.7 μs to 1.3 μs ≥ -0.5 V to +1 V at ≥ 0.5 mA	 ≥ 0.5 mA
36	Clock Shield		

Characteristic		Performance Requirement	
J 201 Reference Zone Program			
		True	False
Pin	Program		
1	A 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
2	A 0% Position 4		
3	A 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
4	A 0% Position 1		
5	A 0% Position 0.5		
6	A 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
7	A 0% Width 2		
8	External Volts	≤ +2 V, ≤ 6 mA	≥ +6 V, ≤ 2.9 mA
9	A 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
10	A 100% Position 4		
11	A 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
12	A 100% Position 1		
13	A 100% Position 0.5		
14	A 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
15	A 100% Width 2		
16	A Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.1 mA
17	Program Common		
18	Program Common		
19	B 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
20	B 0% Position 4		
21	B 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
22	B 0% Position 1		
23	B 0% Position 0.5		
24	B 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
25	B 0% Width 2		
26	Measurement Average	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≥ -2.4 mA
27	B 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
28	B 100% Position 4		
29	B 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
30	B 100% Position 1		
31	B 100% Position 0.5		
32	B 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
33	B 100% Width 2		
34	B Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.03 mA
35	Program Common	≤ +24 V, ≤ 500 mA	
36	Program Common		

Characteristic		Performance Requirement	
J 201 Reference Zone Program			
		True	False
Pin	Program		
1	A 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
2	A 0% Position 4		
3	A 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
4	A 0% Position 1		
5	A 0% Position 0.5		
6	A 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
7	A 0% Width 2		
8	External Volts	≤ +2 V, ≤ 6 mA	≥ +6 V, ≤ 2.9 mA
9	A 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
10	A 100% Position 4		
11	A 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
12	A 100% Position 1		
13	A 100% Position 0.5		
14	A 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
15	A 100% Width 2		
16	A Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.1 mA
17	Program Common		
18	Program Common		
19	B 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
20	B 0% Position 4		
21	B 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
22	B 0% Position 1		
23	B 0% Position 0.5		
24	B 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
25	B 0% Width 2		
26	Measurement Average	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≥ -2.4 mA
27	B 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
28	B 100% Position 4		
29	B 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
30	B 100% Position 1		
31	B 100% Position 0.5		
32	B 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
33	B 100% Width 2		
34	B Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.03 mA
35	Program Common	≤ +24 V, ≤ 500 mA	
36	Program Common		

Characteristic		Performance Requirement	
J 202 Comparator Program			
Pin	Program	True	False
1	Start B Channel	≤ +2 V, ≤ 7.1 mA	≥ +6 V, ≤ 2.9 mA
2	Start HORIZ mm	≤ +2 V, ≤ 4 mA	≥ +6 V, ≤ 2.7 mA
3	Start Percent Between	≤ +2 V, ≤ 5.9 mA	≥ +6 V, ≤ 2.9 mA
4	Start mm BELOW Reference Zone	≤ +2 V, ≤ 2.9 mA	≥ +6 V, ≤ 3.7 mA
5	Start Offset from 100%	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≤ 2.9 mA
6	Start Minus Slope	≤ +2 V, ≤ 1.4 mA	≥ +6 V, ≤ 0.8 mA
7	Start Second Slope		
8	Counter Reset Inhibit	≤ +2 V, ≤ 2.5 mA	≥ +6 V, ≥ -0.5 mA
9	Start Offset 80	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
10	Start Offset 40		
11	Start Offset 20		
12	Start Offset 10		
13	Start Offset 8	≤ +2 V, ≤ 3.7 mA	≥ +6 V, 0.0 mA
14	Start Offset 4	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
15	Start Offset 2		
16	Start Offset 1		
17	Program Common		
18	Program Common		
19	Stop B Channel	≤ +2 V, ≤ 7.1 mA	≥ +6 V, ≤ 2.9 mA
20	Stop HORIZ mm	≤ +2 V, ≤ 4.0 mA	≥ +6 V, ≤ 2.7 mA
21	Stop Percent Between	≤ +2 V, ≤ 5.9 mA	≥ +6 V, ≤ 2.9 mA
22	Stop mm BELOW Reference Zone	≤ +2 V, ≤ 4.9 mA	≥ +6 V, ≤ 3.7 mA
23	Stop Offset from 100%	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≤ 2.9 mA
24	Stop Minus Slope	≤ +2 V, ≤ 1.4 mA	≥ +6 V, ≤ 0.8 mA
25	Stop Second Slope		
26	External Scale	≤ +2 V, ≤ 1.4 mA	≥ +6 V, ≤ 0.1 mA
27	Stop Offset 80	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
28	Stop Offset 40		
29	Stop Offset 20		
30	Stop Offset 10		
31	Stop Offset 8	≤ +2 V, ≤ 3.7 mA	≥ +6V, 0.0 mA
32	Stop Offset 4	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
33	Stop Offset 2		
34	Stop Offset 1		
35	Program Common		
36	Program Common		

Characteristic		Performance Requirement	
J 203 Limit Program			
		True	False
Pin	Program		
1	External ÷ 2	≤ +2 V, ≤ 2.4 mA	≥ +6 V, ≤ 0.5 mA
2	Upper Minus	≤ +2 V, ≤ 1.9 mA	≥ +6 V, 0.0 mA
4	Upper 1000		
6	Upper 400		
8	Upper 100		
10	Upper 40		
12	Upper 10		
14	Upper 4		
16	Upper 1		
3	Upper 2000	≤ +2 V, ≤ 1.2 mA	≥ +6 V, ≤ 0.5 mA
5	Upper 800		
7	Upper 200		
9	Upper 80		
11	Upper 20		
13	Upper 8		
15	Upper 2		
17	Program Common		
18	Program Common		
19	Ext ÷ 5	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≥ -0.4 mA
20	Lower Minus	≤ +2 V, ≤ 1.0 mA	≥ +6 V, 0.0 mA
21	Lower 2000	≤ +2 V, ≤ 1.2 mA	≥ +6 V, ≤ 0.5 mA
23	Lower 800		
25	Lower 200		
27	Lower 80		
29	Lower 20		
31	Lower 8		
33	Lower 2		
22	Lower 1000	≤ +2 V, ≤ 1.9 mA	≥ +6 V, 0.0 mA
24	Lower 400		
26	Lower 100		
28	Lower 40		
30	Lower 10		
32	Lower 4	≤ +2 V, ≤ 1.9 mA	≥ +6 V, 0.0 mA
34	Lower 1		
35	Lower 1		
36	Program Common		

Characteristic		Performance Requirement	
J 204 Miscillaneous Inputs and Outputs			
		True	False
Pin	Indicates		
1	Print Command	≤ +2 V, at ≤ 20 mA	+12 V at 3 kΩ ±10%
2	External Hold		
	Hold	≤ +2 V, ≤ 6 mA	
	Release	≥ +7 V, ≤ 2.4 mA	
3	Red Light	≤ +2 V at ≤ 20 mA	≥ +10 V at ≤ 100 Ω
4	Green Light		
5	Yellow Light		
6	+ Trigger		
	Risetime	≤1 µs	
	Amplitude	≥ 3 V (positive step)	
7	- Trigger		
	Risetime	≤ 1 µs	
	Amplitude	≥ 3 V (negative step)	
8	Program 3T4 H.S.	≤ +2 V, ≤ 4.4 mA	≥ +6 V, ≥ -1.7 mA
9	3T4 Speed Up	≥ +1 V, ≤ 2.5 mA	≥ -11 V at 68 kΩ ±10%
10	3T4 Single Sweep		
11	A Chopper Drive	≤ +1 V, ≤ 20 mA	+12 V at 12 kΩ ±10%
12	B Chopper Drive		
13	Ext Decimal 2	≤ +2 V, ≤ 2.8 mA	≥ +6 V, 0.0 mA
14	Ext Decimal 3	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≤ 0.05 mA
15	Ext Decimal 4		
16	not used		
17	Ext Letter V	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≥ -0.14 mA
18	Ext Letter s		
19	Ext Letter m		
20	Ext Letter µ		
21	Ext Letter n		
22	+50 V	±1% at ≤ 25 mA	
23	+12 V	±1% at ≤ 350 mA	
24	+3.8 V	±1% at ≤ 200 mA	
25	-50 V	±1% at ≤ 25 mA	
26	not used		
27	not used		
28	not used		
29	not used		
30	not used		
31	not used		
32	not used		
33	not used		
34	not used		
35	Program Common		
36	Ground		

Characteristic		Performance Requirement	
J 301 Readout Connector		True	False
Pin	Indicates		
1	+	≤ 2 V at ≤ 20 mA	+12 V at 2.4 kΩ ±10%
2	-		
3	2000	≤ +2 V, ≤ +20 mA	≥ +12 V at ≤ 1 mA
4	1000		
5	800		
6	400		
7	200		
8	100		
9	80		
10	40		
11	20		
12	10		
13	8		
14	4		
15	2	≤ +2 V, ≤ +20 mA	≥ +12 V at ≤ 1 mA
16	1		
17	not used		
18	not used		
19	X 10^{-1}	≤ +5 V at ≤ 1 mA	+12 V at 120 kΩ ±15%
20	X 10^{-2}		
21	X 10^{-4}		
22	V	≤ 2 V at ≤ 20 mA	+12 V at 2.4 kΩ ±10%
23	S		
24	m		
25	μ		
26	n		
27	Red	≤ 2 V at ≤ 20 mA	≥ +10 V at ≤ 100 Ω
28	Green		
29	Yellow		
30	External Hold	Hold ≤ +2 V at ≤ 6 mA, Release ≥ +7 V at ≤ 2.4 mA	
31	Print Command	≤ 2 V at ≤ 20 mA	+12 V at 6.2 kΩ ±5%
32	not used		
33	+12 V Out	±1% at ≤ 350 mA	Ripple ≤ 5 mV
34	not used		
35	not used		
36	Ground		

TYPE 230/R230 TENT SN B190910

ELECTRICAL PARTS LIST CORRECTION

CHANGE TO:

Q2421	151-0292-00	Silicon	Nixie Driver
Q2423	151-0292-00	Silicon	Nixie Driver
Q2425	151-0292-00	Silicon	Nixie Driver
Q2427	151-0292-00	Silicon	Nixie Driver
Q2431	151-0292-00	Silicon	Nixie Driver
Q2433	151-0292-00	Silicon	Nixie Driver
Q2481	151-0292-00	Silicon	Nixie Driver
Q2483	151-0292-00	Silicon	Nixie Driver
Q2485	151-0292-00	Silicon	Nixie Driver
Q2487	151-0292-00	Silicon	Nixie Driver
Q2489	151-0292-00	Silicon	Nixie Driver

TYPE 230/R230

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

SYNCHRONIZER CARD - Series F

CHANGE TO:

R1778	315-0753-00	75 kΩ	1/4 W	5%	Model 9-up

M15,856/1269

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

SYNCHRONIZER CARD Series F

CHANGE TO:

R1790	315-0103-00	10 kΩ	1/4 W	5%	Model 10-up