TEKTRONIX®

314 STORAGE OSCILLOSCOPE

SERVICE

INSTRUCTION MANUAL

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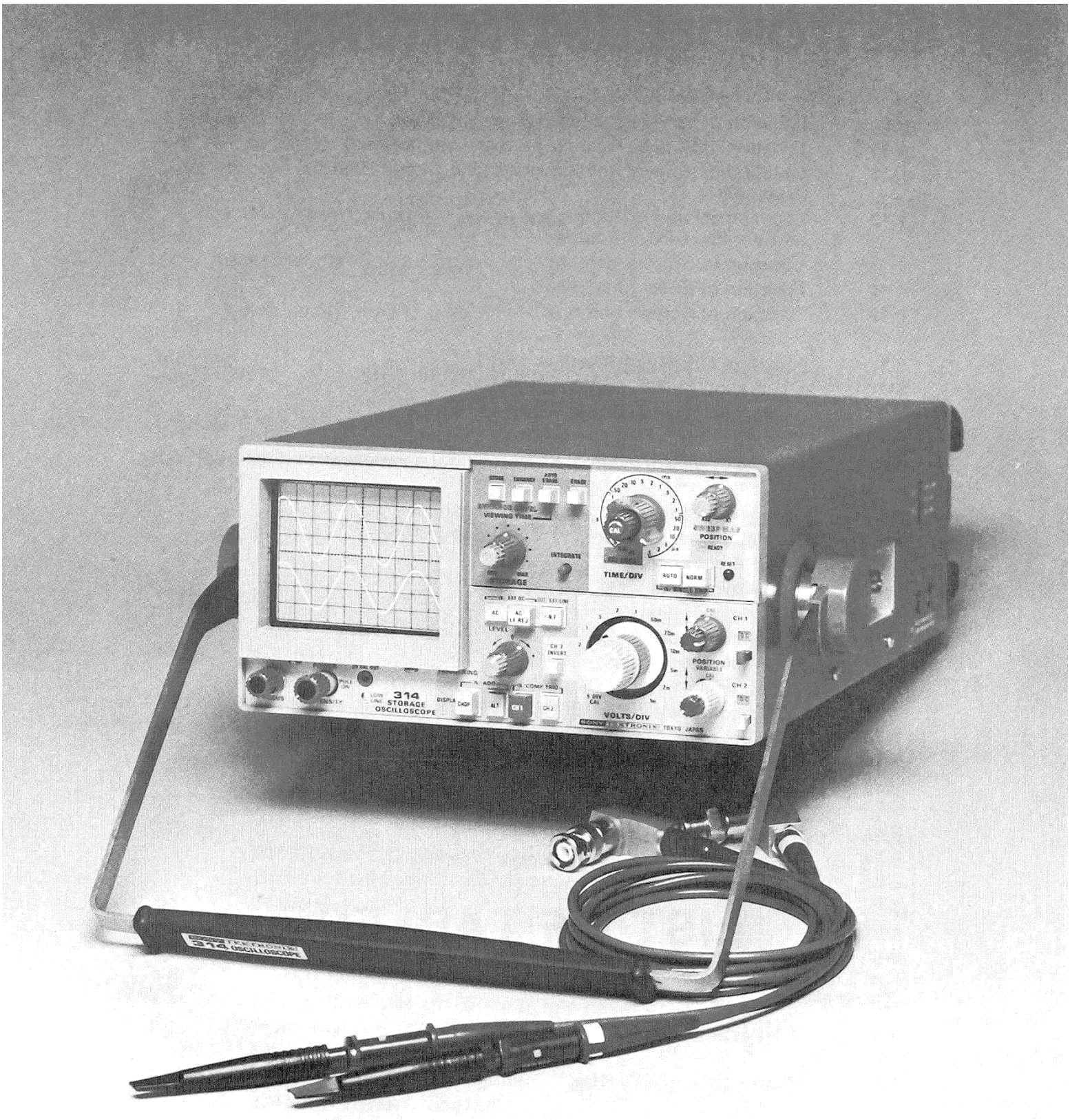
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

070-1824-00

First Printing MAR 1975


314
STORAGE
OSCILLOSCOPE
TIME/DIV
VOLTS/DIV
POSITION
VIEWING TIME
INTEGRATE
AUTO
NORM
READY
TEKTRONIX TOKYO JAPAN

1824-49

SPECIFICATION

The Sony-Tektronix 314 is a dual-channel, 10 megahertz, portable storage oscilloscope. The instrument is constructed to withstand a wide range of environmental conditions.

Dc to 10 megahertz vertical bandwidth provides calibrated deflection factors from 1 millivolt to 10 volts/division.

The horizontal system provides calibrated sweep rates from 5 seconds to 1 microsecond/division and a X10 sweep magnifier to increase the fastest sweep rate to 0.1 microsecond/division. Three sweep modes are available: AUTO, NORM, and SINGLE SWP. The trigger circuit provides a stable display over the full bandwidth.

External horizontal input provides deflection factors of 20 millivolts to 2 volts/division for external sweep signal.

The crt is a direct-view, bistable storage device having an 8 x 10 division internal graticule. Each graticule division equals 0.25-inch. An enhance mode increases single-sweep writing rate.

The internal 1 kilohertz calibrator is connected internally to the vertical inputs and to a front-panel connector.

The 314 operates from a line voltage of 100, 115, 120, 200, 230, or 240 volts ac, or from a +12- or +24-volt dc source. The following tables contain a detailed listing of the 314 characteristics.

TABLE 1-1

Electrical Characteristics

Characteristic	Performance Requirement		Supplemental Information
VERTICAL			
Deflection Factor			
Calibrated Range	1 mV to 10 V/Div		13 steps in a 1-2-5 sequence
Accuracy	Within 3% over the calibrated range		
Uncalibrated Range (VOLTS/DIV VARIABLE)	Continuously variable between calibrated deflection factor settings. Extends highest deflection factor to at least 25 V/Div.		
Frequency Response			
Bandwidth	Without Probe	With P6149 Probe	
Direct Coupled, 4-div reference	At least 10 MHz	At least 10 MHz	1 mV to 10 V/Div with VARIABLE at CAL
Capacitively Coupled, 4-div reference	10 Hz or less to at least 10 MHz	1 Hz or less to at least 10 MHz	1 mV to 10 V/Div with VARIABLE at CAL
Step Response			
Risetime, 4-division Step Input	36 ns or less		1 mV to 10 V/Div

TABLE 1-1 (cont)

Characteristic	Performance Requirement		Supplemental Information
Maximum Input Voltage	Without Probe	With P6149 Probe	
Direct Coupled (DC)	300 V, dc plus peak ac	500 V, dc plus peak ac	
Capacitively Coupled (AC)	300 V dc		
Input R and C			
Resistance	1 MΩ, within 2%	10 MΩ, within 2%	
Capacitance	47 pF, within 4 pF	13.5 pF or less	
Signal Delay	Permits viewing leading edge of waveform that initiates trigger		
Chopped Repetition Rate	Approximately 100 kHz		
HORIZONTAL SYSTEM			
Sweep Time/Div			
Calibrated Range	5 s to 1 μs/Div. X10 magnifier extends sweep time/div to 0.1 μs		21 steps in a 1-2-5 sequence
Accuracy			
Unmagnified			
5 s to 0.5 s/Div	Within 4% over center 8 graticule divisions. Within 5% over any 2 division interval within center 8 divisions.		
0.2 s to 1 μs/Div	Within 3% over center 8 graticule divisions. Within 4% over any 2 division interval within center 8 divisions.		
Magnified			
0.5 s to 50 ms/Div	Within 5% over center 8 graticule divisions. Within 6% over any 2 division interval within center 8 divisions.		
20 ms to 0.5 μs/Div	Within 4% over center 8 graticule divisions. Within 5% over any 2 division interval within center 8 divisions.		
0.2 μs and 0.1 μs/Div	Within 5% over center 8 graticule divisions. Within 6% over any 2 division interval within center 8 divisions, excluding first and last 2 divisions of magnified sweep.		
TIME/DIV Variable	At least 2.5:1		

TABLE 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
	TRIGGERING SYSTEM	
Trigger Sensitivity		
Internal		INT button pressed in
AC	0.3 divisions from ≈50 Hz to 1 MHz, increasing to 1.0 division at 10 MHz	AC button pressed in
AC LF REJ	0.3 divisions from ≈50 kHz to 1 MHz, increasing to 1.0 division at 10 MHz	AC LF REJ button pressed in
External		INT button out and ATTEN-LINE on side panel in 1X or 10X position
DC	150 mV from dc to ≈1 MHz, increasing to 500 mV at ≈10 MHz	AC and AC LF REJ buttons both pressed in
AC	150 mV from ≈50 Hz to ≈1 MHz, increasing to 500 mV at ≈10 MHz	AC button pressed in
AC LF REJ	150 mV from ≈50 kHz to ≈1 MHz, increasing to 500 mV at ≈10 MHz	AC LF REJ button pressed in
LINE	≈150 mV, peak-to-peak, line voltage signal	INT button out and ATTEN-LINE switch on side panel in LINE position
External Trigger		
Level Range		
X1 Attenuator	−0.8 to +0.8 V	
X10 Attenuator	−8 to +8 V	
Maximum Input Voltage	300 V dc plus peak ac	
Input Resistance	1 mΩ, within 2%	
Input Capacitance	62 pF, within 4 pF	
	CALIBRATOR	
Output Voltage		
From +20°C (+68°F) to +30°C (+86°F)	0.5 V, peak-to-peak within 1%	
Repetition Rate	1 kHz, within 250 Hz	

TABLE 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
EXTERNAL HORIZONTAL INPUT		
Deflection Factor		
Horiz Gain X10, Atten 1X	≈20 mV/Div	
Horiz Gain X1, Atten 1X	≈200 mV/Div	
Horiz Gain X10, Atten 10X	≈200 mV/Div	
Horiz Gain X1, Atten 10X	≈2 V/Div	
Input Resistance		≈1 MΩ
Input Capacitance		≈62 pF
Bandwidth	DC to at least 200 kHz	
Variable Range	At least 10:1	
EXTERNAL BLANKING		
Sensitivity	+5 V to +20 V (direct coupled)	
Usable Freqency Range	100 kHz or greater	
Maximum Input Voltage		50 V dc plus peak ac
CRT DISPLAY SYSTEM		
CRT		
Graticule Area	8 x 10 divisions (1/4-inch/div)	
Graticule Type	Internal, non-illuminated	
Phosphor	P44	
STORAGE SYSTEM		
Storage Time	≈4 hours, maximum recommended	
Erase Time	≈300 ms	
Stored Writing Speed at 0.2 mA Cathode Current		
Normal	At least 80 div/ms (50 cm/ms)	
Enhanced	At least 400 div/ms (250 cm/ms)	
Auto Erase		
Viewing Time	≤1 sec to ≥5 sec	

TABLE 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
	POWER SOURCES	
Line Voltage		
Regulating Ranges		
115 V		
Low (LO)	100 V, ±10%	
Medium (M)	115 V, ±10%	
High (HI)	120 V, ±10%	
230 V		
Low (LO)	200 V, ±10%	
Medium (M)	230 V, ±10%	
High (HI)	240 V, ±10%	
Line Frequency	48 to 440 Hz	
Maximum Power Consumption	29 W at 115 V, 60 Hz (M position)	
External DC Voltage		
Range		
+12 V	+11 to +14 V	
+24 V	+22 to +28 V	
Maximum Input Current		
+12 V	1.6 A	Full Intensity in stored mode
+24 V	0.8 A	

Environmental Characteristics

Characteristic	Performance Requirement	Supplemental Information
Temperature		
Operating	−15°C to +55°C (+5°F to +131°F)	
Non-operating		−40°C to +75°C (−40°F to +167°F)
Altitude		
Operating	To 20,000 feet. Maximum allowable ambient temperature decreased by 1°C/1,000 feet from 5,000 feet to 20,000 feet	
Non-operating		To 50,000 feet

TABLE 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Humidity Non-operating		5 cycles (120 hours) of MIL-I-6181D. Omit freezing and vibration. Post test after drying period at +25°C, ±5°C at 20% to 80% relative humidity
Vibration Operating		15 minutes along each of the 3 major axes at a total displacement of 0.025-inches, peak-to-peak (4 g's at 55 cycles/sec) with frequency varied from 10 to 55 to 10 cycles/sec in 1-minute cycles. Hold for 3 minutes at 55 cycles/sec. All major resonances must be above 55 cycles/sec
Shock Operating and Non-operating		30 g's, 1/2 sine, 11 ms duration, 2 guillotine-type shocks per axis for a total of 12 shocks
Electromagnetic Interference as Tested in MIL-I-6181D Radiated Interference (from the Instrument under Test)		150 kHz to 1000 MHz
Transportation Package Vibration		1 hour slightly in excess of 1 g
Package Drop		30 inches on any corner, edge or flat surface

Physical Characteristics

Characteristic	Performance Requirement	Supplemental Information
Warmup Time		At least 5 minutes
Weight Net, without accessories		10 pounds (4.7 kilograms)
Shipping, Domestic		19.4 pounds (8.8 kilograms)
Dimensions		See Fig. 1-2.

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THEORY OF OPERATION

This section of the manual contains a description of the circuitry used in the 314 Oscilloscope. The description begins with a discussion of the instrument using the basic block diagram shown in Fig. 3-1. Then, each circuit is described in detail, using a detailed block diagram to show the interconnections between the stages in each major circuit and the relationship of the front-panel controls to the individual stages.

A complete block diagram is located in the Diagrams section at the rear of this manual. This block diagram shows the overall relationship of the circuits. A complete schematic of each circuit is also given in the Diagrams section. Refer to these diagrams throughout the following circuit description for electrical values and relationships.

BLOCK DIAGRAM

Description

The following discussion is provided to aid in understanding the overall concept of the 314 before the individual circuits are discussed in detail. A basic block diagram of the 314 is shown in Fig. 3-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each block represents a major circuit within the instrument. The number on each block corresponds to the numbers on the complete circuit diagram, which is located at the rear of this manual.

Vertical Amplifier

Signals to be displayed on the crt are applied to the CH 1 or CH 2 input connectors. The input signals are then amplified by the Channel 1 preamp or the Channel 2 preamp circuit. Each vertical preamp circuit includes separate vertical deflection factor, position, input coupling, gain, variable attenuation, and balance controls. A sample of each channel signal is supplied to the Trigger Pickoff circuit. The Channel 2 Preamp circuit contains an invert feature to invert the channel 2 signal displayed on the crt. The outputs of both Vertical Preamp circuits are connected to the Channel Switching circuit. This switching circuit selects the channel(s) to be displayed. An output signal from this circuit is connected to the Unblanking Amplifier circuit to blank the switching transients when in the chopped mode of operation. A sample of the signal present in the Channel Switching circuit is supplied to the Trigger Pickoff circuit.

The output of the Channel Switching circuit is connected to the Vertical Output amplifier through the delay line. The Vertical Output Amplifier circuit provides the final amplification for the signal before it is connected to the vertical deflection plates of the crt.

Triggering

The Trigger pickoff and Trigger Preamplifier circuits select a trigger signal (determined by the TRIGGERING Source switch) and produces an output signal that initiates the sweep signal produced by the Sweep Generator circuit. The internal trigger signal is selected from each channel circuit or the Channel Switching circuit. A sample of the line voltage applied to the instrument or an external signal applied to the EXT TRIG OR HORIZ input connector can also be used to generate a sweep-starting signal. The Trigger circuit contains level, slope, coupling, and source controls.

Sweep Generator

The Sweep Generator circuit produces a linear sawtooth output signal when inititated by the Sweep Trigger circuit. The slope of the sawtooth produced by the Sweep Generator circuit is controlled by the TIME/DIV switch.

The operating mode of the Sweep Generator circuit is controlled by the Sweep Mode switch. In the Auto mode of operation, the absence of an adequate trigger signal causes the sweep to free run. In the NORM mode, a horizontal sweep is presented only when triggered by an adequate trigger signal. The Single Sweep mode of operation allows one (and only one) sweep to be initiated after the circuit is reset with the RESET button.

The Sweep Generator circuit also produces an unblanking gate signal to unblank the crt. This gate is coincident with the sawtooth produced by the Sweep Generator circuit. Additionally, the Sweep Generator circuit produces an alternate trace sync pulse that is connected to the Channel Switching circuit. This pulse switches the display between channels at the end of each sweep when in the Alt mode of operation.

The output of the Sweep Generator circuit is amplified by the Horizontal Amplifier circuit to produce horizontal deflection for the crt in all positions of the TIME/DIV switch except EXT HORIZ.

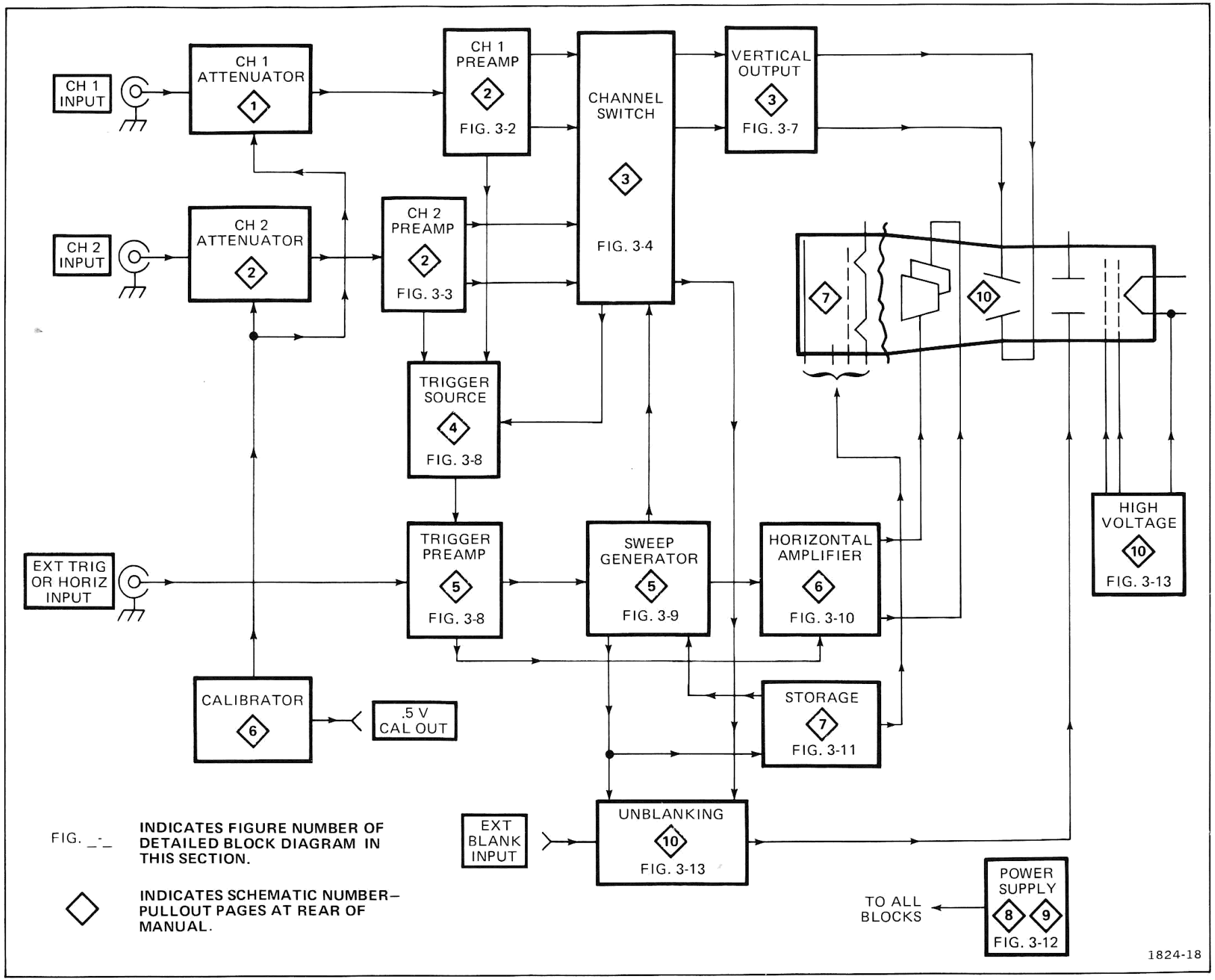

Fig. 3-1. Basic Block Diagram.

Other horizontal deflection signals can be connected to the horizontal amplifier by using the Ext Horizontal mode of operation. For the Ext Horizontal mode, the trigger preamplifier is used as a high-impedance-input amplifier, and when so used, the sweep generator is disabled.

CRT and Power Supply

The crt circuit contains the controls necessary for operation of the cathode-ray tube. Trace storage is accomplished by the Storage circuit. The Power Supply and crt circuits provide all the voltages necessary for operation of the instrument.

Calibrator

The Calibrator circuit provides a square-wave output with accurate amplitude, which can be used to check calibration of the vertical portion of the instrument and for probe compensation.

CIRCUIT OPERATION

This section provides a description of the electrical operation and relationship of the circuits in the 314. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits that are commonly used in the electronics industry are not described in detail.

CHANNEL 1 PREAMP ◇1◇ ◇2◇ AND CALIBRATOR ◇6◇

General

Input signals for vertical deflection on the crt are connected to the CH 1 connector. The Channel 1 Preamp circuit provides control of input coupling, vertical deflection factor, balance, vertical position, and vertical gain. A sample of the Channel 1 input signal is provided to the Trigger Source and Trigger Preamp circuits to provide internal triggering from the Channel 1 signal only. Fig. 3-2 is a detailed block diagram of the Channel 1 Preamp circuit. The signal from the calibrator is connected to the vertical system following the attenuators.

Input Coupling

Input signals applied to the CH 1 input connector can be ac coupled, dc coupled, or internally disconnected. When input coupling switch S2 is in the dc position, the input signal is coupled directly to the Input Attenuator circuit. In the ac position, the input signal passes through C2. This capacitor prevents the dc component of the signal from passing to the amplifier. In the GND position, S2 opens the signal path and connects the input of the amplifier to ground, providing ground reference without the need to disconnect the applied signal from the input connector. R2, connected across the input coupling switch, permits C2 to precharge in the ground position, so that the trace remains on screen when switched to the ac position.

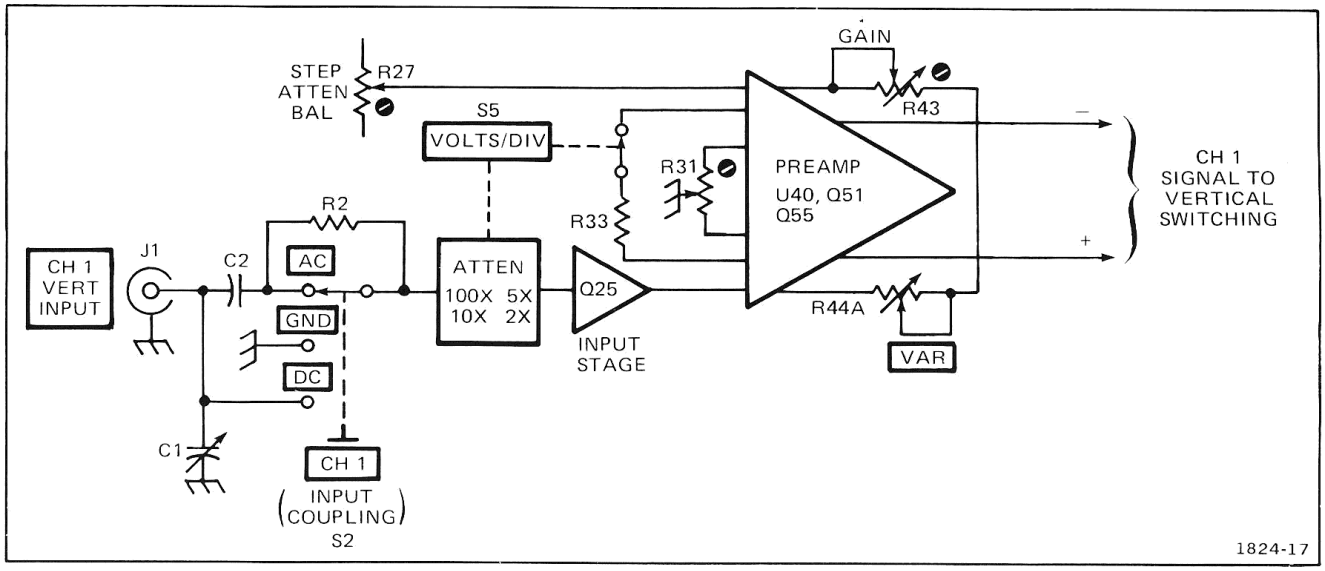

Fig. 3-2. CH 1 Preamp circuit block diagram.

Input Attenuator

The channel 1 deflection factor is determined by the CH 1 VOLTS/DIV switch.

The basic deflection factor of the vertical deflection system is 10 m/Div in the ten positions of the VOLTS/DIV switch above 5 m. In the 1, 2, and 5 m positions of the VOLTS/DIV switch, the basic deflection factor is 1 m/Div. For VOLTS/DIV switch positions other than 1 m/Div and 10 m/Div, attenuators are switched into the circuit to produce the vertical deflection factors indicated on the front panel. These attenuators are frequency-compensated voltage dividers. In addition to providing constant attenuation at all frequencies within the bandwidth of the instrument, the input attenuators are designed to maintain the same input RC characteristics (one megohm and approximately 47 picofarads) for each setting of the VOLTS/DIV switch. Each attenuator contains an adjustable series capacitor to provide correct attenuation at high frequencies and an adjustable shunt capacitor to provide correct input capacitance.

5 Division Calibrator

Switching either VOLTS/DIV switch to 5 DIV CAL provides a five-division (at approximately 1 kilohertz) display on the crt. The calibrator square-wave amplitude is accurate enough to permit vertical gain calibration. This calibrator signal also appears at the .5 V CAL OUT jack (on the front panel) for compensating attenuator probes (see Diagrams 1 and 6).

Input Stage

Channel 1 signal from the input attenuator is connected to the input stage through C22, R22B, and R22A. R23 provides the input resistance for this stage. R22A limits the current drive to the gate of Q25. CR23 and CR24 protect the circuit by clamping the gate of Q25A at about +6 or −6 volts if a high-amplitude signal is applied to the CH 1 input connector. Q25B is a relatively constant-current source and provides temperature compensation for Q25A.

Preamp Stage

The Preamp stage, U40, is a multiple-stage integrated-circuit amplifier. Adjusting the gain (R43) of this stage sets the overall gain for channel 1. R44A permits continuously variable, uncalibrated deflection factors between the calibrated settings of the VOLTS/DIV switch position. Var Balance R31 adjusts for no base-line shift of the crt display when rotating the VAR control.

In the 1 and 10m position of the VOLTS/DIV switch, no attenuation is used in the input attenuator stage. The correct vertical deflection factors are obtained by changing the gain of the Channel 1 Preamp stage. This gain change is accomplished by changing the value of the gain-setting resistance connected between pins 7 and 8 of U40. The Step Atten Bal adjustment, R27, adjusts for no baseline shift of the crt display when switching between the 1, 2, 5, and 10m positions of the VOLTS/DIV switch.

C34 is a compensation adjustment to provide optimum high-frequency response through the channel 1 amplifier. A sample of the signal being amplified in channel 1 is connected between pin 19 of U40 and the Trigger Source and Trigger Preamp circuits to permit "channel 1 only" triggering operation. Q51 and Q55, in the Output Amplifier stage, are connected as common-base amplifiers to provide a low-impedance load for the Preamp stage. Q51 and Q55 also provide isolation between the Preamp circuit and the Channel Switching circuit.

The Limit Centering adjustment, R53, sets the collector currents of Q51 and Q55 to match the center level of the signal in the Current Limiter stage to the center level of the linear operating region in the Vertical Output stage.

CHANNEL 2 PREAMP ◇1 ◇2

General

The Channel 2 Preamp circuit is basically the same as the Channel 1 Preamp circuit. Only the differences between the two circuits are described here. Portions of this circuit not described in the following description operate in the same manner as for the Channel 1 Preamp. Fig. 3-3 is a detailed block diagram of the Channel 2 Preamp.

Preamp Stage

Basically, the Channel 2 Preamp stage operates as described for Channel 1. However, the INVERT switch, S98, in the Channel 2 circuit, inverts the displayed signal.

CHANNEL SWITCH ◇3

General

The Channel Switching circuit determines which output signal (CH 1 or CH 2) is connected to the Vertical Output Amplifier circuit. In the Alt and Chop modes, the channels are displayed alternately on a shared-time basis. Fig. 3-4 is a detailed block diagram of the Channel Switching circuit. A schematic of this circuit is shown on Diagram 3 at the rear of this manual.

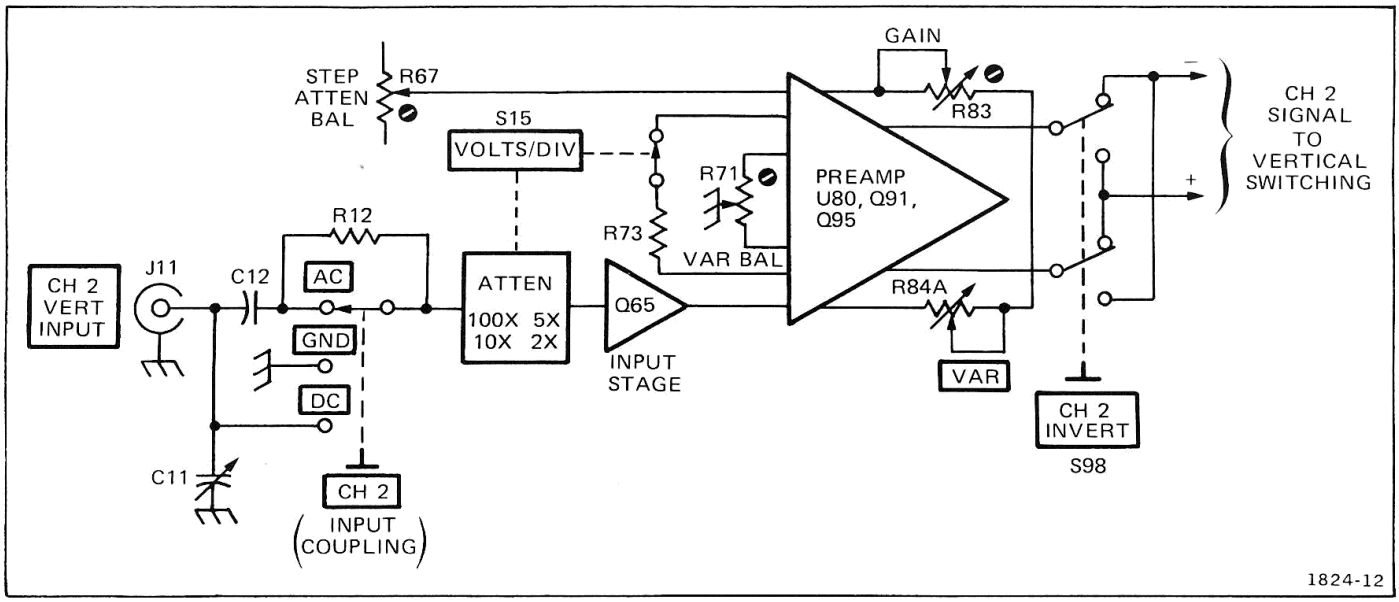

Fig. 3-3. CH 2 Preamp circuit block diagram.

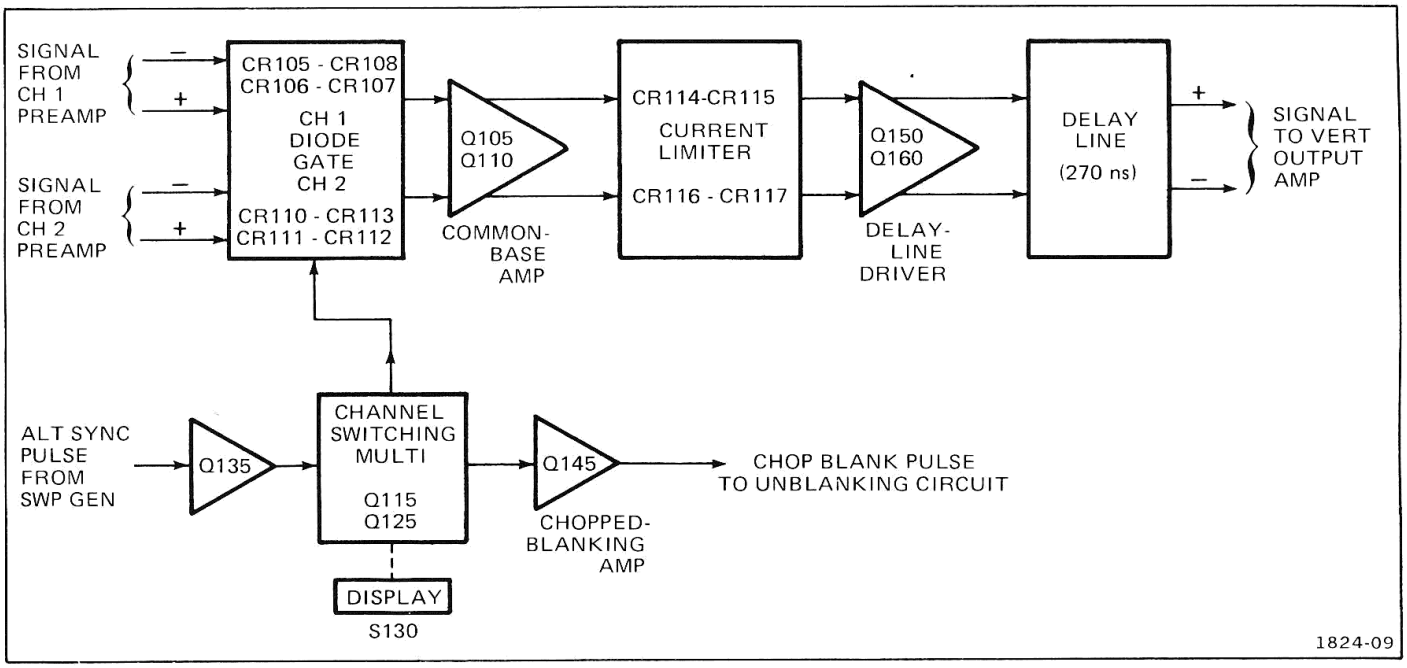

Fig. 3-4. Channel Switching block diagram.

Diode Gates

The diode gates (see Fig. 3-5) consisting of four diodes each, can be thought of as switches that permit either of the vertical preamp output signals to be coupled to the Common-Base Amplifier stage. CR105, CR106, CR107, and CR108 control the channel 1 signal output, and CR110, CR111, CR112, and CR113 control the channel 2 signal output. These diodes are, in turn, controlled by the Switching Multivibrator for dual-trace displays, or by the Vertical Mode switch for single-trace displays.

CH 1. In the CH 1 mode, −6 volts is applied to the junction of CR111-CR112 in the channel 2 diode gate through vertical mode switch S130C, R131, and CR130 (see simplified diagram, Fig. 3-5). This −6 volts forward biases CR111 and CR112 and reverse biases CR110 and CR113 since the input to the common-base amplifier stage is at about +0.6 volts. CR110-CR113 block the Channel 2 signal so it cannot pass to the Common-Base Amplifier. At the same time, in the Channel 1 Diode Gate, CR106 and CR107 are connected to +6 volts through R115. CR106

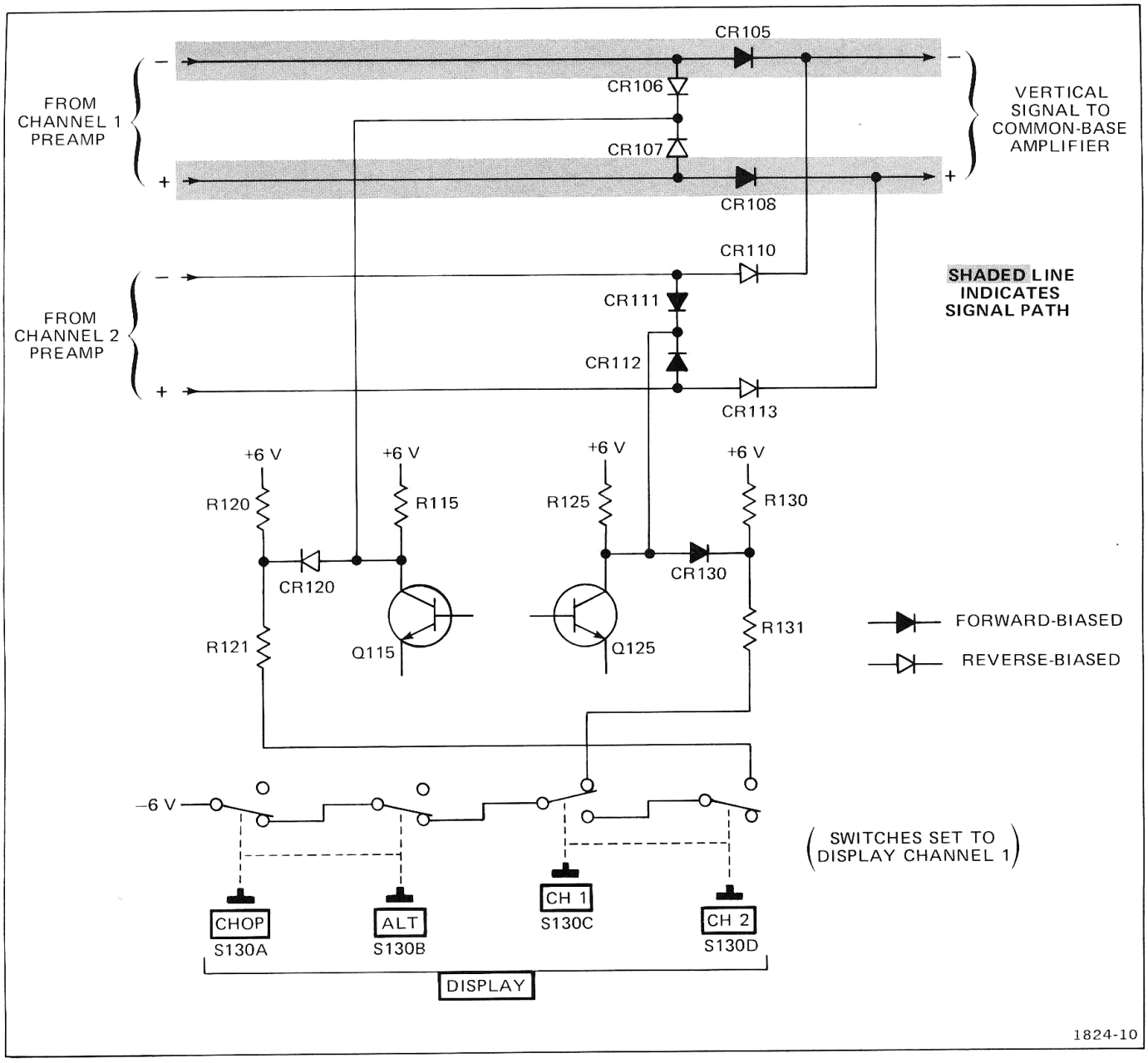

Fig. 3-5. Signal path, CH 1.

and CR107 are held reverse biased, while CR105 and CR108 are forward biased. Therefore, the Channel 1 signal can pass to the Common-Base Amplifier stage.

CH 2. In the CH 2 mode, the above conditions are reversed (see Fig. 3-6). CR106 and CR107 are connected to −6 volts through S130D, R121, and CR120, while CR111 and CR112 are connected to +6 volts through R125. The Channel 1 Diode Gate blocks the signal and the Channel 2 Diode Gate permits signal to pass.

Switching Multivibrator

ALT. In this mode, the Switching Multivibrator operates as a bistable multivibrator. −6 volts is connected to Q135 emitter (Alternate Trace Switching Amplifier stage, see Diagram 3), through R136. Q135 is forward biased and supplies current to the "on" transistor in the Switching Multivibrator stage through R135 and CR118 or CR128. For example, if Q115 is conducting, current is supplied to Q115 through CR118. The current through collector resistor R115 drops the CR106-CR107 cathode level negative with respect to the cathode of CR105 and CR108,

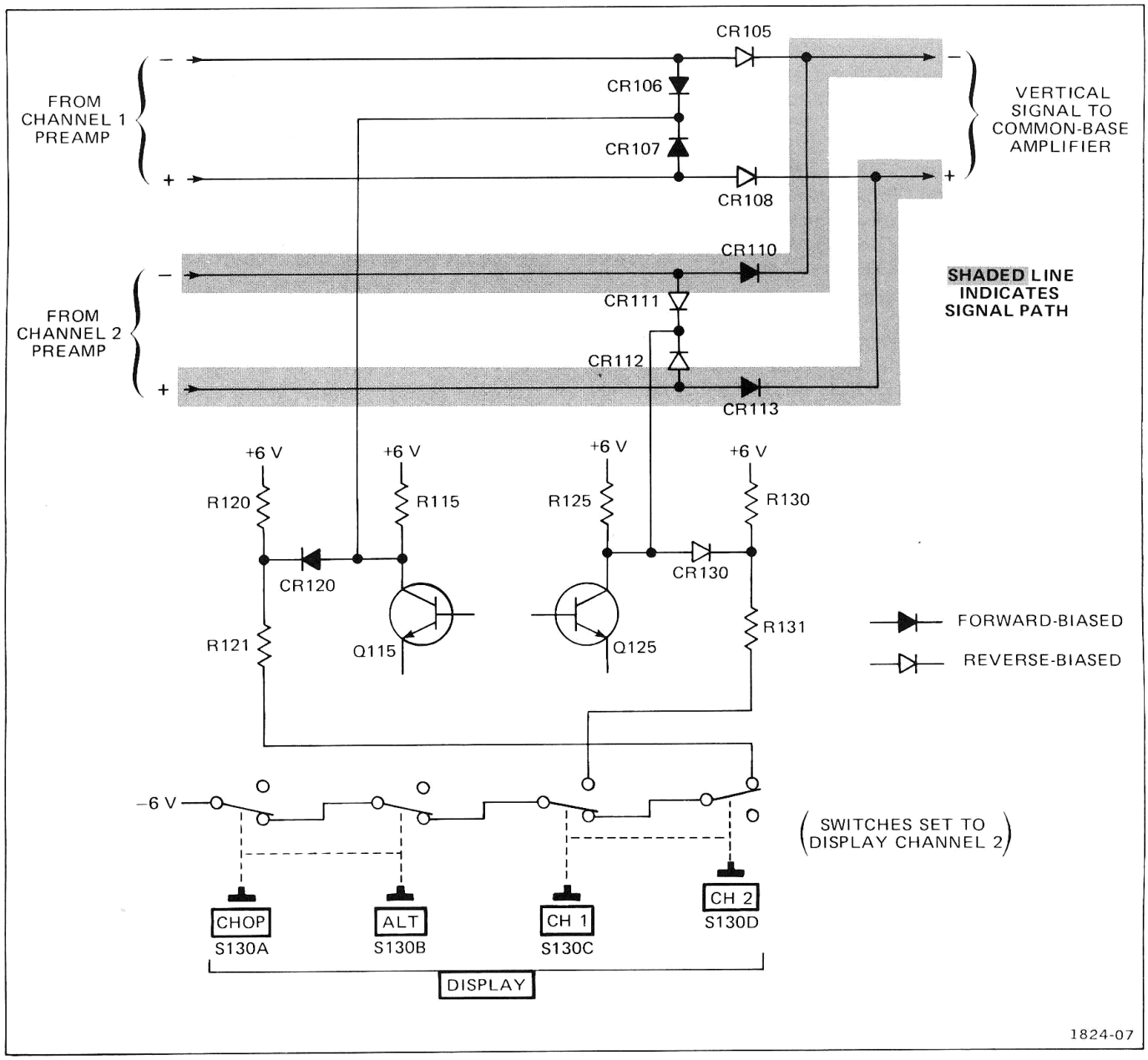

Fig. 3-6. Signal path, CH 2.

blocking the Channel 1 Diode Gate, as for Channel 2 only operation. The signal passes through the Channel 2 Diode Gate to the Common-Base Amplifier.

The alternate-trace sync pulse is applied to Q135 through R139 and C138 at the end of each sweep. This differentiated negative-going sync pulse momentarily interrupts the current through Q135, and both Q115 and Q125 are turned off. When Q135 turns on again after the alternate-trace sync pulse, the charge on C119 determines whether Q115 or Q125 conducts. For example, when Q115 is conducting, C119 is charged more positively on the CR118 side to the emitter level of Q115, and more negatively on the CR128 side. This charge is stored while Q135 is off, and holds the emitter of Q125 more negative than the emitter of Q115. When both Q115 and Q125 are off, the voltages at their bases become approximately equal. When Q135 turns on, the transistor with the most negative emitter starts conducting first, with the resulting negative movement at its collector holding the other transistor off. On the next sync pulse, the conditions described previously are reversed; now the Channel 2 Diode gate is reverse biased, and the Channel 1 signal passes through the Channel 1 Diode Gate.

CHOP. In the Chop mode, the Switching Multivibrator stage free runs as an astable multivibrator at about 100 kilohertz. The emitters of Q115 and Q125 are connected to −6 volts through R118, R128, through R140 and T140 primary. At the time of turn on, one of the transistors begins to conduct; for example, Q115. The negative level at Q115 collector forward biases CR106 and CR107 and back biases CR105 and CR108, preventing the Channel 1 signal from reaching the Common-Base Amplifier. Meanwhile, the Channel 2 Diode Gate passes the Channel 2 signal to the Common-Base Amplifier.

The frequency-determining components in the Chop mode are C119, R119, R118, and R128. Switching action occurs as follows: when Q115 is on, C119 attempts to charge to −6 volts through R128. The emitter of Q125 goes slowly toward −6 volts as C119 charges. The base of Q125 is held at a negative voltage determined by the voltage divider R116-R127, between −6 volts and the collector voltage of Q115. When the emitter voltage of Q125 reaches a level slightly more negative than its base, Q125 conducts. Q125 collector level goes negative and pulls the base of Q115 negative through divider R117-R126 to turn Q115 off, switching the Diode Gate stage to connect the opposite half to the Common-Base Amplifier stage. Again, C119 begins to charge toward −6 volts, this time through R118. As C119 charges, the emitter of Q115 goes slowly negative until Q115 turns on. Q125 is off and the cycle begins again.

The Chopped Blanking Amplifier stage, Q145, provides an output pulse to the Unblanking circuit that blanks the transitions between the Channel 1 and the Channel 2 traces. When the Switching Multivibrator stage changes states, the voltage across T140 momentarily increases. A negative pulse is applied to the base of Q145 to turn Q145 off. The width of the pulse at the base of Q145 is determined by R142 and C142. Q145 is driven quickly into cutoff, and the positive-going output pulse, which coincides with trace switching, is connected to the Unblanking circuit through R147.

ADD. In the Add mode, S130A and B closed, the Diode Gate stage permits both signals to pass to the Common-Base Amplifier stage. The Diode Gates are both held on by −6 volts applied to their cathodes through R108 and R105-R106. Since both signals are applied to the Common-Base Amplifier stage, the output is the algebraic sum of the signals on Channels 1 and 2.

The Common-Mode Adjustment, R108, sets the deflection plate levels of the Vertical Output Amplifier in the Add mode.

Q105 and Q110 are connected as common-base amplifiers to provide a low impedance load, with about +0.6 volt on Q105-Q110 emitters, to ensure the operation of the Diode Gate stage. Q105 and Q110 also provide the current drive for the Current Limiter stage.

Current Limiter

The Current Limiter stage (CR114, CR115, CR116, and CR117, see Fig. 3-4) decouples the Delay-Line Driver stage from the Common-Base Amplifier during overdrive conditions, preventing the Output Amplifier from being driven to a non-linear operating region.

Delay-Line Driver

Output of the Current Limiter stage is applied to the Delay-Line Driver stage, Q150 and Q160. Q150 and Q160 are connected as feedback amplifiers with R150-R156 and R160-R166 providing feedback from the collector to the base of their respective transistor. A sample of the signal in the collector circuit of Q160 is used for triggering in the COMP TRIG mode. C153-C154 and R154 provide high-frequency compensation of the delay line termination. The output of the Delay-Line Driver stage is connected to the Vertical Output amplifier through the Delay Line, DL180.

VERTICAL OUTPUT AMPLIFIER ◇3

General

The Vertical Output Amplifier circuit provides the final amplification for the vertical deflection signal. This circuit includes the delay line. Fig. 3-7 is a detailed block diagram of the Vertical Output Amplifier circuit.

Delay Line

Delay Line DL180 provides approximately 270 nanoseconds delay to the vertical signal to give the Sweep Generator circuit time to initiate a sweep before the vertical signal reaches the vertical deflection plates of the crt. This delay permits display of the leading edge of the signal that initiates the trigger (when using internal triggering).

Output Amplifier

Q188 and Q198 are connected as common-base amplifiers to provide a low input impedance to properly terminate the delay line. Q188 and Q198 also provide isolation between the delay line and the following stages.

Q200, Q202, Q205, Q206, Q210, Q212, Q215, and Q216 are connected as push-pull multi-stage operational

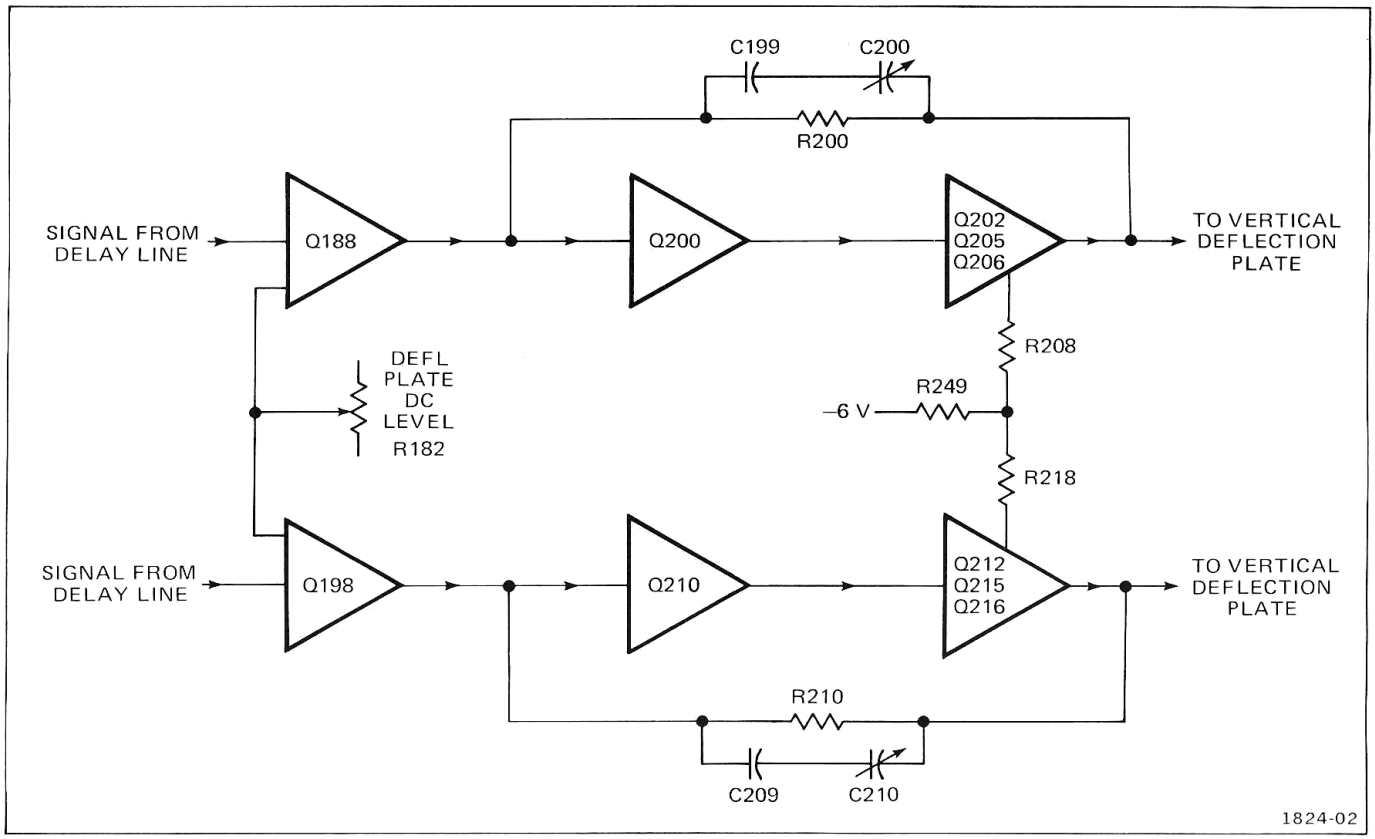

Fig. 3-7. Vertical Output Amplifier block diagram.

amplifiers, quiescently supplying approximately 50 volts dc to each of the crt vertical deflection plates. The deflection plate dc levels are adjusted by R182, Defl Plt DC Level. Q200 and Q210 (emitter follower amplifiers) drive the Output stage. The two halves of the Output amplifier operate in push-pull. Current in one side decreases as current increases in the other. C200 and C210 are compensation adjustments to provide optimum high-frequency response.

TRIGGER SOURCE ◈4

Internal

The Internal Trigger Source circuit (see Fig. 3-8) selects and amplifies the internal trigger signal to the level required at the input of the Trigger Preamplifier stage. Input signal for the Internal Trigger Source circuit is a sample (from pin 19 of U40 or U80) of the signal applied to CH 1 or CH 2, or a sample of the composite vertical signal from the Delay-Line Driver stage.

Diode Gate. The diode gates, consisting of two diodes each, can be thought of as switches that allow one of the three internal trigger signals to be coupled to the Trigger Source Amplifier. CR225 and CR226 control the Channel 1 signal, CR229 and CR230 control the Channel 2 signal, and CR222 and CR223 control the composite signal. These diodes are controlled by the Trigger Source switch, ganged with the DISPLAY switch. Q165 provides high impedence input to prevent loading the Delay-Line Driver stage. The composite signal applied to the base of Q165 causes signal in the collector of Q220. Q232 and Q237 compose an emitter-coupled comparator amplifier. Q235 is a feedback amplifier with R233 providing the feedback. Q236 is an emitter-follower amplifier providing low output impedance.

Source and Coupling

The Trigger Source switches, S130 and S305A (see Fig. 3-5 and Fig. 3-8), select the trigger signal source. Five trigger sources are available: CH 1, CH 2, COMP, EXT, and LINE. When the INT or EXT/LINE switch, S305A, is pressed, one of the internal trigger signals is obtained from the Trigger Source circuit. When the INT or EXT/LINE switch is released, either the external signal or the line trigger signal is available by switching LINE/EXT ATTEN switch S300. S300 also provides ten times attenua-

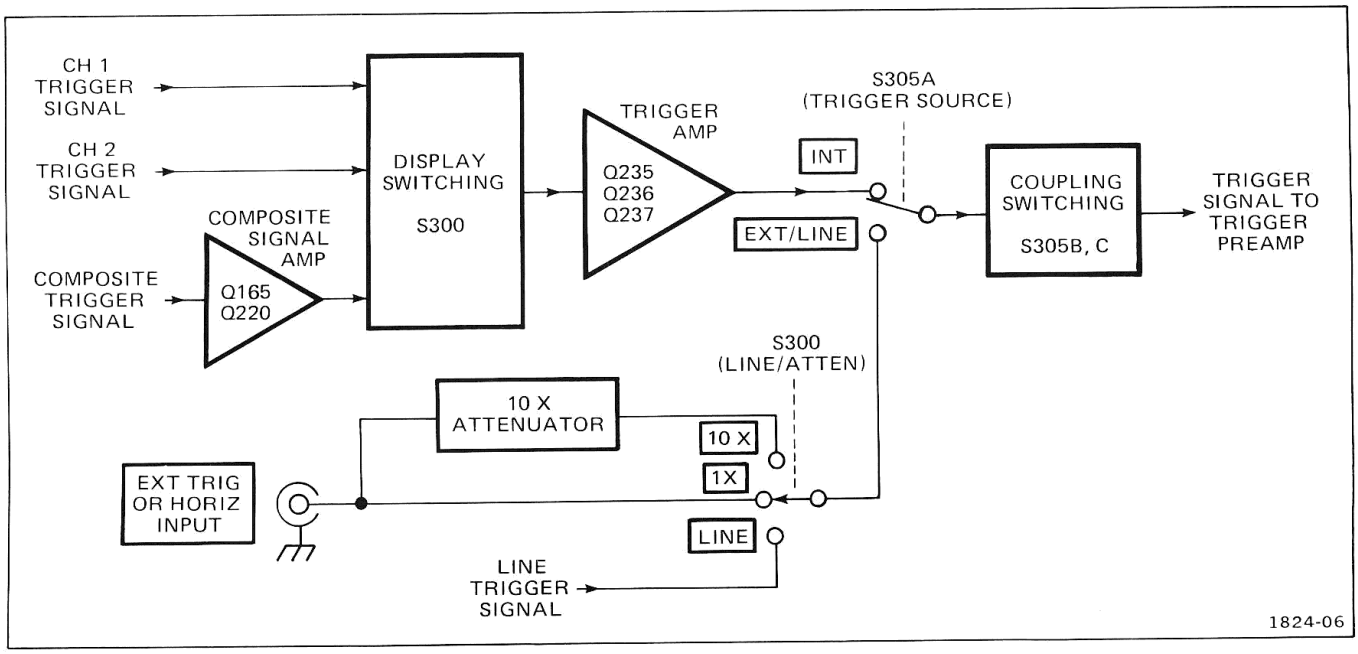

Fig. 3-8. Trigger Source block diagram.

tion for the external trigger signal. Input impedance of the EXT TRIG OR HORIZ input is 1 megohm, paralleled by about 62 picofarads. The line trigger signal is obtained from the secondary of transformer T600 through the voltage divider C601-C602 and switch S300. Fig. 3-8 is a block diagram of the Trigger Source circuit.

Trigger Coupling switch S305 offers a means of accepting or rejecting certain components of the trigger signal. In the AC and AC LF REJ modes of trigger coupling, the dc component of the trigger signal is blocked by coupling capacitor C305 or C306. Frequency components below about 50 hertz are attenuated when using AC coupling and below about 50 kilohertz when using AC LF REJ. The higher-frequency components of the trigger signal are passed without attenuation. In the INT trigger mode, AC and AC LF REJ trigger coupling are available. In the EXT or LINE mode, AC, AC LF REJ and DC are available.

The line trigger signal is obtained from the secondary of T600 in the Power Supply circuit. This sample of the line frequency is coupled to the Trigger Preamp circuit in the LINE mode. The Trigger Coupling switches should not be in the AC LF REJ mode when using this trigger source, as the trigger signal is blocked by the AC LF REJ circuit.

TRIGGER PREAMP AND SWEEP GENERATOR 5

Trigger Preamplifier

Q313A, Q313B, Q318, and Q320 (see Fig. 3-9) form a voltage comparator system to select the amplitude of a triggering signal on which a sweep can be initiated. The triggering signal is applied to the gate of Q313A and a dc level established by R331, (TRIGGERING LEVEL) is applied to the gate of Q313B. When the two halves of the comparator are balanced, the voltage at Q318 collector is about zero and the current through R323 is zero. When the triggering signal passes through the selected dc level, the conduction of the two halves of the comparator is shifted and when the collector of Q318 moves away (positive or negative) from about zero volts, far enough to produce the drive current through R323, a trigger is initiated in U340

Sweep Generator

The Sweep Generator circuit produces a linear saw tooth voltage that is used to provide sweep deflection in the oscilloscope. The Sweep Generator also provides positive-going and negative-going gates to perform sweep-related functions such as time-shared switching and crt unblanking.

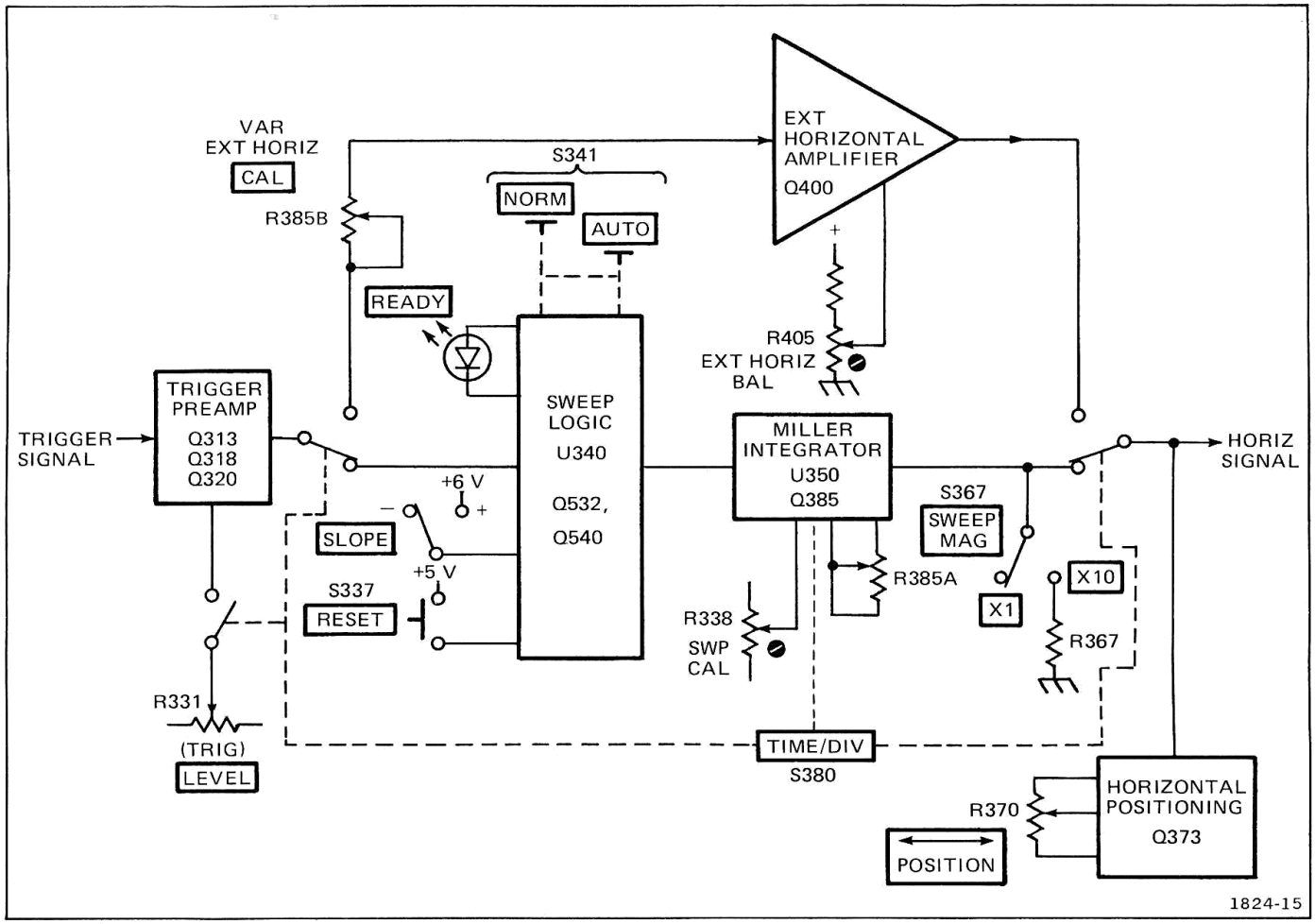

Fig. 3-9. Sweep Generator and External Horizontal block diagram.

The Sweep Generator circuit is composed of two integrated circuits, Sweep Logic (U340) and Miller integrator (U350) and associated discrete circuit components. The primary functions of these components are trigger slope selection and pulse forming; sawtooth start and stop; holdoff and single-sweep lockout; and bright-baseline generation. Table 3-1 lists each IC pin and its function. All pins are digital unless otherwise noted and positive logic is employed. Pins not used are grounded.

The Triggering and Sweep Mode switch, S341, permits three modes of operation: Normal, Auto, and Single Sweep.

Fig. 3-9 is a block diagram of the Sweep Generator and External Horizontal Amplifier circuits.

TABLE 3-1

SWEEP GENERATOR IC INPUT-OUTPUT

Sweep Logic, U340

Pin		Function
1	End Sweep	Current (logic 1) for at least 20 nanoseconds ends sweep. Continuous current locks out sweep. No input (logic 0) permits U340 to operate.
2	Not used	Grounded to chassis
3	Not used	Grounded to chassis
4	Trigger Input	Low impedance analog input. Accepts analog current triggering signal.

TABLE 3-1 (cont)

Pin		Function
5	Slope Select	Logic 1 permits trigger to be initiated on the positive slope of a triggering signal; logic 0 permits trigger to be initiated on the negative slope.
6	Single Sweep Control	Logic 1 permits repetitive sweep. Logic 0 permits only a single sweep to be produced unless reset (see pin 7).
7	Single Sweep Reset	Current into pin 7 (logic 1) for at least 20 nanoseconds resets single sweep system and allows sweep to be retriggered. After reset occurs, C335 and R336 permit this input to return to ground (logic 0).
8	GND (Substrate)	Provides ground reference for the device.
9	READY Indicator	Provides power to READY indicator when sweep is ready for triggering (Single Sweep Mode). Removes power, extinguishes indicator upon receipt of sweep trigger. Open at other times.
10	Lockout	Logic 1, sweep is locked out. Logic 0, lockout off.
11	Holdoff Timing	Connects timing components that set trigger lockout period after end of sweep. Capacitor discharges as soon as sweep is started, and timing starts at end of sweep as capacitor charges. When capacitor charges to upper threshold, new sweep can be produced either upon receipt of next trigger or if pin 12 is above its upper threshold (see pin 12).
12	Bright Baseline Timing/Off	Used in Auto Trigger Mode to connect timing components that set bright baseline off period after trigger recognition. If triggering signal is absent or occurring at a rate less than 15 hertz, capacitor charges toward the +3.5-volt threshold. Above the +3.5-volt level, U340 is conditioned to provide a free-running sweep at a rate determined by the holdoff RC and sweep timing. As soon as a trigger arrives at pin 4 of U340, pin 12 is driven to ground and C345 is discharged.
13	Bright Baseline Control	Current into pin 13 (logic 1) for ≥20 nanoseconds keeps pin 12 at ground, holding Bright Baseline off. Baseline remains off for one timing period after current level is removed. No input (logic 0) allows Bright Baseline to function (see pin 12).
14	+Gate Output	Provides a +5-volt source through 2 kilohms (logic 1) during sweep, driving current into pin 1 of U350. Logic 0, sweep is not being produced. Maximum delay after fast-rise trigger initiation is 30 nanoseconds.
15	−Gate Output	Logic 0 during sweep. Provides +5-volt source through 2 kilohms (logic 1) when sweep is not being produced. Maximum delay after fast-rise trigger initiation is 25 nanoseconds.
16	Power Supply	+5-volt supply terminal.

Miller Integrator, U350

Pin		Function
1	Sweep Gate In	Current into pin 1 results in sawtooth voltage at pin 8.
2	Oscillation Suppressor	Connects discrete components to prevent oscillation of the Miller integrator.
3	Ground	Provides ground reference to the device.
4	End Sweep-Pulse Gate Out	Drives current into pin 1 of U340 to terminate sweep.
5	Not used	Function blocked.
6	End Sweep Level	Connects voltage divider to a reference comparator inside the device, establishing the level at which the sweep sawtooth is terminated.

TABLE 3-1 (cont)

Pin		Function
7	Power Supply	+12-volt supply terminal.
8	Sawtooth Output (Integrator Output)	Produces sweep sawtooth voltage when current is gated into pin 1. Sawtooth is positive going, with amplitude from 0 to about +6 volts.
9	Timing Current Input	Connects timing components which determine sweep rate.
10	Substrate	Supply of about 11 milliamperes applied.

Normal Triggered Mode

The Trigger Preamplifier circuit provides current drive to pin 4 of U340 at selected levels on both the positive- and negative-going slopes of the triggering signal. Slope switch S338 controls the level at pin 5 to determine the slope at which the sweep is initiated.

When the trigger is initiated in U340, a positive transition occurs at pin 14. This output remains high until the sweep terminates. At the same time, a negative-going gate is produced at pin 15, which is used to unblank the crt.

U350 is a Miller integrator, a type of operational amplifier in which the feedback element is the timing capacitor. Before a positive gate is received from U340, timing capacitor C360, C361, or C363 has essentially no charge, as it is clamped by a network inside U350. Current through the timing resistor network (R360, R382, and R385A) is input to pin 9 of U350. When the positive gate arrives from U340, the current is switched into the timing capacitor and the timing capacitor begins to charge. The current is nearly constant, and since pin 9 is the operational null point, a linearly increasing voltage (sawtooth) is produced at pin 8. The rate of the sawtooth rise is a function of the constant current through the timing resistors and the capacitance of C360, C361, or C363.

The voltage at pin 8 of U350 continues to go positive until it reaches the level set at pin 6 by voltage divider R352 and R353. At this point, a reference comparator inside U350 produces a current output at pin 4, which is conducted through CR333 to pin 1 of U340, causing the outputs at points 14 and 15 to revert to their original states. With the positive voltage removed at pin 1 of U350, the timing capacitors discharge into pin 9 and the sweep terminates.

A short-duration trigger-lockout period (to allow the sweep circuits to stabilize when the sweep terminates) is provided by the holdoff network at pin 11 of U340. For U340 to function, the voltage at pin 11 must be at least +3.5 volts. When the sweep starts, the voltage at pin 11 is driven to ground, discharging the holdoff capacitors (C347, C348, or C349). The capacitors begin to charge as the sweep progresses, and continue to charge as the sweep terminates. The time between sweep termination and the point at which pin 11 reaches the +3.5-volt threshold is the holdoff period.

The timing and holdoff RC components are selected by the TIME/DIV switch, S380. Sweep Cal Adjustment R388 permits calibration of this circuit for accurate timing when Variable control R385A is in the CAL detent position. The Variable control provides uncalibrated, continuously variable timing.

Auto-Triggered Mode

Operation of the Sweep Generator in the Auto Triggered mode is the same as that described for the Normal Triggered mode when a trigger is present and occurring at a rate greater than 15 hertz. However, when a trigger is not present within a specified time, a free-running referenece trace, or bright baseline is produced. This is accomplished as follows: when the AUTO button is pushed in, R340 is disconnected from +6 volts, removing the bright baseline lockout current from pin 13 of U340, permitting the Bright Baseline Timing circuit, R345-C345 to function. Each time a trigger is initiated in U340, pin 12 is driven to ground and C345 is discharged. C345 immediately begins to recharge. If the capacitor is allowed to charge above the +3.5-volt threshold level, U340 is conditioned to provide a positive gate at pin 14 and a negative gate at pin 15 as soon as the holdoff period is completed (when pin 11 rises above its threshold). The sweep free runs at a rate determined by the timing and holdoff networks.

Single Sweep Mode

Operation of the Sweep Generator in the Single Sweep mode is similar to operation in the Normal Triggered mode. However, after one sweep has been produced, further triggers are locked out in U340 until the RESET button is pressed.

When both NORM and AUTO buttons are pushed in (Single-Sweep) the following conditions are established in U340. +5 volts is applied to R340 to drive current into pin 13, keeping pin 12 at ground and holding the bright baseline feature off. Pin 6 is grounded, requiring U340 to be manually reset. Ready indicator CR340 is connected to pin 9 through R342 to indicate that the system is reset and triggerable. As soon as the system is triggered, the Ready indicator is extinguished.

The system is reset when RESET button S337 is pushed. +5 volts is applied to differentiating network C335, R336, C332, and R332. The positive spike appearing at pin 1 terminates any sweep that is in progress and the spike appearing at pin 7 resets the system.

Sweep Magnification and Positioning

X10 magnification of the sweep is achieved by changing the attenuation ratio of the output sawtooth. For an unmagnified sweep, R366, R367, and R368 provide about 20X attenuation of the sawtooth, reducing the sweep amplitude from about +6 volts to about +0.3 volts. The deflection sensitivity of the crt is such that this amplitude gives one screen width of deflection, provided that the output sawtooth is centered about ground, which corresponds with screen center.

When the Sweep Mag Switch, S367, is switched to the X10 position, R367 is disconnected, changing the attenuation to about 2X, increasing the sawtooth amplitude to about +3 volts. Since only one-tenth of this amplitude is accepted by the oscilloscope, the displayed segment appears as an X10 magnification. In X10 position of X10 Mag switch, all sweep rates indicated on the panel are magnified by a factor of ten.

POSITION Control R370 provides an adjustable change in the conduciton of Q373 to alter the dc level of the output signal. Positioning range is sufficient to move any portion of a magnified sweep into the on-screen window.

EXT HORIZ ◇5

General

To operate the horizontal in the amplifier mode, the TIME/DIV switch is rotated counterclockwise into one of the two EXT HORIZ positions. In this condition, the Sweep Generator circuit is disabled (including the crt blanking gate), and the output of the Trigger Preamplifier is connected to the Horizontal Amplifier circuit through the common-base amplifier.

Input Stage

A signal applied to input connector J300 is passed to the gate of Q313A, through switches S300 and S305. Q313A, Q313B, Q318, and Q320 form a non-inverting operational amplifier, which is operated as an X2 gain amplifier to isolate the next amplifier stage from the high impedance input circuitry.

LEVEL control R331 is disconnected from the gate of Q313B.

Output Stage

The output from the collector of Q318 is connected to the emitter circuit of Q400, which is a common-base amplifier. The signal produced at Q400 collector is in phase with the applied signal. Two steps of gain selection are available. In X1 gain position of the TIME/DIV switch, the deflection factor is about 200 mV/Div. In X10 gain position, the deflection factor decreases to about 20 mV/Div. As R385B is varied, more resistance is added to the emitter circuit, decreasing the gain. R405 adjusts for no beam position shift of the crt display when rotating the VAR control. The output signal of this stage is applied to the horizontal amplifier.

HORIZONTAL AMPLIFIER ◇6

General

The horizontal amplifier accepts a horizontal sweep voltage from the sweep generator, amplifies it, and applies the resulting push-pull signal to the horizontal deflection plates of the crt. During EXT HORIZ operation, the input from the sweep generator is disconnected, allowing EXT HORIZ input signals to be amplified and applied to the horizontal deflection plates. Fig. 3-10 is a block diagram of the Horizontal Amplifier stage.

Emitter-Follower Amplifier

The signal from either sweep generator or EXT HORIZ amplifier is applied to the emitter-follower stage, Q430. This stage provides a high input impedance to prevent loading the preceding stage.

Common-Base Amplifier

The signal output of Q430 is passed to the output amplifier through the common-base amplifier, Q435. Q435 isolates the input circuit from the output amplifier. When the crt display mode is in Store, R429 is short circuited by the Store switch, S500A, to increase the gain of the horizontal amplifier, correcting for the crt deflection sensitivity change that occurs when the display is shifted to the stored state.

Output Amplifier and Output Inverter Amplifier

Assume that a positive-going sweep signal is arriving at the input of the amplifier. The positive-going voltage is applied to Q440 base. Q440 and Q442 form a non-inverting amplifier circuit, and a positive signal is developed at Q442 collector. This signal is amplified and inverted by Q450, providing a negative-going signal for the left deflection plate. The collector of Q450 is also applied to feedback circuit R443A-R443B-C443. The changing voltage of Q450 causes most of the signal current required by the input signal to flow through the R443A-R443B-C443 network. Therefore, only a very small part of the input signal is seen at the base of Q440.

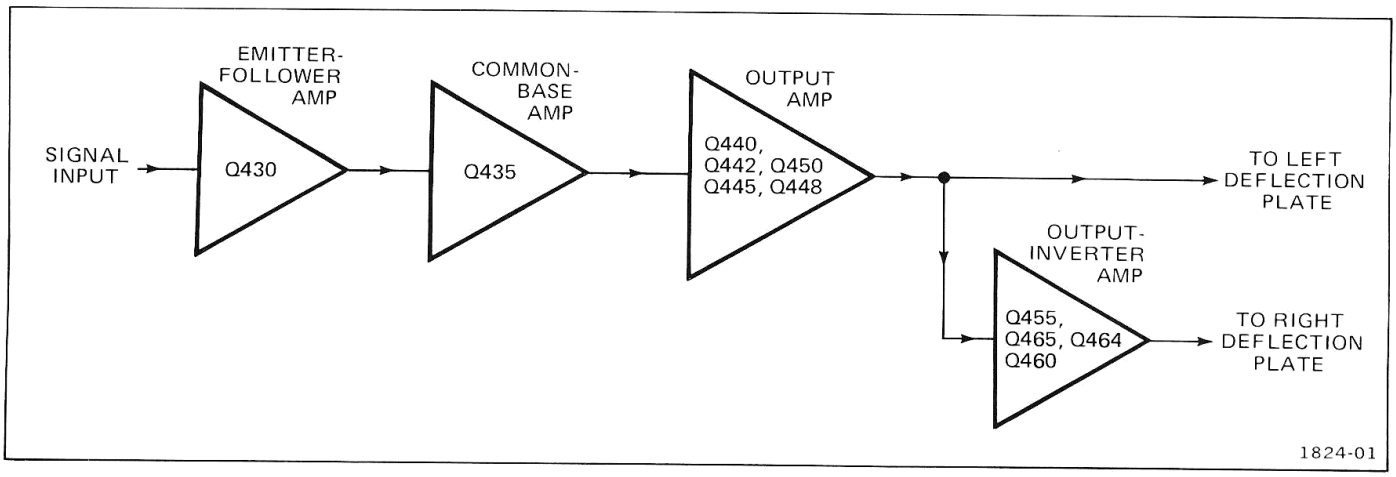

Fig. 3-10. Horizontal Amplifier block diagram.

The gain of the output amplifier is determined by the ratio of feedback resistor R443A-R443B to the resistance of R429-R432. This ratio is approximately 450.

The voltage at Q450 collector is also applied through R455 to the Q455-Q465 output inverter circuit. This circuit is also an operational amplifier, with the feedback resistor, R458, equal to the input resistor, R455. Gain of the circuit is therefore equal to one, providing a signal (equal and opposite that of the left deflection plate) to the right deflection plate.

Standing current for Q450 is provided by Q448 and its associated emitter circuit, which consists of Q445 and resistors R445, R446, R447, and R448. The base voltage of Q448 is established by VR451. This voltage sets the voltage at the Q448 emitter and therefore at the base of Q445. Q445 and Q448 provide the principal current paths for Q448. When slow sweep rates are selected, this current is relatively unchanged by the sweep signal. The Q465 standing current is achieved in a similar manner.

When fast sweep rates are selected, the positive-going signal at Q442 collector is applied through C445 to the base of Q445. This decreases the drive to Q445 and therefore to Q448, aiding in the generation of the negative-going signal for the left deflection plate. During this time, the negative-going signal at Q455 emitter is coupled through C459 to Q460 base. This increases Q460 drive and therefore increases Q460 current, aiding in the generation of the positive-going signal for the right deflection plate. During retrace, the signal changes in a direction opposite to that just described, and the Q445 and Q460 circuits reverse their functions.

STORAGE 7

General

The Storage circuit (see Fig. 3-11) provides the voltage levels necessary to operate the crt flood guns, collimation electrodes, and target backplate.

The circuitry includes an erase multivibrator, a target-control amplifier, an enhance generator, and an integrate circuit. Fig. 3-11 is a block diagram of the Storage circuitry.

The Enhance Generator circuit permits very fast single-sweep signals to be stored. The integrate feature permits storage of a number of repetitive sweeps, each of which would be too fast to store as a single-sweep event.

The Auto Erase Generator circuit automatically produces an erase trigger pulse that initiates an erase pulse following the end of the sweep.

The Sweep Reset Delay Multivibrator circuit produces a sweep reset pulse after written information has been erased in the Auto Erase mode.

Storage Tube

The crt used in the 314 is a direct-view, bistable storage cathode ray tube. Storage, which is the retention on the crt of a displayed event, is based on a secondary emission principle. A stream of primary electrons strikes an insulated target surface with sufficient energy to dislodge electrons. As the potential increases, each primary electron dislodges more than one secondary electron, resulting in the target material charging positive. The

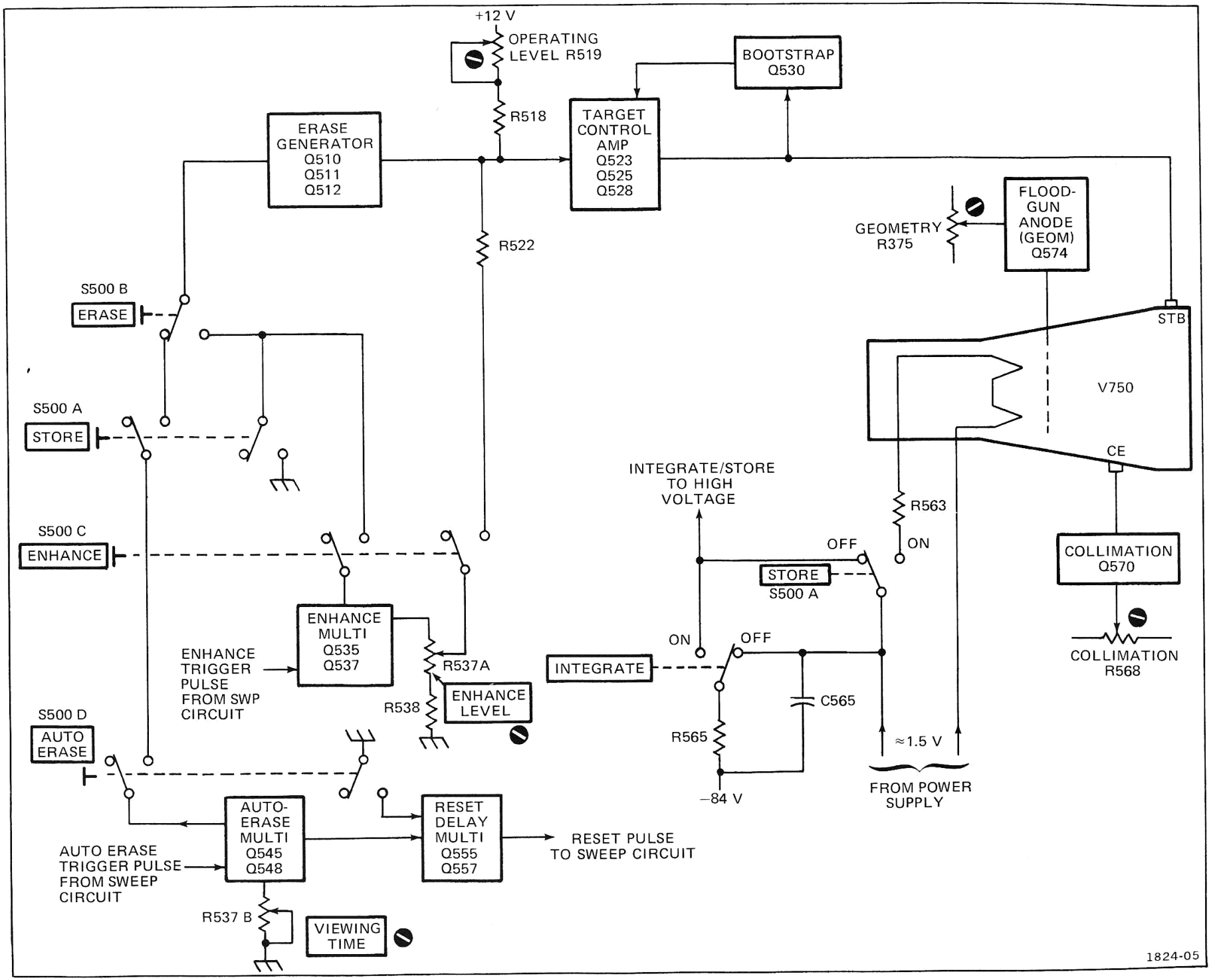

Fig. 3-11. Storage block diagram.

target approaches the backplate potential, yielding higher-energy flood electrons, resulting in light output.

The storage cathode-ray tube contains special storage elements in addition to the conventional writing-gun elements. The operating mode of the tube depends primarily on the voltage applied to these storage electrodes. With one condition of applied potential, the storage screen or target backplate operates in the ready-to-write state; then, when it is bombarded with high-energy writing-beam current, the bombarded portion shifts to the stored mode to store a written display. With a different set of applied voltages, the screen (target) operates in the conventional mode, similar to a conventional crt.

Flood Guns and Collimation Electrodes

Two low-energy electron guns (flood guns) are used in the 314 crt. The cathodes are connected to −120 volts through the Integrate switch, S565, and R565, VR564, and VR565. The voltage drop across VR564-VR565 sets the voltage level of the cathode at about −90 volts. The flood gun anode and the geometry electrode are connected together, and the voltage levels of these electrodes are set by adjustment R575, through Q574.

The collimation electrodes serve as an electrostatic lens to distribute the flood gun electrons uniformly over the storage target, and have no effect on the landing energy of the electrons. R568 determines the voltage level of CE, through Q570 and R573.

Target-Control Amplifier

The Target Control Amplifier is used to maintain a high degree of control of storage backplate voltage. These amplifiers are emitter-follower feedback amplifiers consisting of Q523, Q525, and Q528. A bootstrapping circuit is provided for each target control amplifier to maintain transistor operating voltage during the positive-going portion of the erase waveform (fade positive). The bootstrapping circuits are described in full detail in the Erase Generator description. Operating level of the storage backplate is set by R519, Operating Level.

Erase Generator

To erase the stored display, a fade-positive pulse is first applied to the storage target backplate. This pulse increases the potential difference between the flood-gun cathodes and target backplate, raising the operating level above the upper writing limit, writing the entire target areas with flood-gun electrons. Next, the backplate voltage is pulled negative, well below the retention threshold. Then, as the backplate is gradually returned, the target is charged to the rest potential and returned to the ready-to-write state. The following paragraphs describe how the erase waveform is generated.

The Erase Multivibrator is composed of Q510, Q511, and Q512, and associated circuitry. This is a monostable multivibrator with Q510 quiescently saturated and Q511 biased off. The collector of Q512 is clamped slightly above ground by the conduction of CR513. C509 is charged to the voltage difference between the junction of R508-R509 and the collector level of Q512.

When the ERASE button is pushed, the contacts of S500B are closed, grounding the junction of R501-R502. This produces a negative-going step which turns Q510 off and Q511-Q512 on. The collector of Q512 moves down very close to −12 volts as Q512 saturates and conducts through R512 and Q523. The output of the feedback amplifier steps positive, pulling the target backplate with it. This positive step increases the operating level of the crt and the entire target area is written.

When Q512 turns on, the negative step produced at its collector is also coupled through C509, which turns CR508 off, ensuring cutoff of Q510. C509 begins to discharge through R509, and after an RC-controlled period, the current through R509 has diminished sufficiently to permit the voltage at the anode of CR508 to rise above the turn-on level. The base of Q510 is also raised to the turn-on level and the multivibrator is switched back to its quiescent state.

While Q512 is conducting, the charge on C513 is removed. When Q512 turns off, its collector rises rapidly and is clamped slightly above ground by CR513. This positive-going step is coupled through C513, reverse-biasing CR516. This positive-going step is applied to the input of the feedback amplifier, causing the output to step quickly negative, well below the rest potential. As C513 charges, the voltage at the junction of R515-R516 decays at an RC rate until CR516 turns on and clamps the junction of R515-R516 at about −12.5 volts. This negative-going sawtooth voltage is applied to the feedback amplifier, which produces a positive-going sawtooth at its output to raise the backplate to the ready-to-write state.

Bootstrapping maintains operating voltage for Q525 and Q528 during the fade-positive portion of the erase waveform when the emitter of Q528 is pulled positive. The voltage drop across VR527 sets the base of Q530 approximately 51 volts below the emitter of Q528. This voltage drop is kept constant under dynamic conditions by the essentially constant current established by Q530 forward-bias voltage. When Q528 emitter is suddenly stepped positive by the erase waveform, the base of Q530 is stepped positive by the same amplitude. Q530 emitter follows the base, and the positive-going step is coupled

through C530 to raise the collector of Q528 positive by essentially the same amplitude as that at its emitter, thus maintaining a fairly constant collector-to-emitter voltage. This action reverse biases CR528, temporarily disconnecting the +100-volt supply. When the fade-positive pulse is terminated and the emitter of Q528 is pulled negative, CR529 turns off, disconnecting the bootstrap circuit, allowing the collector of Q528 to return to its +100-volt level.

Enhance Generator

Writing speed is primarily a function of the writing-gun beam current density and physical properties of the storage tube. At very fast sweep speeds, the writing beam does not charge the scanned portion of the target sufficiently to shift the target to the stored state, and the flood-gun electrons discharge the small deposited charge back down to the rest potential before the next sweep occurs.

Writing beyond the normal writing speed of the crt is attained through the process of enhancement or integration.

The Enhance Generator produces an approximate 10-millisecond, negative-going pulse, which is applied to the feedback amplifier summing point, resulting in a positive-going pulse to the target backplate. This conditions the target so that less writing-gun current is required to shift the scanned section to the stored state.

Q535, Q537, and associated circutry form a monstable multivibrator. Operation of this circuit is similar to that described for the Erase multivibrator. When the ENHANCE button is pushed in, Q535 has a conduction path to ground through R535. Q535 saturates and the low voltage level at Q535 collector keeps Q537 turned off. The negative-going portion of the enhance trigger pulse from the sweep circuit is coupled through C532 to switch the Enhance multivibrator. Q535 turns off and Q537 turns on. The collector of Q537 steps down to about −12 volts, producing a negative-going step that is coupled through C535, turning CR533 off. The time that the multivibrator remains in this state, and thus the pulse width, is determined by the values of R534 and C535. The setting of ENHANCE LEVEL control R537A determines the amplitude of the pulse that is applied to the feedback amplifier summing point.

Auto Erase

The Auto Erase circuit provides a repetitive trigger pulse to the Erase multivibrator. When the AUTO ERASE button is pushed in, a trigger is generated after each sweep. A Reset Delay multivibrator is also triggered, which resets the Time Base Single Sweep circuit.

The viewing time can be varied from approximately 1 second to approximately 5 seconds.

Auto-Erase Generator

Q545-Q548 and associated circuitry form a monostable multivibrator. Q545 is an N-channel FET that permits conduction when its gate is grounded through R542 and R537B, VIEWING TIME. Q545 is quiescently conducting and the low-voltage level at Q545 drain keeps Q548 turned off.

When the sweep ends, the negative-going pulse from the Sweep Generator is applied to Q545 gate through C540, R540, and C541. Q545 turns off and Q548 turns on. Q548 collector steps to near ground level. This negative step at Q548 collector is coupled through C548, ensuring Q545 cutoff. C548 then begins to discharge through R542 and R537B. After the time determined by the RC value of C548 and R537B, Q545 gate level recovers sufficiently to permit Q545 to turn on. At Q545 turn on, the negative-going step at Q545 drain turns Q548 off, and the multivibrator switches back to its quiescent state.

The negative-going step produced at Q545 drain is also coupled through C546 and CR550, initiating an erase cycle in the Erase Generator circuit. The stored information is therefore erased after the time period determined by the VIEWING TIME control.

The negative-going pulse at Q545 drain is also applied to the Sweep Reset Delay Multivibrator circuit.

Sweep Reset Delay Multivibrator

When the instrument is operating in the Auto Erase mode, the Sweep Reset Delay acts as a monostable multivibrator. This delay multivibrator generates a sweep reset after each erasure.

Q555, Q557, and associated circuitry form a monostable multivibrator. When the AUTO ERASE button is pushed in (in Single Sweep mode), Q577 is turned on and Q555 is turned off in the quiescent state. C555 is charged to the voltage difference between Q555 collector and R558-R559 junction. The negative-going pulse from the Auto Erase Generator is coupled through R551, C551, and CR560 to switch the Sweep Reset Multivibrator, turning Q557 off and Q555 on.

Q555 collector steps down to about −12 volts. This negative-going step is coupled through C555, turning CR557 off. After a time determined by R559 and C555 (C555 charges through R559), CR557 anode rises above its cathode, turning Q557 on and Q555 off. When Q555

turns off, the positive step at Q555 collector is coupled through C554 to reset the Sweep Generator.

The Q555 "on" time is the sweep reset delay time.

Integrate

In the Integrate mode the flood-gun beam is interrupted by pressing the INTEGRATE button (S565) momentarily, permitting the writing-gun beam to sum small amounts of charge for successive sweeps. These areas of accumulated charge shift to the stored state when the flood electrons are turned on again (INTEGRATE button released).

Pressing the INTEGRATE button also connects about −90 volts to the high-voltage regulator HV Compensation input. This −90 volts, through R722B, shifts the high-voltage level slightly, correcting for the deflection-sensitivity changes that occur when the flood guns are turned off.

POWER SUPPLY 8

General

Fig. 3-12 is a block diagram of the power supply circuitry. The Power Supply provides input voltage source selection, dc-to-dc converter, series regulator, current protection, automatic turn off, and the low line indicator.

AC Power Input

Power is applied to the primary of transformer T600 through Line Fuse F600; POWER switch S600; Line-Voltage selector switch S601; and the Regulating Range

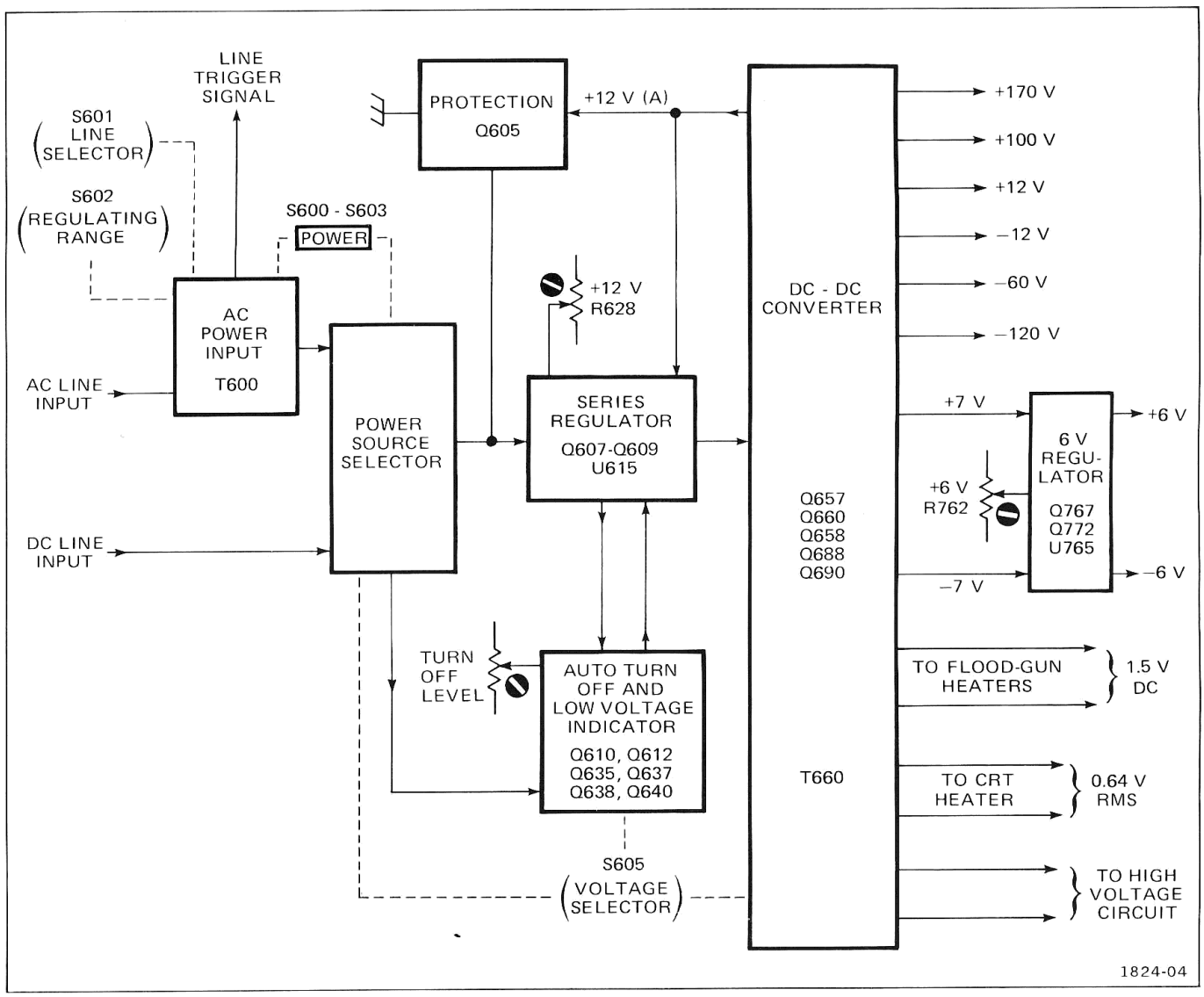

Fig. 3-12. Power Supply block diagram.

selector switch, S602. The Line-Voltage selector, S601, connects the split primaries of T600 in parallel for 115-volt operation and in series for 230-volt operation.

The Line Fuse, F600, should be of the proper value for each nominal line voltage to protect the instrument. Fuses are internally accessible. Procedures for fuse replacement and cabinet removal may be found in the Maintenance section of this manual. Refer fuse replacement to qualified service personnel only. See Electrical Parts List for correct fuse values.

Power Source Selector

The Power Source selector switch, S605, selects one of three sources: 115/230-V ac, +12-V dc, or +24-V dc. The regulating ranges (HI-LO-MED) of these voltages are listed on the rear cover of the instrument.

Series Regulator

The Series Regulator circuit regulates the output of the dc-to-dc Converter circuit.

U615, Q607, and Q609 and associated circuitry make up the series regulator circuit. U615 includes a comparator amplifier and a reference voltage output. Q609 serves as a regulating device. R627, R628, and R629 form the output voltage monitoring system.

The voltage from R628 (voltage-monitor output) is applied to one input (pin 2) of U615. The other comparator input (pin 3) receives a reference voltage from pin 4 of U615 through R626. The monitoring voltage is compared to the reference voltage, and any error voltage is amplified in U615. The amplified error voltage (at pin 7 of U615) drives Q607 and Q609. This drive from pin 7 of U615 controls Q607 impedance, holding the dc-to-dc converter output voltage constant. R628, +12 V Adjust, sets the converter output level.

DC-to-DC Converter

The converter multivibrator (Q657, Q660, Q658 and T665) converts the dc supply voltage (from Q607) to ac. This ac is applied to T600 primary. T600 secondary voltages are rectified to provide dc operating voltages for the instrument.

The voltage at +12(A) provides the dc voltage to the comparison divider R627, R628, and R629.

Regulator Protection

If the input voltage to the Series Regulator circuit rises above about +40 volts, Q605 (SCR) turns on and is held in the on state. When Q605 conducts, the input to the Series Regulator is short circuited to ground through R602. The large current drawn by R602 opens the line fuse.

Auto Turn Off

When the input level of the Series Regulator falls below the specified levels (about +20.5 volts in the 115/230-volt ac and the +24 V dc positions of Power Source selector switch S605 or about +10.75 volts in the +12 V dc position), Q612 and Q610 turn on. Q607, through Q609 and U615, turns off, preventing the operation of the dc-to-dc converter.

Low-Line Indicator

When the input level of the Series Regulator falls below the specified levels (about +22 volts in the 115/230 V ac and +24 V dc position of Power Source selector switch S605, or about +11 volts in the +12 V dc position), Q635 turns on. The reference for Q635 and Q637 bases is pin 4 of U615. When Q635 turns on, astable multivibrator Q638-Q640 runs at about two hertz, causing low-line indicator to blink.

+6 V and −6 V Regulators ◇9

The +12-volt supply and VR760 provide the reference voltage for the +6-volt regulator. R762 adjusts the output to 6 volts. U765 is the regulator and Q767 the pass transistor.

U765B is the regulator for the −6-volt supply, with the +6-volt supply providing the reference voltage. Q772 is the −6-volt pass transistor.

HV AND UNBLANKING ◇10

General

This circuit provides the high voltage and control circuitry for crt operation. Fig. 3-13 is a block diagram of the circuit.

High Voltage and CRT

Multiples of T660 secondary voltage are obtained between CR692A cathode and CR692F anode. CR692E (cathode) is connected to one end of the voltage divider network, R697 through R707. The R707 end of the divider connects to CR692F anode, providing operating voltage for Q700. This divider network also provides voltages for the Intensity and Focus controls and the crt writing-gun cathode. Any change in the writing-gun cathode level is fed back to a series regulator circuit (Q710, Q712, and Q717) through feedback resistor R712. This series regulator circuit amplifies and inverts the error signal. The

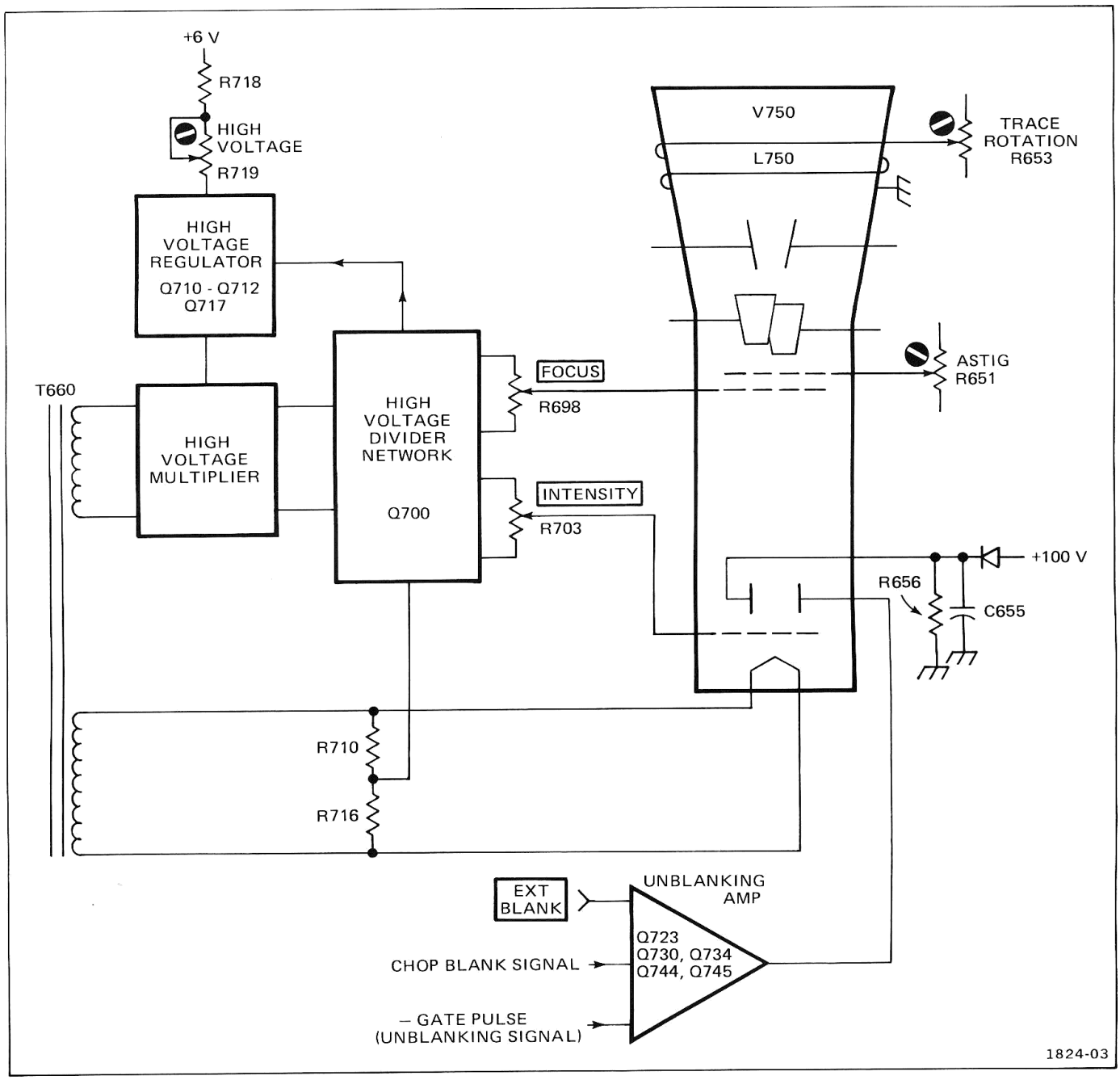

Fig. 3-13. CRT and H V block diagram.

amplified and inverted signal is applied to CR692F anode (via transformer winding and high-voltage multiplier) thus holding the writing-gun cathode level constant.

R719 sets the writing-gun cathode level at −1900 volts in the non-store mode.

Difference in crt sensitivity between store and non-store modes are compensated by R721, High Voltage Compensation.

The Intensity Limit control, R702, sets the minimum difference voltage that can exist between the crt control grid and cathode, thus preventing excessive crt cathode current. For SN 300200 and up, an additional control, R706, provides a second Intensity Limit adjustment to prevent excessive crt cathode current at sweep speeds of 10 ms and slower.

Focus Control R698 in combination with R651 (Astig) determines trace sharpness. Only the Focus control is used during routine operation, and provides a sharp trace

at any intensity setting, once the Astig control has been set.

Geometry Control R575 adjusts for minimum bowing of horizontal and vertical traces within the graticule area.

Trace Rotation control R563 sets the current in the Trace Rotation coil, creating a magnetic field through which the crt electron beam passes. This current permits the horizontal trace to follow a path parallel to the horizontal graticule lines.

Blanking and Unblanking

Signals for unblanking come from one of three sources: Sweep output (U430, pin 15, −Gate), the vertical switching circuit (chopped mode), or the EXT BLANK connector on the rear panel.

The Unblanking amplifier (consisting of Q723, Q730, Q734, Q744, Q745, and associated circuitry) provides crt beam blanking during sweep retrace and during switching interval in chopped mode.

C655-R656 hold the undriven blanking plate at a higher potential than that of the driven plate for a brief period after oscilloscope turn off. This voltage blanks the crt beam until the high voltage power supply discharges and the crt heater cools.

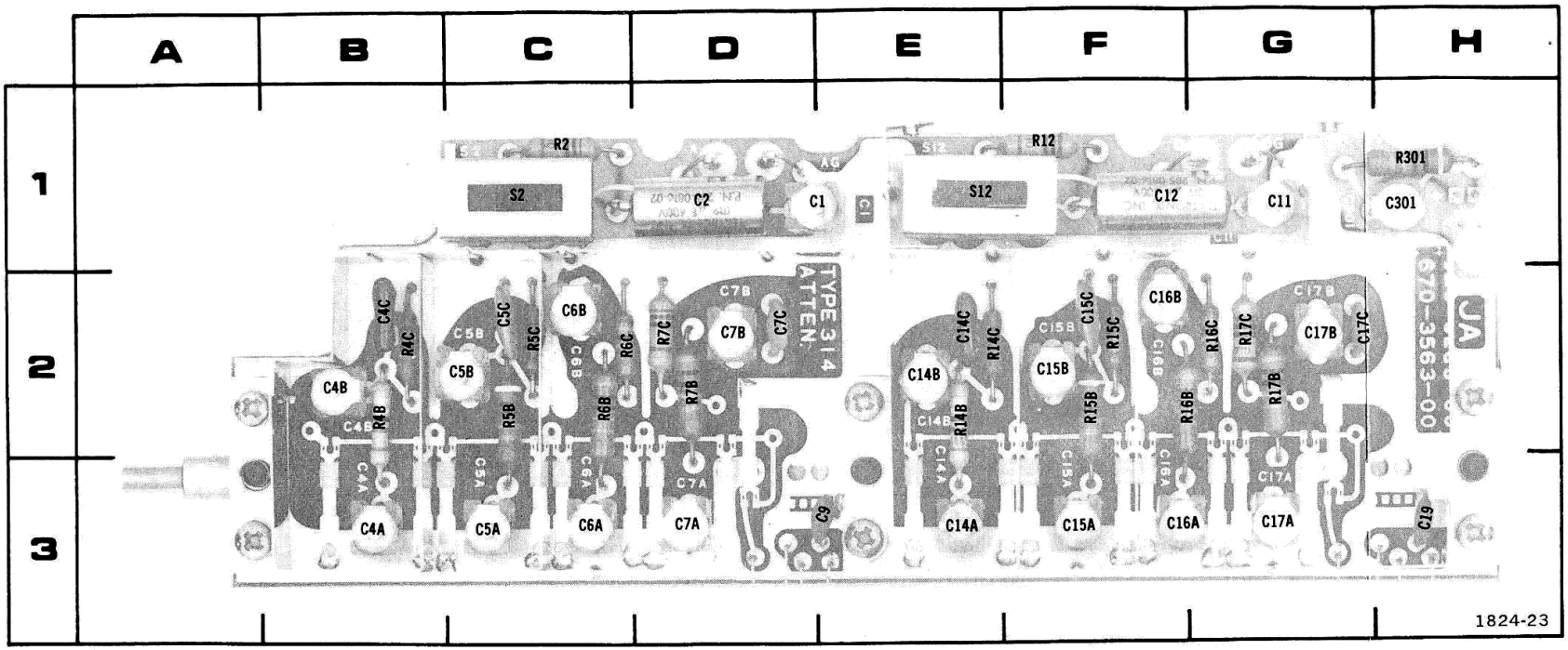

Figure 7-7. A1—Attenuator circuit board.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C1	1D	C11	1G	C301	1H	R15B	2F
C2	1D	C12	1F			R15C	2F
C4A	3B	C14A	3E	R2	1C	R16B	2F
C4B	2B	C14B	2E	R4B	2B	R16C	2G
C4C	2B	C14C	2E	R4C	2B	R17B	2G
C5A	3C	C15A	3F	R5B	2C	R17C	2G
C5B	2C	C15B	2F	R5C	2C	R301	1H
C5C	2C	C15C	2F	R6B	2C		
C6A	3C	C16A	3F	R6C	2C	S2	1C
C6B	2C	C16B	2F	R7B	2D	S12	1E
C7A	3D	C17A	3G	R7C	2D		
C7B	2D	C17B	2G	R12	1F		
C7C	2D	C17C	2G	R14B	2E		
C9	3E	C19	3H	R14C	2E		

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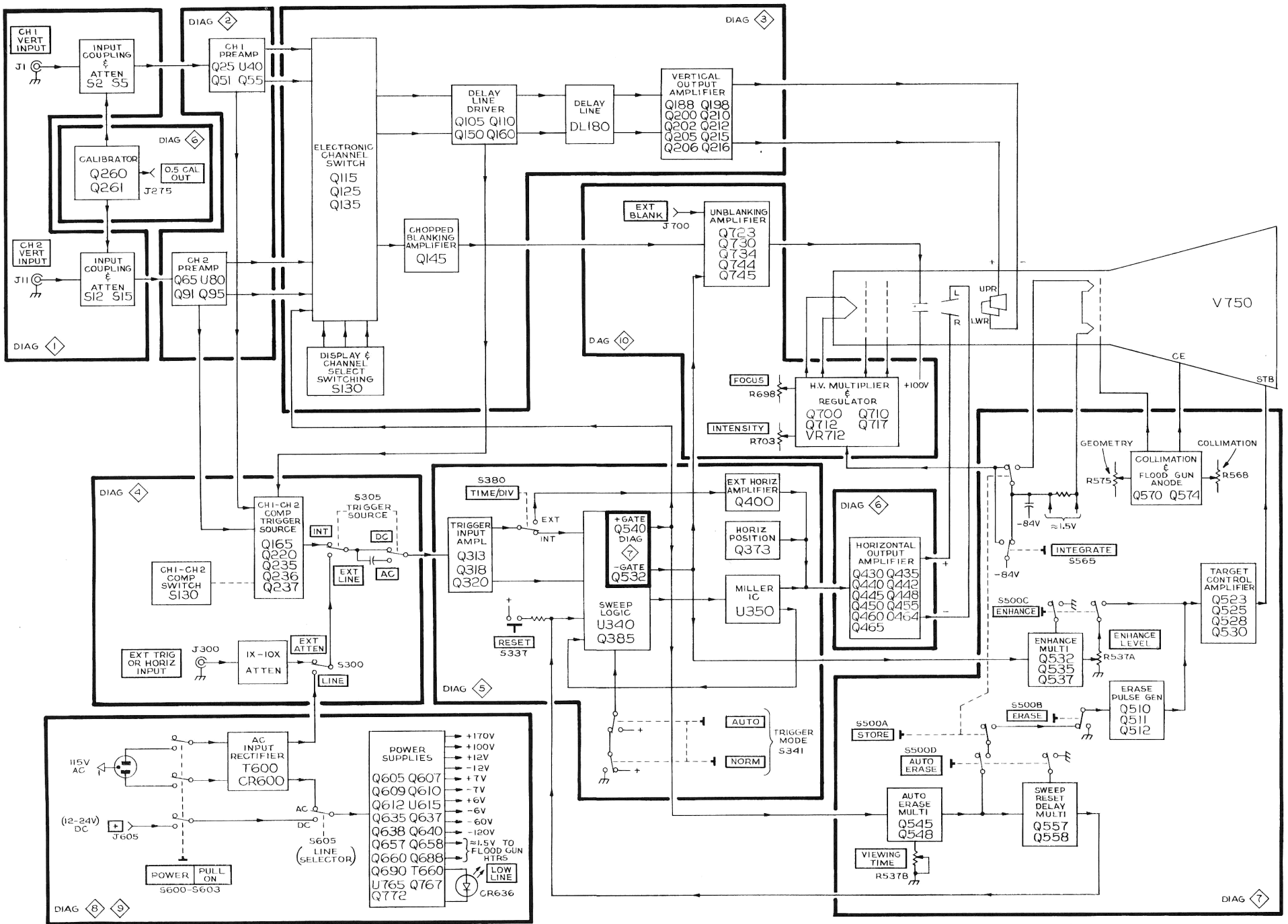

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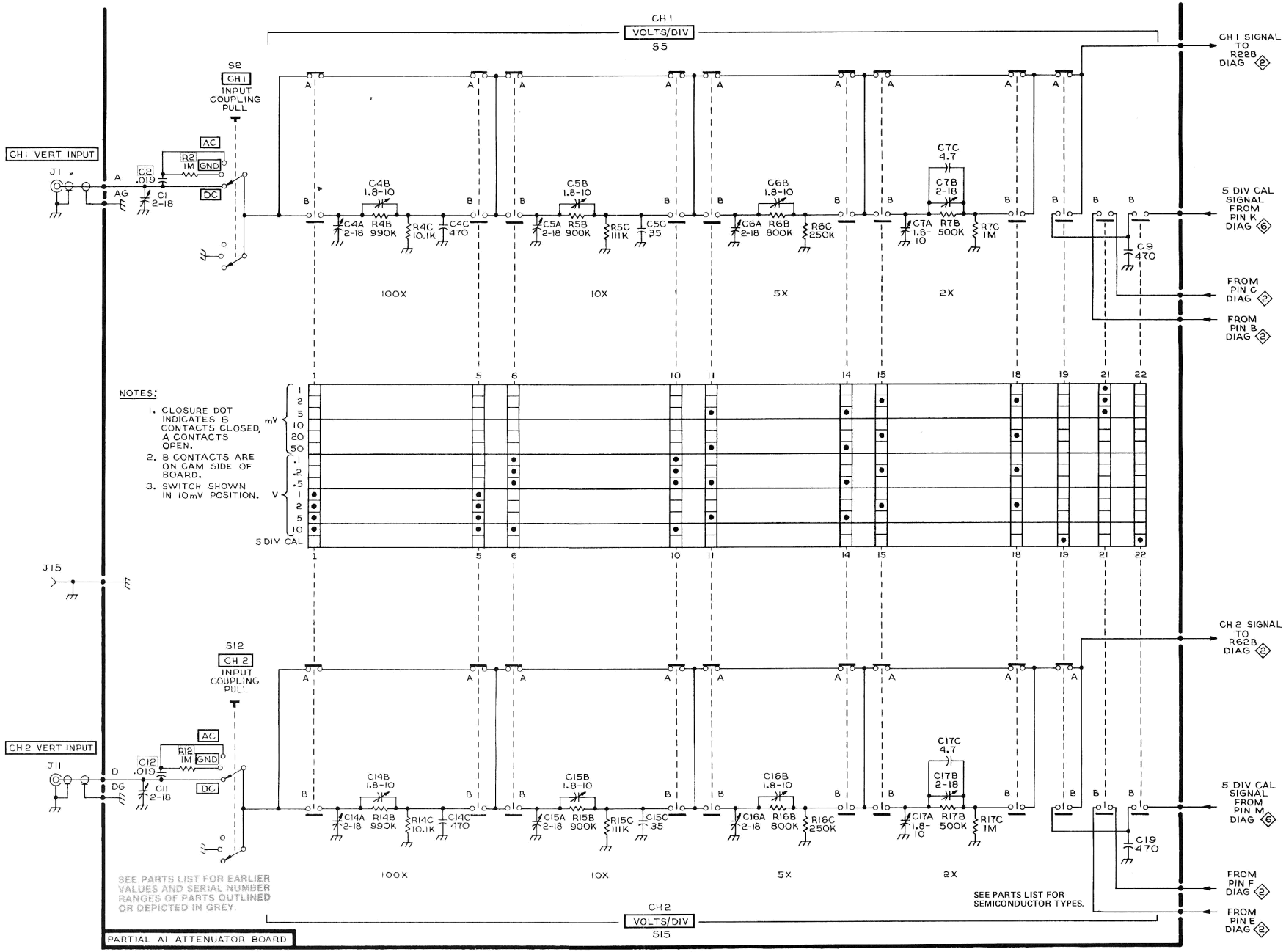
BLOCK DIAGRAM



1824-55
REV. B, AUG 1977

CH 1 & CH 2 ATTENUATOR 1

PS 8-74

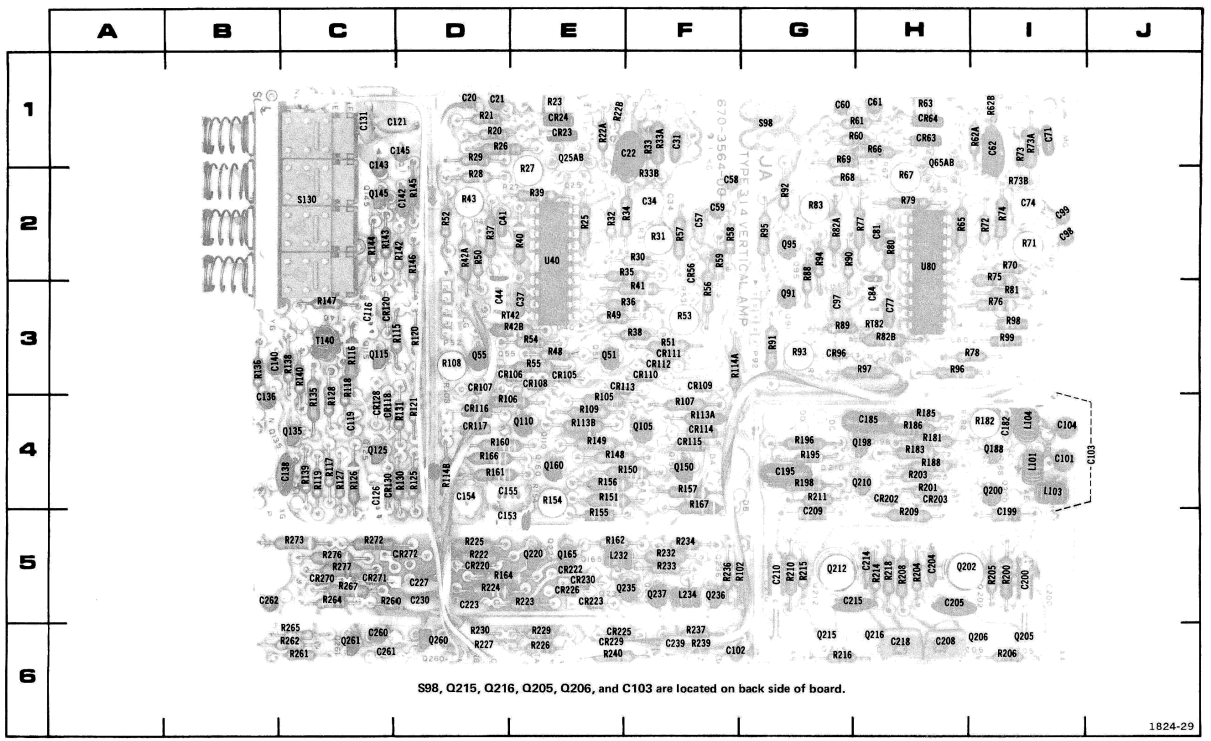
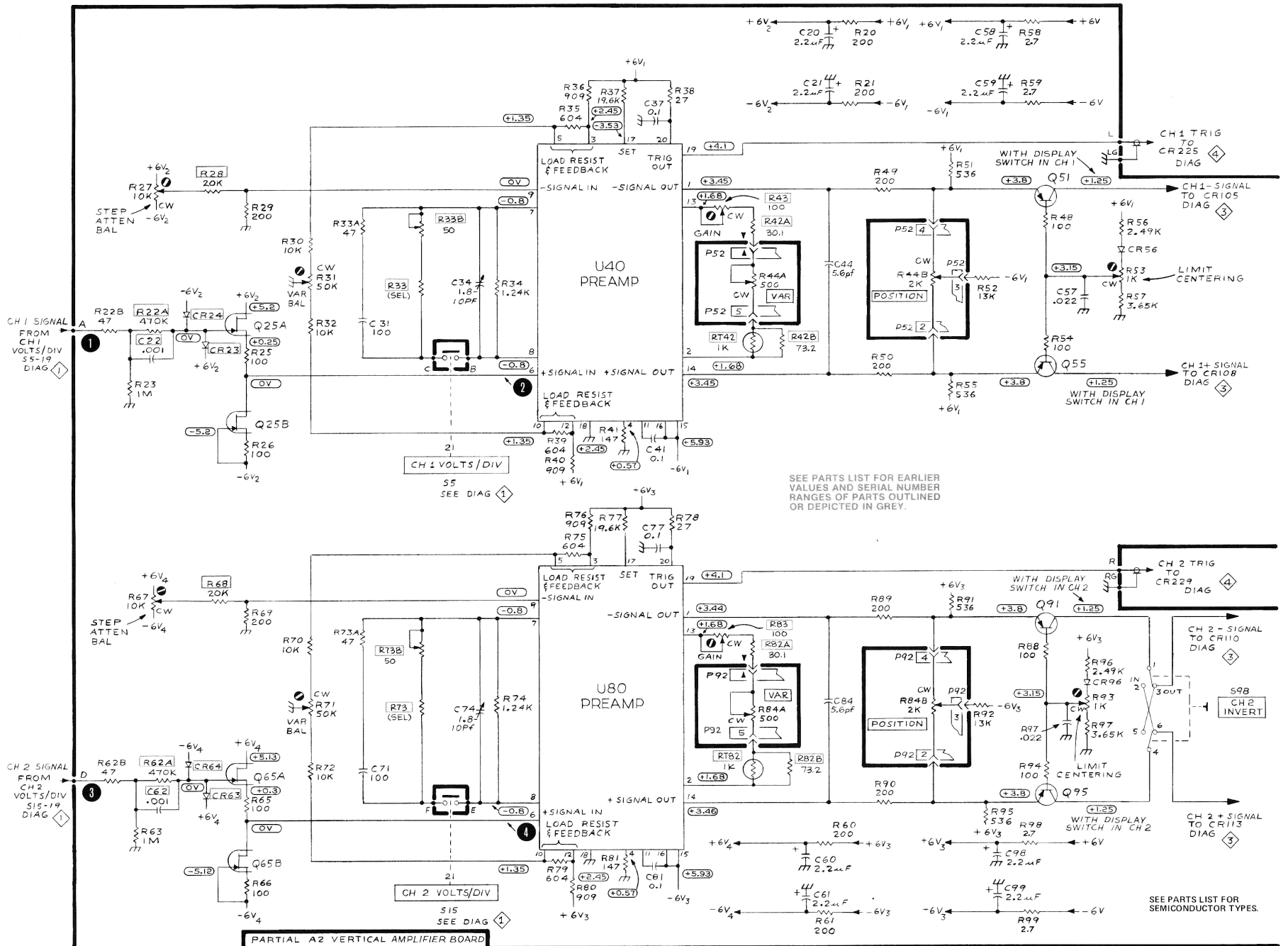
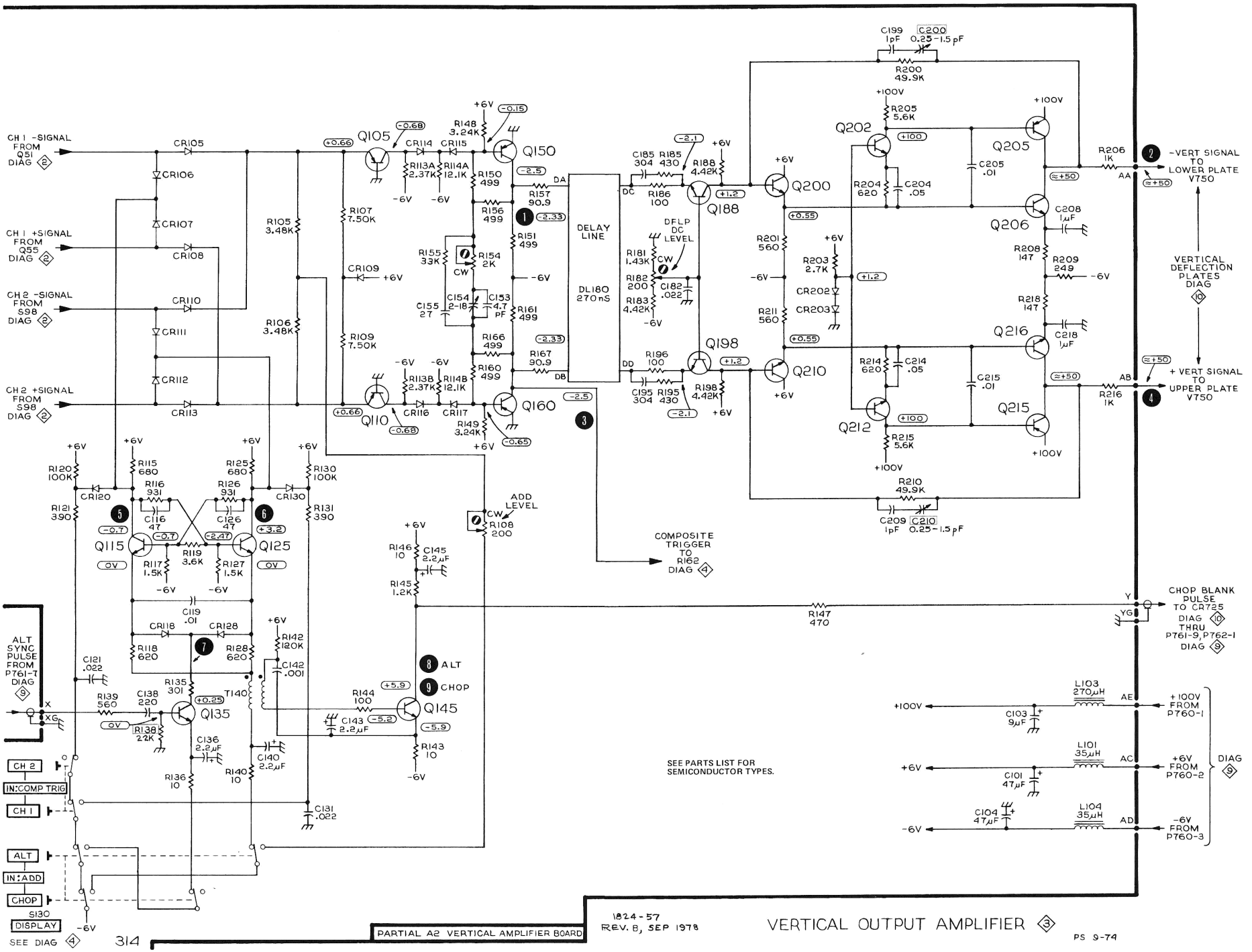


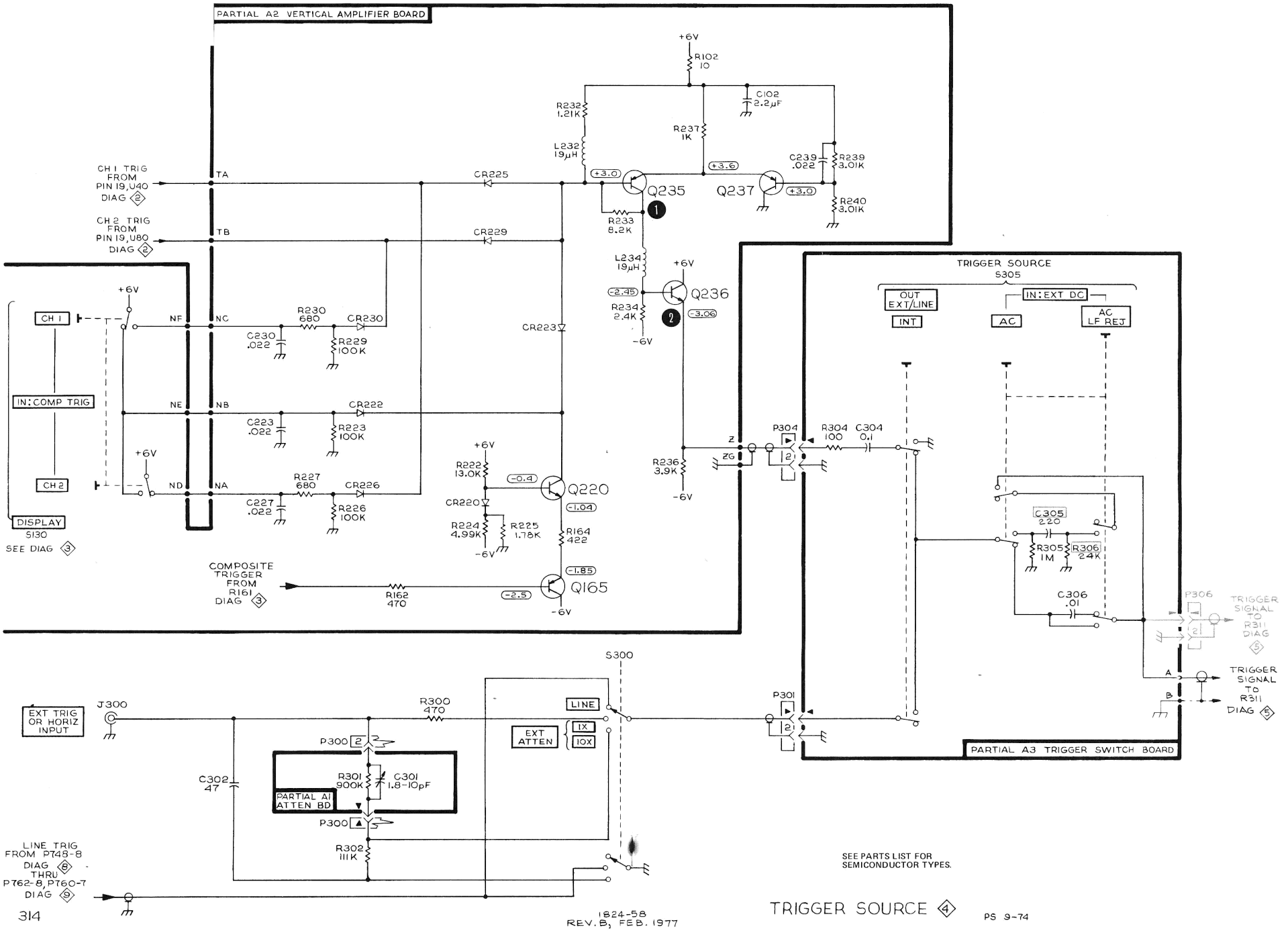
Figure 7-8. A2—Vertical Amplifier circuit board.

*See Parts List for serial number ranges.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C20	1D	C204	5H	CR226	5E	R20	1D	R67	2H	R119	4C	R203	4H
C21	1D	C205	5H	CR229	6E	R21	1D	R68	2G	R120	3D	R204	5H
C22	1F	C208	6H	CR230	5E	R22A	1E	R69	1G	R121	4D	R205	5I
C31	1F	C209	5G	CR270	5C	R22B	1E	R70	2I	R125	4D	R206	6I
C34	2F	C210	5G	CR271	5C	R23	1E	R71	2I	R126	4C	R208	5H
C37	3E	C214	5H	CR272	5D	R25	2E	R72	2I	R127	4C	R209	5H
C41	2D	C215	5G			R26	1D	R73	1I	R128	4C	R210	5G
C44	3D	C218	6H	L101	4I	R27	2E	R73A	1I	R130	4D	R211	4G
C57	2F	C223	5D	L103	4I	R28	2D	R73B*	2I	R131	4D	R214	5H
C58	2F	C227	5D	L104	4I	R29	1D	R74	2I	R135	4C	R215	5G
C59	2F	C230	5D	L232	5E	R30	2F	R75	2I	R136	3B	R216	6G
C60	1G	C239	6F	L234	5F	R31	2F	R76	3I	R138	3C	R218	5H
C61	1H	C260	6C			R32	2E	R77	2H	R139	4C	R222	5D
C62	1I	C261	6C	Q25AB	1E	R33	1F	R78	3H	R140	3C	R223	5E
C71	1I	C262	5B	Q51	3E	R33A	1F	R79	2H	R142	2D	R224	5D
C74	2I			Q55	3D	R33B*	2F	R80	2H	R143	2C	R225	5D
C77	3H	CR23	1E	Q65AB	1H	R34	2E	R81	3I	R144	2C	R226	6E
C81	2H	CR24	1E	Q91	3G	R35	2E	R82A	2G	R145	2D	R227	6D
C84	3H	CR56	2F	Q95	2G	R36	3E	R82B	3H	R146	2D	R229	6E
C97	3G	CR63	1H	Q105	4F	R37	2D	R83	2G	R147	3C	R230	6D
C98	2I	CR64	1H	Q110	4E	R38	3F	R88	2G	R148	4E	R232	5F
C99	2I	CR96	3G	Q115	3C	R39	2E	R89	3G	R149	4E	R233	5F
C101	4I	CR105	3E	Q125	4C	R40	2E	R90	2G	R150	4E	R234	5F
C102	6F	CR106	3D	Q135	4C	R41	3F	R91	3G	R151	4E	R236	5F
C103	4J	CR107	3D	Q145	2C	R42A	2D	R92	2G	R154	4E	R237	6F
C104	4I	CR108	3E	Q150	4F	R42B	3E	R93	3G	R155	5E	R239	6F
C116	3C	CR109	3F	Q160	4E	R43	2D	R94	2G	R156	4E	R240	6E
C119	4C	CR110	3F	Q165	5E	R48	3E	R95	2G	R157	4F	R260	5C
C121	1D	CR111	3F	Q188	4I	R49	3E	R96	3H	R160	4D	R261	6C
C126	4C	CR112	3F	Q198	4H	R50	2D	R97	3H	R161	4D	R262	6C
C131	1C	CR113	3E	Q200	4I	R51	3F	R98	3I	R162	5E	R264	5C
C136	4B	CR114	4F	Q202	5H	R52	2D	R99	3I	R164	5D	R265	6C
C138	4C	CR115	4F	Q205	6I	R53	3F	R102	5G	R166	4D	R267	5C
C140	3B	CR116	4D	Q206	6I	R54	3E	R105	4E	R167	4F	R272	5C
C142	2D	CR117	4D	Q210	4H	R55	3E	R106	4D	R181	4H	R273	5C
C143	1C	CR118	4C	Q212	5G	R56	3F	R107	4F	R182	4I	R276	5C
C145	1D	CR120	3C	Q215	6G	R57	2F	R108	3D	R183	4H	R277	5C
C153	5D	CR128	4C	Q216	6H	R58	2F	R109	4E	R185	4H	RT42*	3E
C154	4D	CR130	4C	Q220	5E	R59	2F	R113A	4F	R186	4H	RT82*	3H
C155	4D	CR202	4H	Q235	5F	R60	1H	R113B	4E	R188	4H		
C182	4I	CR203	4H	Q236	5F	R61	1H	R114A	3F	R195	4G	S98	1G
C185	4H	CR220	5D	Q237	5F	R62A	1I	R114B	4D	R196	4G	S130	2C
C195	4G	CR222	5E	Q260	6D	R62B	1I	R115	3D	R198	4G	T140	3C
C199	5I	CR223	5E	Q261	6C	R63	1H	R116	3C	R200	5I	U40	2E
C200	5I	CR225	6E			R65	2H	R117	4C	R201	4H	U80	2H
						R66	1H	R118	4C				


U40 PREAMP
U80 PREAMP
CH 1 SIGNAL FROM CH1 VOLTS/DIV S5-19 DIAG 1
CH 2 SIGNAL FROM CH2 VOLTS/DIV S15-19 DIAG 1
STEP ATTEN BAL
VAR BAL
GAIN
POSITION
LOAD RESIST & FEEDBACK
SET TRIG OUT
-SIGNAL IN
-SIGNAL OUT
+SIGNAL IN
+SIGNAL OUT
CH 1 VOLTS/DIV S5 SEE DIAG 1
CH 2 VOLTS/DIV S15 SEE DIAG 1
CH 1 TRIG TO CR225 DIAG 4
CH 2 TRIG TO CR229 DIAG 4
WITH DISPLAY SWITCH IN CH 1
WITH DISPLAY SWITCH IN CH 2
CH1- SIGNAL TO CR105 DIAG 3
CH1+ SIGNAL TO CR108 DIAG 3
CH 2 - SIGNAL TO CR110 DIAG 3
CH 2 + SIGNAL TO CR113 DIAG 3
LIMIT CENTERING
CH 2 INVERT
S98
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
PARTIAL A2 VERTICAL AMPLIFIER BOARD


CH 1 -SIGNAL FROM Q51 DIAG 2
CH 1 +SIGNAL FROM Q55 DIAG 2
CH 2 -SIGNAL FROM S98 DIAG 2
CH 2 +SIGNAL FROM S98 DIAG 2
CR105
CR106
CR107
CR108
CR109
CR110
CR111
CR112
CR113
Q105
Q110
Q150
Q160
DELAY LINE
DL180 270nS
Q188
Q198
Q200
Q210
Q202
Q212
Q205
Q215
Q206
Q216
-VERT SIGNAL TO LOWER PLATE V750
+ VERT SIGNAL TO UPPER PLATE V750
VERTICAL DEFLECTION PLATES DIAG 10
COMPOSITE TRIGGER TO R162 DIAG 4
ADD LEVEL
DFLP DC LEVEL
CHOP BLANK PULSE TO CR725 DIAG 10 THRU P761-9, P762-1 DIAG 9
ALT SYNC PULSE FROM P761-7 DIAG 9
Q115
Q125
Q135
Q145
T140
CH 2
IN:COMP TRIG
CH 1
ALT
IN:ADD
CHOP
S130
DISPLAY
SEE DIAG 4
+100V FROM P760-1
+6V FROM P760-2
-6V FROM P760-3
DIAG 9
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
PARTIAL A2 VERTICAL AMPLIFIER BOARD
1824-57
REV. B, SEP 1978
VERTICAL OUTPUT AMPLIFIER 3
PS 9-74
314



SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

TRIGGER SOURCE 4

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1824-58
REV. B, FEB. 1977

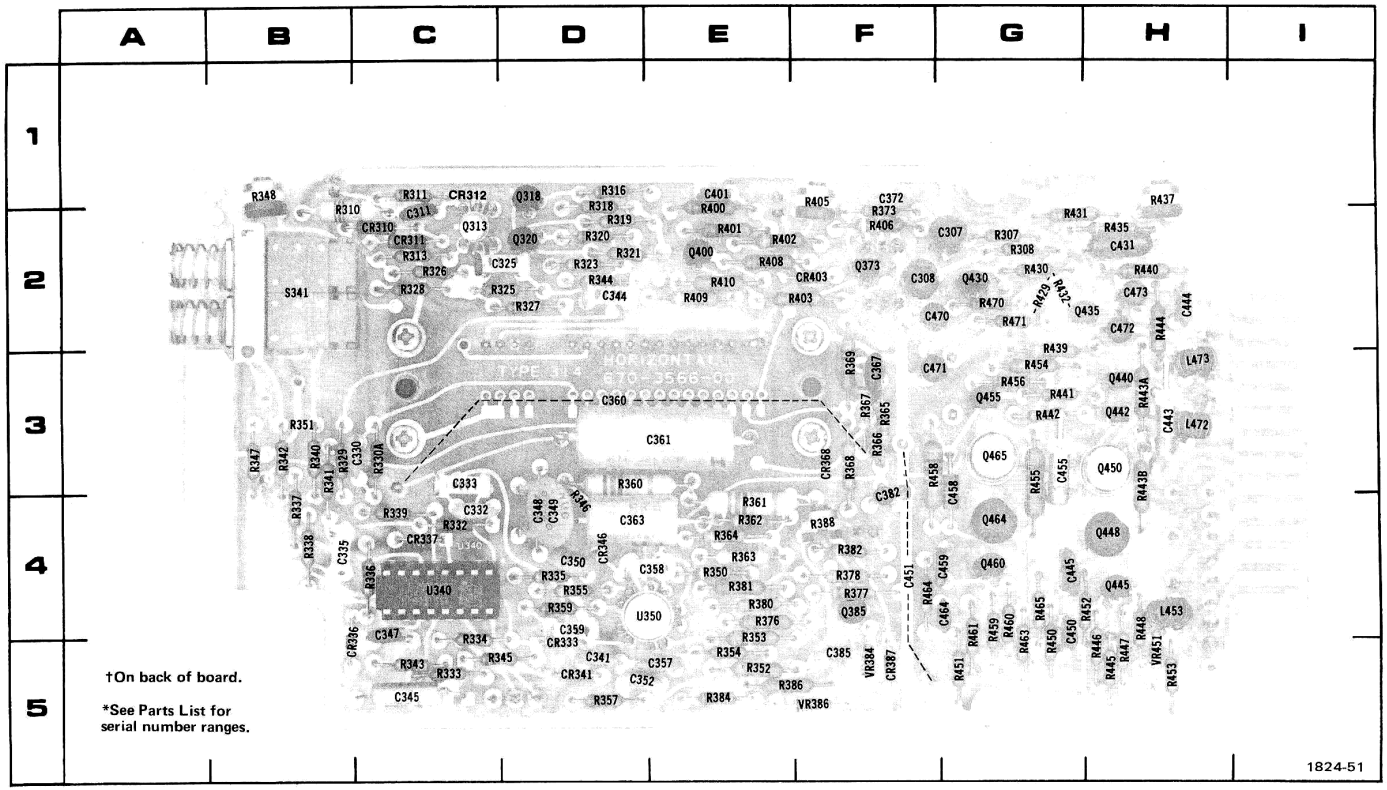
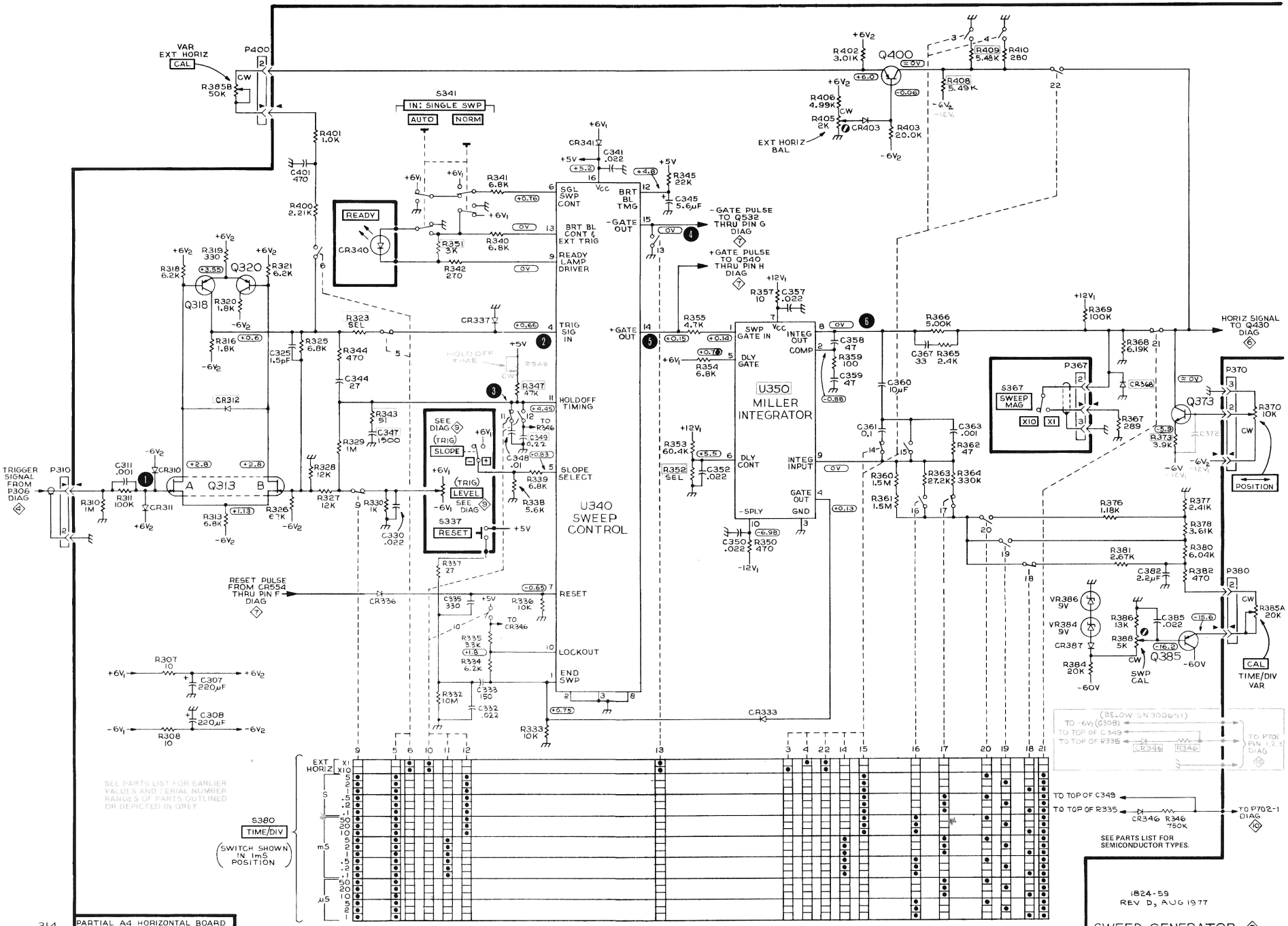
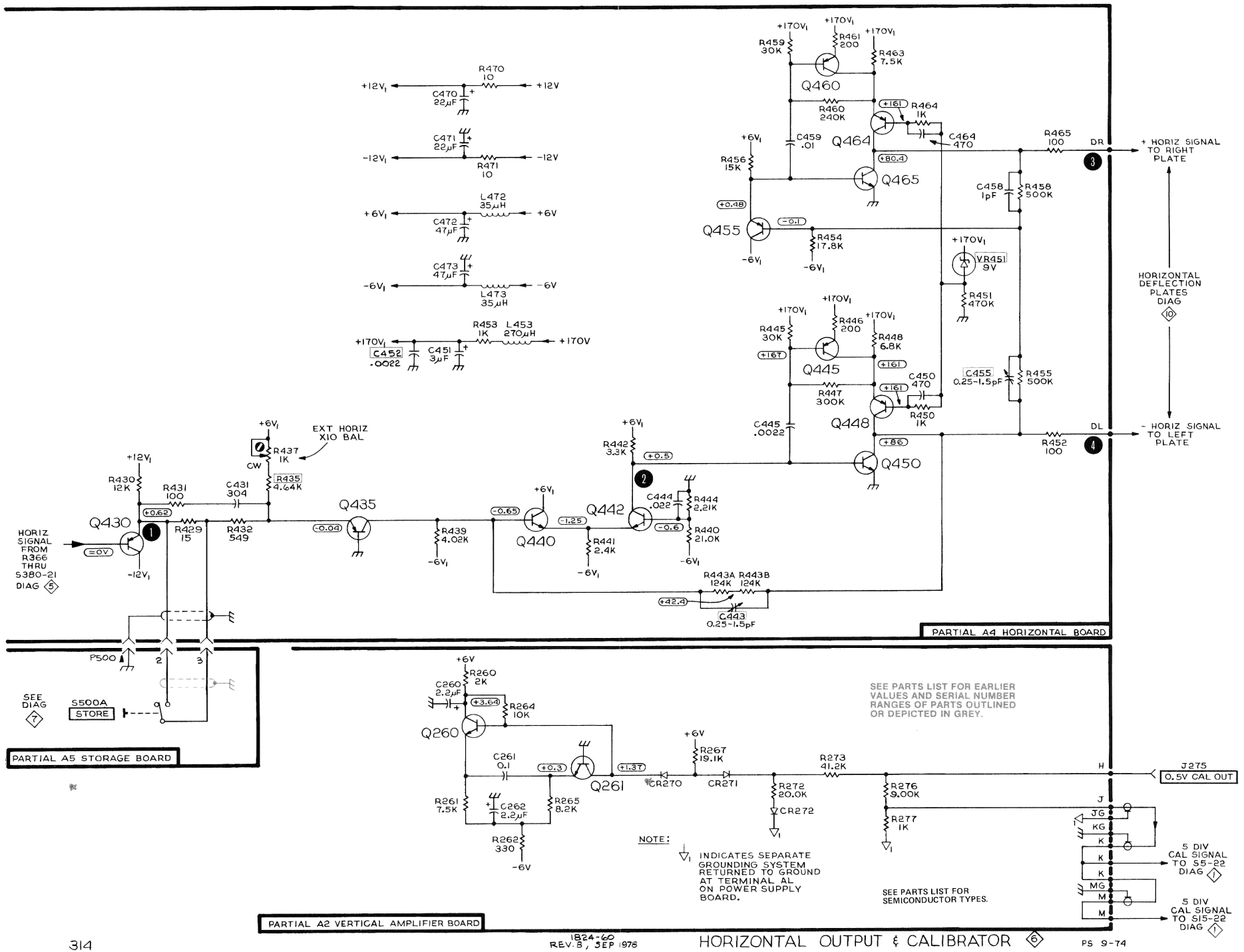


Figure 7-10. A4—Horizontal circuit board.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C307	2G	C360†	3D	C471	3F	Q320	2D	R311	1C	R337	4B	R361	4E	R400	2E	R443A	3H	R464	4F
C308	2F	C361	3E	C472	2H	Q373	2F	R313	2C	R338	4B	R362	4E	R401	2E	R443B	3H	R465	4G
C311	2C	C363	4D	C473	2H	Q385	4F	R316	1D	R339	4C	R363	4E	R402	2E	R444	2H	R470	2G
C325	2D	C367	3F			Q400	2E	R318	1D	R340	3B	R364	4E	R403	2F	R445	5H	R471	2G
C330	3C	C372*	1F	CR310	2C	Q430	2G	R319	2D	R341	3B	R365	3F	R405	1F	R446	5H		
C332	4C	C382	4F	CR311	2C	Q435	2H	R320	2D	R342	3B	R366	3F	R406	2F	R447	5H	S341	2B
C333	3C	C385	5F	CR312*†	1C	Q440	3H	R321	2D	R343	5C	R367	3F	R408	2E	R448	4H		
C335	4B	C401	1E	CR333	5D	Q442	3H	R323	2D	R344	2D	R368	3F	R409	2E	R450	5G	U340	4C
C341	5D	C431	2H	CR336	5B	Q445	4H	R325	2D	R345	5C	R369	3F	R410	2E	R451	5G	U350	4E
C344	2D	C443	3H	CR337	4C	Q448	4H	R326	2C	R346*	4D	R373	2F	R429†	2G	R452	4H		
C345	5C	C444	2H	CR341	5D	Q450	3H	R327	3D	R347	3B	R376	4E	R430	2G	R453	5H	VR384	5F
C347	4C	C445	4G	CR346*	4D	Q455	3G	R328	2C	R348	1B	R377	4F	R431	2G	R454	3G	VR386	5F
C348	4D	C450	5G	CR368*	3F	Q560	4G	R329	3B	R350	4E	R378	4F	R432†	2G	R455	3G	VR451	5H
C349	4D	C451†	4F	CR387	5F	Q464	4G	R330A	3C	R351*	3B	R380	4E	R435	2H	R456	3G		
C350	4D	C455	3G	CR403	2F	Q465	3G	R332	4C	R352	5E	R381	4E	R437	1H	R458	3F		
C352	5D	C458	4G					R333	5C	R353	4E	R382	4F	R439	2G	R459	4G		
C357	5E	C459	4G	L453	4H	R307	2G	R334	5C	R354	5E	R384	5E	R440	2H	R460	4G		
C358	4E	C464	4G	L472	3H	R308	2G	R335	4D	R355	4D	R386	5E	R441	3G	R461	4G		
C359	4D	C470	2F	L473	3H	R310	2B	R336	4C	R357	5D	R388	4F	R442	3G	R463	5G		
										R359	4D								
				Q313	2C					R360	3D								
				Q318	1D														



SWEEP GENERATOR ⑤



1824-60
REV. B, SEP 1978

HORIZONTAL OUTPUT & CALIBRATOR 6

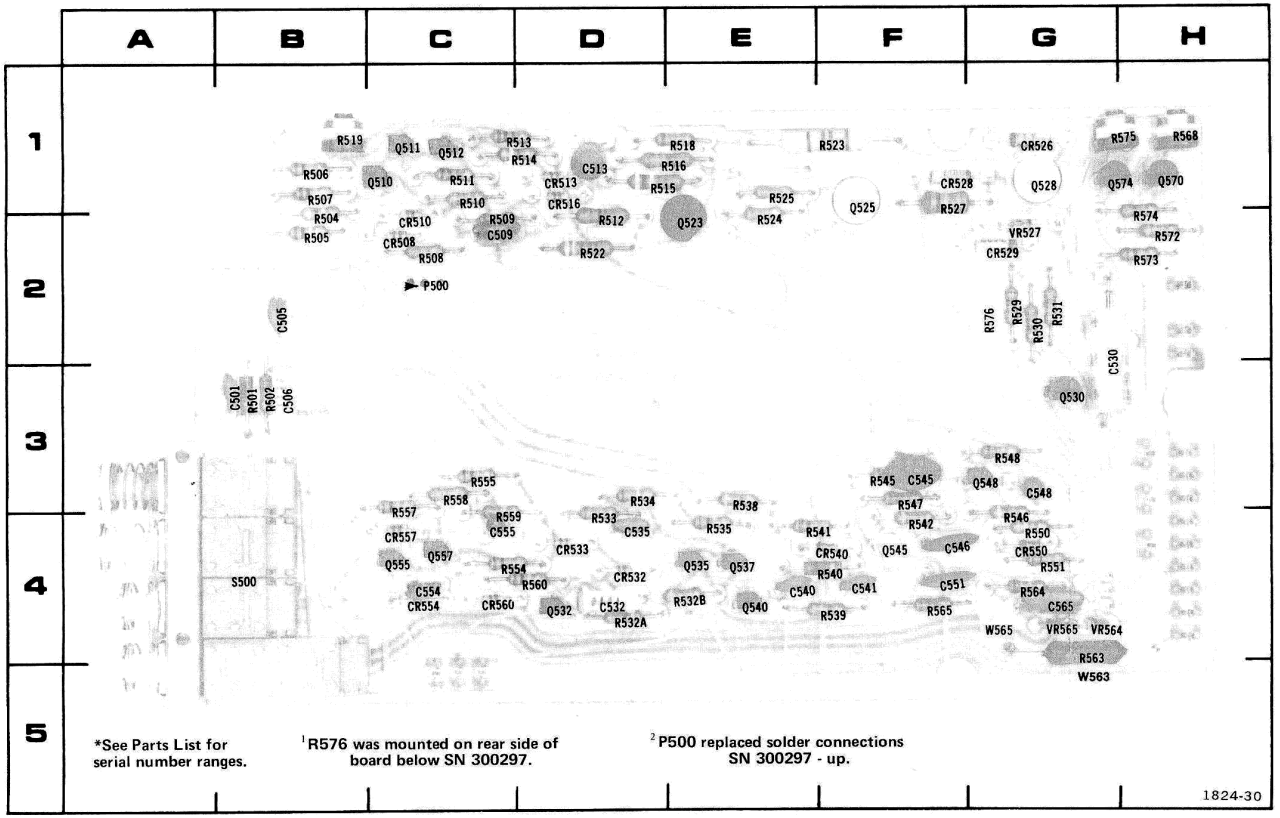
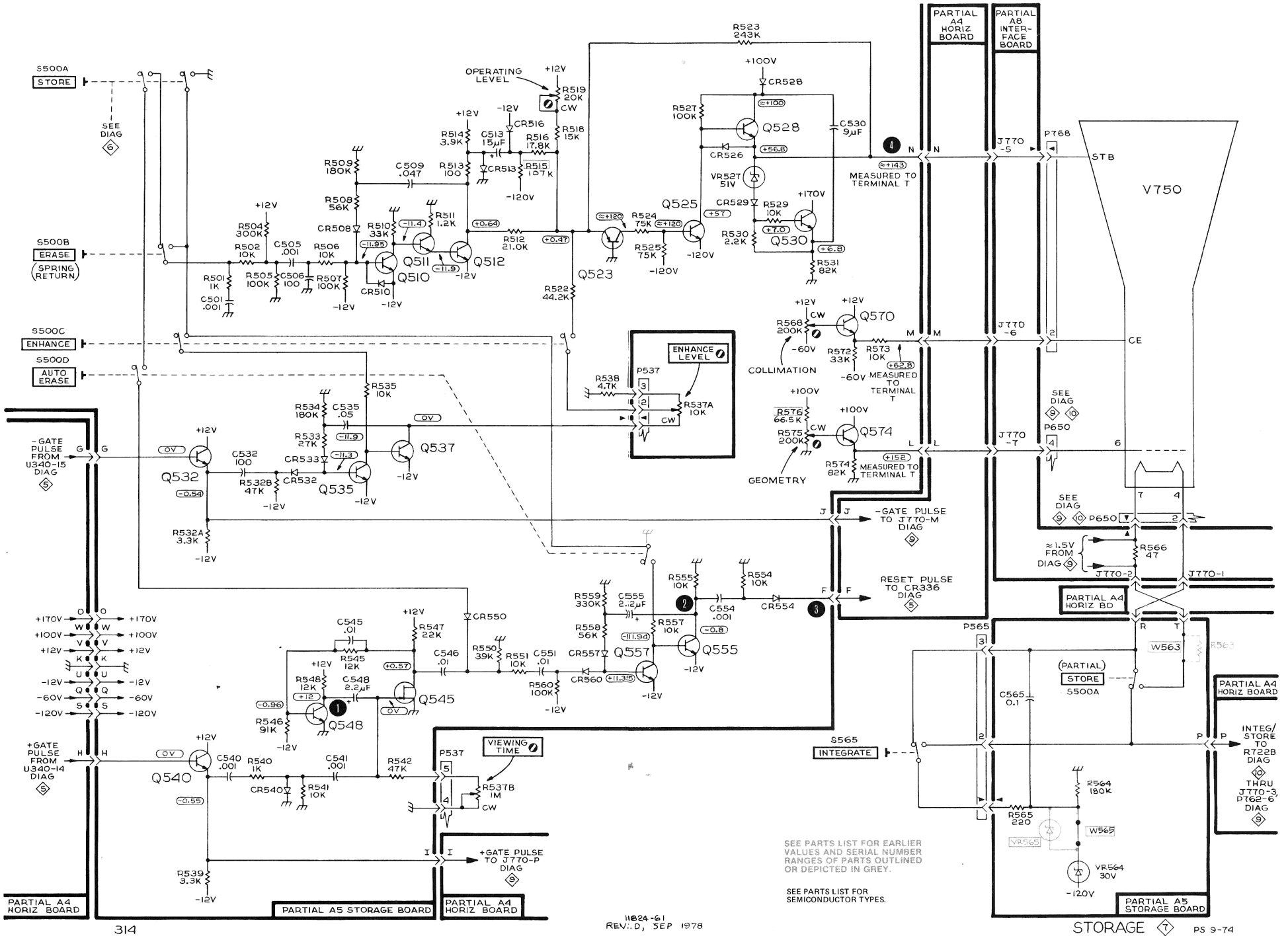


Figure 7-11. A5—Storage circuit board.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C501	3B	C551	4F	CR533	4D	Q530	3G	R502	3B	R516	1E	R533	4D	R551	4G	R574	2H
C505	2B	C554	4C	CR540	4F	Q532	4D	R504	2B	R518	1E	R534	3D	R554	4C	R575	1H
C506	3B	C555	4C	CR550	4G	Q535	4E	R505	2B	R519	1B	R535	4E	R555	3C	R576[1]	2G
C509	2C	C565	4G	CR554	4C	Q537	4E	R506	1B	R522	2D	R538	3E	R557	4C		
C513	1D			CR557	4C	Q540	4E	R507	1B	R523	1F	R539	4F	R558	3C	S500	4B
C530	3G	CR508	2C	CR560	4C	Q545	4F	R508	2C	R524	2E	R540	4F	R559	4C		
C532	4D	CR510	2C	P500[2]	2C	Q548	3G	R509	2C	R525	1E	R541	4F	R560	4D	VR527	2G
C535	4D	CR513	1D	Q510	1C	Q555	4C	R510	1C	R527	2F	R542	4F	R563*	5G	VR564	4G
C540	4E	CR516	1D	Q511	1C	Q557	4C	R511	1C	R529	2G	R545	3F	R564	4G	VR565*	4G
C541	4F	CR526	1G	Q512	1C	Q570	1H	R512	2D	R530	2G	R546	4G	R565	4F		
C545	3F	CR528	1F	Q523	2E	Q574	1H	R513	1D	R531	2G	R547	3F	R568	1H	W563*	5G
C546	4F	CR529	2G	Q525	1F			R514	1D	R532A	4D	R548	3G	R572	2H	W565*	4E
C548	3G	CR532	4D	Q528	1G	R501	3B	R515	1D	R532B	4E	R550	4G	R573	2H		


S500A STORE
SEE DIAG 6
S500B ERASE (SPRING RETURN)
S500C ENHANCE
S500D AUTO ERASE
OPERATING LEVEL
ENHANCE LEVEL
COLLIMATION
GEOMETRY
VIEWING TIME
MEASURED TO TERMINAL T
-GATE PULSE FROM U340-15 DIAG 5
+GATE PULSE FROM U340-14 DIAG 5
-GATE PULSE TO J770-M DIAG 9
+GATE PULSE TO J770-P DIAG 9
RESET PULSE TO CR336 DIAG 5
≈1.5V FROM DIAG 9
S565 INTEGRATE
(PARTIAL) STORE S500A
INTEG/STORE TO RT22B DIAG 10 THRU J770-3, P762-6 DIAG 9
PARTIAL A4 HORIZ BOARD
PARTIAL A5 STORAGE BOARD
PARTIAL A4 HORIZ BD
PARTIAL A4 HORIZ BOARD
PARTIAL A8 INTERFACE BOARD
V750
STB
CE
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
11824-61
REV. D, SEP 1978
314
STORAGE 7 PS 9-74

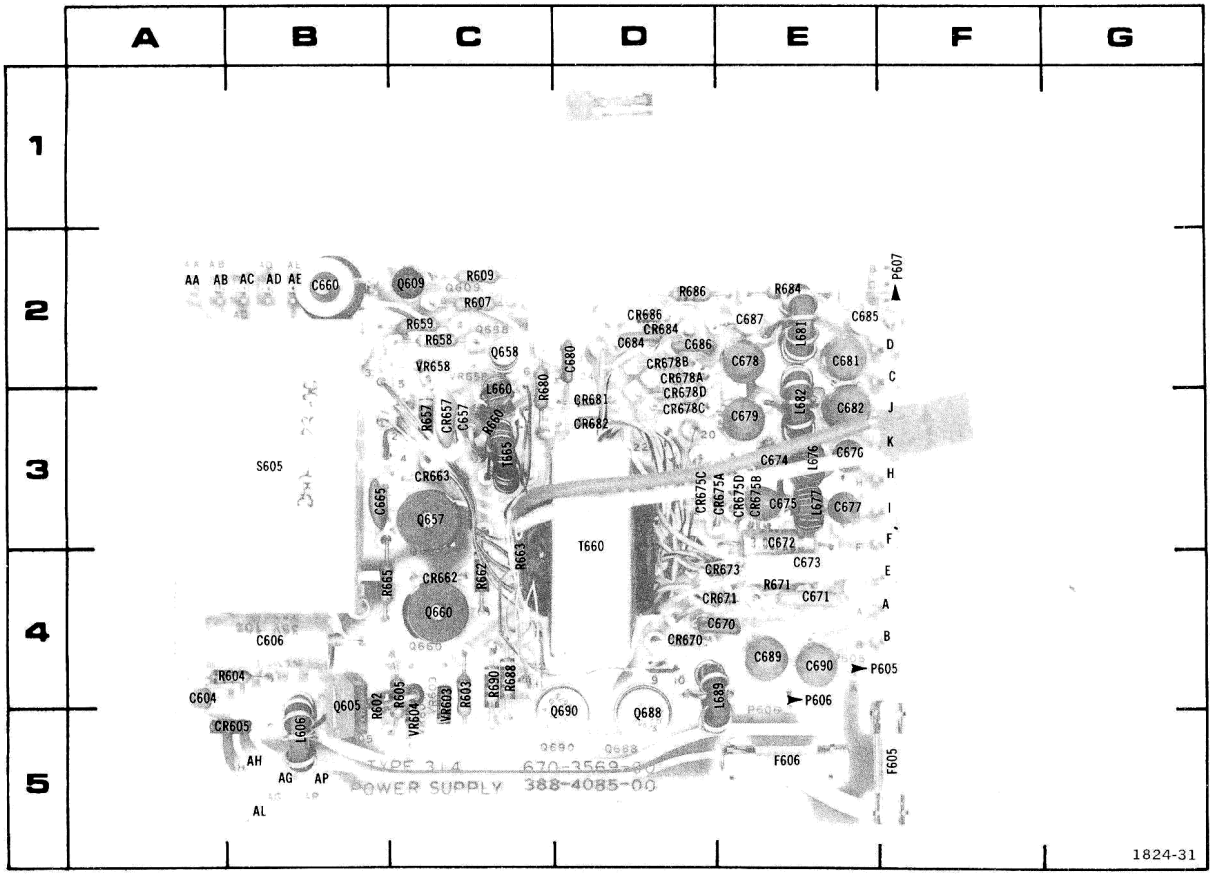
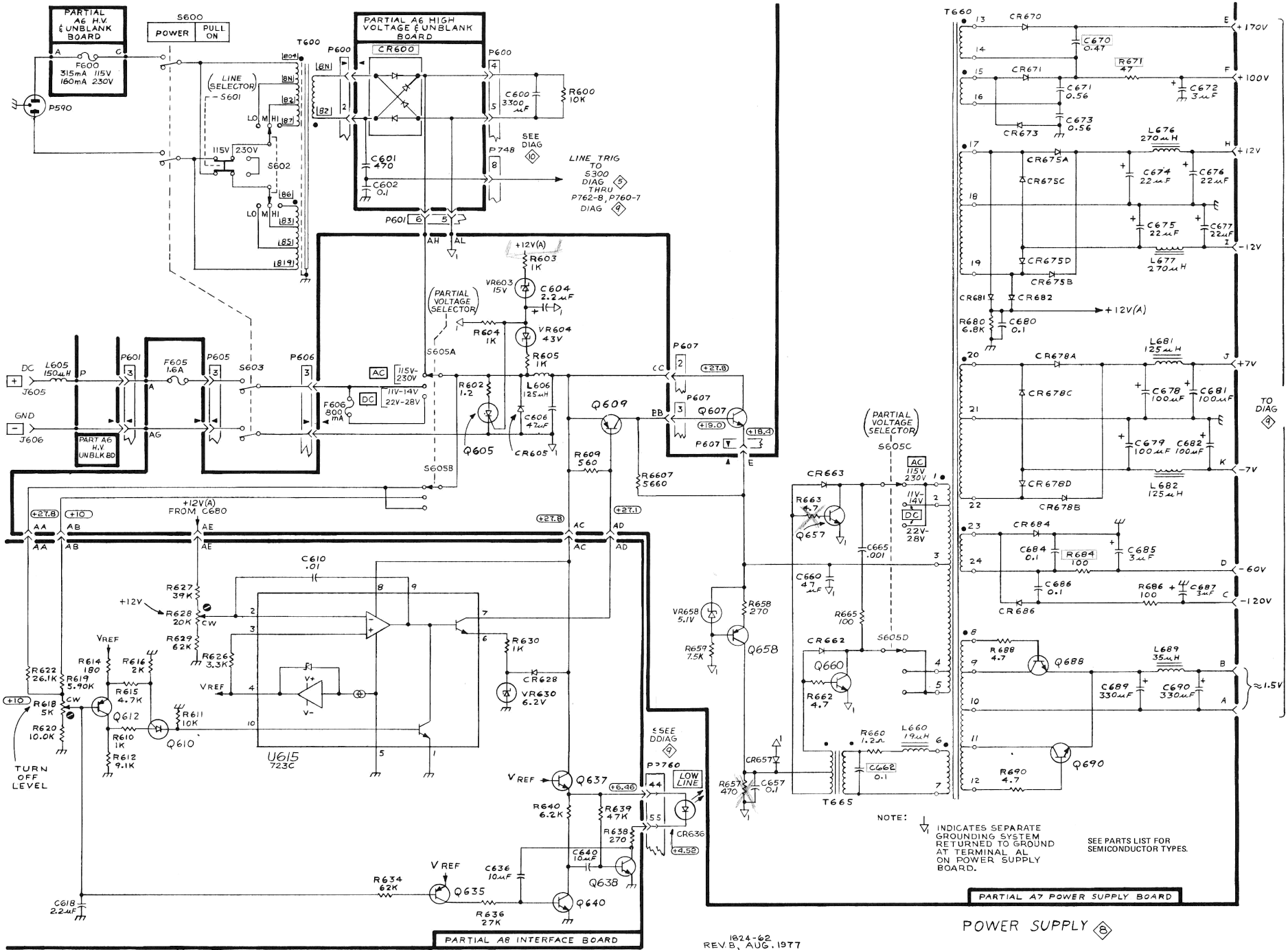


Figure 7-12. A7—Power Supply circuit board.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C604	4A	C685	2E	CR678C	3D	Q605	4B	R671	4E
C606	4B	C686	2D	CR678D	3D	Q609	2C	R680	3C
C657	3C	C687	2E	CR681	3D	Q657	3C	R684	2E
C660	2B	C689	4E	CR682	3D	Q658	2C	R686	2D
C665	3B	C690	4E	CR684	2D	Q660	4C	R688	4C
C670	4E			CR686	2D	Q688	5D	R690	4C
C671	4E	CR605	5B			Q690	5D		
C672	3E	CR657	3C	F605	5F			S605	3B
C673	4E	CR662	4C	F606	5E	R602	4B		
C674	3E	CR663	3C			R603	4C	T660	3D
C675	3E	CR670	4D	L606	5B	R604	4B	T665	3C
C676	3E	CR671	4E	L660	2C	R605	4C		
C677	3E	CR673	4E	L676	3E	R607	2C	VR603	4C
C678	2E	CR675A	3E	L677	3E	R609	2C	VR604	5C
C679	3E	CR675B	3E	L681	2E	R657	3C	VR658	2C
C680	2D	CR675C	3D	L682	3E	R658	2C		
C681	2E	CR675D	3E	L689	4E	R659	2C		
C682	3E	CR678A	2D			R660	3C		
C684	2D	CR678B	2D	P605	4E	R662	4C		
				P606	4E	R663	4C		
				P607	2F	R665	4C		



1824-62
REV.B, AUG. 1977

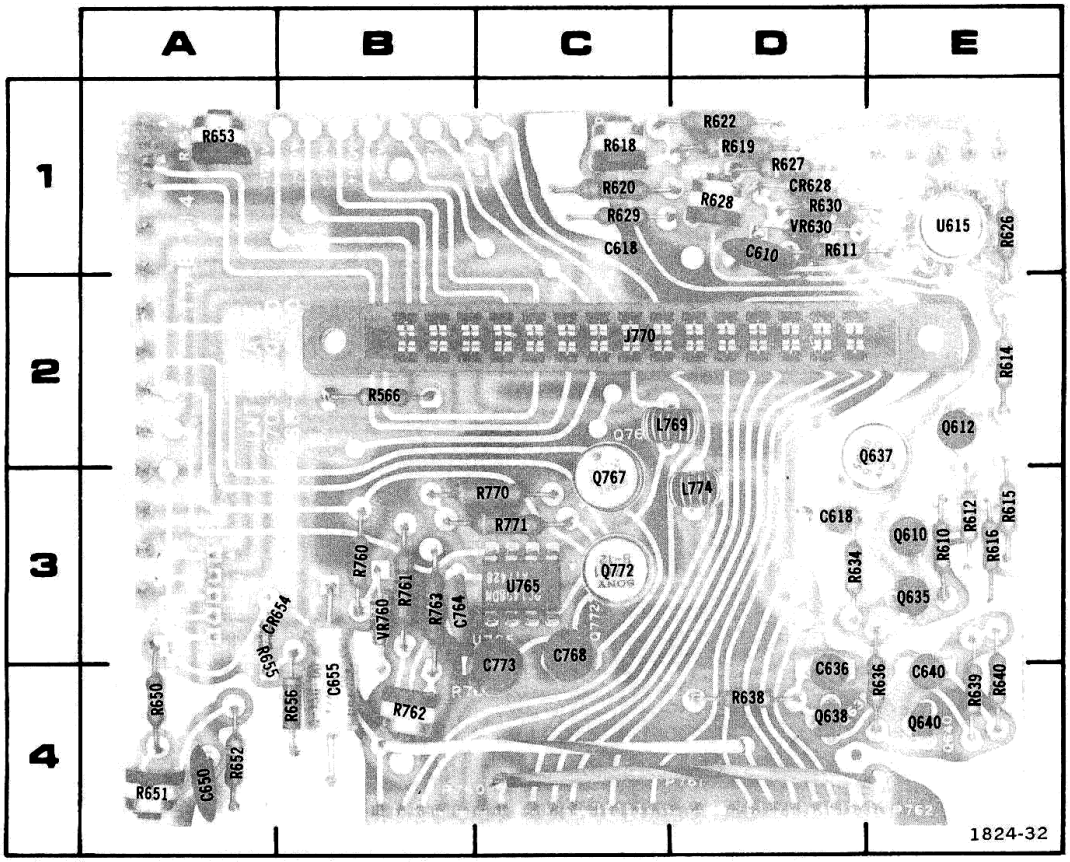
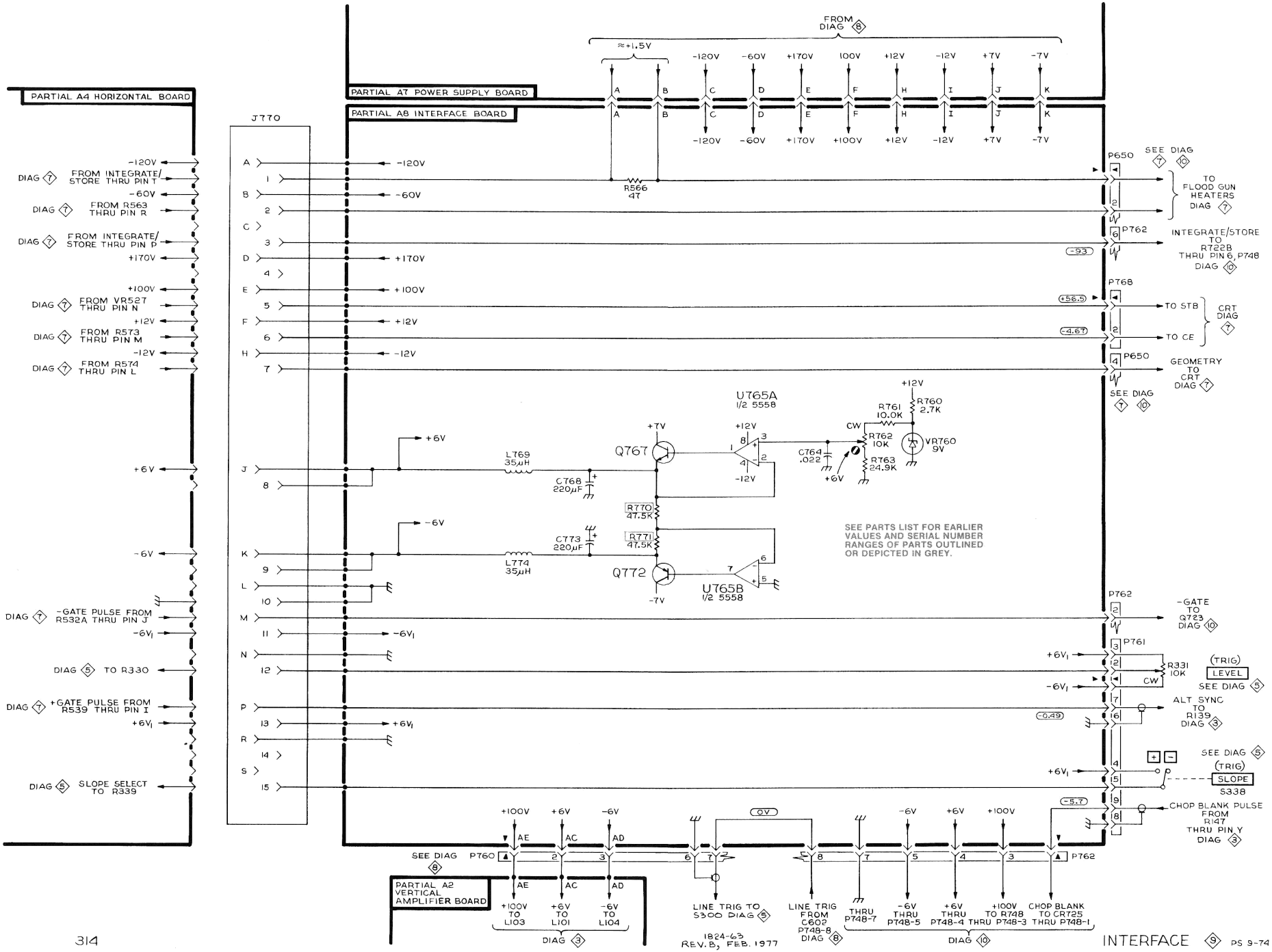


Figure 7-13. A8—Interface circuit board.

[1]Late production location

[2]Early production location

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C610	1D	CR628	1D	Q612	2E	R610	3E	R622	1D	R639	4E	R762	4B
C618[1]	1C	CR654	3A	Q635	3E	R611	1D	R626	1E	R640	4E	R763	3B
C618[2]	3D			Q637	2E	R612	3E	R627	1D	R650	4A	R770	3C
C636	4D	J770	2C	Q638	4D	R614	2E	R628	1D	R651	4A	R771	3C
C640	4E			Q640	4E	R615	3E	R629	1C	R652	4A		
C650	4A	L769	2D	Q767	3C	R616	3E	R630	1D	R653	1A	U615	1E
C655	4B	L774	3D	Q772	3C	R618	1C	R634	3D	R655*	3A	U765	3C
C764	3B					R619	1D	R636	4E	R656	4B	VR630	1D
C768	3C	Q610	3E	R566	2B	R620	1C	R638	4D	R760	3B	VR760	3B
C773	4C									R761	3B		


PARTIAL A4 HORIZONTAL BOARD
PARTIAL A7 POWER SUPPLY BOARD
PARTIAL A8 INTERFACE BOARD
J770
FROM DIAG 8
≈+1.5V
-120V
-60V
+170V
100V
+12V
-12V
+7V
-7V
R566 4T
P650
SEE DIAG 7 10
TO FLOOD GUN HEATERS DIAG 7
P762
INTEGRATE/STORE TO R722B THRU PIN 6, P748 DIAG 10
PT68
TO STB
TO CE
CRT DIAG 7
GEOMETRY TO CRT DIAG 7
U765A 1/2 5558
U765B 1/2 5558
Q767
Q772
R761 10.0K
R760 2.7K
R762 10K
R763 24.9K
VR760 9V
C764 .022
L769 35μH
L774 35μH
C768 220μF
C773 220μF
R770 47.5K
R771 47.5K
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
DIAG 7 FROM INTEGRATE/ STORE THRU PIN T
DIAG 7 FROM R563 THRU PIN R
DIAG 7 FROM INTEGRATE/ STORE THRU PIN P
DIAG 7 FROM VR527 THRU PIN N
DIAG 7 FROM R573 THRU PIN M
DIAG 7 FROM R574 THRU PIN L
DIAG 7 -GATE PULSE FROM R532A THRU PIN J
DIAG 5 TO R330
DIAG 7 +GATE PULSE FROM R539 THRU PIN I
DIAG 5 SLOPE SELECT TO R339
P762
-GATE TO Q723 DIAG 10
P761
R331 10K
(TRIG) LEVEL
SEE DIAG 5
ALT SYNC TO R139 DIAG 3
SEE DIAG 5 (TRIG) SLOPE S338
CHOP BLANK PULSE FROM R147 THRU PIN Y DIAG 3
SEE DIAG 8 P760
PARTIAL A2 VERTICAL AMPLIFIER BOARD
+100V TO L103
+6V TO L101
-6V TO L104
DIAG 3
LINE TRIG TO S300 DIAG 5
LINE TRIG FROM C602 P748-8 DIAG 8
THRU P748-7
-6V THRU P748-5
+6V THRU P748-4
+100V TO R748 THRU P748-3
CHOP BLANK TO CR725 THRU P748-1
DIAG 10
1824-63 REV. B, FEB. 1977
INTERFACE 9 PS 9-74

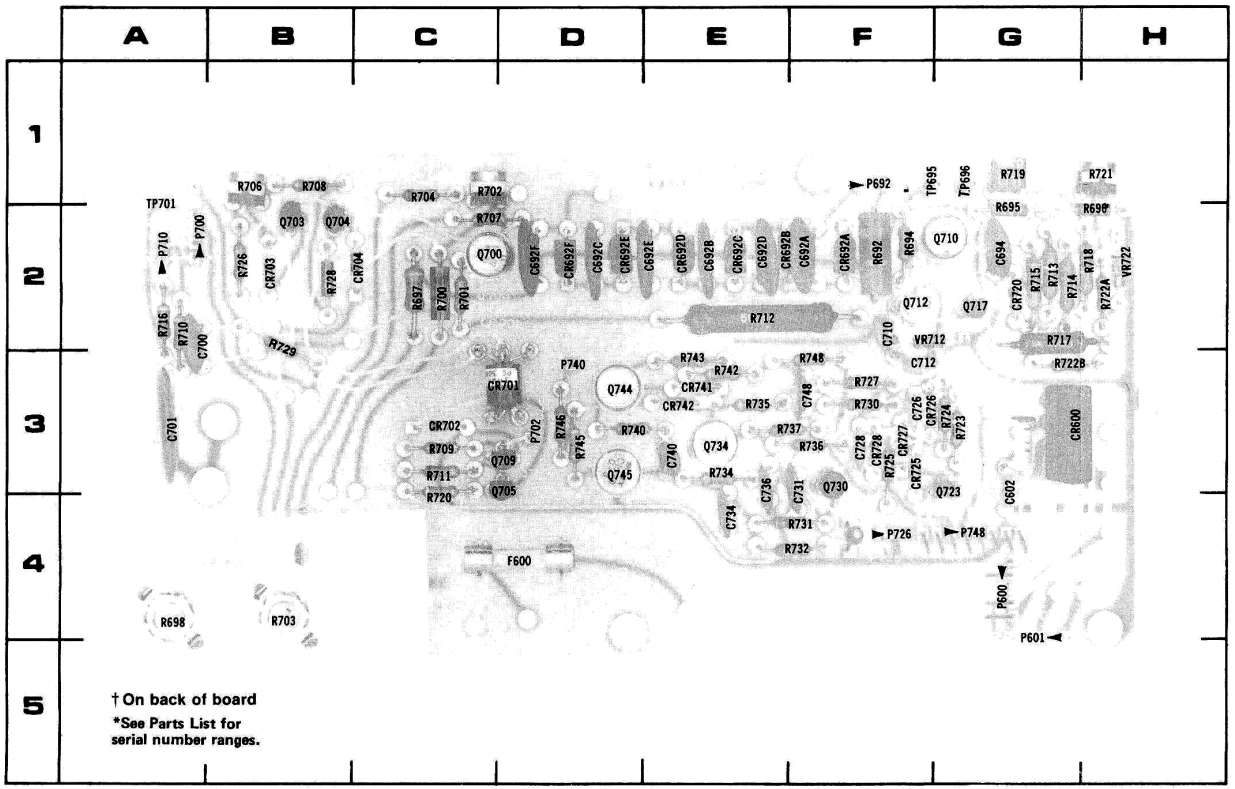


Figure 7-14A. A6—HV & Unblanking circuit board (SN 300651-up).

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C601	3G	C731	3F	CR720	2G	Q712	2F	P748	4G	R710	2A	R722A	2H	R738*†	
C602	4G	C734	4E	CR725	3F	Q717	2G					R722B	3G	R740	3D
C692A	2F	C736	3E	CR726	3F	Q723	3G	R692	2F	R709	3C	R723	3G	R742	3E
C692B	2E	C738*†		CR727	3F	Q730	3F	R694	2F	R710	2A	R724	3G	R743	3E
C692C	2D	C740	3E	CR728	3F	Q734	3E	R695	2G	R711	3C	R725	3F	R745	3D
C692D	2E	C748	3F	CR741	3E	Q744	3D	R696	2H	R712	2E	R726	2B	R746	3D
C692E	2E	CR600	3G	CR742	3E	Q745	3D	R697	2C	R713	2G	R727	3F	R748	3F
C692F	2D	CR692A	2F					R698	4A	R714	2G	R728	2B		
C694	2G	CR692B	2E	F600	4D	P600	4G	R700	2C	R715	2G	R729*	2B	TP695	1F
C700	2A	CR692C	2E			P601	4G	R701	2C			R730	3F	TP696	1G
C701	3A	CR692D	2E	Q700	2C	P692	1F	R702	1C	R716	2A	R731	4F	TP701	1A
C710	2F	CR692E	2D	Q703	2B	P692	1F	R703	4B	R717	2G	R732	4F		
C712	3F	CR692F	2D	Q704	2B	P700	2A	R704	1C	R718	2H	R734	3E	VR712	2F
C726	3F	CR701	3D	Q705	3D	P702	3D	R706	1B	R719	1G	R735	3E	VR722	2H
C728	3F	CR702	3C	Q709	3D	P710	2A	R707	2C	R720	4C	R736	3F		
C730	4F	CR703	2B	Q710	2G	P726	4F	R708	1B	R721	1H	R737	3F		
		CR704	2C			P740	3D								

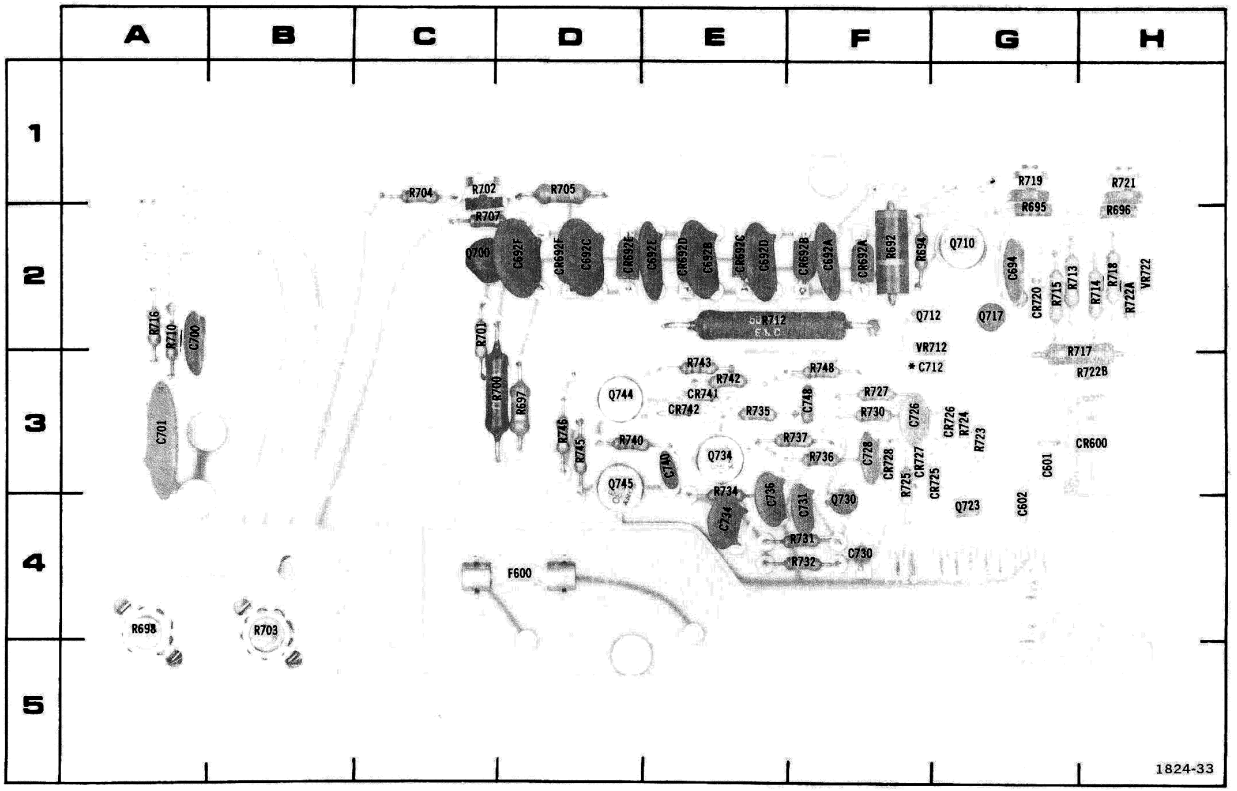
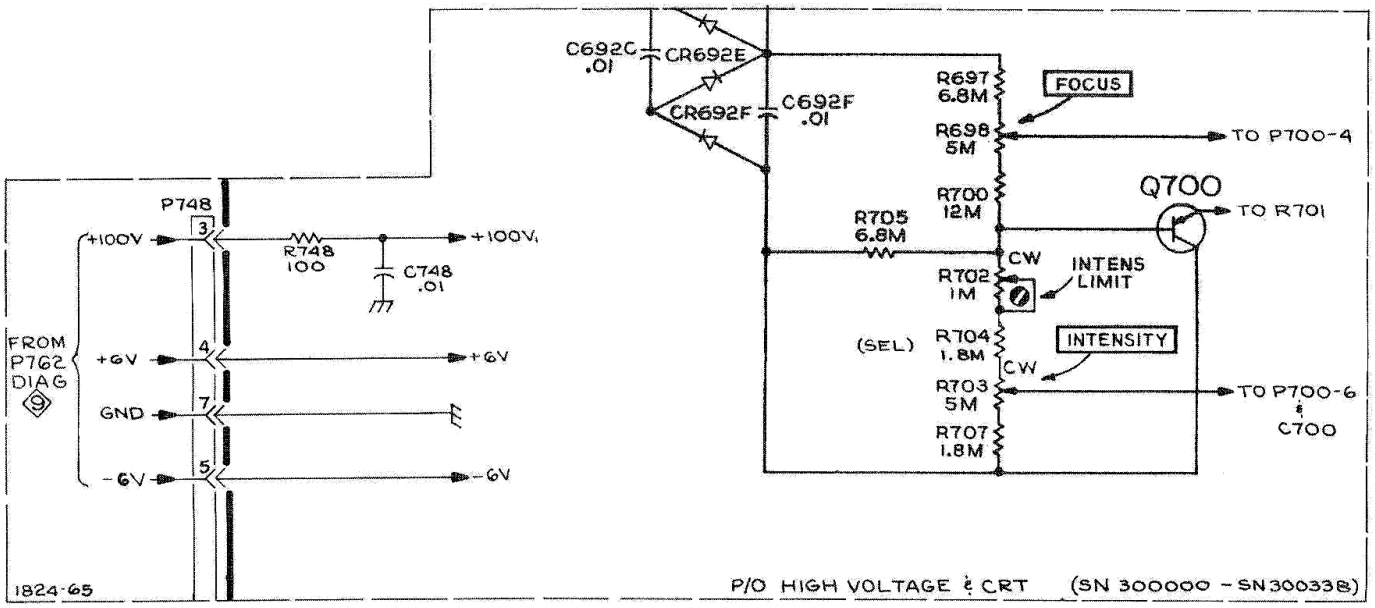
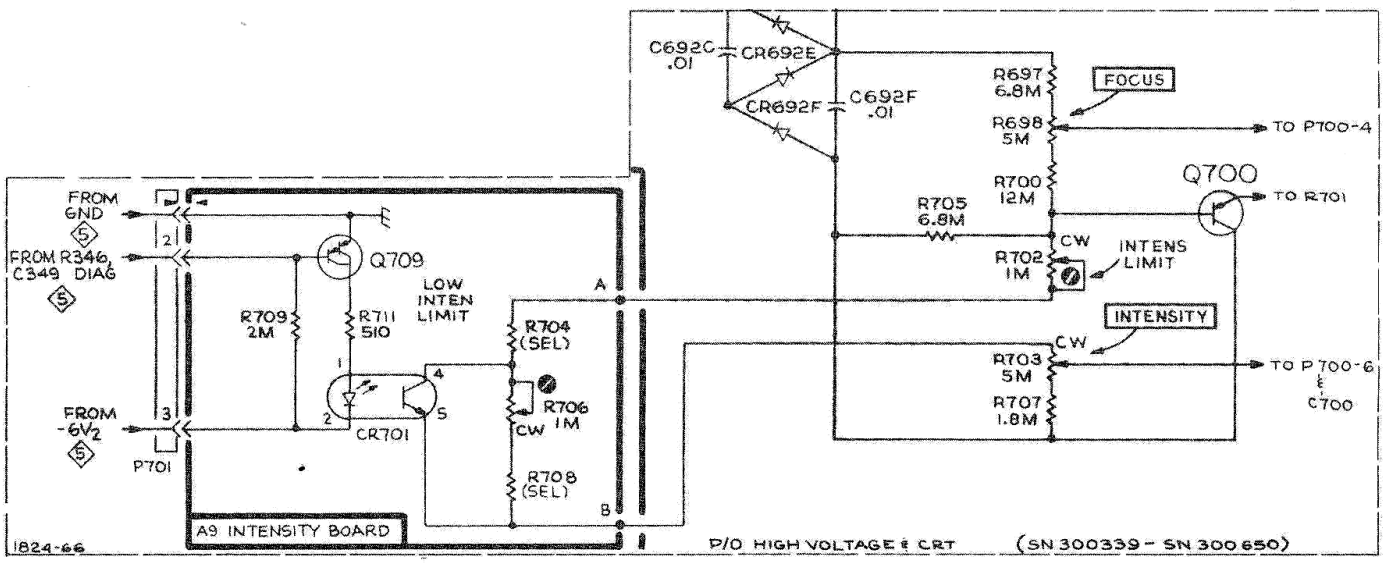


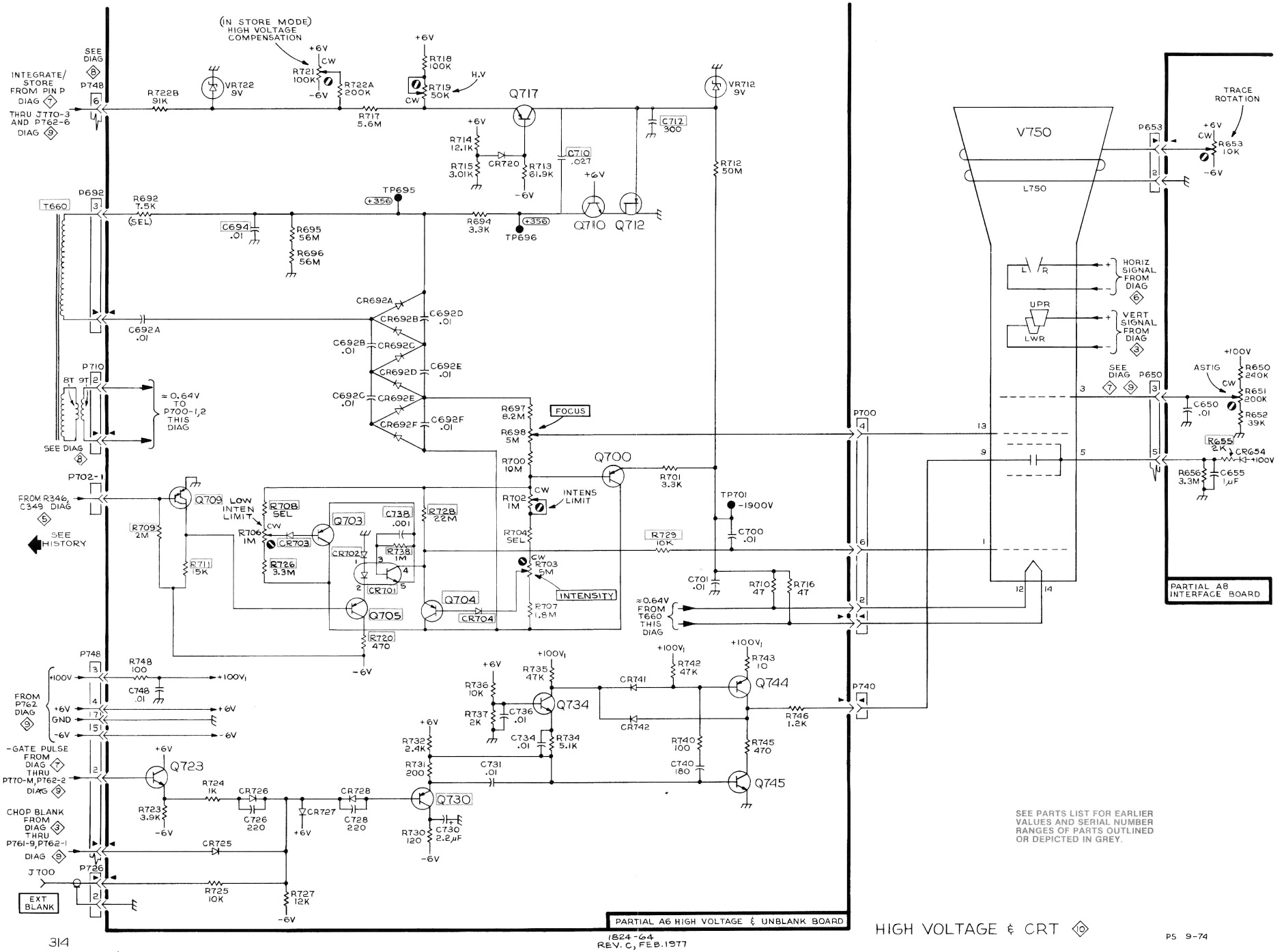
Figure 7-14B. A6—HV & Unblanking circuit board (SN 300000-300650).

*See Parts List for serial number ranges.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C601	3G	C726	3F	CR692D	2E	Q700	2C	R695	2G	R712	2E	R724	3G	R743	3E
C602	4G	C728	3F	CR692E	2D	Q710	2G	R696	2H	R713	2G	R725	3F	R745	3D
C692A	2F	C730	4F	CR692F	2D	Q712	2F	R697	3D	R714	2H	R727	3F	R736	3D
C692B	2E	C731	4F	CR720	2G	Q717	2G	R698	4A	R715	2G	R730	3F	R748	3F
C692C	2D	C734	4E	CR725	3G	Q723	4G	R700	3D	R716	2A	R731	3F		
C692D	2E	C736	3E	CR726	3G	Q730	4F	R701	2C	R717	2G	R732	4F	VR712	2G
C692E	2E	C740	3E	CR727	3F	Q734	3E	R702	1C	R718	2H	R734	3E	VR722	2H
C692F	2D	C748	3F	CR728	3F	Q744	3D	R703	4B	R719	1G	R735	3E		
C694	2G	CR600	3H	CR741	3E	Q745	3D	R704	1C	R721	1H	R736	3F		
C700	2A	CR692A	2F	CR742	3E			R705	1D	R722A	2H	R737	3F		
C701	3A	CR692B	2F			R692	2F	R707	2C	R722B	3H	R740	3D		
C712*	3G	CR692C	2E	F600	4D	R694	2F	R710	2A	R723	3G	R742	3E		


C692C .01
CR692E
CR692F
C692F .01
R697 6.8M
FOCUS
R698 5M
TO P700-4
R700 12M
Q700
TO R701
R705 6.8M
CW
R702 1M
INTENS LIMIT
(SEL)
R704 1.8M
INTENSITY
CW
R703 5M
TO P700-6 & C700
R707 1.8M
P748
3
+100V
R748 100
+100V1
C748 .01
FROM P762 DIAG 9
4
+6V
+6V
7
GND
5
-6V
-6V
1824-65
P/O HIGH VOLTAGE & CRT (SN 300000 - SN300338)


C692C .01
CR692E
CR692F
C692F .01
R697 6.8M
FOCUS
R698 5M
TO P700-4
R700 12M
Q700
TO R701
R705 6.8M
CW
R702 1M
INTENS LIMIT
INTENSITY
CW
R703 5M
TO P700-6 & C700
R707 1.8M
FROM GND 5
FROM R346, C349 DIAG 5
FROM -6V2 5
P701
Q709
LOW INTEN LIMIT
R709 2M
R711 510
R704 (SEL)
R706 1M
CW
R708 (SEL)
CR701
A
B
A9 INTENSITY BOARD
1824-66
P/O HIGH VOLTAGE & CRT (SN 300339 - SN 300650)



1824-64
REV. C, FEB. 1977

HIGH VOLTAGE & CRT 10