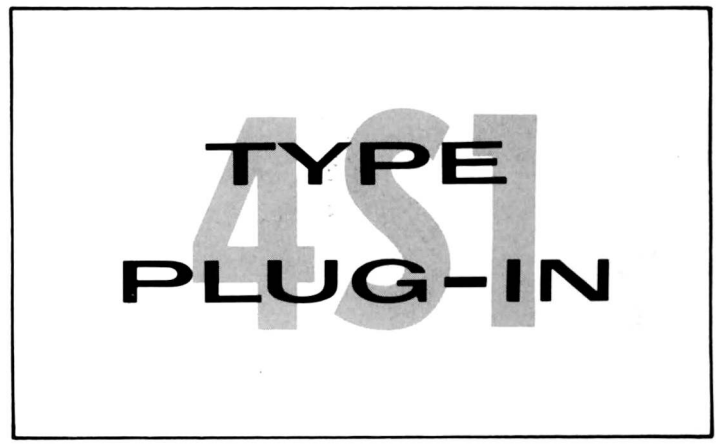
INSTRUCTION MANUAL

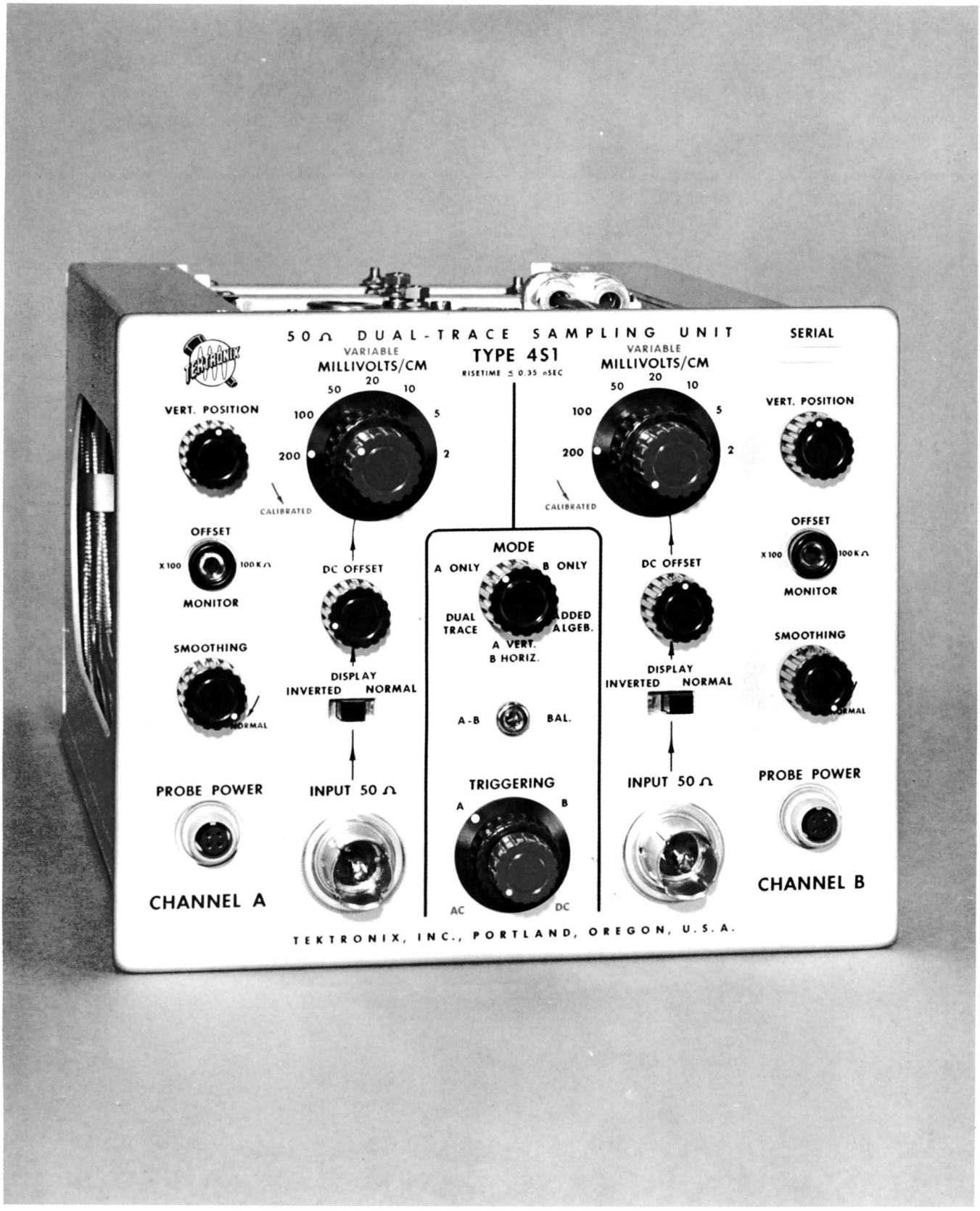
Serial Number _____



Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon ● Phone MI 4-0161 ● Cables: Tektronix

Tektronix International A.G.
Terrassenweg 1A ● Zug, Switzerland ● PH. 042-49192 ● Cable: Tekintag, Zug Switzerland ● Telex 53.574

070-329 1063


50 Ω DUAL-TRACE SAMPLING UNIT
SERIAL
TYPE 4S1
RISETIME ≤ 0.35 nSEC
VARIABLE
MILLIVOLTS/CM
50
20
10
100
5
200
2
CALIBRATED
VERT. POSITION
OFFSET
X100
100KΩ
MONITOR
SMOOTHING
NORMAL
DC OFFSET
DISPLAY
INVERTED
NORMAL
PROBE POWER
INPUT 50 Ω
CHANNEL A
MODE
A ONLY
B ONLY
DUAL TRACE
ADDED ALGEB.
A VERT.
B HORIZ.
A-B
BAL.
TRIGGERING
A
B
AC
DC
CHANNEL B
TEKTRONIX, INC., PORTLAND, OREGON, U.S.A.

Type 4S1

SECTION 1
CHARACTERISTICS

GENERAL INFORMATION

The Tektronix Type 4S1 50 Ω Dual-Trace Sampling Unit is a general-purpose vertical-channel plug-in unit for use with the Type 661 Oscilloscope. It has a risetime of 0.35 nsec (nanosecond = 10^{-9} second) or less. Seven calibrated deflection factors range from 2 mv/cm to 200 mv/cm, and uncalibrated variable deflection factors between these steps provide up to three times increase in sensitivity at each step. Minimum deflection factor is about 2/3 mv/cm.

The Type 4S1 in a Type 661 Oscilloscope is capable of presenting either single- or dual-trace displays of repetitive fast-rise signals. Two signals may also be displayed in an X-Y mode (lissajous) or added algebraically. The balanced-bridge input and the error-sensing method of signal reconstruction provide a very low level of trace noise and minimum kick-back from the input circuit. Internal delay lines and trigger takeoff in the Type 4S1 allow the system to be operated with no external delay or trigger cables.

The system samples the input signal, each sample at a slightly later time, and reconstructs the signal on an equivalent time base.

OPERATING CHARACTERISTICS

Risetime

0.35 nsec or less, measured between 10% and 90% amplitudes.

Bandpass

Equivalent to Dc to 1 Gc (gigacycle = 10^9 cps).

Input Impedance

50 ohms. A higher impedance may be obtained by using Tektronix passive or cathode-follower signal probes.

Dynamic Range

2 volts peak-to-peak, without overloading input circuitry. Maximum short-time dc overload is plus or minus 10 volts.

Deflection Factors

Calibrated steps of 2, 5, 10, 20, 50, 100 and 200 mv/cm. Accuracy: ±1% at 200 mv/cm, with DISPLAY switch at NORMAL; ±3% from 100 mv/cm through 10 mv/cm; ±4% at 5 mv/cm and 2 mv/cm. With DISPLAY switch at INVERTED, 200 mv/cm accuracy is ±2%. An uncalibrated VARIABLE control, with a range of three-to-one, permits increasing the sensitivity between the calibrated steps of the MILLIVOLTS/CM switch. The 2 mv/cm deflection factor can be extended to 2/3 mv/cm with the VARIABLE control.

DC Offset

Up to ±1 volt, with a five-turn control, for making measurements or positioning the trace vertically. With a deflection factor of 200 mv/cm, the DC OFFSET control can cause a +1-volt (±12%) to −1-volt (±3%) change at the corresponding vertical output jack on the oscilloscope.

Offset Monitor

Front-panel jack permits measurement of dc voltage-level changes made with DC OFFSET control. Voltage change at OFFSET MONITOR jack is 100 times the voltage change seen in the display. Monitor voltage range is +104.5 volts (±10%) to −100 volts (±5%), and output impedance is 100 k ohms.

Modes of Operation

A Only, B Only, Dual Trace, Added Algebraic and A Vertical-B Horizontal (lissajous). Dual trace switching frequency is approximately 50 kc. Rejection ratio for Added Algebraic mode is 40:1 or better when each channel is driven with a ½-volt flat-topped pulse and the deflection factor for each channel is 50 mv/cm.

Internal Delay Lines

Approximately 45-nsec signal delay between trigger takeoff and sampling bridge, on each channel.

Internal Trigger Signal

Triggering signal is selected from either input channel for use by timing unit. Trigger amplitude to timing unit is about ⅛th the input signal amplitude, ac- or dc-coupled.

Time Coincidence Between Channels

In Dual Trace mode, display time difference between two indentical signals is no more than 30 psec (picoseconds = 10^{-12} seconds).

Display

Normal or inverted. A separate control for each channel permits inversion of either or both signals, allowing signals to be added or subtracted in the Added Algebraic mode. An additional ±1% error may be added to deflection factor error with DISPLAY switch at INVERTED position.

Noise

No more than 1 mv peak-to-peak, at 2 mv/cm, with SMOOTHING control at NORMAL, and MODE switch at A ONLY, B ONLY or A VERT. B HORIZ.; no more than 1.5 mv peak-to-peak with MODE switch at DUAL TRACE or ADDED ALGEB. Noise is typically less than 0.5 mv peak-to-peak with SMOOTHING control fully counterclockwise.

Smoothing

Reduces noise amplitude to about ½ the noise amplitude normally present. Useable when dot density is sufficient. Less than 3 mv noise when rotating SMOOTHING control slowly.

Crosstalk

Less than 1.5% crosstalk between channels when observing a 400 mv pulse such as the Delayed Pulse signal from the Type 661 Oscilloscope.

Dot Slash

No visible vertical drift of sampling dots with triggering rate above 150 cps; no more than 2 mm vertical drift at triggering rate of 50 cps.

Probe Power

Power provided through front-panel connector for operation of cathode-follower probes. Filament voltage is 12.6 volts dc (terminals B and C), and cathode-to-plate voltage is 100 volts (terminals A and D). These voltages are regulated by the oscilloscope.

Signal Outputs through Oscilloscope

Within 3% of signal voltages at input connectors, plus offset, when deflection factor is 200 mv/cm. Output impedance is 10 k ohms ±2%.

MECHANICAL

Construction

Aluminum-alloy chassis, with six plug-in subchassis units. Photo-etched anodized front panel.

Dimensions

Height—7 inches; width—8½ inches; depth—14 inches.

Weight

Approximately 15½ pounds.

STANDARD ACCESSORIES

2—50-ohm 10X T Attenuators, with GR connectors . 017-044

2—50-ohm 5-nsec coax cables, with GR connectors . . 017-502

2—Instruction manuals 070-329

SECTION 3

CIRCUIT DESCRIPTION

GENERAL INFORMATION

The Type 4S1 is a balanced-bridge error-correction type sampling unit providing vertical deflection voltages for the Type 661 Oscilloscope. The unit has two independent channels controlled by the MODE switch. Each channel has an internal trigger-takeoff circuit which may be used to trigger the timing unit. The input signal is delayed 45 nsec after the trigger takeoff to allow the timing unit to begin the sampling cycle before the signal has reached the sampling gate diode bridge. A zero-order-hold memory is used in each channel to remember the value of the previous sample.

The sampling repetition rate ranges from 50 cps to 100 kc. This rate is determined by both the repetition rate of the triggering signal and the recovery time of the timing unit. If a rate slower than 150 cps is used, the memory output may drift, and memory "dot slash" may be seen. The maximum rate of 100 kc allows sufficient time for the sampling unit to pass a sample and recover before another sample is taken. Above 100 kc countdown must be provided, either by the timing unit or by some external device.

Most of the circuitry in the Type 4S1 is mounted on plug-in subchassis. The front panel and main frame unit contains only the controls, delay lines, interconnecting wiring, attenuators and Trigger Amplifier subchassis. The plug-in subchassis are: Sampler; AC Amplifier; Memory (one for each channel); Inverter, and Dual Trace. Each of these will be discussed here. The two interconnecting plugs at the rear of the frame, and the two coaxial connectors on top, connect the circuitry of the Type 4S1 to the oscilloscope and the timing unit.

This circuit description will be limited to a discussion of the operation of the various circuits. Anyone not familiar with the general concept and principles of sampling may also wish to refer to some introductory material on sampling, such as the Tektronix publication, "Sampling Notes."

SIMPLIFIED BLOCK DIAGRAM

A simplified diagram of the Type 4S1 circuitry is shown in Fig. 3-1. Each functional circuit is represented as a block, with external controls labeled. More detailed block diagrams may be found at the beginning of the Schematics section and with the descriptions of the individual circuits. Refer to the simplified block diagram during the following discussion.

The input signal is applied to the Type 4S1 through a 50-ohm coaxial connector, then travels through the Trigger Takeoff system and 45 nsec of 50-ohm delay cable to the Sampling Gate. The Trigger Takeoff circuit takes off a small portion of the input signal and sends trigger pulses to the Trigger Amplifier. The output of the Trigger Amplifier is then applied to the triggering circuitry of the timing unit to start the sampling cycle. The timing unit may also be triggered by pulses from an external trigger source.

After being triggered, the timing unit sends a command pulse to the Blocking Oscillator on the Sampler subchassis of the Type 4S1. The Blocking Oscillator pulses the Snap-Off circuit with a fast pulse and the Memory Driver with a slower pulse. Short push-pull pulses from the Snap-Off circuit are applied to the Sampling Gates in both channels, strobing the Sampling Gates into conduction for about 0.35 nsec. During this brief period, the input signal in each channel is passed through the Sampling Gate. The signal attempts to charge the stray capacitance (C_s) of the circuitry from its previous voltage level to the level of the input signal at the instant of sampling. However, the strobe pulse ends and the gate stops passing signal before the input capacitance has had time to charge completely.

The small correction sample pulse that was passed by the Sampling Gate is amplified about 2.5 times in the Sampler Amplifier, then passes through the MILLIVOLTS/CM switch, where it may be attenuated, and is sent on to the AC Amplifier to be inverted and amplified about 280 times.

By the time the signal pulse reaches the Memory Gate, the Memory Gate Driver has pulsed this gate into conduction, so the sample is passed from the AC Amplifier to the Memory circuit. The Memory re-inverts the signal and stores the value of the pulse on the memory capacitor. The output of the Memory is then applied to the Dual Trace circuit, either bypassing the Inverter for normal display, or passing through the Inverter for inverted display.

Between the Inverter and the Dual Trace circuit, the display gain is set by the A-B BAL. control (for Channel A) or the B CAL. control (for Channel B). Passage of either or both of the two signals through the Dual Trace circuit to the oscilloscope vertical circuitry is determined by an electronic switch controlled by the front-panel MODE switch.

A portion of the Memory output is sent back through a positive feedback loop to the sampling bridge. Since the Memory Gate stops conducting immediately after the sample pulse has passed, the feedback signal cannot regenerate through the main signal path. Amplitude of the signal in the feedback loop is set so that it will bring the charge on C_s up to the total input signal voltage at the instant it was sampled. The Sampler is then ready for the next sample, which will be initiated by the next trigger pulse.

Fig. 3-2 traces a single sample pulse through the sampling channel, and shows the effect of feedback. In the illustration, the attenuator switch is set at 200 MILLIVOLTS/CM (fully counterclockwise). A sample pulse is shown resulting from sampling the input signal ("a") at a time when it is 100 millivolts above the level at the output of the Sampling Gate. The level of the previous sample is taken as zero for convenience.

A very fast rise is seen at the output of the Sampling Gate ("b") while the gate is forward biased. The pulse amplitude reaches about 25 millivolts before the gate stops passing signal, then the signal begins to drop very slowly.

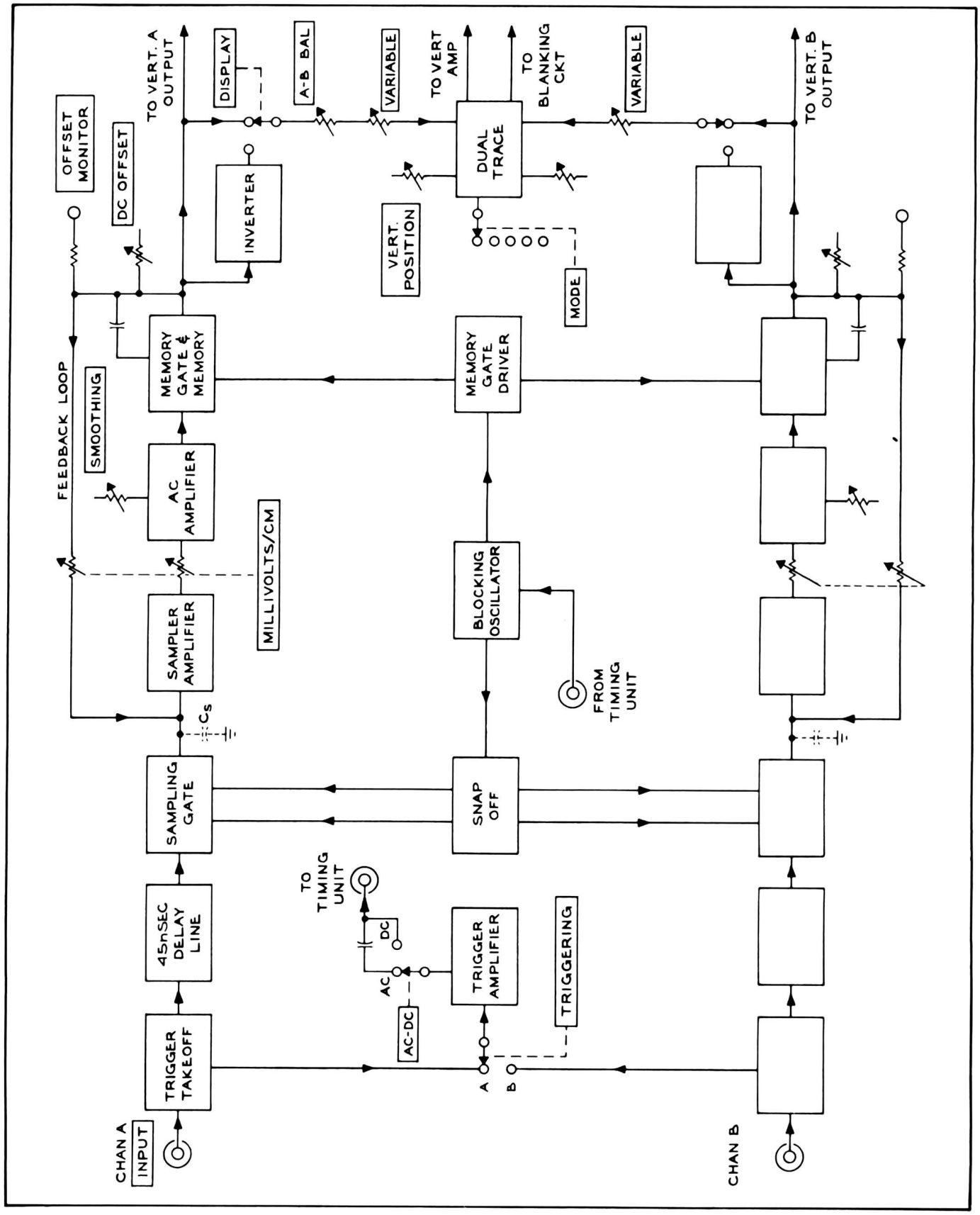


Fig. 3-1. Simplified Block Diagram of Type 4S1. Channel B is identical to Channel A, except where indicated.

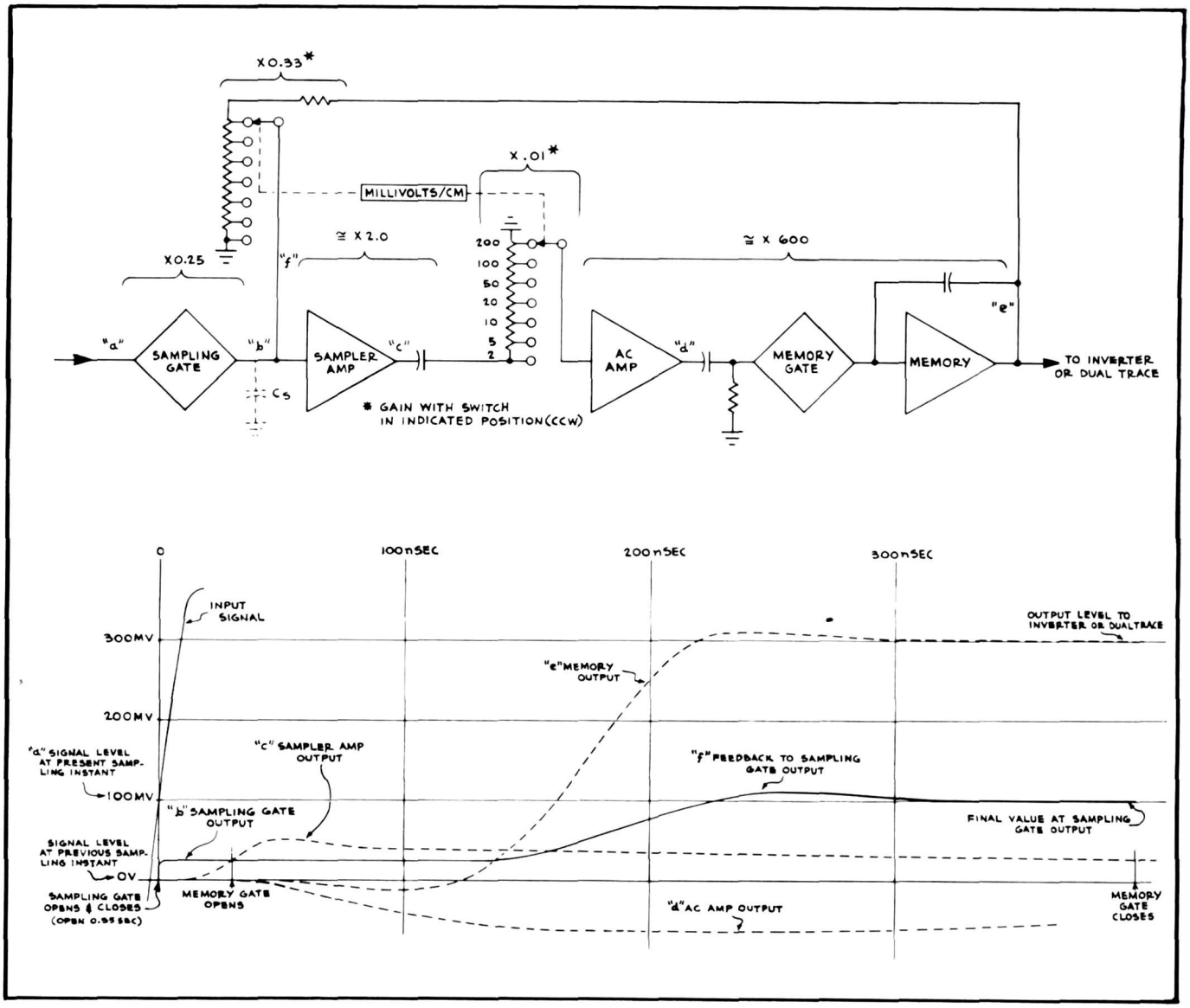


Fig. 3-2. A single sample signal traced through the feedback loop (see text).

The Sampler Amplifier amplifies the step about 2.5 times to give an output of 62 millivolts. Due to circuit losses, especially in capacitive coupling, the gain of this and subsequent stages is only about 60% of the cumulative gain of the individual circuits. Thus the actual amplitude out of the Sampler Amplifier is about 50 millivolts ("c"). The gain factors given in Fig. 3-2 are the actual gain factors in the various sections of the feedback loop. The Sampler Amplifier output is attenuated by a factor of 100 with the MILLIVOLTS/CM switch set at 200, giving an amplitude of .5 millivolts. The attenuated signal is not shown in the illustration. (Attenuation can be deceased to zero when the MILLIVOLTS/CM switch is set to 2).

The error-correction signal is then amplified about 280 times in the AC Amplifier to produce an output of about 100 millivolts ("d"). This amplitude is not seen at the input to the Memory circuit, however, due to the fact that the Memory is a high gain amplifier with negative feedback that holds its input nearly stationary.

Circuit gain of the Memory is about 3. Therefore, taking circuit losses into consideration, the gain from the AC Amplifier to the Memory output is about 600, producing an amplitude of about 300 millivolts in the illustration ("e"). The Memory Gate then stops conducting and the charge on the memory capacitor holds the output level at 300 millivolts. The output is sent back through the feedback attenuator where it is attenuated by a factor of 3 to give an amplitude of 100 millivolts. (Feedback attenuation can be inceased to 300 with the MILLIVOLTS/CM switch set to 2). The attenuator applies the signal to the Sampler to bring the output level of the Sampling Gate up to the 100 millivolt value of the input signal at the instant of sampling ("f"). The channel is then ready to take another sample.

Each subsequent sample is taken at a later point on the waveform, as determined by the staircase generator of the timing unit. Thus the signal through the circuitry, from the Sampler to the oscilloscope, is a series of pulses, each of which is proportional to the change in signal level between

sampling instants. The series of level-correction signals from the Type 4S1 is sent to the oscilloscope vertical circuitry where it draws out the input signal as a series of dots on the crt. If the signal level does not change between samples, no signal passes through the circuitry, and a straight line of dots is presented.

Since the vertical circuitry of the Type 661 Oscilloscope requires 600 millivolts of signal amplitude from the sampling unit for each centimeter of trace deflection on the crt, the output deflection factor of the Type 4S1 must remain constant at 600 mv/cm in relation to the input. To maintain this relationship and still be able to change the input deflection factor for viewing both large and small signals, the signal gain of the channel and the sample-pulse amplification must both be varied. These two functions are performed simultaneously by the action of two attenuators operated by the front-panel MILLIVOLTS/CM switch, as explained later in the description of the Feedback Loop.

The front-panel SMOOTHING control in the AC Amplifier feedback decreases the gain of the sample amplification loop. This reduces random noise by limiting the ability of the circuit to keep up with input signal changes, but does not normally affect the crt display amplitude set by the feedback attenuator, circuit parameters and display gain controls.

INPUT AND TRIGGER TAKEOFF

Input

The input connectors on the Type 4S1 are 50-ohm GR Type 874 connectors. These assure maximum uniformity of input impedance and a universal quick-mate system. Characteristic impedance of the input is within 1% of 50 ohms.

Trigger Takeoff

The Trigger Takeoff circuit is located immediately behind the front-panel input connector. It consists of a ferrite core transformer, T1001, and a dc connection to the coax center conductor. Fig. 3-3 shows an exploded view of the Trigger Take-off. The circuit extracts about 1% of the signal energy, and sends this triggering information to the Trigger Amplifier. The transformer delivers an ac output signal equal to about one-eighth the voltage at the input terminal, over the range from about 350 kc to 1 gigacycle. The direct connection to the coax provides an output signal of approximately the same amplitude, from dc to 350 kc. Frequency compensation in the Trigger Takeoff nearly eliminates signal aberrations.

Delay Line

To be able to display the signal that was used to trigger the first sampling cycle of a sweep, the input signal must be delayed by at least 40 nsec to allow for the 40 nsec the timing unit requires to respond to internal triggering information.

This signal delay is provided by passing the signal through a special 45-nsec delay cable between the Trigger Takeoff and the Sampling Gate. The timing unit can then start the sampling cycle before the signal reaches the input bridge, and samples can be taken on the leading edge of a fractional nanosecond signal. The delay line, which is manufactured by Tektronix to be within 2% of 50 ohms characteristic impedance, has negligible fast-rise signal reflections.

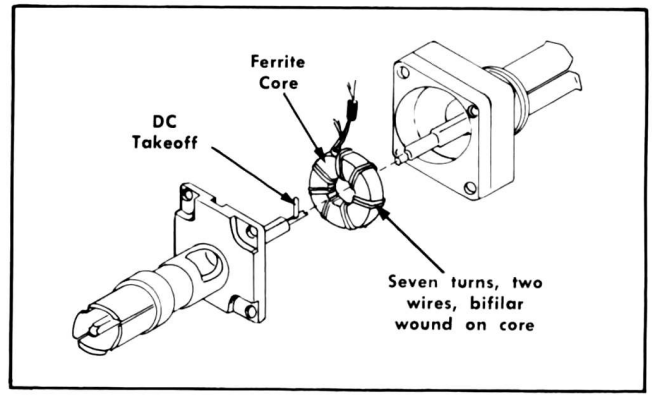


Fig. 3-3. Exploded view of trigger takeoff.

TRIGGER AMPLIFIER

The Trigger Amplifier has a low-frequency section and a high-frequency section. The outputs from these two sections are combined to supply trigger signals to the timing unit, over the operating range from dc to 1 gigacycle. Effective crossover from dc to ac operation occurs at about 350 kc. Refer to Fig. 3-4 and the Trigger Amplifier diagram in the Schematics section during the following discussion.

The high-frequency portion of the circuit consists of transistor Q1014, which receives the ac signals from the transformers in the Trigger Takeoff circuits. The output from the trigger takeoff transformer in either channel is connected through the TRIGGERING switch, SW1004, to the emitter circuit of Q1014. High-frequency trigger pulses from the collector of Q1014 pass through the AC-DC switch, SW1019, to be sent to the triggering circuit of the timing unit. Inductor L1015 serves to isolate the collector circuit of Q1014 from the low-frequency trigger amplifier.

The low-frequency portion of the Trigger Amplifier consists of a transistor amplifier pair, Q1023 and Q1024, which receives signals from the direct connection to the coax center conductor in the Trigger Takeoff. Input is through either R1002 or R2002, selected by the TRIGGERING switch. Emitter follower Q1023 drives Q1024 which is collector-coupled through the AC-DC switch to the output jack. In the two negative feedback loops around the amplifier pair, low-frequency feedback is provided by R1033 and C1032, and mid-frequency feedback is provided by R1036, C1036 and C1037.

SAMPLER
Subchassis Series 1 and 7

Mounted on the Sampler subchassis are a Sampling Gate diode bridge and Sampler Amplifier for each of the two

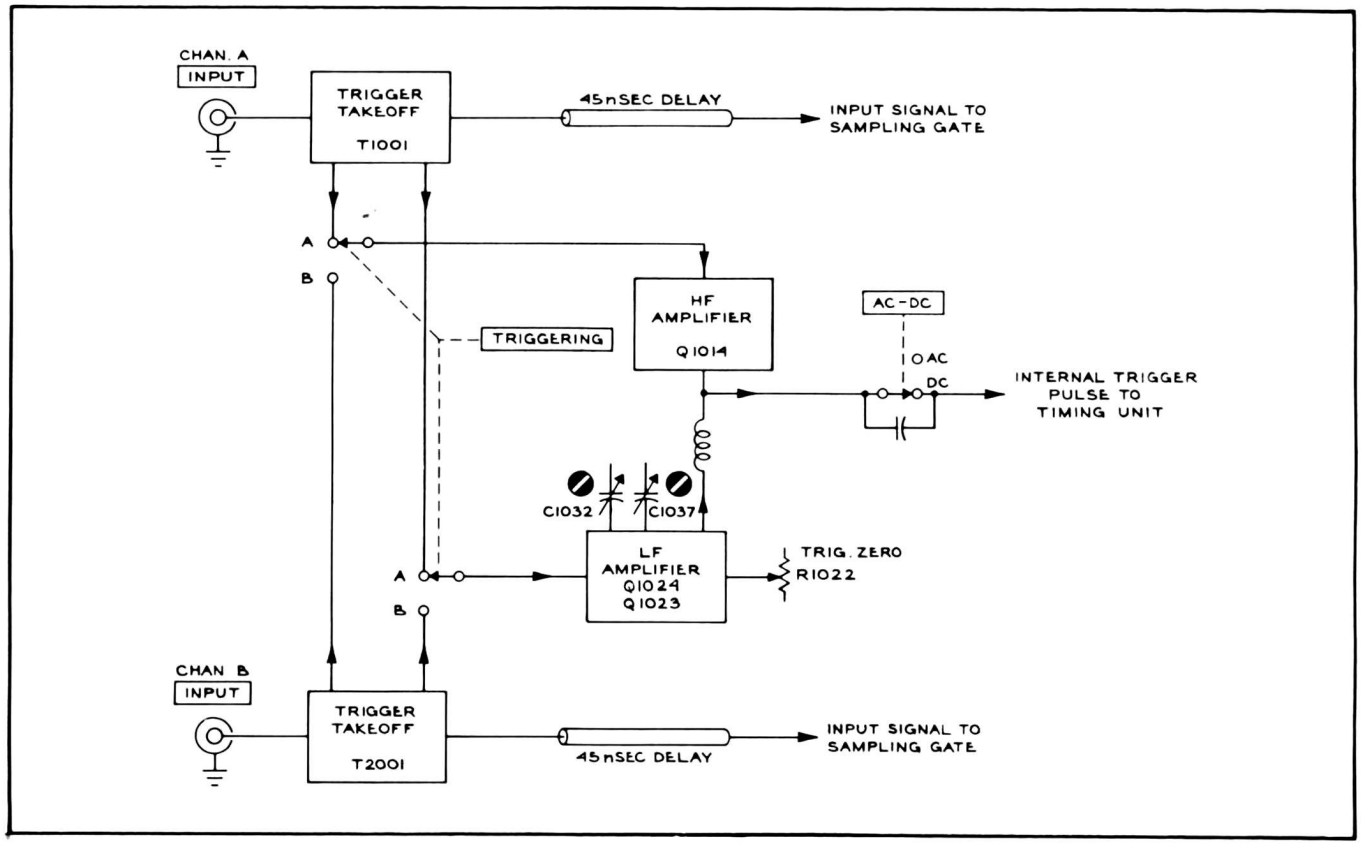


Fig. 3-4. Block Diagram of Trigger Amplifier.

channels, and also the Blocking Oscillator, the Snap-Off Circuit and the Memory Gate Driver. A detailed block diagram of the Sampler circuitry is shown in Fig. 3-5. Refer also to the Sampler schematic diagram in the back of this manual. Since the two channels are identical only the Channel A Sampler circuitry will be discussed.

Blocking Oscillator

A positive command pulse of about 2 volts is received from the timing unit by way of a 50-ohm coax which is threaded through a toroid to prevent transmission of stray pickup from the Sampler. The pulse is applied through C2018 and D2018 to the collector of the Blocking Oscillator transistor, Q2010, and is coupled to the base circuit as a negative pulse. Quiescently, Q2010 is turned off, being reverse-biased by D2013. When a pulse is received, the combination of a negative-going base and a positive-going collector causes this transistor to turn on and saturate very fast, due to the common-emitter configuration. As Q2010 turns on, a fast 10-volt positive pulse is sent through C2010 to T2004 in the Snap-Off circuit. At the same time the two-turn coil of T2010 couples a negative pulse to the Memory Gate Driver circuit.

After saturation has occurred in Q2010, the normal blocking oscillator backswing begins, but D2010 stops the backswing at about —19 volts, so that no overvoltage is applied to the transistor. At the same time, the charge on C2013 reverse-biases the base of Q2010, allowing a quick return to equilibrium.

Memory Gate Driver

The Memory Gate Driver transistor, Q2024, is normally biased to cutoff by a slightly positive voltage on its base. As a negative pulse is received from the Blocking Oscillator, D2022 conducts and forward biases Q2024 into conduction, then into saturation. Collector current flows through R2027, R2028 and the Memory Gate coils (not through D2024 and R2024).

As the pulse from the Blocking Oscillator ends, D2022 becomes reverse biased and decouples the circuits. The positive output pulse to the Memory Gates continues until the base of Q2024 becomes slightly positive again and cuts off this transistor. With D2022 reverse biased, the only discharge path for the base circuit is through R2022 and the MEMORY GATE WIDTH control, R2023. Therefore, these two resistors determine the length of time that Q2024 remains saturated, and thus the duration of the Memory Gate Driver output pulse. D2024 and R2024 reduce ringing in the collector circuit when Q2024 cuts off.

Snap-Off Circuit

Quiescently, the current-storage (snap-off) diode, D2004, is conducting with a forward current of about 10 to 80 milliamperes from —19 volts to ground, through the SNAP-OFF CURRENT control, R2007. This control adjusts the quiescent current and thus the storage of D2004. As transformer T2004 receives a positive pulse from the Blocking Oscillator, it converts the pulse to push-pull and applies

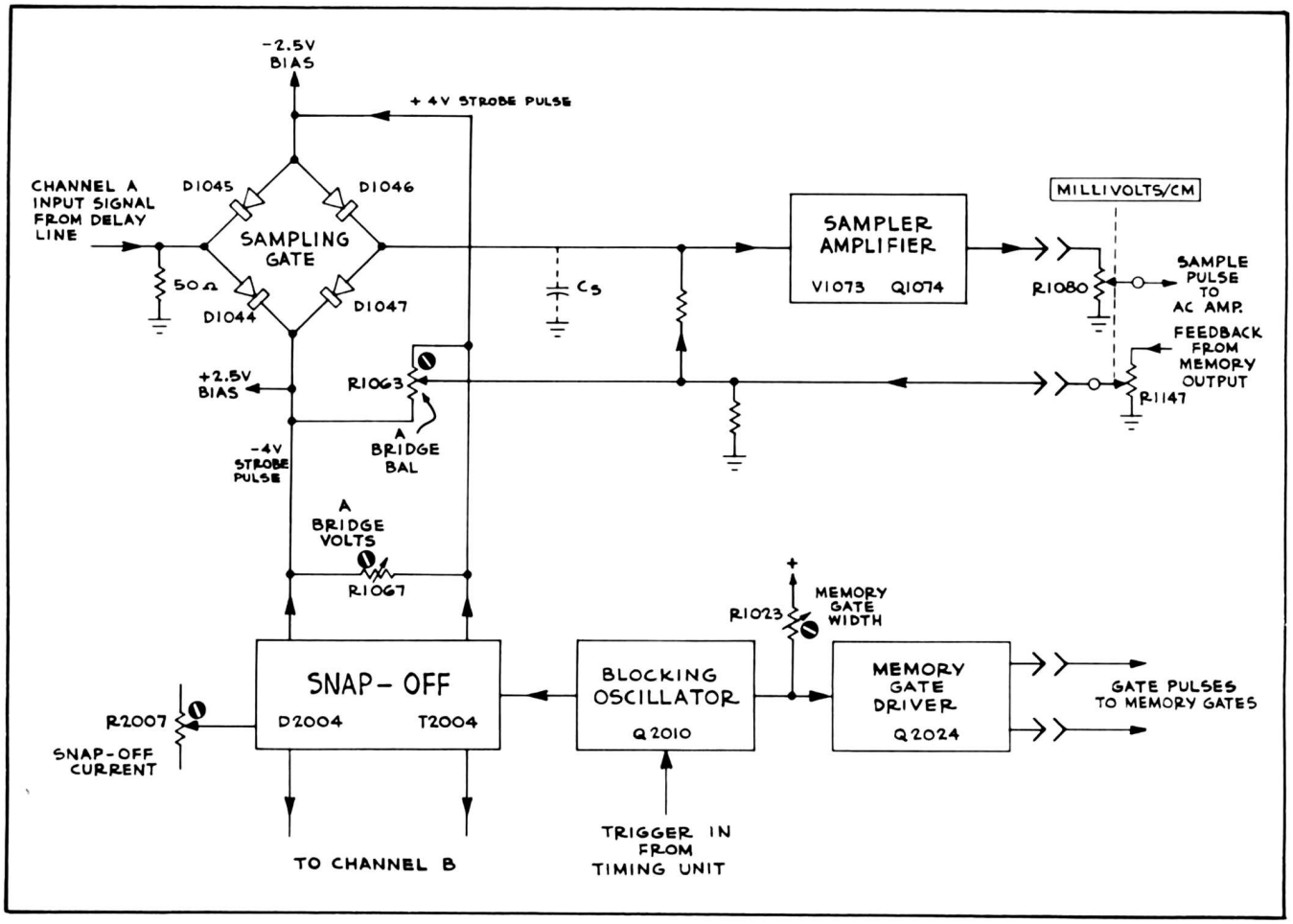


Fig.3-5. Block Diagram of Sampler.

it to D2004, which then begins to conduct heavily in the reverse direction as its stored charge is "swept out." This reverse current sends a heavy push-pull current pulse into the 50-ohm clipping line.

When the stored charge in the diode has been depleted, the current pulse ends sharply, forming push-pull voltage pulses at the input to the clipping line and the sampling bridge strobe leads. The voltage pulses pass through isolation and balancing circuitry to the Sampling Gate where they overcome the reverse bias of the bridge diodes and allow the Sampling Gate to pass the input signal for an instant. At the same time, the voltage pulses propagate down the clipping line, which is essentially a transmission line terminated in a short, and are reflected back as inverted pulses. When the inverted pulses reach the strobe leads, they cancel the strobe pulses, allowing the Sampling Gate to return to its normal non-conducting state. The double-transit time of the clipping line is approximately 0.35 nsec, establishing the duration of the sampling pulses. After D2004 has cut off, R2008 and C2008 act as a termination for the Blocking Oscillator until its pulse has ended. The reflection energy stored in C2004 discharges through the snap-off bias path before the next sample.

T1052 couples the push-pull strobe pulse to the corners of the sampling bridge and isolates the triggering circuitry and the bridge in the other channel from the signal input. L2057 and R2057 between the clipping line leads are provided to reduce multiple reflections of the strobe pulses.

Sampling Gate

The diodes in the Sampling Gate bridge (D1044 through D1047 in Channel A), are special gallium arsenide diodes with very fast switching characteristics. The delay line is terminated at the input to the Sampling Gate by the 50-ohm disc resistor, R1041, to prevent reflections.

Quiescently, the Sampling Gate bridge diodes are reverse biased, preventing passage of the input signal which is always connected through the delay line to the input of the bridge. Reverse bias is about 2.5 volts across each diode, set by the A BRIDGE VOLTS control, R1067. When a push-pull strobe signal from the Snap-Off circuit is received by the sampling bridge, about 1.5 volts of forward bias is applied across each of the four diodes, causing about 10 milliamps of forward current, and for a moment the diodes pass the applied input signal. Balance of the reverse bias is adjusted with the A BRIDGE BAL. control, R1063, so that no error-correction signals are produced when there is no voltage change at the input.

The Sampling Gate source resistance is 25 ohms, since the input circuit is a 50-ohm transmission line paralleled by a 50-ohm resistor. The response time of the Sampling Gate and the Sampler Amplifier grid circuit is determined by this resistance as well as by gate resistance, shunt stray capacitance and series inductance. The 0.35-nsec duration of the Snap-Off pulse, which is much shorter than the Sampler response time, limits the amplitude of the sampled signal to about 25% of the difference between the feedback level and the level of the new sample. If there is no difference between the feedback and the new sample level, no correction signal will pass through the channel, and the new dot will be displayed at the same level as the previous one.

The Blocking Oscillator, Snap-Off circuit and Sampling Gate are the critical circuits determining the effective duration of the strobe pulse, and thus the risetime of the unit. Because only about 25% of the difference signal gets through the Sampling Gate, leaving 75% of the Memory output signal to be made up by the amplifier stages, the Type 4S1 is said to have a sampling efficiency of 25%. A short time after the sample has been taken the positive feedback from the Memory output brings the level of the Sampling Gate output and strobe input corners up to the full signal value. Then the next sample corrects only for any change since the previous sample.

All the internal adjustments that control sampling efficiency for both channels are located on the Sampler subchassis. These are: SNAP-OFF CURRENT, R2007; MEMORY GATE WIDTH, R2023; A and B BRIDGE VOLTS, R1067 and R2067; and A and B BRIDGE BAL., R1063 and R2063.

Sampler Amplifier

The sampled pulses from the Sampling Gate are sent through L1070 to the Sampler Amplifier, consisting of V1073 and Q1074. V1073 amplifies the sample signal and sends it to the base of Q1074. The signal is amplified again by Q1074 and sent through blocking capacitor C1079 to the MILLIVOLTS/CM switch, SW1101, to be applied to the AC Amplifier. Amplification through the Sampler Amplifier circuit is about 2.5 times, and the output is stretched due to the capacitance at the input grid. The feedback loop from the collector of Q1074 to the cathode of V1073 sets the output amplitude and also bootstraps V1073 to keep the impedance of the grid circuit relatively high.

Because the amplitude of the pulses from the Sampling Gate is proportional to the change in signal amplitude since the previous sample, the output signal from the Sampler Amplifier is only the amplified and stretched correction signal.

ERROR-SIGNAL ATTENUATOR

The sample signal passes through attenuator R1080 (R2080 in Channel B), on its way from the Sampler Amplifier to the AC Amplifier. The value of R1080 is controlled by the position of the front-panel MILLIVOLTS/CM switch SW1101 (SW2101 in Channel B), which also operates the feedback attenuator. Sample attenuation at each step of the switch is set to maintain a loop gain of 1 in the feedback loop as the output signal amplitude is changed by the feedback attenuator. R1080 provides seven attenuation values, ranging from zero at the 2 mv/cm position to 100X at 200 mv/cm.

AC AMPLIFIER

Subchassis Series 2

The AC Amplifier subchassis contains an amplifier for each of the two channels. Since the two amplifiers are identical, only Channel A will be described. Refer to the block diagram in Fig. 3-6, and to the AC Amplifier schematic diagram.

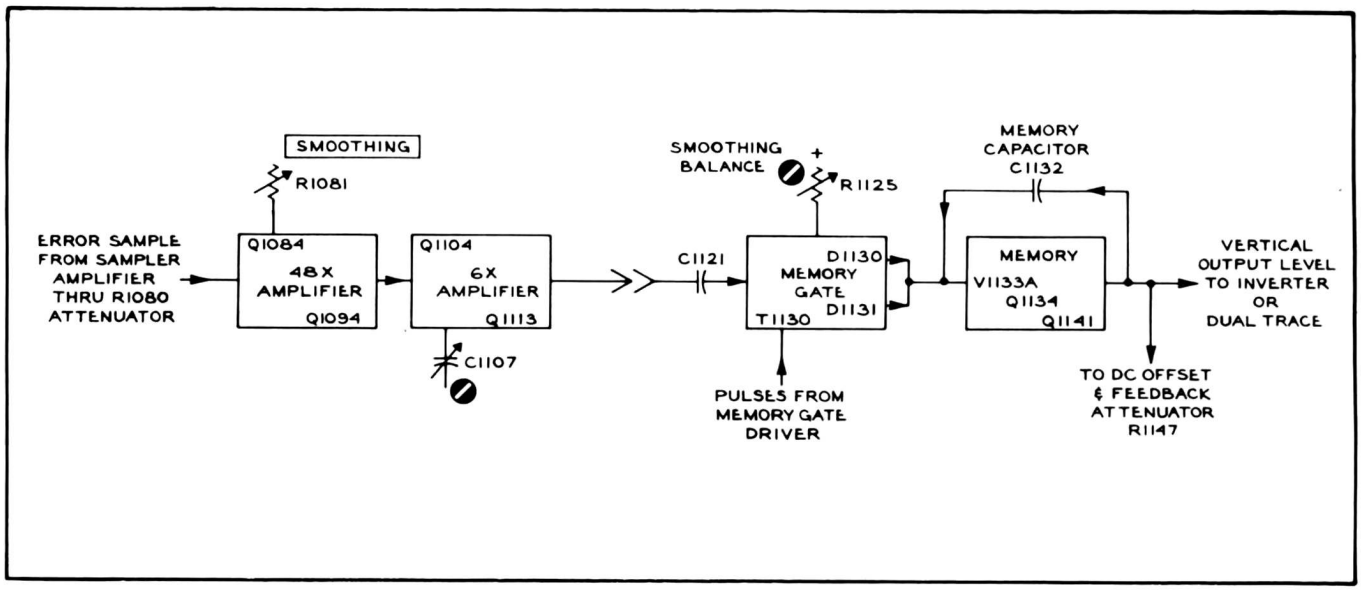


Fig. 3-6. Block Diagram of AC Amplifier and Memory.

The amplifier receives signals (correction samples) from the Sampler Amplifier through the MILLIVOLTS/CM switch, amplifies them about 280 times, inverts the signals and sends them to the Memory circuit.

The AC Amplifier is made up of two stages of amplification with dc-coupled feedback for each stage, and a third dc feedback path around the whole circuit. The input dc level is zero volts to ground, and the input resistance to ground ranges from 10 ohms at 200 mv/cm to 1000 ohms at 2 mv/cm. Dc stabilization provided by R1115 in the external feedback loop does not affect the pulse signals through the circuit. The external feedback path includes the front-panel SMOOTHING control, R1081, that allows a gain reduction of about four-to-one to reduce random noise.

When the SMOOTHING control is set to NORMAL (zero resistance), the gain of the first stage (Q1084 and Q1094) is about 48, set by the ratio of R1089 to R1083. When using full smoothing, the gain is about 9, set by the ratio of R1089 to R1083 and R1081 (SMOOTHING) in series. The gain of the second stage (Q1104 and Q1113) remains fixed at about 6, set by the ratio of R1107 to R1096.

The high-frequency stability of the first amplifier stage is determined by the fixed capacitor, C1089. Compensation of the second stage is adjusted during calibration by C1107.

The duration of signal pulses passed by the amplifier is about 1 μsec. Normally the feedback loop limits the amplitude of the AC Amplifier output pulses to less than 1 volt, but if the display has to move 8 centimeters in one sample, the output pulse will be about 1.6 volts peak. The output impedance of the circuit is low, so it is able to drive the Memory input.

MEMORY

Subchassis Series 3, 8 and 11

Located on the Memory subchassis are the Memory Gate, the Memory and the DC Offset circuits. The two channels have separate plug-in Memory subchassis.

Just before the Memory Gate receives the stretched error-correction sample, it is pulsed into conduction by the Memory Gate Driver, and passes the signal to the Memory circuit. The Memory Gate then is allowed to return to its normal non-conducting state before the output of the AC Amplifier returns to its quiescent level and before the feedback has had time to regenerate through the amplifiers. The Memory inverts the signal and stores its final value. The output of the Memory is connected to the Inverter or Dual-Trace circuit and a portion is also coupled back to the Sampler Amplifier to correct the input level.

Memory Gate

The Memory Gate consists of diodes D1130 and D1131, which are pulsed by the Memory Gate Driver through T1130. Refer to the Memory schematic diagram and to the block diagram in Fig. 3-6 during the following discussion. The purpose of the Memory Gate is to allow the sampled error-correction signal to pass through to drive the Memory circuit, but prevent the feedback signal from being sent back through the amplifiers into the Memory again as a new error signal. Although feedback is coupled through the amplification channel to C1121, it does not pass through the Memory Gate between samples. C1121 discharges through the Smoothing Balance network consisting of R1123, R1124, R1127 and the SMOOTHING BALANCE control, R1125, and the circuit returns to a normal quiescent state before the next sample is received.

The gate diodes are normally reverse biased by the voltage across zener diode D1122. When the Memory Gate Driver sends a pulse through T1130, a voltage is developed across each winding, forward biasing the diodes. The signal then passes from C1121 through the gate to the input of the Memory circuit. The MEMORY GATE WIDTH control in the Memory Gate Driver circuit adjusts the duration of conduction of the Memory Gate so that signals are transmitted as a result of sample pulses only. Capacitor C1122 assures that both sides of D1122 follow the signal equally well.

The dc level at the Memory Gate input is set by the Smoothing Balance divider network. The balance is adjusted during calibration so that with no error signal present at the input, there will be no change in the Memory output level. Imbalance in the dc level is seen as trace shift when the SMOOTHING control is operated, thus the control for adjusting the Memory input balance is called the SMOOTHING BALANCE control (early models were called MEMORY BALANCE). Diodes D1125 and D1127, which limit the signal amplitudes, are normally not conducting.

Memory Circuit

The Memory circuit is a feedback amplifier which has capacitors for both the input and the feedback elements. A block diagram of the Memory is shown in Fig. 3-6. The input capacitor is C1121, and the feedback (memory) capacitor is C1132. V1133A is the input cathode follower, Q1134 is the amplifier, and Q1141 is an output emitter follower. Although gain of the Memory is only a little more than 3, set by the ratio of C1132 to C1121, high gain capability is needed to keep the excursion at the grid of V1133A very small compared to the Memory output.

The action of the Memory develops a charge on C1132 opposing the charge applied to C1121. The circuit between the input to R1121 and the grid of V1133A is effectively 150 ohms in series with 510 pf when the Memory Gate is conducting. As a sample signal is received by C1121 from the AC Amplifier, this capacitor couples the pulse to the grid of V1133A. The input impedance in the grid circuit is very high, and any tendency for the grid level to change is amplified and returned as negative feedback through C1132, holding the grid level practically stationary. This feedback action places a charge on C1132 equal to that applied to the input capacitor. Then the Memory Gate disconnects the Memory before the stretched pulse from the AC Amplifier has ended, and C1132 is left in a charged condition. Between samples, C1121 discharges through the Smoothing Balance network, and the AC Amplifier output returns to a quiescent level. At the next sample, if there is a change at the input, C1121 will receive the new signal and will add or subtract the new signal from the residual charge on C1132, depending on whether the new level is above or below the previous value. Grid current in V1133A is very

low, and total leakage from C1132 and diodes D1130 and D1131 is very small, so there is essentially no change in the Memory output voltage between samples, even when sampling at the low rate of 50 samples/second. Memory drift or "dot slash" at sampling rates in the range below 50 samples/second is caused by small leakage currents.

The following components in the Memory circuit perform the indicated functions: C1138 in the collector circuit of Q1134 corrects for transistor phase shift; D1136 determines the emitter voltage of Q1134; D1143 limits the positive swing of the output to the value determined by D1144; D1140 limits the negative swing of the output by setting the voltage on the collector of Q1141 and limiting the emitter to this value as the transistor saturates; R1145 suppresses reverse reflections in the output cable. The emitter-to-base junction of Q1141 is protected from over-voltage by D1142.

FEEDBACK LOOP

Each channel has a feedback loop consisting of the feedback attenuator, the Sampling Gate, the Sampler Amplifier, the error-signal attenuator, the AC Amplifier, the Memory Gate and the Memory. The purpose of the loop is to set the signal gain of the channel and to correct for the 25% sampling efficiency of the Sampling Gate. The loop in Channel B is identical to the Channel A loop described in the following paragraphs.

Since the Memory output level determines the level of each displayed sample, the amount of attenuation introduced into the feedback loop sets the signal gain by establishing the ratio between the voltage level at the Memory output and that at the Sampling Gate. The voltage excursion sent back to the Sampling Gate must be the same as that of the input signal, therefore the Memory output amplitude will change in proportion to the feedback attenuation. The front-panel MILLIVOLTS/CM switch operates the feedback attenuator, R1147, providing seven values of attenuation that range from 300X at the 2 mv/cm position of the switch, to 3X at the 200 mv/cm position.

For best response the feedback signal following each sample must be of the amplitude required to bring the level at the Sampling Gate up to the level of the input signal at the previous sampling instant. When it is set to do this, the loop is said to have a gain of 1. As feedback attenuation is increased, to change the signal gain, amplification of the error-correction samples must also be increased to keep the feedback loop gain at 1. Since the gain of the amplifiers is fixed, the additional amplification is produced by allowing more of the error-correction signal to pass through attenuator R1080 to the AC Amplifier. Thus, the error-signal attenuation produced by R1080 must decrease as the feedback attenuation of R1147 is increased. These two attenuators are operated simultaneously by the MILLIVOLTS/CM switch, SW1101.

Random noise through the system can be reduced by decreasing the gain of the feedback loop. The front-panel SMOOTHING control changes the loop gain without affecting the output amplitude, by reducing amplification in the first stage of the AC Amplifier. Smoothing also reduces the response of the system by allowing the feedback voltage to lag slightly behind the input signal changes, but it does not normally change the appearance of the display unless the dot density is too low. The display must have a dot density great enough for the feedback to follow the signal, or the transient response will be affected and the display amplitude may be reduced.

DC Offset

The DC Offset circuit consists of a cathode follower which introduces dc shift into the feedback loop. Fig. 3-7 is a block diagram of the DC Offset injection circuit. The grid voltage of V1133B is set by a resistance divider that includes the front-panel DC OFFSET control, R1159, in the main frame of the Type 4S1. Rotating the DC OFFSET control from one end to the other causes a −50-volt to +50-volt swing at the cathode of V1133B. The cathode swing, following the grid, produces a ±0.25-milliamp change through R1146. The DC OFFSET control ±100-volt swing also causes a ±0.50 milliamp change in current through R1149. The resulting voltage drop of ±1 volt across both R1146 and R1149 is the offset voltage injected into the feedback loop on both sides of attenuator R1147. Adding the dc offset voltage at these two points assures that no offset current will flow in R1147, so there will be no interaction between operation of the feedback attenuator and of the offset circuit.

The front-panel OFFSET MONITOR jack permits connection of a voltmeter for reading the offset voltage amplified 100 times.

INVERTER

Subchassis Series 4 and 9

The Inverter consists of two X1 amplifiers, one for each channel, with inverted output signals. The function of each amplifier is to invert the display when the front-panel DISPLAY switch is in the INVERTED position. The following description pertains to Channel A. Operation of the Channel B Inverter is identical. Refer to the Inverter diagram in the Schematics section.

The Inverter input transistor, Q1164, is collector-coupled through D1167 to the output emitter follower, Q1163. D1167 is a voltage-offset zener diode that raises the voltage at the base of Q1163 above that at the collector of Q1164, without producing signal attenuation. R1161, the A INVERTER ZERO, and R1162 are a dc-balance network for adjusting the output dc level to eliminate trace shift when moving the DISPLAY switch from NORMAL to INVERTED. R1163 is the feedback resistor in the negative feedback loop.

With the DISPLAY switch set to INVERTED, the inverted output is connected to the Dual Trace circuit. When the DISPLAY switch is at NORMAL, the Inverter is bypassed through interconnecting wiring in the main frame of the Type 4S1, and the signal from the Memory is applied directly to the Dual Trace circuit.

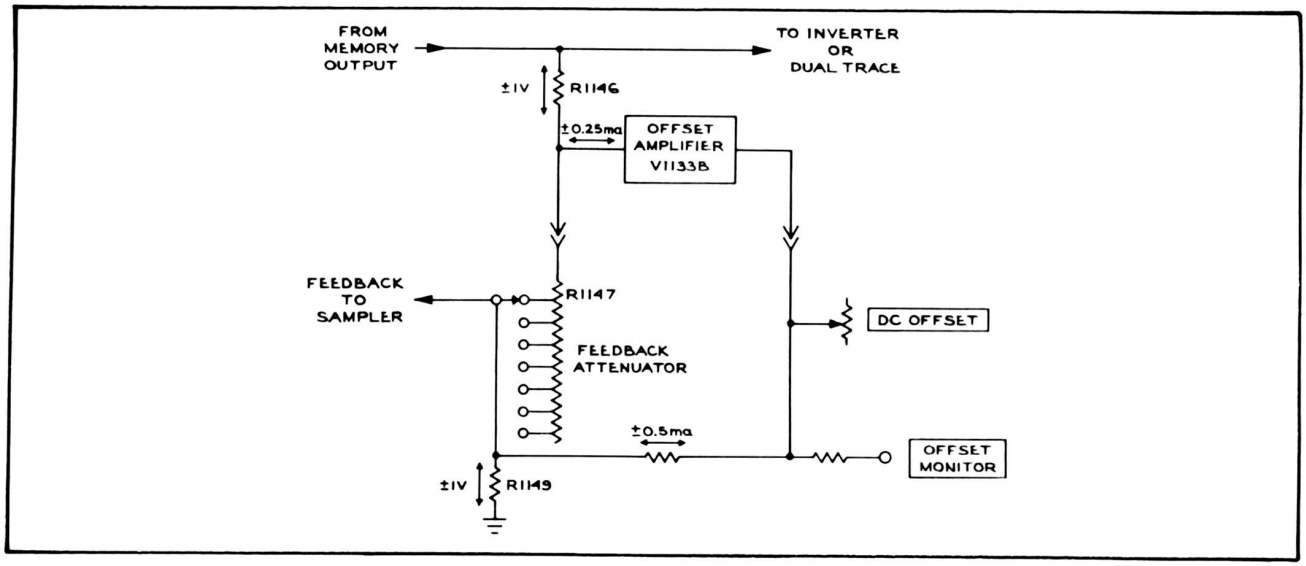


Fig. 3-7. DC Offset Injection and Memory Feedback.

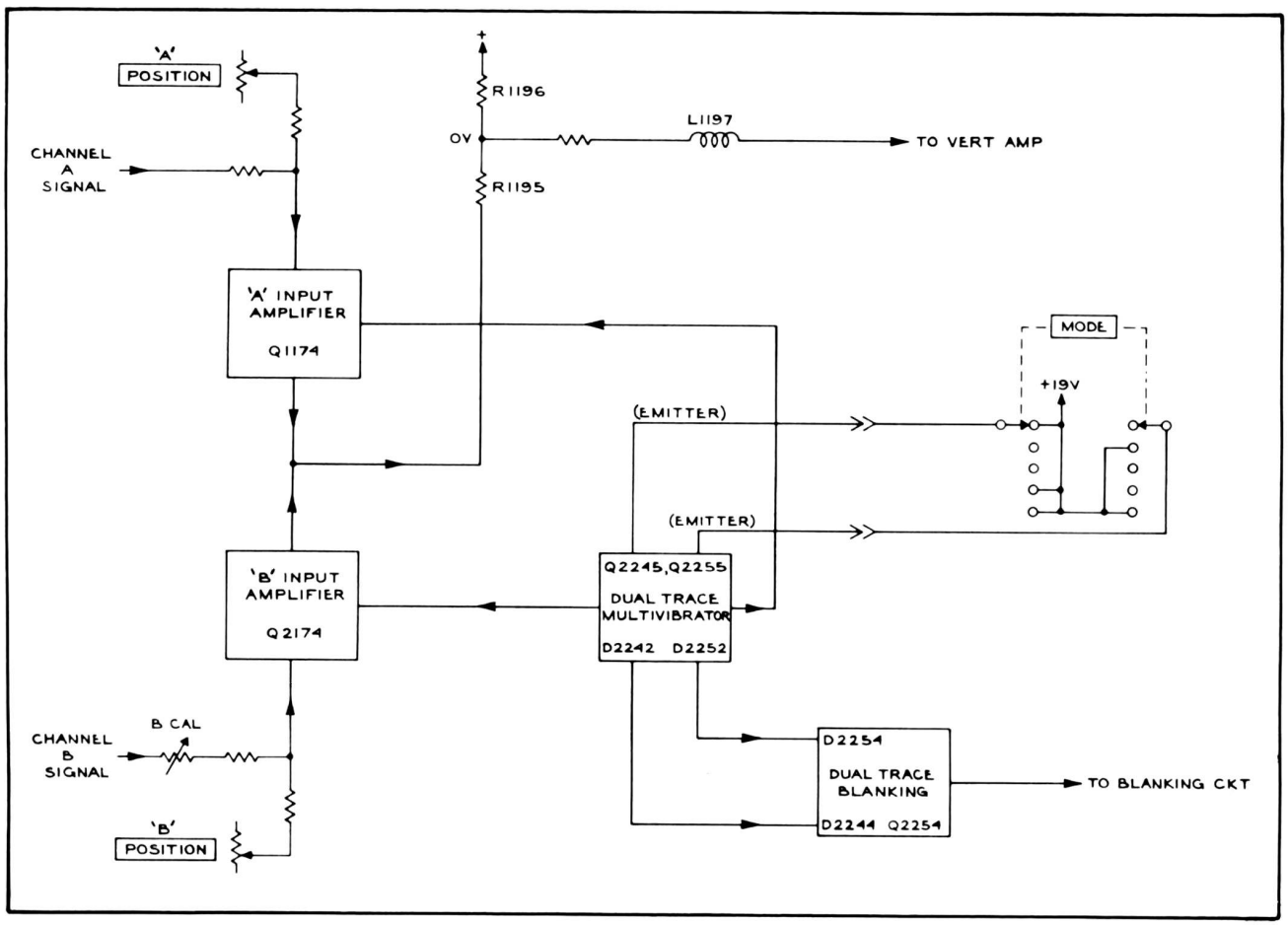


Fig. 3-8. Dual Trace Block Diagram, Models 1 and 2.

DUAL TRACE

Subchassis 5

The Dual Trace circuitry determines which channel signal is allowed to be displayed by the oscilloscope. In some modes, both signals pass through the Dual Trace circuit. Figs. 3-8 and 3-9 are block diagrams of the Dual Trace circuitry. Because of the various modes of operation possible, both channels will be discussed.

Models 1 and 2 Only

Passage of the signals from the two channels is controlled by the two inverter amplifier transistors, Q1174 and Q2174, which are gated by the multivibrator, Q2245 and Q2255. Emitter voltage determining the mode of operation is applied to the multivibrator through the front-panel MODE switch. A 0.25-μsec delay line couples the signal from the Dual Trace circuit to the oscilloscope vertical output amplifier. This delay allows the signal to phase properly with the timing unit unblanking of the crt.

In the A ONLY and A VERT. B HORIZ. modes, only transistor Q2245 is energized, and in the B ONLY mode only Q2255 has voltage applied. In the ADDED ALGEB. mode neither transistor is conducting, and in the DUAL TRACE mode both are conducting. The multivibrator free runs in DUAL TRACE mode, at a switching rate of about 50 kc. Q2254 provides a dual-trace blanking signal to the oscilloscope when the multivibrator is switching.

Each of the Dual Trace input transistors receives its respective channel signal from the Memory or Inverter circuit through the DISPLAY switch, the VARIABLE control, and the display gain control. The signal is applied to the emitter circuit, which also provides positioning voltage through the front panel POSITION control (R1180 or R2180) and R1181 or R2181. The major emitter current path is from the +19-volt supply, through the MODE switch, SW2190, and through R1176 and R2176 to the two emitters. In the ADDED ALGEB. position of the MODE switch, current-limiting resistor R1179 (in the Type 4S1 switching circuitry) is inserted in the emitter circuit to keep the average voltage on the common lead the same as when only one transistor is conducting. The input inverter transistors are connected in the common base configuration. The voltage at each base is switched between two levels by the multivibrator to turn the transistors on or off.

In the A ONLY mode, transistor Q2255 is not conducting. Its collector, and thus the base of Q1174, is held at about —0.3 volt by D1184, so Q1174 conducts, passing the Channel A signal through R1195 and R1197 to the delay line. Transistor Q2245 is turned on by the MODE switch, with the emitter connected to the +19-volt supply through R2241. This sets the collector voltage of Q2245 and the base of Q2174 at about +3.3 volts, cutting off Q2174 in the Channel B signal path.

In the B ONLY mode, operation of the multivibrator and input transistors is just the opposite of operation in A ONLY. Q2255 is conducting, Q2245 and Q1174 are cut off and Q2174 is passing Channel B signal.

In the ADDED ALGEB. mode, neither transistor is supplied from the +19-volt supply and both are turned off. Thus both input transistors are conducting, allowing signals to pass. The output to the delay line then is the algebraic sum of the Channel A and Channel B signals.

Operation of the Dual Trace circuit in the A VERT. B HORIZ. mode is the same as in A ONLY. The Channel B signal bypasses the Dual Trace circuit and is applied through other circuitry to the horizontal deflection system of the oscilloscope.

In the DUAL TRACE mode, both Q2245 and Q2255 are energized, and operate as a free-running multivibrator at approximately 50 kc (some units operate at 40 kc). During dual-trace operation, the multivibrator switching time is determined by C2241 in series with the emitter-return resistor of the transistor that is not conducting (R2241 or R2251). As the collectors of the two multivibrator transistors alternately go negative, then positive, the input transistors alternately allow the Channel A signal to pass, then the Channel B signal, producing the dual-trace display. The collector-to-base coupling circuits (R2243-C2243 and R2253-C2253) are for high-frequency coupling to assure fast switching, and do not set the switching time.

Blanking transistor Q2254 normally rests in cutoff. As the multivibrator switches, C2244 or C2254 couples a negative pulse to the base of Q2254, turning it on. The 2 μsec positive blanking pulse from the collector is fed through the interconnecting wiring of the Type 4S1 main frame to the oscilloscope blanking circuit.

Model 3

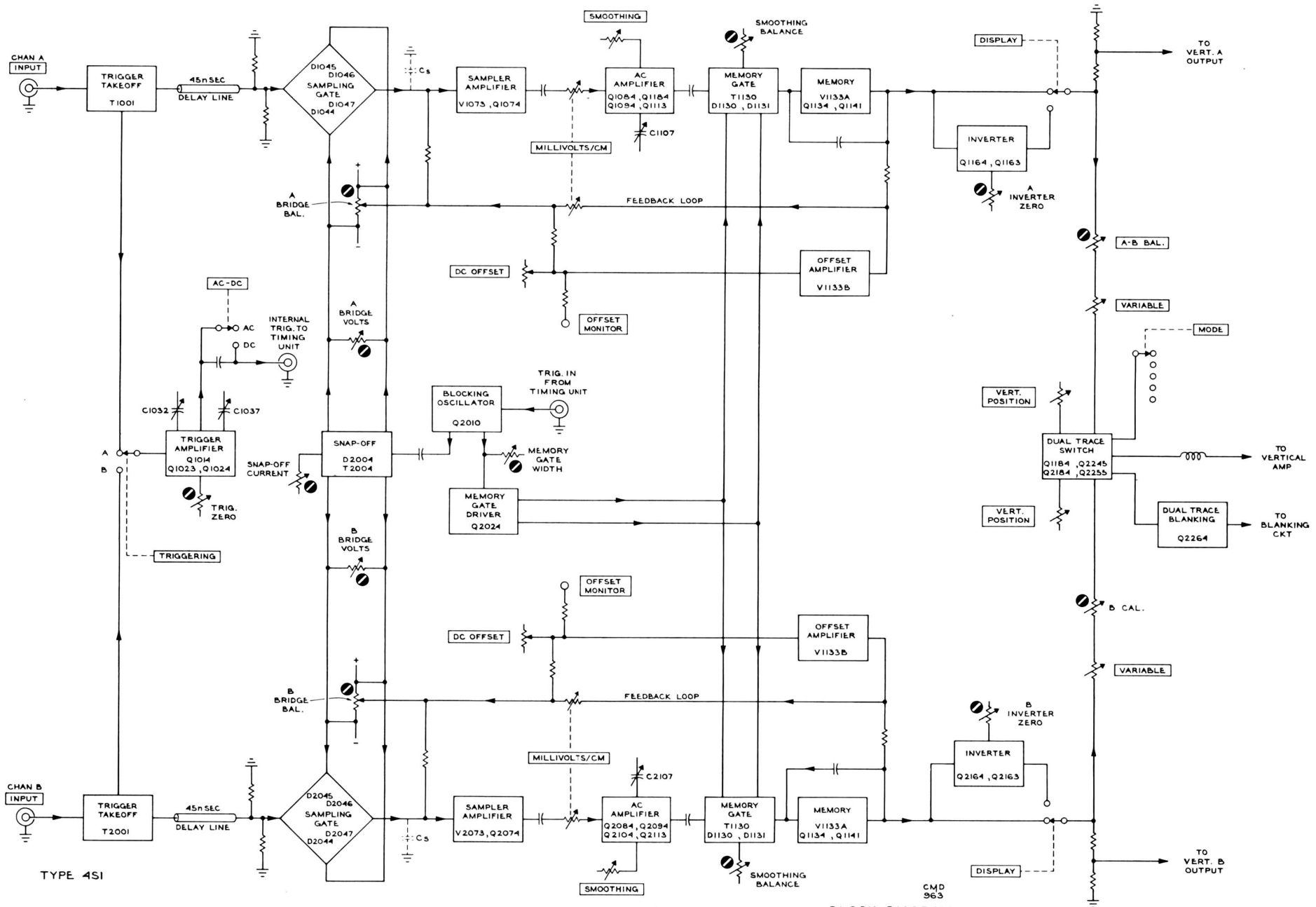
Passage of the signals from the two channels is controlled by the two diode gates in the collector circuit of input amplifier transistors, Q1184 and Q2184. The diode gates are controlled by the state of multivibrator Q2245 and Q2255. The mode of operation of the multivibrator is determined by positive voltage applied through the MODE switch to the bases of the multivibrator transistors. See Fig. 3-9. A 0.25-μsec delay line couples the signal from the Dual Trace circuit to the oscilloscope vertical output amplifier. This delay allows the signal to phase properly with the timing unit unblanking of the crt.

In the A ONLY and A VERT. B HORIZ. modes, only transistor Q2255 conducts, and in the B ONLY mode only Q2245 conducts. In the ADDED ALGEB. mode both transistors are conducting, and in the DUAL TRACE mode, the multivibrator free runs at a switching rate of about 50 kc. Q2264 provides a dual-trace blanking signal to the oscilloscope when the multivibrator is switching.

Each of the dual trace input transistors receives its respective channel signal from the Memory or Inverter circuit through the DISPLAY switch, the VARIABLE control and the display gain control. The signal is applied to the emitter circuit, which also provides positioning voltage through the front panel POSITION control (R1180 or R2180) and through R1181 or R2181. The major emitter current path is from the +19-volt supply, through the MODE switch, SW2190, and through R1185 and R2185 to the two emitters. In the ADDED ALGEB. position of the MODE switch, current-limiting resistor R1179 (in the Type 4S1 main-frame circuitry) is inserted in the current path to keep the average voltage on the common lead the same as when only one transistor is passing signal to the output. The input transistors are con-

emitter return resistor of the nonconducting side (R2240 or R2250). The collector-to-base coupling circuits (R2246-C2246 and R2256-C2256) are for high-frequency coupling to assure fast switching, and do not set the switching time.

Blanking transistor Q2264 normally rests in cutoff with its base at about +0.8 volt. As the multivibrator switches, C2240 or C2250 couples about a —2-volt signal to the base of Q2264, turning it on. The pulse lasts only about 0.5 μsec, but this is long enough to saturate Q2264. Storage time of the blanking transistor is about 1 μsec to 1.5 μsec and is consistent for a particular instrument, so that the crt will be properly blanked during the time that the dual-trace multivibrator is switching channels.

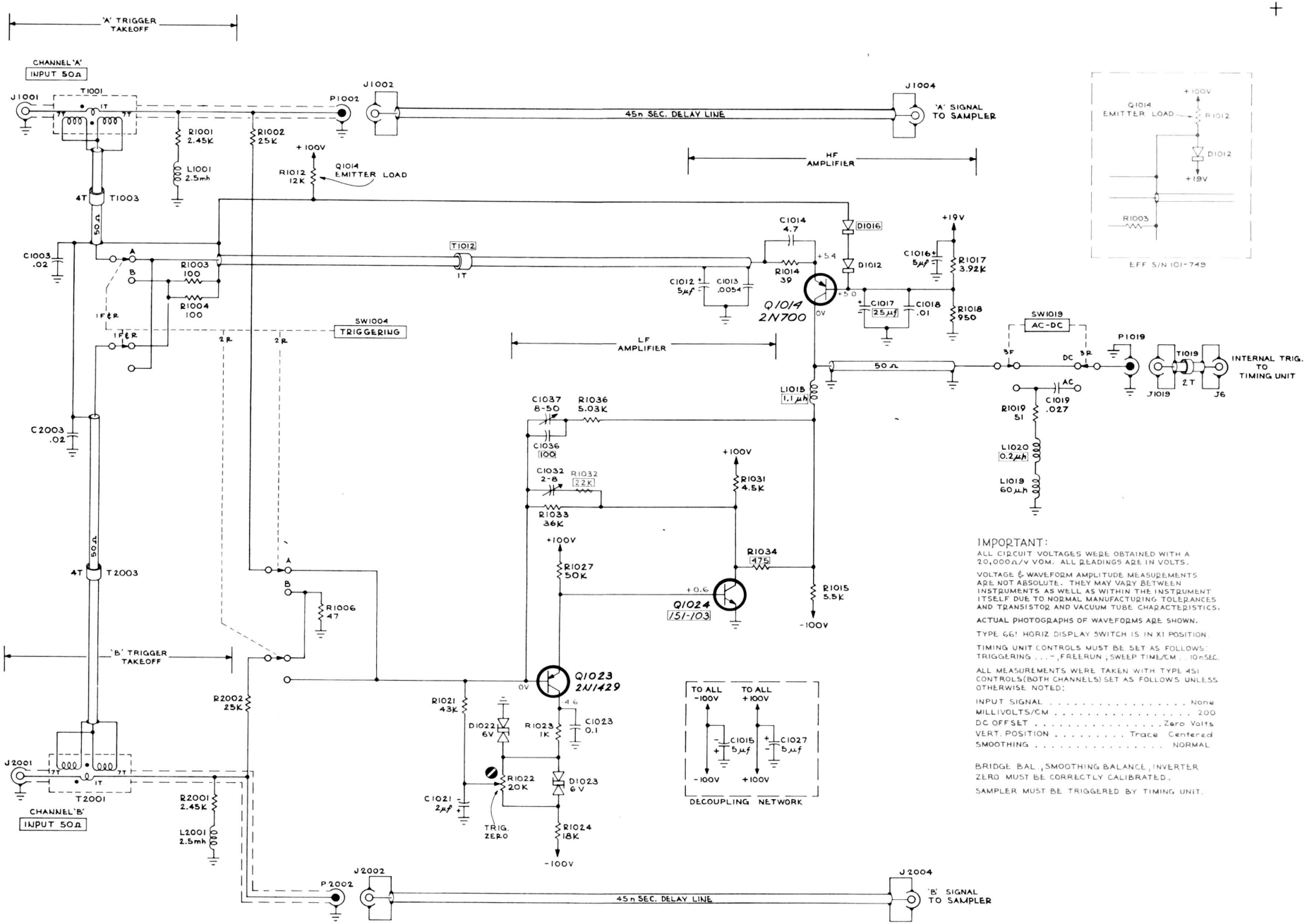


TYPE 451

CMD 963

A

BLOCK DIAGRAM



IMPORTANT:

ALL CIRCUIT VOLTAGES WERE OBTAINED WITH A 20,000Ω/V VOM. ALL READINGS ARE IN VOLTS.

VOLTAGE & WAVEFORM AMPLITUDE MEASUREMENTS ARE NOT ABSOLUTE. THEY MAY VARY BETWEEN INSTRUMENTS AS WELL AS WITHIN THE INSTRUMENT ITSELF DUE TO NORMAL MANUFACTURING TOLERANCES AND TRANSISTOR AND VACUUM TUBE CHARACTERISTICS.

ACTUAL PHOTOGRAPHS OF WAVEFORMS ARE SHOWN.

TYPE 66' HORIZ DISPLAY SWITCH IS IN X1 POSITION.

TIMING UNIT CONTROLS MUST BE SET AS FOLLOWS: TRIGGERING ...=, FREERUN, SWEEP TIME/CM. 10nSEC.

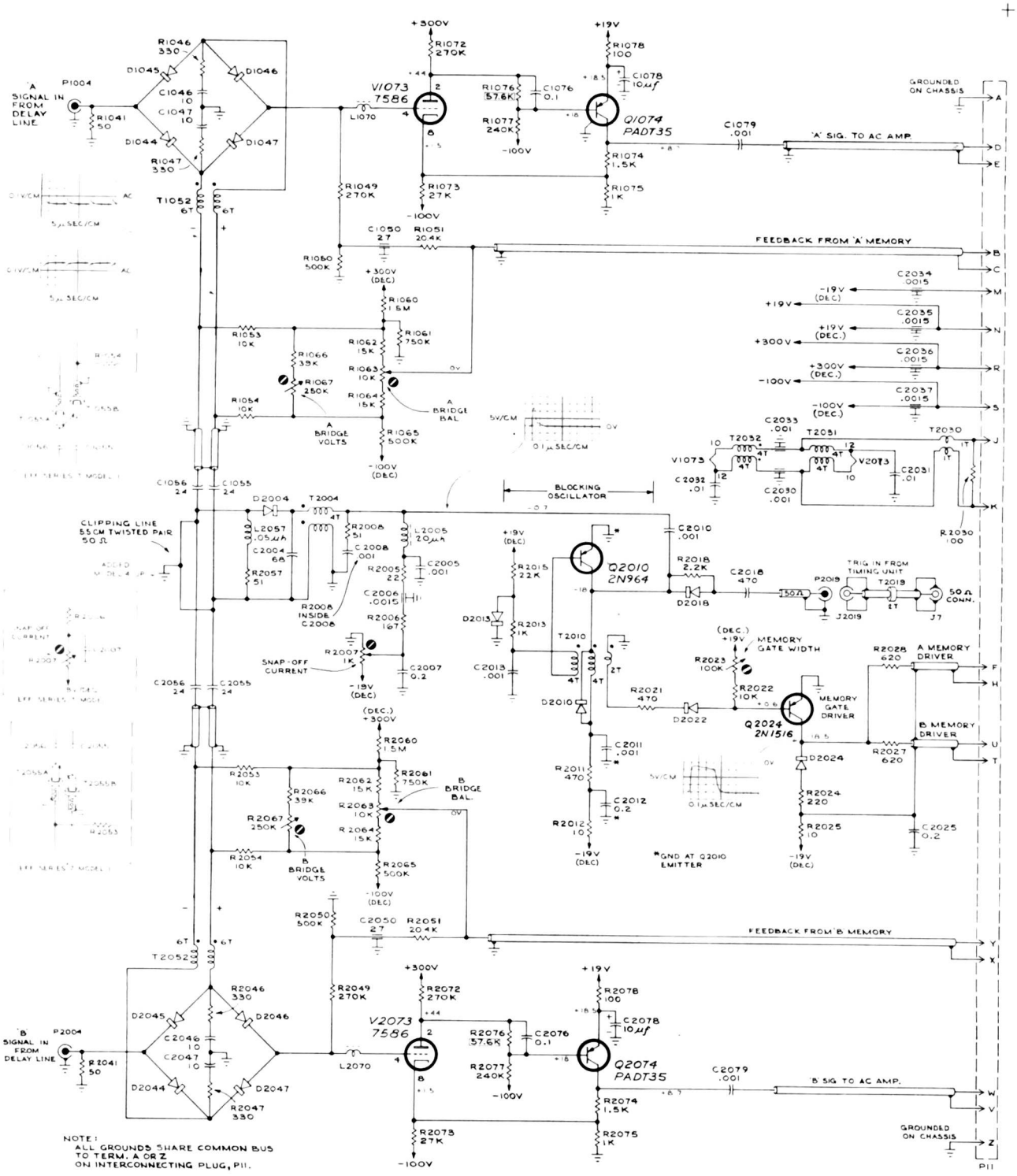
ALL MEASUREMENTS WERE TAKEN WITH TYPE 451 CONTROLS (BOTH CHANNELS) SET AS FOLLOWS UNLESS OTHERWISE NOTED:

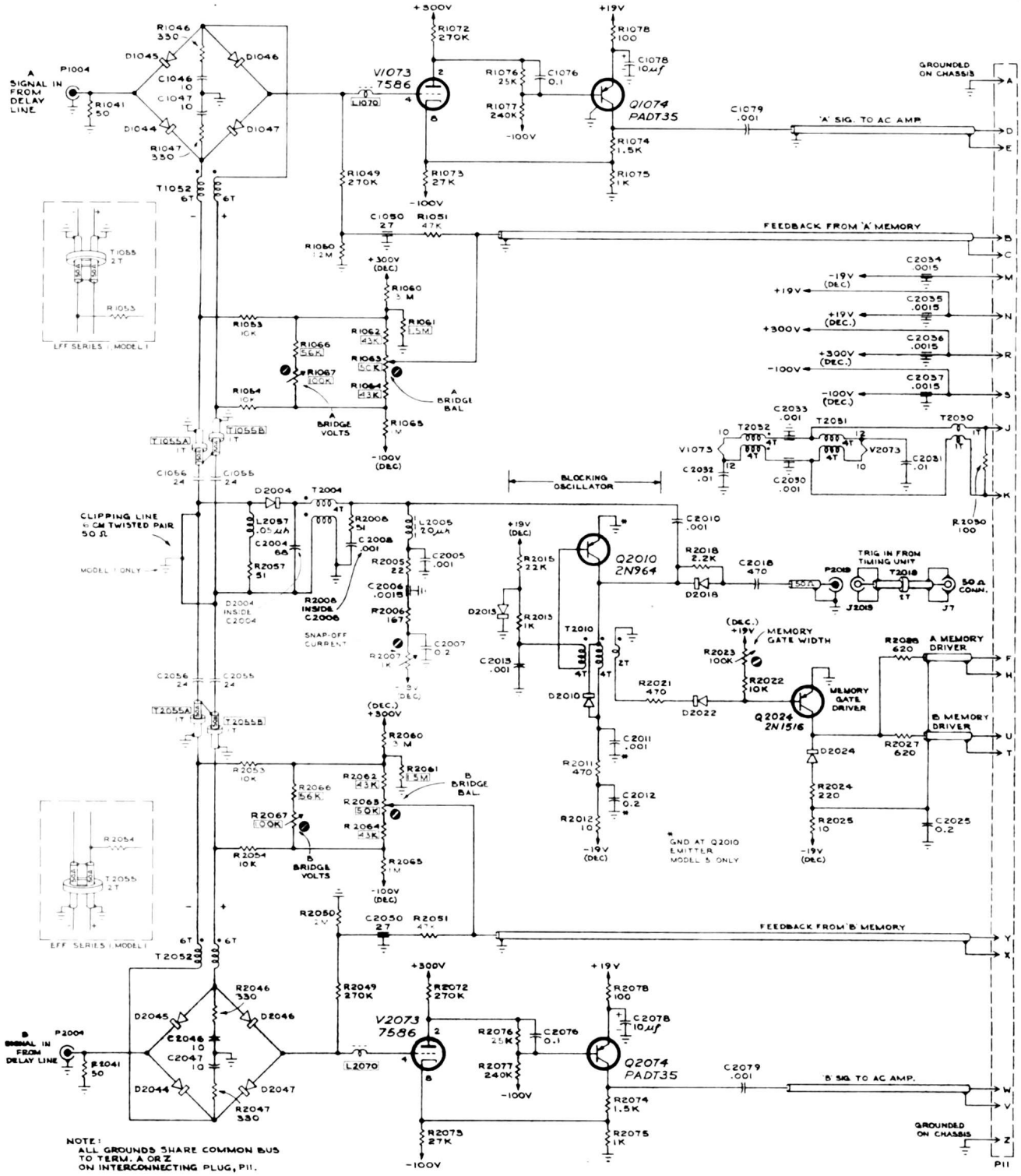
INPUT SIGNAL	None
MILLIVOLTS/CM	200
DC OFFSET	Zero Volts
VERT. POSITION	Trace Centered
SMOOTHING	NORMAL

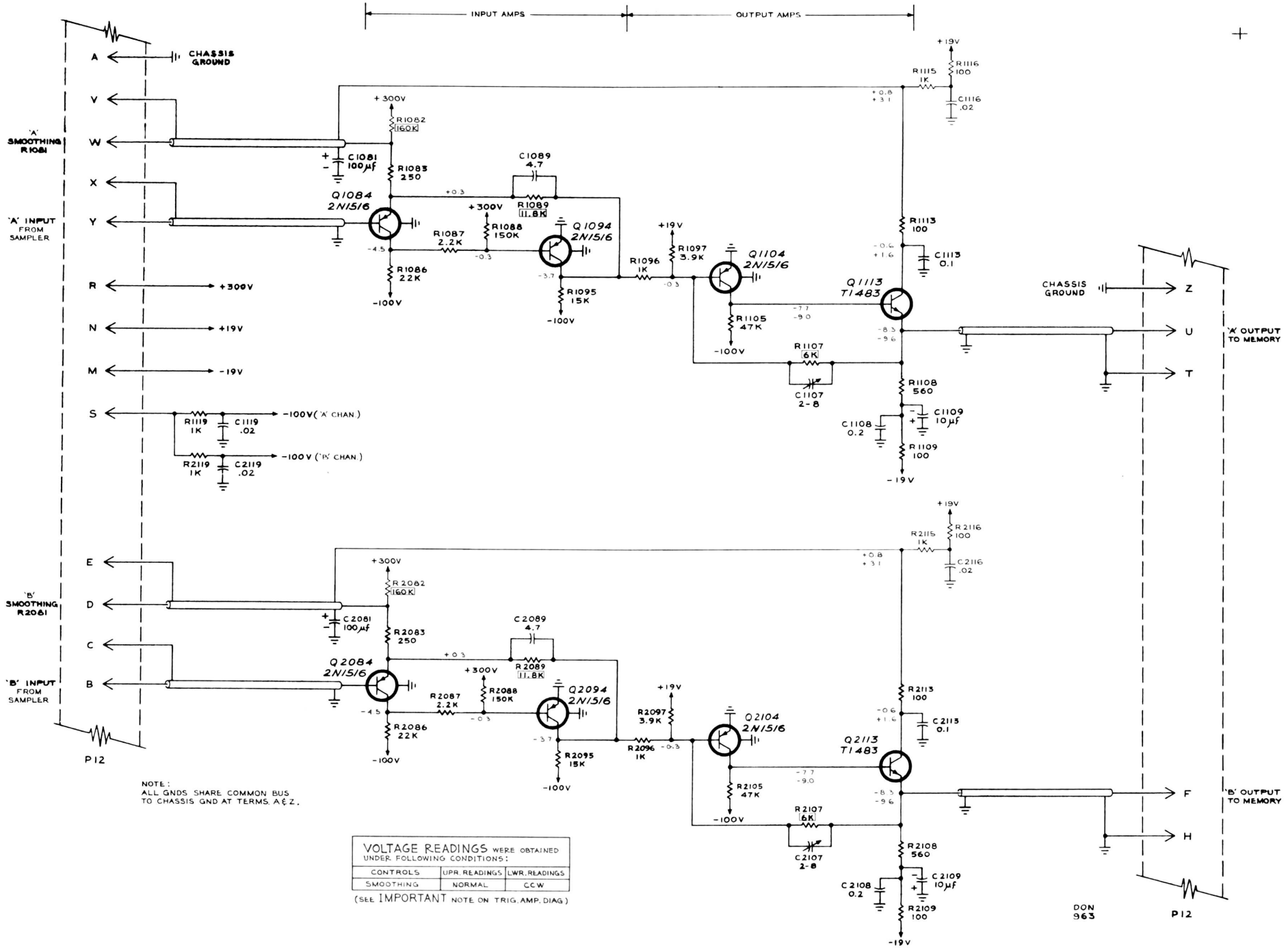
BRIDGE BAL., SMOOTHING BALANCE, INVERTER ZERO MUST BE CORRECTLY CALIBRATED.

SAMPLER MUST BE TRIGGERED BY TIMING UNIT.

TRIGGER AMPLIFIER


'A' SIGNAL IN FROM DELAY LINE
P1004
R1041 50
R1046 330
R1047 330
D1045
D1046
D1044
D1047
C1046 10
C1047 10
T1052
6T
6T
R1049 270K
L1070
V1073 7586
+300V
R1072 270K
+44
-100V
R1073 27K
+19V
R1078 100
C1078 10μf
R1076 57.6K
C1076 0.1
R1077 240K
-100V
Q1074 PADT35
R1074 1.5K
R1075 1K
C1079 .001
'A' SIG. TO AC AMP.
GROUNDED ON CHASSIS
A
D
E
C1050 27
R1051 20.4K
R1050 500K
FEEDBACK FROM 'A' MEMORY
B
C
+300V (DEC.)
R1060 1.5M
R1053 10K
R1066 39K
R1062 15K
R1061 750K
R1063 10K
R1067 250K
R1064 15K
R1054 10K
A BRIDGE BAL.
A BRIDGE VOLTS
R1065 500K
-100V (DEC.)
0V
5V/CM
0.1μSEC/CM
C1056 24
C1055 24
BLOCKING OSCILLATOR
D2004
T2004
4T
CLIPPING LINE 55CM TWISTED PAIR 50Ω
L2057 .05μh
C2004 68
R2057 51
R2008 51
L2005 20μh
C2008 .001
C2005 .001
R2005 22
C2006 .0015
R2006 16T
R2008 INSIDE C2008
R2007 1K
SNAP-OFF CURRENT
C2007 0.2
-15V (DEC.)
C2056 24
C2055 24
C2010 .001
+19V (DEC.)
R2015 22K
Q2010 2N964
R2018 2.2K
C2018 470
D2018
150Ω
P2019
J2019
TRIG IN FROM TIMING UNIT
T2019
1T
50Ω CONN.
J7
D2013
R2013 1K
C2013 .001
T2010
2T
4T
4T
R2021 470
D2010
D2022
(DEC.) +19V
MEMORY GATE WIDTH
R2023 100K
R2022 10K
MEMORY GATE DRIVER
Q2024 2N1516
D2024
R2024 220
R2025 10
-19V (DEC.)
C2025 0.2
R2028 620
A MEMORY DRIVER
F
H
B MEMORY DRIVER
R2027 620
U
T
C2011 .001
R2011 470
C2012 0.2
R2012 10
-19V (DEC.)
*GND AT Q2010 EMITTER
5V/CM
0.1μSEC/CM
C2033 .001
T2032
T2031
T2030
V1073
V2073
C2032 .01
C2030 .001
C2031 .01
1T
R2030 100
J
K
C2034 .0015
-19V (DEC.)
+19V
M
C2035 .0015
+19V (DEC.)
+300V
N
C2036 .0015
+300V (DEC.)
-100V
R
C2037 .0015
-100V (DEC.)
S
(DEC.) +300V
R2060 1.5M
R2053 10K
R2066 39K
R2062 15K
R2061 750K
R2063 10K
R2067 250K
R2064 15K
R2054 10K
B BRIDGE BAL.
B BRIDGE VOLTS
R2065 500K
-100V (DEC.)
0V
R2050 500K
C2050 27
R2051 20.4K
FEEDBACK FROM 'B' MEMORY
Y
X
6T
6T
T2052
'B' SIGNAL IN FROM DELAY LINE
P2004
R2041 50
R2046 330
R2047 330
D2045
D2046
D2044
D2047
C2046 10
C2047 10
L2070
V2073 7586
+300V
R2072 270K
+44
-100V
R2073 27K
R2049 270K
+19V
R2078 100
C2078 10μf
R2076 57.6K
C2076 0.1
R2077 240K
-100V
Q2074 PADT35
R2074 1.5K
R2075 1K
C2079 .001
'B' SIG. TO AC AMP.
GROUNDED ON CHASSIS
W
V
Z
P11
NOTE: ALL GROUNDS SHARE COMMON BUS TO TERM. A OR Z ON INTERCONNECTING PLUG, P11.


A SIGNAL IN FROM DELAY LINE
P1004
R1046 330
D1045
D1046
C1046 10
C1047 10
D1044
D1047
R1047 330
R1041 50
T1052 6T 6T
V1073 7586
L1070
+300V
R1072 270K
R1076 25K
C1076 0.1
R1077 240K
-100V
+19V
R1078 100
C1078 10μf
Q1074 PADT35
C1079 .001
'A' SIG. TO AC AMP.
R1074 1.5K
R1075 1K
R1049 270K
R1073 27K
-100V
C1050 27
R1051 47K
R1050 2.2M
FEEDBACK FROM 'A' MEMORY
GROUNDED ON CHASSIS
A
B
C
M
N
R
S
J
K
C2034 .0015
-19V (DEC.)
+19V
C2035 .0015
+19V (DEC.)
+300V
C2036 .0015
+300V (DEC.)
-100V
C2037 .0015
-100V (DEC.)
C2033 .001
T2050
T2051
T2052
V1073
V2073
C2032 .01
C2030 .001
C2031 .01
R2030 100
T1055 EFF SERIES 1 MODEL 1
T1055A 1T
T1055B 1T
R1053 10K
R1066 56K
R1067 100K
R1064 43K
R1063 50K
R1062 43K
R1061 1.5M
R1060 3 M
+300V (DEC.)
R1065 1M
-100V (DEC.)
A BRIDGE BAL
A BRIDGE VOLTS
C1056 24
C1055 24
BLOCKING OSCILLATOR
D2004
T2004
CLIPPING LINE 4 CM TWISTED PAIR 50 Ω
MODEL 1 ONLY
L2007 .05 μh
C2004 68
R2057 51
D2004 INSIDE C2004
L2005 20 μh
C2008 .001
R2008 51
R2008 INSIDE C2008
C2005 .001
R2005 22
C2006 .0015
R2006 167
R2007 1K
C2007 0.2
SNAP-OFF CURRENT
-19V (DEC.)
C2010 .001
Q2010 2N964
R2018 2.2K
C2018 470
D2018
TRIG IN FROM TIMING UNIT
P2018
T2018
J2018
50 Ω CONN.
J7
+19V (DEC.)
R2015 22K
D2015
R2015 1K
C2015 .001
T2010
D2010
R2021 470
D2022
(DEC.) +19V MEMORY GATE WIDTH
R2023 100K
R2022 10K
MEMORY GATE DRIVER
Q2024 2N1516
R2086 620
A MEMORY DRIVER
F
H
B MEMORY DRIVER
R2027 620
U
T
D2024
R2024 220
R2025 10
C2025 0.2
-19V (DEC.)
C2011 .001
R2011 470
C2012 0.2
R2012 10
-19V (DEC.)
* GND AT Q2010 EMITTER MODEL 5 ONLY
C2056 24
C2055 24
T2055A 1T
T2055B 1T
R2053 10K
R2066 56K
R2067 100K
R2054 10K
B BRIDGE BAL
B BRIDGE VOLTS
R2060 3 M
R2061 1.5M
R2062 43K
R2063 50K
R2064 43K
R2065 1M
-100V (DEC.)
T2055 EFF SERIES 1 MODEL 1
R2050 2M
C2050 27
R2051 47K
FEEDBACK FROM 'B' MEMORY
Y
X
T2052 6T 6T
R2046 330
D2045
D2046
C2046 10
C2047 10
D2044
D2047
R2047 330
B SIGNAL IN FROM DELAY LINE
P2004
R2041 50
R2049 270K
+300V
R2072 270K
V2073 7586
L2070
R2076 25K
C2076 0.1
R2077 240K
-100V
+19V
R2078 100
C2078 10μf
Q2074 PADT35
C2079 .001
'B' SIG. TO AC AMP.
R2074 1.5K
R2075 1K
R2075 27K
-100V
GROUNDED ON CHASSIS
W
V
Z
P11
NOTE:
ALL GROUNDS SHARE COMMON BUS TO TERM. A OR Z ON INTERCONNECTING PLUG, P11.

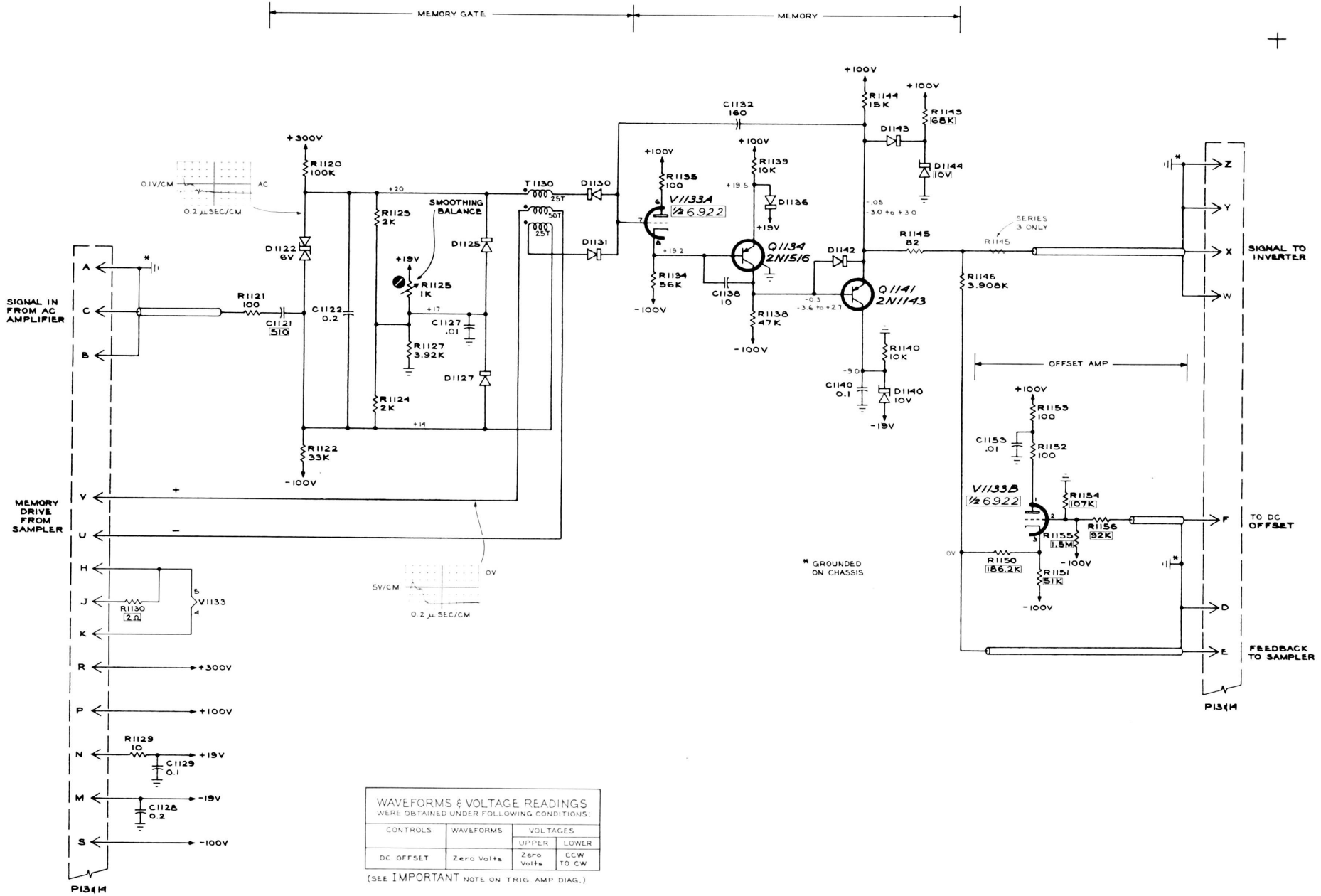


NOTE:
ALL GNDS SHARE COMMON BUS TO CHASSIS GND AT TERMS. A & Z.

VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:

CONTROLS	UPR. READINGS	LWR. READINGS
SMOOTHING	NORMAL	CCW

(SEE IMPORTANT NOTE ON TRIG. AMP. DIAG.)



WAVEFORMS & VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:			
CONTROLS	WAVEFORMS	VOLTAGES	
		UPPER	LOWER
DC OFFSET	Zero Volts	Zero Volts	CCW TO CW

(SEE IMPORTANT NOTE ON TRIG. AMP. DIAG.)

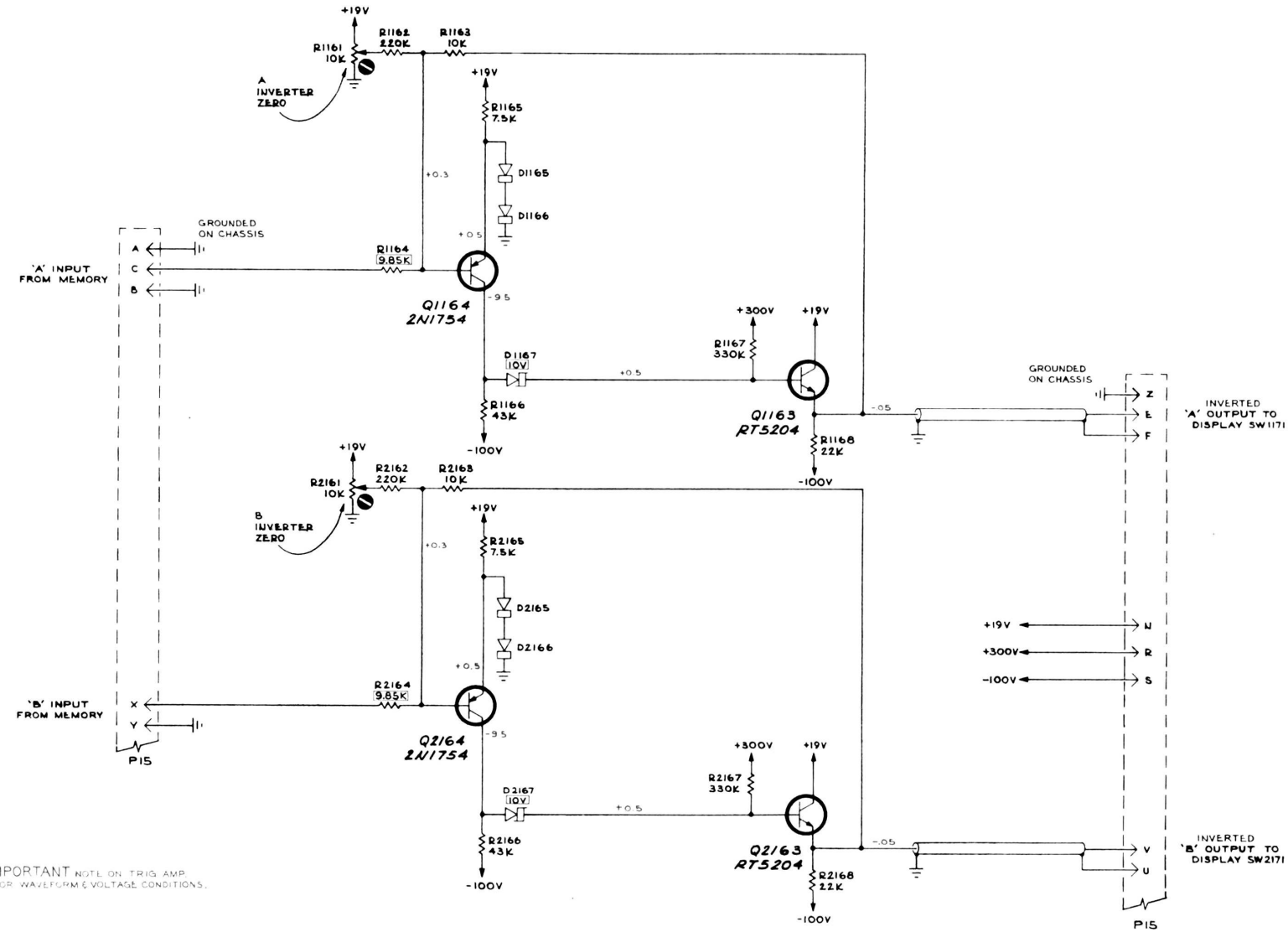
TYPE 451

A

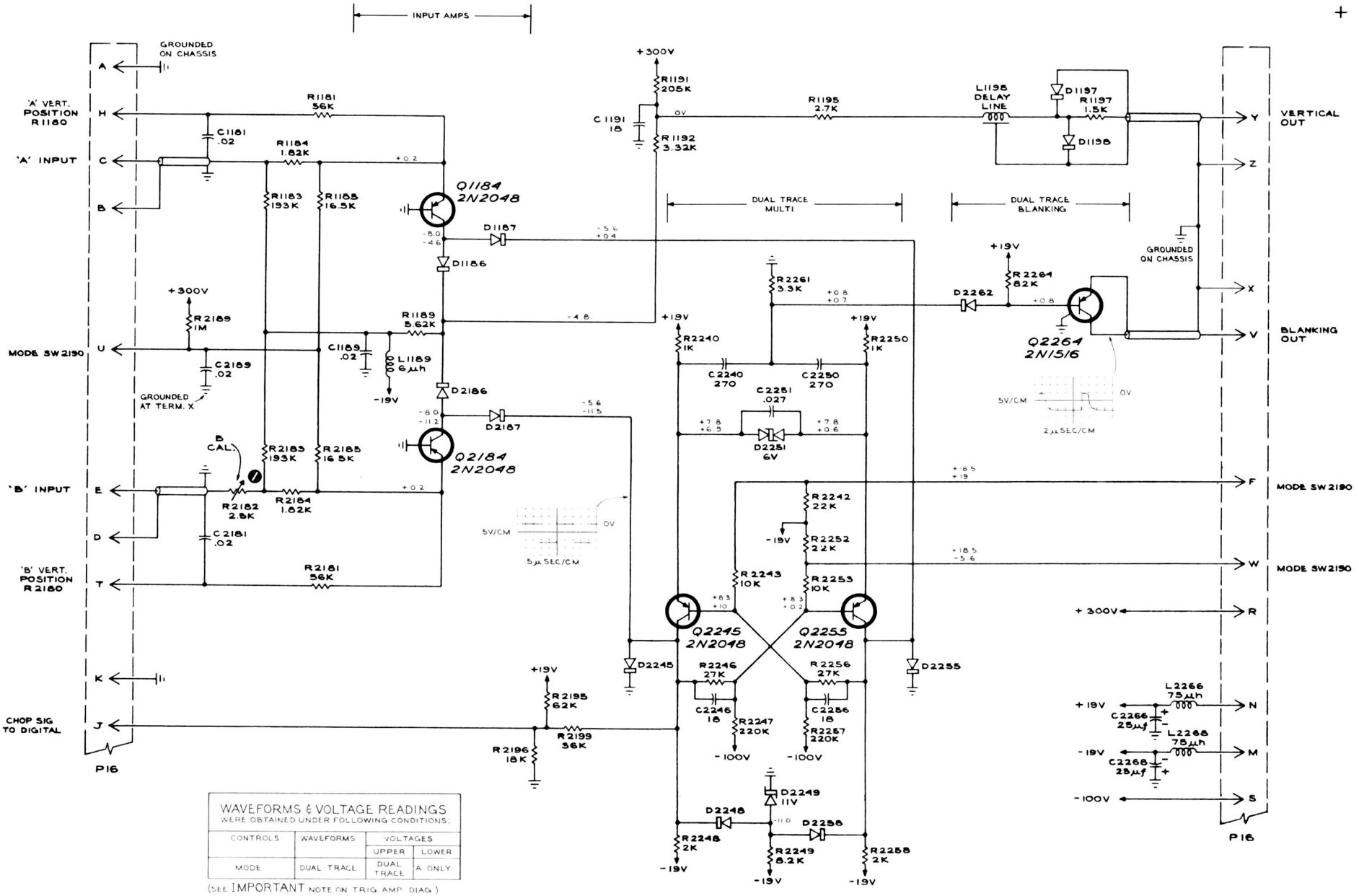
CMD 963

MEMORY

SERIES 3 MODELS 1,2
SERIES 8 MODELS 1,2
SERIES 11 MODELS 1,2

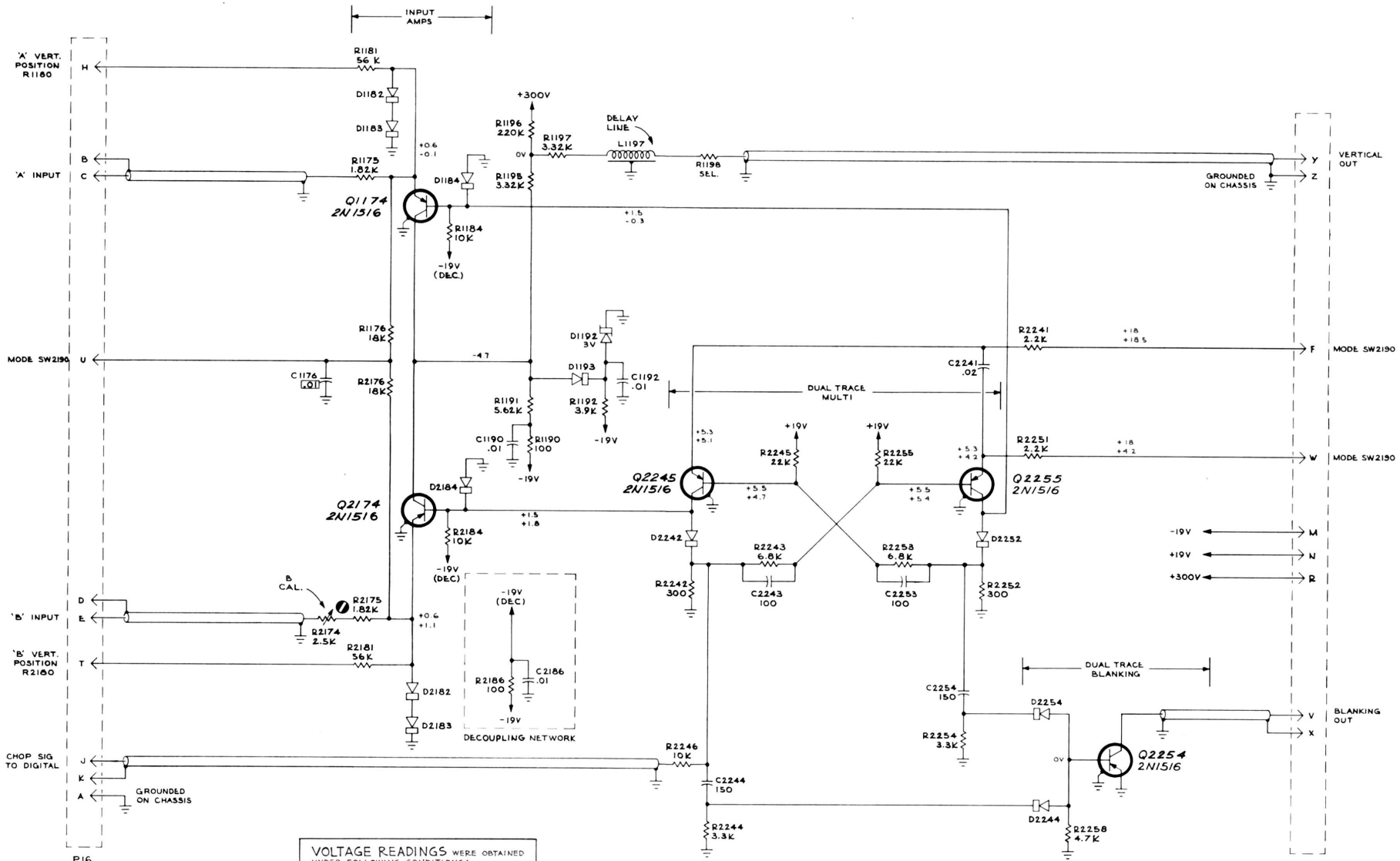


SEE IMPORTANT NOTE ON TRIG AMP. DIAG. FOR WAVEFORM & VOLTAGE CONDITIONS.



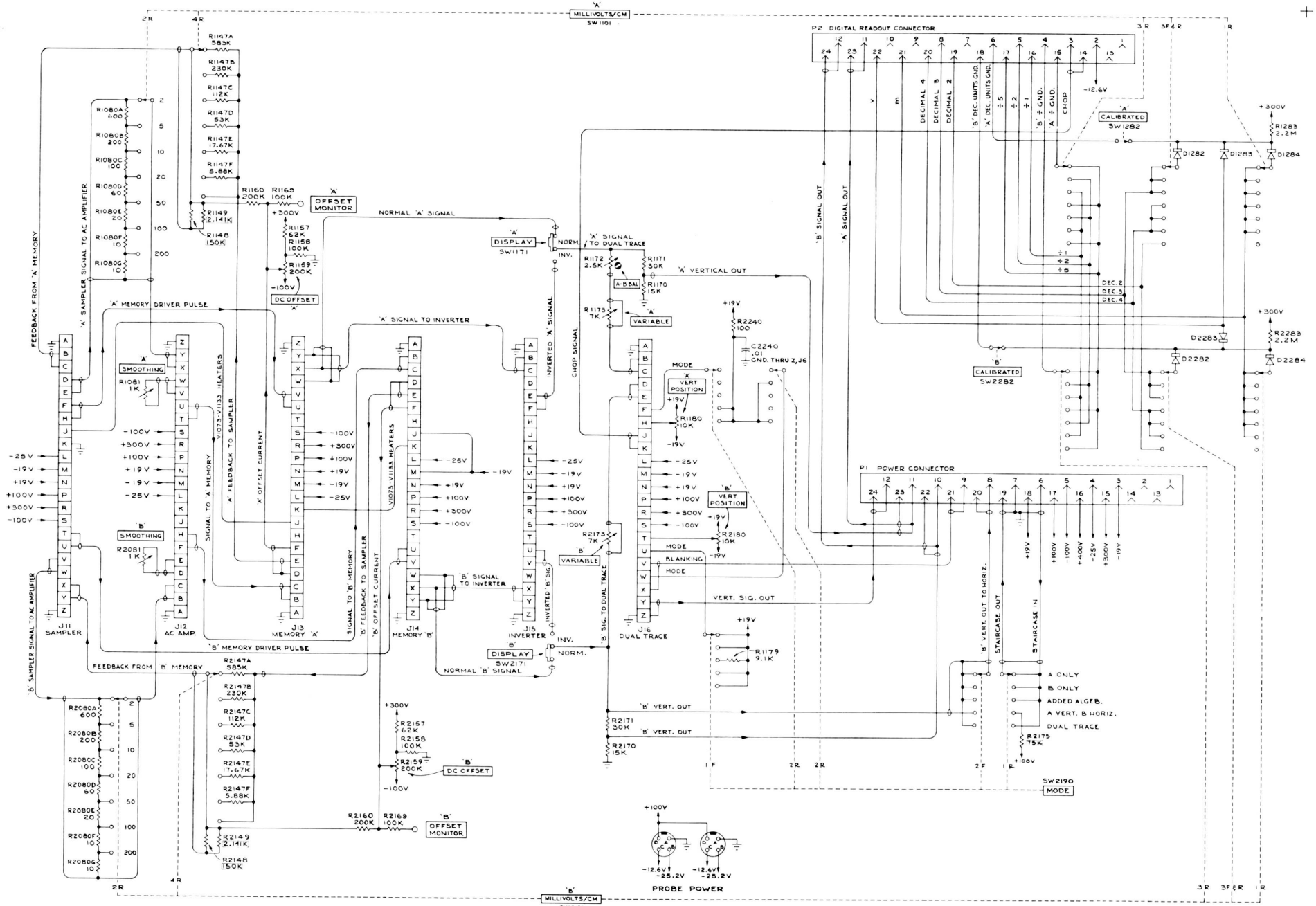
WAVEFORMS & VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:			
CONTROLS	WAVEFORMS	VOLTAGES	
		UPPER	LOWER
MODE	DUAL TRACE	DUAL TRACE	A ONLY

(SEE IMPORTANT NOTE ON TRIG. AMP. DIAG.)



VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:		
CONTROLS	UPR. READINGS	LWR. READINGS
MODE	DUAL TRACE	A ONLY

(SEE IMPORTANT NOTE ON TRIG AMP DIAG.)


'A' MILLIVOLTS/CM SW1101
'B' MILLIVOLTS/CM SW2101
P2 DIGITAL READOUT CONNECTOR
P1 POWER CONNECTOR
'A' CALIBRATED SW1282
'B' CALIBRATED SW2282
'A' OFFSET MONITOR
'B' OFFSET MONITOR
'A' DISPLAY SW1171
'B' DISPLAY SW2171
'A' SIGNAL TO DUAL TRACE
'B' SIG. TO DUAL TRACE
'A' VERTICAL OUT
'B' VERT. OUT
VERT. SIG. OUT
'A' SIGNAL OUT
'B' SIGNAL OUT
CHOP SIGNAL
NORMAL 'A' SIGNAL
NORMAL 'B' SIGNAL
INVERTED 'A' SIGNAL
INVERTED 'B' SIG.
'A' SIGNAL TO INVERTER
'B' SIGNAL TO INVERTER
'A' MEMORY DRIVER PULSE
'B' MEMORY DRIVER PULSE
FEEDBACK FROM 'A' MEMORY
FEEDBACK FROM 'B' MEMORY
'A' SAMPLER SIGNAL TO AC AMPLIFIER
'B' SAMPLER SIGNAL TO AC AMPLIFIER
SIGNAL TO 'A' MEMORY
SIGNAL TO 'B' MEMORY
'A' FEEDBACK TO SAMPLER
'B' FEEDBACK TO SAMPLER
'A' OFFSET CURRENT
'B' OFFSET CURRENT
V1073, V1133 HEATERS
'A' SMOOTHING R1081 1K
'B' SMOOTHING R2081 1K
'A' DC OFFSET
'B' DC OFFSET
'A' VARIABLE
'B' VARIABLE
'A' VERT POSITION
'B' VERT POSITION
MODE
BLANKING
STAIRCASE OUT
STAIRCASE IN
'B' VERT. OUT TO HORIZ.
A ONLY
B ONLY
ADDED ALGEB.
A VERT. B HORIZ.
DUAL TRACE
SW2190 MODE
PROBE POWER
J11 SAMPLER
J12 AC AMP.
J13 MEMORY 'A'
J14 MEMORY 'B'
J15 INVERTER
J16 DUAL TRACE
GND. THRU Z, J6
DECIMAL 4
DECIMAL 5
DECIMAL 2
'B' DEC. UNITS GND.
'A' DEC. UNITS GND.
÷5
÷2
÷1
'B' ÷ GND.
'A' ÷ GND.
CHOP
DEC 2
DEC 5
DEC 4
-12.6V
+300V
+100V
+19V
-19V
-25V
-100V