INSTRUCTION MANUAL

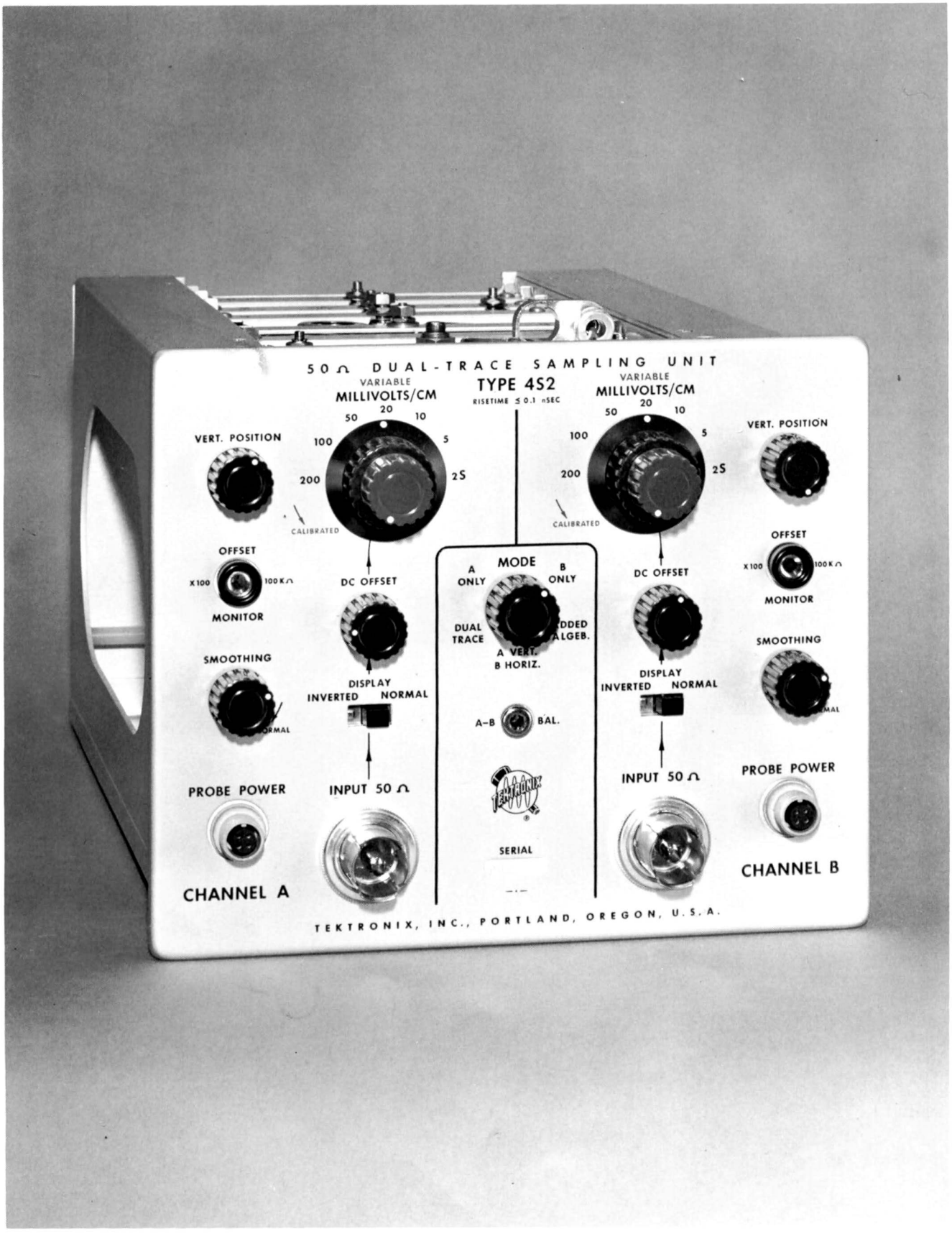
Serial Number _____

Type 4S2 Plug-In Unit

Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon ● Phone MI 4-0161 ● Cables: Tektronix

070-356

664


50 Ω DUAL-TRACE SAMPLING UNIT
TYPE 4S2
RISETIME ≤ 0.1 nSEC
VARIABLE
MILLIVOLTS/CM
50
20
10
100
5
200
2S
CALIBRATED
VERT. POSITION
OFFSET
X100
100 KΩ
MONITOR
SMOOTHING
DC OFFSET
DISPLAY
INVERTED
NORMAL
INPUT 50 Ω
PROBE POWER
CHANNEL A
MODE
A ONLY
B ONLY
DUAL TRACE
ADDED ALGEB.
A VERT.
B HORIZ.
A–B
BAL.
SERIAL
CHANNEL B
TEKTRONIX, INC., PORTLAND, OREGON, U.S.A.

SECTION 1

CHARACTERISTICS

General Information

The Tektronix Type 4S2 50 Ω Dual-Trace Sampling Unit is a vertical channel plug-in unit for the Type 661 Oscilloscope. The Type 4S2 has a risetime of 0.1 nanosecond or less. It is capable of presenting accurate single- or dual-trace displays of repetitive high-speed signals with fractional nanosecond risetime. By taking successive samples of a repetitive signal, each sample at a slightly later time with respect to the previous sample, the system reconstructs the signal on a relatively long time base.

Characteristics

Input Impedance

50 ohms ±1% at dc. Fig. 1-1 shows input VSWR up to 4 gc. Passive and cathode follower probes are available for higher input impedance at reduced sensitivity.

Risetime

0.1 nsec or less, 10% to 90%. Typical risetime and transient response is shown in Fig. 1-2. (Frequency response shown in Fig. 1-1.) Aberrations during the first 4 to 5 nsec after the fast transition are due to the Type 4S2 input circuit, not the pulser. The transient aberrations are related to the frequency response curve of Fig. 1-1.

NOTE

The large reflections in Fig. 1-2e are re-reflections. The first reflection occurs at the Type 4S2 input termination resistor, goes back to the pulser, and is then returned to the Type 4S2. The pulser is a tunnel diode type with "clean" tapered line from diode < 5 ohm source impedance to the 50 ohm output line. Pulse slope (after fast transition) is < 5 mv for 30 nsec. Pulse amplitude is 560 mv. Total time from tunnel diode to Type 4S2 termination is essentially 1.6 nsec (without an attenuator) causing the re-reflection to appear 3.2 nsec after fast transition.

Deflection Factors

Calibrated steps of 2S, 5, 10, 20, 50, 100 and 200 mv/cm. Accuracies: DISPLAY switch at NORMAL, 10 through 200 mv/cm ±2.5%, 2S and 5 mv/cm, ±3%; at INVERTED, add 1% more error possible. The 2 mv/cm factor is automatically smoothed 40% to 50%. SMOOTHING control still operates in addition to the fixed smoothing. An uncalibrated VARIABLE control with a 3:1 range permits decreasing the deflection factor of each setting of the MILLIVOLTS/CM switch setting. The 2S mv/cm factor can be decreased to about 2/3 mv/cm.

Dynamic Range

Input signals as high as ±1 volt may be viewed without overloading the system. Safe overload, plus or minus 10 volts dc.

Noise

At deflection factor of 5 mv/cm, SMOOTHING control at NORMAL, MODE switch at A ONLY, B ONLY, or A VERT. B HORIZ: 80% of the dots are within 4 mv peak-to-peak (see Fig. 1-2c). With MODE switch at DUAL TRACE or ADDED ALGEB: 80% of the dots are within 5 mv peak-to-peak. With SMOOTHING control fully counterclockwise; 80% of the dots are typically with 1.5 mv peak-to-peak.

Triggering

External to Timing Unit only.

Operating Modes

A Only, B Only, Dual Trace, Added Algebraically, and A Vertical-B Horizontal (X-Y operation). The dual-trace switching frequency is approximately 50 kc.

Rejection ratio for Added Algebraic mode is 40:1 or better when each channel is driven with a 1-volt flat-top pulse and the deflection factor is 50 mv/cm, each channel. At 200 mv/cm, Added Algebraic Mode, a 4-cm identical signal in each channel will produce an 8-cm display, ±1.5 mm.

Display

Normal or Inverted, permitting the addition or subtraction of dual-trace displays. Valuable in X-Y displays for observation of hysterisis loops, or for inverting the phase of signals in or out of an amplifier for phase comparison. Inverted operation can add an additional 1% to 2% error to the deflection factors. With the Type 661 vertical signal outputs at zero, 200 mv/cm, the trace will not shift more than 0.5 cm when switching the DISPLAY switch.

Smoothing

Each channel SMOOTHING control permits reduction of time jitter and random noise. Valuable when operating at lowest deflection factors. At 200 mv/cm, the trace will not move more than 1.5 cm while rotating the SMOOTHING control.

Dc Offset

The dc component of a signal may be offset up to ±1 volt (with a five-turn control) to either bring a display back onto the crt, or to make an incremental measurement.

Signal Outputs to Type 661

(The Type 661 signal output terminals are connected directly to the plug-in unit circuits through the interconnecting socket.) The signal output voltages are within 3% of a

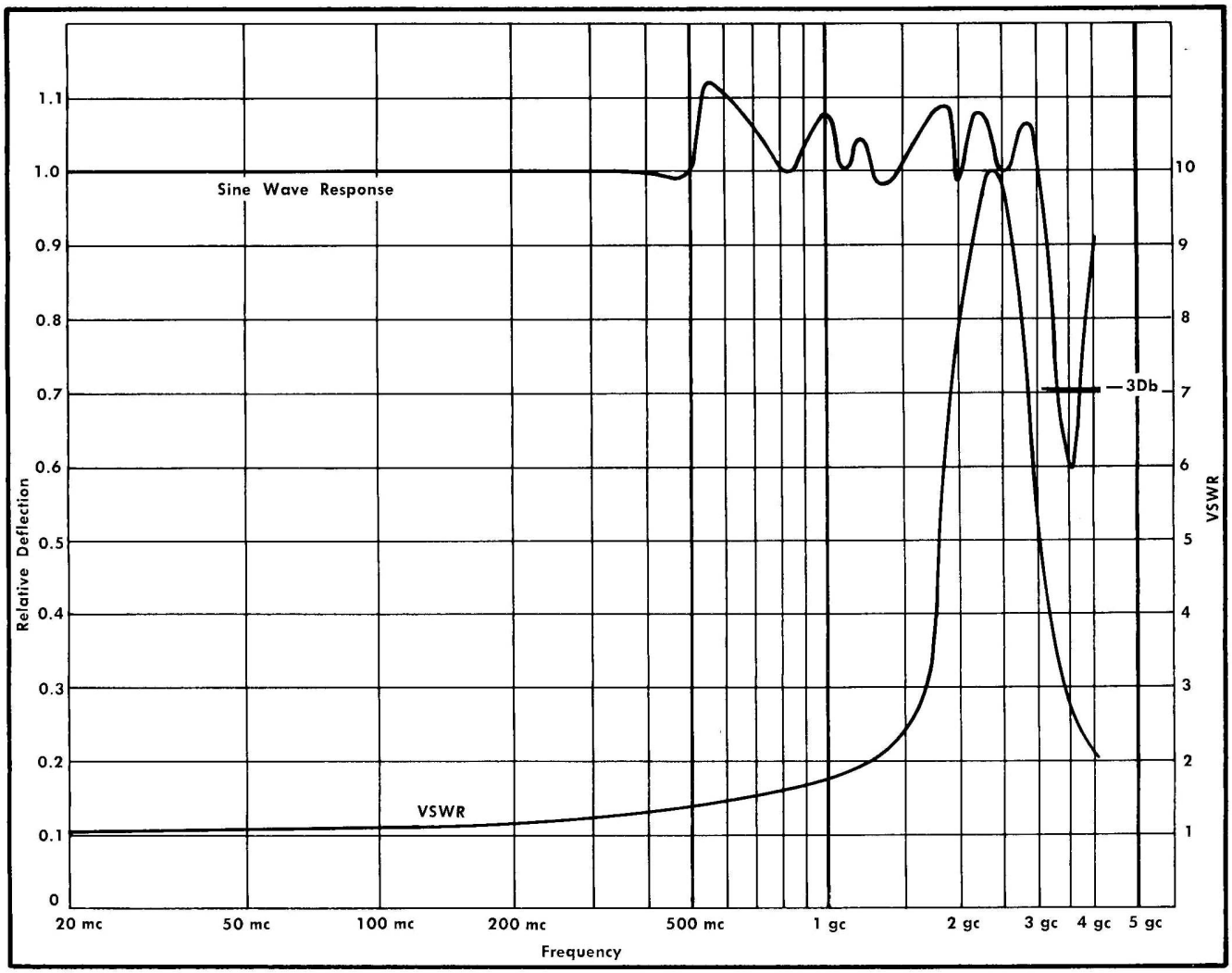


Fig. 1-1. Typical Type 4S2 VSWR and relative amplitude response to sine waves, S/N 301 up.

1-volt signal applied to the input connectors when the deflection factor is 200 mv/cm. (Does not include crt display.) Output impedance is 10 k, ±2%.

Dot Slash

The sampling dot vertical stability is such that no drift is visible when triggering at a rate above about 150 cps. At a triggering rate of 50 cps, the dot drift will not exceed 0.2 cm.

Co-Channel Time Coincidence

Dual-trace display of a fast rise pulse will produce no more than a 20-picosecond time difference between channels.

Probe Power

Two front panel connectors permit operation of Tektronix cathode-follower probes.

Mechanical

Aluminum-alloy chassis with six plug-in circuit boards. Photo-etched anodized panel.

Dimensions

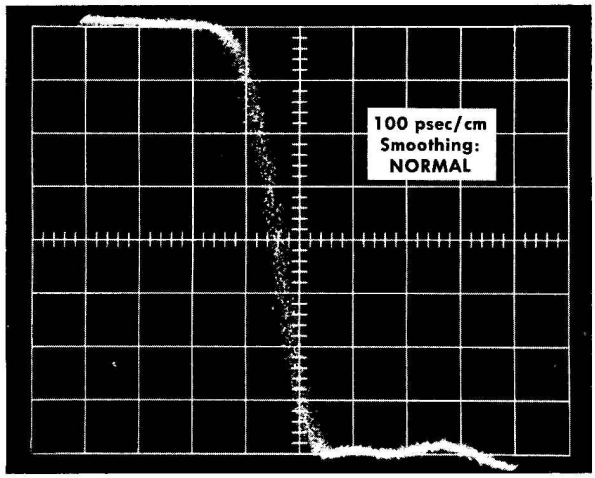
Height 7 inches, width 8½ inches, depth 14 inches.

Weight

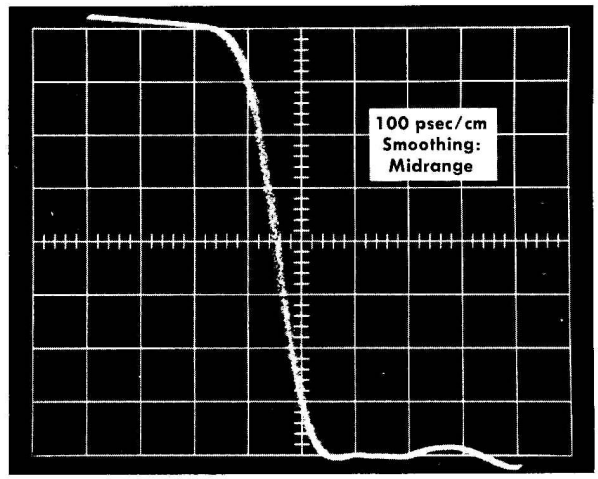
9 pounds, 9 ounces.

Accessories Included

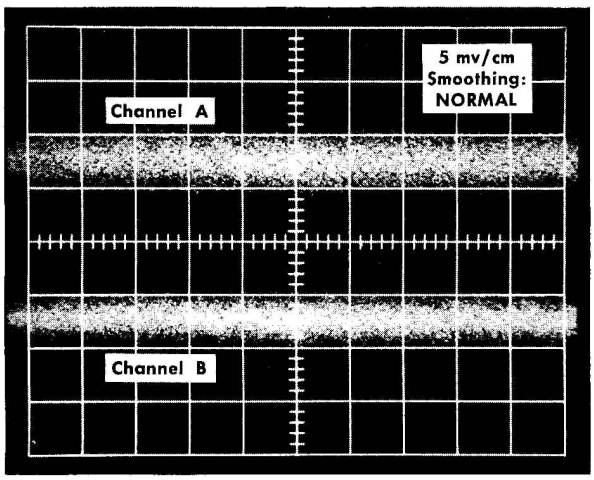
	Tektronix Part Number
2—10× 50 Ω Attenuators with GR Type 874 Connectors.	017-0044-00
2—5 nsec delay RG-8A/U 50 Ω cables.	017-0502-00
2—Instruction Manuals.	070-0356-00



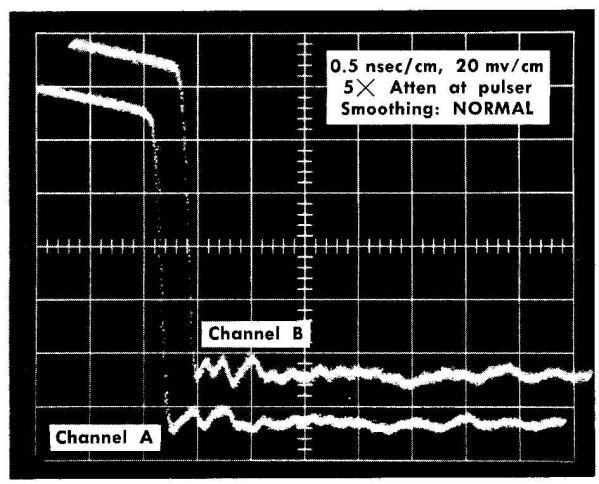
a.



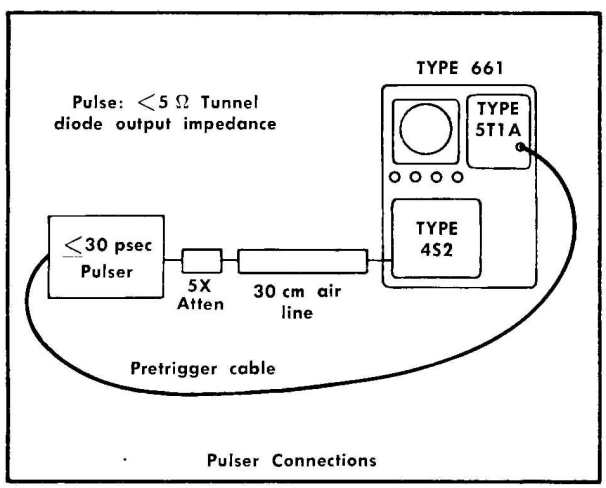
b.

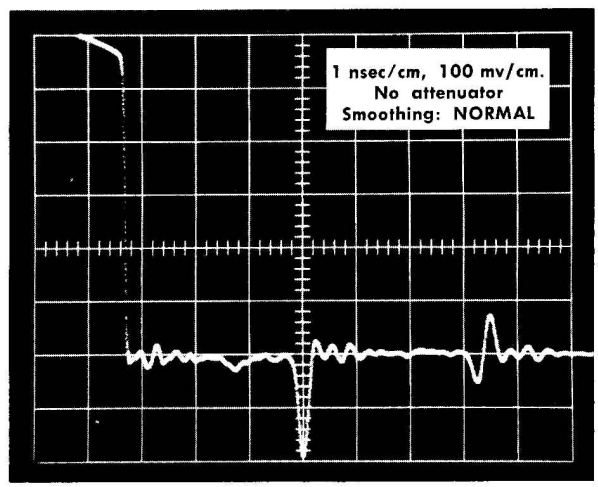


c.



d.





e.

Fig. 1-2. Typical Type 4S2 risetime, noise and aberration characteristics. Pulser connections are shown.

SECTION 4

CIRCUIT DESCRIPTION

General Information

Most circuits in the Type 4S2 are on plug-in subchassis. The main frame contains only the sampler circuit, controls, interconnections, and cables. You may wish to refer to the Tektronix publication "Sampling Notes", publication number 061-557, during the following discussion.

Block Diagram

The Type 4S2 simplified block diagram of Fig. 4-1 shows each circuit in block form, with all front panel and internal controls identified. Since the two channels are identical, only the Channel A circuits are identified.

External trigger information to the Timing Unit starts the sampling cycle. The Timing Unit sends command pulses to the Type 4S2 Gate Generator. The Gate Generator sends very short duration push-pull pulses to both Sampler circuits, and slightly longer duration push-pull pulses to both Memory circuits. The two sets of pulses from the Gate Generator connect first the sampling gates to the sampler amplifiers, and then connect the AC Amplifier to the Memory circuits.

Input signals travel through about three inches of 50-ohm air line into the Sampler that includes the sampling gate and sampler amplifier. The sampling gate is biased to conduction by the Gate Generator as command pulses arrive from the timing unit via J7. The sampling gate output signal is a series of pulses, amplified by the sampler amplifier, and coupled through the MILLIVOLTS/CM switch into the Ac Amplifier. The Ac Amplifier (gain of about 200) amplifies the signal and presents it to the Memory. The Gate Generator biases a gate at the Memory input to conduction as the signal arrives.

The Memory amplifies and stores the signal. The Memory output is used by the Type 661 indicator to produce the crt display and to set the input circuit to the voltage of the signal at the time the sample was taken. (When the SMOOTHING control is at NORMAL, the next sample only corrects for any signal changes since the last sample.) The Memory output signal to the Type 661 can be inverted by a unity gain Inverter. The output of both channels then pass through the Dual Trace electronic switch where either or both are sent on to the Type 661.

Input and Sampler

The Type 4S2 input connectors are 50 ohm General Radio Type 874 connectors. They assure maximum uniformity of input impedance and a quick mate universal system. The input characteristic impedance is within 1% of 50 ohms.

The input system is shown in simplified form in Fig. 4-2. The input and sampler are the heart of the sampling system where the 0.1-nsec risetime performance is established. The input termination is a disc type 50-ohm resistor R1001. Located between the termination and the sampling gate is a low resistance ½ watt composition resistor, R1002 (S/N 101-300). Fig. 4-2 shows Cc between R1002 and ground, indicating stray capacitance that helps compensate the input frequency response R1002 is a ¼ watt resistor beginning with S/N 301, and Cc becomes C1002, an adjustable capacitor.

Fig. 4-2 shows the sampling gate is normally reverse biased a total of 4 to 5 volts. The relay contacts represent an equivalent method of applying forward bias to the sampling gate. If the relay is closed momentarily, the gate will be forward biased permitting the signal to be applied to the sampler amplifier. The actual forward biasing signal duration is slightly less than 0.1 nsec; so fast in fact, that the series inductance of L1021 and shunt capacitance of Cs, combined with the 25-ohm source impedance and the series 20 to 40 ohms of the gate, limit the signal to the sampler amplifier grid to about 10% of the input amplitude. Cs is stray input capacitance that stretches the 0.1-nsec signal at the sampler amplifier input. Because only about 10% of the signal gets to the amplifier, the sampling efficiency is about 10%.

The sampler amplifier has a very high input impedance and a gain of about 7. Refer to the Sampler diagram at the back of this manual (Channel A) during the following discussion. The input tube, V1024, amplifies the signal and couples it through a voltage divider to the base of Q1034. Q1034 amplifies the signal and sends it to both the Ac Amplifier subchassis and back to the cathode of V1024. This action bootstraps the input grid assuring a high-input-impedance stable amplifier. The Ac Amplifier, Memory, and feedback loop are discussed following the Gate Generator description.

Gate Generator

The pulses that gate the sampling diodes into conduction are formed by a special snap-off diode, D1065, driven by Avalanche transistor Q1064. The Avalanche transistor is normally biased to cutoff by −3 volts from Zener diode D1054. The collector voltage of Q1064 rests between +75 and +150 volts, as set by the AVALANCHE VOLTS control (R1057). As the positive trigger pulse arrives from the timing unit, Q1064 begins to conduct, soon reaching the avalanche state and conducting very heavily. C1064, at the collector of Q1064, initially prevents the collector voltage from falling. Since the avalanche condition is heavy conduction regardless of bias, the emitter of Q1064 rises abruptly. The heavy avalanche current lasts only as long as it takes to discharge C1064. The avalanche current charges the L1065-C1065 network so that it rings with a peak-to-peak amplitude of several volts.

As C1064 discharges, the collector of Q1064 falls, sending a negative-going signal through C1060 to the memory gate amplifier. Thus, Q1064 avalanche acts first upon its emitter circuit and D1065, then upon its collector circuit and the Memory Gate ampifier, Q2054.

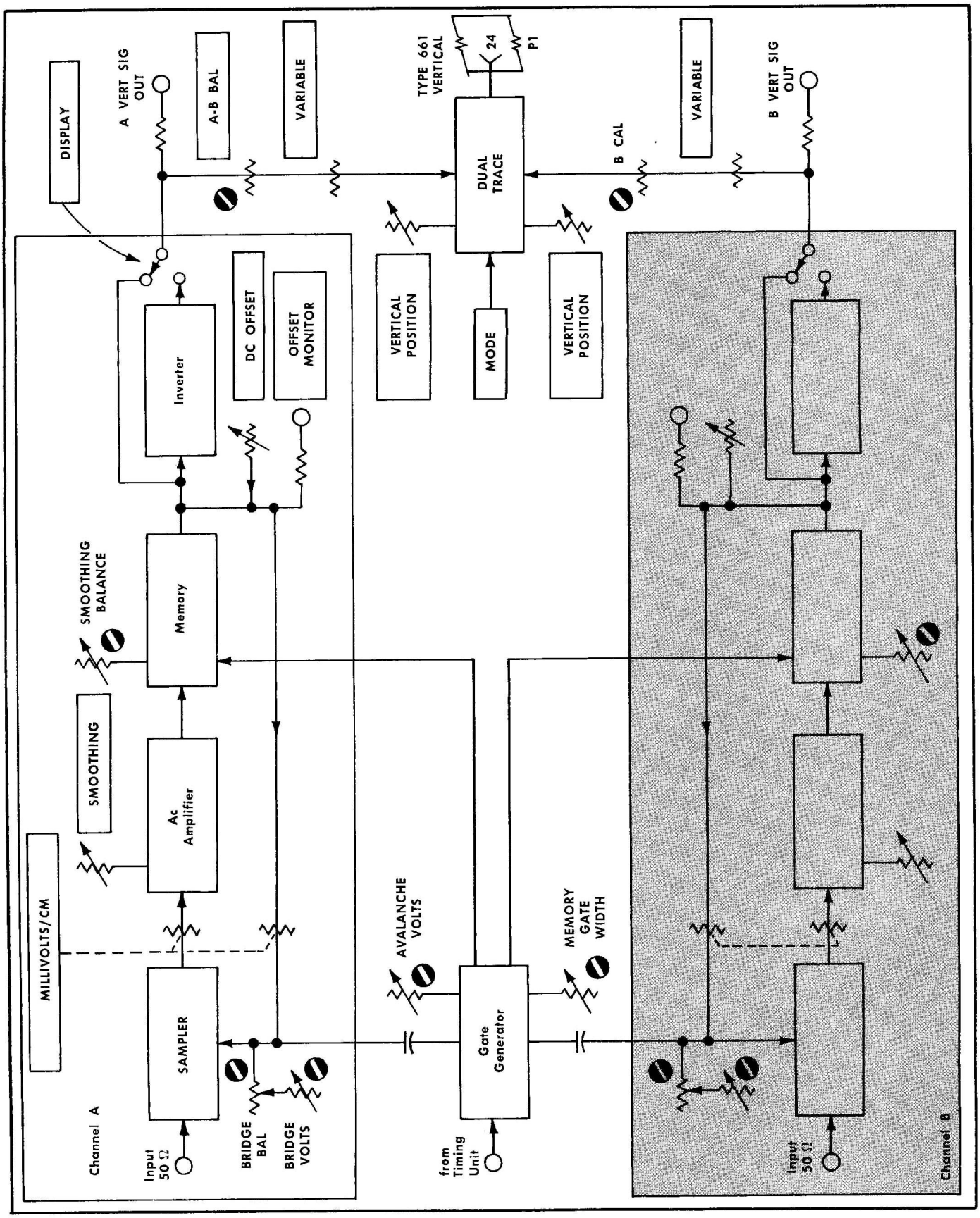


Fig. 4-1. Type 4S2 block diagram. Shaded area of Channel B is identical to corresponding area in Channel A.

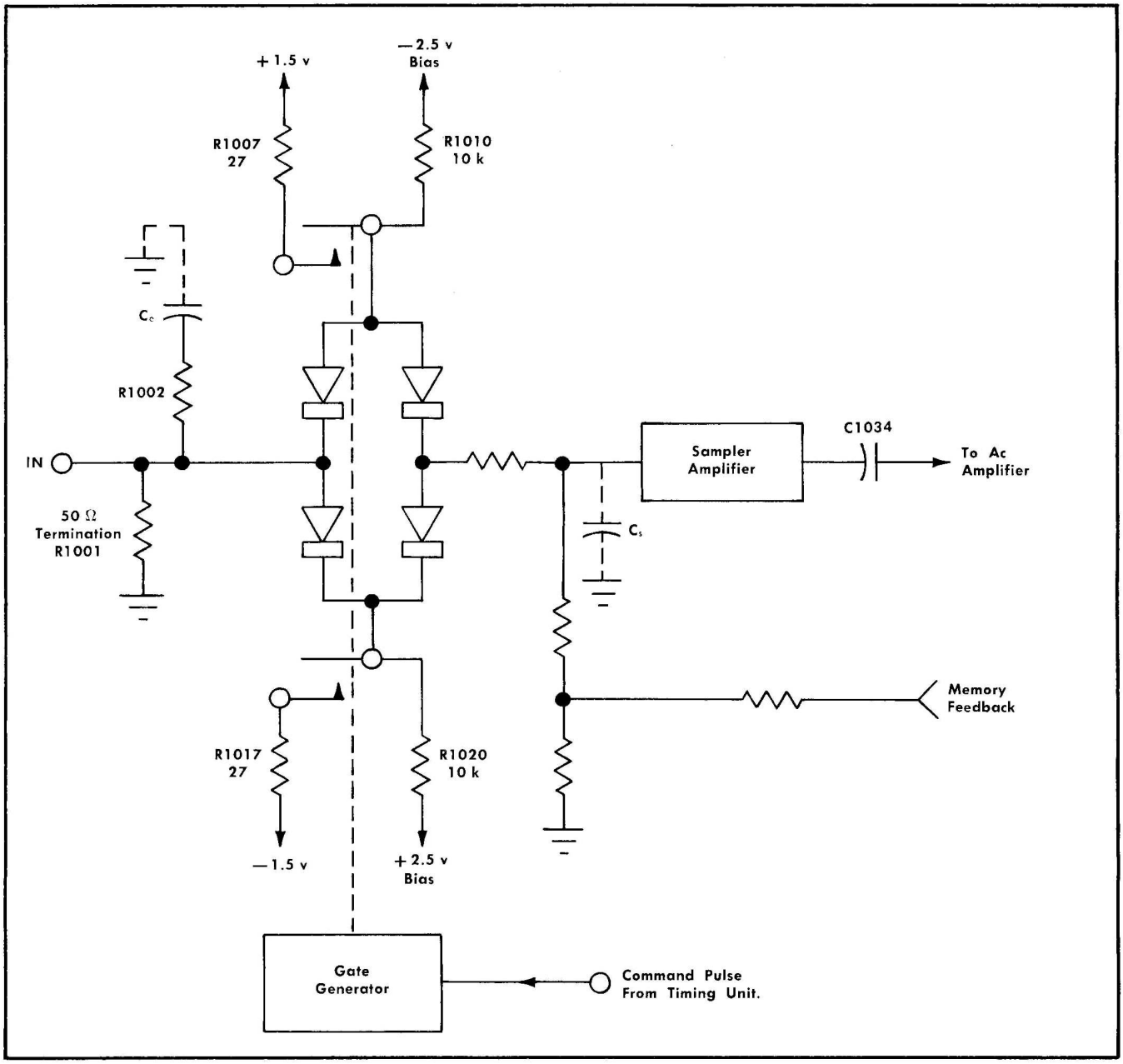


Fig. 4-2. Simplified sampling system input.

Snap Off Action

The emitter signal of Q1064 starts in a positive direction and lasts nearly a complete cycle. As L1065 and C1065 cause the emitter voltage to swing negative, D1065 is reverse biased. D1065 does not become a high impedance at first, sending a high current into the 2-cm strip line. D1065 suddenly becomes a high impedance as the reverse current drops. The current in the strip line then forms a sharp positive pulse at its input, and into the two output cable pairs. The positive voltage step traverses the strip line and returns as a negative step cancelling the pulse. The time taken for the positive pulse to go down the strip line, invert and return to cancel the pulse is slightly longer than 0.1 nsec.

Memory Gate Width

Memory gate amplifier Q2054 is normally biased to cutoff by reverse bias through the MEMORY GATE WIDTH control R2045. Q2054 collector rests at −19 volts. The collector current path is through the two windings of the two Memory gates, not through D2057 and R2058. As the Avalanche transistor collector sends its negative signal to Q2054, D2052 conducts and forward biases Q2054 to saturation. Collector current flows through R2056 and R2057 and the two coils of the Memory gates. D2057 and R2058 reduce ringing when Q2054 again cuts off. The length of time Q2054 remains saturated is controlled over about a 2 to 1 range by the MEMORY GATE WIDTH control.

Sampler Controls

The Gate Generator subchassis contains all sampler internal adjustments that control sampling efficiency and loop gain; they are: AVALANCHE VOLTS, MEMORY GATE WIDTH, A and B BRIDGE VOLTS, and A and B BRIDGE BAL.

The A and B BRIDGE VOLTS adjustments set the amount of sampling gate reverse bias (at least 4 volts). If the sampling gate reverse bias is less, there is a chance that an input signal greater than ±2 volts might break through to the sampler amplifier and distort the display.

The A and B BRIDGE BAL adjustments balance the sampling gate reverse bias to assure equal positive and negative signal linearity. Its effect upon the display is described in the calibration procedure.

AC Amplifier

The AC Amplifier receives its input signal (pulses) from the sampler amplifier through the front panel MILLIVOLTS/CM switch, amplifies it 200 times, inverts it, and feeds the memory circuit. The input dc level (to ground) is zero, and the input resistance ranges from 25 ohms at 200 mv/cm to 1000 ohms at 5 and 2 mv/cm. The Ac Amplifier is made up of two dc-coupled feedback amplifiers with a third dc feedback path around the whole circuit. The "outside" feedback path includes the front panel SMOOTHING control that allows a gain reduction of about 4 to 1 to reduce random noise. (When using SMOOTHING, the dot transient response must be considered and sufficient number of samples per centimeter obtained to make the display response correct.) The outside feedback path is for dc stabilization and does not act upon the main signal.

The signal pulses handled by the AC Amplifier are about 1 μsec in duration. The amplifier output voltage can change 1.6 volts in about 0.1 μsec. Normally the system causes the output pulses to be less than 1 volt, but if the display moves 8 centimeters in one sample, the output pulse will be about 1.6 volts peak. The output impedance of the circuit is low, so it can drive the memory input.

The gain of the first amplifier (Q1084 and Q1094) is about 40 times when the SMOOTHING control (R1081) is set to NORMAL (zero resistance). The gain is set by the ratio of R1089 to R1083. When using full smoothing, the gain is about 8 to 10, set by the ratio of R1089 to R1083 and R1081 (SMOOTHING) in series. The gain of the second amplifier (Q1104 and Q1113) remains fixed at about 5, set by the ratio of R1107 and R1096.

The frequency response of the first amplifier is fixed-compensated by C1089. The second amplifier frequency response is adjusted during calibration by C1107.

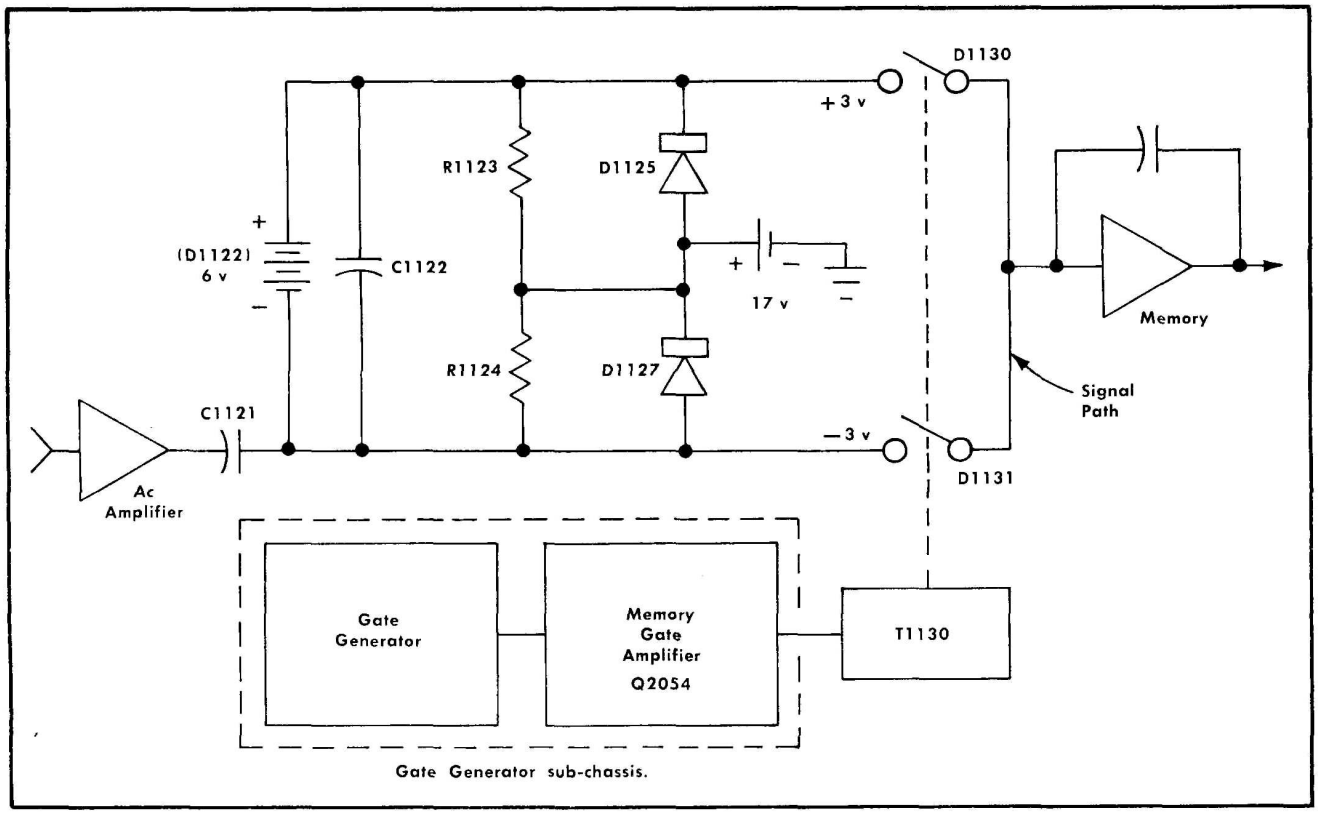


Fig. 4-3. Simplified memory gate.

Memory

A simplified schematic of the Memory circuit is shown in Fig. 4-3. The Gate Generator closes the Memory input gate (D1130 and D1131) at the correct time of each sampling cycle. The Memory circuit is a feedback amplifier with input and feedback elements both capacitors. The input capacitor is C1121, the feedback capacitor is C1132. V1133A is an input cathode follower, Q1134 is the amplifier, and Q1141 is an output emitter follower.

The input impedance at the grid of V1133A acts as a virtual ground because as the input signal changes the grid voltage, the signal is amplified and applied back to the input as negative feedback to cancel the original change.

The action of the memory is to transfer a charge from C1121 to C1132. The circuit between the AC Amplifier output and the grid of V1133A looks like 150 ohms and 510 pf in series (when the memory gate is conducting). Thus, as a signal appears at the AC Amplifier output, C1121 is charged. C1121 tries to couple the signal to the grid of V1133A, but feedback prevents the grid voltage from changing significantly; the result is for both C1121 and C1132 to receive a charge.

When the memory gate is not conducting, the grid of V1133A has a very high impedance to ground, and at this time the only possible discharge path for C1132 is by V1133A grid current or leakage current. The grid current is very low, and can be either positive or negative. Total leakage current is so low that there is essentially no change in the output voltage between samples even when sampling at the low rate of 150 dots/sec.

The circuit elements between C1121 and the grid of V1133A serve several purposes:

1. D1125 and D1127 are amplitude-limiting diodes. They normally do not conduct.

2. D1122 is a 6-volt Zener to provide back-bias for the gating diodes D1130 and D1131.

3. The resistors all aid in standardizing the input quiescent voltage level.

4. T1130 is a pulse transformer that allows instantaneous turn-on of the gating diodes to connect the input circuit to V1133A.

5. C1122 assures that both sides of D1122 follow the signal equally.

Within the memory amplifier:

1. C1138 corrects for transistor phase shift.

2. D1136 permits Q1134 to turn on hard, long enough for the stored charge (of D1136) to be removed, preventing damage to Q1134 in the event of turn-on overload.

3. D1142 assures that fast positive pulses at the base of Q1141 will be coupled to C1132 and the output, even if Q1141 has been momentarily cut off.

4. D1144 limits the positive swing of the output lead to about 10 volts and D1134 assures a high impedance when D1144 is reverse biased.

5. D1140 sets the maximum collector voltage of Q1141 at —9 volts.

6. R1145 prevents reverse reflections in the output cable from disturbing the display.

Between samples, the AC Amplifier output returns to its quiescent level, and C1121 charge (that was gained at the last sample) is cancelled. At the next sample, if there is any change at the sampler unit, C1121 will receive a new charging signal and can add to or subtract from the residual charge of C1132.

System Operation With No Signal

Items to remember when examining signals at various points between the sampler amplifier output and the memory output:

1. It is impossible to install perfectly balanced sampling gate diodes, so at each interrogation there will be some small error signal sent into the system.

2. The memory circuit does not retain a perfectly stable output voltage because C1132 cannot hold a charge permanently.

3. The memory output is coupled back to the sampler input (with proper attenuation).

4. Theoretically, if there is no input at the sampling gate, there will be no AC Amplifier signal, and the memory output will be zero. The memory output will be essentially zero, but there will always be a small pulse at the AC Amplifier output.

5. The SMOOTHING BALANCE control (R1125) sets the quiescent dc level at the memory input and if incorrectly adjusted will cause an offset voltage that looks like a continuous signal. For example, assume the SMOOTHING BALANCE control is off by +1 mv. If the memory amplifier internal gain is 500 (it isn't actually), the memory output will now be off by —500 mv. The —500-mv feedback to the input bridge creates an error signal which will drive the memory output nearly back to zero. After several dots the memory output will stabilize near zero, but slightly off from zero to provide enough error signal to correct for the original +1 mv error. Thus, a continuous minor error signal is amplified to place the output level near zero. If the AC Amplifier gain is reduced by the SMOOTHING control, the memory output must now be larger so the error signal fed into the AC Amplifier is larger, restoring again the —1 mv correction at the memory input. (A trace shift seen when the SMOOTHING control is rotated away from NORMAL is the increased memory output to make up for the reduced amplifier gain). Thus the memory input balance control is called the SMOOTHING BALANCE because its effect is seen by rotation of the SMOOTHING control.

DC Offset

The memory output of Q1141 is fed to the inverter or to the dual trace circuit. It is also fed to a voltage divider that controls the feedback signal sent to the sampler. The feedback attenuator resistors, R1147, (Plug-In Connectors

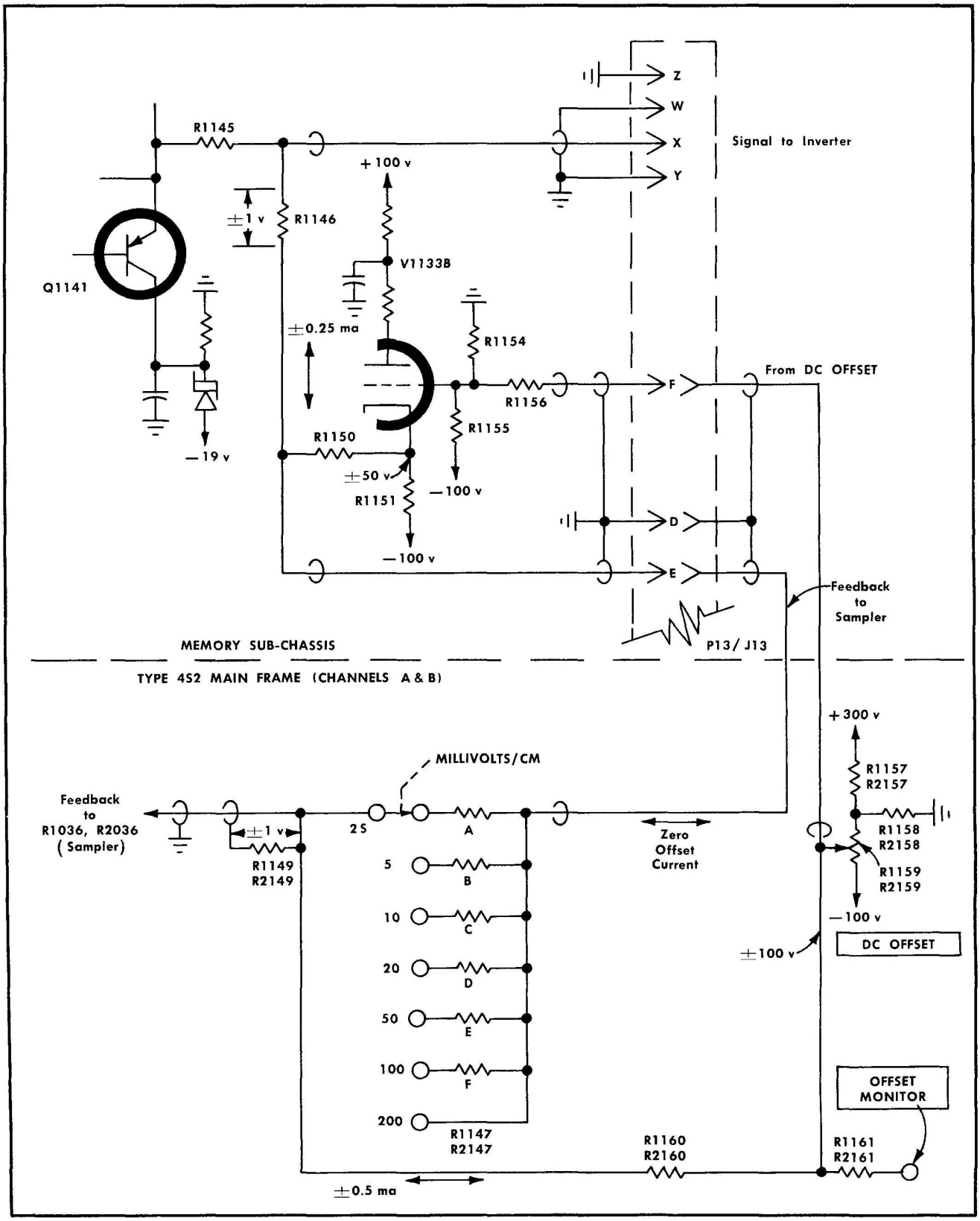


Fig. 4-4. DC Offset and Memory Feedback circuit.

and Switching diagram, Channel A) set the feedback amplitude to keep the basic memory output of 600 mv/cm while the feedback voltage just matches the input signal.

The DC Offset circuit adds a dc shift to the feedback loop. It includes a current cancelling system that prevents offset current from flowing in R1147; see Fig. 4-4. The grid voltage of V1133B is set by the DC OFFSET control through a resistance divider. Rotating the DC OFFSET control from one end to the other causes a ±50 volt swing at the cathode of V1133B. The cathode of V1133B drives ±0.25 ma through R1146 via R1150. The DC OFFSET control ±100-volt swing drives ±0.5 ma through R1149 via R1160. The resulting voltage drop of ±1 volt across both R1146 and R1149 is the offset voltage sent to the sampler amplifier. The two points of offset injection assure there is no offset current in R1147 so that the offset system is not affected by the MILLIVOLTS/CM switch.

The DC OFFSET control may be used to null certain levels of the input signal in order to measure amplitude. The OFFSET MONITOR jack allows a voltmeter connection to read the effective dc offset voltage X100. The offset voltage is also useful when measuring small signals riding on larger signals.

Inverter

The Inverter is an X1 amplifier pair (10k input, 10k feedback) for each channel. Its function is to invert the display when the front panel DISPLAY switch is in the INVERTED position. When the DISPLAY switch is in the NORMAL position, the inverter is bypassed by interconnecting wiring in the Type 4S2 main frame.

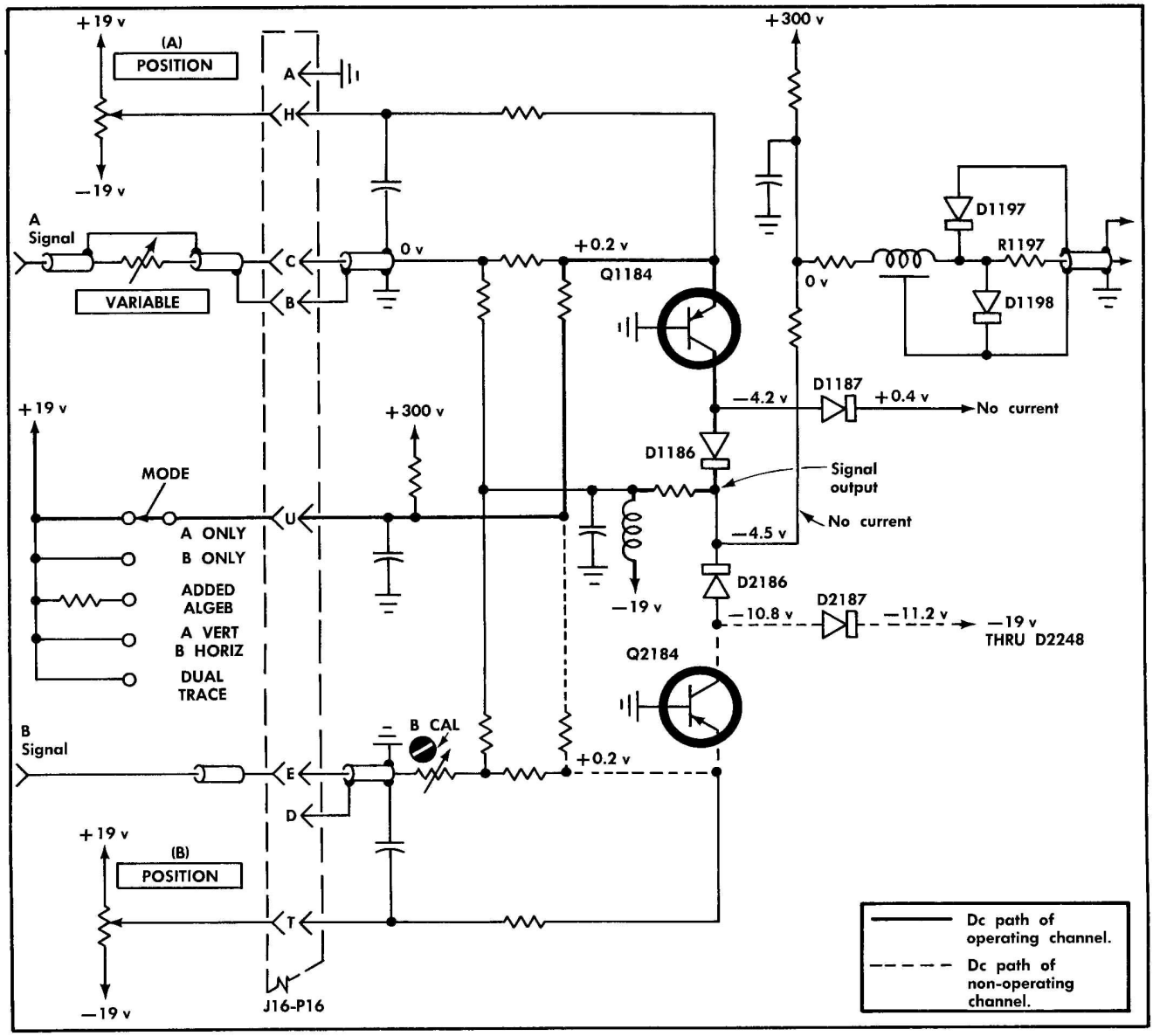


Fig. 4-5. Dual Trace circuit dc conditions. MODE A ONLY, DC OFFSET zero, trace centered, no signal, timing unit FREE RUN.

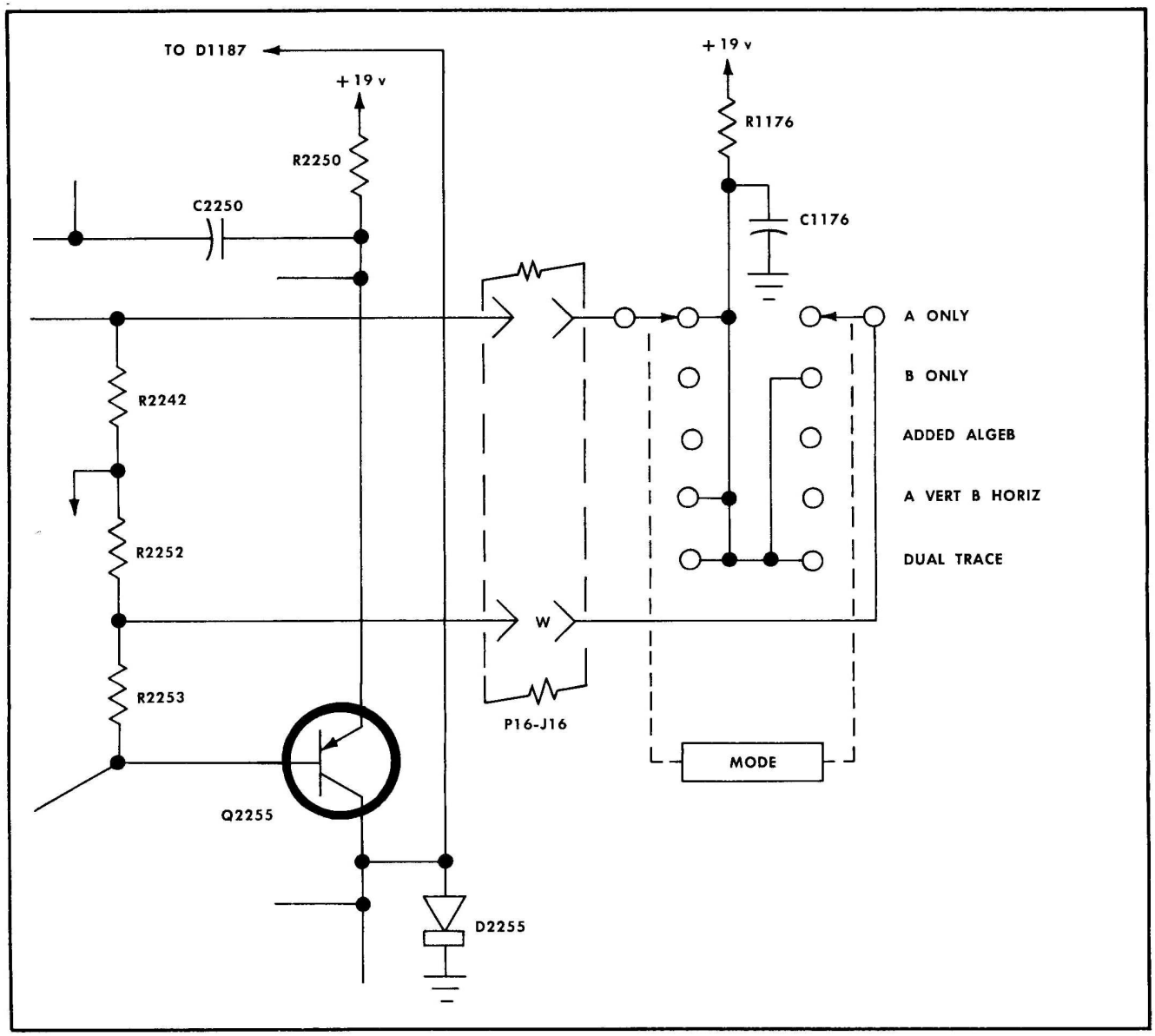


Fig. 4-6. MODE switch connections to the DUAL TRACE multivibrator.

Q1164 is collector coupled to Q1163. D1167 is a voltage offset Zener to raise the voltage at the base of Q1163 above that at the collector of Q1164 without signal attenuation. Q1163 is an output emitter follower. R1161, the A INVERTER ZERO control, and R1162 are a dc balance network to adjust the output dc level, eliminating trace shift when moving the DISPLAY switch from NORMAL to INVERTED. R1163 is the feedback resistor.

Dual Trace Model 3

The Dual Trace subchassis determines which channel is displayed by the Type 661; under some conditions, the signals from both channels are fed to the Type 661. Because of the various modes of operation possible in dual-trace, both the A and B channel will be discussed.

Two gated inverter amplifiers, Q1184 and Q2184, control passage of the signal. A multivibrator, Q2245 and Q2255, control the two amplifiers via switching diodes D116 and D216. Multivibrator operation is controlled by the front panel MODE switch. In the A ONLY, B ONLY, and A VERT B HORIZ modes, only one side of the multivibrator conducts. In the ADDED ALGEB mode, neither side conducts, and in the DUAL TRACE mode, the multivibrator free-runs at a switching rate of about 50 kc. Q2264 provides a dual-trace blanking signal to the Type 661 when the multivibrator switches.

A 0.25-μsec delay line couples the output signal from the dual trace unit to the Type 661 indicator. The delay allows the signal to phase properly with the Timing Unit unblanking of the Type 661 crt.

Refer to Fig. 4-5, the Dual Trace, and the Plug-In Connectors and Switching diagrams during the following discussion. Each inverter is fed signals from the DISPLAY switch for its channel. The Channel A signal arrives through R1184, the Channel B signal arrives through R2182 and R2184. The inverter amplifier emitter circuits include positioning controls (R1180 and R2180) in parallel with the emitter return resistors (R1185 and R2185). Positioning is by current injection into the emitter circuits through R1181 and R2181. The major emitter current comes from the +19-volt supply, through MODE switch SW2190 and to the emitters through R1185 and R2185. In the ADDED ALGEB. position of the MODE switch, current limiting resistor R1179 is inserted in the emitter circuit to keep the common output lead average voltage the same as when only one transistor is conducting.

The amplifiers are connected in a common-base configuration. The current at their collectors is switched between two paths by the multivibrator to connect or disconnect them from the common collector load, R1189. There is essentially no change in the current of either transistor whether it is connected to the output or not. The input impedance is that of the series input resistors, R1184 in channel A, and R2182 and R2184 in channel B. Since the emitters of both transistors rest at about +0.2 volts, R1183 and R2183 are used to offset the input voltage to zero. The —4.5-volt collector voltage is offset to zero (for the output lead) by the series combination of R1191 and R1192.

Fig. 4-6 shows the MODE switch connections that set the operating conditons of the multivibrator. During single channel operation, with only one side of the multivibrator conducting, the conducting transistor saturates and Zener diode D2251 conducts. In A ONLY operation, multivibrator transistor Q2255 operates in saturation, and its collector is held at about +0.4 volt by D2255. This reverse biases both D2258 and D1187, so that Q1184 supplies the output signal. Since transistor Q2245 is cutoff, R2248 forward biases both D2248 and D2187, bypassing Q2184 from the output.

Operation in the A VERT B HORIZ mode sets the multivibrator and the inverter amplifiers the same as in the A ONLY mode. The Channel B signal bypasses the Dual Trace circuit and is fed separately to the Type 661 horizontal deflection system. In the B ONLY mode, operation of the multivibrator and inverter transistors is the reverse, with Q1184 disconnected and Q2184 supplying the output signal.

In the ADDED ALGEB mode, neither multivibrator transistor conducts. Both inverters are turned on, combining both signals in the common collector circuit at R1189. The output to the delay line is the algebraic sum of the A and B signals.

In the DUAL TRACE mode, Q2245 and Q2255 operate as a free-running multivibrator at about 50 kc. The inverter amplifiers pass signals alternately, providing a dual-trace display.

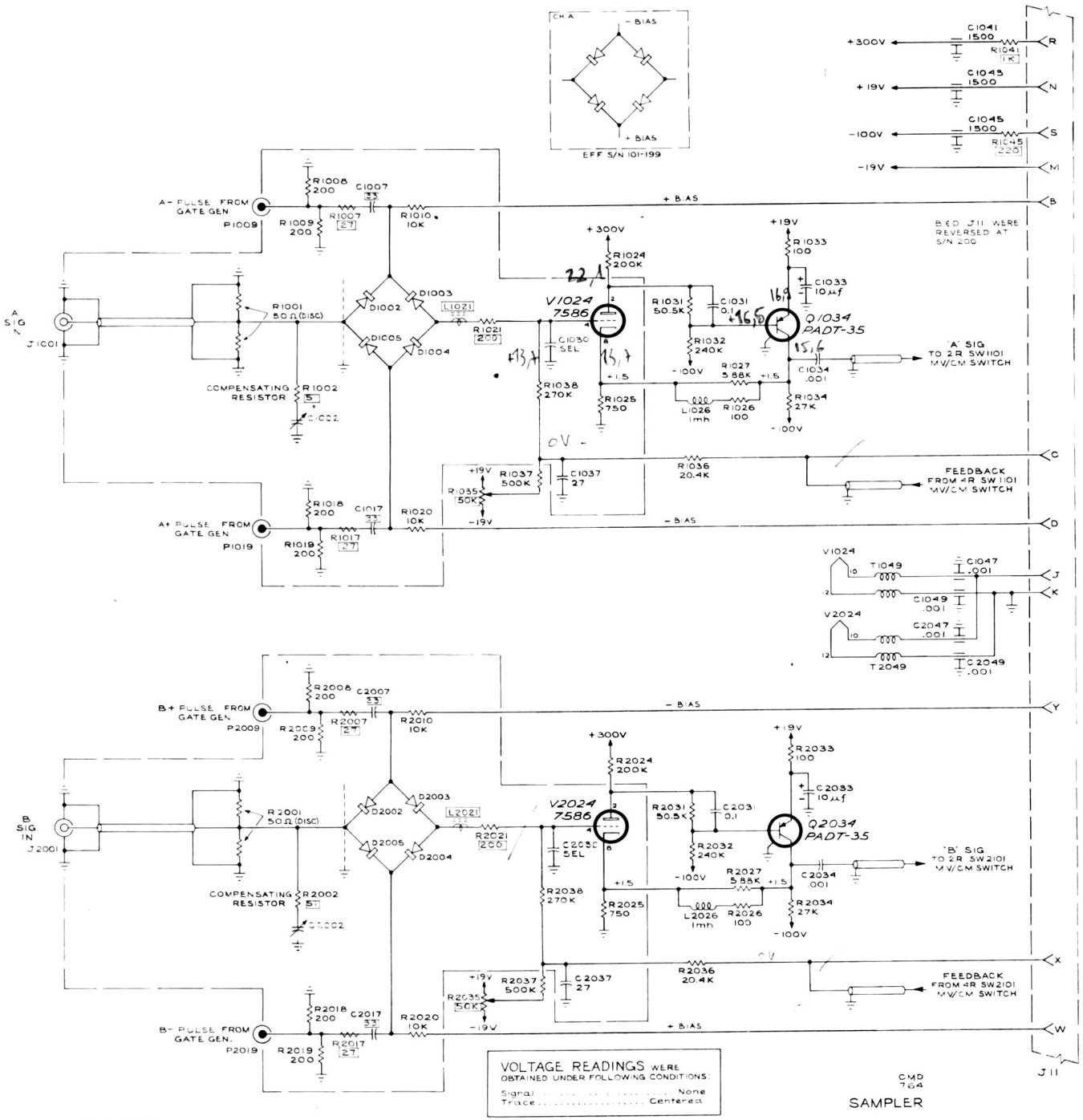
During multivibrator operation, neither transistor saturates, and Zener diode D2251 does not conduct. The multivibrator switching time constant, located between the emitters of Q2245 and Q2255, is composed of C2251 in series with the emitter return resistor (R2240 or R2250) of the nonconducting side. The collector-to-base coupling circuits (R2246-C2246 and R2256-C2256) do not set the time of operation; the capacitors are for high-frequency coupling to assure fast switching.

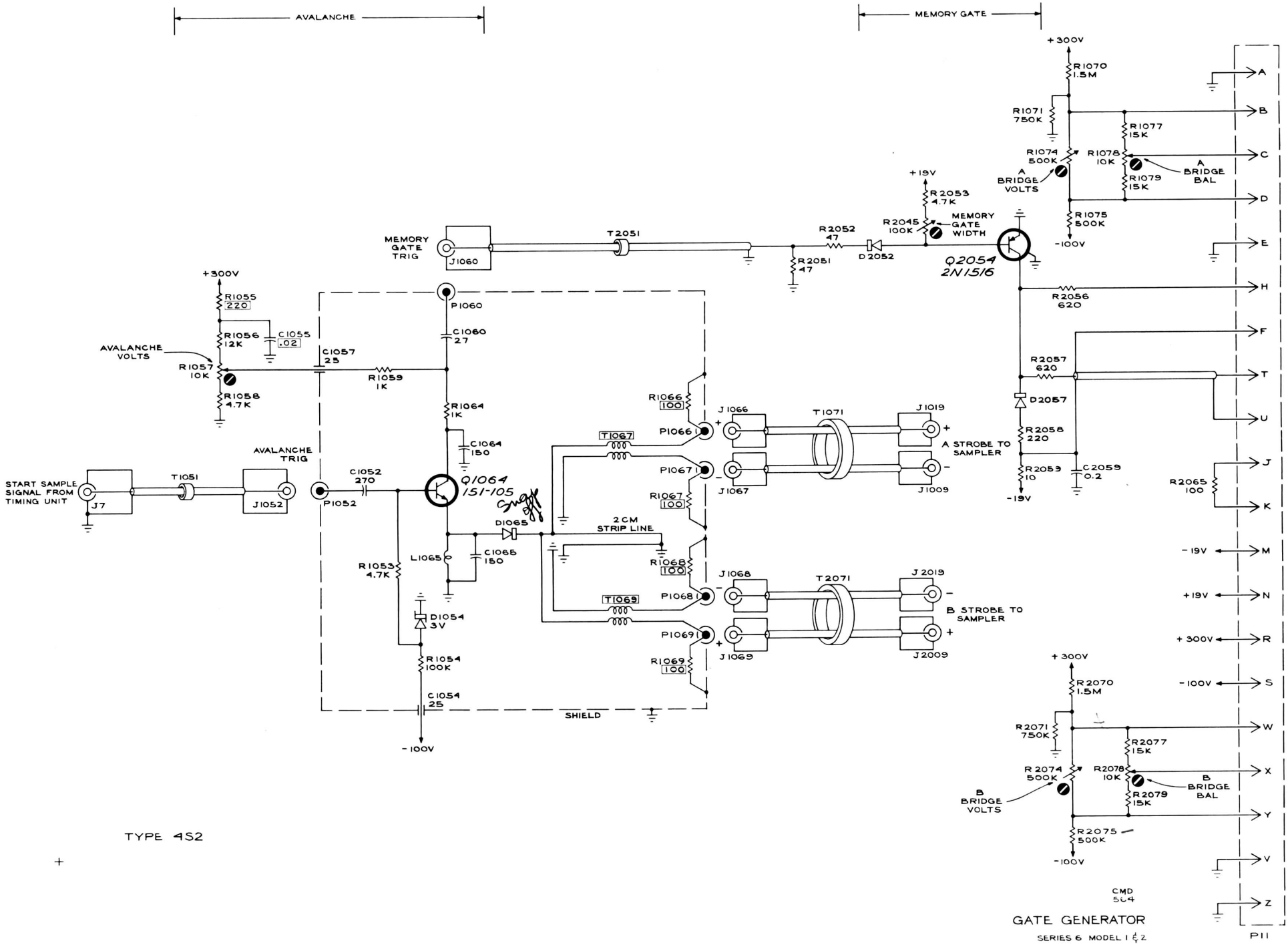
NOTE

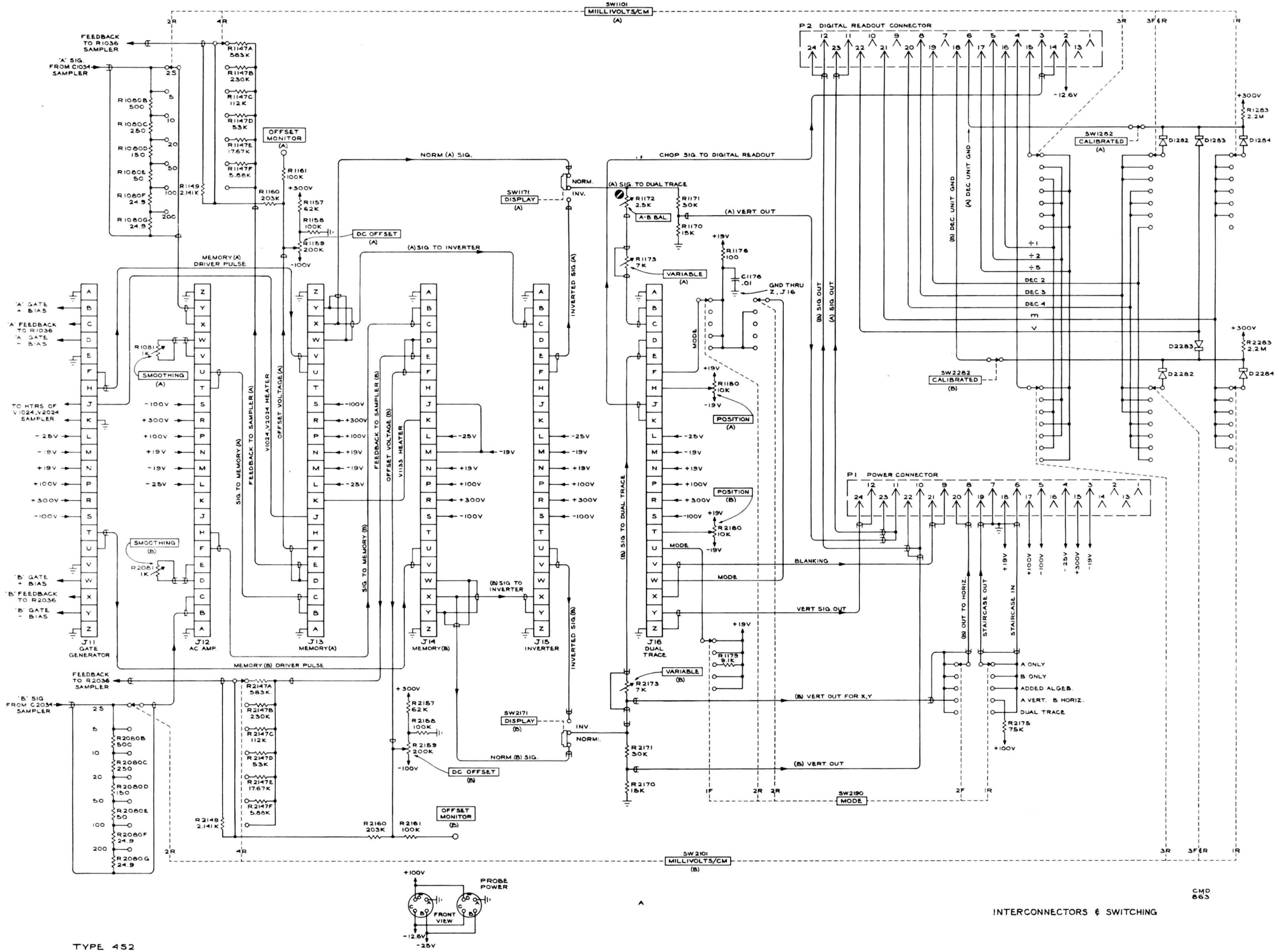
Models 1 and 2 Dual-Trace Subchassis will operate in the Type 4S2, but are not recommended due to noise limits.

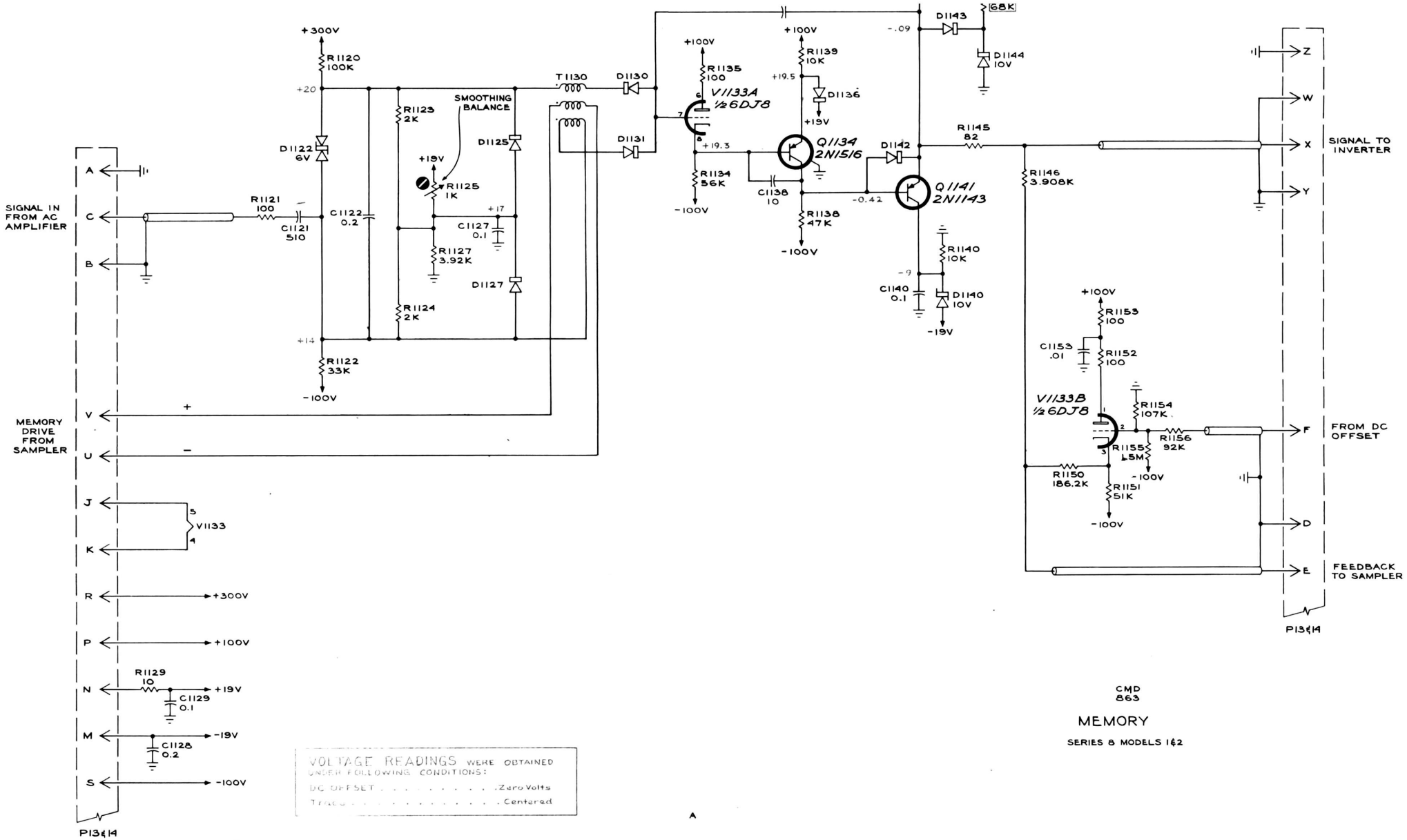
Blanking Circuit

Blanking transistor Q2264 normally rests in cutoff with its base at about +0.8 volt. As the multivibrator switches, C2240 or C2250 couples about a —2 volt signal to the base of Q2264 to turn it on. The turn-on pulse lasts only about 0.5 μsec, but it is heavy enough to saturate Q2264 and give it a storage time of about 1 to 1.5 μsec. There is some positive overshoot immediately before the —2 volt pulse. This is kept from the base of Q2264 by D2262 so that the storage time of Q2264 will be fairly consistent, and the crt will be properly blanked during the time the dual-trace multivibrator is switching channels.


CH A
- BIAS
+ BIAS
EFF S/N 101-199
+300V
C1041 1500
R1041 1K
R
+19V
C1043 1500
N
-100V
C1045 1500
R1045 220
S
-19V
M
A- PULSE FROM GATE GEN
P1009
R1008 200
C1007 33
R1009 200
R1007 27
R1010 10K
+ BIAS
B
A SIG IN
J1001
R1001 50Ω (DISC)
COMPENSATING RESISTOR
R1002 5
D1003
D1002
D1005
D1004
L1021
R1021 200
V1024 7586
+300V
R1024 200K
C1030 SEL
R1038 270K
R1025 750
+1.5
R1031 50.5K
C1031 0.1
R1032 240K
-100V
R1027 5.88K
L1026 1mh
R1026 100
+19V
R1033 100
C1033 10μf
Q1034 PADT-35
C1034 .001
R1034 27K
-100V
'A' SIG TO 2R SW1101 MW/CM SWITCH
B ED J11 WERE REVERSED AT S/N 200
22,1
16,4
16,5
13,7
13,7
15,6
0V -
R1035 50K
+19V
R1037 500K
C1037 27
-19V
R1036 20.4K
C
FEEDBACK FROM 4R SW1101 MW/CM SWITCH
A+ PULSE FROM GATE GEN
P1019
R1018 200
C1017 33
R1019 200
R1017 27
R1020 10K
- BIAS
D
V1024
T1049
C1047 .001
J
K
C1049 .001
V2024
C2047 .001
T2049
C2049 .001
B+ PULSE FROM GATE GEN
P2009
R2008 200
C2007 33
R2009 200
R2007 27
R2010 10K
- BIAS
Y
B SIG IN
J2001
R2001 50Ω (DISC)
COMPENSATING RESISTOR
R2002 5
D2003
D2002
D2005
D2004
L2021
R2021 200
V2024 7586
+300V
R2024 200K
C2030 SEL
R2038 270K
R2025 750
+1.5
R2031 50.5K
C2031 0.1
R2032 240K
-100V
R2027 5.88K
L2026 1mh
R2026 100
+19V
R2033 100
C2033 10μf
Q2034 PADT-35
C2034 .001
R2034 27K
-100V
'B' SIG TO 2R SW2101 MW/CM SWITCH
0V
R2035 50K
+19V
R2037 500K
C2037 27
-19V
R2036 20.4K
X
FEEDBACK FROM 4R SW2101 MW/CM SWITCH
B- PULSE FROM GATE GEN.
P2019
R2018 200
C2017 33
R2019 200
R2017 27
R2020 10K
+ BIAS
W
J11
VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:
Signal ..... None
Trace ..... Centered
CMD 764
SAMPLER
TYPE 4S2


AVALANCHE
MEMORY GATE
+300V
R1070 1.5M
R1071 750K
R1077 15K
R1074 500K
R1078 10K
R1079 15K
A BRIDGE VOLTS
A BRIDGE BAL
R1075 500K
-100V
+19V
R2053 4.7K
R2045 100K
MEMORY GATE WIDTH
R2052 47
R2051 47
D2052
Q2054 2N1516
MEMORY GATE TRIG
J1060
T2051
R2056 620
R2057 620
D2057
R2058 220
R2059 10
C2059 0.2
-19V
R2065 100
+300V
R1055 220
R1056 12K
C1055 .02
AVALANCHE VOLTS
R1057 10K
R1058 4.7K
C1057 25
R1059 1K
P1060
C1060 27
R1064 1K
C1064 150
AVALANCHE TRIG
START SAMPLE SIGNAL FROM TIMING UNIT
J7
T1051
J1052
C1052 270
P1052
Q1064 151-105
D1065
2CM STRIP LINE
L1065
C1065 150
R1053 4.7K
D1054 3V
R1054 100K
C1054 25
SHIELD
-100V
R1066 100
P1066
J1066
T1067
T1071
J1019
J1009
A STROBE TO SAMPLER
R1067 100
P1067
J1067
R1068 100
P1068
J1068
T1069
T2071
J2019
B STROBE TO SAMPLER
R1069 100
P1069
J1069
J2009
+300V
R2070 1.5M
R2071 750K
R2077 15K
R2074 500K
R2078 10K
R2079 15K
B BRIDGE VOLTS
B BRIDGE BAL
R2075 500K
-100V
A
B
C
D
E
H
F
T
U
J
K
-19V
M
+19V
N
+300V
R
-100V
S
W
X
Y
V
Z
P11
CMD 564
GATE GENERATOR
SERIES 6 MODEL 1 & 2
TYPE 4S2


SW1101 MILLIVOLTS/CM (A)
P2 DIGITAL READOUT CONNECTOR
P1 POWER CONNECTOR
FEEDBACK TO R1036 SAMPLER
'A' SIG. FROM C1034 SAMPLER
R1147A 583K
R1147B 230K
R1147C 112K
R1147D 53K
R1147E 17.67K
R1147F 5.88K
R1080B 500
R1080C 250
R1080D 150
R1080E 50
R1080F 24.9
R1080G 24.9
R1149 2.141K
OFFSET MONITOR (A)
R1161 100K
R1160 203K
+300V
R1157 62K
R1158 100K
R1159 200K
-100V
DC OFFSET (A)
NORM (A) SIG.
CHOP SIG. TO DIGITAL READOUT
SW1171 DISPLAY (A)
NORM.
INV.
(A) SIG. TO DUAL TRACE
R1172 2.5K
A-B BAL
R1171 50K
R1170 15K
(A) VERT OUT
+19V
R1176 100
C1176 .01
GND THRU Z, J16
R1173 7K
VARIABLE (A)
MEMORY (A) DRIVER PULSE
(A) SIG. TO INVERTER
INVERTED SIG. (A)
(A) DEC. UNIT GND
(B) DEC. UNIT GND
(B) SIG OUT
(A) SIG OUT
÷1
÷2
÷5
DEC 2
DEC 3
DEC 4
m
V
SW1282 CALIBRATED (A)
D1282
D1283
D1284
R1283 2.2M
+300V
D2283
D2282
D2284
R2283 2.2M
SW2282 CALIBRATED (B)
MODE
R1180 10K
POSITION (A)
'A' GATE + BIAS
'A' FEEDBACK TO R1036
'A' GATE - BIAS
R1081B 1K
SMOOTHING (A)
TO HTRS OF V1024, V2024 SAMPLER
-25V
-19V
+19V
+100V
+300V
-100V
SIG. TO MEMORY (A)
FEEDBACK TO SAMPLER (A)
V1024, V2034 HEATER
OFFSET VOLTAGE (A)
FEEDBACK TO SAMPLER (B)
OFFSET VOLTAGE (B)
V1133 HEATER
SIG. TO MEMORY (B)
(B) SIG. TO DUAL TRACE
POSITION (B)
R2180 10K
MODE
BLANKING
VERT SIG. OUT
'B' GATE + BIAS
'B' FEEDBACK TO R2036
'B' GATE - BIAS
R2081 1K
SMOOTHING (B)
(B) SIG. TO INVERTER
INVERTED SIG. (B)
J11 GATE GENERATOR
J12 AC AMP
J13 MEMORY (A)
J14 MEMORY (B)
J15 INVERTER
J16 DUAL TRACE
MEMORY (B) DRIVER PULSE
FEEDBACK TO R2036 SAMPLER
'B' SIG. FROM C2034 SAMPLER
R2147A 583K
R2147B 230K
R2147C 112K
R2147D 53K
R2147E 17.67K
R2147F 5.88K
R2080B 500
R2080C 250
R2080D 150
R2080E 50
R2080F 24.9
R2080G 24.9
R2149 2.141K
R2160 203K
R2161 100K
OFFSET MONITOR (B)
+300V
R2157 62K
R2158 100K
R2159 200K
-100V
DC OFFSET (B)
NORM (B) SIG.
SW2171 DISPLAY (B)
INV.
NORM.
R2171 50K
R2170 15K
(B) VERT OUT
(B) VERT OUT FOR X,Y
VARIABLE (B)
R2173 7K
R1175 91K
(B) OUT TO HORIZ
STAIRCASE OUT
STAIRCASE IN
A ONLY
B ONLY
ADDED ALGEB.
A VERT. B HORIZ.
DUAL TRACE
R2175 75K
+100V
SW2190 MODE
SW2101 MILLIVOLTS/CM (B)
PROBE POWER
FRONT VIEW
-12.6V
-25V
CMD 863
INTERCONNECTORS & SWITCHING
TYPE 452



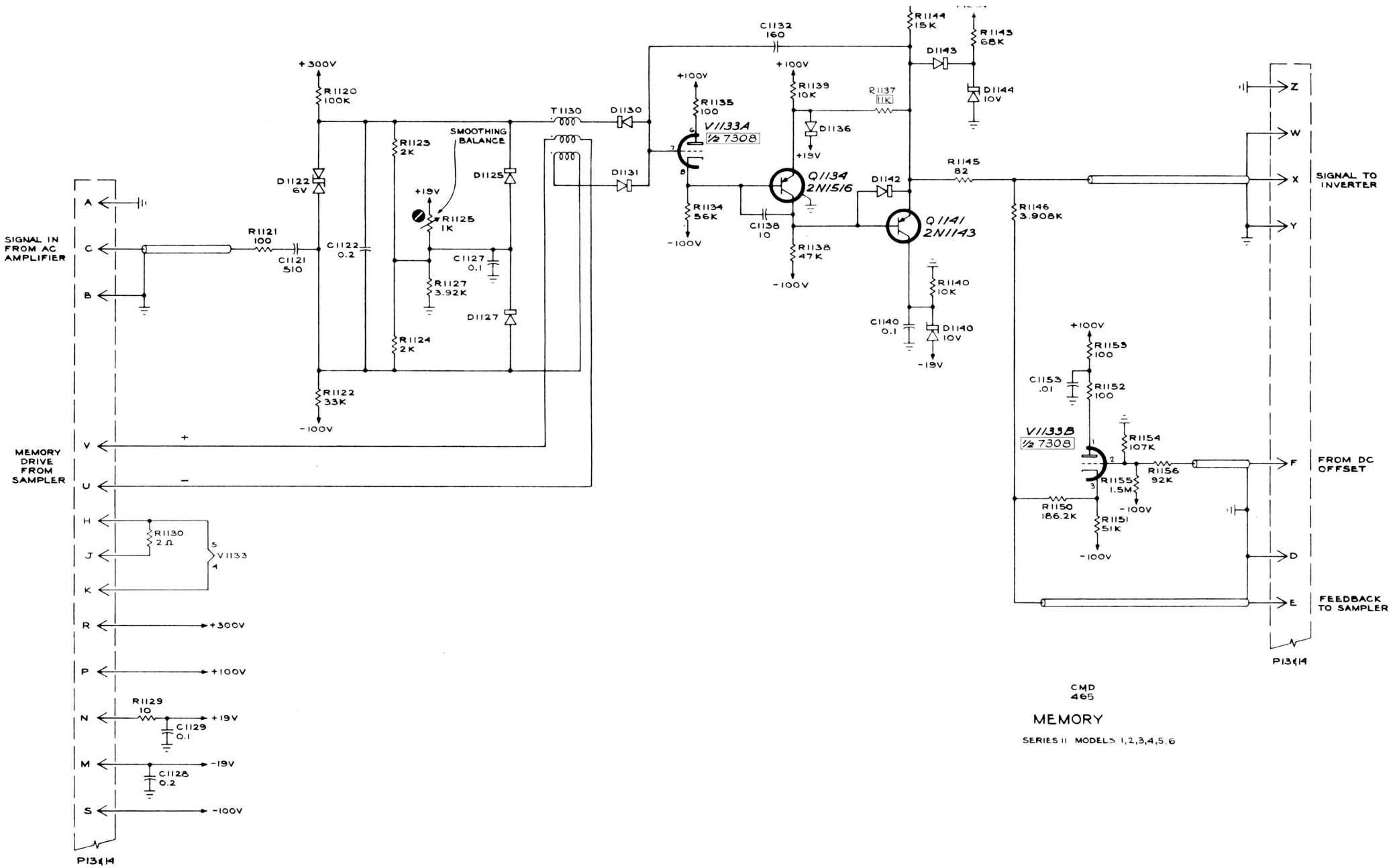
TYPE 4S2

CMD 863

MEMORY

SERIES 8 MODELS 1&2

A

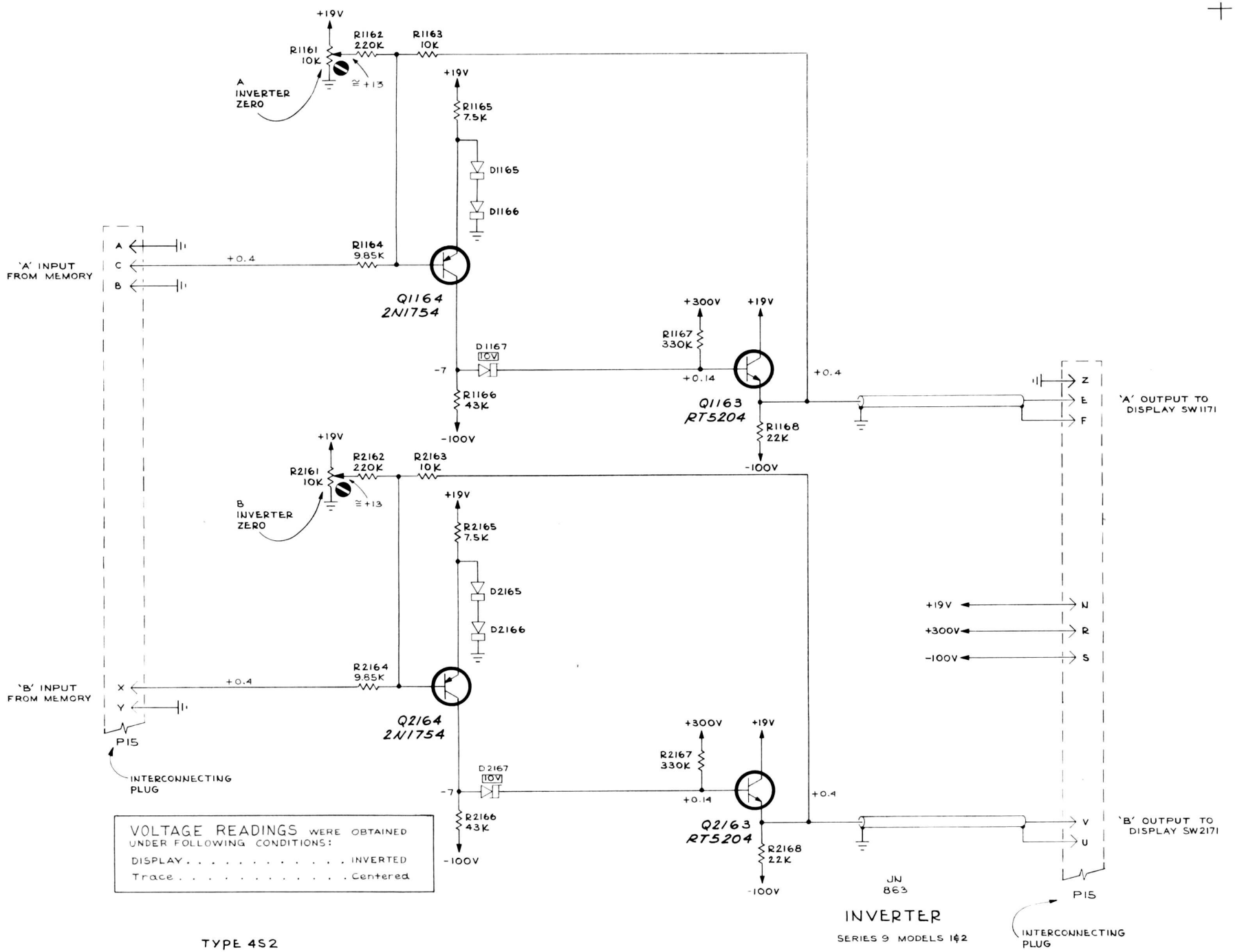


CMD 465

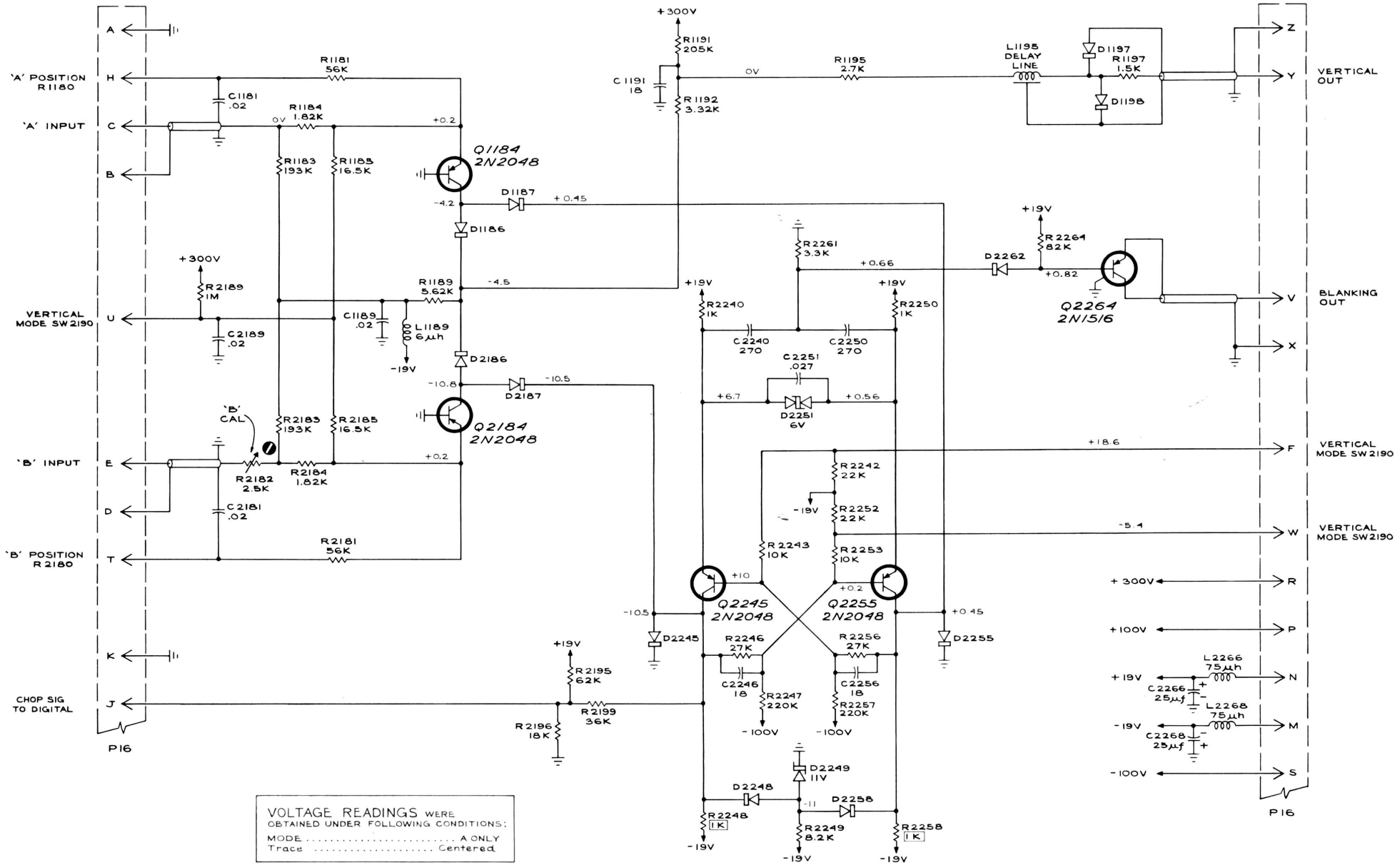
MEMORY

SERIES II MODELS 1,2,3,4,5,6

TYPE 452


+19V
R1161 10K
R1162 220K
R1163 10K
A INVERTER ZERO
≅ +13
R1165 7.5K
D1165
D1166
'A' INPUT FROM MEMORY
A
C
B
+0.4
R1164 9.85K
Q1164 2N1754
+300V
R1167 330K
D1167 10V
-7
+0.14
R1166 43K
-100V
Q1163 RT5204
R1168 22K
+0.4
Z
E
F
'A' OUTPUT TO DISPLAY SW1171
R2161 10K
R2162 220K
R2163 10K
B INVERTER ZERO
R2165 7.5K
D2165
D2166
'B' INPUT FROM MEMORY
X
Y
R2164 9.85K
Q2164 2N1754
R2167 330K
D2167 10V
R2166 43K
Q2163 RT5204
R2168 22K
+19V
+300V
-100V
N
R
S
V
U
'B' OUTPUT TO DISPLAY SW2171
P15
INTERCONNECTING PLUG
VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:
DISPLAY . . . . . INVERTED
Trace . . . . . Centered
JN 863
INVERTER
SERIES 9 MODELS 1&2
INTERCONNECTING PLUG

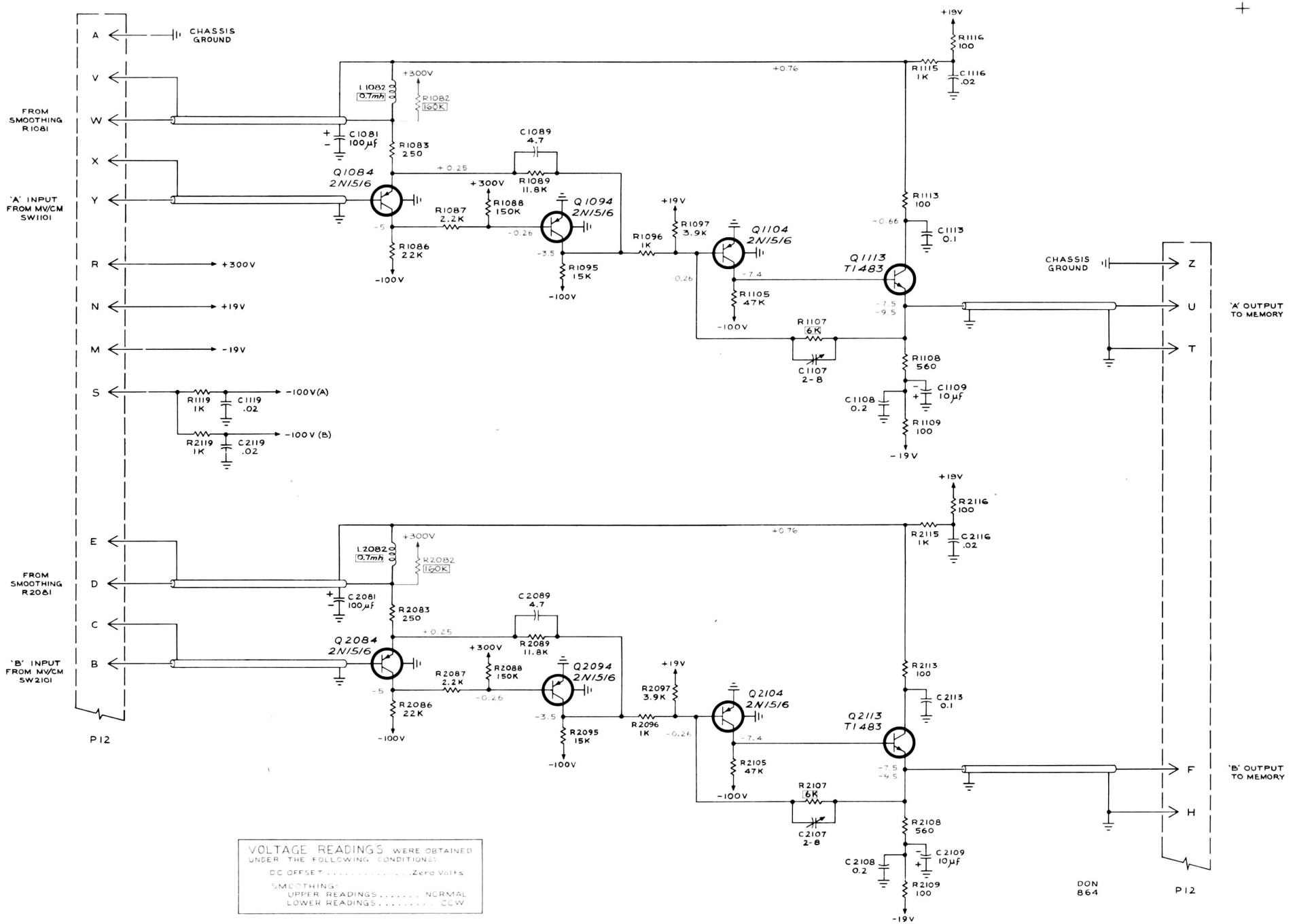
TYPE 452



TYPE 452

CMD 863

B



TYPE 452

AC AMPLIFIER

SERIES 2
MODELS 2,3,4,5