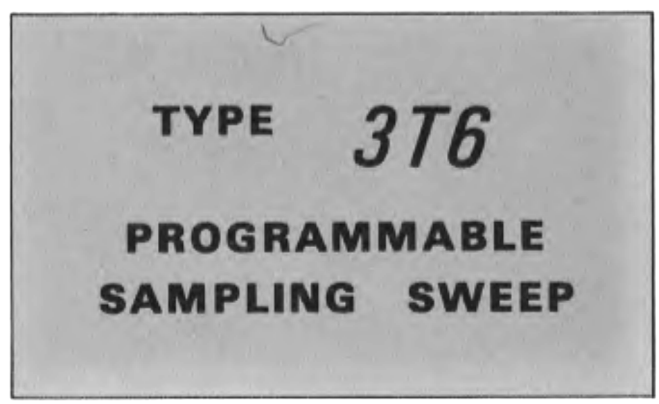
INSTRUCTION MANUAL

Serial Number _____



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070-0761-00

1068


TYPE 3T6 PROGRAMMABLE SAMPLING SWEEP
HORIZ POS
HORIZ GAIN
TIME/DIV
TIME/DIV
DECADE
MULTIPLIER
SAMPLES/SWEEP
1
1000
POSITION
DELAY
0 0 0 0
PROGRAM SELECTOR
INT
EXT
TRIGGER
SENSITIVITY
RECOVERY TIME
MODE
POLARITY
INT
EXT
SYNC
AUTO
SERIAL
TEKTRONIX
EXTERNAL PROGRAM

SECTION 1
SPECIFICATION

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

The Type 3T6 Programmable Sampling Sweep unit provides a wide range of equivalent and real-time sweep rates. Accurate delay of the equivalent-time time window extends from 0 to 999.9 μs. All sweep rates, samples per sweep and equivalent time sampling sweep-start delay times are controlled either at the front panel or by an external programmer. When using external triggering, use of the automatic triggering feature will maintain proper triggering over a wide range of trigger amplitudes and repetition rates. Special external high-speed programming of the Type 3T6 increases the number of measurements per second that can be made in the system described in Section 2 under High-Speed Programming.

The Type 3T6 is intended for use with the Type 568 Oscilloscope. Any Tektronix 3S-series sampling unit may be used with the Type 3T6, normal use recommended to be with the Type 3S6 Programmable Sampling Unit.

The Type 3T6 and Type 3S6 can be externally programmed from connectors on the rear panel of a Type 568 Oscilloscope. The external program connector at the rear of the Type 568 can be connected to a Tektronix Type 240 Program Control Unit, or the Type 241 Programmer.

The Type 3T6 provides all necessary timing information for making accurate measurements when operated with a Tektronix digital readout system such as the Type 568-Type 230, or the Type 567-Type 6R1A.

With the Type 3T6 PROGRAM SELECTOR set at INT, sweep rate, delay, and samples/sweep (sweep reset) are all manually controlled at the 3T6 front panel. With the PROGRAM SELECTOR at EXT, sweep rate, delay, sweep reset, and dot density may all be externally programmed.

Characteristics

The following characteristics apply over an ambient temperature range of 0° C to +50° C and after a five minute warmup, providing the instrument was calibrated at a temperature between +20° C and +30° C.

Characteristics listed below apply for either front panel operation or external programming only after the Type 3T6 front panel control (HORIZ GAIN) has been properly adjusted for the particular oscilloscope in which the unit is operating.

For particular system warmup requirements, refer to the main-frame oscilloscope instruction manual.

A procedure for mating the Type 3T6 to the oscilloscope can be found in the Operating Instructions section of this manual.

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement

NOTE

In the following trigger section, the amplitudes listed following the Sensitivity Range title are the ranges in which the TRIGGER SENSITIVITY control permits triggering at the low amplitude value, and allows the control to hold off the trigger circuits for signals up to the high amplitude value. However, satisfactory triggering can be obtained for most signals at amplitudes up to the maximum permitted. When using an external trigger signal the maximum trigger input voltage is ±1 V (DC + peak AC).

TRIGGERING	
External Trigger Input	
Input Impedance	Nominally 50 Ω
Maximum Input Voltage	±1 V (DC + Peak AC)
Trigger Requirements	
External SYNC	
Frequency Range	100 MHz to 1 GHz
Sensitivity Range	10 mV to 500 mV P-P
External Sine wave	
Frequency Range	1 Hz to 100 MHz
Sensitivity Range	10 mV to 500 mV P-P
External Pulse	
Frequency Range	DC to 100 MHz
Sensitivity Range	5 mV to 250 mV
Internal Sine wave	
Frequency Range	100 kHz to 100 MHz
Sensitivity Range	100 mV to 2 V P-P
Internal Pulse	
Frequency Range	1 Hz to 100 MHz
Sensitivity Range	100 mV to 2 V
External Auto	
Frequency Range	DC to 100 MHz
Amplitude Range	100 mV to 500 mV
Pretrigger Requirement (lead time required for	

ELECTRICAL CHARACTERISTICS (Cont)	
Characteristic	**Performance Requirement**
3T6 alone to position the triggering edge 1 div from sweep start)	
TIME/DIV	
10 ns	44 ns within 20%
100 ns	141 ns within 20%
1 μs	1 μs within 20%
10 μs	10 μs within 20%
100 μs	100 μs within 20%
500 μs	500 μs within 20%
Trigger Jitter	
Internal	
Sine wave	200 ps or less with 1 V P-P signal at 30 MHz
Pulse	30 ps or less with 500 mV pulse, 2 ns or less wide
External	
Sine wave	200 ps or less with 100 mV P-P signal at 30 MHz
Pulse	30 ps or less with 50 mV pulse, 2 ns or less wide
External Automatic	
Sine wave	200 ps or less with 300 mV P-P signal at 30 MHz
Pulse	30 ps or less with 300 mV pulse, 2 ns or less wide
External Sync	50 ps or less with 100 mV P-P signal at 1 GHz
RECOVERY TIME Range (Reset time)	At least 1.25:1

SWEEP RATES	
TIME/DIV Range	
Real Time	500 ms to 1 ms in 9 calibrated steps, 1-2-5 sequence
Accuracy	Within 3%
Equivalent Time	500 μs to 100 ps in 21 calibrated steps, 1-2-5 sequence.
Accuracy	Within 3% except as noted below
500 μs to 200 μs	Exclude first 150 μs of sweep
100 μs to 20 μs	Exclude first 15 μs of sweep
10 μs to 2 μs	Exclude first 1.5 μs of sweep
1 μs to 200 ns	Exclude first 150 ns of sweep
100 ns to 20 ns	Exclude first 15 ns of sweep
10 ns to 2 ns	Exclude first 15 ns of sweep
1 ns to 100 ps	Exclude first 15 ns of sweep

Characteristic	Performance Requirement
	DELAY
DELAY Range	
TIME/DIV	
500 μs to 2 μs	0 to 999.9 μs in 100 ns increments
1 μs to 1 ns	0 to 9.999 μs in 1 ns increments
500 ps to 100 ps	0 to 999.9 ns in 100 ps increments
DELAY Accuracy (with A B C D representing the Delay Window Integers)	Within 3% (see below)
0 to 1 ms	$\frac{AB+3CD}{AB+CD}$ = max error in %
0 to 10 μs	$\frac{AB+3CD}{AB+CD}$ = max error in %
0 to 1 μs	$\frac{A+3BCD}{A+BCD}$ = max error in %

HORIZONTAL DEFLECTION	
Dot Density	
1 SAMPLE/SWEEP	Dot stationary at sweep start
100 SAMPLES/SWEEP	+20%, –0%, at 100 kHz (available only when externally programming, and then only with DECADE set for equivalent time)
1000 SAMPLES/SWEEP	Within 0.5% at 100 kHz, within 3% at 30 Hz
Horizontal Positioning Range	At least 4 divisions
Horizontal Gain Range	At least 1.5:1
Position Indicators	Appropriate indicator on, the other off when trace is positioned 5 divisions from graticule center

PROGRAMMABLE FUNCTIONS	
Auto Calibration Sensitivity	Approximately 1% change in timing for each 75 μA change in timing current.
External Programming	Negative logic
True (logical ONE)	0 V to +2 V
False (logical ZERO)	+6 V to +15 V or open circuit

ENVIRONMENTAL CHARACTERISTICS	
Storage Temperature — −40° C to +65° C	Operating Temperature — As stated above Electrical Characteristics table
Altitude - To 50,000 feet	Altitude — To 15,000 feet

MECHANICAL CHARACTERISTICS	
Dimensions — Height	≈6 1/4 inches
Width	≈ 4 1/4 inches
Length	≈ 14 1/2 inches
Construction	Aluminum alloy chassis with epoxy laminated circuit boards. Front panel is anodized aluminum.
Accessories	An illustrated list of the accessories supplied with the Type 3T6 is at the end of the Mechanical Parts List pullout pages.

SECTION 3
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

General

The Type 3T6 Programmable Sampling Sweep unit has two basic modes of operation. The chief difference between them is that one mode constructs an equivalent time display by a conventional (sequential) process requiring that the signal be repeated for each sample, and the other mode presents a real time display of any one signal. Neither mode can display the triggering event itself without a signal delay to the sampling unit, or a pretrigger event to the Type 3T6. The instrument changes modes automatically when the sweep rate is changed from 500 μs/div to 1 ms/div, and vice versa. A fixed range of the signal time region is viewed in either mode. In DECADES 1, 2 and 3 the mode is real time and in DECADES 4 through 0 the mode is equivalent time. Only the equivalent time mode allows the time region to be positioned (delayed) away from (after) the triggering event (T_0) that starts the process for one equivalent time sweep. Time positioning of the sampled time region is referred to as the positioning of a time window. Time window positioning (delay) is not available when the unit is presenting a real time sampling display.

When the Type 3T6 is producing an equivalent time display, the time window can be positioned by the DELAY switches to start just after trigger recognition. The actual minimum delay time after trigger recognition is discussed in the Operating Instructions, as is the maximum delay time.

Another important feature of the Type 3T6 is that its operation can be controlled remotely by special programming equipment. Remote programming is discussed in detail in the Operating Instructions, and later in this section during the Block Diagram description. First, the two modes of sweep generation are discussed.

Sweep Generation

Sweep generation[1] within the Type 3T6 is different for equivalent time than for real time mode of operation. The primary difference is in the operation of the triggering circuits and the method of timing the step drive sent to the staircase generator. Fig. 3-1 shows a simplified representation of sweep voltage vs CRT display dot position for both modes of operation. Real time operation causes the period between staircase step drive pulses to be constant, while the equivalent time operation may present a valid display with considerable variation in time between staircase drive pulses.

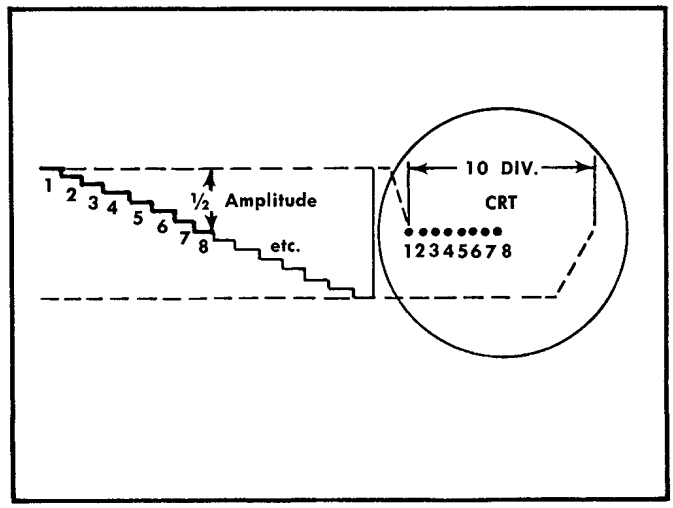


Fig. 3-1. Staircase signal and sequential dot display.

Fig. 3-1 shows a simplified picture of the way in which both equivalent time and real time sweep generation move the dot across the CRT. The figure shows uniform voltage steps and time duration of each part of the staircase signal. Such conditions are true for real time sampling, but equivalent time sampling can require non-uniform time periods for each staircase step.

Equivalent Time Sampling Process

The equivalent time sampling process is shown in basic form in Fig. 3-2. The waveforms represent just two samples in a sequence, such as the fifth and sixth dots of a 1000-dot display. Each waveform is identified with its block, or with interconnections in the adjacent block diagram.

The trigger regenerator circuit is the master programmer of Fig. 3-2. It delivers a positive step pulse at the time of trigger recognition, T_0, to start the process that takes and displays one sample. Immediately after T_0 the trigger circuits lock out any more triggers until the rest of the circuits have operated and the dot has been properly displayed. (The period of time during which triggers are locked out is called the holdoff time, and is made variable by the Type 3T6 front panel RECOVERY TIME control. See the Operating Instructions for RECOVERY TIME control uses.)

[1]**Compare this part of the circuit description with the sampling unit (Type 3S5 or 3S6) instruction manual section on Tektronix Sampling Principles for a more complete understanding.**

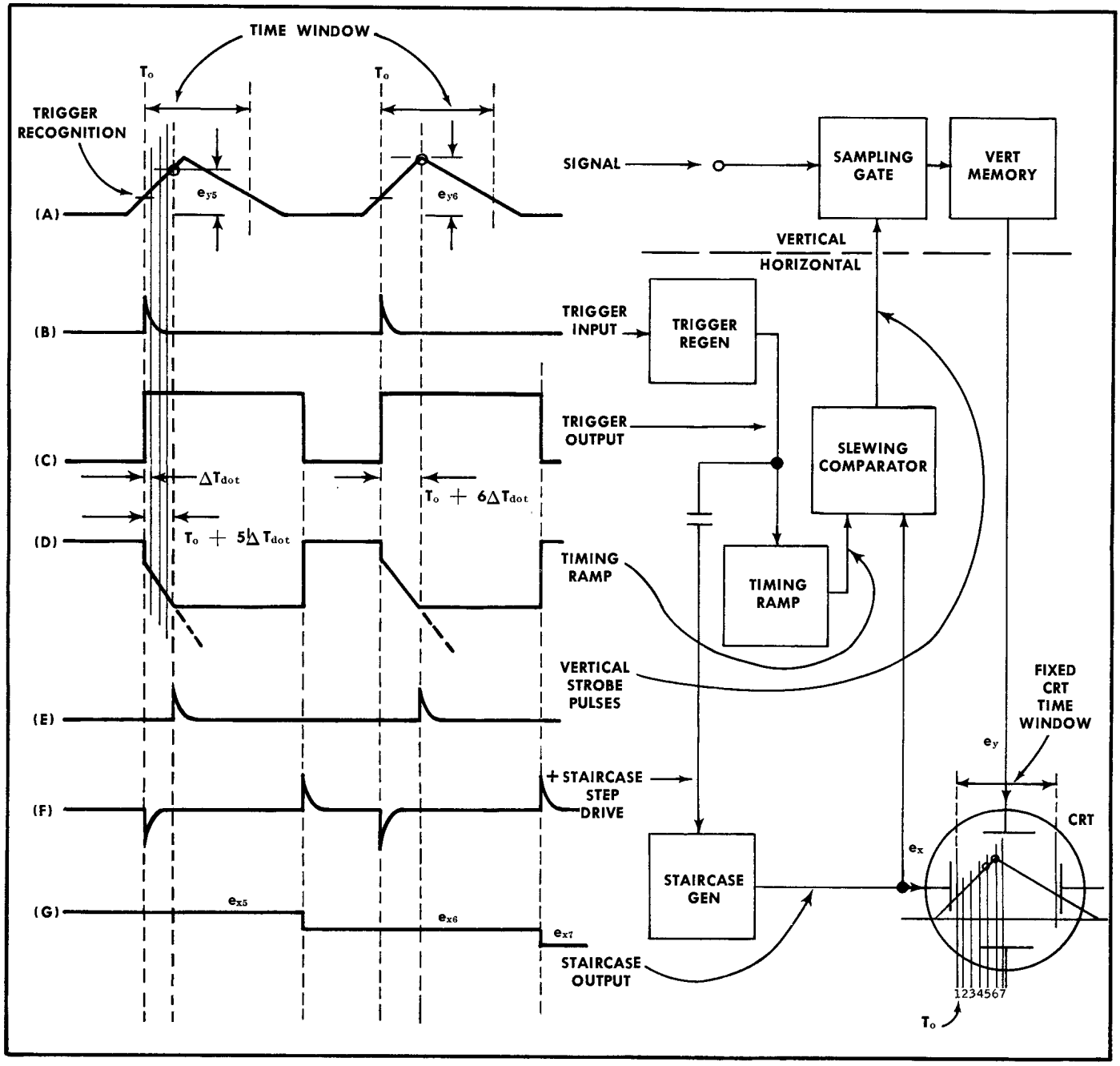


Fig. 3-2. Basic equivalent time sampling oscilloscope.

At T_o, the trigger circuit starts the timing ramp running in a negative direction. The timing ramp "times" the occurrence of the strobe drive pulse sent to the vertical sampling unit as the timing ramp is compared with the voltage of the staircase generator in the Slewing Comparator block. Since the staircase output signal voltage is different for each trigger circuit output pulse, the timing ramp is allowed to run down farther for each successive sample. The result is a time "slewing" of successive sampling times. The slewing increment is identified in Fig. 3-2 as ΔT_{dot} and is a fixed time increment per sample. ΔT_{dot} is set by both the timing ramp slope and the staircase step amplitude.

The waveforms of Fig. 3-2 imply that there can be a CRT dot displayed from the time of the vertical strobe pulse to the time of the timing ramp reset. Actually the CRT blanking is also controlled by the vertical sampling unit. The vertical unit prevents CRT beam current at the time of the vertical strobe pulse and until the vertical memory is stable, typically for 2 to 3 μs.

Adding Sweep Rate and Movable Time Window Controls

The time window (sampled signal time domain) identi-

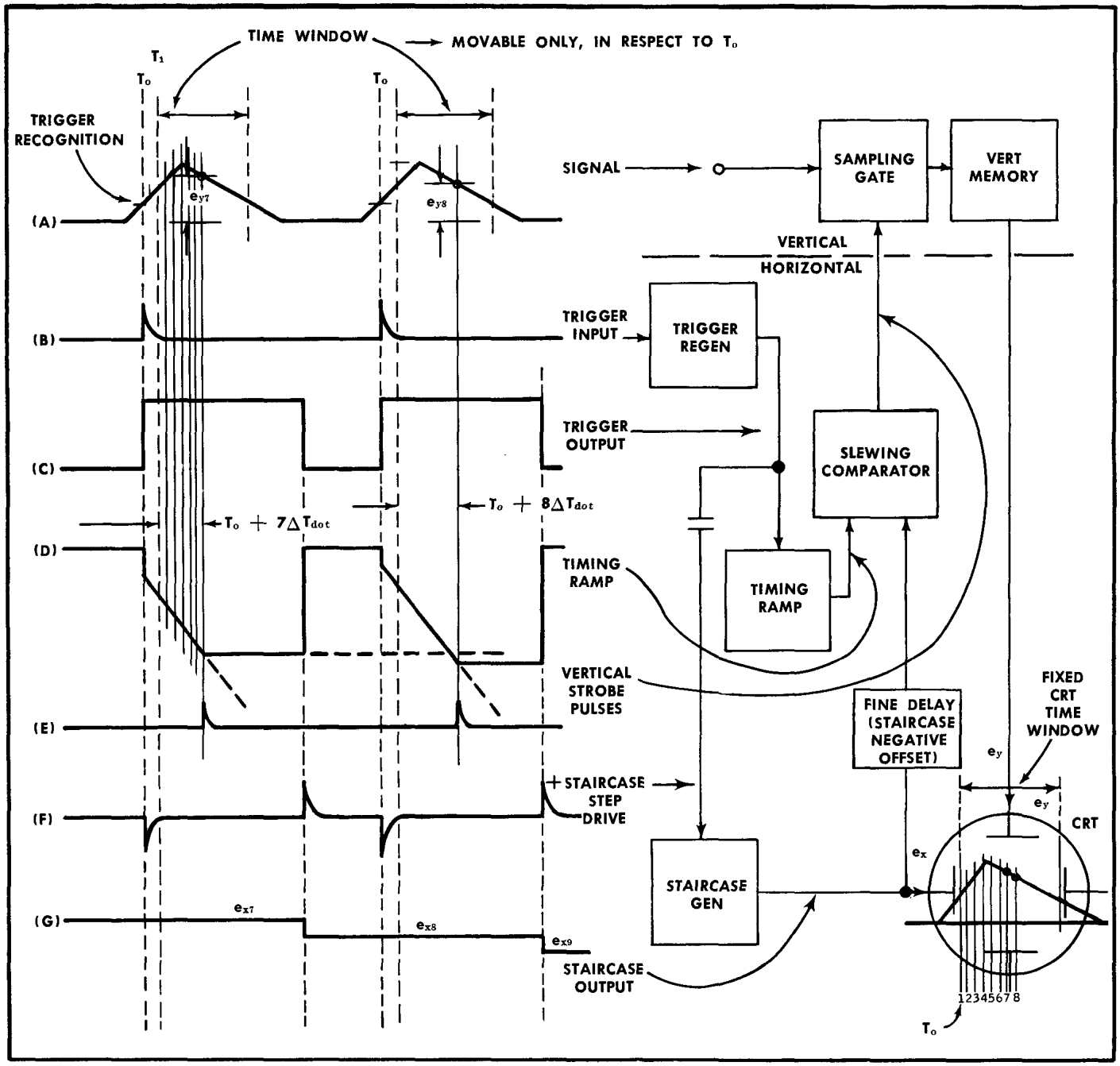


Fig. 3-3. Adding a time-window Delay control to basic block of Fig. 3-2.

fied in Fig. 3-2 can be moved so that a different portion of the signal is displayed. Fig. 3-3 shows a Delay control added between the Staircase Gen block and the Slewing Comparator block. This new circuit allows a negative DC voltage offset to be applied to the staircase signal that is compared with the timing ramp signal. Since the comparator block is a DC coupled comparator, changing the DC level of the staircase signal in a negative direction causes the timing ramp signal to travel farther negative before comparison occurs. Since the timing ramp signal is a ramp, the more negative comparison results in a later comparison and later vertical strobe pulses than before the staircase signal was offset.

The staircase signal sent to the CRT is not altered; thus, the voltages that set the CRT dot positions are not changed, the first dot occurring at the CRT left side. If the Delay control applies a negative offset to the staircase signal that feeds the comparator block, the first displayed dot at the CRT left side will have a vertical voltage related to the signal amplitude at time T_1 (see Fig. 3-3 upper left). The result is an apparent horizontal shift of the displayed signal

to the left. The circuits of the Type 3T6 allow only a negative offset to be applied to the staircase signal, thus permitting the movable time window to include only portions of the signal AFTER trigger recognition time, T_o.

Fig. 3-3 does not show any method that will alter the equivalent time sweep rate. Two different controls are used to alter the Type 3T6 sweep rate. One is called the Decade control and the other the Multiplier control. Both controls operate BCD digital logic circuits that change the equivalent time sweep rate thus: the slope of the Timing Ramp is altered and the Staircase signal amplitude is altered before it is sent to the Slewing Comparator block.

To decrease the rate of fall (dV/dt) of the timing ramp is to increase the time assigned to ΔT_{dot} (ΔT_{dot} is the equivalent time between dots). If the staircase signal to the CRT is not altered and the real time presentation of dots is not altered, increasing ΔT_{dot} makes the display have a slower equivalent time sweep rate (more time per CRT division). A slower sweep rate will allow a longer period of the input signal to be displayed.

To increase the rate of fall of the timing ramp is to speed up the equivalent time sweep rate. The Type 3T6 also alters the trigger circuit reset time to avoid display confusion, so the trigger circuits don't recognize the input signal until after the dot has been properly displayed.

To reduce the amplitude of the staircase signal sent to the Slewing Comparator block is to reduce the time assigned to ΔT_{dot}. Since the staircase signal to the CRT is not altered, and the real time presentation of dots is not altered, reducing ΔT_{dot} makes the display have a shorter equivalent time sweep rate (less time per CRT division).

Sweep Generation, Real Time

The real time sampling process is shown in basic form in Fig. 3-4. The waveforms represent two full sweeps, with 7 samples shown for the first sweep. Instead of the Trigger Regenerator initiating all of an individual sample cycle, it starts the cycle for one full sweep, and is then locked out until after the Staircase Generator resets and is ready to start another sweep. The Staircase Generator steps are driven by a Clock and Counter circuit that controls the time between samples and ensures that once started, the samples occur at a precision rate until the end of each sweep.

At T_o, the trigger circuit sends a start pulse to the Clock and Counter circuit. The Clock and Counter circuit delivers pulses to the Strobe Driver, which sends pulses to both the Staircase Generator and the vertical sampling unit. Just as soon as the Staircase Generator starts, the Trigger Lockout circuit inhibits the trigger circuit from responding to any more trigger input signals until after a full sweep has been completed. (The maximum real time Clock and Counter rate is 100 kHz in the Type 3T6.)

The real-time time window cannot be delayed (positioned) with respect to T_o; therefore, the display beginning always occurs at T_o. The dot sequence must include many dots for each vertical signal cycle in order to present a meaningful display. Too few dots per signal cycle cause distortion that may make the display difficult to interpret. It is this characteristic of real time sampling along with the maximum sampling rate, which limits the upper signal frequency that can be properly displayed.

BLOCK DIAGRAM

Two complete block diagrams appear at the back of this manual preceding the main circuit diagrams. The first applies to equivalent time operation, and the second to real time operation. Circuits not used for each of the two modes of operation are shaded to show a visual contrast with the circuits in use.

Central Timing Logic Block (both diagrams)

The three blocks in the upper right corner outline the integrated circuit numbers used to convert the DECADE and MULTIPLIER switches (or external program) binary coded decimal inputs to actuate proper internal circuits and digital unit control lines. (Note that the T2 line of the three Muliplier lines is dashed. That means it is not actually connected internally, but that an external program connector pin is made available so three-line BCD negative logic programmers can be used without confusion.) The sweep rate (both equivalent and real time) is equal to a three line BCD Multiplier binary number multiplied by 10 to the −E power (T X 10^{-E} SEC/div); where E is a BCD Decade (0=10) binary number. These two numbers are read into the Type 3T6 as 3 and 4 Bit BCD numbers respectively. The Central Timing Logic block converts information from the two sets of BCD input lines to proper logic states of all output lines shown leaving the block. Lines going to the Digital Unit Control Logic block and the Sweep Rate Readout Logic block are not individually identified. However, other lines used throughout the other Type 3T6 circuits are identified by either assigned letters or Roman numerals (which are used as Boolean Algebra Symbols) and in most cases with names and pin numbers to show their true function. All lines drawn horizontally to the right of the Central Timing Logic block have the pin numbers of either the Logic One or Logic Two circuit card interconnecting jack included, so that a test oscilloscope can be used to check the output function during maintenance or troubleshooting. The four lines leaving the bottom of the Central Timing Logic block and the one line leaving the left side of the Sweep Rate Readout Logic block all control only the real time sweep rate. Only the bottom two of the fourteen lines leaving the right side of the Central Timing Logic block are used in real time operation. All fourteen lines are used during equivalent time operation.

The Digital Unit Control Logic block does not function until the associated digital unit (Type 230)delivers a logical ONE at the D, U, GND line. When the digital unit grounds the D, U, GND line, the integrated circuits of the Digital Unit Control Logic block control the readout units-of-measure and decimal (including the M, N and μ multipliers)

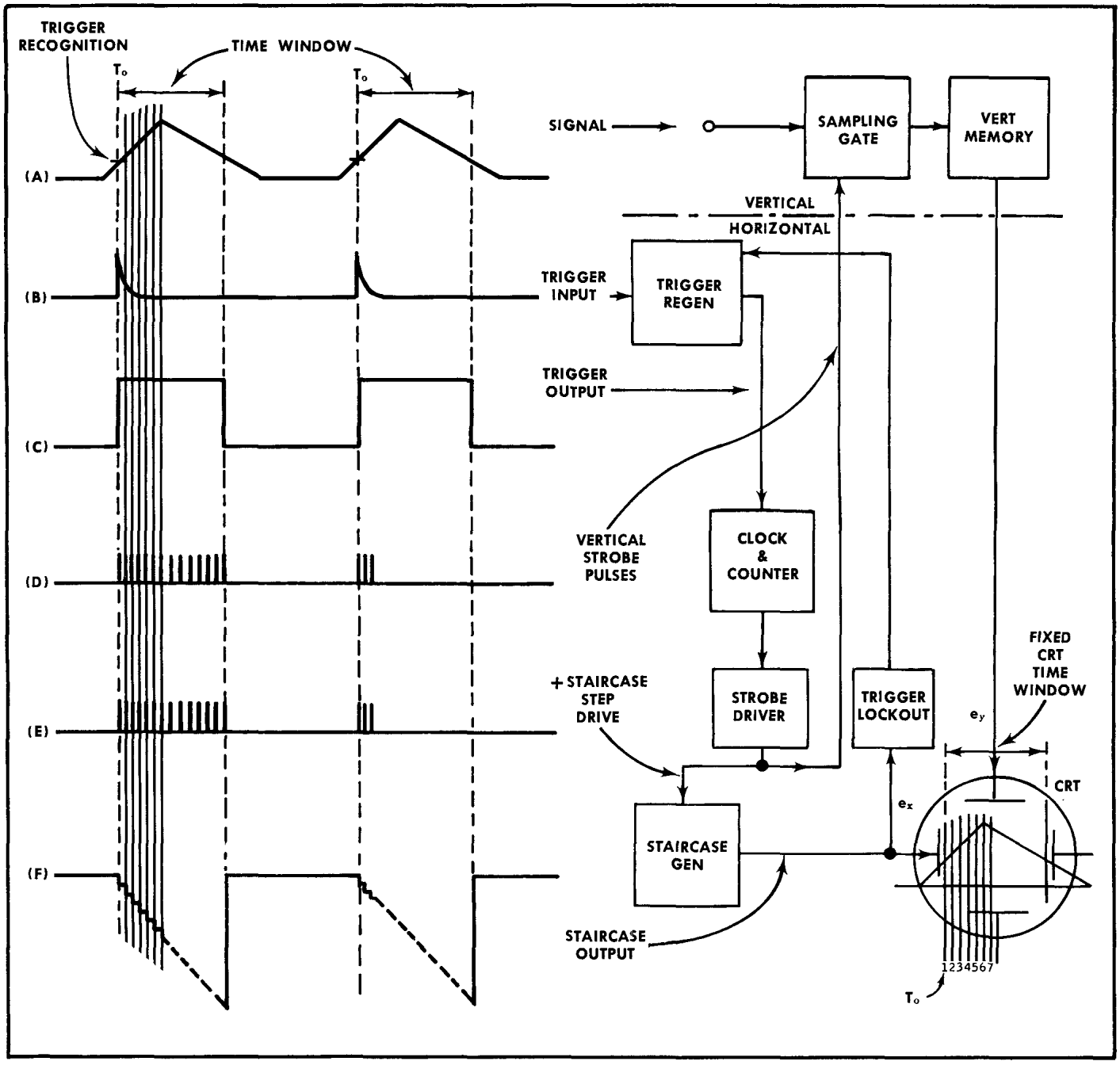


Fig. 3-4. Basic real time sampling oscilloscope.

of the digital unit. Correct output lines are a logical ONE (saturated transistor that grounds the line) for whichever digital unit decimal and unit-of-measure is required by the particular sweep rate in use. The digital unit makes its actual time measurement using the Digital Clock signal diagrammed at the block diagram lower right and leaving the Type 3T6 at P21, pin 13. All Digital Unit Control Logic block output lines are a logical ZERO (up, and at about +8 volts when used with the Type 230) when the digital unit calls for an amplitude (Volts or Amps) measurement and the D, U, GND line is a logical ZERO (up).

The Sweep Rate Readout Logic block operates the Type 3T6 incandescent lamps in the TIME/DIV readout window located on the front panel. (The incandescent lamps of the DELAY switches, ns, μs and the decimal, are all operated directly from the DELAY switch contacts, and are therefore not included in the block diagrams. These lamps are turned off for both real time sweep rates and when the Type 3T6 is externally programmed.)

Equivalent Time Sampling Block

The basic Trigger Regenerator block of Fig. 3-1 is shown at the upper left corner of the main block diagrams as the Trigger and Clock. All of the circuits of schematic diagram

1 are included. The Trigger and Clock circuits start the sampling process for each individual sample trigger recognition, and then automatically reject any more input triggers until reset by other circuits. Reset begins at the end of the Timing Ramp by a signal from the Timing Ramp Reset Comparator. Reset duration is prolonged by the Reset Ramp and Reset Multi until a time when all other circuits have completed their functions and are ready for another sample to be taken.

Assume that all circuits are ready for another sample to be taken, and that only the trigger must arrive to start the process. The conditions and sequence of operation for one sample follow.

Condition

1. D28 and D106 are both at their low voltage state, D106 taking some of the arming current from the Reset Multi through D110. D112 is cut off and D114 and D168 are at their low voltage state. The 10 MHz Oscillator Clock is clamped (and not running) by the Clock Osc Clamp. The Clock Osc Clamp causes the Trigger Inhibit (Q135) to release the Isolation Amp so a trigger can be received at D28.

2. D168 is at its low voltage state with one or two arming currents applied. Initial bias is applied from the Reset Multi block, and arming current may be supplied by U440 via R168. Whether the second arming current is applied depends upon the position of the X100 and X1000 DELAY dials (or external programmed delay). When the X100 and X1000 Delay lines are programmed for a digital zero, U440 applies a steady arming bias to D168. When either set of lines is programmed for other than a digital zero, U440 applies a steady arming bias to D168. When either set of lines is programmed for other than a digital zero, U440 applies its arming current to D168 only after the Clock Counter has made an appropriate count. D168 remains at its low voltage state with both arming biases and holds the Ramp Clamp in a state to hold the Timing Ramp at its starting voltage.

3. The Trigger Reset Multi has set the Counter Reset block to a state that reset the 100/1 Divider and the two decades of the Clock Counter. The two decades of the Clock Counter are reset to zero. If the X100 or X1000 Delay programming is other than zero, U440 removes the arming bias to D168 until a later time.

NOTE

Two arming bias situations have just been described. The first allows D168 to start the sampling process exactly at the time a trigger signal reaches D114. The second delays D168 arming bias from U440 until the Counters have counted out the programmed delay. After the programmed count, U440 arms D168, which can then be tripped to its high state by the next pulse from the Clock Current Pulser to start the sampling process.

4. The Staircase Generator (block diagram lower right) is resting at a fixed DC voltage output. The DC value depends upon whether the next trigger starts the first dot of a full sweep or whether the trigger starts a dot somewhere along the sweep.

Operation Sequence:

1. The trigger signal arrives, passes through the Isolation Amp and causes D28 to switch to its high voltage state. Almost immediately D106 switches to its high voltage state, causing some of the Reset Multi arming bias to go through D112 to D114. D110 is now at cutoff, and thus prevents any Isolation Amp output signal from propagating into D114 via D112. The trigger signal from D28 is also delayed (through a 5 ns Delay Line) and then trips D114 to its high voltage state. As D114 reaches its high voltage state, D110 again conducts, holding D106 at its high voltage state and locking out any more triggers to D114. D114 remains at its high state until reset later.

2. As D114 steps to its high voltage state, a pulse is sent through C118 to D168. D168 may respond if U440 is providing its arming bias. If U440 is not providing arming bias, the pulse through C118 has no effect upon D168.

D114 also starts a pulse through the Clock Start Delay and Clock Osc Clamp blocks that will start the 10 MHz clock oscillator so as to produce the first clock current pulse exactly 100 ns later.

NOTE

Now the two choices of arming D168 by U440 have significance. If the X100 and X1000 Delay lines are both digital zeros, the Timing Ramp is started by D168 when D114 goes to its high voltage state. If either of the X100 or X1000 Delay lines is not a digital zero, D168 is armed later by U440 and then tripped to its high voltage state at the next clock current pulse from Q160. Also, with X100 and X1000 both zeros, D168 starts the Timing Ramp immediately after a trigger pulse. Once D168 is at its high voltage state, only the Reset Multi can reset it to the low voltage state; removing U440 arming bias has no effect upon D168. Thus it can be said that the 100/1 Divider, Clock Counter and both Digital Comparator blocks serve no useful purpose for the special case when both X100 and X1000 Delay lines are digital zeros.

As the 10 MHz Oscillator Clock starts, the Trigger Inhibit block (Q135) takes current away from D28, preventing it from recognizing any more input trigger signals.

3. The 10 MHz clock delivers its signal to both the Clock Current Pulser and the Counter Clock Pulse Shaper. These blocks convert the oscillator sine wave signal to pulses, negative-edge actuating through the Shaper and positive-edge actuating through the Current Pulser.

The total Trigger and Clock circuits remain in the conditions of parts 2 and 3 until the end of the Timing Ramp.

4. As the Timing Ramp runs negative (from about +18 volts) two comparisons are made with it. One is a non-loading comparison at the Slewing Comparator block. The comparison is made between the Timing Ramp voltage and an attenuated staircase voltage that is related to the CRT deflection voltage. When the comparison occurs, a negative-going drive pulse causes the Strobe Driver block Avalanche transistor to deliver two very fast positive-going output pulses, one to the Staircase Stepper, and the other to the vertical channel sampling unit. These actions are described in 6 below.

The second Timing Ramp comparison is made in the Timing Ramp Reset Comparator block. The comparison is made with a fixed DC voltage that stops the ramp from running. (The DC voltage is altered, for the 100 ns Timing Ramp to increase the ramp negative limit. This increases the ramp time to a point that prevents resetting the Trigger circuits too soon, which would be the case if the voltage was not changed for the faster sweep rates.) At the time the ramp is stopped, the Timing Ramp Reset Comparator block sends a negative edge pulse to the Trigger circuit Reset Multi block.

5. The Reset Multi is turned off when the Timing Ramp is stopped. As the multi turns off, all arming current to D106 and D114 is stopped, and most of the arming current to D168 is stopped. D168 drops back to its low voltage state causing the Ramp Clamp to pull the Timing Ramp back up to +18 volts, ready for the next sample. At the same time, the Counter Reset block sends out a positive-going pulse whose leading edge resets the 100/1 Divider and the Clock Counter circuits.

The Reset Ramp runs for a period of time that assures an adequate CRT display of the sample taken a few nanoseconds after the non-loading slewing comparison described in 4 above and all circuits have settled down after reset. The trigger recognition circuits are inactive and cannot respond to any incoming triggers during the Reset Ramp running time. The Reset Ramp running time can be altered by the front panel RECOVERY TIME control to prevent problems in cases where its natural end occurs almost synchronously with a trigger signal arrival. As the ramp ends, the Reset Multi rearms the trigger circuit tunnel diodes and another sample cycle can be made.

6. The Strobe Driver output pulses mentioned in 4 above cause two actions. First, the Staircase Generator output voltage is stepped to place the CRT deflection voltages ready for a new horizontal dot position and for the next slewing comparison. Second, the vertical channel sampling unit receives a strobe command pulse telling it to take a sample of the input signal. Thus the Slewing Comparator and the Timing Ramp and Staircase Inverter are the circuits that assure there is a proper ΔT_{dot} equivalent time between successive samples of each full sweep sampling display.

Sweep Rate Control

The equivalent time sweep rate is changed in two ways. The primary method is to change the rate of the Timing Ramp. The secondary way is to change the amplitude of the staircase fed to the Slewing Comparator. The two methods are combined in a manner that changes ΔT_{dot} out of the Strobe Driver block. This in no way alters the position or number of dots presented in one horizontal scan. The number of samples per sweep is controlled by the Staircase Generator alone.

Changing the sweep rate is accomplished by Central Timing Logic signals sent to the Timing Ramp block, the Staircase Inverter Amp Input Resistors Attenuator block and the 0 Decade X10 Gain Switching block. The last two blocks are part of the Staircase Inverter amplifier which is an (inverting) operational amplifier with its gain set by the ratio of the feedback resistance to the input resistance. Thus, changing the value of either alters the amplitude of the inverted staircase used at the Slewing Comparator.

Changing the rate of the Timing Ramp does not alter the voltage of the slewing comparison, but changes the time after the Timing Ramp is started before the voltage reaches a value that allows the slewing comparison to occur.

Time Window Delay Control

Earlier in the equivalent time sampling sequence of operations, large increment time window delay was mentioned. The delay was stated as controlled by the X100 and X1000 lines fed to the Digital Comparator blocks. The delay was caused by delaying the arming of D168 and thus delaying the start of the Timing Ramp after trigger recognition, T_o.

Small increment time window delay is controlled by the two least significant digits of the DELAY controls (or external program), the Digital To Analog Amp block, and the Fine Delay Atten block. The small increment time window delay information is fed from the Fine Delay Atten block as a DC current into the summing input point of the Staircase Inverter Amp block operational amplifier. The Staircase Inverter Amp output signal staircase is offset by the fine delay information, changing the voltage value of the slewing comparison. This alters the generation of strobe drive in relation to trigger recognition, T_o.

Now the relation between total Timing Ramp length (and duration) and staircase average DC voltage is significant. With the two least significant DELAY dials at 0 (00), the staircase voltage entering the Slewing Comparator starts the first sample (of a sweep) very soon after the Timing Ramp starts. The staircase end comparison is made slightly less than half way down the Timing Ramp total voltage run. With the two least significant DELAY dials at 9 (99), the staircase voltage entering the Slewing Comparator starts the first sample (of a sweep) at a point part way down the Timing Ramp voltage run. The last staircase comparison is made very near the end of the Timing Ramp voltage run, which is almost twice the time delay (slewing) from T_o as was the case for the last sample when the DELAY dials were 00. Refer to the waveforms (D) and (G) of Fig. 3-3 for support of the above statements regarding slewing compari-

sons and staircase delay offset.

The total of the large increment delay (counter controlled) and the total of the small increment delay (staircase offset controlled) are listed in Table 2-4 in individual columns. The delay times are given for each equivalent time sweep rate. Also in Table 2-4 is a column headed Max. Total X10 and X1 Delay. That column lists the occurrence described above as the last staircase voltage slewing comparison when the two least significant DELAY dials are at 99. The table includes the combined large and small increment delays in the column headed Positionable End of Time Window After T_o. That column includes both kinds of delay and the time duration of the displayed time window for each equivalent time sweep rate.

Special Features, Staircase Generator

The Sweep Reset Tripper block allows either the front panel SAMPLES/SWEEP switch or an external program to reset the Staircase Generator back to its starting voltage. As long as the SAMPLES/SWEEP switch remains at 1, the display will be just one dot located at the sweep start. The circuit is intended primarily for externally programming a sweep reset at the end of a Type 230 measurement or after the last memory zone. It can be used in conjunction with the Sweep Speed-Up Enable block to reduce total measurement time, increasing the number of measurements that can be taken as compared to the number taken if the sweep continues running after the last zone or after the measurement is taken.

The Sweep Speed-Up Enable block allows an external programmer to speed the sweep rate from 100 samples/division to approximately 10 samples/division. When the Type 230 is controlling the sweep speed-up, there are 10 dots/div during non-zone time and 100 dots/div during zone time. The sweep is reset after the last zone. During the measurement sweep, there are 100 dots/div from sweep start to the end of the measurement, and the sweep is reset at the end of the measurement.

The Staircase Stepper block is actually part of the Staircase Generator itself, but is separated to highlight the function. The stepper responds to positive pulses from the Strobe Driver and controls the amplitude of the individual staircase steps. The stepper changes the staircase step amplitude to approximately 10 times as large as normal during the 10 samples/division sweep speed-up function.

The Staircase Reset Multi responds to both the Sweep Reset Tripper and to the staircase output signal. As the output signal reaches approximately +52 volts, the Reset Multi causes the steps to stop advancing the output voltage and quickly returns the output back to zero volts. Actually, samples are taken during the reset time, but the CRT is blanked by Q640 so there is no display evidence of the samples. Sampling during retrace is purposely provided so that the vertical channel memory circuits will never have to respond to full screen changes during retrace. (Full screen changes during retrace could occur if there were no samples taken between the end of a sweep at the graticule top and the next sweep beginning at the graticule bottom.)

Q605, and Q650 blocks provide needed information to the digital unit for digital measurements (in addition to the staircase voltage from the Staircase Generator). The four signals leave the block diagram at the lower right, through P22.

Real Time Sampling Block

Real Time operation uses the Staircase Generator in almost exactly the same manner as just described above. The only difference is that the samples per sweep cannot be altered because of the resultant change in real time sweep rate.

The trigger circuits are used in a manner similar to equivalent time operation. The trigger circuit is armed, then responds to a trigger and locks out other triggers for a definite period. The difference in real time operation is that only one trigger is required for a full sweep, rather than one trigger per sample as in equivalent time. Real time operation does not use D168, to prevent the Timing Ramp blocks (described earlier) from operating, but instead uses just one trigger to start the 10 MHz clock. The 10 MHz clock indirectly drives the Strobe driver and Staircase Generator. Once started, the clock continues to run until the Staircase Generator resets itself. As the Staircase Generator resets, it sends a clock-stop signal through the block labeled Trigger Circuit Control In Real Time to the trigger Reset Multi. As the trigger circuit is reset, the clock stops, one reset ramp runs to allow the staircase generator to fully reset, and then the Reset Multi rearms the trigger circuit, making it ready to receive another trigger and start another real time sweep.

The 10 MHz clock frequency is counted down to 100 kHz by the 100/1 Divider block for the fastest real time sweep rate of 1 ms/div. The Clock Counter block and the Real Time 1, 2, 5 Divider block do not enter into the clock dividing at 1 ms/div, but do operate at slower real time sweep rates. (1 ms/div is true because real time sweep rates always use 1000 samples per sweep. 100 kHz pulses have a 10 μs period. 1000 samples per sweep equals 100 samples/div. Then 100 pulses at 10 μs each equals 1 ms/div.) Note that the 100 kHz line from the 100/1 Divider block to the Clock Pulse Selector block is also labeled Decade 3. 1 ms/div, 2 ms/div and 5 ms/div all require the 100 kHz clock rate to be fed to the Real Time 1, 2, 5 Divider block.

A 10 ms/div sweep rate requires that the clock rate to the Strobe Driver have a 100 μs period. This is done by setting the DECADE switch to 2, and the MULTIPLIER switch to 1. Now the 2nd decade Clock Counter divides the 100/1 Divider 100 kHz signal to 10 kHz, which has a 100 μs pulse period. The same sort of division continues as the real time sweep rate is progressively made slower, including the use of the 1st decade Clock Counter when the DECADE switch is set to 1.

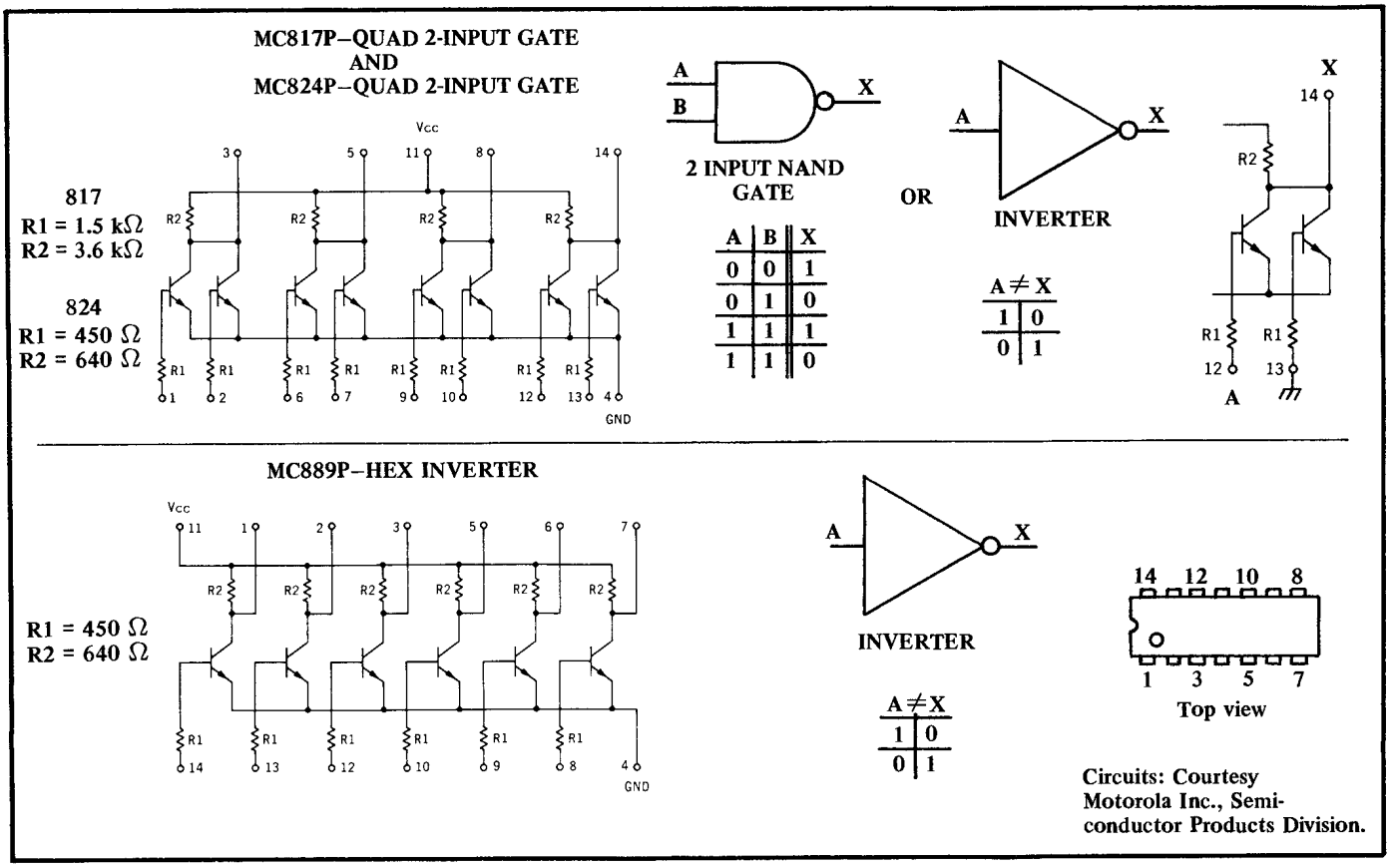


Fig. 3-5. Integrated circuit details. Negative logic symbols.

INTEGRATED CIRCUITS

Several schematic diagrams of the Type 3T6 are drawn using negative logic symbols only. Diagram 1 includes one positive logic OR gate. Internal circuit details, logic symbols and truth tables for all integrated circuits are contained in Figures 3-5 through 3-8. All but U180A are drawn with negative logic symbols, regardless of use within a circuit sequence or chain of events. Logic symbols are based on ASA Y32.14-1962 Standard, adopted as MIL Standard 806-C.

Details of input logic states for external programming are given in the Operating Instructions. Other limited internal logic details are given earlier in this section where a logic function is significant to the block diagram description.

Logic Voltages

Negative logic used internally in the Type 3T6 always means that a logical ONE is a low voltage from 0 V to about +0.2 V. A logical ZERO is basically an "up" voltage of about +1 V for IC's whose input leads do not contain resistors, and up to about +3 V for RTL units. Keeping these voltage limits in mind, defective units can be found using a voltmeter with at least an 11 MΩ input resistance and the truth tables given in Figures 3-5 through 3-8. Troubleshooting should be planned using the block diagram description and classical texts on counters and logic gates.

Each logic symbol can be tested for proper function without regard for the rest of the circuits as long as the logic symbols and truth tables are used.

All Motorola 14 pin flat-pack IC's have a top view pin order shown in Fig. 3-5.

CIRCUIT DESCRIPTION

General

The following pages include detailed circuit descriptions of those diagrams that contain transistors and other components in normal schematic form. Diagram pages that include only integrated circuit symbols are not described. See the Block Diagram description for details of the integrated circuit sections of the Type 3T6.

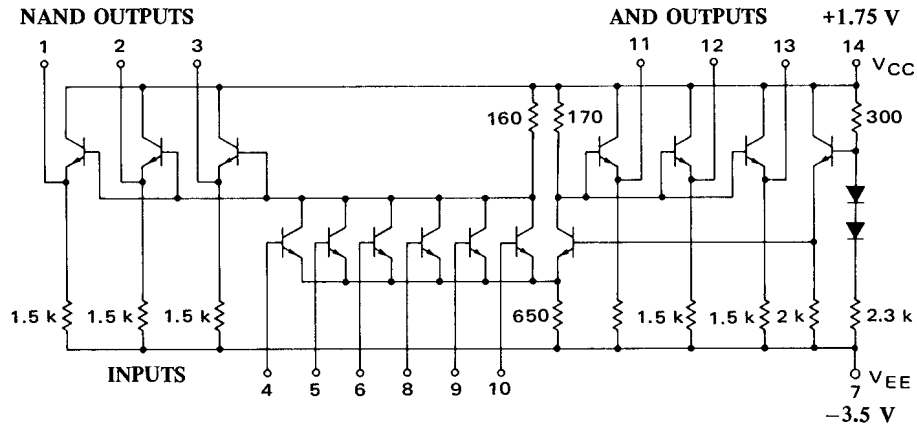
Trigger & Clock Circuits ①

The trigger circuit has an internal input through pins 3 and 4 of P21 and an external input through J5. The internal trigger is AC coupled through C1 to the TRIG MODE switch while L1 grounds the internal trigger input for DC signals. R4-R5 terminate the unused input to prevent noise pickup.

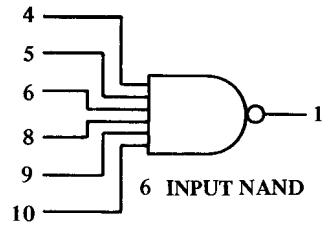
With the TRIGGER POLARITY switch in the plus position, the signal goes through P10 to drive Q20 emitter. In

(A)

6–INPUT GATES
MC1001P CIRCUIT SCHEMATIC



USED AT U440 ONLY



$\overline{1} = 4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10$

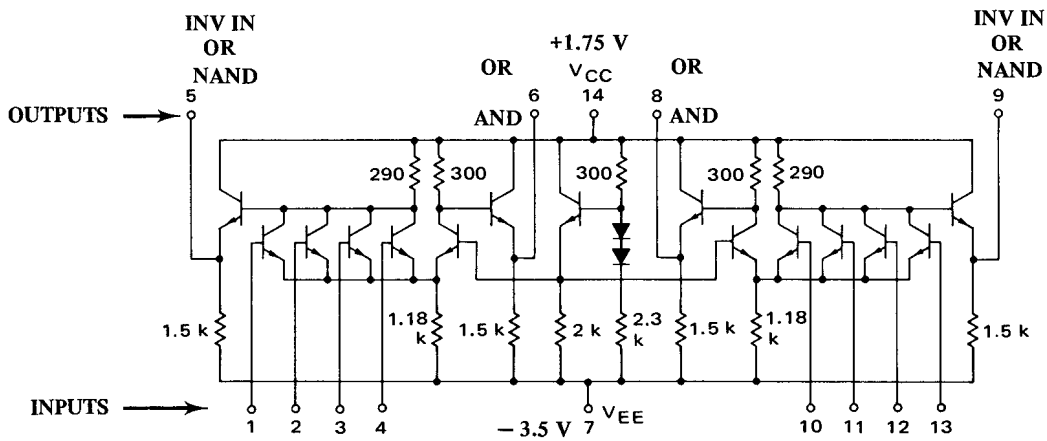
2 INPUT NAND GATE

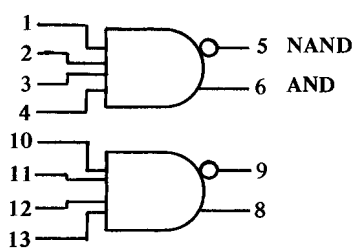
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

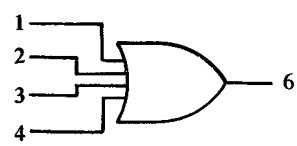
D168 ARMED →

(B)

DUAL 4–INPUT GATES
MC1004P CIRCUIT SCHEMATIC







Positive Logic OR gate
U180A only

$6 = 1 \cdot 2 \cdot 3 \cdot 4$

2 INPUT AND GATE

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

$5 = 1 \cdot 2 \cdot 3 \cdot 4$

2 INPUT NAND GATE

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

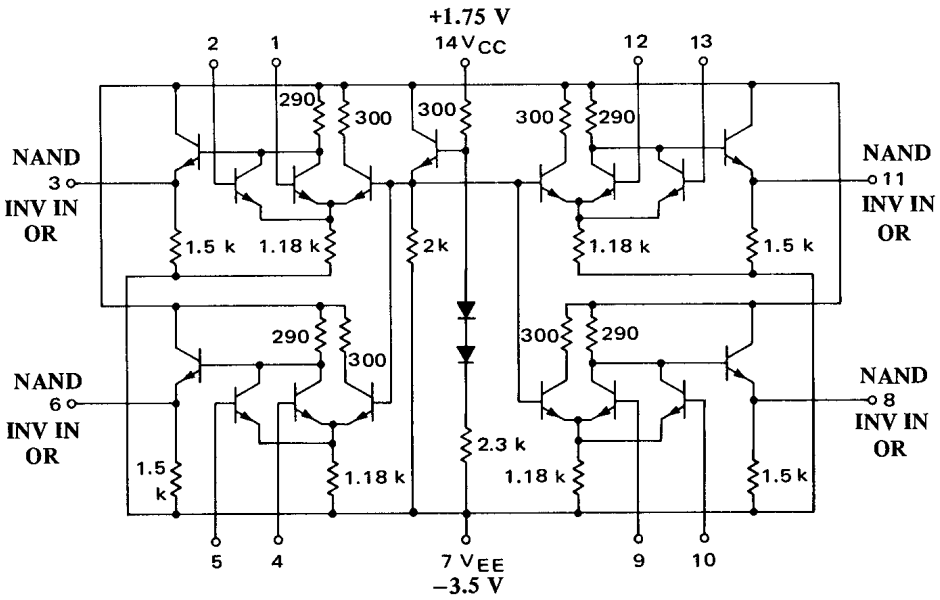
2 INPUT OR TRUTH TABLE

1	2	6
HI	HI	HI
LO	HI	HI
HI	LO	HI
LO	LO	LO

Circuits: Courtesy of Motorola Inc., Semiconductor Products Division.

Fig. 3-6. Integrated circuit details. Negative logic symbols.

MC1010P QUAD 2 INPUT GATE CIRCUIT SCHEMATIC



2 INPUT AND GATE

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$\overline{3} = 1 \cdot 2$

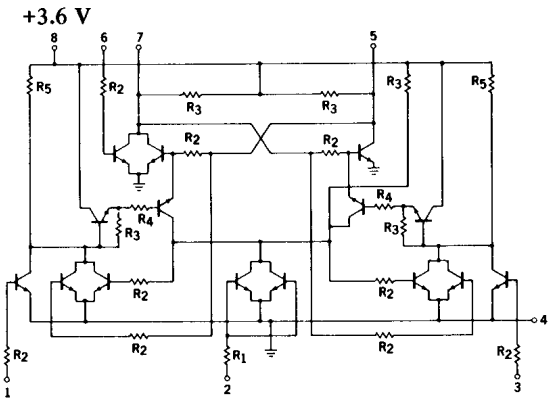
$\overline{6} = 4 \cdot 5$

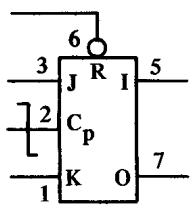
$\overline{8} = 9 \cdot 10$

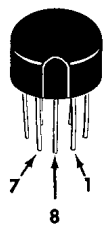
$\overline{11} = 12 \cdot 13$

Circuit: Courtesy of Motorola Inc., Semiconductor Products Division.

TYPE μL 923 (clocked J-K flipflop)







Top view

J	K	P	t^{n+1}	
0	0	0	0	1
0	0	0	0	1
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1
0	0	1	Q^n	*
0	1	1	0	1
1	0	1	1	0
1	1	1	$\overline{Q^n}$	*

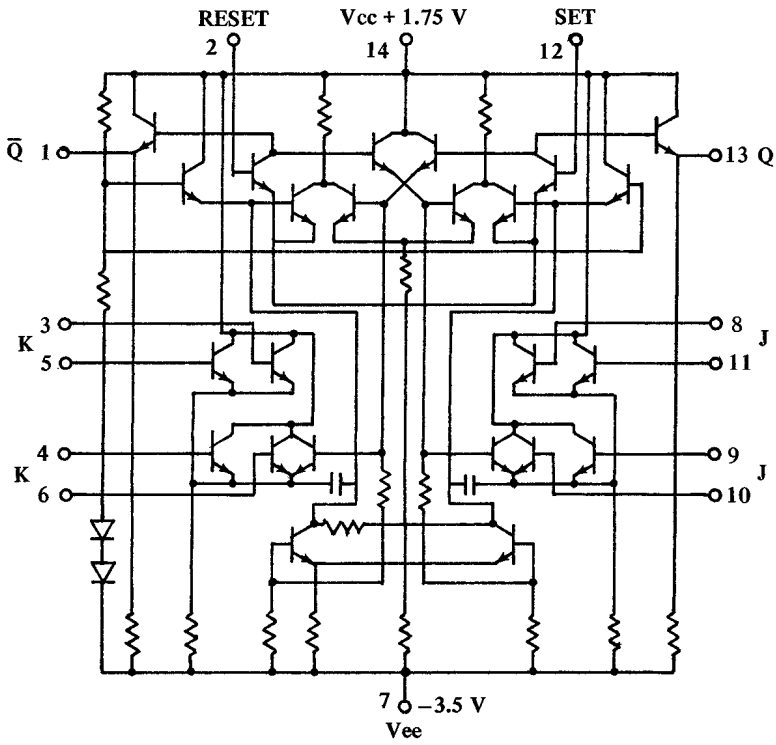
*Q^n = No output changes

$\overline{Q^n}$ = Complement

Data furnished courtesy of Fairchild Camera and Instrument Corporation

Fig. 3-7. Integrated circuit details. Negative logic symbols.

MC1013P AC COUPLED J–K FLIP-FLOP CIRCUIT SCHEMATIC



S = SET
R = RESET

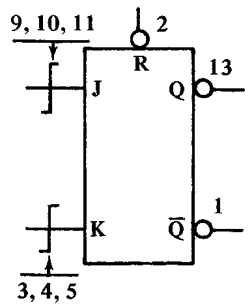
S	R	Q	$\overline{Q}$
0	0	NOT PERMITTED	
0	1	1	0
1	0	0	1
1	1	NO CHANGE	

DC

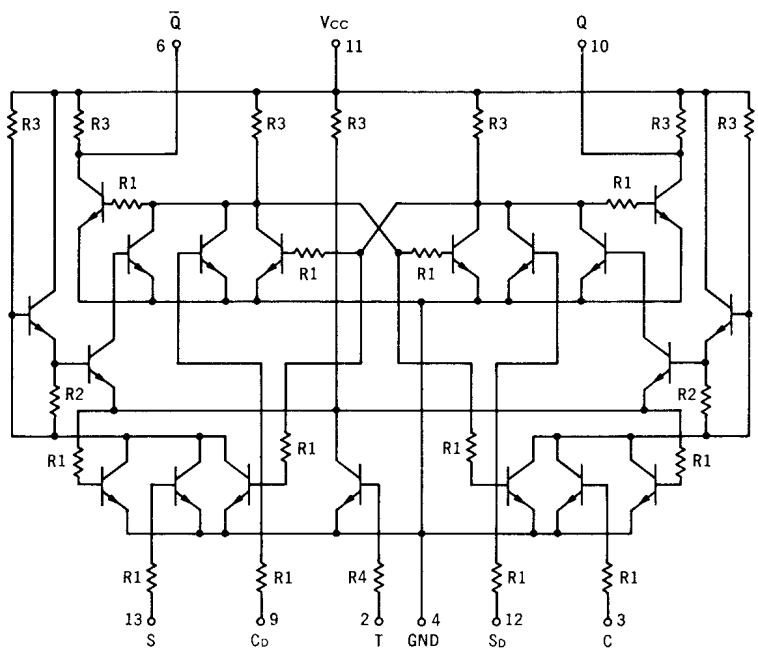
OVERRIDES

+ EDGE

J	K	Q	$\overline{Q}$
0	0	NO CHANGE	
0	1	0	1
1	0	1	0
1	1	COMPLEMENT	



MC 822P – J-K FLIP-FLOP



TYPICAL RESISTANCE VALUES
R1 = 1.5 k R3 = 3.6 k
R2 = 2.0 k R4 = 750 Ω

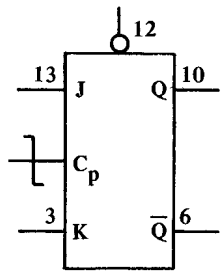
S	R	Q	$\overline{Q}$
0	0	NOT PERMITTED	
0	1	1	0
1	0	0	1
1	1	NO CHANGE	

DC

OVERRIDES

+ EDGE (t^{n+1})

J	K	Q	$\overline{Q}$
0	0	NO CHANGE	
0	1	0	1
1	0	1	0
1	1	COMPLEMENT	



Circuits: Courtesy of Motorola Inc., Semiconductor Products Division.

Fig. 3-8. Integrated circuit details. Negative logic symbols.

the minus position the high frequency component of the signal goes through transformer T10, which inverts the signal before going to P10. The low frequency portion of the signal goes to Q20 base.

A short summary of the Trigger circuit operation follows. It is assumed that the SENSITIVITY control is adjusted for a properly triggered display (RECOVERY TIME control not at its SYNC position). A trigger signal is received by the Isolation Amplifier Q20; its output switches tunnel diode D28 to its high voltage state, which drives D106 and about 5 ns later, D114 (D114 is driven through a delay line with approximately 5 ns signal delay). The resulting output pulse from D114 sends a signal to D168 and to Q120.

Initial conditions before the trigger sequence can occur require that Q75 and Q72 be conducting. Q75 collector is at approximately +20 V. R100-R102 sets approximately 5.5 mA of bias to D106 (a 10 milliampere tunnel diode). D114 (also a 10 mA TD) is biased through R112-R113 at about the same current. R115 raises D114 slightly positive with respect to D106 voltage; therefore, D112 is reverse biased (cut off) and D110 conducts all of R110 current (3 mA) to D106.

An active cycle begins when Q20 conducts a trigger signal that switches D28 to its high voltage state. A positive pulse is conducted through C58 to trigger D106 to its high state (almost instantly) and thereby reverse bias D110. The 3 mA from R110 is now conducted by D112 to arm D114, so it will switch to its high state when D28 delayed pulse arrives through C50 and the 5 ns Delay Line. As D114 switches high, three events occur: 1) D114 sends a pulse through C118-R118 to D168. (The pulse may or may not be used by D168, depending upon whether D168 is armed from the Digital Comparators through R168). 2) D112 is reverse biased and D110 conducts the 3 mA from R110. D106 is then held at its high state to lock out any more triggers, and D114 remains in its high state until Q75 is turned off at the end of the sample cycle. 3) The Clock Start Delay circuit delays D114 signal from starting the Clock for exactly 50 ns. The next trigger cannot be recognized until the full sampling cycle is complete, and D106 and D114 are reset to their low voltage states by Q72 and Q75 at the end of the Timing Ramp running period (see Block Diagram description).

As the 10 MHz Clock is started by the Clock Start Delay circuit, Q135 is caused to conduct enough Q20 current so that D28 is prevented from responding to any more trigger pulses from Q20.

The Reset Cycle starts after the Timing Ramp has run and been stopped by its Reset Comparator (D538-Q548, as described later in the description of diagram 5), and a negative current pulse is delivered to Q70 base to turn it on. Current from Q70 reverse biases Q75, which then turns off the Reset Multivibrator Q72-Q75, starting the trigger circuit Reset Ramp running.

When the Reset Multivibrator is off, Q90 collector rises to about +1 V from its previous on value of 0 V. Q90 resets the 100/1 Divider, the Clock Counter and Digital Comparators, and the Real Time 1, 2, 5 Divider. D90 clamps Q90 base from going more than −0.6 V negative during its time of non-conduction.

The Reset Multivibrator remains off for the Reset Ramp period, which is determined by one of several capacitors switched into the circuit by saturating transistor switches Q80, Q82, Q84 or Q86. The bases of these switches are controlled from the Type 3T5 Central Timing Logic, which selects the proper reset time for each sweep rate. If 10 μs/div is being used, terminal AQ is at a high level (logical ZERO) and Q84 connects C84 to ground. Note that C74 is in parallel with C84. While the Reset Multivibrator is on, the capacitors are charged to approximately +20 V. When Q72 turns off, the capacitors discharge through R76-R78 to a level of approximately −3.5 V. The time constant is controlled by the RECOVERY TIME control R78. Q72 base is at approximately −3.5 V and the transistor becomes forward biased when the capacitor discharges to a more negative value. When this happens, Q72 turns on Q75 and conducts current to the following four places: 1) C106 via D102. 2) Q90, which turns on. 3) R162 which provides bias to the Timing Ramp Enable TD D168 to help arm it, and 4) To the junction of R112-R110, to rearm D114.

Reset ends when Q75 turns on. Current through D102 causes its junction voltage drop to cut off Q100. As C106 charges through R100-R102-D102, R106 introduces current to D106 slowly to assure that D114 is armed before D106 is armed. When Q75 turns off, D102 no longer reverse biases Q100, which turns on and discharges C106 to −3.5 Volts.

The Trigger SENSITIVITY control circuit includes Q35, which is turned on to saturation for both INT and EXT trigger operation. Q35 conduction forms a monostable multivibrator of D28-L47-L34-R34 and Q35 (Q40 is at cutoff). D28 will step to its high voltage state if it is properly biased and if Q135 is turned off, allowing trigger signals from Q20 to reach D28. D28 bias adjustment control is R30, the SENSITIVITY control; R36 sets the range of control of R30. When D28 switches up, its pulse duration is determined by L34-L47 and the saturation resistance of Q35, as modified by the TRIG SENS ZERO control, R36.

High frequency synchronized operation is possible when the RECOVERY TIME control is placed in its SYNC position. The bias voltage supplied by the SENSITIVITY control is now made more positive to cause the multivibrator to free run. The repetition rate can be altered somewhat by R30, so that D28 can synchronize with Q20 output signal and thereby present a stabilized, synchronized CRT display.

Automatic triggering is obtained when Q40 is turned on and Q35 is turned off by the trigger MODE switch when set

to the EXT AUTO position. A bistable multivibrator is formed by D28-L47 and R44. D28 trigger level bias is adjusted during calibration by R32, the AUTO LEVEL control. When a trigger signal of sufficient amplitude arrives from Q20, D28 switches to its high state and remains there until the trigger signal is removed.

Special Trigger Circuit components include R46-R47 and D46 which provide first order temperature compensation for D28. C12-C13-R13 form an all-pass termination to make the trigger circuit input appear as 50 Ω at all frequencies. R23-R24-R26 set Q20 emitter at 0 V for proper external DC triggered operation. D24 temperature compensates the emitter-base junction of Q20. C26 provides a high frequency AC ground for Q20 base. C21-R21 provide frequency compensation to Q20 emitter-base junction, so it always appears resistive to incoming signals. R20 sets the no-signal current of Q20.

Clock Circuit

Initial conditions of the clock circuit (when the Trigger Circuit is armed, ready to be triggered) are such that it is not running. The Clock Start Delay circuit holds the Clock Oscillator Clamp in a condition that prevents the 10 MHz Clock from running. In the Clock Start Delay circuit, D114 holds Q120 in non-conduction, and the voltage divider R121-R122-R124-D124 and R125 holds Q125 in non-conduction. Q130 is off, Q135 is off and Q140-Q145 hold the clock from running.

An operating cycle begins when a trigger signal is recognized by D28 and the output tunnel diode D114 switches to its high state. Then, two things occur: first, C118-R118 conducts a pulse to D168 which, if armed by the Digital Comparator, will switch to its high state and start the cycle for one sample; second, Q120 of the Clock Start Delay circuit (which includes Q125) conducts the current from R122 previously taken by R124, turning on Q125.

When Q120 conducts, D124 is cut off and C124 discharges through R125. Q125 conducts after C124 discharges below −0.6 V and turns on Q130, 50 ns after D114 has switched to its high state.

Before Q130 turns on, L145 conducts some current from Q140 15 mA current and Q150A gate is at approximately ground potential. The inductor current provides magnetic field energy which controls the self-inductance starting characteristics of the Clock when it turns on. The Clock starts when Q130 turns on, and reverse biases D136 and Q145 by −12 V. As Q130 saturates, its collector takes all Q140 current and its −12.2 volts reverse biases D136 and Q145, allowing the self-inductance of L145 to start the clock cycle at the correct amplitude and frequency. Q150A gate voltage starts negative (as L145 maintains the electron flow in the same direction as controlled by Q140) and the Clock starts (described in more detail below).

When Q130 turns on, Q135 is also turned on. Q135 conducts part of the bias current of D28, thereby preventing further trigger pulses from D28.

The Clock is composed of Q150A-Q150B-Q155 and the tank circuit L145-C145-C146. When D136 and Q145 are cut off, L145 magnetic field collapses and charges C145-C146, with C145 and Q150A gate voltage going negative for the first half cycle. Source follower Q150A drives emitter follower Q155. R158 feeds back sufficient energy to maintain self-oscillation. (Incorrect adjustment of R158 will cause the oscillations to increase or decrease in amplitude. D145 and D146 limit the feedback amplitude so the useful adjustment range of R158 is increased.) Q150B is a constant current drain for Q150A. D155 sets the bias for Q150A and B, and temperature-compensates Q155.

The Clock output is at 0 V before the Clock starts. The clock load is Q160 and Q170 emitters through D160 and D171. (D160 and D171 are hot carrier diodes which conduct with about 0.3 V forward voltage drop, whereas Q160 and Q170 have 0.6 V forward voltage drop across their emitter-base junctions before they conduct.) The oscillator output voltage goes negative when the Clock starts. This turns off D171, which has been conducting current from R160-D160 to R172. R172 now conducts current from Q170 emitter, changing Q170 collector voltage from approximately +1 V to 0 V. D160 remains on until the Clock sine wave rises above ground, at which time it turns off and D171 conducts. Q170 collector then rises back to approximately +1 V. As the sine wave goes positive, D160 turns off and Q160 conducts the current of R160. This provides a Clock current pulse into D168 (100 ns after D114 pulses the Clock Start Delay circuit) which lasts until the Clock sine wave amplitude falls below ground.

The Timing Ramp Enable TD, D168 must have three signals coincident at its anode before it will switch positive. The three signals are (with approximate values): 6 mA bias from the Reset Multi through R162-R163, 3 mA arming signal from the Digital Comparator through R168, and 2.6 mA Clock pulse from Q160 through R165 or from D114 through C118-R118. If the arming signal through R168 is absent D168 will receive clock pulses, but will not switch high. When D168 switches, its anode voltage goes positive, generating the Timing Ramp Enable signal that starts the Timing Ramp (diagram 4). D168 remains in its high state until the Reset Multivibrator switches and removes bias current, at which time D168 switches back to its low voltage state.

The operation of U170A and U170B, U180A and U60A is discussed in the Block Diagram description earlier in this section. R164 guarantees D168 will switch to its low state when the bias from the Reset Multi is removed. R175-R178 sets Q170 output to +1 V for the high logic level.

Delay Gating and Digital To Analog Converter 2

The Delay Gating circuit accepts binary information supplied by four decades of binary coded decimal (BCD), to program the CRT display time window Delay. The two most significant decades are fed directly to the Digital Com-

parators (diagram 3). The two least significant decades are fed directly to the Digital To Analog Converter circuit. The 3rd decade (X100) does feed the Digital To Analog Converter when the TIME/DIV DECADE switch is at 0 (10). The Digital To Analog Converter drives the Staircase Inverter (diagram 5), whose output drives the Slewing Comparator for proper generation of ΔT_{dot} in equivalent time sampling. Output of the Digital To Analog Converter is a DC voltage, used to offset the Staircase Inverter output for time window delay as described in the block diagram description earlier in this section.

Each of the four DELAY switch decades provides four output lines, internally converting the dial decimal number to a BCD number. The output lines connect to the Delay Gating networks through program isolation diodes. The isolation diodes assure there will be no electrical confusion between internal and external programming of the time window delay. The Delay Gating networks convert the input negative logic voltage limits of 0 V to +2 V for a logical ONE, and +6 V to +15 V for a logical ZERO, to narrower circuit related limits.

Following each input isolation diode is a resistor network which standardizes the internal logic voltages to approximately 0 V (or a negative value) for a logical ONE and approximately +1 V or more positive for a logical ZERO. The X100 and X1000 decades have an in-circuit logical ZERO that does not exceed +1.2 V due to the clamping action of diodes D899A through D899I.

The X100 and X1000 decades program the Digital Comparator. The X1, X10 and sometimes the X100 decades program an analog current developed by the operational amplifier Q360-Q370-Q375 to supply the Staircase Inverter Amplifier with a staircase offset current.

The Digital To Analog Converter is an operational amplifier (Q360-Q370-Q375) with FET Q360 the input transistor. Though the input signal to the amplifier summing point (Q360 gate lead) is a current signal, there is a signal voltage at the summing point equal to the amplifier output voltage divided by the open loop gain of the amplifier. A positive signal to Q360A gate makes its source voltage go positive, which decreases the current in Q360B so its drain voltage goes positive. Q360B forward biases Q370 and its collector voltage goes negative. Q375 is an emitter follower, and its emitter voltage also goes negative. R360 feeds back the negative output voltage signal as a current to Q360A gate summing point so that R360 current and the input programming current are equal.

The operational amplifier zero signal DC input is +0.6 V as set by D364 at Q360B gate. This voltage sets the quiescent anode voltage of all the input isolating diodes connected to the common input line (gate of Q360A). The current in the common line is determined by precision resistors that are diode connected by the Delay Gating program. In the X1 decade, the current through D358, D348, D338 or D328 is inversely proportional to the associated series resistor. The values of the series resistors are a binary ratio. The resistors are returned to −10 V which is supplied by the voltage divider R327-R329.

The X10 decade is identical to the X1 decade, except that the four series resistors are connected to −100 V instead of −10 V. The current in each case is increased over the X1 decade by a factor of 10. The X100 decade resistors are one-tenth the value of their counterparts in the X10 decade and the current in each case is increased over the X10 decade by a factor of ten.

Placing a logical ZERO at the Delay X10 decade 4 line (not grounded by either the DELAY switch or external program) causes the voltage divider R292-R294-R296 to place +1 V at D296 anode. D296 cathode is at about +0.4 V due to current in R298. Since the operational amplifier input holds D298 anode at +0.6 V, the 0.2 V forward bias prevents D298 from conducting. Thus R298 current does not affect the amplifier.

Placing a logical ONE at the Delay X10 decade 4 line places D296 anode at about −1 V. The diode is reverse biased and does not conduct. D298 now conducts, placing R298 as an input resistor to the amplifier. R298 current of 0.05 mA is provided by feedback current through R360, causing the amplifier output voltage to change +3 V from its previous value.

When no time-window delay is wanted, there is no input to the operational amplifier and the output voltage at D375 cathode is 0 V. When time-window delay is wanted on sweep rates that include the TIME/DIV DECADE switch positions of 4 through 9, the operational amplifier maximum output voltage is +7.5 V. Those sweep rates use the Delay X100 decade lines in the clocked form of delay only (described with the block diagram). When the TIME/DIV DECADE switch is at 0 (10), then the Delay X100 decade lines are included in the analog form of delay and the operational amplifier maximum output voltage is +75 V. The X100 decade lines are included in the analog delay by the Central Timing Logic placing a logical ONE at pin J (diagrammed connected to the anodes of D247-D257-D267-D277). The line feeding pin J is named "IV' Fine Delay Comp", meaning that there is a compensation of Delay switching for the three fastest sweep rates. The least significant Delay switch now provides 100 ps of delay per step, which amounts to 1 major graticule division at the fastest sweep rate of 100 ps/div.

NOTE

Referring to the Equivalent Time Block Diagram, at the same time the Central Timing Logic makes the IV' line a logical ONE, it makes the γ Ist Decade Enable line a logical ZERO to turn off the Clock Counter 1st decade. With the 1st decade off, the Delay X100 lines have no effect upon the clock form of delay. Then the Delay X1000 lines operate the Digital Comparator 2nd decade as if it were a 1st decade, and the total delay operation now uses the most signifi-

cant Delay decade in the clock form of delay and the three least significant Delay decades in the analog form of delay.

The Fine Delay Attenuator converts the voltage at the Analog to Digital Converter output (at D375 cathode) to a current at the summing input to the Staircase Inverter Amplifier (diagram 5). This signal offsets the Staircase Inverter output signal into the Slewing Comparator to delay the time window display away from T_o.

The output current (staircase offset current) magnitude is altered by switching FET's which are programmed by the Central Timing Logic to select one of three values of output resistance. Maximum current output occurs when Q395 conducts. (Its on resistance is less than 30 Ω.) This places R394 in parallel with R377-R378. A current one-tenth of this value is obtained when Q385 conducts. R384 is then in parallel with R377-R378. With both Q395 and Q385 off, the current is reduced to one-hundredth of the maximum value. If Q398 is on (saturated), the output current is one-thousandth of the maximum value since it bypasses about 90% of the current to ground through R398.

Q380 and Q390 serve as signal level converters. Their gain is sufficient to reduce the gate voltages of Q395 and Q385 from −12.2 V to 0 V when +1 V is applied to their emitters. The input signals come from the TIMING LOGIC to these transistors and Q398. When conducting, voltage drops across D382 and D392 reduce the gate voltages to 0 Volt.

Timing Ramp & Staircase Inv Amp. ⑤

The Timing Ramp circuit generates six timing ramps which, together with the staircase signal fed to the Slewing Comparator, provides strobe drive pulses for the vertical channel sampling unit and stepping pulses for the Type 3T6 Staircase Generator.

A separate capacitor is used for each timing ramp. C538-C539 provide the fastest ramp and C503 through C516 provide successively slower rate ramps. The Timing Ramp capacitors are switched in by their respective constant current transistor switches, Q500 through Q516. Each transistor emitter is connected to the common timing current setting resistors R518-R519 and the −100 V supply. Only one switch is on at a time, but C538-C539 are always in the circuit. Timing current is adjusted by R518 and timing accuracy between ranges is assured by the accuracy (error ratios) of timing capacitors C503 through C516.

To obtain a 100 ns/div timing ramp (1 μs ramp), input terminal S is held up at approximately +1 V and Q503 base is at +0.9 V due to the two junction voltage drops of D502 and D514. Q503 conducts, setting its emitter and all of the other common emitters at +0.3 V. The other switches are open because they are reverse biased with their bases at 0 V. D503 through D516 isolate the unused timing capacitors from the one in use. Auto calibration may be provided at terminal K by use of special equipment admitting an increase or decrease to the timing current value set by R518.

Q525-Q530-Q535 form the Ramp Clamp. Q525 and Q530 conduct when the anode of D520 is at 0 V. Q530 collector signal turns on Q535. Q535 collector voltage clamps at approximately +18 V due to feedback to Q530 emitter through D528. The output is then limited to +18 V because R530 and R531 set Q530 base voltage to +18 V. A +0.5 V pulse to D520 from the Timing Ramp Enable diode D168 in the Clock circuit turns off Q525 and stops the current in Q530. R532-D534 set Q535 base voltage 0.6 V above +20 V, turning Q535 off. This allows the timing ramp to begin its rundown from a starting value of +18 V. At the end of a sampling cycle, the anode of D520 is returned to 0 V. Q525 again conducts and Q530 collector voltage drop turns Q535 on to reset the timing ramp voltage back to +18 V.

C525 is a speed-up capacitor that helps start (unclamp) the ramp quickly when D520 gets a positive pulse from the trigger circuit. R501 provides for the I_{CBO} leakage of the Timing Ramp transistors that are cut off.

The Slewing Comparator Q550-Q555 and its constant current drain Q553, compares the Timing Ramp voltage with the Staircase Inverter Amplifier output voltage which is applied to Q555 base. Q555 is normally at cutoff forcing all of Q553 current into Q550. When the voltage at Q550 base becomes less than Q555 base voltage, Q550 turns off. Q555 now conducts all of Q553 current and the negative voltage step at its collector causes Q565 to avalanche. A 20 V positive pulse is produced at Q565 collector and this signal couples through C566 to become the vertical channel sampling unit strobe drive. C567-R567 supplies a similar signal to the Staircase Stepper.

Q548-D538 form the Timing Ramp Reset Comparator. On all ramps except the 100 ns ramp, the Timing Ramp runs negative from about +18 V to about +8 V and stops. It is stopped by current in D538 and Q548. Before the ramp is stopped, Q548 is conducting only about 1/2 mA and its base voltage is set to about +9 V by R547-R549 and the +20-V supply. As the Timing Ramp voltage reaches a value that is about two silicon junction drops (1.2 V) below Q548 base, D538 conducts, causing Q548 to take all the timing current away from the timing capacitor. As the timing current enters Q548, its collector provides a negative step signal to Q70 in the trigger circuit Reset Multivibrator. This initiates reset of both the trigger circuit and the Timing Ramp by returning D520 anode to 0 V.

For the 100 ns ramp only, terminal AD voltage is up, turning Q545 on to saturation. This places R546 in parallel with R549 so that the voltage divider output to Q548 base changes from about +9 V to about +2.5 V. This permits the 100 ns Timing Ramp to run to about +1.5 V before the loading comparison occurs and both the trigger and ramp circuits are reset.

During Equivalent Time operation, the input signal to

terminal AV is inhibited by D540 (a germanium diode) whose cathode is at 0 V. During Real Time operation, approximately +1 V is applied to terminal AT and Q540 conducts when a positive signal arrives at terminal AV as the Staircase Generator resets at the sweep end. The voltage at Q70 is lowered and the trigger and timing ramp are reset in the same way as when Q548 turned on.

The method of providing strobe drives in real time is provided by Q560, which is driven from the Clock at a proper rate. For each positive pulse at terminal X, one strobe pulse is produced.

The Staircase Inverter operational amplifier Q590-Q578 gives an inverted output signal at the collector of Q578 for an input signal to Q590A gate. The input signal is composed of a fine delay current from the Digital to Analog converter, the 0 to +7.5 V Staircase signal (converted to a signal current by one or more of the input resistors) and the Delay Zero current, which is adjusted by R591. The output signal is fed directly to the Slewing Comparator at Q555 base and is used to control the equivalent time duration of ΔT_{dot} described near the beginning of this section. Logic control of the staircase signal output amplitude comes from the Central Timing Logic of diagram 7. Input resistors are switched in or out of the circuit (to change the gain) by switching FET's, Q581, Q584 and Q587.

The amplifier input resistance consists of R589 in combination with R582, R585 or R588. When the switching FET Q587 is turned on, R588 is connected in parallel with R589 and the resulting amplifier gain is unity. In like manner, Q584 connects R585 in parallel with R589 for a gain of one-half and Q581-R582 gives a gain of one-fifth. With the three switches open, the input resistance is R589 and the gain is one-tenth.

Each FET switch is turned off with a reverse bias of −12.2 V and is turned on with 0 V gate bias. An input voltage at terminal BT of approximately +1 V turns on Q586 to take all of R587 current which zero biases the FET switch Q587. The slightly positive voltage at Q586 collector is reduced to 0 V for Q587 gate by the D587 junction voltage drop. The remaining FET switches are controlled in the same way at terminals BS and BR and Q583-D584 and Q580-D581.

Terminal BQ receives a voltage of approximately +1 V when the three fastest sweep rates are programmed. Q570, with D571 turn on Q572 and Q575. Q575 places R576 in parallel with feedback resistor R578 to reduce the operational amplifier gain by a factor of 10. Connecting R576 in the circuit causes an unwanted output DC shift that is cancelled by Q572 and R573-R574. The 0 Decade Delay Zero control adjusts the amplifier output to the proper level. Zener diode D573 conducts when Q572 is turned off, otherwise the emitter would follow the base voltage down to −12.2 V and the transistor would not stop conducting. D596 acts as a clamp to prevent base-emitter breakdown of Q578 if Q590 is removed from its socket while the power is on. R579-C579 form an oscillation damping circuit.

Staircase Generator And Horiz Amp ⑥

The Staircase Generator is composed of a Staircase Amplifier Q680, Q685, Q690 and Q695, Staircase Reset Multivibrator Q610, Q630, and Q635, Staircase Stepper Q670 and Q675, Sweep Speed-up Enable Q660, Q840 and Q845 and Sweep Reset Tripper Q600. The output of the Staircase Generator drives the Horizontal Amplifier, the Digital Unit and the Staircase Inverter Amplifier.

The Staircase Generator is an operational amplifier used as a Miller integrator with input at Q680A gate and output at D690 cathode. A negative current pulse to Q680A gate starts to drive Q685 base negative and its output drives emitter follower Q690 positive. C680 feeds back an inverted current pulse to the input of the amplifier. D684 sets the bias and current for both Q680A and B so that Q680A source lead slightly forward biases Q685 when Q680A gate is at 0 V. D690 assures that the collector voltage of Q685 will be at about +1.2 V when the output is at 0 V (thus Q685 does not saturate). Q695 is a constant-current emitter return for Q690 to assure a constant voltage drop across D690 and assure good amplifier linearity. D693 conducts negative signals to the output when Q690 is cut off. This happens when the Staircase is being reduced from +52 V back to 0 V.

The staircase output voltage is changed (made to take a positive step) by input pulses of charge (current X time) from the Staircase Stepper during the 1000 dots/sweep rate. Q690 output current gives C680 a fixed amount of charge (which it retains) each time a pulse from the Staircase Stepper drives Q680A input negative. Hence a staircase of increasing voltage vs time is formed. The staircase is stopped at about +52 V and returned to 0 V. The Reset Multivibrator must turn on again before another staircase can be generated.

During staircase run-up, Q630 and Q635 of the Reset Multivibrator are saturated. To begin the staircase, a positive pulse to terminal BK from the Strobe Driver (Q565 diagram 5) turns on Q670 of the Staircase Stepper, which gives a negative pulse to Q630 base through R605 to turn it on. Q630 drives Q635 into conduction and its collector drops to −12 V. R634 conducts this signal back to Q630 and both transistors are locked on. D680 and D682A are reverse biased and do not conduct.

Q610 base is biased two junction voltage drops below approximately +52 V (which is the top of the staircase). When the staircase exceeds +52 V, D614 conducts a pulse through Q610 to Q630 and turns it off. (R604 is the major current drain, though not the only one, for the several currents that enter the summing point, which is the base of Q630. Only the controlling currents will be mentioned.) Q635 is then reverse biased and its collector goes positive. Q630 is now held off by the positive bias through R634 as clamped by D634, and D682A is biased into conduction.

The positive signal voltage through D682A to Q680A gate results in an amplified negative change to the Staircase Amplifier output, which causes the output voltage to drop to 0 V, at which point, D680 conducts. During this time C625 (which was charged to +52 V) has been discharging through R624-R604, and the cycle begins again when a negative pulse from Q670 through R605 is greater than the diminishing current from R624-C625, turning on Q630.

Q670 and Q675 form the Staircase Stepper. Initial conditions (before each step drive pulse) are: Q670 collector is at +20.6 V, clamped there by D671 and reverse biasing D672. Q675 is conducting about 1.6 mA from +20 V through R672-D678-D668 and D667; Q675 base is at about +4.4 volts as set during calibration by R676 (Samples/Sweep Cal control) and the voltage divider resistors R674-R675; C672 is charged to about +5 volts. The two silicon diode junction drops of +1.2 V across D667-D668 assure that D682B (at the Staircase Amplifier input) is reverse biased and the Staircase Stepper is disconnected from Q680A gate.

A cycle of operation starts when the step drive pulse arrives at Q670 base from the Strobe Driver. Q670 saturates for a very short time, (less than the input pulse duration) and its collector drops to about 0 V. Q670 saturation is intended to, and does, discharge C672 down to about +0.6 V due to the drop across D672. Q670 also takes all the current of R672, placing Q675 at cutoff. D678 disconnects Q675 collector, allowing R668 to forward bias D682B and become the input resistor to the Staircase Generator operational amplifier. (D668 is reverse biased when Q660 is at normal conduction for 1000 samples/sweep. However, should 100 samples/sweep be programmed, D668 remains forward biased and R667 is placed in parallel with R668 as the input to the operational amplifier. See 100 samples/sweep described below.) As long as R668 remains connected to the Staircase Generator (Q680A gate) the output voltage changes in a positive direction. The duration of input current from R668 is very short, controlled by the saturation time of Q670 and the RC charge time of R672-C672. As C672 charges positive, Q675 is caused to conduct again and disconnect R668 from the operational amplifier input, thereby stopping the output voltage change. Each staircase step (output voltage) is the same amplitude because R668 remains as the input resistor for the same amount of time each step. During the time R668 is not the input resistor, D682B remains cut off and the Staircase Amplifier output voltage remains stable. C678 assures that all the charge that should reach the amplifier input does. As R668 is connected, it conducts current out of the amplifier input faster than the amplifier output can follow (and by following, provide an equal current through C680). Therefore, C678 is a temporary current source for R668. Any charge gained by C678 is removed by feedback current through C680 at the end of the stepping time after R668 current has been removed from the amplifier input. R682 develops a small negative feedback signal due to C680 current into C678, helping to prevent overshoot of the operational amplifier output step and "smooth out" the input current pulses from the Staircase Stepper circuit at Q680A gate lead.

Q670 collector also provides drive to the Digital Clock amplifier Q605. Q605 is normally not conducting, its base reverse biased about 0.6 volt by Q670 collector voltage, clamped at +20.6 V by D671. As Q670 saturates, do does Q605, sending a +1.8 V square clock pulse to an associated digital unit.

When 100 samples/sweep is programmed (available by external programming only), additional step current is drawn from the Staircase Generator operational amplifier input by R667 placed in parallel with R668 to make each staircase voltage step 10 times larger than at 1000 samples/sweep. The sweep speed-up program (such as applying a logical ONE at J24 pin B) saturates Q845 to turn off Q660. Initial conditions (at equivalent time sweep rates) for 1000 samples/sweep are: Q840 base is at ground due to the logical ONE signal from the Central Timing Logic $\overline{RT}$ line. Q845 is at cutoff because both the base and emitter return resistors are connected to +3.6 V and the external programming line is at a logical ZERO. Q660 base is held at +3.34 volts by R660-R662; thus, R664 sets the collector current at 2 mA. Nearly I mA passes through R667, 0.134 mA passes through R666 and the rest of the 2 mA passes through D666 and D667. This condition assures that D668 is reverse biased during staircase step times and R667 is isolated from the staircase operational amplifier input.

As the external program applies a logical ONE to J24 pin B, Q845 emitter is taken sufficiently negative that R843 current to Q845 base saturates the transistor. Q845 collector now takes all of R664 current, cutting off Q660. R666 takes Q660 collector to −12.2 V, reverse biasing D666 and placing R667 in parallel with R668 for X10 staircase output voltage steps.

Any sweep can be reset at any time, independent of the staircase output voltage (either real time or equivalent time) by grounding J24 pin 15 (during external programming) or by placing the front panel SAMPLES/SWEEP switch to 1. Either mode of operation grounds pin BN, which turns on Sweep Reset Tripper Q600. Current from R603 turns off Reset Multivibrator Q630-Q635 as long as terminal BN is held down.

The Blanking Amplifier Q640 provides CRT blanking during the reset of the sweep. When the Reset Multivibrator turns off for reset, Q640 base is forward biased to turn it on. This lowers pin 13 of P21 to Zener diode D640 voltage of +43 V from the +125.6 V as set by D641 when Q640 is not conducting. The SAMPLES/SWEEP switch placed in the 1 position actuates the Sweep Reset Tripper, and also grounds out (through D644) any positive signal to Q640. This removes blanking so that the dot can be seen during reset. When 1 sample/sweep is externally programmed (sweep reset) the CRT dot is blanked.

Q650 provides a sweep gate to the Digital Unit when the sweep starts. Turning on Q635 puts a negative bias on Q650

base and it turns off. The voltage at the junction of R651 and R652 increases to +5 V and remains at that value until Q635 turns off at the end of the sweep.

Trigger circuit control for real time sweep rates is synchronized with each sweep by Q540 (included at top of both diagrams 5 and 6). (Q540 is held at cutoff by the $\overline{RT}$ line being a logical ONE for equivalent time sweep rates.) Real time sweep rates place the $\overline{RT}$ line to Q540 at a logical ZERO allowing the Reset Multivibrator to control Q540.

When the Reset Multivibrator turns off at the end of the staircase, Q635 collector goes positive. C626 conducts a positive pulse to Q540 to pulse it on. This produces a negative step to the base of Q70 to initiate trigger circuit reset time. R625 provides a trigger holdoff (only in real time) when terminal BN (drive to Q600 base) is in the reset mode. In equivalent time, terminal AT (the $\overline{RT}$ line) is near ground potential and D540 clamps the base of Q540 at approximately +0.3 V. Q540 then ignores any pulses through C626 or current through R625.

Horizontal Amplifier

The Staircase Amplifier drives an attenuation network R696-R697 which reduces the 0 V to +52 V Staircase to 0 V to +7.5 V. The voltage divider is isolated by emitter followers Q700 and Q705, which provide temperature and offset compensation.

Output Differential Amplifier. The linear output differential amplifier employs two special high voltage transistors Q720-Q730. These transistors have a BV_{CBO} rating of 300 volts, and are used to drive the CRT horizontal deflection plates directly. The emitter circuit is both "long tail" and highly degenerative between transistors, assuring that neither transistor cuts off.

Assume both amplifier bases are at +3.75 volts; R722 and R732 assure that both transistors conduct 2 mA. As Q720 base voltage goes positive, its emitter goes positive, applying a positive turn-off signal to Q730 emitter through R724-R734-R736. Q720 then increases its current, and Q730 decreases its current; Q720 collector goes negative and Q730 collector goes positive. The amplifier thus converts a single input signal to a push-pull output signal. The amount of signal coupled from one emitter to the other emitter is made adjustable by the front-panel HORIZ GAIN control, R736. R736 permits the operator to alter the output stage gain sufficiently to mate the horizontal deflection to the particular oscilloscope in which the Type 3T6 is operated.

The output average voltage value of both Q720 and Q730 is adjustable over a range by the front panel HORIZ POS control, R711. R711 sets the base voltage of emitter-follower Q710, which sets the base voltage of Q730. Total range of voltage at Q710 emitter is from about +1.1 V to +6.6 V, approximately 2 volts less than the total staircase signal amplitude into Q720 base. The differential connection of Q720-Q730 permits the HORIZ POS control to alter the staircase output voltages at Q720 and Q730 collectors without distorting the CRT display time linearity.

Spot Position Indicators

The horizontal spot position indicator lamps are driven by a switching comparator amplifier, Q740-Q745. The comparator is driven by the output amplifier emitter circuit by the voltage across the HORIZ GAIN control. If the CRT driver output amplifier transistor conduction differs enough to cause about 0.5 volt difference at Q740-Q745 bases, the most positive-base transistor saturates and the other transistor is cut off. The long tail resistance in the emitter of the lamp drivers permits the CRT driver emitter circuit to float between 0 V and +7.5 V and still operate the switching comparator properly. Whichever transistor saturates, it then turns on the associated neon lamp in its collector lead. The cutoff transistor assures that its collector circuit lamp has no current and therefore remains dark.

The two series base resistors R740-R746 assure that the pulse caused by neon ignition is not coupled back into the sampling sweep unit circuits. (Without the series base resistors, each time a neon turned on, its effects would be seen on the CRT.) The large resistance between transistor collector leads assures that the off transistor collector voltage does not rise to +125 volts. When a transistor is cut off, its collector voltage is held at about +70 volts by Townsend (dark) current through the associated neon passing through R472 to the other collector. R742 keeps the off transistor collector about +10 to +15 volts from its emitter (the emitter voltage being set by the other neon drop and its saturated transistor). The circuit never operates with both transistors cut off.

Power Supply ⟨11⟩

The low voltage power supply provides the operating power for the Type 3T6 from four regulated supplies to supplement the main frame power supplies. Electronic regulation provides stable low ripple output voltages.

The oscilloscope main frame provides 6.3 VAC to power transformer T901. The primary of the transformer is fused by F900, which is mounted on the rear panel.

The transistors are mounted on the Display circuit board except for Q915 and Q935, which are heat-sinked to the chassis near the rear of the unit.

The +20-Volt power supply is composed of differential amplifier Q900-Q905, an error signal amplifier Q910 and a series regulating element Q915.

Zener diode D903 biases Q900 base 9 V below the +20 V output. The bias for Q905 base is set by the voltage divider R907-R908-R909.

The regulator action is as follows: a fast changing output error voltage is fully applied to Q900 base through D903. C908 prevents fast error signals from reaching Q905 base.

Therefore, such errors are applied as an input to only one side of the differential comparator. Q900 emitter then drives Q905 emitter, and Q905 responds as a common base amplifier. Q905 collector voltage change is thus of the same polarity as the error signal that reached Q900 base.

C908 does not prevent very low rate-of-change error signals from reaching Q905 base as attenuated by R907-R908-R909. Thus the low frequency, or DC gain of the comparator is less than the high frequency gain.

Assume a positive error signal arrives at Q900 base. Q905 collector goes more positive and the current in Q910 is decreased. The base of Q915 is driven more negative due to the decrease in the current through R916. Q915 current is also decreased (its internal resistance is increased) increasing the voltage across the transistor. The voltage drop across the load is decreased due to the decrease in current and the normal load voltage is restored. The regulator action is similar for a negative error signal.

Special components serve the following functions: R904, R906, R912, R914 and C912 prevent parasitic oscillation. C908 stabilizes the base voltage of Q905 at high frequencies and C906 is a bypass which reduces the supply high frequency output impedance. R903 sets the Zener diode average current to the proper value. R901 will act as a slow-blowing fuse and protect the rectifier diodes and transformer secondary in the event of a short circuit at the supply output. R908 is adjusted during calibration to obtain the correct output voltage.

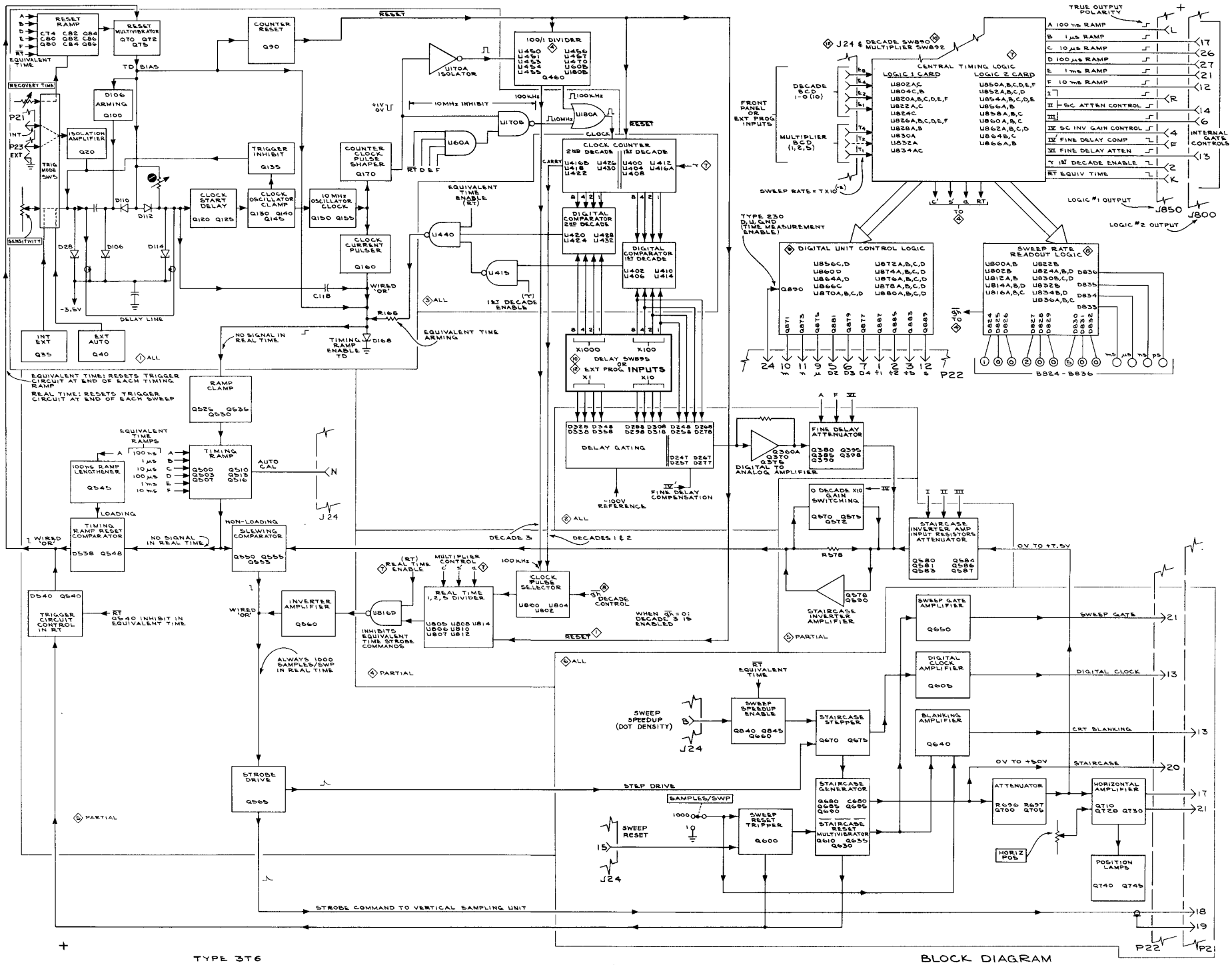
The +3.6-Volt power supply regulator action is similar to that in the +20-Volt supply. Q925 is reference biased for proper supply output voltage by the +20-Volt supply through the voltage divider R927-R928. Error signals are applied only to Q920 base through R921.

Special components include C928, R932 and R934, each of which aids in suppressing parasitic oscillations.

The +1.75-Volt supply uses the +3.6-Volt supply as its power source. The regulator action is similar to that in the +20-Volt supply. The reference bias and output voltage are set by R941 and the error signal is applied directly to Q945 base. The output voltage is purposely given a temperature controlled change by D940 and D942 to stabilize the operation of some of the integrated circuits in the Type 3T6.

The series element in the regulator that controls the current to the load is formed by R948 and Q948 in parallel with R949. Maximum resistance exists when Q948 is not conducting and only R949 conducts current. When Q948 is conducting, the resistance is less due to the parallel combination.

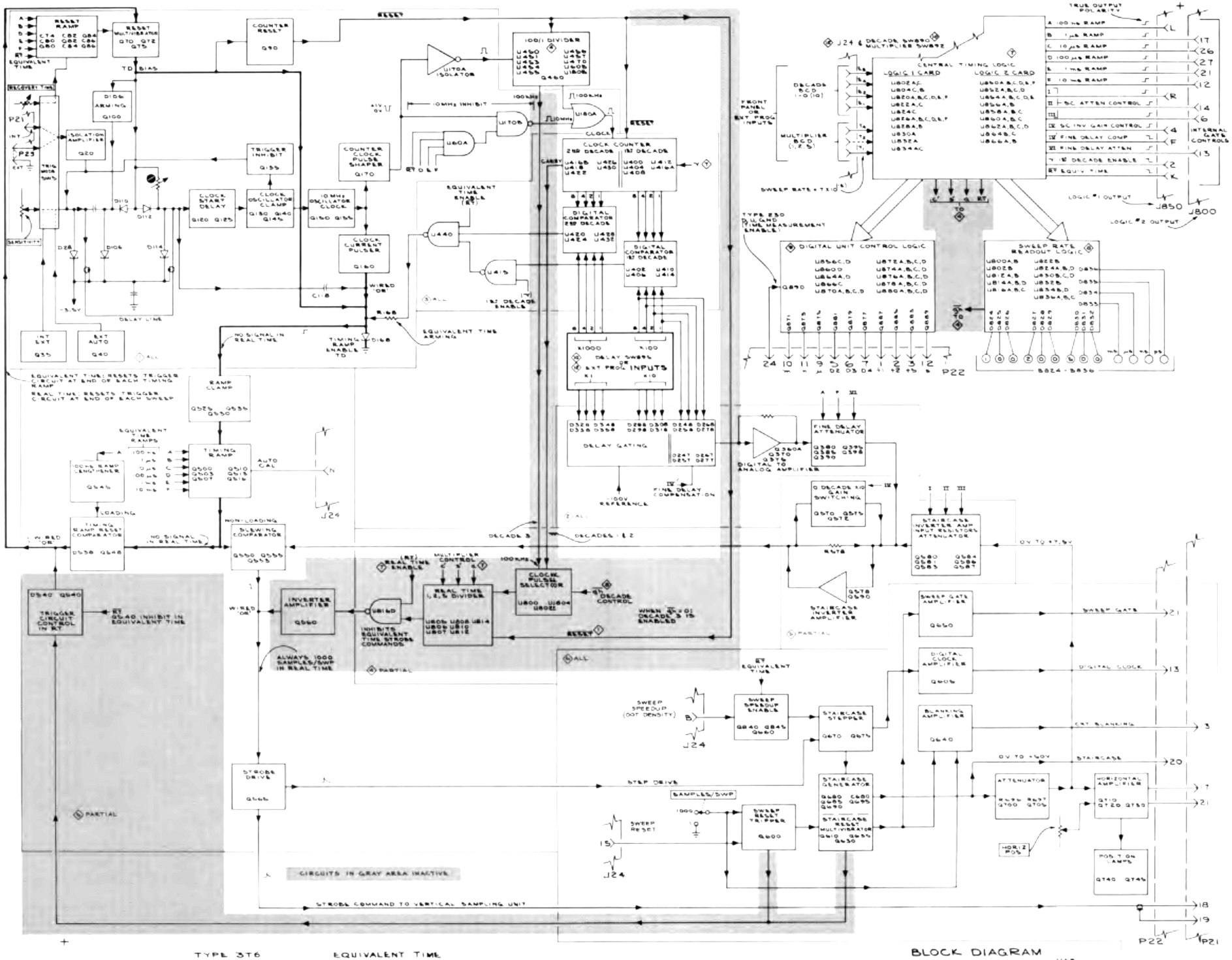
The −3.5-Volt supply uses the oscilloscope −12.2-Volt supply as its power source. The regulator action is similar to that in the +20-Volt supply. The oscilloscope −100-Volt supply reference biases Q950 through the voltage divider R951-R952 and also sets the output voltage. The error signal is applied to Q955 base. The series regulating element is formed by Q960-R966 in parallel with R956 and its action is similar to that in the +1.75-Volt supply.

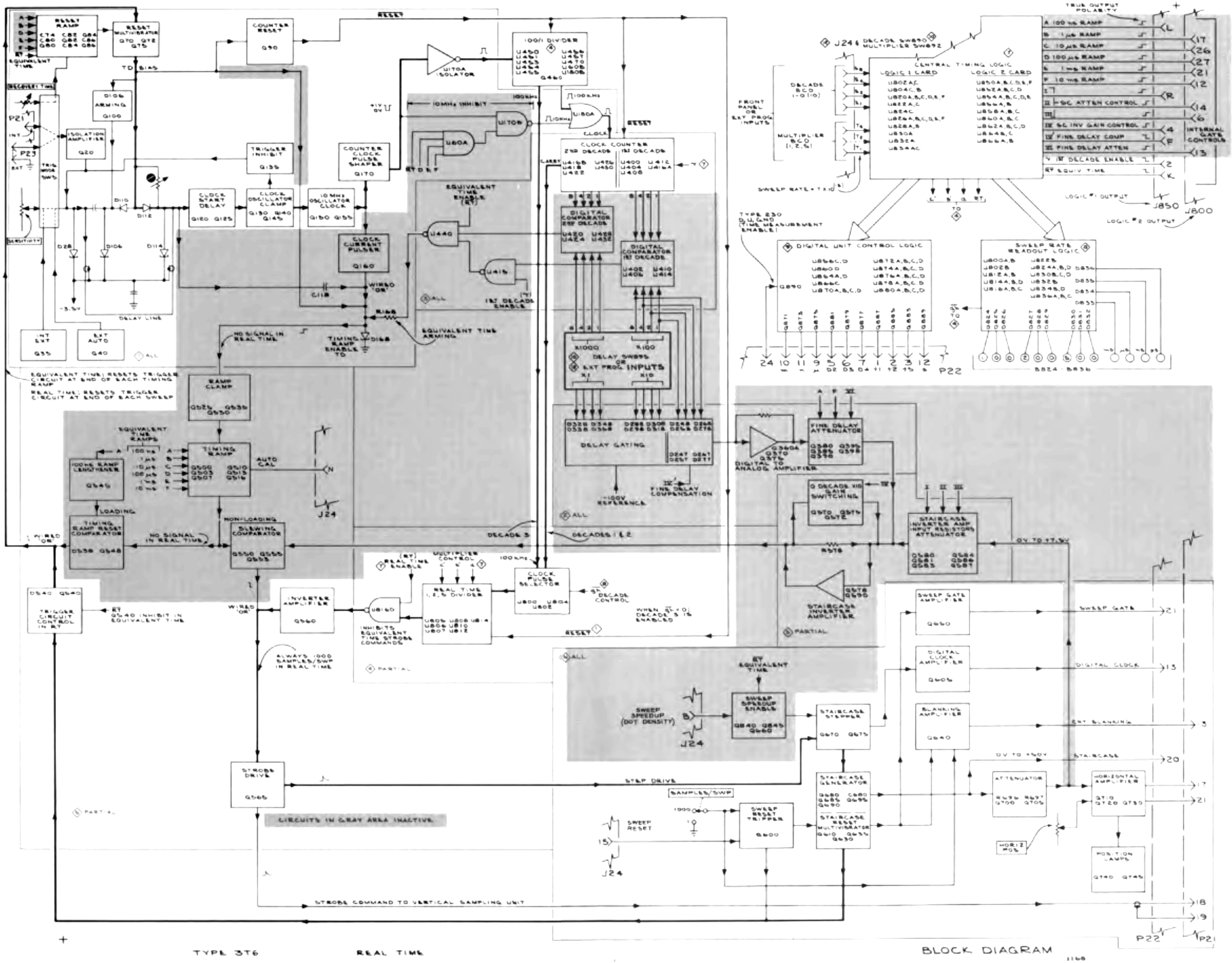


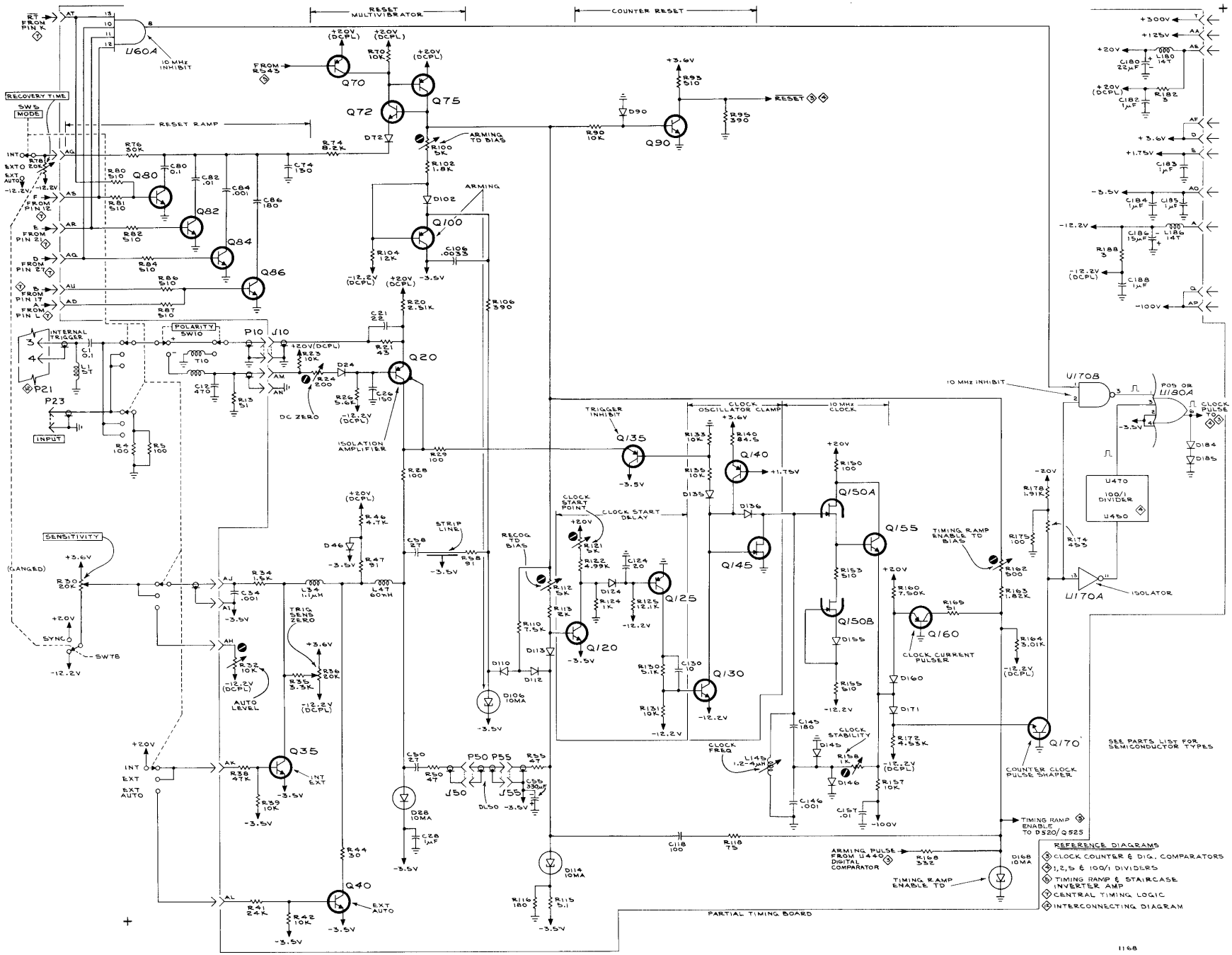
TYPE 3T6

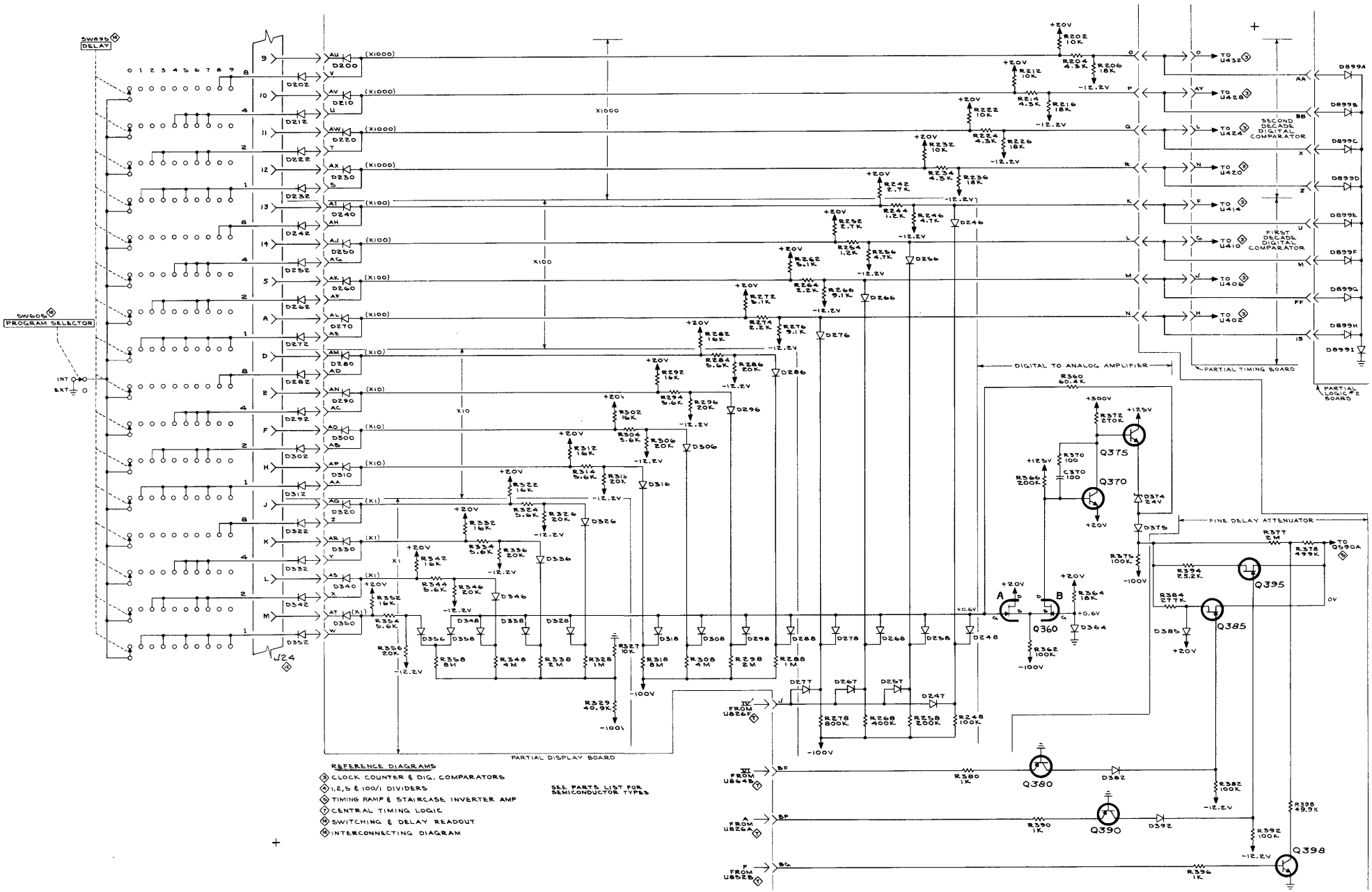
BLOCK DIAGRAM

1168

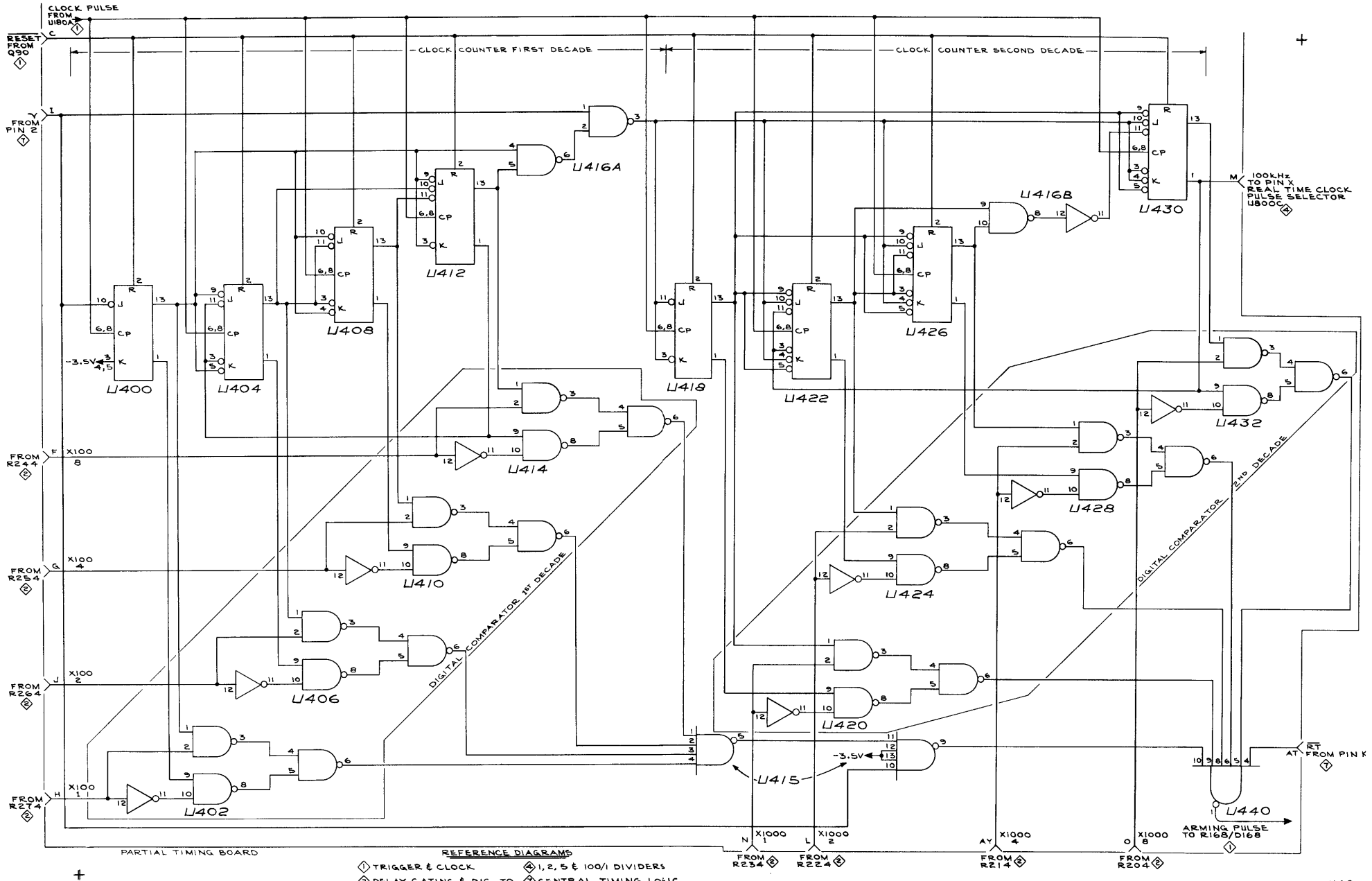

RESET RAMP
RESET MULTIVIBRATOR
Q70 Q72 Q75
EQUIVALENT TIME
TD BIAS
RECOVERY TIME
P21
P23
INT
EXT
TRIG MODE SWITCH
D106 ARMING Q100
ISOLATION AMPLIFIER Q20
TRIGGER INHIBIT Q135
CLOCK START DELAY Q120 Q125
CLOCK OSCILLATOR CLAMP Q130 Q140 Q145
10MHz OSCILLATOR CLOCK Q150 Q155
COUNTER CLOCK PULSE SHAPER Q170
CLOCK CURRENT PULSER Q160
SENSITIVITY
D108
D110
D112
D28
D106
D114
-3.5V
DELAY LINE
C118
R68
WIRED "OR"
INT EXT Q35
EXT AUTO Q40
NO SIGNAL IN REAL TIME
TIMING RAMP ENABLE TD
D168
EQUIVALENT TIME ARMING
EQUIVALENT TIME RESETS TRIGGER CIRCUIT AT END OF EACH TIMING RAMP
REAL TIME RESETS TRIGGER CIRCUIT AT END OF EACH SWEEP
RAMP CLAMP Q525 Q535 Q530
EQUIVALENT TIME RAMPS
100 n s
1 µs
10 µs
100 µs
1 ms
10 ms
100 ns RAMP LENGTHENER Q545
TIMING RAMP Q500 Q503 Q507 Q510 Q513 Q516
AUTO CAL
J24
LOADING
TIMING RAMP RESET COMPARATOR Q538 Q548
NON-LOADING
BLOWING COMPARATOR Q550 Q555 Q553
TRIGGER CIRCUIT CONTROL IN RT
RT Q540 INHIBIT IN EQUIVALENT TIME
INVERTER AMPLIFIER Q560
ALWAYS 1000 SAMPLES/SWP IN REAL TIME
PARTIAL
STROBE DRIVE Q565
STEP DRIVE
SAMPLES/SWP
SWEEP RESET
J24
CIRCUITS IN GRAY AREA INACTIVE
STROBE COMMAND TO VERTICAL SAMPLING UNIT
RESET
100/1 DIVIDER Q460
U110A ISOLATOR
100MHz INHIBIT
100kHz
10MHz
U110B
U110A
U60A
CLOCK
CLOCK COUNTER 2 DECADE 167 DECADES
CARRY
DIGITAL COMPARATOR 2 DECADE
DIGITAL COMPARATOR 167 DECADES
EQUIVALENT TIME ENABLE (RT)
U440
U415
167 DECADE ENABLE
DELAY SWEEP OR EXT PROG INPUTS
X1000
X100
X1
X10
DELAY GATING
100V REFERENCE
FINE DELAY COMPENSATION
DECADE 3
DECADES 1 & 2
REAL TIME ENABLE
MULTIPLIER CONTROL
REAL TIME 1, 2, 5 DIVIDER
CLOCK PULSE SELECTOR
DECADE CONTROL
WHEN 1, 2 OR DECADE 3 IS ENABLED
INHIBITS EQUIVALENT TIME STROBE COMMANDS
U60A
RESET
J24 & DECADE SWEEP MULTIPLIER SWEEP
CENTRAL TIMING LOGIC
LOGIC 1 CARD
LOGIC 2 CARD
DECADE B,C,D 1-0 (10)
MULTIPLIER B,C,D (1, 2, 5)
FRONT PANEL OR EXT PROG INPUTS
SWEEP RATE 1-2-10
TRUE OUTPUT POLARITY
A 100 ns RAMP
B 1 µs RAMP
C 10 µs RAMP
D 100 µs RAMP
E 1 ms RAMP
F 10 ms RAMP
I
II 5C ATTEN CONTROL
III
IV 5C INV GAIN CONTROL
IV FINE DELAY COMP
VII FINE DELAY ATTEN
V VI DECADE ENABLE
RT EQUIV TIME
INTERNAL GATE CONTROLS
LOGIC #1 OUTPUT
LOGIC #2 OUTPUT
J850
J800
TO
TYPE 230 PLUG-ON TIME MEASUREMENT ENABLE
DIGITAL UNIT CONTROL LOGIC Q890
SWEEP RATE READOUT LOGIC
D8324 - D8356
P22
DIGITAL TO ANALOG AMPLIFIER Q360A Q370 Q375 Q390
FINE DELAY ATTENUATOR Q380 Q395 Q385 Q398 Q390
Q DECADE X10 GAIN SWITCHING Q570 Q575 Q572
STAIRCASE INVERTER AMP INPUT RESISTORS ATTENUATOR Q680 Q684 Q681 Q686 Q683 Q687
0V TO +7.5V
R678
STAIRCASE INVERTER AMPLIFIER Q678 Q690
SWEEP GATE AMPLIFIER Q650
DIGITAL CLOCK AMPLIFIER Q606
BLANKING AMPLIFIER Q640
SWEEP GATE
DIGITAL CLOCK
CRT BLANKING
STAIRCASE
0V TO +60V
SWEEP SPEEDUP ENABLE Q840 Q845 Q860
SWEEP SPEEDUP (DOT DENSITY)
STAIRCASE STEPPER Q670 Q675
STAIRCASE GENERATOR Q680 Q685 Q690 Q695
STAIRCASE RESET MULTIVIBRATOR Q810 Q815 Q830 Q835
SWEEP RESET TRIPPER Q600
ATTENUATOR R690 R697 Q700 Q705
HORIZ POS
HORIZONTAL AMPLIFIER Q710 Q720 Q730
POSITION LAMPS Q740 Q745
P22
P21
TYPE 3T6 EQUIVALENT TIME
BLOCK DIAGRAM
1168

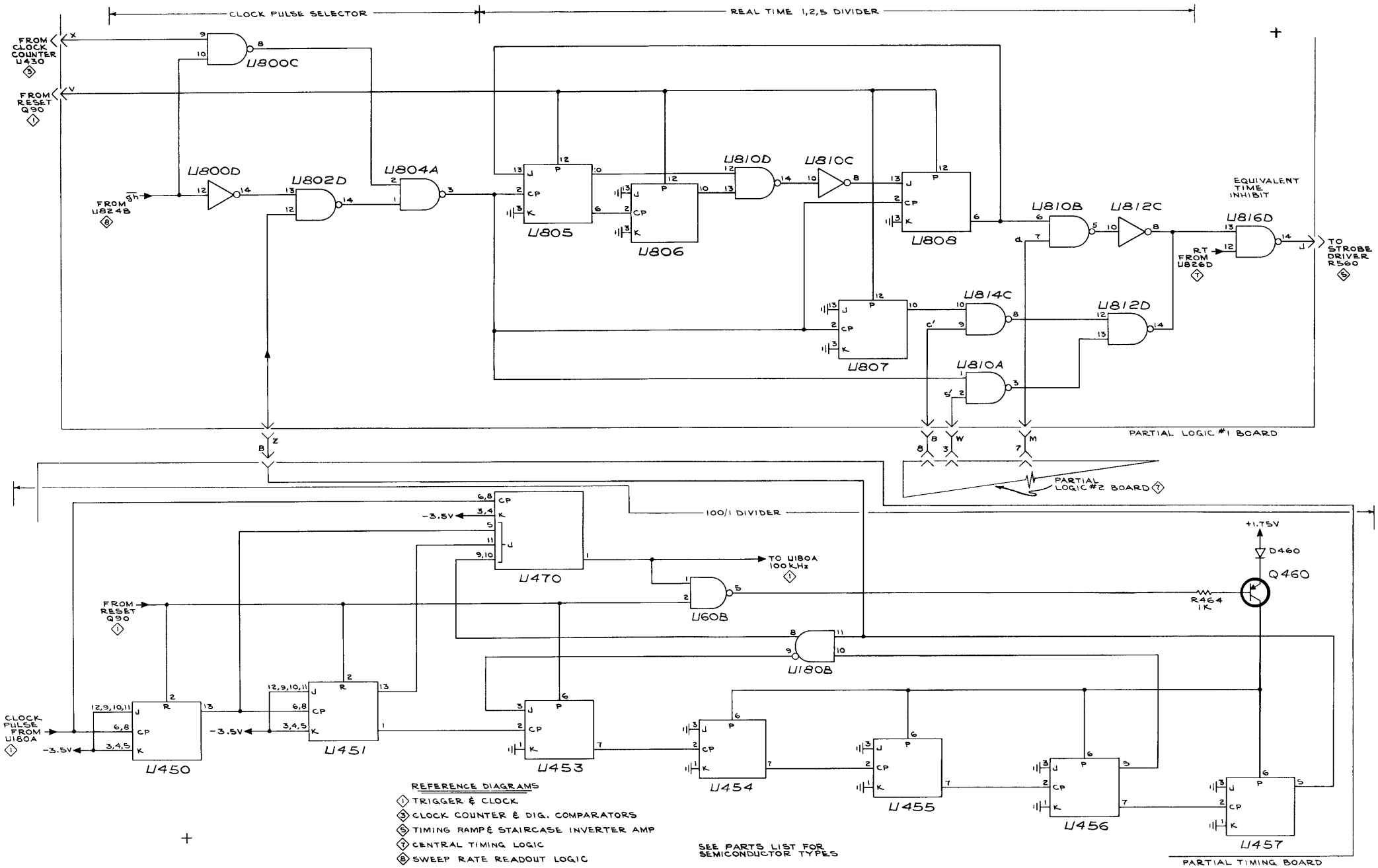

RESET
TRIG OUTPUT POLARITY
CENTRAL TIMING LOGIC
LOGIC 1 CARD
LOGIC 2 CARD
DIGITAL UNIT CONTROL LOGIC
SWEEP RATE READOUT LOGIC
TYPE 830 D,U,C,N,D (TIME MEASUREMENT ENABLE)
A 100 ns RAMP
B 1 µs RAMP
C 10 µs RAMP
D 100 µs RAMP
E 1 ms RAMP
F 10 ms RAMP
II 10X ATTEN CONTROL
IV 5X INV GAIN CONTROL
V FINE DELAY COMP
VI FINE DELAY ATTEN
VII 1ST DECADE ENABLE
EQUIV TIME
INTERNAL GATE CONTROLS
LOGIC "1" OUTPUT
LOGIC "2" OUTPUT
J850
J800
P22
P21
RESET RAMP
RESET MULTIVIBRATOR
COUNTER RESET
100/1 DIVIDER
ISOLATOR
TD BIAS
ARMING
ISOLATION AMPLIFIER
TRIGGER INHIBIT
CLOCK START DELAY
CLOCK OSCILLATOR CLAMP
10 MHz OSCILLATOR CLOCK
COUNTER CLOCK PULSE SHAPER
CLOCK COUNTER
2ND DECADE
1ST DECADES
EQUIVALENT TIME ENABLE (ET)
CLOCK CURRENT PULSER
DIGITAL COMPARATOR 2ND DECADE
DIGITAL COMPARATOR 1ST DECADES
WIRED "OR"
1ST DECADES ENABLE
TIMING RAMP ENABLE TD
EQUIVALENT TIME ARMING
NO SIGNAL IN REAL TIME
INT EXT
EXT AUTO
DELAY LINE
SENSITIVITY
EQUIVALENT TIME: RESETS TRIGGER CIRCUIT AT END OF EACH TIMING RAMP
REAL TIME: RESETS TRIGGER CIRCUIT AT END OF EACH SWEEP
RAMP CLAMP
EQUIVALENT TIME RAMPS
TIMING RAMP
AUTO CAL
100 MHz RAMP LENGTHENER
LOADING
TIMING RAMP RESET COMPARATOR
NONLOADING
SLEWING COMPARATOR
DELAY GATING
DIGITAL TO ANALOG AMPLIFIER
FINE DELAY ATTENUATOR
FINE DELAY COMPENSATION
-100V REFERENCE
DECADE 3
DECADES 1 & 2
DECADE CONTROL
MULTIPLIER CONTROL
REAL TIME ENABLE
REAL TIME 1, 2, 5 DIVIDER
CLOCK PULSE SELECTOR
INVERTER AMPLIFIER
TRIGGER CIRCUIT CONTROL IN ET
ET Q540 INHIBIT IN EQUIVALENT TIME
INHIBITS EQUIVALENT TIME STROBE COMMANDS
ALWAYS 1000 SAMPLES/SWP IN REAL TIME
STROBE DRIVE
CIRCUITS IN GRAY AREA INACTIVE
STEP DRIVE
STROBE COMMAND TO VERTICAL SAMPLING UNIT
STAIRCASE INVERTER AMP INPUT RESISTORS ATTENUATOR
STAIRCASE INVERTER AMPLIFIER
0 DECADE X10 GAIN SWITCHING
0 V TO +7.5 V
SWEEP GATE AMPLIFIER
DIGITAL CLOCK AMPLIFIER
BLANKING AMPLIFIER
STAIRCASE STEPPER
STAIRCASE GENERATOR
STAIRCASE RESET MULTIVIBRATOR
SWEEP RESET TRIPPLER
SWEEP SPEEDUP ENABLE
SWEEP SPEEDUP (DOT DENSITY)
SAMPLES/SWP
SWEEP RESET
ATTENUATOR
HORIZ POS
HORIZONTAL AMPLIFIER
POSITION LAMPS
SWEEP GATE
DIGITAL CLOCK
EXT BLANKING
STAIRCASE
TYPE 3T6
REAL TIME
BLOCK DIAGRAM
1168


RESET MULTIVIBRATOR
COUNTER RESET
RECOVERY TIME
SWS MODE
RESET RAMP
U60A
10 MHz INHIBIT
Q70
Q72
Q75
Q90
Q80
Q82
Q84
Q86
Q100
ARMING
ARMING TO BIAS
RESET
INTERNAL TRIGGER
POLARITY SW10
P10 J10
P21
P23
INPUT
Q20
DC ZERO
ISOLATION AMPLIFIER
SENSITIVITY
(GANGED)
SYNC
SW7B
AUTO LEVEL
TRIG SENS ZERO
Q35
INT EXT
EXT AUTO
Q40
STRIP LINE
P50 P55
J50 J55
D28 10MA
D106 10MA
D114 10MA
TRIGGER INHIBIT
Q135
Q40
CLOCK OSCILLATOR CLAMP
10 MHz CLOCK
CLOCK START POINT
CLOCK START DELAY
RECOG TO BIAS
Q125
Q120
Q130
Q50A
Q155
Q145
Q50B
Q160
CLOCK CURRENT PULSER
TIMING RAMP ENABLE TD BIAS
CLOCK FREQ
CLOCK STABILITY
Q170
COUNTER CLOCK PULSE SHAPER
ARMING PULSE FROM U440 DIGITAL COMPARATOR
TIMING RAMP ENABLE TD
TIMING RAMP ENABLE TO D520/Q525
PARTIAL TIMING BOARD
U170A
ISOLATOR
U170B
POS OR
CLOCK PULSE TO
U470
100/1 DIVIDER
U450
+300V
+125V
+20V
+3.6V
+1.75V
-3.5V
-12.2V
-100V
REFERENCE DIAGRAMS
1 CLOCK COUNTER & DIG. COMPARATORS
2 1, 2, 5 & 100/1 DIVIDERS
5 TIMING RAMP & STAIRCASE INVERTER AMP
7 CENTRAL TIMING LOGIC
8 INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3T6
TRIGGER & CLOCK 1
1168


SW635 DELAY
SW605 PROGRAM SELECTOR
INT
EXT
J24
X1000
X100
X10
X1
DIGITAL TO ANALOG AMPLIFIER
PARTIAL TIMING BOARD
PARTIAL LOGIC 'E' BOARD
PARTIAL DISPLAY BOARD
SECOND DECADE DIGITAL COMPARATOR
FIRST DECADE DIGITAL COMPARATOR
FINE DELAY ATTENUATOR
Q360
Q370
Q375
Q380
Q385
Q390
Q395
Q398
REFERENCE DIAGRAMS
③ CLOCK COUNTER & DIG. COMPARATORS
④ 1,2,5 & 100/1 DIVIDERS
⑤ TIMING RAMP & STAIRCASE INVERTER AMP
⑦ CENTRAL TIMING LOGIC
⑧ SWITCHING & DELAY READOUT
⑩ INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

TYPE 3T6

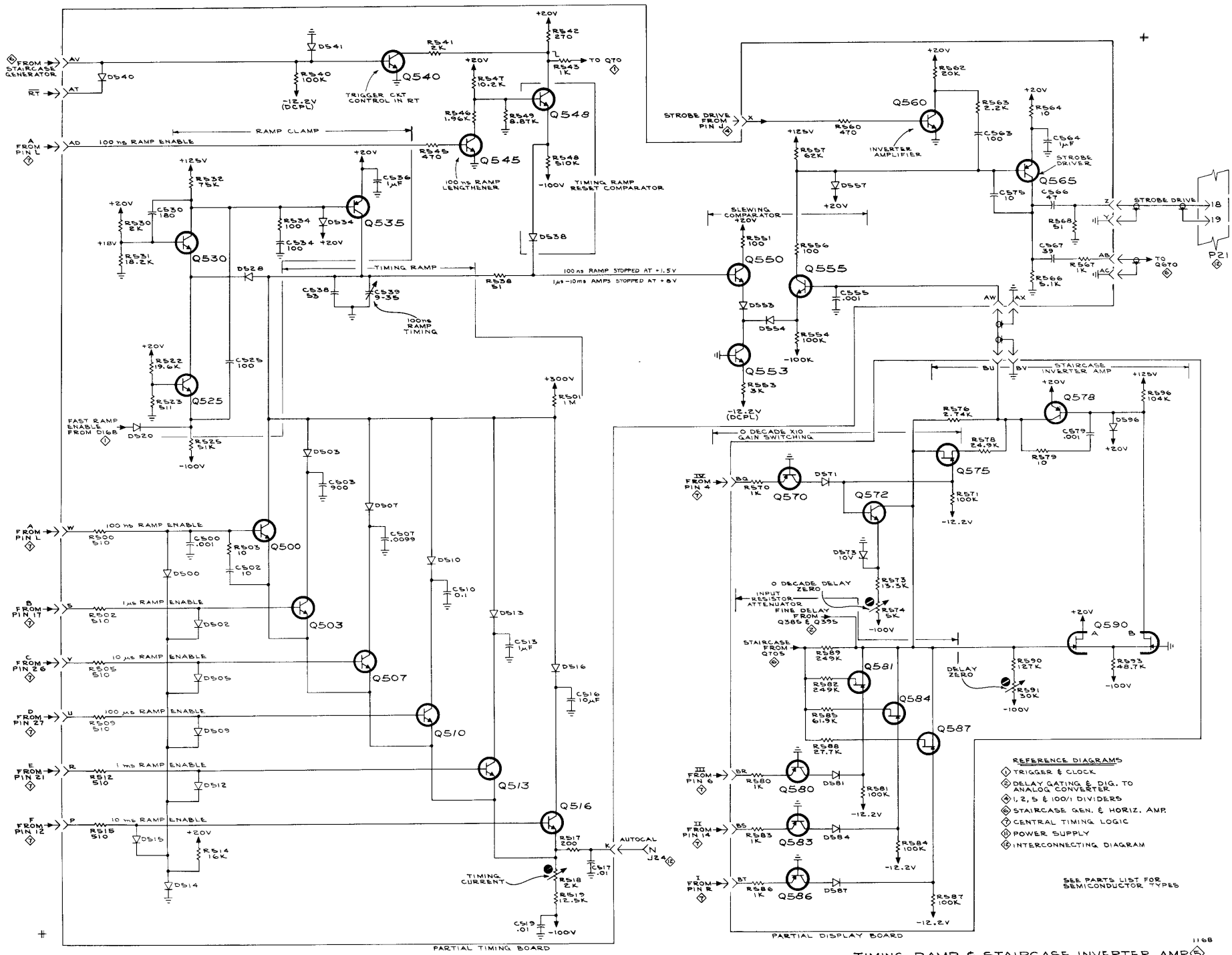

CLOCK PULSE FROM U180A
RESET FROM Q90
CLOCK COUNTER FIRST DECADE
CLOCK COUNTER SECOND DECADE
FROM PIN 2
U400
U404
U408
U412
U416A
U416B
U418
U422
U426
U430
U432
100KHz TO PIN X REAL TIME CLOCK PULSE SELECTOR U800
-3.5V
FROM R244
FROM R254
FROM R264
FROM R274
X100 8
X100 4
X100 2
X100 1
U414
U410
U406
U402
U428
U424
U420
U415
DIGITAL COMPARATOR 1ST DECADE
DIGITAL COMPARATOR 2ND DECADE
AT RT FROM PIN K
U440
ARMING PULSE TO R168/D168
X1000 1
X1000 2
X1000 4
X1000 8
FROM R234
FROM R224
FROM R214
FROM R204
PARTIAL TIMING BOARD
REFERENCE DIAGRAMS
1 TRIGGER & CLOCK
2 DELAY GATING & DIG. TO ANALOG CONVERTER
4 1, 2, 5 & 100/1 DIVIDERS
7 CENTRAL TIMING LOGIC
TYPE 3T6
A
CLOCK COUNTER & DIG. COMPARATORS 3
1168

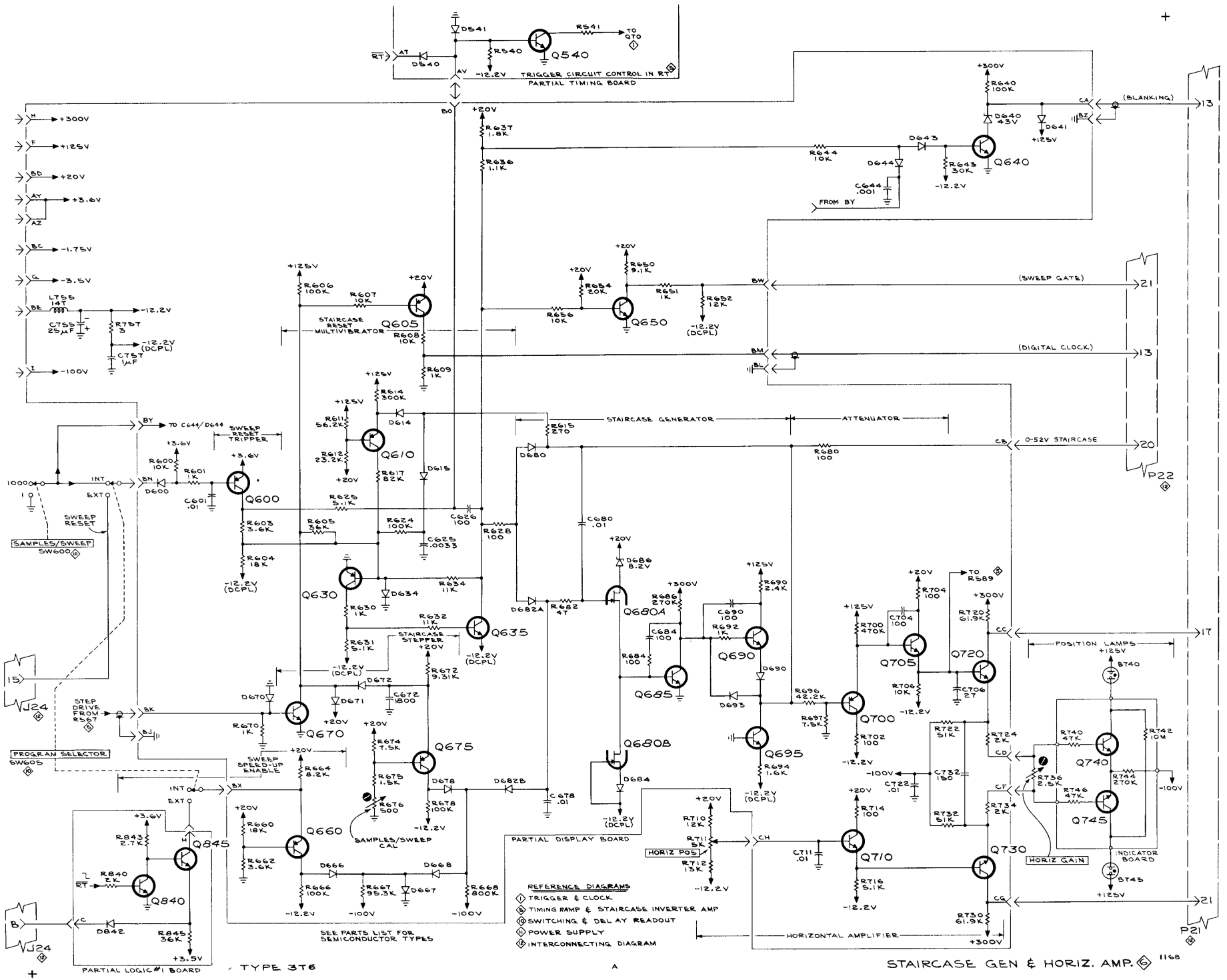


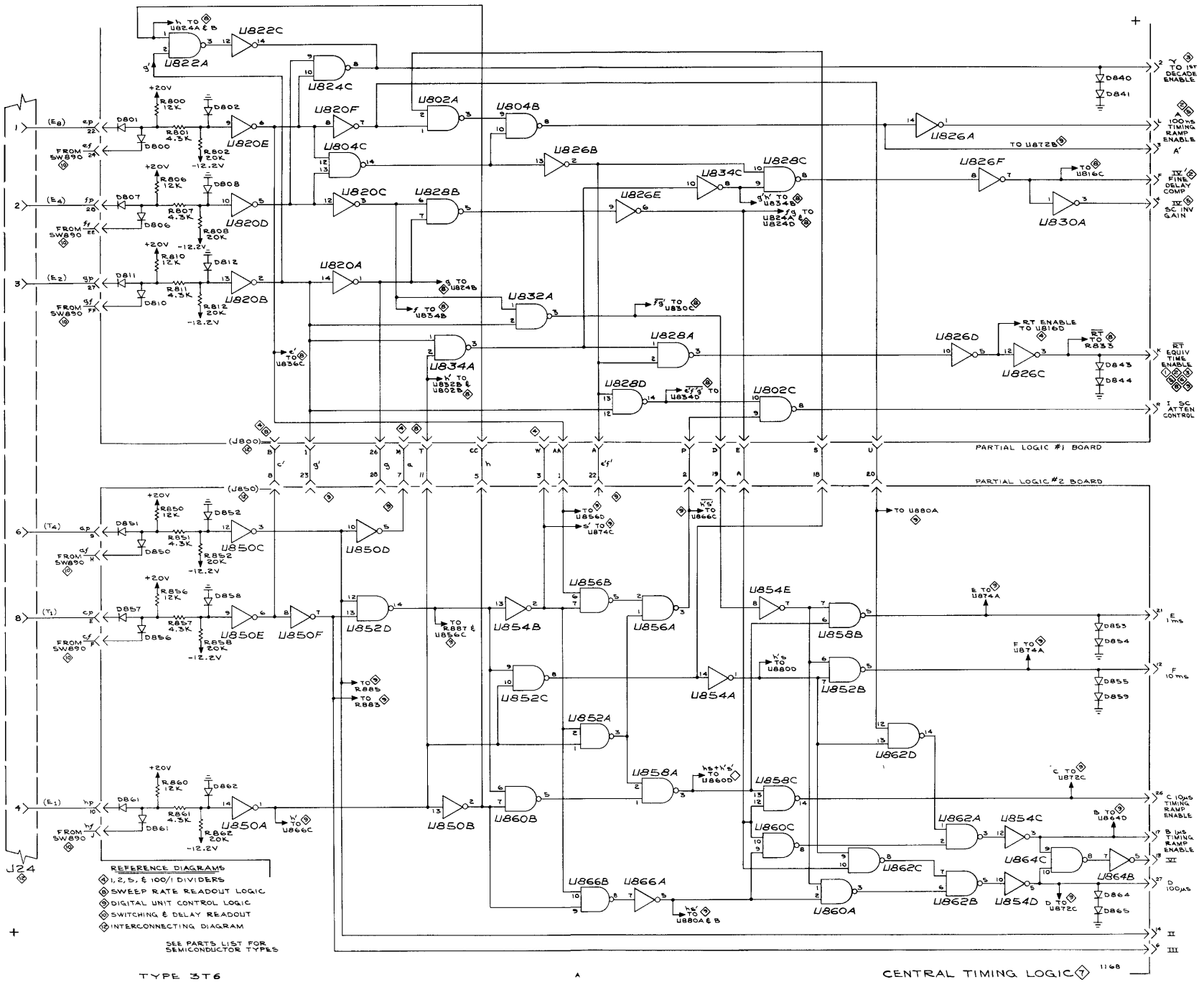
TYPE 3T6

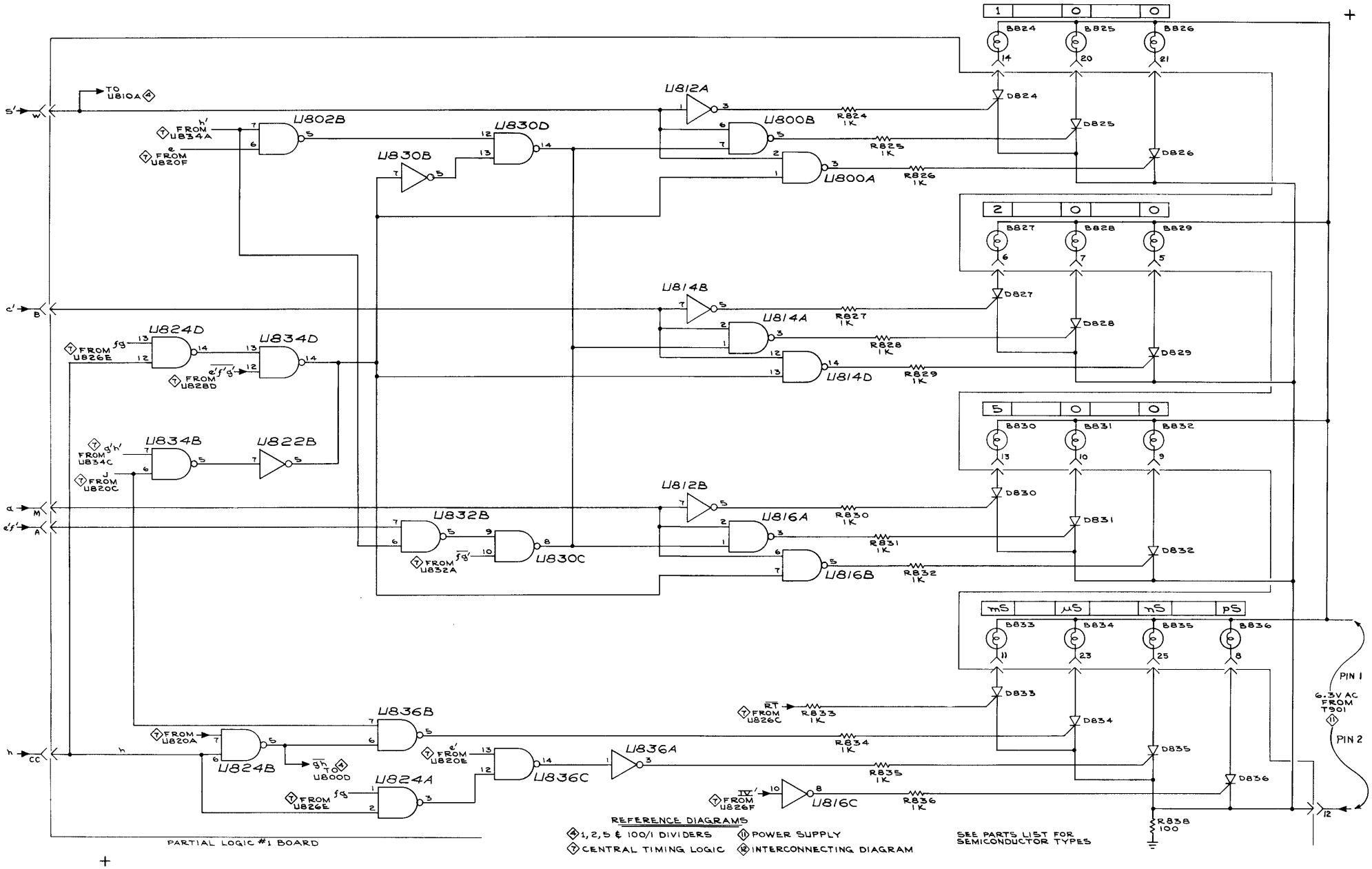
A

1, 2, 5 & 100/1 DIVIDERS ④ 1168


FROM STAIRCASE GENERATOR
RT
RAMP CLAMP
100 ns RAMP ENABLE
TRIGGER CKT CONTROL IN RT
100 ns RAMP LENGTHENER
TIMING RAMP RESET COMPARATOR
TO Q570
STROBE DRIVE FROM PIN U
INVERTER AMPLIFIER
STROBE DRIVER
STROBE DRIVE
SLEWING COMPARATOR
TIMING RAMP
100 ns RAMP STOPPED AT +1.5V
1µs–10ms AMPS STOPPED AT +8V
100ns RAMP TIMING
STAIRCASE INVERTER AMP
FAST RAMP ENABLE FROM D16B
1 µs RAMP ENABLE
10 µs RAMP ENABLE
100 µs RAMP ENABLE
1 ms RAMP ENABLE
10 ms RAMP ENABLE
TIMING CURRENT
AUTOCAL
0 DECADE X10 GAIN SWITCHING
0 DECADE DELAY ZERO
INPUT RESISTOR ATTENUATOR
FINE DELAY FROM Q385 & Q395
STAIRCASE FROM Q705
DELAY ZERO
REFERENCE DIAGRAMS
1 TRIGGER & CLOCK
2 DELAY GATING & DIG. TO ANALOG CONVERTER
4 1, 2, 5 & 100/1 DIVIDERS
5 STAIRCASE GEN. & HORIZ. AMP.
7 CENTRAL TIMING LOGIC
11 POWER SUPPLY
12 INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
PARTIAL TIMING BOARD
PARTIAL DISPLAY BOARD
TYPE 3T6
TIMING RAMP & STAIRCASE INVERTER AMP 5
1168


TRIGGER CIRCUIT CONTROL IN RT
PARTIAL TIMING BOARD
STAIRCASE RESET MULTIVIBRATOR
SWEEP RESET TRIPPER
STAIRCASE GENERATOR
ATTENUATOR
STAIRCASE STEPPER
SWEEP SPEED-UP ENABLE
SAMPLES/SWEEP CAL
PARTIAL DISPLAY BOARD
HORIZ POS
HORIZ GAIN
POSITION LAMPS
INDICATOR BOARD
HORIZONTAL AMPLIFIER
PARTIAL LOGIC #1 BOARD
SAMPLES/SWEEP SW600
PROGRAM SELECTOR SW605
STEP DRIVE FROM RSET
SWEEP RESET
(BLANKING)
(SWEEP GATE)
(DIGITAL CLOCK)
0-52V STAIRCASE
TO C644/D644
FROM BY
REFERENCE DIAGRAMS
TRIGGER & CLOCK
TIMING RAMP & STAIRCASE INVERTER AMP
SWITCHING & DELAY READOUT
POWER SUPPLY
INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3T6
STAIRCASE GEN & HORIZ. AMP.
1168


U822C
U822A
U824C
U820F
U802A
U804B
U804C
U826B
U820C
U828B
U826E
U834C
U828C
U826A
U826F
U830A
U820E
U820D
U820B
U820A
U832A
U828A
U834A
U828D
U802C
U826D
U826C
U850C
U850D
U852D
U856B
U854E
U858B
U856A
U854B
U852C
U854A
U852B
U852A
U862D
U858A
U858C
U860C
U862C
U860B
U850B
U850A
U862A
U854C
U864C
U864B
U862B
U854D
U860A
U866B
U866A
J24
(J800)
(J850)
PARTIAL LOGIC #1 BOARD
PARTIAL LOGIC #2 BOARD
REFERENCE DIAGRAMS
1, 2, 5, & 100/1 DIVIDERS
SWEEP RATE READOUT LOGIC
DIGITAL UNIT CONTROL LOGIC
SWITCHING & DELAY READOUT
INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3T6
CENTRAL TIMING LOGIC
1168

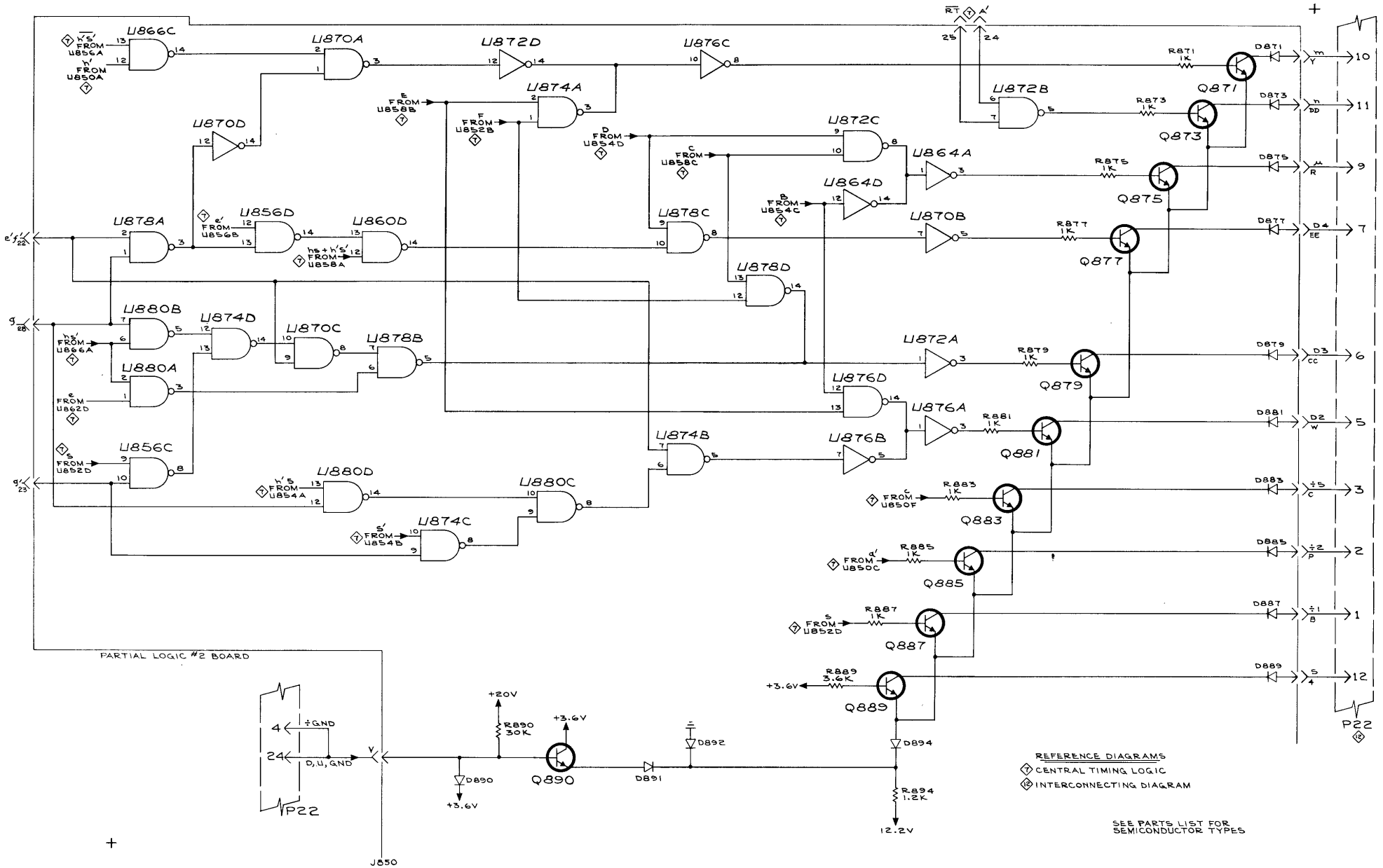


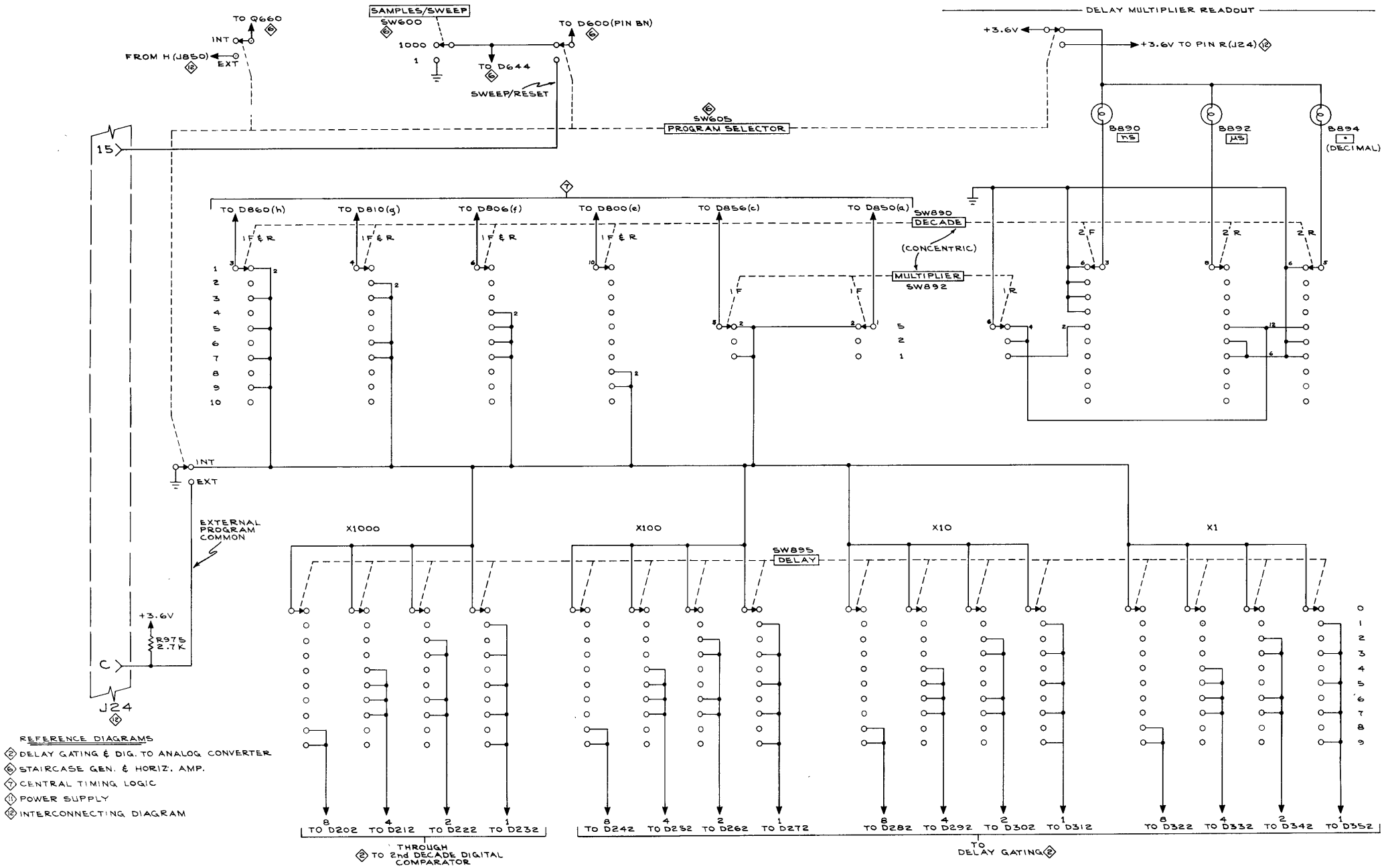
TYPE 3T6

A

SWEEP RATE READOUT LOGIC

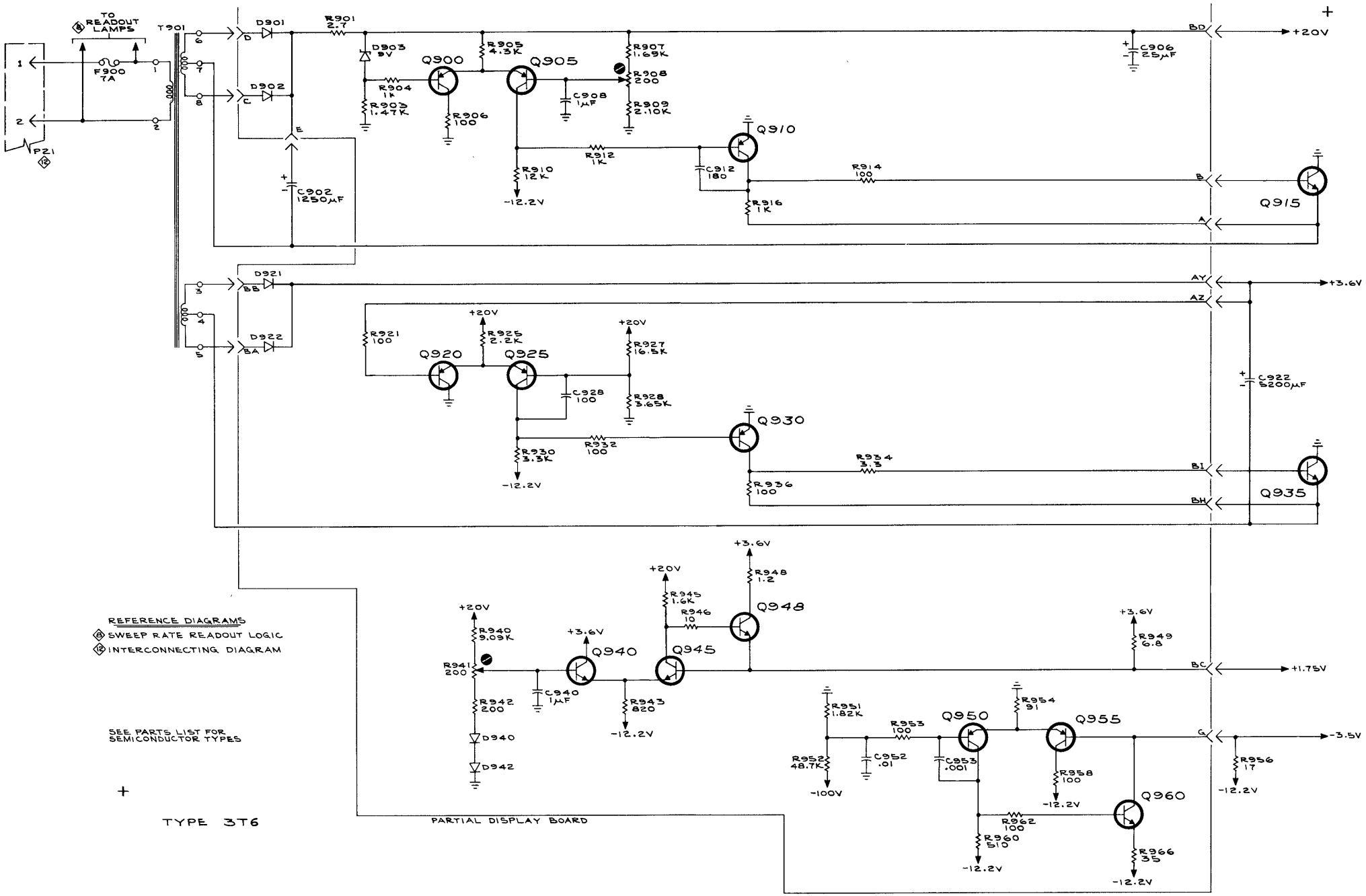
1168

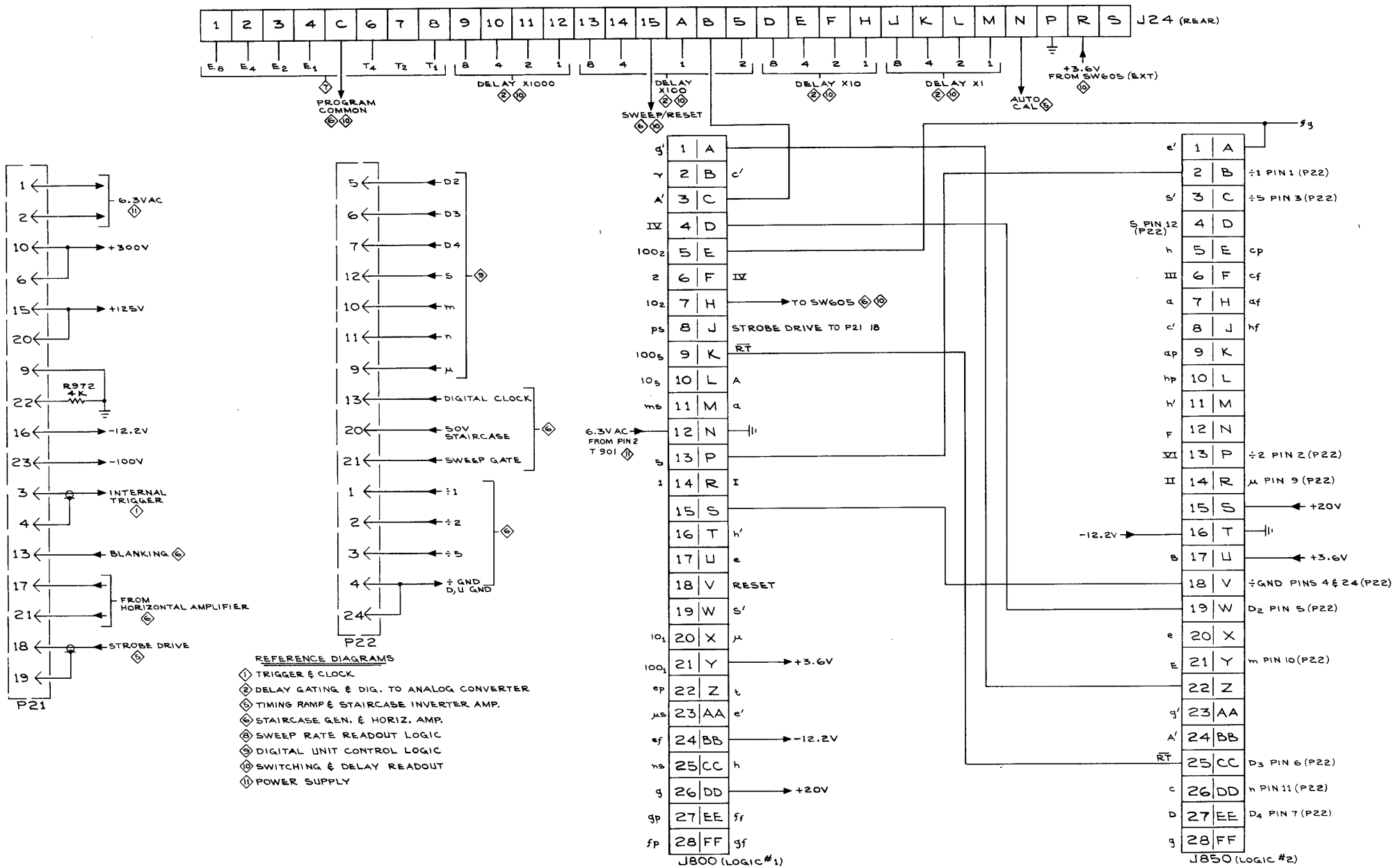

U866C
U870A
U872D
U876C
U870D
U874A
U872C
U864A
U864D
U872B
U878A
U856D
U860D
U878C
U870B
U878D
U880B
U874D
U870C
U878B
U872A
U876D
U880A
U876A
U874B
U876B
U856C
U880D
U880C
U874C
Q871
Q873
Q875
Q877
Q879
Q881
Q883
Q885
Q887
Q889
Q890
R871 1K
R873 1K
R875 1K
R877 1K
R879 1K
R881 1K
R883 1K
R885 1K
R887 1K
R889 3.6K
R890 30K
R894 1.2K
D871
D873
D875
D877
D879
D881
D883
D885
D887
D889
D890
D891
D892
D894
+20V
+3.6V
12.2V
P22
J850
PARTIAL LOGIC #2 BOARD
TYPE 3T6
A
DIGITAL UNIT CONTROL LOGIC 9 1168
REFERENCE DIAGRAMS
7 CENTRAL TIMING LOGIC
12 INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES



REFERENCE DIAGRAMS

- DELAY GATING & DIG. TO ANALOG CONVERTER
- STAIRCASE GEN. & HORIZ. AMP.
- CENTRAL TIMING LOGIC
- POWER SUPPLY
- INTERCONNECTING DIAGRAM


TO READOUT LAMPS
T901
F900 TA
P21
D901
D902
D903 9V
R901 2.7
R903 1.47K
R904 1K
R905 4.3K
R906 100
R907 1.69K
R908 200
R909 2.10K
C902 1250µF
C906 2.5µF
C908 1µF
Q900
Q905
Q910
R910 12K
R912 1K
C912 180
R914 100
R916 1K
-12.2V
+20V
BD
B
A
Q915
D921
D922
R921 100
R925 2.2K
R927 16.5K
R928 3.65K
C928 100
Q920
Q925
Q930
R930 3.3K
R932 100
R934 3.5
R936 100
AY
AZ
BI
BH
C922 5200µF
Q935
+3.6V
R940 9.09K
R941 200
R942 200
R943 820
R945 1.6K
R946 10
R948 1.2
C940 1µF
Q940
Q945
Q948
D940
D942
R949 6.8
BC
+1.75V
R951 1.82K
R952 48.7K
R953 100
R954 91
R956 17
R958 100
R960 510
R962 100
R966 35
C952 .01
C953 .001
Q950
Q955
Q960
-100V
-3.5V
REFERENCE DIAGRAMS
SWEEP RATE READOUT LOGIC
INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3T6
PARTIAL DISPLAY BOARD
POWER SUPPLY
1168



REFERENCE DIAGRAMS

1. TRIGGER & CLOCK
2. DELAY GATING & DIG. TO ANALOG CONVERTER
3. TIMING RAMP & STAIRCASE INVERTER AMP.
4. STAIRCASE GEN. & HORIZ. AMP.
5. SWEEP RATE READOUT LOGIC
6. DIGITAL UNIT CONTROL LOGIC
7. SWITCHING & DELAY READOUT
8. POWER SUPPLY

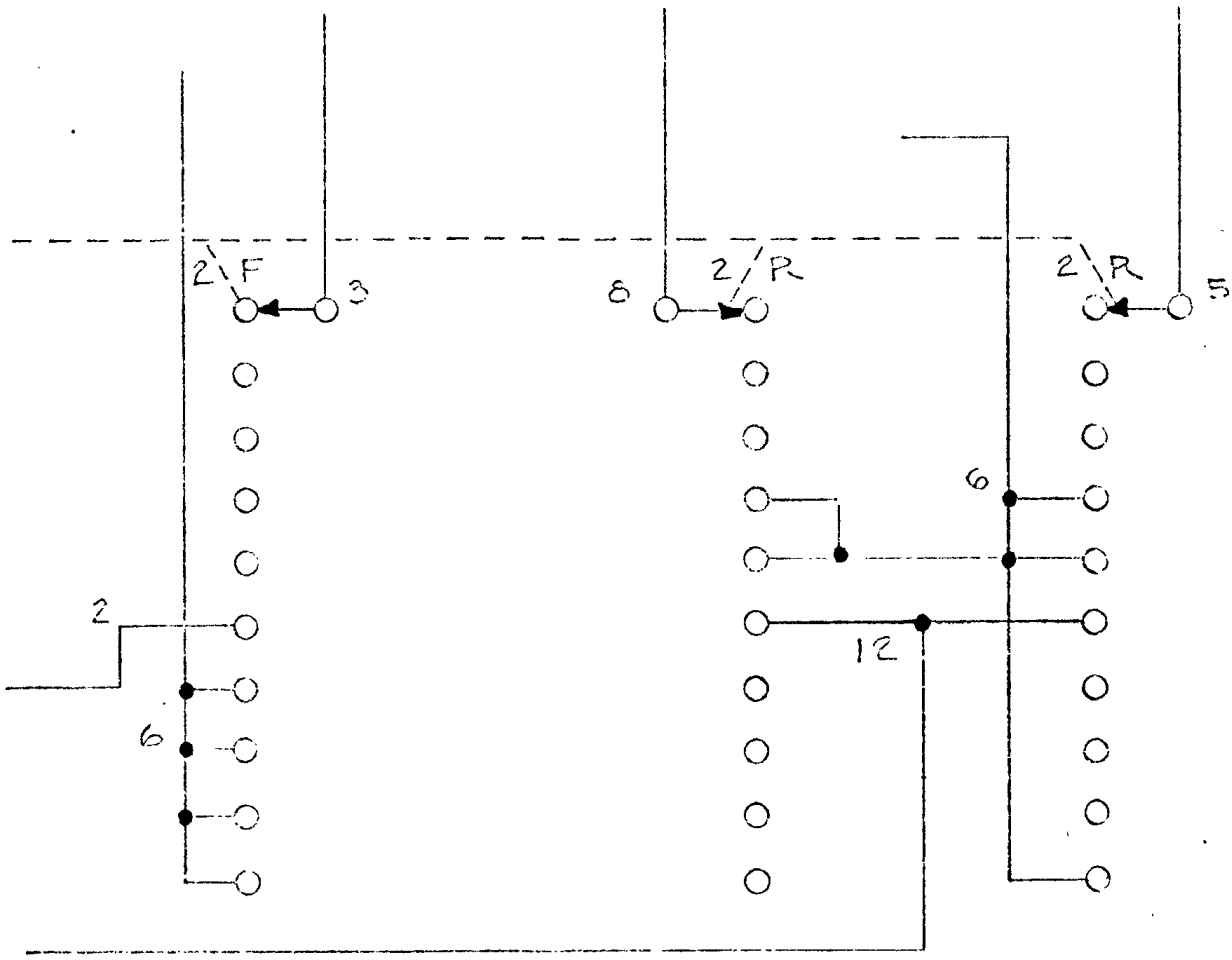
TYPE 3T6

A

INTERCONNECTING DIAGRAM 12 1168

TYPE 3T6

SCHEMATIC CORRECTION



PARTIAL
SWITCHING &
DELAY READOUT

C1/1168

General Information

This modification changes circuits that affect the External Automatic triggering mode of operation and the required time per sample at some of the equivalent-time sweep rates.

TEXT CORRECTION

Section 1 Specification

Page 1-1

CHANGE: Electrical Characteristics under External Auto, change Amplitude Range to the following:

Signal Voltage	
POLARITY Sw. +	
Positive Peak	Between +100 mV and +500 mV
Negative Peak	Between +10 mV and -500 mV
POLARITY Sw. -	
Positive Peak	Between -10 mV and +500 mV
Negative Peak	Between -100 mV and -500 mV

Page 1-2

CHANGE: the last two lines of the left column to read:

10 ns to 1 ns	Exclude first 15 ns of sweep
500 ps to 100 ps	Exclude first 15 ns of sweep NOTE: Accurate within 5%

Section 2 Operating Instructions

Page 2-6

ADD: immediately under the Triggering heading, right column:

Three basic modes of triggering are available in the Type 3T6, as controlled by the trigger MODE switch. The modes are: Internal, External and External Automatic. Internal triggering is AC coupled only, and both external modes are DC coupled. The external mode (not automatic) can be altered from a normal triggering function to be Synchronized with high frequency information above 100 MHz. (Synchronized operation is not recommended for the Internal mode because internal trigger pickoff circuits and connections do not allow sine wave signals above about 100 MHz to reach the trigger circuits.)

Each Basic triggering mode causes the triggering event to occur on only the positive or the negative signal slope as controlled by the POLARITY switch. Both the External and External Auto modes require the triggering signal to have a voltage component positive with respect to ground for +POLARITY triggering, and have a voltage component negative with respect to ground for -POLARITY triggering. Section 1 lists the minimum and maximum signals required for each mode of operation.

CHANGE: first two words, Internal Triggering under present Triggering heading, underline them to delineate that following text is a discussion of internal triggering only.

CHANGE: beginning with third paragraph under Triggering, replace remainder of triggering text with the following:

External triggering (not automatic) must be selected when the pretrigger signal amplitude is less than 100 mV peak to peak. The POLARITY switch must be set to equal the polarity of the triggering signal. If the trigger signal peaks are at ground and +50 mV, set the POLARITY switch to + to obtain proper displays. If the trigger signal peaks are at ground and -50 mV, set the POLARITY switch to - to obtain proper displays. (In some cases, a triggered display can be obtained when the POLARITY switch is incorrectly set, but at that time, removal of the triggering signal will reveal a free running trigger circuit. This is not considered normal or proper triggering.)

NOTE

Earlier models of the Type 568 Oscilloscope require installation of Field Modification Kit, Tektronix Part No. 040-0492-00 to provide a means of externally triggering the Type 3T6. This modification consists of installation of J23 on the Type 568 rear panel and J23 at the rear of the vertical plug-in compartment.

External Auto triggering is desirable when the triggering signal is known to be greater than 100 mV peak to peak with one peak at ground. Then the operator need not make any control adjustments to obtain proper displays. The External Auto triggering mode is of particular advantage when the Type 3T6 is used in an automatically

programmed system where the triggering signal can be planned to always have sufficient amplitude. The primary limitation of EXT AUTO triggering is that the signal must always have one peak within 10 mV of ground. Signals that are offset from ground more than 10 mV in the direction that the POLARITY Switch is set, may not permit the external automatic circuit to operate, thereby preventing a display. If it is not possible to obtain a triggering signal with one peak near ground, place an AC coupling capacitor in series with the trigger cable. If the trigger signal has a duty factor near 50%, then the signal received by the trigger circuit will pass through zero, but the total amplitude will have to be $\geq$ 200 mV peak-to-peak in order to obtain a display.

Use of the SENSITIVITY and RECOVERY TIME controls. These two controls must be properly adjusted when the triggering mode is either Internal or External (not automatic). The SENSITIVITY control has a range of control over the various trigger signals as listed on page 1-1 in the Electrical Characteristics table. Full counterclockwise rotation of the control will assure there is no sweep when the triggering signal maximum value is less than the maximum value for the particular sensitivity range listed. Turning the control clockwise past its midpoint will cause the trigger circuits to free run and provide a display when there is no triggering signal.

The RECOVERY TIME control should be adjusted whenever the display is confused, even though the SENSITIVITY control is adjusted in the proper region. The RECOVERY TIME control must be adjusted any time a trigger pulse duration is longer than the sampling cycle recovery time, or when the trigger signal period is harmonically related to the trigger circuit countdown rate (discussed below). (Choose a slower sweep rate if the trigger period is longer than the numbers in the right column of Table 2-1.) Both controls should always be adjusted when first obtaining a display from a new signal, with the goal that proper setting assures minimum displayed time jitter. In cases where the display is a pulse chain, the recovery time can be made longer by switching in more clock controlled DELAY (Defined in the left column of page 3-6). This method does

not apply when only one step function is displayed and to add delay would only place the desired signal portion out of sight off the CRT left side.

CHANGE: lines 1, 2 and 4 of TABLE 2-1 to read:

100 ps to 1 ns	12 µs
2 ns to 10 ns	12 µs
20 ns to 100 ns	12 µs
200 ns to 1 µs	22 µs

Page 2-11 second column, 3rd paragraph

CHANGE: last line to read:

..as listed in column 3 of Table 2-4.

second column, 2nd paragraph under Display Rate When Using Equivalent-Time Sampling

CHANGE: the 12th line to read:

..as is 3 µs to 6 µs at all sweep rates. Adding time intervals...

Page 2-12 Table 2-4, 6th column

CHANGE: lines 9 through 11 to read 4 µs and lines 12 through 21 to read 6 µs.

Fig. 2-9

CHANGE: the arming time, 7th time zone to read:

"3 µs to 6 µs"

Section 3 Circuit Description

Page 3-6 second column, 2nd paragraph

CHANGE: lines 7 and 8 to read:

D114 via D112. The trigger signal from D28 is also delayed (through a 3.75 ns Delay Line, DL50) and then trips D114 to...

Page 3-13 left column, 2nd paragraph

CHANGE: line 5 through the end of the paragraph to read:

by the Isolation Amplifier Q20; its output through L20-R28 (D20 is reverse biased) switches tunnel diode D28 to its high voltage state, which drives D106 and about 4 ns later, D114 (D114 is driven through DL50). The resulting output pulse from D114 sends a signal to D168 and to Q120.

left column, 4th paragraph

CHANGE: line 7 to read:

arrives through C50 and the 4 ns Delay Line, DL50.

left column, 5th paragraph

CHANGE: line 2 to read:

circuit, Q135 and D20 are caused to conduct enough Q20 current so...

right column, 3rd paragraph

CHANGE: the last sentence to read:

When Q75 turns off, D102 no longer reverse biases Q100, which turns on and discharges C106 to -3.5 volts.

Page 3-14 left column, Special Trigger Circuit

ADD: 2 sentences into line 7 of Special Trigger Circuit as follows:

compensates the emitter-base junction of Q20. D20 isolates Q20 collector circuit from Q135 emitter circuit when Q135 is at cut-off. L20 prevents Q20 from oscillating while Q135 is conducting. C26 provides...

Page 3-16 Q530-Q535 form the Ramp Clamp

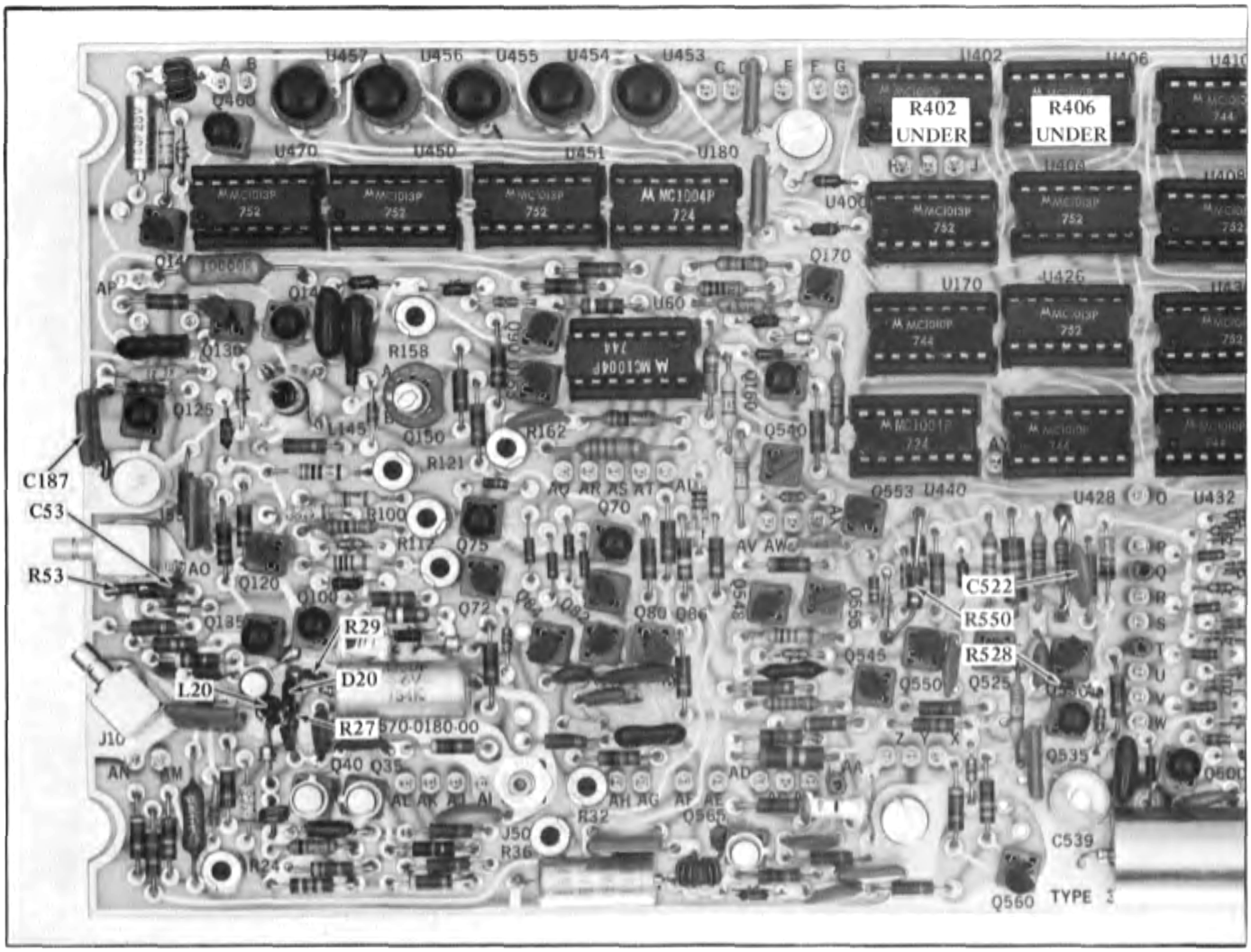
ADD: the following sentences to the 2nd paragraph under Q520-Q530 for the Ramp Clamp:

C522 holds Q525 base impedance low so the drive pulse through D520 stops Q525 conduction rapidly. R528 pulls up on Q525 collector to aid in rapidly clearing the carriers out of the transistor junction region as the drive pulse stops conduction.

The Slewing Comparator

ADD: the following sentence after the 3rd sentence under The Slewing Comparator:

R550 assures that D553 junction carriers are cleared out rapidly at the time it turns off, aiding to make the comparison occur as rapidly as possible.



New parts location on the Timing Circuit board due to M14,392/1268.

Section 5 Performance Check/Calibration

Page 5-4 left column.

ADD: to the Equipment Required List:

30. A 1.5 Volt size D Dry cell (not shown).

31. A 2.5 kΩ potentiometer, 2 watt, such as Tektronix Part No. 311-0395-00. (Not shown.)

32. A 47 Ω 1/2 watt carbon composition resistor (not shown).

Page 5-19 left column, Step 18 (d) and Step 19

REPLACE: the text with the following:

d. Disconnect the signal generator and cables.

19. Adjust Auto Level, R32

a. Set the Type 3T6 TIME/DIV to 1 μs (DECADE switch to 6, MULTIPLIER switch to 1). Trigger switches for + External triggering, and the DELAY controls all to zero.

b. Make connections between the Type 284 and both the sampling head input and the Type 3T6 external trigger INPUT connector. The equipment includes:

Variable Attenuator (item 21).

2X Attenuator (item 20).

GR 874-T, Coaxial tee (item 22).

GR 874-TPD, Power Divider Tee (item 23).

Two 5 ns signal delay cables with GR 874 connectors (item 15).

GR to BNC male adapter (item 24).

1.5 volt dry cell battery (item 30).

2.5 kΩ potentiometer, 2 watt (item 31).

47 Ω, 1/2 watt carbon resistor (item 32).

Leads that place the battery, potentiometer and 47 Ω resistor in series to be clipped to the open port of the tee connector, see Fig. 5-18A.

Install the Variable Attenuator (with the arrow pointing outward) to the Type 284 Square Wave Or Sine Wave Output connector. Install, in order, to the Variable Attenuator, a GR Tee, a GR TPD to one port of the Tee, and the two coaxiable cables to the two remaining ports of the GR TPD. This leaves one port of the Tee open for connecting a DC offset current from the battery and potentiometer. Connect one of the cables to the sampling head input, and the other cable to a GR to BNC adapter and then to the Type 3T6 external trigger INPUT connector. See Fig. 5-18A.

c. Set the sampling unit vertical deflection factor to 50 mV/Div. Set the Type 284 controls:

Square Wave Amplitude	1.0 V
Period	10 μs
Mode	For Square Wave

Set the Variable Attenuator control fully clockwise. Adjust the Type 3T6 Trigger SENSITIVITY and RECOVERY TIME controls for a stable CRT display. Use the sampling unit DC Offset control to position the signal zero-volt point one major division below graticule center. Reduce the signal amplitude to 100 mV peak to peak by adjusting the Variable Attenuator control. The display will be like waveform number 1 of Fig. 5-18C.

If the display disappears before the signal amplitude reaches 100 mV, turn R32 (location shown in Fig. 5-18B) a few degrees clockwise. Clockwise rotation of R32 may ultimately produce a free running trace because D28 is oscillating. The final adjustment includes only a few degrees of the total rotation of R32.

d. Waveforms 2 and 3 of Fig. 5-18C are operations that check the hysteresis gap of the Schmidt type Trigger Recognition circuit and D28. The final hysteresis gap must center around +55 mV, and have a magnitude that is either $\geq$ 20 mV or $\leq$ 90 mV. When the hysteresis gap is 20 mV, the display will remain triggered by a signal with a positive excursion that exceeds +65 mV and with a negative excursion that is less positive than +45 mV. The Specification section states only the maximum hysteresis gap of 90 mV, which means there will be a triggered display when the signal maximum positive excursion is $\geq$ 100 mV and the negative excursion is less

positive than +10 mV. The same hysteresis gap limits apply for negative signals below ground with the limits between $\geq$ -100 mV and $\leq$ -10 mV.

Waveform number 2, produced by reducing the signal amplitude to be less than +100 mV, checks the Trigger Recognition circuit hysteresis gap positive voltage. Slowly reduce the signal amplitude (using the Variable Attenuator control) until the trace disappears. Note the signal positive value at the point that just restores the display.

Waveform number 3 is obtained by applying a positive offset to the 100 mV peak to peak signal. Offset is applied by connecting the 1.5 volt dry cell, 47 ohm resistor and clip leads to the Tee open port; see Fig. 5-18A. Before making connections, place the variable resistor for maximum resistance of 2.5 kΩ. Connect the positive lead to the Tee center conductor, and the negative lead to the outer conductor.

Now increase the offset voltage until the trace disappears. Note the signal negative excursion positive voltage value at the point that just restores the display.

If the two signal voltages that permit a triggered display are +90 mV and +50 mV, then R32 must be turned slightly clockwise to lower the hysteresis gap to be centered around +55 mV. The Specification has been met if the hysteresis gap limits are 90 mV, centered around +55 mV.

e. Reverse the offset leads so the signal can be offset negative, and set the Type 3T6 Triggering POLARITY switch to -. It may be necessary to change the Trigger MODE switch to EXT in order to properly offset the signal, and then return it to EXT AUTO once the 100 mV peak to peak display is centered around -55 mV. (The 47 Ω resistor limits the battery current to about 21 mA when the variable resistance is zero, preventing damage to the 2X attenuator and/or the GR 874-TPD.)

Check that the Trigger Recognition circuit negative triggered hysteresis gap limits are the same as the positive limits, but centered around ≈ -55 mV. It is not required that the negative gap center be precisely at -55 mV, but it is important that there be a trace when the trigger signal DC peak values are at -100 mV (or more negative) and at -10 mV (or less negative).

In the event R32 does not move the hysteresis gap center voltage, but instead only affects the positive voltage at which the trace stops (part d above), then D28 is oscillating and must be replaced by a new

tunnel diode. Use only a tunnel diode and R44 purchased from Tektronix, because they have been specially checked to operate in this particular circuit.

In the event the hysteresis gap is less than 20 mV, change Q40. A too narrow hysteresis gap means that Q40 saturation resistance is too high. A too wide hysteresis gap is very unlikely.

(In an emergency, R44 may be changed. However, it must be a precision metal film resistor. Change it to be larger if a larger hysteresis gap is needed, at a value rate of approximately 1 Ω for an additional 9 mV of gap voltage limits.)

f. Disconnect the hook-up and the Type 284.

ELECTRICAL PARTS AND SCHEMATIC CORRECTIONS

REMOVE:

C130	281-0634-00	10 pF	Mica	100 V	1%
C157	283-0002-00	0.01 µF	Cer	500 V	
C534	283-0060-00	100 pF	Cer	200 V	5%
R534	315-0101-00	100 Ω	1/4 W		5%

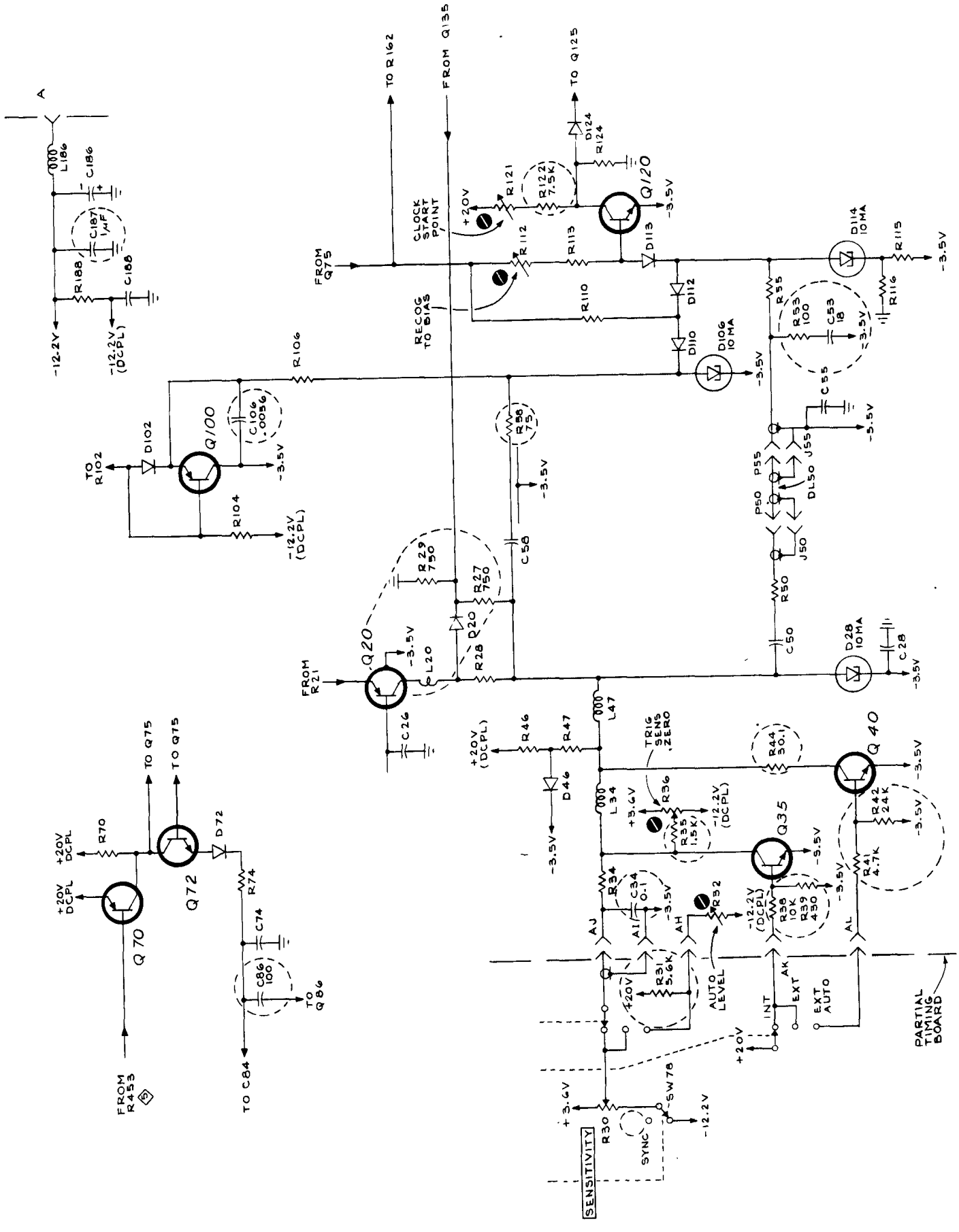
CHANGE TO:

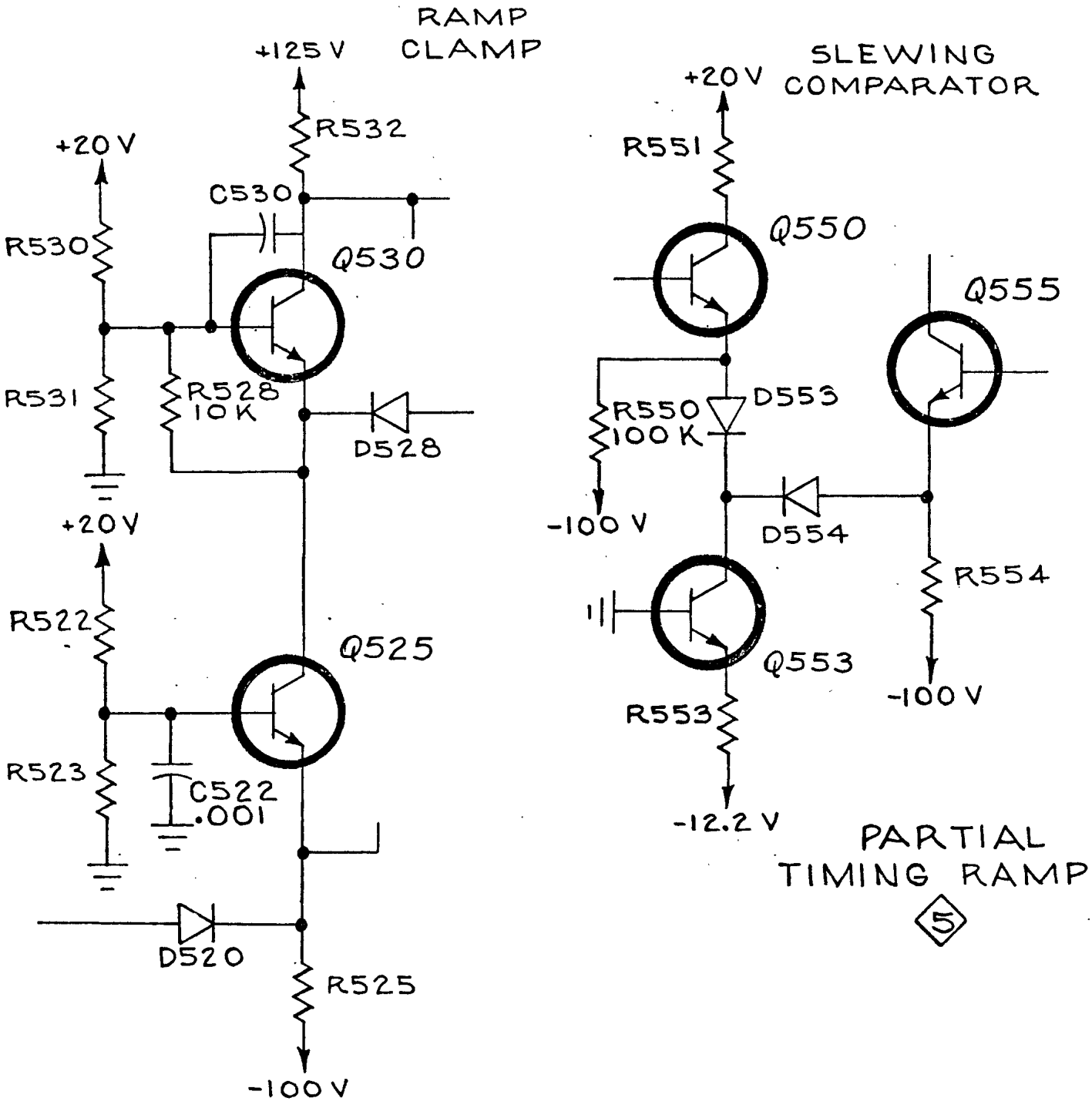
C34	283-0023-00	.1 µF	Cer	10 V	
C50	283-0094-00	27 pF	Cer	200 V	5%
C58	283-0094-00	27 pF	Cer	200 V	5%
C86	283-0128-00	100 pF	Cer	500 V	10%
C106	281-0591-00	5600 pF	Cer	200 V	
C625	281-0591-00	5600 pF	Cer	200 V	
D28/R44	*153-0042-00	Tunnel diode and resistor pair			
DL50	179-1302-00	30 inch (3.75 ns) Delay Line			
Q20	151-0202-00	Silicon	2N4261		
Q40	151-0190-01	Silicon	2N3904		
Q72	151-0190-01	Silicon	2N3904		
Q500	151-0190-01	Silicon	2N3904		
Q550	151-0190-01	Silicon	2N3904		
Q555	151-0190-01	Silicon	2N3904		
R29	317-0751-00	750 Ω	1/8 W		5%
R35	315-0152-00	1.5 kΩ	1/4 W		5%
R38	315-0103-00	10 kΩ	1/4 W		5%
R39	315-0431-00	430 Ω	1/4 W		5%
R41	315-0472-00	4.7 kΩ	1/4 W		5%
R42	315-0243-00	24 kΩ	1/4 W		5%
R44	321-0047-00	30.1 Ω	1/8 W	Prec	1%
R58	315-0750-00	75 Ω	1/4 W		5%
R122	321-0277-00	7.5 kΩ	1/8 W	Prec	1%

ADD:

C53	283-0159-00	18 pF	Cer	50 V	
C187	283-0059-00	1 µF	Cer	25 V	
C522	283-0078-00	0.001 µF	Cer	500 V	
D20	152-0322-00	Silicon	Tek Spec		
L20	276-0507-00	Ferramic Suppressor			
R27	317-0751-00	750 Ω	1/8 W		5%
R31	315-0562-00	5.6 kΩ	1/4 W		5%
R53	317-0101-00	100 Ω	1/8 W		5%
R402	315-0152-00	1.5 kΩ	1/4 W		5%
R406	315-0152-00	1.5 kΩ	1/4 W		5%
R528	317-0103-00	10 kΩ	1/8 W		5%
R550	315-0104-00	100 kΩ	1/4 W		5%

SCHEMATIC CORRECTION




RAMP CLAMP
+125 V
R532
+20 V
C530
R530
Q530
R531
R528 10 K
D528
+20 V
R522
Q525
R523
C522 .001
D520
R525
-100 V
SLEWING COMPARATOR
+20 V
R551
Q550
Q555
R550 100 K
D553
-100 V
D554
R554
Q553
R553
-100 V
-12.2 V
PARTIAL TIMING RAMP
5