INSTRUCTION MANUAL

TYPE 3T77 SAMPLING SWEEP UNIT

Tektronix, Inc.
S.W. Millikan Way • P. O. Box 500 • Beaverton, Oregon • Phone MI 4-0161 • Cables: Tektronix

070-333

763


TYPE 3T77 SAMPLING SWEEP
POSITION
VARIABLE
TIME/DIV.
GAIN ADJ.
μSEC
nSEC
.1
.2
.5
1
2
5
10
20
50
100
CALIB.
UNCAL.
HORIZ.
MAG.
X10
X1
DOTS
PER DIV.
10
100
DELAY
TRIGGER
SENSITIVITY
MANUAL SCAN
OR EXT. ATTEN.
SWEEP MODE
MANUAL
NORMAL
SINGLE
DISPLAY
RESET
RECOVERY TIME
INT.
EXT.
+ EXT.
SWEEP
INPUT
SWEEP
OUTPUT
1V/DIV.
(10 KΩ)
TRIG.
OUT.
EXT.
INPUT
SERIAL
TEKTRONIX, INC.
PORTLAND, OREGON, U.S.A.

SECTION 1
CHARACTERISTICS

General Information

The Type 3T77 Sampling Sweep Plug-In Unit is designed for use with all Tektronix Type 560-Series Oscilloscopes except the Type 560 and Type 565. The Type 3T77 is equipped to drive a digital unit in the Type 567 Readout Oscilloscope.

The Type 3T77 must be inserted into the right-hand plug-in compartment of the oscilloscope and a vertical sampling plug-in unit (such as the Type 3S76) must be inserted into the left-hand plug-in compartment to complete the composite sampling system.

Equivalent Sweep Rates

Variable in fifteen steps from 0.2 nsec/div to 10 μsec/div (0.02 nsec/div to 1 μsec/div with HORIZ. MAG. switch at X10). Accuracy typically within 1%, and in all cases within 3% of the indicated sweep rate with HORIZ. MAG. switch at X1. With HORIZ. MAG. switch at X10, accuracy is within 5%. The sweep rate at any given setting of the TIME/DIV. switch can be increased by about 3 times with the VARIABLE control.

Samples Per Division

10/div or 100/div.

External Triggering

Pulse Repetition Rate: Up to 3×10^8 pulses/second (300 megacycles). Trigger circuitry counts down to a maximum sampling rate of about 100 kilocycles/second.

Minimum Pulse Amplitude and Width: 10 millivolts, peak-to-peak, with at least a 2-nanosecond width. With larger pulse amplitudes (up to 800 millivolts) minimum pulse width decreases. Overload damage occurs at 5 volts and above.

Sinusoidal Frequency Range: 100 kilocycles to 300 megacycles; 10 to 800 millivolts amplitude.

Low Frequency Response (to trigger pulses): 300 kilocycles (3-db down point).

Jitter: 50 picoseconds or 0.001× fast ramp duration, whichever is greater (for 50-millivolt amplitude, 2-nanosecond width pulses with a repetition rate less than 10 megacycles). Jitter increases as pulse amplitude and/or width decreases when repetition rates exceed 10 megacycles.

Internal Triggering

Same characteristics as External Triggering but modified by vertical plug-in unit used. When used with the Type 3S76, all characteristics are the same except five times more amplitude is required at the Type 3S76 INPUT A or INPUT B connectors and the low-frequency response is 3-db down at 450 kilocycles.

External Sweep Input

Sensitivity: Adjustable from 5 to 25 volts per horizontal division (50 volts required for a full 10-division display, 250 volts maximum).

Input Resistance: 28 to 100 kilohms, depending on setting of EXT. ATTEN. control.

Sweep Output

Amplitude: 1 volt/div from a source impedance of 10 kilohms.

Delay

Variable through 100 nsec.

Mechanical

Construction: Aluminum alloy chassis.

Finish: Photo-etched, anodized front panel.

Weight: 5 pounds.

Accessories Supplied With the Type 3T77

	Tektronix Part Number
2 50Ω, 10-nsec cables RG-58/AU with General Radio connectors.	(017-501)
1 Adapter, BNC-to-GR	(017-025)
1 Adapter, male BNC-to-female UHF	(103-032)
2 Attenuators, 10XT, 50 Ω with GR connectors	(017-044)
2 Instruction manuals	(070-333)

SECTION 4

CIRCUIT DESCRIPTION

General Operation

The Type 3T77 contains four main circuits: the Trigger and Holdoff circuit, the Fast Ramp circuit, the Staircase Generator circuit, and the Horizontal Amplifier.

The Type 3T77 provides horizontal deflection potentials to the crt. In addition, it controls the exact time that the vertical plug-in unit samples the applied signal. The following discussion describes the basic technique involved.

Basic Sampling Technique

To recreate a repetitive signal using the sampling technique, samples must be taken over the portion of the signal you wish to display. When sampling a fixed point on a waveform, a trigger circuit trips the sampling gate in the vertical system and allows a sample of the incoming signal to pass through. A block diagram of this system appears in Fig. 4-1.

In actual practice, the system shown in Fig. 4-1 could not take a sample on the leading edge of the signal because of the finite time delay in the Trigger circuit. Therefore, if a delay is introduced in the input circuit of the vertical system, the Trigger circuit will have time to open the sampling gate in the vertical system just as the leading edge of the incoming signal reaches the gate. Fig. 4-2 shows a block diagram with a delay circuit added in the vertical system.

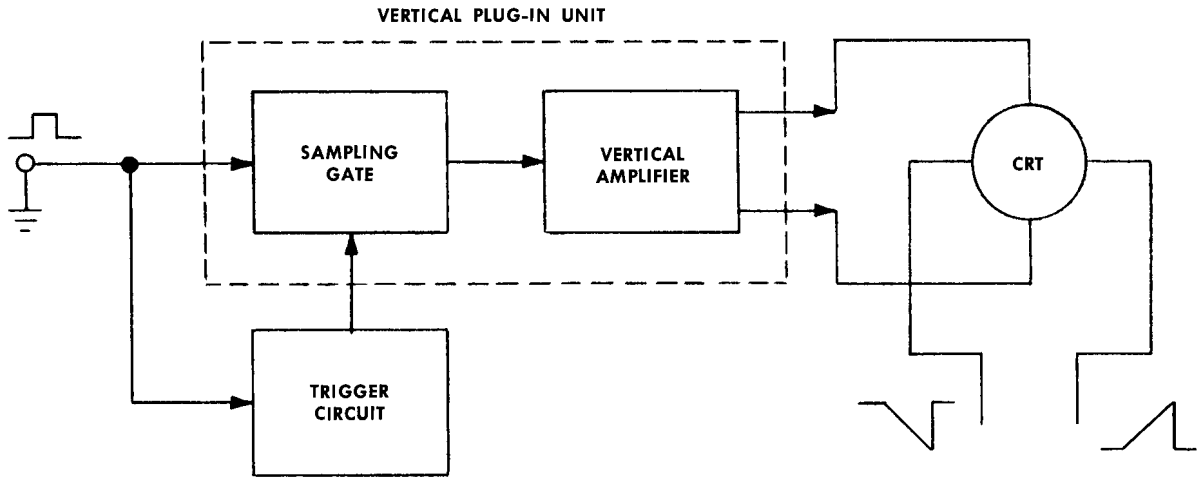


Fig. 4-1. Circuit required for sampling at a fixed point on an input signal.

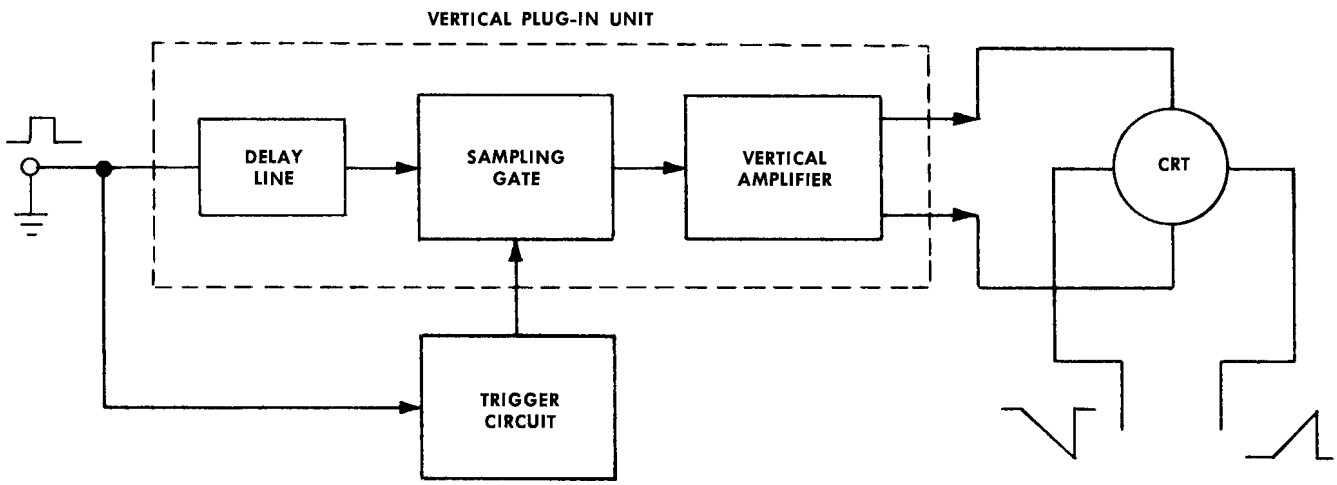


Fig. 4-2. Delay line added to the circuit of Fig. 4-1 so sampling takes place on the leading edge of the input signal.

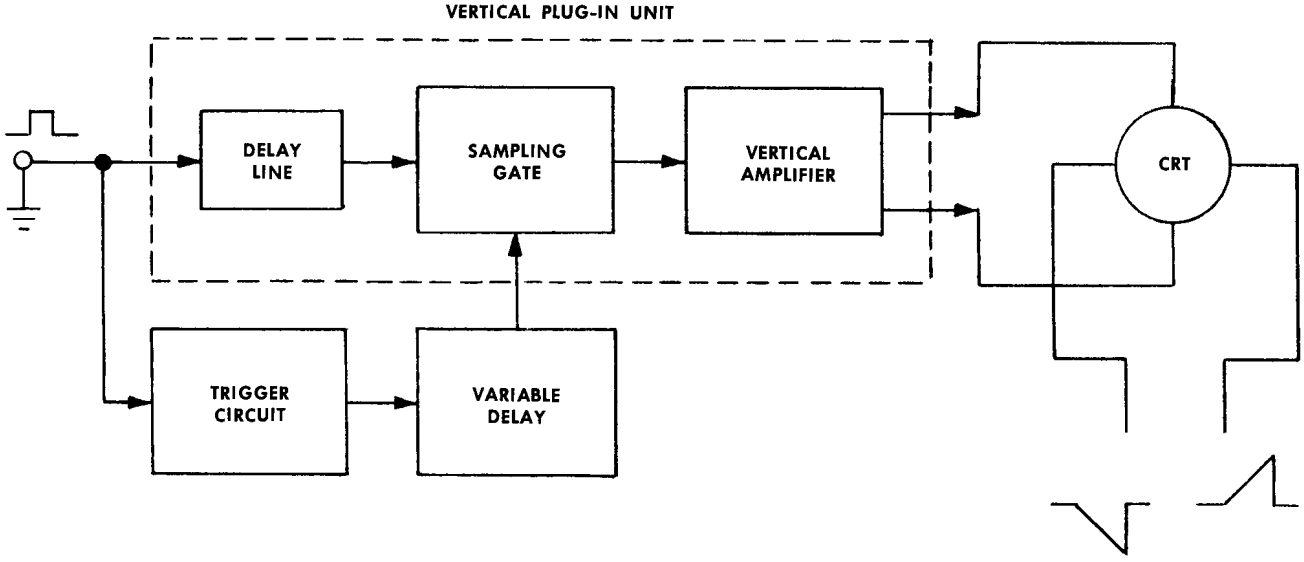


Fig. 4-3. Variable delay circuit added so sampling takes place at various points on the input signal.

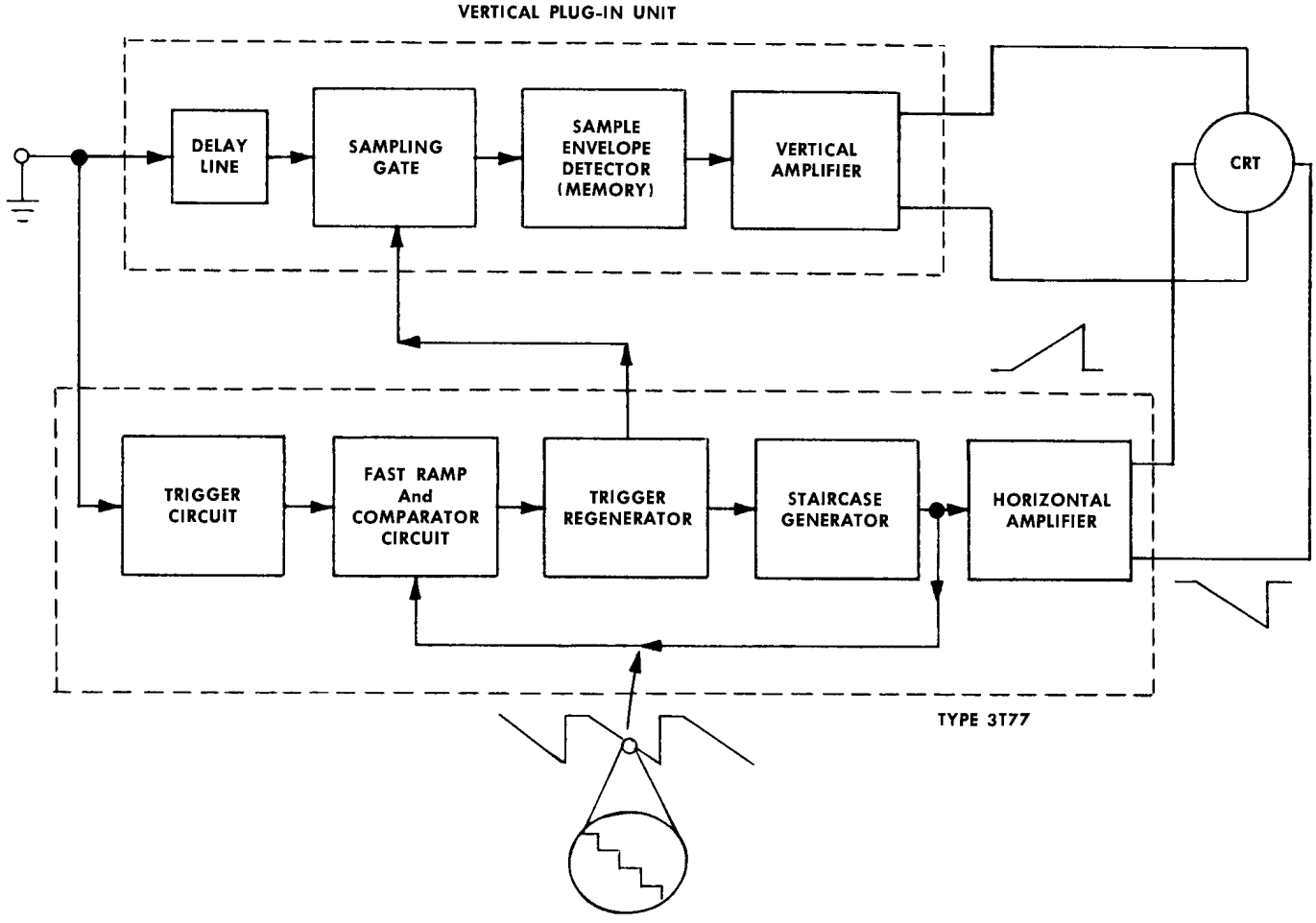


Fig. 4-4. Complete block diagram of the sampling system.

Although the system represented in Fig. 4-2 could sample an incoming signal at one point on its leading edge, it could not sample the signal over its entire duration. Instead, it would consistently sample the same point on the signal each time it was triggered.

In order to sample over the entire duration of the signal, a varying delay must be introduced so the samples can be taken at various points on the signal. This system would resemble Fig. 4-3. The variable delay we introduce must produce fairly long delays (up to 0.1 millisecond) and must continuously vary the amount of delay.

The variable delay circuit used in the Type 3T77 produces an electronic delay by a method called "trigger slewing". The trigger circuit initiates a fast-rising voltage ramp when triggered by the incoming signal. This ramp voltage must fall to the slewing voltage level of the comparator, then a new pulse (slewed trigger) is generated to operate the sampling gate. How long the slewed trigger is delayed depends upon the rate of the fast ramp and the level of the slewing voltage. The slewing voltage, and thus the time delay, is directly proportional to horizontal crt deflection. Horizontal deflection voltage and slewing voltage may be obtained manually but are normally obtained from the Staircase Generator, which automatically increases the voltage after each sample is taken. Thus, the sampling gate will open slightly later and the incoming signal will be sampled at a different point. Fig. 4-4 shows the improved sampling system with the comparator circuit replacing the variable delay block.

In the discussion of a sampling system the terms "real time" and "equivalent time" are often used. To understand the meanings of these terms, consider the following case: If we recreate a repetitive pulse 50 nanoseconds wide by taking 50 samples (one sample per incoming pulse) the real time between successive samples depends on the repetition rate of the signal. However, by using 50 samples to reconstruct a waveform display, we are, in effect, pretending that all of the samples were taken from a single input pulse. If this were true, the time between samples in the example would be one nanosecond (50 samples along a 50-nanosecond pulse). This is the equivalent time between samples and a 10-division display would have an equivalent rate of 5 nanoseconds per division. Fig. 4-5 illustrates the relationship between real time, equivalent time, and an input signal.

CIRCUIT ANALYSIS

The basic operation of the sampling system is covered previously in this section. This portion of the circuit description contains a detailed discussion of each of the major circuits of the Type 3T77. Refer to the schematics at the rear of the manual as you read through this discussion.

Tunnel Diodes

Since tunnel diodes are used in several circuits of the Type 3T77, their basic operation is discussed here, rather than under the operation of a specific circuit.

Tunnel diodes have low inductance and capacitance, and therefore make good switching devices. Fig. 4-6 shows the voltage-current characteristics of a typical 20-ma tunnel diode. Notice that as the current is increased from zero to the 20-ma point, the terminal voltage increases slowly to about 75 millivolts (the "low-voltage" state). Then suddenly, a further increase in current causes an abrupt switch in terminal voltage to about 500 millivolts (the "high-voltage" state). The current must then be reduced to about 2 ma to switch the tunnel diode from the "high-voltage" state back to the "low-voltage" state.

Trigger and Holdoff Circuit

When the Type 3T77 is waiting to be triggered, tunnel diodes D22 and D42 are in the "low-voltage" state and D25 is in its "high-voltage" state. With D22 in its low state, there is about +50 millivolts on the base of Q24 . . . . not enough to turn it on. Q34 and Q44 are also off.

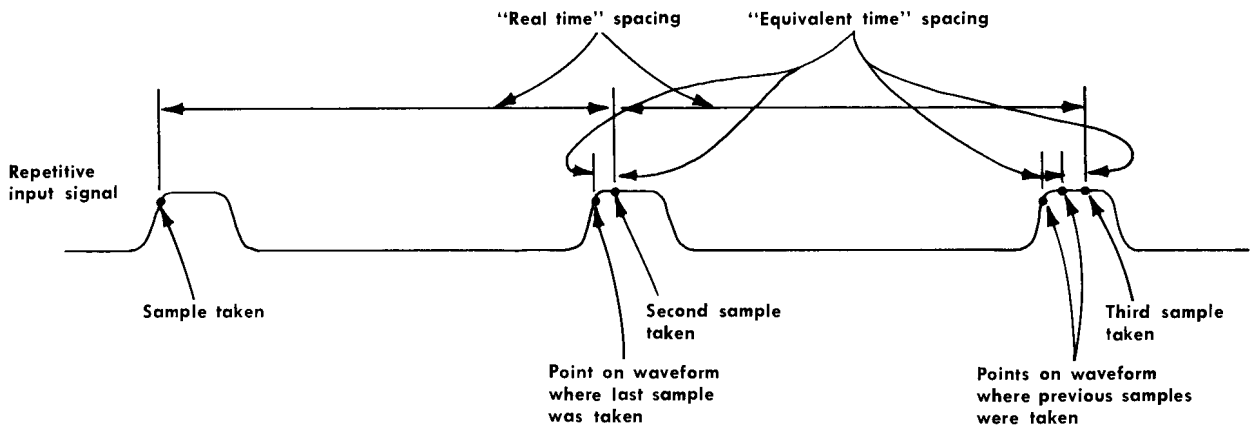


Fig. 4-5. Relationship between real time, equivalent time, and the input signal.

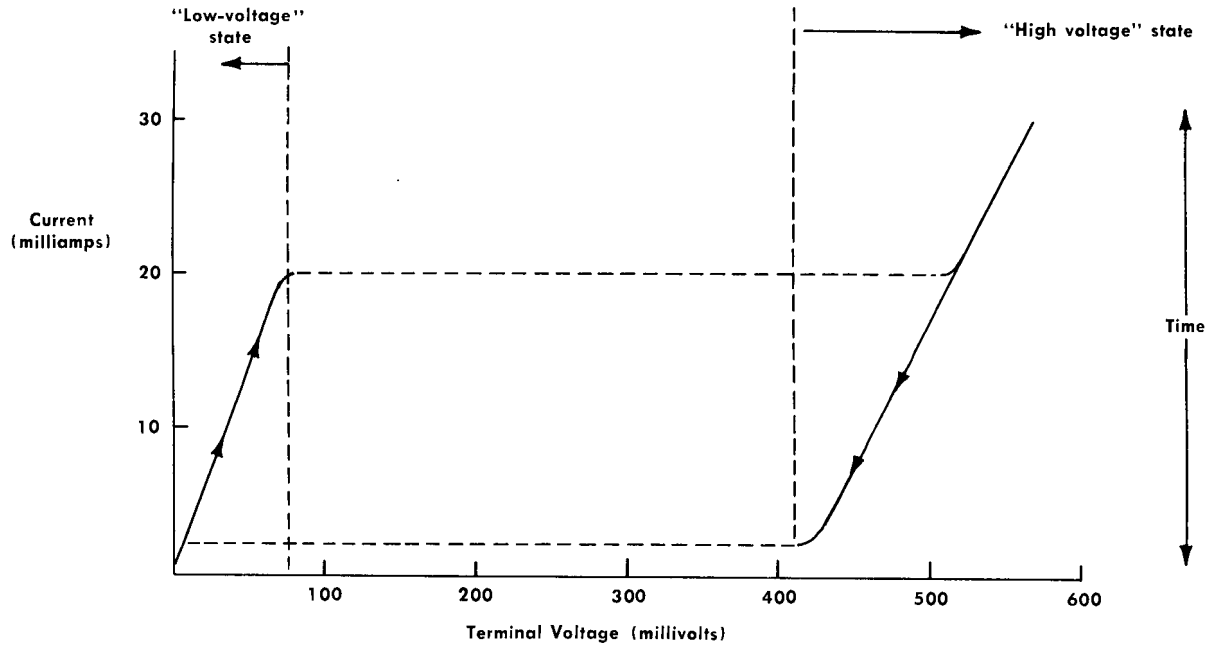


Fig. 4-6. Voltage-current characteristics of a typical 20-ma tunnel diode.

Triggering is initiated by bringing D22 from its low state to its high state. Therefore, a positive-going signal is required from the collector of Q14 to produce a trigger. The size of the positive signal required to switch D22 to its high state is determined by the setting of SENSITIVITY control R19, and TRIG. SENS. RANGE adjustment R21.

A portion of the input signal from the vertical plug-in unit is coupled to Q14 for internal triggering via pin 3 of the interconnecting plug. T5 provides trigger slope selection. Q14 is a grounded-base (non-inverting) amplifier with a current gain of nearly 1.

A portion of the Q14 collector current passes through D22. When the collector current of Q14 passes a certain value set by the SENSITIVITY control, D22 switches to its high state of about +500 millivolts. This positive switching pulse from D22 passes through R40 and C40 to D42 and switches D42 from its low state to its high state. The switching pulse of D42 drives the Fast Ramp circuit.

The positive switching pulse from D22 also passes to the base of Q24 and turns it on, and the collector voltage of Q24 drops toward ground. As a result, D27 turns on and the increased drop across R26 reduces the current through D25 and switches it to its low state. Also, current through D28 increases the voltage drop across R22 and causes D22 to return to its low state. D22 is then held in its low state as long as D25 remains in its low state. Therefore, D25 serves as a trigger holdoff because D22 cannot be triggered until D25 changes states. Q34 and Q44 and associated circuitry hold D25 in its low state for a period determined by the time constant of C30, C31, R31, and RECOVERY TIME control R30. The holdoff time is considerably greater than the amount of equivalent time displayed on the crt. In the fast sweep rates it is greater than 10 microseconds and increases to about 300 microseconds at the slowest sweep rate.

Q24 turns off almost immediately after it is turned on. However, during the time it is turned on, C30 and C31 discharge. Then, when Q24 turns off, C30 and C31 must charge through R30, R31, and Q34. This charging current turns Q34 on and Q34 supplies current to hold D22 and D25 in their low state. Current through Q34 also discharges C34. Charging current through C30 stops when D31 becomes forward biased. This allows Q34 to turn off and Q44 to turn on from the charging of C34 through R34 and the base of Q44. At the same time, Q34 turns off and allows current from R21 and R22 to pass through D22. However, D22 still cannot be triggered since D25 is still in its low state. The current through Q44 holds D25 in its low state until C34 completes its charge. At this point, Q44 will turn off and allow more current to pass through D25 and switch it to its high state. D22 can then be triggered again.

With R19 set to maximum resistance (fully clockwise) the circuit free-runs. In this case, D22 switches to its high state each time D25 switches to its high state following the holdoff period.

Fast Ramp

This circuit generates a fast-ramp waveform, compares it with an existing slow-ramp voltage from the Staircase Generator, and produces a positive-polarity slewed pulse. The fast-ramp waveform is developed across Ramp Slope Capacitor C88. Comparison with the slow-ramp waveform takes place at Q93. The slewed pulse is generated at D93 and appears, inverted and amplified, at the collector of Q94. The positive trigger from the Trigger and Holdoff circuit initiates the action of the Fast Ramp circuit. It is coupled through Q74 whose collector current switches D74 from its quiescent high state to its low state. The resulting fast positive step turns Q84 off. Current from constant-

current tube V61 is now diverted into the Ramp Slope Capacitor. Charging of this capacitor carries the emitter of Q93 negative.

The Staircase Generator and the DELAY control set the output voltage level of the Slow Ramp Inverter, which, in turn, sets the voltage on the base of Q93. (Slow Ramp is another name for the staircase waveform.)

When the fast ramp starts, the base of Q93 is negative with respect to its emitter, so Q93 is not conducting. It remains cut off until the fast-ramp voltage at the emitter falls below the base voltage of Q93. Q93 then turns on, passing current through D93 which is quiescently in its low state.

When this happens, D93 switches to its high state, developing a negative step. This negative output is stepped up through T95 and is applied to the base of Q94. The resulting positive step at the collector of Q94 is the slewed pulse. It is differentiated through C97 and applied through pin 18 of the interconnecting plug to the vertical plug-in unit to start the sampling process, and is passed through R99 to the Staircase Generator to advance the staircase one step.

The negative step at the cathode of D93 is also coupled back through D75 to switch D74 to its high state. This turns Q84 on again, ends the fast ramp, and discharges the Ramp Slope Capacitor.

With the load impedance made up basically of R95 and the inductance of T95, D93 is monostable. Therefore, it will automatically reset itself to its low state before the next fast ramp is generated.

The output of the Staircase Generator is applied to the top of R51. At this point, this is about a 50-volt positive-going staircase of 100 or 1000 steps. Thus, each step is either 0.5 or 0.05 volt in amplitude. Q63 and Q64 form an inverting amplifier with 20 k feedback resistance. The gain of this stage, from the input of R53 to the output of R90, ranges from 0.2 to 0.004 depending upon the value of R53 selected by the TIME/DIV. switch. R54 maintains a constant load on R51 and R52. The steps at the Q93 base are negative-going steps of 0.1-volt to 0.2-millivolt amplitude. The smaller the steps, the less the equivalent time between samples, and the faster the equivalent sweep rate.

The CALIB. position of R51 (counterclockwise position of the VARIABLE control) is with the wiper at the top of R51. Thus, as you move the control away from CALIB., you decrease the size of the steps at the base of Q93, decrease the equivalent time between samples, and consequently increase the equivalent rate.

The slope of the fast ramp is changed between ranges by changing the size of the Ramp Slope Capacitor. The steeper the ramp, the less difference there will be in the time required for the ramp to reach successive levels of the staircase at Q93. Thus, the equivalent time per division is controlled by varying both the size of the steps at the base of Q93 and the slope of the fast ramp at the emitter of Q93.

Staircase Generator

This circuit develops either a 0.5-volt per step or 0.05-volt per step positive-going staircase signal of about 50 volts amplitude and applies it to the Horizontal Amplifier and to the Slow Ramp Inverter circuit. It also develops a sweep gate voltage, a positive gate lasting for the duration of one complete staircase signal.

First, consider the Staircase Generator in its quiescent condition, when no staircase is being generated. Assume the SWEEP MODE switch is in the NORMAL position. Both Q135 and Q145 are off, so Disconnect Diodes D152 and D153 are conducting and the Miller Tube V161 is on. D125 is in its low state.

The positive slewed pulse fires the Miller-Stepping Blocking Oscillator Q110. The collector of Q110 is held constant by C111 and C110, and the base and emitter of Q110 move with current. The resulting negative swing at the emitter momentarily increases current through tunnel diode D125 and switches it to its high state. This turns on Q124. The resulting negative swing at the collector of Q124 passes through C127 and R127 to the base of Q135. Q135 turns on, and the resulting positive swing at its collector turns Q145 on. The negative swing at the collector of Q145 back biases the Disconnect Diodes releasing the Miller-Capacitor C160 so it can be charged. Conduction through Q145 also holds Q135 on through R140, so both transistors remain on during the entire staircase.

At the same time, the negative gating voltage at the collector of Q145 is inverted and amplified by V194A and is applied to the crt unblanking deflection plate to unblank the crt.

The negative-going voltage step at the Miller-Stepping Blocking Oscillator (emitter of Q110) also transfers a charge from Miller-Stepping Capacitors C156 or C158 through D160 to C160. This raises the output level of the Miller Integrator one step. The positive-going trailing edge of the Miller-Stepping Blocking Oscillator then recharges the selected Miller-Stepping Capacitor through D161 and C162 in preparation for the next pulse. The size of the charge, and therefore the size of the steps, is determined by the size of the Miller-Stepping Capacitors and the output voltage swing from the Miller-Stepping Blocking Oscillator.

Each successive slewed pulse causes an identical charge to transfer from the selected Miller-Stepping Capacitor to C160, and thus raise the Miller Integrator output in identical increments. The output of the Miller Integrator, then, is a positive staircase that goes to the Horizontal Amplifier and to the Fast Ramp Generator.

D177 couples the output voltage of the Miller Integrator through V173A to the top of the V161 plate load resistor R172. Thus, as the plate voltage of V161 changes, the voltage at the top of its plate load resistor (R172) changes a like amount and the current through R172 remains constant. The gain of the Miller Integrator approaches the amplification factor of V161, and the circuit operates with very small changes in grid voltage. Cathode follower V173B provides large output current capability. D178 changes the dc level of the Miller output from +75 volts to about zero volts.

The STAIRCASE DC LEVEL adjustment R181 sets the start of the staircase to exactly zero volts.

When the staircase voltage reaches about +50 volts it pulls the base of Q135 positive and turns off both transistors in the Staircase-Gating Multivibrator. This turns on the

Disconnect Diodes and discharges C160 which resets the Miller Integrator.

D145 disconnects from the staircase during reset while C145 holds the base of Q135 positive for sufficient time to allow complete recovery of the Miller Integrator.

In the SINGLE DISPLAY position of the SWEEP MODE switch, the cathode of tunnel diode D125 is connected through 3.9 k to —12.2 volts. This provides about 3 ma through the tunnel diode so it may be in either its high state or its low state. Assume that it is in its high state.

This puts about —0.5 volt at the D125 cathode, and Q124 will be turned on. This draws the collector of Q124 to ground and the negative blocking oscillator pulses arriving at its emitter will have no effect. Thus, with D125 in its high state, the Staircase Generator is locked out and cannot be started.

When the reset button is pushed, current to D125 is momentarily interrupted by the positive pulse at the top of R125, and D125 switches to its low state. Once the reset pulse has passed, the current through D125 is again 3 ma, but D125 remains in its low state. This cuts off Q124, and the next pulse from the blocking oscillator Q110 will pass through Q124 to start the staircase runup. The same blocking oscillator pulse will also reset D125 to its high state so the Staircase Generator cannot be started again without a reset pulse. The result is a single staircase.

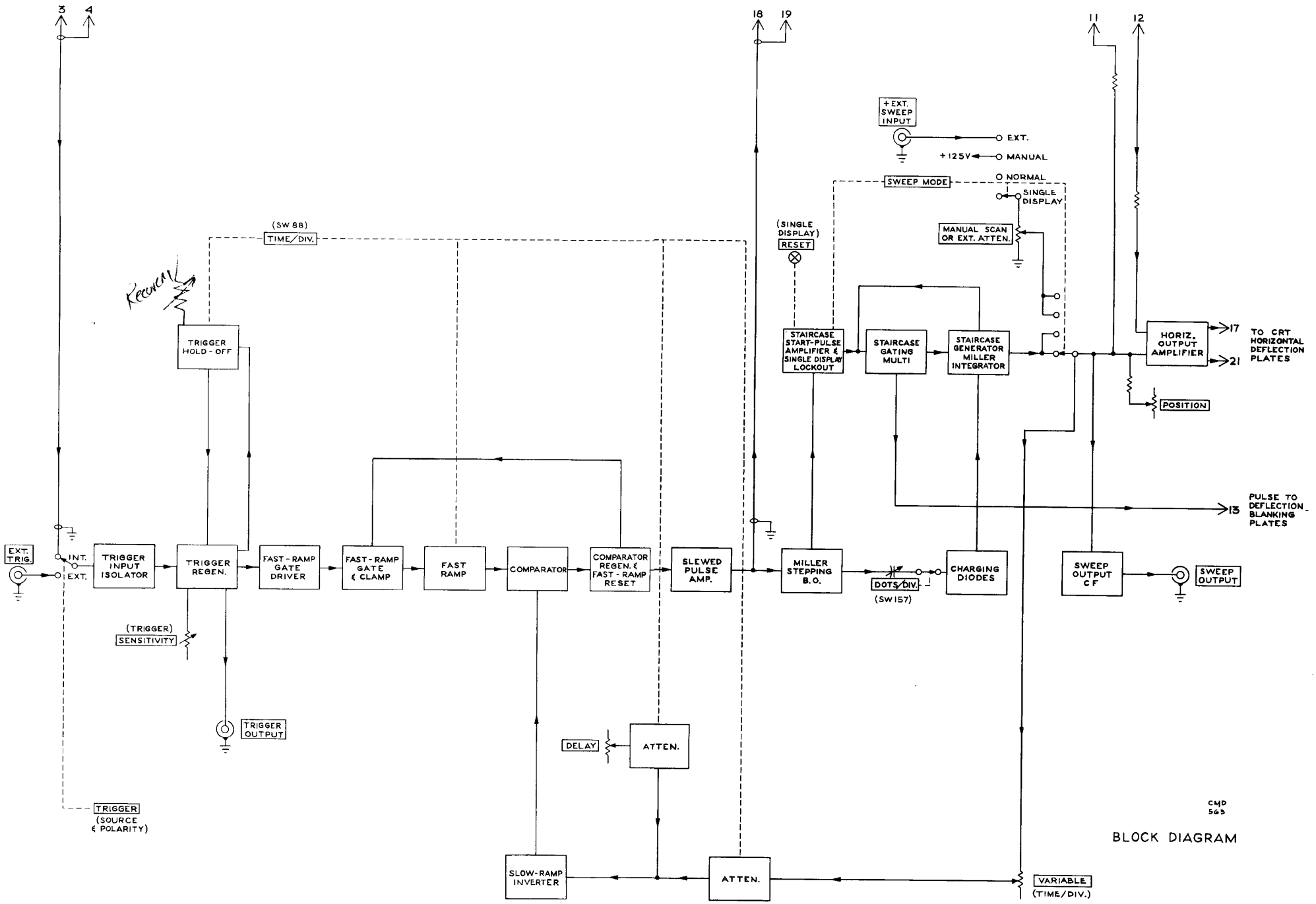
The +EXT. SWEEP INPUT and MANUAL positions of the SWEEP MODE switch disable the Miller-Stepping Blocking Oscillator by removing collector voltage from Q110. They also turn off Q135 and Q145, thereby turning on the Disconnect Diodes to prevent the Miller Integrator from running up.

The MANUAL SCAN control supplies voltage to RC filter R304-C304 (Horizontal Amplifier Schematic) for smoothing the scan.

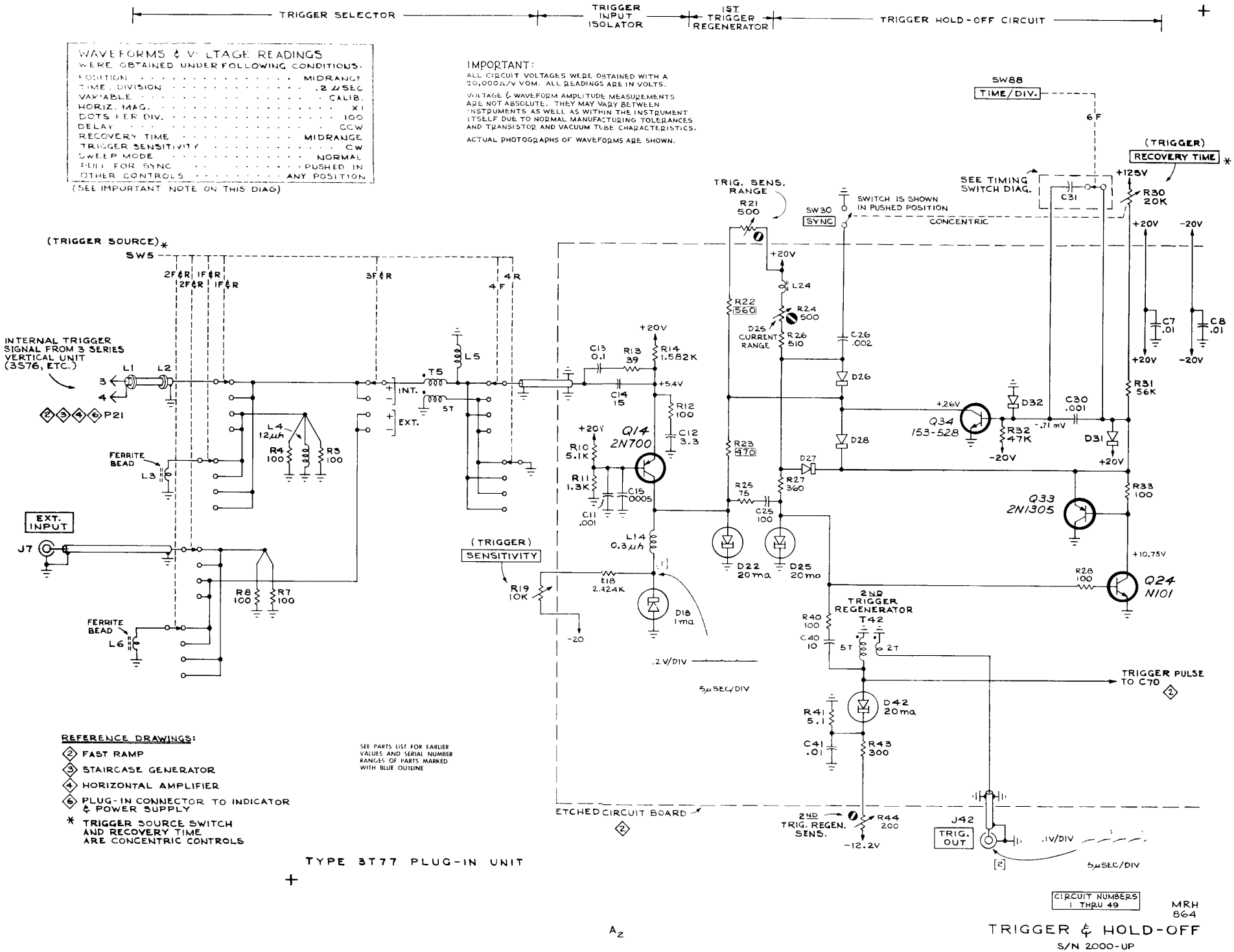
Horizontal Amplifier

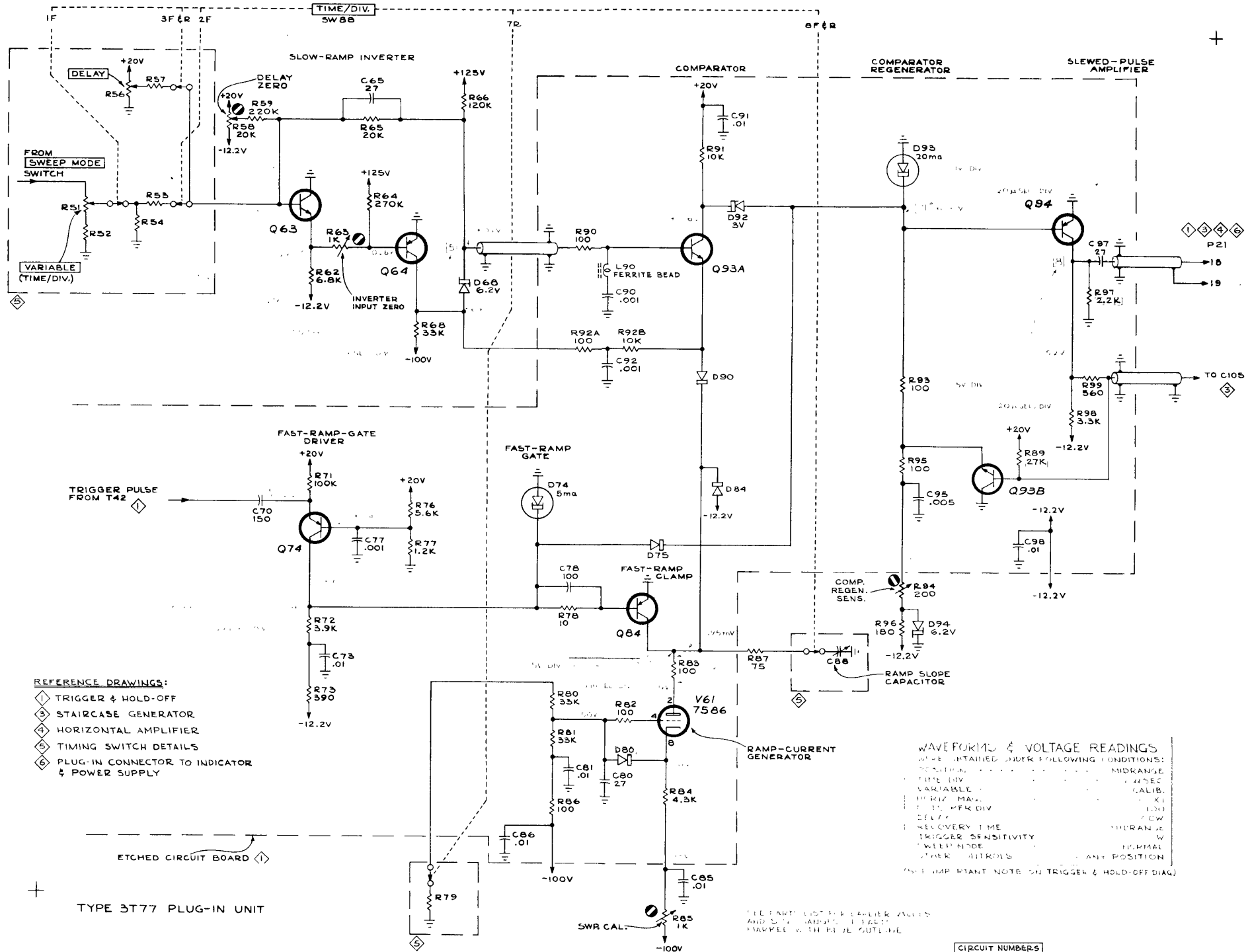
With the SWEEP MODE switch set to NORMAL, the staircase passes through R319 to the base of Q334. Q334 and Q333 form a feedback amplifier through R330. The output of this amplifier is coupled either directly, or through a 10X divider, to paraphase amplifier V364-V354, and then through cathode followers V373A-V373B to the crt deflection plates via pins 17 and 21 of the interconnecting plug.

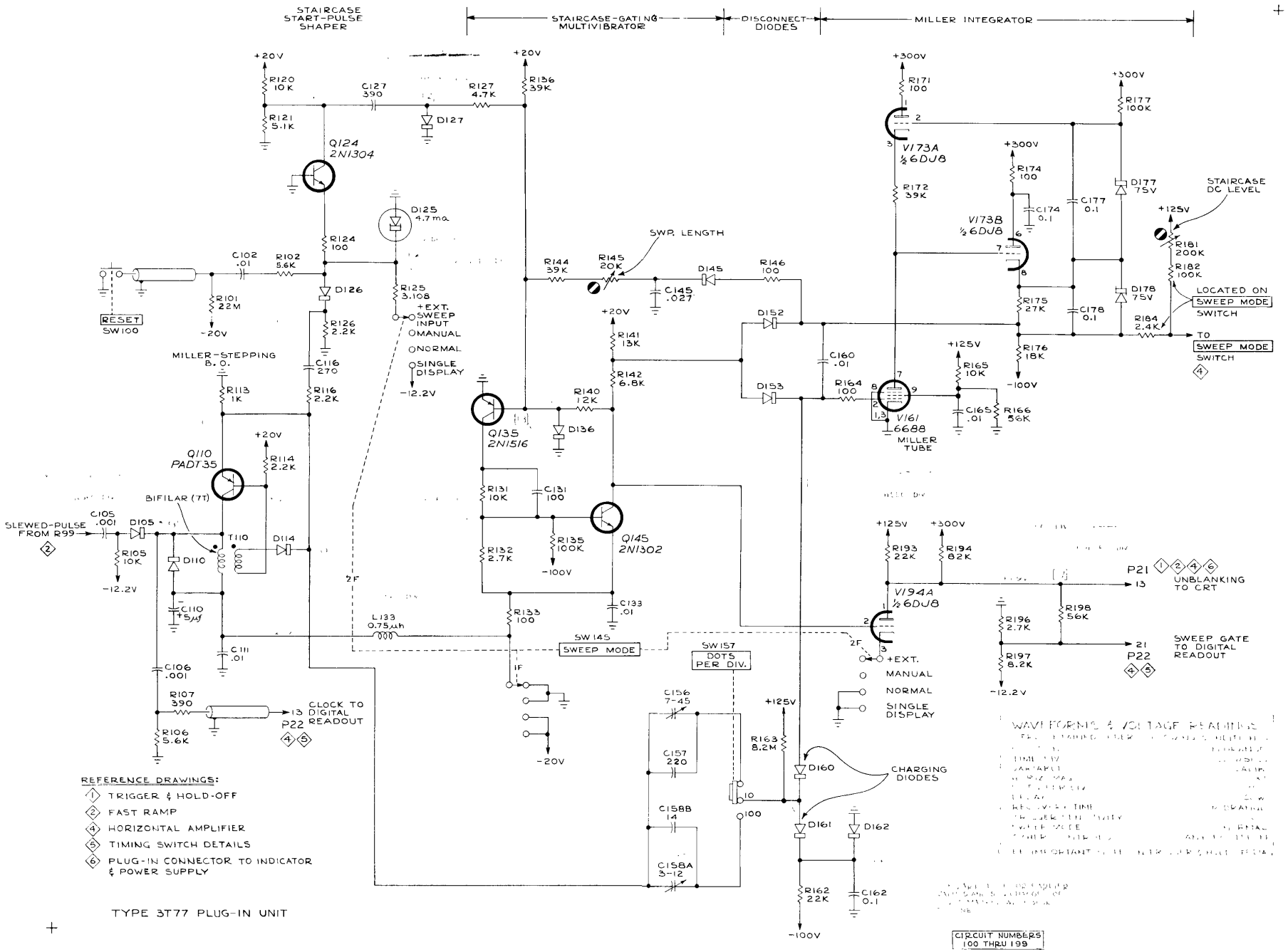
Note the leads at pins 11 and 12 of the interconnecting plug. Normally D327 is conducting 1 ma through R328, and pin 12 of the interconnecting plug is grounded. When the vertical plug-in unit is set for X-Y operation (Vertical Mode switch in A VERT. B. HORIZ. on Type 3S76), pin 11 is switched from —100 volts through 47 k to +300 volts through 47 k (in the vertical plug-in unit). This cuts off D327 and drives Q334 into saturation so the staircase signal cannot get through. At the same time, pin 12 is switched from ground to the output of channel B in the vertical plug-in unit. The channel B signal is then applied to the horizontal deflection plates rather than the staircase waveform. Meanwhile, the channel A signal is coupled to the vertical deflection plates. This produces X-Y operation.

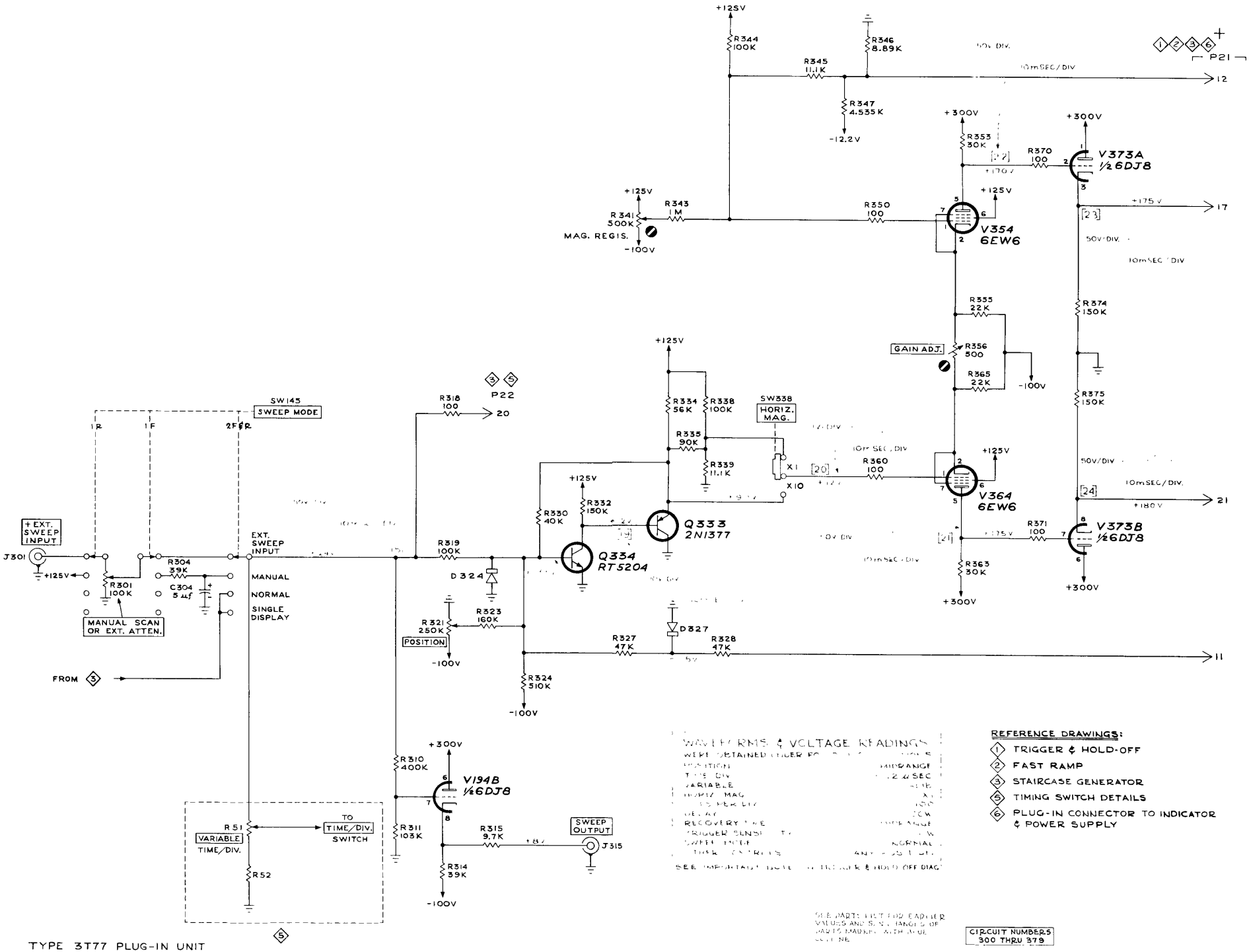


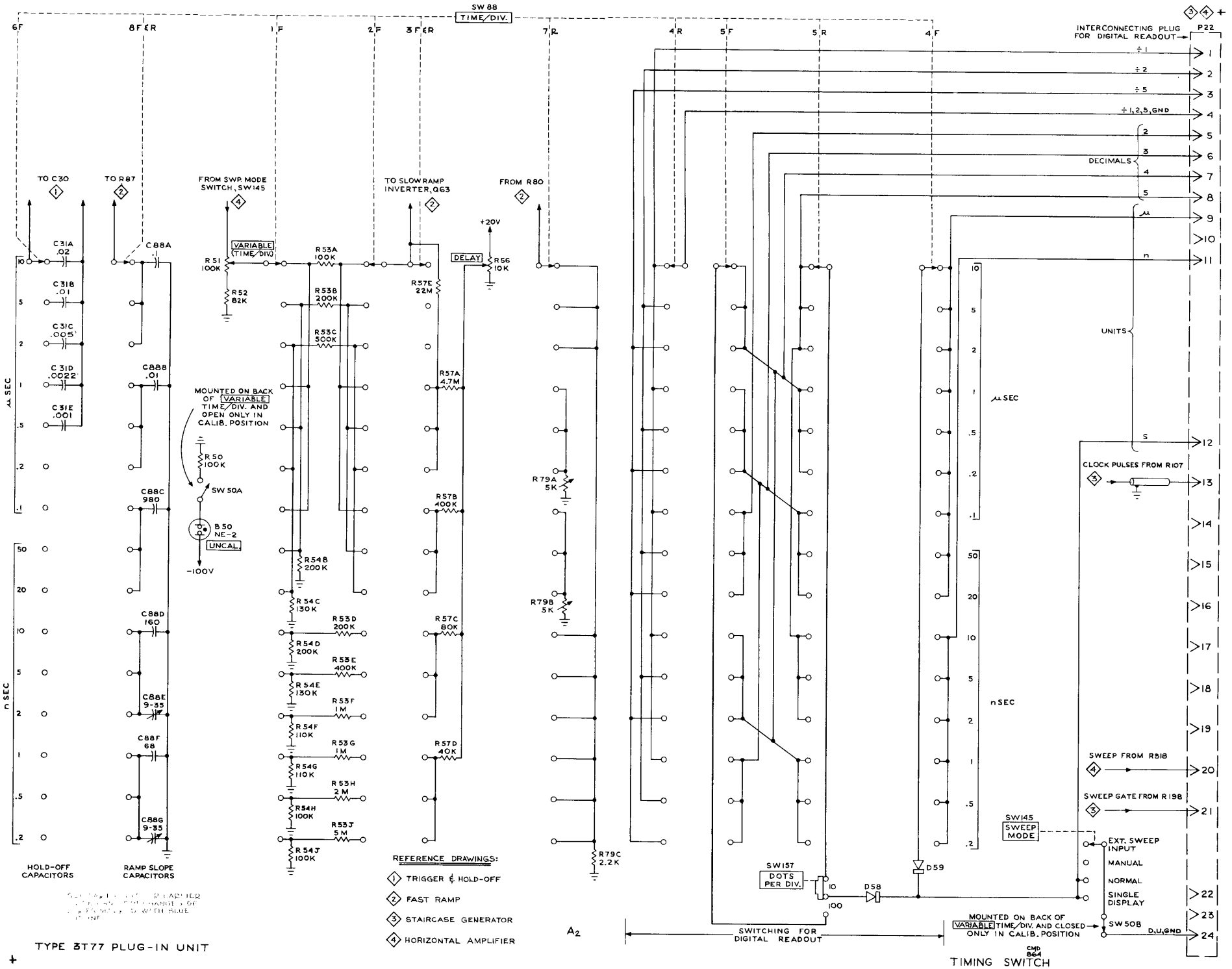
TYPE 3T77 SAMPLING SWEEP

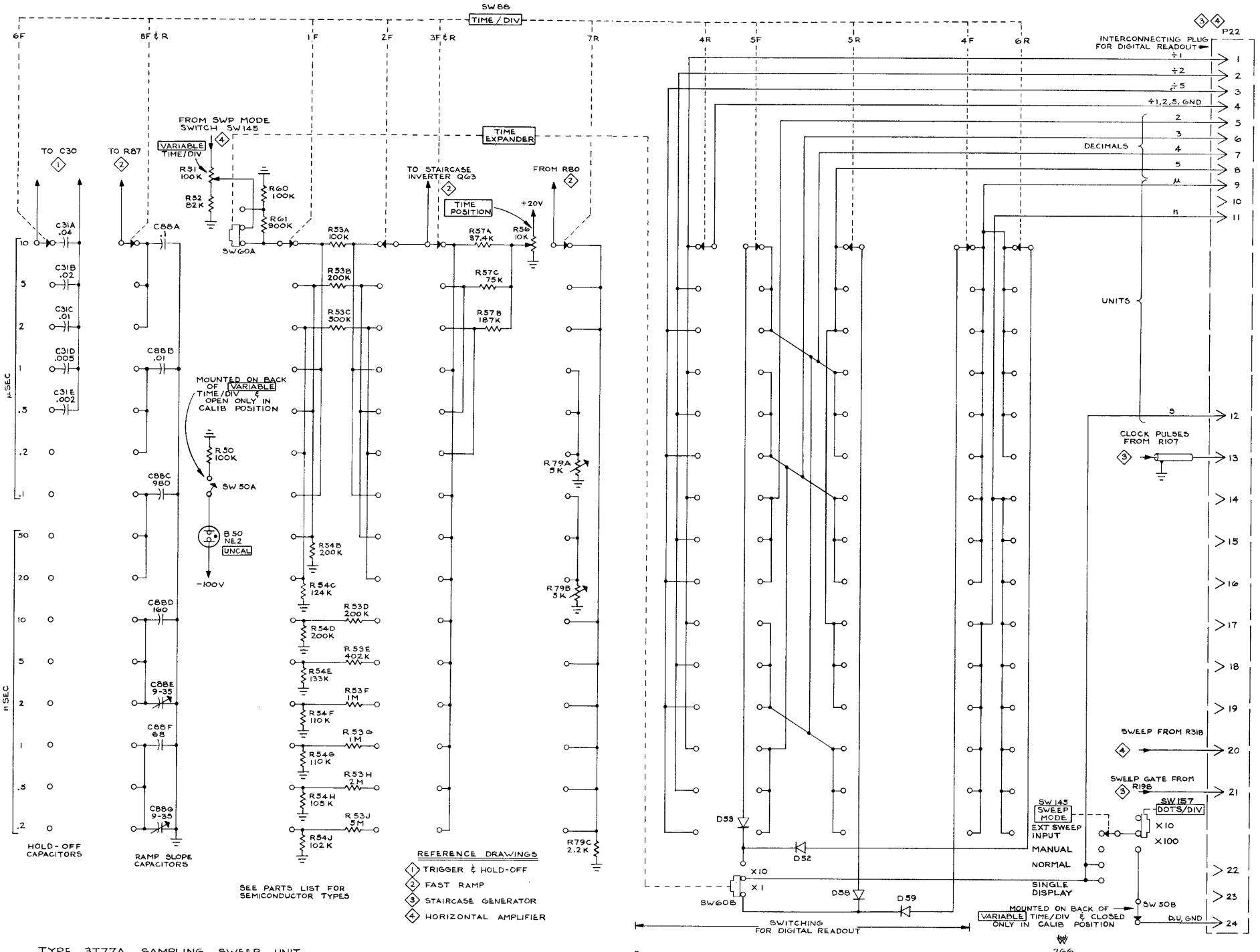

TRIGGER SELECTOR
TRIGGER INPUT ISOLATOR
1ST TRIGGER REGENERATOR
TRIGGER HOLD-OFF CIRCUIT
WAVEFORMS & VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS.
POSITION ... MIDRANGE
TIME / DIVISION ... .2 μSEC
VARIABLE ... CALIB.
HORIZ. MAG. ... X1
DOTS PER DIV. ... 100
DELAY ... CCW
RECOVERY TIME ... MIDRANGE
TRIGGER SENSITIVITY ... CW
SWEEP MODE ... NORMAL
FULL FOR SYNC ... PUSHED IN
OTHER CONTROLS ... ANY POSITION
(SEE IMPORTANT NOTE ON THIS DIAG)
IMPORTANT:
ALL CIRCUIT VOLTAGES WERE OBTAINED WITH A 20,000Ω/V VOM. ALL READINGS ARE IN VOLTS.
VOLTAGE & WAVEFORM AMPLITUDE MEASUREMENTS ARE NOT ABSOLUTE. THEY MAY VARY BETWEEN INSTRUMENTS AS WELL AS WITHIN THE INSTRUMENT ITSELF DUE TO NORMAL MANUFACTURING TOLERANCES AND TRANSISTOR AND VACUUM TUBE CHARACTERISTICS.
ACTUAL PHOTOGRAPHS OF WAVEFORMS ARE SHOWN.
SW88 TIME/DIV.
6F
(TRIGGER) RECOVERY TIME *
SEE TIMING SWITCH DIAG.
C31
+125V
R30 20K
SW30 SYNC
SWITCH IS SHOWN IN PUSHED POSITION
CONCENTRIC
TRIG. SENS. RANGE
R21 500
(TRIGGER SOURCE) *
SW5
2F&R 1F&R 2F&R 1F&R
3F&R
4F 4R
INTERNAL TRIGGER SIGNAL FROM 3 SERIES VERTICAL UNIT (3S76, ETC.)
L1 L2
3
4
2 3 4 6 P21
T5
L5
INT.
EXT.
5T
L4 12μh
R4 100
R3 100
FERRITE BEAD
L3
EXT. INPUT
J7
R8 100
R7 100
FERRITE BEAD
L6
C13 0.1
R13 39
R14 1.582K
+20V
+5.4V
C14 15
R12 100
C12 3.3
Q14 2N700
R10 5.1K
R11 1.3K
C15 0005
C11 .001
L14 0.3μh
(TRIGGER) SENSITIVITY
R19 10K
R18 2.424K
-20
D18 1ma
.2V/DIV
5μSEC/DIV
R22 560
R24 500
L24
D25 CURRENT RANGE
R26 510
C26 .002
D26
D28
R23 470
R25 75
C25 100
R27 360
D27
D22 20ma
D25 20ma
+4.26V
Q34 153-528
D32
C30 .001
-.71 mV
R32 47K
-20V
D31
+20V
R31 56K
+20V -20V
C7 .01
C8 .01
Q33 2N1305
R33 100
+10.75V
R28 100
Q24 N101
2ND TRIGGER REGENERATOR T42
R40 100
C40 10
5T 2T
TRIGGER PULSE TO C70
D42 20ma
R41 5.1
C41 .01
R43 300
ETCHED CIRCUIT BOARD
2ND TRIG. REGEN. SENS.
R44 200
-12.2V
J42 TRIG. OUT
.1V/DIV
5μSEC/DIV
REFERENCE DRAWINGS:
2 FAST RAMP
3 STAIRCASE GENERATOR
4 HORIZONTAL AMPLIFIER
6 PLUG-IN CONNECTOR TO INDICATOR & POWER SUPPLY
* TRIGGER SOURCE SWITCH AND RECOVERY TIME ARE CONCENTRIC CONTROLS
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE
TYPE 3T77 PLUG-IN UNIT
CIRCUIT NUMBERS 1 THRU 49
MRH 864
TRIGGER & HOLD-OFF
S/N 2000-UP
A2


TIME/DIV. SW 88
1F
3F & R
2F
7R
8F & R
SLOW-RAMP INVERTER
COMPARATOR
COMPARATOR REGENERATOR
SLEWED-PULSE AMPLIFIER
DELAY
+20V
R57
R56
DELAY ZERO
R59 220K
R58 20K
-12.2V
C65 27
R65 20K
+125V
R66 120K
FROM SWEEP MODE SWITCH
R51
R52
R53
R54
VARIABLE (TIME/DIV.)
Q63
R63 1K
R64 270K
Q64
R62 6.8K
INVERTER INPUT ZERO
R68 33K
-100V
D68 6.2V
R90 100
L90 FERRITE BEAD
C90 .001
R92A 100
R92B 10K
C92 .001
Q93A
D90
R91 10K
C91 .01
D92 3V
D93 20ma
Q94
C97 27
R97 2.2K
R98 3.3K
R99 560
TO C105
P21
18
19
R93 100
R95 100
C95 .005
Q93B
R89 27K
C98 .01
R84 200
COMP. REGEN. SENS.
R96 180
D94 6.2V
R87 75
C88
RAMP SLOPE CAPACITOR
FAST-RAMP-GATE DRIVER
TRIGGER PULSE FROM T42
C70 150
R71 100K
Q74
C77 .001
R76 5.6K
R77 1.2K
R72 3.9K
C73 .01
R73 390
FAST-RAMP GATE
D74 5ma
D84
D75
FAST-RAMP CLAMP
C78 100
R78 10
Q84
R83 100
V61 7586
R80 33K
R82 100
R81 33K
C81 .01
D80
C80 27
R84 4.3K
R86 100
C86 .01
C85 .01
R85 1K
SWP CAL
R79
ETCHED CIRCUIT BOARD
REFERENCE DRAWINGS:
1 TRIGGER & HOLD-OFF
3 STAIRCASE GENERATOR
4 HORIZONTAL AMPLIFIER
5 TIMING SWITCH DETAILS
6 PLUG-IN CONNECTOR TO INDICATOR & POWER SUPPLY
WAVEFORMS & VOLTAGE READINGS
MIDRANGE
CALIB.
ANY POSITION
NORMAL
TYPE 3T77 PLUG-IN UNIT
CIRCUIT NUMBERS 50 THRU 99
PLM 565
FAST RAMP
S/N 840 - UP
D1


STAIRCASE START-PULSE SHAPER
STAIRCASE-GATING MULTIVIBRATOR
DISCONNECT DIODES
MILLER INTEGRATOR
+20V
R120 10K
R121 5.1K
C127 390
R127 4.7K
R136 39K
D127
Q124 2N1304
D125 4.7 ma
R124 100
C102 .01
R102 5.6K
R101 22M
-20V
RESET SW100
D126
R125 3.108
+EXT. SWEEP INPUT
MANUAL
NORMAL
SINGLE DISPLAY
-12.2V
SWP. LENGTH
R144 39K
R145 20K
C145 .027
D145
R146 100
MILLER-STEPPING B. O.
R113 1K
R116 2.2K
C116 270
R126 2.2K
Q110 PADT35
R114 2.2K
BIFILAR (7T)
SLEWED-PULSE FROM R99
C105 .001
D105
R105 10K
T110
D110
D114
C110 +5 µf
C111 .01
C106 .001
R107 390
R106 5.6K
CLOCK TO 13 DIGITAL P22 READOUT
Q135 2N1516
R140 12K
D136
R141 13K
R142 6.8K
R131 10K
C131 100
R132 2.7K
R135 100K
Q145 2N1302
R133 100
C133 .01
L133 0.75 µh
SW145 SWEEP MODE
SW157 DOTS PER DIV.
C156 7-45
C157 220
C158B 14
C158A 3-12
D152
D153
C160 .01
R164 100
V161 6688 MILLER TUBE
R165 10K
C165 .01
R166 56K
R176 18K
R175 27K
C178 0.1
D178 75V
R184 2.4K
R182 100K
R181 200K
+125V
STAIRCASE DC LEVEL
LOCATED ON SWEEP MODE SWITCH
TO SWEEP MODE SWITCH
+300V
R171 100
V173A ½6DU8
R172 39K
R174 100
C174 0.1
V173B ½6DU8
C177 0.1
R177 100K
D177 75V
R193 22K
R194 82K
V194A ½6DU8
P21 UNBLANKING TO CRT
R196 2.7K
R198 56K
R197 8.2K
SWEEP GATE TO DIGITAL READOUT
P22
+EXT.
MANUAL
NORMAL
SINGLE DISPLAY
R163 8.2M
D160
CHARGING DIODES
D161
D162
R162 22K
C162 0.1
-100V
WAVEFORMS & VOLTAGE READINGS
CIRCUIT NUMBERS 100 THRU 199
PLM 465
STAIRCASE GENERATOR
TYPE 3T77 PLUG-IN UNIT
REFERENCE DRAWINGS:
1 TRIGGER & HOLD-OFF
2 FAST RAMP
4 HORIZONTAL AMPLIFIER
5 TIMING SWITCH DETAILS
6 PLUG-IN CONNECTOR TO INDICATOR & POWER SUPPLY


+125V
R344 100K
R346 8.89K
R345 11.1K
R347 4.535K
-12.2V
10mSEC/DIV
P21
+300V
R353 30K
R370 100
V373A ½6DJ8
+175V
R343 1M
R341 500K
MAG. REGIS.
-100V
R350 100
V354 6EW6
50V/DIV.
R355 22K
R374 150K
GAIN ADJ.
R356 500
R365 22K
R375 150K
SW145
SWEEP MODE
1R
1F
2F&R
R318 100
P22
20
R334 56K
R338 100K
SW338
HORIZ. MAG.
R335 90K
R339 11.1K
X1
X10
R360 100
V364 6EW6
+180V
21
+ EXT. SWEEP INPUT
J301
EXT. SWEEP INPUT
R330 40K
R332 150K
Q333 2N1377
Q334 RT5204
R319 100K
D324
R304 39K
C304 5 μf
R301 100K
MANUAL
NORMAL
SINGLE DISPLAY
MANUAL SCAN OR EXT. ATTEN.
FROM
R321 250K
POSITION
R323 160K
D327
R327 47K
R328 47K
R324 510K
R371 100
V373B ½6DJ8
R363 30K
R310 400K
V194B ½6DJ8
R311 103K
R315 9.7K
SWEEP OUTPUT
J315
R314 39K
R51
VARIABLE TIME/DIV.
TO TIME/DIV. SWITCH
R52
WAVEFORMS & VOLTAGE READINGS
REFERENCE DRAWINGS:
1 TRIGGER & HOLD-OFF
2 FAST RAMP
3 STAIRCASE GENERATOR
5 TIMING SWITCH DETAILS
6 PLUG-IN CONNECTOR TO INDICATOR & POWER SUPPLY
SEE PARTS LIST FOR EARLIER VALUES AND S.N. RANGE OF PARTS MARKED WITH ABOVE SYMBOL
CIRCUIT NUMBERS 300 THRU 379
TYPE 3T77 PLUG-IN UNIT
A1
CMD 563
HORIZONTAL AMPLIFIER


SW 88
TIME/DIV.
6F
8F ER
1F
2F
3F ER
7R
4R
5F
5R
4F
INTERCONNECTING PLUG FOR DIGITAL READOUT
P22
÷1
÷2
÷5
÷1,2,5,GND
DECIMALS
UNITS
μSEC
nSEC
TO C30
TO R87
FROM SWP. MODE SWITCH, SW145
TO SLOW RAMP INVERTER, Q63
FROM R80
+20V
VARIABLE (TIME/DIV.)
DELAY
R51 100K
R52 82K
R53A 100K
R53B 200K
R53C 500K
R53D 200K
R53E 400K
R53F 1M
R53G 1M
R53H 2M
R53J 5M
R54B 200K
R54C 130K
R54D 200K
R54E 130K
R54F 110K
R54G 110K
R54H 100K
R54J 100K
R56 10K
R57A 4.7M
R57B 400K
R57C 80K
R57D 40K
R57E 22M
R79A 5K
R79B 5K
R79C 2.2K
C31A .02
C31B .01
C31C .005
C31D .0022
C31E .001
C88A
C88B .01
C88C 980
C88D 160
C88E 9-35
C88F 68
C88G 9-35
MOUNTED ON BACK OF VARIABLE TIME/DIV. AND OPEN ONLY IN CALIB. POSITION
R50 100K
SW 50A
B50 NE-2
UNCAL.
-100V
HOLD-OFF CAPACITORS
RAMP SLOPE CAPACITORS
CLOCK PULSES FROM R107
SWEEP FROM R818
SWEEP GATE FROM R198
SW145 SWEEP MODE
EXT. SWEEP INPUT
MANUAL
NORMAL
SINGLE DISPLAY
SW157 DOTS PER DIV.
D58
D59
SW 50B
MOUNTED ON BACK OF VARIABLE TIME/DIV. AND CLOSED ONLY IN CALIB. POSITION
D.U.GND
SWITCHING FOR DIGITAL READOUT
A2
REFERENCE DRAWINGS:
1 TRIGGER & HOLD-OFF
2 FAST RAMP
3 STAIRCASE GENERATOR
4 HORIZONTAL AMPLIFIER
TYPE 3T77 PLUG-IN UNIT
TIMING SWITCH
CMD 864



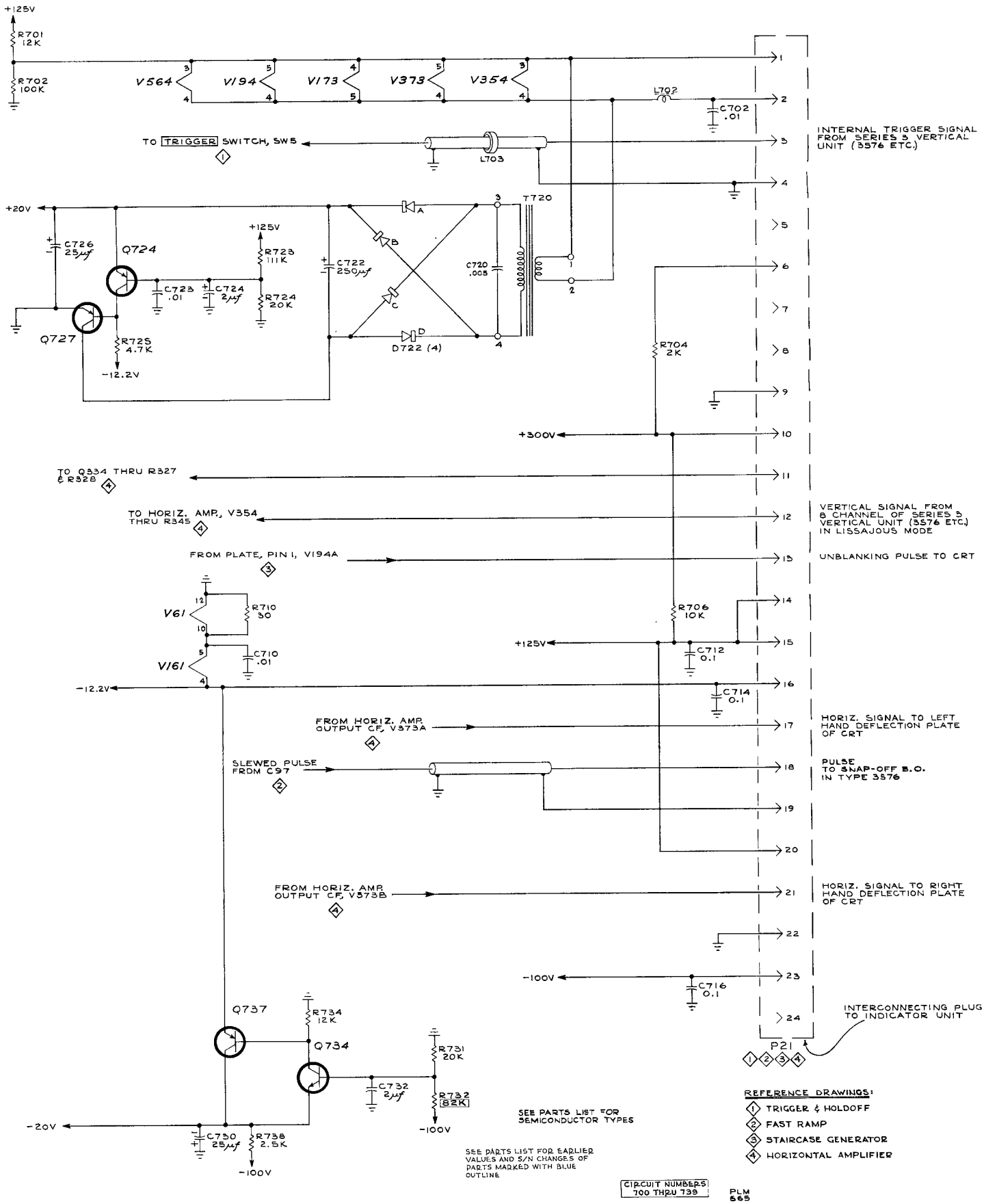
TYPE 3T77A SAMPLING SWEEP UNIT

B

266

5 TIMING SWITCH

S/N 4000-UP



TYPE 3T77 PLUG-IN UNIT

B

PLUG-IN CONNECTOR TO INDICATOR & POWER SUPPLY

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages. If it does not, your manual is correct as printed.

TYPE 3T77 -- TENT SN 3440*

CHANGE TO:

D22	152-0203-00	Tunnel	20 mA	
L14	108-0170-00	.5 μH		
Q33	151-0162-00	Replaceable by 2N3324		
R33	316-0122-00	1.2 kΩ	1/4 W	10%

*Some instruments with earlier Serial Numbers may contain these changes. The modification may be identified by Part Number 388-0605-01 on the Trigger and Fast Ramp circuit board.

TEXT CORRECTIONS

General Information

As a result of certain circuit improvements in the Type 3T77, the instrument designation has been changed to Type 3T77A to distinquish the new version from the older one.

In general, the new circuitry substitutes a Time Expander for the Horizontal Magnifier and substitutes a Time Position control for the Delay control. The Time Expander provides display expansion without decreasing the display dot density (dots/div), and the Time Position control provides display positioning that is commensurate with the sweep rate used, rather than a fixed-range delay. This permits the display to be positioned through at least one screen diameter on all equivalent sweep rates.

Control Name Changes

Because of possible confusion between names, the POSITION control has been renamed the HORIZONTAL POSITION control to distinguish it from the TIME POSITION control. Therefore, wherever the manual refers to the POSITION control, it should be interpreted as the HORIZONTAL POSITION control. This control positions the display with respect to the CRT graticule, whereas the TIME POSITION control positions the signal display through a "time window" that is referenced to the triggering signal.

Wherever the text refers to the HORIZ MAG switch, interpret this as the TIME EXPANDER switch. The same general function is accomplished by the TIME EXPANDER switch, with the following differences: (1) the dot density of the display is the same whether the TIME EXPANDER is at X1 or X10 (this means that there are actually 10 times as many dots per unit equivalent time on the displayed signal); (2) the display expands following the left edge of the display, rather than from the center of the display; (3) the trace length does not change and does not extend past the normal limits of the CRT screen.

Except where instructed otherwise, interpret any references to the DELAY control in the manual text as the TIME POSITION control. Please note, however, that the TIME POSITION control is display-oriented and operates in the opposite direction from that of the DELAY control described in the manual. That is,

when the TIME POSITION control is turned toward the right (clockwise), the display moves toward the right. Minimum delay of the displayed signal, with respect to the triggering signal, is obtained with the TIME POSITION control turned fully clockwise. (With the former DELAY control, minimum delay was obtained when the control was turned fully counterclockwise, so that when the control was turned clockwise, increasing the delay with respect to the triggering signal, the display moved toward the left.) Wherever the instructions in the manual say to turn the DELAY control in a particular direction, it will be necessary to turn the TIME POSITION control in the opposite direction.

SECTION 1 -- CHARACTERISTICS

Page 1-1, column 1,
Substitute the following for the subsection titled

External Triggering:

Pulse Amplitude and Width Requirements -- 10 millivolts, peak to peak minimum amplitude, with at least 2 nanoseconds of pulse width. Maximum useable trigger pulse amplitude is approximately 800 millivolts. Overload damage may occur in the External Trigger Input circuit if a signal amplitude of 5 volts or more is applied.

Pulse Triggering Repetition Rate -- Up to 10^9 pulses/second (1 gigacycle). Trigger circuitry counts down to a sampling rate of approximately 100 kilocycles or less, depending on the sweep rate used. Pulse triggering jitter is typically no greater than 50 picoseconds or 0.1% of the fast ramp duration (whichever is greater) with a pulse signal of 50 millivolts amplitude and 2 nanoseconds pulse width.

Sine-Wave Triggering Frequency -- From 100 kilocycles through 1 gigacycle. (Trigger circuitry counts down as described under Pulse Triggering.) Sine-wave triggering jitter varies with signal amplitude, frequency and sweep rate. Typical jitter is less than 50 picoseconds on a 100-millivolt/50-megacycle sine wave. Synchronized triggering mode provides stable triggering above 30 megacycles.

Page 1-1, column 2,
Substitute the following for the subsection titled Delay:

Time Positioning

Adjustable to position the start of the display by at least one screen

diameter (up to approximately 45 screen diameters at the fastest sweep rates) for a non-expanded display; permits the displayed signal to be positioned through at least 10 screen diameters (up to 450 diameters) with the TIME EXPANDER switch at X10.

Disregard the subsection titled Accessories Supplied With the Type 3T77 and refer to the Accessories list in the Mechanical Parts List.

SECTION 4 -- CIRCUIT DESCRIPTION

Page 4-3 and 4-4,
Substitute the following for the entire subsection titled Trigger and Holdoff Circuit:

When the Type 3T77A is in the triggerable condition, tunnel diodes D22, D25 and D42 are in the low-voltage state and transistors Q14, Q24, Q33 and Q34 are turned off. Back diode D18 is in the high-voltage stage, conducting approximately 100 μA of current. With Q24 and Q33 turned off, diodes D27 and D28 are reverse biased and diode D31 is forward biased, holding the emitter of Q33 at +20 volts. The base of Q34 is clamped one junction below ground by current through D32, thus trigger holdoff capacitors C30 and C31 are charged to about 20 volts.

The input triggering signal is applied through the TRIGGER Source switch, SW5, to the emitter of common-base amplifier Q14, either from the trigger take-off circuit of the vertical sampling unit or from the TRIGGER EXT INPUT J7 on the front of the Type 3T77A. Triggering is initiated when the triggering signal increases current through Q14 and D22 to the switching point of the tunnel diode, causing D22 to switch to its high-voltage state. The amount of current increase through Q14 that is required to switch D22 is determined by the current setting of the SENSITIVITY control, R19, and the TRIG SENS RANGE adjustment, R21.

Pulse and Sine-Wave Triggering. For normal triggered operation (for signals below 30 megacycles), the PULL FOR SYNC switch is pushed in, effectively disconnecting C26 from the circuit. As D22 switches to its high-voltage state, the positive-going switching pulse passes through R25 and C25 to D25, switching D25 to its high-voltage state. A positive-going step is applied to the base of Q24 and to the anode of D42 when D25 switches to its high state, turning on Q24 and switching D42 to its high-voltage state. As D42 switches, a trigger pulse is sent to the Fast Ramp circuit to initiate the operation of that circuit.

As Q24 turns on, starting the holdoff cycle of the Trigger circuit, its collector drops toward ground, turning on Q33 and forward biasing D27 and D28. The increased current through R21 and R22 and through R24 and R26 causes D22 and D25 to reset to the low-voltage state. The negative-going voltage step that resets D25 is also applied to the base of Q24, turning that transistor off again. Even though Q24 is turned on for only a short period of time, it discharges trigger holdoff capacitors C30 and C31 during that time by means of the

low-impedance current path through D32. When Q24 then turns off, its collector voltage starts to go positive, turning on Q34 through the holdoff capacitors. As D32 becomes reverse biased, C30 and C31 have to charge through the relatively high impedance of R30 (RECOVERY TIME) and R31, so the voltage at the collector of Q24 rises slowly after the initial small fast step. The charging current for holdoff capacitors C30 and C31 is obtained through Q34, holding the transistor turned on for the period of time determined by the RC time constant of C30, C31, R30 and R31.

Diodes D27 and D28 are reverse biased as Q34 turns on, but tunnel diodes D22 and D25 are held in their low-voltage state for the remainder of the holdoff cycle by current through Q34 and D26. When C30 and C31 have charged to the point that the anode of D31 reaches +20 volts, this diode becomes forward biased again, clamping the voltage at +20 volts. With the charging current removed from Q34, the transistor turns off, ending the holdoff interval as bias is restored to D22 and D25. The circuit is then ready to be triggered by the next excursion of the input triggering signal.

If the TRIGGER SENSITIVITY control, R19, is set to its maximum resistance position (fully clockwise), the circuit free runs. In this case, D22 switches to its high state each time Q34 turns off at the end of the holdoff interval.

Synchronized Triggering. When the PULL FOR SYNC switch is pulled out, SW30 connects C26 to ground, slowing down the recovery of tunnel diode D25 at the end of the holdoff interval. This permits D22 to be triggerable for a short period of time before bias is restored to D25. For trigger signals above about 30 megacycles, back diode D18, inductor L14 and tunnel diode D22, in conjunction with R18 and R19, form a monostable multivibrator that synchronizes with the input signal during the time that D22 is triggerable and before bias has been restored to D25. During this short interval, D22 and D18 switch back and forth between the low-voltage state and the high-voltage state (about 3 to 9 times) as current through Q14 increases and decreases. The first trigger pulse produced by D22 after D25 has recovered to the triggerable bias level switches D25 to its high-voltage state, starting the operation of the holdoff circuit in synchronization with an excursion of the triggering signal. The cycle of operation of the holdoff circuit is then essentially the same as that for pulse or sine-wave triggered operation, except that C26 is discharged through D26 when Q34 turns on.

When Q34 turns off at the end of the holdoff cycle, diode D22 becomes triggerable as its bias is restored, but the bias level returns more slowly to D25 as C26 becomes charged. Thus D22 again becomes synchronized with the input signal as D25 recovers to its triggerable level through an RC time constant of about 1 microsecond.

Pages 4-4 and 4-5,
Substitute the following for the entire subsection titled Fast Ramp:

This circuit generates a fast-ramp waveform, compares it with an existing slow-ramp voltage from the Staircase Generator, and produces a positive-polarity slewed pulse. The fast-ramp waveform is developed across Ramp Slope Capacitor C88 and compared with the slow-ramp (staircase) waveform at Q93A. The negative-going slewed pulse is generated by D93 and is inverted and amplified by Q94.

The action of the Fast Ramp circuit is initiated by the positive-going trigger from the Trigger and Holdoff circuit which is coupled through common-base amplifier Q74. The collector current of Q74 switches fast-ramp gate diode D74 from its quiescent high state to its low state. The resulting fast positive step turns off Q84, diverting the current from constant-current tube V61 into the Ramp Slope Capacitor. Charging of this capacitor carries the cathode of D90 in the negative direction.

The staircase voltage from the Staircase Generator is applied to the Slow-Ramp Inverter through an attenuator consisting of R51 (VARIABLE TIME/DIV), R52, R60, R61, R53 and R54 (see the Timing Switch schematic in this insert). At the input to this attenuator, the signal is a 50-volt positive-going staircase of 100 or 1000 steps, depending on the setting of the DOTS/DIV switch, SW157, shown on the Staircase Generator diagram. Thus, each step of the waveform (into the attenuator) is either 0.5 or 0.05 volt in amplitude. Transistors Q63 and Q64 form an inverting amplifier with a feedback resistance of 10 kΩ. The gain of this stage, from the input of R51 to the output of R90, ranges from 0.1 to 0.0002, depending on the value of R53 selected by the TIME/DIV switch, and by the position of the TIME EXPANDER switch, SW60A. When SW60A is switched from the X1 position to the X10 position, R61 is connected in series with R53, decreasing the gain of the Slow-Ramp Inverter by a factor of ten. Attenuator resistors R60 and R54 maintain a constant load on the Staircase Generator. The steps at the base of Q93A are negative-going steps of 50-millivolt to 0.01-millivolt amplitude. The smaller the steps, the

less the equivalent time between samples and the faster the equivalent sweep rate. When the TIME/DIV VARIABLE control is in the CALIB position, the wiper arm is at the top of R51, as shown on the schematic. Thus, as the control is moved away from the CALIB position, the resistance of R51 increases, decreasing the size of the steps at the base of Q93A and consequently increasing the equivalent sweep rate.

Each time the fast ramp starts, the base of Q93A is negative with respect to its emitter, so the transistor is not conducting. When the fast-ramp voltage at the cathode of D90 falls below the base voltage of Q93A, D90 and D93A turn on, increasing current through D93 which is quiescently in its low state.

When this happens, D93 switches to its high state, developing a negative step that is applied to the base of Q94. The resulting positive step at the collector of Q94 is the slewed pulse which is differentiated through C97 and applied through the interconnecting plug to the vertical plug-in unit to start the sampling process. The slewed pulse is also applied through R99 to the Staircase Generator to advance the staircase one step, and to the base of Q93B to reset tunnel diode D93 to its low state.

The negative step at the cathode of D93 is also coupled back through D75 and L75 to switch D74 back to its quiescent high state. This turns Q84 on again, ends the fast ramp, and discharges the Ramp Slope Capacitor.

The slope of the fast ramp is changed between timing ranges by changing the size of the Ramp Slope Capacitor. The steeper the ramp, the less difference there is in the time required for the ramp to reach successive levels of the staircase at Q93A. Thus, the equivalent time per division is controlled by varying both the size of the steps at the base of Q93A and the slope of the fast ramp at the emitter of Q93A.

The DC level of the Slow-Ramp Inverter output is varied by the TIME POSITION control, R58, to move the comparison level and thus the comparison time with respect to the triggering event.

PARTS LIST CORRECTION

REMOVE:

R57D	309-0155-00	40 kΩ	1/2 W	1%
R57E	301-0226-00	22 MΩ	1/2 W	5%
SW338	260-0145-00	Slide	HORIZ	MAG

ADD:

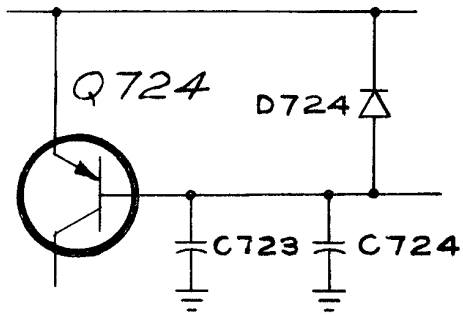
C155	283-0003-00	0.01 µF	Cer	150 V
D52	152-0066-00	Silicon, Replaceable by 1N3194		
D53	152-0066-00	Silicon, Replaceable by 1N3194		
D95	152-0185-00	Silicon, Replaceable by 1N6185		
D96	152-0185-00	Silicon, Replaceable by 1N6185		
D724	152-0141-00	Silicon, Replaceable by 1N3605		
L75	108-0260-00	0.1 µH		
R60	323-0611-00	900 kΩ	1/2 W	1%
R61	323-0385-00	100 kΩ	1/2 W	1%
R155	302-0121-00	120 Ω	1/2 W	5%
SW60A,B	260-0212-00	Slide	TIME EXPANDER	

CHANGE TO:

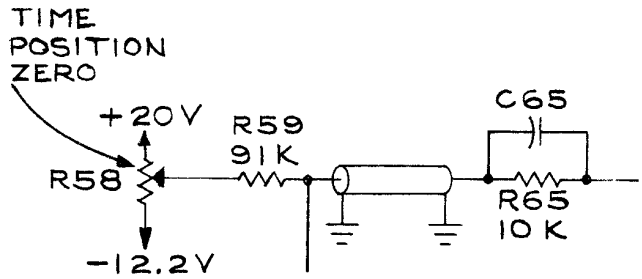
C30	283-0088-00	0.0011 µF	Cer	5%
C31A	285-0629-00	0.047 µF	PTM	100 V
C31B	283-0004-00	0.02 µF	Cer	150 V
C31C	283-0003-00	0.01 µF	Cer	150 V
C31D	283-0110-00	0.005 µF	Cer	150 V
C31E	283-0104-00	0.002 µF	Cer	500 V
D94	152-0139-00	Zener, 1N751, 5.1 V		
Q334	151-0136-00	Silicon, 2N3053		
Q724	151-0133-00	Silicon, Tek Spec		
Q727	151-0165-00	Replaceable by 2N3614		
Q737	151-0165-00	Replaceable by 2N3614		
R31	301-0563-00	56 kΩ	1/2 W	5%
R53A	323-0385-00	100 kΩ	1/2 W	1%
R53B	323-0414-00	200 kΩ	1/2 W	1%
R53C	323-0452-00	499 kΩ	1/2 W	1%
R53D	323-0414-00	200 kΩ	1/2 W	1%
R53E	323-0443-00	402 kΩ	1/2 W	1%
R53F	323-0481-00	1 MΩ	1/2 W	1%
R53G	323-0481-00	1 MΩ	1/2 W	1%
R54B	323-0414-00	200 kΩ	1/2 W	1%
R54C	323-0394-00	124 kΩ	1/2 W	1%
R54D	323-0414-00	200 kΩ	1/2 W	1%
R54E	323-0397-00	133 kΩ	1/2 W	1%
R54F	323-0389-00	110 kΩ	1/2 W	1%
R54G	323-0389-00	110 kΩ	1/2 W	1%
R54H	323-0387-00	105 kΩ	1/2 W	1%
R54J	323-0386-00	102 kΩ	1/2 W	1%

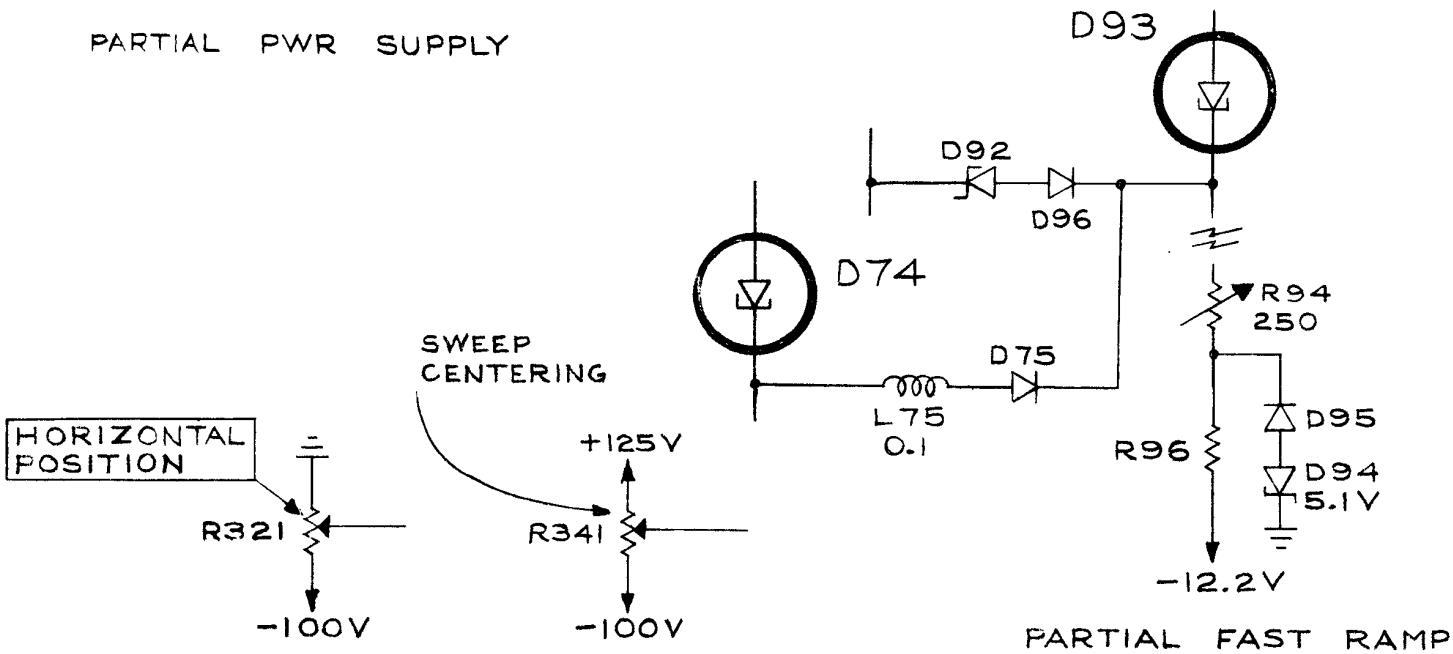
CHANGE TO:

R57A	323-0344-00	37.4 kΩ	1/2 W	1%
R57B	323-0411-00	187 kΩ	1/2 W	1%
R57C	323-0373-00	75 kΩ	1/2 W	1%
R59	301-0913-00	91 kΩ	1/2 W	5%
R65	323-0289-00	10 kΩ	1/2 W	1%
R68	301-0303-00	30 kΩ	1/2 W	5%
R80	315-0333-00	33 kΩ	1/4 W	5%
R81	315-0333-00	33 kΩ	1/4 W	5%
R84	323-0284-00	8.87 kΩ	1/2 W	1%
R85	311-0120-00	2.5 kΩ	Var	
R87	316-0680-00	68 Ω	1/4 W	10%
R94	311-0485-00	250 Ω	Var	
R315	323-0288-00	9.76 kΩ	1/2 W	1%
SW88	262-0760-00	Rotary	TIME/DIV switch	

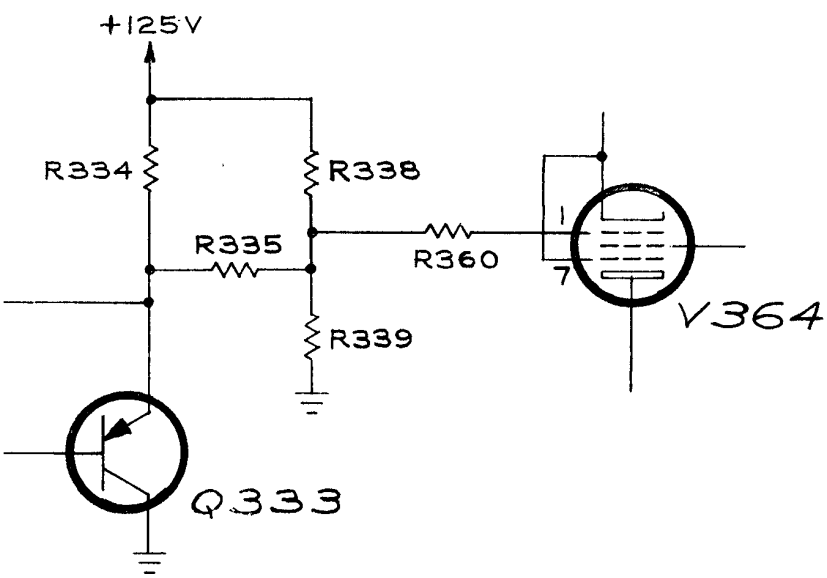


PARTIAL PWR SUPPLY

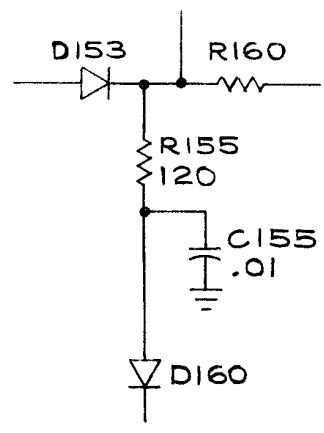




PARTIAL FAST RAMP



PARTIAL HORIZONTAL AMPLIFIER



PARTIAL STAIRCASE GEN

TYPE 3T77A TENT SN 4000

PARTS LIST CORRECTION

CHANGE TO:

D110	152-0071-00	Replaceable by ED2007

M10652/266

TEXT CORRECTIONS

This information supplements and/or supersedes the information in your Manual.

The trigger circuit is changed to allow switching to a 'lock-on' type of operation when displaying high frequency sine waves. This eliminates the display break-up caused by drift in recovery time.

A new front-panel RECOVERY control with a push-pull switch replaces the old control. Pulling the switch to the ON position allows the RECOVERY control to synchronize the circuit on sine waves above approximately 30 mc. Pushed in, the same control is used to trigger on signals below 30 mc.

CIRCUIT DESCRIPTION

With the front-panel switch in the ON (pulled out) position, both D22 and D25 are off (in low state) during the hold-off interval between samples. At the end of the hold-off interval the collector of Q34 goes positive. This action restores the bias to D22 while at the same time the bias to D25 is allowed to 'crawl up' with an RC time constant of about a microsecond. D25 turns on after this interval, initiating a trigger pulse to the Fast Ramp. D22, L14 and BD-4 diode form a 50-nsec monostable multivibrator which can fire several times before D25 is finally triggered by D22. This allows the one-shot multivibrator to become better synchronized to the input sine wave with each succeeding cycle and thus provides a firmer lock than if the first cycle were used for triggering. The setting of potentiometer R24 (a form of recovery control) will determine the optimum triggering point for synchronized and pulse operation.

With the switch OFF, the capacitor of the hold-bias network is disconnected. This allows D25 to fire and generate a Fast Ramp pulse each time there is an input trigger to D22. This action corresponds to the pulse mode of operation.

CALIBRATION, Page 6-2

Change step 5 to read as follows:

5. Turn the TRIGGER SENSITIVITY control fully clockwise and note the repetition rate of the signal. This will be referred to under 'Trigger Regenerator Sensitivity'.

Following step 5 please add:

D25 CURRENT RANGE (S/N 2000 and higher only)

1. With the test oscilloscope connected to test point [1] and the TRIGGER SENSITIVITY control fully clockwise, pull out the PULL FOR SYNC knob on the RECOVERY TIME control.

2. Turn R24 (D25 CURRENT RANGE) clockwise just to the point where the signal appears at test point [1].

3. Back off R24 to about 10° past the point where the signal disappears. This is the proper setting of R24.

4. Disconnect the test oscilloscope from test point [1] and push in the PULL FOR SYNC knob.