INSTRUCTION MANUAL

Serial Number 1734

5T1A
PLUG-IN UNIT

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070- 387


TYPE 5T1A TIMING UNIT
TRIGGERING
SWEEP MODE
SAMPLES/CM
50
20
10
5
100
1000
TIMED
START
SINGLE
DISPLAY
NORMAL
SOURCE
INT.
EXT.
POLARITY
FREE
RUN
CAL.
RECOVERY TIME
THRESHOLD
0
MIN.
MAX.
EXTERNAL
TRIGGER INPUT
5-250mV 50 Ω
TIME EXPANDER
X 5
X 10
X 20
X 2
X 50
X 1
X 100
TIME POSITION
VARIABLE
SWEEP TIME/CM
1
.5
.2
.1
2
5
μSEC
10
20
50
100
50
20
nSEC
10
5
2
1
CALIBRATED
SERIAL
TEKTRONIX, INC. PORTLAND, OREGON, U. S. A.

SECTION 1
CHARACTERISTICS

General

The Type 5T1A Timing Unit is a sampling-type timing plug-in unit for use with the Tektronix Type 661 Oscilloscope, and '4' Series sampling plug-in units. The Type 5T1A can receive trigger signals either through a front-panel connector (externally supplied) or through interconnecting wiring from vertical sampling units which have provisions for internal trigger takeoff. Trigger signals must bear a fixed time relationship to the signals to be displayed by the sampling unit.

The Type 5T1A has 16 calibrated equivalent-time sweep rates. Any sweep rate may be continuously increased to about 3X faster than the calibrated rate. A 7-position TIME EXPANDER switch allows any portion of the display to be expanded with a constant dot density. A front-panel control selects the number of samples per centimeter of horizontal deflection. A single-display circuit allows the operator to start a single horizontal sweep.

The triggering circuit will operate either on negative-going or positive-going signals. Trigger threshold is adjustable over a ±200-millivolt range for either positive-going or negative-going signals. Trigger source may be selected internally from the sampling unit, externally through a front-panel connector on the Type 5T1A, or internally from the Type 661 Amplitude/Time Calibrator. The trigger circuit may also be free-run at its maximum repetition rate. The repetition rate of the trigger circuit is determined by the setting of the SWEEP TIME/CM switch and the RECOVERY TIME control. The RECOVERY TIME control provides a range of trigger recovery times, allowing the operator to adjust for jitter-free triggering.

A TIME POSITION control provides a variable time delay for time-positioning the signal display in the TIME EXPANDER switch X1 position. In the expanded positions, the TIME POSITION control moves the time "window" anywhere within the original range displayed in the X1 position of the TIME EXPANDER switch.

CHARACTERISTICS

Sweep Time/CM

Sweep rates in 16 calibrated steps of equivalent time from 1 nsec/cm to 100 μsec/cm in a 1, 2, 5, 10 sequence. An uncalibrated variable control provides a continuous range up to 3X the calibrated rate between steps. A variable control extends the fastest rate to about 1/3 nsec/cm. All calibrated rates better than 3% accuracy.

Samples/CM

5, 10, 50, and 100, ±3% accuracy; also 1000 and timed sweep, with an unmagnified display.

Sweep Mode

Repetitive or single display.

Trigger Source

External, internal, free run, and calibrator. Sensitive to positive-going or negative-going slope.

Triggering Threshold

Continuously variable over a ±200-mv range.

Trigger Sensitivity

Internal or External: 5 mv external for a 1 nsec pulse. (Internal level is determined by output of sampling unit trigger-takeoff circuit.)

Recovery Time

Variable from about 10 to about 13 μsec on sweep rates faster than 0.2 μsec/cm; longer on slower sweep rates.

Time Expansion

Provides X1, X2, X5, X10, X20, X50, and X100 expansion of sweep rate selected with a constant number of samples/cm. Expansion may be selected to fall anywhere in basic time-base range, determined by SWEEP TIME/CM switch setting.

TABLE 1-1

Time Range of TIME POSITION Control

SWEEP TIME/CM Switch Setting	TIME EXPANDER Switch Setting		
	X1	X2	X5, X10, X20, X50, X100
100, 50, or 20 μSEC	100 μsec	500 μsec	1000 μsec
10, 5, or 2 μSEC	10 μsec	50 μsec	100 μsec
1, .5, or .2 μSEC	1 μsec	5 μsec	10 μsec
.1 μSEC, 50 nSEC, or 20 nSEC	0.1 μsec	0.5 μsec	1 μsec
10, 5, or 2 nSEC	100 nsec	100 nsec	200 nsec
1 nSEC	10 nsec	10 nsec	20 nsec

Time Position

Provides continuously variable time display window. Time position range is controlled by the TIME EXPANDER and SWEEP TIME/CM switches. Table 1-1 lists the ranges as a function of control settings.

Time Jitter

Less than 30 psec (picoseconds), or 10^{-4} X (fast ramp duration), whichever is greater, in 100-μsec through 2-nsec/cm sweep rates. Less than 10 psec at 1 nsec/cm sweep rate.

External trigger "kickout" is less than 5 mv.

SECTION 3

CIRCUIT DESCRIPTION

General

The Type 5T1A Timing Unit is used with '4' Series sampling units in the Type 661 Oscilloscope. The Timing Unit is triggered by signals with a fixed time relationship to repetitive identical signals displayed on the crt. The sampling technique allows resolution of repetitive identical signal-voltage changes occurring at fractional nanosecond (less than 10^{-9} second) rates with a broad bandpass for resolution of signals approaching dc.

The function of the Type 5T1A is to control the time at which the sampling unit takes the sample, and to simultaneously provide the display oscilloscope with a horizontal deflection signal. The horizontal deflection signal represents the time that elapses after the Type 5T1A is triggered before the sample is taken. By taking a series of samples, each one occurring a little later after triggering than the last, the display constructs a representation of the repetitive signals that were sampled.

The Type 5T1A has three major functional sections shown in simplified block diagram, Fig. 3-1. First is the trigger recognition and regeneration circuit, which triggers the operation of the remainder of the unit, and in turn must be triggered by a signal time-related to that displayed. Second is the fast ramp and comparator circuit. The fast ramp is a voltage fall with a constant calibrated slope. This voltage is fed to the comparator and compared with another voltage which represents the amount of horizontal deflection. The comparator provides a pulse output trigger to the sampling unit when the voltages are equal. Thus, the horizontal deflection voltage level fed to the comparator represents a calibrated interval of time following the operation of the trigger circuit.

Third is the staircase generator. When the Type 5T1A provides the horizontal deflection (Type 661 HORIZONTAL DISPLAY control in a SWEEP MAGNIFIER position), the staircase generator provides the horizontal deflection signal. The staircase steps one voltage increment after each sample is taken. When enough increments are stepped over, and a full display sweep is completed (about 10½ cm), the staircase resets and repeats the display. The size of each increment is controlled by the SAMPLES/CM switch determining the density (in equivalent time) of the samples.

The system may be triggered by an external 5 to 250 mv signal through a front-panel connector. Internal triggering from the signal applied to the sampling unit is also possible when the sampling unit used has a trigger takeoff circuit (such as the Type 4S1). Trigger circuit threshold may be set by a front-panel control.

The trigger recognition and regeneration circuit must receive trigger signals having a fixed time relation to the signal to be displayed. This circuit provides an output pulse to the time base (fast ramp) and the Type 661 Delayed Pulse generator for each trigger signal that operates the circuit. The holdoff circuit allows the trigger recognition circuit to operate only when the system is prepared for a new sample (never more often than about every 10 microseconds).

The trigger-recognition circuit triggers a fast-ramp voltage-rundown circuit. The fast-ramp circuit generates a voltage with a constant calibrated slope. Because the slope of the ramp is constant, some given time after triggering is equivalent to the time required for the fast-ramp voltage to travel from its starting point to a specific voltage. Thus, if the ramp slope is —5 volts/μsec, the equiva-

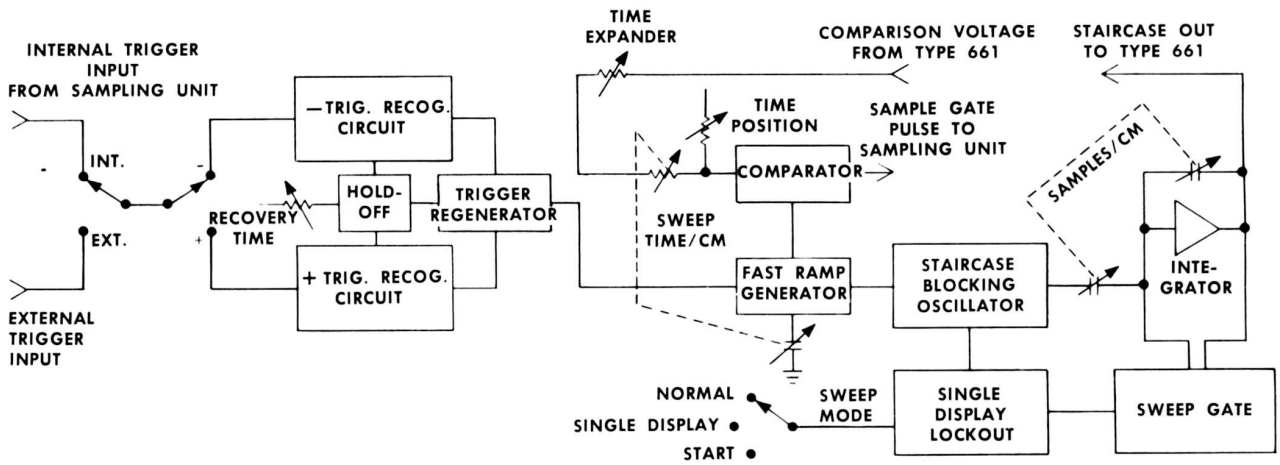


Fig. 3-1. Type 5T1A Simplified block diagram.

lent voltage for 2 μsec is —10 volts. In the Type 5T1A, the fast-ramp slope is controlled by the SWEEP TIME/CM switch. The total voltage change of the fast ramp, representing full-scale horizontal deflection on the crt, is selected by the SWEEP TIME/CM and TIME EXPANDER switches.

The Type 5T1A is provided with a staircase generator which advances a voltage increment after each run of the fast ramp. The staircase output voltage is normally fed to the Type 661 horizontal amplifier. When the Type 661 HORIZONTAL DISPLAY switch is in a SWEEP MAGNIFIER position, the staircase voltage is supplied to the comparator portion of the fast-ramp circuit. When the fast ramp has run from its starting voltage to the comparison voltage fed to the comparator, the comparator initiates a pulse, which is sent to the sampling plug-in unit. The staircase voltage, which represents time after the trigger has occurred, is also fed to the horizontal display circuit of the Type 661. The horizontal deflection caused by the staircase voltage represents the time it takes the ramp voltage to run down to the same voltage as the staircase level. The voltage increments of each step of the staircase voltages determine the equivalent time-spacing between samples.

When the Type 661 HORIZONTAL DISPLAY switch is in the EXT. HORIZ. INPUT positions, the staircase voltage is not used. Instead, the deflection caused by the external horizontal input voltage determines the time after triggering when samples are taken. The Type 5T1A must be triggered in the same manner as it was when the staircase was used to provide horizontal deflection. The position of the trace on the crt, determined by the horizontal input signal, determines the time after triggering when a sample will be taken. Thus, if the left graticule edge represents a specific time T_o, and the SWEEP TIME/CM switch is set at 10 nSEC, the vertical deflection at the fifth graticule mark will represent the signal at the input occurring 50 nsec after T_o. Note that the input voltage to the external horizontal circuit of the Type 661 and Type 5T1A system always represent time when displayed on the crt.

Manual scan also provides a display of equivalent time. With the SWEEP TIME/CM switch at 10 nSEC, scanning the crt with the HORIZONTAL POSITION controls will cover an equivalent time from T_o to (T_o + 100) nsec.

Time-expander circuit allows the system to view only a portion of the fast-ramp rundown time, displaying this time as a full 10 cm display. The expanded time portion of the rundown is determined by the TIME EXPANDER switch and TIME POSITION control. The TIME EXPANDER switch determines the length (difference in voltage between beginning and end) of the fast-ramp rundown portion used. The TIME POSITION control sets the dc level of the portion used, effectively shifting the time scanned. Notice that magnifying the signal with the TIME EXPANDER switch allows a portion of the signal to be viewed with a constant number of samples/cm. The Type 661 SWEEP MAGNIFIER switch allows a portion of the signal to be viewed, with a decrease in the number of samples/centimeter (constant time/dot) in the crt display. A combination of the two magnification methods may be used.

Trigger Recognition Circuits

Two trigger-recognition circuits are used. One responds to positive-trigger information, and one responds to negative-trigger information. The trigger-recognition circuit used is selected by POLARITY switch SW10B. When the POLARITY switch is in the CAL. position, the signal from the Type 661 Amplitude/Time Calibrator is fed to the negative-trigger recognition circuit. The trigger-recognition circuits are similar except that they use opposite input and supply voltage polarities. The external trigger information is inverted by T2 before being fed to the trigger-recognition circuits. Isolation amplifier Q4 isolates the external trigger input from the trigger-recognition circuits.

The trigger source is selected by SOURCE switch SW10A. Trigger signals may be internally supplied by the sampling unit if the sampling unit has a trigger takeoff circuit. They may also be supplied from an external source. External triggering is necessary when the sampling unit has no provisions for trigger takeoff or when low amplitude signals are being sampled. The SOURCE switch selects the trigger source and feeds the signals to the POLARITY switch which directs the signals to one of the trigger-recognition circuits. When the SOURCE switch is in the FREE RUN position, a bias is applied to the trigger-recognition circuit selected by the POLARITY switch, causing the trigger-recognition circuit to free-run. The THRESHOLD control sets the level (over a ±200 mv range) at which triggering occurs, and the + and — positions of the POLARITY switch set the direction in which the signal must move to cause triggering.

Assume TRIGGERING SWITCHES SW10A and SW10B are set to —INT as shown on the Trigger and Holdoff schematic. The THRESHOLD control is set far enough into the — region to hold off the trigger circuit. Assume also that the trigger circuits are ready to retrigger. D25 rests at its low state, near the switching point. D25 receives bias current from two sources. One is through R20, R21, R22, and L25. In addition, D35 is already in the high state, and current is supplied through R33. D25 is ready to trigger. If we move the THRESHOLD control to its + region, the small additional current supplied through the THRESHOLD control switches D25 to its high state. This sends a positive pulse to T65 through C60 and R60. The other end of the drive winding of T65 is connected to +19 volts through C61, R61, R47, R48, R49, and through R19 and the POLARITY switch. The connection through POLARITY switch SW10B locks out positive trigger-recognition circuit D45 and D55.

The pulse from D25, through the drive winding of regenerator transformer T65, causes enough additional current to flow in the circuit of D65 to switch D65 to its high state. After the pulse, D65 switches back to its low state. The regenerated output is taken from D65 through C65 and used to trigger the fast-ramp circuit. A negative gate signal is supplied by Q73 and D72 for use by the Type 661 Delayed Pulse generator. This gate circuit is driven by a separate winding on T65. D72 starts the delayed pulse and Q73 ends it.

The positive pulse at D25 is also fed to the emitter of holdoff driver Q104, starting operation of the holdoff circuit. The holdoff assures that the sampling cycle does not repeat before the system is prepared to take another sample. The circuit will not retrigger until D35 is turned to the high state and Q84 and Q94 are turned off. Under the free-running conditions described, D25 will retrigger immediately after D35 switches to its high state, which occurs after Q84 and Q94 are turned off.

With normal trigger operation, D25 will not have sufficient bias to switch to its high state until a trigger signal is received. THRESHOLD control R16 determines the signal level needed to trigger D25 to its high state. Trigger signals are fed either from the external or the internal trigger inputs, depending on the setting of SOURCE switch SW10A.

Operation of the positive trigger-recognition circuit is similar to that of the negative circuit. D45 is the recognition diode, and D55 is the recovery diode. The negative trigger-recognition circuit is locked out by —19 volts through POLARITY switch SW10A, and R17. The holdoff circuit is driven when D45 switches to the high state and sends a signal to the base of Q104. D55 is switched to the low state by the collector of Q84. D45 and D55 are connected opposite in polarity to D25 and D35. Note that the negative trigger-recognition circuit actually operates on positive-going signals, and the positive trigger-recognition circuit operates on negative-going signals. This is because trigger signals provided to the Type 5T1A are inverted before being fed to the trigger-recognition circuits.

Operation of the trigger-recognition circuits in FREE RUN is similar to the operation described previously. The input is driven by either +19 volts, in the — POLARITY, or —19 volts in the + POLARITY position.

Holdoff

The holdoff circuit prevents the trigger-recognition circuit from operating after a trigger has been received and recognized until the remainder of the system is ready to take a new sample. The holdoff period is required to allow the fast ramp to run for a time equivalent to 10 cm of display; then reset, or to limit the system repetition rate to 100 kc, whichever time is longer. The holdoff period is variable; 1.3:1 from the MAX. to the MIN. position of the front-panel RECOVERY TIME control. This may be adjusted to aid stable triggering if the triggering input frequency and the holdoff repetition rate are equal.

The holdoff circuit consists of two bistable multivibrators and a Miller integrator. Each bistable multivibrator drives a transistor which shunts supply current from one pair of the trigger-recognition circuit tunnel diodes. The ouput of the Miller integrator is also fed to a gate which switches both multivibrators. Recognition tunnel-diode multivibrator Q115-Q125 drives Q94. Recovery-diode multivibrator Q165-Q175 drives Q84. Miller integrator Q144 drives Q154 and gate D144. Tunnel diodes D25 and D45 are the recognition diodes, and D35 and D55 are the recovery diodes. Q104 drives the holdoff circuit.

When a trigger signal is received and recognized (assume the same conditions as for the trigger-recognition circuit discussion), D25 switches to the high state. This causes the emitter of Q104 to go positive, forward biasing the transistor. The collector voltage of Q104 rises, forward biasing Q115. The collector of Q115 drops, turning Q125 off. The same collector voltage drop at Q115 causes D92 to become forward biased, shunting the current source for D25 and causing D25 to return to its low state.

When Q125 turns off, its collector voltage rises, and current is supplied through R132 and RECOVERY TIME control R136, forward biasing Q144. This causes a voltage drop at the collector of Q144 which was clamped by Q154 at +19 volts. The collector drop of Q144 is fed back to its base through C145 and C146, preventing any large voltage swing at the base of Q144. Thus, the current through R132 and R136 that is charging C145 and C146 remains essentially constant. The value of C145 determines the rate of voltage fall at the collector of Q144, and is selected by the SWEEP TIME/CM switch for the desired holdoff time. As soon as the collector voltage of Q144 begins to fall, Q154 becomes back-biased, and its collector voltage drops to ground.

When the collector of Q144 reaches ground, D144 is forward biased which lowers the base voltage of Q165, turning it off and raising its collector voltage. C166 and R166 couple this collector voltage rise to Q175, turning it on. The collector of Q175 drops, forward biasing D82 and Q84. When Q84 is turned on, it shunts the current source for D35, returning D35 to the low state.

The collector voltage rise at Q165 is also coupled through D164, C164, and R164, to the base circuit of Q125, turning Q125 on. The collector voltage of Q125 drops, and this drop, coupled through C126 and R126, turns Q115 off. The collector voltage of Q115 rises, back biasing D92 and Q94, and restoring the current source to D25. Note, however, that D35 is in the low state, and that no current is available to D25 through R35. Thus, D25 remains in the low state, and cannot be triggered yet.

When Q125 is turned on, its collector voltage drops, and C145 and C146 discharge through R132 and R136. The voltage falls at the base of Q144 which decreases the collector current, causing the collector voltage to rise. This rise is fed back through C145 and C146, and the collector voltage of Q144 runs back up at a rate proportional to the total capacitance of C145 and C146. When the collector voltage of Q144 reaches +19 volts, Q154 becomes forward biased. This clamps the collector voltage of Q144 at +19 volts. When Q154 becomes forward biased, its collector voltage rises, forward biasing Q165. The collector voltage of Q165 drops, and this drop, coupled through C166 and R166, turns Q175 off. The collector voltage clamps the base of Q144, through D146, from going below the collector voltage of Q165. D164 is back biased, preventing the drop at the collector of Q165 from operating multivibrator Q115-Q125.

The collector voltage rise of Q175 back biases D82, and turns Q84 off. This restores the operating current to D35, and D35 immediately switches to the high state. With D35 in the high state, D25 receives additional current through R33, and is ready to be retriggered to initiate a new sampling cycle.

Fast Ramp

The fast-ramp circuit consists of a comparison-voltage amplifier, a ramp generator, and a pulse-forming comparator. The output of the ramp generator is a voltage fall with a constant calibrated slope used as an internal time base. The comparison voltage is received either from the staircase generator or externally through the Type 661. In the manual scan mode, the comparison voltage is supplied by the Type 661. For this discussion, assume that the Type 661 HORIZONTAL DISPLAY control is in the X1 position unless otherwise stated.

The comparison and fast-ramp voltages are fed to the pulse-forming comparator. When the two voltages are just equal, the comparator circuit generates a pulse used to drive the sampler in the '4' Series sampling unit. A pulse from the compartor circuit also drives the staircase generator, causing it to advance one step. The fast-ramp circuit operates each time a trigger output signal is fed to it from the trigger circuit. As the staircase voltage advances, step by step, the fast-ramp voltage must become greater, and thus will run a little longer with each succeeding rundown before the comparator circuit generates a pulse. The fast-ramp voltage represents the real time on which the system reconstructs the signal.

Ramp Generator

Q261 is a constant-current supply. Before a trigger signal is received from the trigger circuit, D255 is in the high state and holds Q254 on. Current from Q261 passes through Q254 and holds C260 near ground voltage. D255 is held in the high state by current through R244. Current through R244 also provides base current for Q254, and Q254 conducts the current supplied by Q261.

Q261 receives a constant base voltage from the —19-volt supply through decoupling filter R261 and C261. Q261 emitter current, which comes from the —100-volt supply, passes through R265 and R267 which drop about 81 volts. This determines the current through Q261. Current supplied by the transistor is determined by emitter current, and is little affected by any change in collector voltage.

The trigger circuit sends a positive pulse which causes Q244 to conduct more current. The collector voltage of Q244 rises to ground, and switches D255 to its low state, turning Q254 off. After the trigger pulse passes, Q254 remains cut off, held by D255 which remains in the low state. Q261 collector current now flows through ramp-slope capacitor C260, whose value is selected by SWEEP TIME/CM switch SW260. Before the beginning of the fast-ramp rundown, comparator diode D270 is back biased, and all current from Q261 is fed to C260. The ramp voltage runs down until D270 becomes forward biased. Collector current from Q261 is now fed through D270 and Q276, and the collector voltage of Q276 drops. D275 switches to the high state.

Before D275 switches, the voltage on either side of D276 is about zero volts. When the current from Q261 passes through Q276, it causes a step at D275, quickly switching D275 to the high state. Because D276 was not conducting, it appears as an open circuit as D275 switches.

When D275 switches, D276 becomes back biased. Because it is a tunnel diode, D276 conducts current easily, coupling the step caused by the switching of D275 to D285. This causes D285 to switch. When D285 switches, a step is fed to T284, which is a doubling transformer. The output of T284 forward biases Q284, causing the collector voltage of Q284 to rise. This gate, which appears at the collector of Q284, is connected directly through interconnecting cables to the '4' Series sampling unit. The gate is also sent, through isolation resistance network R285, R286, and R287, to the stairstep generator, where it is used to advance the stairstep one step. When the current through T284 (fed from R288 and R289) rises, D285 is switched back to the low state.

The fast ramp is reset by the comparator pulse. When D275 changes to the high state, D256 conducts, and changes D255 to the high state. Q254 now conducts the current supplied by Q261 and discharges C260. RAMP RECOVERY control R254 sets the maximum current through Q254 to a safe value commensurate with speedy ramp recovery.

Because the fast ramp is triggered by the incoming signal (or in a fixed time relationship to it), the instant, in real time, when the comparator pulse is sent to the sampling unit is determined by the comparison voltage. This determines the time the fast ramp must take to run down before the comparator pulse is sent to the sampling unit.

The rate of fall of the fast-ramp voltage, except the 1 nsec/cm rate, is determined by C260. Five capacitors allow five rates of fall or ramp slope (in volts/μsec) over the range above 1 nsec/cm. The 1 nsec/cm sweep rate is set by C263 and circuit stray capacitance. With C260 disconnected, C263 remains in the collector circuit of Q261 at all sweep rates, but is a small fraction of the circuit capacitance in sweep rates slower than 1 nsec/cm.

The effective portion of the fast-ramp voltage used is determined by the range of comparison voltage fed to the base of comparator transistor Q276. In the .1 μSEC position of the SWEEP TIME/CM switch, the effective ramp length is 10 volts; in the 50 nSEC position, 5 volts; and in the 20 nSEC position, 2 volts. (These voltages are true with the TIME EXPANDER switch in X1.) In each of these three positions, the slope of the ramp voltage is the same.

The voltage fed to comparator transistor Q276 is determined by the current fed to the operational amplifier preceding it; Q223 and Q234. Because Q223 is an emitter follower, the amplifier is current driven. Because Q234 is collector loaded, the output is a voltage output. Feedback resistor R231 determines the characteristics of the amplifier. There are three sources of current for Q223; from DELAY ZERO control R220 fed through R223 (this is a calibration adjustment); from the TIME POSITION control circuit, and from the Type 661 HORIZONTAL DISPLAY switch. When the HORIZONTAL DISPLAY switch is in any of the SWEEP MAGNIFIER switch positions, the staircase voltage is fed to the comparator circuit through two attenuator networks. One network, R214 and R215, always looks like a constant impedance at the input to the attenuator, but divides the current fed to Q223. Table 3-1 lists the positions of the SWEEP TIME/CM switch and the current attenuation introduced in each position. The SWEEP TIME/CM switch controls the values of R214 and R215. Table 3-1 also lists the resulting comparison voltage output equal to 10 cm of horizontal deflection. This voltage is seen at the base of Q276.

A second attenuator, R208 and R209, may be cascaded ahead of R214 and R215. R208 and R209 are controlled by the TIME EXPANDER switch, and are used to introduce further current division, above that introduced by R214 and R215. When R208 and R209 are switched into the circuit, the input continues to look like a constant impedance, and the current source for the comparator circuit is subjected only to a constant load impedance regardless of the settings of the SWEEP TIME/CM and TIME EXPANDER switches.

The range of the TIME POSITION control depends on both the SWEEP TIME/CM and the TIME EXPANDER switch settings. This control is a variable current supply, and its

range of operation (in time) depends on the voltage shift it can impose on the comparison voltage. Table 3-1 shows the voltages of the fast-ramp duration in SWEEP TIME/CM switch settings. Table 1-1 shows the range of the TIME POSITION control in time according to SWEEP TIME/CM and TIME EXPANDER switch settings. The voltage ranges over which the TIME EXPANDER control can shift the comparison voltage limits are as follows:

(a) ALT. SWEEP TIME/CM switch settings slower than 10 nsec/cm, and TIME EXPANDER switch at X1:1 volt.

(b) 10 nsec-cm through 1 nsec/cm sweep rates and TIME EXPANDER switch at X1: 5 volts.

(c) All SWEEP TIME/CM switch settings and TIME EXPANDER switch at X2: 5 volts.

(d) All SWEEP TIME/CM switch settings and TIME EXPANDER switch at X5, X10, X20, X50, or X100: 10 volts.

The voltage at the base of Q223 is controlled by INVERTER INPUT ZERO control R225. This control is set so that the base of Q223 is at zero volts dc, allowing proper operation of the current sources feeding Q223.

Staircase Generator

With the Type 661 HORIZONTAL DISPLAY switch in the SWEEP MAGNIFIER positions, the staircase generator provides a staircase voltage for the comparison circuit of the fast ramp.

TABLE 3-1

SWEEP TIME/CM Switch

SWEEP TIME/CM Switch Setting	Fast Ramp Slope	Attenuator Ratio	Duration of Fast Ramp Voltage = 10 cm Sweep
100 μSEC	0.01 volt/μsec	X1	10 volts
50 μSEC		X2	5 volts
20 μSEC		X5	2 volts
10 μSEC	0.1 volt/μsec	X1	10 volts
5 μSEC		X2	5 volts
2 μSEC		X5	2 volts
1 μSEC	1.0 volt/μsec	X1	10 volts
.5 μSEC		X2	5 volts
.2 μSEC		X5	2 volts
.1 μSEC	10 volts/μsec	X1	10 volts
50 nSEC		X2	5 volts
20 nSEC		X5	2 volts
10 nSEC	50 volts/μsec	X2	5 volts
5 nSEC		X4	2.5 volts
2 nSEC		X10	1 volt
1 nSEC	500 volts/μsec	X2	5 volts

The staircase generator is triggered by the fast-ramp comparator pulse, and steps one step for each comparison pulse fed to it. The voltage increment of each step is determined by the SAMPLES/CM switch. When the staircase has stepped over a voltage equivalent to the sweep length, a reset circuit returns the staircase voltage and a new trace begins. In the TIME position of the SAMPLES/CM switch, the staircase generator is allowed to run up linearly in a smooth runup. A single-sweep lockout circuit may be selected by SWEEP MODE switch SW325. A single sweep is obtained by preventing the staircase from starting until the SWEEP MODE switch is set to START. The staircase will then step through one display cycle, return, and be locked out until the SWEEP MODE switch is set to START again.

The staircase circuit includes gate circuit Q335-Q345, single display lockout D325-Q324, blocking oscillator Q300, and step integrator V361-V373.

Assume that the gating circuit is allowing a staircase voltage run, and that the SWEEP MODE switch is in NORMAL with Q335 and Q345 conducting. Note that Q335 is a PNP transistor, and that +345 is NPN. The circuit operates with both transistors turned on or turned off simultaneously. The collector circuit of each transistor is connected to the base of the other, and the circuit has two stable states. Its operation will be discussed later. With both Q335 and Q345 conducting, disconnect diodes D352 and D353 are back biased, allowing staircase capacitor C360 to be charged by the staircase step integrator as pulses arrive from the blocking oscillator.

A pulse from the fast-ramp comparator passes through C30 into the blocking oscillator circuit. The pulse sends current through the collector winding of T300. The trigger current induces a current in the base winding of T300 which turns on blocking oscillator transistor Q300. Normal blocking oscillator saturation follows. D306 completes the base-winding circuit of T300. The negative emitter-output signal of Q300 is fed through C358 (SAMPLES/CM switch SW358) to the step integrator. The amplitude of the pulse fed to C358 is controlled by R304, the internal SAMPLES/CM control.

Saturation occurs, and the blocking oscillator starts its backswing. D300 becomes forward biased and current passes through D300 instead of the collector winding of T300.

The negative pulse passed through C358 back biases D361, and forward biases D360. The pulse energy is fed directly to C360 and the grid of V361. V361 and associated circuit is a Miller integrator. The pulse energy starts to charge C360, and lowers the grid voltage of V361 which allows plate voltage to rise. This rise is coupled to the grid of cathode follower V373B. The cathode of V373B is coupled to C360 via C378 and D378. The rise of V373B cathode voltage raises the voltage to C360. The result is that the voltage of the V361 grid side of C360 remains nearly constant. The amount of charge given C360 is proportional to the capacitance of C358, which is controlled by SAMPLES/CM switch SW358. In the TIMED position of the SAMPLES/CM switch, current through R355 and R356 causes C360 to charge in a linear ramp. C360 is paralled by C361 in the SAMPLES/CM switch 1000 and TIMED positions, decreasing the staircase (or ramp) voltage slope for a given amount of charge fed through C358.

A positive feedback loop keeps the plate current of V361 constant over the output range to improve linearity and response time. The cathode voltage of V373B is fed through Zener diode D377 and C377 to the grid ofV373A. As C360

charges, the grid voltage of V373A rises. The cathode of V373A follows the grid and keeps the current through R371 and V361 essentially constant.

The staircase voltage at the cathode of V373B is fed through a resistance divider to pin 22 of P4 and to the Type 661 HORIZONTAL DISPLAY switch. The voltage at pin 24 of P4 runs from about 0 to 50 volts. Dc level of the output is set by DC LEVEL control R381. This voltage is fed back to the comparator of the Type 5T1A as a comparison voltage when the Type 661 HORIZONTAL DISPLAY switch is in any of the SWEEP MAGNIFIER positions.

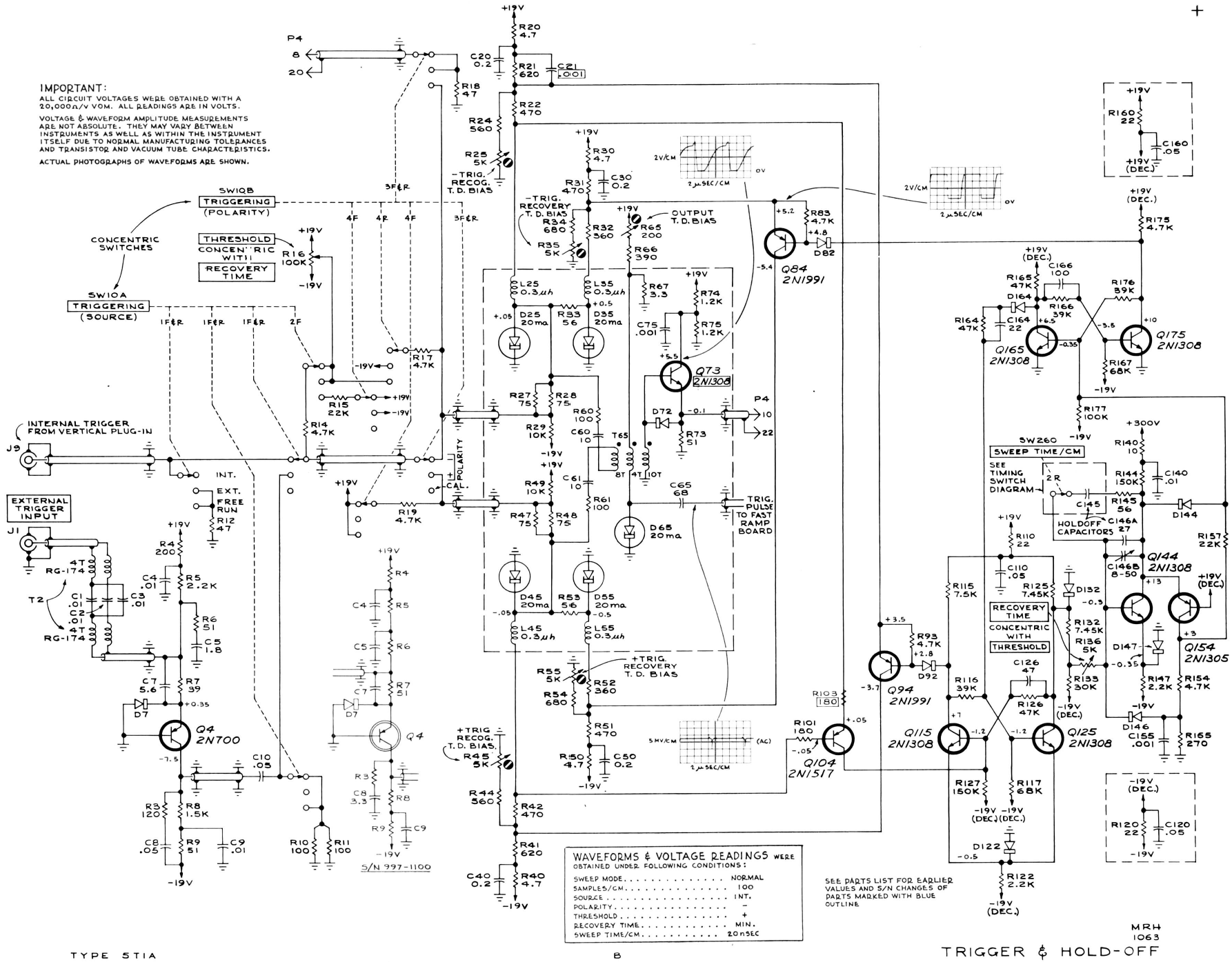
Staircase Gating Circuit

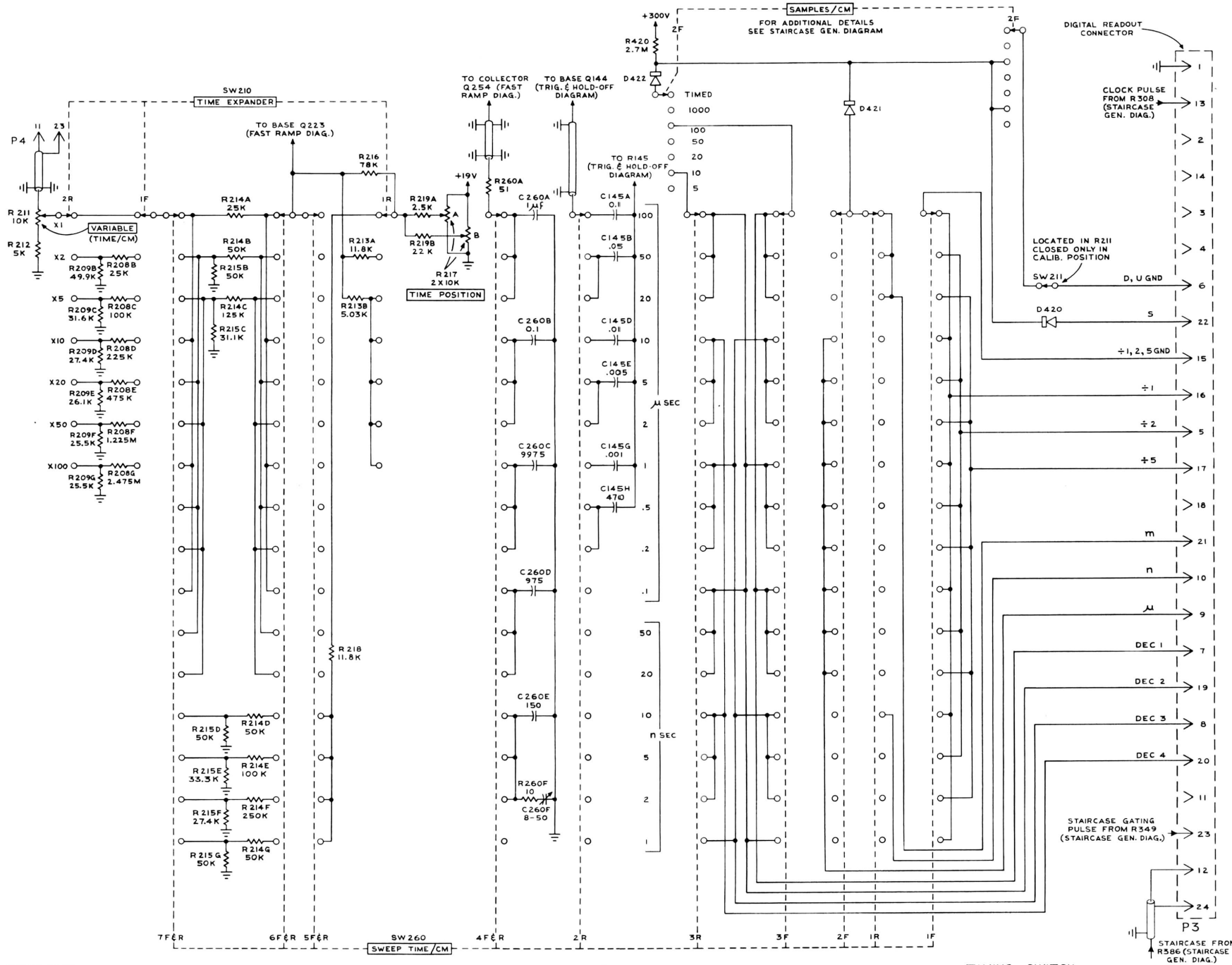
The unattenuated output signal is fed from C360 to the gating circuit. This signal passes through R346, D345, R345, and R344 to the base circuit of Q335. As the staircase voltage rises, the base of Q335 is moved toward cutoff. SWP LENGTH control R345 determines the amount of signal sent to Q335. When the base current approaches about 0.1 ma, the transistor turns off, and its collector voltage falls from 0 to —18 volts. This fall is coupled through R332 and C332 to the base of Q345 where the voltage drops from —18 to —20 volts. Q345 turns off, and its collector voltage raises from —18 to 0 volts. The grid of V361 is at about —0.9 volts, and D353 becomes forward biased. This raises the grid voltage of V361, since a current path is established through D353 to the +19-volt supply. The step integrator circuit now runs down and discharges C360 until D352 becomes forward biased, and a state of clamped equilibrium exists. When the Miller step-integrator circuit has discharged C360, D345 becomes back biased, and a current path no longer exists between the integrator circuit and the base of Q335. This prevents the staircase voltage from turning Q335 and Q345 back on.

The pulses from the blocking-oscillator circuit are fed through Q324 to switch the gate back to start the next staircase output. C303 transmits each negative pulse through R324 to D325 and the emitter of Q324. Each pulse switches D325 to the high state and forward biases Q324, which causes the emitter of Q324 to fall from 6.3 volts to zero. At the end of each blocking oscillator pulse, D325 switches back to the low state, and Q324 turns off. The negative pulse at the collector of Q324 is transmitted through C322 and R336 to the base of Q335. The first pulse received after D345 becomes back biased and C345 has discharged allows Q335 to conduct, raising its collector to ground, and allowing Q345 to conduct. C345 is paralled by C346 in the SAMPLES/CM switch TIMED and 1000 positions which lengthens the holdoff time before Q335 can be turned back on. The collector of Q345 drops back to about —18 volts, back biasing D352 and D353, and the step integrator is free to run up again until the feedback path from the integrator to the base of Q335 stops the run-up.

Blanking mixer Q314 is driven by the gate circuit, and by blocking oscillator to provide blanking signals to the Type 661. When the gate is in the off state (neither Q335 or Q345 conducting), Q314 is turned on through R331. When the gate is in the on state, (staircase run-up permitted) the collector of Q335 turns off Q314 and permits each pulse from the blocking oscillator to turn on Q314 for the duration of the pulse. The collector circuit of Q314 is completed in the Type 661. Whenever Q314 is forward biased, collector current flows, and crt blanking occurs. Thus, the crt beam is off whenever deflection is occurring.

A single sweep is obtained by moving SWEEP MODE switch SW325 to the SINGLE SWEEP position. R325 is connected, by SW325, to the —19-volt supply, and holds D325 in the high state. With D325 held in the high state, Q324 remains in conduction, and the negative pulse necessary to switch the gate transistors back into conduction is blocked. This locks the staircase at zero output. When the SWEEP MODE switch is moved to the START position, the junction of R310 and C310, which was at —19 volts, is grounded. C310 sends a positive pulse through R312 and R315 to D325, causing it to switch back to the low state momentarily, turning Q324 off. D325 switches back to the high state with the next pulse from blocking oscillator Q335, and allows the staircase generator to generate one display. At the end of the single sweep, Q335 is turned back off in the normal manner, and the SWEEP MODE switch must be set to START to obtain the next staircase output.


IMPORTANT:
ALL CIRCUIT VOLTAGES WERE OBTAINED WITH A 20,000Ω/V VOM. ALL READINGS ARE IN VOLTS.
VOLTAGE & WAVEFORM AMPLITUDE MEASUREMENTS ARE NOT ABSOLUTE. THEY MAY VARY BETWEEN INSTRUMENTS AS WELL AS WITHIN THE INSTRUMENT ITSELF DUE TO NORMAL MANUFACTURING TOLERANCES AND TRANSISTOR AND VACUUM TUBE CHARACTERISTICS.
ACTUAL PHOTOGRAPHS OF WAVEFORMS ARE SHOWN.
CONCENTRIC SWITCHES
SW10B
TRIGGERING
(POLARITY)
THRESHOLD
CONCENTRIC WITH RECOVERY TIME
SW10A
TRIGGERING
(SOURCE)
INTERNAL TRIGGER FROM VERTICAL PLUG-IN
J9
INT.
EXT.
FREE RUN
EXTERNAL TRIGGER INPUT
J1
T2
RG-174
POLARITY
+ CAL. -
TRIG. PULSE TO FAST RAMP BOARD
-TRIG. RECOG. T.D. BIAS
-TRIG. RECOVERY T.D. BIAS
+TRIG. RECOVERY T.D. BIAS
+TRIG. RECOG. T.D. BIAS
OUTPUT T.D. BIAS
Q4 2N700
Q73 2N1308
Q84 2N1991
Q104 2N1517
Q165 2N1308
Q175 2N1308
Q94 2N1991
Q115 2N1308
Q125 2N1308
Q144 2N1308
Q154 2N1305
D7
D45 20ma
D55 20ma
D65 20ma
D25 20ma
D35 20ma
D72
D82
D92
D122
D132
D144
D146
D147
D164
L25 0.3μh
L35 0.3μh
L45 0.3μh
L55 0.3μh
T65
SWEEP TIME/CM
SEE TIMING SWITCH DIAGRAM
HOLDOFF CAPACITORS
RECOVERY TIME CONCENTRIC WITH THRESHOLD
2V/CM
2μSEC/CM
5MV/CM
(AC)
S/N 997-1100
WAVEFORMS & VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:
SWEEP MODE . . . . . NORMAL
SAMPLES/CM 100
SOURCE . . . . . INT.
POLARITY . . . . . -
THRESHOLD . . . . . +
RECOVERY TIME . . . . . MIN.
SWEEP TIME/CM 20nSEC
SEE PARTS LIST FOR EARLIER VALUES AND S/N CHANGES OF PARTS MARKED WITH BLUE OUTLINE
MRH 1063
TRIGGER & HOLD-OFF
TYPE 5T1A
B

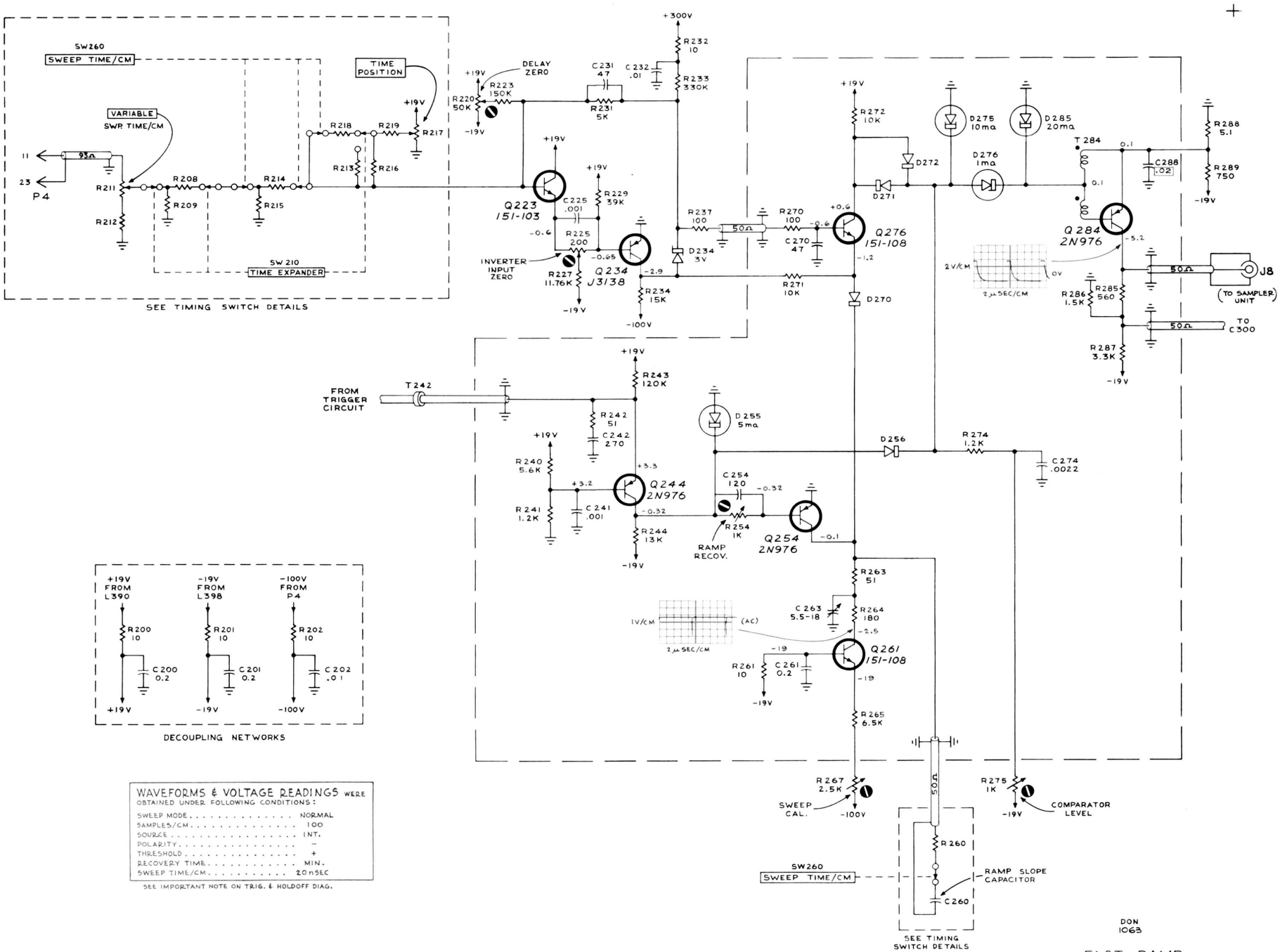


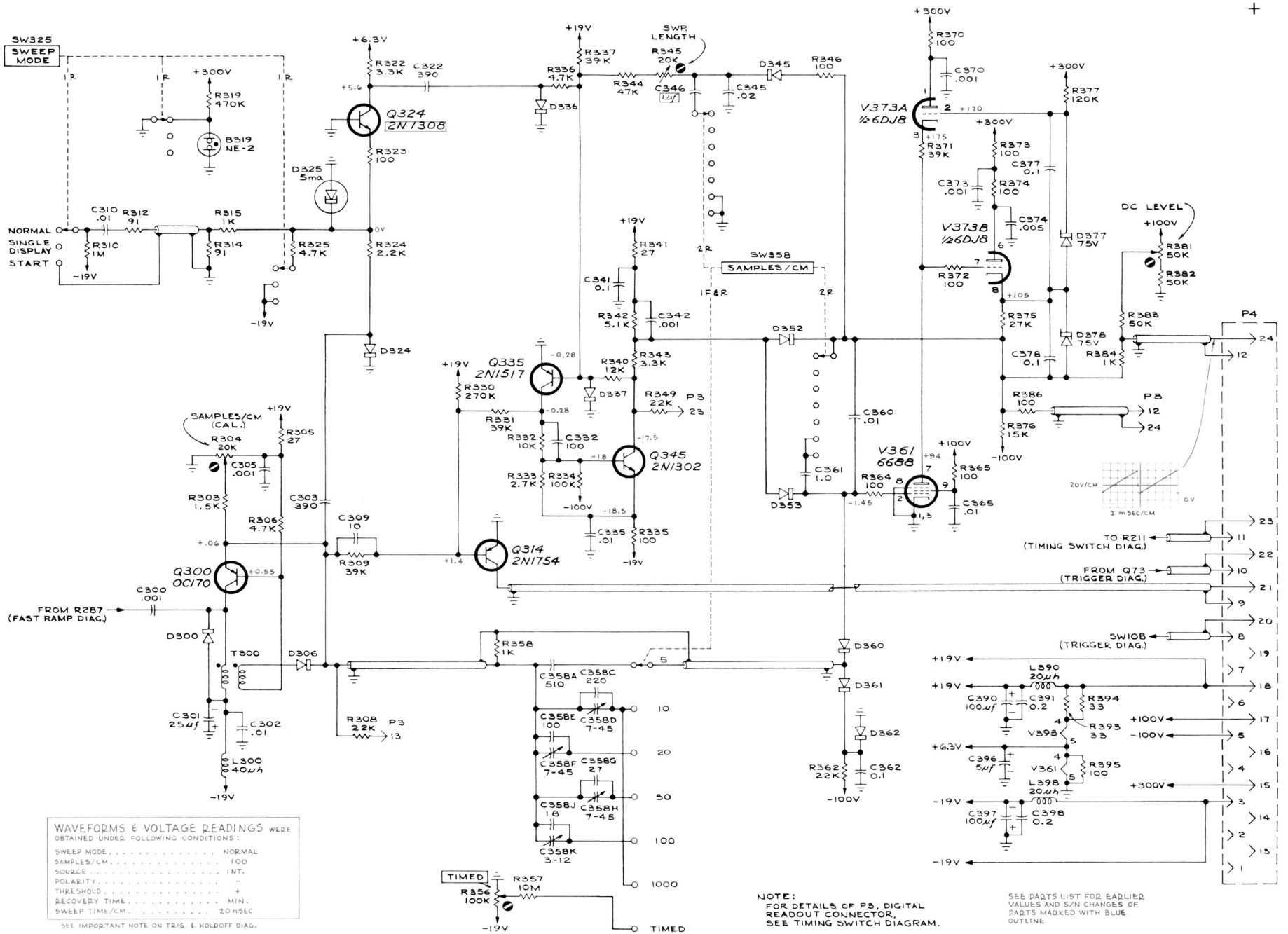
TYPE 5T1A

A1

TIMING SWITCH

DON 365


SW260
SWEEP TIME/CM
TIME POSITION
VARIABLE
SWP TIME/CM
+19V
R218
R219
R217
R213
R216
11
23
P4
93Ω
R211
R208
R214
R209
R215
R212
SW 210
TIME EXPANDER
SEE TIMING SWITCH DETAILS
+300V
R232
10
DELAY
ZERO
+19V
R223
150K
R220
50K
-19V
C231
47
C232
.01
R233
330K
R231
5K
+19V
Q223
151-103
C225
.001
R229
39K
-0.6
R225
200
INVERTER
INPUT
ZERO
R227
11.76K
-19V
-0.65
Q234
J3138
-2.9
R234
15K
-100V
R237
100
50Ω
D234
3V
R270
100
-0.6
+0.6
C270
47
Q276
151-108
-1.2
R271
10K
D270
+19V
R272
10K
D272
D271
D275
10ma
D285
20ma
D276
1ma
T284
0.1
C288
.02
R288
5.1
R289
750
-19V
Q284
2N976
-5.2
2V/CM
0V
2μSEC/CM
50Ω
J8
(TO SAMPLER UNIT)
R286
1.5K
R285
560
50Ω
TO C300
R287
3.3K
-19V
FROM
TRIGGER
CIRCUIT
T242
+19V
R243
120K
R242
51
C242
270
D255
5ma
D256
R274
1.2K
C274
.0022
+19V
R240
5.6K
+3.3
+3.2
Q244
2N976
R241
1.2K
C241
.001
-0.32
C254
120
-0.32
R254
1K
RAMP
RECOV.
Q254
2N976
-0.1
R244
13K
-19V
R263
51
C263
5.5-18
R264
180
-2.5
1V/CM
(AC)
2μSEC/CM
Q261
151-108
-19
R261
10
C261
0.2
-19V
-19
R265
6.5K
R267
2.5K
SWEEP
CAL.
-100V
50Ω
R275
1K
-19V
COMPARATOR
LEVEL
R260
SW260
SWEEP TIME/CM
RAMP SLOPE
CAPACITOR
C260
SEE TIMING
SWITCH DETAILS
+19V
FROM
L390
-19V
FROM
L398
-100V
FROM
P4
R200
10
R201
10
R202
10
C200
0.2
C201
0.2
C202
.01
+19V
-19V
-100V
DECOUPLING NETWORKS
WAVEFORMS & VOLTAGE READINGS WERE
OBTAINED UNDER FOLLOWING CONDITIONS:
SWEEP MODE . . . . . NORMAL
SAMPLES/CM 100
SOURCE . . . . . INT.
POLARITY . . . . . −
THRESHOLD . . . . . +
RECOVERY TIME . . . . . MIN.
SWEEP TIME/CM . . . . . 20 nSEC
SEE IMPORTANT NOTE ON TRIG. & HOLDOFF DIAG.
DON
1063



MRH
463

STAIRCASE GENERATOR

TYPE 5T1A

A2

Switches

Ckt. No.	Tektronix Part No. Unwired	Wired	Description		S/N Range
SW10B	260-438	*262-452	Rotary	TRIGGERING (Source)	
SW10A			Rotary	TRIGGERING (Polarity)	
SW210	260-527	*262-552	Rotary	TIME EXPANDER	
SW211†	*311-295				
SW260	260-528	*262-553	Rotary	SWEEP TIME/CM	
SW325	260-526	*262-554	Rotary	SWEEP MODE	
SW358			Rotary	SAMPLES/CM	

Transformers

T2	276-519	Core, Ceramic		
T65	*120-263	Toroid	3T	TD60
T284	*120-264	Toroid	3T	TD61
T300	*120-265	Toroid	7T	TD62
T242	*120-262	Toroid	1T	TD59

Transistors

Q4	151-027	2N700	
Q73	Use 151-072	2N1308	
Q84	151-065	2N1991	
Q94	151-065	2N1991	
Q104	151-031	2N1517	
Q115	151-072	2N1308	
Q125	151-072	2N1308	
Q144	151-072	2N1308	
Q154	151-071	2N1305	
Q165	151-072	2N1308	
Q175	151-072	2N1308	
Q223	151-103	Planar Silicon	
Q234	151-087	J3138	
Q244	Use 151-123	2N976	
Q254	Use 151-123	2N976	
Q261	151-108	Tek Spec.	
Q276	151-108	Tek Spec.	
Q284	Use 151-123	2N976	
Q300	*153-511	OC170	Checked
Q314	151-054	2N1754	
Q324	Use 151-072	2N1308	
Q335	151-031	2N1517	
Q345	151-040	2N1302	

Electron Tubes

V361	154-215	6688/E180F
V373	154-187	6DJ8/ECC88

† Concentric with R211. Furnished as a unit.