INSTRUCTION MANUAL

Serial Number _____

5A13N

DIFFERENTIAL COMPARATOR

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070-1228-00

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5A13N Differential Comparator

SECTION 2
THEORY OF OPERATION

Introduction

This section of the manual contains an electrical description of the circuits in the 5A13N Differential Comparator. Complete schematics and an overall block diagram of the unit are given on pullout pages at the rear of this manual.

BLOCK DIAGRAM DESCRIPTION

When the *DISPLAY* button is pressed, a logic level is applied to the oscilloscope to enable 5A13N operation (switch function is limited to operation in a vertical compartment), and the front-panel readout lamp lights to indicate the ON mode.

Signals applied to the + and − input connectors can be passed directly to the attenuators (DC coupled) or they can be capacitively (AC) coupled to block the DC component of the signal. The GND switch disconnects the signals and applies a reference ground to the amplifier input; for AC-coupled signals, the coupling capacitor is allowed to pre-charge to the DC level of the signal, preventing a damaging current surge when the ground is removed.

The input attenuators are frequency-compensated voltage dividers. 1X attenuation is provided for the 1 mV to 50 mV positions of the *VOLTS/DIV* switch, and *100X* attenuation is provided for the 0.1 V to 5 V positions.

The comparison voltage supply permits connecting either the + or the − input to an accurate voltage. The supply provides two ranges of comparison voltage, 0-1 V and 0-10 V, selectable in either positive or negative polarity from the front panel. The voltage is also made available to a front-panel jack for monitoring. Also, the ZERO V_C REF control permits grounding the amplifier inputs, to provide a reference.

The input source and emitter followers present a very high input impedance at the output of the attenuators. This stage incorporates circuitry to limit the common-mode and differential voltage dynamic ranges. The gain of this stage is approximately one.

The differential comparator amplifies the difference between the two inputs. The VOLTS/DIV switch changes the value of output collector-load resistors, thus providing gains of 1, 2.5, and 5 for various deflection factors. A bootstrap supply and a feedback amplifier are incorporated to reject common-mode signals. An emitter follower output is provided for this stage, and the push-pull output signal is opposite in polarity to that applied to the inputs.

The 1X-10X gain-switching amplifier receives the differential signal from the differential comparator. The gain of this stage is changed by the VOLTS/DIV switch. An emitter follower output is provided for this stage also, and the push-pull output signal is in phase with the applied signal.

The output amplifier is operated push-pull, presenting a signal to the output terminals that is 180° out of phase with that applied to the *5A13N* input. Emitter degeneration produced by the Variable Volts/Div control provides an uncalibrated deflection factor for the 5A13N. A positioning-current driver is connected across the output lines to alter the quiescent trace position.

A triggering signal is tapped from the output amplifier stage, amplified and made available to an associated time-base plug-in unit. Triggering signal amplitude is about 0.25 volt per displayed division.

CIRCUIT DESCRIPTION

Plug-In Logic

When DISPLAY button S340 is pressed, a logic level is applied to the electronic switching circuit in the oscilloscope to enable plug-in operation. Power is applied to light the front-panel knob-skirt readout lamp, indicating the ON mode.

Input Coupling

Signals applied to the front-panel + and − input connectors may be capacitive coupled (AC), direct coupled (DC), or internally disconnected (GND). Input coupling is selected by means of two pushbutton switches at each input, S1A and S1B for the + input and S21A and S21B for the − input. When the AC button is pressed, a coupling capacitor (*C1* or *C21*) is placed in the circuit to couple signals of about 2 hertz (−3 dB point) and higher to the attenuator. When the GND button is pressed, a ground reference is provided to the input of the amplifier without the need to remove the applied signal from the input

connector. When both the AC and GND buttons are pressed, the coupling capacitor can be pre-charged or discharged, protecting the circuit under test and the input circuit of the 5A13N from surge currents.

Input Attenuator

The input attenuators are frequency-compensated voltage dividers that provide 100X attenuation in the 0.1-volt to 5-volt positions of the VOLTS/DIV switch. For DC and low-frequency signals, the dividers are essentially resistive (attenuation ratio determined by the resistance ratio). A low-frequency common-mode signal between the attenuators of the two inputs is balanced by adjustment of R10, LF CMR. At higher frequencies where the capacitive reactance becomes effective, the attenuation ratio is determined by the impedance ratio.

Comparison Voltage

When either front-panel V_c button is pressed, the respective amplifier input stage is connected to an accurate comparison voltage. S50 permits either side of reference Zener VR50 to be tapped, providing either a positive or a negative comparison voltage. The comparison voltage is set to exactly 10 volts by adjustment of R54. S55 permits either of two ranges to be chosen, 0 to 10 volts, or 0 to 1 volt. Precise 10:1 voltage division is obtained by adjustment of R57. The exact amount of comparison voltage is dialed by the front-panel COMPARISON VOLTAGE control, R60. The comparison voltage is also available at front-panel V_c OUT jack J60 for monitoring. ZERO V_c REF switch S100 allows both amplifier input stages to be connected to ground, permitting the trace to be established as a zero reference.

Input Source and Emitter Follower

The Input Source and Emitter Follower stage provides a very high input impedance to prevent loading the passive input circuit elements. The + and − sides are identical except for the balancing components; therefore, only the + side will be described. CR102 and Q109 provide input protection as well as providing a common-mode voltage limit. Q110A is an FET source follower which drives emitter follower Q115A. Q108-Q109 provides a constant-current source for this stage, and Q114A and Q117 provide a constant-current return. Q122 and CR123 provide bootstrapping to the Q115A collector, maintaining nearly constant voltage across the transistor. Gain of this stage is X1. Coarse and Fine Input Balance controls R112 and R212 permit matching the quiescent output voltages to the input gate voltages.

Under normal operating conditions, Q120 and Q220 are biased to pass the signals to the input of the comparator stage. These transistors function as disconnect switches if an overdrive signal causes conduction of the diodes between their bases.

Differential Comparator

The Differential Comparator is composed of Q130A and Q140A connected in cascode on one side, and Q130B and Q140B connected in cascode on the other side. Q135 provides a current source for these transistors. The differential input signal is developed across R133 and R233, changing the conduction of the two halves of the amplifier. The output of this stage is a push-pull signal, opposite in polarity to that applied to the input. The gain of the stage is 1, 2.5, or 5, depending on the collector-load resistance selected by VOLTS/DIV switch S260.

A bootstrap supply and a feedback amplifier are incorporated to reject common-mode signals. A common-mode signal applied to the bases of Q130A and Q130B is sensed at the base of Q149, and then applied through emitter-follower action to the bases of Q140A and Q140B. The effect of this bootstrap supply is to maintain constant operating characteristics of the amplifier transistors. Q146 supplies a constant current to the bootstrap supply. Common-mode signals that reach the collectors of Q140A and Q140B are sensed by the base of Q158. Q155 and Q158 are connected as a paraphase amplifier, thus a signal in-phase with the common-mode signal is developed at the collector of Q155 and applied to the current-source transistor, Q135. This control of the current through the two halves of the amplifier helps to remove common-mode signals. Emitter follower Q143 maintains a constant voltage at the bases of Q146 and Q155.

The differential output signal is applied through emitter followers Q170A and Q170B to the 1X-10X Gain-Switching Amplifier. Voltage-limiting diodes are connected across the bases of the emitter followers to protect the transistors in the following stage and to ensure quick overdrive recovery.

1X-10X Gain-Switching Amplifier

The 1X-10X Gain-Switching Amplifier stage consists of push-pull amplifier Q190A-Q190B, grounded base amplifiers Q195 and Q295, and emitter followers Q300 and Q400. Q190A and Q190B are supplied by constant-current source transistor Q175. Conduction of the two halves of this amplifier is balanced by adjustment of R178, 1X-10X Bal. R180, Gain, permits adjustment of the emitter resistance, allowing the overall gain of the 5A13N to be adjusted to match the mainframe requirements. 1X-10X gain switching is achieved by changing the collector-load resistance of Q195 and Q295 with the VOLTS/DIV switch. Variable Balance control R194 is adjusted to minimize trace shift when the Variable Volts/Div control in the next stage is rotated. The output signal is passed through emitter followers Q300 and Q400.

Output Amplifier

The Output Amplifier consists of push-pull amplifier Q310-Q410. The input to this stage is diode-protected.

Variable Volts/Div potentiometer R414 allows the gain of the 5A13N to be adjustable over a 2.5 to 1 ratio.

Q330 and Q430, connected across the output lines of the 5A13N, are positioning-current drivers. POSITION control R335 provides an adjustable change in the conduction of the transistors, which provide a current to sum with the Q310-Q410 currents, controlling the quiescent vertical position of the display. S337 and S339 allow capacitors to be switched in across the output lines to limit the amplifier bandwidth.

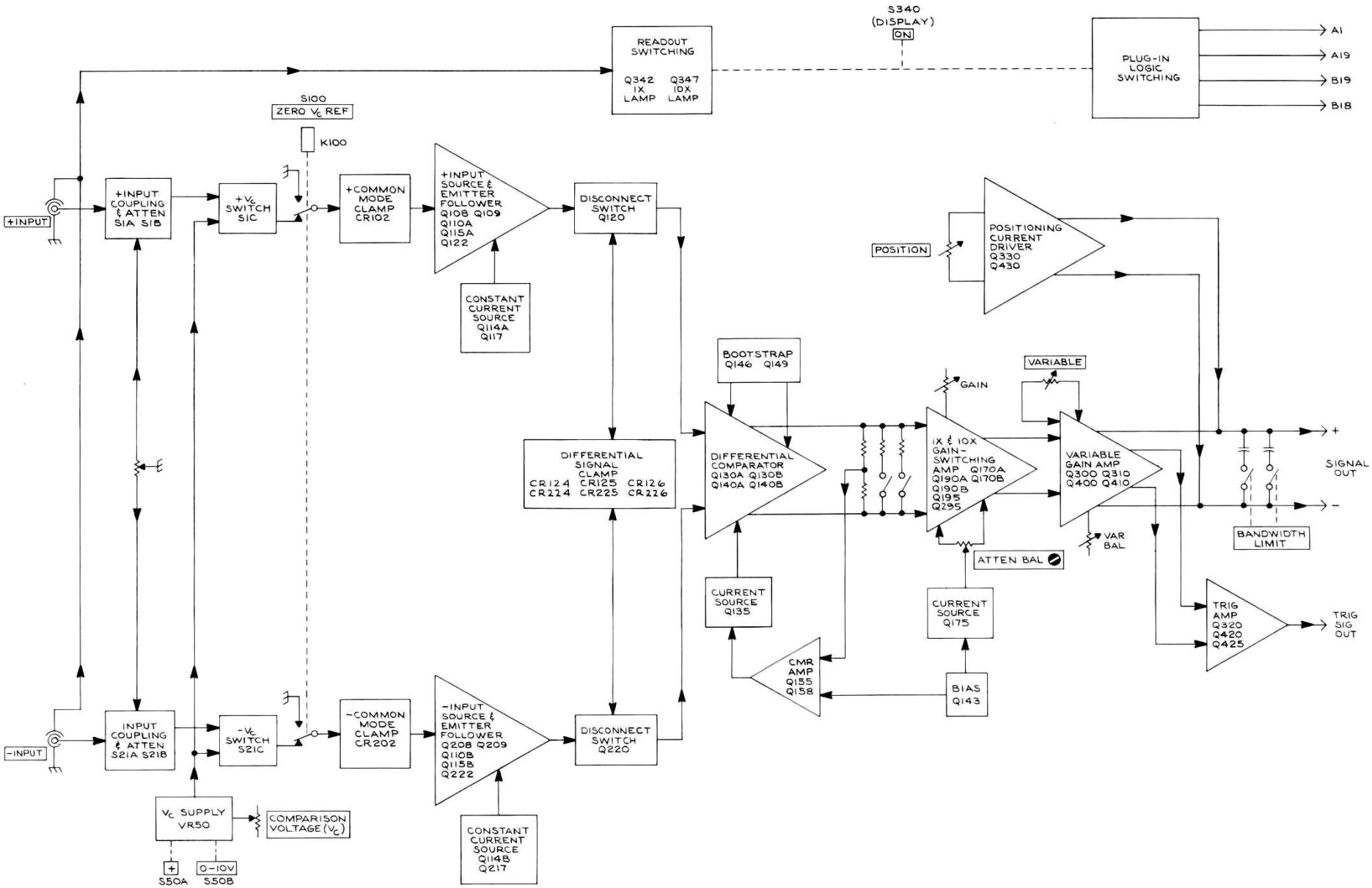
Trigger Signal Amplifier

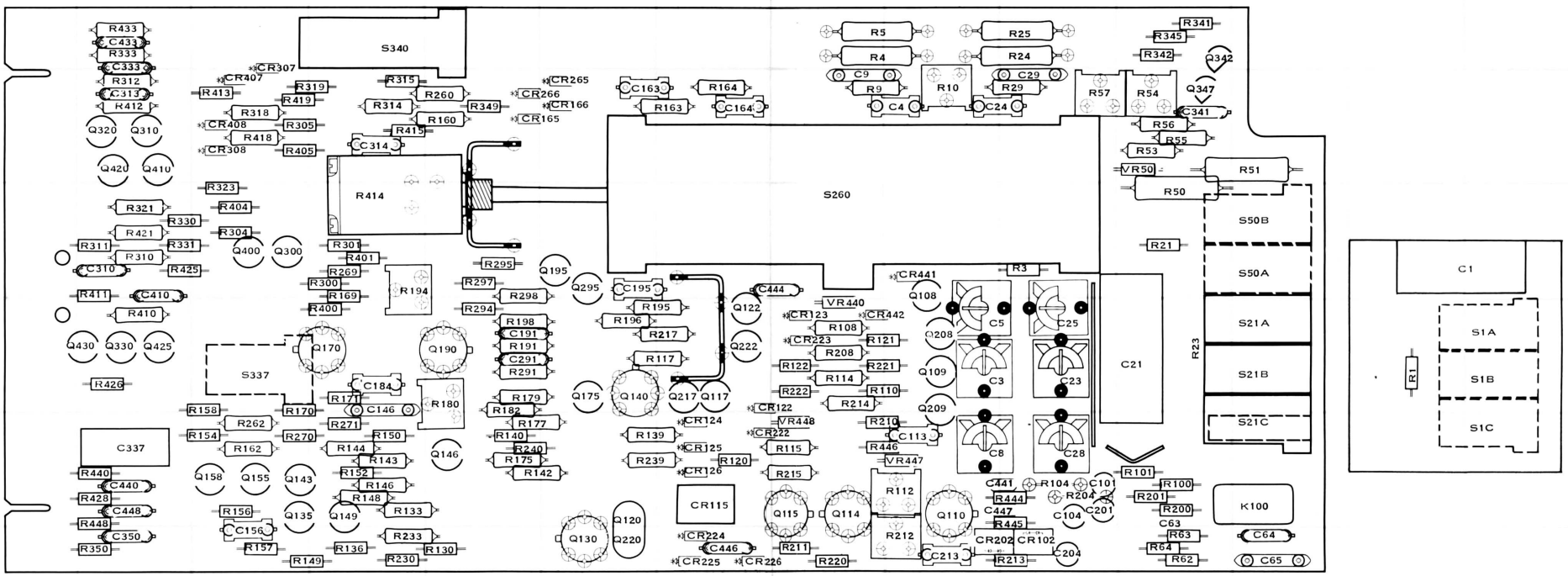
Differential amplifier Q320-Q420 receives the triggering signal from the emitters of Q310-Q410. The triggering signal is amplified and passed through emitter follower Q425, where it is made available to an associated time-base unit via output contact A4. The triggering signal is of the same polarity as that applied to the gate of Q110A, and has an amplitude of about 0.25 volt per displayed division.

Vertical Switching and Readout

The VOLTS/DIV switch, S260, is made up of a series of cam lobes, which engage and disengage various contacts at different positions of the switch. The contacts that are engaged at any given position of the switch are shown by black dots on the switch logic diagram.

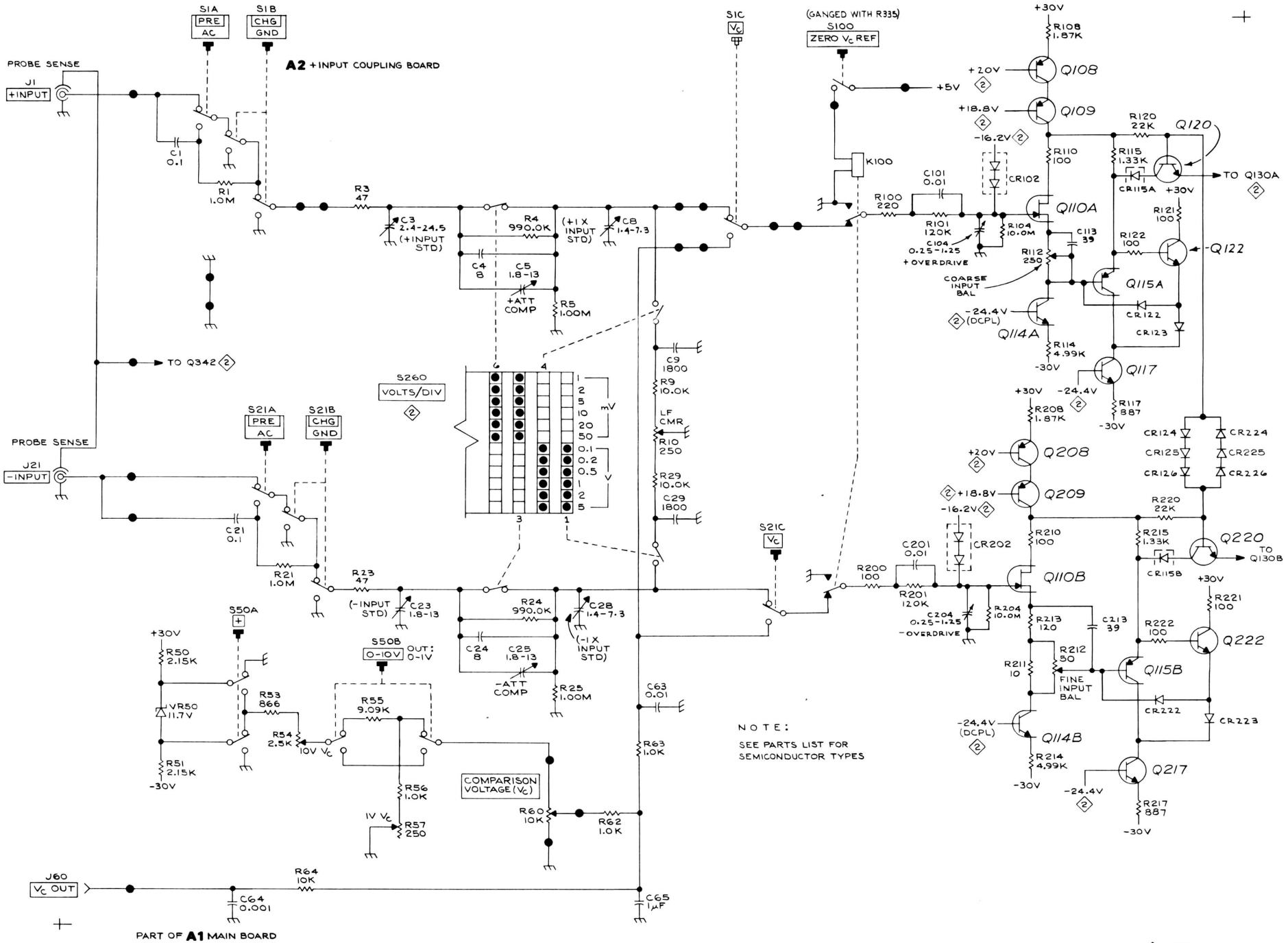
Either of two lamp bulbs located behind the knob skirt of the VOLTS/DIV switch lights the selected deflection factor to provide a direct readout. Normally DS342, which is physically located behind the upper left portion of the knob skirt, is lit. Connection of a readout-coded 10X probe to either input connector automatically changes the readout by a factor of 10 (i.e., turns off DS342 and lights DS347) to indicate the correction of probe attenuation. J1 and J21, the + and − INPUT connectors, have probe rings, allowing the 10X probe to apply a ground connection to the base of Q342. Q342 turns off, allowing Q347 to turn on, switching current from DS342 to DS347.


S340
(DISPLAY)
ON
READOUT SWITCHING
Q342 1X LAMP
Q347 10X LAMP
PLUG-IN LOGIC SWITCHING
A1
A19
B19
B18
S100
ZERO V_C REF
K100
+INPUT
+INPUT COUPLING & ATTEN S1A S1B
+V_C SWITCH S1C
+COMMON MODE CLAMP CR102
+INPUT SOURCE & EMITTER FOLLOWER Q108 Q109 Q110A Q115A Q122
CONSTANT CURRENT SOURCE Q114A Q117
DISCONNECT SWITCH Q120
POSITION
POSITIONING CURRENT DRIVER Q330 Q430
BOOTSTRAP Q146 Q149
GAIN
VARIABLE
DIFFERENTIAL SIGNAL CLAMP CR124 CR125 CR126 CR224 CR225 CR226
DIFFERENTIAL COMPARATOR Q130A Q130B Q140A Q140B
1X & 10X GAIN-SWITCHING AMP Q170A Q190A Q170B Q190B Q195 Q295
VARIABLE GAIN AMP Q300 Q310 Q400 Q410
+
-
SIGNAL OUT
VAR BAL
BANDWIDTH LIMIT
ATTEN BAL
CURRENT SOURCE Q135
CURRENT SOURCE Q175
TRIG AMP Q320 Q420 Q425
TRIG SIG OUT
CMR AMP Q155 Q158
BIAS Q143
-INPUT
INPUT COUPLING & ATTEN S2A S2B
-V_C SWITCH S2C
-COMMON MODE CLAMP CR202
-INPUT SOURCE & EMITTER FOLLOWER Q208 Q209 Q110B Q115B Q222
DISCONNECT SWITCH Q220
V_C SUPPLY VR50
COMPARISON VOLTAGE (V_C)
+
S50A
0-10V
S50B
CONSTANT CURRENT SOURCE Q114B Q217



NOTE. COMPONENTS SHOWN WITH DASHED LINES ARE LOCATED ON BACK SIDE OF BOARD.

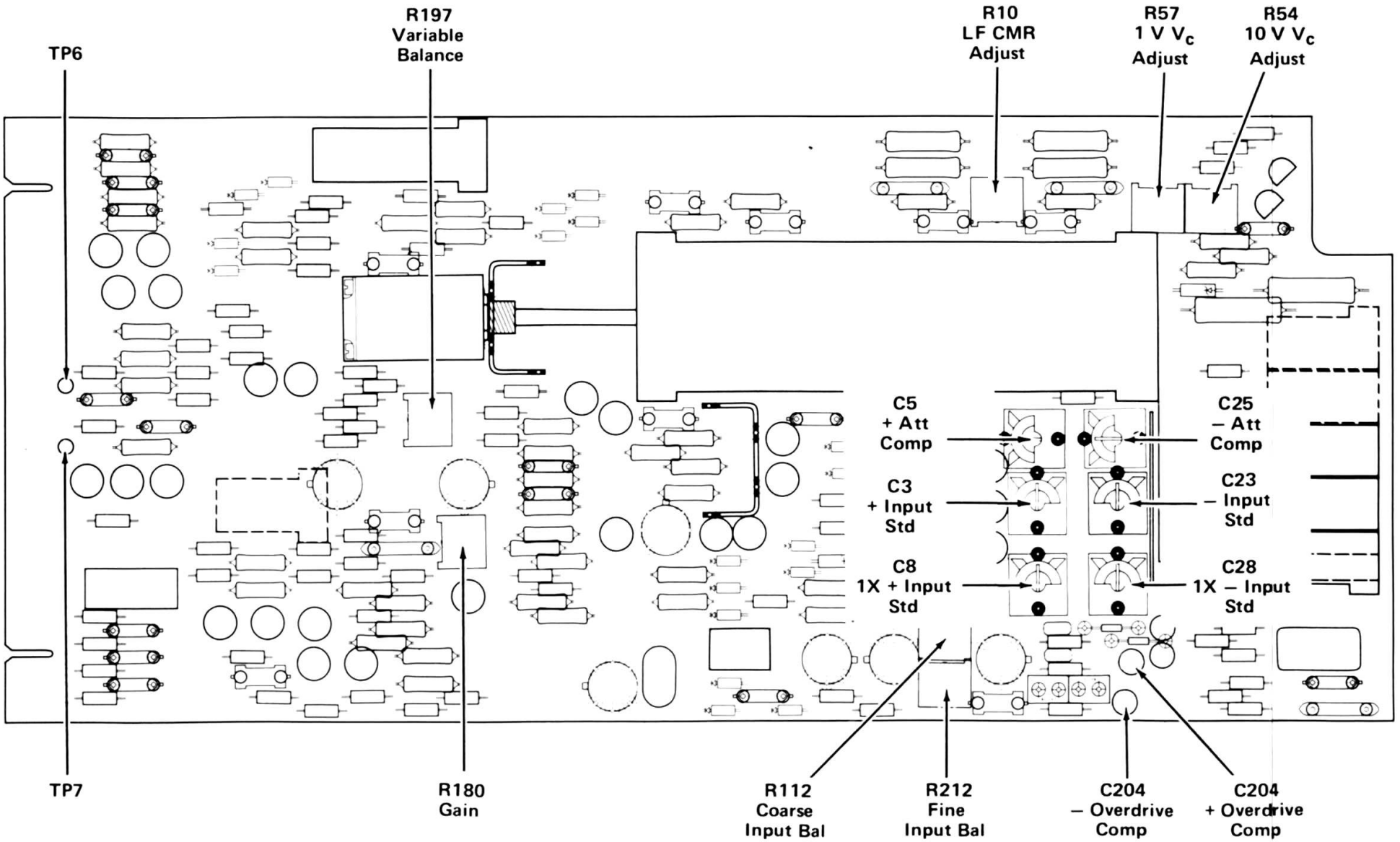
Fig. 4-1. Component location grid. See parts list for coordinates.

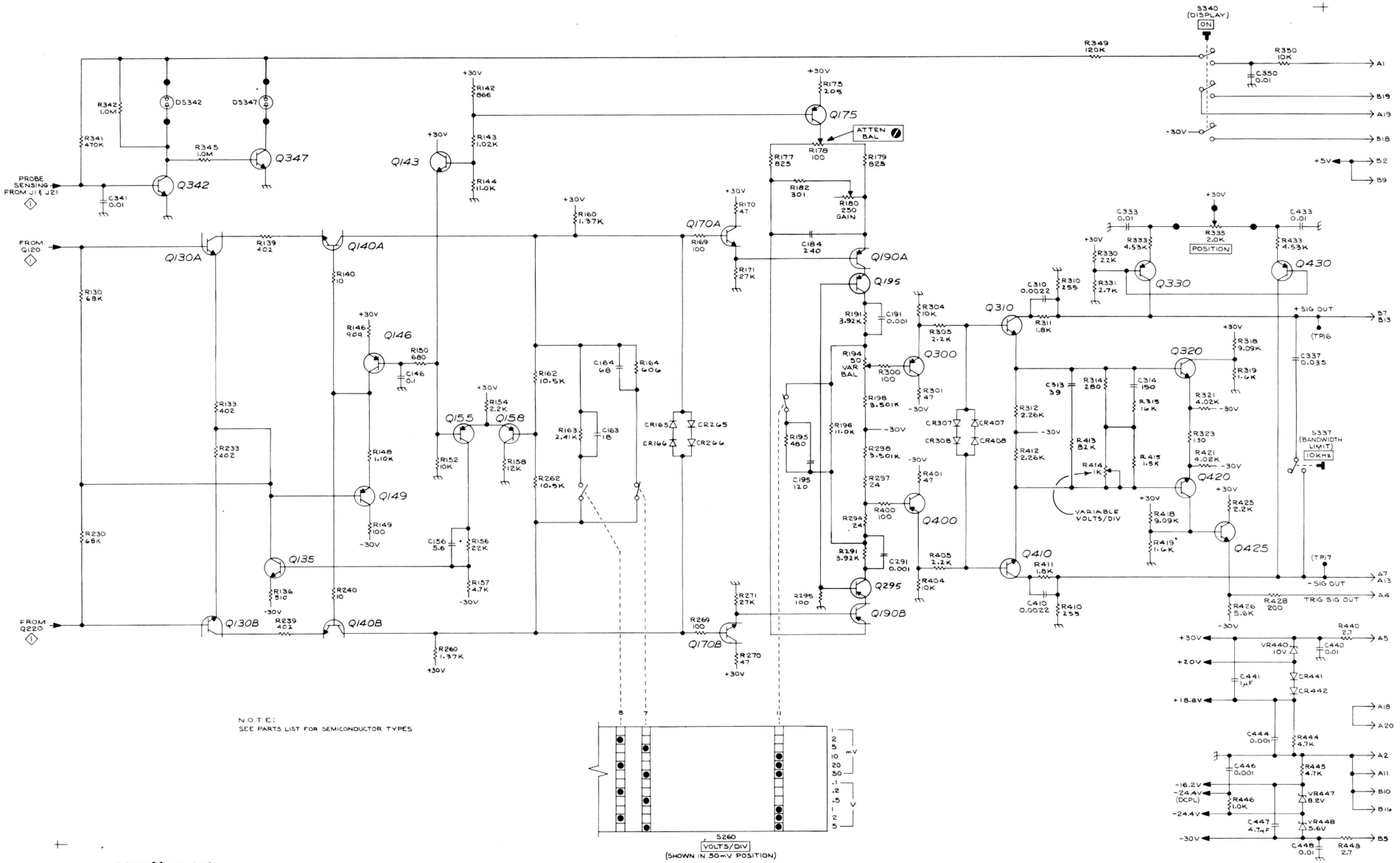


5AI3N

INPUT CIRCUIT & V_C SUPPLY 1 GRS 1171

5A13N


TP6
R197
Variable
Balance
R10
LF CMR
Adjust
R57
1 V V_c
Adjust
R54
10 V V_c
Adjust
C5
+ Att
Comp
C25
– Att
Comp
C3
+ Input
Std
C23
– Input
Std
C8
1X + Input
Std
C28
1X – Input
Std
TP7
R180
Gain
R112
Coarse
Input Bal
R212
Fine
Input Bal
C204
– Overdrive
Comp
C204
+ Overdrive
Comp


S340 (DISPLAY) ON
R349 120K
R350 10K
C350 0.01
A1
B19
A19
B18
+5V
B2
B9
-30V
DS342
DS347
R342 1.0M
R341 470K
R345 1.0M
Q347
Q342
C341 0.01
PROBE SENSING FROM J1 & J21
+30V
R142 866
R143 1.02K
R144 11.0K
Q143
R175 205
Q175
ATTEN BAL
R178 100
R177 825
R179 825
R182 301
R180 250 GAIN
C184 2.40
Q190A
Q195
R191 3.92K
C191 0.001
R194 50 VAR BAL
R198 3.501K
R196 11.0K
R195 480
C195 120
R298 3.501K
R297 24
R294 24
R291 3.92K
C291 0.001
Q295
Q190B
R295 100
R160 1.37K
R170 47
Q170A
R169 100
R171 27K
R269 100
Q170B
R271 27K
R270 47
R260 1.37K
FROM Q120
FROM Q220
Q130A
Q140A
Q130B
Q140B
R139 402
R239 402
R140 10
R240 10
R130 68K
R230 68K
R133 402
R233 402
R146 909
Q146
R150 680
C146 0.1
R148 1.10K
Q149
R149 100
Q135
R136 510
R154 2.2K
Q155
Q158
R152 10K
R158 12K
C156 5.6
R156 22K
R157 4.7K
R162 10.5K
R262 10.5K
C164 68
R164 606
R163 2.41K
C163 18
CR165
CR166
CR265
CR266
R304 10K
R305 2.2K
Q300
R300 100
R301 47
R401 47
Q400
R400 100
R405 2.2K
R404 10K
CR307
CR308
CR407
CR408
Q310
Q410
R310 255
C310 0.0022
R311 1.8K
R411 1.8K
C410 0.0022
R410 255
R312 2.26K
R412 2.26K
C333 0.01
R335 2.0K POSITION
C433 0.01
R333 4.53K
R330 22K
R331 2.7K
Q330
R433 4.53K
Q430
+SIG OUT
(TP)6
B7
B13
C313 39
R314 280
C314 150
R315 1.6K
R413 82K
R414 1K
R415 1.5K
VARIABLE VOLTS/DIV
Q320
R318 9.09K
R319 1.6K
C337 0.035
R321 4.02K
R323 130
R421 4.02K
Q420
R418 9.09K
R419 1.6K
R425 2.2K
Q425
S337 (BANDWIDTH LIMIT) 10KHz
(TP)7
-SIG OUT
A7
A13
TRIG SIG OUT
A4
R426 5.6K
R428 200
R440 2.7
A5
VR440 10V
C440 0.01
+2.0V
C441 1μF
CR441
CR442
+18.8V
A18
A20
C444 0.001
R444 4.7K
A2
C446 0.001
R445 4.7K
A11
-16.2V
-24.4V (DCPL)
R446 1.0K
VR447 8.2V
B10
B16
-24.4V
C447 4.7μF
VR448 5.6V
B5
C448 0.01
R448 2.7
S260 VOLTS/DIV (SHOWN IN 50mV POSITION)
5 2 1 .5 .2 .1 50 20 10 5 2 1 mV
.5 .2 .1 1 2 5 V
NOTE: SEE PARTS LIST FOR SEMICONDUCTOR TYPES
PART OF A1 MAIN BOARD
5A13N
DIFFERENTIAL AMPLIFIER 2 GR5 1171

TEXT CORRECTION

Page 1-6, Electrical Characteristics

CHANGE as follows:

POSITION RANGE. + and - approximately 8 divisions from graticule center.

INTERNAL COMPARISON VOLTAGE. Ranges, 0 V to ±10 V, and 0 V to ±1 V. Accuracy, within 0.2 % of dial setting plus 5 mV from ±1 V to ±10 V; within 0.2 % of dial setting plus 1 mV from ±25 mV to ±1 V on the 0 V to ±1 V range. Electrical zero is 0.5 mV or less; mechanical zero is 0.25 minor divisions or less.

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTION

MAIN Circuit Board Assembly

CHANGE TO:

C184	281-0605-00	200 pF, Cer, 500 V		
C314	281-0602-00	68 pF, Cer, 500 V, 5%		
R101	315-0104-00	100 kΩ	1/4 W	5%
R182	321-0157-00	422 Ω	1/8 W	1%
R201	315-0104-00	100 kΩ	1/4 W	5%
R315	316-0273-00	27 kΩ	1/4 W	10%
R415	315-0182-00	1.8 kΩ	1/4 W	5%

ADD:

C323	281-0524-00	150 pF, Cer, 500 V		

ELECTRICAL CHARACTERISTICS

DEFLECTION FACTOR. 1 mV/div to 5 V/div. 12 calibrated steps in a 1-2-5 sequence. Accuracy is within 2%. Uncalibrated variable is continuous between steps; its minimum ratio extends deflection factor to at least 12.5 V/div.

FREQUENCY RESPONSE (6 Division Reference). For DC-coupled input, overall bandwidth is DC to 2 MHz. AC-coupled input lower bandwidth frequency is 2 Hz or less at −3 dB. 10 kHz bandwidth mode, DC to 10 kHz within 2 kHz.

STEP RESPONSE (6 Division Reference). For either AC or DC coupled input risetime is 165 nanoseconds or less for all deflection factors.

INPUT R AND C. 1 MΩ paralleled by about 51 pF. Time constant normalized for 51 microseconds, within 3% between channels.

MAXIMUM SAFE INPUT VOLTAGES. For DC-coupled input, ±350 V (DC + peak AC, 1 kHz or less). For AC-coupled input, 350 VDC.

MAXIMUM INPUT GATE CURRENT. 100 picoamperes or less at +25°C.

COMMON-MODE SIGNAL RANGE. For deflection factors 1 mV/div to 50 mV/div, at least + and − 15 V; for 0.1 V/div to 5 V/div, at least + and − 350 V.

OVERDRIVE RECOVERY. 1 μs to recover to within 3.0 mV, and 0.1 ms to recover to within 1.5 mV after removal of signal between ±15 V.

COMMON-MODE REJECTION RATIO. At least 10,000:1, DC to 10 kHz at 1 mV/div to 50 mV/div DC coupled, with up to 20-volt peak-to-peak sine wave, decreasing to 100:1 at 1 MHz. At least 400:1, DC to 10 kHz at 0.1 V/div to 5 V/div DC coupled, with up to 100-volt peak-to-peak sine wave, decreasing to 40:1 at 1 MHz. For frequencies above 5 kHz AC coupled, CMRR is the same as stated for DC coupled. Below 5 kHz AC coupled, CMRR decreases to 400:1 at 10 Hz.

POSITION RANGE. At least + and − 8 divisions from graticule center.

INTERNAL COMPARISON VOLTAGE. Ranges, 0 V to ±10 V and 0 V to ±1 V. Accuracy, within 0.2% of dial setting plus 0.05% of full scale. Electrical zero is 0.5 mV or less, mechanical zero is 0.25 minor dial divisions or less.

COMPARISON VOLTAGE OUTPUT JACK. V_C OUT resistance is 15 kΩ ±5 kΩ, electrical zero is 0.5 mV or less.