INSTRUCTION MANUAL

Serial Number labo CEA

TYPE 4S2A DUAL-TRACE SAMPLING UNIT

Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon 97005 ● Phone 644-0161 ● Cables: Tektronix
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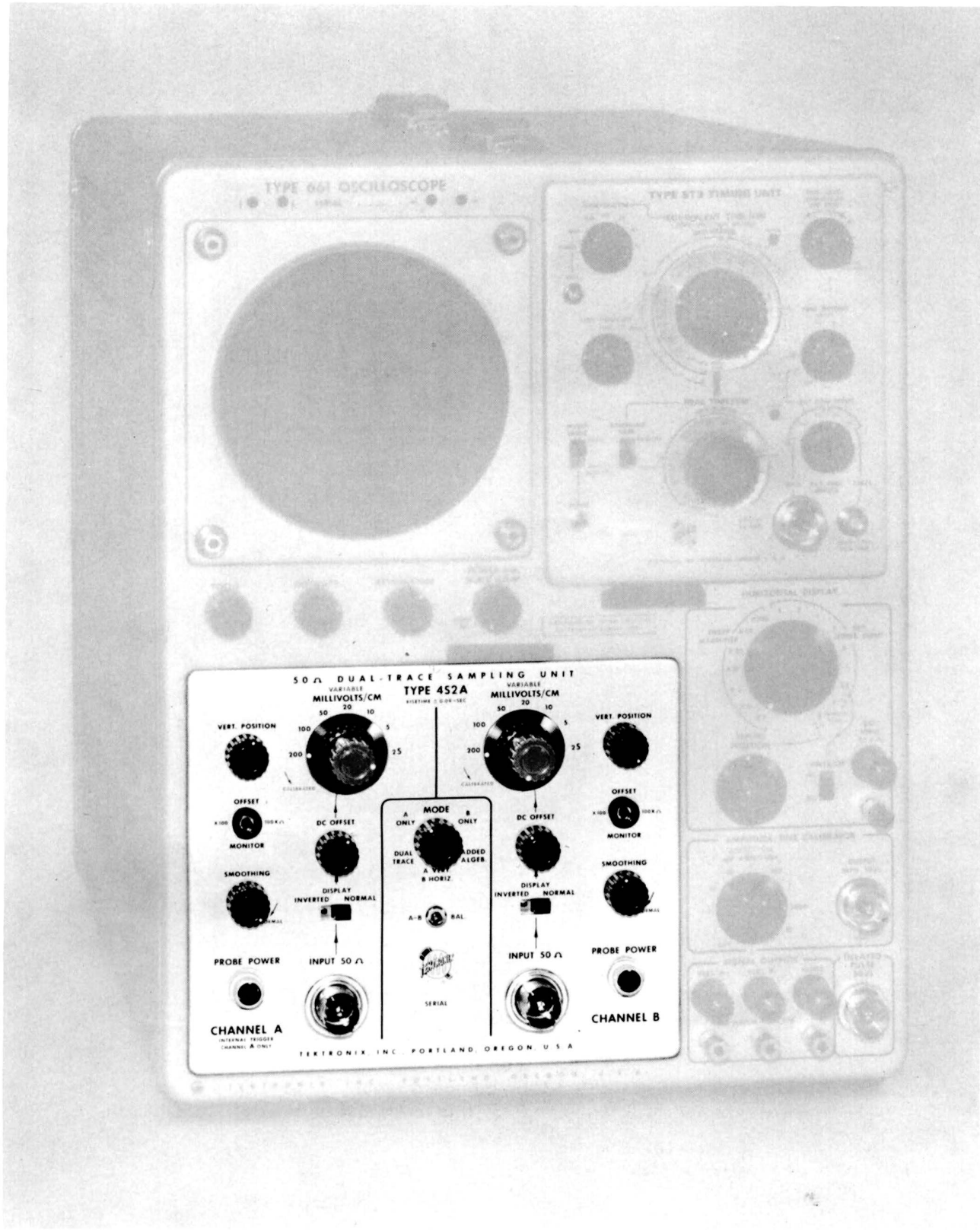


Fig. 1-1. Type 4S2A Dual-Trace Sampling Unit.

SECTION 1

CHARACTERISTICS

General Description

The Tektronix Type 4S2A 50 Ω Dual-Trace Sampling Unit is a vertical channel plug-in unit for the Type 661 Oscilloscope. When used in a sampling system consisting of the Type 661 Oscilloscope, Sampling Time Base Unit, and the Type 4S2A, the Type 4S2A enables the system to present accurate single- or dual-trace displays of repetitive high-speed signals with fractional nanosecond risetime. Such a system produces a CRT display by reconstructing the signal waveform from a series of single samples taken from many repetitions of the input signal. The Type 4S2A gives such a system an equivalent bandwidth of at least 3.9 GHz.

ELECTRICAL CHARACTERISTICS

The following characteristics indicated by footnote (1) apply over an ambient temperature range of 0° C to +50° C. Warm-up time for the given accuracy is 20 minutes.

Operating Modes

A Only, B Only, Dual Trace, Added Algebraically, and A Vertical—B Horizontal (X-Y) operation.

Rejection ratio for Added Algebraic mode is 40:1 or better when each channel is driven with a 1-volt flat-topped pulse and the deflection factor is 50 mV/cm, each channel.

Switching frequency in Dual Trace operation is approximately 50 kHz.

Deflection Factors

Calibrated steps of 2, 5, 10, 20, 50, 100, and 200 mV/cm. Accuracy[1] with the DISPLAY switch in the NORMAL position is ±2.5%; with the switch in the INVERTED position, accuracy is ±3%.

Risetime (T_r)

Risetime of the Type 4S2A is 90 ps or less, 10% to 90%.[2] Risetime and transient response of a randomly selected production-line unit are shown in Fig. 1-2. (Typical frequency response and VSWR curves are shown in Fig. 1-3.)

The displayed output of either or both channels can be presented either normally or inverted, premitting the addition or subtraction of dual-trace displays. This versatility is valuable in X-Y displays for observation of hysteresis loops, or for inverting the phase of signals into or out of an amplifier for phase comparison. Inverted operation can add an additional ½% error to the deflection factors.

[1]**Performance requirement checked at the factory.**

[2]**T_r is somewhat dependent on ambient temperature. Adjustment of Bridge Volts Control may be necessary if operation at extremes of specified temperature range is required.**

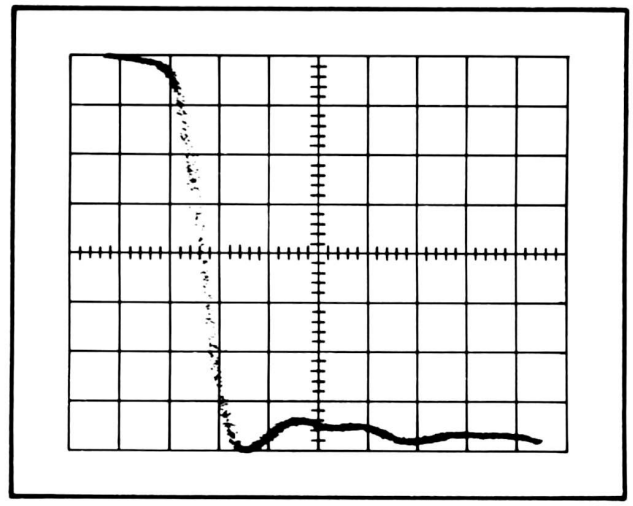


Fig. 1-2. Photograph showing risetime and transient response of the Type 4S2A. Horizontal scale 100 picoseconds/division.

Display Noise

At a deflection factor of 5 mV/cm, SMOOTHING control adjusted to unity dot transient response, MODE switch at A ONLY, B ONLY, or A VERT B HORIZ, 80% of the dots are within 4 mV peak to peak. With the MODE switch at DUAL TRACE or ADDED ALGEB, 80% of the dots are within 5 mV peak to peak. With the SMOOTHING control fully counterclockwise, 80% of the dots are within 2 mV peak to peak.

Smoothing

Each Channel SMOOTHING control permits reduction of random noise. The SMOOTHING control also permits adjustment of servo loop gain to exactly unity dot transient response (DTR).[3] At 200 mV/cm, the trace will not move more than 1.5 cm while rotating the SMOOTHING control.

Memory Drift

The sampling dot vertical stability is such that no drift is visible when triggering at a rate above about 150 Hz. At a triggering rate of 50 Hz, the dot drift does not exceed 0.2 cm.[1]

Co-Channel Time Coincidence

Dual-trace display of a fast-rise pulse will produce no more than a 20-picosecond time difference between channels.

[3]**Setting the SMOOTHING control for a DTR <1 helps to reduce random noise effects when operating in equivalent time and at low deflection factors. When operating a sampling system in real time mode with a timing unit such as the Type 5T3, certain measurements require that the SMOOTHING control have sufficient range to permit the Type 4S2A DTR to be adjusted through unity.**

DC Offset

The DC component of a signal can be offset up to ±1 volt (with a five-turn control) to bring a display back onto the CRT, or to make an incremental measurement.

Offset Monitoring

The voltage change at the front-panel OFFSET MONITOR jack is 100 times the voltage change (±1%) of the display produced by use of the DC OFFSET control.[1] The OFFSET MONITOR jack permits accurate measurement of DC voltage level changes.

Input Impedance

50 ohms ±1% at DC. Fig. 1-3 shows input VSWR to 5 GHz. Passive probes, cathode follower probes and a 1 megohm to 50 Ω probe adapter are available for higher input impedance at reduced sensitivity and/or bandwidth.

Probe Power

The two front-panel PROBE POWER connectors permit operation of Tektronix cathode-follower probes and accessory devices.

Input Coupling

DC coupled from the 50 Ω input connectors to the sampling bridges.

Dynamic Range

Input signals as high as ±1 volt can be viewed without overloading the system. Safe overload is ±5 VDC, or 10 volt peak-to-peak pulses if the duty factor is 50% or less.

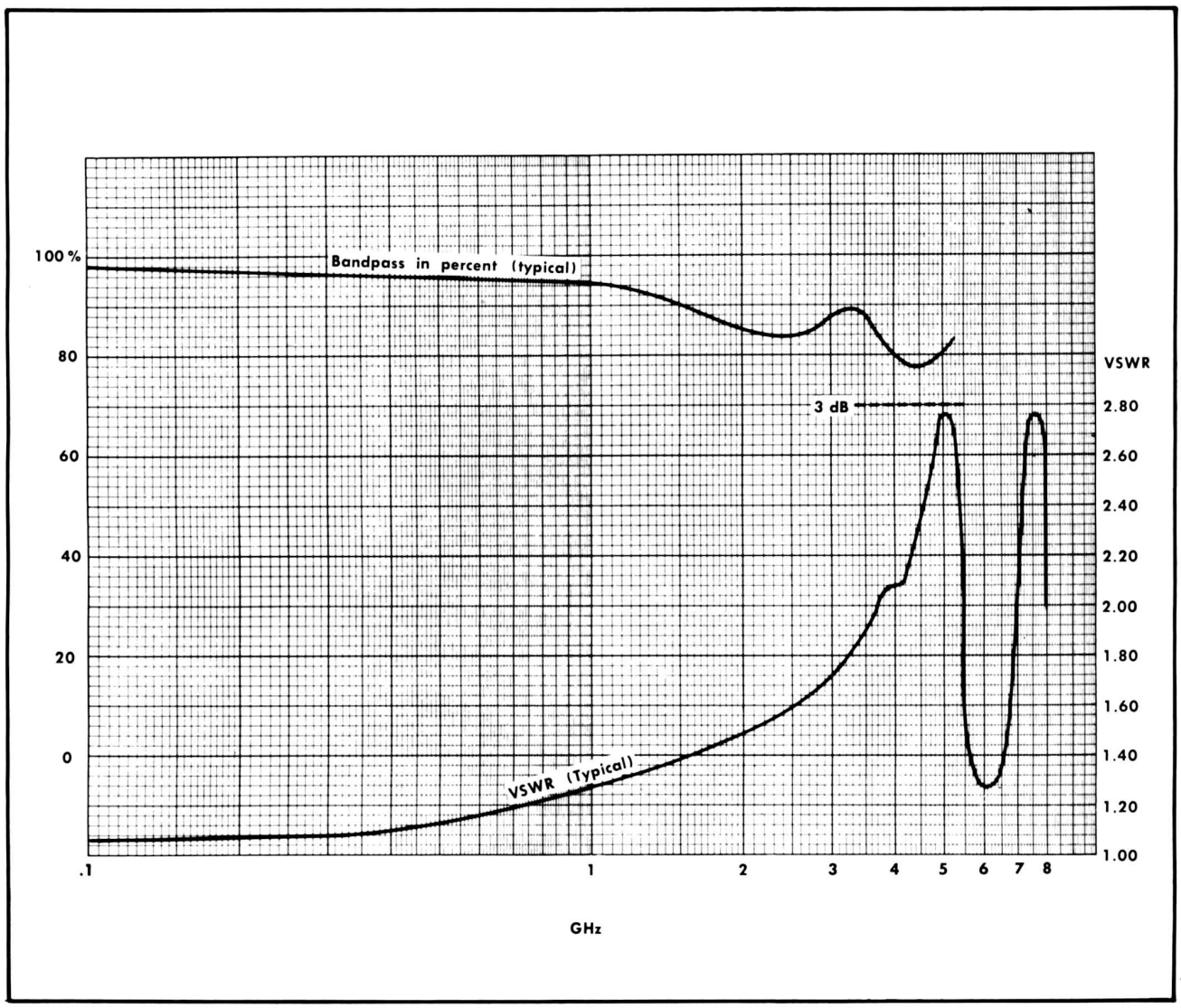


Fig. 1-3. Typical Type 4S2A VSWR and relative amplitude response to sine waves.

Triggering Output

Internal triggering takeoff from Channel A only. The amplitude of the trigger output to the time base unit is 0.1 × signal voltage. Risetime of the trigger pulse is less than 1 ns, 10% to 50%.

Signal Outputs to Type 661

The signal output voltages to the Type 661 are within 3% of a 1-volt signal applied to the input connectors when the deflection factor is 200 mV/cm (this 3% figure does not include any error that may be introduced between the output of the Type 4S2A and a reading obtained from the CRT display).

ENVIRONMENTAL CHARACTERISTICS

Temperature

Operating—0° C to +50° C.

Non-Operating— —40° C to +65° C.

Altitude

Operating—15,000 feet maximum

Non-Operating—50,000 feet maximum

MECHANICAL CHARACTERISTICS

Construction

Aluminum-alloy chassis with six plug-in circuit card assemblies. The front-panel is anodized and printed.

Forced-air cooling is provided by the fan in the Type 661, which means that the oscilloscope system should be operated with side panels in place. A constant temperature is important for proper operation of the instrument.

Dimensions

Height 7 inches, width 8½ inches, depth 14 inches.

Weight

9 pounds, 9 ounces.

STANDARD ACCESSORIES

Standard accessories supplied with the Type 4S2A are listed on the last pullout page at the rear of this manual. For optional accessories available for use with this instrument, see the current Tektronix, Inc. catalog.

SECTION 3
CIRCUIT DESCRIPTION

Introduction

This section of the manual contains a block diagram analysis of the Type 4S2A followed by a detailed circuit description. The reader will find it helpful to refer to Basic Sampling Techniques in Section 2 of this manual if the purpose of a particular circuit is not immediately clear.

BLOCK ANALYSIS

The Type 4S2A simplified block diagram of Fig. 3-1 shows each circuit in block form, with all front panel and internal controls identified. Since the two channels are identical except for the internal trigger pickoff circuit, only the Channel A circuits are identified.

Trigger information (either picked off the input signal or externally applied) to the Timing Unit starts the sampling cycle. The Timing Unit in turn sends command pulses to the Type 4S2A Gate Generator. The Gate Generator sends very short duration push-pull pulses to both Sampler circuits, and slightly longer duration push-pull pulses to both Memory circuits. The two sets of pulses from the Gate Generator connect first the sampling gates to the sampler preamplifiers, and then connect the AC Amplifier to the Memory circuits.

Input signals travel through about three inches of 50-ohm air line into the Sampler which includes the sampling gate, charge-nulling amplifier, trigger pickoff, and sampler preamplifier. When the command pulse is received from the Gate Generator via J7, the sampling gate is biased to conduction. The sampling gate output signal is a series of pulses (one for each command pulse), which are amplified by the sampler preamplifier and coupled through the MILLIVOLTS/CM switch into the AC Amplifier. The AC Amplifier (gain of about 300) amplifies the signal and presents it to the Memory. The Gate Generator biases a gate at the Memory input to conduction as the signal arrives.

The Memory amplifies and stores the signal. The Memory output is applied to two circuits, one of which leads back to the Sampler, the other leading to the Type 661 indicator. The signal sent back to the Sampler sets the input circuit to the voltage of the signal at the time the sample was taken. (When the SMOOTHING control is set to unity dot transient response, the next sample corrects only for any signal changes since the last sample.) The Memory output signal to the Type 661 can be inverted by a unity-gain inverter, or applied without inversion. After the normal-inverted choice is made, the outputs of both channels then pass through the Dual Trace electronic switch where either or both are sent on to the Type 661. The signal applied to the Type 661 is used to produce the CRT display.

CIRCUIT ANALYSIS

Input and Sampler

The input and sampler (shown in simplified form in Fig. 3-2) are the heart of the sampling system where the 90 ps risetime performance is established. Input connectors on the Type 4S2A are 50 ohm General Radio Type 874 connectors. These connectors simplify input cabling problems and ensure close tolerance (1%) of the 50 ohm input impedance. The input termination is made up of a series-parallel resistor network which provides proper termination and a trigger pickoff point. Power dissipation rating of the terminating resistors limits the applied voltage to + or — 5 VDC, or pulse inputs of 10 volts peak to peak at 50% duty cycle.

The relay contacts shown in Fig. 3-2 represent an equivalent method of applying forward bias to the sampling gate and do not exist in the actual equipment. The sampling diodes D1011 and D1012 are normally reverse biased about 3 volts, but if the relay is momentarily closed, the gate becomes forward biased, permitting the signal to be applied to the sampler preamplifier. The actual forward biasing signal lasts slightly less than 90 ps; its period is so short, in fact, that the stray capacitance C_s of the input circuit combined with the input impedance and the series resistance of the sampling diodes limit the signal to the sampler preamplifier to about 2.5% of the input amplitude.

Operation of charge-nulling amplifier Q1004 (see circuit diagram at the rear of this manual) is explained as follows: If a square-wave signal is applied to the sampler gate, a charge of the amount C_dV is coupled to the preamplifier (V1033) grid, C_d being the shunt capacitance of the gate diodes and V is the voltage of the square wave. This charge is known as blow-by. A gate with extremely bad blow-by problems works very well on short (2 ns wide) pulses or on a 100 MHz sine-wave signal. With signals of this type, the relatively slow preamplifier does not have a chance to operate on the blown-in charge before the charge is pulled back out of the grid. The charge-nulling amplifier used in the Type 4S2A operates by cancelling out all low frequency blow-by components upon which the preamplifier could operate. A small sample of the real time square-wave signal is taken off through R1001 in the input termination and inverted by Q1004. If a capacitor C_{null} (C1010) of the correct size is placed between the output of Q1004 and the preamplifier grid, then the blown-in charge C_dV will be pulled back out by the nulling amplifier. Any charge blown into the preamplifier grid by a square-wave signal will thus be pulled back out in less than 2 ns by the inverting amplifier and does not appear in the output of the preamplifier.

The BRIDGE VOLTS control (R1023) adjusts the reverse bias on gate diodes D1011 and D1012. A higher reverse voltage allows the sampler diodes to be turned on for a shorter period of time. A lower voltage gives a slower risetime. Feedback is brought into BRIDGE BAL potentiometer R1027, which is adjusted to compensate for diode, strobe, and other system unbalance signals in synchronism with the strobe generator.

The preamplifier uses a single 6688 tube (V1033) triode connected and run at a gm of 25,000 μmho. This tube provides impedance transformation for driving emitter follower Q1043. The emitter follower drives the emitter of Q1044 in the common base stage through C1042.

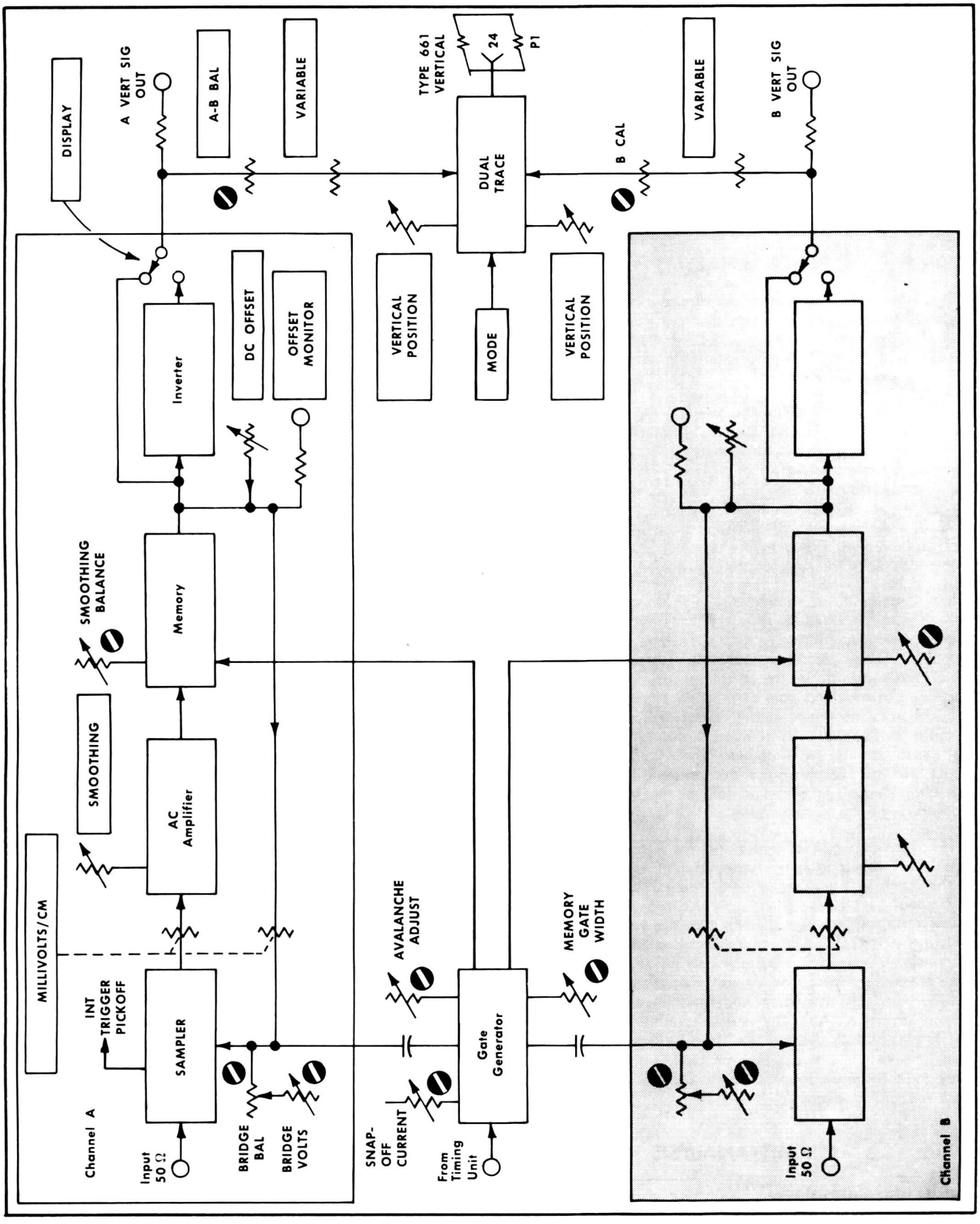


Fig. 3-1. Type 4S2A block diagram. Shaded area of Channel B is identical to corresponding area in Channel A.

Operation of the preamplifier is quite simple; a small sampled charge from the gate charges the grid-to-ground capacitance of V1033 to a small voltage V. This same voltage is made to appear across C1042, coupling the transistor emitters. A charge gain roughly equal to the ratio of emitter coupling capacitance to grid capacitance is achieved. Rise-time of the preamplifier is about 40 ns, and by operating both the emitter follower and the common base stages at the same quiescent current levels, the preamplifier has very close to the same response for both plus and minus signals.

In Channel A, the output load for nulling amplifier transistor Q1004 is connected to the emitter of the grounded base, isolation amplifier Q1014. The grounded base stage supplies AC coupled trigger information to the timing unit. No delay line is incorporated, so the leading edge of a pulse cannot be viewed without pre-triggering the timing unit. The trigger pickoff is provided primarily for viewing high repetition rate pulses or sine-wave signals.

Gate Generator

The Gate Generator circuit board contains two basic circuits; the strobe generator and the memory gate driver.

Strobe Generator. The strobe pulses that gate the sampling diodes into conduction are formed by a special snap-off diode (charge storage diode), D1066, driven by a base-triggered, NPN silicon avalanche transistor, Q1054. Transistor

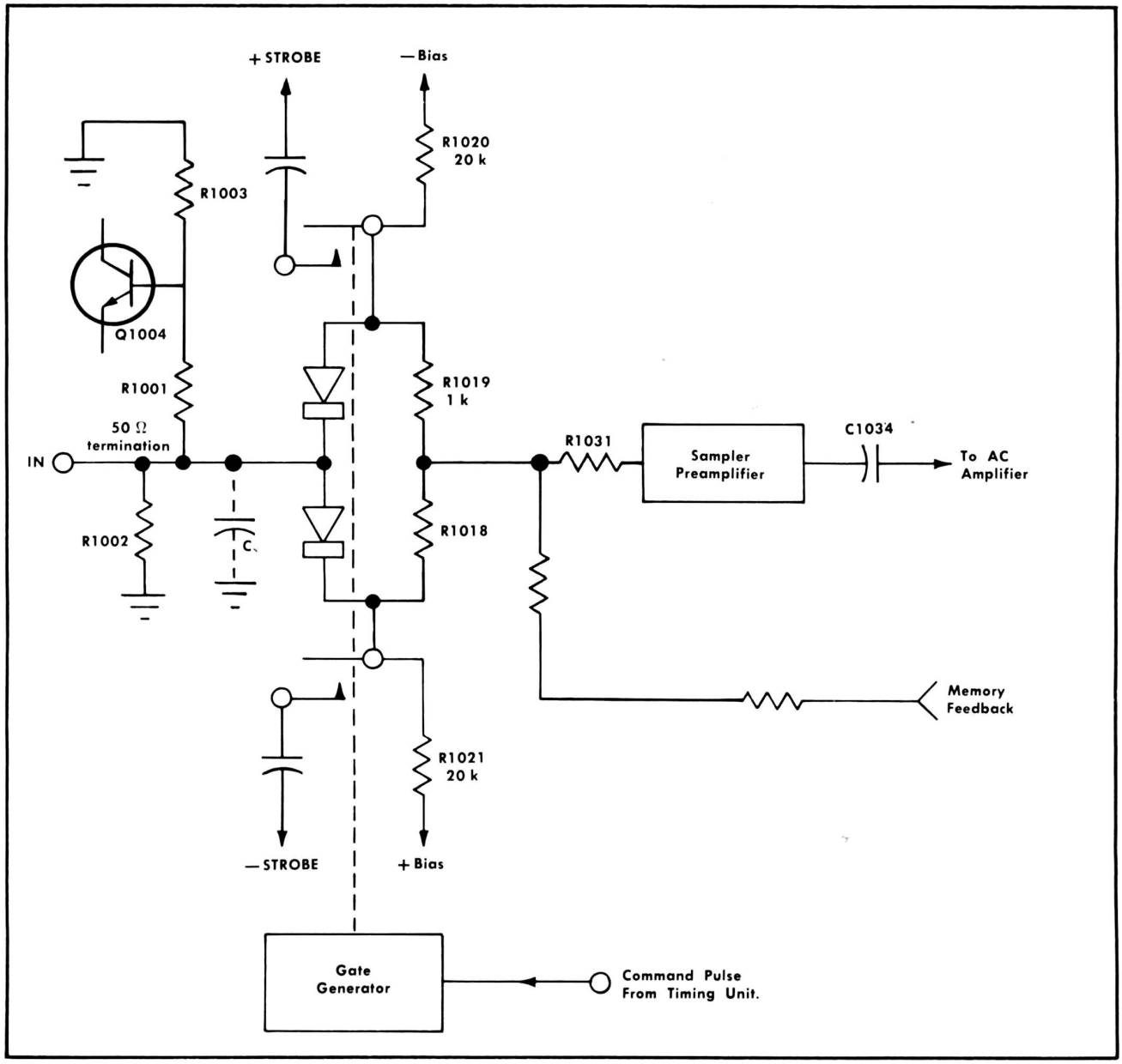


Fig. 3-2. Simplified sampling system input.

Q1054 is set for optimum operation by adjusting AVAL ADJ R1054, a 100 kΩ potentiometer that establishes the conducting bias of Q1053. The setting of R1054 and the conduction of Q1053 sets the collector voltage of Q1054 somewhere in the range between +100 and +175 volts since Q1054 operates without forward bias, and is normally non-conducting. The avalanche transistor is collector-coupled to the snap-off circuit through a small capacitor (C1058). The 10 kΩ collector load ensures ample time for the circuit to recover within a few tenths of a percent when operated at a 100 kHz repetition rate.

Between sampling-drive (trigger) pulses from the Timing Unit, snap-off diode D1066 is forward biased by the emitter current of Q1063. SNAP-OFF CURRENT adjustment R1063 adjusts the current through D1066, and thus adjusts the stored charge in the diode for best sampling efficiency. The 5-turn bifilar transformer changes the single-ended avalanche pulse output of Q1054 into a push-pull signal which reverse biases D1066. Diode D1066 is mounted in a very low inductance system of balanced clip lines and 50 Ω strip transmission lines for close control of the width and balance of the plus and minus strobe signals.

When a positive sampling drive pulse is received from the Timing Unit, the pulse is differentiated by C1051 and R1051, then applied to the base of Q1054. With the application of the pulse, Q1054 is biased into conduction, soon reaching the avalanche state and conducting very heavily. The collector voltage of Q1054 drops sharply, and the negative output of Q1054 is coupled through C1058 and R1058 to 5-turn pulse transformer T1065. The 5-turn pulse transformer turns the negative pulse into a push-pull signal which reverse biases D1066 and pulls out the charge stored therein. As soon as the charge is depleted, D1066 becomes a high impedance and the resulting fast voltage transition across the diode is sent through capacitors C1063 and C1064 to the clipping line. As the pulse travels down the clipping line, part of the energy is coupled out and sent to the sampling gates, biasing the sampling diodes into conduction. When the pulse hits the shorted end of the line, it is reflected back with opposite polarity, turning off the sampling gates.

Memory Gate Driver. Transistor Q1064 in the memory gate driver circuit operates as a saturated pulse standardizer, the output of which is applied to output transistor Q1074. The coupling circuit between the collector of Q1064 and the base of Q1074 consists of a ramp circuit. The collector voltage of Q1064, and therefore the height of the ramp, is set by MEMORY GATE WIDTH potentiometer R1067. The width of the ramp is determined by its height and the time constant of R1069 and C1068.

Under quiescent conditions, both transistors are biased to cutoff. Current flow through R1069 and series diode D1070 to the + 19-volt supply is 4 mA, 2 mA of which flows through R1071 from the —19-volt supply, the other 2 mA through shunt diode D1071 from ground.

The arrival of a sample drive pulse through L1051 and C1066 drives Q1064 into saturation for several hundred nanoseconds. The negative excursion of Q1064 collector is coupled to the base of Q1074 through C1068 and D1070. The negative pulse reverse biases D1070, and the junction of R1069 and D1070 is driven negative by the same amount that Q1064 collector voltage falls. Shunt diode D1071 turns off, and the 2 mA from the 10 kΩ resistor R1071 is now switched into Q1074, driving it into saturation. A memory drive pulse is thus started.

After this initial switching action, the Q1074 side of C1060 starts charging toward +19 volts from the current supplied to it by R1069. When the junction of R1069, C1068 and D1070 reaches +0.3 volts, D1070 turns on again and switches the charging current into the base of Q1074, turning off Q1074 and ending the memory drive pulse. A short time later Q1064 comes out of saturation, allowing the Q1064 side of C1068 to charge back toward the voltage value selected by the MEMORY GATE WIDTH Control.

AC Amplifier

The AC Amplifier receives its input signal (pulse) from the sampler preamplifier through the front panel MILLIVOLTS/CM switch, amplifies it 300 times, inverts it, and feeds the memory circuit. The input DC level (to ground) is zero, and the input resistance is switched from 25 ohms at 200 mV/cm to 1000 ohms at 5 and 2 mV/cm. The AC Amplifier is made up of two DC-coupled feedback amplifiers with a third DC feedback path around the whole circuit (see circuit diagram). The outside feedback path includes the front panel SMOOTHING control that allows a gain reduction of about 4 to 1 to reduce random noise. (When using SMOOTHING, the dot transient response must be considered and sufficient number of samples per centimeter obtained to make the display response correct.) The outside feedback path is for DC stabilization and does not act upon the main signal.

The signal pulses handled by the AC Amplifier are about 1 μs in duration. The amplifier output voltage can change 1.6 volts in about 0.1 μs. Normally the system causes the output pulses to be less than 1 volt, but if the display moves 8 centimeters in one sample, the output pulse will be about 1.6 volts peak. The output impedance of the circuit is low, so it can drive the memory input.

The gain of the first amplifier (Q1084 and Q1094) is about 45 when the SMOOTHING control (R1081) is set to NORMAL (zero resistance). The gain is set by the ratio of R1089 and R1083. When using full smoothing, the gain is about 8 to 10, set by the ratio of R1089 to R1083 and R1081 (SMOOTHING) in series. The gain of the second amplifier (Q1104 and Q1113) remains fixed at about 6, set by the ratio of R1107 and R1096.

The frequency response of the first amplifier is fixed-compensated by C1089. The second amplifier frequency response is adjusted during calibration by C1107.

Memory

A simplified schematic of the Memory circuit is shown in Fig. 3-3. The Gate Generator closes the Memory input gate (D1130 and D1131) at the correct time of each sampling cycle. The Memory circuit is a feedback amplifier with input and feedback elements both capacitors. The input capacitor is C1121, the feedback capacitor is C1132. V1133A (see circuit diagram) is an input cathode follower, Q1134 is the amplifier, and Q1141 is an output emitter follower.

The input impedance at the grid of V1133A acts as a virtual ground because as the input signal changes the grid voltage, the signal is amplified and applied back to the input as negative feedback to cancel the original change.

The action of the memory is to transfer a charge from C1121 to C1132. The circuit between the AC Amplifier output and the grid of V1133A looks like 150 ohms and 510 pF in series (when the memory gate is conducting). Thus, as a signal appears at the AC Amplifier output, C1121 is charged. C1121 tries to couple the signal to the grid of V1133A, but feedback prevents the grid voltage from changing significantly; the result is that both C1121 and C1132 receive a charge.

When the memory gate is not conducting, the grid of V1133A has a very high impedance to ground, and at this time the only possible discharge path for C1132 is by V1133A grid current or leakage current. The grid current is very low, and can be either positive or negative. Total leakage current is so low that there is essentially no change in the output voltage between samples even when sampling at the low rate of 150 dots/sec.

The circuit elements between C1121 and the grid of V1133A serve several purposes:

1. D1125 and D1127 are amplitude-limiting diodes. They normally do not conduct.

2. D1122 is a 6-volt Zener to provide back-bias for the gating diodes D1130 and D1131.

3. The resistors all aid in standardizing the input quiescent voltage level.

4. T1130 is a pulse transformer that allows instantaneous turn-on of the gating diodes to connect the input circuit to V1133A.

5. C1122 assures that both sides of D1122 follow the signal equally.

Within the memory amplifier:

1. C1138 corrects for transistor phase shift.

2. D1136 permits Q1134 to turn on hard, long enough for the stored charge (of D1136) to be removed, preventing damage to Q1134 in the event of turn-on overload.

3. D1142 assures that fast positive pulses at the base of Q1141 will be coupled to C1132 and the output, even if Q1141 has been momentarily cut off.

4. D1144 limits the positive swing of the output lead to about 10 volts and D1143 assures a high impedance when D1144 is reverse biased.

5. D1140 sets the maximum collector voltage of Q1141 at —9 volts.

6. R1145 prevents reverse reflections in the output cable from disturbing the display.

Between samples, the AC Amplifier output returns to its quiescent level, and C1121 charge (that was gained at the last sample) is cancelled. At the last sample, if there is any change at the sampler unit, C1121 will receive a new charging signal and can add to or subtract from the residual charge of C1132.

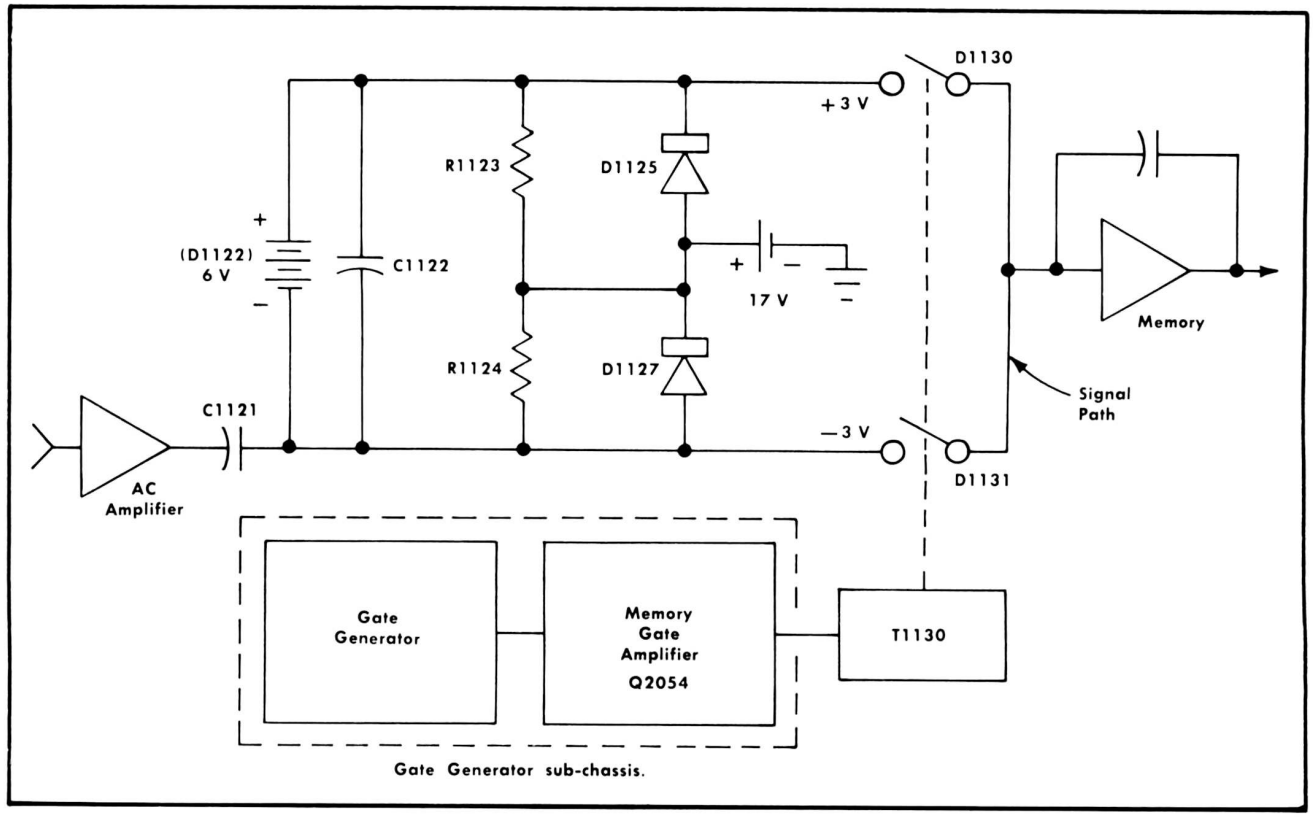


Fig. 3-3. Simplified memory gate.

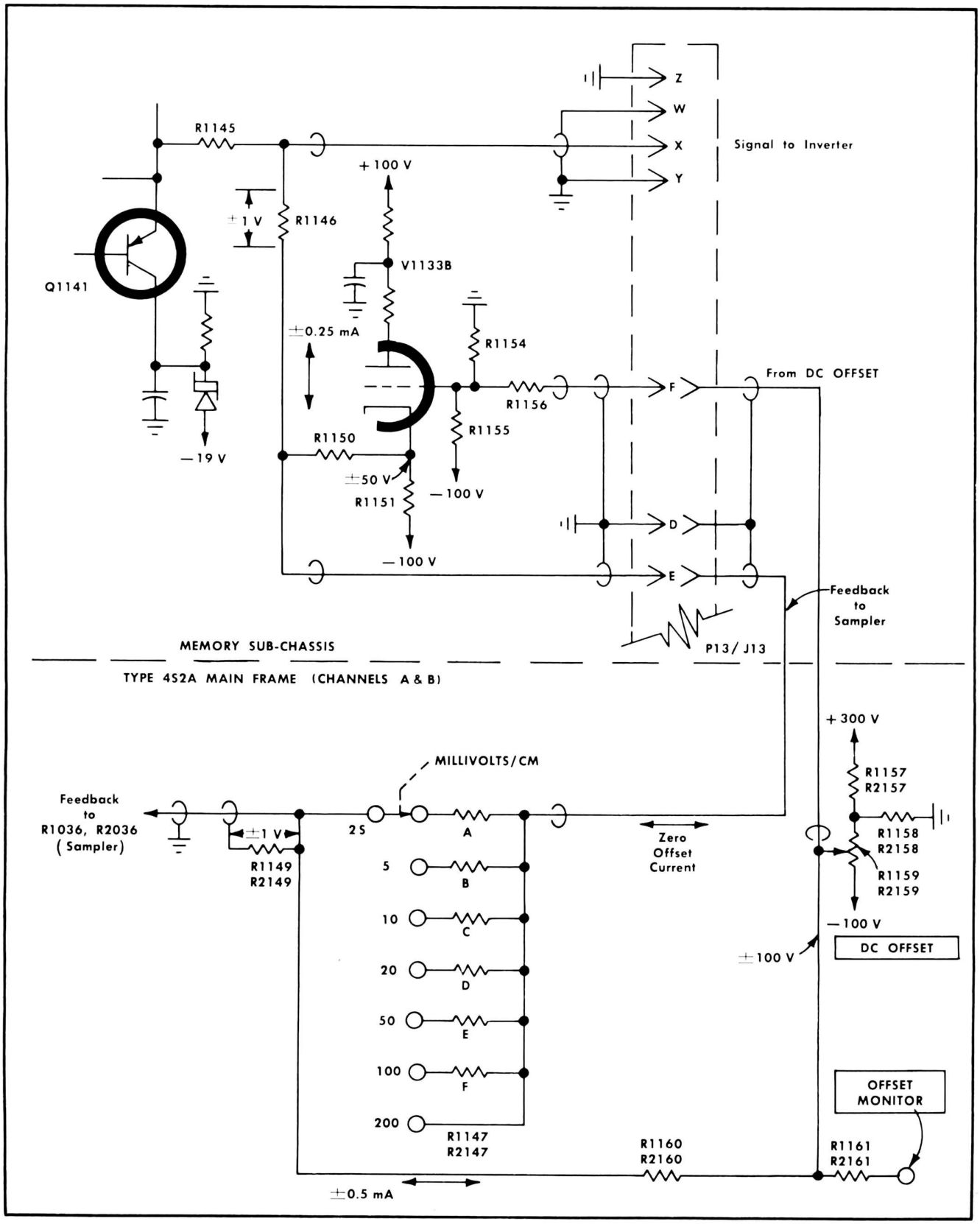


Fig. 3-4. DC Offset and Memory Feedback circuit.

System Operation With No Signal

Items to remember when examining signals at various points between the sampler amplifier output and the memory output:

1. It is impossible to install perfectly balanced sampling gate diodes, so at each interrogation there will be some small error signal sent into the system.

2. The memory circuit does not retain a perfectly stable output voltage because C1132 cannot hold a charge permanently.

3. The memory output is coupled back to the sampler input (with proper attenuation).

4. Theoretically, if there is no input at the sampling gate, there will be no AC Amplifier signal, and the memory output will be zero. The memory output will be essentially zero, but there will always be a small pulse at the AC Amplifier output.

5. The SMOOTHING BALANCE control (R1125) sets the quiescent DC level at the memory input and if incorrectly adjusted will cause an offset voltage that looks like a continuous signal. For example, assume the SMOOTHING BALANCE control is off by +1 mV. If the memory amplifier internal gain is 500 (it isn't actually), the memory output will now be off by —500 mV. The —500 mV feedback to the input bridge creates an error signal which will drive the memory output nearly back to zero. After several dots the memory output will stabilize near zero, but slightly off from zero to provide enough error signal to correct for the original +1 mV error. Thus, a continuous minor error signal is amplified to place the output level near zero. If the AC Amplifier gain is reduced by the SMOOTHING control, the memory output must now be larger so the error signal fed into the AC Amplifier is larger, restoring again the —1 mV correction at the memory input. (A trace shift seen when the SMOOTHING control is rotated away from NORMAL is the increased memory output to make up for the reduced amplifier gain). Thus the memory input balance control is called the SMOOTHING BALANCE because its effect is seen by rotation of the SMOOTHING control.

DC Offset

The memory output of Q1141 is fed to the inverter or to the dual trace circuit. It is also fed to a voltage divider that controls the feedback signal sent to the sampler. The feedback attenuator resistors, R1147, (Plug-In Connectors and Switching diagram, Channel A) set the feedback amplitude to keep the basic memory output of 600 mV/cm while the feedback voltage just matches the input signal.

The DC Offset circuit adds a DC shift to the feedback loop. It includes a current cancelling system that prevents offset current from flowing in R1147; see Fig. 3-4. The grid voltage of V1133B is set by the DC OFFSET control through a resistance divider. Rotating the DC OFFSET control from one end to the other causes a ±50 volt swing at the cathode of V1133B. The cathode of V1133B drives ±0.25 mA through R1146 via R1150. The DC OFFSET control ±100-volt swing drives ±0.2 mA through R1149 via R1160. The resulting voltage drop of ±1 volt across both R1146 and R1149 is the offset voltage sent to the sampler amplifier. The two points of offset injection ensure there is no offset current in R1147 so that the offset system is not affected by the MILLIVOLTS/CM switch.

The DC OFFSET control may be used to null certain levels of the input signal in order to measure amplitude. The OFFSET MONITOR jack allows a voltmeter connection to read the effective DC offset voltage ×100. The offset voltage is also useful when measuring small signals riding on larger signals.

Inverter

The Inverter is an ×1 amplifier pair (10 kΩ input, 10 kΩ feedback) for each channel. Its function is to invert the display when the front panel DISPLAY switch is in the INVERTED position. When the DISPLAY switch is in the NORMAL position, the inverter is bypassed by interconnecting wiring in the Type 4S2A main frame.

Q1164 is collector coupled to Q1163. D1167 is a voltage offset Zener to raise the voltage at the base of Q1163 above that at the collector of Q1164 without signal attenuation. Q1163 is an output emitter follower. R1161, the A INVERTER ZERO control, and R1162 are a DC balance network to adjust the output DC level, eliminating trace shift when moving the DISPLAY switch from NORMAL to INVERTED. R1163 is the feedback resistor.

Dual Trace

The Dual Trace subchassis determines which channel is displayed by the Type 661; under some conditions, the signals from both channels are fed to the Type 661. Because of the various modes of operation possible in dual-trace, both the A and B channel will be discussed.

Two gated inverter amplifiers, Q1184 and Q2184 (see circuit diagram) control passage of the signal. A multivibrator, Q2245 and Q2255, controls the two amplifiers via switching diodes D1187 and D2187. Multivibrator operation is controlled by the front panel MODE switch. In the A ONLY, B ONLY, and A VERT B HORIZ modes, only one side of the multivibrator conducts. In the ADDED ALGEB mode, neither side conducts, and in the DUAL TRACE mode, the multivibrator free-runs at a switching rate of about 50 kHz. Q2264 provides a dual-trace blanking signal to the Type 661 when the multivibrator switches.

A 0.25-μs delay line couples the output signal from the dual trace unit to the Type 661 indicator. The delay allows the signal to pass properly with the Timing Unit unblanking of the Type 661 CRT.

Refer to Fig. 3-5, the Dual Trace, and the Plug-In Connectors and Switching diagrams during the following discussion. Each inverter is fed signals from the DISPLAY switch for its channel. The Channel A signal arrives through R1184, the Channel B signal arrives through R2182 and R2184. The inverter amplifier emitter circuits include positioning controls (R1180 and R2180) in parallel with the emitter return resistors (R1185 and R2185). Positioning is by current injection into the emitter circuits through R1181 and R2181. The major emitter current comes from the +19-volt supply, through MODE switch SW2190 and to the emitters through R1185 and R2185. In the ADDED ALGEB position of the MODE

switch, current limiting resistor R1179 is inserted in the emitter to keep the common output lead average voltage the same as when only one transistor is conducting.

The amplifiers are connected in a common-base configuration. The current at their collectors is switched between two paths by the multivibrator to connect or disconnect them from the common collector load, R1189. There is essentially no change in the current of either transistor whether it is connected to the output or not. The input impedance is that of the series input resistors, R1184 in channel A, and R2182 and R2184 in channel B. Since the emitters of both transistors rest at about +0.2 volts, R1183 and R2183 are used to offset the input voltage to zero. The —4.5 volt collector voltage is offset to zero (for the output lead) by the series combination of R1191 and R1192.

Fig. 3-6 shows the MODE switch connections that set the operating conditions of the multivibrator. During single channel operation, with only one side of the multivibrator conducting, the conducting transistor saturates and Zener diode D2251 conducts. In A ONLY operation, multivibrator transistor Q2255 operates in saturation, and its collector is held at about +0.4 volt by D2255. This reverse biases both D2258 and D1187, so that Q1184 supplies the output signal. Since transistor Q2245 is cut off, R2248 forward biases both D2248 and D2187, bypassing Q2184 from the output.

Operation in the A VERT B HORIZ mode sets the multivibrator and the inverter amplifiers the same as in the A ONLY mode. The Channel B signal bypasses the Dual Trace circuit and is fed separately to the Type 661 horizontal deflection system. In the B ONLY mode, operation of the multivibrator and inverter transistors is the reverse, with Q1184 disconnected and Q2184 supplying the output signal.

In the ADDED ALGEB mode, neither multivibrator transistor conducts. Both inverters are turned on, combining both

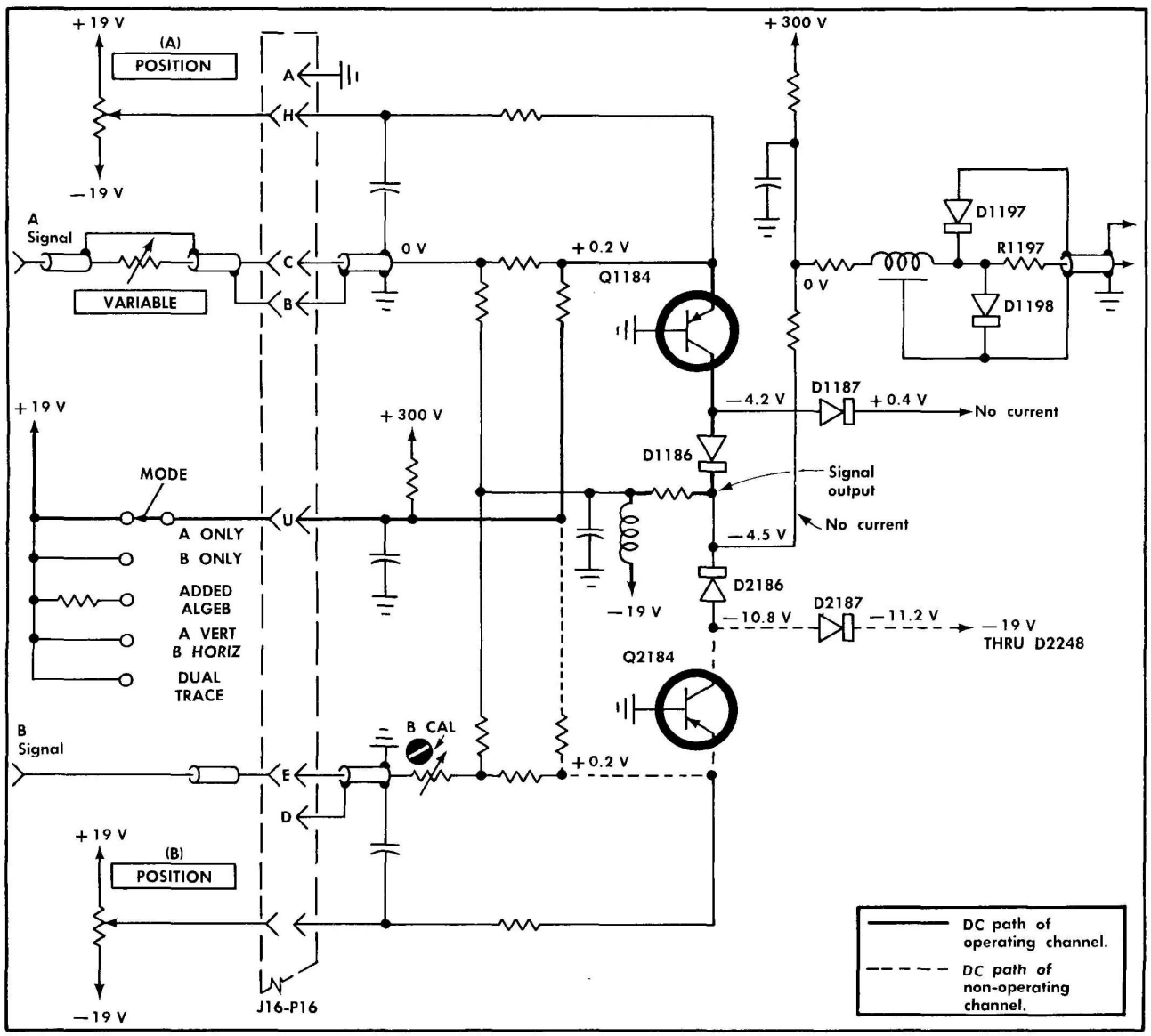


Fig. 3-5. Dual Trace circuit DC conditions. MODE A ONLY, DC OFFSET zero, trace centered, no signal, timing unit FREE RUN.

signals in the common collector circuit at R1189. The output to the delay line is the algebraic sum of the A and B signals.

In the DUAL TRACE mode, Q2245 and Q2255 operate as a free-running multivibrator at a frequency of at least 50 kHz. The inverter amplifiers pass signals alternately, providing a dual-trace display.

During multivibrator operation, neither transistor saturates, and Zener diode D2251 does not conduct. The multivibrator switching time constant, located between the emitters of Q2245 and Q2255, is composed of C2251 in series with the emitter return resistor (R2240 or R2250) of the non-conducting side. The collector-to-base coupling circuits (R2246-C2246 and R2256-C2256) do not set the time of operation; the capacitors are for high-frequency coupling to ensure fast switching.

Blanking Circuit

Blanking transistor Q2264 normally rests in cutoff with its base at about +0.8 volts. As the multivibrator switches, C2240 or C2250 couples about a —2 volt signal to the base of Q2264 to turn it on. The turn-on pulse lasts only about 0.5 μs, but it is heavy enough to saturate Q2264 and give it a storage time of about 1 to 1.5 μs. There is some positive overshoot immediately before the —2 volt pulse. This is kept from the base of Q2264 by D2262 so that the storage time of Q2264 will be fairly consistent, and the CRT will be properly blanked during the time the dual-trace multivibrator is switching channels.

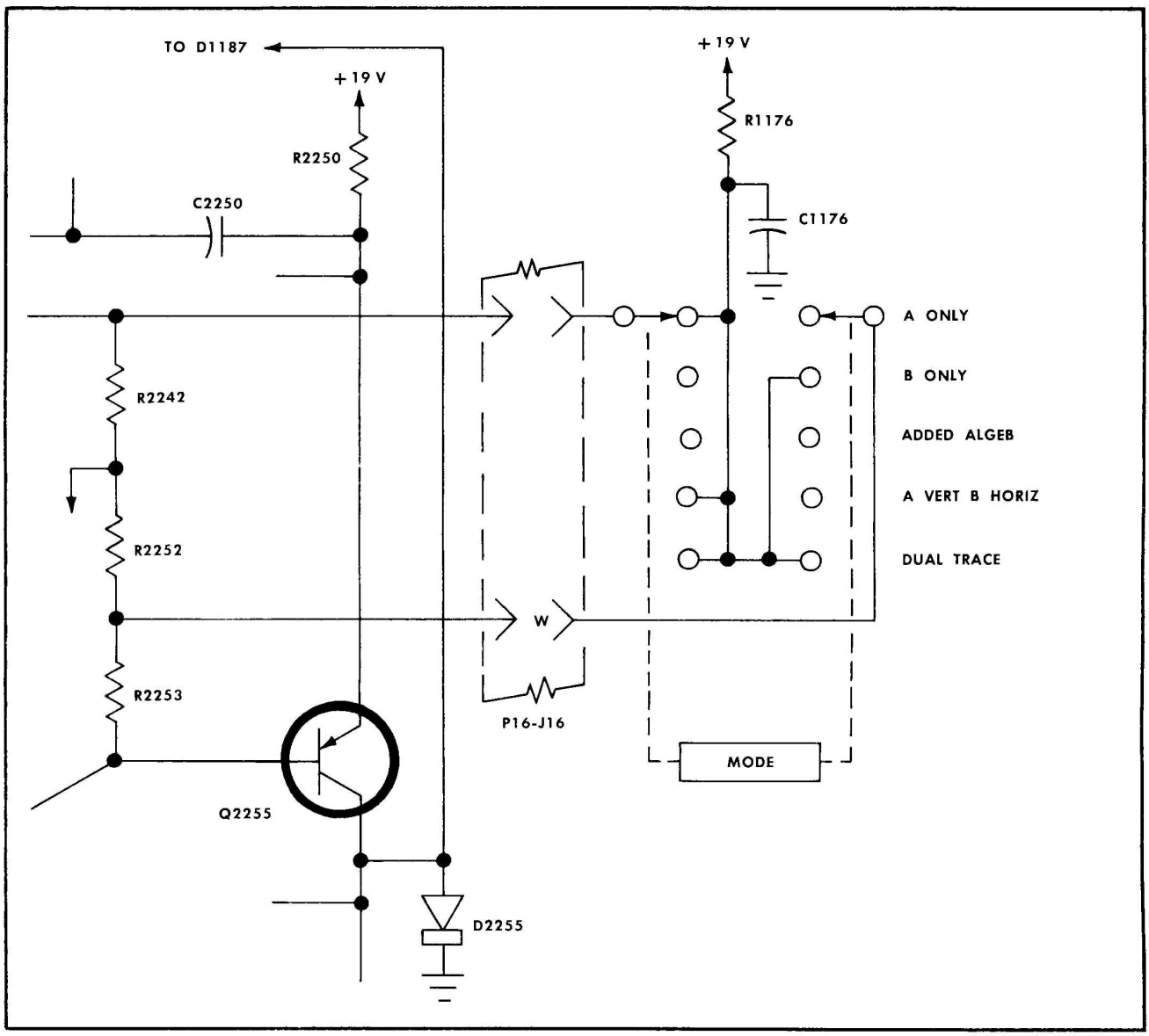
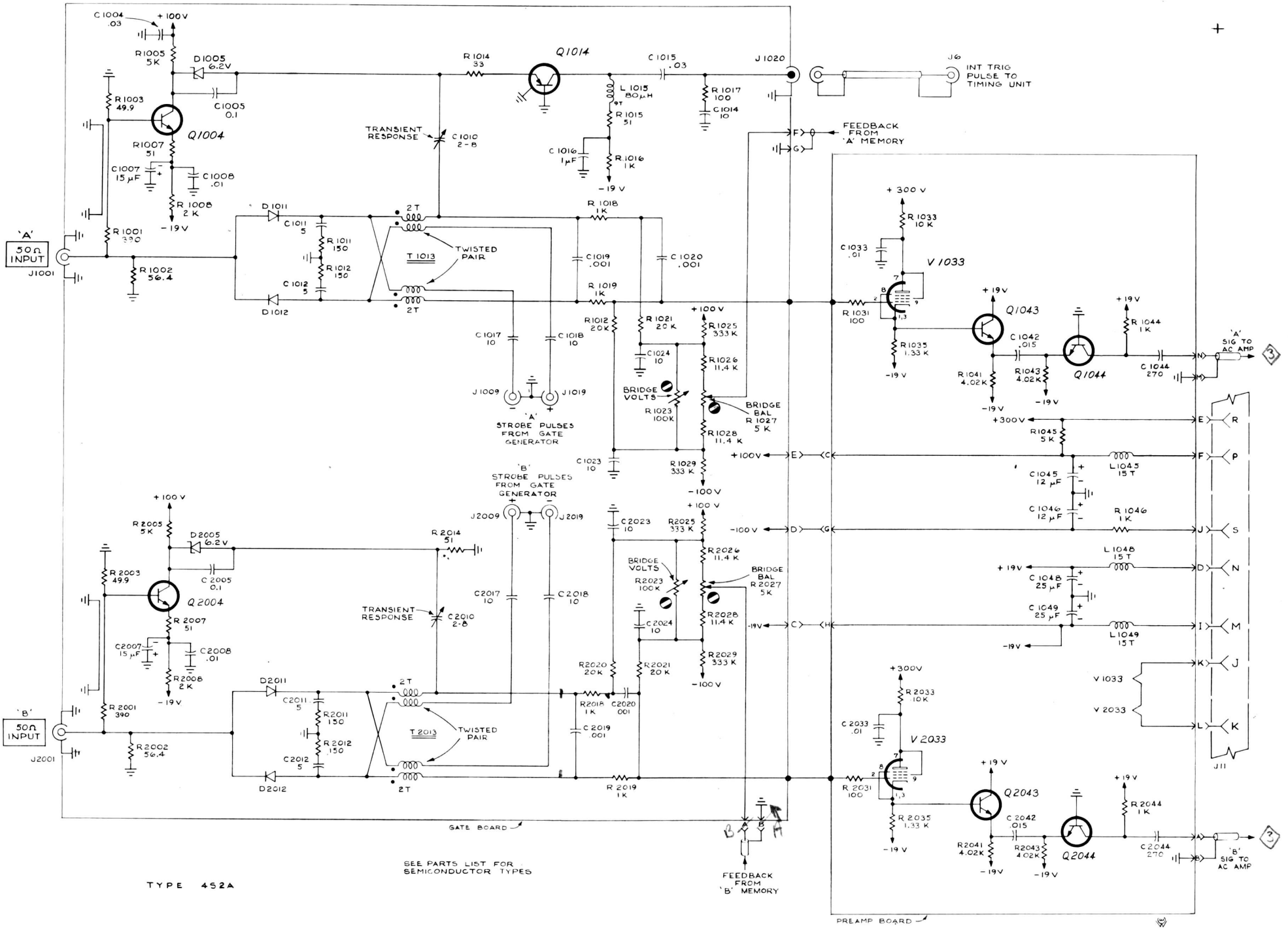
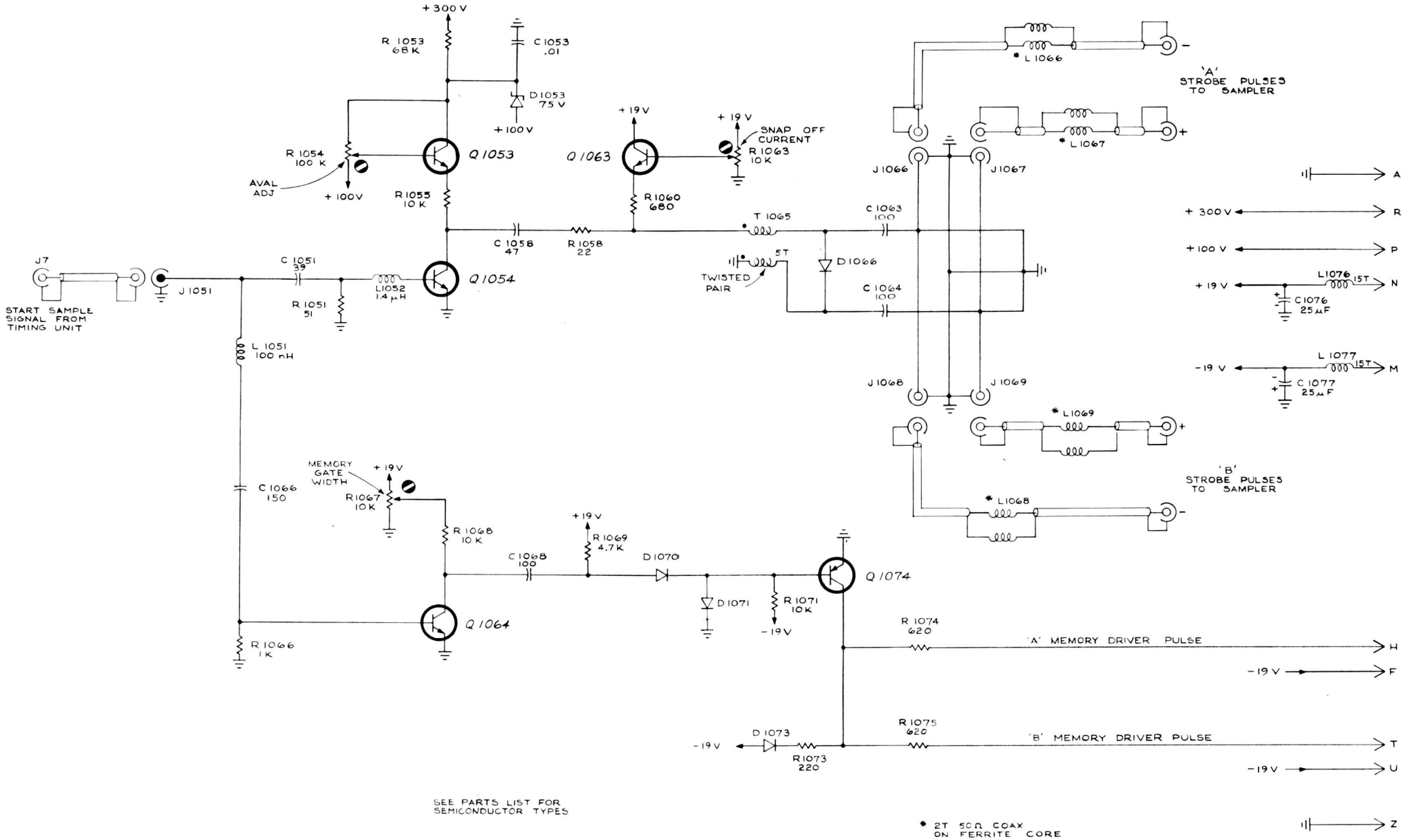


Fig. 3-6. MODE switch connections to the DUAL TRACE multivibrator.


'A' 50Ω INPUT
J1001
'B' 50Ω INPUT
J2001
+100V
-100V
+300V
-19V
+19V
Q1004
Q2004
Q1014
Q1043
Q1044
Q2043
Q2044
V1033
V2033
T1013
T2013
TWISTED PAIR
TRANSIENT RESPONSE
BRIDGE VOLTS
BRIDGE BAL
'A' STROBE PULSES FROM GATE GENERATOR
'B' STROBE PULSES FROM GATE GENERATOR
J1009
J1019
J2009
J2019
J1020
J6
INT TRIG PULSE TO TIMING UNIT
FEEDBACK FROM 'A' MEMORY
FEEDBACK FROM 'B' MEMORY
'A' SIG TO AC AMP
'B' SIG TO AC AMP
J11
GATE BOARD
PREAMP BOARD
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 452A
666
SAMPLER



SEE PARTS LIST FOR SEMICONDUCTOR TYPES

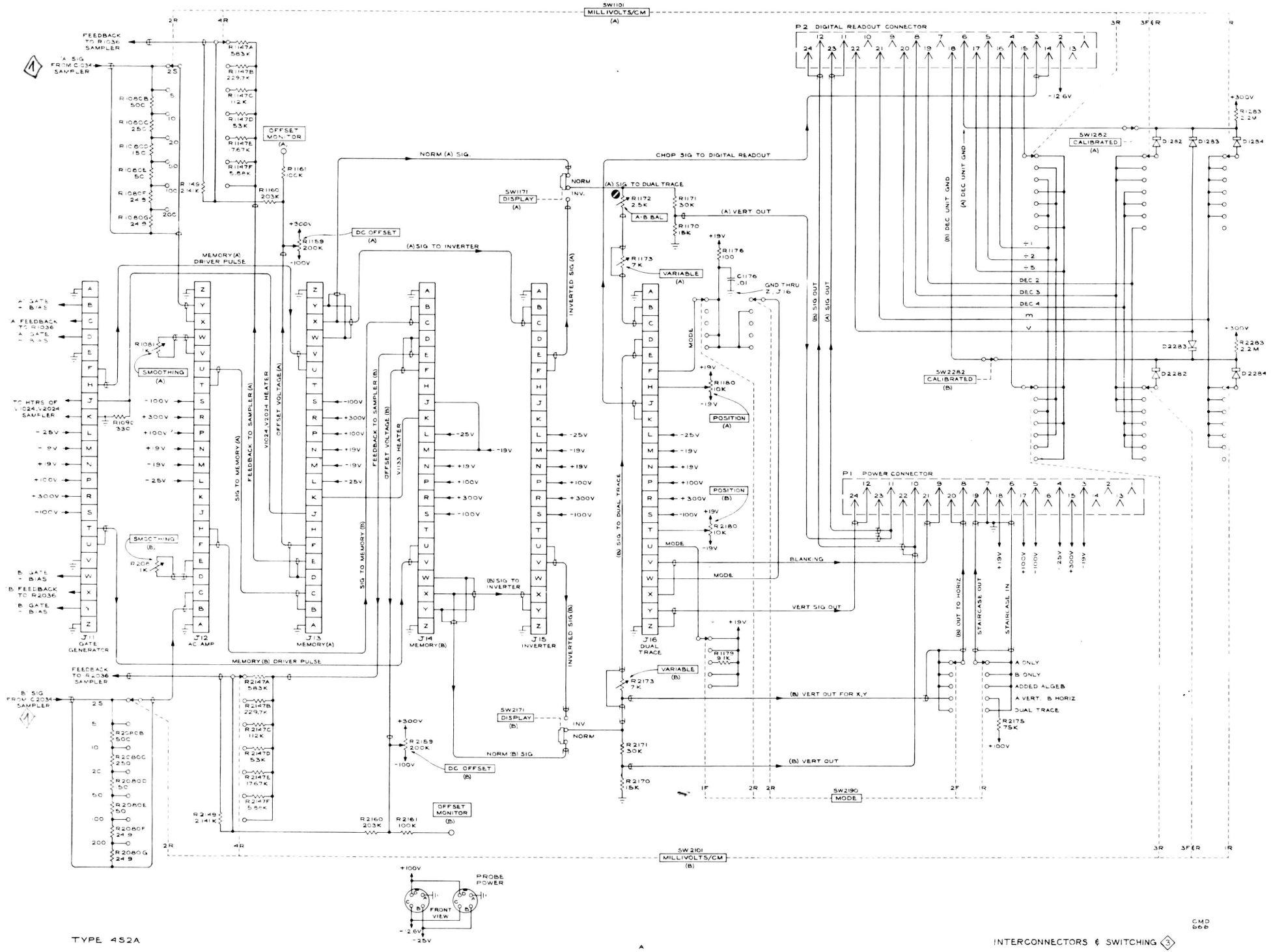
* 2T 50Ω COAX ON FERRITE CORE

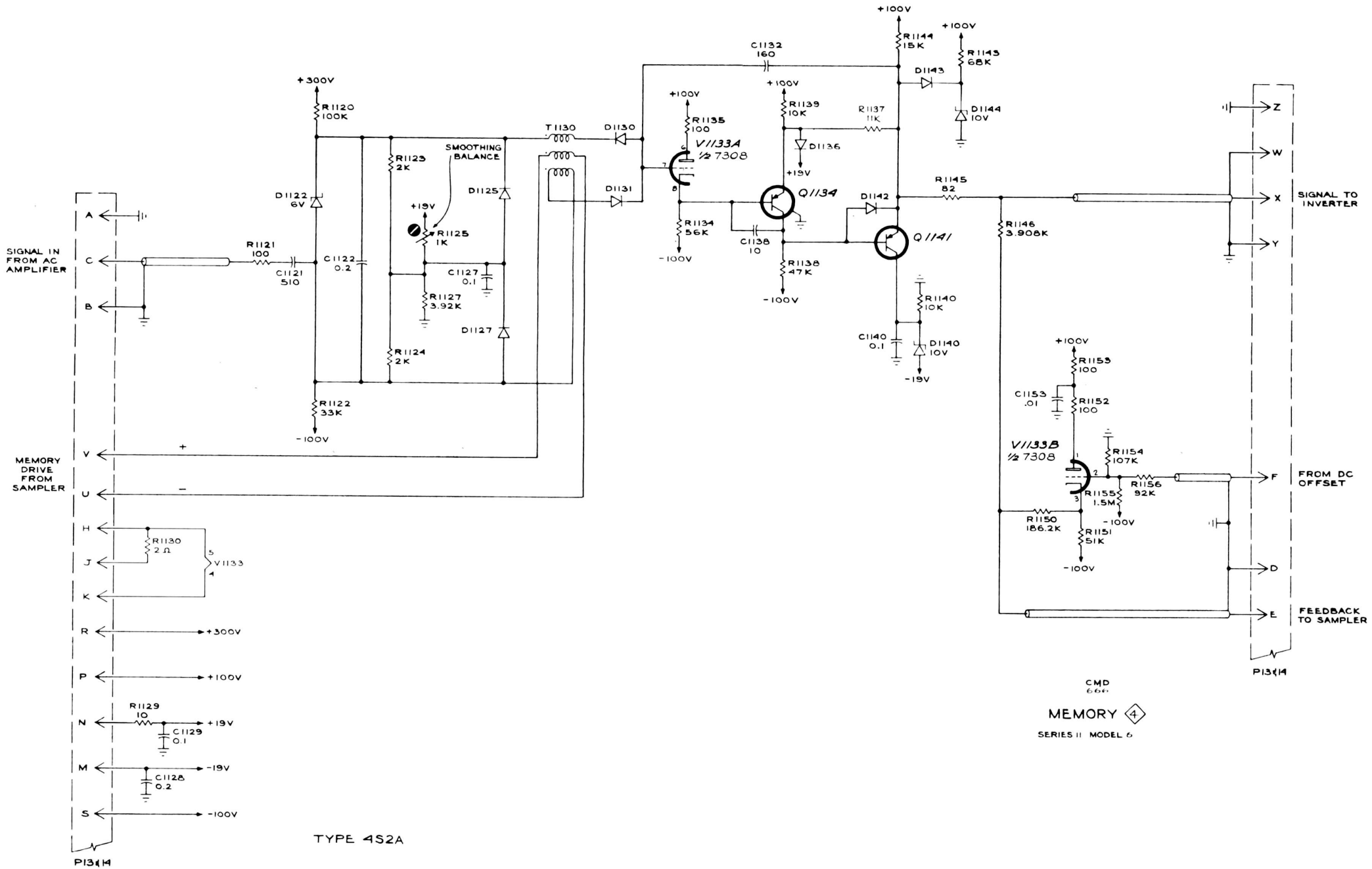
TYPE 452A

666

PULSE GENERATOR ②

SERIES 12


SW1101 MILLIVOLTS/CM (A)
P2 DIGITAL READOUT CONNECTOR
P1 POWER CONNECTOR
A SIG FROM C 2034 SAMPLER
B SIG FROM C 2034 SAMPLER
FEEDBACK TO R1036 SAMPLER
OFFSET MONITOR (A)
DC OFFSET (A)
NORM (A) SIG.
CHOP SIG TO DIGITAL READOUT
(A) SIG TO DUAL TRACE
A-B BAL
(A) VERT OUT
VARIABLE (A)
SW1171 DISPLAY (A)
NORM
INV.
(A) SIG TO INVERTER
MEMORY (A) DRIVER PULSE
SMOOTHING (A)
SMOOTHING (B)
POSITION (A)
POSITION (B)
MODE
BLANKING
VERT SIG OUT
(B) VERT OUT FOR X,Y
(B) VERT OUT
VARIABLE (B)
SW2171 DISPLAY (B)
DC OFFSET (B)
NORM (B) SIG.
(B) SIG TO INVERTER
MEMORY (B) DRIVER PULSE
OFFSET MONITOR (B)
SW2190 MODE
SW2101 MILLIVOLTS/CM (B)
SW1282 CALIBRATED (A)
SW2282 CALIBRATED (B)
(A) DEC UNIT GND
(B) DEC UNIT GND
GND THRU Z, J16
(A) SIG OUT
(B) SIG OUT
(B) SIG TO DUAL TRACE
INVERTED SIG (A)
INVERTED SIG (B)
SIG TO MEMORY (A)
SIG TO MEMORY (B)
FEEDBACK TO SAMPLER (A)
FEEDBACK TO SAMPLER (B)
OFFSET VOLTAGE (A)
OFFSET VOLTAGE (B)
V1024, V2024 HEATER
V1133 HEATER
TO HTRS OF V1024, V2024 SAMPLER
A GATE - BIAS
A FEEDBACK TO R1036
B GATE - BIAS
B FEEDBACK TO R2036
(B) OUT TO HORIZ.
STAIRCASE OUT
STAIRCASE IN
A ONLY
B ONLY
ADDED ALGEB
A VERT, B HORIZ
DUAL TRACE
J11 GATE GENERATOR
J12 AC AMP
J13 MEMORY (A)
J14 MEMORY (B)
J15 INVERTER
J16 DUAL TRACE
PROBE POWER
FRONT VIEW
TYPE 452A
INTERCONNECTORS & SWITCHING 3
CMD 668

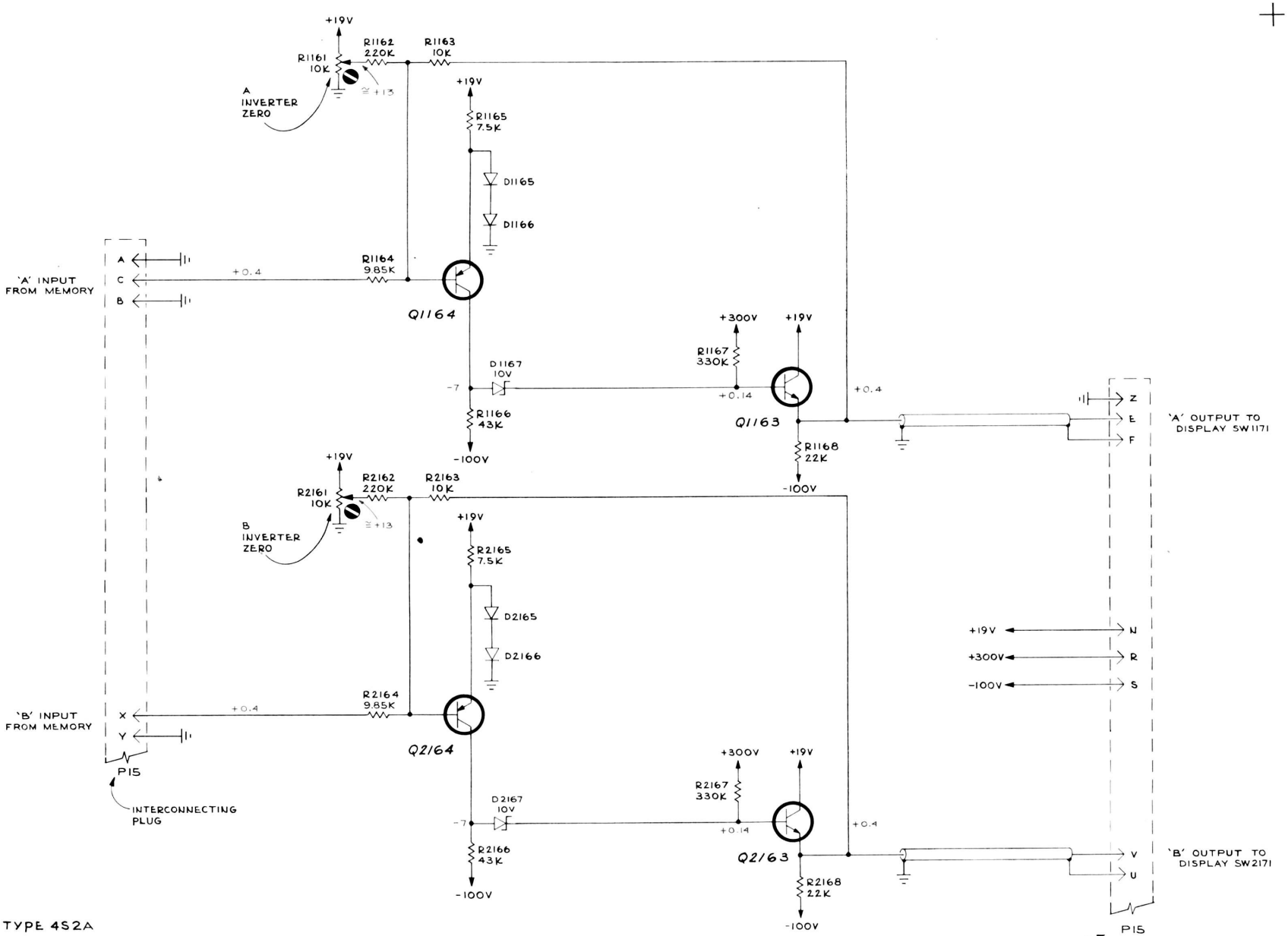


TYPE 4S2A

CMD 666

MEMORY ④

SERIES II MODEL 6



TYPE 4S2A

VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:

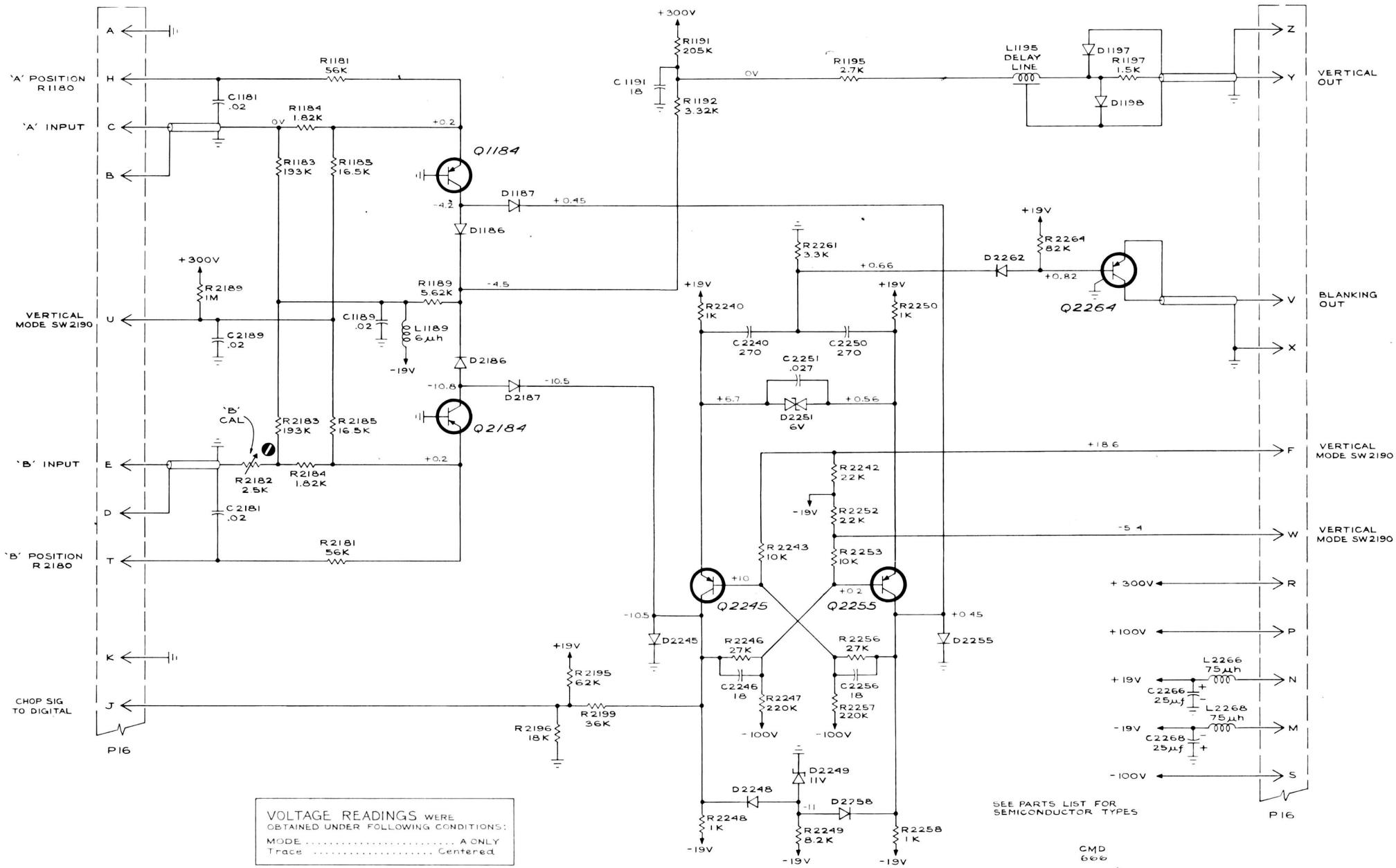
DISPLAY . . . . . INVERTED

Trace . . . . . Centered

JN 666

INVERTER ⑤

SERIES 9 MODEL 2



VOLTAGE READINGS WERE OBTAINED UNDER FOLLOWING CONDITIONS:

MODE ..... A ONLY

Trace ..... Centered

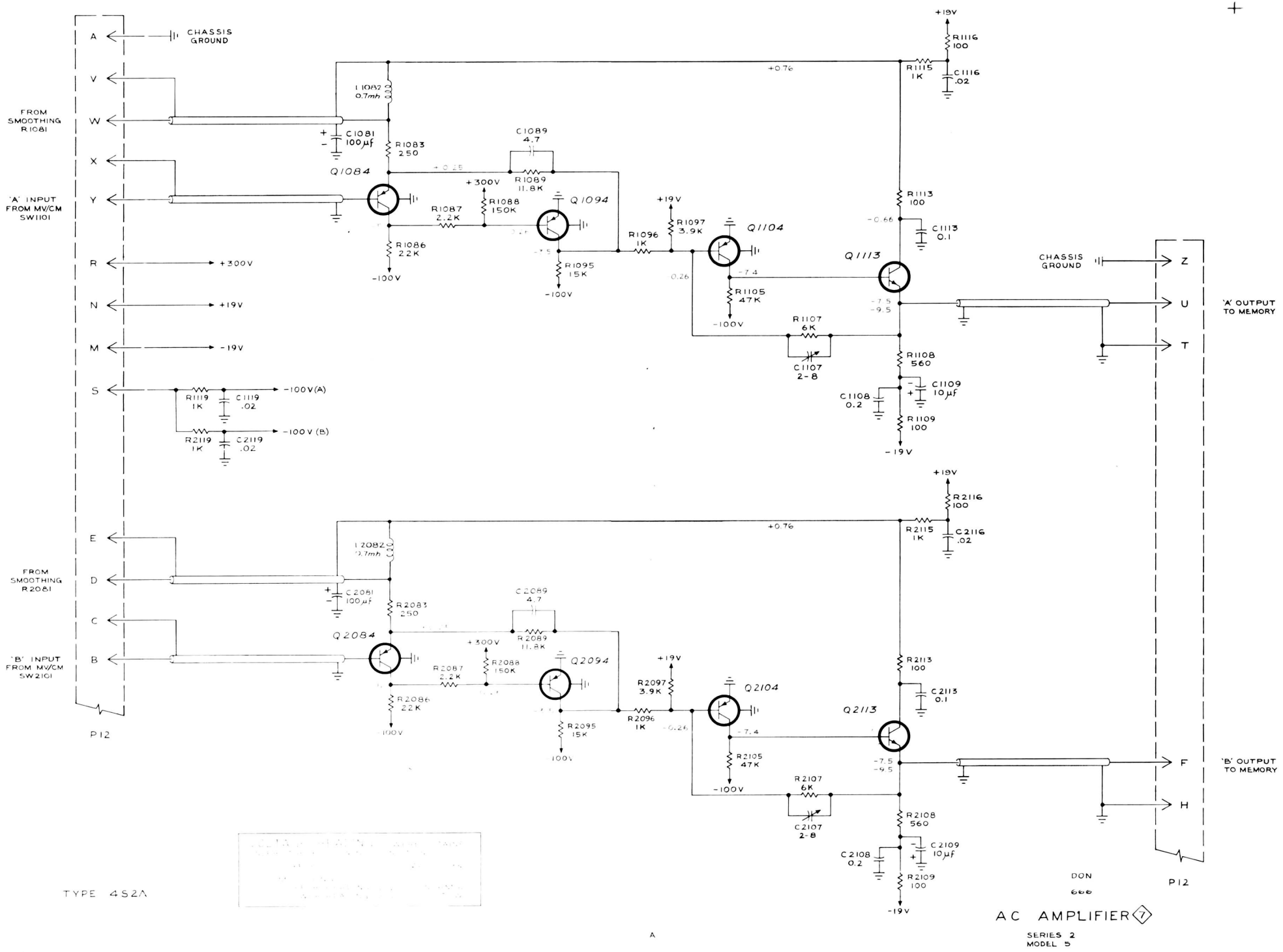
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

CMD 666

DUAL TRACE (6)

SERIES 5 MODEL 4

TYPE 452A


A
V
W
X
Y
R
N
M
S
P12
CHASSIS GROUND
FROM SMOOTHING R1081
'A' INPUT FROM MV/CM SW1101
+300V
+19V
-19V
-100V(A)
-100V (B)
R1119 1K
C1119 .02
R2119 1K
C2119 .02
L1082 0.7mh
C1081 100µf
R1083 250
Q1084
C1089 4.7
R1089 11.8K
+0.25
+300V
R1088 150K
R1087 2.2K
R1086 2.2K
-100V
Q1094
R1095 15K
-100V
+19V
R1096 1K
R1097 3.9K
Q1104
-7.4
R1105 47K
-100V
0.26
+0.76
R1115 1K
R1116 100
C1116 .02
R1113 100
-0.66
C1113 0.1
Q1113
-7.5
-9.5
R1107 6K
C1107 2-8
R1108 560
C1108 0.2
C1109 10µf
R1109 100
-19V
CHASSIS GROUND
Z
U
T
'A' OUTPUT TO MEMORY
E
D
C
B
FROM SMOOTHING R2081
'B' INPUT FROM MV/CM SW2101
L2082 0.7mh
C2081 100µf
R2083 250
Q2084
C2089 4.7
R2089 11.8K
+300V
R2088 150K
R2087 2.2K
R2086 .22K
-100V
Q2094
R2095 15K
100V
+19V
R2097 3.9K
R2096 1K
Q2104
-7.4
R2105 47K
-100V
-0.26
+0.76
R2115 1K
R2116 100
C2116 .02
R2113 100
C2113 0.1
Q2113
-7.5
-9.5
R2107 6K
C2107 2-8
R2108 560
C2108 0.2
C2109 10µf
R2109 100
-19V
F
H
'B' OUTPUT TO MEMORY
P12
TYPE 452A
DON
666
AC AMPLIFIER 7
SERIES 2
MODEL 5
A