INSTRUCTION MANUAL

Serial Number _____

TYPE 3B5

AUTOMATIC/ PROGRAMMABLE TIME BASE

Tektronix, Inc.
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070-0538-00

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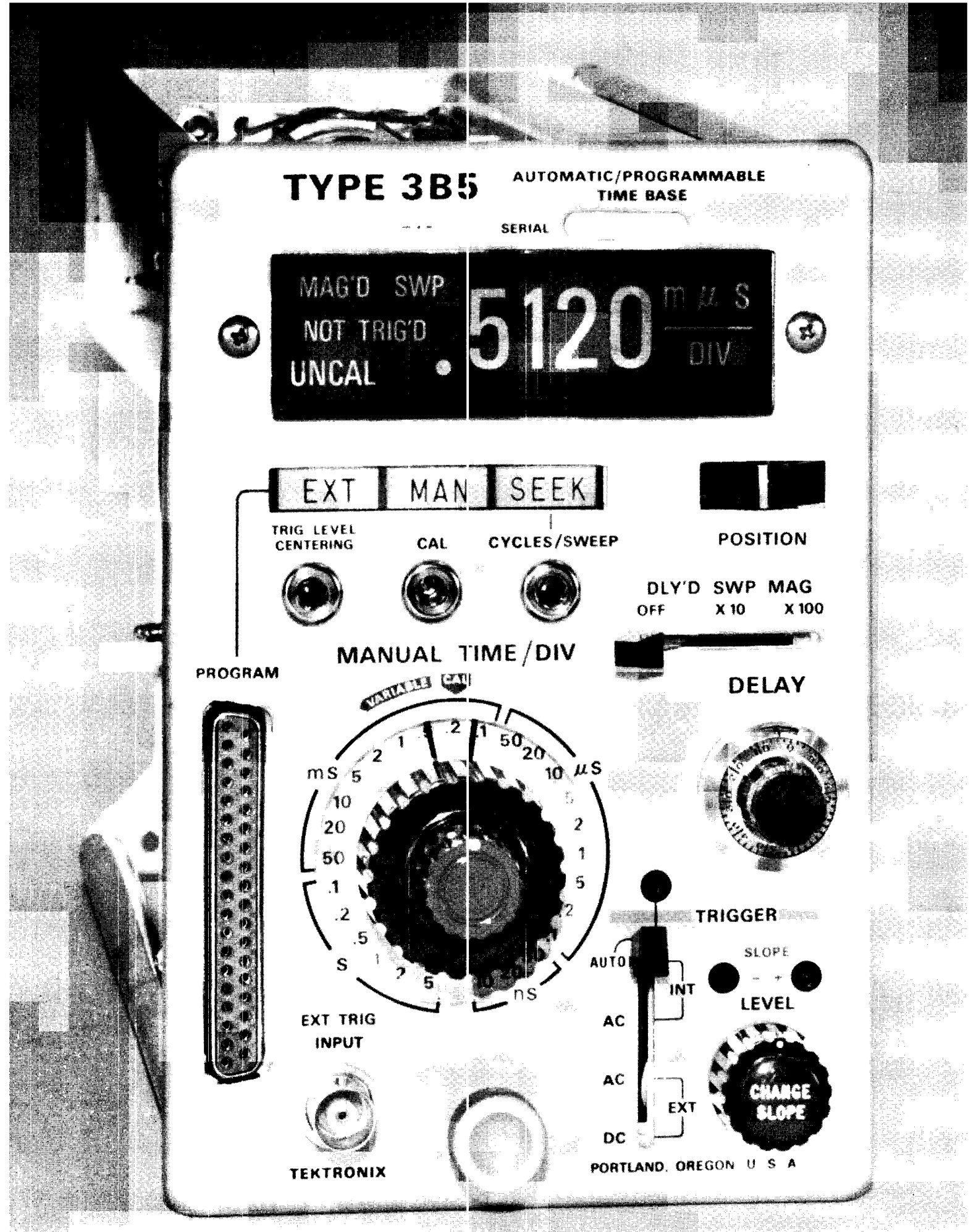

TYPE 3B5
AUTOMATIC/PROGRAMMABLE
TIME BASE
SERIAL
MAG'D SWP
NOT TRIG'D
UNCAL
5120
m μ S
DIV
EXT
MAN
SEEK
TRIG LEVEL
CENTERING
CAL
CYCLES/SWEEP
POSITION
DLY'D SWP MAG
OFF
X 10
X 100
PROGRAM
MANUAL TIME/DIV
DELAY
mS
μS
nS
S
EXT TRIG
INPUT
TRIGGER
AUTO
INT
AC
AC
EXT
DC
SLOPE
LEVEL
CHANGE
SLOPE
TEKTRONIX
PORTLAND, OREGON U S A

SECTION 1

CHARACTERISTICS

The Tektronix Type 3B5 Automatic/Programmable Time Base unit provides automatic and programmable time-base features, in addition to conventional time-base features, for Tektronix oscilloscopes which accept 3-series time-base units[1]. The Type 3B5 provides automatic sweep rate and trigger seeking on Seek command either from the front-panel SEEK button, from a remote-seeking probe (through an associated automatic/programmable amplifier unit) or from an external source (through either the front-panel PROGRAM connector or the program connector of the associated automatic/programmable amplifier unit). All front-panel control functions (except variable sweep rate) can be externally programmed through the front-panel PROGRAM connector. The MANUAL TIME/DIV switch provides selection of sweep rates from 5 seconds/division to 10 nanoseconds/division with delayed sweep magnification of 10 and 100 times (up to a maximum magnified sweep rate of 0.1 microseconds/division).

A front-panel illuminated readout panel indicates sweep rate, magnified sweep (with correct indication of magnified sweep rate), non-triggered sweep and uncalibrated sweep. The readout panel functions in all modes of operation.

The characteristics which follow are divided into two categories. Characteristics listed in the Performance Requirement column are checked in the Performance Check and Calibration sections of this manual. Items listed in the Supplemental Information column are provided for reference use and do not directly reflect the measurement capabilities of this instrument. The Performance Check procedure given in Section 5 of this manual provides a convenient method of checking the Performance Requirements listed in this section. The following characteristics apply over an ambient temperature range of 0° C to +50° C, except as otherwise indicated. Warm-up time for given accuracy is five minutes.

[1]**Except the Type 561 (SN 5000 and below). When used in a Type 565, a vertical sweep is provided.**

ELECTRICAL CHARACTERISTICS

TRIGGERING

Characteristic	Performance Requirement	Supplemental Information
Source	Internal or external	
Coupling	AC internal AC or DC external	
Polarity	Sweep can be triggered from positive-going or negative-going portion of trigger signal.	Slope changed automatically each time CHANGE SLOPE button is pressed.
Mode	Auto triggering Normal triggering adjustable for desired level	
Internal Trigger Sensitivity AUTO and AC	0.5 division of deflection, minimum, 50 Hz to 20 MHz	Checked with Type 3A5 signal displayed, 10 millivolts/division or greater sine wave. Typically —3 dB down at 10 Hz
External Trigger Sensitivity AC	1.0 volt, peak to peak, 50 Hz to 20 MHz	Typically —3 dB down at 10 Hz
DC	1.0 volt, peak to peak, 10 Hz to 20 MHz	2.5 volts, peak to peak, DC to 10 Hz
Trigger LEVEL Control Range INT-AC		At least + and — 10 volts
EXT-AC	At least + and — 20 volts	
EXT-DC	At least + and — 10 volts	
AUTO		Approximately 10% and 90% of trigger signal transition with a minimum of 0.5 division, (10 millivolts/division or greater) 1 kHz sine wave displayed with Type 3A5
External Program Trigger Level Range		Same as front-panel range with current change between about 0 and 400 microamps
External Trigger Input RC Characteristics		Approximately 150 kilohms paralleled by about 22 pF
Maximum Input Voltage at EXT TRIG INPUT connector		100 volts, DC + peak AC

HORIZONTAL DEFLECTION SYSTEM

Characteristic	Performance Requirement	Supplemental Information
Sweep Rates		
Manual Mode	5 seconds/division to 10 nanoseconds/division in 27 calibrated steps. Sweep rate indicated on readout panel	Selected by front-panel MANUAL TIME/DIV switch. Steps in 1-2-5 sequence
Seek Mode	5 seconds/division to 0.1 microseconds/division in 24 calibrated steps. Sweep rate indicated on readout panel	Automatically selected when seek command is received. Steps in 1-2-5 sequence
External Mode	5 seconds/division to 10 nanoseconds/division in 27 calibrated steps. Sweep rate indicated on readout panel	Selected by external program connected to PROGRAM connector. Steps in 1-2-5 sequence
Sweep Accuracy (at 25° C, ±5°)		VARIABLE control fully clockwise (UNCAL readout off) and DLY'D SWP MAG switch set to OFF (MAG'D SWP readout off). 10, 20 and 50 ns accuracy must be checked in accordance with Performance Check
1 s to 10 ns	Within ±3% of indicated sweep rate	
5 s and 2 s	Within ±5% of indicated sweep rate	
Variable Sweep Rate	Uncalibrated sweep rate to 2.5 times, or greater, the indicated sweep rate. s/DIV readout turns off and UNCAL readout turns on when VARIABLE control is not set to CAL position	Slowest sweep rate 12.5 seconds/division, or greater, in 5 s position
Sweep Length		Measured at 1 ms/DIV sweep rate
DLY'D SWP MAG at OFF	10.3 to 11.3 divisions	
DLY'D SWP MAG on	12 to 15 divisions	
Delayed Sweep Magnification	Basic sweep rates between 5 s and 1 μs can be magnified with the Delayed Sweep Magnifier. Calibrated DELAY control selects portion to be magnified. Basic sweep rates between 5 s and 10 μs can be magnified 100 times; basic sweep rates between 5 s and 1 μs can be magnified 10 times	Readout panel indicates correct magnified sweep rate
Magnified Sweep Accuracy (at 25° C, ±5°)		VARIABLE control fully clockwise (UNCAL readout off)
1 s to 1 μs	Within ±3% of sweep rate indicated on readout panel	
5 s and 2 s	Within ±5% of sweep rate indicated on readout panel	
Calibrated Delay Range	Continuous from 0 to 10 divisions from the start of the trace	
Delay Accuracy	Within ±1.5% of full scale at 1 ms/DIV. Within ±3% of full scale at all other sweep rates	Calibrated at 1 ms/DIV. Exclude first 0.2 division of display. Includes incremental DELAY dial linearity
Incremental DELAY Dial Linearity	Within ±0.4% of full scale	Exclude first 0.2 division of display
Delayed Sweep Magnifier Jitter	3 parts or less per 10,000	Equal to 0.3 division or less when measured with ×100 magnification at 1 ms/DIV basic sweep rate
Output DC Level	+180 volts, ±10 volts	Beam positioned to CRT electrical center

SEEK MODE

Cycles Per Sweep	Between two and six cycles with nominal CYCLES/SWEEP setting obtained in Calibration procedure	Automatically selected when seek command is received. Front-panel CYCLES/SWEEP adjustment provides range of about 0.5 to 3 times this nominal setting
Automatic Seek Cycling Time	One to two seconds	When seek command is continuous
Automatic Seeking Time		500 milliseconds or less with 10 MHz sine wave input and Trigger Function switch set to INT-AUTO
Frequency Range for Seek Mode Operation	30 Hz to 20 MHz	
Seek Mono Pulse Width	1.0 to 1.8 seconds	

PROGRAMMABLE FUNCTIONS

Characteristic	Performance Requirement	Supplemental Information
Trigger Function	Int Auto—If not programmed Int AC—Terminal 31 Ext AC—Terminal 30 Ext DC—Terminal 28	Grounding (zero volt) digital logic to given terminal of PROGRAM connector activates function
Trigger Slope	+Slope—If not programmed —Slope—Terminal 27	
Trigger Level		Analog current change between about 0 and 400 microamps at terminal 15 of PROGRAM connector provides same trigger level range as front-panel LEVEL control
Sweep Rate Multiplier	×1—Terminal 2 ×2—Terminal 3 ×5—Terminal 5	Sweep multiplier, sweep decade and decade enable must be programmed for each sweep rate. Grounding (zero volt) digital logic to given terminals of PROGRAM connector activates function
Enable	A—Terminal 23 B—Terminal 24	
Decade	Enable Logic: A / B → Terminal 1 s / 0.1 s → 6 10 ms / 1 ms → 8 0.1 ms / 10 μs → 9 1 μs / 0.1 μs → 11 — / 10 ns → 26	
Horizontal Position		Analog current change between about 0 and 500 microamps at terminal 14 of PROGRAM connector provides ±3 division external horizontal position range
Delayed Sweep Magnifier	OFF—Terminal 33 ×10—Terminal 34 ×100—Terminal 36	Grounding (zero volt) digital logic to given terminal of PROGRAM connector activates function
Magnifier Delay		Analog current change between about 350 and 200 microamps at terminal 17 of PROGRAM connector provides 0 to 10 division external delay range
External Mode Command	Type 3B5 switches to External Mode when terminal 21 of PROGRAM connector is grounded	
Remote Seek	Type 3B5 switches to Seek Mode (except when External Mode Command is present) when terminal 12 of PROGRAM connector is grounded	Momentary ground produces two to six cycles (nominal adjustment) display; continuous ground recycles unit every one to two seconds
Single Sweep		+125-volt external holdoff lockout applied to terminal 7 and —12-volts reset momentarily applied to terminal 25 of PROGRAM connector provides single-sweep operation

ADDITIONAL FUNCTIONS AVAILABLE AT PROGRAM CONNECTOR

External Horizontal Input		Applied to terminal 4 of PROGRAM connector. Sweep lockout at terminal 7, external unblanking at terminal 13 and horizontal position centering at terminal 14 also necessary.
Deflection factor		5 volts/division ±5%
Bandwidth		DC to 750 kHz, or greater
Maximum input voltage		75 volts, DC + peak AC
Input resistance		Approximately 100 kilohms

Additional Functions *(cont)*

Characteristic	Performance Requirement	Supplemental Information
Sweep Out		0.05 milliamp/division, ±10%, at terminal 16 of program connector[2]
External Unblanking	—12 volts DC unblanks CRT	Apply to terminal 13 of PROGRAM connector
Current Available from PROGRAM Connector (maximum)		Supply / Terminal / Current: +125 V / 18 / 30 mA; —12.2 V / 1 / 75 mA; —100 V / 19 / 1 mA

ENVIRONMENTAL CHARACTERISTICS

The following environmental test limits apply when tested in accordance with the recommended test procedure. This instrument will meet the electrical performance requirements given in this section following environmental test. Complete details on environmental test procedures, including failure criteria, etc., may be obtained from Tektronix, Inc. Contact your local Tektronix Field Office or representative.

Characteristic	Performance Requirement	Supplemental Information
Temperature		
Operating	0° C to +50° C	
Non-operating	—40° C to +65° C	
Altitude		
Operating	15,000 feet maximum	
Non-operating	50,000 feet maximum	May be tested during non-operating temperature tests
Vibration		
Operating	Vibrate for 15 minutes along each axis at a total displacement of 0.015 inch (1.9 g at 50 c/s) with the frequency varied from 10-50-10 c/s in one-minute cycles. Hold at any resonant point for three minutes. If no resonant points are found, vibrate at 50 c/s for three minutes on each axis.	Instrument secured to vibration platform during test. Total vibration time about 55 minutes.
Shock		
Non-operating	One shock of 30 g, one-half sine, 11 millisecond duration along each major axis.	Guillotine type shock
Transportation	Meets National Safe Transit type of test when correctly packaged	
Package vibration	Vibrate for one hour slightly in excess of 1 g	Package should just leave vibration surface
Package drop	Drop from a height of 30 inches on one corner, all edges radiating from that corner and all flat surfaces	Total of 10 drops

MECHANICAL CHARACTERISTICS

Characteristic	Information
Construction	
Chassis	Aluminum alloy
Panel	Aluminum alloy with anodized finish
Circuit boards	Glass-expoxy laminate
Dimensions	Fits 3-series compartments of 560-series Oscilloscopes

[2]**Similar output available at terminal 18 of the interconnecting plug.**

Connectors	
EXT TRIG INPUT	BNC
PROGRAM	37-terminal connector. Mates with Cinch No. DC-37P-C33 (Tektronix Part No. 131-0422-00)

STANDARD ACCESSORIES

Standard accessories supplied with the Type 3B5 are listed on the last pullout page at the rear of this manual. For optional accessories available for use with this instrument, see the current Tektronix, Inc. catalog.

TYPE 3B5 CONTROL SET-UP CHART

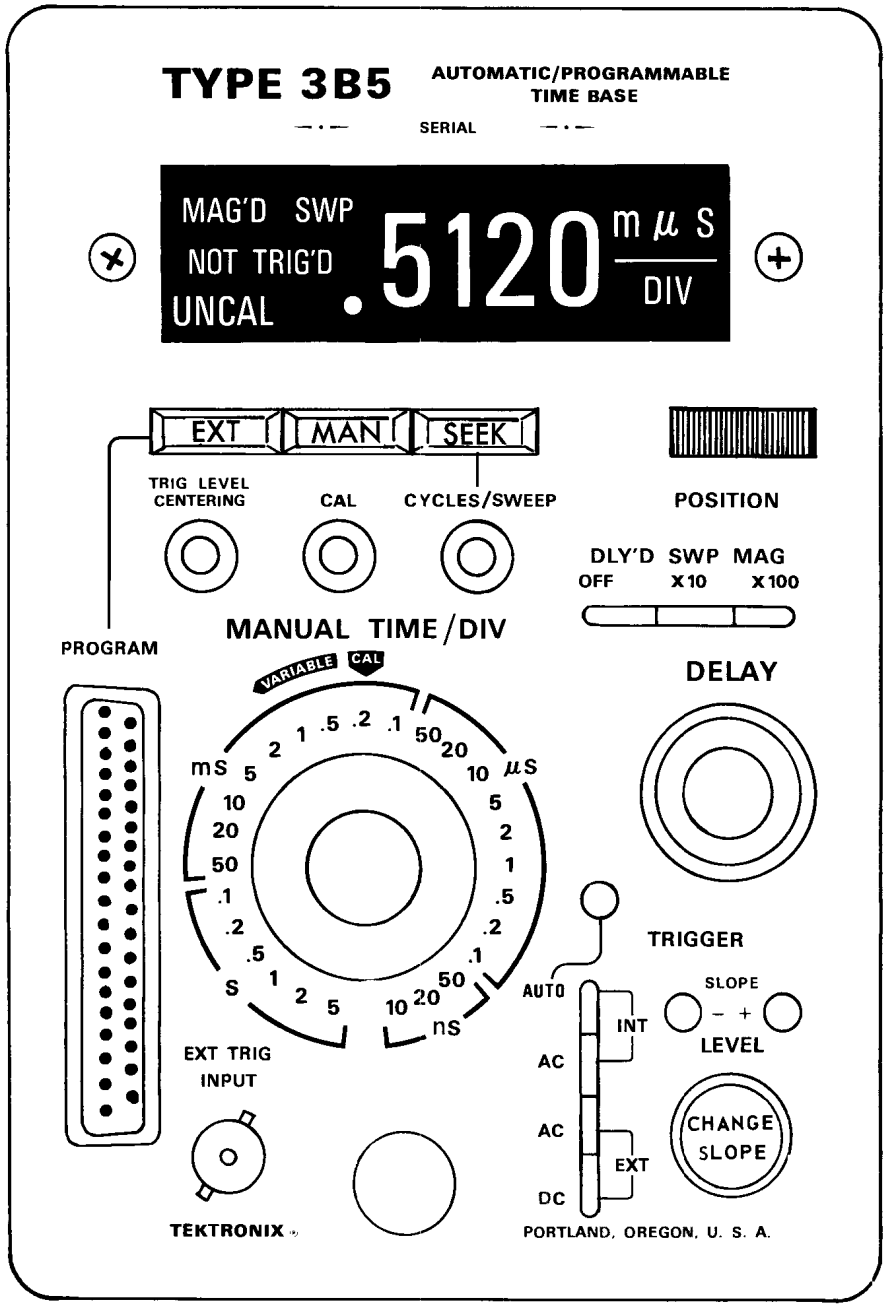


Fig. 2-2. Control set-up chart.

SECTION 3

CIRCUIT DESCRIPTION

Introduction

This section of the manual contains an electrical description of the circuitry used in the Type 3B5 Automatic/Programmable Time Base unit. This section begins with a basic block-diagram discussion of the instrument using the simplified block diagram shown in Fig. 3-1. Then, a logic discussion explains which blocks operate in each of the three modes of operation; Manual Mode, Seek Mode and External Mode. In the detailed Circuit Description, a logic block diagram shows the interconnections between the stages in each major circuit and the input and output signals. Also shown is the relationship of the front-panel controls to the individual circuits. A complete block diagram is located in the Diagrams section at the rear of this manual. This block diagram shows the overall relationship between all circuits in this instrument. Complete schematic diagrams of each circuit are also given in the Diagrams section. Refer to these diagram throughout the following circuit description for electrical values and relationship.

BLOCK DIAGRAM DISCUSSION

A simplified block diagram of the Type 3B5 is shown in Fig. 3-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each block in this block diagram represents a major circuit within the instrument. The number on each block refers to the circuit diagram at the rear of this manual which shows the complete circuit.

The Sweep Trigger circuit produces an output pulse which turns on the Sweep Generator circuit to produce the sweep signal. The output pulse from the Sweep Trigger circuit is derived from the input trigger signal. The input signal can be either an internal signal from the amplifier unit, which is a sample of the vertical deflection signal, or an external signal applied to the EXT TRIG INPUT connector. Trigger slope, level, mode, coupling and source are externally programmable in the External Mode of operation (EXT). For Seek Mode operation (SEEK) a control signal from the Seek Circuit allows the Sweep Trigger circuit to switch to auto triggering if the front-panel controls are incorrectly set or the correct trigger signal is not applied.

The Sweep Generator produces a linear sawtooth signal when triggered by the Sweep Trigger circuit. The slope of the sawtooth produced by the Sweep Generator circuit is controlled by the Delay and Timing Circuit. The output of the Sweep Generator is amplified by the Horizontal Amplifier to produce the horizontal deflection for the indicator oscilloscope CRT. Other signals for horizontal deflection can also be applied to the Horizontal Amplifier through the PROGRAM connector. The horizontal position of the trace can be externally programmed in the External Mode of operation.

The Delay and Timing Circuit provides delayed sweep magnification in addition to selecting the basic sweep rate. The sweep rate is controlled by the MANUAL TIME/DIV switch for Manual Mode operation or by the Counter Circuit for Seek and External Mode operation. The amount of delay before sweep magnification begins is controlled by the front-panel multi-turn DELAY control for Manual and Seek Mode operation, or is externally programmed in the External Mode of operation. The Delayed Sweep Magnifier Control circuit determines the magnification ratio and also provides a correct readout on the readout panel. The magnification ratio (×1, ×10, ×100) is selected by the front-panel DLY'D SWP MAG switch for Manual and Seek Mode operation or it is externally programmed for External Mode operation.

In the Seek Mode of operation, the Seek Circuit produces output pulses which allow the Counter Circuit to select the proper sweep rate for a two to six cycle display (nominal CYCLES/SWEEP adjustment). The Counter Circuit can also be externally programmed to select the sweep rate in the External Mode. The Readout Logic circuit decodes the sweep rate control logic levels from the Counter Circuit and the magnification logic level from the Delayed Sweep Magnifier Control circuit to provide the correct readout panel display in the Seek and External Modes of operation. For Manual Mode operation, the sweep rate and readout-panel display are determined by the MANUAL TIME/DIV switch and the DLY'D SWP MAG switch located in the Readout Logic circuit.

The Readout Board provides the front-panel readout of instrument operation. The bulbs which produce the readout are controlled by the Sweep Generator, Delay and Timing Circuit and the Readout Logic circuit.

The operating mode of the instrument is controlled by the Operating Mode Power circuit. This circuit produces output voltages to control those circuits associated with the Manual Mode, Seek Mode or External Mode functions. External Mode operation can be selected by external program and it has priority over the other modes. The Seek Mode can be selected (when not in the External Mode) by a seek command from the front-panel SEEK button, remote seek command from the amplifier unit or remote seek command through the front-panel PROGRAM connector. The Manual Mode is obtained (except when in External Mode) when the unit is first turned on, when the MAN button is pressed, when the MANUAL TIME /DIV switch setting is changed or when the external program is removed. The Voltage Distribution circuit provides the power supply voltages from the indicator oscilloscope to all of the circuits within this unit. This circuit contains the decoupling networks to provide the decoupled voltages used throughout this unit.

LOGIC DISCUSSION

Manual Mode Operation

Fig. 3-2 shows the circuits in the Type 3B5 which are operative in the Manual Mode. In this mode of operation, the unit operates as a conventional time base with operation determined by the front-panel controls. The Operating Mode Power circuit applies a control level to the other circuits to either lock out the Seek and External Mode functions or to activate Manual Mode functions. The MANUAL

TIME/DIV switch and DLY'D SWP MAG switch provide the correct normal and magnified sweep rate readout on the readout panel.

Seek Mode Operation

The operating circuits for the Seek Mode of operation are shown in Fig. 3-3. This includes all blocks which were operative for Manual Mode (except Manual Operating Mode Power) plus the automatic circuits in the Seek Circuit, Counter Circuit and Readout Logic circuit. The Operating Mode Power circuit applies power to the various circuits to operate the automatic seek functions. The Sweep Trigger circuits operate as determined by the front-panel controls unless the controls are incorrectly set or the applied trigger signal is not correct. Then, the Seek Circuit switches the Sweep Trigger circuit to auto trigger operation and a stable display is presented, if possible. If a trigger signal is not present in the auto trigger mode, the NOT TRIG'D readout comes on and the sweep free runs.

The Seek Circuit resets the sweep to the slowest sweep rate at the start of each seek cycle. Then, the Seek Circuit compares the trigger pulses produced by the Sweep Trigger circuit against a window-gate signal derived from the sawtooth and the sweep gate signal (see Seek Circuit discussion). If trigger pulses occur during the window gate, the Seek Circuit produces an advance pulse which advances the Counter Circuit to the next faster sweep rate and a sweep reset pulse resets the sweep so it starts again at the left side of the graticule at the new sweep rate. Again, the Seek Circuit compares the trigger pulses against the window-gate signal and advances the Counter Circuit if trigger pulses are present. This continues until the sweep rate is fast enough so no trigger pulses occur during the window-gate signal (see Seek Circuit discussion for more complete explanation). The final sweep rate is maintained until another seek command is received or the operating mode is changed. This complete seeking action takes place each time a seek command is received.

Fig. 3-4 shows the logic sequence for Seek Mode operation including a full explanation of operation. The circled numbers on this logic diagram refer to the step in the explanation which describes the action of this individual circuit.

External Mode Operation

The circuits which are operative for External Mode are shown in Fig. 3-5. In this mode of operation, most of the circuits are controlled by external program logic applied to the circuits from an external programmer through the front-panel PROGRAM connector. An E is shown beside each block which is controlled from the programmer. The programmable capabilities of this instrument are the same as the front-panel capabilities (except for variable sweep rate).

The External Mode of operation is established by applying an external mode command to the Operating Mode Power circuit. External Power is then applied to those circuits which control external mode operation and Manual or Seek Mode operation is locked out. Sweep rate, delayed sweep magnification, delay, horizontal position, trigger mode, source, coupling, slope and level are externally programmable. If auto triggering is programmed, the front-panel LEVEL control determines the starting level of the display.

CIRCUIT DESCRIPTION

Sweep Trigger

General

The Sweep Trigger circuit produces trigger pulses to turn on the Sweep Generator circuit. This trigger pulse is derived either from the vertical input signal or an external signal connected to the EXT TRIG INPUT connector. Control stages in this circuit select the source, coupling, level, mode and slope of the trigger signal. Fig. 3-6 shows a logic block diagram of the Sweep Trigger circuit. A diagram of this circuit is shown on diagram 1 at the rear of this manual.

Trigger Source and Coupling

Relay K3-1 selects the trigger signal either from an internal signal from the amplifier unit or an external signal applied to the EXT TRIG INPUT connector. This relay is controlled by the Trigger Mode Logic stage. When K3 is not energized, internal triggering is provided from the vertical signal. When K3 is energized, K3-1 connects the external trigger signal to the input circuit. Trigger coupling is selected by K4. When K4-1 is open, the trigger signal must pass through coupling capacitor C3. This capacitor blocks the DC component of the trigger signal and attenuates low-frequency AC signals below about 50 Hz. When K4 is energized, K4-1 closes and C3 is by-passed to directly couple all components of the trigger signal to the Input Emitter Follower. DC coupling is provided only in the EXT-DC position of the Trigger Function switch, SW50 or when externally programmed for external DC. More information on how trigger source and coupling are controlled is given under Trigger Mode Logic.

Input Emitter Follower

The Input Emitter Follower, Q23, provides a high input impedance for the trigger signal. It also provides isolation between the Sweep Trigger circuits and the triggering source. The level on the trigger signal at which the trigger circuits respond is controlled by varying the bias level at the base of Q23. The bias level is determined by the LEVEL control, the Auto Trigger P-P Level stage or the external program trigger level. Further information concerning operation of the level control circuit is given under Trigger Level Amplifier. The network D23-D24-D26-C23-C26-R25B in the emitter circuit of Q23 provides stable triggering in the auto trigger mode throughout the complete rotation of the Trigger LEVEL control. This is described in detail under Auto Trigger P-P Level.

The trigger signal at the emitter of Q23 is coupled to the base of Q74 through D62. This diode returns the DC level of the trigger signal to that at the base of Q23 by off-setting the base-emitter voltage drop of Q23. D62 also provides temperature compensation for Q23. The trigger signal at this point follows the level established at the base of Q23 by the trigger signal or the Trigger Level Amplifier circuit.

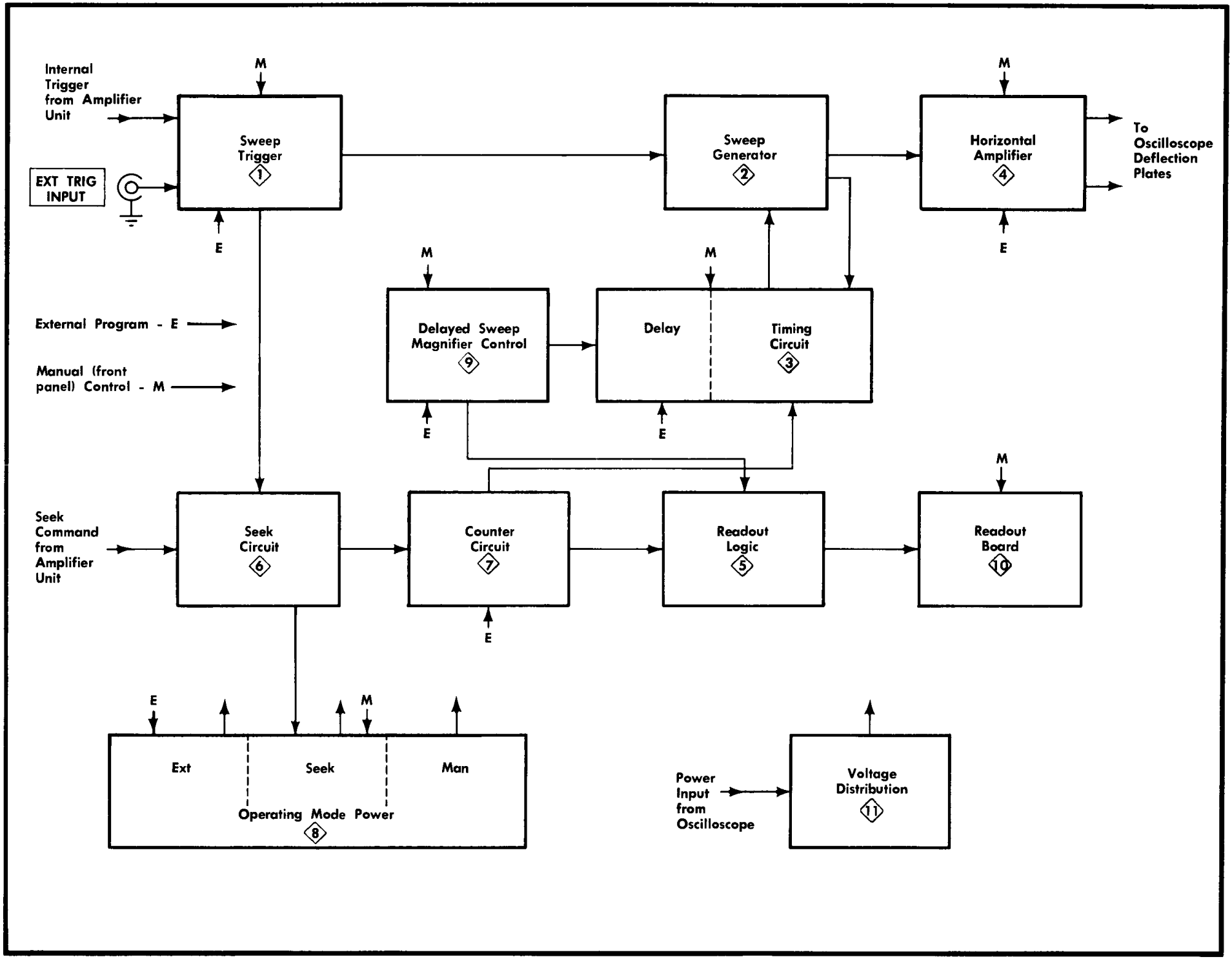


Fig. 3-1. Simplified block diagram of Type 3B5.

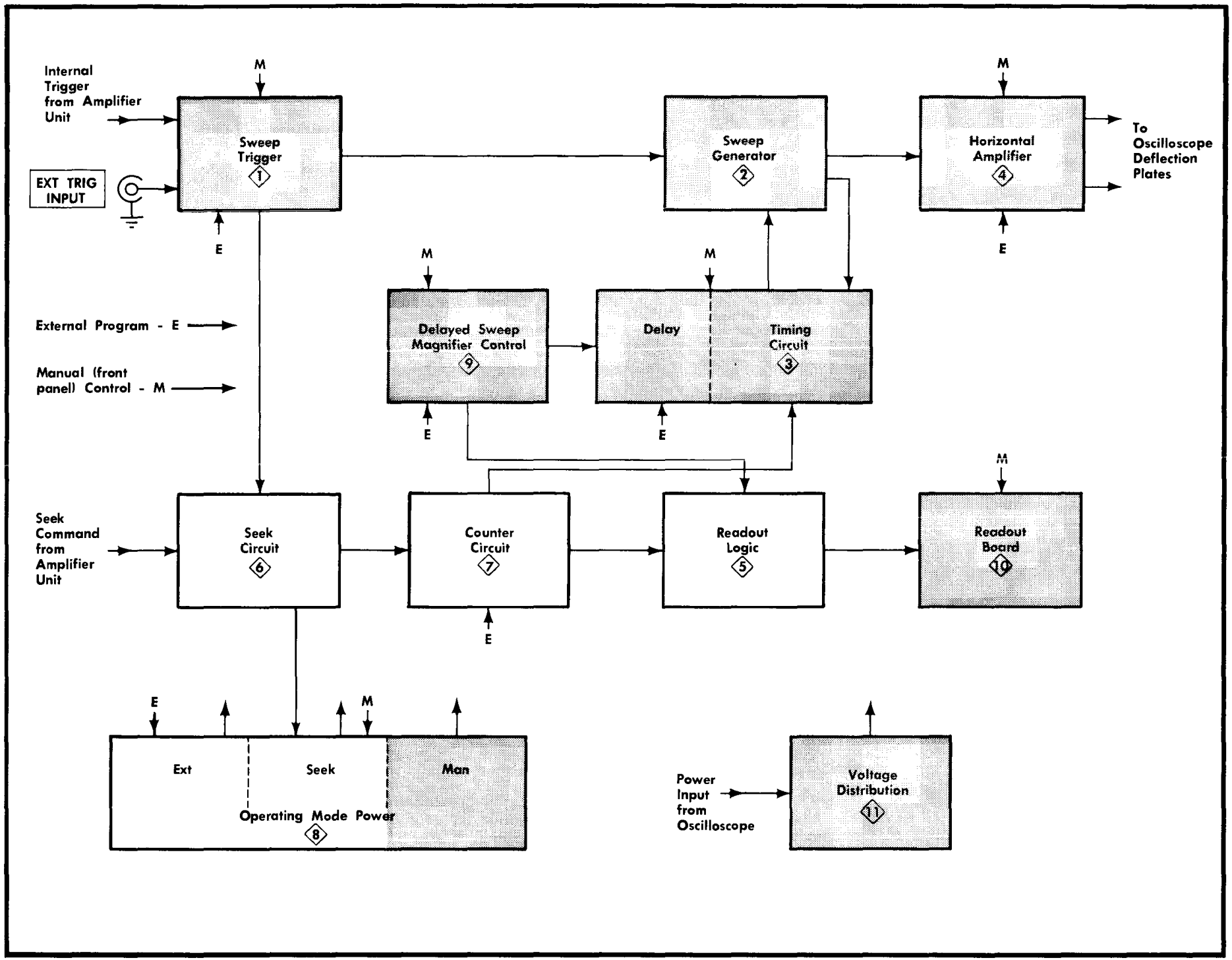


Fig. 3-2. Manual Mode operation (conventional time base). Shaded blocks are operative.

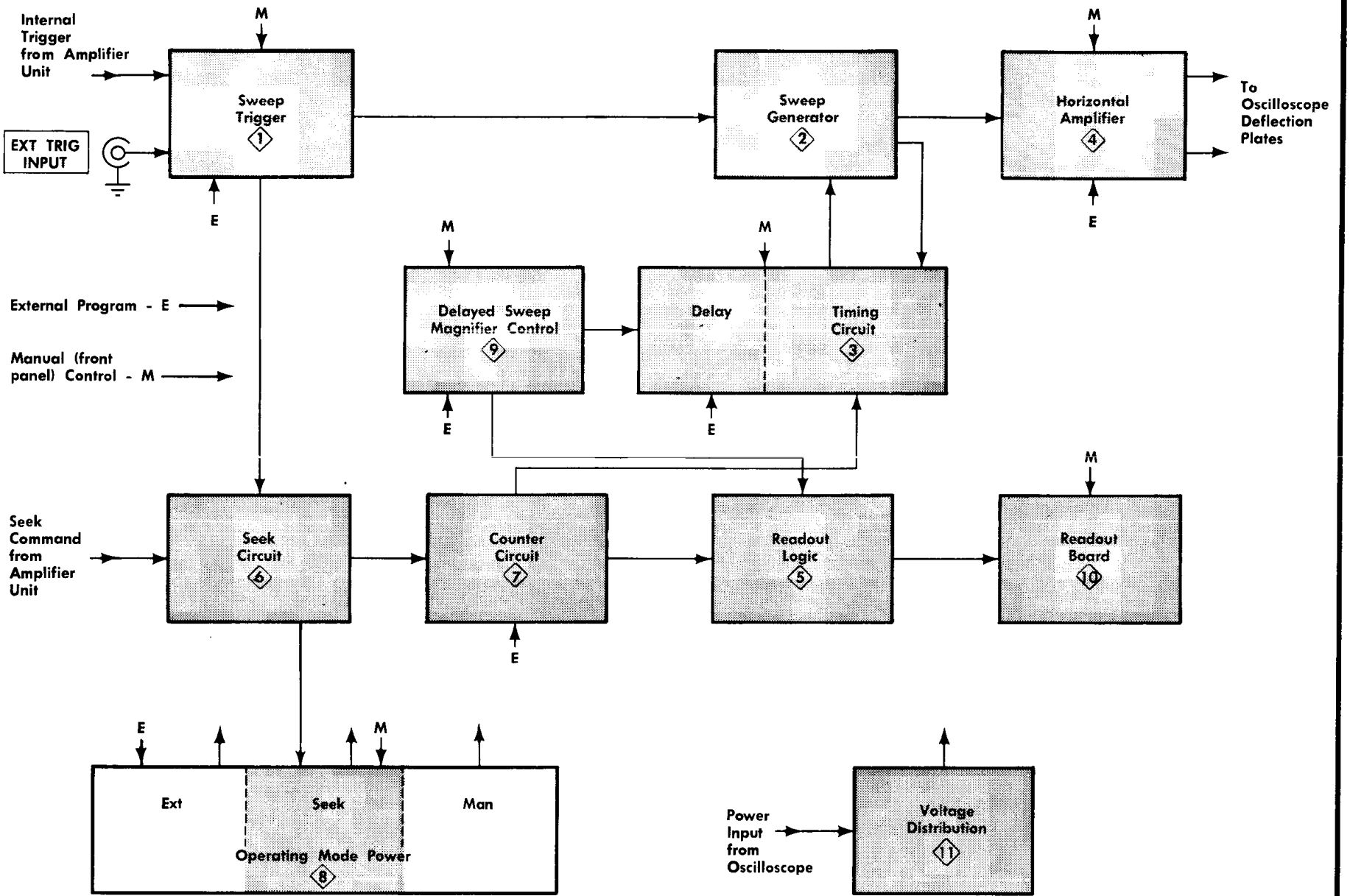
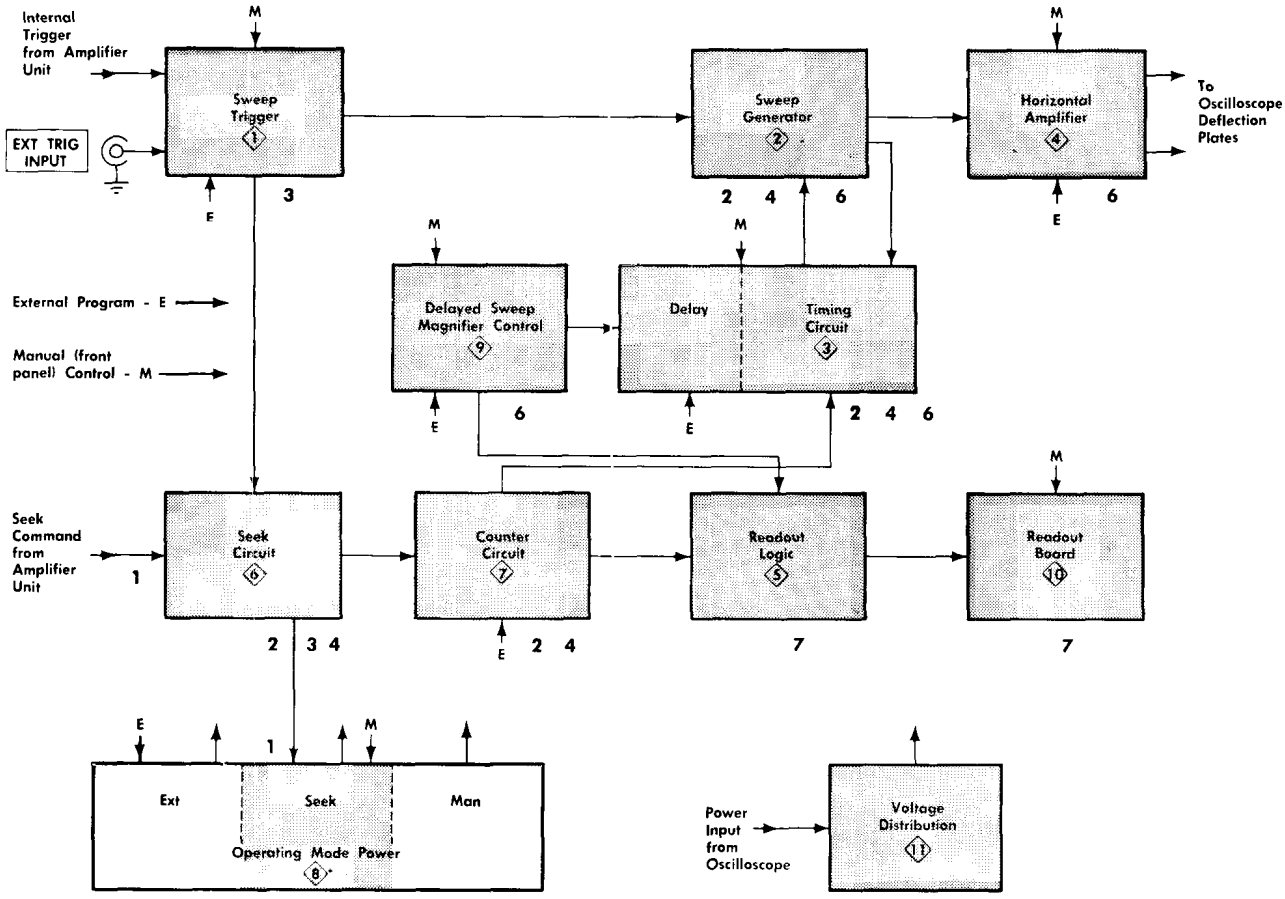


Fig. 3-3. Seek Mode operation (automatic seeking). Shaded blocks are operative.



Seek Mode Logic Sequence

1. Seek command received from front-panel SEEK button, remote seek through PROGRAM connector or remote seek from amplifier unit. Operating Mode Power circuit switches to Seek Power (except when in External Mode).
2. Seek Circuit resets Counter Circuit to five second/division conditions. Counter Circuit in turn produces output levels to select five second/division sweep rate in the Delay and Timing Circuit. Sweep Generator is reset to start sweep at the left side of the graticule.
3. Sweep Trigger circuit operates as set by the front-panel controls. If unit is not correctly triggered with these settings, the Seek Circuit switches unit to auto triggering. Then, if the unit is triggered it operates as described in the next step. If not triggered, the NOT TRIG'D readout comes on and the sweep free runs (normally at 2 s/DIV sweep rate).
4. Seek Circuit combines sawtooth signal and sweep gate signal to produce a window-gate signal. The duration of this window-gate signal is typically about 20% to 60% of the total sweep duration (10 times sweep rate). Trigger signals from the Sweep Trigger circuit are compared to the window gate. If a trigger pulse occurs during the window gate, an advance pulse is produced which advances the Counter Circuit (and the Delay and Timing Circuit) to the next faster sweep rate and a sweep reset pulse resets the Sweep Generator so it starts over at the left side of the graticule at the new sweep rate.
5. Step 4 is repeated until the Counter Circuit (and the sweep rate) have been advanced until a trigger pulse does not occur during the window-gate. If the .1 μs/DIV sweep rate is reached before this occurs, the Counter Circuit stops and remains at this condition until reset (by next seek command).
6. The Sweep Generator starts to run up at the sweep rate selected by the Counter Circuit. If the Delayed Sweep Magnifier Control circuit is set for ×10 or ×100 magnification, current is added to the Sweep Generator at a point determined by the DELAY control in the Delay and Timing Circuit to magnify a portion of the trace. The final sawtooth at the output of the Sweep Generator circuit is amplified by the Horizontal Amplifier circuit to produce the horizontal deflection.
7. The Readout Logic circuit decodes the sweep-rate logic from the Counter Card and the magnifier logic from the Delayed Sweep Magnifier Control circuit. The output of the Readout Logic circuit is connected to the Readout Board to indicate the sweep rate. If the sweep is magnified, the Readout Board indicates the sweep rate of the magnified portion.

Fig. 3-4. Logic sequence for Seek Mode. Numbers below blocks refer to the step which explains the operation of this block.

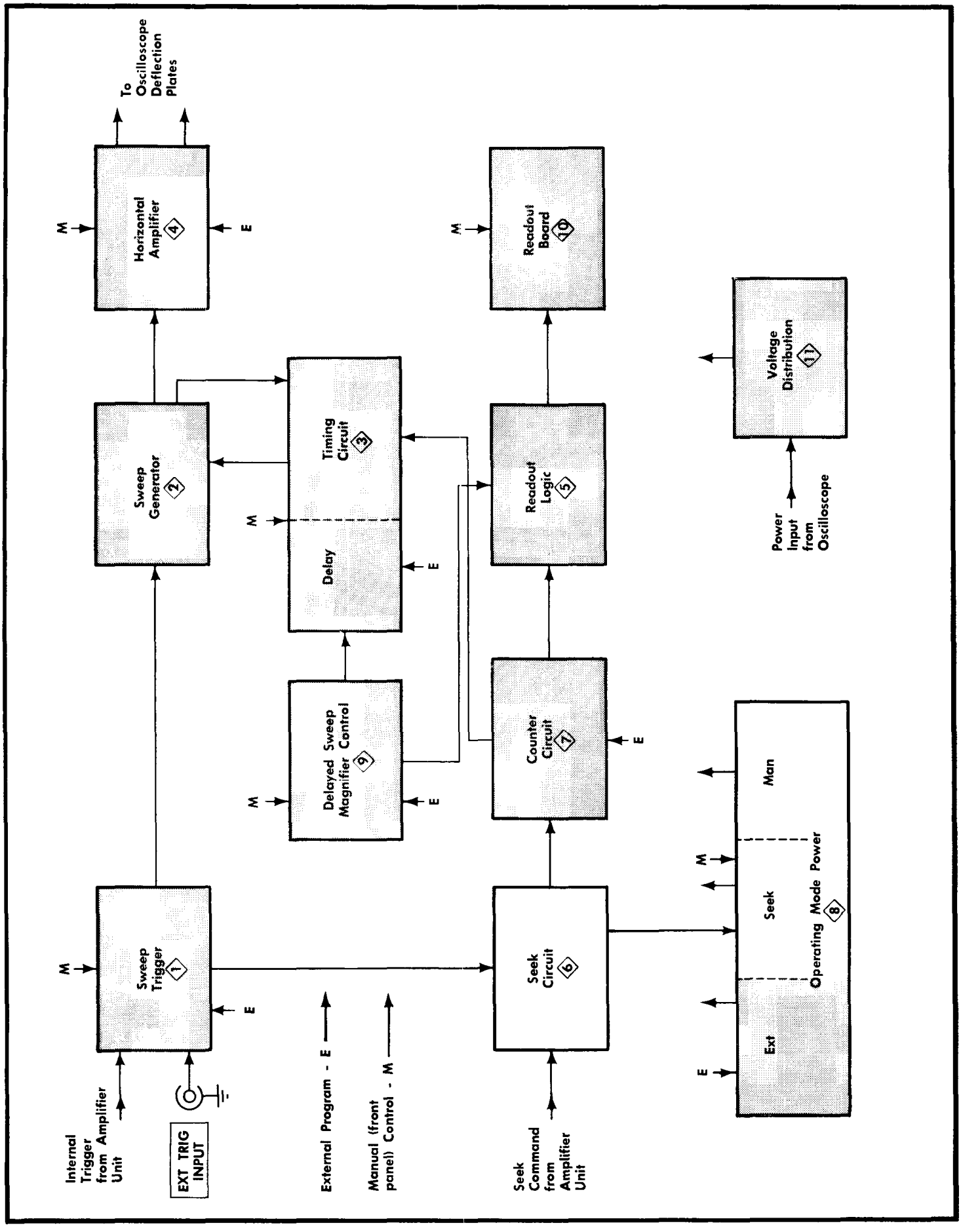


Fig. 3-5. External Mode operation (programmable). Shaded blocks are operative.

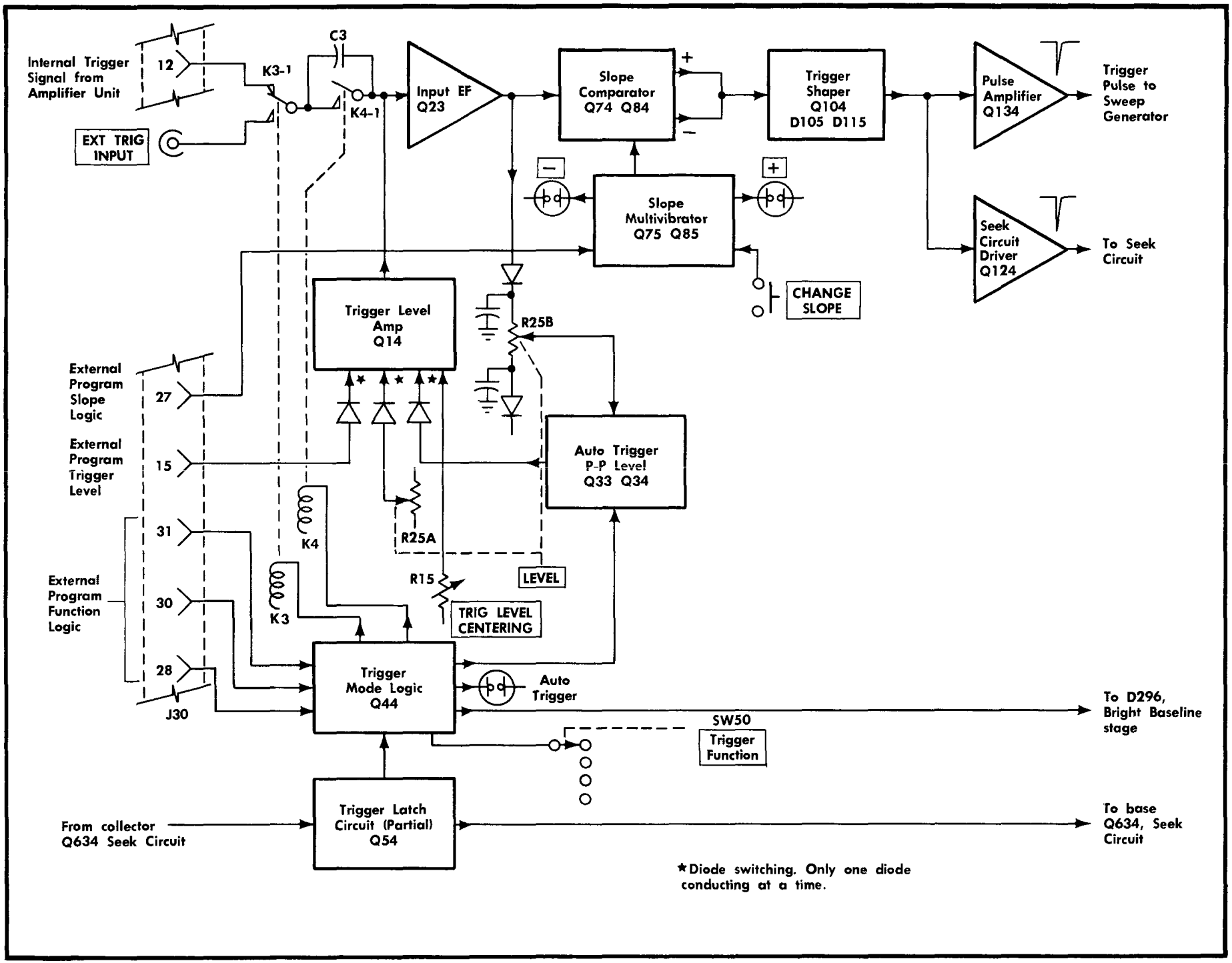


Fig. 3-6. Sweep Trigger logic block diagram.

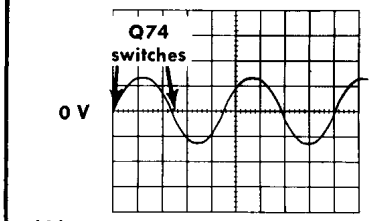
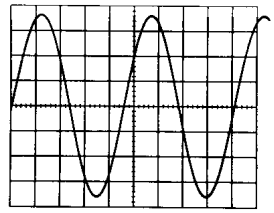
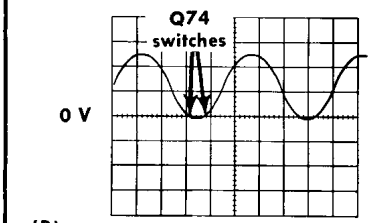
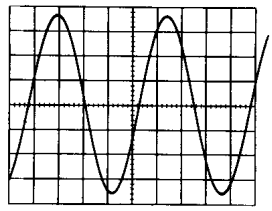
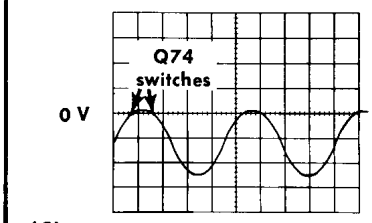
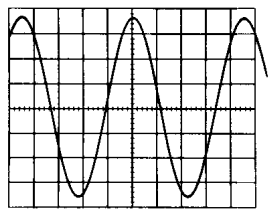
Signal at base of Q74	Condition	CRT display (+ slope)
 (A)	LEVEL control centered. Sweep triggered at midpoint of signal.	
 (B)	LEVEL control counterclockwise from midrange. Sweep triggered on negative portion of signal.	
 (C)	LEVEL control clockwise from midrange. Sweep triggered on positive portion of signal.	

Fig. 3-7. Effect of LEVEL control on AC coupled, symmetrical trigger signal at the base of Q74 for small-signal operation (less than ±5 volts). One kilohertz sine-wave displayed.

Slope Comparator

Q74 and Q84 are connected as a comparator. The comparator is referenced to ground through R94 at the base of Q84. The emitters of Q74 and Q84 are connected together through D91-D92 or C92-R92. Signals with amplitudes higher than about one volt, peak to peak, are DC-coupled between the emitters of Q74 and Q84 through D91 or D92. Smaller signals are AC-coupled through C92 and R92. Since there is very little voltage drop in this coupling between emitters, the voltage at each emitter is essentially the same. Therefore, the transistor which is forward biased controls conduction. For example, assume that the trigger signal applied to the base of Q74 is negative going and it forward biases Q74. The increased current flow through R63 and R93 produces a larger voltage drop and the emitters of both Q74 and Q84 go more negative (less positive). A more negative voltage at the emitter of Q84 reverse biases this transistor and the collector voltage goes negative. At the same time, the collector current of Q74 has increased and its collector goes more positive. Notice that the signal current at the collectors of Q74 and Q84 is opposite in phase. The negative-going signal has been inverted through Q74 but not through Q84. The sweep can be triggered from either the negative-going or positive-going slope of the input signal by producing the trigger pulse from either the inverted signal at the collector of Q74 or the uninverted signal at the collector of Q84. This selection is made by the Slope Multivibrator stage (see Slope Multivibrator discussion).

The DC level of the trigger signal at the emitter of Q23 can be varied by the LEVEL control, the Auto Trigger P-P Level stage or external program trigger level. This also changes the bias level on Q74 and determines the change in trigger signal necessary to turn Q74 on (or off). For example, when the LEVEL control (also applies to auto trigger or external level) is set near midrange, the base of Q74 is at about zero volts (TRIG LEVEL CENTERING adjustment set correctly). Therefore, signal changes around the zero-volt level will turn Q74 on or off (see Fig. 3-7A). If the LEVEL control is set counterclockwise, a more positive level is established at the base of Q74 and this shifts the trigger signal at the base of Q74 to a more positive level (see Fig. 3-7B). Since Q74 still switches near zero volts, it now switches at a more negative point on the trigger signal than when the LEVEL control was centered. This produces an output pulse from the Sweep Triggered circuit at an earlier time, which starts the Sweep Generator sooner. The resultant display shows more of the positive-going edge of the displayed waveform (positive slope triggering). The effect is the opposite when the LEVEL control is set clockwise from midrange (see Fig. 3-7C). The DC level of the waveform is shifted negative and Q74 switches at a later time. Less of the positive-going edge is shown on the displayed waveform (positive slope triggering). The LEVEL control was used to change the trigger level for this explanation. However, the effect will be the same when either the external program level or Auto Trigger P-P Level circuit sets the trigger level.

Slope Multivibrator

The Slope Multivibrator, Q75 and Q85, selects the Slope Comparator output signal which triggers the sweep. This is accomplished by forward biasing either D66 or D96. Q75 and Q85 are connected as a bistable multivibrator. For positive slope triggering, Q85 is biased off and Q75 is conducting. Since the current flow through R82 is reduced with Q85 off, the voltage level at the collector of Q85 rises positive. D82 is reverse biased and the voltage across B82, + SLOPE indicator, ignites it. Meanwhile, on the Q75 side of the multivibrator, the emitter level is at about —7 volts as established by zener diode D86. The base level established by the voltage divider R74-R75-R99 from —12.2 volts to ground is positive enough (less negative) to bias Q75 on and D72 is forward biased. The collector current of Q75 through R72 pulls the collector more negative and B72, — SLOPE indicator, is held off. The negative voltage level at the collector of Q75 reverse biases D66 through D65. This blocks the inverted trigger signal at the collector of Q74 from being passed on to the Trigger Shaper stage. At the same time D96 is forward biased through D95 by the —2 volt level at the cathode of D95 established by divider R74-R75-R99. With D96 forward biased, the trigger signal at the collector of Q84 is coupled to the Trigger Shaper stage to provide positive-slope triggering.

For negative-slope triggering, conditions are reversed. Q75 is off and Q85 is conducting. The collector of Q75 rises positive and B72, —SLOPE indicator, is turned on. D72 is reverse biased and the less negative voltage at the cathode of D65 established by divider R69-R71-R85-R84 forward biases D66 through D65. The inverted trigger signal at the collector of Q74 passes to the Trigger Shaper stage. Q85 is held in conduction by a less negative voltage at its base established by the voltage divider R69-R71-R84-R85 from —12.2 volts to ground. With Q85 conducting, its collector goes negative and B82, + SLOPE indicator, is held off. The negative level at the collector of Q85 reverse biases D96 through D95 and D82 to block the trigger signal from Q84. Q75 is held off by a level of about —6 volts at its base established by divider R74-R75 from —12.2 volts to the collector of Q85.

When the CHANGE SLOPE pushbutton, SW87, is pressed, the slope of the trigger signal changes. The circuit operates as follows to change slope: When SW87 is pressed, the positive level (with respect to negative levels in this circuit) at the base of the on transistor is coupled to the base of the off transistor. This raises the level at the base of the off transistor enough to bring it into conduction and its collector goes negative. The negative-going change at the collector of this transistor is connected to the base of the on transistor to turn it off. The multivibrator switches states and the unit is triggered from the opposite slope. The circuit remains in this condition until the CHANGE SLOPE button is pressed again (or changed by external program).

The trigger slope can be externally programmed through terminal 27 of the front-panel PROGRAM connector, J30. In the External Mode of operation, —12.2 volts is applied to the base of Q85 through D89, R89 and R85 (see Operating Mode Power for explanation of how External Power is obtained). Q85 is reverse biased by this negative voltage at its base and positive-slope triggering is established. Operation of the remainder of the circuit is the same as just described for positive-slope triggering in the Manual Mode. To change the trigger slope to minus, grounding external program slope logic is connected to terminal 27 of J30. This raises the level at the base of Q85 positive to forward bias it. Q85 turns on and establishes negative-slope triggering. Operation of the circuit is the same as described previously for negative-slope triggering. When the grounding level at terminal 27 is removed, the Slope Multivibrator reverts to positive-slope triggering.

Trigger Shaper

The input transistor, Q104, of the Trigger Shaper stage is a low-impedance, current driven amplifier. The base level of Q104 is set at about —4 volts by divider R101-R102 between —12.2 volts and ground. This establishes a level of about —3.5 volts at the emitter. The input signal to this stage is applied through either D66 or D96 as described under Slope Comparator and Slope Multivibrator. When the Slope Multivibrator raises the anode level of either diode above about 3 volts, the corresponding half of the Slope Comparator is connected to the Trigger Shaper stage.

Tunnel diodes[1] D105 and D115 are connected so that when one diode is in its high-voltage state the other diode must be in its low-voltage state. Therefore, when switched by the trigger signal, either D105 or D115 changes to its high-voltage state and the other diode changes to its low-voltage state. Tunnel diodes characteristically switch from the low-voltage state to the high-voltage state very rapidly. However, they are slower when switching back to the low-voltage state. The configuration used in this stage provides both a fast leading edge and a fast trailing edge on the trigger signal.

Circuit operation is as follows: Assume that the signal at the emitter of Q104 is at its most negative level. This also produces a negative level at the collector of Q104 which holds D105 in its low-voltage state and D115 in its high-voltage state. As the Slope Comparator switches, the current through Q104 increases. This increase in collector current switches D105 to its high-voltage state to produce a fast leading edge on the trigger signal. The increase in current through Q104 also depletes enough current from D115 to switch it back to its low-voltage state. L106 opposes the sudden change in current at the collector of Q104 and provides a higher collector load during the transition period to aid in switching the tunnel diodes. The circuit remains in this condition until the Slope Comparator is switched again by the trigger signal applied to the input. Then, the collector current of Q104 decreases and the current through D115 increases. D115 switches to its high-voltage state to produce a fast trailing edge on the trigger signal. Current through D105 decreases and it returns to its low-voltage state. Again L106 aids in switching the tunnel diodes.

The trigger signal at the output of this stage is connected to the Sweep Generator circuit through the Pulse Amplifier and to the Seek Circuit through the Seek Circuit Driver.

Pulse Amplifier

The trigger signal at the output of the Trigger Shaper stage is connected to the base of Q134 through R131. The

[1]See General Electric "Tunnel Diode Manual" for explanation of tunnel diode operation.

trigger signal at this point is basically a rectangular pulse with a fast rise and fall. The width of this pulse depends upon the input signal waveshape and the LEVEL control setting. Q134 is connected as an amplifier with the primary of T140 providing the only collector load. Since transformers respond only to a changing current, the signal at the secondary of T140 consists of negative-going pulses approximately 10 nanoseconds wide, which are coincident with the fall of the positive-going signal at the base of Q134 (inverted by transformer). The secondary of T140 is prevented from going negative by D142. Therefore, only the positive-going trigger pulses are applied to the Sweep Generator. The negative-going trigger pulses at the collector of Q134 are also coupled to the Bright Baseline circuit through D281.

Seek Circuit Driver

The trigger signal at the output of the Trigger Shaper stage is also connected to the base of Q124 through R119. The output signal at the collector of Q124 is connected to the Seek Circuit through terminal 14 of J400.

Trigger Level Amplifier

The Trigger Level Amplifier, Q14, establishes the bias level at the base of the Input Emitter Follower, Q23. The level on the input signal at which the trigger circuit responds is determined by changing this bias level. The base level of Q14 is set at about —6 volts by divider R13-R14 between —12.2 volts and ground. This sets the level at the emitter of Q14 near —6 volts also. The quiescent current through Q14 is adjusted by the TRIG LEVEL CENTERING adjustment, R15, to provide a zero-volt level at the base of Q23 when the LEVEL control is centered. The source of the control current which determines the triggering level is selected by the Trigger Mode Logic stage. Level current may come from the manual LEVEL control, R25A, through D10, the Auto Trigger P-P Level stage through D39 or external program trigger level through D42. The Trigger Mode Logic stage allows current from only one of these sources to pass to the emitter of Q14 (see Trigger Logic discussion).

Auto Trigger P-P Level

The trigger level for auto triggering is established by the Auto Trigger P-P Level stage, Q33 and Q34. The output level from this stage is determined by R25B at the base of Q33. The network D23-D24-D26-C23-C26 around R25B comprises a peak-level sensing network which allows R25B to be adjusted between two voltage levels representing the most negative and positive peaks of the trigger signal. This provides trigger level adjustment for the auto trigger mode over at least a 10% to 90% range of the trigger signal transistion. It also allows the unit to be triggered at all positions of the LEVEL control if the minimum frequency and amplitude specifications are met. This is accomplished as follows: when the trigger signal at the emitter of Q23 rises positive, D23 is forward biased and C23 charges toward this positive level. When the signal goes negative, D23 is reverse biased and D26 is forward biased through D24. C26 charges toward the level of the negative peak. After several cycles, C23 is charged to the level of the positive peaks and C26 to the level of the negative peaks. This effectively places the peak-to-peak voltage of the input signal across R25B at all times. Due to some losses in the circuit, this voltage will be slightly lower than the total this positive level. When the signal goes negative, D23 is peak-to-peak voltage which results in a range of at least 10% to 90% of the trigger signal transition. Therefore, in the auto trigger mode, the trigger level can not be set to a point which does not allow the unit to trigger.

The level selected by R25B is connected to the base of Q33. Q33 and Q34 are connected to operate with very low input current. C31, connected from the collector of Q34 to the base of Q33, slows down the action of the circuit and keeps it from changing the output level too quickly due to a transient change in trigger signal amplitude. The output level at the collector of Q34 is connected to the Trigger Level Amplifier stage through D39 as selected by the Trigger Mode Logic stage.

Trigger Latch Circuit

The Trigger Latch Circuit is comprised of Q54 in the Sweep Trigger circuit and Q634 in the Seek Circuit. A simplified diagram of this circuit is shown in Fig. 3-8. Only the components essential to this explanation are shown on this diagram. Note that the collector of Q634 is connected to the base of Q54 and the collector of Q54 is connected to the base of Q634. Connected in this manner, Q54 and Q634 comprise a latch circuit. When either transistor is on, they are both on and when either transistor is off, they are both off. The output levels from this stage control the Trigger Mode Logic stage and the trigger-level diodes through D9 and D52. The following description explains the condition of this stage in each mode of operation. More information on the operation of this circuit is given under Trigger Mode Logic.

Manual Mode. In the Manual Mode of operation, —12.2 volts Manual Power (see Operating Mode Power discussion) is applied to the base of Q54 through D54 and R54. This negative voltage forward biases Q54 and its collector goes positive to about zero volts. This in turn forward biases Q634 to "latch up" the circuit. (Since Q54 is held on through D54, the unit may be operated without the Logic Card for Manual Mode only operation.) The positive collector level of Q54 also forward biases D52 to allow the Trigger Function switch (or external program) to determine trigger coupling, source and mode (note exception for auto triggering) and reverse biases D9 to allow manual level current to pass through D10. For auto triggering in the Manual Mode of operation, the base of Q54 is connected to ground by SW50 and the Trigger Latch Circuit turns off. When the Trigger Latch Circuit turns off, D9 disconnects the manual level control current and D52 is reverse biased to disconnect the Trigger Function switch. Now the Auto Trigger P-P Level stage determines the trigger level (see Trigger Mode Logic discussion for more information).

Seek Mode. In the Seek Mode, operation of the Trigger Latch Circuit is determined by a voltage level from the Bright Baseline stage (see Bright Baseline discussion) which is connected to the base of Q54 through D299. When a seek command is received, the seek mono pulse produced by Q625 (see Seek Circuit discussion) momentarily forward biases Q634 through D632-C632. If the unit is correctly triggered, the voltage level from the Bright Baseline stage is negative enough to reverse bias D299. This allows Q54 to conduct and the Trigger Latch Circuit remains on. When

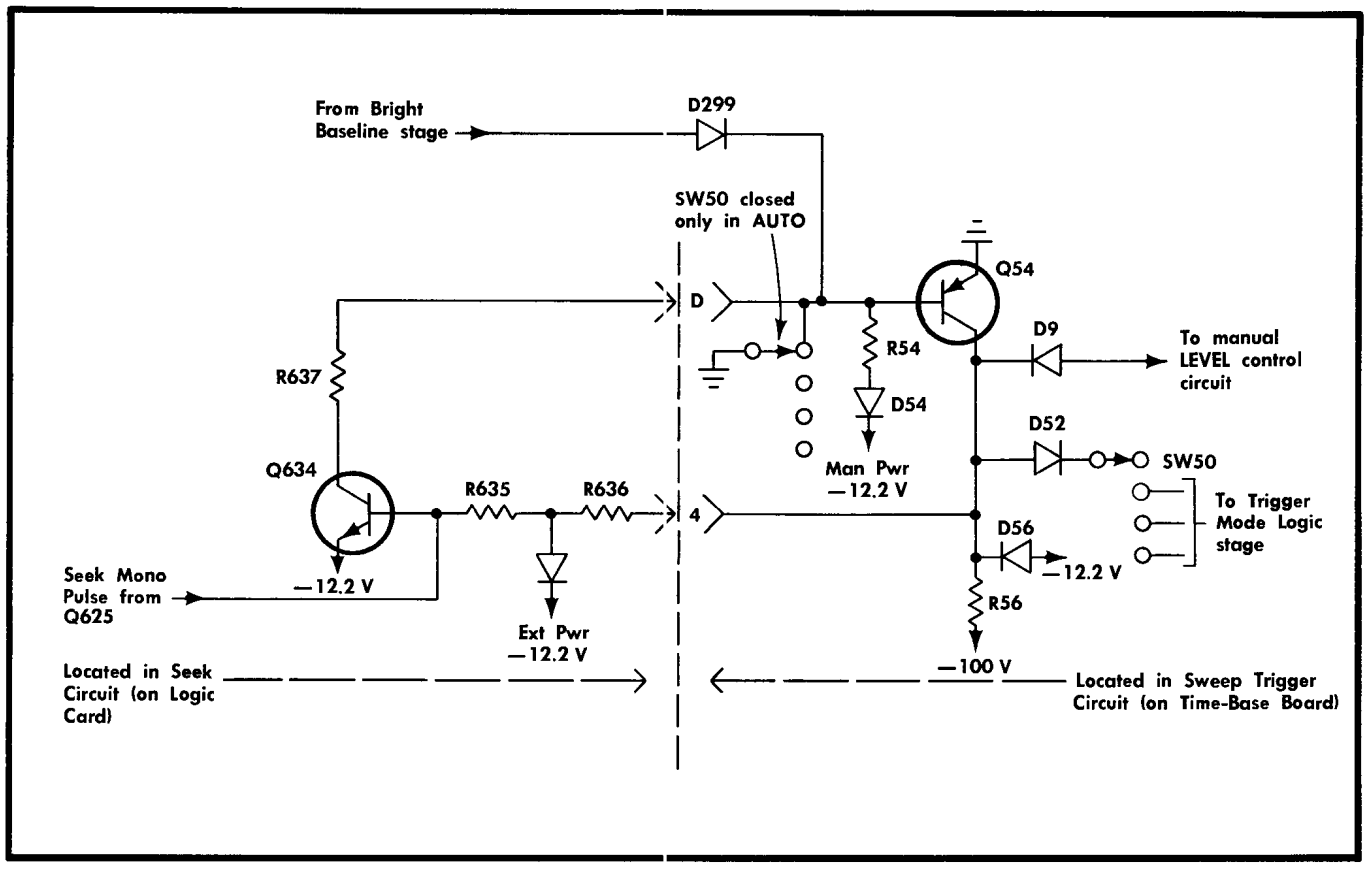


Fig. 3-8. Simplified diagram of Trigger Latch Circuit.

the Trigger Latch Circuit is on, the front-panel trigger controls determine the circuit operation. However, if the unit is not correctly triggered, the output level of the Bright Baseline stage is positive enough to forward bias D299. With D299 forward biased, the base of Q54 rises positive and the Trigger Latch Circuit is shut off. This disconnects the front-panel trigger controls and the Trigger Mode Logic stage switches to auto trigger operation. The operation described here allows the unit to switch to the auto trigger mode, if not correctly triggered, to present a stable display whenever possible in the Seek Mode of operation.

The following logic sequence takes place each time a seek command is received:

TABLE 3-1

Trigger Logic Sequence (Seek Mode)	Visual Indication
I. Seek mono pulse (produced when seek command is received) momentarily turns on Trigger Latch Circuit.	SEEK button lights.
II. Trigger Latch Circuit checks for correct triggering as set by front-panel controls.	
A. Triggered	
1. Trigger Latch Circuit remains on and unit operates as set by the front-panel controls.	Stable CRT display presented.
2. If the unit is no longer correctly triggered after correct triggering has been established as set by the front panel controls (e.g., level of trigger signal changes or external trigger signal is interrupted) the unit reverts to auto triggering (see next step).	
B. Not triggered Trigger Latch Circuit shuts off and Trigger Mode Logic stage switches to auto triggering. Auto Trigger P-P Level stage checks for internal trigger signal.	NOT TRIG'D readout and Auto Trigger light come on.
1. **Triggered.** If auto trigger level can be obtained, sweep rate seeking is performed. Unit remains in auto trigger mode until next seek command is received.	Auto trigger light remains on. NOT TRIG'D readout turns off. Stable CRT display presented.
2. **Still not triggered.** If auto trigger level cannot be obtained, Bright Baseline stage free runs sweep (typically 2 s/DIV sweep rate).	NOT TRIG'D readout and Auto Trigger light remain on. Free running sweep presented.
III. This logic sequence is repeated when the next seek command is received.	

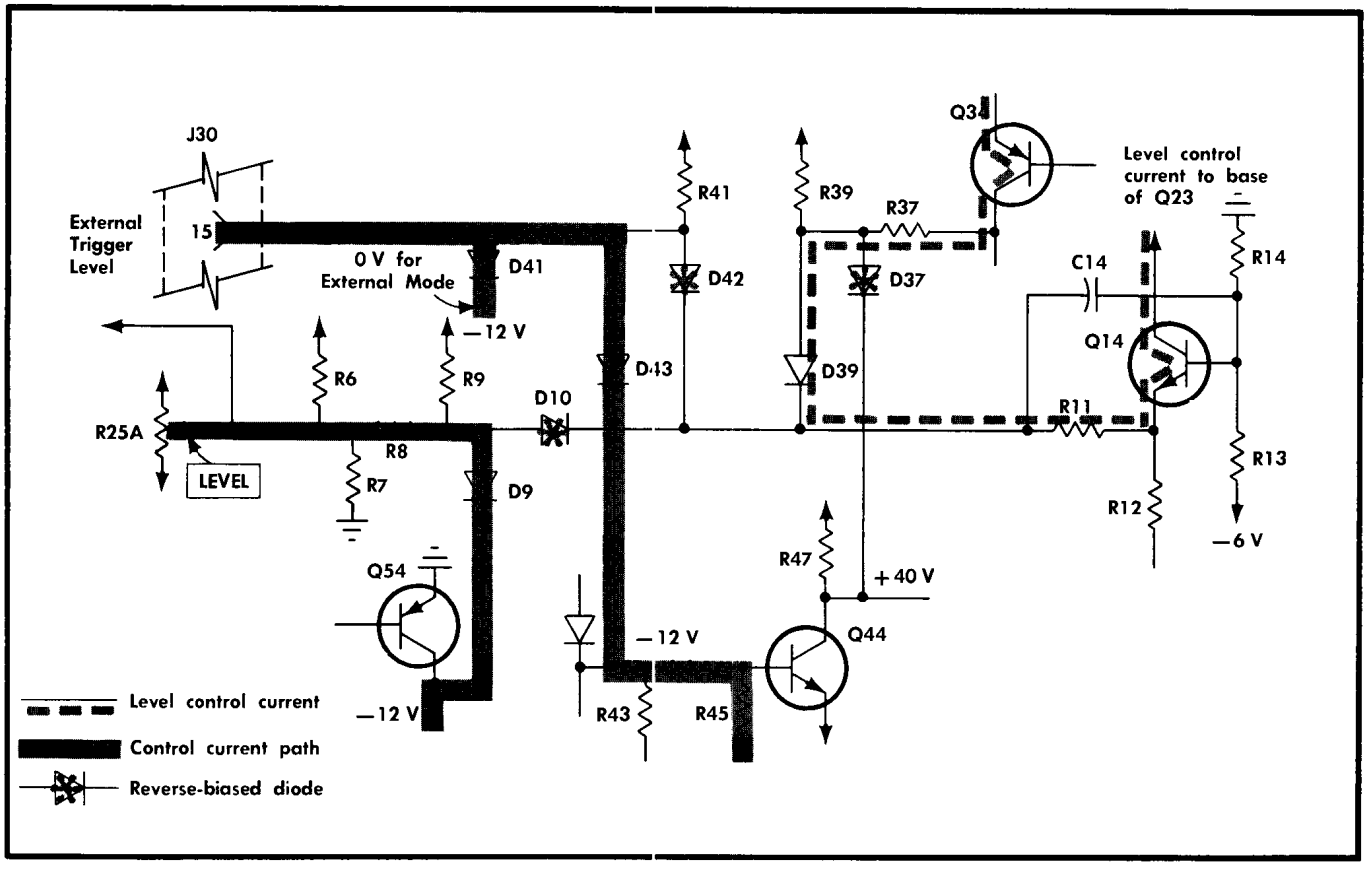


Fig. 3-9. Trigger level current for auto triggering (Manual Mode, Seek Mode or External Mode operation).

External Mode. For External Mode operation, —12.2 volts External Power is applied to the base of Q634 through D635. This holds the Trigger Latch Circuit off and the manual trigger LEVEL control and the Trigger Function switch are disconnected. Now, the operation of the Trigger Mode Logic stage is controlled by the external program function logic connected to J30.

Trigger Mode Logic

General. The Trigger Mode Logic stage selects the trigger mode, coupling and source. For Manual and Seek Mode operation, the Trigger Function switch controls operation (note exception given above for Seek Mode). For External Mode operation, these functions are controlled by external program function logic through J30. In all modes of operation, trigger source, coupling, mode and level are determined by the condition of relays K3 and K4 and diodes D10, D39 and D42. Therefore, the following description is written to relate circuit operation in each mode to these components.

Manual Mode. The Trigger Function switch, SW50, controls Sweep Trigger circuit operation for the Manual Mode of operation. In the INT-AUTO position, D52 is disconnected from the Trigger Mode Logic stage. SW50 also connects the base of Q54 to ground to shut off the Trigger Latch Circuit and the collector of Q54 goes negative. This forward biases D9 and drops the voltage level at the anode of D10 to a level that reverse biases it. Fig. 3-9 shows the condition of the logic diodes for auto triggering. The level-control current from the front-panel LEVEL control is shunted away from the Trigger Level Amplifier. No connections are made to K3 or K4 so no control current flows through either relay and the corresponding switches are not actuated. This means that the applied trigger signal is AC coupled from the internal source. With no current through K3 or K4, the cathode of D46 drops to about —12 volts. D43 is forward biased and D42 reverse biased to divert the external program level current away from the Trigger Level Amplifier. In addition, Seek/Manual Power (see Operating Mode Power discussion) is connected to the cathode of D41 to forward bias it and insure that D42 remains reverse biased. The —12-volt level at the cathode of D46 allows the base of Q44 to go toward —12.2 volts and it is reverse biased. The collector of Q44 rises toward the +125-volt supply and when this voltage reaches the firing potential of B47, Auto Trigger indicator, it comes on to indicate that the trigger circuits are operating in the auto trigger mode. The positive-going potential at the collector of Q44 reverse biases D37 and allows D39 to conduct. This connects the auto trigger level control current from the Auto Trigger P-P Level stage to the emitter of the Trigger Level Amplifier. The collector level of Q44 is also connected to the Bright Baseline stage through D296.

Complete operation is only described for the INT-AC position of normal triggering since operation in the INT-AC, EXT-AC and EXT-DC positions of the Trigger Function switch are basically the same except for control of the current through K3 and K4. Only the differences are given for EXT-AC and EXT-DC. When SW50 is in the INT-AC position,

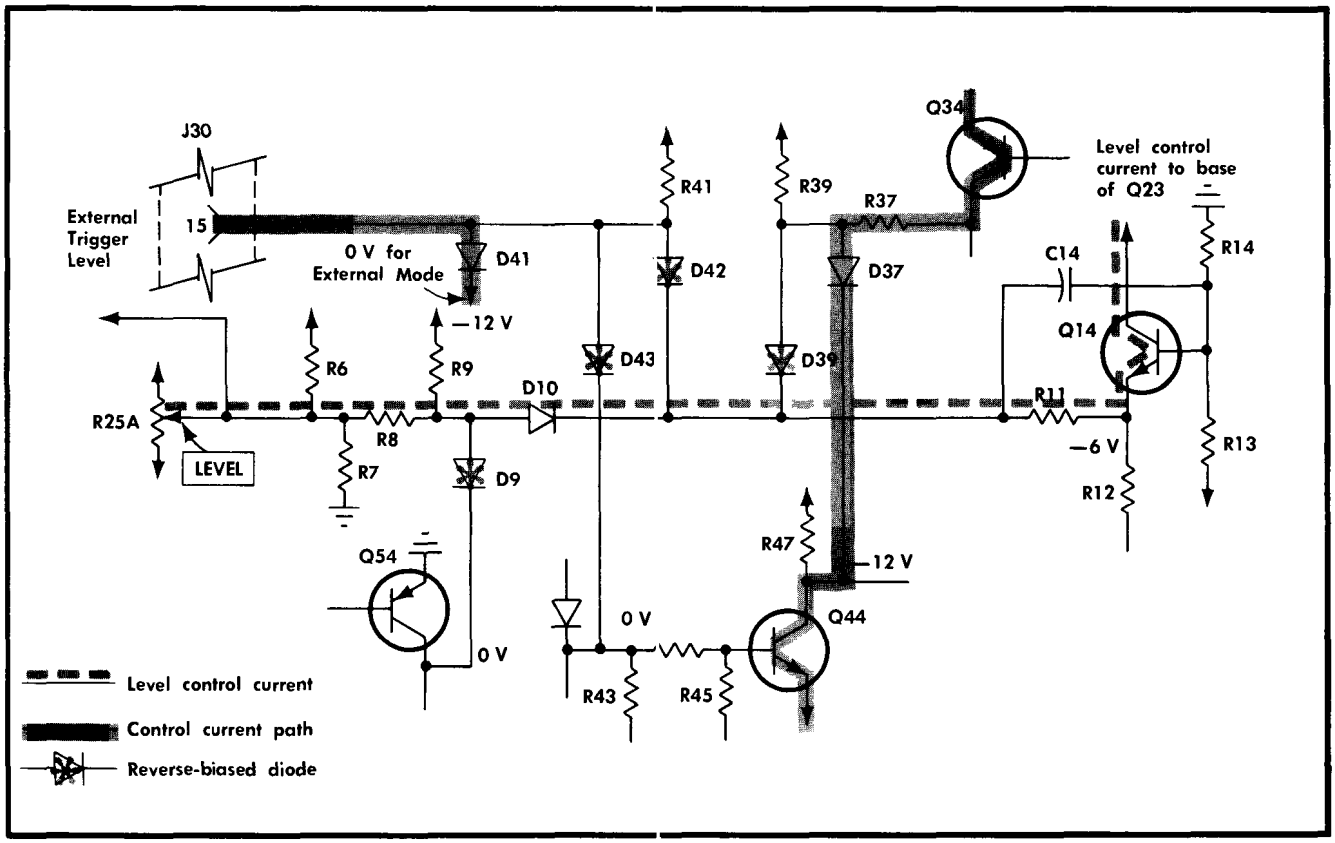


Fig. 3-10. Trigger level current for Manual Mode triggering (non-auto).

the base of Q54 is pulled toward −12.2 volts by the Manual Power applied as previously discussed. The Trigger Latch Circuit turns on and forward biases D52 and reverse biases D9. When D9 is reverse biased, manual level current from the LEVEL control, R25A, is connected to the emitter of Q14 through D10. Fig. 3-10 shows the condition of the logic diodes for manual level operation. The output of the Trigger Latch Circuit rises to about zero volts and this level is connected to the cathode of D46 through D52 and SW50. D46 remains reverse biased and no current flows through either K3 or K4. K3-1 remains in the internal position and K4-1 remains in the AC position. The positive level at the cathode of D46 reverse biases D43. However, the external program level current is still shunted from Q14 by D41 due to the Seek/Manual power applied to it. Q44 is also biased into conduction and its collector goes negative to turn off the Auto Trigger light. With the collector of Q44 negative, D37 is forward biased and the auto trigger level current is shunted.

In the EXT-AC position of SW50, the zero-volt output of the Trigger Latch Circuit is applied to the anode of D46. D45 remains reverse biased and current does not flow through K4. However, current does flow through K3 and K3-1 switches from the internal source to the external. D46 is forward biased and the base of Q44 rises positive to forward bias it. The remainder of the circuit operates as described for INT-AC.

In the EXT-DC position of SW50, the near-ground potential at the collector of Q54 is connected to the anode of D45. Current flows through K4 and K4-1 closes to provide DC-coupling of the signal to the Input Emitter Follower. Also, D45 is forward biased and current flows through K3 to switch K3-1 to the external trigger source. Q44 is turned on through D46 to lock out the auto trigger level current. The remainder of the circuit operates as described for INT-AC.

Seek Mode. In the Seek Mode, operation is determined by the setting of the LEVEL control, Trigger Function switch and the presence (or absence) of a trigger signal. As described in the Trigger Latch Circuit description, Q54 is momentarily turned on each time a seek command is received (except in INT-AUTO). Then, Q54 remains on if the unit is correctly triggered and operation is the same as described for Manual Mode (not auto triggering). However, if the unit is not correctly triggered or SW50 is set to INT-AUTO, Q54 turns off and the instrument switches to auto triggering. Then, operation is the same as described for auto triggering under Manual Mode.

If for some reason the trigger circuit is no longer triggered because, for example, the level of the trigger signal has changed after normal triggering has been established, the output of the Trigger Latch Circuit goes negative. Manual trigger level current is disconnected and the Trigger Mode Logic circuit reverts to auto triggering.

External Mode. In the External Mode of operation, the output of the Trigger Latch Circuit is negative as determined by External Power applied to the circuit (see Trigger Latch Circuit discussion). D9 is forward biased to shunt the manual

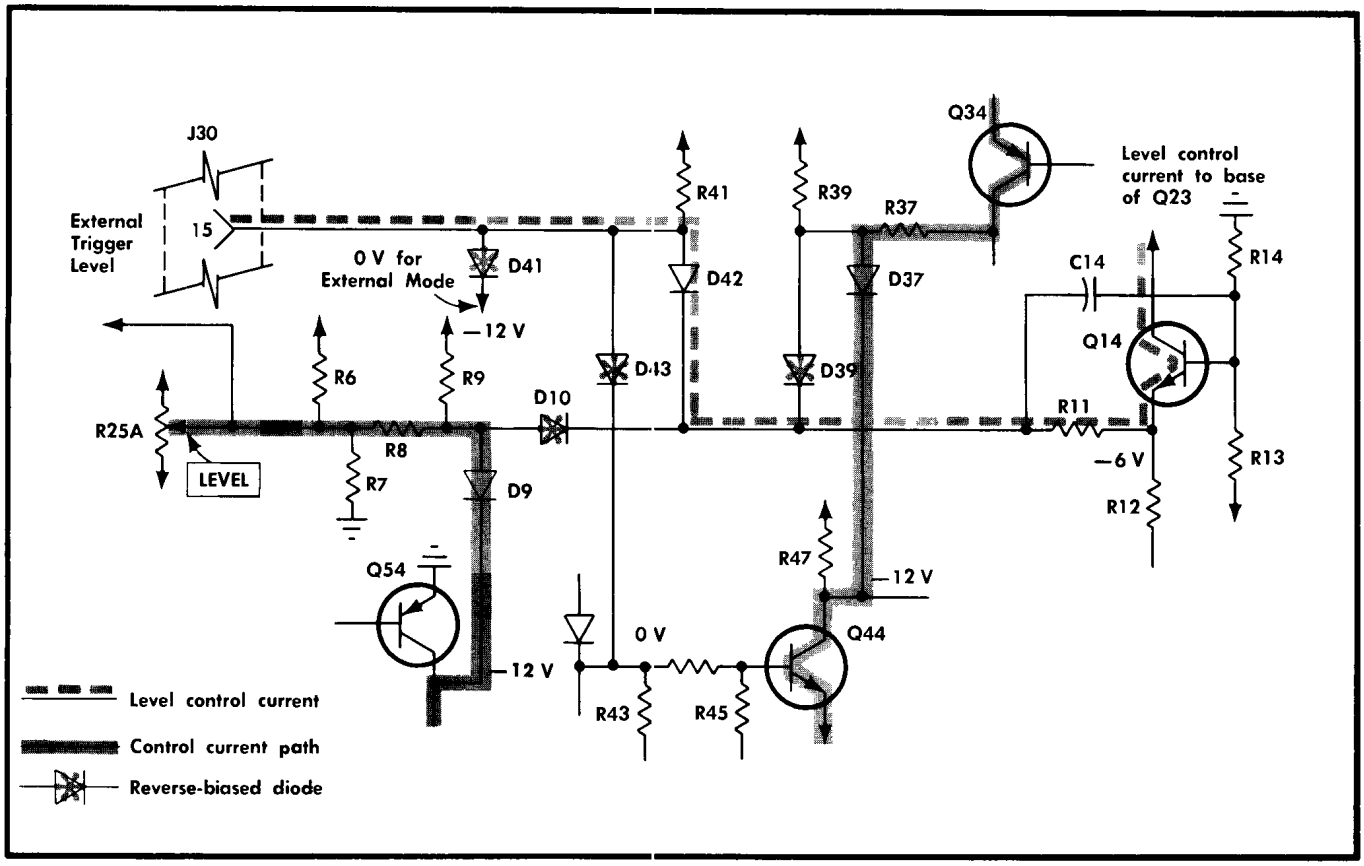


Fig. 3-11. Trigger level current for External Mode triggering (non-auto).

level current and D52 is reverse biased to disconnect the Trigger Function switch. Now, trigger source, coupling and mode are selected by connecting grounding (zero-volt external program function logic to either terminal 28, 30 or 31 of the PROGRAM connector. If no connections are made to these three terminals, the circuit operates in the auto trigger mode. Since there are no connections to the base of Q44, it goes negative and turns off. The Auto Trigger light comes on and D37 is reverse biased to allow auto trigger level current (controlled by the front-panel LEVEL control) to be connected to the Trigger Level Amplifier. Also, D43 is forward biased by the negative potential in the base circuit of Q44 and it shunts the external program level control current away from Q14. The Seek/Manual Power at the cathode of D41 is disconnected in the External Mode of operation so this diode is, in effect, reverse biased.

For Int AC operation, grounding external program function logic is connected to terminal 31 of J30. This places a zero-volt potential at the cathodes of D46 and D43. D46 remains reverse biased and no current flows through either K3 or K4. K3-1 and K4-1 remain in their unactuated positions for AC coupling from the internal trigger signal. However, D43 is reverse biased and the external program level control current is coupled to the Trigger Level Amplifier through D42. Fig. 3-11 shows the condition of the logic diodes for external level control. Zero-volt logic to terminal 31 also raises the potential at the base of Q44 and it conducts. The Auto Trigger light goes out and D37 is forward biased to shunt the auto trigger level current away from the Trigger Level Amplifier.

For Ext AC operation, grounding external program function logic is connected to terminal 30 of J30. This places a zero-volt potential at the anode of D46. D45 remains reverse biased and current does not flow through K4. However, current does flow through K3 and K3-1 is switched from the internal source to the external source. D46 is forward biased and the base of Q44 rises positive enough for it to conduct. Also, D43 is reverse biased by this positive level. The remainder of the circuit operates as described for Int AC.

For Ext DC operation, grounding external program function logic is connected to terminal 28 of J30. This places a zero-volt level at the anode of D45. Current flows through K4 and K4-1 closes to direct couple the signal to the Input Emitter Follower. Also, D45 is forward biased and allows current to flow through K3 to select the external trigger source. D43 is reverse biased and Q44 is turned on through D46 as for Ext AC operation. The remainder of the circuit operates as described for Int AC.

Sweep Generator

General

The Sweep Generator circuit produces a sawtooth voltage to provide horizontal deflection. This output signal is generated on command (trigger pulse) from the Sweep Trigger circuit. The Sweep Generator circuit also produces an unblanking pulse to unblank the CRT to display a signal. In addition, the Sweep Generator circuit can produce a

delayed, magnified sweep as controlled by the Delay and Timing Circuit. The Bright Baseline stage allows the Sweep Generator circuit to free-run when a trigger signal is not present for auto triggering. Fig. 3-12 shows a logic block diagram of the Sweep Generator circuit. A diagram of this circuit is shown on diagram 2 at the rear of this manual.

Sweep Gate

The trigger signal at the output of the Sweep Trigger circuit is applied to the Sweep Gate stage through T140. Only the negative-going portions of the trigger signal produce a voltage across the primary of T140 because D142 reflects a minimum impedance back to the primary for the positive-going portions. This produces a positive-going trigger pulse at the secondary of T140. Tunnel diode D145 is quiescently conducting about three milliamps of current which is not enough to switch it to its high-voltage state. The positive-going trigger pulse at the anode of D145 increases its current and it rapidly switches to the high-voltage state where it remains until reset by the Sweep Reset Multivibrator at the end of the sweep. The positive-going level at the anode of D145 forward biases Q144 through R145. When Q144 comes on, its collector rapidly goes negative. This negative-going step is coupled to the output emitter follower Q253 and the Disconnect Emitter Follower, Q153.

Emitter Follower Q253 provides isolation between the Sweep Gate stage and the Unblanking Driver stage. D254 clamps the emitter of Q253 so it does not go more than about 0.5 volts above ground level. The signal at the emitter of Q253 is coupled to the base of the Unblanking Driver stage through R257 and C257. This signal is also coupled to terminal 4 of the interconnecting plug, P21, and to the Seek Circuit. The signal to terminal 4 of P21 is AC coupled by C255 and it provides the alternate trace sync pulse for a multi-trace amplifier unit. The signal to the Seek Circuit is a negative-going sweep gate with an amplitude of about —6 volts. Duration of the sweep gate is the same as the duration of the total displayed sweep.

Disconnect Emitter Follower and Diode

Q153 is quiescently conducting and it forward biases the Disconnect Diode, D155. With D155 conducting, current from the Timing Resistor passes through the Disconnect Diode rather than charging the Timing Capacitor. The negative-going sweep gate at the collector of Q144 turns the Disconnect Emitter Follower, Q153, off and reverse biases the Disconnect Diode. Timing current through the Timing Resistor now begins to charge the Timing Capacitor and the sweep starts to run up. The Disconnect Diode is a low-capacitance, low-leakage, fast turn-off diode to reduce the switching time and improve timing linearity at the start of the sweep.

Sawtooth Sweep Generator, Sweep Output Emitter Follower and Timing Capacitor and Resistor

The basic sweep generator circuit is a Miller Integrator.[2] The Sawtooth Sweep Generator, Sweep Output Emitter Follower and the Timing Capacitor and Resistor stages all operate together to produce the sawtooth for horizontal sweep. When the current flow through the Disconnect Diode is interrupted by the sweep gate signal, the Timing Capacitor begins to charge through the Timing Resistor. The Timing Capacitor and Resistor are changed for the various sweep rates listed on the front panel (see Delay and Timing Circuit discussion). In the 0.1 μs position, variable capacitor C168 is the Timing Capacitor. This capacitor remains in the circuit at all sweep rates and is paralleled by the remaining Timing Capacitors for the slower sweep rates. The charging current to the Timing Capacitor provided by the Timing Resistor is increased 10 times or 100 times to provide delayed sweep magnification (see ×10 and ×100 Magnifier Gates discussion).

As the Timing Capacitor begins to charge toward —100 volts through the Timing Resistor, the grid of V163 goes negative also. This produces a negative-going change at the cathode of V163 which is coupled to the base of Q161. D162 limits the reverse voltage across the Disconnect Diode to protect it during warm up. Q161 amplifies and inverts the voltage change at the cathode of V163 to produce a positive-going signal at its collector. D165 clamps the base of Q161 to protect it during warm up. The positive-going change at the collector of Q161 is coupled to the base of the Sweep Output Emitter Follower, Q174. D172 helps turn Q174 off faster during sweep retrace. The voltage level at the emitter of Q174 is shifted six volts negative by zener diode D173 to provide the correct output DC level without attenuating the signal. The positive-going voltage change at the anode of D173 is the sweep output voltage. This voltage is also connected back to the positive side of the Timing Capacitor. This feedback rises positive at the same rate that the Timing Capacitor charges negative. Therefore, the Timing Capacitor appears to be charging toward the same potential at all times, maintaining a constant charge rate and providing a linear sawtooth output voltage. The output voltage continues to rise positive until the circuit is reset through the Sweep Reset Multivibrator.

The output voltage from the Sweep Output Emitter Follower is connected to the Horizontal Amplifier to produce the horizontal CRT deflection. It is also connected to terminal 18 of the interconnecting plug through R187 to provide a sweep signal current to the amplifier unit and to terminal 16 of the front-panel PROGRAM connector through R189 for sweep output.

Sweep Reset Multivibrator

The positive-going sawtooth voltage at the emitter of Q174 is coupled to the Sweep Reset Multivibrator through R201 and D228. The DC level of the positive-going sweep holds D228 reverse biased during most of the sweep time. However, when the sweep voltage at its anode rises positive enough to forward bias D228, it conducts and Q235 is turned off. The level of the sawtooth at which D228 conducts determines the sweep length. For unmagnified operation, $\overline{\times 1}$ (bar ×1 magnifier) logic from the Delayed Sweep Magnifier Control circuit holds the cathode of D202 near zero volts and the displayed sweep is between 10.3 and 11.3 divisions long. However, for either ×10 or ×100 magnifier operation, the $\overline{\times 1}$ logic level is about —12 volts and D203 is reverse biased. The cathode of D202 is now returned to —12.2 volts through R203. This lowers the

[2]Pulse and Digital Circuits, Millman and Taub, McGraw-Hill, 1956, P.214.

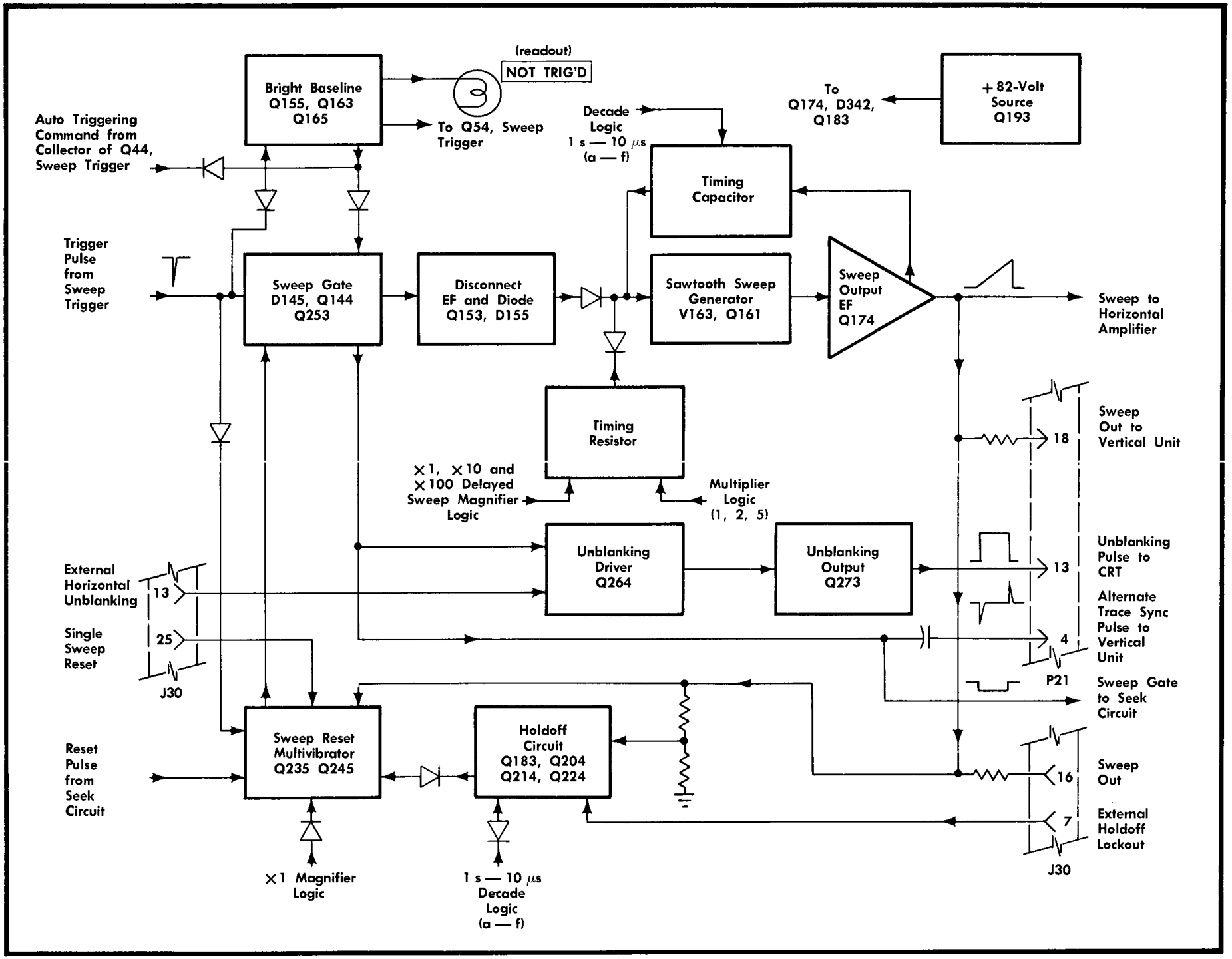


Fig. 3-12. Sweep Generator logic block diagram.

overall sawtooth level and the sawtooth must run up farther to forward bias D228. The effect is a longer sweep of between 12 and 15 divisions for magnified operation.

When the sweep rises positive enough to forward bias D228, it turns Q235 off and Q245 comes on. The Sweep Reset Multivibrator remains in this condition until reset. With Q235 shut off, its collector voltage goes negative. This pulls the anode of the Sweep Gate tunnel diode negative also and D145 reverts to its low-voltage state. D145 is held reverse biased so it cannot accept incoming trigger pulses until the Sweep Reset Multivibrator is reset. The sweep gate output pulse to Q153 and Q253 ends and Q153 and the Disconnect Diode are again forward biased. The Timing Capacitor discharges rapidly through D155 and Q153 until the grid of the Sawtooth Sweep Generator stage is returned to its original level. Now, the Sweep Generator circuit is ready to produce another sweep when the Sweep Reset Multivibrator is reset by the Holdoff Circuit and another trigger is received.

For Seek Mode operation, a positive-going reset pulse is coupled to the base of Q235 each time an advance pulse is produced (see Seek Circuit discussion). This pulse resets the Sweep Generator circuit so it starts over at the next faster sweep rate (faster sweep rate determined by advance pulse to Counter Circuit). A reset pulse can also be applied to this circuit through terminal 25 of J30. This pulse resets the Sweep Generator circuit for single-sweep operation.

Holdoff Circuit

The Holdoff Circuit allows all circuits to return to their original condition before the next sweep is started. The sweep output at the emitter of Q174 is coupled to Q183 through a 2:1 voltage divider, R181-R182. The sawtooth voltage at the emitter of Q183 is connected to the holdoff capacitors through D183 to charge them to one-half the sweep voltage level. C183 is the holdoff capacitor for the fastest sweep ranges and is connected in the circuit at all times. Holdoff capacitors C207, C217 or C227 are connected into the circuit as Q204, Q214 or Q224 are biased into operation by the decade logic level from the Readout Logic circuit. Only one of these transistors is on at a time. When the sweep retraces, D183 is reverse biased since its cathode is held at the charge level of the holdoff capacitor and its anode rapidly goes negative with the sweep retrace voltage. This interrupts the charging current to the holdoff capacitor and it begins to discharge through R183 toward −100 volts (C207, C217 or C227 discharge path includes the associated transistor and related components). When the charge on the holdoff capacitor drops to about zero volts, D229 is forward biased and the base of Q235 goes negative. Q235 comes into conduction and Q245 shuts off. The bias on the Sweep Gate tunnel diode returns to a level that allows it to accept the next trigger pulse.

For fast sweep rates, the network D241-R241-R242 forces the Sweep Reset Multivibrator to reset up to about 10% before the normal holdoff period ends. Positive trigger pulses from the Sweep Trigger circuit are coupled to D241 through T140. These trigger pulses are applied to the base of Q245 and attempt to turn it off and turn Q235 back on. However, Q235 will not come back into conduction unless its base is near the level where it would normally turn on. Then, the positive pulse at the base of Q245 raises the common emitters of Q235 and Q245 positive to bias Q235 on. The circuit is reset and the Sweep Gate tunnel diode returns to a bias level that allows it to switch on the next trigger pulse. A slight current is also added to the Holdoff Circuit from the LEVEL control, R25A, through R185 to change the charge and discharge rate for fast sweep rates and aid in this forced reset. The forced holdoff recovery is only effective at the fastest sweep rates and allows sweep synchronization for less trigger jitter at these faster sweep rates.

For single-sweep operation, a positive voltage can be connected to the Holdoff Circuit through terminal 7 of J30 and R184. This positive voltage prevents the holdoff capacitor from discharging in the normal manner at the end of each sweep. Therefore, the circuit is locked out after each sweep. The next sweep can be produced by resetting the Reset Multivibrator with a positive pulse through terminal 25 of J30. See Single-Sweep Operation in the Operating Instructions section for more information.

Unblanking Driver

The negative-going sweep gate pulse at the emitter of the Sweep Gate emitter follower, Q253, is connected to the base of the Unblanking Driver, Q264 through R257 and C257. C257 improves the response of the circuit to the fast rising and falling portions of the pulse. The emitter level of Q264 is set at about −0.4 volts by D261. Therefore, Q264 is reverse-biased when its base is pulled negative from ground. Quiescently before the sweep is triggered, the base of Q264 rests slightly positive from ground. As the sweep is triggered, the sweep gate signal at the emitter of Q253 drops to about −6 volts. Q264 is reverse biased and its collector rises positive. The DC level change at the collector of Q264 is coupled to Q273 through D265 and R265. Zener diode D265 provides DC voltage matching without a corresponding loss in signal amplitude.

An external unblanking control voltage can be connected to the base of Q264 through terminal 13 of the PROGRAM connector. −12 volts connected to this terminal reverse biases Q264 and unblanks the CRT. This method of unblanking is required for use of the external horizontal input feature.

Unblanking Output

Q273 is connected as an emitter follower. The positive-going level at the collector of Q264 produces a corresponding change at the emitter of Q273. When Q264 is turned off, its collector attempts to rise to +300 volts but is clamped at about +125 volts by D269. This level unblanks the CRT. When the sweep gate signal ends, the emitter of Q273 must be returned to its quiescent level of about +50 volts very rapidly to produce a fast falling edge on the unblanking pulse. However, when the base of Q273 drops negative, Q273 is reverse biased and it does not conduct any of this falling-edge current. D272 is then forward biased and allows the emitter level of Q273 to be pulled back to its original level through C266. This provides a sharp turn off of the trace intensity at the end of the displayed sweep.

+82-Volt Source

Q193 provides +82 volts for operation of Q174, Q183 and D342. The divider R192-R193 from +125 volts to ground sets the base level of Q193 near +82 volts. Since the emitter

level follows the base, the voltage at the emitter is about 0.5 volt less positive to establish the desired source voltage.

Bright Baseline

The negative trigger pulses applied to the primary pulses of T140 are also connected to the Bright Baseline stage through D281. Q285 and Q295 are connected as a latch circuit with the collector of Q285 connected to the base of Q295 through R291 and the collector of Q295 connected to the base of Q285 through C284-R284-D282. Negative-going trigger pulses from Q134 in the Sweep Trigger circuit are applied to the base of Q285 to turn it on and its collector goes positive. This positive-going voltage is connected to the base of Q295 and it also turns on. The collector of Q295 goes negative to about —12 volts and C284 begins to charge through R282, D282, and the base-emitter junction of Q285. This charging current holds Q285 in conduction and the circuit is latched up. If only one trigger pulse is applied, the circuit remains latched up for about 50 milliseconds until C284 is near full charge and the charging current can no longer hold Q285 in conduction. Then, the latch circuit shuts off and C284 rapidly discharges through D284 and R294. However, if another trigger pulse (repetitive trigger signal) is applied to the base of Q285 before C284 is near full charge, Q295 quickly discharges C284 and the recharge cycle begins again to hold the circuit latched up.

When the latch circuit is on (unit triggered), the base of Q293 is held negative so current does not flow through B985, NOT TRIG'D readout. The anode of D299 drops to about —6 volts and this level allows the Trigger Latch Circuit to remain on and the unit operates as set by the front-panel controls. When the unit is not triggered, the base of Q293 rises positive to forward bias Q293. The NOT TRIG'D readout, B985, comes on and the anode of D299 rises positive enough so it is forward biased. When D299 conducts it turns the Trigger Latch Circuit off and the unit switches to auto triggering (Seek Mode only). The voltage level at the collector of Q44 in the Sweep Trigger circuit is applied to this stage through D296. This voltage is about —12 volts when the instrument is triggered in the normal trigger mode and it rises to about +40 volts when the unit is in the auto trigger mode. For normal triggering, current flows through D296 or D297 to hold the anode of D148 negative enough to disconnect the Bright Baseline stage from the Sweep Gate stage. However, in the auto trigger mode, D296 is reverse biased and the only current holding D148 reverse biased is through D297 to the Bright Baseline stage. This current is high enough to hold D148 reverse biased when Q293 is off (unit triggered). However, when Q293 comes on (unit not triggered) the cathode of D297 rises to about —5 volts and it is reverse biased. Now, since D296 is also reverse biased for auto triggering, all the current through R149 flows through D149 and D148 to the Sweep Gate tunnel diode. This added current to the tunnel diode automatically switches it to its high-voltage state immediately after it is reset. The result is that the Sweep Generator circuit is automatically retriggered after the end of each holdoff period and a free-running sweep is produced. Since this trace free-runs at the sweep rate produced by the Sweep Generator, it is about the same intensity at all sweep rates.

Delay and Timing Circuit

General

The Delay and Timing Circuit selects a Timing Resistor and Timing Capacitor to determine the sweep rate of the sawtooth produced by the Sweep Generator circuit. The Timing Capacitor is selected by the decade logic and the Timing Resistor is selected by the multiplier logic from the MANUAL TIME/DIV switch or the Counter Circuit. In addition, the ×10 and ×100 Magnifier Gates increase the timing current to provide magnified sweep rates. The Delay Comparator determines the start of the magnified sweep. Fig. 3-13 shows a logic block diagram of the Delay and Timing Circuit. A diagram of this circuit is shown on diagram 3 at the rear of this manual.

Timing Capacitor

The Timing Capacitor determines the decade range of the sweep rate. The Timing Capacitor is selected by coils K310-K315 which actuate corresponding reed relays K310-1 to K315-1. Decade logic from the Readout Logic Circuit (originating at the MANUAL TIME/DIV switch or the Counter Circuit) is applied to the 1 s - 10 μs decade logic lines (a-f). To select one of the timing capacitors, the corresponding decade logic line is dropped to the —12-volt level. The remaining logic lines are held at zero volts. For example to select the 10 μs decade (10, 20 and 50 μs sweep rates), —12 volts is applied to the 10 μs (f) logic line and current passes through K315. K315-1 closes to connect C315 and C316 to the Timing Resistor. The 10, 20 or 50 μs sweep rate within this decade is selected by the multiplier logic applied to the Timing Resistor.

To select the 1 ms and slower sweep decades, K310-1 must be closed in addition to the reed relay which selects the desired Timing Capacitor. For example, to select the 10 ms decade, —12 volts is applied to the 10 ms (c) logic line. Current flows through K312 and K312-1 is actuated. In addition, D304 is forward biased and current flows through K310 to actuate K310-1. For the 1 s (a) decade range, an additional switch is actuated. Current passes through K395 to actuate K395-1 (located in Timing Resistor stage). R394, R395 and R398 are connectd into the Timing Resistor circuit to reduce the timing current through the Timing Resistor 10 times. Since the same Timing Capacitor is used for the 1 s decade as for the 0.1 s decade, the sweep rate is reduced 10 times. The Timing Capacitor for the 1 μs and faster decades is C168 (see Sweep Generator discussion). The ×10 Magnifier Gate stage is used to obtain the 0.1 μs decade and both the ×10 Magnifier Gate stage and a ×10 gain network in the Horizontal Amplifier are used to obtain the 10 ns decade.

When the decade logic to a coil ends, the collapsing magnetic field in the coil produces a reverse inductive voltage. A diode is connected across each of the coils to protect the circuit from this positive-going pulse. D302-D307 provide this protection for K310 and K311. Since all logic lines except one are at zero volts, some of the interconnecting diodes are forward biased for the positive-going pulse

Delay Comparator

The Delay Comparator stage allows selection of the amount of delay before the delayed sweep magnifier is

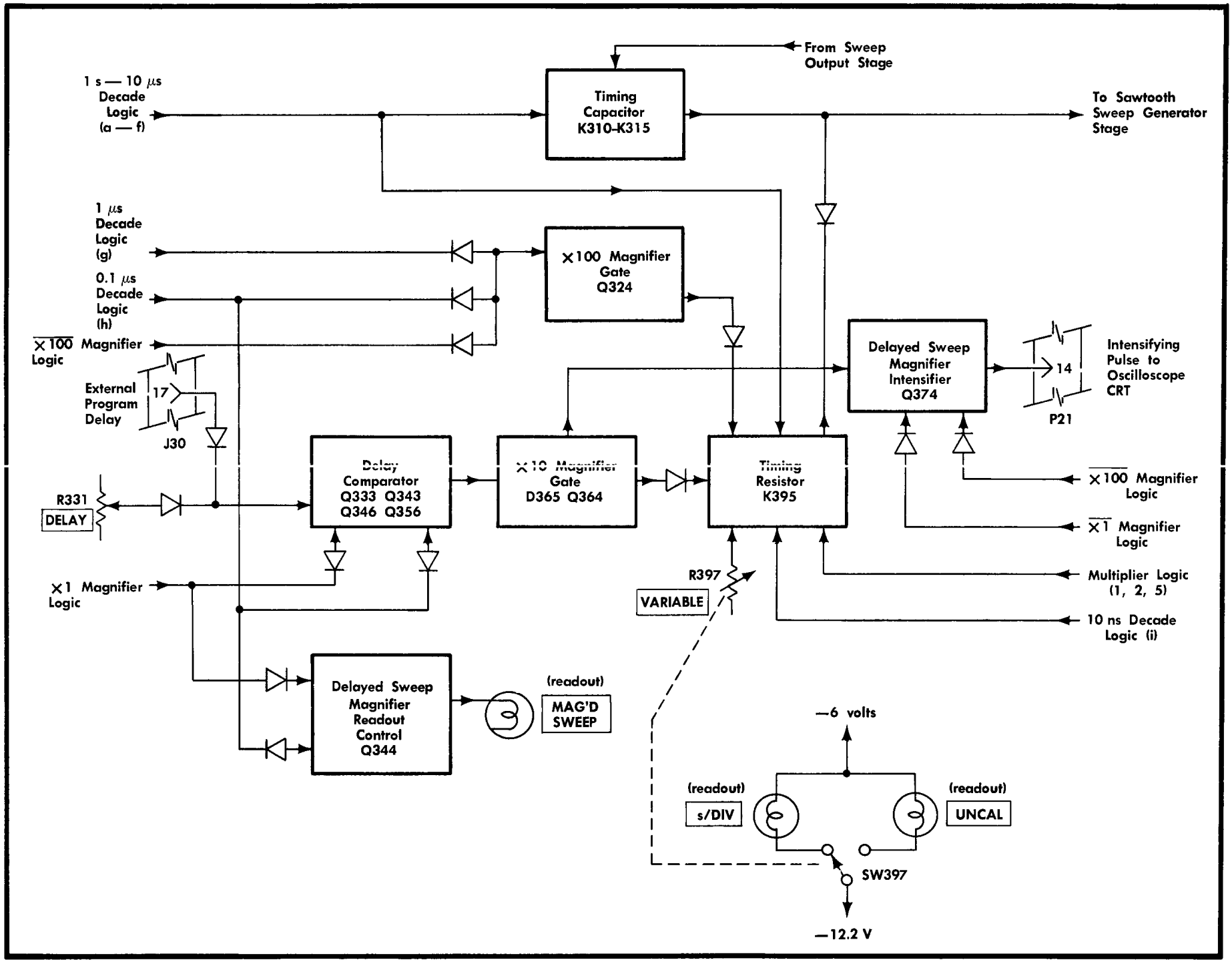


Fig. 3-13. Delay and Timing Circuit logic block diagram.

turned on. This allows any portion of the sweep to be magnified by selecting, with the DELAY control, the voltage level on the sawtooth where the delayed sweep magnifier is turned on. The DELAY control is calibrated in terms of divisions of display. For example if the DELAY dial is set to 5.00, the delayed sweep magnifier magnifies the portion of the sweep beginning five divisions after the start of the sweep.

For ×1 operation, —7 volt ×1 magnifier logic is connected to the base of Q346 through D348. The base of Q346 goes negative and is clamped at about —6 volts by D349. Q346 is reverse biased and the Delay Comparator stage is locked out so the sweep can not be magnified (note the exception for the 0.1 μs and faster decades). For ×10 and ×100 delayed sweep magnification, the ×1 magnifier logic rises to zero volts to reverse bias D348 and allow the Delay Comparator to switch at the level selected by the DELAY control. This action is as follows: quiescently at the start of the sweep, about two milliamps of current is flowing through R349. Current is also flowing through D338. The current through D338 is a combination of the current supplied by R337 and the current supplied by R336. The current through R336 can be varied between zero and one milliamp by changing the emitter level of Q333 with the DELAY control, R331. R331 is a 10-turn potentiometer to provide precise control of the current through R336. R330 and R333 provide adjustment for the voltage potential across R331. This allows R331 to be accurately calibrated for delay in terms of divisions of CRT display. When R331 is fully counterclockwise (minimum delay), the emitter of Q333 is at its most positive level and little or no current flows through R336. Therefore, there is no additional current at the base of Q346 which must be overcome to switch the comparator. However, in the fully clockwise position (maximum delay) about one milliamp of current flows through R336. This, in effect, adds an additional milliamp of current at the base of Q346 which must be overcome before the comparator can switch.

Quiescently, Q356 is on and controls the conduction of the comparator. The base of Q356 is held at about —3 volts as established by divider R352-R353 from —100 volts to ground. Therefore, the base of Q346 must rise more positive than about —3 volts before it can come on. When Q356 is on, the delayed sweep magnifier circuits are locked out. When Q346 turns on, the delayed sweep magnifier circuits are turned on also.

In addition to the quiescent currents flowing through R336, R337 and R349, the sawtooth voltage is connected to the base of Q346 through R309 and C309. This produces a current change between about zero and one milliamp at the base of Q346 as the sawtooth voltage rises. For minimum delay (zero current through R336) the two milliamp current flow through R349 and R337 holds the base level of Q346 very near its switching level. Then as the sawtooth starts to run up, only a slight level change at the base of Q346 turns it on. The delayed sweep magnifier circuits are turned on at the start of the sweep to magnify the total display. For maximum delay (maximum current through R336) the additional current from Q333 allows the base level of Q346 to go more negative. D349 clamps the base of Q346 at about —6 volts. Now, when the sawtooth starts to run up, it must offset this extra current supplied by Q333 before Q346 can switch. This will be near the positive peak of the sawtooth to turn on the delayed sweep magnifier circuits at the tenth division of display. Only the portion of the trace following the tenth division is magnified (the sweep length is increased several divisions for magnified operation; see the Sweep Generator discussion). Operation of the Delay Comparator for delay between these two extremes is much the same. A precise amount of current as determined by the DELAY control is added to the circuit by Q333. This determines the amount that the sawtooth must run up before the Delay Comparator is switched, thereby determining the point on the sweep where the magnifier is turned on.

In the External Mode of operation, —12.2 volts External Power is applied to the anode of D338 through D337. D338 is reverse biased and the DELAY control and Q333 are disconnected from the Delay Comparator stage. Then, an external program delay current can be supplied through terminal 17 of J30. The stage operates in a similar manner to that described for internal delay. However, since R336 and R337 are disconnected, the external program delay control sets the total quiescent current level in the circuit. Q343 provides 10 times current gain to provide more linear control of the external program delay.

For the 0.1 μs and 10 ns timing decades, the 0.1 μs (h) decade logic line is at —12 volts. This level is connected to the base of Q356 through D354 and R354 to hold Q356 reverse biased, and the magnifier circuit remains on to magnify the total sweep for the 0.1 μs timing decade. In the 10 ns timing decade, 10× gain of the 0.1 μs timing decade is provided by the Horizontal Amplifier. The Delay Comparator stage has no affect upon the turn-on point of the magnified circuits in these timing decades so the total sweep is magnified.

Timing Resistor

The multiplier logic applied to the Timing Resistor determines the sweep rate within the decade established by the Timing Capacitor. Resistor R381-R382-R383 form the "1" timing group, R384-R385-R386 form the "2" timing group and R387-R388-R389 form the "5" timing group. To select a timing group, either D317, D318 or D319 is allowed to conduct by reverse biasing the corresponding logic diode D391, D392 or D393 with the multiplier logic level. This level is —12-volts for the multiplier logic line to the timing group desired and zero volts for the other two logic lines. The timing current through the two timing groups not selected is shunted to the corresponding multiplier logic lines. For example, to select the "2" timing group, —12 volts is applied to the "2" logic line and zero volts to the "1" and "5" logic lines. The anode level of D317, D318 and D319 is at about —3.5 volts. Therefore, the zero-volt multiplier logic level applied to the "1" and "5" logic lines forward biases D391 and D393 to shunt the "1" and "5" timing current. The "2" logic reverse biases D392 and allows the "2" timing current to pass to the Timing Capacitor through D318. Further selection of the specific timing resistor within each timing group provides ×1, ×10 or ×100 sweep magnification. This is explained under ×10 and ×100 Magnifier Gates.

In the 10 ns decade, —12 volts 10 ns (i) decade logic is connected to the timing circuit through R390 and D390. This adds approximately 10% more current to the timing circuit for the 10 ns timing decade to improve timing accuracy.

For all sweep rates, the VARIABLE control, R397, adds additional resistance in series with the Timing Resistor when not in the CAL detent. This provides continuously variable, uncalibrated sweep rates between the 1-2-5 steps. Also note that this control is ganged with SW397 to turn on the UNCAL readout and turn off the s/DIV readout (see s/DIV and UNCAL Readout Control).

s/DIV and UNCAL Readout Control

SW397 is ganged with the VARIABLE control, R397. When the VARIABLE control is in the CAL detent, B999, s/DIV readout, is connected into the circuit. However, whenever the VARIABLE control is turned away from the CAL detent, SW397 turns off B999 and turns on B987, UNCAL readout, to indicate that the sweep rate is not calibrated. The current through B987 or B999 from the —12.2 volts supply provides current to the —6 volt line for the heater of V163. This current is provided in parallel with current supplied by the mode-indicating bulbs in the Operating Mode Power circuit.

×10 and ×100 Magnifier Gates

Q364 is the ×10 Magnifier Gate and Q324 is the ×100 Magnifier Gate. When both of these transistors are on, the sweep magnification is ×1. ×10 delayed sweep magnification is provided when Q364 is off and Q324 remains on. When both Q364 and Q324 are off, the delayed sweep magnification is ×100.

R381, R384 and R387 are the ×1 timing resistors. Only one of these resistors supplies timing current for ×1 sweep magnification as selected by the multiplier logic. For example, Fig. 3-14 shows the timing-current path for a sweep rate of one millisecond/division with ×1 sweep magnification. The 1 ms (d) decade logic actuates K310 and K313 to select the 1 ms decade. D392 and D393 are forward biased by the multiplier logic (approximately zero volts) applied to the "2" and "5" logic lines and the "2" and "5" timing currents are shunted. —12 volts on the "1" logic line reverse biases D391 and allows the "1"" timing current to pass to the Timing Capacitor through D317. The ×10 Magnifier Gate is held on by the ×1 magnifier logic applied to the Delay Comparator (see Delay Comparator discussion). This places the collector of Q364 near zero volts and the ×10 timing current is shunted through D367, D366 and Q364. The ×100 Magnifier Gate is held on by the $\overline{\times 100}$ (bar ×100 magnifier) logic. The ×100 timing current is shunted through D327 and Q324. Therefore, only the timing current through R381 charges the Timing Capacitor.

For ×10 delayed sweep magnification, ×10 timing current through R382, R385 or R388 is added to the ×1 timing current. The Delay Comparator switches Q364 off at the sweep level selected by the DELAY control (note exception for 0.1 μs and 10 ns decades; see Delay Comparator discussion). When the comparator switches, the collector of Q356 goes positive. This decreases the current through tunnel diode D365 and it switches from its high-voltage state to its low-voltage state. D365 produces a fast voltage change at the base of Q364 to turn it off quickly. When Q364 turns off, its collector drops to about —12 volts and the ×10 shunt diodes D367-D368-D369 are reverse biased. ×10 timing current is added to the ×1 timing current in the timing group that is charging the Timing Capacitor (as determined by the multiplier logic). The timing current in the other two timing groups is shunted away from the timing capacitor. For example, Fig. 3-15 shows the timing current path for ×10 delayed sweep magnification at a magnified sweep rate of 0.1 millisecond/division. Note that the same Timing Capacitor is used as in the previous example for ×1 magnification. D391 is reverse biased by the multiplier logic applied to the "1"-logic line to allow timing current to charge the Timing Capacitor through D317. The total ×10 timing current is supplied through both R381 and R382. This total timing current is 10 times greater than the ×1 timing current to increase the sweep rate 10 times. The ×100 timing current is shunted by D327 since Q364 is held on by the $\overline{\times 100}$ magnifier logic level.

For ×100 delayed sweep magnification the ×10 Magnifier Gate still controls the starting point of the magnified sweep as described for ×10 operation. The ×100 timing current is a combination of the ×1, ×10 and ×100 timing current. R383, R386 and R389 are the ×100 timing resistors. The ×100 Magnifier Gate is controlled by several logic levels. For the 1 μs timing decade, the 1 μs (g) logic line is at —12 volts. Since its base is held negative, Q324 is conducting and the ×100 timing current is locked out through D327, D328 or D329. In the 0.1 μs and 10 ns timing decades, the 0.1 μs (h) logic line is at —12 volts and the ×100 timing current is similarly locked out. These logic levels prevent sweep rates faster than 10 microseconds/division from being magnified 100 times. In addition, the $\overline{\times 100}$ magnifier logic holds the ×100 Magnifier Gate on for ×1 and ×10 sweep magnification. However, for ×100 sweep magnification the $\overline{\times 100}$ magnifier logic is zero volts and Q324 is reverse biased. The collector of Q324 goes to about —12 volts and the ×100 shunt diodes, D327-D328-D329, are reverse biased. Since the ×10 Magnifier Gate still controls the turn-on point for the delayed sweep magnifier, the ×100 timing current is shunted along with the ×10 timing current. Then, as the ×10 Magnifier Gate is turned on, both the ×10 and ×100 timing current are added to the ×1 timing current to charge the Timing Capacitor. This produces a sweep rate 100 times faster than the basic ×1 sweep rate. Fig. 3-16 shows the timing current path for delayed sweep magnification at a magnified sweep rate of 10 microseconds/division with ×100 magnification. The total ×100 timing current is supplied through R381, R382 and R383. This total current is 100 times greater than the ×1 timing current to increase the sweep rate 100 times.

NOTE

Although the DLY'D SWP MAG switch can be set to ×100 for sweep rates of 1, 2 and 5 μs, only ×10 delayed sweep magnification is provided. Sweep rates between 10 ns and 0.5 μs cannot be magnified with the delayed sweep magnifier.

Delayed Sweep Magnifier Intensifier

Q374 provides an intensifying pulse to the grid circuit of the indicator oscilloscope CRT to compensate for the lower display intensity when the sweep is magnified (due to increased sweep rate.) For ×1 magnification, the $\overline{\times 1}$ magnifier logic level at the anode of D371 is zero volts. This clamps the base of Q374 so it can not go more negative than about zero volts. The $\overline{\times 100}$ magnifier logic level at the anode of D376 is —12 volts. D376 is reverse biased and

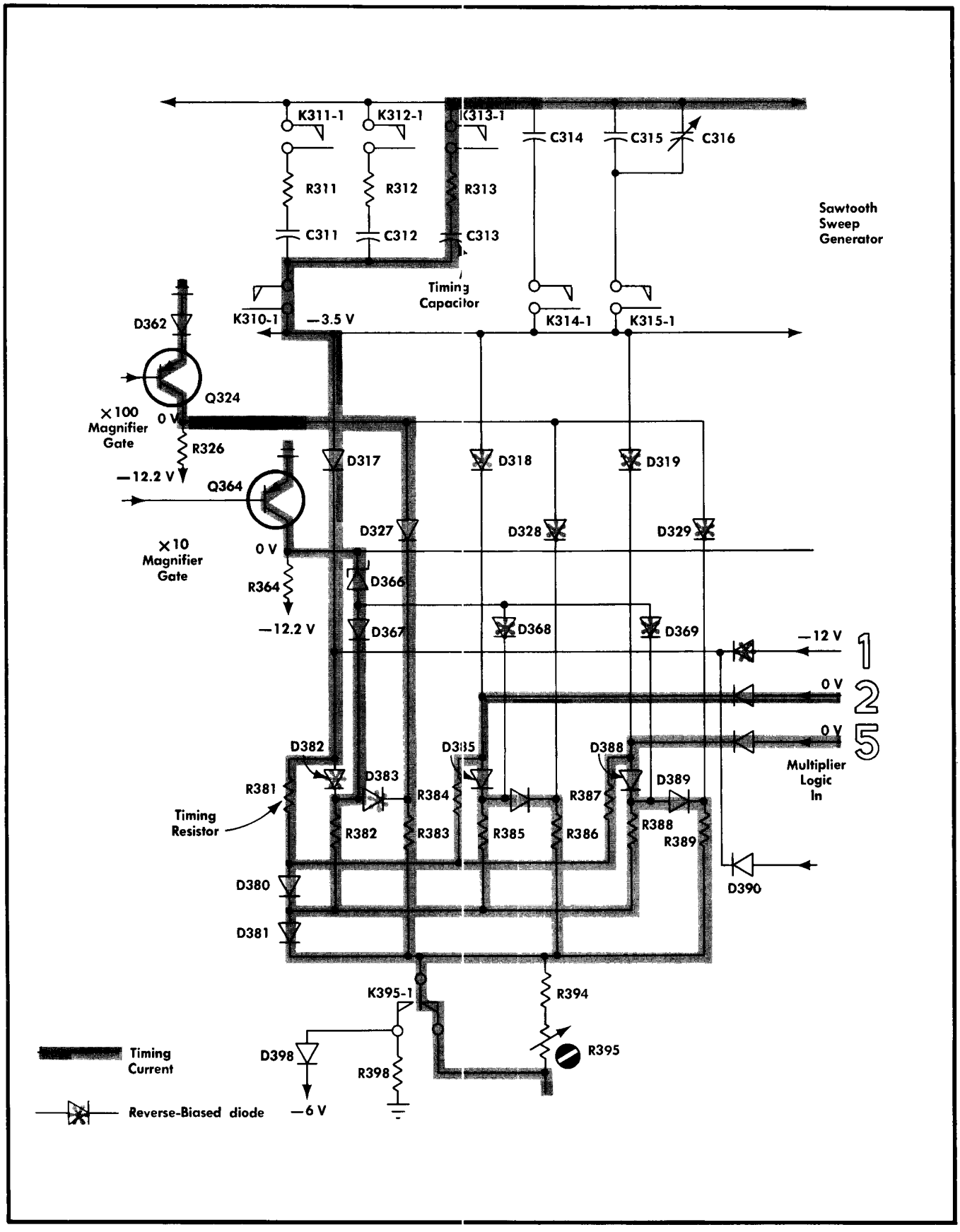


Fig. 3-14. Timing resistor for ×1 magnification (DLY'D SWP MAG switch at OFF). Sweep rate, 1 millisecond/division.

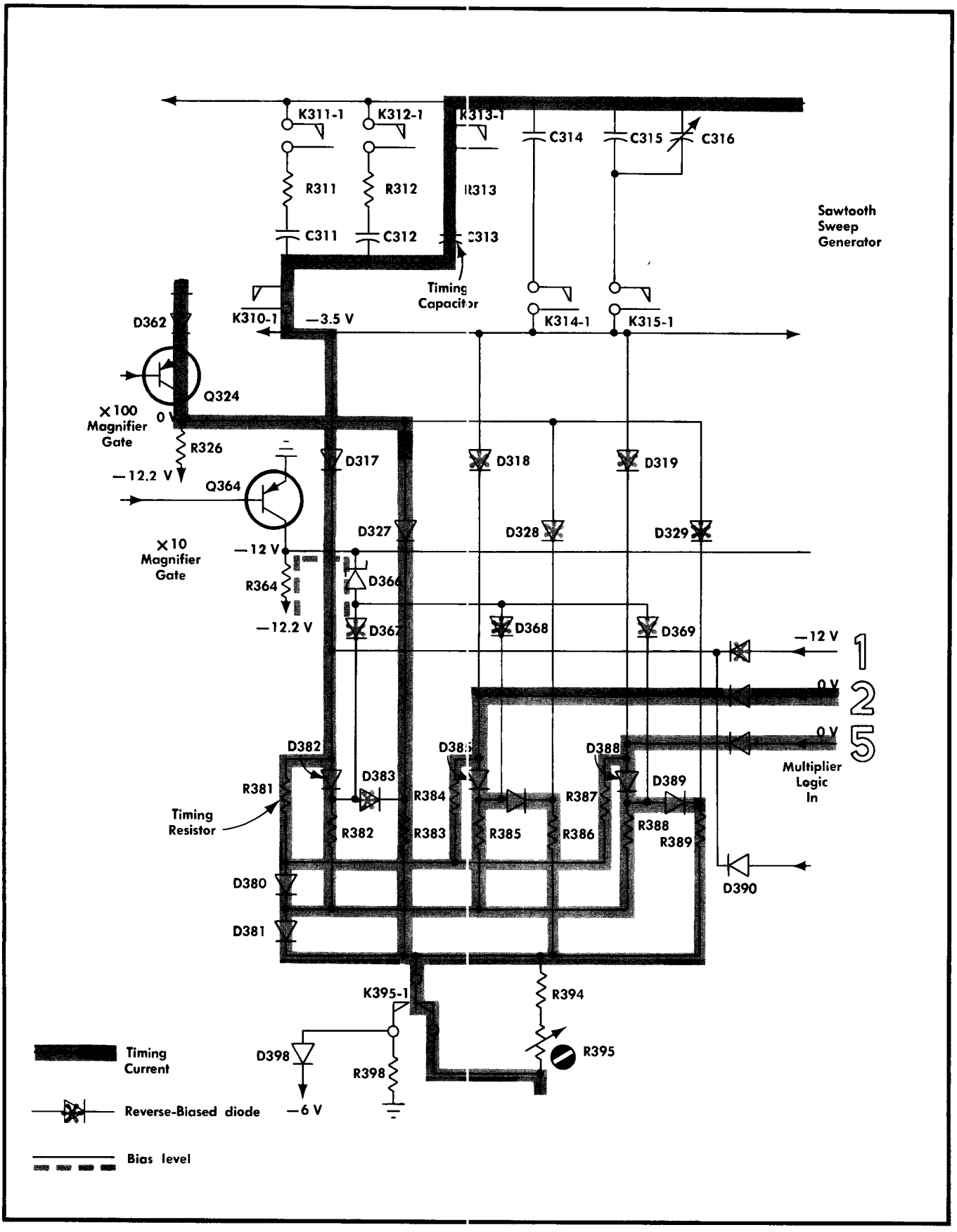


Fig. 3-15. Timing resistor for ×10 delayed sweep magnification. Magnified sweep rate, 0.1 millisecond/division.

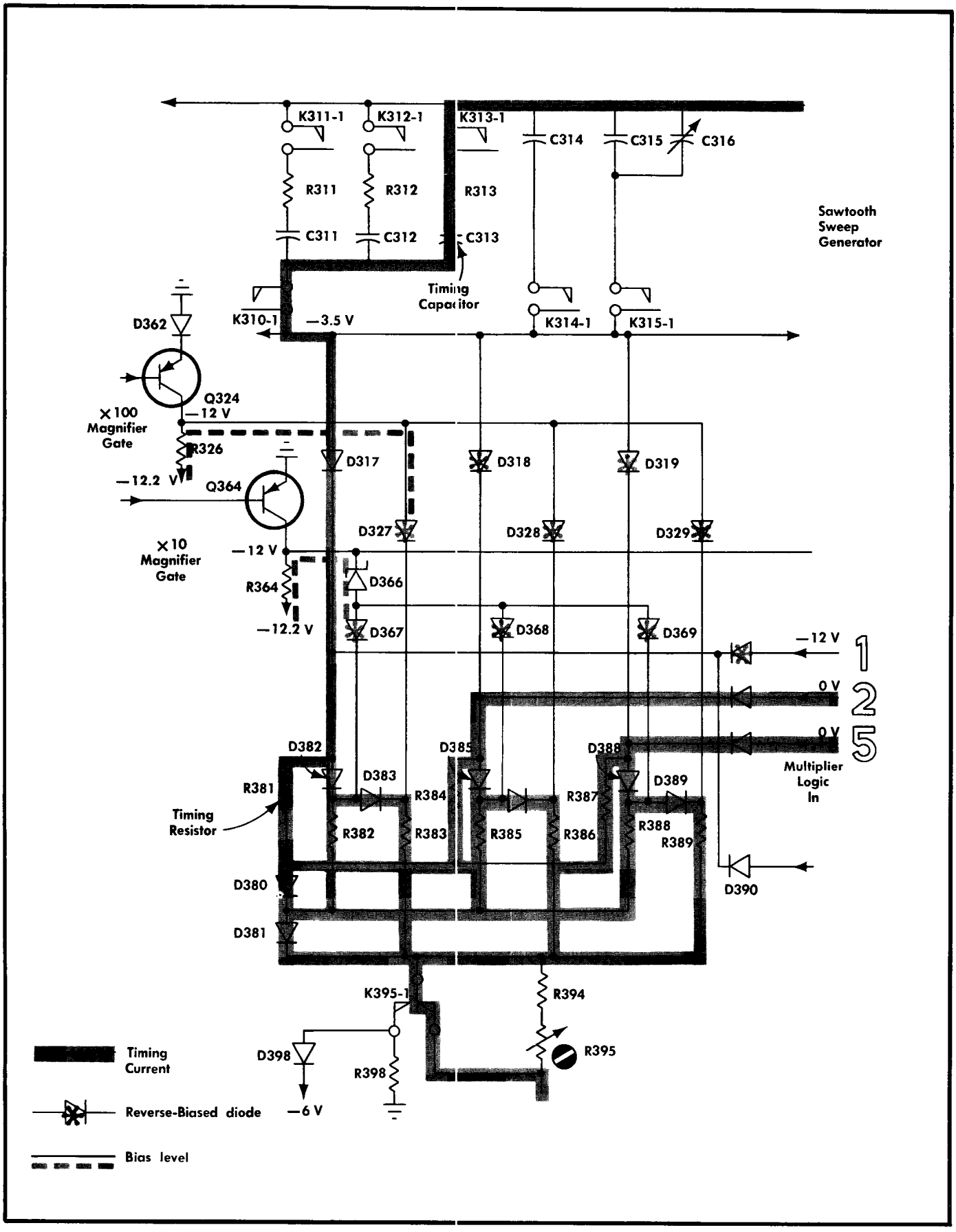


Fig. 3-16. Timing resistor for ×100 delayed sweep magnification. Magnified sweep rate, 10 microseconds/division.

zener diode D375 sets the level at the emitter of Q374 to —6 volts. Since its base is held near zero volts, Q374 is reverse biased. The collector of Q374 goes negative toward the —100-volt supply and is clamped near —12 volts by D374. This voltage level remains constant over the entire sweep for ×1 magnification. This level is coupled to the CRT grid circuit through terminal 14 of the interconnecting plug.

For ×10 delayed sweep magnification, the anode of D371 is held at —12 volts by the $\overline{\times 1}$ magnifier logic and it is reverse biased. The $\overline{\times 100}$ magnifier logic remains at —12 volts and D375 holds the emitter of Q374 at —6 volts. When the ×10 Magnifier Gate stage is turned off by the Delay Comparator, the negative voltage at its collector is connected to the base of Q374 through divider R371-R372-R373. Q374 is forward bisaed and its collector rises positive (less negative) to about —6 volts. This voltage level determines the display intensity for the magnified portion of the trace only.

Operation of the Delayed Sweep Magnifier Intensifier is basically the same for ×100 delayed sweep magnification as for ×10 except that the output is more positive to intensify the trace more. The $\overline{\times 100}$ magnifier logic level to the anode of D376 is zero volts for ×100 delayed sweep magnification. This sets the emitter level of Q374 near zero also. Now as the ×10 Magnifier Gate switches off, the collector of Q374 rises positive to about zero volts. The grid of the indicator oscilloscope CRT is raised more positive to provide a brighter intensity for the magnified portion of the trace only.

Delayed Sweep Magnifier Readout Control

The Delayed Sweep Magnifier Readout Control stage indicates when the basic sweep rate is magnified (except for basic sweep rates of 0.5 microsecond/division and faster). The ×1 magnifier logic level is connected to the base of Q344 through D345 and divider R345-R346-R347. For ×1 sweep magnification, the ×1 magnifier logic level is —12 volts and Q344 is reverse biased. Current does not flow through the readout bulbs. For ×10 and ×100 delayed sweep magnification, the ×1 magnifier logic level is zero volts. Q344 is turned on and its collector goes negative to about —12 volts. Current flows through B982 and B983, MAG'D SWP readout. In the 0.1 μs and 10 ns timing decades, the "h" decade logic line is at —12 volts. This level is connected to the base of Q344 through D344 and divider R346-R347. Q344 is again reverse biased and the indicator bulbs turn off. This logic level over-rides the ×1 magnifier logic level. Since the magnifier is used to provide the basic sweep rate when using the 0.1 μs (h) timing decade, the delayed sweep magnifier is not operable and the MAG'D SWP readout is locked out.

Horizontal Amplifier

General

The Horizontal Amplifier provides the output signal to the left and right deflection plates of the indicator oscilloscope

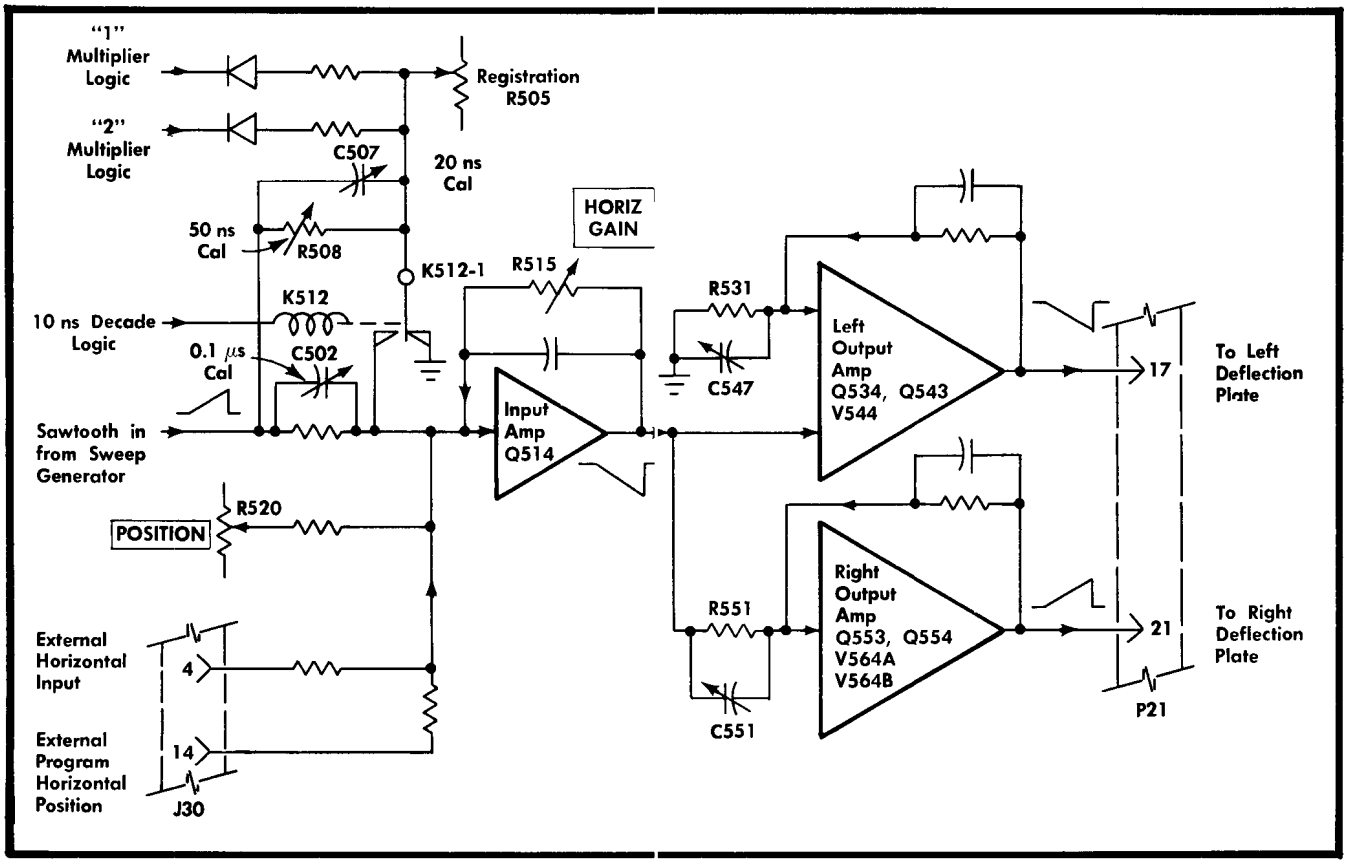


Fig. 3-17. Horizontal Amplifier logic block diagram.

CRT for horizontal deflection. This circuit contains the horizontal positioning network and an adjustment to calibrate the horizontal gain of this unit to the deflection sensitivity of the indicator oscilloscope. An external horizontal deflection signal can be applied to the circuit through terminal 4 of J30 and an external horizontal position level through terminal 14 of J30. A ×10 gain network is connected to the base circuit of the Input Amplifier to provide the correct sweep rate for the 10 ns timing decade (i). Fig. 3-17 shows a logic block diagram of the Horizontal Amplifier. A diagram of this cirucit is shown on diagram 4 at the rear of this manual.

Input Amplifier

The Input Amplifier, Q514, is a feedback (operational) amplifier to provide stable gain and low input impedance. The HORIZ GAIN adjustment, R515, in the feedback loop controls the amount of feedback from the collector to the base, thereby setting the overall gain of the stage. The input impedance of the Input Amplifier is low and it is a current-driven amplifier. For normal operation, the base of Q514 is driven from three current sources: 1) The sawtooth voltage applied through R501-R502-C502 produces a corresponding sawtooth current at the base of Q514; 2) A quiescent bias current is applied to the base of Q514 through R523 and R529; 3) The horizontal POSITION control adds or removes current at the base of Q514.

For the 10 ns timing decade, 10 ns (i) decade logic energizes K512. K512-1 connects the network C507-R507-R508-R509 in parallel with C502-R502 to provide 10 times more sawtooth current to Q514. This produces an output sawtooth which rises 10 times faster to provide the desired 10 times gain increase for the 10 ns timing decade. R505 adds a positioning current to the base circuit for registration in the 10 ns timing decade. This added current allows the trace to start at the same point on the graticule when switching from 0.1 microseconds/division to 50 nanoseconds/division. For the 10 nanosecond and 20 nanosecond sweep rates, an additional positioning current is added by the —12-volt level on either the "1" or "2" logic line.

The Horizontal Amplifier may be used to provide horizontal deflection from sources other than the internal sweep generator by applying the horizontal deflection signal to terminal 4 of J30. The Sweep Generator must be disabled by applying a lockout signal through terminal 7 of J30. An unblanking voltage is also necessary at terminal 13 of J30. See External Horizontal Deflection in Section 2 for complete operating information.

For External Mode operation, the horizontal position of the display can be externally controlled through terminal 14 of J30. In this mode, —12.2 volts External Power is applied to the anode of D526 to reverse-bias it. Then, the current through R528, which normally flows through D526 and R525, is connected through D528 and R523 to establish a negative bias level at the base of Q514. By adding current through terminal 14, the desired external program horizontal position can be established. Notice that the front-panel POSITION control is not disconnected for External Mode operation. The external program position level operates as a vernier for the front-panel POSITION control.

Left Output Amplifier

Q534, Q543 and V544 are connected as a feedback amplifier for gain stabilization and linear output to the CRT deflection plates. The output signal at the plate of V544 is in phase with the negative-going signal applied to the base of Q534. Negative feedback is provided from the plate of V544 to the emitter of Q534 through R546 and C546. Diodes D531 and D532 connected between the emitter and collector of Q534 protect this transistor from excess input voltage. In addition, they improve the recovery time of Q534 when driven by a large signal, particularly for magnified operation at fast sweep rates. The negative-going deflection signal at the plate of V544 is connected to the left CRT deflection plate through terminal 17 of P21.

Right Output Amplifier

The Right Output Amplifier is basically the same as the Left Output Amplifier except that it produces an output signal 180° out of phase with the input signal. The negative-going signal at the collector of Q514 is connected to the base of Q553 through the compensated voltage divider C551-R551-R552. C551 provides high-frequency compensation for the Horizontal Amplifier. Q553, Q554, V564A and V564B are connected as a feedback amplifier. Negative feedback is provided from the cathode of V564B to the base of Q553 through R567 and C567. The input signal is inverted through Q553-Q554 but is not inverted through the remainder of the circuit to produce a positive-going output signal. This positive-going deflection signal is connected to the right CRT deflection plate through terminal 21 of P21

Readout Logic

General

The Readout Logic circuit determines the decade and multiplier readout on the front panel of the unit. For manual operation, the MANUAL TIME/DIV and DLY'D SWP MAG switches determine the logic to control the readout panel. For Seek or External Mode operation, the readout is controlled by the decade, multiplier and magnifier logic applied from the Counter Circuit and the Delayed Sweep Magnifier Control circuit. The decade logic and multiplier logic is distributed from this circuit to the Sweep Generator, Delay and Timing Circuit and the Horizontal Amplifier circuits. Fig. 3-18 shows a logic block diagram of the Readout Logic circuit. A diagram of this circuit is shown on diagram 5 at the rear of this manual.

Multiplier and Decade Readout

The Multiplier and Decade Readout stages provide the front-panel readout of the sweep rate. These stages are controlled by the Manual Readout Decoding stage for Manual Mode operation or the decade and multiplier logic from the Counter Circuit for Seek and External Mode Operation.

Manual Readout Decoding

The MANUAL TIME/DIV switch, SW450, and the DLY'D SWP MAG switch, SW940, determine the readout panel

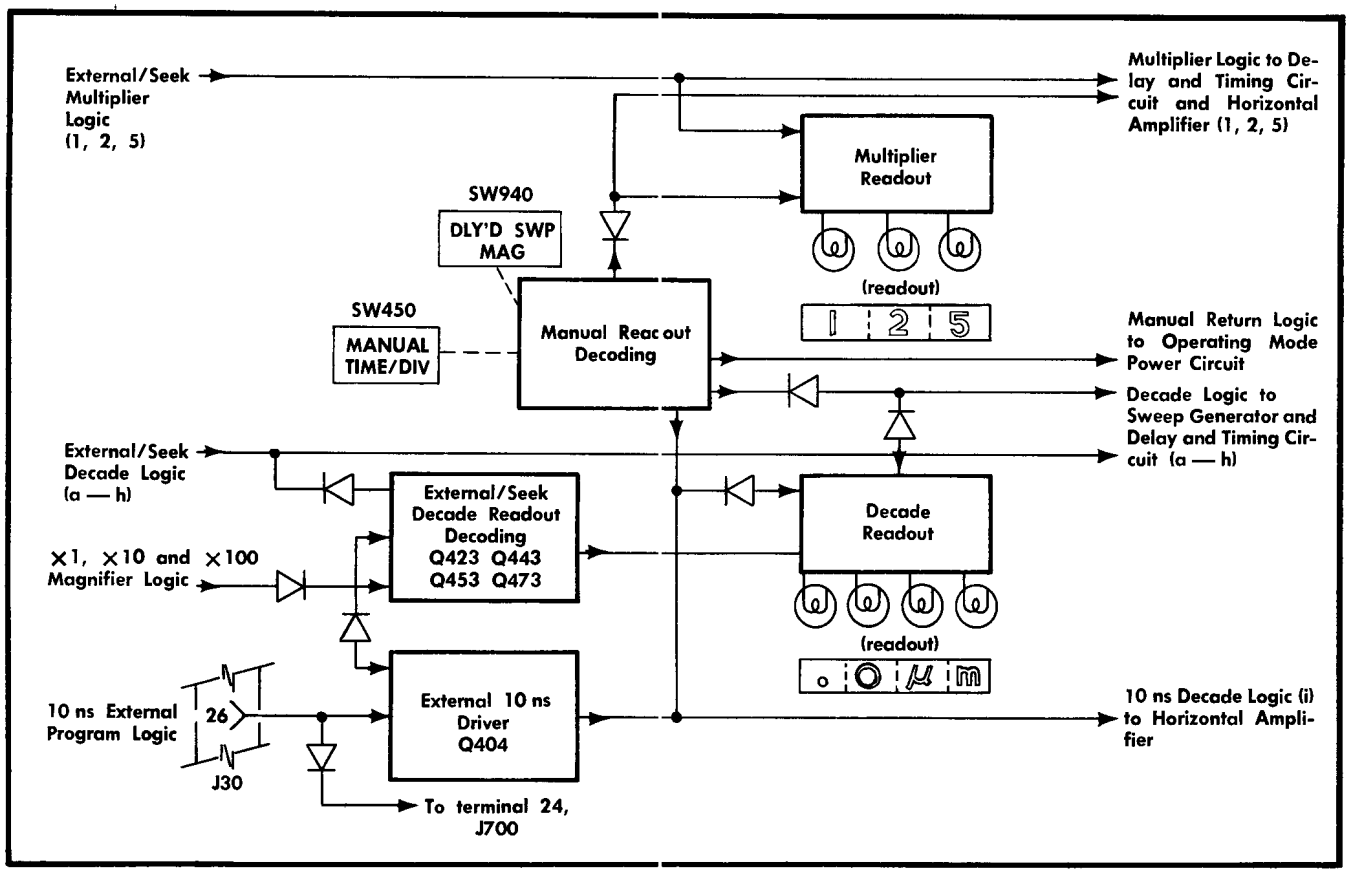


Fig. 3-18. Readout Logic block diagram.

indications for Manual Mode operation. The wiper contacts of these switches are connected to Manual Power through diodes. In the Manual Mode of operation, —12.2 volts Manual Power is applied and the diodes are forward biased. For Seek or External Mode operation, Manual Power is disconnected from the diodes and the setting of these switches does not affect operation of this circuit. Wafer 3F of SW450 determines the Manual Mode multiplier logic to the 1, 2, 5 readout bulbs. This logic is —12 volts for the desired multiplier. The Manual Mode multiplier logic sequence is 5-2-1 throughout the rotation of the switch. This wafer also provides the Manual Mode multiplier logic to the Sweep Generator and the Delay and Timing Circuit.

Wafer 3R of SW450 provides the Manual Mode decade logic to the Sweep Generator and the Delay and Timing Circuit. A —12 volt level is connected to one of the 1 s - 0.1 μs (a-h) decade logic lines to select the timing decade. In the last three clockwise positions (10, 20 and 50 ns), D404 applies —12 volts to the 0.1 μs (h) logic line to hold this decade on. The 10 ns (i) logic level established in these positions turns on the "0", "m", "μ" readout through diodes D485, D486 and D487. The 10 ns logic is also connected to the Horizontal Amplifier circuit.

Wafers 1R, 2F and 2R provide the decade readout for the Manual Mode. Only one of these wafers is returned to —12.2 volts Manual Power through the DLY'D SWP MAG switch, SW940. These two switches in combination provide Manual Mode magnifier decoding. For example, when the MANUAL TIME/DIV switch is in the 5 s position and the DLY'D SWP MAG switch is set to ×1, there is no output from the decade readout. The 5 and s/DIV readouts are on as controlled by other circuits previously discussed. For ×10 delayed sweep magnification, the DLY'D SWP MAG switch applies —12 volts to wafer 2F. This logic level turns on the "." readout to indicate a magnified sweep rate of 0.5 seconds/division. In the ×100 position of SW940, Manual Power is applied to wafer 2R. The "0" and "m" readouts are turned on through diodes D491 and D492 to indicate a magnified sweep rate of 50 milliseconds/division.

Wafer 1F provides manual-return logic to the Operating Mode Power circuit. As the MANUAL TIME/DIV switch position is changed, this wafer opens the ground return to the Seek Mode Control stage and the unit returns to Manual Mode operation (see Operating Mode Power for more information).

External/Seek Decade Readout Decoding

Decade logic from the Counter Circuit and ×1, ×10 and ×100 magnifier logic from the Delayed Sweep Magnifier Control circuit are applied to the External/Seek Decade Readout Decoding stage to determine the decade readout in the Seek and External Modes of operation. The decade logic level applied is —12 volts for the decade logic line that is on and zero volts for the remaining lines. Magnifier Logic Level is —12 volts[3] for the delayed sweep magnifica-

[3]The magnifier logic level may be as low as —5.5 volts or, on the ×100 logic line (×100 magnifier logic) it may drop to zero under certain conditions; see Delayed Sweep Magnifier Control circuit discussion for explanation. However, these differing levels do not affect operation.

tion desired and zero volts for the other two lines. These logic levels are connected through the diode matrix to control the readout driver transistors, Q423-Q443-Q453-Q473. These transistors in turn control the ".", (Q423), "0" (Q443), "m" (Q453) and "μ" (Q473) readouts on the front panel.

Figs. 3-19, 3-20 and 3-21 show current flow and diode conditions in the diode matrix and driver transistors to illustrate the operation of this circuit. For convenience in explaining this circuit, only part of the diagram is reproduced in these figures. Also, conditions are explained with only one basic sweep decade (one millisecond decade) with the changes in circuit conditions shown for ×1, ×10 and ×100 delayed sweep magnification of this basic sweep rate. Condition of components not essential to this explanation is omitted.

Fig. 3-19 shows circuit conditions for ×1 sweep magnification at sweep rates of 1, 2 and 5 milliseconds/division. The 1 ms (d) decade logic line is at —12 volts and the remaining decade logic lines are at zero volts. The ×1 logic line is at about —7 volts and the ×10 and ×100 magnifier logic lines are at zero volts. The decade logic level to the "." readout driver, Q423, is shunted by the zero volt ×10 magnifier logic at the anode of D421. D422 is reverse biased and the "." readout remains off. The decade logic level connected to the "0" readout driver, Q443, is shunted by the zero-volt ×100 magnifier logic at the anode of D431. D432 is reverse biased and the "0" readout remains off. The decade logic level connected to the base circuit of the "μ" readout driver, Q473, is shunted by the zero-volt ×100 magnifier logic at the anode of D471 and the "μ" readout remains off. The decade logic is also connected to the base circuit of the "m" readout driver through both R463 and R466. The current through R463 is shunted by the ×10 magnifier logic through D463. However, the decade logic is applied to the base of Q453 through D467 because the —7 volts ×1 magnifier logic reverse biases shunt diode D466. The base of Q453 drops to about —6 volts and it is forward biased. Current passes through B997 and the "m" readout comes on. This logic combination provides a readout of ____ms/DIV, with the multiplier provided by the Multiplier Readout stage.

Circuit conditions for ×10 delayed sweep magnification of the same basic sweep rate described above are shown in Fig. 3-20. The 1 ms decade logic is still —12 volts. However, the ×10 magnifier logic line is at —12 volts and the ×1 and ×100 lines are at zero volts. The decade logic applied to the base circuit of the "." readout driver is allowed to pass to the base of Q423 because the shunt diode D421 is held reverse biased by the —12-volt ×10 magnifier logic level. Current passes through B991 and the "." readout comes on. The decade logic to the "0" readout driver, Q443, is shunted by D431. Decade logic to the "m" readout driver, Q453, biases this transistor on since the shunt diode D463 is reverse biased by the —12-volt ×10 magnifier logic level. Current through the parallel path to Q453 is shunted through D466 to the ×1 magnifier logic line. The "μ" readout driver, Q473, remains off because the decade logic current is shunted by D471. This logic combination provides a readout of .____ms/DIV, with the multiplier provided by the Multiplier Readout stage.

×100 delayed sweep magnification of the basic 1, 2 or 5 millisecond sweep rate is shown in Fig. 3-21. Decade logic to the 1 ms logic line remains at —12 volts. Magnifier logic to the ×100 magnifier logic line is now —12 volts and zero volts to the ×1 and ×10 lines. Decade logic to the base of Q423 is shunted to the ×10 magnifier logic line by D421. The —12 volt level on the anode of D431 holds it reverse biased and allows the decade logic level to turn Q443 on. Current flows through B995 and the "0" readout comes on. Decade logic to the "m" readout driver is shunted because the ×1 magnifier logic level forward biases D466 and the ×10 magnifier logic level forward biases D463. D471 is held reverse biased by the —12-volt ×100 magnifier logic and the decade logic biases Q473 on. Current flows through B998 and the "μ" readout comes on. This logic combination provides a readout of ____0 μs/DIV, with the multiplier provided by the Multiplier Readout stage.

"1" multiplier and 0.1 μs decade (h) logic levels are connected to the Seek Circuit to lock out the Seek circuit when the 0.1 microsecond sweep rate is reached (see Advance Gate discussion). In the Seek Mode of operation, the 0.1 microsecond position is the only sweep rate when both of these logic levels are —12 volts.

External 10 Nanosecond Driver

To select the 10 ns decade (i) for External Mode operation, zero-volts external program logic is applied to terminal 26 of J30. The base of Q404 rises positive enough to bias it on and its collector goes negative to about —12 volts. This places —12 volts on the 10 ns decade logic line and the "0", "m", "μ" readouts are turned on through diodes D485, D486 and D487. D403 couples the 10 ns external program logic to pin 24 of J700 to turn on the 0.1 μs timing decade (h) to provide the correct sweep rate. The 10 ns logic level is also connected to the Horizontal Amplifier circuit.

In addition to turning on Q404 and the 0.1 μs timing decade, the 10 ns external program logic at terminal 26 of J30 locks out the "." readout driver, Q423, through D447 and the "μ" readout driver, Q473, through D470 to prevent parallel currents to the readout bulbs.

Seek Circuit

General

The Seek Circuit initiates the automatic time-base and trigger seeking functions of the Type 3B5 upon receipt of a seek command. This circuit provides reset and advance pulses to the Counter Circuit to automatically select sweep rate and, in conjunction with the Trigger Circuit, select auto triggering if the front-panel Trigger controls are incorrectly set or a trigger signal is not applied. Fig. 3-22 shows a logic block diagram of the Seek Circuit. A diagram of this circuit is shown on diagram 6 at the rear of this manual. Fig. 3-23 shows operating waveforms from the Seek Circuit to aid in this explanation.

Seek Input Circuit

The seek command to actuate this circuit can come from one of three sources: 1) front-panel SEEK button, SW604; 2) remote seek through terminal 12 of the front-panel PROGGRAM connector, J30; 3) remote seek through the amplifier unit from a remote-seeking probe or the amplifier unit program connector. The remote seek command from the amplifier

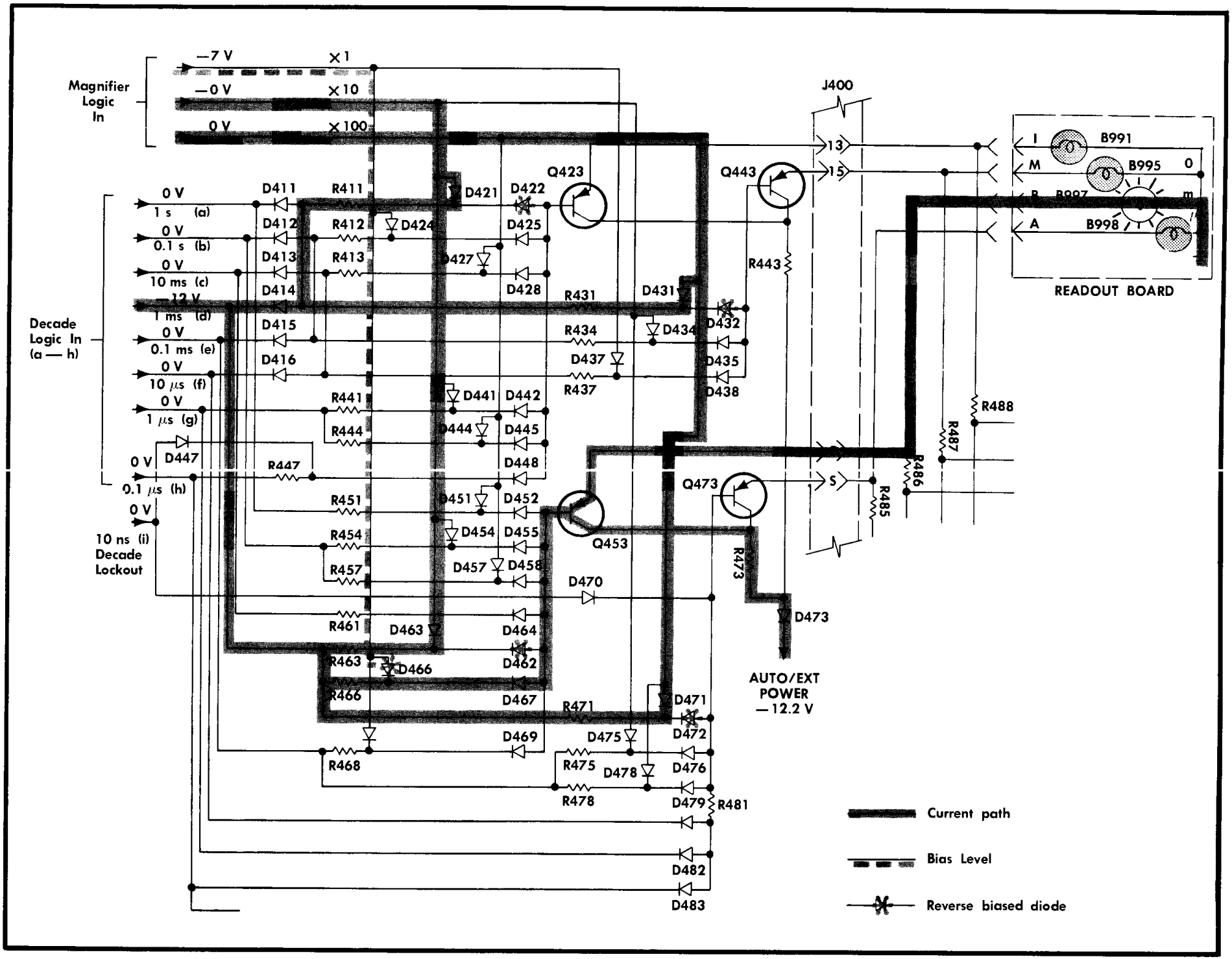


Fig. 3-19. Decade readout current for 1, 2 and 5 millisecond sweep rates (×1 sweep magnification).

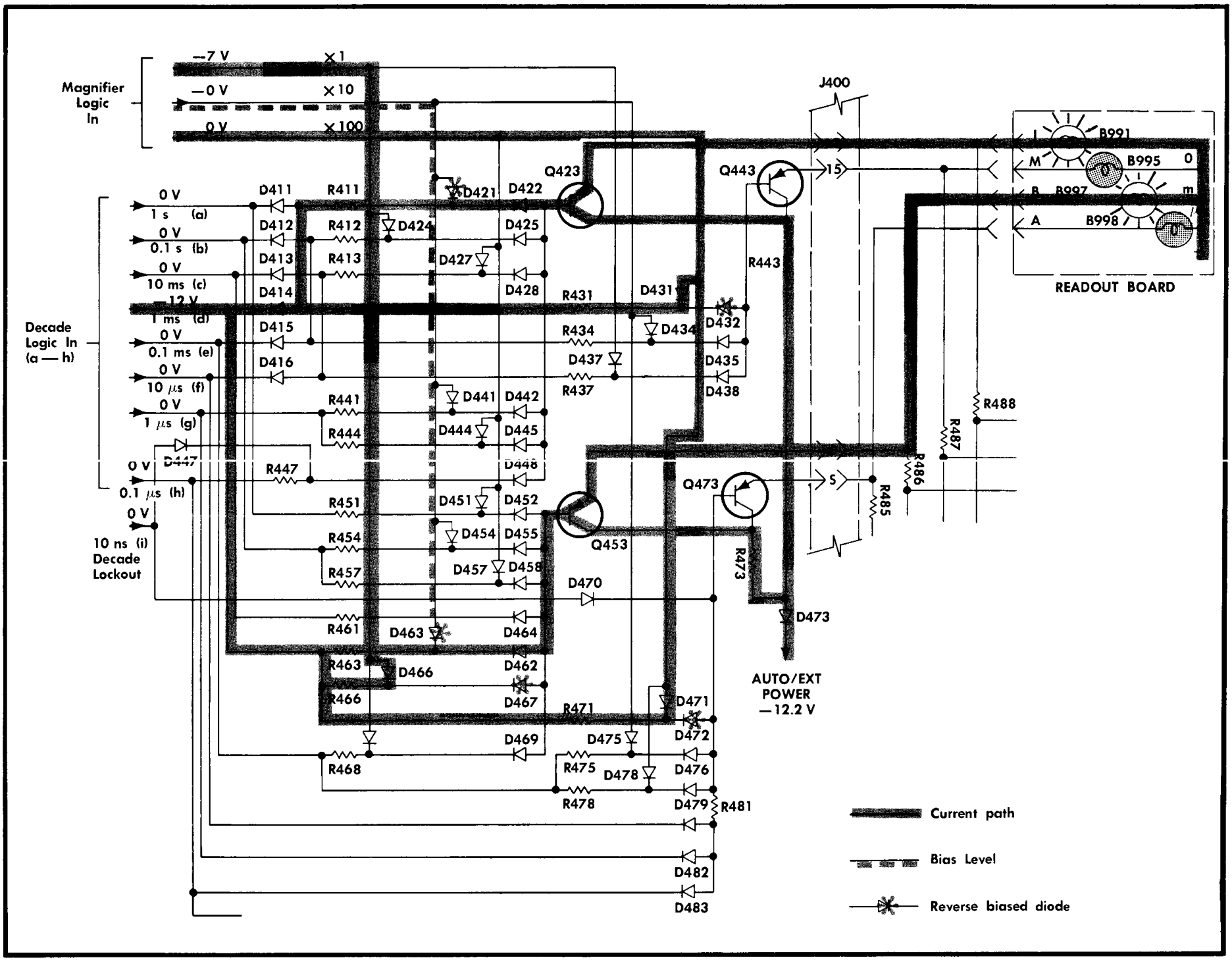


Fig. 3-20. Decade readout current for 0.1, 0.2 and 0.5 millisecond magnified sweep rates (×10 delayed sweep magnification).

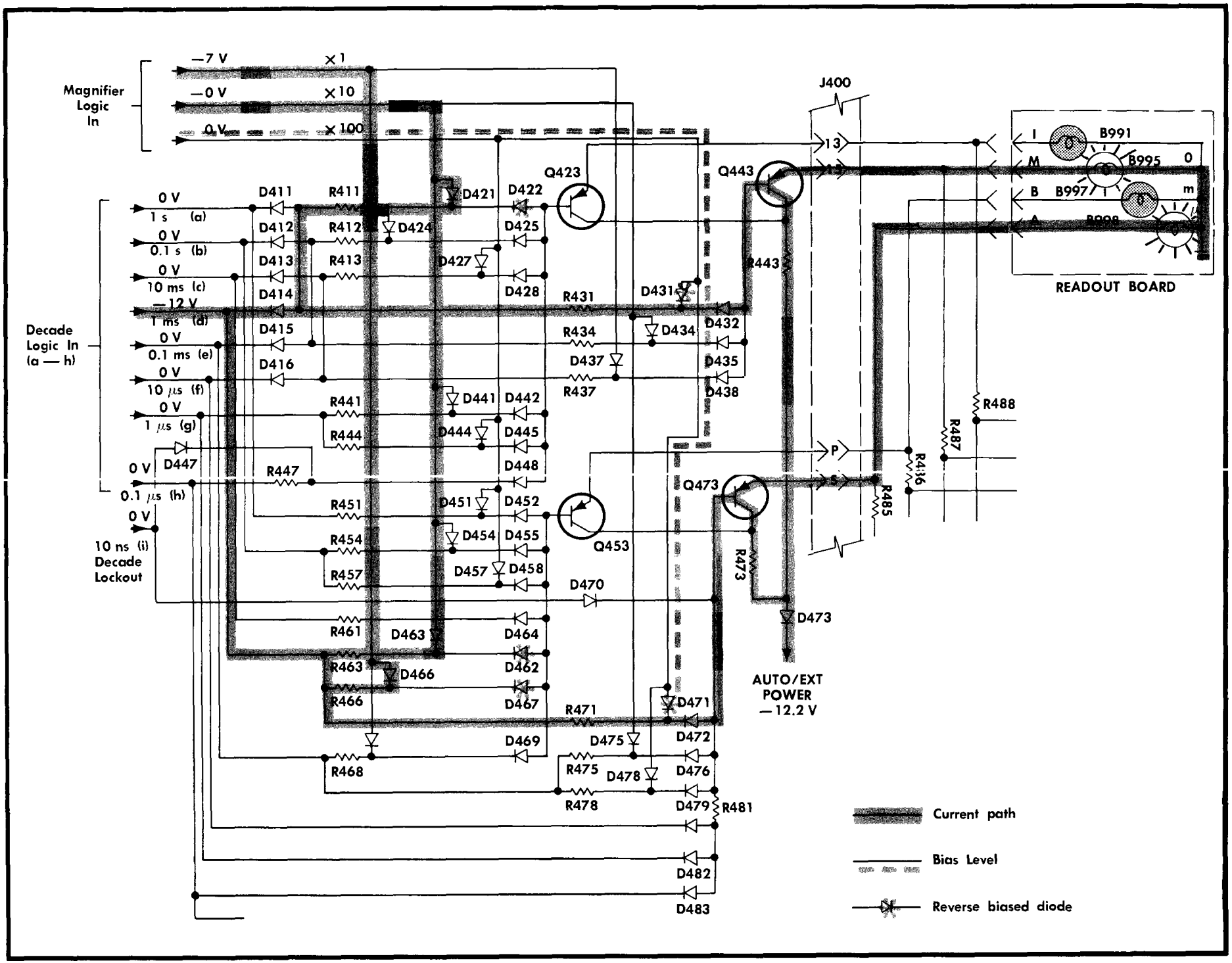


Fig. 3-21. Decade readout current for 10, 20 and 50 microsecond magnified sweep rates (×100 delayed sweep magnification).

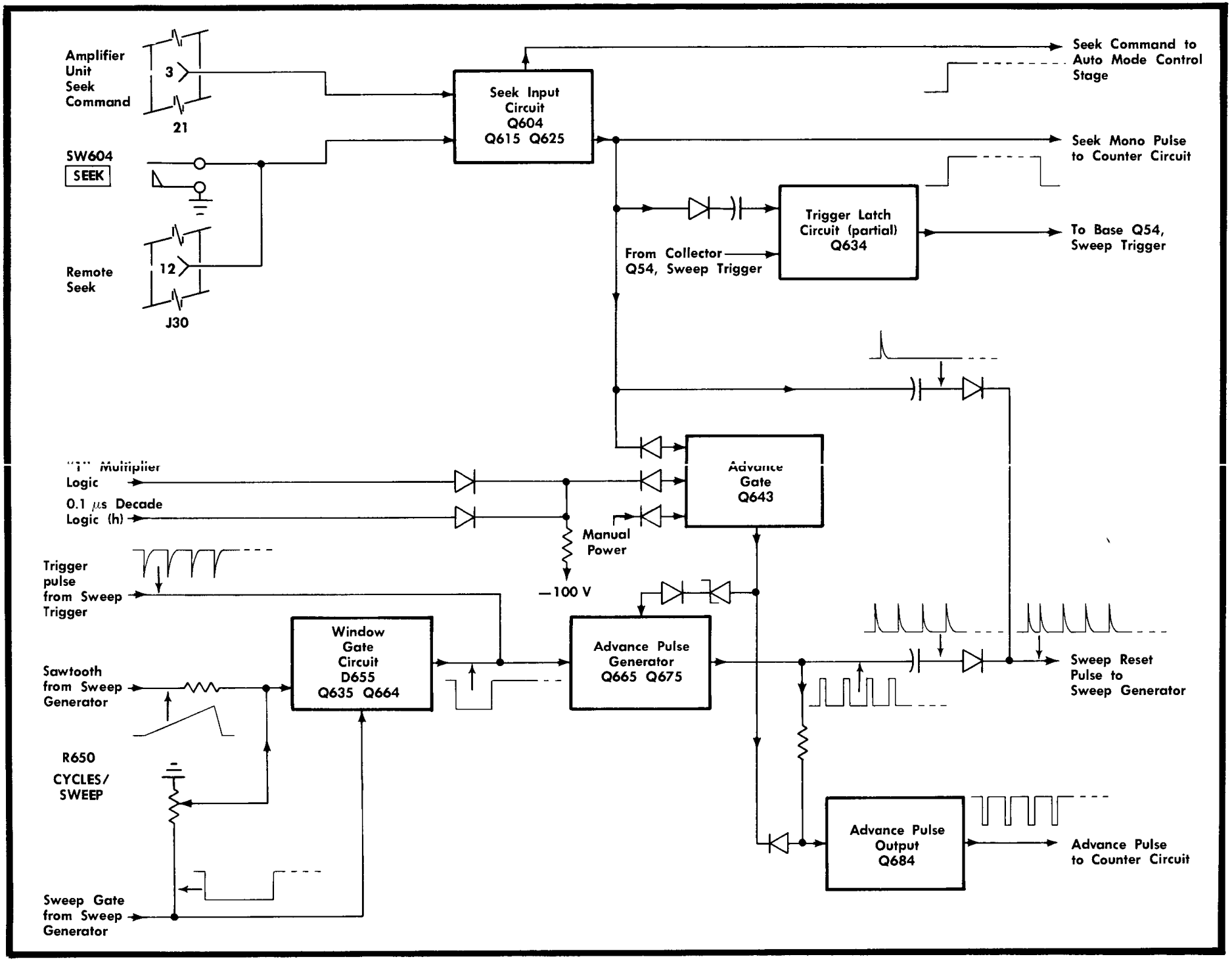
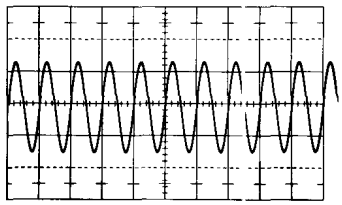
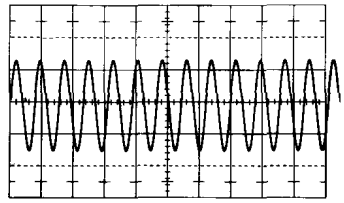
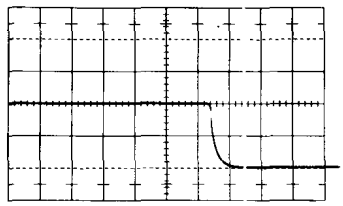
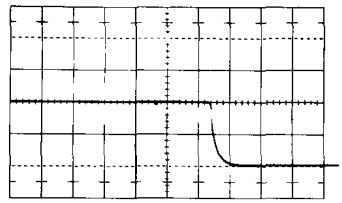
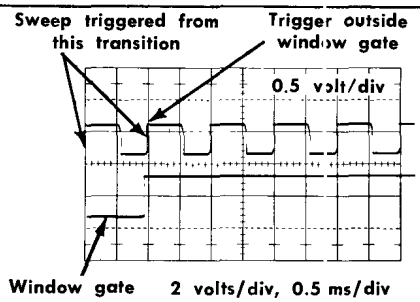
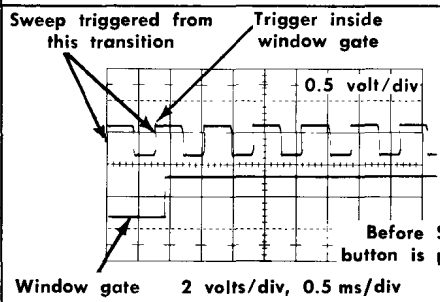
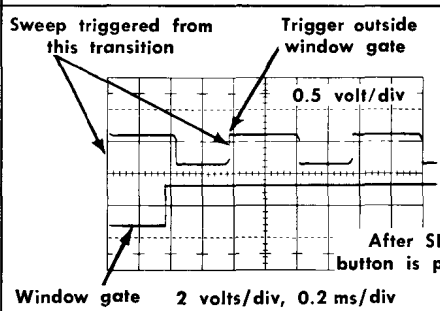
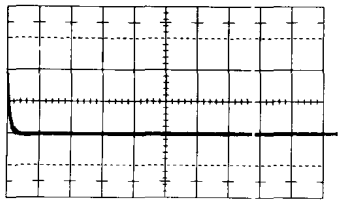
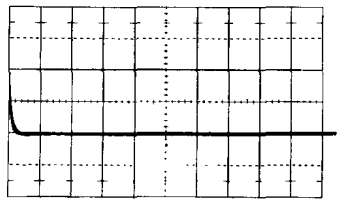
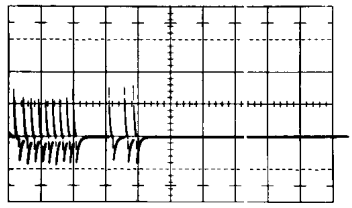
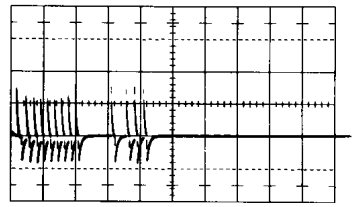
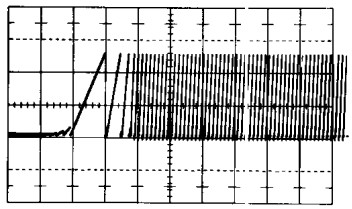
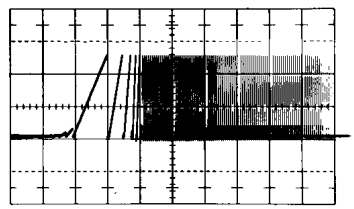
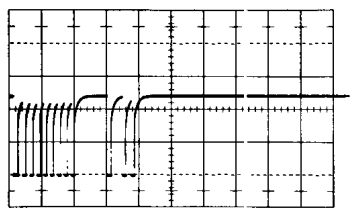
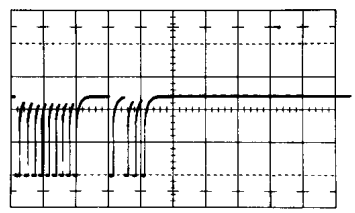
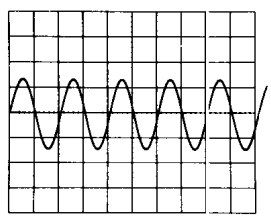
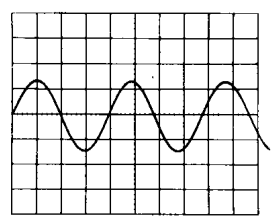


Fig. 3-22. Seek Circuit Logic block diagram

SEEK CIRCUIT OPERATION

Waveform Source	1 kHz sine-wave signal applied, 3B5 seeks to 0.5 ms/DIV (CYCLES/SWEEP adjustment set according to Calibration procedure).	1.3 kHz sine-wave signal applied, 3B5 seeks to 0.2 ms/DIV (CYCLES/SWEEP adjustment set according to Calibration procedure).
Input Signal.	 2 volts/div, 1 ms/div	 2 volts/div, 1 ms/div
Seek mono pulse at pin 8 of J400.	 5 volts/div, 0.2 s/div	 5 volts/div, 0.2 s/div
Trigger pulse (at junction of D105 and D115) and window-gate (at TP664) coincidence shown on dual-trace display.	 2 volts/div, 0.5 ms/div	 2 volts/div, 0.5 ms/div
		 2 volts/div, 0.2 ms/div
Sweep reset pulse at anode of D629.	 5 volts/div, 50 ms/div	 5 volts/div, 50 ms/div

Seek Circuit Operation (cont)

Sweep reset pulse at anode of D681[1].	 5 volts/div, 50 ms/div	 5 volts/div, 50 ms/div
Sawtooth sweep signal at TP500[1].	 20 volts/div, 50 ms/div	 20 volts/div, 50 ms/div
Advance pulses at pin 11 of J400[1].	 5 volts/div, 50 ms/div	 5 volts/div, 50 ms/div
Resultant CRT display.	 2 volts/div, 0.5 ms/div	 2 volts/div, 0.2 ms/div

[1]Repetition rate of these waveforms is a function of sweep range, CYCLES/SWEEP adjustment and holdoff time.

Fig. 3-23. Seek Circuit waveforms showing circuit operation when SEEK button is pressed. External triggering was used to indicate overall time relationship.

unit is connected to this unit through terminal 3 of the interconnecting plug and the interconnecting cables in the indicator oscilloscope. The network D601-D602-R601-R602-R603-C602-C603-C604 eliminates all signals at the base of Q604 except the seek command to prevent a false seek command to the Seek Circuit. A remote seek command from the amplifier unit turns on Q604 and its collector rises positive to about zero volts. Likewise, the front-panel seek command or the remote seek command through J30 raises the circuit potential to zero volts. The seek command may either be momentary or it may be a continuous seek command. The seek command is connected to the base of Q615 to produce the seek mono pulse and to the Operating Mode Power circuit through D605 (see Seek Mode Control discussion) to switch the instrument to the Seek Mode of operation.

Q615 and Q625 are connected as an AC-coupled multivibrator. Quiescently, Q615 is held on by the negative potential at its base established by the —12.2 volt level at the collector of Q604 (no seek command applied). The base of Q625 is clamped at about +0.5 volts by D619 and Q625 is held off. When a seek command is received, the base of Q615 rises positive and it turns off. Its collector goes negative toward —100 volts and is clamped when it reaches about —12 volts by D614. C616 begins to charge and this charge current flows through R616 to pull the base of Q625 negative and turn it on. The collector of Q625 rises positive to produce the seek mono pulse. This pulse is connected to the Counter Circuit, Trigger Latch Circuit and the Advance Gate stage. It also provides a sweep reset pulse to the Sweep Generator circuit through C629 and D629.

The circuit remains in this condition until C616 is fully charged. Then, the current through R616 returns to its quiescent level and Q625 is turned off again. Its collector goes negative to about —8 volts to end the seek mono pulse. This negative change is coupled back to the base of Q615 through R626-R627-C627. If the seek command has ended, this feedback has no effect on circuit operation. However, if a seek command still holds the base of Q615 near zero volts, this feedback pulls the base of Q615 negative enough to turn it on again and produce another seek mono pulse. As long as a seek command is applied, Q615 and Q625 act as a free-running multivibrator.

Trigger Latch Circuit

Q634 operates in conjunction with Q54 in the Trigger Circuit to provide auto triggering if the front-panel controls are incorrectly set or a trigger signal is not applied (Seek Mode operation only). Full operation of this circuit is explained under Trigger Latch Circuit in the Sweep Trigger discussion

Advance Gate

The Advance Gate stage produces an output level which either locks out or enables the Advance Pulse Generator and the Advance Pulse Output stage. For Manual Mode operation, the Advance Gate output level is held at —12 volts by Manual Power applied to the base of Q643 through D644. This holds both Q665 and Q684 reverse biased to lock out any advance pulses. In the Seek Mode of operation, the output level from the Advance Gate depends upon the input levels. D640 and D641 comprise an "and" gate for the "1" multiplier and 0.1 μs decade (h) logic levels. When both of these logic levels are —12 volts, the base of the Advance Gate stage goes negative and succeeding advance pulses are locked out. This condition is met only in the 0.1 microsecond sweep rate when the "1" logic connected to D640 and the 0.1 μs logic connected to D641 are both at —12 volts. Current then flows through R641, D642 and R643 and the base of Q643 goes negative. This lock-out action prevents the Counter Circuit from returning to the 5 s sweep rate on fast signals.

When a seek mono pulse is received at the base of Q643, its emitter rises positive to about zero volts. The duration of the output pulse at the collector is the same as the duration of the seek mono pulse at the base unless the 0.1 microsecond sweep rate is reached. This positive output level enables the Advance Pulse Generator and the Advance Pulse Output stages to allow advance and sweep reset pulses to be produced.

Window Gate and Advance Pulse Generator

The Window Gate circuit turns on the Advance Pulse Generator circuit to produce advance pulses for the Counter Circuit. When an Advance Gate enable pulse is applied to the emitter of Q665 through D666 and D665 (only in Seek Mode with seek command applied), its emitter level rises to about —2.5 volts as set by D668 and zener diode D669. Therefore, the base of Q665 must go below about —3.0 volts before Q665 can be biased on. Trigger pulses from the Seek Circuit Driver stage in the Sweep Trigger circuit are connected to the base of Q665 through T660 and D661. However, these negative-going trigger pulses are only about 1.5 volts in amplitude so they do not turn Q665 on. An additional negative level must be provided by the collector level of Q664 to turn Q665 on. The time duration of this negative window-gate signal from Q664 is controlled by the CYCLES/SWEEP adjustment, R650, to determine the number of cycles in the CRT display.

Circuit operation is as follows: the sawtooth produced by the Sweep Generator circuit is connected to the base of Q653 through R186. The bias level of Q653 is set by the sweep gate connected to the base through R650 and R651 (only during a sweep). This bias level can be adjusted by the CYCLES/SWEEP adjustment, R650; the setting of R650 determines the amount that the sawtooth must run up before it turns Q653 on. At the start of the sweep, both Q653 and Q664 are biased off. The sweep gate signal also provides the collector supply for Q664. Since Q664 is biased off at the start of the sweep, its collector goes negative toward —6 volts and is clamped at about —2.5 volts by divider R657-R658 and D657. This collector level allows the trigger pulses to turn on Q665. However, when the sawtooth overcomes the bias level at the base of Q653 as set by R650, Q653 turns on and its collector goes negative. D655 switches to its high-voltage state and Q664 turns on very rapidly. The collector of Q664 rises to about zero volts to end the window-gate signal. This locks out any further trigger pulses at the base of Q665.

At the start of each seek cycle, the sweep rate is reset to 5 seconds/division by the seek mono pulse to the Counter Circuit and the sweep is reset to the left side of the graticule by the sweep reset pulse produced by the Advance Pulse Generator stage. The sawtooth at the base of Q653 starts

to run up at this sweep rate. The Advance Pulse Generator is not turned on by the trigger pulse which starts the sweep, due to normal delay time designed into this circuit. However, if the next trigger pulse is applied to Q665 before the sawtooth turns the Window Gate circuit on (i.e., collector of Q664 still negative), the Advance Pulse Generator, Q665 and Q675, is turned on. When Q665 turns on, its collector rises positive to bias Q675 on. The resulting negative-going change at the collector of Q675 holds Q665 in conduction through C671-R671 until the charge on C671 equalizes. When C671 is charged, the base of Q665 rises positive and it turns off. The signal at the collector of Q665 provides the advance pulse to the Advance Pulse Output stage. It also provides a sweep reset pulse to the Sweep Generator circuit through C681-D681 so the sweep restarts with each advance pulse. Each time a trigger signal produces an advance pulse during the window-gate signal (before the sawtooth biases Q653 on), the sawtoooth starts to run up again at the next faster sweep rate (advance pulse increases sweep rate; see Counter Circuit discussion). This action continues each time Q665 is triggered until the sweep rate is fast enough to turn Q653 on (to end window-gate signal) before a trigger can produce an advance pulse.

The amount that the sawtooth must run up before it turns Q653 on is set by the CYCLES/SWEEP adjustment. Since voltage level on the sawtooth is related to divisions on the CRT, the setting of this control determines the number of cycles in the CRT display. For example, assume a constant input signal produces a three-cycle display in the Seek Mode when R650 is set to midrange. Then, when R650 is set clockwise, the base of Q653 is less negative and the sawtooth must overcome less of the sweep gate current to turn Q653 on. Therefore, fewer advance pulses are produced before the sweep rate is advanced enough so that Q653 turns on before Q655 can be triggered. With fewer advance pulses to the Counter Circuit, a slower sweep rate is produced to display more cycles of the signal. On the other hand, if the CYCLES/SWEEP adjustment is set counterclockwise, the sawtooth must overcome more sweep-gate current and run up farther to turn Q653 on. More advance pulses are produced before the sawtooth reaches the level where it turns Q653 on before Q665 can be triggered. More advance pulses to the Counter Circuit produce a faster sweep rate which results in less cycles in the display.

Advance Pulse Output

Q684 provides amplification for the advance pulses produced by the Advance Pulse Generator stage and couples them to the Counter Circuit. This stage only produces an output when enabled by the Advance Gate stage through D682. Locking this stage out in addition to locking out the Advance Pulse Generator circuit insures that all advance pulses are locked out after the 0.1 microsecond sweep rate has been reached. It also prevents the Counter Circuit from being advanced by noise or other extraneous pulses in the Seek Circuit when a seek command is not present.

Fig. 3-23 shows operating waveforms from the Seek Circuit. The first set of waveforms shows circuit conditions with a 1-kHz sine wave applied (CYCLES/SWEEP adjustment set according to Calibration Procedure). The second set of waveforms shows circuit conditions with a 1.3 kHz sine-wave signal.

Counter Circuit

General

The Counter Circuit produces the multiplier and decade logic levels for the Seek and External modes of operation. In the Seek Mode, the output of this circuit is controlled by the seek mono pulse and advance pulses produced by the Seek Circuit. For external Mode operation, the output of this circuit is controlled by external program logic levels applied through the front-panel PROGRAM connector. Fig. 3-24 shows a logic block diagram of the Counter Circuit. A diagram of this circuit is shown on diagram 7 at the rear of this manual.

Multiplier Counter

The three-state Multiplier Counter produces the 1-2-5 logic to select the sweep-rate multiplier within the timing decade selected by the Decade Counter stage. Fig. 3-25 shows circuit conditions for "5" output. The positive-going seek mono pulse from the Seek Circuit turns on Q705 at the start of each seek cycle through C731, D731 and R731. The collector level of Q705 is coupled to Q715 and Q725 through D713 and D723 to hold them off. The first advance pulse produced by the Seek Circuit is coupled to the base of Q705 through C704 and D704. Q705 turns off and its collector rises positive. This level change turns Q715 on through C709.

Fig. 3-26 shows circuit conditions for "2" multiplier output. Q715 turns on when Q705 is turned off by the advance pulse. Then, the collector level of Q715 holds Q705 and Q725 off through D703 and D723. The second advance pulse produced by the Seek Circuit is coupled to the base of Q715 through C714 and D714. This negative-going pulse turns Q715 off and its collector rises positive. C719 couples this change to the base of Q725 to turn it on.

"1" multiplier logic is produced by Q725 as shown in Fig. 3-27. Q725 is turned on by Q715. As it turns on, the collector level of Q725 goes negative to hold Q705 and Q715 off through D702 and D712. The third advance pulse produced by the Seek Circuit is connected to the base of Q725 through C724 and D724. Q725 turns off and its collector rises positive. This positive level change turns Q705 back on through C729. As Q705 comes back on, the negative-going change at its collector produces an advance command level to the Enable Multivibrator stage. The action described starts over and repeats until the Seek Circuit stops producing advance pulses. One advance command to the Enable Multivibrator is produced for each three advance pulses produced by the Seek Circuit.

For External Mode operation grounding (zero-volt) external multiplier program logic is applied to the Multiplier Counter circuit through either terminal 2, 3 or 5 of J30. This external program logic biases on the associated transistor to produce the desired multiplier logic output. The transistor which is turned on by the external program logic holds the other transistors off and this transistor remains on until the external program logic is removed.

For Manual Mode operation, —12.2-volt Seek/External Power to the Counter Circuit is disconnected. This enables the entire circuit in this mode and the output levels of this circuit rise to about zero volts.

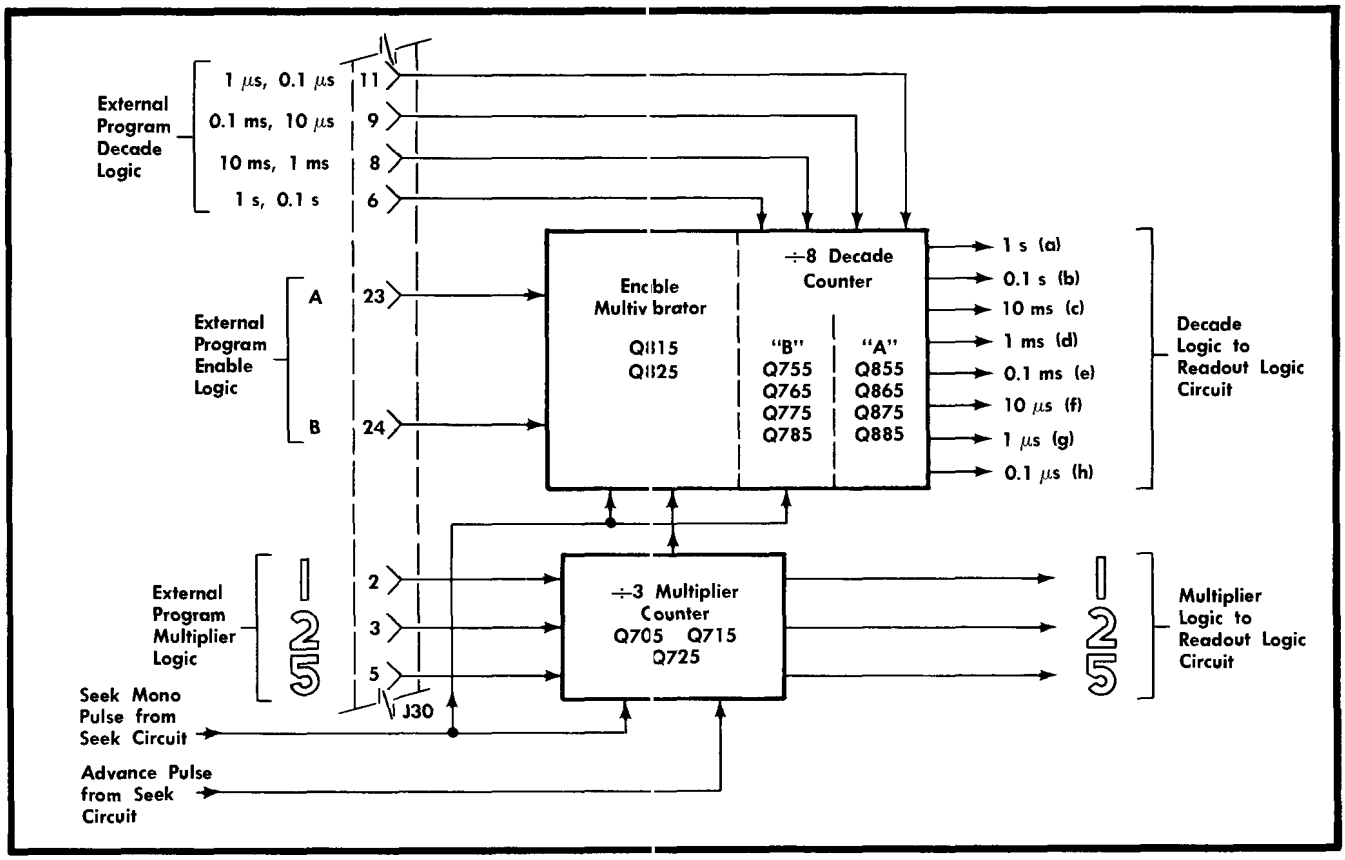


Fig. 3-24. Counter Circuit Logic block diagram.

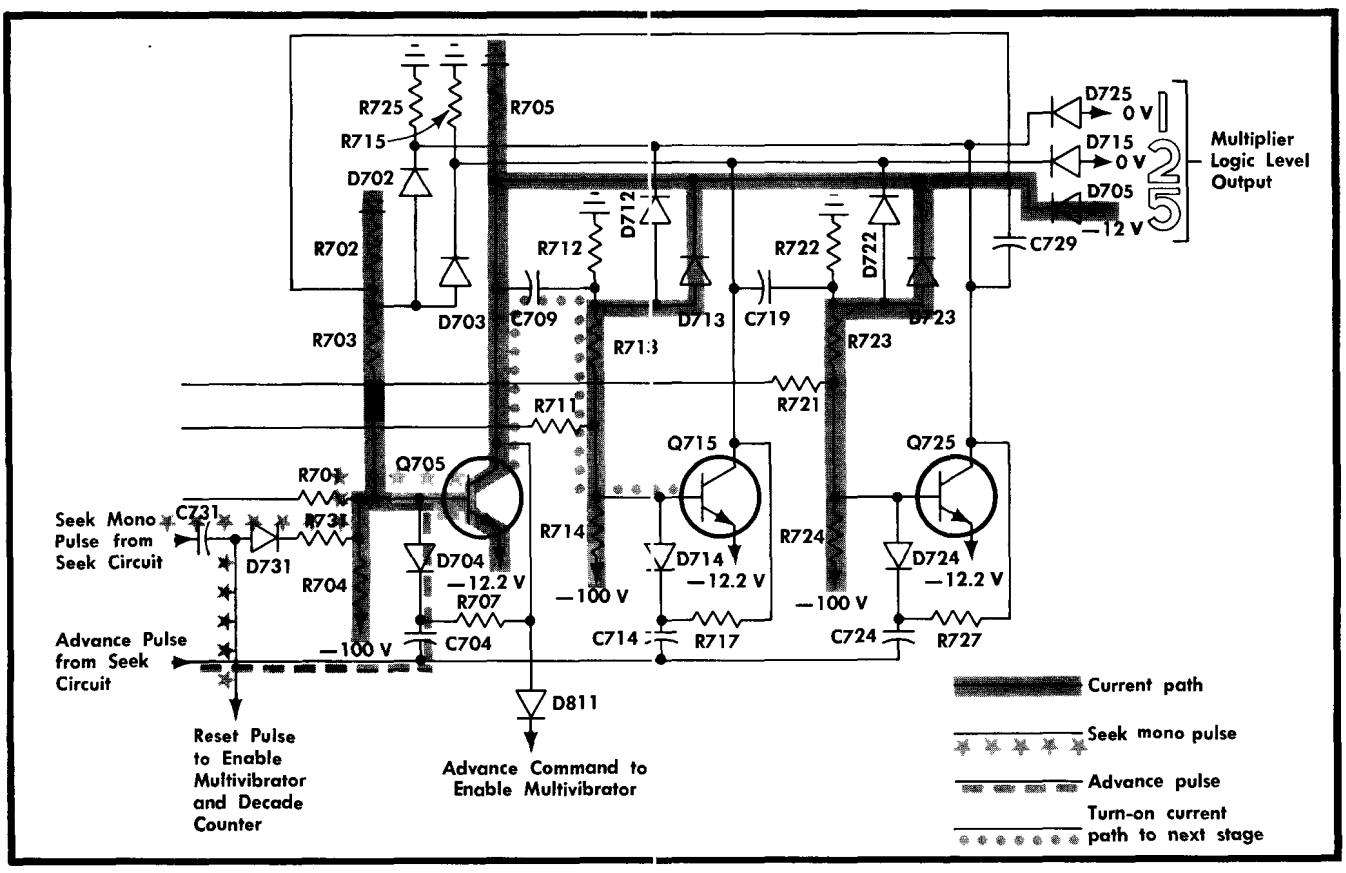


Fig. 3-25. Multiplier Counter circuit conditions for "5" output.

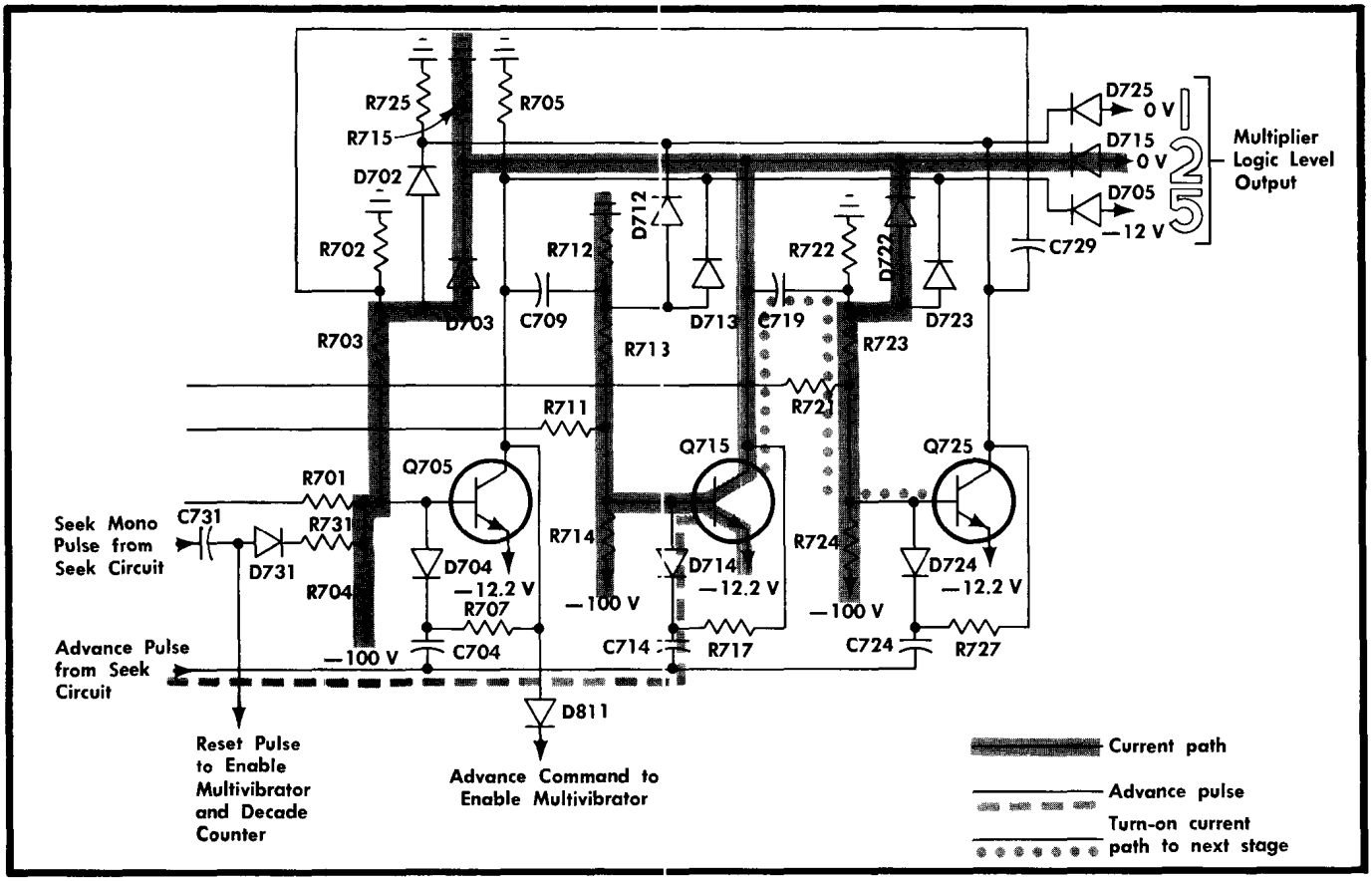


Fig. 3-26. Multiplier Counter circuit conditions for "2" output.

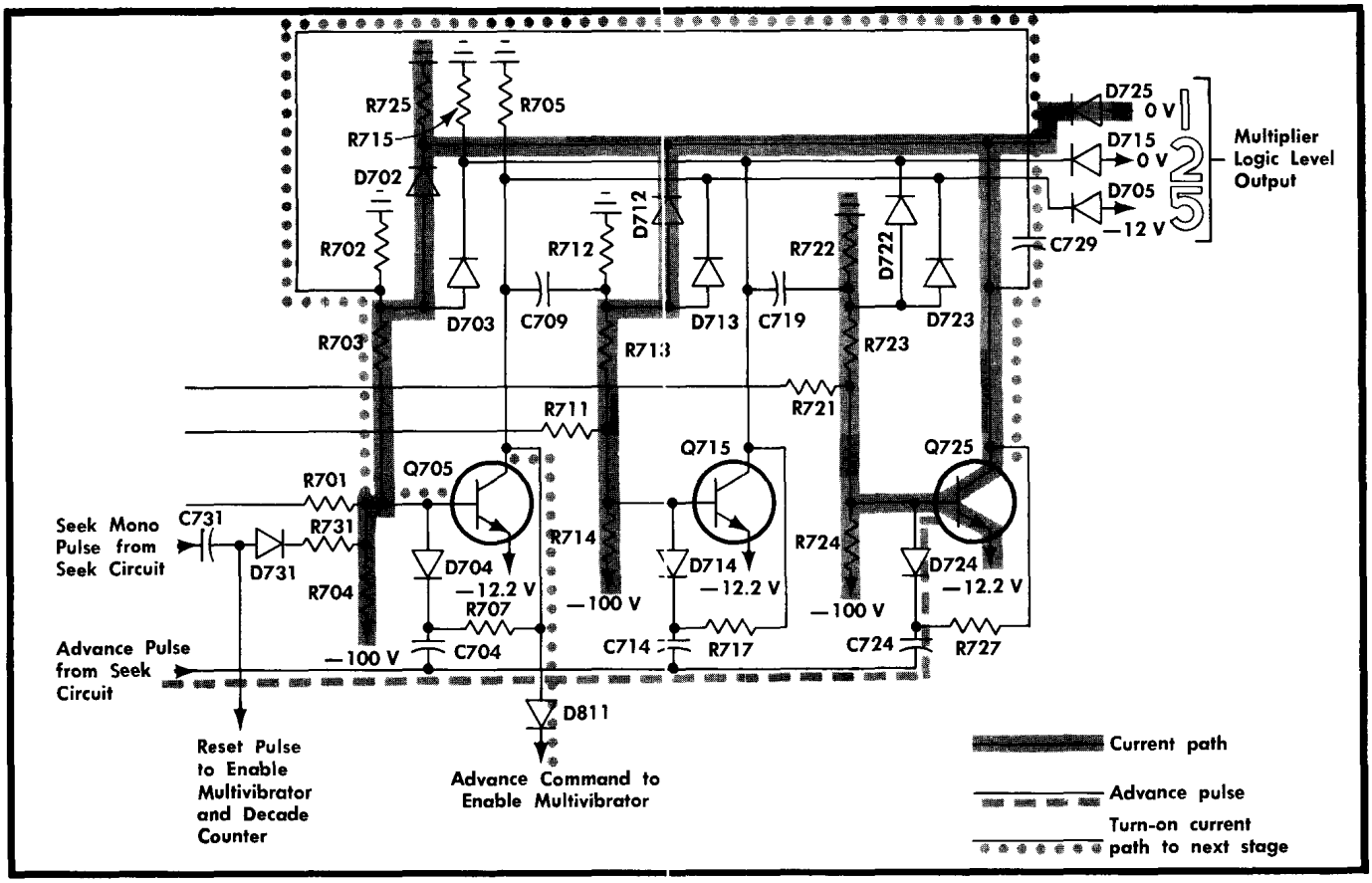


Fig. 3-27. Multiplier Counter circuit conditions for "1" output.

Enable Multivibrator

For Seek Mode operation, Q815 and Q825 are coupled as a bistable multivibrator. The multivibrator switches each time an advance command is received from the Multiplier Counter stage. The collector level of Q815 and Q825 determines which group of transistors in the Decade Counter can conduct. At the start of the seek cycle, the seek mono pulse from the Seek Circuit turns Q815 on through D818 and R818. The collector of Q815 goes negative and the base level of transistors Q755, Q765, Q775 and Q785 (B group) is pulled negative to hold them off. The collector of Q825 rises positive and Q855, Q865, Q875 and Q885 (A group) are enabled. Only one of the transistors in the A group conducts, however (see Decade Counter discussion).

The third advance pulse from the Seek Circuit produces an advance command to the Enable Multivibrator through D811. This advance command turns off the on transistor. For example, the first advance command (third advance pulse) after the circuit has been reset is connected to the base of Q815 through C812 and D814. Q815 turns off and Q825 comes on. Now the B group transistors are enabled and the A group is locked out. With the sixth advance pulse to the Multiplier Counter circuit, the Enable Multivibrator returns to the original condition and the A group transistors are enabled. The Enable Multivibrator switches with each third advance pulse produced by the Seek Circuit.

For External Mode operation, either Q815 or Q825 is held on by the grounding external program enable logic applied through terminal 23 or 24 of J30. This holds the associated transistor on and locks out the corresponding group of Decade Counter transistors. For example, external program enable logic applied to terminal 23 (A logic line) holds Q815 on. The collector level of Q815 goes negative to lock out the B group transistors and allow the A group transistors to conduct.

Decade Counter

The Decade Counter is an eight-state (alternate four-four) ring counter which provides the decade logic levels in the Seek and External Modes of operation. The transistors in the Decade Counter are divided into two groups; Q755, Q765, Q775 and Q785 form group B and Q855, Q865, Q875 and Q885 form group A. Only one of these transistor groups can conduct at one time as enabled by the Enable Multivibrator. Furthermore, only one transistor within the enabled group conducts as determined by the ring-counter action.

The seek mono pulse from the Seek Circuit biases Q855 on. Also the Enable Multivibrator is reset as described previously to allow the A group transistors to conduct. When Q855 conducts, its collector level goes negative and it reverse biases transistors Q865, Q875 and Q885 through D862, D872 and D882. The 1 s decade (a) logic line drops to —12 volts to select the 1 s timing decade. The Decade Counter remains in this condition until the Enable Multivibrator is switched by the advance command from the Multiplier Counter (every third advance pulse from Seek Circuit). Then, the opposite group of transistors is enabled; in this example, the B group. As Q855 turns off, the positive-going level change at its collector is coupled to the base of Q755 through C856 and R753. The collector of Q755 goes negative to lock out the remaining transistors in the B group. The decade logic output on the 0.1 s decade (b) logic line (0.1 second timing decade) is —12 volts. This action continues each time an advance command switches the Enable Multivibrator. As the on transistor is switched off by the Enable Multivibrator, it turns on the next transistor in the opposite group. Decade logic from the output of the Decade Counter is connected to the Readout Logic circuit. The alternate four-four ring counter configuration just described is used to insure that the ring counter does not free run as sometimes occurs in conventional counters with this number of states.

For External Mode operation, external program decade logic connected to terminals 6, 8, 9 or 11 of J30 controls the Decade Counter. The grounding external program decade logic is connected to the bases of the corresponding transistors in both groups A and B. Only the transistor in the group which is enabled by the Enable Multivibrator conducts. For example, if the external program logic is connected to terminals 9 and 23 of J30 (0.1 ms or 10 ms decade logic and A enable logic) the external program decade logic is connected to both Q775 and Q875. However, the A external program enable logic connected to the Enable Multivibrator locks out the B group transistors so only Q875 can turn on. The decade logic output is on the 0.1 ms decade (e) logic line to select the 0.1 ms timing decade.

Operating Mode Power

General

The Operating Mode Power circuit provides Seek/Manual Power, Manual Power, Seek/External Power and External Power to the unit. The output power from this circuit is changed to control the operating mode. For example in the Seek Mode of operation, Seek/Manual and Seek/External Power output is available and in the External Mode of operation Seek/External and External Power output is available. Fig. 3-28 shows a logic block diagram of the Operating Mode Power circuit. A diagram of this circuit is shown on diagram 8 at the rear of this manual.

Manual Mode Control

In the Manual Mode of operation, Q915 determines the output of this circuit. Fig. 3-29 shows circuit conditions for Manual Mode operation. Q915 is forward biased by the level at its base established by divider R911-R912-R913. This level is more positive than the level at the base of Q905 so that Q915 comes on when the unit is first turned on to provide Manual Mode operation (except when programmed for External Mode). The collector current of Q915 flows through B915 and the MAN pushbutton lights up. This bulb drops about 6 volts of the —12-volt level at the collector of Q915 to provide current to the —6-volt line for the heater of V163. This current is supplied in parallel with the current from the s/DIV and UNCAL Readout Control stage. Current also flows through K915 and K915-1 is actuated to connect —12.2 volts to the Manual Power line. Seek/Manual Power output is provided through D919. The collector level of Q915 is connected to the Seek Mode Control stage through D901 to lock it off during Manual Mode operation

The Manual Mode of operation can be selected by pressing the MAN button or by changing the sweep rate with the MANUAL TIME/DIV switch. When the MAN button is

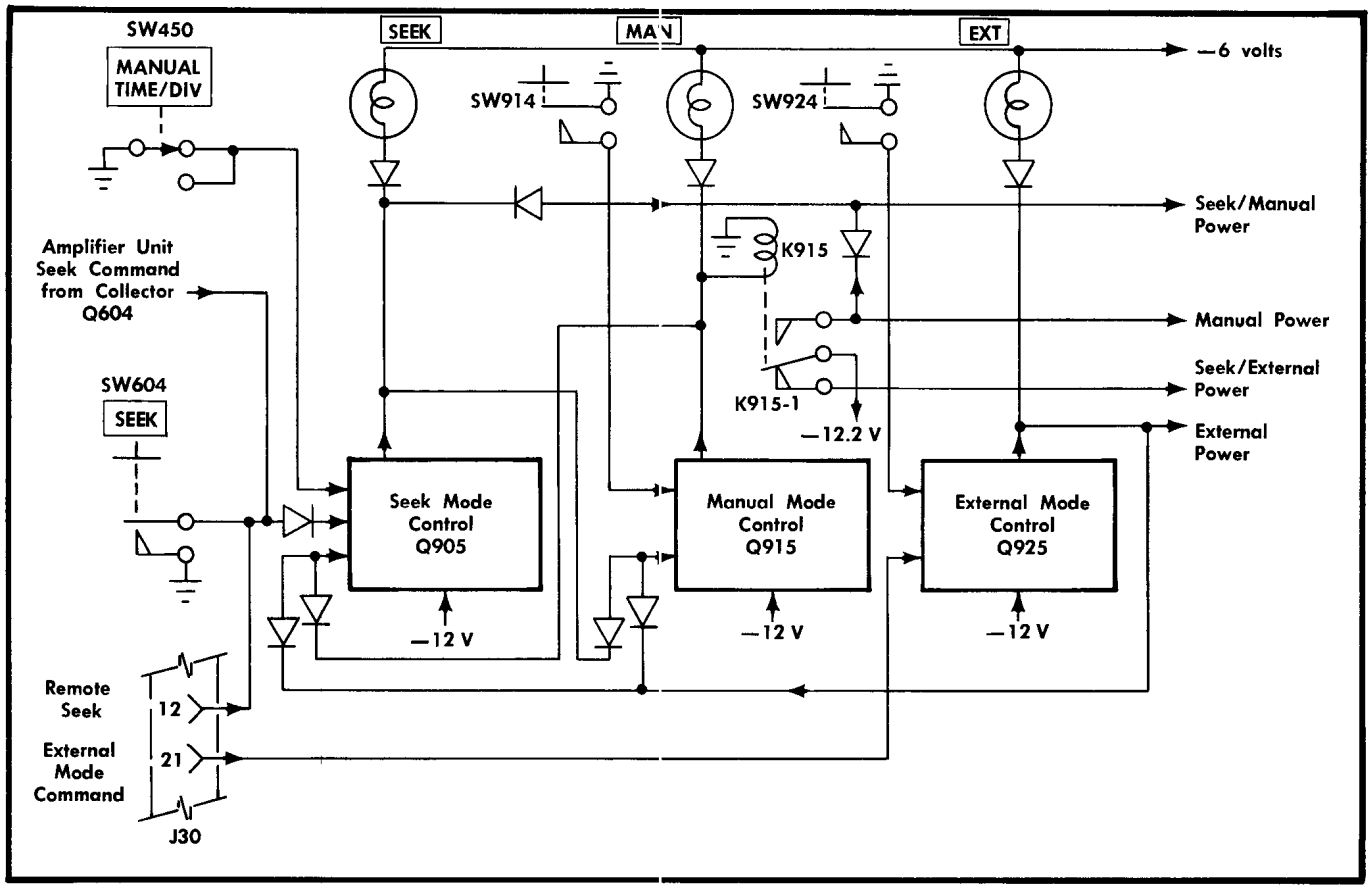


Fig. 3-28. Operating Mode Power logic block diagram.

pressed, SW914 raises the base of Q915 positive enough to turn it on and its collector goes negative. Q905 is turned off through D901 and Q915 controls the circuit (except in External Mode; see External Mode Control discussion). Changing the MANUAL TIME/DIV switch returns the unit to the Manual Mode of operation when in the Seek Mode. The base level of Q905 is established by a divider to ground through the MANUAL TIME/DIV switch (note that only part of this switch is shown on this diagram; see diagram 5 for complete switch). As this switch is rotated between steps, the ground connection for the divider is momentarily opened. The base of Q905 goes negative and it shuts off. Then, Q915 comes on and locks off Q905 to establish Manual Mode operation. Divider R911-R912-R913 holds the base of Q915 slightly more positive than the base of Q905 to return the unit to Manual Mode operation when the external mode command is disconnected.

Seek Mode Control

Fig. 3-30 shows circuit conditions for the Seek Mode of operation. In this mode of operation, Q905 determines the output from this circuit. Q905 is forward biased by the level at its base established by divider R901-R902-R903. This bias level is interrupted to return the unit to Manual Mode operation when the MANUAL TIME/DIV switch is rotated (see Manual Mode Control discussion). The collector current of Q905 flows through B905 and the SEEK pushbutton lights up. This bulb drops about six volts of the —12-volt level at the collector of Q905 to provide current to the —6-volt output line Current also flows through D909 to provide Seek/Manual Power output and through D911 to lock Q915 off. With Q915 off, K915-1 connects —12.2 volts to the Seek/External Power output.

The Seek Mode of operation can be obtained from four sources; front-panel SEEK button, remote seek command through the front-panel PROGRAM connector, seek command from a remote-seeking probe through an automatic/programmable amplifier unit and remote seek command through the amplifier unit program connector. When the Type 3B5 front-panel SEEK button is pressed, SW604 raises the base of Q905 positive enough to turn it on and its collector goes negative. Q915 is turned off through D911 and Q905 controls the circuit (except in External Mode; see External Mode Control discussion). The seek command from the amplifier unit or the remote seek command similarly raises the base level of Q905 to allow it to come into conduction.

External Mode Control

External Mode operation is provided only when the EXT button is held depressed or when an external mode command is applied through the PROGRAM connector. The circuit is connected so that this stage over-rides the other two control stages. Fig. 3-31 shows circuit conditions for External Mode operation. Q925 is on when the base is held positive enough to forward bias the transistor either by holding the EXT button depressed or by external mode command through terminal 21 of J30. When Q925 is on, col

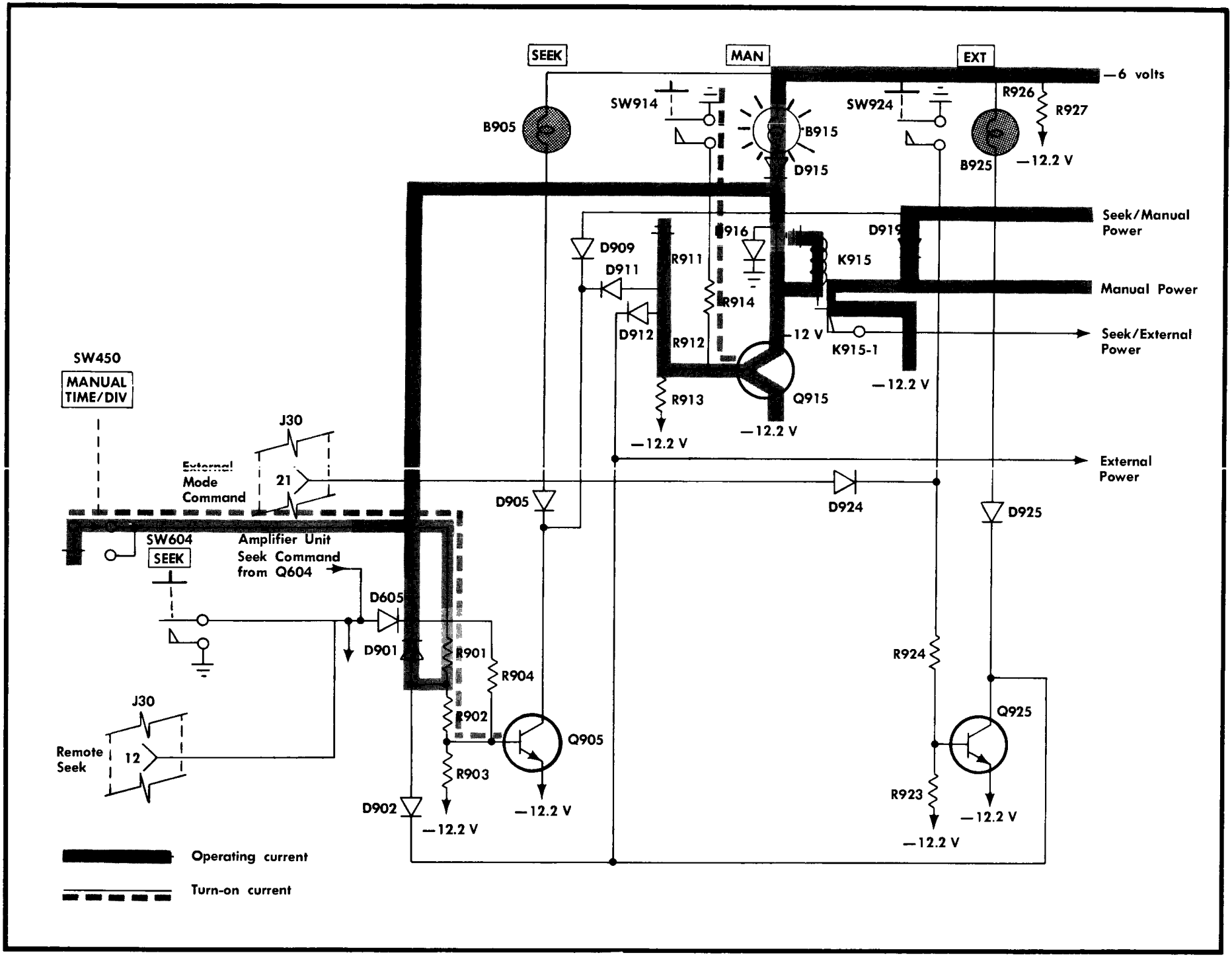


Fig. 3-29. Circuit conditions for Manual Mode operation.

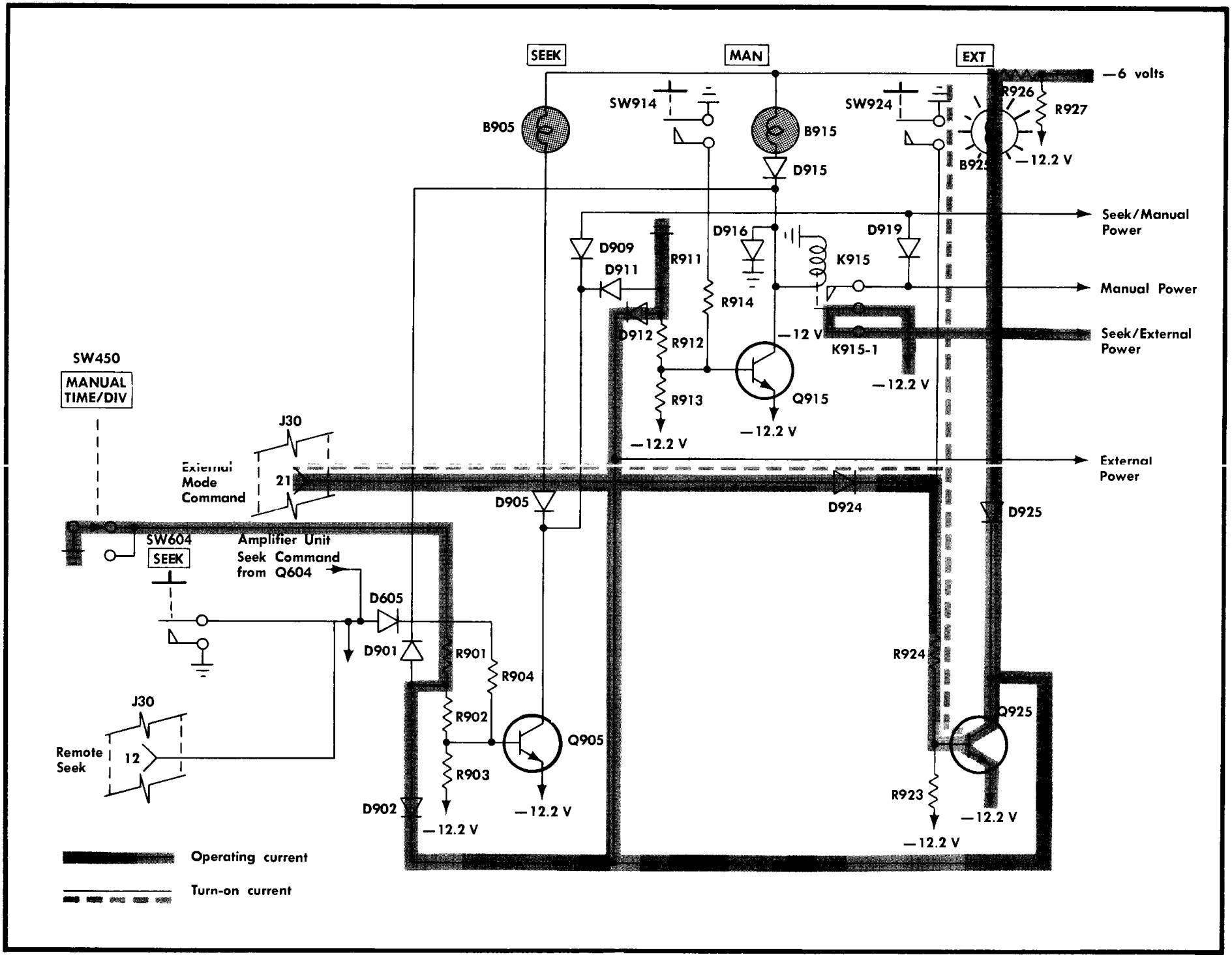


Fig. 3-31. Circuit conditions for External Mode operation.

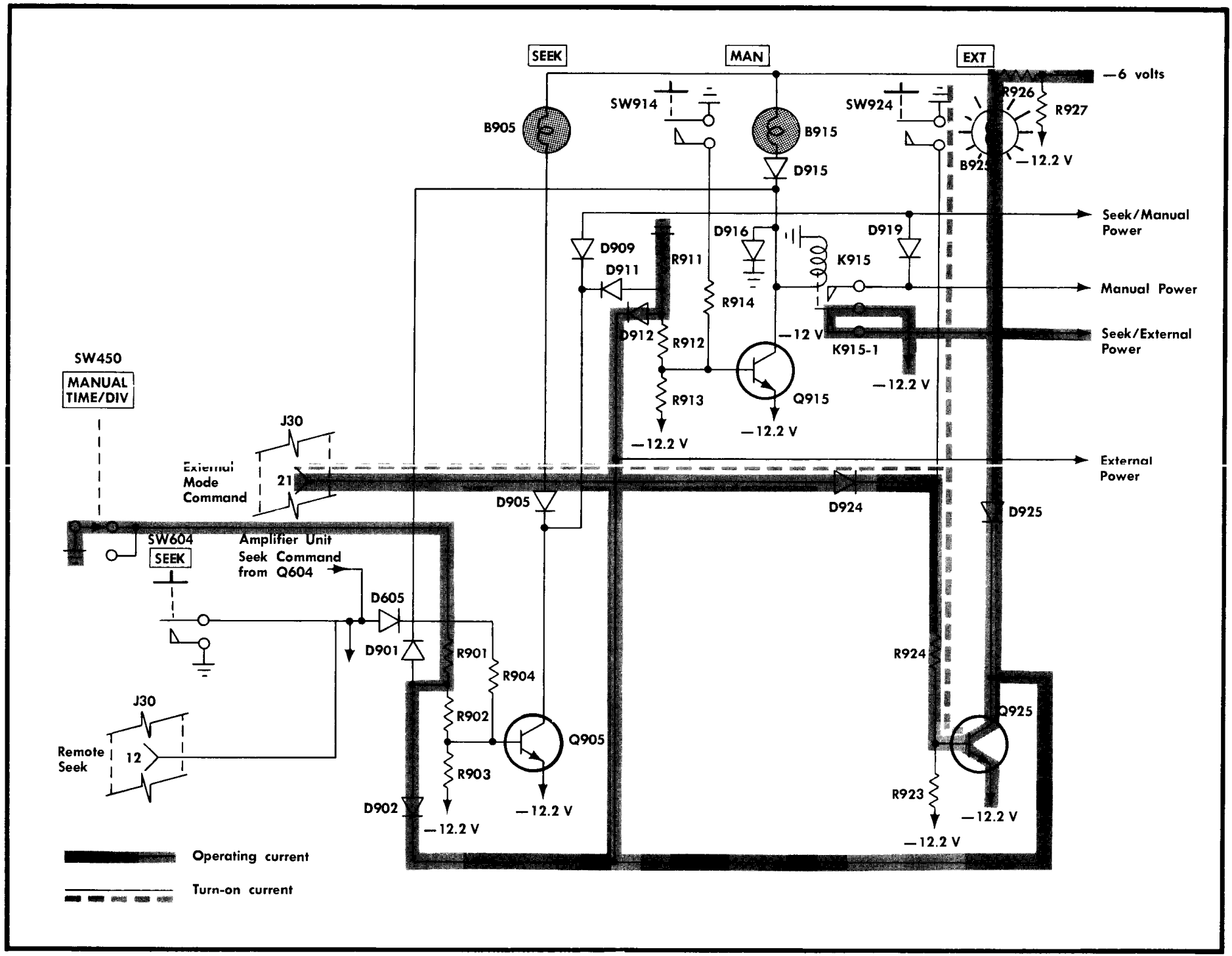


Fig. 3-31. Circuit conditions for External Mode operation.

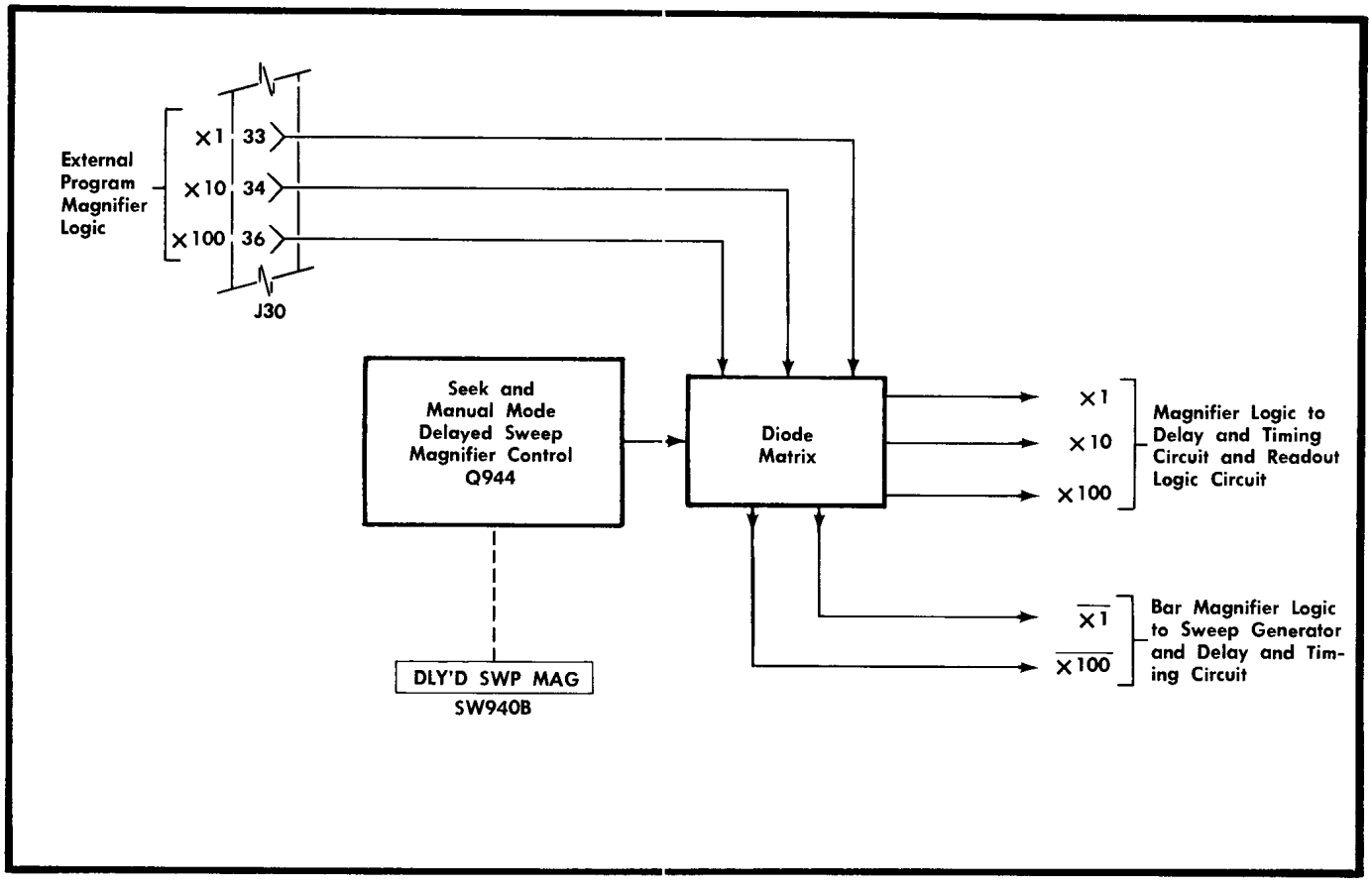


Fig. 3-32. Delayed Sweep Magnifier Control circuit logic block diagram.

lector current flows through B925 and the EXT light comes on. This bulb drops about six volts of the —12-volt level at the collector of Q925 to provide current to the —6-volt output line. The collector level of Q925 provides the External Power output. In addition, the collector level of Q925 is connected to Q905 through D902 and to Q915 through D912 to lock out the Seek and Manual Mode Control circuits. Since Q915 is held off, K915-1 connects —12.2 volts to the Seek/External Power output.

Interconnecting Diagram

General

Diagram 9 shows the interconnections between Interconnecting Plug P21, PROGRAM connector J30, Logic Card connector J400 and Counter Card connector J700. Although these interconnections are shown in part on other diagrams, this diagram gives an overall view of the interconnections. This diagram also includes the Delayed Sweep Magnifier Control circuit which is described below.

Delayed Sweep Magnifier Control

Fig. 3-32 shows a block diagram of the Delayed Sweep Magnifier Control circuit. This circuit is controlled by Q944 and the DLY'D SWP MAG switch in Seek and Manual Mode operation. For External Mode operation, the bias level is disconnected from Q944 and the circuit is controlled by external program magnifier logic through terminal 33, 34 or 36 of J30. However, circuit operation is the same regardless of the mode of operation. Table 3-1 lists the typical logic output levels on the magnifier logic lines.

For ×1 magnification, the anodes of D947 and D949 are held at zero volts by Q944 or the external program ×1 magnifier logic at terminal 33 of J30. This holds the $\overline{\times 1}$ (bar ×1 magnifier) logic line at zero volts along with the ×10 and ×100 logic lines through D947 and D949. The ×1 magnifier logic level drops to about —7 volts where it is clamped by D348 and D349 in the Delay and Timing Circuit. The $\overline{\times 100}$ (bar ×100 magnifier) logic level is also set at about —7 volts through D944.

For ×10 delayed sweep magnification, the anodes of D946 and D948 are held at zero volts by the input level which also holds the ×1 and ×100 magnifier logic lines at zero through D946 and D948. The ×10 magnifier logic line is pulled to —12 volts through resistor R949 and both the $\overline{\times 1}$ and $\overline{\times 100}$ magnifier logic lines are held at about —12 volts through D945 and D947.

×100 delayed sweep magnification places zero volts on the $\overline{\times 100}$ magnifier logic line. The ×1 and ×100 magnifier logic lines are held at zero volts through D944 and D945. D947 is reverse biased and the $\overline{\times 1}$ magnifier logic line drops to about —12 volts through R204 (Sweep Generator circuit). D949 is reverse biased and the ×100 magnifier logic line rests at about —5.5 volts as established by the

shunt diodes in the Readout Logic circuit. (The ×100 magnifier logic level may be zero volts for ×100 magnification in some positions of the MANUAL TIME/DIV switch.)

TABLE 3-1

Magnifier and Bar Magnifier Logic Output Levels

Magnification Ratio (switch position or external program logic)	Logic output Level on Logic Lines				
	×1	×10	×100	$\overline{\times 1}$	$\overline{\times 100}$
×1 (OFF)	−7 V	0 V	0 V	0 V	−7 V
×10	0 V	−12 V	0 V	−12 V	−12 V
×100	0 V	0 V	−12 V[4]	−12 V	0 V

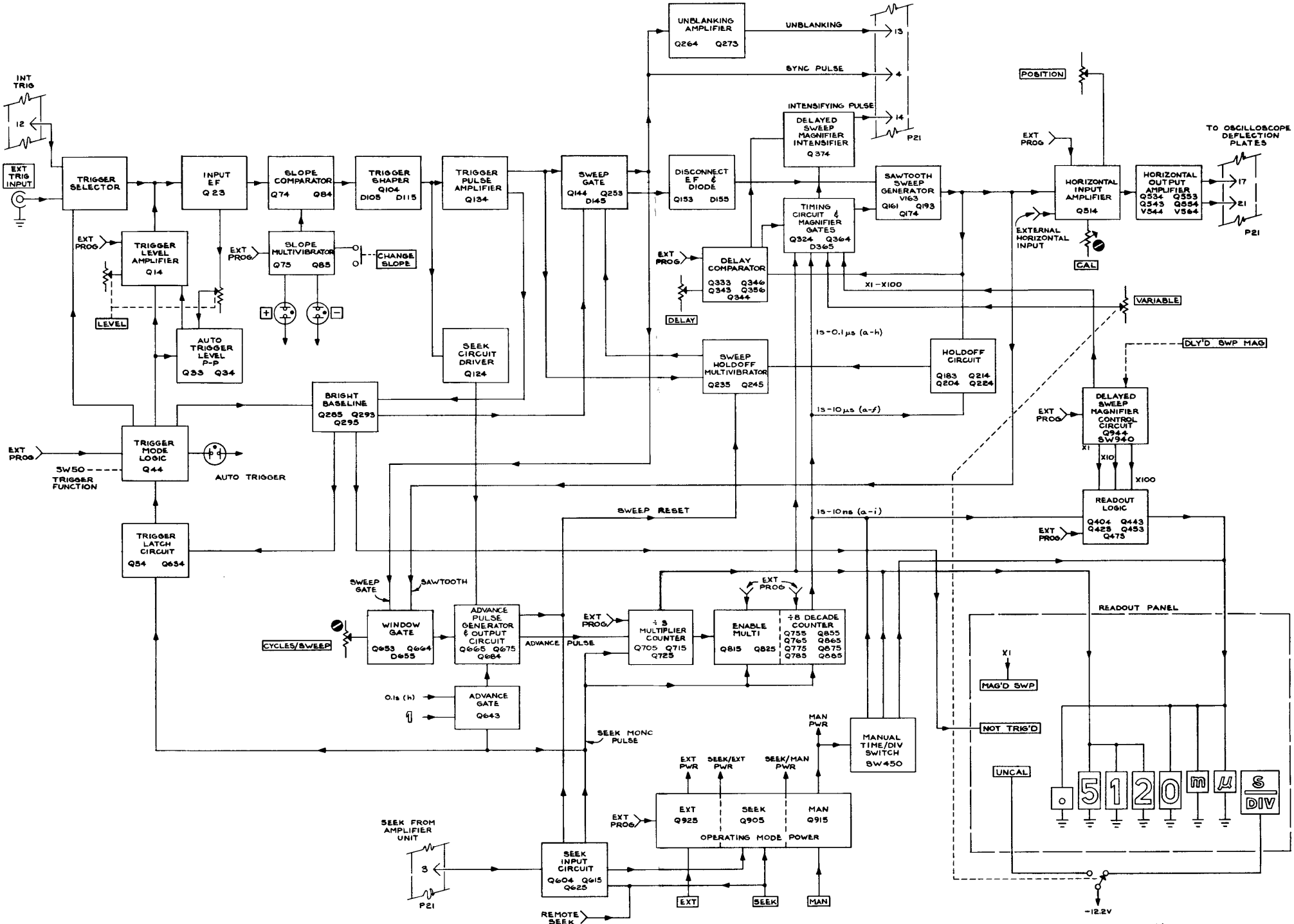
[4]Normally −12 volts. May vary between zero and −12 volts since there is no "pull-down" resistor on the ×100 magnifier logic line.

Readout Board

The Readout Board circuit shown on diagram 10 shows the connection to this board and the bulbs which produce the readout-panel display. The function of the bulbs and the operating circuitry is described in the Sweep Generator, Delay and Timing Circuit and the Readout Logic discussions

Voltage Distribution

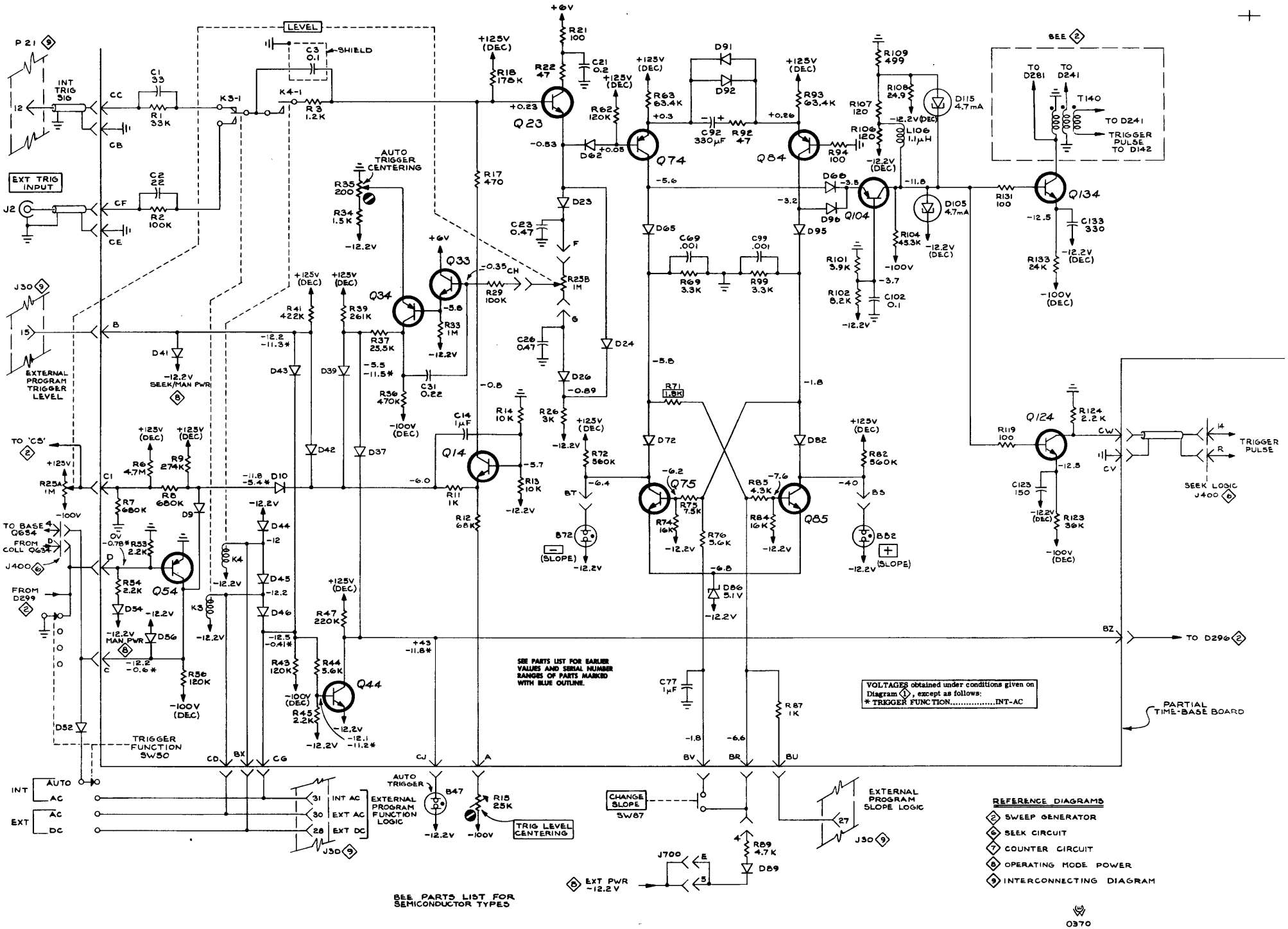
Diagram 11 shows the distribution of the voltage from the indicator oscilloscope through connector P21 to the boards and connectors in this instrument. The decoupling networks which provide decoupled operating voltages are shown in this diagram and are not repeated on the individual circuit diagrams.

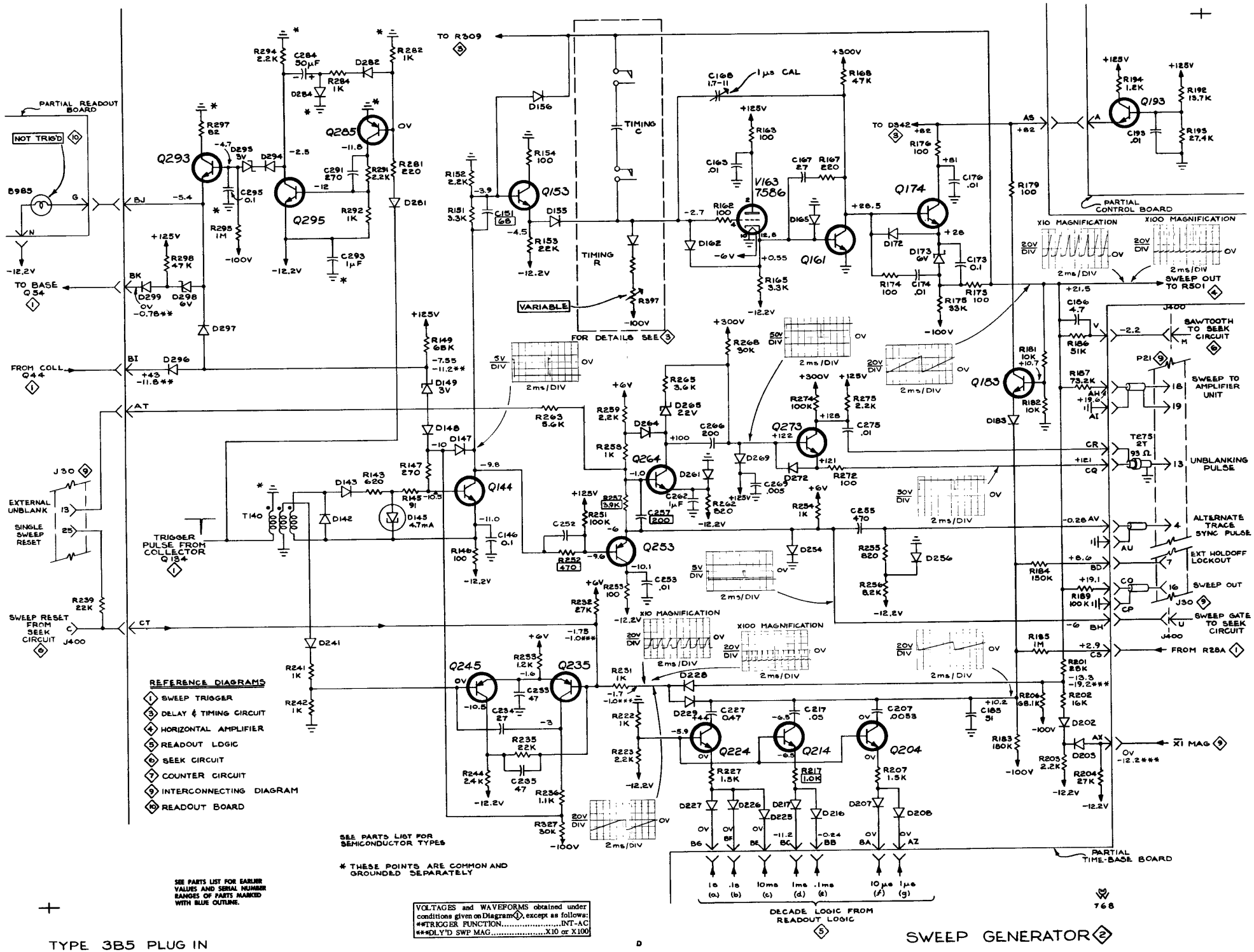


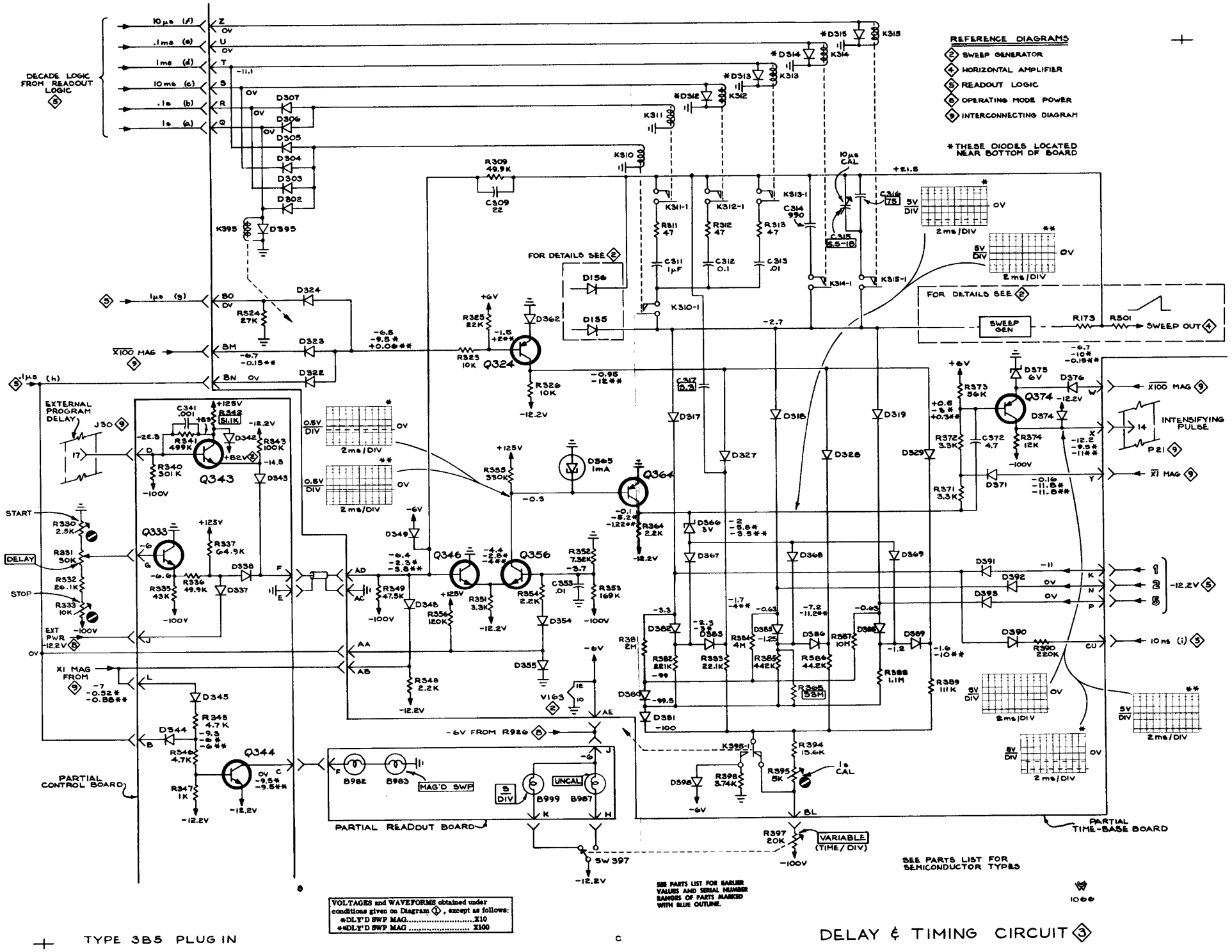
TYPE 3B5 PLUG-IN

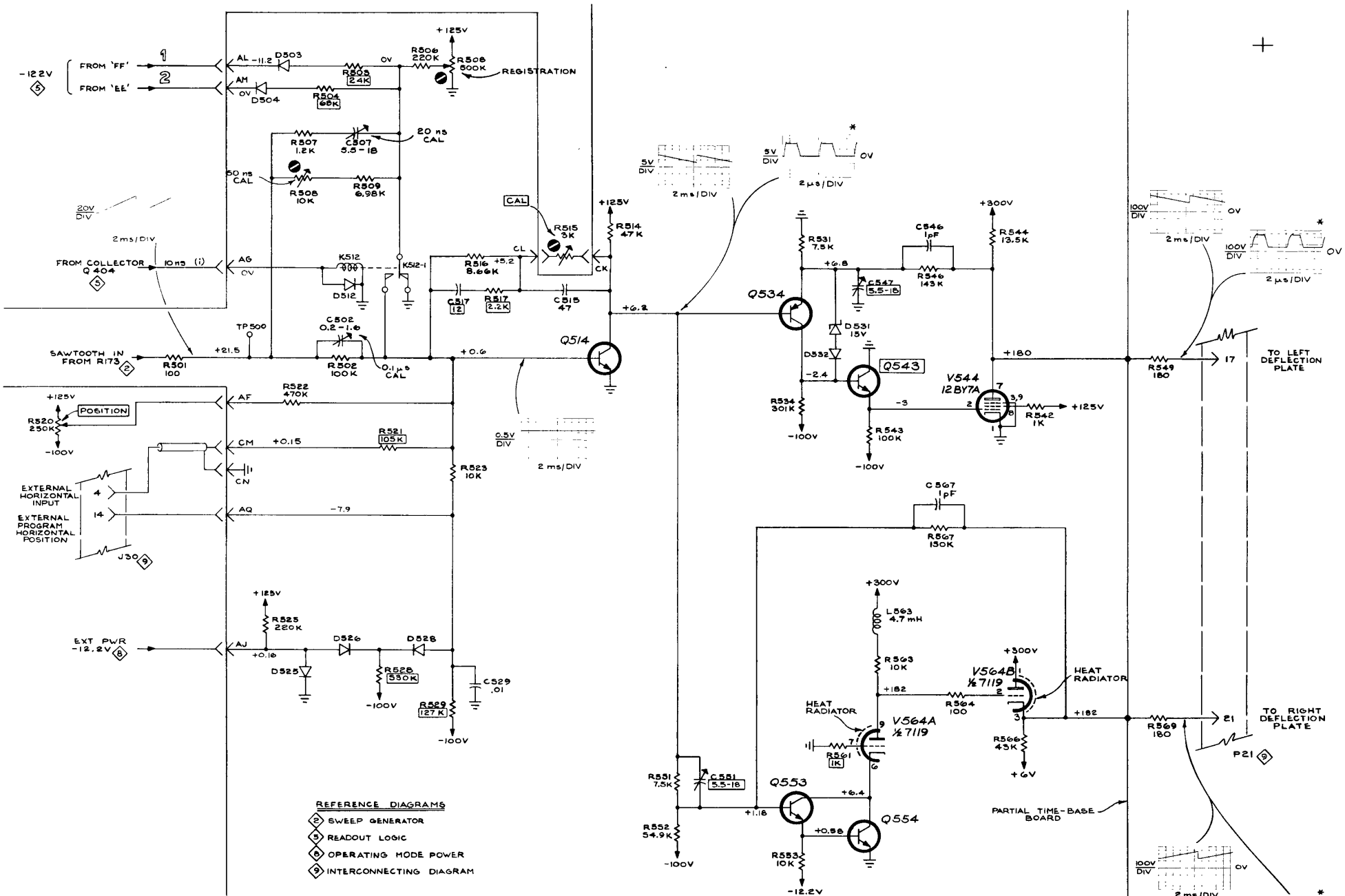
A

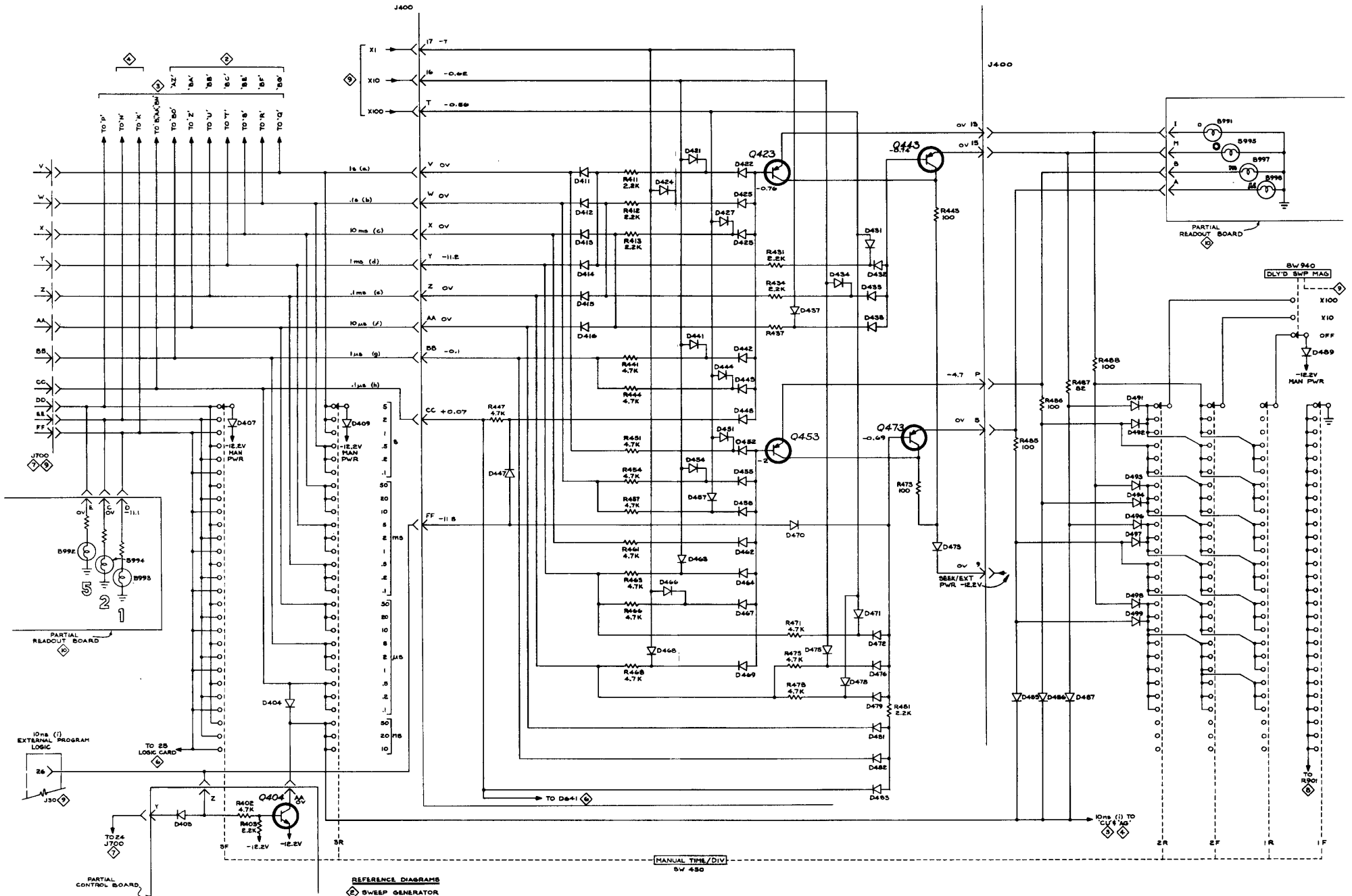
BLOCK DIAGRAM


LEVEL
SHIELD
INT TRIG SIG
EXT TRIG INPUT
AUTO TRIGGER CENTERING
EXTERNAL PROGRAM TRIGGER LEVEL
SEEK/MAN PWR
TO 'C5'
FROM D299
TO BASE Q654
FROM COLL Q634
TRIGGER FUNCTION SW50
INT
EXT
AUTO
AC
DC
INT AC
EXT AC
EXT DC
EXTERNAL PROGRAM FUNCTION LOGIC
AUTO TRIGGER
TRIG LEVEL CENTERING
CHANGE SLOPE SW87
EXTERNAL PROGRAM SLOPE LOGIC
EXT PWR -12.2V
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
VOLTAGES obtained under conditions given on Diagram 1, except as follows:
* TRIGGER FUNCTION.....INT-AC
TO D241
TO D281
T140
TRIGGER PULSE TO D142
TRIGGER PULSE
SEEK LOGIC J400
TO D296
PARTIAL TIME-BASE BOARD
REFERENCE DIAGRAMS
2 SWEEP GENERATOR
6 SEEK CIRCUIT
7 COUNTER CIRCUIT
8 OPERATING MODE POWER
9 INTERCONNECTING DIAGRAM
0370


PARTIAL READOUT BOARD
NOT TRIG'D
8985
TO BASE Q54
FROM COLL Q44
EXTERNAL UNBLANK
SINGLE SWEEP RESET
SWEEP RESET FROM SEEK CIRCUIT
TRIGGER PULSE FROM COLLECTOR Q134
TO R309
TIMING C
TIMING R
VARIABLE
FOR DETAILS SEE
1μs CAL
V163 7586
TO D342
PARTIAL CONTROL BOARD
X10 MAGNIFICATION
X100 MAGNIFICATION
SWEEP OUT TO R501
SAWTOOTH TO SEEK CIRCUIT
SWEEP TO AMPLIFIER UNIT
UNBLANKING PULSE
ALTERNATE TRACE SYNC PULSE
EXT HOLDOFF LOCKOUT
SWEEP OUT
SWEEP GATE TO SEEK CIRCUIT
FROM R28A
X1 MAG
REFERENCE DIAGRAMS
1 SWEEP TRIGGER
3 DELAY & TIMING CIRCUIT
4 HORIZONTAL AMPLIFIER
5 READOUT LOGIC
6 SEEK CIRCUIT
7 COUNTER CIRCUIT
9 INTERCONNECTING DIAGRAM
10 READOUT BOARD
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
* THESE POINTS ARE COMMON AND GROUNDED SEPARATELY
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
VOLTAGES and WAVEFORMS obtained under conditions given on Diagram 2, except as follows:
**TRIGGER FUNCTION.....INT-AC
***DLY'D SWP MAG.....X10 or X100
DECADE LOGIC FROM READOUT LOGIC 5
PARTIAL TIME-BASE BOARD
1s .1s 10ms 1ms .1ms 10μs 1μs
(a) (b) (c) (d) (e) (f) (g)
768
TYPE 3B5 PLUG IN
SWEEP GENERATOR 2


REFERENCE DIAGRAMS
2 SWEEP GENERATOR
4 HORIZONTAL AMPLIFIER
5 READOUT LOGIC
6 OPERATING MODE POWER
9 INTERCONNECTING DIAGRAM
*THESE DIODES LOCATED NEAR BOTTOM OF BOARD
DECADE LOGIC FROM READOUT LOGIC 5
10 µs (f)
.1ms (e)
1ms (d)
10ms (c)
.1s (b)
1s (a)
Z
U
T
S
R
Q
K315
K314
K313
K312
K311
K310
D315
D314
D313
D312
D307
D306
D305
D304
D303
D302
K395
D395
R309 49.9K
C309 22
10µs CAL
C316 75
C314 990
C315 5.5-18
K311-1
K312-1
K313-1
K314-1
K315-1
K310-1
R311 47
R312 47
R313 47
C311 1µF
C312 0.1
C313 .01
5V DIV
2ms/DIV
FOR DETAILS SEE 2
SWEEP GEN
R173
R501
SWEEP OUT 4
1µs (g)
BO
D324
R524 27K
X100 MAG 9
BM
D323
D322
BN
1µs (h)
D156
D155
D362
R325 22K
R323 10K
Q324
R326 10K
-12.2V
C317 5.3
D317
D318
D319
D327
D328
D329
+6V
R373 56K
D375 6V
D376
Q374
D374
R372 3.3K
C372 4.7
R374 12K
-100V
D371
R371 3.3K
X100 MAG 9
INTENSIFYING PULSE
P21 9
X1 MAG 9
EXTERNAL PROGRAM DELAY
J30 9
C341 .001
R342 51.1K
R341 499K
R343 100K
R340 301K
Q343
D342
D343
+125V
+82V 2
0.5V DIV
2ms/DIV
D365 1mA
Q364
R355 330K
R364 2.2K
D366 3V
D367
D368
D369
START
DELAY
STOP
EXT PWR -12.2V 6
R330 2.5K
R331 50K
R332 26.1K
R333 10K
Q333
R337 64.9K
R336 49.9K
R335 43K
D338
D337
D349
Q346
Q356
R352 7.32K
R354 2.2K
R353 169K
C353 .01
R349 47.5K
R356 120K
D348
D354
D355
R351 3.3K
R348 2.2K
V163 2
D391
D392
D393
D390
R390 220K
10ns (i) 5
1 2 5
-12.2V 5
D382
D383
D384
D385
D386
D387
D388
D389
R381 2M
R382 221K
R383 22.1K
R384 4M
R385 442K
R386 44.2K
R387 10M
R388 1.1M
R389 111K
R365 33M
D381
D380
AA
AB
AC
AD
AE
-6V FROM R926 6
K395-1
R394 15.6K
R395 5K
1s CAL
D398
R398 3.74K
PARTIAL CONTROL BOARD
D345
D344
R345 4.7K
R346 4.7K
R347 1K
Q344
B982
B983
MAG'D SWP
5 DIV
UNCAL
B999
B987
PARTIAL READOUT BOARD
PARTIAL TIME-BASE BOARD
R397 20K
VARIABLE (TIME/DIV)
SW 397
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
VOLTAGES and WAVEFORMS obtained under conditions given on Diagram 1, except as follows:
*DLY'D SWP MAG. X10
*DLY'D SWP MAG X100
TYPE 3B5 PLUG IN
DELAY & TIMING CIRCUIT 3
1066


-12.2V
FROM 'FF'
FROM 'EE'
AL -11.2
AM
D503
D504
R503 2.4K
R504 68K
R506 220K
R508 500K
REGISTRATION
+125V
R507 1.2K
C507 5.5-18
20 ns CAL
50 ns CAL
R508 10K
R509 6.98K
CAL
R515 5K
R514 4.7K
20V/DIV
2ms/DIV
FROM COLLECTOR Q 404
10ns (i)
AG
K512
K512-1
D512
R516 8.66K
C517 12
R517 2.2K
C515 47
CL
CK
+6.2
TP500
C502 0.2-1.6
SAWTOOTH IN FROM R173
R501 100
+21.5
R502 100K
0.1μs CAL
+0.6
Q514
+125V
POSITION
R520 250K
-100V
AF
R522 470K
CM
+0.15
R521 105K
CN
R523 10K
EXTERNAL HORIZONTAL INPUT
EXTERNAL PROGRAM HORIZONTAL POSITION
J30
AQ
-7.9
EXT PWR -12.2V
AJ
+0.18
R525 220K
D525
D526
D528
R526 330K
R529 127K
C529 .01
-100V
0.5V/DIV
2 ms/DIV
5V/DIV
2 ms/DIV
5V/DIV
2μs/DIV
+300V
R531 7.5K
C546 1pF
R544 13.5K
+6.8
C547 5.5-18
R546 143K
Q534
D531 15V
D532
Q543
-2.4
R534 301K
-100V
R543 100K
-100V
V544 12BY7A
-3
R542 1K
+125V
+180
R549 180
17
TO LEFT DEFLECTION PLATE
100V/DIV
2 ms/DIV
2μs/DIV
C567 1pF
R567 150K
+300V
L563 4.7 mH
R563 10K
+182
R564 100
V564B ½7119
HEAT RADIATOR
R566 43K
+6V
V564A ½7119
HEAT RADIATOR
R561 1K
R569 180
21
TO RIGHT DEFLECTION PLATE
P21
C551 5.5-18
R551 7.5K
Q553
+6.4
Q554
+1.18
+0.58
R552 54.9K
-100V
R553 10K
-12.2V
PARTIAL TIME-BASE BOARD
2 ms/DIV
2μs/DIV
REFERENCE DIAGRAMS
2 SWEEP GENERATOR
5 READOUT LOGIC
8 OPERATING MODE POWER
9 INTERCONNECTING DIAGRAM
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
VOLTAGES and WAVEFORMS obtained under conditions given on Diagram 1, except as follows:
*MANUAL TIME/DIV.....50ns
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
867


J400
J400
X1
X10
X100
V
W
X
Y
Z
AA
BB
CC
DD
EE
FF
1s (a)
.1s (b)
10 ms (c)
1 ms (d)
.1 ms (e)
10 µs (f)
1 µs (g)
.1 µs (h)
V 0V
W 0V
X 0V
Y -11.2
Z 0V
AA 0V
BB -0.1
CC +0.07
FF -11.8
Q423
-0.78
Q443
-0.74
Q453
-2
Q473
-0.69
Q404
AA 0V
D411
D412
D413
D414
D415
D416
D421
D422
D424
D425
D427
D431
D432
D433
D434
D435
D437
D438
D441
D442
D444
D445
D447
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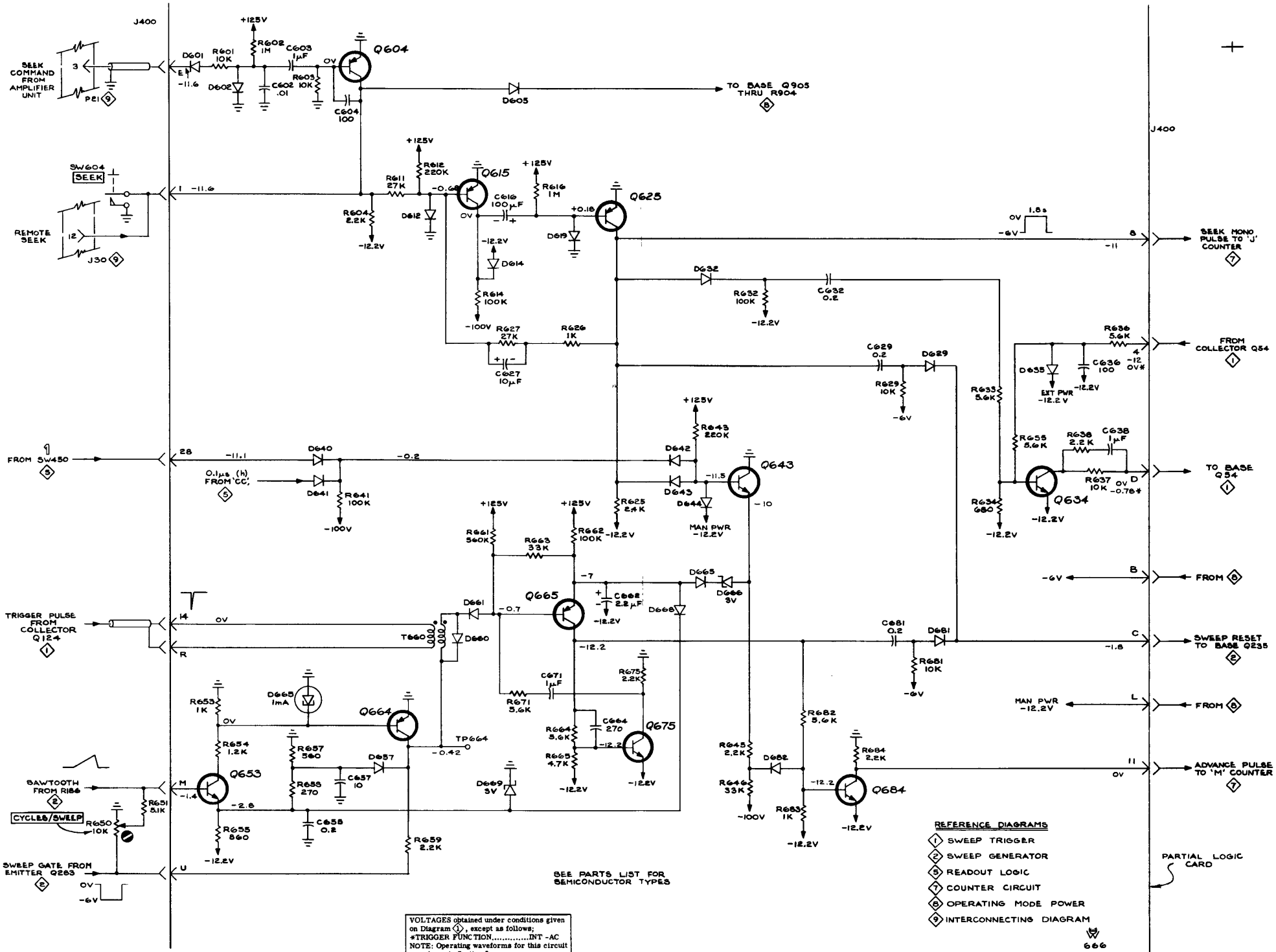
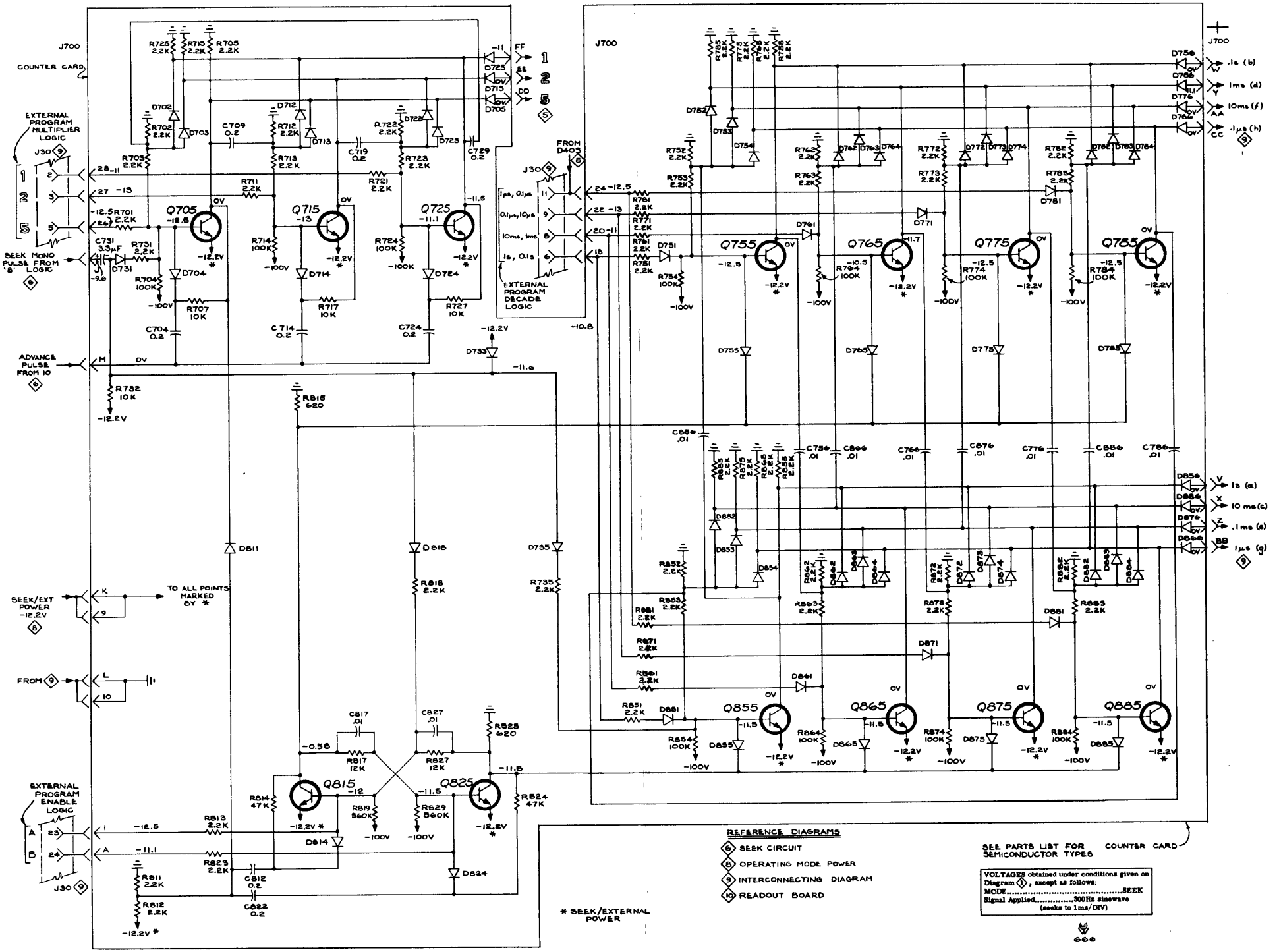
D482
D483
D485
D486
D487
D489
D491
D492
D493
D494
D496
D497
D498
D499
R411 2.2K
R412 2.2K
R413 2.2K
R431 2.2K
R434 2.2K
R437
R441 4.7K
R444 4.7K
R447 4.7K
R451 4.7K
R454 4.7K
R457 4.7K
R461 4.7K
R463 4.7K
R466 4.7K
R468 4.7K
R471 4.7K
R475 4.7K
R478 4.7K
R481 2.2K
R402 4.7K
R405 2.2K
R445 100
R455 100
R465 100
R473 100
R485 100
R488 100
R487 82
-4.7 P
0V 5
0V 9
0V 13
0V 15
-12.2V MAN PWR
SEEK/EXT PWR -12.2V
B991
B995
B997
B998
PARTIAL READOUT BOARD
B992
B994
B993
PARTIAL READOUT BOARD
SW 940
DLY'D SWP MAG
X100
X10
OFF
TO R901
10ns (1) EXTERNAL PROGRAM LOGIC
TO 25 LOGIC CARD
J30
TO 24 J700
PARTIAL CONTROL BOARD
TO D641
10ns (1) TO CUE 'AG'
MANUAL TIME/DIV SW 450
2R
2F
1R
1F
3F
3R
REFERENCE DIAGRAMS
2 SWEEP GENERATOR
3 DELAY & TIMING CIRCUIT
4 HORIZONTAL AMPLIFIER
6 SEEK CIRCUIT
8 OPERATING MODE POWER
9 INTERCONNECTING DIAGRAM
10 READOUT BOARD
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3B5 PLUG-IN
A
666
READOUT LOGIC 5



TYPE 3B5 PLUG-IN

A

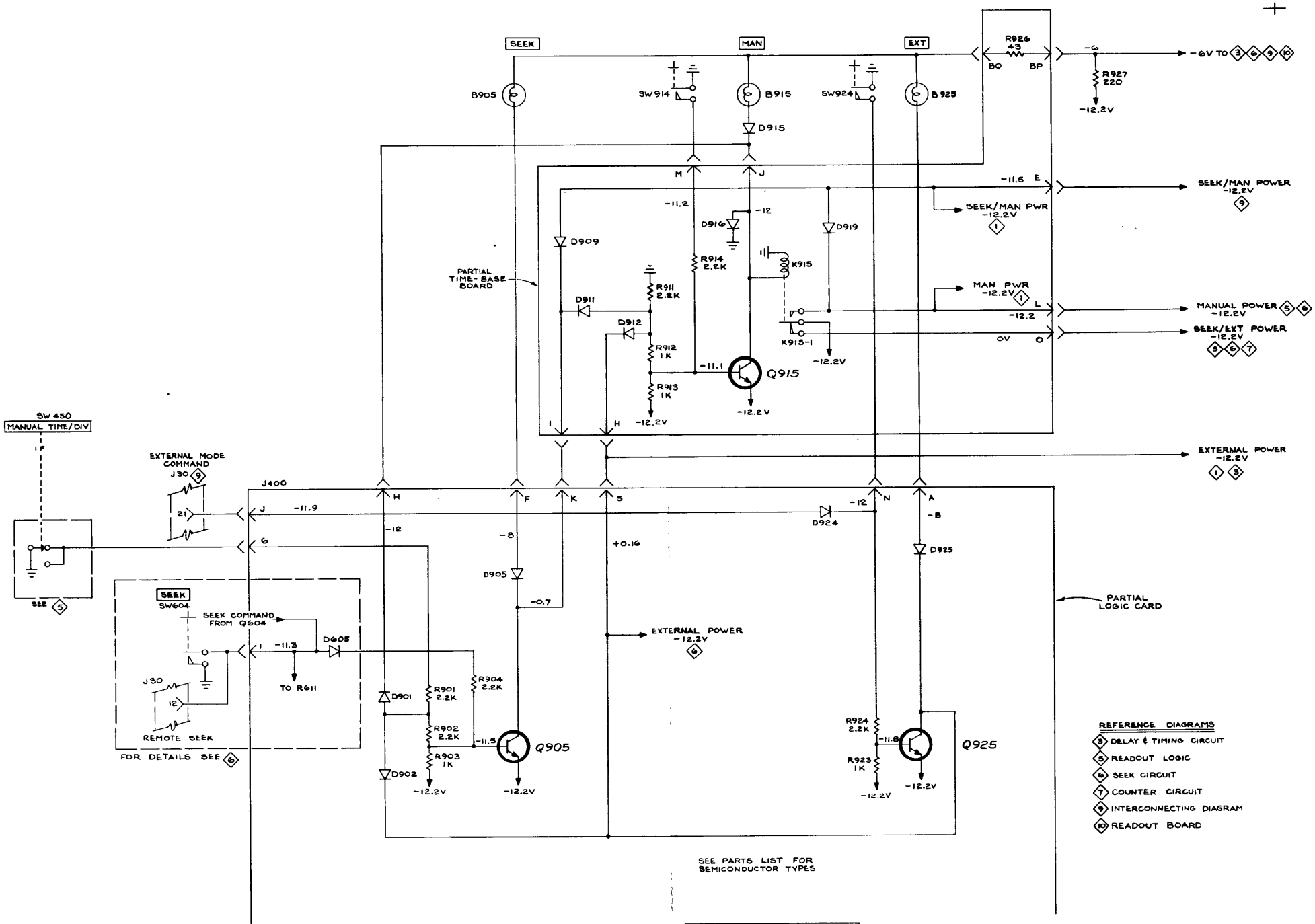
SEEK CIRCUIT 6



TYPE 3B5 PLUG-IN

A

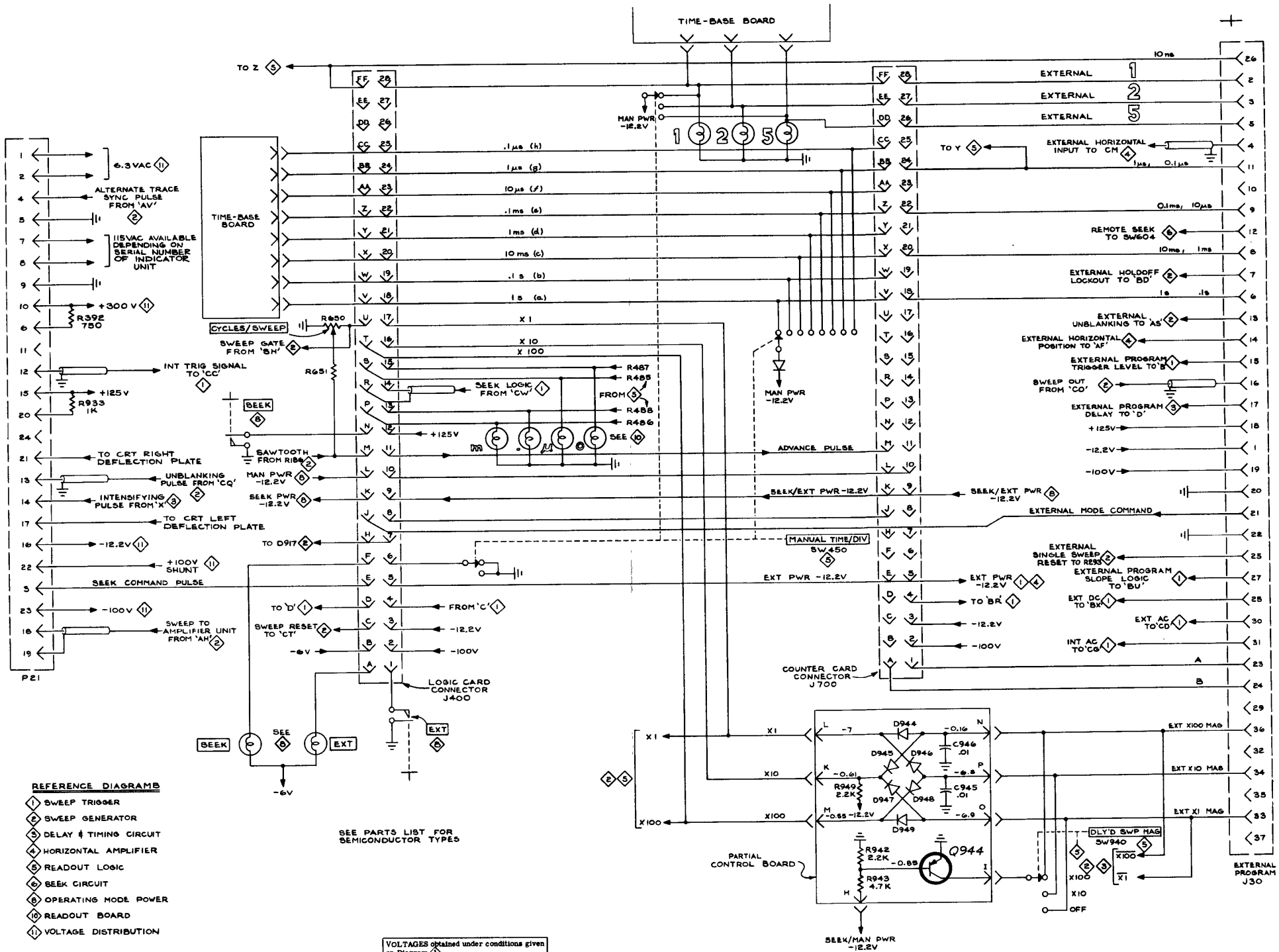
COUNTER CIRCUIT 7



TYPE 3B5 PLUG-IN

A

OPERATING MODE POWER 8



REFERENCE DIAGRAMS

1. SWEEP TRIGGER
2. SWEEP GENERATOR
3. DELAY & TIMING CIRCUIT
4. HORIZONTAL AMPLIFIER
5. READOUT LOGIC
6. SEEK CIRCUIT
8. OPERATING MODE POWER
10. READOUT BOARD
11. VOLTAGE DISTRIBUTION

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

VOLTAGES obtained under conditions given on Diagram 1.

668

TYPE 3B5 PLUG-IN

A1

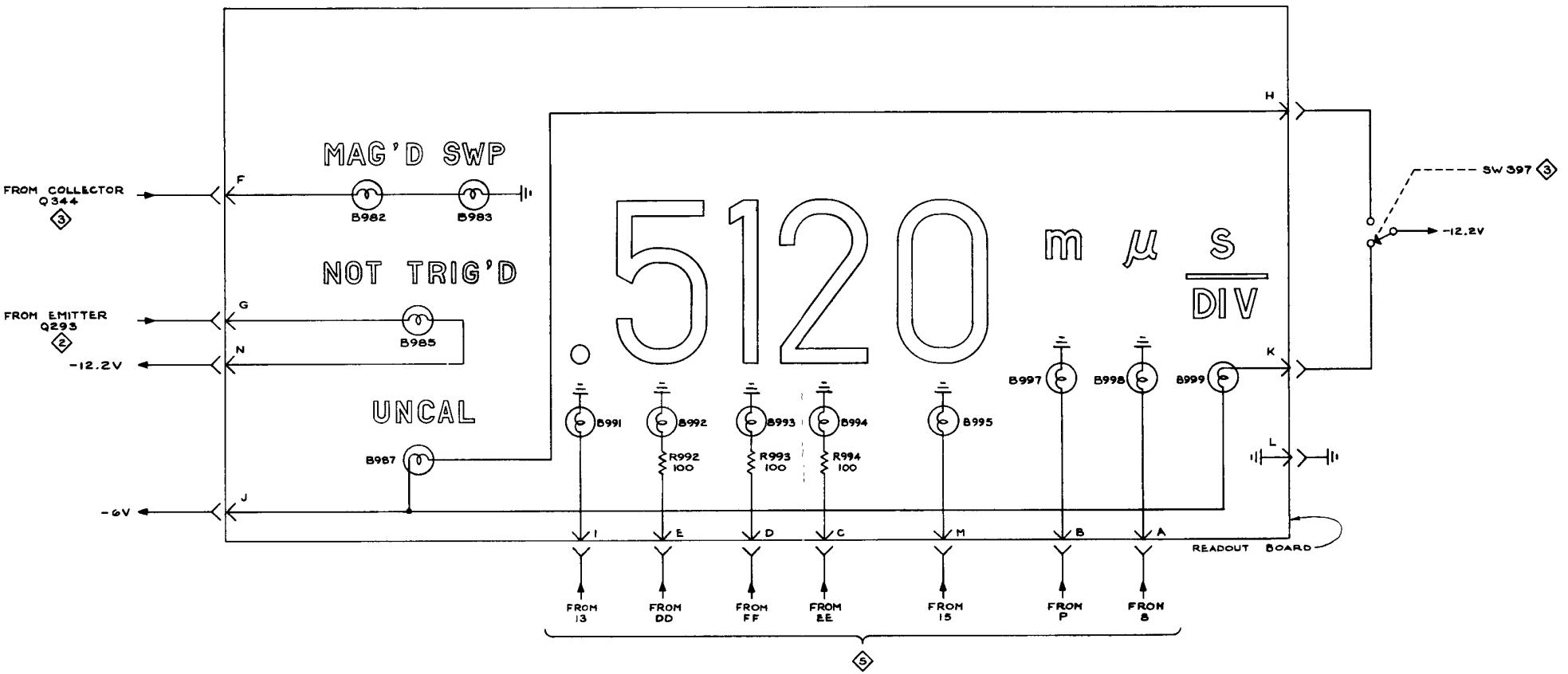
INTERCONNECTING DIAGRAM 9

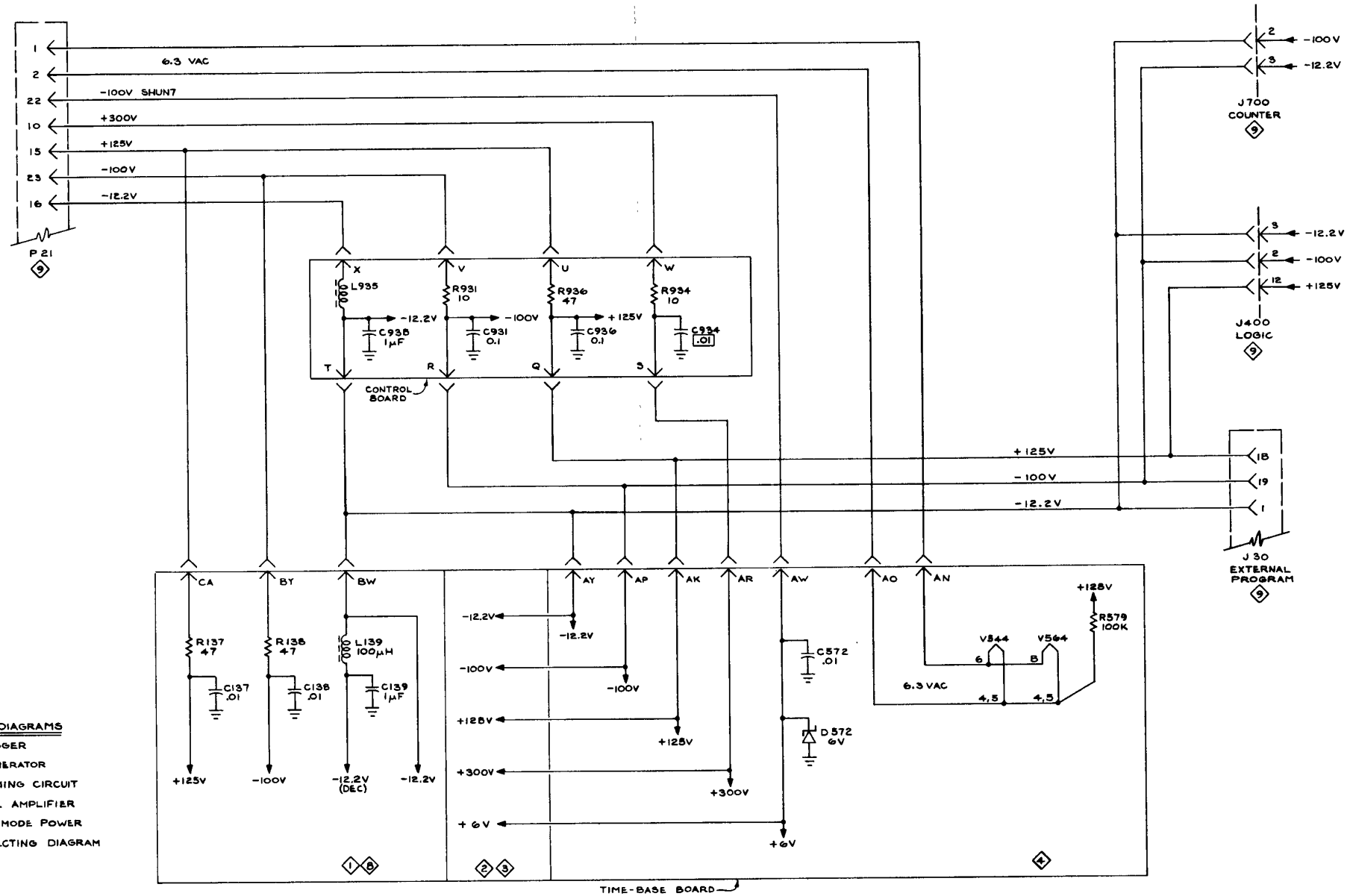
REFERENCE DIAGRAMS

2 SWEEP GENERATOR

3 DELAY & TIMING CIRCUIT

5 READOUT LOGIC





REFERENCE DIAGRAMS

1. SWEEP TRIGGER
2. SWEEP GENERATOR
3. DELAY & TIMING CIRCUIT
4. HORIZONTAL AMPLIFIER
5. OPERATING MODE POWER
9. INTERCONNECTING DIAGRAM

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

1166

+ TYPE 385 PLUG-IN

VOLTAGE DISTRIBUTION 11