INSTRUCTION MANUAL

TYPE 3S76 SAMPLING DUAL-TRACE UNIT

Tektronix, Inc.
S.W. Millikan Way • P. O. Box 500 • Beaverton, Oregon • Phone MI 4-0161 • Cables: Tektronix


TYPE 3S76 SAMPLING DUAL-TRACE
A
POSITION
DUAL-TRACE
SMOOTH
NORMAL
B
POSITION
A ONLY
B ONLY
2-200 VAR.
MV/DIV.
100 50 20
200 10
5
A+B
A VERT.
B HORIZ.
X1 H. MAG.
NORM.
NORM.
INV.
INV.
CALIB.
DC OFFSET
-1V +1V
GAIN ADJ.
INPUT A
2V P-P MAX., 50Ω
INTERNAL TRIGGER
A OFF B
X 100 OFFSET
MONITOR (100 KΩ)
INPUT B
2V P-P MAX., 50Ω
PROBE
A OUT
B OUT
(A+B)
1V/DIV. (10KΩ)
TEKTRONIX, INC.
PORTLAND, OREGON, U.S.A.

SECTION 1
CHARACTERISTICS

General Information

The Type 3S76 Dual-Trace Sampling Plug-In Unit is designed for vertical deflection of Tektronix Types 561A and RM561A Oscilloscopes and the Type 567 Readout Oscilloscope. Also, it is equipped to drive the readout circuitry of the Type 6R1 Digital Unit. A sampling sweep plug-in unit (such as the Tektronix Type 3T77) must be used with the Type 3S76.

The Type 3S76 permits observation of low-level signals of fractional nanosecond duration or risetime. These observations can be made at frequencies up to 875 megacycles*. The dual-trace feature of the Type 3S76 permits simultaneous displays of two signals.

The Type 3S76 takes a small sample of successive input signals. Each sample is completed in a fraction of a nanosecond. Each sample is initiated by the sweep plug-in unit, slightly later in time with respect to the last sampled pulse. The samples are reconstructed on a relatively slow time base provided by the sampling sweep plug-in unit.

The sampling process is unaffected by the characteristics of the device under test or by changes in sensitivity settings. Low noise and absence of jitter provide a high-resolution display comparable to conventional oscilloscopes.

Risetime

0.4 nsec (corresponding to an upper 3-db frequency of about 875 mc), each channel.

Input Impedance

50 ohms, ±1%, each channel.

Deflection Factor

Variable in seven steps of 2, 5, 10, 20, 50, 100, and 200 mv/div, each channel. For 10 to 200 mv/div, accuracy is ±3% when the 2-200 VAR. control is set to CALIB. For 2 and 5 mv/div, accuracy is ±5%. The 2-200 VAR. controls provide a continuously variable deflection factor (uncalibrated) from 2 to 200 mv/div.

Maximum Allowable Signal Input

±2 volts, combined dc and peak ac, with respect to ground.

Noise (Referred to Input)

1 mv, peak-to-peak, with SMOOTH-NORMAL switch at SMOOTH.

2 mv, peak-to-peak, with SMOOTH-NORMAL switch at NORMAL.

*The Type 3T77 Time Base will trigger to 500 mc. For signals above this limit, a trigger-countdown circuit may be employed to furnish trigger signals for the Type 3T77.

Operating Modes

Single-Channel Operation: Channel A display or channel B display only.

Dual-Trace Operation: Both channels display signals simultaneously.

A + B: Display of the algebraic sum or difference (±A±B) of two signals.

A Vertical — B Horizontal: Both channels operate. Channel A provides vertical deflection, channel B provides horizontal deflection. Permits X-Y operation at 0.4-nsec risetime.

Vertical Signal Output

Dc-coupled signal output from either channel. Output of A OUT or B OUT jacks is 1 volt for each division of vertical deflection, with a source impedance of 10 kilohms. Open-circuit output voltage swing is about +2 to +18 volts.

Dynamic Range

±8 major graticule divisions.

Dc Offset

±1 volt, referred to input, available in each channel. Monitor voltage is ±100 volts through 100 kilohms.

Signal Delay

55 nsec in both channels. For example, when used with the Type 3T77 Sampling Sweep Plug-In Unit with minimum delay, the sweep function reaches the crt deflection plates about 12 nanoseconds ahead of the signal.

Mechanical

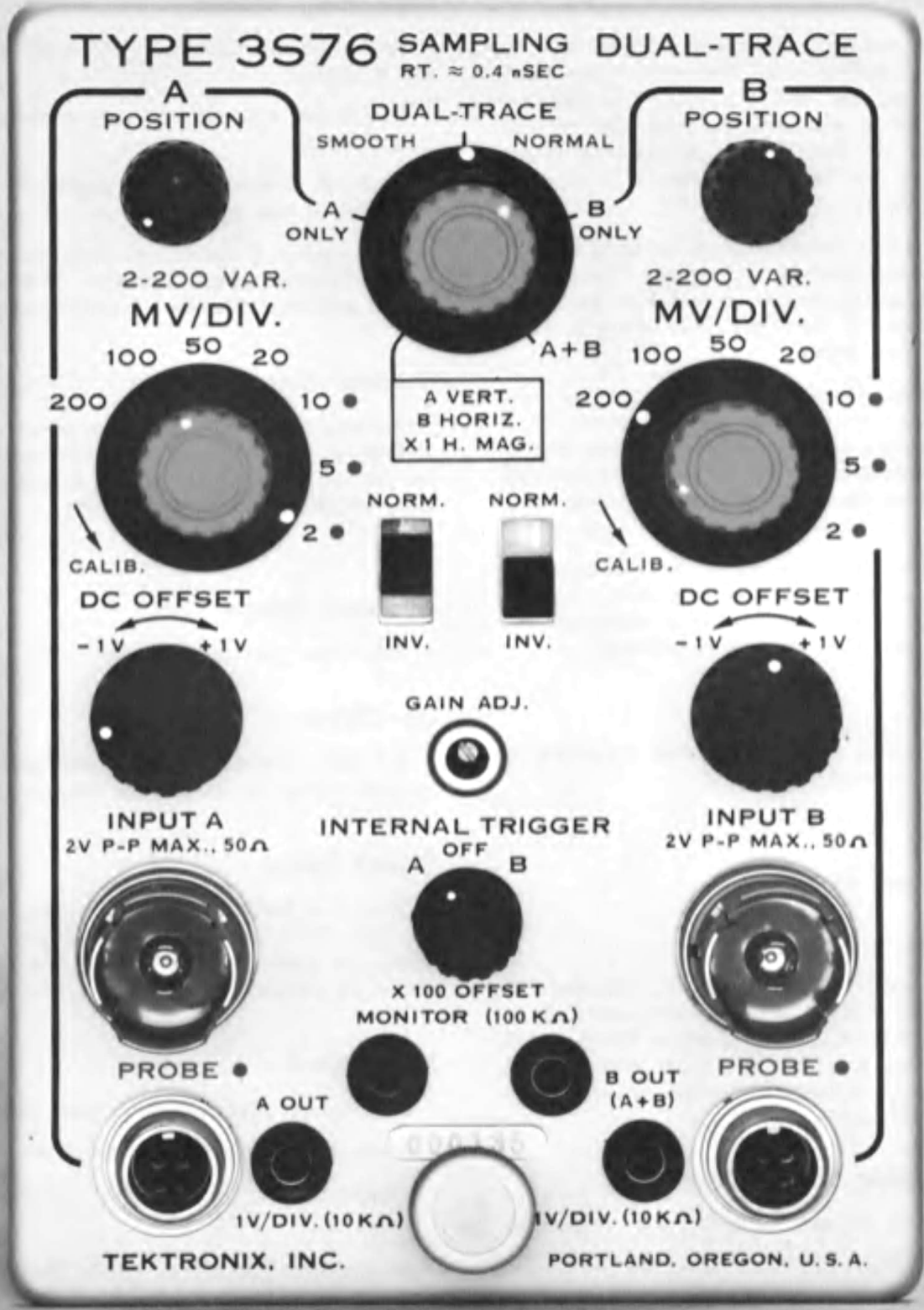
Construction: Aluminum-alloy front panel and chassis.

Finish: Photo-etched, anodized front panel.

Weight: 7 lbs.

Accessories Supplied With the Type 3S76

		Tektronix Part Number
2	10XT attenuators, 50-ohm GR connectors	(017-044)
2	5-nanosecond, 50-ohm cables, RG/58 with 50-ohm GR connectors	(017-502)
2	Instruction manuals	(070-332)


TYPE 3S76 SAMPLING DUAL-TRACE
RT. ≈ 0.4 nSEC
A
POSITION
DUAL-TRACE
SMOOTH
NORMAL
A ONLY
B ONLY
B
POSITION
2-200 VAR.
MV/DIV.
100 50 20
200
10
5
2
A+B
A VERT.
B HORIZ.
X1 H. MAG.
CALIB.
NORM.
INV.
DC OFFSET
-1V +1V
GAIN ADJ.
INPUT A
2V P-P MAX., 50Ω
INTERNAL TRIGGER
OFF
A B
INPUT B
X 100 OFFSET
MONITOR (100 KΩ)
PROBE
A OUT
B OUT
(A+B)
1V/DIV. (10KΩ)
TEKTRONIX, INC.
PORTLAND, OREGON, U.S.A.

SECTION 4

CIRCUIT DESCRIPTION

General Operation

Operation of a sampling system is somewhat different from that of conventional oscilloscope circuitry. In a conventional oscilloscope system, the crt beam is continuously deflected vertically by the signal applied to the input; thus, the selected portion of the signal is displayed completely each time the electron beam makes a sweep. This is not the case in a sampling system. Instead, only a very small segment or sample of the input signal is displayed each time the sampling system is triggered. The Type 3S76 takes very short samples of the input signal amplitude. Each sample is obtained progressively later in time on successive (but not necessarily consecutive) pulses. The precise time at which the samples are taken is controlled by the sampling sweep plug-in unit. A thorough discussion of the timing technique is contained in the sweep unit instruction manual.

The samples are reconstructed on a slow sweep and appear as dots on the crt. The slow sweep is actually a series of horizontal steps; one for each sample. The rate of the slow sweep depends on how many dots are contained in the total display and the repetition rate of the input signal. Since each sample represents the instantaneous amplitude at the time the sample was taken, the position of the dots on the crt corresponds to sampled points along the input signal.

SNAP-OFF & MEMORY CIRCUITS

Input Circuitry

From the front-panel 50 Ω INPUT A or INPUT B connector, the incoming signal passes through the primary winding of the Trigger Takeoff Transformer T1030 or T2030, depending on which channel is used. At this point, about one-fifth of the input signal voltage is coupled to the transformer secondary and sent to the sampling sweep plug-in unit for triggering. The INTERNAL TRIGGER switch selects either channel A or B as an internal trigger source. The INTERNAL TRIGGER switch should be turned OFF when external triggering is used to minimize undesired signal coupling between plug-in units.

From T1030 or T2030, the input signal goes through a 55-nanosecond delay line. This 55-nanosecond delay follows the sweep unit time to operate before the signal is applied to the vertical system.

The matching network at the output of the delay line serves three functions: (1) It properly terminates the line, thus preventing reflections; (2) It compensates for the inherent losses of the delay line; (3) It corrects for the trigger signal removed by the Trigger Takeoff transformer.

The diodes in the four-diode Sampling Gates are special gallium arsenide diodes with very fast switching characteristics. The diodes are quiescently back biased to prevent the incoming signal from reaching the grid of Nuvistors V1073 or V2073. The exact amount of quiescent back-bias voltage is set by the A or B BRIDGE VOLTS adjustment. When properly calibrated, the bridge voltage is normally 1.6 to 2.0 volts with respect to ground. When a sample is taken, the diodes are forward biased for a fraction of a nanosecond by a sharp pulse from the Driver Blocking Oscillator (Q2010) and Snap-Off circuit (D2002). The Driver Blocking Oscillator is, in turn, triggered by a signal from the sweep plug-in unit.

Driver Blocking Oscillator and Snap-Off Circuit

The Driver Blocking Oscillator Q2010 is a triggered (monostable) oscillator which receives a trigger pulse from the sweep unit through pin 18 of the interconnecting plug. The output pulse of the Driver Blocking Oscillator goes to the Snap-Off circuit, the Memory Gate Driver Q2024, and the Dual-Trace Blocking Oscillator Q2230.

The Snap-Off circuit operates from the Driver Blocking Oscillator pulse to produce sharp spikes for application to the Sampling Gate. Snap-Off diode D2002 operates quiescently with a forward current of about 60 milliamps. A positive-going pulse from T2010 tries to reverse this current abruptly. Storage effects in diode D2002 prevent blocking-oscillator current from passing into the bridge-driving circuit during storage time of D2002. Suddenly, storage current through D2002 ends, and no further current flows to ground. This sudden diversion of current through D2002 to the output circuit produces the sharp sampling spike waveshape. T2001 converts the spike to push-pull. The clipping line sets the length of the spike or pulse.

Preamp and Memory Circuit

Operation of the Preamp and Memory circuits is identical for both channel A and B. The following discussion will therefore describe only the operation of channel A.

The Preamp circuits consist of V1073, Q1074, Q1084, and Q1094. The Preamp circuits are permitted at least 10 microseconds to amplify the samples of the input signal, couple the new sample to the Memory circuit, and come to rest again before the next sample.

The Memory circuit consists of V1133A, Q1134, and Q1141 and is a form of gated operational amplifier which remembers the previous sample levels. The signal amplified by the Preamp circuit is proportional to the change in signal voltage between the last sample (remembered by the Memory circuit) and the new sample of signal voltage. Thus, only the error signal, or difference signal, produces an input through the four-diode Sampling Gate to the grid of V1073. The information that passes through the Preamp circuits from the last sample is properly attenuated by the MV/DIV. switch.

To further describe the operation of the individual circuits of the Preamp and Memory, the following discussion traces the path of the sample through each circuit.

During the short time the Sampling Gate is open, the signal voltage is coupled to the grid circuit of cathode-follower V1073. The grid of V1073 is permitted to charge to about 25% of the instantaneous signal voltage.

V1073 has a capacitive input which remembers the signal amplitude for a time after the Sampling Gate is closed. The grid of V1073 receives two signals; the sample information admitted by the Sampling Gate and, shortly afterward, the "feedback" voltage from the Memory circuit developed on C1049. Whenever the feedback voltage equals the instantaneous voltage of the new sample, no error signal passes the Preamp circuit.

The output signal of the cathode follower is coupled directly to the base of transistor Q1074. Ac gain of Q1074 is about 6 when the SMOOTH-NORMAL switch is at NORMAL, and about 1.5 at SMOOTH. With the ac gain of the stage decreased in the SMOOTH position, the error voltage coupled to the Memory circuit is decreased. Consequently, it takes slightly longer for the Memory circuit to respond to changing peak voltages of the incoming samples. Thus, with the SMOOTH-NORMAL switch at SMOOTH, the output of the Memory circuit is only 25% of each sample. Thus, the response to random noise is reduced. This change in gain causes a lag in following the input signal changes which can only be overcome by selecting at least 100 dots during transition time of the input signal. However, the calibrated deflection factor of the Type 3S76 is not affected.

The output from Q1074 is coupled through the MV/DIV. switch to the base of Q1084. Precision divider R1081, together with R1147 (both part of the MV/DIV. switch) select the desired deflection factor.

Q1084 and Q1094 normally amplify the error signal about 100 times. Feedback resistor R1090 and the A PRE-AMP SENS. adjustment R1088 set the gain of the circuit. Thus, R1088 adjusts for proper error signal gain of the amplifier.

The output of Q1084/Q1094 amplifier is coupled through C1124 to the Memory Gate circuit. Just after each sample is passed into the Memory circuit, C1124 discharges and is again ready to accept the next error signal. The Memory Gate is a form of diode bridge. Zener diode D1124 clamps the voltage across the bridge at 6 volts. R1126 and R1127 provide the proper bridge balance so the voltage on the ends of the bridge is +3 and −3 volts with respect to ground. After the sample is taken and before the error signal passes through the delay of the Preamp circuits, the Memory Gate is opened by a pulse from Memory Gate Driver Q2024. The gating pulse from Q2024 is coupled to the center winding of T1130. This 12-volt drive pulse momentarily turns on D1130 and D1132. This allows the error signal (if any) to pass on to the grid of V1133A. When the output pulse of the Preamp circuits reaches C1124, the charge is transferred from C1124 through the Memory Gate to C1132 of the Memory circuit, according to $Q = CE$. After the error voltage reaches its peak at C1124, the gate closes from the removal of the Memory Gate Driver pulse and no further charge can be transferred to the Memory circuit until the next Memory Gate Driver pulse.

The Memory circuit, consisting of V1133A, Q1134, and Q1141, is a wide-band operational amplifier with feedback through C1132. With the Memory Gate diodes back biased, its output voltage must equal the sum of the dc voltage at the grid of V1133A and the stored voltage in C1132. The output of the Memory circuit is from the collector of Q1141 which is capable of supplying ±5 milliamps into the following stage.

When a charge (or error signal) is introduced to the grid of V1133A through the Memory Gate, the charge passes through C1132 changing its output voltage according to $E = Q/C$. However, the input voltage to V1133A remains essentially constant due to the high amplifier gain and degenerative feedback through C1132 to the grid of V1133A.

Dc Offset Circuit

The Dc Offset circuit, consisting of V2133A, is a controllable voltage source. Voltage from this circuit is fed back to three points on the four-diode Sampling Gate. In addition, voltage from this circuit appears at the X100 OFFSET MONITOR jack. This voltage is 100/0.772* times the equivalent voltage that is fed back to the Sampling Gate. The voltage division occurs through R1158, R1148 and R1149, and related shunt resistors.

CHANNEL A & B AMPLIFIERS

Vertical Amplifier

The channel A Amplifier consists of Q1173, Q1184, and Q1183. In addition, the Inversion Stage (Q1163/Q1164) is in the circuit when the NORM.-INV. switch is in the NORM. position. When the NORM.-INV. switch is at NORM., the polarity of the displayed signal is the same as the applied signal. Gain of the Inversion Stage is set to exactly 1 with the A INV. GAIN control R1161. The A NORM. GAIN control R1172 is adjusted to set the signal amplitude at the base of Q1173. R1172 is adjusted with the NORM.-INV. switch at INV. so the Inversion Stage has no effect. When the MV/DIV. switch is set at 2, the 2-200 VAR. control (adjustable portion of R1171) is bypassed and the full resistance of R1171 appears in the circuit for maximum input signal.

The output of emitter follower Q1173 is developed across R1173. Gain of this stage is essentially unity. The signal is then coupled through the Vertical Mode switch SW2190 (in all positions except A+B) to the remaining stages of the Vertical Amplifier. In the A+B position, the signal is coupled through R2177 and combined with the signal in channel B. Channel B then produces the algebraic sum of the two signals.

From SW2190, the channel A signal passes through R1175 to the base of Q1184. Q1184 and Q1183 form a feedback amplifier which inverts and amplifies the signal. The A POSITION control R1180 provides a variable dc current through R1181 for positioning the trace on the crt. Emitter

*0.772 is the gain factor that the input signal encounters through equalization at the end of the delay line in the input circuit.

follower Q1183 provides an extremely low output impedance to drive the A OUT jack, the signal pickoff for the digital unit, and the Common Output Amplifier.

DUAL-TRACE SWITCHING & COMMON OUTPUT AMPLIFIER

Dual-Trace Multivibrator

The Dual-Trace Switching Multivibrator has three states, selected by the Vertical Mode switch SW2190. The state of the Multivibrator determines whether the output of channel A or B is applied to the Common Output Amplifier. The Dual-Trace Switching Multivibrator operates so the outputs of both channels are never applied to the Common Output Amplifier simultaneously. In dual-trace operation, the outputs of channel A and B are applied alternately to the Common Output Amplifier, with switching occurring after each sample.

When the Vertical Mode switch is set to A ONLY, a negative voltage is applied to the base of Q2255 and a positive voltage to the base of Q2245. In this mode, Q2255 is cut off and Q2245 is conducting. The collector voltage of Q2255 is at its most positive point, and the collector voltage of Q2245 is at its most negative point. The voltage difference between the two collectors is connected directly across the channel A and B diode gates. Current through R1196 and R1197 forward biases the channel A gate, and the channel A signal is passed to the Common Output Amplifier. The diodes in the channel B gate are reverse biased and cannot pass the channel B signal.

If the Vertical Mode switch is set to B ONLY, the polarity of the voltage difference between the collectors of Q2245 and Q2255 is reversed. This forward biases the channel B gate diodes and reverse biases the channel A gate diodes. This, in turn, allows only the channel B signal to pass to the Common Output Amplifier.

If the Vertical Mode switch is set to DUAL-TRACE, R2245 and R2255 are both connected to —12.2 volts. This converts the Multivibrator to a bistable configuration. In dual-trace operation, the Dual-Trace Blocking Oscillator Q2230 is monostable and is triggered by the pulses from the Memory Gate Driver. The output triggering signal of the Dual-Trace Blocking Oscillator passes through diodes D2238 and D2239 to trigger the Switching Multivibrator.

The Dual-Trace Blocking Oscillator is in operation only when the Vertical Mode switch is in the DUAL-TRACE position. At all other times, collector voltage is removed from Q2230 and the circuit is inoperative.

Common Output Amplifier

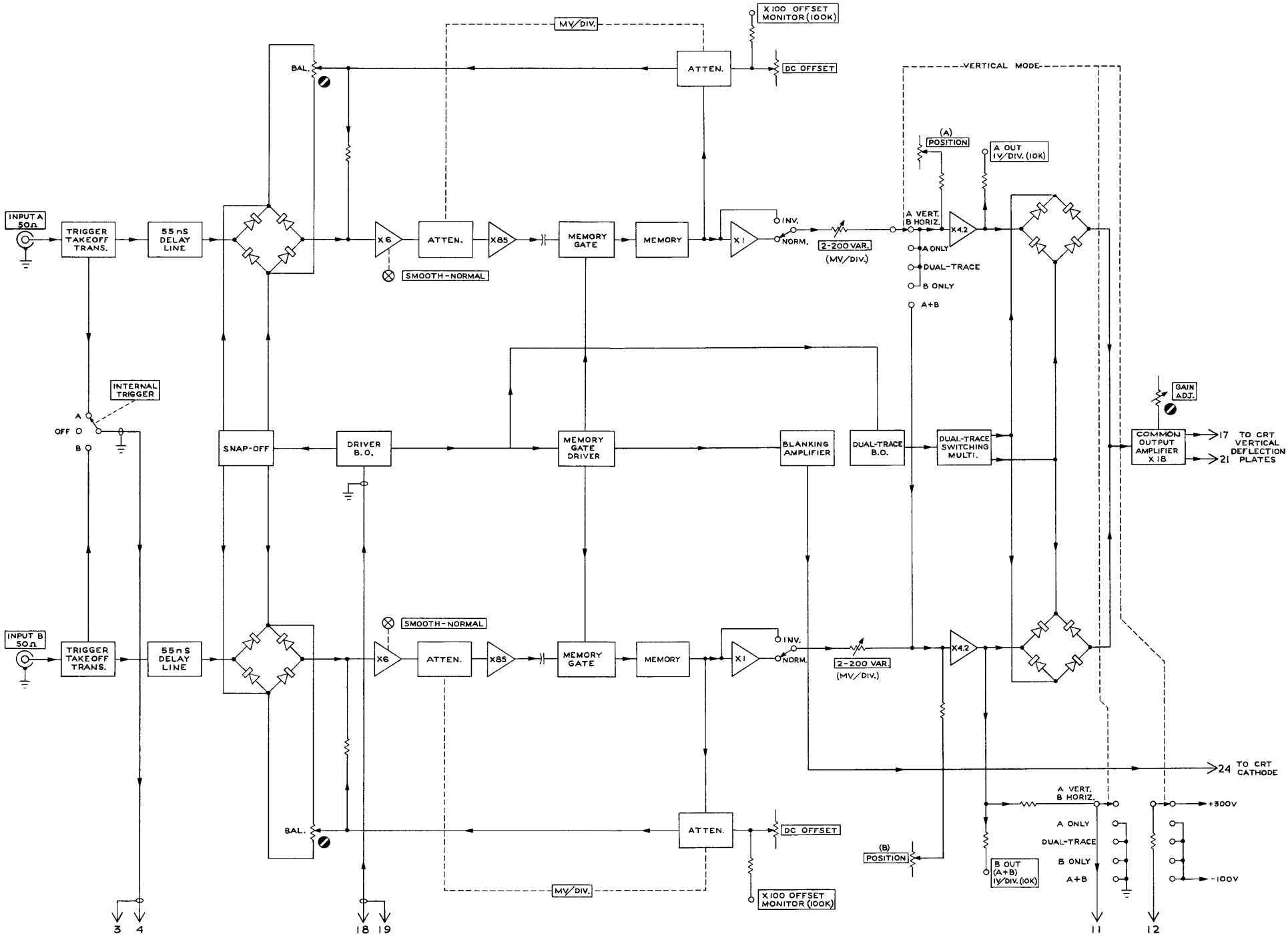
The Output Amplifier V1224 (A and B), Q1204, and Q1214, is a cathode-emitter-coupled paraphase amplifier. It converts the signal at the base of Q1204 to a push-pull signal between the plates of V1224. The output from the amplifier drives the vertical deflection plates of the crt via pins 17 and 21 of the interconnecting plug. The GAIN ADJ. control R1209 varies the coupling between the emitters of Q1204 and Q1214 and is used to set the gain of the stage. The gain is greatest when R1209 is set for minimum resistance.

+100-Volt Power Source

The +100-Volt Power Source furnishes power to the Bridge Gates (emitter of Q2287) and the PROBE power connectors (emitter of Q2297). The source voltage is held constant by voltage regulator V2289. V2289 maintains a constant voltage drop of about 82 volts over a relatively wide current range. The 20-volt source elevates the total voltage output to about +100 volts with respect to ground.

+20- and +70-Volt Power Source

The +70 volts is obtained with a voltage divider from the +125-volt supply of the oscilloscope. Transistors Q2274 and Q2277 provide a stable +20-volt supply. Q2277 is a shunt regulator driven by Q2274. The base of Q2274 is at —0.3 volt when the emitter of Q2277 is at +20 volts. If the emitter voltage of Q2277 attempts to change from +20 volts, the base of Q2274 will move in the same direction. The change in voltage at the base of Q2274 forces the collector voltage of Q2274 and the base voltage of Q2277 to move in the opposite direction. This change appears at the emitter of Q2277 and cancels the original attempt of the +20-volt supply to change.

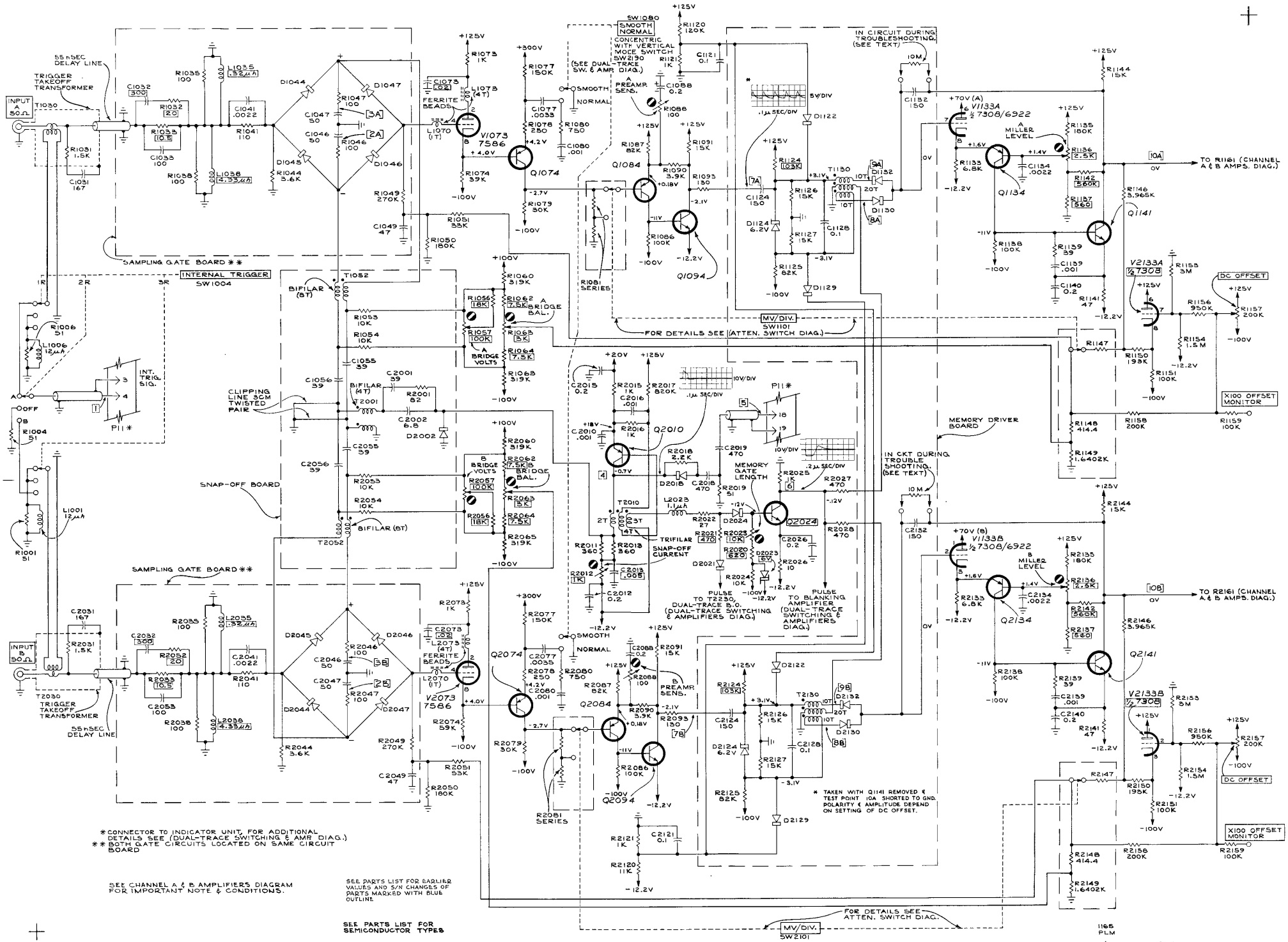


TYPE 3S76 SAMPLING DUAL-TRACE

A

BLOCK DIAGRAM

CMD 565

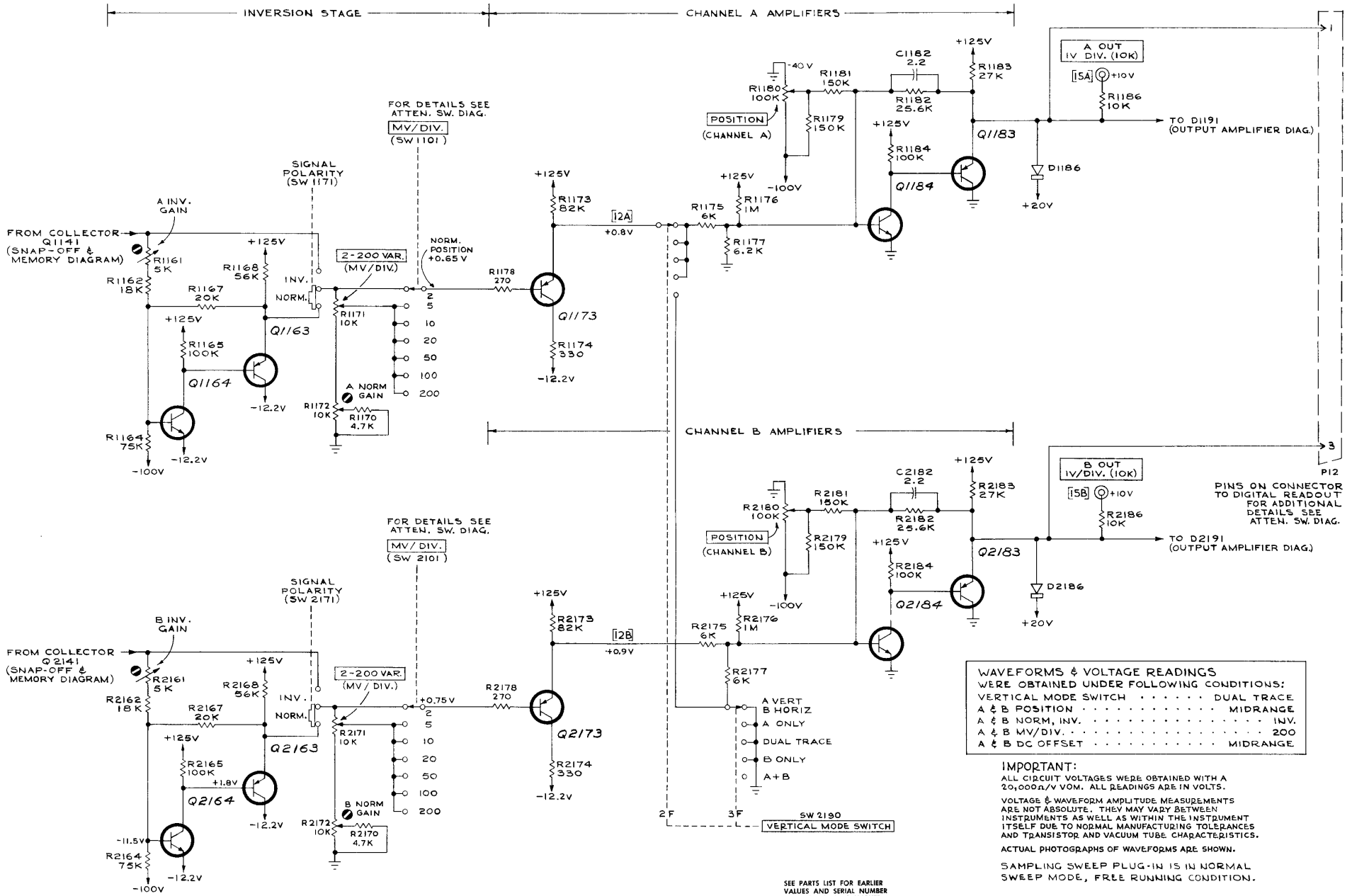


TYPE 3S76 PLUG-IN UNIT

C

1165 PLM

SNAP-OFF & MEMORY



WAVEFORMS & VOLTAGE READINGS
WERE OBTAINED UNDER FOLLOWING CONDITIONS:

VERTICAL MODE SWITCH	DUAL TRACE
A & B POSITION	MIDRANGE
A & B NORM, INV.	INV.
A & B MV/DIV.	200
A & B DC OFFSET	MIDRANGE

IMPORTANT:
ALL CIRCUIT VOLTAGES WERE OBTAINED WITH A 20,000Ω/V VOM. ALL READINGS ARE IN VOLTS.

VOLTAGE & WAVEFORM AMPLITUDE MEASUREMENTS ARE NOT ABSOLUTE. THEY MAY VARY BETWEEN INSTRUMENTS AS WELL AS WITHIN THE INSTRUMENT ITSELF DUE TO NORMAL MANUFACTURING TOLERANCES AND TRANSISTOR AND VACUUM TUBE CHARACTERISTICS.

ACTUAL PHOTOGRAPHS OF WAVEFORMS ARE SHOWN.

SAMPLING SWEEP PLUG-IN IS IN NORMAL SWEEP MODE, FREE RUNNING CONDITION.

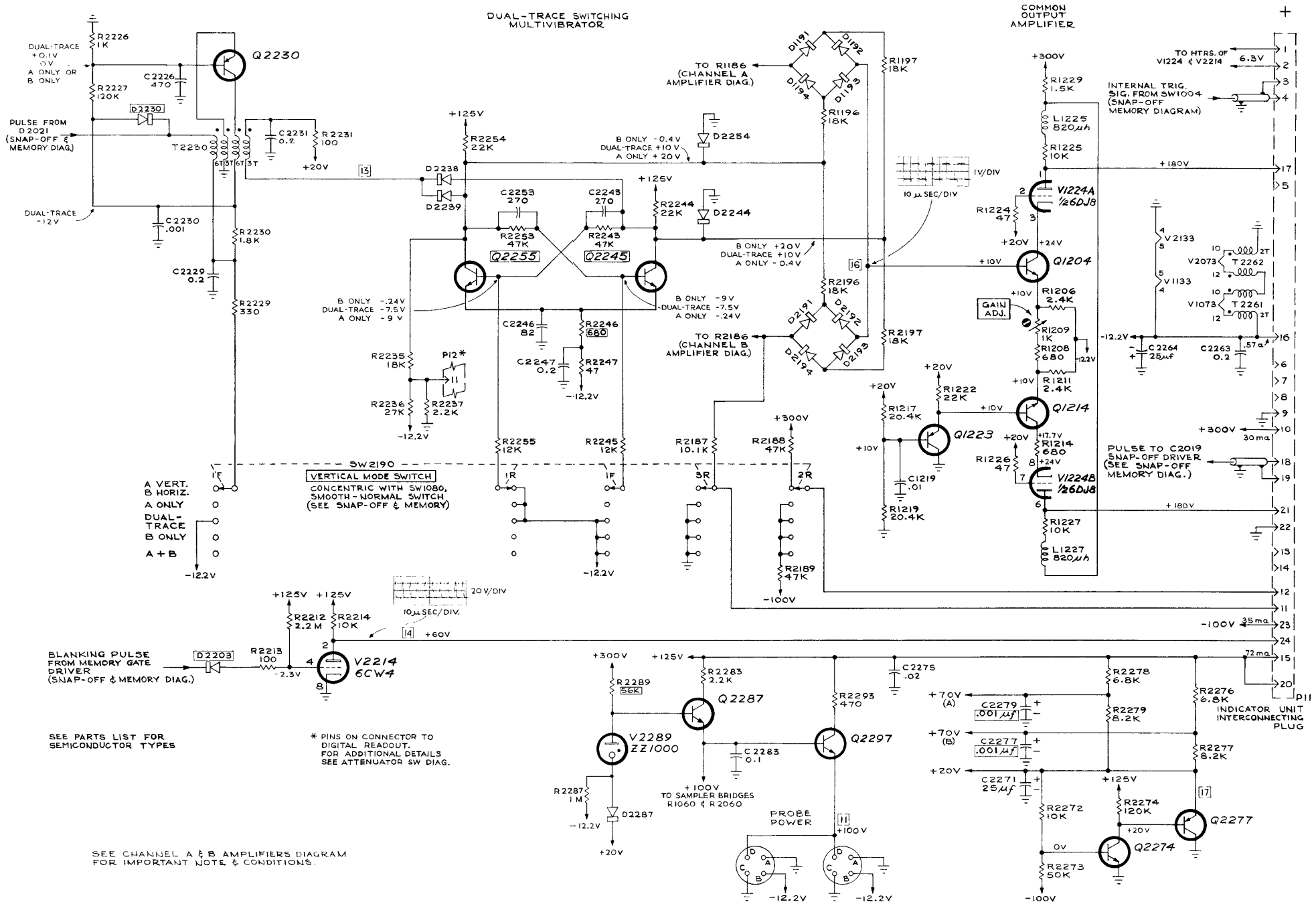
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

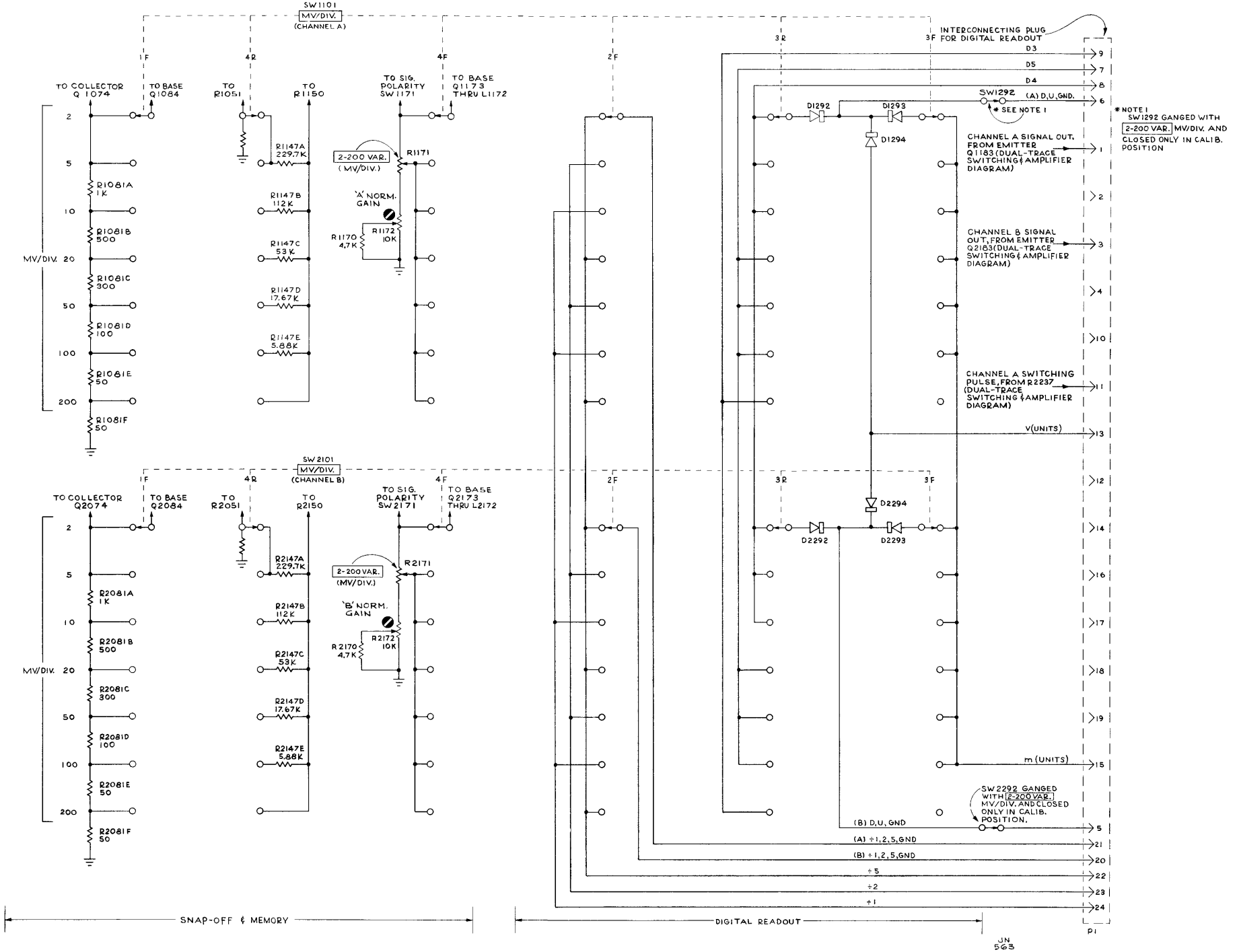
MRH
563

TYPE 3S76 PLUG-IN UNIT

A1

CHANNEL A & B AMPLIFIERS


DUAL-TRACE SWITCHING MULTIVIBRATOR
COMMON OUTPUT AMPLIFIER
Q2230
Q2255
Q2245
V1224A ½6DJ8
V1224B ½6DJ8
Q1204
Q1214
Q1223
V2214 6CW4
V2289 ZZ1000
Q2287
Q2297
Q2277
Q2274
SW2190
VERTICAL MODE SWITCH
CONCENTRIC WITH SW1080, SMOOTH - NORMAL SWITCH (SEE SNAP-OFF & MEMORY)
A VERT. B HORIZ.
A ONLY
DUAL-TRACE B ONLY
A + B
PULSE FROM D 2021 (SNAP-OFF & MEMORY DIAG.)
DUAL-TRACE +0.1V 0V - A ONLY OR B ONLY
DUAL-TRACE -12V
BLANKING PULSE FROM MEMORY GATE DRIVER (SNAP-OFF & MEMORY DIAG.)
TO R1186 (CHANNEL A AMPLIFIER DIAG.)
TO R2186 (CHANNEL B AMPLIFIER DIAG.)
INTERNAL TRIG. SIG. FROM SW1004 (SNAP-OFF MEMORY DIAGRAM)
TO HTRS. OF V1224 & V2214
6.3V
PULSE TO C2019 SNAP-OFF DRIVER (SEE SNAP-OFF MEMORY DIAG.)
GAIN ADJ.
PROBE POWER
INDICATOR UNIT INTERCONNECTING PLUG
P11
B ONLY -.24V DUAL-TRACE -7.5V A ONLY -9 V
B ONLY -9V DUAL-TRACE -7.5V A ONLY -.24V
B ONLY -0.4V DUAL-TRACE +10 V A ONLY +20 V
B ONLY +20V DUAL-TRACE +10V A ONLY -0.4V
1V/DIV
10 μ SEC/DIV
20 V/DIV
10μ SEC/DIV.
+60V
+100V TO SAMPLER BRIDGES R1060 & R2060
+300V
+180V
+125V
+20V
+10V
-12.2V
-100V
30 ma
35 ma
72 ma
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
* PINS ON CONNECTOR TO DIGITAL READOUT. FOR ADDITIONAL DETAILS SEE ATTENUATOR SW DIAG.
SEE CHANNEL A & B AMPLIFIERS DIAGRAM FOR IMPORTANT NOTE & CONDITIONS.
SEE PARTS LIST FOR EARLIER VALUES AND S/N CHANGES OF PARTS MARKED WITH BLUE OUTLINE
MRH 1265


SW1101
MV/DIV.
(CHANNEL A)
1F
4R
4F
2F
3R
3F
TO COLLECTOR Q 1074
TO BASE Q1084
TO R1051
TO R1150
TO SIG. POLARITY SW1171
TO BASE Q1173 THRU L1172
MV/DIV.
2
5
10
20
50
100
200
R1081A 1K
R1081B 500
R1081C 300
R1081D 100
R1081E 50
R1081F 50
R1147A 229.7K
R1147B 112K
R1147C 53K
R1147D 17.67K
R1147E 5.88K
2-200 VAR. (MV/DIV.)
R1171
'A' NORM. GAIN
R1172 10K
R1170 4.7K
SW2101
MV/DIV.
(CHANNEL B)
TO COLLECTOR Q2074
TO BASE Q2084
TO R2051
TO R2150
TO SIG. POLARITY SW2171
TO BASE Q2173 THRU L2172
R2081A 1K
R2081B 500
R2081C 300
R2081D 100
R2081E 50
R2081F 50
R2147A 229.7K
R2147B 112K
R2147C 53K
R2147D 17.67K
R2147E 5.88K
2-200 VAR. (MV/DIV.)
R2171
'B' NORM. GAIN
R2172 10K
R2170 4.7K
INTERCONNECTING PLUG FOR DIGITAL READOUT
D3
D5
D4
SW1292
(A) D,U,GND.
* SEE NOTE 1
D1292
D1293
D1294
D2292
D2293
D2294
CHANNEL A SIGNAL OUT, FROM EMITTER Q1183 (DUAL-TRACE SWITCHING & AMPLIFIER DIAGRAM)
CHANNEL B SIGNAL OUT, FROM EMITTER Q2183 (DUAL-TRACE SWITCHING & AMPLIFIER DIAGRAM)
CHANNEL A SWITCHING PULSE, FROM R2237 (DUAL-TRACE SWITCHING & AMPLIFIER DIAGRAM)
V(UNITS)
m (UNITS)
SW 2292 GANGED WITH 2-200 VAR. MV/DIV. AND CLOSED ONLY IN CALIB. POSITION.
(B) D,U, GND
(A) ÷1,2,5,GND
(B) ÷1,2,5,GND
÷5
÷2
÷1
* NOTE 1
SW1292 GANGED WITH 2-200 VAR. MV/DIV. AND CLOSED ONLY IN CALIB. POSITION
9
7
8
6
1
2
3
4
10
11
13
12
14
16
17
18
19
15
5
21
20
22
23
24
P1
SNAP-OFF & MEMORY
DIGITAL READOUT
JN 563

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages. If it does not, your manual is correct as printed.

TEXT CORRECTION

The following should replace paragraph (1) and (2) under 'Checks to Make'

of the Troubleshooting Chart on page 5-4.

1. Apply a 20-nsec, 1-volt pulse from the pulse generator to the Type 3S76 INPUT A connector. With the test oscilloscope, check for a 1-volt, peak, pulse at pin 4 of P11. (P11 is the top interconnecting plug).

2. Set the INTERNAL TRIGGER switch to B and apply the pulse generator output to the INPUT B connector. With the test oscilloscope, check for a 1-volt, peak, pulse at pin 4 of P11.

Page 1-1, Column 2:

Under "Vertical Signal Output," the last sentence should read, "Open-circuit output voltage swing is about +5 to +15 volts."

Page 6-1, Column 2:

Item 17 of the Equipment Required list should be a 330-ohm 1/2-watt resistor (10% or 20% tolerance). Tektronix Part Number 302-0331-00.

Under "Preliminary Procedure," the Type 3T77 front-panel TRIGGER SENSITIVITY control should be set fully counterclockwise instead of fully clockwise.

Page 6-2, Column 1:

Under "Snap-Off Blocking Oscillator Check," turn the Type 3T77 TRIGGER SENSITIVITY control fully clockwise before step 1. In step 1, add "Test point (4) is the collector of Q2010."

Under "Blanking Amplifier Check," in step 2 set the test oscilloscope sweep rate to 10 μsec/cm.

Page 6-4, Column 1:

Under "A NORM GAIN Adjustment," replace Fig. 6-5 with the following.

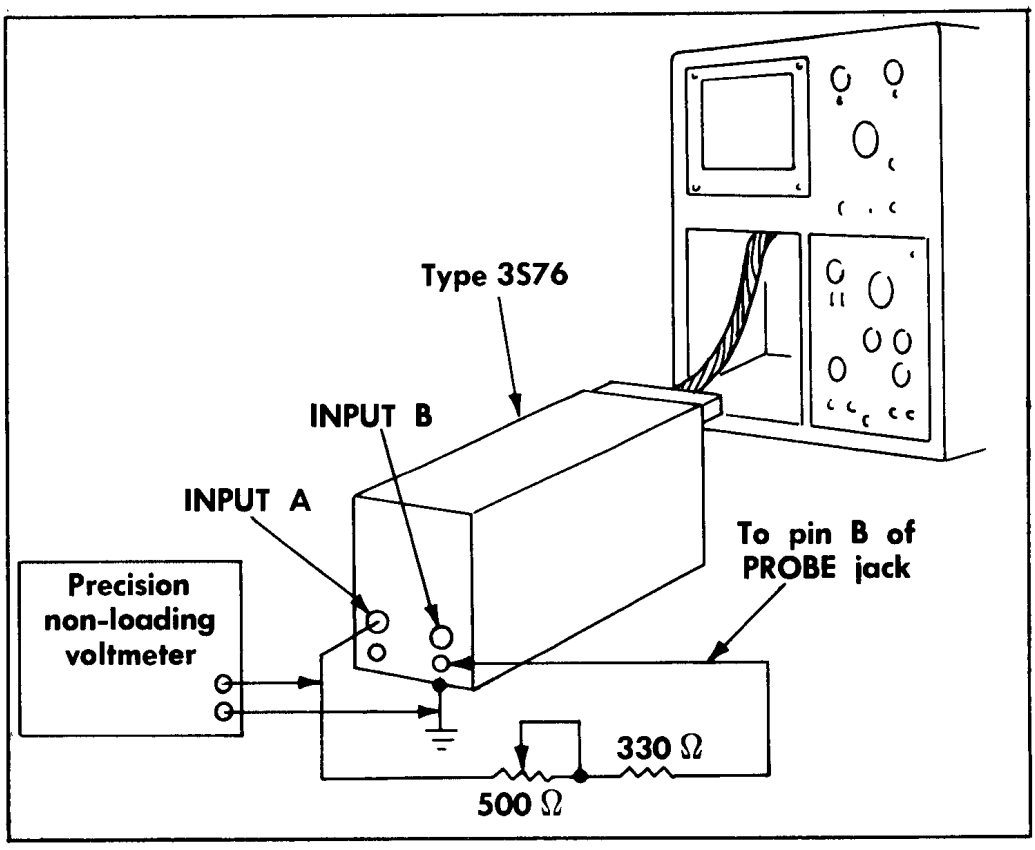


Fig. 6-5. Circuit used to set Type 3S76 gain.

Page 6-5, Column 2:

Under "A BRIDGE BAL Adjustment," add the following at the end of step 2: "Leave the channel A MV/DIV switch set to the 10 position."

Under "B BRIDGE BAL Adjustment," add the following at the end of step 1: "Leave the channel B MV/DIV switch set to the 10 position.

Page 6-7, Column 1:

Under "Memory Drift Check," change step 4 to read:

4. Set the output frequency of the Type 105 Square-Wave Generator to 10 kc and adjust the output amplitude for about 5 divisions of deflection.

Also under "Memory Drift Check," change the first sentence of step 6 to read:

6. Set the Type 105 output frequency to 30 cycles then check the display for the amount of vertical elongation of the dots (memory drift).

Page 6-7, Column 2:

Under "Lissajous Check," step 4, set the TIME/DIV switch to 5 nSEC instead of 50 nSEC.

TYPE 3S76 TENT SN 3500

PARTS LIST CORRECTION

CHANGE TO:

Q2230	151-0188-00	Silicon	2N3906	
R2226	301-0222-00	2.2 kΩ	1/2 W	5%
R2227	301-0563-00	56 kΩ	1/2 W	5%

TYPE 3S76 TENT SN 3390

PARTS LIST CORRECTION

CHANGE TO:

R1147B	318-0006-00	111 kΩ	1/8 W	1%
R2147B	318-0006-00	111 kΩ	1/8 W	1%