INSTRUCTION MANUAL

Serial Number _____

TYPE 3T2 RANDOM SAMPLING SWEEP

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070-0631-00

7-67


TYPE 3T2 RANDOM SAMPLING SWEEP
TIME POSITION
FINE
TIME /DIV
HORIZ POSITION
SAMPLES/DIV
RANGE
START POINT
WITH TRIGGER
TIME MAGNIFIER
CAL
VARIABLE
BEFORE TRIGGER
DISPLAY MAG
X1
X10
100µs
10µs
1µs
1 ms
100 ns
X5
X10
X2
X20
X1
X50
LOW REP RATE
HORIZ GAIN
DISPLAY MODE
EXT HORIZ ATTEN
MANUAL SCAN
MANUAL
NORMAL
EXT HORIZ
SINGLE SWP
START
TRIG SENSITIVITY
RECOVERY TIME
POLARITY
+
–
SOURCE
INT
EXT
TRIGGER INPUTS
50Ω
10–250 mV
5V MAX
1MΩ / UHF SYNC
PULSE OUT
≈150 mV
INTO 50Ω
SWP OUT
1V/DIV (10KΩ)
SERIAL
EXT HORIZ INPUT
150V MAX
10–500 mV
100V MAX
TEKTRONIX
ORTLAND, OREGON, U. S. A.

SECTION 1

CHARACTERISTICS

Introduction

The Tektronix Type 3T2 Random Sampling Sweep plug-in unit is a wide range sampling time base designed to provide high speed displays with vertical units that have no signal delay following the trigger take-off point. It will operate in any of the Tektronix 560 Series oscilloscopes except the Type 560 and the Type 561. (It will operate in the Type 561A.) The Type 3T2 provides all the horizontal information needed for time measurements by either Tektronix digital readout system, the Type 567-Type 6R1A, or the Type 568-Type 230.

The Type 3T2 Random Sampling Sweep unit is designed to operate within the Type 561A, RM561A, 564, RM564, 567, RM567, 568 and R568 Oscilloscope main frames, and with the following Tektronix equipment.

Type 3S1, 3S3, or other 3-Series vertical sampling units.

Type 230, 6R1A, and some 6R1 Digital Units, (see below).

Digital readout is available only when the Type 3T2 is operated in a Type 567, RM567, 568 or R568 Oscilloscope main frame.

Controlled Sequence Random Sampling operation is the main feature of the Type 3T2. The sampling process may be changed from random to conventional by one switch (the START POINT switch). Conventional process sampling requires either a vertical unit signal delay after trigger take-off or an external pretrigger signal to the Type 3T2 in order to display the signal point at which triggering occurs. Random process sampling permits the display to start in advance of the triggering event, thus allowing the signal time region to be displayed both before and after the related triggering event.

Critical analysis of low repetition rate signals is possible through the use of either storage oscilloscope or a photograph. Storage displays are obtained by using the Type 3T2 in a Type 564 or RM564 Storage Oscilloscope. Permanent record photographs of CRT displays are possible with any one of several Tektronix Oscilloscope cameras.

ELECTRICAL CHARACTERISTICS

Digital Unit Compatability

The Type 3T2 Random Sampling Sweep unit is compatible for operation with all Type 230 Digital Units and all Type 6R1A Digital Units. It is compatible with all Type 6R1 Digital Units SN 695 and up. Type 6R1 Digital Units SN 101-694 (with exceptions beginning at SN 391) require the installation of Tektronix Modification Kit 040-0342-00 when operated with a Type 3T2. See your Tektronix Field Engineer for details.

The Type 3T2 will perform within all specifications when operated with a Type 6R1A in a Type 567 SN 300-up, or in a Type RM567 SN 130-up. This applies only if the Type 3T2 is operated in a calibrated system. Prime requirement of the oscilloscope power supplies is that all adjustable supplies be within 1% of stated values. If using sampling with the Type 567 and Type RM567, it is best to adjust low-voltage supplies to within 0.5%. If the Type 3T2 is to be operated in earlier 567 oscilloscopes, it is necessary to install Field Modification Kit 040-0319-00. Individually purchased Type 3T2 units (not calibrated in a system at the factory) require calibration in the system into which it is placed if operated with a Type 6R1, and/or in a Type 567 SN 299 or below or a Type RM567 SN 129 or below. Perform the following steps of the Calibration Procedure at the back of this manual: steps 14, 19 and 20.

The following characteristics apply over an ambient temperature range of 0° C to +50° C. These characteristics apply only after the Type 3T2 has been properly mated to the oscilloscope and after suitable warm-up time. For prescribed warm-up time in a particular system, refer to the Main Frame oscilloscope Instruction Manual. A procedure for mating the Type 3T2 to each oscilloscope can be found in the Operating Instructions section of this manual.

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
TRIGGERING		
NOTE **In the following trigger section, the amplitudes listed following the Sensitivity Range title, are those in which the TRIG SENSITIVITY control permits triggering at the low amplitude value, and allows the control to hold off the trigger circuits for signals up to the high amplitude value. However, satisfactory triggering can be obtained for most signals at amplitudes up to the maximum permitted:—±5 V External 50 Ω, ±2 V Internal and ±100 V External 1 MΩ/UHF SYNC.**		
Sine wave Triggering Internal		Trigger signal amplitude may have to be adjusted for minimum display jitter, depending upon frequency and RECOVERY TIME control. Minimum display jitter may not meet jitter limits stated below if triggering frequency is other than 30 MHz.
Frequency Range	100 kHz to 500 MHz	
Sensitivity Range	(3S1) 80 mV to 2.00 V P-P at vert input. (3S76) 50 mV to 1.25 V P-P at vert input.	

ELECTRICAL CHARACTERISTICS (cont)

Characteristic	Performance Requirement	Supplemental Information
Sine Wave Triggering (cont)		
External		
50 Ω Input		
Frequency Range	100 kHz to 500 MHz	
Sensitivity Range	10 mV to 250 mV P-P	
1 MΩ/UHF SYNC Input		
Frequency Range		
+ POLARITY	10 kHz to 100 MHz, triggered. 500 MHz to 3 GHz, UHF SYNC.	UHF SYNC displays may be affected by the POLARITY switch. Check both positions of the POLARITY switch for best UHF SYNC displays.
— POLARITY	100 kHz to 100 MHz, triggered. 500 MHz to 3 GHz, UHF Sync.	
Sensitivity Range	10 mV to 500 mV P-P	
Pulse Triggering		Trigger signal amplitude may have to be adjusted for minimum display jitter, depending upon pulse rise rate, repetition rate and RECOVERY TIME control.
Internal		
Repetition Rate Range	10 Hz to 600 MHz	
Sensitivity Range	(3S1) 80 mV to 1.00 V P-P at vert input. (3S76) 50 mV to 625 mV P-P at vert input.	Applies for pulses of 10 Hz to 100 kHz and low duty factor above 100 kHz. As duty factor approaches 50% (above 100 kHz), maximum amplitude that TRIG SENSITIVITY control can hold off increases to: (3S76) 1.25 V P-P and (3S1) 2.00 V P-P.
External		Trigger signal amplitude may have to be adjusted for minimum display jitter, depending upon pulse rise rate, repetition rate and RECOVERY TIME control.
50 Ω Input		
Repetition Rate Range	10 Hz to 600 MHz	
Sensitivity Range	5 mV to 125 mV	Applies for pulses of 10 Hz to 100 kHz and low duty factor pulses above 100 kHz. As duty factor approaches 50% (above 100 kHz), maximum amplitude that TRIG SENSITIVITY control can hold off increases to 250 mV P-P.
1 MΩ/UHF SYNC		
Input		
Repetition Rate Range	10 Hz to 100 MHz, triggered. 600 MHz to 3 GHz, UHF SYNC.	
Sensitivity Range	10 mV to 250 mV	As duty factor approaches 50% (above 10 kHz), maximum amplitude increases to 500 mV.
Trigger Jitter		
Sinewave		Sine wave display jitter is checked with START POINT switch at WITH TRIGGER only.
Internal	(3S1) $\leq$200 ps when signal is 900 mV P-P at 30 MHz. (3S76) $\leq$200 ps when signal is 500 mV P-P at 30 MHz.	
External		External limits checked for best (least) jitter at + and — POLARITY. Limits valid for one polarity, but not necessarily both polarities.
50 Ω Input	$\leq$200 ps when signal is 100 mV P-P at 30 MHz.	
1 MΩ/UHF SYNC	$\leq$50 ps when signal is 100 mV P-P at 1 GHz.	
Pulse		
Internal		
With Trigger	(3S1) $\leq$30 ps when pulse is 400 mV, 2 ns duration. (3S76) $\leq$30 ps when pulse is 250 mV, 2 ns duration.	

ELECTRICAL CHARACTERISTICS (cont)

Characteristic	Performance Requirement	Supplemental Information
Pulse (cont)		
Before Trigger	(3S1) ≤50 ps when pulse is 400 mV, 2 ns duration. (3S76) ≤50 ps when pulse is 250 mV, 2 ns duration.	
External (50 Ω Input)		
With Trigger	30 ps or less trigger jitter with 50 mV, 2 ns duration pulse. 2 ps or less trigger jitter with 150 mV, 2 ns duration pulse.	
Before Trigger	50 ps or less trigger jitter with 50 mV, 2 ns duration pulse.	
Minimum trigger repetition rate in BEFORE TRIGGER operating mode		
RANGE		
1 ms and 100 μs	10 Hz	LOW REP RATE light turns on and sweep stops when trigger signal is below these limits.
10 μs	100 Hz	
1 μs	1 kHz	
100 ns	10 kHz	
Minimum trigger signal rise rate.	150 mV/μs.	Applies for External 50 Ω input and Internal triggering, — POLARITY only.
Maximum input voltage to external trigger input connectors.		
50 Ω Input		±5 V.
1 MΩ/UHF SYNC Input		±100 V.

HORIZONTAL DEFLECTION SYSTEM

Timing Accuracy		Limits apply after adjustment of front panel HORIZ GAIN control. See Step 9 of the Calibration procedure in this manual.
DISPLAY mag SW: ×1	±3% (±5% on 100 ns Range when TIME MAGNIFIER is at ×5 through ×50.)	
DISPLAY mag SW: ×10	±5% (±7% on 100 ns Range when TIME MAGNIFIER is at ×5 through ×50.)	Measured in graticule center eight divisions and excluding first part of sweep as listed below under RANGE Exclusion.
RANGE Exclusion	Range beginning which is non-linear; above timing tolerances do not apply.	
1 ms	First 15 μs. (1.5% of Range)	Displayed sweep is fully within limits when TIME POSITION controls position non-linear region to left of time window, off the CRT.
100 μs	First 1.5 μs. (1.5% of Range)	
10 μs	First 150 ns. (1.5% of Range)	
1 μs	First 15 ns. (1.5% of Range)	
100 nS	First 10 ns. (10% of Range)	
EXT. HORIZ INPUT Deflection Factor	Adjusted by HORIZ GAIN control to 1.5 V/Div, ±3%.	
MANUAL SCAN Range	Adjusted by HORIZ GAIN control to be 10 divisions.	
Time Magnifier VARIABLE Range	2.5:1	Fully clockwise, fastest sweep rate is approximately 80 ps/div.
SWP OUT Connector signal (SN B080970-up)	1 V/Div, ±5% (through 10 kΩ) 1× MAG 0.1 V/Div, ±5% (through 10 kΩ) 10× MAG	
SWP OUT Connector signal (SN B010100-B070969)	1 V/Div, ±5%	Through 10 kΩ

ENVIRONMENTAL CHARACTERISTICS

Storage

Temperature— −40°C to +65°C.

Altitude—To 50,000 feet.

Operating

Operating Temperature— 0°C to +50°C.

Operating Altitude—To 15,000 feet.

MECHANICAL CHARACTERISTICS

Dimensions—	Height	$6\frac{5}{16}$ inches.	Approximate dimensions including knobs and connectors.
	Width	$4\frac{5}{16}$ inches.	
	Length	$14\frac{1}{4}$ inches.	

Construction— Aluminum alloy chassis with epoxy laminated circuit boards.
Front panel is anodized aluminum.

Accessories— An illustrated list of the accessories with the Type 3T2 is at the end of the Mechanical Parts List pullout pages.

NOTES

SECTION 2
PRINCIPLES OF TYPE 3T2 RANDOM PROCESS SAMPLING

NOTE

A glossary of terms can be found at the end of this section of the manual.

General

The Type 3T2 Random Sampling Sweep unit has two basic modes of operation. The chief difference between them is that one mode constructs the equivalent time sampling display by a conventional process, where the triggering event itself cannot be fully displayed without the use of a second delay line or a pretrigger. Since it is more desirable to view the triggering event fully by somehow starting the sweep early, or by delaying the vertical signal, a second mode of operation is included in the Type 3T2. The second mode can randomly sample the signal time region both before and after the triggering event; so the triggering event itself can be conveniently displayed on the CRT. A fixed range of the signal time region can be viewed by either mode, except that the second (random) process allows the time region range to be positioned to include information before, as well as after, the triggering event. Time positioning of the sampled time region is referred to as the positioning of a time window.

When the Type 3T2 is producing a display by the conventional process, the time window can be positioned to start with (or within a few nanoseconds after, but not before) trigger recognition. When the Type 3T2 is randomly sampling before and after the triggering event, the time window can be positioned to start before trigger recognition. The front panel Time Position Range START POINT switch selects the operating process (WITH TRIGGER or BEFORE TRIGGER) for the Type 3T2. Random sampling permits viewing the triggering event without the use of a vertical-channel delay line or a pretrigger signal. The conventional process sampling circuits are included in the Type 3T2 for operating with very low repetition rate signals that cannot be displayed by random circuitry, and for displaying signals when smoothing must be used in the vertical unit.

The following Logic Description defines conventional-process and random-process sampling within the Type 3T2 by the use of block diagrams and time-ladder waveforms.

Sweep Generation

Sweep generation within the Type 3T2 is different for the two modes of operation. Operation with the START POINT switch at WITH TRIGGER causes the sweep to be driven by a staircase signal. Operation with the START POINT switch at BEFORE TRIGGER causes the sweep to be driven by the output of the horizontal memory, whose DC voltage is determined by a series of ramps interrupted at different amplitudes. Each different ramp amplitude corresponds to a different horizontal dot position on the CRT screen. The two generalized forms of sweep generation signals are shown in the drawings of Fig. 2-1.

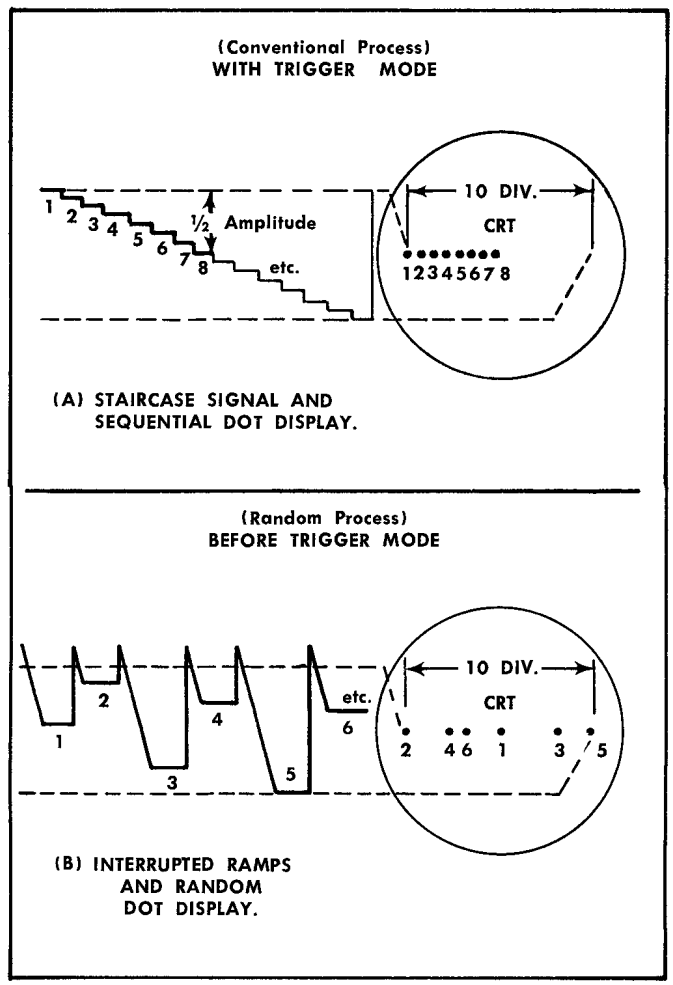


Fig. 2-1. Comparison of CRT horizontal dot display of staircase and interrupted ramps.

Fig. 2-1A is a negative-going staircase signal where each fixed voltage level corresponds to a fixed CRT dot position. The CRT is blanked off during the time the staircase is stepping.

Fig. 2-1B is of a series of negative-going ramp signals each stopped for a definite time. Each fixed voltage level of each interrupted ramp corresponds to a fixed CRT dot postion. The CRT is blanked off when a sample is taken, and unblanked after the horizontal memory is repositioned.

With Trigger Mode (Conventional Sampling Process)

The conventional sampling process (the with-trigger mode) is shown in basic form in Fig. 2-2. The waveforms represent just two samples in a sequence, such as the fifth and sixth dots of a many-dot display. Each waveform is identified with its block or interconnections in the adjacent block diagram.

The trigger regenerator circuit is the master programmer of Fig. 2-2. It delivers a negative step pulse at the time of trigger recognition, T_o, to start the process that takes and displays one sample. Immediately after T_o the trigger circuits lock out any more triggers until the rest of the circuits have operated and the dot has been properly displayed. (The period of time during which triggers are locked out is called the holdoff time, and is made variable by the Type 3T2 front panel RECOVERY TIME control. See the Operating Instructions for RECOVERY TIME control uses.)

At T_o, the trigger circuit starts the timing ramp running in a negative direction. The timing ramp "times" the occurrence of the strobe drive pulse sent to the vertical sampling unit

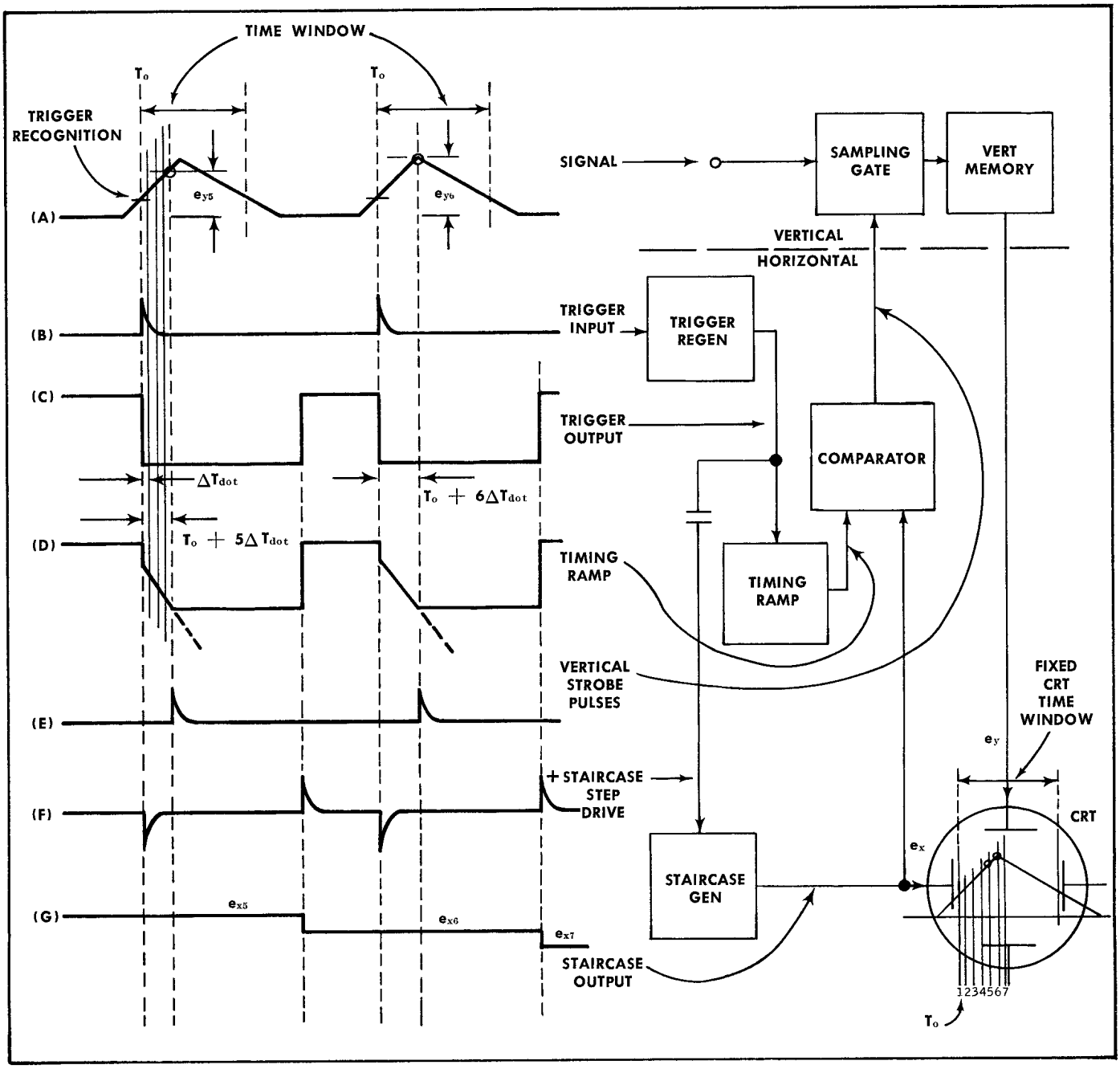


Fig. 2-2. Basic "with trigger" mode sequential sampling oscilloscope.

as the timing ramp is compared with the voltage of the staircase generator in the comparator block. Since the staircase output signal voltage is different for each trigger circuit output pulse, the timing ramp is allowed to run down farther for each successive sample. The result is a time "slewing" of successive sampling times. The slewing increment is identified in Fig. 2-2 as ΔT_{dot} and is a fixed time increment per sample. ΔT_{dot} is set by both the timing ramp slope and the staircase step amplitude.

The waveforms of Fig. 2-2 imply that there can be a CRT dot displayed from the time of the vertical strobe pulse to the time of the timing ramp reset. Actually the CRT blanking is also controlled by the vertical sampling unit. The vertical unit prevents CRT beam current at the time of the vertical strobe pulse and until the vertical memory is stable, typically for 2 to 3 μs.

Adding Sweep Rate and Movable Time Window Controls

The Time window (sampled signal time domain) identified in Fig. 2-2 can be moved so that a different portion of

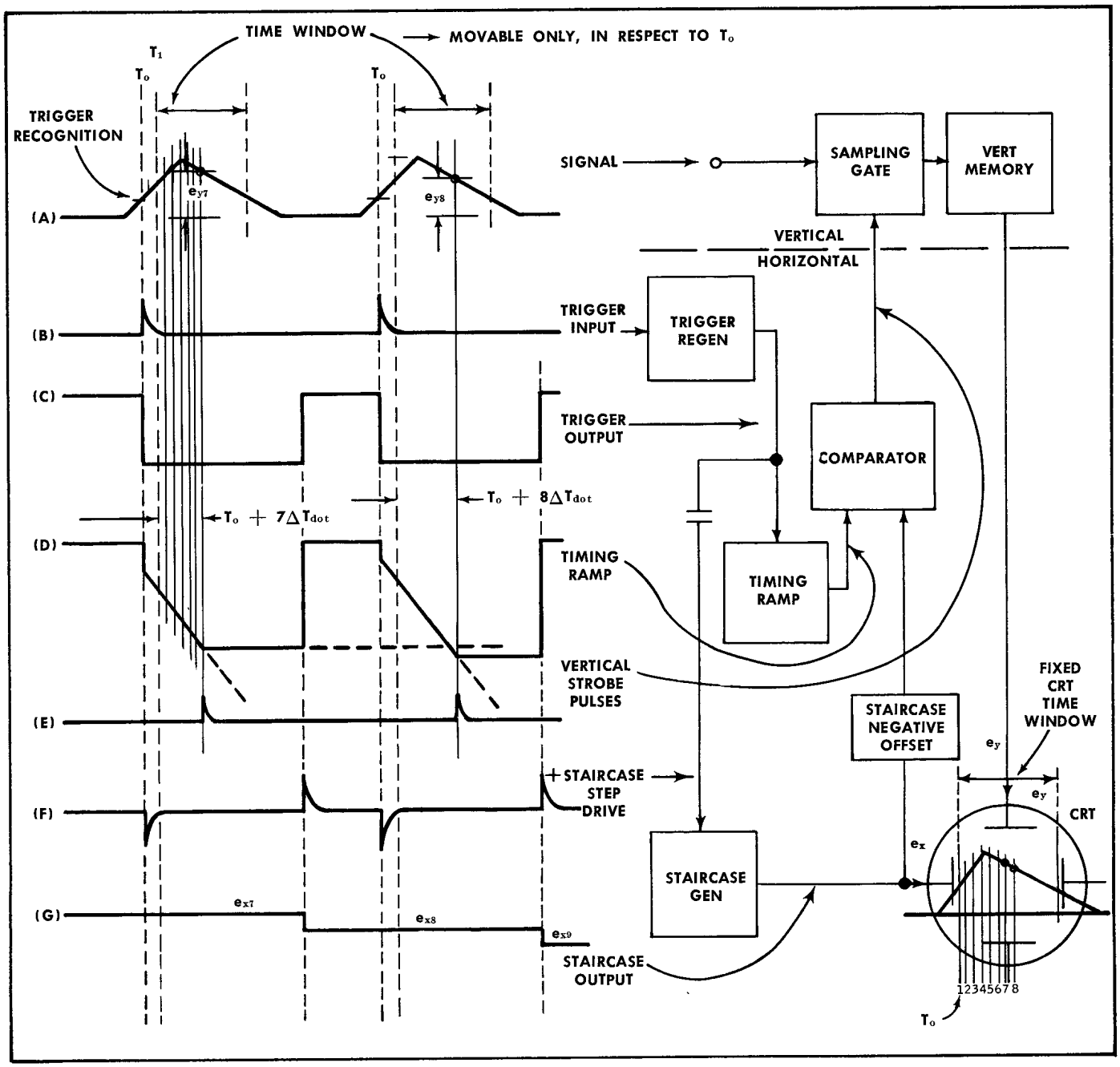


Fig. 2-3. Adding a Time Position control to basic block of Fig. 2-2.

the signal is displayed. Fig. 2-3 shows a Time Position control added between the Staircase Gen block and the comparator block. This new circuit allows a negative DC voltage offset to be applied to the staircase signal that is compared with the timing ramp signal. Since the comparator block is a DC coupled comparator, changing the DC level of the staircase signal in a negative direction causes the timing ramp signal to travel farther negative before comparison occurs. Since the timing ramp signal is a ramp, the more negative comparison results in a later comparison and later vertical strobe pulses than before the staircase signal was offset.

The staircase signal sent to the CRT is not altered; thus, the voltages that set the CRT dot positions are not changed, the first dot occurring at the CRT left side. If the Time Position control applies a negative offset to the staircase signal that feeds the comparator block, the first displayed dot at the CRT left side will have a vertical voltage related to the signal amplitude at time T_1 (see Fig. 2-3 upper left). The result is an apparent horizontal shift of the displayed signal to the left. The circuits of the Type 3T2 allow only a negative offset to be applied to the staircase signal, thus permitting the movable time window to include only portions of the signal AFTER trigger recognition time, T_o.

Fig. 2-3 does not show any method that will alter the equivalent time sweep rate. Three different controls are used to alter the Type 3T2 sweep rate. One is the Range control that alters the slope of the Timing Ramp; another is the Time Magnifier control that alters the amplitude of the staircase signal sent to the Comparator block. The third method is a Display Magnifier which changes the horizontal amplifier gain.

To decrease the rate of fall $\frac{dV}{dt}$ of the timing ramp is to increase the time assigned to ΔT_{dot} (ΔT_{dot} is the equivalent time between dots). Since the staircase signal to the CRT is not altered and the real time presentation of dots is not altered, increasing ΔT makes the display have a slower equivalent time sweep rate (more time per CRT division). A slower sweep rate will allow a longer period of the input signal to be displayed.

To increase the rate of fall of the timing ramp is to speed up the equivalent time sweep rate. The Type 3T2 RANGE control changes the timing ramp rundown rate. (It also alters the trigger circuit holdoff time to avoid display confusion, so the trigger circuits don't recognize the input signal until after the dot has been properly displayed.)

To reduce the amplitude of the staircase signal sent to the Comparator block is to reduce the time assigned to ΔT_{dot}. Since the staircase signal to the CRT is not altered, and the real time presentation of dots is not altered, reducing ΔT_{dot} makes the display have a shorter equivalent time sweep rate (less time per CRT division). The Type 3T2 TIME MAGNIFIER control attenuates the staircase signal (when at other than at $\times 1$) that is sent to the Comparator block.

Manual Scan

The above description of "With Trigger" operation is complete so far as a continuously running sweep display is concerned. The Type 3T2 front panel DISPLAY MODE switch must be at its NORMAL position for the system to function as described. If the DISPLAY MODE switch is placed at MANUAL SCAN, the operator can manually control the horizontal position and rate of movement of the sampling dot, even leaving the dot at a fixed position. Manual Scan operation substitutes a manually variable DC voltage for the staircase signal. The manually variable voltage has the same limits as the staircase signal so that with the MANUAL SCAN control fully counterclockwise, the sampling dot position is at the CRT display left end. With the MANUAL SCAN control fully clockwise, the sampling dot position is at the CRT display right end.

During manual scan operation, Comparator block input signals are the timing ramp and the variable DC voltage. If the variable DC (manual scan) voltage is left at a fixed value, the Comparator block sends a strobe pulse to the vertical sampling unit at a constant interval after each T_o. There is no ΔT_{dot}, and therefore no slewing of the strobe drive in relation to T_o.

Moving the MANUAL SCAN control changes both the voltage level along the timing ramp signal and the voltage sent to the CRT. Since the trigger circuits function exactly as they do during NORMAL scan operation, the operator can now position the dot along the display at a rate to suit his convenience.

External Horizontal Scan

The Type 3T2 DISPLAY MODE switch permits an externally generated variable voltage to scan the sampled display when the switch is placed at its EXT HORIZ position. The external voltage is applied to the comparator block and to the CRT in the same manner as the Manual Scan voltage is applied. Thus, the external voltage can move the CRT dot along the triggered display. Some Y-T recorders can supply a potentiometrically derived voltage corresponding to the T-coordinate of the stylus.

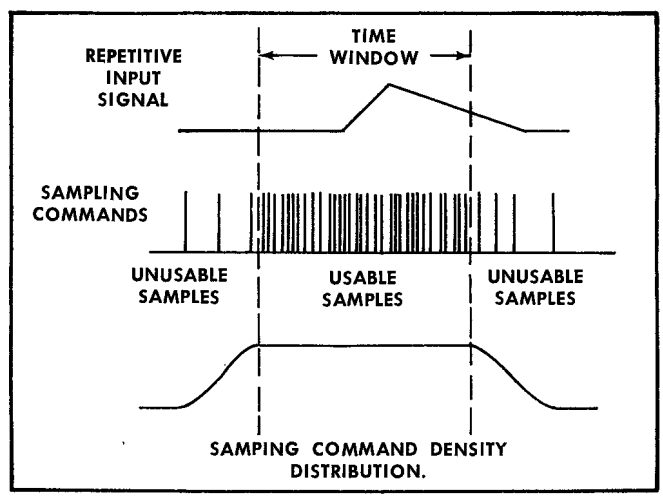


Fig. 2-4. Distribution of random samples related to repetitive input signal and CRT time window.

Before Trigger Mode (Random Sampling Process)

The "Before Trigger" mode or Random process of sampling by the Type 3T2 Random Sampling Sweep unit may be described as a system that produces a CRT display by a series of dots that are usually displayed in a nearly se-

quential manner from left to right. The dots are presented from left to right with a small region of randomness visible at very slow sweep rates. At fast sweep rates, or when the signal repetition rate is jittery, the display either appears to sparkle, or looks like a normal oscilloscope display.

The circuit processes of random sampling differ from both normal oscilloscope sweeps and conventional sampling oscilloscope sweeps. The processes of a random sampler are divided into two parts: timing the samples to fall somewhere within the CRT time window, and construction of a meaningful display from a series of randomly determined samples. The following description begins with a basic random sampling system and then deals directly with the controlled sequence circuit logic within the Type 3T2.

A Basic Random Equivalent-Time System

Fig. 2-4 shows how random samples may be distributed in relation to a triggering event, then how most of the samples are considered usable. Those samples considered usable are presented in the CRT display time window, and those considered not useful are eliminated by blanking of the CRT. The sampling density distribution shown applies to the Type 3T2 and is described later with the Ratemeter description.

Deriving the two analog signals that produce the coherent display of randomly taken samples is the second part of the random sampling process.

The "y", or vertical coordinate of a sample is obtained by the same sample-and-hold process used in conventional sampling oscilloscopes. This is accomplished by the vertical part of the system as referred to briefly in Fig. 2-5. The "x", or horizontal coordinate of a sample is obtained differently than in conventional sampling and is shown in basic detail in Fig. 2-5.

Five samples, taken on successive repetitions of the signal, are shown at Fig. 2-5A. Trigger recognition of the signal occurs at T_o and starts a timing ramp running up at Fig. 2-5E.

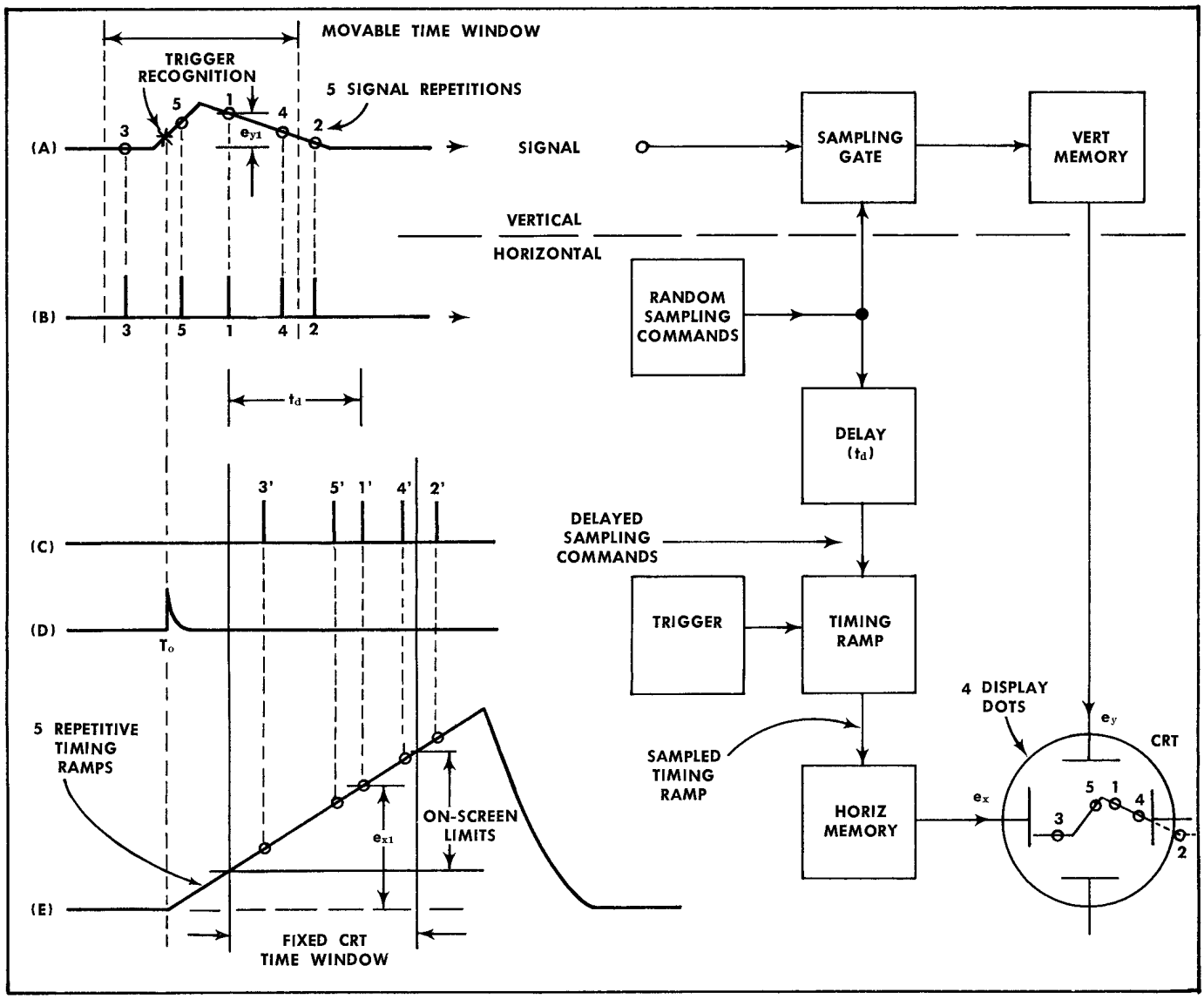


Fig. 2-5. Basic random sampling system derivation of "x" and "y" deflection signals. Signal is repetitive. Sweep rate is "equivalent time".

Each time the vertical input signal is recognized, during or before the timing ramp is started and at some random point the timing ramp, a vertical sample (e_y) is taken. The y-component, e_y, of sample number 1 is held in the vertical Memory, and used to position the CRT spot vertically. The number 1 sampling command (Fig. 2-5B) that takes the first sample is then delayed by a fixed interval t_d, and shown as 1 in Fig. 2-5C. The delayed sampling command samples the timing ramp and places a DC voltage in the horizontal Memory. The resulting "held" sample, e_{x1} is used to position the CRT spot horizontally in agreement with the original horizontal position of sample number 1 in Fig. 2-5A.

By this same process each sample supplies both vertical and horizontal information to deflect the CRT beam from dot to dot to construct a meaningful display of those samples that fall within the time window.

Remembering that the trigger recognition time T_o always starts the timing ramp at the same time with respect to the input signal, an increase in the interval t_d moves the time window to an earlier position along the time axis. Likewise, a decrease in the time interval t_d, moves the time window to a later position along the time axis. The effect is that of a movable time window in relation to the triggering event time T_o. The time window start can be moved to a time earlier than T_o by delaying the sampling commands to the timing ramp, and at the same time causing random sampling commands to occur in advance of T_o. It is through proper time separation of the two groups of sampling commands (Fig. 2-5 B and C) that the CRT display produces an equivalent-time replica of the input signal including information ahead of the trigger recognition time T_o.

A Controlled Sequence Random Process Sampling System

A simplified operational random process sampling system is shown in Fig. 2-6. The system contains a feedback

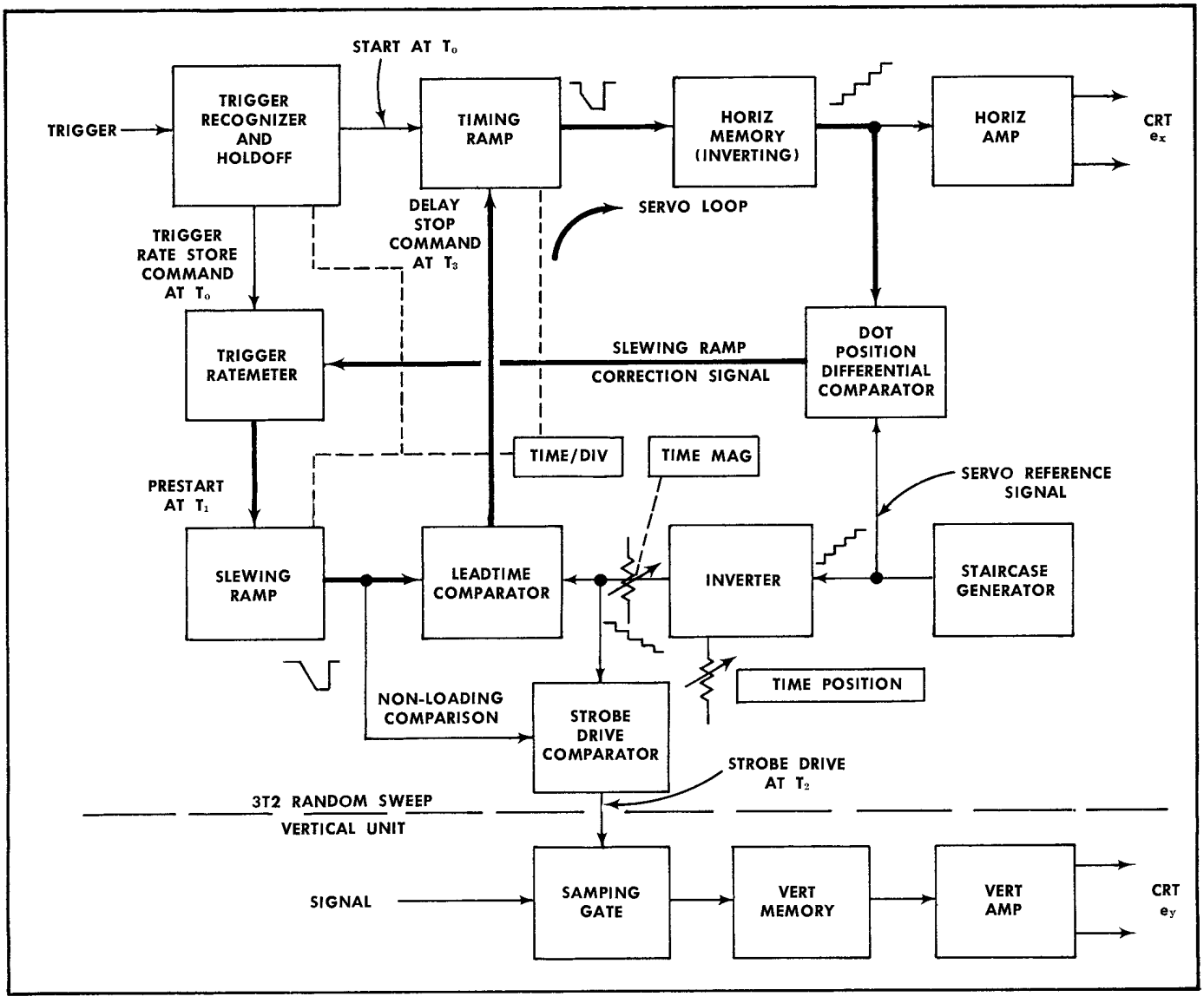


Fig. 2-6. Type 3T2 simplified random sampling process block diagram. See Fig. 3-7 for related waveforms.

loop (Servo Loop) that controls the position of the random distribution of samples across the sampled time window. The blocks belonging to the horizontal portions of the system are those of the Type 3T2 Random Sampling Sweep.

Trigger Recognizer And Holdoff

The Trigger Recognizer And Holdoff block is the master programmer for the horizontal system. This block responds to a suitable trigger signal and immediately starts the Timing Ramp. The holdoff function prevents restarting the Timing Ramp until the whole system has had time to complete its cycle begun at T_o (when the Timing Ramp was started).

Trigger Ratemeter

The Trigger Ratemeter block is fed signals from the Trigger Recognizer And Holdoff circuits so it can measure the repetition rate of the trigger recognitions over a wide range of trigger repetition rates. On the basis of several sequential trigger rate measurements, plus a correcting signal supplied by the Dot Position Comparator, the Trigger Ratemeter then starts the Slewing Ramp **before** the next trigger recognition. The Slewing Ramp prestart command is the ratemeter's "best guess" as to when to start the Slewing Ramp (in advance of the next Timing Ramp) and may contain considerable time uncertainty from sample to sample. However, if the Slewing Ramp is started too late several times, the Dot Position Comparator recognizes the error of the Horiz Memory signal related to the Staircase signal and sends a correction signal to the ratemeter. The correcting signal causes the ratemeter to start the Slewing Ramp earlier for the next few samples.

Slewing Comparisons

The Slewing Ramp is a linear ramp that runs at the same rate as the Timing Ramp. The Slewing Ramp provides its signal to two comparators. One comparator delivers the strobe signal to the vertical unit for setting the CRT dot vertical position. The other comparator then stops the Timing Ramp, thus setting the CRT dot horizontal position. Each comparison occurs when the relatively fast slewing ramp signal reaches each of two different inverted staircase voltages. See Fig. 2-7M and its description below. Successive excursions of the slewing ramp signal find the two inverted staircase voltages at slightly more negative values. The result is that the two comparisons are successively delayed or slewed in time. The delayed stop command to the timing ramp (from the Leadtime Comparator) is generated in a manner similar to the strobe drive pulses (from the Strobe Drive comparator), but a DC offset is added to the inverted staircase signal in the Leadtime Comparator block. Thus the delayed stop commands occur later than the strobe drive pulses by the fixed time interval t_d.

Servo Loop

The closed loop (Servo Loop) causes a random distribution of samples to slew across the time window under control of the Staircase Generator signal. The resulting sampling distribution is shown in Fig. 2-4. If the uncertainty of the Slewing Ramp prestart signal generated by the Trigger Ratemeter block is purely random, then the skirts of the sampling distribution will have a gaussion shape and the central portion within the time window will contain a uniform distribution of samples. The Servo Loop keeps the average sampling density constant over the time window period in spite of trigger repetition rate jitter or ratemeter uncertainty. Construction of a display with the triggering event at center screen (without a pretrigger signal) is thus possible.

Functional Waveforms

Waveforms of Fig. 2-7 apply to both the simplified random process block diagram of Fig. 2-6 and to the functional Type 3T2. The shaded area of Fig. 2-7 is discussed later under the heading "Type 3T2 Time Position Control". Fig. 2-7 waveforms can be helpful at a time of troubleshooting because they were obtained under actual operating conditions. Two general kinds of waveforms are shown in Fig. 2-7; single line type that apply to only two successive samples, and multiple line type that apply to the samples of one whole sweep. For example, waveforms (A) through (K) and (M) apply to only two samples, and waveforms (L), (N), (O) and (P) apply to a full Type 3T2 sweep. The triggering signal had very little jitter. This caused the ratemeter ramp waveform to be identical and stable for both samples shown.

The triggering event is identified at the figure top by the term T_o. The left T_o term and the following T_1, T_2 and T_3 terms all apply to one trigger recognition (one sample). Therefore, the shaded area covers those parts of the figure that do not relate to the first T_o, but rather to a previous T_o that is not shown. The amount of real time included in the CRT equivalent time display is shown at the top of the page at T_o. Obviously that period of real time is presented on the CRT by many dots with an equivalent time sweep rate.

Fig. 2-7 has two columns of waveform identification: on the left, the signal source or circuit element where the test oscilloscope probe was connected. On the right, the name of the function related to particular part of the waveform, and in some cases the relationship of two waveforms or circuits, is stated.

At the time of trigger recognition T_o, the trigger circuits start actions represented by waveforms (B), (F), (G), (H), (I) and (O). These waveforms show; (B) the trigger holdoff time starts; (F) the holdoff circuit delivers a timing ramp start signal; (G) a negative pulse is delivered to the front panel PULSE OUT connector; (H) the ratemeter memory gate is driven to conduction so; (I) the ratemeter memory stores the voltage value of the ratemeter ramp; (O) and the timing ramp starts its rundown.

At the holdoff time half-way point, actions take place that are represented by all the remaining waveforms except (A) and (H). These actions do not all take place simultaneously, but rather in three quick steps. 1)Just before the holdoff waveform reaches its negative turn around point, the horizontal memory is pulsed so it takes a sample of the timing ramp voltage just before the timing ramp resets. 2)About 5 microseconds later, several things happen: a memory circuit is pulsed to memorize the output voltage of the Dot Position Comparator (waveform D), the timing ramp is reset so it can be started at the next T_o (waveforms F and O), the front panel PULSE OUT signal returns positive, the ratemeter ramp is reset for a new trigger rate measurement (waveform I), the ratemeter output drops below —10 volts and thereby resets

the previous slewing ramp (waveforms J, K, L and M), and both the strobe driver and the timing ramp stop-circuit reset (waveforms N and P). 3)About 1 microsecond later the holdoff circuit steps the staircase generator (waveforms D and E) which also steps the inverted staircase signals at the slewing comparators (waveform M).

Slewing Ramp Start Time (T_1)

After the third action at one-half holdoff time, the significant circuit is the ratemeter. (The ratemeter ramp circuit operates without any commands until the next one half holdoff time.) After being reset, the ramp voltage rises positive, discharging the ramp slope capacitor. When it reaches bottom, it resets and starts the trigger rate metering ramp rundown. The ramp is designed to run more negative than shown, so that the system will operate properly on reasonably low repetition rate trigger signals.

Four waveforms, (I), (J), (K) and (L) show that the ratemeter rundown ramp (I) is inverted (J) and sets the slewing ramp start time (K) and (L). The inverted ramp (J) receives a DC offset signal from the Dot Position Comparator block to shift the conduction time of the slewing ramp clamp and the time the slewing ramp starts. The DC offset to the inverted ramp is shown in waveform (J) by dashed lines above and below the inverted ramp. It is the inverted ramp, plus the DC offset signal from the Dot Position Comparator that determine when the slewing ramp starts. This time is identified as T_1. T_1 must occur a fixed time in advance (½ Time Position Range) of the next T_0 in order for the display to properly show the triggering event. If everything is running smoothly (no trigger jitter and no rate meter uncertainity), there will be no Dot Position Comparator correction signal to the inverted ramp at the ratemeter output circuit.

Leadtime

Shortly after T_1, the two slewing comparisons previously mentioned occur. Fig. 2-7M shows the relationship between the slewing ramp signal and the two inverted staircase signals. The first comparison, at T_2, sends a strobe pulse to the vertical channel. The second comparison, at what might be called T_3, stops both the slewing ramp and the timing ramp and sets the timing ramp voltage for the CRT next horizontal dot position.

The voltage difference between the two inverted staircase signals (M) controls the time difference between the two slewing comparisons. The time difference between the two comparisons sets the amount of time that can be displayed in advance of the triggering event. This advance triggering is known as "leadtime".

In a stable operating system triggered on a jitterless trigger signal, the time between each T_0 and its T_1 is fixed. However, the time between T_1 and the sample being taken increases with each successive sample. The time increase between samples is identified as ΔT_{dot} in Fig. 2-2, and is an increment related to the equivalent time sweep rate. ΔT_{dot} is due to each voltage change of the inverted staircase signal at the two slewing comparators. The time between T_1 and T_2 is not dependent upon trigger signal jitter. The time between each T_0 and its T_1 is dependent upon trigger signal jitter.

Time Position Range Controls

Fig. 2-7 timing and slewing ramp waveforms (L and O) include extending dashes at the bottom of the sloping portion. The dashes indicate that the ramps can run farther negative if not stopped by inverted staircase comparison. Each of the two ramps is designed to run for at least twice the time required to display one basic equivalent-time time-window (when the Time Magnifier switch is at ×1). This allows the operator to move the time window beginning over a time region of one range, and to view a maximum of two ranges.

The Type 3T2 front panel RANGE switch positions are labeled with values equal to one time-position range, which is ½ the timing ramp maximum rundown time. With the RANGE switch at 10 μs, for example, the timing ramp must have a rundown time longer than 20 μs. With the TIME MAGNIFIER switch at ×1, the sweep rate is 1 μs/Div. With the two TIME POSITION controls fully clockwise, all slewing comparisons are made from essentially the start to half way down each ramp. With the TIME POSITION controls both fully counterclockwise, the inverted staircase signals are made more negative so that the slewing comparisons are made from essentially halfway down the ramps to their maximum negative values.

The timing and slewing ramp waveforms at the right side of Fig. 2-7 represent conditions when both TIME POSITION controls are fully clockwise. The first set of ramp waveforms (in the shaded area) show comparisons beginning down their slopes as if the TIME POSITION controls were somewhere about midrange. Note the changes in time between T_1 and T_2 for the two different TIME POSITION control conditions.

Time Magnifier Control

When the TIME MAGNIFIER switch is at ×1, all comparisons of one sweep occur over approximately half of the timing and slewing ramps' maximum rundown. This is known as "one time-position range". Thus, the Type 3T2 "time window" will cover an equivalent period of time equal to one Time Position Range. The time window start (leadtime related to the next T_0) will be moved over an equivalent period of time equal to one time position range by the TIME POSITION controls. The Time Position Controls shift the slewing comparisons (waveform M) down the slewing ramp when turned away from their fully clockwise positions.

When the TIME MAGNIFIER is at other than ×1, the step amplitude of the two inverted staircase signals to the slewing comparators is attenuated. With the TIME MAGNIFIER at ×2, for example, the step amplitude is halved, and the displayed time window has an equivalent time one half the time window as with the control at ×1. Now the slewing comparisons use only approximately one quarter of the ramps' rundown amplitude for one equivalent time sweep. The TIME POSITION controls can still move the first comparisons of a sweep half way down the ramps. More attenuation of the inverted staircase signals further reduces the amount of the slewing and timing ramps used for one time window scan.

In each case above, the time difference between each slewing ramp/inverted staircase comparison at T_2, and the associated timing ramp/inverted staircase comparison at

T_3 (T_3 of Fig. 2-7) covers one quarter of the timing ramp maximum rundown, or ½ time position range. This term is abbreviated ½ TPR.

½ TPR is obtained by a DC voltage offset to the inverted staircase signal in the "½ TPR Leadtime Comparator" block. The word "leadtime" refers to the prestart time T_1, ahead of timing ramp comparison, and was referred to in Fig. 2-5 and 2-7 as t_d, a delay time. The circuit action is truly a delay down the slewing ramp from T_1, but the result of this delay as displayed on the CRT is time window **leadtime**, showing information ahead of the triggering event when the TIME POSITION controls are clockwise. The display leadtime, with the Time Position controls both fully clockwise is equal to one half of one "basic" time window (Time Magnifier at ×1) regardless of the Time Magnifier control position.

Samples/Div Control

Related to the previous Time Position Range discussion of staircase signal step amplitude is the number of samples per division or samples per sweep. The Type 3T2 SAMPLES/DIV control alters the staircase generator step amplitude without altering its minimum and maximum voltage values. (The Time Magnifier switch alters both the step amplitude and total staircase amplitude.)

The multiple slewing and timing ramp comparisons drawn in Fig. 2-7 represent very few samples per sweep. Counterclockwise rotation of the SAMPLES/DIV control would cause many more samples to be taken in the same amount of ramp time. (Changing the Time Magnifier would keep the number of samples the same, but use less ramp time for a complete sweep.)

GLOSSARY

CRT Blanking	Turning off the Cathode Ray Tube electrons that strike the phosphor, thus turning off any phosphor light output.
Coherent Display	A plot of a set of dots (samples) in which the time-sequence of signal events thus indicated is preserved.
Equivalent Time	The time scale associated with the display of signal events. An apparant sweep rate visible in the CRT display due to the electronic reconstruction of fast signals on a slower piece-by-piece basis.
Holdoff Time	A period of time during which one circuit prevents another circuit from acting.
Leadtime	That part of a display that occurs prior to the displayed trigger recognition.
Pretrigger	An externally derived triggering signal that is sent to the timing unit external trigger input connector in advance of the rime related vertical input signal.
Ramp	A changing voltage, where the magnitude of change is constant per unit of time.
Random Sampling	A process of signal reconstruction of an equivalent-time coherent display wherein the dots are not necessarily displayed one after the other spacially across the CRT.
Range	A period of time. (See Time Position Range)
Real Time	The time scale associated with the signal events themselves.
Sample	A voltage obtained by electronically looking at a signal for a very short period of time. The voltage is memorized and displayed with correct X and Y voltage coordinates. One dot of a many-dot sampling display.
Sampling Distribution	A function which describes how the density of a large number of randomly placed samples varies across the observed signal time region.
Sampling Command	Otherwise known as a strobe pulse. The command signal that determines when a sample is to be taken.
Servo Loop	A self regulating feedback system that does not have instantaneous response—that part of the Type 3T2 circuits that assures a minimum amount of dot jitter in a display (randomness) created by a system that has significant time uncertainty between the signal being sampled and the sample-taking operation.
Sampling Dot Density	The number of samples per sweep. Dot density is variable over a range from a point where each dot can be distinguished in the display to a number so large that the dots blend together.
Slewing	The process of incrementally delaying successive samples or a set of samples with respect to the signal being sampled.
Staircase	A ramp constructed of many amplitude-stable steps. The slewing increment between steps is equal for normal process sampling, but not necessarily equal for random process sampling.
Strobe	A sampling command voltage applied to the circuit that samples the vertical signal.
t_d	t = time, sub d = delay. A time delay or fixed period between two events.
ΔT_{dot}	The equivalent time between sampling display dots. ΔT_{dot} is equal to the time slewing increment.
Time Magnifier	A control that speeds up the sweep rate without altering the number of dots per sweep.
Time Position Range	The combination of two controls that allow the Time Window start to be positioned over an equivalent period of time equal to one range (the range equivalent time is set by the RANGE control).
Time Window	The amount of time included between the start and end of the CRT display. The equivalent time for ten divisions of horizontal scan; ten times the sweep rate.

Triggering Event	That time at which the trigger circuits respond to the triggering signal.
Trigger Recognition (T_o)	The process of responding to a suitably applied trigger signal. Such response is the time reference for the time window.
Usable Samples	Those samples that fall within the time window.
Unusable Samples	Those samples that do not fall within the time window.

SECTION 4

CIRCUIT DESCRIPTION

General

The circuitry of the Type 3T2 Random Sampling Sweep unit is completely solid state. Major wiring is on etched circuit boards that are interconnected by color coded wires and coaxial cables. Section two describes the unit functions by ladder waveforms and simplified block diagrams. This section of the manual describes individual circuits without emphasis upon interconnections or logic functions. Refer to the diagrams at the back of this manual during the following discussions.

TRIGGER AND HOLDOFF CIRCUITS

The Type 3T2 trigger circuits are all drawn on Diagram 1, the Trigger & Holdoff diagram. Five front panel controls affect the trigger circuit operations. They are the variable TRIG SENSITIVITY and RECOVERY TIME controls, and the POLARITY, SOURCE and RANGE switches. The individual control functions are described in the Operating Instructions section, and below.

Controls

The SOURCE switch selects the triggering signal source (internal or external) by turning on or off appropriate circuits. When the SOURCE switch is placed at EXT, the 1 MΩ to 100 Ω Trigger Amp Q11 and Q12, and the Source Select transistor Q20 are turned on. The internal Source Select transistor Q30 is turned off. When the SOURCE switch is placed at INT, Q30 is on, and Q11, Q12 and Q20 are off.

The POLARITY switch selects one of two common base transistors, Q41 or Q51, to couple the triggering signal from the Source Select circuit to the Trigger Recognizer circuit. When the POLARITY switch is at +, Q41 conducts and passes the triggering signal without inversion. When the POLARITY switch is set at —, Q51 conducts and passes T55 inverted triggering signal to the Trigger Generator.

The TRIG SENSITIVITY control allows the operator to adjust the operating bias of Trigger Recognition tunnel diode D62. The operating bias range is great enough so that the tunnel diode circuit can be made to oscillate, or can be made to require a maximum amplitude triggering signal. Clockwise rotation of the control increases trigger sensitivity until the circuit oscillates. Counterclockwise rotation of the control reduces trigger sensitivity, but will not lock out large amplitude triggering signals.

The RECOVERY TIME control changes the Holdoff Multivibrator period of trigger lockout by changing the holdoff ramp capacitor charging current.

The RANGE control changes the Holdoff Multi holdoff capacitor to assure proper trigger lockout period for each major range of sweep rates.

External Trigger Circuits

Two external input connectors, J1 and J21, offer the option of externally triggering the Type 3T2 with signals from a 50 Ω source or from a high impedance source. The low impedance source signals fed to the 50 Ω input are fed directly into the emitter circuit of common-base amplifier Q20. High impedance source signals are fed to the 1 MΩ/UHF SYNC input and then into an impedance transforming unity gain amplifier (Q11-Q12) that has a bandpass of approximately 100 MHz. The 1 MΩ to 100 Ω non-inverting amplifier couples the signal directly to the emitter of the same non-inverting common-base amplifier used for low input impedance triggering signals.

The collector circuit of the common base amplifier (Q20) is in parallel with the collector circuit of the internal trigger common-base amplifier Q30. Since Q30 is biased to cutoff, its collector circuit does not significantly load Q20 collector, and external signals are properly coupled to the polarity select circuit.

1 MΩ To 100 Ω Trigger Amplifier

External trigger operation is permitted when the SOURCE switch is at EXT. Turn-on bias is applied to Q11 and Q12 by connecting R7 and R18 to —19 volts. Q11 gate lead rests at —9.5 volts due to the voltage division of equal value resistors R5 and R7. The input circuit is AC coupled and an external circuit DC resistance will not change the amplifier input bias and operating point.

Signals into the trigger amplifier pass through a short section of coaxial cable which is looped through a ferrite toroid core three times. The toroid (L1) isolates J1 and J2 ground connections from high frequency ground current signals that could cause false triggering.

Once the signal leaves the cable, it passes through C2, R2 and C5 into Q11 gate. The two diodes, D2 and D3, clamp large input signals to protect the amplifier, and also provide a DC charge path for C2 when a triggering signal source contains DC. R2 limits the changing current of C2 from low impedance signal sources. Thus, the amplifier input impedance is the parallel value of R5 and R7 (1 MΩ) only during times when D2 and D3 are not conducting.

Q11 gate lead input impedance is normally high due to the field effect construction. To assure the high input impedance, Q12 drives Q11 source in phase with the signal. The amplifier can be divided into two parts: Q11 as a source follower (electrically similar to a vacuum tube cathode follower), and Q12 as a bootstrap amplifier driving Q11 source in phase with the signal. Assume a positive signal; Q11 increases conduction, causing its drain lead to go negative. The negative going change at Q11 drain increases Q12 conduction. Q12 collector then goes positive until it takes Q11 source to a point that limits Q11 conduction. Thus, the stage is a self-stabilizing unity gain amplifier with very high input impedance and very low output impedance. The output impedance

is then essentially the value of R13. R18/C17 decouple the circuit from the —19-volt power supply. D10 protects Q12 base-emitter junction from reverse bias damage when the SOURCE switch turns the amplifier off for internal triggering operation.

50 Ω Input

Signals connected to the 50 Ω input connector pass through a coaxial cable that is looped three times through a ferrite toroid. The toroid (L21) reduces possible ground currents between J21 and J22 to prevent false triggering. Once the signal leaves the cable, it passes through C24 and R24 to the emitter of common-base amplifier Q20. L22-R22 and C24-R24 in series with Q20 internal emitter resistance present a 50 Ω load to the input signal over a wide range of frequencies.

The amplifier is forward biased into conduction by R15 and the +19-volt supply. Q20 collector return resistor is R39. The signal load varies from 100 Ω (R45) for high frequencies, to 2.7 kΩ (R39) for low frequencies. When the SOURCE switch is placed at INT, Q20 base-emitter junction is reversed biased by electron flow through R27-R26-D24 which places Q20 emitter about —0.6 volt from the base. D24 assures that Q20 base-emitter junction reverse bias does not exceed the transistor ratings (and at the same time does not load input signals when Q20 is conducting). The amplifier input impedance is 50 Ω, unless a high amplitude negative signal causes D24 to conduct. If D24 conducts, R24 limits C24 charging current. Steady DC signals greater than 3.5 volts can damage R22.

Internal Trigger Circuits

Internal triggering signals come from the associated vertical sampling unit, if that unit has a trigger takeoff circuit. The internal signal arrives through the Type 3T2 rear panel interconnecting plug, P21, and enters the shielded trigger circuit at J32. The input coaxial cable is looped three times through a ferrite toriod core just before the signal enters J32. The common base amplifier, Q30, functions identically as described above for Q20. The only circuit difference is that the interconnecting cable termination is 50 Ω for high frequencies only. L32 grounds the input signal path at DC.

Polarity Selection

Triggering signals can be inverted by changing the front panel POLARITY switch setting. The major components of the polarity selection circuit are SW40, T55, Q41 and Q51. They serve to pass the triggering signal to the Trigger Recognizer with the same phase as at the input, or inverted to invert the CRT display of the triggering event.

Non-inverted operation takes place when the POLARITY switch is at +. At + polarity, Q51 is placed at cutoff by current in D53, setting Q51 emitter about +0.4 volt from the base. The electron path is from ground, through D53, T55 secondary, and R58 to the +19-volt supply. Q41 is conducting due to electrons flowing from the —19-volt supply through R46, R45, T55 primary, Q41, R41 and R59 to the +19-volt supply. Q41 (and Q51, when operating) is a common base amplifier. D43 (and D53) are special hot carrier diodes with very low dynamic forward resistance, assuring a good connection when forward biased by the POLARITY switch.

As the triggering signal leaves either Q20 or Q30 and passes through C43, T55 primary passes the signal to Q41 emitter without inversion. Q41 then amplifies the signal without inversion and drives the Trigger Recognizer through C59.

Inverted operation takes place when the POLARITY switch is at —. At — polarity, Q41 is placed at cutoff by D43 forward bias voltage. Q51 is now a common base amplifier receiving inverted signals from T55 secondary. T55 secondary has a low impedance signal path at C55 assuring that secondary signal currents are injected at Q51 emitter. Q51 amplifies the inverted signal without further inversion and drives the Trigger Recognizer through C59. T55 limits the low frequency triggering when at — POLARITY (see the Characteristics section under sine wave triggering).

UHF Sync

The triggering signal paths described above have an upper frequency bandpass limit that is considerably less than the upper frequency limit of the Trigger Recognizer circuit. Two components, C1 and R1 couple very high frequencies around the normal trigger amplifier input circuits directly to the trigger recognition tunnel diode D62.

Trigger Recognizer and Holdoff Multi

The separately identified Trigger Recognizer and Holdoff Multi circuits function as a unit circuit. The Trigger Recognizer drives the Holdoff Multi; the Holdoff Multi then locks out additional trigger recognitions for a period long enough to allow all other Type 3T2 circuits to operate. Trigger recognition lockout is actually performed by the Trigger Lockout double comparators Q70-Q72 and Q80-Q82, but control of the lockout period is by the Lockout Multi.

The trigger recognition circuit contains four major sections: 1) an input trigger recognition pair of diodes, tunnel diode D62 and back diode D66;[1] 2) an output tunnel diode D90; 3) three transistors that drive other circuits: Q90, the PULSE OUT source, Q101 driving the Holdoff Multi and the Rate Meter Memory Gate and Q102 driving the Timing Ramp Clamp; and 4) the Trigger Lockout double comparators Q70-Q72 and Q80-Q82 and their control transistor Q74.

Quiescent Conditions

Trigger circuit quiescent conditions (before the arrival of a trigger signal) depend upon the setting of the front panel TRIG SENSITIVITY control. With the TRIG SENSITIVITY control set counterclockwise from the free-run midrange position, the following conditions exist.

1. Q72 and Q80 are conducting. Q72 and the TRIG SENSITIVITY control supply current to D62. D66 conducts a small amount of current at the low voltage state of D62.

2. D62 is resting at its low voltage state, at a current value near its peak, so that a small drive signal from Q41 or Q51 will cause D62 to switch to its high voltage state.

3. D90 and Q90 are conducting all of Q80 current (~10 mA). D90 is at its low voltage state but near peak current, armed by Q80.

[1]See June, 1966 and August, 1966 editions of Tektronix Service Scope for the article: Tunnel Diode Switching Circuits and the Back Diode.

4. Q90 is a germanium transistor. Q90 +0.27-volt emitter voltage, plus D90 low voltage condition is not enough voltage to forward bias either Q101 or Q102 into conduction.

5. Q101 and Q102 are not conducting. Q102 prevents the Timing Ramp from running, and Q101 permits the Holdoff Multi to rest at its quiescent conditions.

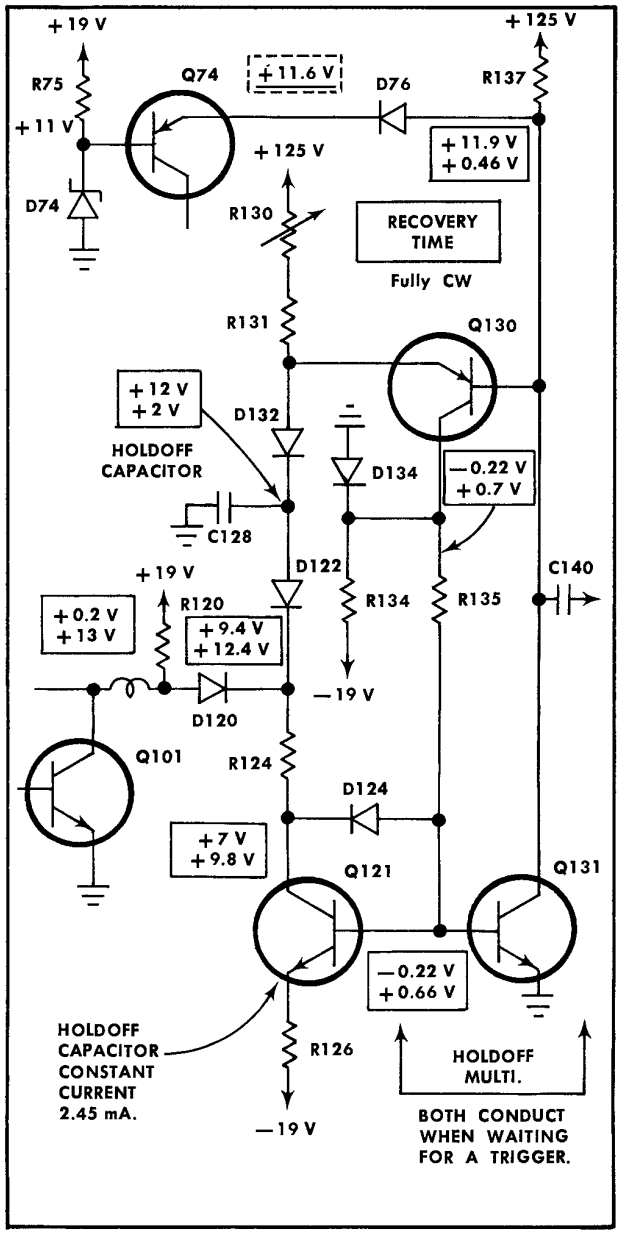


Fig. 4-1 Holdoff multi circuit voltages. Upper voltages: Q101 saturated, Lower voltages: Q101 cut off.

The Holdoff Multi quiescent conditions (see Fig. 4-1) are:

1. Q121 is conducting 2.45 mA through R124, D120 and R120.

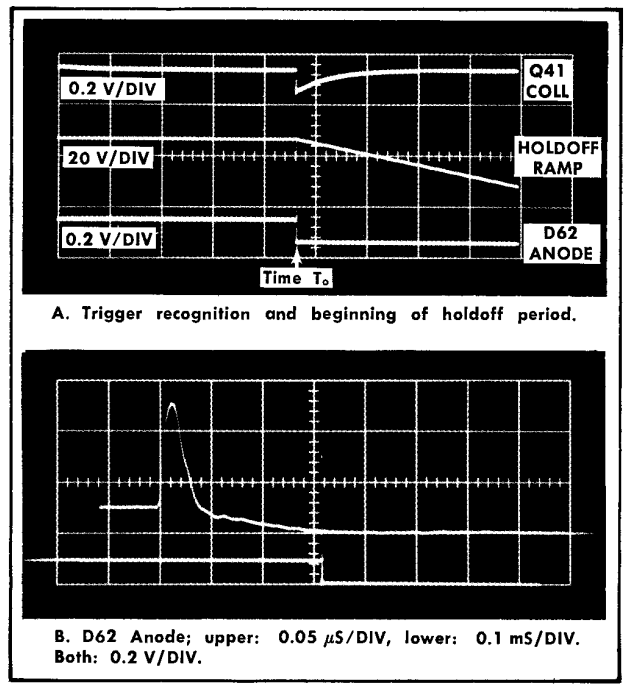
2. Q130-Q131 are both conducting. Q130 emitter voltage is +0.71 volt, and its current path is through the Recovery Time control. Q131 collector voltage is +0.46 volt, which holds Q130 in conduction and reverse biases D76 so Q74 does not conduct.

3. C128 voltage rests at +12 volts where it was left after the previous trigger recognition cycle. Both D122 and D132 are reverse biased.

4. Both D124 and D134 are reverse biased.

Triggered Functions

The previous trigger and hold off circuit quiescent conditions apply at the end of each holdoff period. A trigger signal always applies a positive drive to D62 to start the system operating for each sample taken. The instant when D62 receives enough energy to switch to its high voltage state is identified as T_o (both in this discussion, and in Section 2). Two sets of waveforms in Fig. 4-2 and Fig. 4-3 support the following discussion of one sampling cycle; T_o is identified in each figure.



A. Trigger recognition and beginning of holdoff period.

B. D62 Anode; upper: 0.05 μS/DIV, lower: 0.1 mS/DIV. Both: 0.2 V/DIV.

Fig. 4-2. Trigger recognition waveforms. Test oscilloscope: 85 MHz bandpass.

At the arrival of a positive going signal at D62 anode, D62 switches to its high voltage state and the sequence of actions that occurs is described below.

1. D62 switches to its high voltage state.

2. L62 is a high impedance at switching time, so R62-C62 couple D62 output to D90. Almost immediately, L62 conducts and D62 positive output is coupled to back diode D66.

3. D66 conducts when its cathode reaches +0.25 volt; it then takes all the current from Q72-R68 allowing D62 to switch back to its low voltage state.

4. Before D62 reaches its low voltage state, D90 switches to its high voltage state and saturates both Q101 and Q102. This reduces the current in Q90. The actions that follow D90 switching high occur in two steps: Q90 and Q102 respond to D90 first, because L104 slows the drive to Q101 emitter.

5. As D90 switches to its high voltage state, its anode tries to rise positive, but is prevented by the emitter-base junction of Q102. Q102 emitter can go only about +0.7 volt positive, so D90 cathode must go negative. Q90 is a germanium transistor and does not go to cutoff when its emitter is driven nearly to ground. Instead, its current is reduced causing the Pulse Out signal to make a negative step. At the same time, the current from D90 is reduced from about 10 mA to about 2 mA. (D90 stays at the high voltage side of its valley minimum voltage because its valley current is less than 2 mA.) Thus, the nearly 10 mA current provided by Q80 is now divided between D90-Q90, Q102 emitter current and Q101 base current.

6. As Q102 saturates, the Timing Ramp starts its rundown.

7. L102 slows Q101 collector signal to the Holdoff Multi circuit, allowing D68 to be forward biased before the holdoff ramp starts negative. D68 conduction takes essentially all of Q72 current away from both D62 and D66, locking out any trigger (or self oscillations should the TRIG SENSITIVITY control be turned clockwise into a normal free-run position).

The upper waveform of Fig. 4-2B shows the fast positive, then fast negative voltage change across D62, then the slower slope as Q101-D68 takes all of Q72 current.

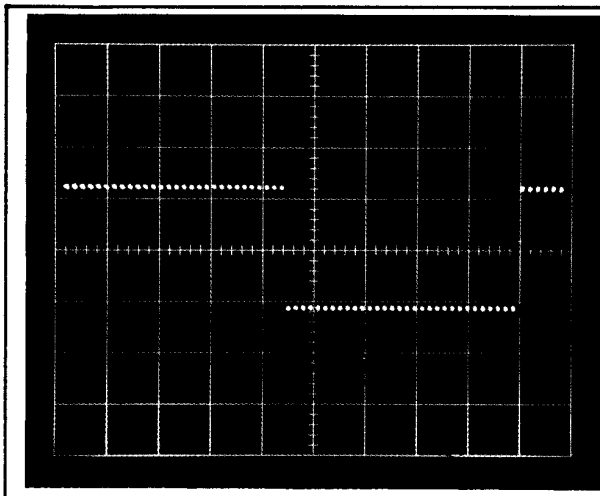
8. As L102 passes Q101 signal to the Holdoff Multi circuit, the current passing in R120 is switched away from D120-Q121 and taken to ground through Q101. This action releases Q121 current and D122 switches it into the holdoff capacitor C128.

9. C128 voltage starts negative at a constant slope controlled by its capacitance and the 2.45 mA of Q121. Fig. 4-3B bottom waveform shows that the holdoff capacitor voltage changes slope just before it switches the Holdoff Multi into non-conduction. The change in slope is due to D124 becoming forward biased and Q131 losing base current before the multi switches. Fig. 4-3B 3rd waveform shows Q130 base—Q131 collector waveform as Q131 starts to turn off. Then as Q131 base-emitter junction becomes reverse biased, the multi switches off rapidly and Q130 base—Q131 collector signal rises positive.

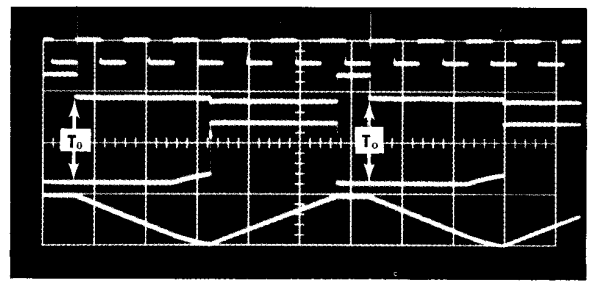
10. Q131 collector signal rises to +11.9 volts in 5 μs; it is stopped as D76 is forward biased and Q74 takes all R137 current.

11. As Q74 conducts, its collector rises positive and switches the two trigger lockout comparators so that Q70 and Q82 conduct. Q72 stops conducting, which removes any possibility of current into either Q101 or D62-D66. Q80 stops conducting, which removes the drive from D90, Q101 and Q102. Q82 current all passes into Q90 emitter and restores the positive Pulse Out waveform. Now D90, Q101 and Q102 are all without current.

12. As Q101 stops conducting, R120 raises D120 anode positive. This forward biases D120. R120 current is greater than the Recovery Time maximum current, so Q121 collector



A. "With Trigger" display of 1 kHz square wave. 100 μs/DIV.



B. Upper: 1 kHz signal.
2nd: D62 anode. 0.2 V/DIV.
3rd: Q130 base, Q131 collector. 20 V/DIV.
Lower: Holdoff cap. 20 V/DIV.
All: 1 mS/DIV.

Fig. 4-3. Trigger circuit waveforms for two samples of upper display.

rises positive and reverse biases D122. With D122 reverse biased and Q130 not conducting, all the Recovery Time control current is switched into C128, charging it in a positive direction.

13. In steps 9 and 10 above, as Q131 collector signal goes positive at the holdoff period half-way point, C140 couples a turn-on signal to the Logic Drivers Q141 and Q143. Both Logic Driver transistors were previously not conducting. As Q141 conducts to saturation, C142 is charged for a limited time turn-on pulse to Q143 after Q141 stops conducting. Thus, the two RC input circuits to Q141 and Q143 cause them to conduct into saturation for a limited period of time, one after the other, just as Q131 collector goes positive.

The action within the rest of the Type 3T2 circuits due to the two successive pulses of the Logic Driver transistors is discussed in detail in Section 2 in the text associated with Fig. 2-7. That basic description is expanded throughout the rest of this circuit description.

14. The Recovery Time control charge of C128 soon takes C128-Q130 emitter voltage far enough positive for Q130 base-emitter junction to be forward biased. As Q130 con-

ducts, it and Q131 switch rapidly to their previous conducting condition, turning off Q74 and restoring both Trigger Lockout comparators to their Q72-Q80 quiescent conducting conditions. Q72 and Q80 restore the trigger recognition circuit, D62 and D66 (and D90) to an armed state ready for another positive trigger from Q41 or Q51.

Trigger Lockout Comparators

The trigger lockout comparators are both used in a switching mode to control the trigger recognition tunnel diode and output tunnel diode operating conditions. Operating functions are described in the preceding paragraphs. Operating voltages of the circuits are set by Zener diode D74 and the +19-volt supply. D74 sets the base voltage of all four comparator transistors, and of their switching control transistor Q74. When Q74 is not conducting, R77-R78 voltage divider sets the base voltage of Q72 and Q80 about 1 volt negative with respect to Q70 and Q82 base voltage. Thus Q72 and Q80 conduct when the system is armed and ready to receive a trigger signal.

Q72 and D62 current is adjusted during calibration by the TRIG SENS BAL control in the emitter return lead of Q70-Q72. The current value in Q80, D90 and Q90 is adjusted during calibration by the OUTPUT TD BIAS control R82 in the emitter return lead of Q80-Q82. Both adjustments set the two trigger tunnel diodes to their ready or armed current value of slightly less than 10 mA.

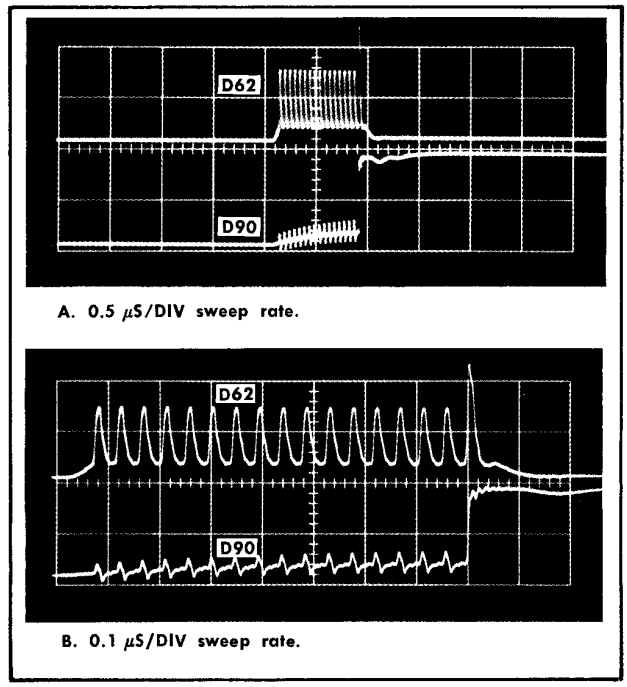
Halfway through a triggered holdoff period, when Q74 conducts, Q74 collector current reverse biases Q72 and Q80 by making their base voltage more positive than Q70 and Q82 base voltage. At this time the current originally supplied to the two tunnel diodes is stopped. The comparators' emitter current is still nearly 10 mA, but is passes through R70 to ground and through R85-Q90 to the —19-volt supply.

At the end of the holdoff period when Q74 emitter releases its current path, the two lockout comparators restore to their original quiescent state. Two capacitors (C80 and C85) slow the collector signals at Q80 and Q82 from the rate of change of Q72 collector signal. These capacitors allow Q72 to arm D62 before D90 is armed, for proper UHF Sync operation.

UHF Sync Operation

Tunnel diode D62 and back diode D66 can be biased into oscillation by advancing the TRIG SENSITIVITY control clockwise past its midrange position. Oscillations take place between about 12 and 20 MHz depending upon the TRIG SENSITIVITY control setting. Almost immediately after D62 switches to its high voltage state, L62 lets D66 pull D62 off its high state. Soon after D62 goes back to its low voltage state, D66 stops conducting and the cycle repeats. Oscillations begin right after Q72 conducts at the end of a normal holdoff period.

D62-D66 oscillate through several cycles before D90 is armed. The time difference is about 0.8 μs, caused by the capacitors at Q80 and Q82 collectors. Fig. 4-4 waveforms show D62-D66 oscillations and D90 switching to its high state when the TRIG SENSITIVITY control is fully clockwise (no UHF Sync signal is connected to the Type 3T2). Note that D90 switches to its high voltage state (and starts the holdoff period for one sample) just as D62 anode goes positive.



A. 0.5 μS/DIV sweep rate.

B. 0.1 μS/DIV sweep rate.

Fig. 4-4. D62 and D90 UHF Sync waveforms. Test oscilloscope: Externally triggered; 85 MHz bandpass.

UHF Sync operation results when a high frequency signal arrives at D62 anode through C1 and R1 causing D62 to switch positive slightly in advance of its normal switching time. D90 goes to its high voltage state exactly as shown in Fig. 4-4, but at a time when the UHF Sync signal switches D62. The normal holdoff period and functions previously described follow D90 switching positive.

RAMP GENERATORS

The Ramp Generators diagram at the back of this manual contains the following circuits: Timing Ramp, Slewing Ramp, Staircase Inverter, Leadtime Comparator, Timing Ramp Comparator, Slewing Ramp Comparator, Vert Strobe Drive, Time Position Offset and Timing Ramp amplifier. Circuits used during With Trigger operation include only the Staircase Inverter, Timing Ramp, Timing Ramp Comparator and the Vert Strobe Driver. Circuits used during Before Trigger operation include all but the Timing Ramp Comparator. The following description begins with the system operating with the START POINT switch at BEFORE TRIGGER and concludes with the START POINT switch at WITH TRIGGER.

Before Trigger Operation

During Before Trigger operation, the circuits diagrammed on the Ramp Generators page serve a special coordinating function of the CRT display horizontal and vertical deflection voltages. The deflection voltages are not generated there, but each dot horizontal position is determined.

A detailed block diagram of the Ramp Generators is shown in Fig. 4-5. Using Fig. 4-5, the purpose of the ramp generators

is to relate the ratemeter-started slewing ramp and the trigger-started timing ramp to the reference staircase signal to produce horizontal signals that are properly related to the vertical strobe drive pulses. The horizontal output signals span a fixed voltage range equal to the CRT horizontal scan, regardless of sweep rate or time window location (Time Position control setting). Section 2 controlled sequence random sampling system description implies (at waveform (O) of Fig. 2-7) that the timing ramp stopped voltage is memorized as it comes out of the Timing Ramp generator. This is not true. It is true that the Timing Ramp generator output voltage does operate through a variable range when turning the Time Position controls, but that voltage is not memorized. The variable range of Timing Ramp output voltage is a side effect of varying the slewing ramp output voltage range for proper operation of the Slewing Ramp Comparator. If the range of Timing Ramp output voltages was fed to the horizontal memory, the physical position of the CRT display would shift. Instead, only the time window shifts across a fixed CRT display.

The Timing Ramp movable output voltage range is converted to a fixed voltage scan at the output of the Timing Ramp Amplifier. The fixed scan is referenced to the fixed staircase signal steps fed in at the Staircase Inverter Amplifier input. Two front panel controls that affect the Timing Ramp range of output voltage are the TIME MAGNIFIER and the TIME POSITION controls. These controls alter the Slewing Ramp stopped voltage range within the Ramp Generators circuits, and then cancel the associated Timing Ramp changes at the Timing Ramp Amplifier output. Equal and opposite changes to the system are introduced. The TIME MAGNIFIER control alters the Staircase Inverter Amplifier output by decreasing its gain. It therefore alters the Timing Ramp Amplifier output by increasing its gain an identical amount. Likewise, the TIME POSITION controls apply a negative offset to the Staircase Inverter Amplifier output (when other than fully clockwise). They therefore alter the Timing Ramp Amplifier output in a positive manner exactly equal and opposite to that of the Staircase Inverter Amplifier output. The result then

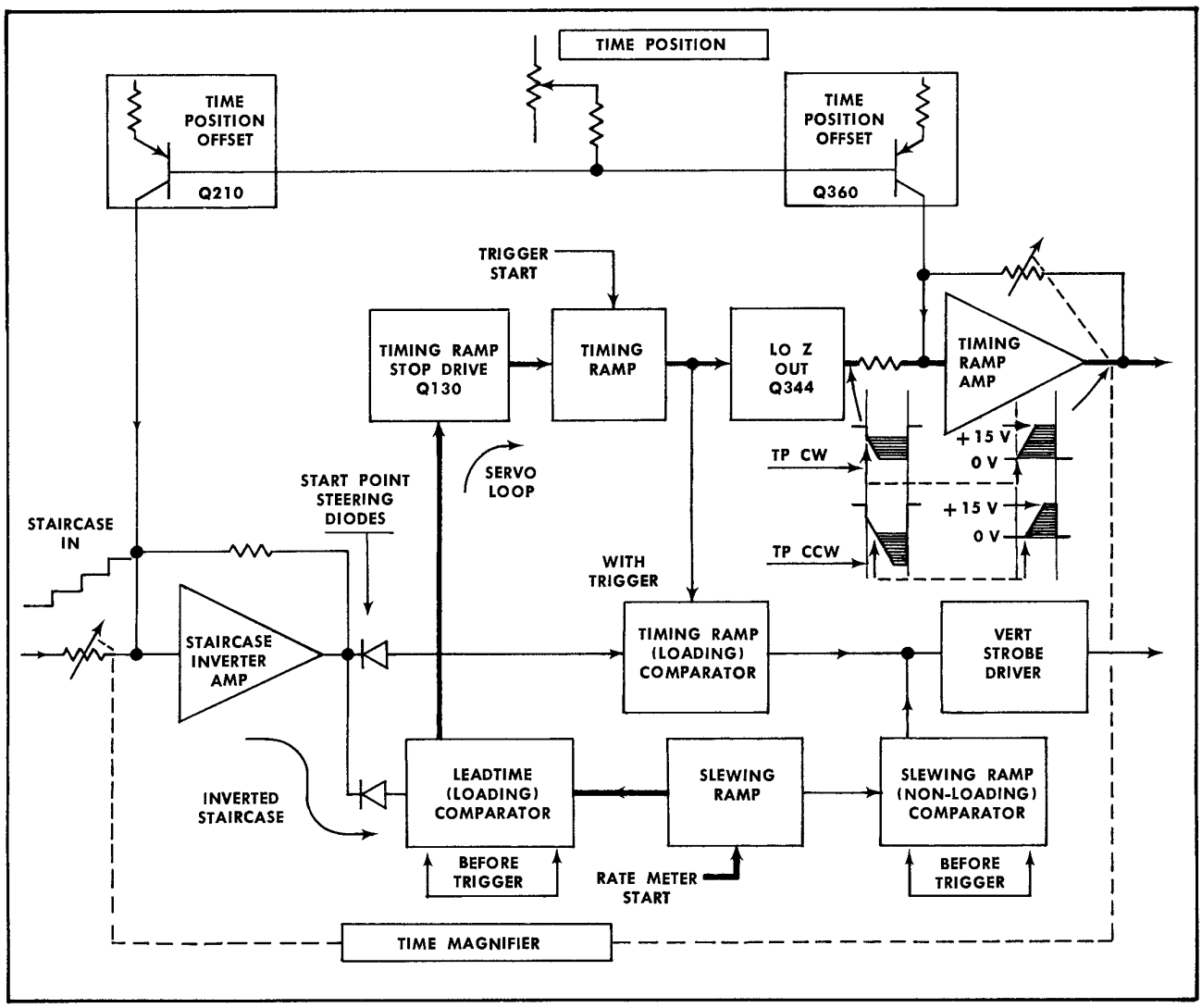


Fig. 4-5. Ramp Generators block diagram.

is that the Timing Ramp signals out of the Timing Ramp Amplifier always stay within the same zero volt to +15 limits. Four drawn waveforms near the Timing Ramp Amplifier in Fig. 4-5 and the waveforms of Fig. 4-6, show the Timing Ramp Amplifier output signals when the TIME POSITION controls are at their two extremes. Descriptions of the individual circuits follow.

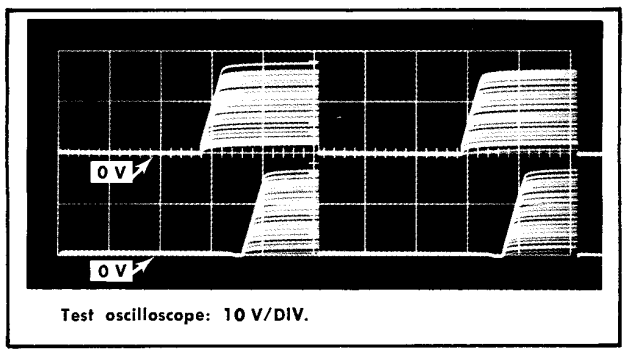


Fig. 4-6. Timing Ramp output signal. Upper: TIME POSITION fully cw. Lower: TIME POSITION fully ccw.

Timing Ramp Generator

The Timing Ramp Generator consists of five selectable constant current transistors and 5 capacitors that charge at a linear rate; a clamp circuit to hold the output voltage near ground, and then release the chosen ramp circuit to run negative upon trigger circuit command; a four transistor high impedance to low impedance output circuit; and a Stop Drive transistor that responds to the Leadtime Comparator during Before Trigger operation. Many diodes are used in the overall Timing Ramp circuit for signal switching with low impedance, no loss conduction, and high impedance low leakage reverse bias nonconduction. Connections from the trigger circuit to the Timing Ramp Clamp, and three of the five ramp generators are shown in Fig. 4-7.

Timing Ramp Clamp

When the trigger circuit is armed and ready, Q102 nonconduction places the Timing Ramp Clamp transistors in their quiescent conducting condition and the Timing Ramp generator output is clamped near ground. Q301 and Q302 are not saturated due to the two-diode voltage difference between Q302 collector and Q301 emitter, and the voltage at Q301 base. Q302 collector pulls toward ground due to Q301 collector current drive to Q302 base. D306-D307 pull Q301 emitter up until Q301 current is reduced, reducing Q302 base current. The clamp then holds itself with Q302 about —0.4 volt from ground. Q102 conduction takes Q301 collector current away from Q302 base, cutting Q302 off. The negative voltage change at Q302 collector reverse biases D307, which then lets R306 set Q301 maximum current at about 1 mA. D306 is reverse biased by any negative change at Q306 emitter, assuring that Q301 does not load the Timing Ramp rundown. At the end of a Timing Ramp period, when Q102 is cut off and Q301 collector current (1 mA) is switched into Q302 base, C300-R300 limit the rate at which Q302 base receives its turn-on drive. C300-R300 then slow the rate at which the Timing Ramp is reset; which assures that the Horizontal Memory circuit has enough time to properly store the stable stopped Timing Ramp voltage.

Ramp Generator Circuit

One of five ramp generator circuits is selected by the front panel RANGE switch. The one selected conducts a constant current all the time, while the other four are cut off with no emitter return circuit. Fig. 4-7 shows two of the ramp generators, with the RANGE switch drawn connected to Q325 emitter and the 10 μs range in operation. Constant current is assured by the pentode-like collector characteristics of Q325 and the large value of resistance between its emitter and the —100-volt supply. The collector voltage range is from about —3.3 volts when Q302 conducts, to about —19 volts when the Time Position controls are both fully counterclockwise and the Time Magnifier switch it at ×1. This change in collector voltage may change the transistor bias a fraction of a volt, but not enough to significantly change the 7.5 mA current through R335 and R336.

There is no loading comparison made between the inverted staircase and the timing ramp. Instead, the inverted staircase is compared with the slewing ramp at Q231, the Leadtime Comparator. Q231 collector current is less than 1 mA before the slewing ramp forward biases D236. After D236 is forward biased, the slewing ramp 7.5 mA flows through Q231 and the current forward biases the Timing Ramp Stop Drive transistor Q310. Prior to this event, Q310 is cut off due to R311 current through D311. Before Q310 conducts, its collector circuit rests at —19 volts, reverse biasing D325, D327 etc. When Q310 conducts, D314 forward voltage drop places D325 anode sufficiently positive to take all of the 7.5 mA through R335 and the Timing Current control, R336. This takes current from Q325 and stops charging C324, which stops the ramp running negative.

With Trigger Operation (Fig. 4-8)

As Q302 cuts off, Q325 7.5 mA current has four possible paths: 1) C324 the capacitor between its collector and ground; 2) R330 to ground; 3) Q306 base current and 4) D277 and Q271 emitter. At the beginning of the timing ramp rundown, almost all of the 7.5 mA is used to charge C324. Almost no current is required by Q306 base because its emitter circuit current is used only to charge C308 and almost no current flows in R330. As C324 charges negative, the ramp voltage soon is stopped going negative by the loading comparison with the inverted staircase. The loading comparison takes place at Q271 base-emitter junction and all of Q325 7 mA then flows through the series connections of D324, D330, D277 and Q271.

Special Timing Ramp Components

Several component functions within the Timing Ramp circuit are not obvious from the previous descriptions. R332 and C332 decouple the —19-volt supply from the Ramp Generator base circuit. R333 and C333 add stabilization to the active transistor emitter-base circuit to prevent parasitic oscillations. D330 disconnects the other ramp generators when the 100 ns ramp is in use (Q329). R330 then provides leakage current (I_{CBO}) to the cutoff ramp transistors and assures that D330 cathode remains essentially at ground.

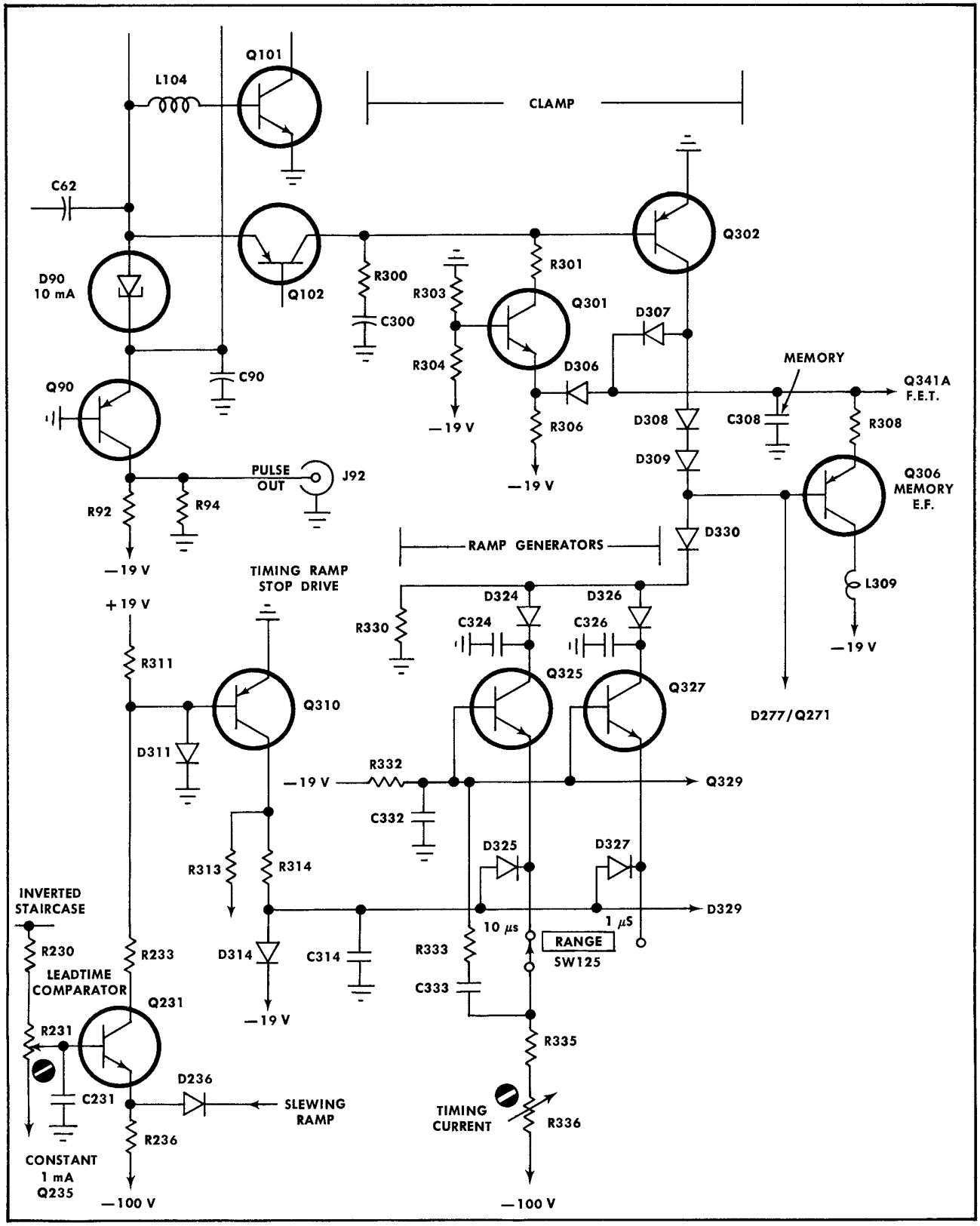


Fig. 4-7. Before Trigger Timing Ramp Connections.

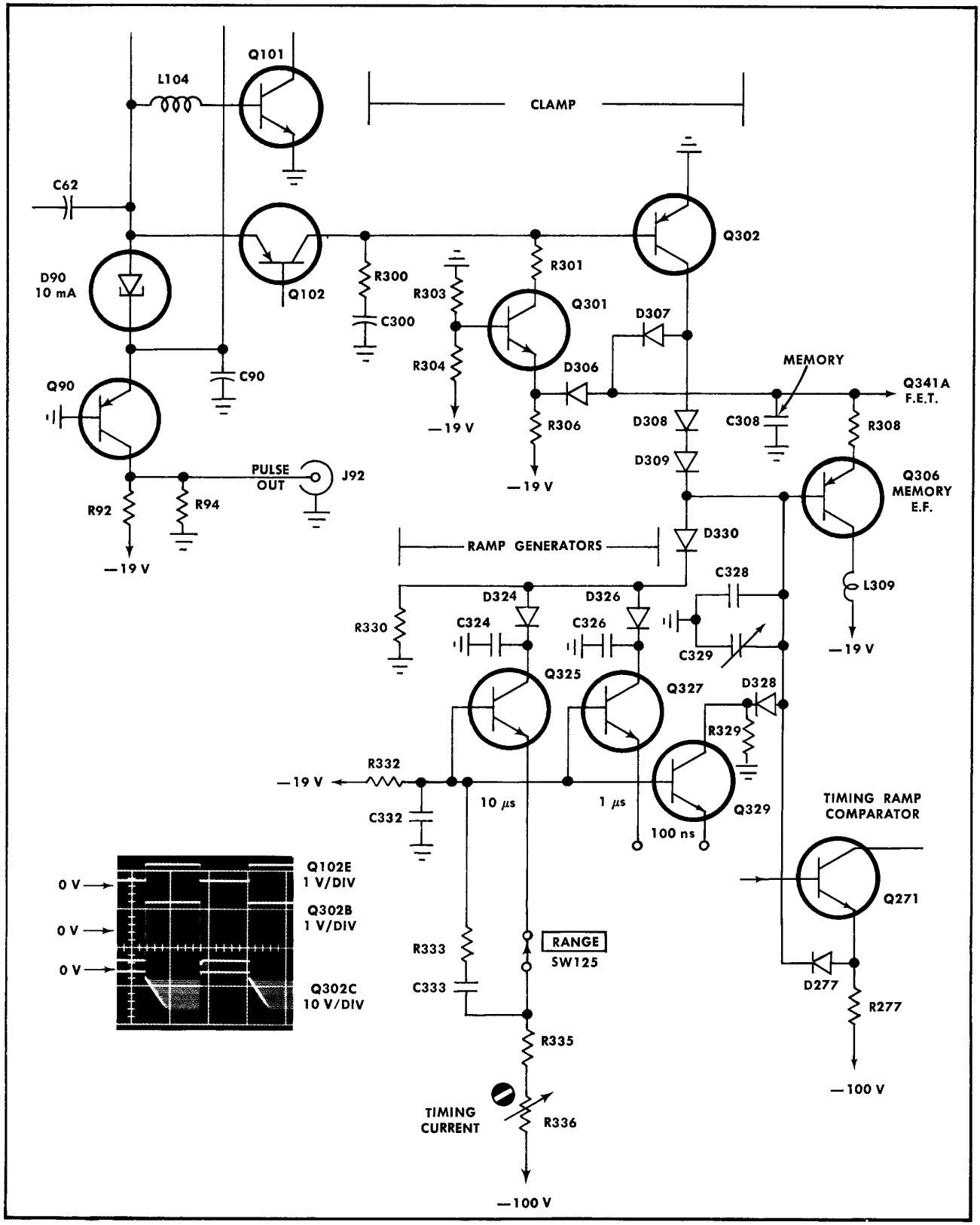


Fig. 4-8. With Trigger Timing Ramp Connections.

D328 and R329 perform the same disconnect function when Q329 is not in use.

Two diodes between Q302 collector and Q301 emitter limit the self-generating drive and prevent both Q301 and Q302 from saturating. D306 disconnects Q301 and R306 from the released negative-going ramp signal. D307 discharges C308 memory capacitor at the time the Timing Ramp is reset.

Memory and Memory E.F.

The memory capacitor C308 and emitter follower Q306 serve to stablize the timing ramp voltage between the time when the rundown is stopped and the circuit is reset. C308 is about 7 times larger then the100 ns ramp capacitors, providing about one seventh the rate of leakage that would exist if C328-C329 were connected directly to Q341A gate lead. Q306 provides current gain during the ramp rundown, which isolates C308 charging current from the ramp generator collector current. Then as the ramp stops running negative, C308 stores the stopped ramp voltage with several times the stability that can be obtained from C328-C329.

Q306 does not provide the discharge current for C308 during ramp reset. Instead, C308 is discharged by Q302 and D307. D308 and D309 forward voltage drop (during reset) assures that Q306 base voltage never completely cuts off collector current. Then, when the timing ramp is released for another rundown, Q306 is already conducting and the ramp signal out of Q306 emitter (and C308) starts linearly with no delay.

High Impedance to Low Impedance Driver

Fig. 4-9 includes the Timing Ramp output transistors, Q341 and Q344. Q341A, Q341B, D343 and Q344 are connected so that Q341A input gate voltage and Q344 emitter output voltage are essentially identical. If there is any voltage difference, it never exceeds about 20 or 30 millivolts. The input-output voltage equality with high impedance input to low impedance output is accomplished by special attention to transistor bias voltages.

Q341B is a zero biased constant current stage. Zero bias is assured by directly connecting the gate to the source. The zero bias connection firmly fixes the channel current at the natural value for zero bias. With the two halves of Q341 matched chips mounted in the same can, the zero bias channel current of one half equals the zero bias channel current of the other half. Thus with Q341B forced to conduct a channel current at its natural zero bias value, Q341A (in series) also conducts at its natural zero bias value. Q341B also temperature compensates Q341A, automatically changing the zero bias channel current for both halves to maintain Q341A zero bias operation.

Q341A is connected as a source follower (similar to an emitter follower) that drives a junction transistor emitter follower. Since Q341A source voltage equals its gate voltage, the second transistor base-emitter drop is compensated by D343. The forward voltage drop across D343 is almost equal to the forward voltage drop across Q344 base-emitter junction, thus setting Q344 emitter at the same voltage as Q341A gate. D343 temperature compensates Q344, making the two followers unusually stable over a normal operating temperature range.

Q344 emitter signal drives the input resistance of the Timing Ramp amplifier, R348 and R349. The emitter signal swings from about —1 volt to about —13.3 volts throughout the range of Timing Ramp signal.

Timing Ramp Amplifier

The Timing Ramp Amplifier consists of two operational amplifiers, one inverting, the other non-inverting. The inverting amplifier is always used, and the non-inverting amplifier is used only when the Time Magnifier control is at ×10, ×20, or ×50. Each time the Time Magnifier switch is advanced away from ×1, the Timing Ramp signal amplitude out of Q344 emitter is reduced. However, the feedback resistors of the Timing Ramp Amplifier increase its gain an equal amount so the output swing limits never change. The same is true when using the Time Magnifier VARIABLE control. Table 4-1 lists the input signal changes and amplifier gain changes through the range of Time Magnifier switch positions.

The Timing Ramp one time-window range of signal amplitude is 7.5 volts (at Time Magnifier = ×1). Add to this the Timing Ramp Amplifier basic ×2 gain, and the Timing Ramp 7.5 volt range of output signals is converted to a 15 volt signal. Then as the Slewing Ramp - Inverted Staircase comparisons reduce the Timing Ramp amplitude through the Time Magnifier switch positions, the final Timing Ramp Amplifier range of output signals remains at 15 volts.

Special use of a differential comparator at the inverting amplifier input (Q371 allows the amplifier input voltage to be set to to zero when the Timing Ramp is running down. The adjustment is made at Q371B base, compensating for any transistor unbalance of the differential pair. The in-

TABLE 4-1

Timing Ramp Amplifier Gain

Switch position TIME MAG	Input signal attenuation[2]	Feedback Gain[3]	Gain out of Q381 emitter	Gain out of Q395 emitter	Total Amplifier gain
×1	×1	×2	×2	not used	×2
×2	1/2	×4	×4	not used	×4
×5	1/5	×10	×10	not used	×10
×10	1/10	×2	×2	×10	×20
×20	1/20	×4	×4	×10	×40
×50	1/50	×10	×10	×10	×100

[2]**Attenuated at Staircase Inverter input, which attenuates negative run of both Slewing and Timing Ramps.**

[3]**Input Resistance is 2.5 kΩ, feedback resistance is 5 kΩ.**

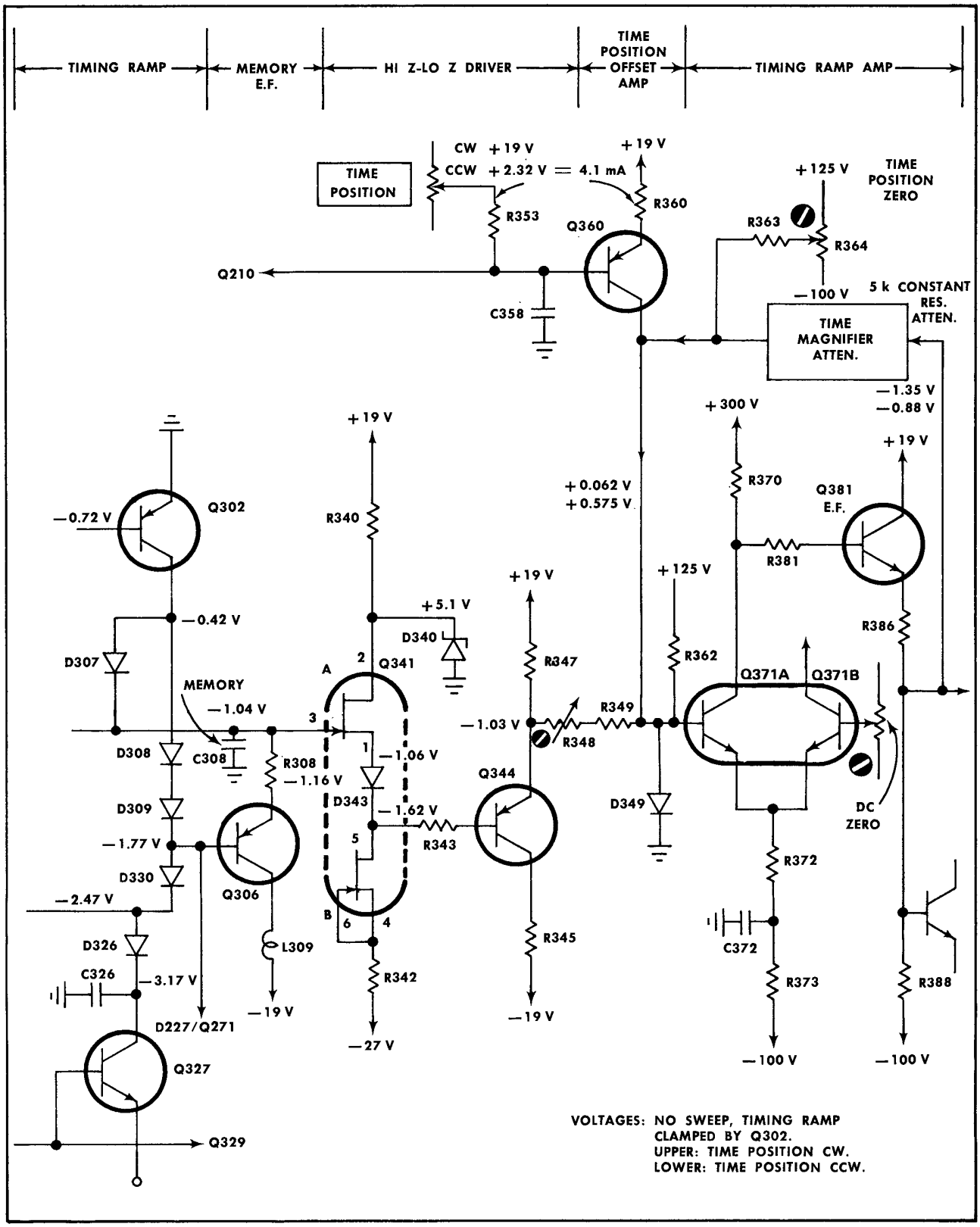


Fig. 4-9. Timing Ramp output, Time Magnifier circuit and Time Position control.

verting operational amplifier (Q371 and Q381) has a very high open loop gain so that essentially all of the input signal current (through R348 and R349) passes into the feedback resistance of the Time Magnifier switch. This assures the usual virtual signal ground at the base of Q371A. It is the voltage of the virtual signal ground input that is adjusted to zero volts while the amplifier is operating through its dynamic range. Once the virtual signal ground input is at zero volts, then the current injection input from the Time Position Zero control (R364) is adjusted so the output first stopped ramp voltage at each sweep start is no more positive than the clamped voltage value.

The feedback resistance on the Time Magnifier attenuator remains at 5 kΩ. This is done so the 10 kΩ maximum resistance VARIABLE control will increase the Timing Ramp Amplifier gain by a factor of 3 for all positions of the Time Magnifier switch. The Variable control also reduces the inverted staircase signal amplitude by a 3 to 1 factor, assuring that the Timing Ramp Amplifier output signal range remains zero to 15 volts for all positions of the VARIABLE control.

The non-inverting amplifier gain is ×10, set by feedbak resistors R395 and R396. The amplifier plus input (Q391A base) receives the signal from Q381. Since the amplifier is not inverting, the feedback is applied to the minus input, Q391B base. Emitter follower Q395 drives both the output lead and the feedback resistors to Q391B. Q395 is not connected to the Time Magnifier attenuator feedback resistors that control the gain of the inverting amplifier.

Special components associated with the Timing Ramp Amplifier that have functions not obvious from the above description are described here. D349 clamps Q371A base at a maximum positive value of +0.6 volt when the timing ramp is clamped and the Time Position controls are fully counterclockwise. The clamp prevents the amplifier output voltage from reaching its most negative value and assures linear operation. R362 provides an offset signal to compensate for the normal quiescent —1 volt output from Q344 emitter. C372-R373 prevent any noise on the —100-volt supply from getting into Q371 emitter and being amplified. C376 assures that Q371B base has a low impedance for high frequencies; otherwise, R376 impedance to ground would limit the stage gain. C370, R381, R383, R391 and R399 all are high frequency oscillation dampers that keep the amplifier stable.

Time Position Offset

The Time Position Offset amplifier Q360, shown in Fig. 4-9, is a high impedance current source for the Timing Ramp Amplifier input. Q360 converts a variable voltage at its base (variable by the Time Position controls) to a variable current into Q371 equivalent signal ground input. Q360 conducts no current when both Time Position controls are fully clockwise, and conducts a maximum of 3.1 mA when the controls are fully counterclockwise. The current value at any Time Position control setting is set by Q360 base voltage (minus the silicon base-emitter drop), and R360 between Q360 emitter and +19 volts.

Voltage limits of the Time Position controls (diagrammed with the Ramp Generators at the back of this manual) are set by the series resistors R357 and R356, in parallel with the resistance of the controls. Diode D355 offsets the maximum positive control output from +19 volts to about +18.4 volts. The voltage across D355 is just sufficient to forward bias Q360 into conduction, giving the controls the ability to alter Q360 current all the way to their fully clockwise rotation stop. If D355 were not there, the Time Position controls would have no effect upon the display time window during the last 2 or 3 degrees of clockwise rotation.

Function of the Time Position controls is described earlier in the test that refers to Fig. 4-6.

Slewing Ramp Generator

The Slewing Ramp Generator is nearly identical to the Timing Ramp Generator previously described. The clamp circuit differs, but once released, the slewing ramp operates at the same rate on the same principle as the timing ramp. Basic differences from the Timing Ramp Generator are: the constant current transistor base voltage is —25.2 volts instead of —19 volts; the ramp negative run is stopped only by a loading comparison with the inverted staircase signal (rather than by a stop drive circuit); there is no memory capacitor or memory emitter-follower output circuit; and the clamp circuit does not hold the clamped output positive with respect to the starting ramp voltage (as the Timing Ramp Clamp does to the Timing Ramp).

Slewing Ramp Clamp

The Slewing Ramp Clamp is made up of three transistors Q251, Q252 and Q254. Quiescently, Q251 and Q252 do not conduct, but Q254 does conduct (without going into saturation), clamping the Slewing Ramp generator at about —0.6 volt. Fig. 4-10 shows the connections of the Slewing Ramp. The clamp is controlled by the Ratemeter Comparator. (See Fig. 2-7 block diagram. There, the Slewing Ramp is driven by the Trigger Ratemeter.) When the Ratemeter Comparator output goes positive, Q590 drives Q251 into saturation. Q251 collector at essentially ground, D256 connects Q252 collector to Q254 base and cuts off Q254 current. This releases the Slewing Ramp generator to run negative.

Halfway through the trigger holdoff time, the Ratemeter ramp is reset and the Ratemeter Comparator turns off Q251. Q251 turn off, soon turns off Q252. The small delay due to both Q251 and Q252 being in saturation does not disturb the circuit operation. As Q252 cuts off, its collector drops to —9 volts and D256 then disconnects Q254 base. Now, R259 (through D258) applies turn-on bias to Q254. Q254 conduction discharges the ramp capacitor much more rapidly than it charged negative. Then, as the voltage at Q254 collector rises positive enough for D259 to conduct, Q254 collector and D259 limit the drive to Q254 base and prevent saturation. Q254 is kept from saturation so it will quickly release the Slewing Ramp at the next Ratemeter "best guess" start command.

Slewing Ramp

The Slewing Ramp consists of five selectable constant current transistors and five different precision capacitors. The front panel RANGE switch selects one of the constant current transistors by connecting its emitter lead to R268 and R269 and the —100-volt supply. Each current transistor base lead is connected to a Zener diode-regulated —25.2-volt supply. Thus, with a fixed base voltage, the current transistor must

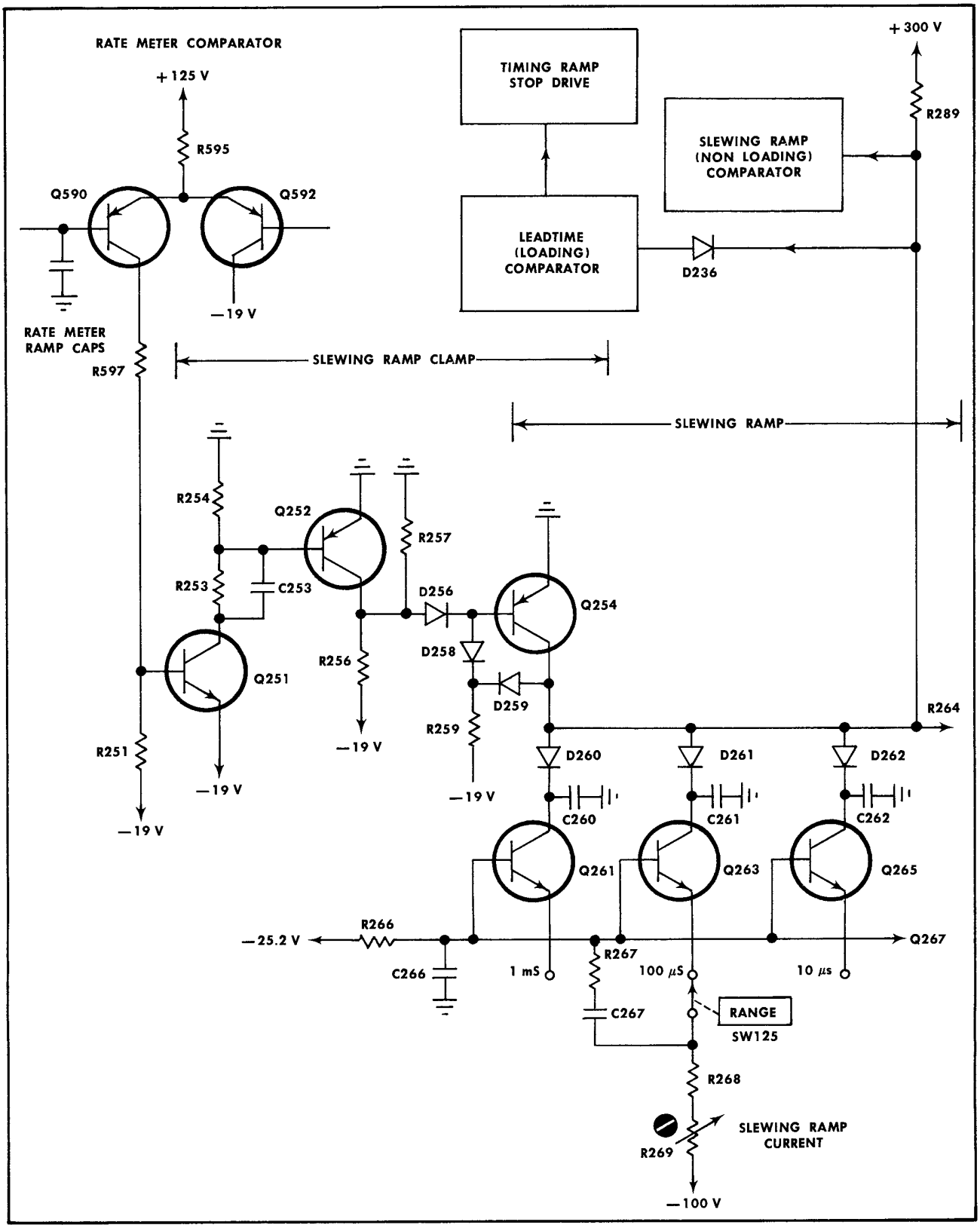


Fig. 4-10. Slewing ramp control and output connections.

conduct a value of current set by the value of R268-R269 and the voltage drop across them. It is the pentode-like characteristics of the transistor collector that then causes the associated ramp capacitor (C260 through C265) to charge negatively at a very linear rate. The selected constant current transistor conducts the same current value whether the clamp circuit holds the output voltage at —0.6 volts or cuts off and releases the ramp to run negative.

While the clamp circuit conducts, all ramp capacitors hold a —0.2-volt charge. Then when one capacitor starts its negative charge, the diodes connected to the other ramp capacitors are reverse biased. Turned-off constant current transistor leakage is not great enough to charge any of the unused timing capacitors sufficently to disturb the rate of fall of the capacitor in use. The 620 kΩ resistor (R289) connected between all the ramp disconnect diodes and +300 volts, assures that the diode connected to the operating ramp capacitor conducts slightly while the ramp runs negative.

The Slewing Ramp output signal drives both the Slewing Ramp Comparator and the Leadtime Comparator.

Slewing Ramp Comparator

The Slewing Ramp Comparator, Q281, D284 and Q283, is a non-loading comparator of the inverted staircase and slewing ramp signals. At the time of comparison, Q281 drives the Vert Strobe Driver avalanche transistor into conduction with very little change in the rate of fall of the slewing ramp signal.

With both Time Position controls fully clockwise and before a sweep is started, conditions are: Q281 base voltage is —1 volt, and its collector current is about 0.75 mA; Q282 base voltage is —0.6 volt and its collector current is about 2.6 mA; and D284 is reverse biased so the two transistor emitters are not connected together.

As the sweep starts, Q281 base remains at essentially —1 volt for the first inverted staircase voltage (regardless of the Time Magnifier or Variable control conditions). As Q283 base goes negative at the slewing ramp signal rate, its emitter also goes negative. As soon as Q283 emitter is about ½ volt below Q281 emitter voltage, D284 parallels R285 across R284 and increases Q281 collector current to about 3.5 mA. Q281 collector then drives essentially all of that current into Q290 base causing the Q290 to avalanche and drive the vertical unit strobe generator. As D284 conducts, Q283 is cut off during the rest of the slewing ramp negative run.

The loading comparison of the inverted staircase and the slewing ramp signals is described below under the Leadtime Comparator discussion.

Vertical Strobe Driver

An avalanche transistor Q290 drives a fast rise differentiated positive pulse to the vertical unit strobe generator each time there is a slewing ramp comparison. (In With Trigger operation, the strobe drive pulse occurs at each timing ramp comparison, described later under With Trigger Operation.) A second DC coupled output from Q290, drives the blanking circuits (diagram 5). The DC coupled signal blanks the CRT from the time of the slewing ramp comparison with the inverted staircase, until the slewing ramp is reset at ½ the holdoff period.

The avalanche transistor operates in its avalanche mode of ionized conduction only during the time it takes for the collector voltage to go from —19 volts to about —6 volts. After that, it goes into saturation as a normal junction transistor. It is the avalanche conduction period that produces a very fast output pulse for proper drive to the vertical unit strobe generator. In Q290 emitter, R292 and L295 limit high power ground currents so other circuits are not disturbed. L291 essentially disconnects the drive circuit to Q290 base during the very high frequency portion of the avalanche conduction period, then permits a steady DC forward bias for the duration of the interdot blanking period. D282 sets the reverse bias at +0.6 volt during the time Q290 is cut off.

Leadtime Comparator

The Leadtime Comparator is a loading comparator of the inverted staircase and slewing ramp signals. Both the slewing and timing ramps are stopped at the time of comparison. Before comparison, Q231 conducts about 0.8 mA, not enough current to turn on the Timing Ramp Stop Drive transistor Q310. Q231 base voltage is offset from the inverted staircase signal by constant current transistor Q235 and R230-R231. The voltage offset is about —3.75 volts (½ the 7.5 volts of one Time Position Range), and remains a fixed value regardless of inverted staircase voltage. The pentode-like characteristics of Q235 collector, and its fixed base voltage and emitter resistor, set the current through R230 and R231 at a constant 1 mA regardless of voltage changes by the inverted staircase signal.

Q231 emitter voltage and the normal silicon diode drop of D236, add about —1.2 volts to Q231 base voltage. Thus, the slewing ramp signal must go about 4.7 volts more negative than the inverted staircase voltage at each comparison. This voltage difference is converted then to a fixed time delay from the slewing ramp start. Q231 is adjusted so the time delay is equal to one half of a Time Position Range, described near the end of Section 2, Principles of 3T2 Random Process Sampling.

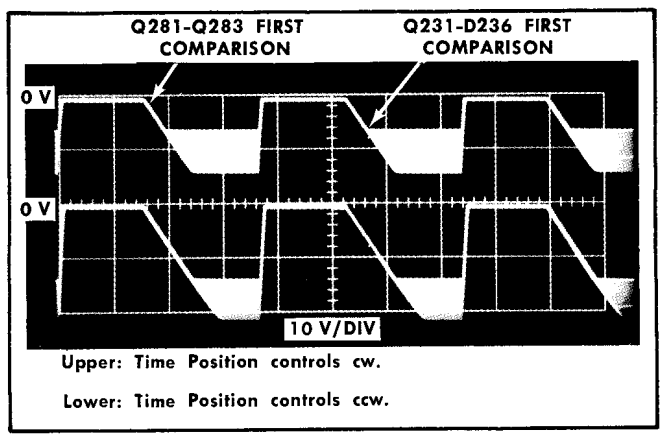


Fig. 4-11. Slewing ramp signal at Q254 collector, D236 anode. (Double exposure.)

Fig. 4-11 shows a double exposure of two slewing ramp waveforms, showing the comparison points for the first sample of a sweep. As shown in the illustration, the Type 3T2 is operating at 1 μs/DIV (10 μs RANGE and ×1 TIME MAG-

NIFIER), and the exposures were made first with the TIME POSITION controls fully clockwise then fully counterclockwise. Each exposure is a time exposure of sufficient time to show all the stopped slewing ramp voltage values for one sweep. Comparing Fig. 4-11 with waveform (O) of Fig. 2-7 may aid in understanding the time window movement action caused by rotation of the TIME POSITION control.

Staircase Inverter Amplifier and Time Position Offset

The Staircase Inverter Amplifier is a three transistor operational (feedback) amplifier with a maximum gain of one-half. The input resistance is the constant resistance 5 kΩ Time Magnifier attenuator, and the feedback resistance is R214. The amplifier is driven (at the Time Mag atten input) with a 0 to +15-volt signal from the Staircase Generator, and by the Variable current from Q210, the Time Position Offset amplifier. Output is from Q220 emitter, which is fed to the two Start Point Steering diodes. The maximum inverted staircase signal output is a 7.5 volt amplitude signal at Q220 emitter ranging from about —2 to —9.5 volts when the Time Position controls are fully clockwise, to about —9.5 to —17 volts when the Time Position controls are fully counterclockwise. Minimum inverted staircase signal output is 150 mV when the Time Magnifier switch is at ×50. (Earlier it was stated that the Timing Ramp Amplifier gain changed from ×2 to ×100 at the two extremes of the Time Magnifier switch positions.) The total range of gain change of the Staircase Inverter Amplifier is from ×0.5 to ×0.01 at the two extremes of the Time Magnifier switch positions. Note that the total gain from the input terminal of the Staircase Inverter Amplifier to the output of the Timing Ramp Amplifier is always unity, even when using the VARIABLE control.

Q212 and Q214 are a differential pair with Q214 temperature-compensating Q212. The inverted signal at Q212 collector drives the output emitter follower Q220. Q220 emitter is returned to Q214 collector so that the amplifier output can rapidly return positive at the staircase signal reset time, and so that equal power is dissipated in Q212 and Q214 collectors.

The Time Position Offset amplifier Q210 is identical with the offset amplifier connected to the Timing Ramp Amplifier. With the Time Position controls fully clockwise, no current is injected into Q212 base. With the Time Position controls fully counterclockwise, Q210 injects about 3 mA offset current into Q212 base, offsetting the Staircase Inverter amplifier output a total of —7.5 volts.

Staircase Inverter amplifier parts with functions not obvious from the above are: R213, which offsets the amplifier output voltage so that the Timing Ramp Comparator (described below) operates correctly for With Trigger operation; R220-C220, R218, and R223, all stabilizing components to assure that the amplifier does not oscillate and C223, which reduces the amplifier high frequency response to reject unwanted short term transient signals.

With Trigger Operation

The following description of the Timing Ramp Comparator and the Start Point Steering diodes, completes the Ramp Generator circuit description.

Start Point Steering Diodes and START POINT Switch

The START POINT switch selects the Before Trigger or With Trigger form of operation. When the switch is at Before Trigger, D228 is biased into conduction, and the Leadtime Comparator and Slewing Ramp Comparator are ready to operate. D225 and Q271 are reverse biased to —19 volts by R275, assuring that the Timing Ramp and Inverted Staircase signals cannot be compared at Q271-D277.

When the START POINT switch is at With Trigger, D225 and Q271 are biased into operation. Q235 saturates taking D228 anode, Q231 base and Q281 base all to —24 volts. This reverse biases D284 in the Slewing Ramp Comparator and assures that the Slewing Ramp and the Inverted Staircase signals cannot be compared.

During With Trigger operation, the START POINT switch disables the Horizontal Dot Position Comparator Memory Gate circuit. The Horizontal Memory will then hold its part of the Servo Loop charged properly for the last triggering rate. Thus, if while operating from a stable trigger the START POINT switch is changed from Before Trigger to With Trigger for a few minutes, and then returned to Before Trigger, the display will return to stable Before Trigger operation without the delay that would be caused if the Horizontal Memory charge were not protected. Fig. 4-12 shows circuit connections to the START POINT switch contacts that are diagrammed with the Ramp Generators.

Two other sections of the START POINT switch serve two other circuit functions. One section prevents the front panel LOW REP RATE lamp from lighting when the switch is at WITH TRIGGER (lower left of diagram 4). The other section selects the proper signal source for the Horizontal Amplifier and Blanking circuits (located at the left edge of diagram 5). The Horizontal Amplifier input signals are plainly identified on the complete block diagram. When the START POINT switch is at WITH TRIGGER, the signal is from the Staircase Generator emitter follower output circuit. When the switch is at BEFORE TRIGGER, the signal is from the Horizontal Memory circuit, Q531 emitter.

Timing Ramp Comparator

Timing Ramp Comparator, Q271-D277, delivers a command signal to the Vertical Strobe Driver transistor when the Timing Ramp and Inverted Staircase signals are compared. This action properly coordinates the X and Y voltages at each CRT dot. The principles of With Trigger operation are described in the first part of Section 2.

Q271 always conducts current during With Trigger operation. Before a comparison, its current is about 0.75 mA, and after comparison its current is about 0.75 mA, and after comparison its current is about 7.5 mA. Before the Timing Ramp starts running negative, D277 is reverse biased and Q271 emitter voltage is set by the inverted staircase signal. As the Timing Ramp rundown voltage reaches about —0.6 volt more negative than Q271 emitter voltage, D277 causes all of the Timing Ramp current to flow in Q271. Q271 collector circuit applies most of that current to Q290 base and a vertical unit strobe drive pulse is formed. Since the Inverted Staircase signal steps a bit more negative for each sample, the comparison times are slewed away from the triggering event

time causing the vertical unit to sample the input signal in time agreement with the CRT horizontal dot position.

During With Trigger operation, The Slewing Ramp Generator may or may not run from about ground to —26 volts each sample. It also may be clamped near ground, or rest at —26 volts full time. Any one of these conditions is normal and will not affect the With Trigger CRT display. Also, the circuits of the Timing Ramp from Q306 through the Timing Ramp Amplifier will continue to operate with no effect upon the CRT display.

STAIRCASE GENERATOR

General

The Staircase Generator circuit (Block diagram in Fig. 4-13) contains a single transistor Trigger Amplifier And Staircase Stepper (Q401) that drives the rest of the circuits. The circuits driven by Q401 are: a Clock Pulse Amplifier that drives an associated digital unit, a Sweep Gating Multivibrator that starts each staircase run, and the Staircase Generator stepping circuit. Other circuits not driven by Q401 are: the Upper Limit Reset circuit that automatically limits the staircase generator maximum amplitude, a Sweep Gate Inverter that drives as associated digital unit, and the Staircase Emitter Follower output stage that drives three loads: 1) the Time Magnifier Variable control at the Staircase Inverter Amplifier input, 2) the Horizontal Amplifier during With Trigger operation, and 3) the Horizontal Dot Position Comparator (Q533).

Trigger Amp and Staircase Stepper

Q401 base circuit is AC coupled and diode clamped so that the Logic Driver output trigger signal positive rise drives Q401 into saturation. C401-R401 discharge and Q401 carrier storage then stretches the trigger pulse so that Q401 collector drives the Staircase Generator circuits with a negative pulse of about 8 or 10 μs duration. The negative step of Q401 collector signal is used once each sweep to trigger the Gating Multi into cutoff and release the Staircase generator to be stepped. The negative portion also discharges the staircase "ladle" capacitor into the staircase generator input. The time sequence of the Logic Driver trigger signal relationship to each step of the staircase signal is shown in Fig. 2-7 at waveform (D) and (E). The time stretching of the trigger signal by Q401 circuit assures that the staircase generator input capacitor has sufficient time to fully transfer its change into the feedback capacitor C448 each step.

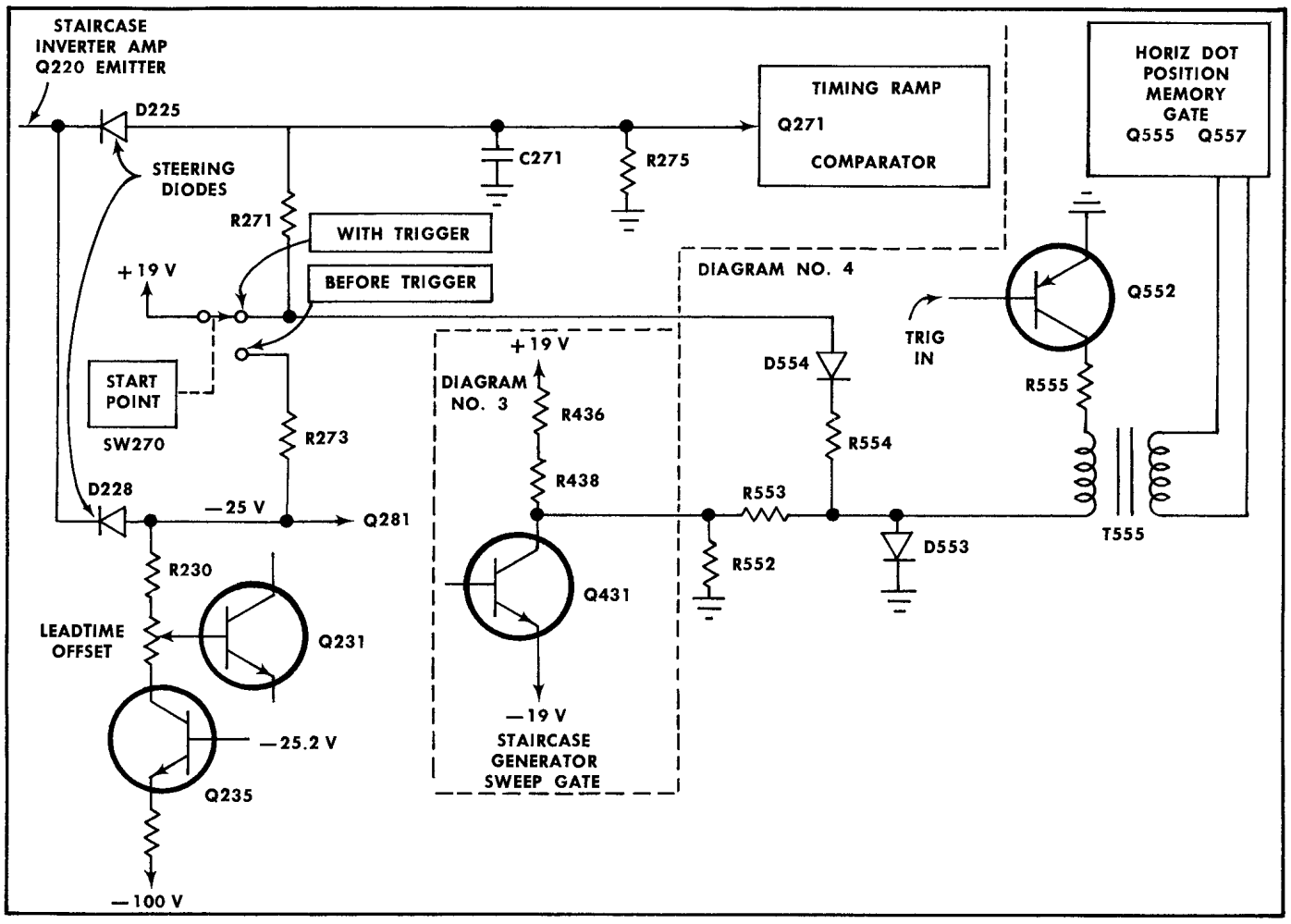


Fig. 4-12. START POINT switch connections.

Staircase Generator Operation (Variable Samples/Div)

Assume during the following discussion that the Gating Multi is conducting so the Staircase Generator can respond to the Logic Driver trigger signal.

The Staircase Generator Amplifier (Q457, Q461, Q465 and Q467) is a high gain operational (feedback) amplifier with capacitors as input and feedback elements. The input "ladle" capacitor is C454 when the SAMPLES/DIV control is in operation, (and C452 in parallel with C453 when the samples per division is calibrated). When Q401 is not conducting, (between trigger pulses) the "ladle" capacitor C454 charges through D454 and R452 to a voltage set by the SAMPLES/DIV control. Then as Q401 collector signal goes negative, C454 charge becomes a current pulse into the amplifier input. The gate lead of Q457A starts to go negative, but the amplifier inverts the signal and applies it back to the input through "bucket" capacitor C448. As soon as C454 is discharged, the output stops charging C448 and the output voltage remains stable until the next trigger pulse. The ratio of input capacitance to feedback capacitance is greater than 10 to 1. Thus, if the input capacitor is charged to +10 volts before Q401 collector goes negative, the output voltage changes less than 1 volt per step as C448 receives the same number of electrons that the ladle capacitor loses during its discharge. Q457A gate lead has a very high leakage resistance, so C448 retains its charge for a considerable amount of time.

When the internal SAMPLES/DIV switch (SW450) is switched up to its 100 position for calibrated digital use, R449 conducts about 1 mA to keep D404 conducting even when Q401 is turned off. When Q401 is turned off, the current passes through D405, D404 and R449 in series. R449 thus assures that driven plates of the staircase ladle capacitor always charges positive to two diode junction drops above +19 volts (when Q401 is cut off), and negative to one diode junction drop above ground (when Q401 saturates).

Each time the ladle capacitor is discharged into C448 (by amplifier feedback action) the output voltage steps positive from its previous value. As the output voltage reaches +52.5 volts, D423 conducts and the Upper Limit Reset transistor (Q420) saturates causing the Gating Multi to cut off; the staircase amplifier then discharges C448. The discharge action amounts to Q431 releasing D448 anode from —19 volts permitting R436-R438 to apply about 5.4 mA positive drive to Q457A gate. This turns Q461 on to heavy conduction, and Q461 collector applies a fast negative signal to C448 through D463. (Q465 is cut off by Q461 fast negative shift and D463 passes the full discharge current to C448.) As soon as C448 and D447 cathode discharge to about 0.3 volts more negative than D447 anode, D447 conducts and stops Q461 turn on by passing the 5.4 mA into Q467 collector. At this time the Staircase Generator output remains at essentially zero volts until the Gating multi is driven into conduction again. (Q467 always conducts 6.3 mA, therefore only 0.9 mA passes through Q465.)

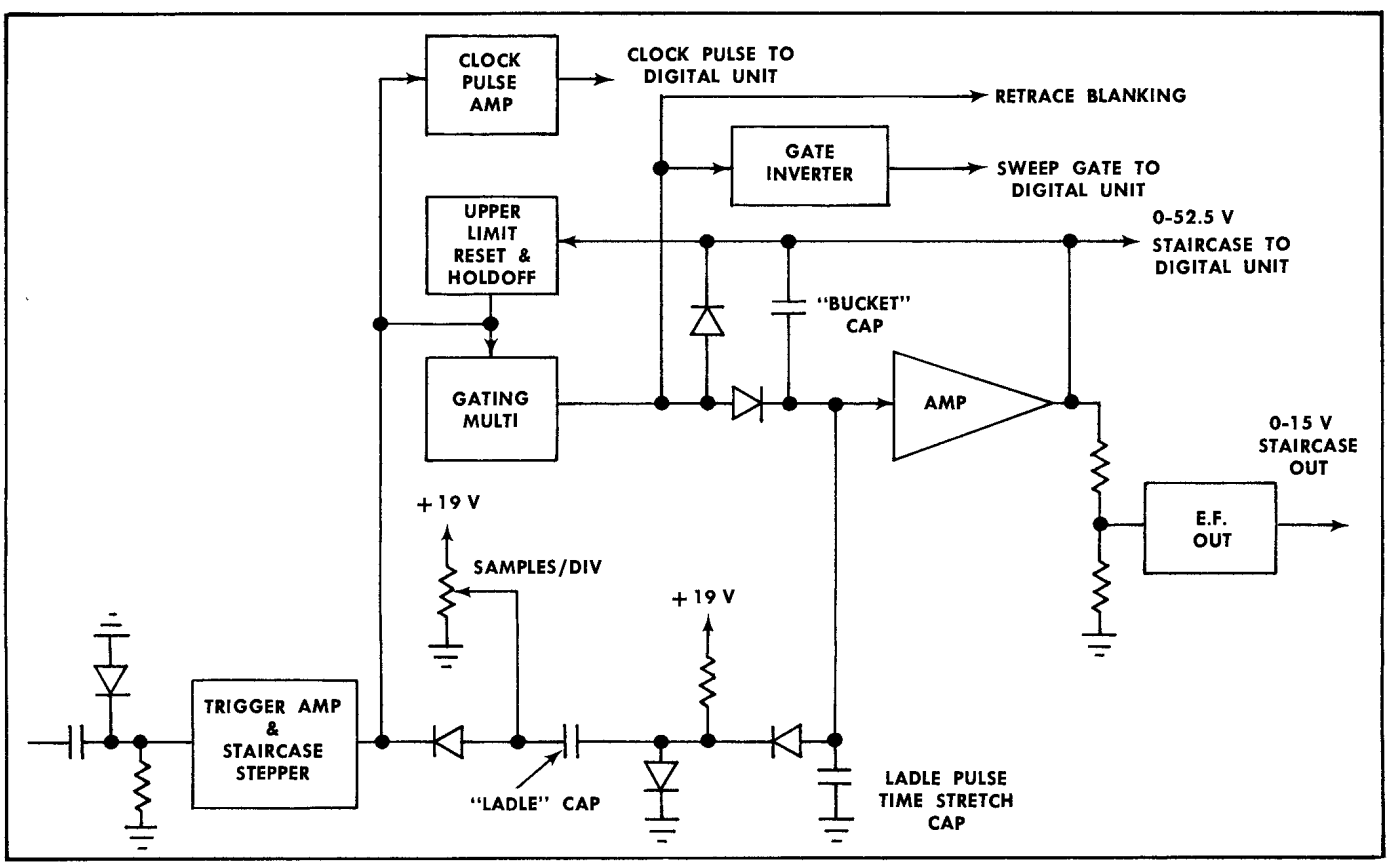


Fig. 4-13. Staircase Generator block diagram.

Q457A gate lead high impedance, plus several matched diode voltage drops, assure that the staircase amplifier input and output leads will both be within a few millivolts of ground when the Gating Multi is cut off. Q457B bias is set to about —0.6 volt by the one-diode drop of D459. The —0.6 volt bias sets Q457B current. Since the two halves of Q457 are essentially identical, Q457B current sets Q457A channel current to its normal value with —0.6 volt bias. Now if Q457A gate voltage is set to zero volts, Q457A source lead biases Q461 into light conduction. Q461 does not quite saturate, and its collector rests at about +1.2 volts. Then Q465 and D464 in series add —1.2 volts' drop to Q465 collector voltage, making the output at D464 cathode zero volts.

With the Gating Multi cut off, D464-Q467 junction goes to zero volts forward biasing D447. D448 applies successively smaller amounts of current to C448, until there is ultimately zero volts drop across it. This then places Q457A gate back to zero and the staircase generator is in a stable condition. If, while the staircase output voltage is held at zero (Single Sweep Operation), trigger recognitions occur, Q401 continues to charge and discharge the ladle capacitor. The ladle ca-

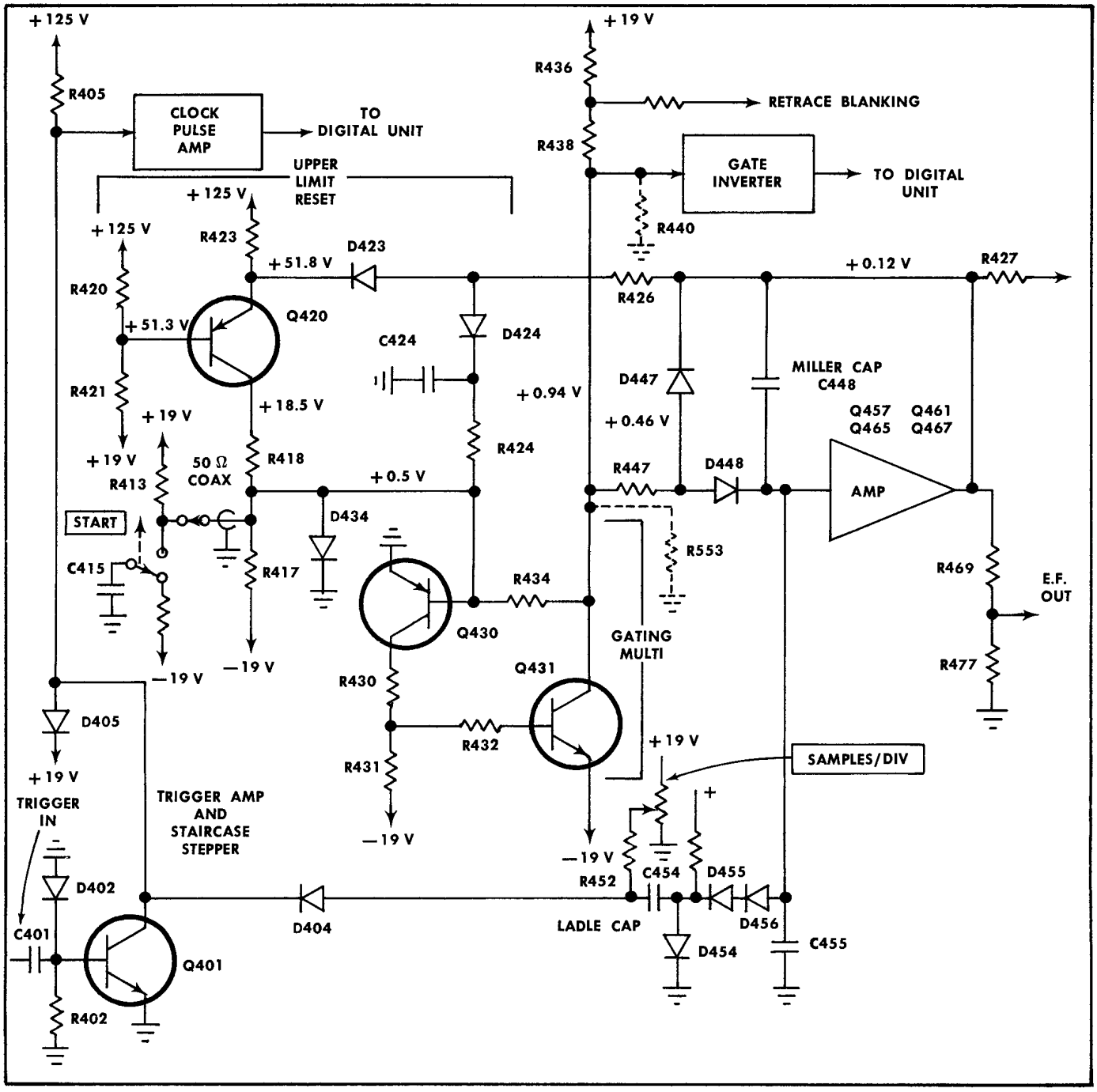


Fig. 4-14. Staircase Generator control circuits.

pacitor charge and discharge current develops a small voltage drop change across the dynamic resistance of D448, and the staircase amplifier output swings about 100 millivolts above and below ground. This action is minimized by C455 between Q457A gate lead and ground. C455 also serves to store the ladle capacitor stepping charge while the staircase amplifier responds at a rate slower than Q401 collector swings.

Functions of some components in the Staircase Generator that are not obvious from the above description are: 1) R454 assures that D454 is conducting slightly when the ladle capacitor starts to charge, which assures a constant number of samples per staircase (sweep) regardless of trigger recognition repetition rate. 2) The series diodes, D455-D456 remain reverse biased except then Q401 is pumping the ladle capacitor charge into C448. D456 assures minimum leakage and D454 provides fast turnoff. The two diodes combine to be almost like a single low-leakage fast turnoff diode. 3) R451 in series with the SAMPLES/DIV control, sets the minimum voltage charge value of the ladle capacitor so full counterclockwise rotation of the SAMPLES/DIV control causes the CRT dot to move one division in ten seconds or longer. 4) R461-C461 and R463-C465 serve to stablize the amplifier and prevent parasitic oscillations. 5) R457 limits the dissipation of Q457A.

Upper Limit Reset and Gating Multi

Fig. 4-14 is a combined schematic and block diagram of the Staircase Generator control circuits. It is drawn with part of the front panel DISPLAY MODE switch and R140 both missing. This then permits the control circuits to be described on a SINGLE SWP basis. NORMAL display mode operation is summarized at the end of the Single Sweep description. Refer to Fig. 4-14 during the following.

The Upper Limit Reset and Gating Multi circuits operate at very low current values. Voltages listed in Fig. 4-14 are obtained when Q401 is receiving 25 kHz triggers, and the front panel DISPLAY MODE switch is at SINGLE SWP. The two resistors, R413-R417 divide the +19 and −19-volt supplies so their junction is zero volts. The 0.25 mA through R418 then forward biases D434 and reverse biases Q430. With Q430 cut off, all drive is removed from Q431 base, and it too is cut off. The circuit will remain in this condition until a negative pulse is received at Q430 base.

As the operator presses the front panel START button, C415 (charged to −19 volts) sends a negative pulse through a 50 Ω coaxial cable to Q430 base. Q430 saturates and drives Q431 to saturation. R434, between Q431 collector and Q430 base, holds the multi in conduction after C415 charge is gone. This action releases the Staircase Generator to step, as described earlier.

Two capacitors, C448 the staircase Miller capacitor, and C424 the Holdoff Capacitor, are charged positive at each staircase step. As the staircase voltage reaches +52.5 volts, D423 is forward biased and Q420 saturates. Q420 collector rises from +18.5 to +51 volts, and R418 current increases from 0.25 mA to about 0.6 mA, just enough to reverse bias Q430 and cut the Gating Multi off. At the time Q431 collector voltage goes positive, more current passes through R424 than when the staircase is reset. When reset occurs, C424 sustains the higher current for a short time. The holdoff action is not significant during Single Sweep operation, but when Q401 drives Q431 base negative during NORMAL operation, C424-R424 prevents the trigger signal from starting a staircase until it is fully reset to zero volts. Refer to diagram number 3 at the back of this manual for the remainder of the Staircase Generator description.

CLOCK Pulse Amplifier

Q401 collector signal swings between essentially ground and +19 volts. The positive value is limited by D405 and the +19-volt supply. The collector signal drives Q406 base through R406 causing Q406 to saturate during the time Q401 is saturated. Q406 collector circuit resistors divide the output signal down to the proper +1.9-volt signal required by the digital unit clock pulse circuits.

Gate Inverter

Q441 inverts the signal from Q431 collector and applies a +7-volt sweep gate signal to an associated digital unit. R440 limits Q441 base current drive when Q431 is off. R440-R441 limit Q431 negative base voltage to protect the base-emitter junction from excessive reverse bias. R444-R445 reduce Q441 conducting collector signal to ground level, and R443-R444-R445 limit the positive voltage to +7 volts.

Staircase E. F. Out and DISPLAY MODE Switch

Q480 and Q481 form a high impedance to low impedance output stage for the Staircase Generator, Manual Scan and External Horizontal Input signals. The dual emitter followers provide a stable low impedance output drive without significantly loading any of the three input sources. Q480 PNP transistor adds one diode drop positive offset to the staircase signal, and Q481 NPN transistor cancels the positive offset by adding one diode drop negative offset. Thus the input and output voltage of the dual emitter follower stage is identical.

External horizontal input signals must operate from ground positive for proper control of the horizontal sampling display. If the input signal exceeds +19 volts, and the EXT HORIZ ATTEN control (R475) is fully clockwise, R476 and D476 protect the emitter follower output stage. Likewise, signals that try to go below −19 volts are limited by R476, and by Q480 going into saturation.

In instruments up to SN B020160, the manual scan voltage drive to Q480 is limited to a calibrated 0 V to 15 V value by the voltage divider R472-R473. Instruments SN B020160-up, have an adjustable control in the voltage divider, R474, which allows the +15 V manual scan voltage source to be accurately set.

R478, C480, R482, R485 and C487 all aid in stablizing the stage against parasitic oscillations.

HORIZONTAL MEMORY and RATEMETER

General

Diagram 4 at the back of this manual contains circuits that operate only for Before Trigger random process sampling. The coordination of horizontal dots for controlled sequence displays is accomplished by circuits in diagram 4. Input signals come from the Timing Ramp amplifier, the Staircase E.F. Output stage, the sweep Gating Multi, the Trigger Circuit and Logic Drivers (three inputs), and a control, the

START POINT switch. One signal output drives the Slewing Ramp Clamp to start the Slewing Ramp running at the right time; and the Ratemeter actuates the LOW REP RATE lamp when the ratemeter ramp circuit runs too far negative (runs for too long a time).

Circuits included in diagram number 4 are: 1) the Horizontal Memory, 2) the Dot Position Comparator, 3) the Horiz Dot Position Comparator Memory, 4) the Ratemeter Ramp, 5) the Ratemeter Memory, 6) the Ratemeter Comparator, and 7) the Correction Matrix that assures the display of at least ½ time window leadtime before trigger recognition.

Horizontal Memory

The Horizontal Memory consists of a unity gain class B input amplifier Q501-Q502-Q504, a memory gate (Q511-Q513) driven into conduction for 5 μs by the Trigger Circuit, and a high impedance to low impedance output stage Q515-Q517-Q520 and Q522.

The unity gain class B input stage provides low impedance drive to the memory capacitor C512. It is class B in order to drive the 0.001 μF memory capacitor a full screen 15 volt change either positive or negative. Q504 does not normally conduct for small changes in timing ramp voltage, but does conduct for large negative signals. The stage operates as if Q501 were an emitter follower, with two signal inversions between Q501 base and Q502 collector.

Assume a positive input signal. Q501 emitter follows the signal and the collector inverts the signal. Q502 amplifies Q501 collector signal and drives Q501 emitter through R504-R505. Negative feedback from Q502 collector to Q501 emitter assures that Q501 emitter follows its base input signal without loss and at a very low output impedance. Both Q501 and Q502 negative return path is through D505 and R506. D505 is a germanium diode, and Q504 is a silicon transistor, thus Q504 base-emitter junction does not normally receive a forward bias.

Assume a large negative input signal. Q501 collector rises to +19.6 volts when D501 conducts. D501 reverse biases Q502 and takes all of Q501 collector current which switches all of R506 current into Q504 base. Then Q504 emitter drives the memory gate and memory capacitor. (The memory gate is described below.)

The high impedance to low impedance output stage provides very low leakage (and long stability) to the charge placed on the memory capacitor C512. The output at Q520 emitter is a low impedance and drives current into both the 6 kΩ Horizontal Amplifier input resistance and the Dot Position Comparator. Q517 is a constant current stage that sets Q515 channel current to a value that requires a Q515 gate to source bias of almost zero volts. The Horiz Output Zero control adjusts Q517 base voltage. This sets the voltage drop across R518, which in turn sets Q517 collector current and Q515 channel current. The control is adjusted so Q515 gate is about —0.3 volt with respect to its source lead. This condition assures Q515 gate leakage is lowest, and C512 charge then remains constant until changed by the class B driver and the memory gate. Q522 is a constant current stage for Q520, the emitter follower output.

The total gain from the Timing Ramp Amplifier input to Q520 emitter is unity, and Q520 memorized output voltage is within millivolts of Q501 input voltage. A DC change of —0.6 volt at Q501 base-emitter junction remains fixed through Q515 source lead. Then an equal +0.6 volt change is added at Q520 base-emitter junction assuring that the memorized Timing Ramp signal is nearly equal to Q501 input.

Memory Gate Circuits

Diagram 4 contains three nearly identical memory gate circuits, differing only in the method of drive. Each consists of two silicon NPN transistors connected base to base and emitter to emitter with the two collectors used as input and output. A pulse transformer secondary drives the base and emitter junctions without DC connection to any other part of the circuit. Between trigger recognition times the transformers do not drive any signal to the joint base-emitter circuit, therefore assuring that both transistors do not conduct. The two collectors are then a very high impedance between the input and output. If there is any voltage difference between input and output, one collector-base junction forward biases and the other collector-base junction reverse biases. The reverse-biased junction allows the remainder of the gate circuit (including transformer secondary) to float on the more negative collector lead. Thus there is always one diode junction that is reverse biased when the pulse transformer does not provide any drive.

A proper polarity pulse applied to the pulse transformer primary applies a turn-on drive to the base-emitter junctions of both transistors. When driven, both transistors saturate and the input and output collector leads are a very low impedance, both at the same voltage. During conduction, the gate affects the charge on the output-side memory capacitor with equal effectiveness for both positive and negative input changes. As the pulse transformer primary drive stops, the secondary self inductance voltage back swing is clamped by a silicon signal diode to protect the gate transistor's base-emitter junctions from reverse voltage breakdown.

The gate conduction duration is controlled primarily by the trigger circuit Logic Driver transistors and their period of saturated conduction. For example, Q511/Q513 are held in firm saturation by base-emitter current drive for at least 5 μs. The series resistance of R510 assures that T510 secondary drives the gate transistor into light saturation with minimum carrier storage so the gate stops conducting immediately after drive is removed. Q555-Q557 drive duration is slightly less than 1 μs without regard to carrier storage. Q601-Q603 drive duration is also slightly less than 1 μs, but may consist of two pulses due to C600-T600 ringing, again without regard for carrier storage.

Dot Position Comparator and Memory

If the signal triggering the Type 3T2 contained no jitter or other instability; if the Slewing Ramp start time occured without jitter in relation to T_o, and if there were no drift in amplifiers or memories, the signal from Q520 emitter would be essentially equal to the Staircase Generator output voltage. Such ideal conditions do not exist. Therefore, the memorized Timing Ramp signal (C512) is compared with the reference Staircase Generator signal at the Dot Position Comparator.

The Dot Position Comparator is a linear differential comparator in which both halves conduct. If there is no voltage

difference between the memorized Timing Ramp signal at Q531 base and the Staircase signal at Q533 base, Q533 collector signal remains at a fixed reference value. Q533 collector voltage changes only when there is a voltage difference between the two signals. The collector can move ±9 volts as Q535 approximately 0.75 mA current path is changed from Q533 to Q531.

The Servo Loop Bal control allows the constant current of Q535 to be altered during calibration. The current value is correct when a triggered stopped display dot (Display Mode switch at MANUAL SCAN) appears at the same CRT horizontal position for both With Trigger and Before Trigger operation.

Q540 is a common base output stage for the Dot Position Comparator. Q540 collector isolates any load current changes (at the time Q555 and Q557 conduct) from the high impedance collector circuit of Q533. The output signal drives the Horizontal Dot Position Comparator Memory capacitor, C559, through either 100 kΩ (R546) or 1 MΩ (R545) and the memory gate Q555-Q557. R545 or R546 limits the amount of charge C559 can obtain whenever there is a Dot Position Comparator signal change. This results in a rather slow response to errors, and a stable dot correction without overshoot or ringing of the servo loop.

The Dot Position Memory output stage is a +9 to −9 volt dynamic range amplifier with high input impedance and low output impedance. Q561-Q563 form a constant current input, variable current output, unity gain impedance converter. Q561 channel current is kept at a constant value by Zener diode D562 holding a constant voltage across R562. With Q561 channel current held constant, its gate-to-source bias remains constant and it passes the voltage of C559 to Q563 base with no incremental loss. Q565 holds the total stage current constant at 5.9 mA. That current divides: 1.1 mA to Q561 and the rest to D562 with a possible +3 or −3 mA output through R563. Even though the total current remains fixed, Q563 current changes from a maximum of 7.8 mA to a minimum of 1.8 mA depending upon the current magnitude and polarity through R563. The use of the output ±3 mA is described below after the Ratemeter, during the Ratemeter Comparator discussion.

The Dot Position Memory Gate control circuit, Q552, assures that the memory capacitor holds a proper charge during sweep retrace time. When the Staircase Generator resets, none of the other circuits follow it closely and the Dot Position Comparator receives what looks like a large correction signal. Thus the Staircase Generator Gating Multi positive swing during staircase reset is converted by R553-D553 to prevent Q552 from pulsing T555. Conduction in D553 removes all of the collector supply voltage to Q552 that is normally provided when the Gating Multi output is at −19 volts.

Q552 collector supply voltage is also removed during With Trigger operation by the START POINT switch connecting D554 anode to +19 volts. Again D553 conducts, even when the Gating Multi output is at −19 volts. This feature of preventing the Dot Position Memory from receiving signals during With Trigger Operation, permits the memory capaci-

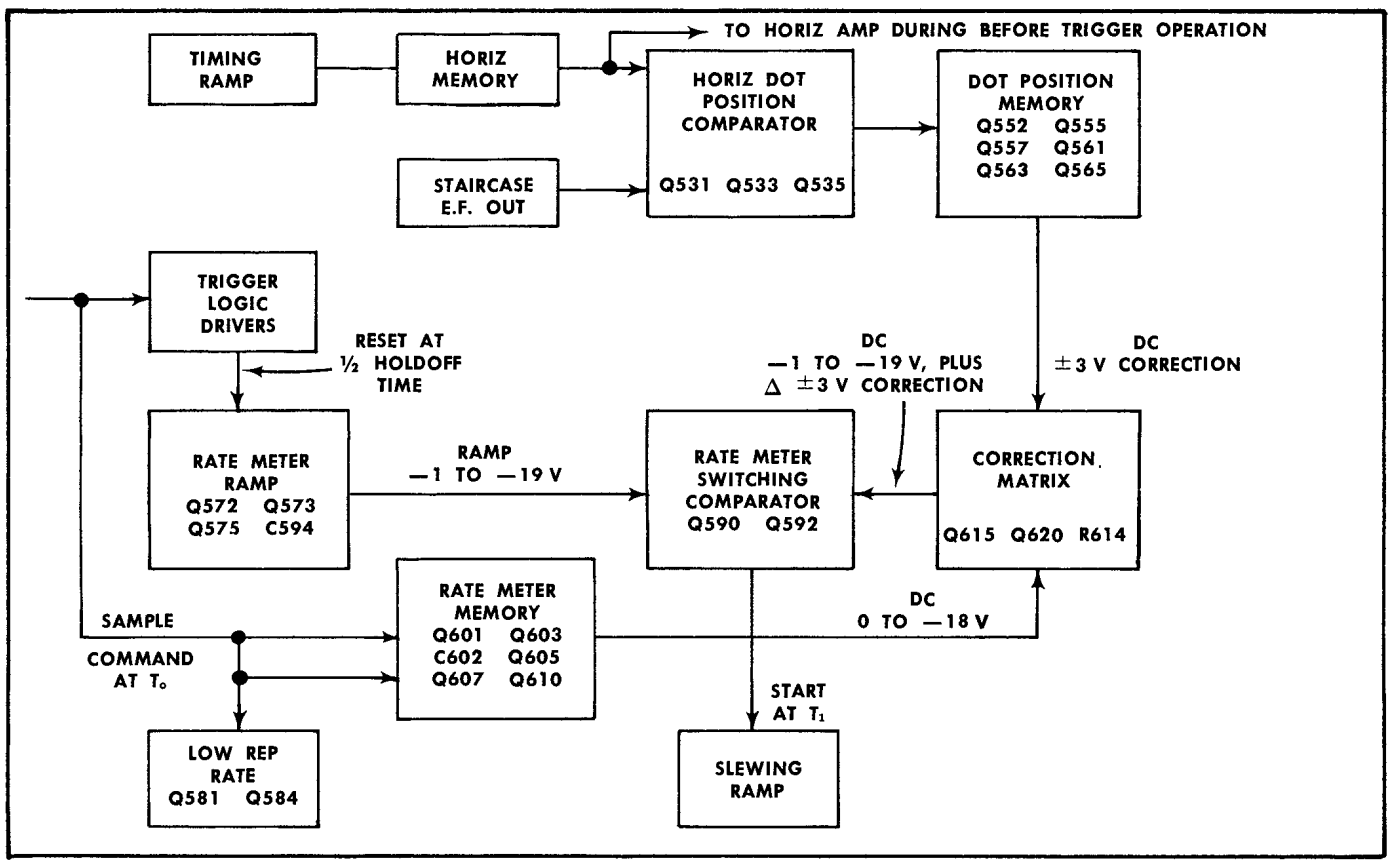


Fig. 4-15. Block diagram of schematic diagram number 4, plus the Timing Ramp, Staircase E.F. Out, and Slewing Ramp blocks.

tor to hold its proper charge for a while when changing the START POINT switch from Before Trigger to With Trigger. Then, if the operator decides to return to Before Trigger operation (while observing the same signal that charged C559) the display will return to the CRT sooner than it would have had the memory capacitor charge been changed by With Trigger operation. D554 disconnects Q552 collector pulses from the (With Trigger) Timing Ramp Comparator and D225 (Start Point Steering Diode) circuits when operating with the START POINT switch at Before Trigger.

Ratemeter Ramp, Ratemeter Memory, Correction Matrix and Low Rep Rate Circuits

As described in Section 2, the Ratemeter Ramp is reset at one half the holdoff period, restarts automatically, and is sampled at the next trigger recognition, T_o. The Ratemeter Memory does the sampling of the ramp to memorize the ramp voltage. The DC voltage out of the Ratemeter Memory, and the DC voltage out of the Horizontal Dot Position Comparator Memory are both converted into current signals at the Correction Matrix circuit and supplied to the Ratemeter Comparator as one correcting voltage.

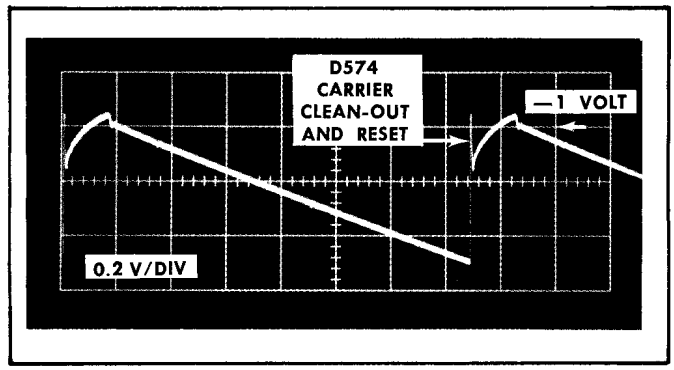


Fig. 4-16. Ratemeter Ramp.

See Fig. 4-15 for a block diagram of diagram 4 with three added blocks: the Timing Ramp, the Staircase E.F. Out, and the Slewing Ramp. The Slewing Ramp is started by a signal from the Ratemeter Comparator. The Ratemeter Comparator is a switching comparator that delivers a pulse output signal at the time the Ratemeter Ramp goes more negative than the signal out of the Correction Matrix circuit.

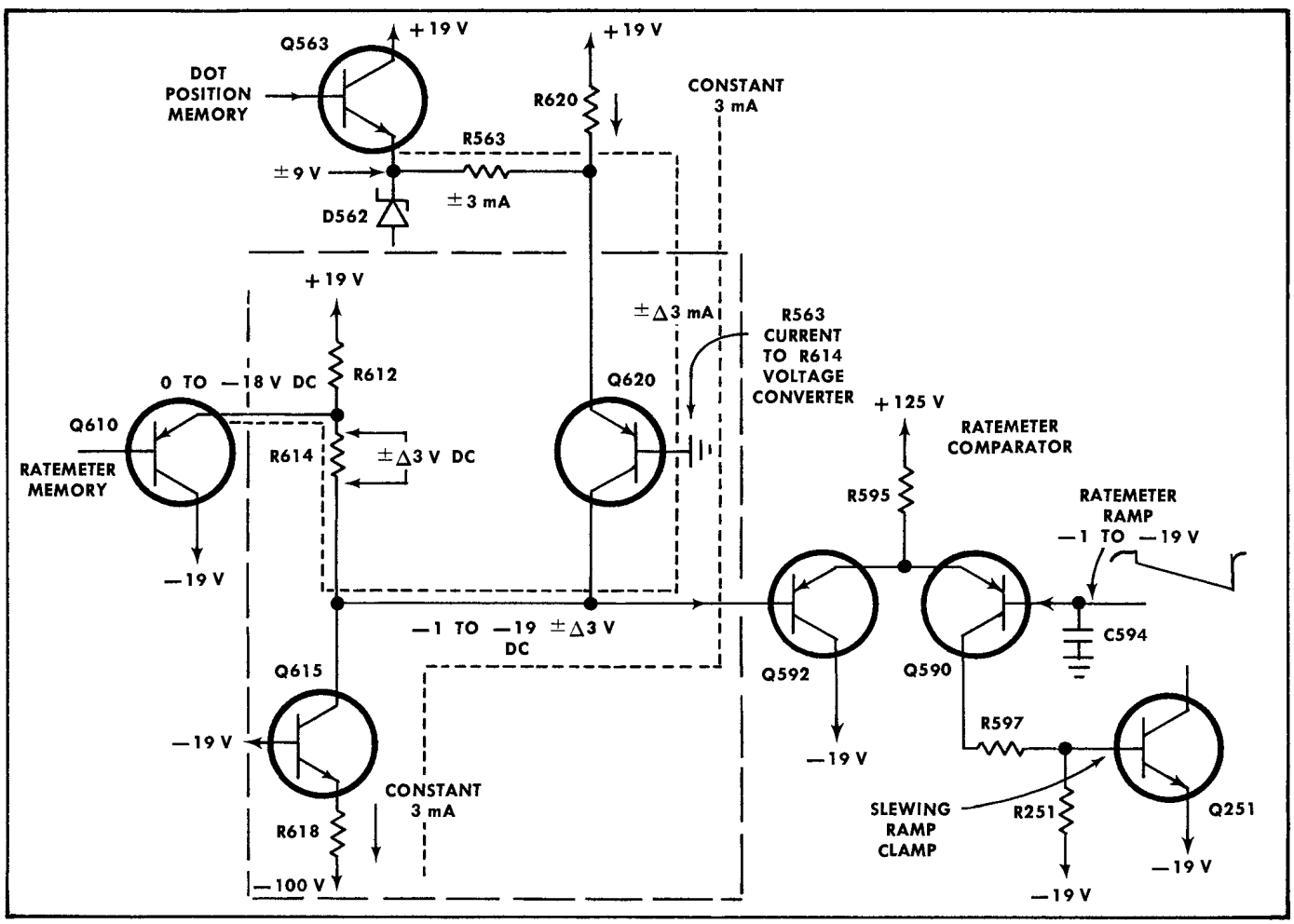


Fig. 4-17. Correction Matrix (outlines) current paths, and voltages applied to Ratemeter Comparator.

The Slewing Ramp start time is alterable by two separate system changes, a change in the trigger signal rate, or a change in the Timing Ramp memorized voltage that is compared to the reference Staircase signal. Both changes cause corrections to the Slewing Ramp start time, but the first is due to external causes, and the second is due to internal causes. Thus the Ratemeter Comparator is the point at which both external and internal timing changes are combined into one common signal that then starts the Slewing Ramp running at a "best guess" time ahead of the next trigger recognition.

The Ratemeter ramp consists of a Reset Multi (Q572-Q573), a constant current capacitor charging transistor (Q575) and the ramp capacitors that are charged at the constant current rate (C591 through C594). The Reset Multi conducts when driven by the Logic Drivers at one half the holdoff period. (See waveform (I) in Fig. 2-7 and Fig. 4-16.) The multi remains in conduction until whatever negative charge was in the ramp capacitor(s) is nearly discharged. When Q573 emitter reaches —0.95 volt, its collector current (mainly from the ramp capacitor) is reduced until R574 current turns D574 on and D572 off, which removes the turn-on bias to Q572. Q572 current drops to zero and both transistors stop conducting. Immediately constant current transistor Q575 starts the ramp capacitor(s) charging negative.

Sometime during the Ratemeter negative ramp, the ramp voltage forward biases the switching comparator transistor Q590 to apply a turn-on pulse to the Slewing Ramp. Then the next trigger recognition causes the Ratemeter Memory Gate to conduct briefly and apply a charge into the memory capacitor C602.

At the next ½ holdoff time the Logic Drivers again pulse the reset multi into conduction. The rate meter ramp capacitor discharge path is through Q573 emitter-collector path, D572, and Q572 base-emitter junction. The base-emitter junction of Q572 is protected from damage when discharging the larger ramp capacitors (C591 or C592) by the 20 Ω resistors in series with the capacitors.

When the Reset Multi is not conducting, R572 assures Q572 remains cut off, and R576 assures Q573 remains cut off.

The Ratemeter Memory capacitor voltage is applied to the Correction Matrix circuit through the high impedance to low impedance circuit of Q605, Q607 and Q610. Q607 is the constant current source for Q605 channel current. With the channel current through Q605 constant, its gate to source bias voltage does not change as C602 voltage changes. Q605 source lead drives emitter follower Q610 base, and Q610 emitter is a low impedance voltage drive source to the Correction Matrix circuit. It is the voltage out of Q610 emitter that receives correction by the Dot Position Memory to alter the Slewing Ramp start time.

The Correction Matrix circuit is redrawn in Fig. 4-17 to show the two electron paths, 1) a constant 3 mA to place Q615 and Q620 into active operation, and 2) a +3 mA to —3 mA signal current to cause a correcting voltage change across R614. Q615 and Q620 collectors are both a very high impedance. The high impedance allows their voltage to be moved by Q610 emitter from about —1 to —19 volts without changing the current in either transistor. Likewise, the Dot Position Memory can change Q620 current, but Q615 "long tail" emitter (constant current, high impedance collector) doesn't recognize the change, forcing Q620 current change to affect only the voltage drop across R614. Thus it is actually R614 that combines the Ratemeter Memory signal and the Dot Position Memory signal to provide the Rate Meter Comparator with one DC correction voltage. The rest of the Correction Matrix is required to force the Dot Position Memory changes into R614 only. The correction signal across R614 does not extend Q592 base signal voltage range greater than 18 volts. The limit is —1 to —19 volts, but Q610 emitter voltage can be corrected as much as ±3 volts within the 18 volt limits. Actual operating conditions require far less than ±3 volts correction. The usual amount at Time Magnifier ×1 is typically —1.4 volts because Q610 emitter is about +1.2 volts from C602 memory voltage.

The 1 ms Correction control (R622 and R623) is used to offset the Dot Position Memory output current (and resulting R614 voltage drop) when operating the RANGE switch at 1 ms. Note that the Ratemeter Ramp capacitor is the same for both the 100 μs and 1 ms ranges. All ranges except 1 ms operate with the rate meter ramp slope 10^3 times longer than the timing ramp slope. At 1 ms range, the rate meter ramp slope is only 10^2 times longer than the timing ramp slope. (The 100 μs Range permits operation down to 10 Hz. Horizontal Memory leakage will not tolerate lower repetition rate operation. Therefore the 100 μs ramp is also used on the 1 ms range.) The additional 1 ms Correction current into Q620 emitter (and resulting voltage across R614) programs the slewing ramp start to be ½ Time Position Range ahead of T_o on the 1 ms range. The 1 ms Correction current speeds servo positioning of the sampling display when changing from the 100 μs to the 1 ms Range.

The Low Rep Rate circuit contains two transistors that are normally biased to cut off. Q581 is in series with neon bulb B580, and Q584 drives Q581. When both transistors are not conducting, B580, the LOW REP RATE lamp is dark. When Q584 is caused to conduct, Q581 saturates and B580 glows.

Q584 emitter circuit is returned to —17.3 volts at the junction of R587-R588. D588 is in series with Q584 emitter to assure no connection of the Ratemeter Ramp to R587-R588 should Q584 base-emitter junction become excessively reverse biased. The Ratemeter Ramp positive voltage takes Q584 base about 16 volts more positive than R587-R588 junction, and D588 assures that Q584 base remains a high resistance and does not load the ramp.

As the Ratemeter Ramp voltage is permitted to run negative to —19 volts (either by very low trigger signal repetition rate, or the TRIG SENSITIVITY control being turned fully counterclockwise and locking out triggers) Q584 is forward biased into saturated conduction by Q575 current. Q584 collector applies turn-on bias to Q581 through R584 and Q581 saturates, turning B580 on. Both transistors turn off whenever the Ratemeter Ramp voltage is more positive than about —18.1 or —18.2 volts. The positive supply to B580 is opened by the START POINT switch for With Trigger Process sampling so the LOW REP RATE lamp will not operate.

HORIZONTAL AMPLIFIER and BLANKING

General

The Horizontal Amplifier and Blanking, diagram 5, contains the transistor CRT horizontal deflection plate drivers, the spot position indicators, and the overscan blanking circuit.

CRT Driver

The CRT Driver amplifier consists of a two transistor operational amplifier, Q741-Q751, and a three transistor variable gain differential output stage, Q761-Q771-Q781. Both amplifiers require external connections in the vertical sampling unit for proper operation. These connections are shown in Fig. 4-18. The external connections control the input signal sources for the differential output amplifier Q771-Q781. When the vertical unit mode is not X-Y, Q781 receives a Type 3T2 staircase signal that horizontally positions the CRT dot, and Q771 base rests at —0.6 volt. When the vertical unit mode is X-Y, Q781 base is held firmly at +9.1 to +9.5 volts and Q771 base is driven with a ±5 volt signal centered on +9.4 volts. (The vertical unit Channel B signal is centered on +10 volts, offset —0.6 volt by emitter follower Q671.)

Input Operational Amplifier. The input operational amplifier, Q741-Q751, operates with a stage gain of 0.66 when the DISPLAY MAG switch is at ×1. The stage gain is 6.66 when the DISPLAY MAG switch is at ×10. Q741 is an inverting high gain amplifier with a collector voltage of ap-

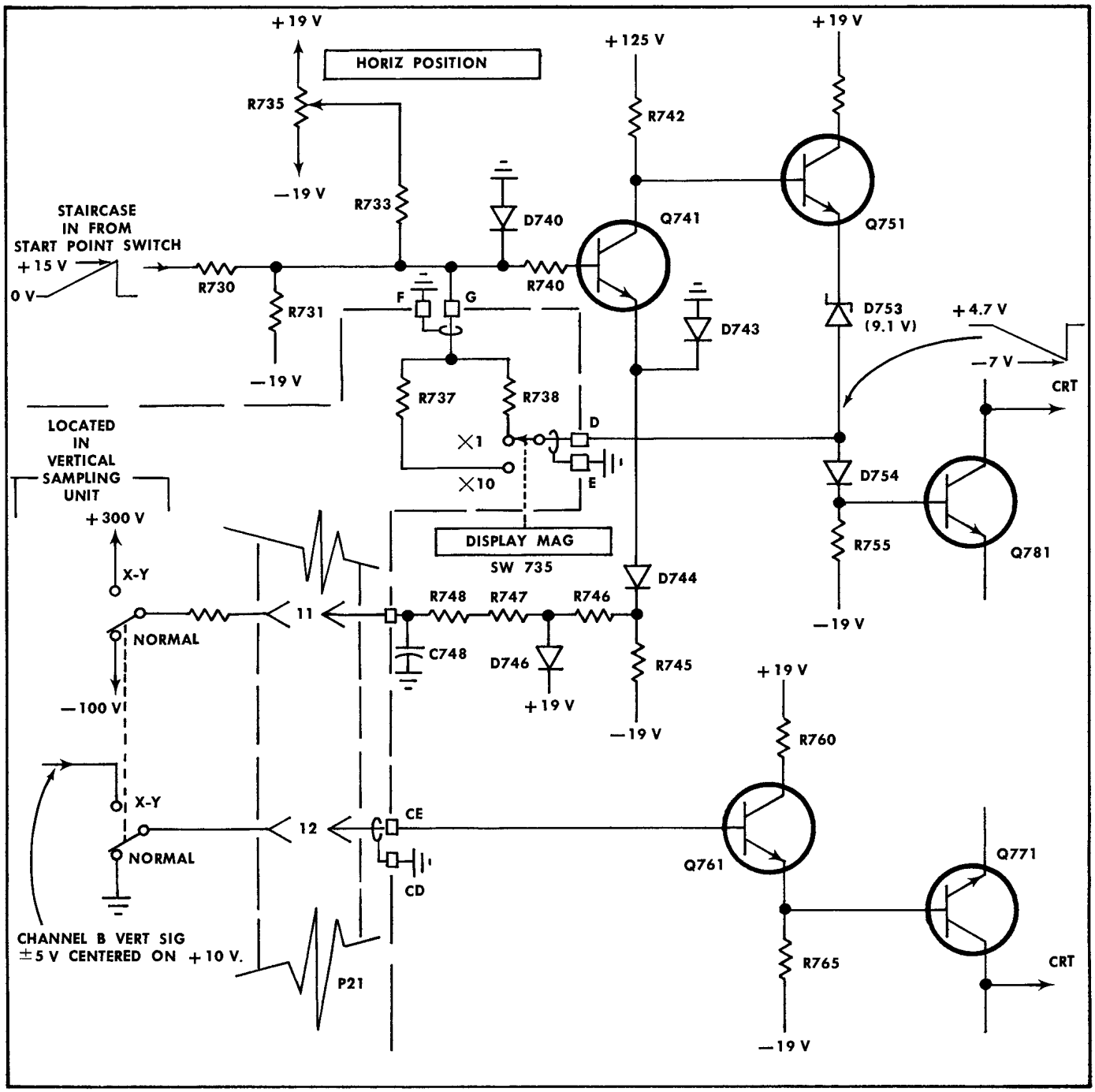


Fig. 4-18. Horizontal amplifier connections from vertical unit.

proximately +9 volts when the CRT dot is at center screen. Emitter follower Q751 and Zener diode D753 offset Q741 collector +9 volts back to zero volts assuring that Q771 and Q781 are each conducting equally at CRT screen center.

Q741 base lead is the input signal equivalent ground point where input signal current is equaled by feedback current. There are essentially three input resistors, 1) R730 for the staircase input, 2) the HORIZ POSITION control and R733, and 3) R731 provides a DC offset current so that the trace starts at the CRT left edge for zero voltage signals when the HORIZ POSITION control is centered. D740 conducts when Q751 base reaches +19 volts and Q751 emitter stops going positive as the input signal continues negative whenever the spot is driven considerably off screen to the left.

Q741 emitter circuit contains three diodes and associated resistors. When the vertical unit mode is not X-Y, D746 does not conduct, and both D743 and D744 do conduct. D743 is forward biased by both R745 and the circuit of the vertical unit. Thus, Q741 emitter rests at —0.52 volts and D743 is a low resistance between the emitter and ground. When the vertical unit mode is X-Y, D746 does conduct, and D743 and D744 do not, thus removing any current from Q741 emitter. Q741 collector then goes positive until Q751 base-collector diode junction forward biases taking all of R742 current. Q751 emitter rises to nearly +19 volts and D753-D754 sets Q781 base firmly at +9.4 volts.

Q761 base is grounded when the vertical unit mode is not X-Y. When the vertical unit mode is X-Y, Q761 is driven by the Channel B vertical output signal which arrives at a sensitivity of 1 V/Div, centered on +10 volts DC.

Output Differential Amplifier. The linear output differential amplifier employs two special high voltage transistors, Q771-Q781. These transistors have a BV_{CBO} rating of 300 volts, and are used to drive the CRT horizontal deflection plates directly. Both transistor base lead input voltages are limited to operation between —19 and +19 volts. The emitter circuit is both "long tail" and highly degenerative between transistors, assuring that neither transistor cuts off at —19 volts in, nor can one cut the other off if its base goes to +19 volts.

Assume both amplifier bases at zero volts; R774 and R784 assure that both transistors conduct 2 mA. As Q781 base voltage goes positive, its emitter goes positive, applying a positive turn-off signal to Q771 emitter through R782-R785-R772. Q781 then increases its current, and Q771 decreases its current; Q781 collector goes negative and Q771 collector goes positive. The amplifier thus converts a single input signal to a push-pull output signal. The amount of signal coupled from one emitter to the other emitter is made adjustable by the front-panel HORIZ GAIN control, R785. R785 permits the operator to alter the output stage gain sufficiently to mate the horizontal deflection to the particular oscilloscope in which the Type 3T2 is operated.

Spot Position Indicators

The horizontal spot position indicator lamps are driven by a switching comparator amplifier, Q791-Q793. The comparator is driven by the output amplifier emitter circuit by the voltage across the HORIZ GAIN control. If the CRT driver output amplifier transistor conduction differs enough to cause about 0.5 volt difference at Q791-Q793 bases, the most positive-base transistor saturates and the other transistor is cut off. The long tail resistance in the emitter of the lamp drivers permits the CRT driver emitter circuit to float between +19 and —19 volts and still operate the switching comparator properly. Whichever transistor saturates, it then turns on the associated neon lamp in its collector lead. The cutoff transistor assures that its collector circuit lamp has no current and therefore remains dark.

The two series base resistors R790-R792 assure that the pulse caused by neon ignition is not coupled back into the Timing Unit circuits. (Without the series base resistors, each time a neon turns on, its effects would be seen on the CRT.) The large resistance between transistor collector leads assures that the off transistor collector voltage does not rise to +125 volts. When a transistor is cut off, its collector voltage is held at about +70 volts by Townsend (dark) current through the associated neon passing through R796 to the other collector. R796 keeps the off transistor collector about +10 to +15 volts from its emitter (the emitter voltage being set by the other neon drop and its saturated transistor). The circuit never operates with both transistors cut off.

Blanking

The blanking circuits drive one of the cathode ray tube deflection blanking plates to turn off the electron beam whenever the dot is moved, or whenever it exceeds ten divisions of horizontal scan. The circuits have three input signal paths, 1) interdot blanking from the Vertical Strobe Driver (Q290) to D700, 2) retrace blanking from the Staircase Generator (R437) to D701, and 3) the normal horizontal input signal to Q741 at Q722 emitter and D709 cathode. The output negative-going blanking signal is taken from D712 cathode and applied through D713 to the CRT deflection blanking plate pin 6, through pin 13 of the interconnecting plug P21. The output voltage is +125 volts when the electron beam is allowed to strike the CRT phosphor and generate a dot. The output voltage is about +43 volts when the electron beam is deflected and does not reach the phosphor, thus blanking off the dot. Q710 is at cutoff during the blanking time, and conducts only as the CRT deflection blanking plate is taken positive at the end of the blanking time. Q710 charges the circuit capacitance (from +43 volts to +125 volts) much faster than R715 could do alone.

Q705 is the blanking amplifier. It has two input signal paths: 1) into its base for interdot and retrace blanking, and for greater than +15 volt horizontal input signals that would overscan the CRT to the right during Before Trigger process sampling, and 2) into its emitter for horizontal input signals that are negative and would overscan the CRT to the left during Before Trigger process sampling.

Overscan Blanking. See Fig. 4-19. Q705 normally conducts only 1 mA of current, set by: D703-D704 which set Q705 base voltage at +0.9 volt, and 100 kΩ emitter return resistor to the —100-volt supply. At 1 mA current, D712 cathode voltage would be at +200 volts ,except that D715 limits the positive value to +125 volts, and D712 limits Q705 collector to +82 volts. Q710 will conduct any stray CRT deflection blanking electrons to the 125-volt supply, but is considered at cutoff as far as the blanking circuit is concerned.

If the CRT Driver horizontal input signal voltage goes negative, D709 becomes forward biased and connects the driving transistor low impedance emitter (Q520) to Q705 emitter. Q705 increases its current sufficiently to saturate, taking Q710 base to approximately +43 volts, deflecting the CRT beam and blanking the CRT spot. Should the input signal try to go several volts negative, most of Q520 emitter current is taken to ground by D705 (connected to its base lead), and D706, connected between Q705 connector and ground.

If the CRT Driver horizontal input signal voltage goes more positive than about +15 volts, Q722 conducts and applies a positive signal to Q705 base. (Q722, PNP transistor, has a base-emitter junction reverse voltage breakdown rating of 20 volts.) When Q705 base is taken positive, D708 (emitter to ground) is forward biased into conduction, bypassing the degeneration of R708. Q705 is then a high gain amplifier, which saturates, and again places the deflection blanking plate at +43 volts to turn off the overscanned CRT dot.

Interdot Blanking. Fig. 4-19 shows the Vertical Strobe Driver circuit connections to the blanking circuit. The voltage divider, R296-R700, sets D700 anode voltage at about —1 volt when the CRT dot is in view, and at about +1.8 volt when

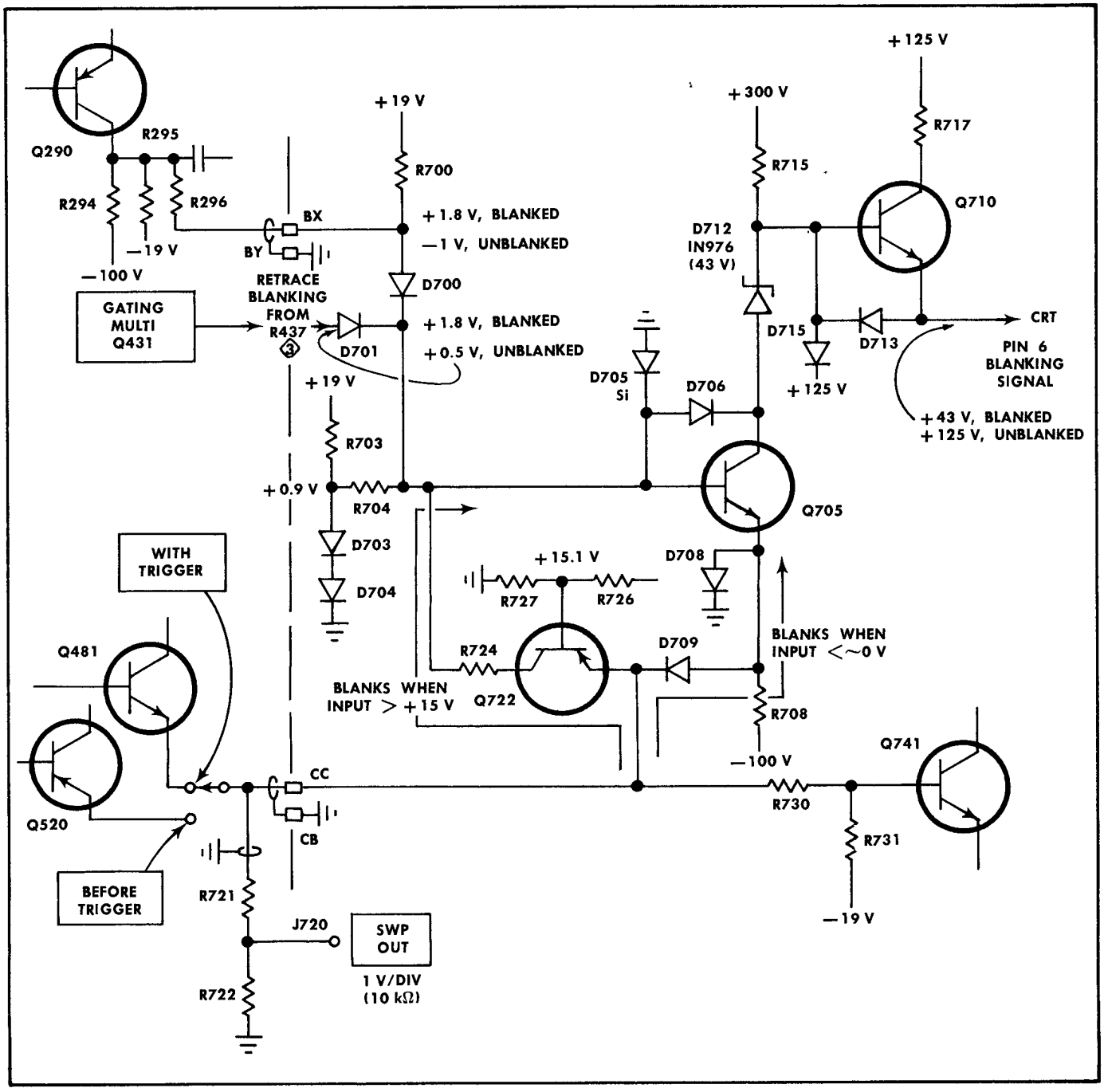


Fig. 4-19. Type 3T2 Blanking circuits.

the dot is blanked. The signal is essentially a square wave that holds the CRT dot blanked for the length of time that Q290 conducts. The positive signal saturates Q705 and blanks the CRT between dots.

Retrace Blanking. The Staircase Generator Gating Multi turns off the CRT beam during staircase reset time. The Gating Multi signal takes D701 anode to +1.8 volts when the staircase is being reset, and rests at about +0.5 volt the rest of the time. The positive signal saturates Q705 and blanks the CRT.

The +1.8 volt maximum positive voltage of the above two blanking signals is set by the diode drops of D708 plus Q705 base-emitter junction and either D700 or D701. Current is limited by the series resistor between the driving transistor and either D700 or D701.

POWER SUPPLY

General

The power supplies and power distribution diagrams show not only the power supply active circuits, but also the interconnections with the oscilloscope and distribution through the Type 3T2 circuits. The oscilloscope main frame provides the —100, —12.2, +125, and +300 Volt power, and 6.3 volts AC to T801 for the internal —19- and +19-Volt Supplies. The —27 Volt supply is a simple shunt Zener diode supplied current by the main frame —100 Volt supply. The —12.2 Volt supply is used only by the incandescent lamps in the front panel TIME/DIV readout panel.

Main Frame Shunts

The main frame power supplies are shunted within the Type 3T2 to provide the correct regulation for the current demanded by the companion Vertical Sampling Unit. Diagram 6 shows the shunts and shunt connections at P21. Pins 15 and 20 are joined, connecting the main frame maximum shunt (minimum resistance) across the 125-Volt supply. In addition, the Type 3T2 allows more +125-Volt supply current to be added to that available from the main frame, taken from the +300 Volt supply by R803. R802, between P21 pins 6 and 10 shunts the main frame +300 supply regulator for proper regulation. R801 shunts the oscilloscope —100-Volt supply for proper regulation.

Internal Supplies

The oscilloscope main frame provides 6.3 volts AC to power transformer T801. The input lead is fused by F801, soldered in place on the readout card. The two transformer secondary windings apply approximately 55 volts AC each to two-diode full wave rectifiers for the —19- and +19-Volt supplies. Each rectifier system is located on the Trigger Board, with the filter capacitors mounted centrally near the instrument rear panel. The —19 Volt supply is the reference for the +19 Volt supply.

—19 Volt Supply

Zener diode D834 provides a zero temperature coefficient 5.1 volt reference for the —19 Volt suply regulator circuit. It is located in the emitter lead of comparator-amplifier Q831. The other Q831 input is at its base lead, taken from voltage divider R840-R841-R842. Q831 is temperature compensated by D832, in series with its base signal.

Correction signals to Q831 are applied directly through D834 to the emitter. Signals applied to the base are an attenuated value of that connected to the emitter. The difference between the two correction signals is amplified by Q831 and applied to emitter follower Q835. Q835 provides current gain to the amplified and inverted correction signals, and drives the series transistor Q841.

Assume the 19-Volt supply load is reduced, making the output voltage more negative. Q831 emitter is driven more negative than the base (the equivalent of a positive base signal) causing the collector current to increase. Increased collector current drives Q835 base more negative, and Q835 emitter drives Q841 base more negative, decreasing its collector current. To decrease Q841 collector current is in essence to increase its emitter to collector dynamic resistance. Increased resistance from Q841 collector to emitter causes the current through it to increase the voltage drop across it. As Q841 voltage drop increases, the rectified 28.5 volts across filter capacitor C825 is shifted positive, which applies the proper polarity correction to the —19 Volt output voltage. The result, then, of supply regulator action is to move the +9.5 volts at Q841 collector in a direction to keep the output —19 volts constant.

Components not described above provide the following functions: C842 assists to reduce the supply high frequency output impedance. R832 provides a small forward bias current to D832, assuring that it always connects the —19 VOLTS control to Q831 base. R834 provides the proper current to D834 to place its operation at its zero temperature coefficient point. C830 stabilizes Q831 against parasitic oscillations. R825 and R827 limit the surge charging currents into filter capacitor C825 to a safe value for both the transformer secondary and the rectifier diodes.

+19 Volt Supply

The +19 Volt supply is almost identical to the —19 Volt supply. The major differences are: Q811 is temperature compensated by D814 at its emitter lead, and the correcting signal is applied to Q811 base only. Regulator action is identical with Q821 collector to emitter resistance varied by feedback action to provide the correct voltage drop across the resistance of the load. The reference voltage is the —19 Volt supply applied to R822 and compared against essentially ground voltage, the voltage at D814 cathode.

Changes of the +19 volts output are divided by R820-R821-R822 and applied directly to Q811 base. Q811 amplifies and inverts the signals to drive Q815, which drives Q821 which in turn changes its resistance to restore the output voltage at its emitter back to +19 volts.

—27 Volt Supply

The —27 Volt supply is taken from Zener diode D850. The two R-C filters between D850 and the two loads filter normal Zener noises from the loads.

READOUT SWITCHING

Four switches on the Type 3T2 front panel affect the illumination of the lamps in the TIME/DIV readout panel. The Time/Div value and unit is affected by three: the RANGE, TIME MAGNIFIER and DISPLAY MAG switches. The readout value is scaled 10×, and the units lamps are turned off any time the switch mounted with the Time Magnifier VARIABLE control is actuated by turning the control away from the CAL position. The logic is all part of the switches, with no transistors or other three-terminal active devices in the circuit. Diodes are in series with each lamp to its common lead to assure isolation between the lamps, so that only the proper one of a group turns on at a time.

DIGITAL SWITCHING

The digital switching diagram 9 contains the circuits of the five switches that affect the associated Digital Unit operation when operating the Type 3T2 in a Type 567 Oscilloscope.

READOUT RESISTOR CARD

The readout resistor card diagram 10 contains all the parts mounted on the card. The parts include part of circuits of 1) the trigger holdoff circuit, 2) the Time Position circuit of the Ramp Generators, 4) the ratemeter of the Horiz Memory & Ratemeter diagram, 6) the Power Supply, and 8) the readout circuit resistors and isolation diodes.

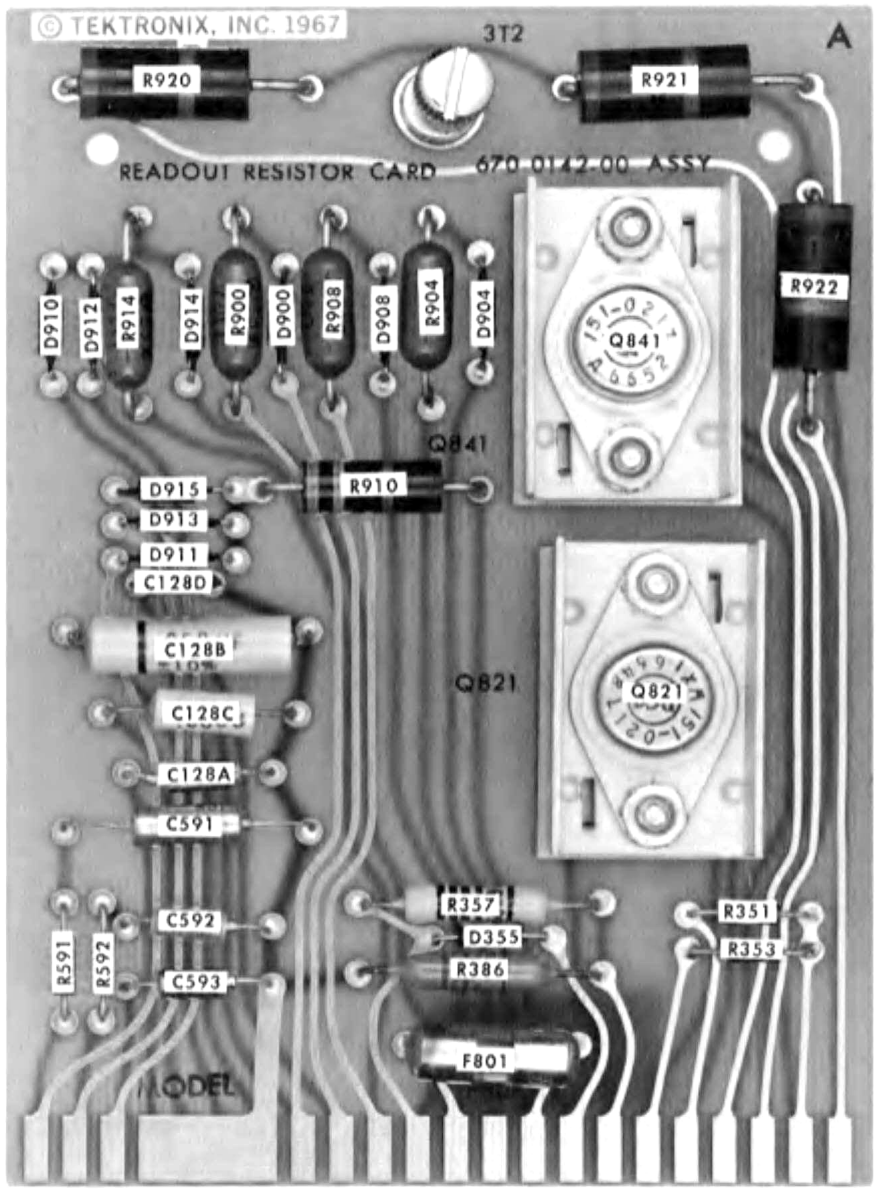


Fig. 5-6. Readout Resistor Card.

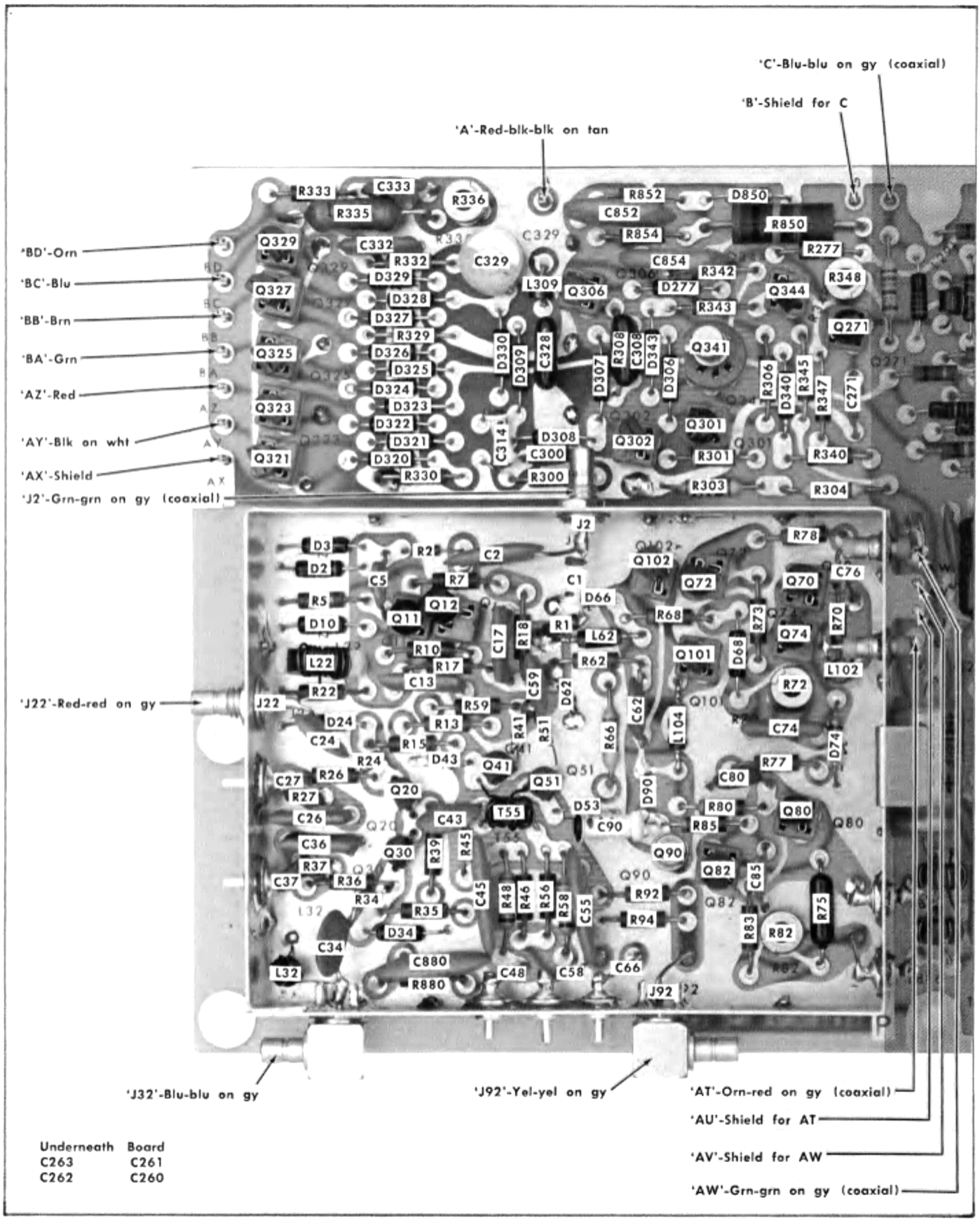


Fig. 5-7A. Trigger Board, Left.

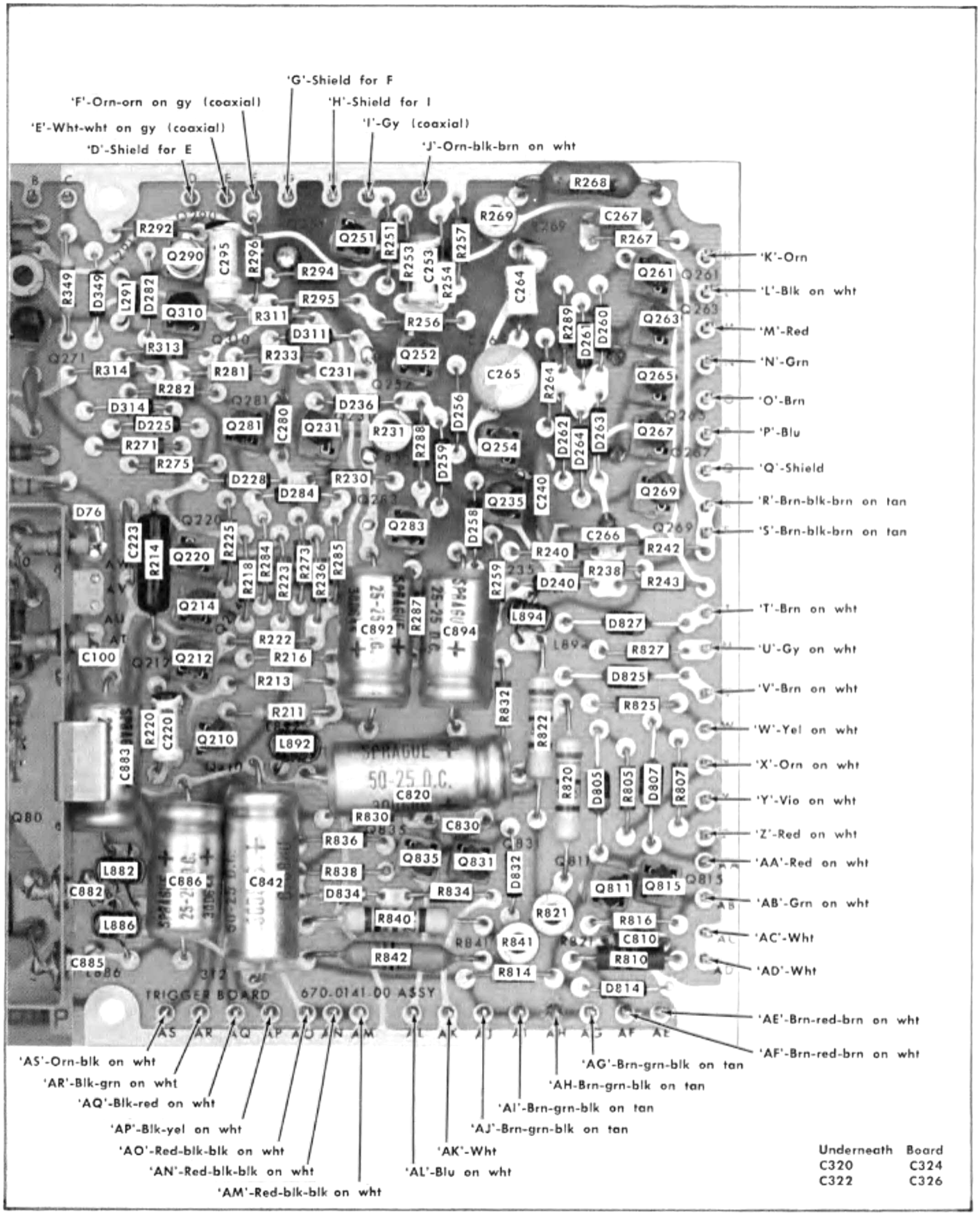


Fig. 5-7B. Trigger Board, Right.

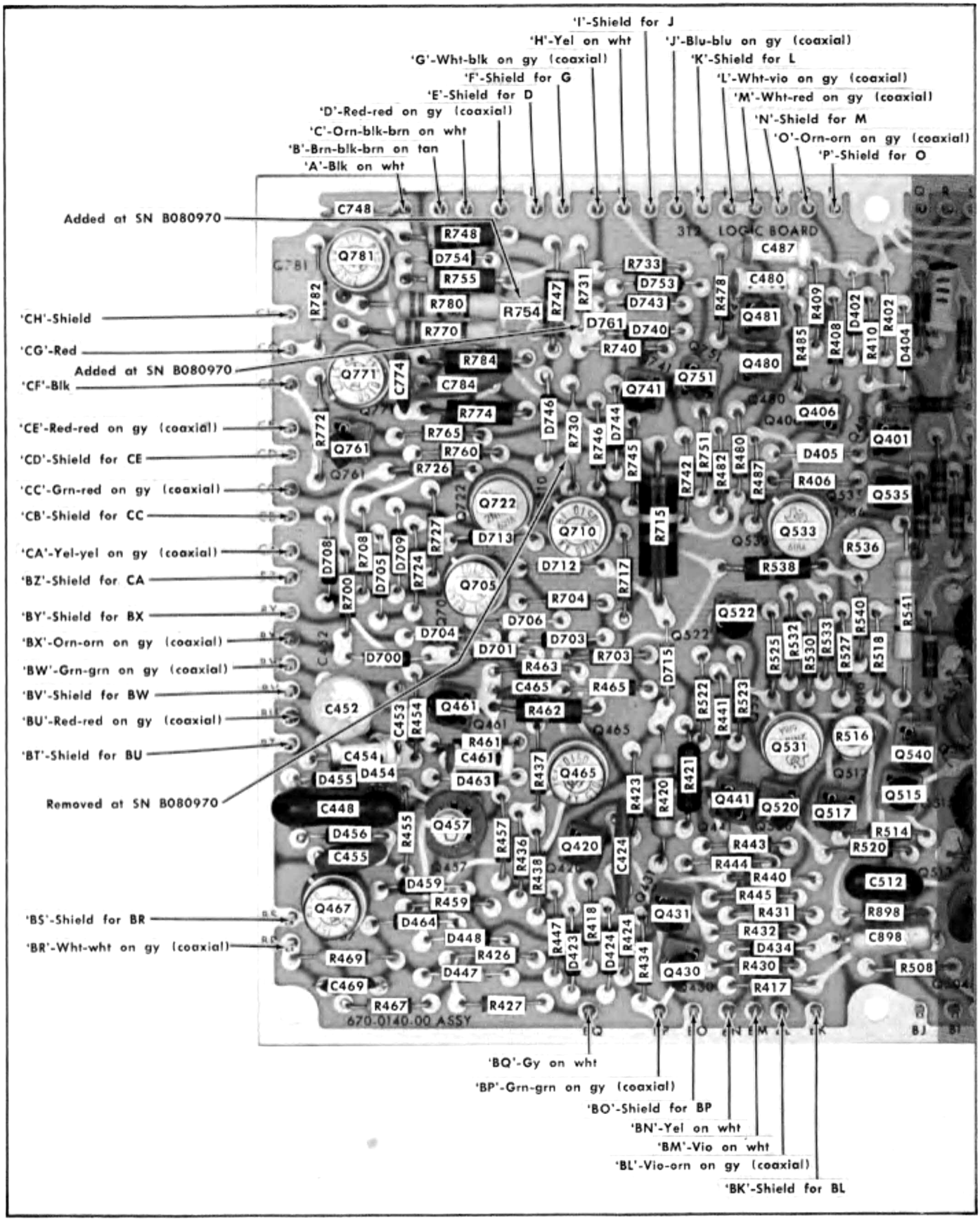


Fig. 5-8 A. Logic Board, Left.

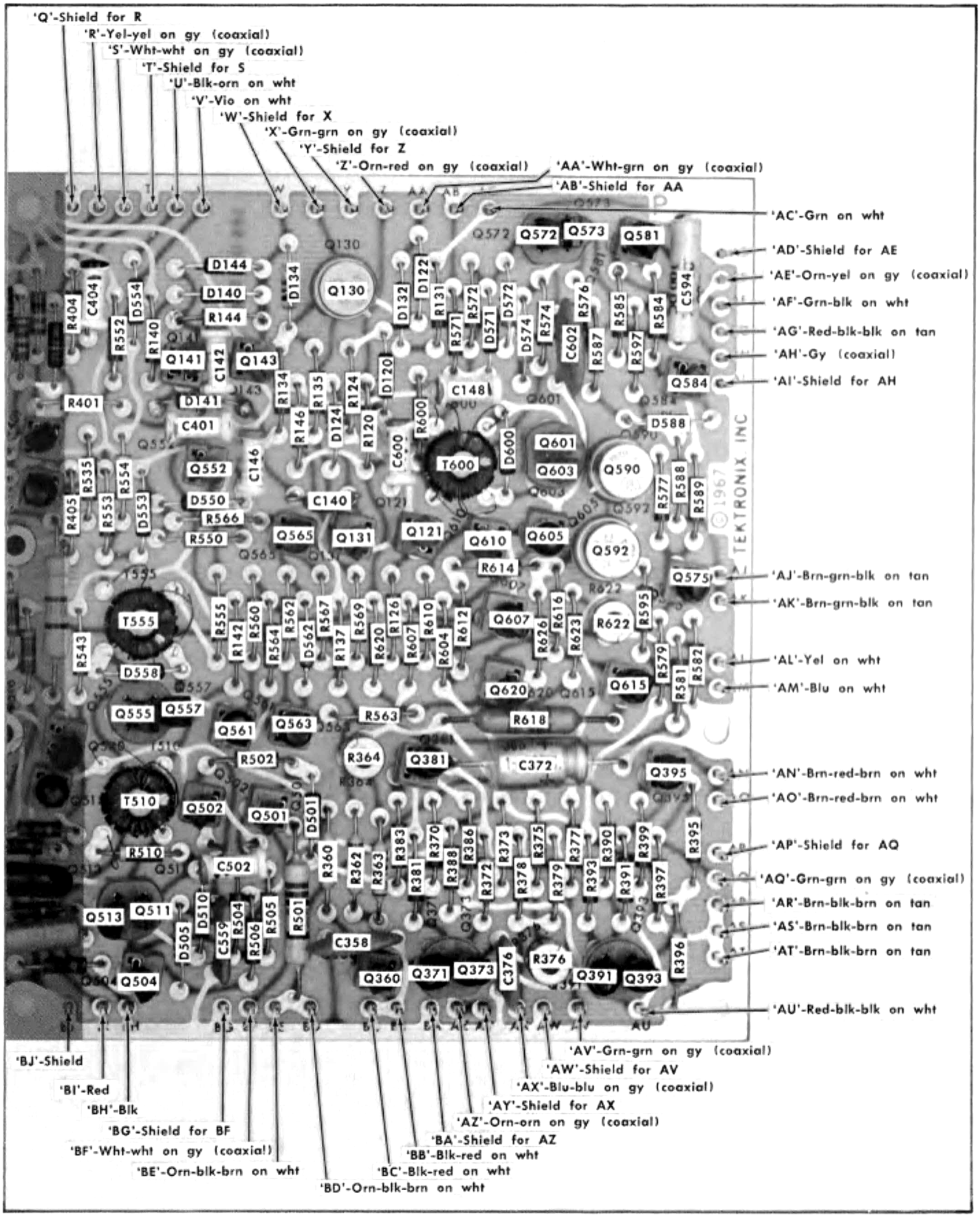


Fig. 5-8B. Logic Board, Right, SN B010100 through B060759.

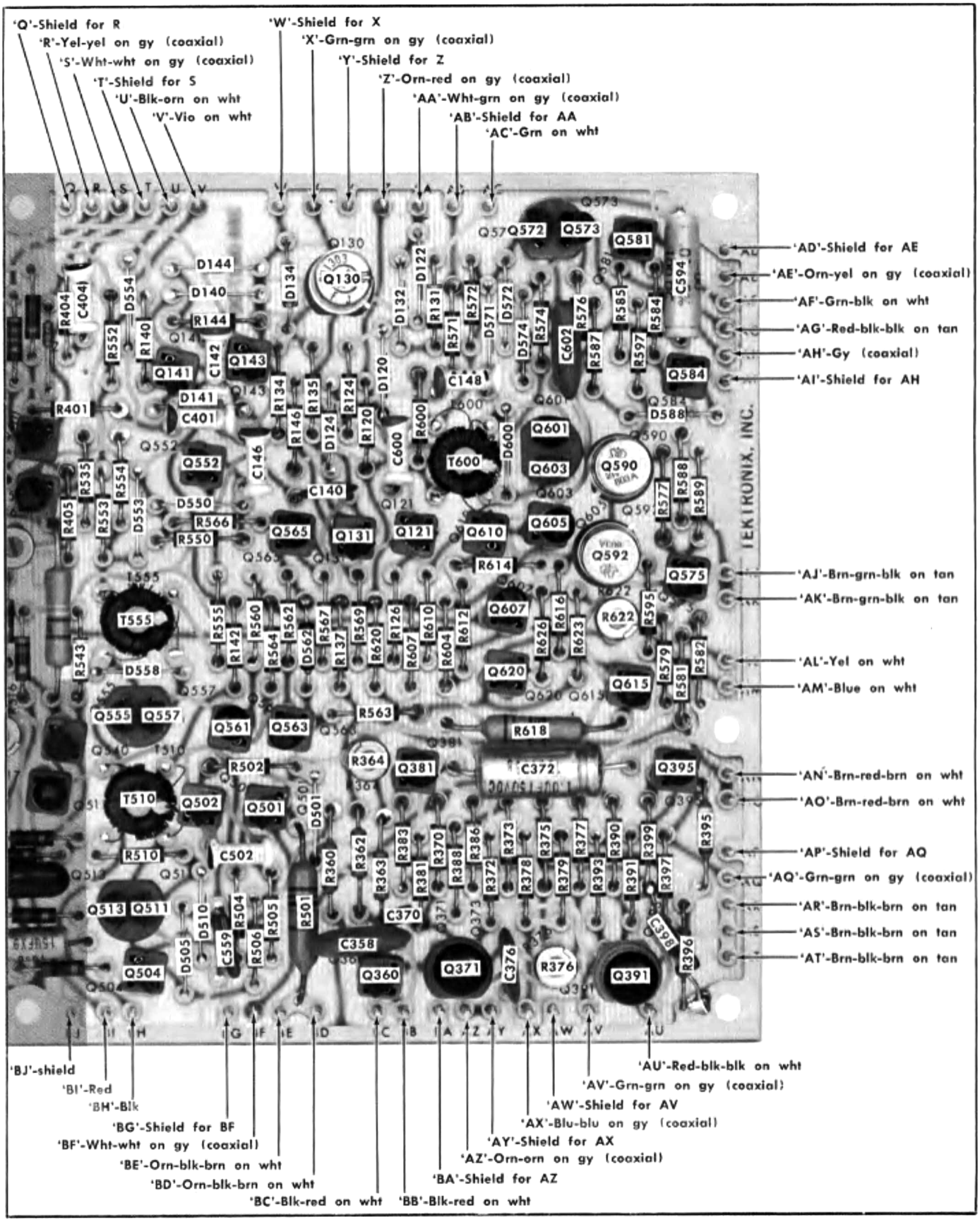


Fig. 5-8B. Logic Board, Right, SN B070760-up.

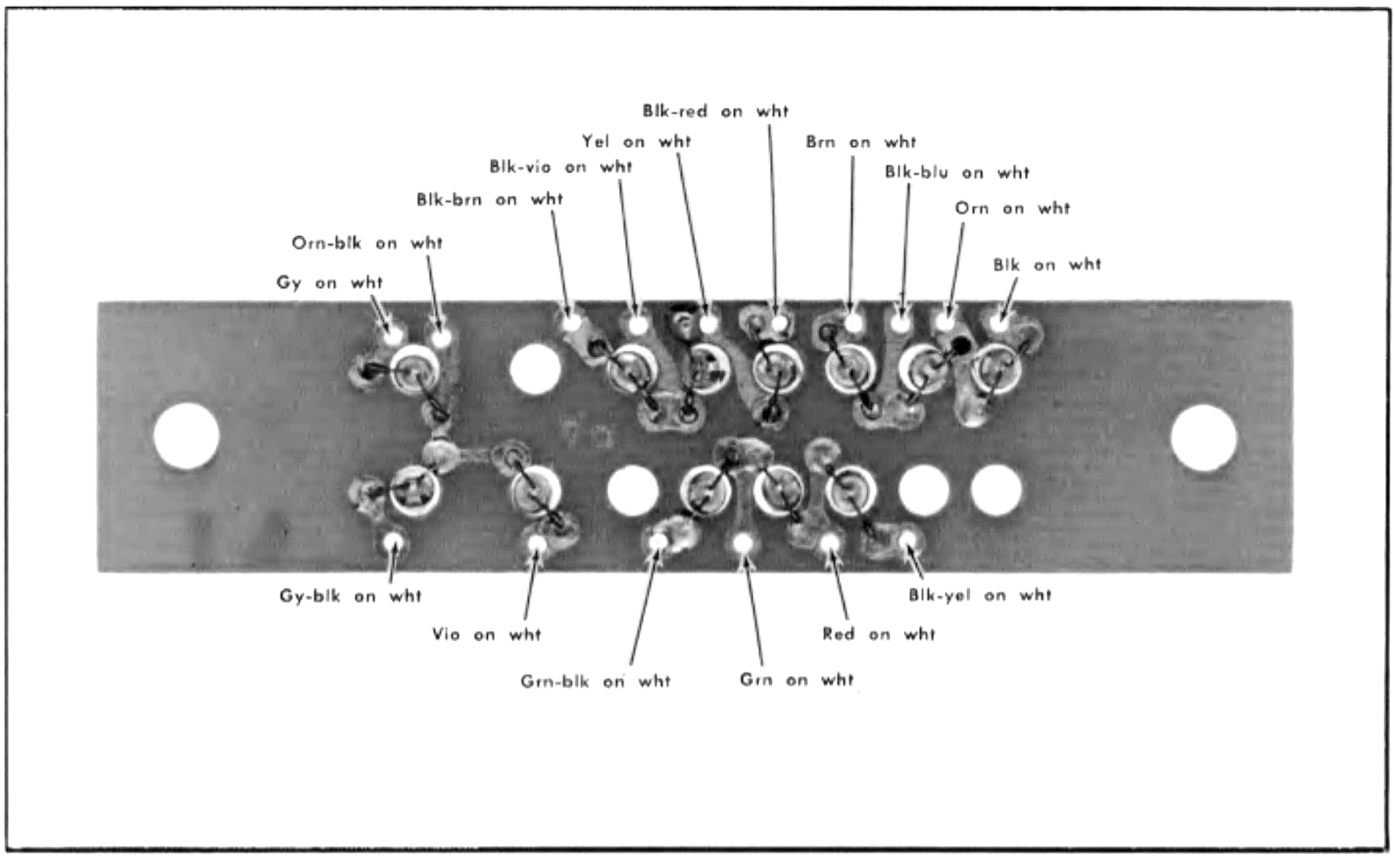


Fig. 5-9. Readout incandescent board assembly.

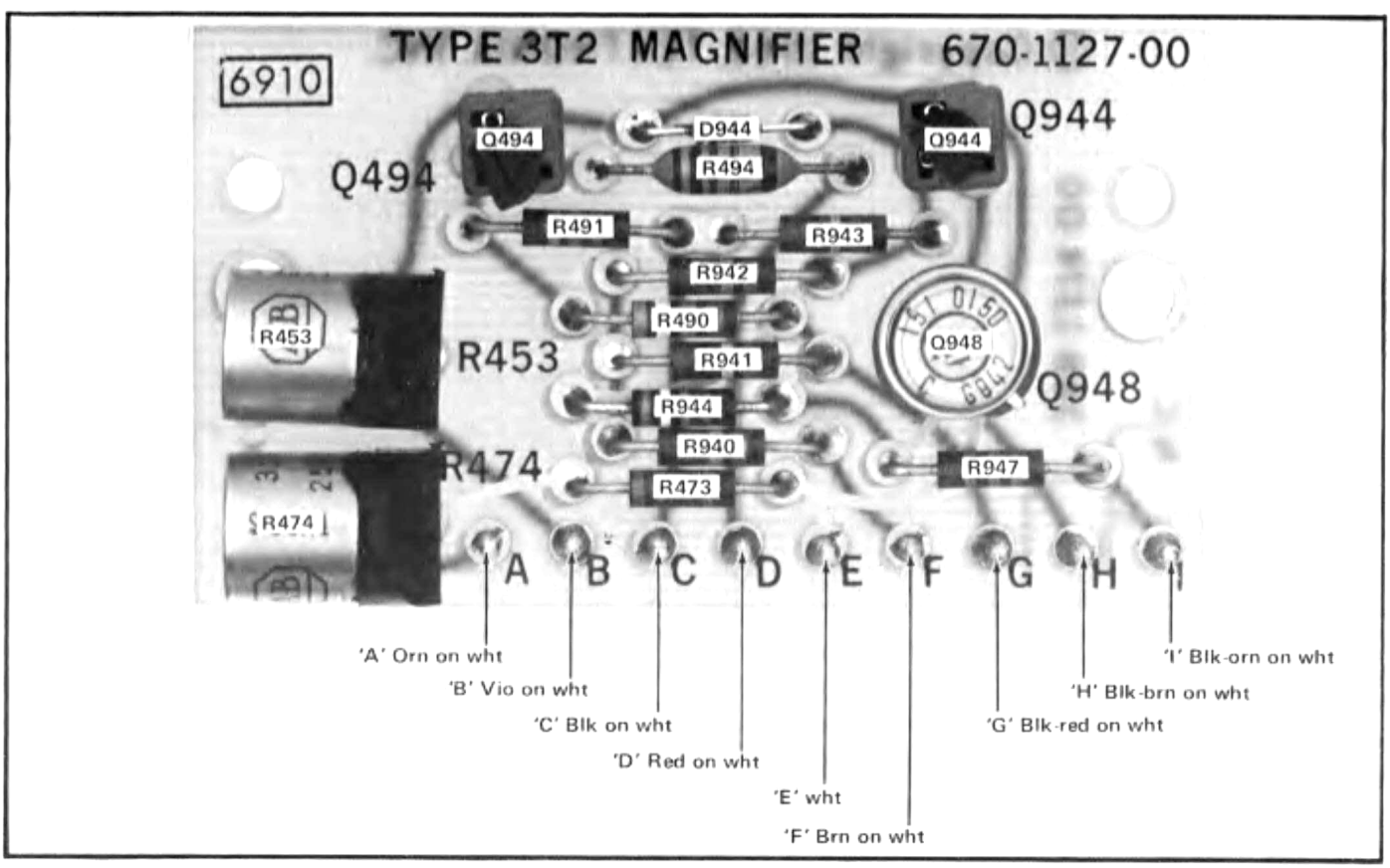
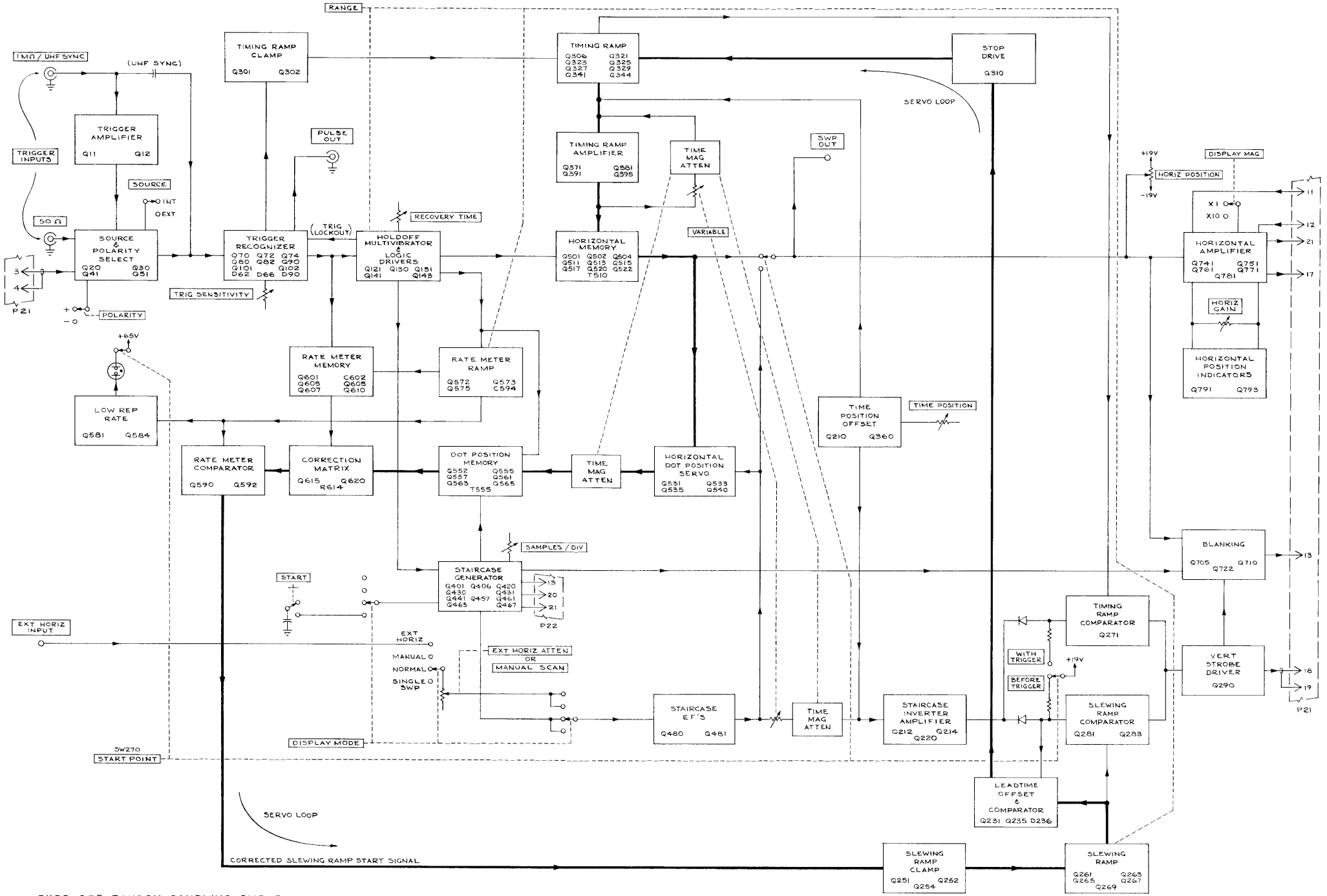
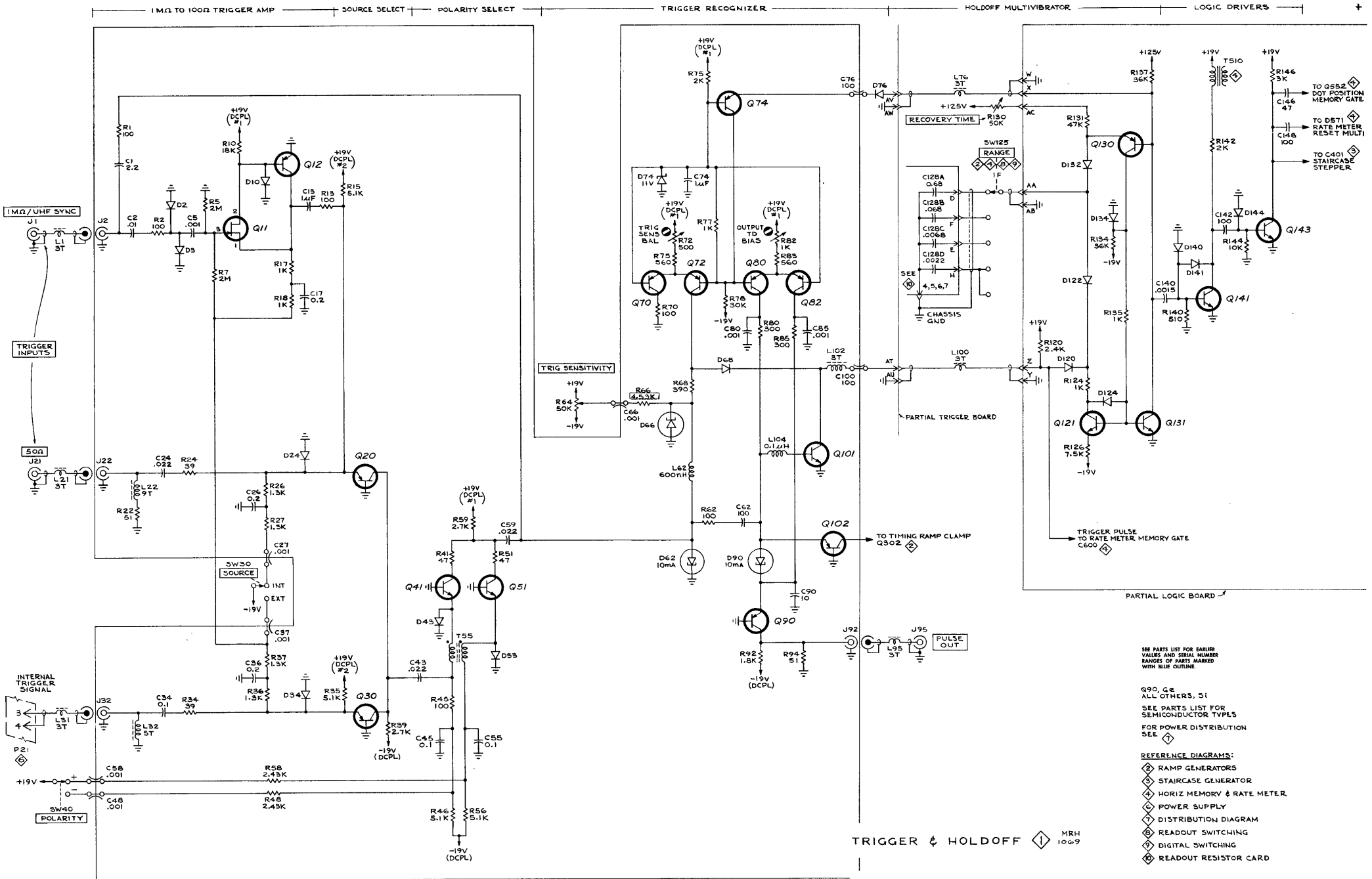


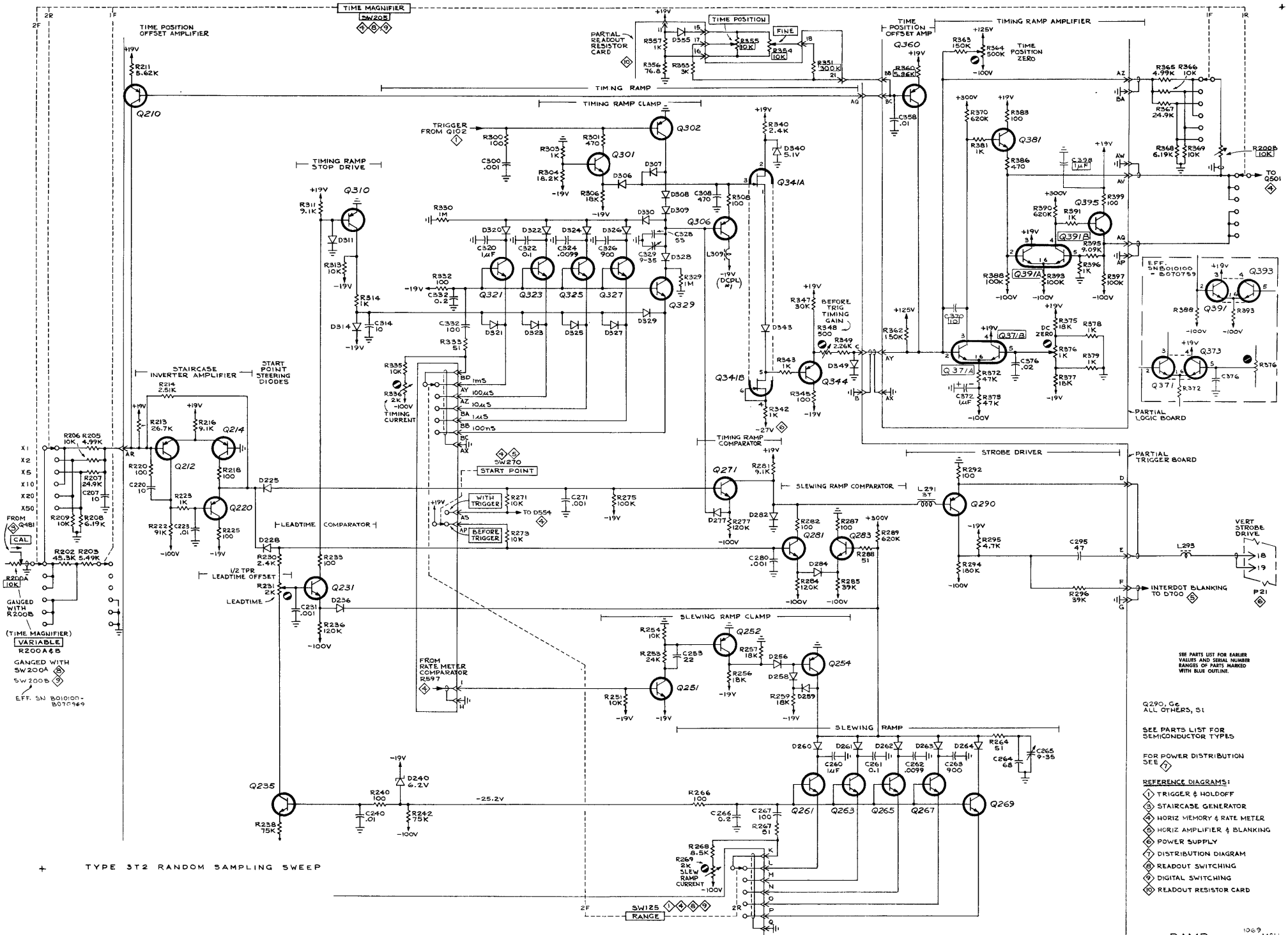
Fig. 5-10. ×10 Magnifier board.

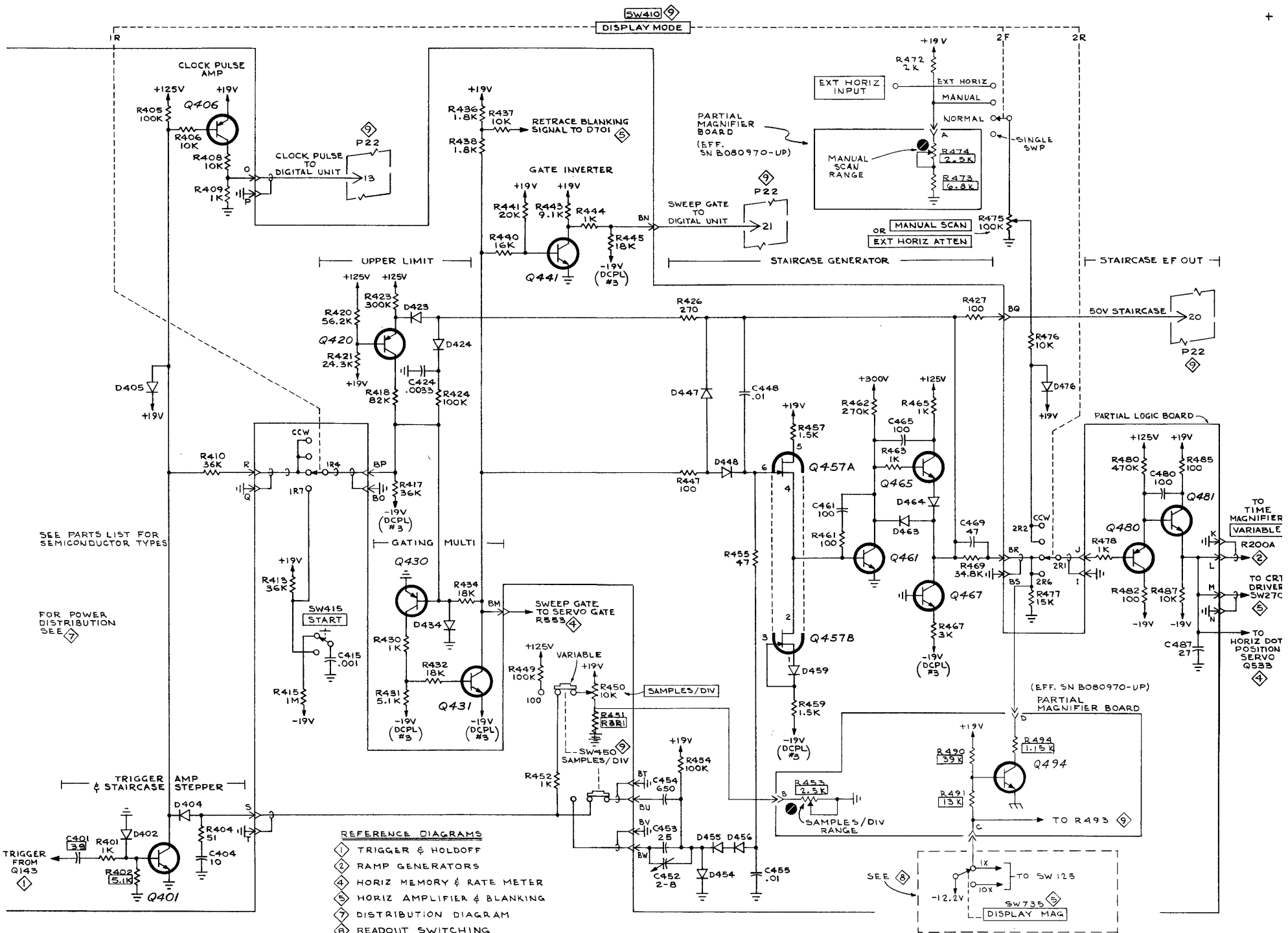


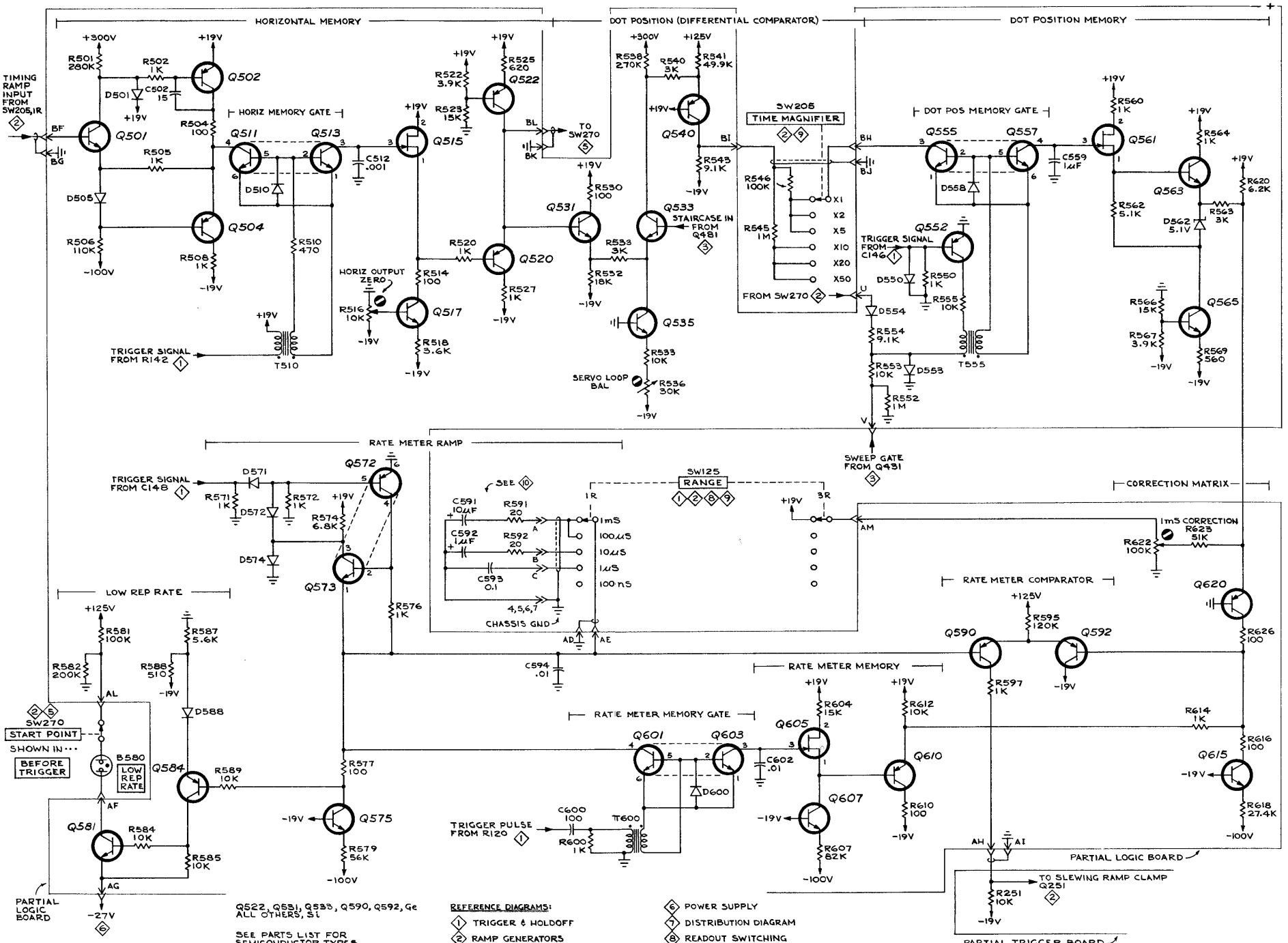
TYPE 3T2 RANDOM SAMPLING SWEEP

BLOCK DIAGRAM MRH 10-9


1MΩ TO 100Ω TRIGGER AMP
SOURCE SELECT
POLARITY SELECT
TRIGGER RECOGNIZER
HOLDOFF MULTIVIBRATOR
LOGIC DRIVERS
1MΩ/UHF SYNC
J1
TRIGGER INPUTS
50Ω
J21
INTERNAL TRIGGER SIGNAL
J32
P21
SW30 SOURCE
INT
EXT
SW40 POLARITY
TRIG SENSITIVITY
R64 50K
R66 4.53K
C66 .001
D66
TRIG SENS BAL R72 500
OUTPUT TD BIAS R82 1K
RECOVERY TIME R130 50K
SW125 RANGE
1F
CHASSIS GND
SEE 10
4,5,6,7
PARTIAL TRIGGER BOARD
PARTIAL LOGIC BOARD
TRIGGER CIRCUIT SHIELD
TRIGGER PULSE TO RATE METER MEMORY GATE C600 4
TO TIMING RAMP CLAMP Q302 2
TO Q552 4 DOT POSITION MEMORY GATE
TO D571 4 RATE METER RESET MULTI
TO C401 3 STAIRCASE STEPPER
J92
J95
PULSE OUT
L95 3T
T510
T55
Q10 Q11 Q12 Q20 Q30 Q41 Q51 Q70 Q72 Q74 Q80 Q82 Q90 Q101 Q102 Q121 Q130 Q131 Q140 Q141 Q143
D10 D24 D34 D43 D53 D62 D68 D90 D120 D122 D124 D132 D134 D140 D141 D144
+19V (DCPL) #1
+19V (DCPL) #2
-19V (DCPL)
+125V
-19V
+19V
TYPE 3T2 RANDOM SAMPLING SWEEP
TRIGGER & HOLDOFF 1 MRH 1069
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
Q90, Ge ALL OTHERS, Si
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
FOR POWER DISTRIBUTION SEE 7
REFERENCE DIAGRAMS:
2 RAMP GENERATORS
3 STAIRCASE GENERATOR
4 HORIZ MEMORY & RATE METER
6 POWER SUPPLY
7 DISTRIBUTION DIAGRAM
8 READOUT SWITCHING
9 DIGITAL SWITCHING
10 READOUT RESISTOR CARD


TIME MAGNIFIER
SW205
TIME POSITION OFFSET AMPLIFIER
TIMING RAMP AMPLIFIER
TIMING RAMP
TIMING RAMP CLAMP
TIMING RAMP STOP DRIVE
TRIGGER FROM Q102
STAIRCASE INVERTER AMPLIFIER
START POINT STEERING DIODES
LEADTIME COMPARATOR
TIMING RAMP COMPARATOR
SLEWING RAMP COMPARATOR
SLEWING RAMP CLAMP
SLEWING RAMP
STROBE DRIVER
PARTIAL TRIGGER BOARD
PARTIAL LOGIC BOARD
TIME POSITION
FINE
TIME POSITION ZERO
BEFORE TRIG TIMING GAIN
DC ZERO
1/2 TPR LEADTIME OFFSET
LEADTIME
START POINT
WITH TRIGGER
BEFORE TRIGGER
TIMING CURRENT
SLEW RAMP CURRENT
RANGE
CAL
VARIABLE
GANGED WITH R200B
GANGED WITH SW200A
SW200B
(TIME MAGNIFIER)
FROM Q481
FROM RATE METER COMPARATOR R597
TO Q501
TO D554
INTERDOT BLANKING TO DTOO
VERT STROBE DRIVE
P21
PARTIAL READOUT RESISTOR CARD
EFF. SN B010100 - B070759
EFF. SN B010100 - B070969
Q210
Q212
Q214
Q220
Q231
Q235
Q251
Q252
Q254
Q261
Q263
Q265
Q267
Q269
Q271
Q281
Q283
Q290
Q301
Q302
Q306
Q310
Q321
Q323
Q325
Q327
Q329
Q341A
Q341B
Q344
Q360
Q373
Q381
Q391
Q391A
Q391B
Q393
Q395
Q397
Q37/A
Q37/B
Q37/1
Q37/4
+19V
-19V
-100V
-25.2V
+125V
+300V
-27V
TYPE 3T2 RANDOM SAMPLING SWEEP
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
Q290, Ge ALL OTHERS, Si
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
FOR POWER DISTRIBUTION SEE 7
REFERENCE DIAGRAMS:
1 TRIGGER & HOLDOFF
3 STAIRCASE GENERATOR
4 HORIZ MEMORY & RATE METER
5 HORIZ AMPLIFIER & BLANKING
6 POWER SUPPLY
7 DISTRIBUTION DIAGRAM
8 READOUT SWITCHING
9 DIGITAL SWITCHING
10 READOUT RESISTOR CARD
RAMP GENERATORS 2
1069 M&H

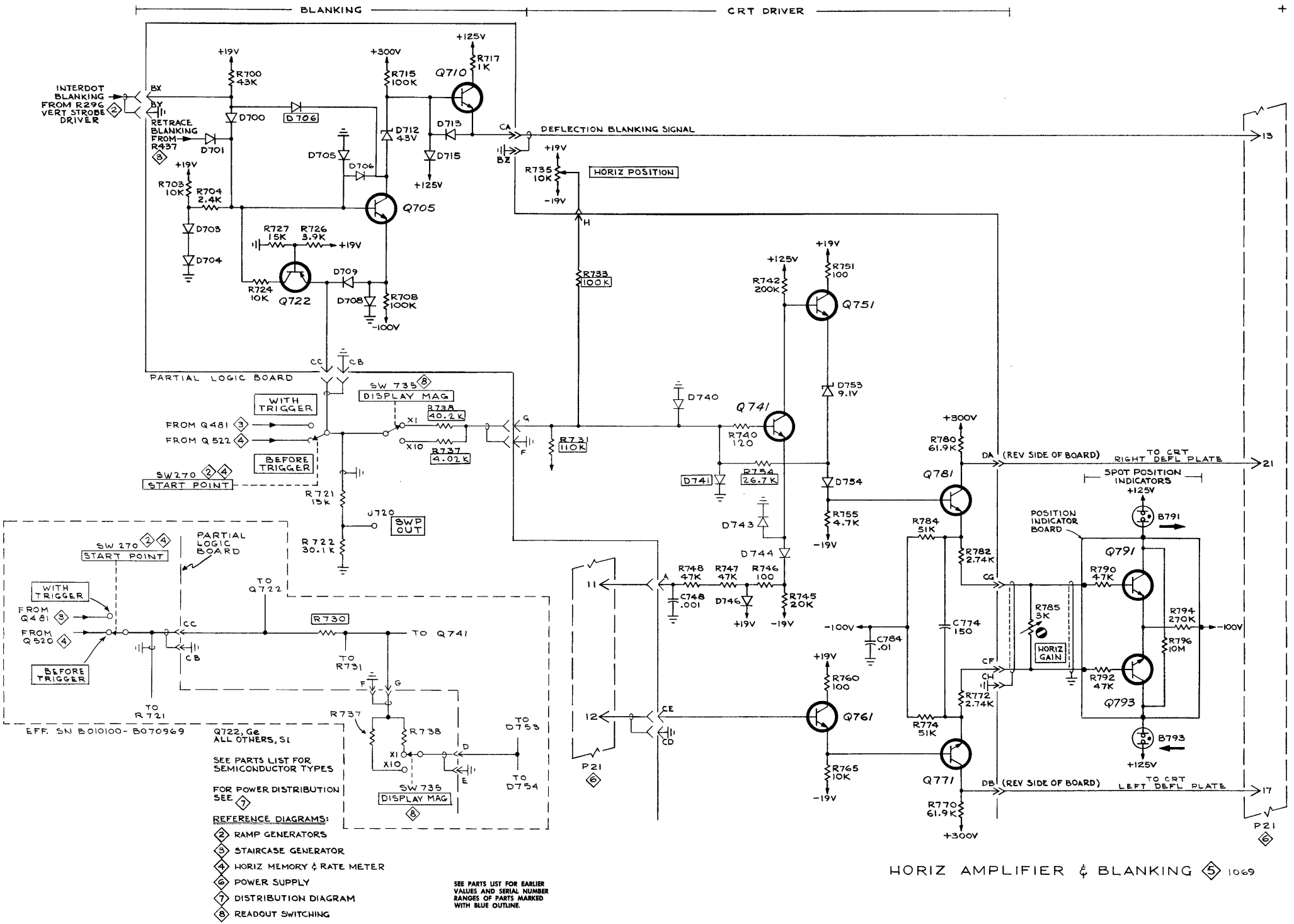

SW410 9
DISPLAY MODE
1R
2F
2R
CLOCK PULSE AMP
+125V
+19V
R405 100K
Q406
R406 10K
R408 10K
R409 1K
CLOCK PULSE TO DIGITAL UNIT
9 P22 13
R436 1.8K
R437 10K
RETRACE BLANKING SIGNAL TO D701 5
R438 1.8K
GATE INVERTER
R441 20K
R443 9.1K
R444 1K
R440 16K
Q441
R445 18K
-19V (DCPL) #3
SWEEP GATE TO DIGITAL UNIT
9 P22 21
BN
+19V
R472 2K
EXT HORIZ INPUT
EXT HORIZ
MANUAL
NORMAL
SINGLE SWP
PARTIAL MAGNIFIER BOARD (EFF. SN B080970-UP)
MANUAL SCAN RANGE
R474 2.5K
R473 6.8K
OR MANUAL SCAN EXT HORIZ ATTEN
R475 100K
UPPER LIMIT
STAIRCASE GENERATOR
STAIRCASE EF OUT
+125V
R423 300K
D423
R420 56.2K
Q420
D424
R421 24.3K
C424 .0033
R418 82K
R424 100K
R426 270
R427 100
BQ
50V STAIRCASE 20 P22 9
R476 10K
D476
D405
D447
C448 .01
D448
R447 100
R410 36K
CCW
R
IR4
IR7
BP
R417 36K
BO
-19V (DCPL) #3
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
GATING MULTI
Q430
R434 18K
D434
BM
SWEEP GATE TO SERVO GATE R553 4
R430 1K
R432 18K
R431 5.1K
Q431
R433 36K
SW415 START
C415 .001
R415 1M
FOR POWER DISTRIBUTION SEE 7
R457 1.5K
Q457A
Q457B
R462 270K
R465 1K
C465 100
R463 1K
Q465
D464
D463
C461 100
R461 100
Q461
R455 47
C469 47
R469 34.8K
Q467
R467 3K
R459 1.5K
D459
PARTIAL LOGIC BOARD
R480 470K
C480 100
R485 100
Q481
Q480
R478 1K
R482 100
R487 10K
C487 27
TO TIME MAGNIFIER VARIABLE R200A 2
TO CRT DRIVER SW270 5
TO HORIZ DOT POSITION SERVO Q533 4
(EFF. SN B080970-UP) PARTIAL MAGNIFIER BOARD
R494 1.15K
Q494
R490 39K
R491 13K
TO R493 9
R453 2.5K
SAMPLES/DIV RANGE
R449 100K
100
VARIABLE
R450 10K
SAMPLES/DIV
R451 R8R1
SW450 SAMPLES/DIV 9
R452 1K
R454 100K
C454 650
C453 25
C452 2-8
D455 D456
D454
C455 .01
TRIGGER & STAIRCASE AMP STEPPER
D404
D402
C401 39
R401 1K
R402 5.1K
Q401
R404 51
C404 10
TRIGGER FROM Q143 1
SEE 8
1X
10X
-12.2V
TO SW 125
SW735 5 DISPLAY MAG
REFERENCE DIAGRAMS
1 TRIGGER & HOLDOFF
2 RAMP GENERATORS
4 HORIZ MEMORY & RATE METER
5 HORIZ AMPLIFIER & BLANKING
7 DISTRIBUTION DIAGRAM
8 READOUT SWITCHING
9 DIGITAL SWITCHING
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
TYPE 3T2 RANDOM SAMPLING SWEEP
STAIRCASE GENERATOR 3 MRH 1069

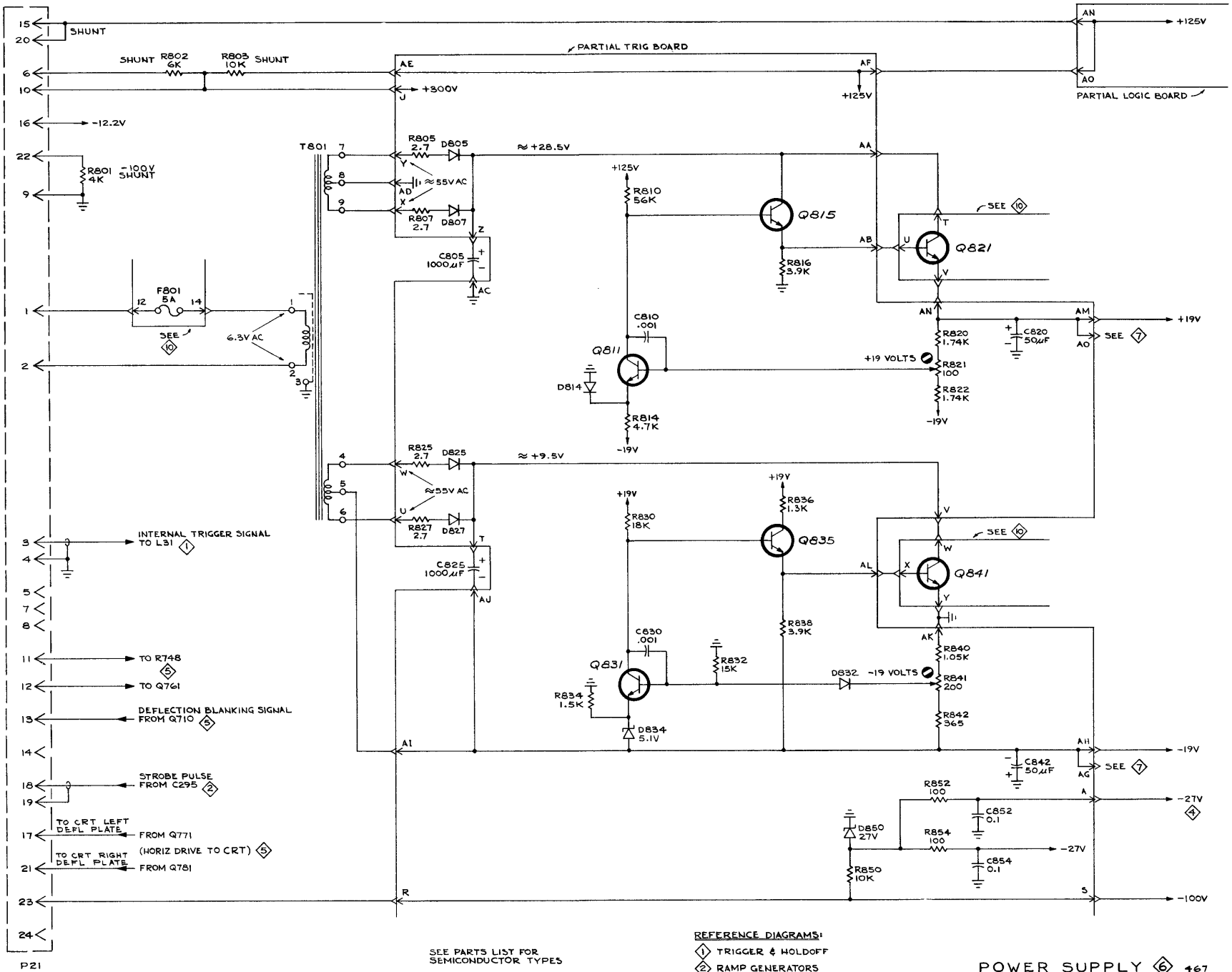


+ TYPE 3T2 RANDOM SAMPLING SWEEP

A1

HORIZ MEMORY & RATE METER 4 MRH 467


BLANKING
CRT DRIVER
INTERDOT BLANKING FROM R296 VERT STROBE DRIVER
RETRACE BLANKING FROM R437
DEFLECTION BLANKING SIGNAL
HORIZ POSITION
PARTIAL LOGIC BOARD
WITH TRIGGER
BEFORE TRIGGER
SW270 START POINT
SW 735 DISPLAY MAG
FROM Q481
FROM Q522
SWP OUT
TO Q722
TO Q741
TO R731
TO R721
TO D753
TO D754
R730
R733 100K
R731 110K
R721 15K
R722 30.1K
R738 40.2K
R737 4.02K
R754 26.7K
R740 120
R745 20K
R748 47K
R747 47K
R746 100
C748 .001
C784 .01
C774 150
R785 3K
HORIZ GAIN
R780 61.9K
R784 51K
R782 2.74K
R772 2.74K
R774 51K
R770 61.9K
R790 4.7K
R792 47K
R794 270K
R796 10M
R760 100
R765 10K
R755 4.7K
R751 100
R742 200K
R735 10K
R717 1K
R715 100K
R700 43K
R703 10K
R704 2.4K
R727 15K
R726 3.9K
R724 10K
R708 100K
Q710
Q705
Q722
Q741
Q751
Q761
Q771
Q781
Q791
Q793
D700
D701
D703
D704
D705
D706
D708
D709
D712 43V
D713
D715
D740
D741
D743
D744
D746
D753 9.1V
D754
B791
B793
POSITION INDICATOR BOARD
SPOT POSITION INDICATORS
DA (REV SIDE OF BOARD)
DB (REV SIDE OF BOARD)
TO CRT RIGHT DEFL PLATE
TO CRT LEFT DEFL PLATE
P21
+125V
+300V
+19V
-19V
-100V
Q722, Ge ALL OTHERS, Si
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
FOR POWER DISTRIBUTION SEE 7
REFERENCE DIAGRAMS:
2 RAMP GENERATORS
3 STAIRCASE GENERATOR
4 HORIZ MEMORY & RATE METER
6 POWER SUPPLY
7 DISTRIBUTION DIAGRAM
8 READOUT SWITCHING
EFF. SN B010100- B070969
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
HORIZ AMPLIFIER & BLANKING 5 1069
TYPE 3T2 RANDOM SAMPLING SWEEP



TYPE 3T2 RANDOM SAMPLING SWEEP

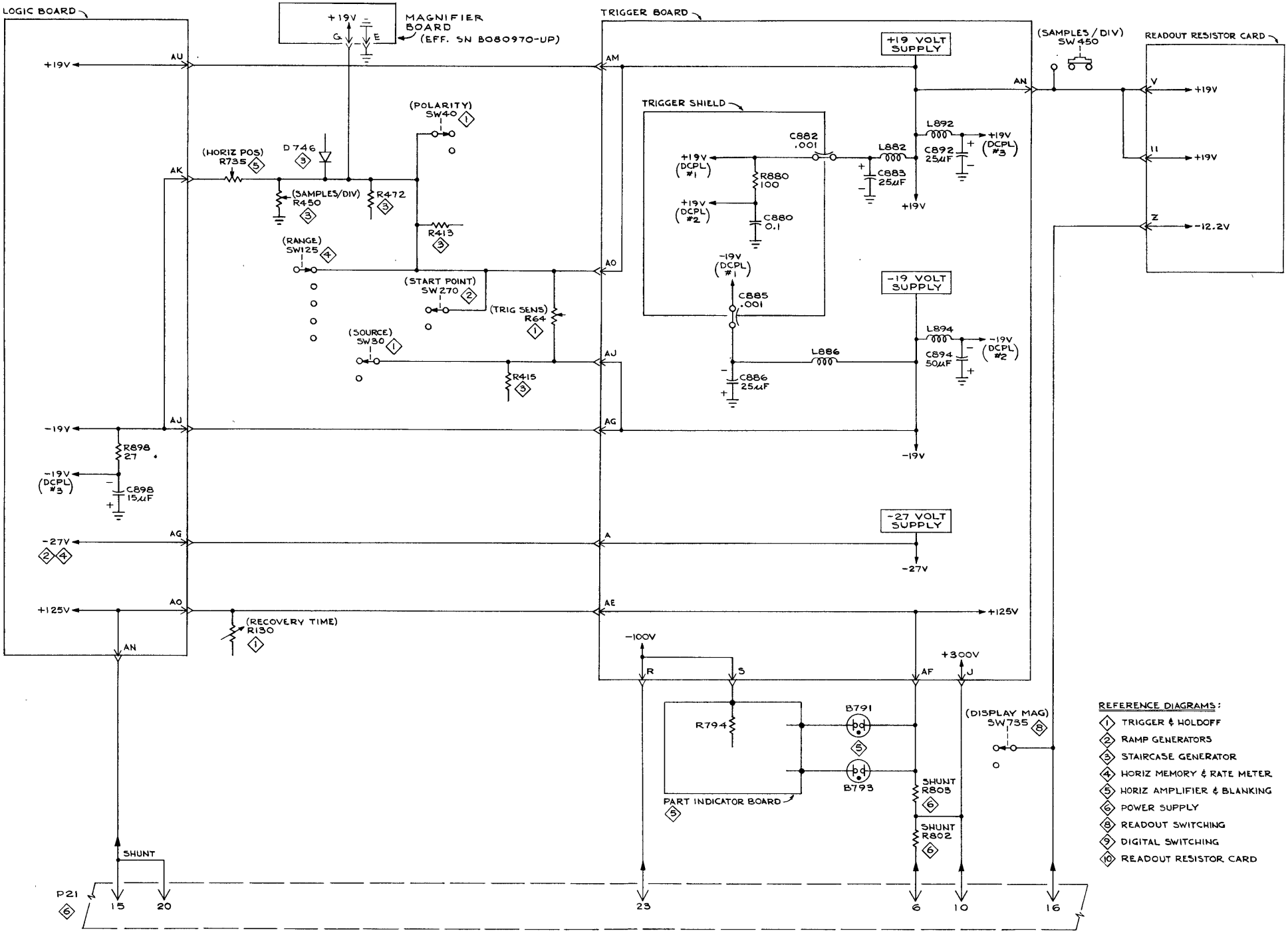
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

FOR POWER DISTRIBUTION SEE 7

REFERENCE DIAGRAMS:

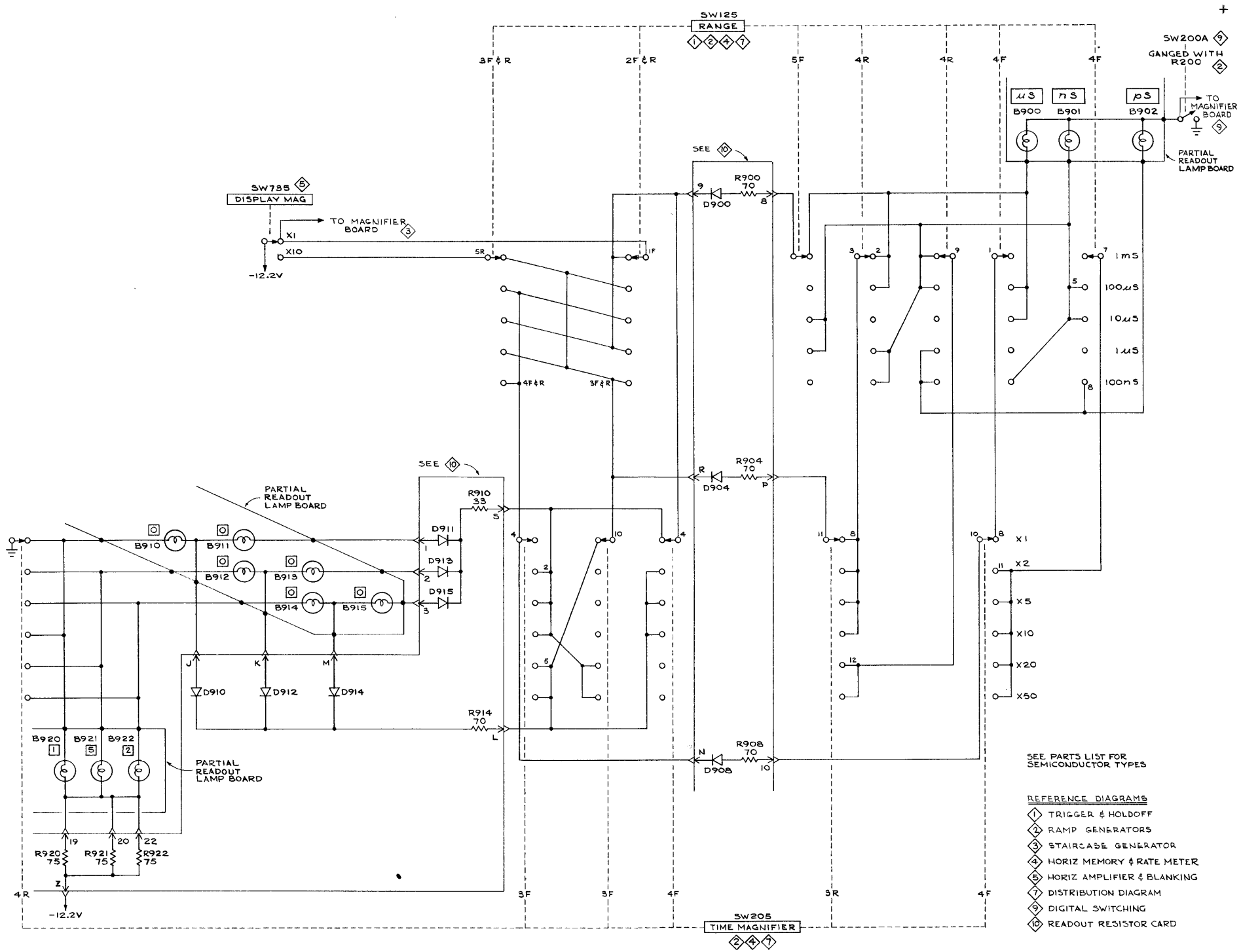
1. TRIGGER & HOLDOFF
2. RAMP GENERATORS
4. HORIZ MEMORY & RATE METER
5. HORIZ AMPLIFIER & BLANKING
7. DISTRIBUTION DIAGRAM
10. READOUT RESISTOR CARD

POWER SUPPLY 6 467

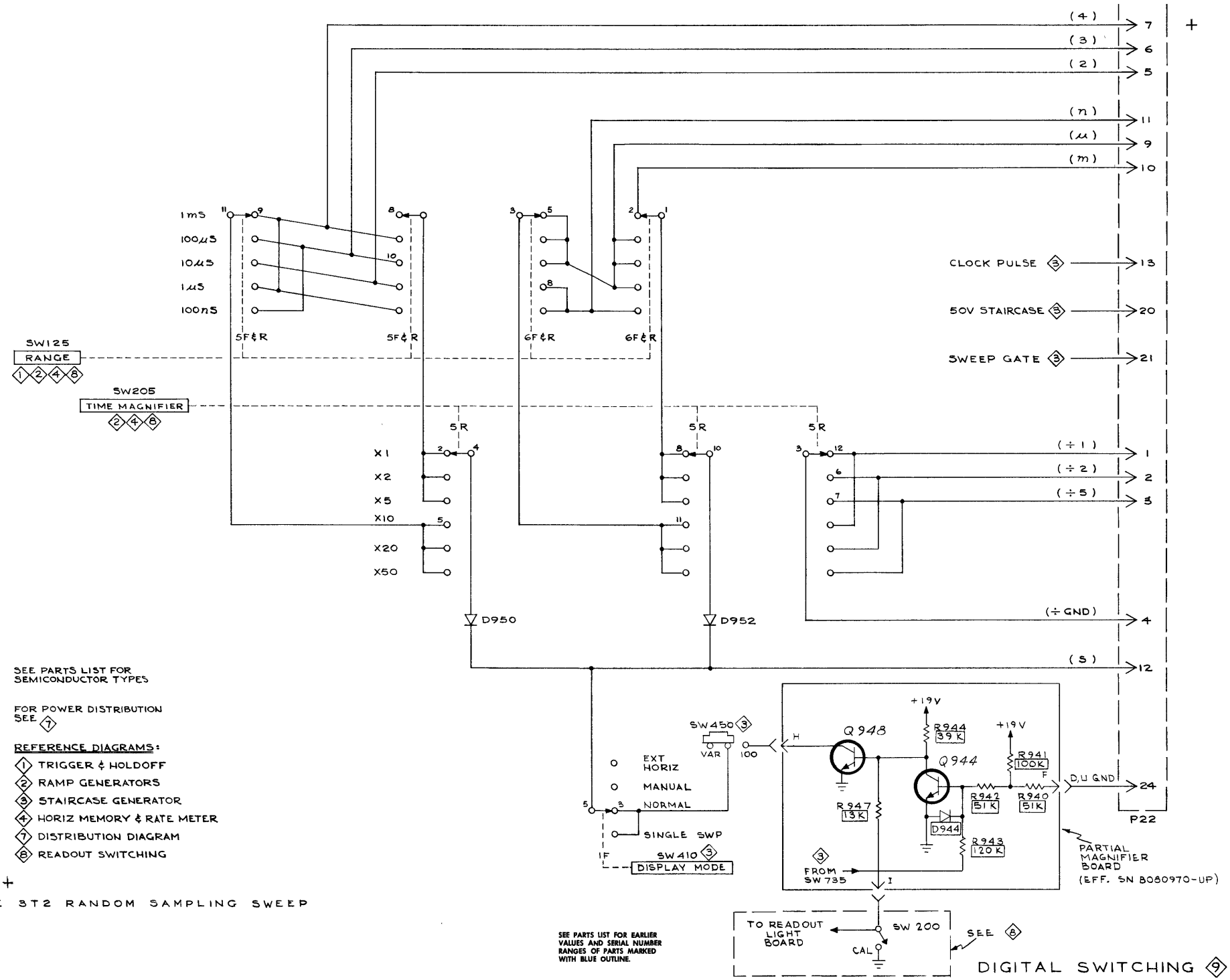


TYPE 3T2 RANDOM SAMPLING SWEEP

DISTRIBUTION DIAGRAM 7 MRH 1069



TYPE 3T2 RANDOM SAMPLING SWEEP



SEE PARTS LIST FOR SEMICONDUCTOR TYPES

FOR POWER DISTRIBUTION SEE 7

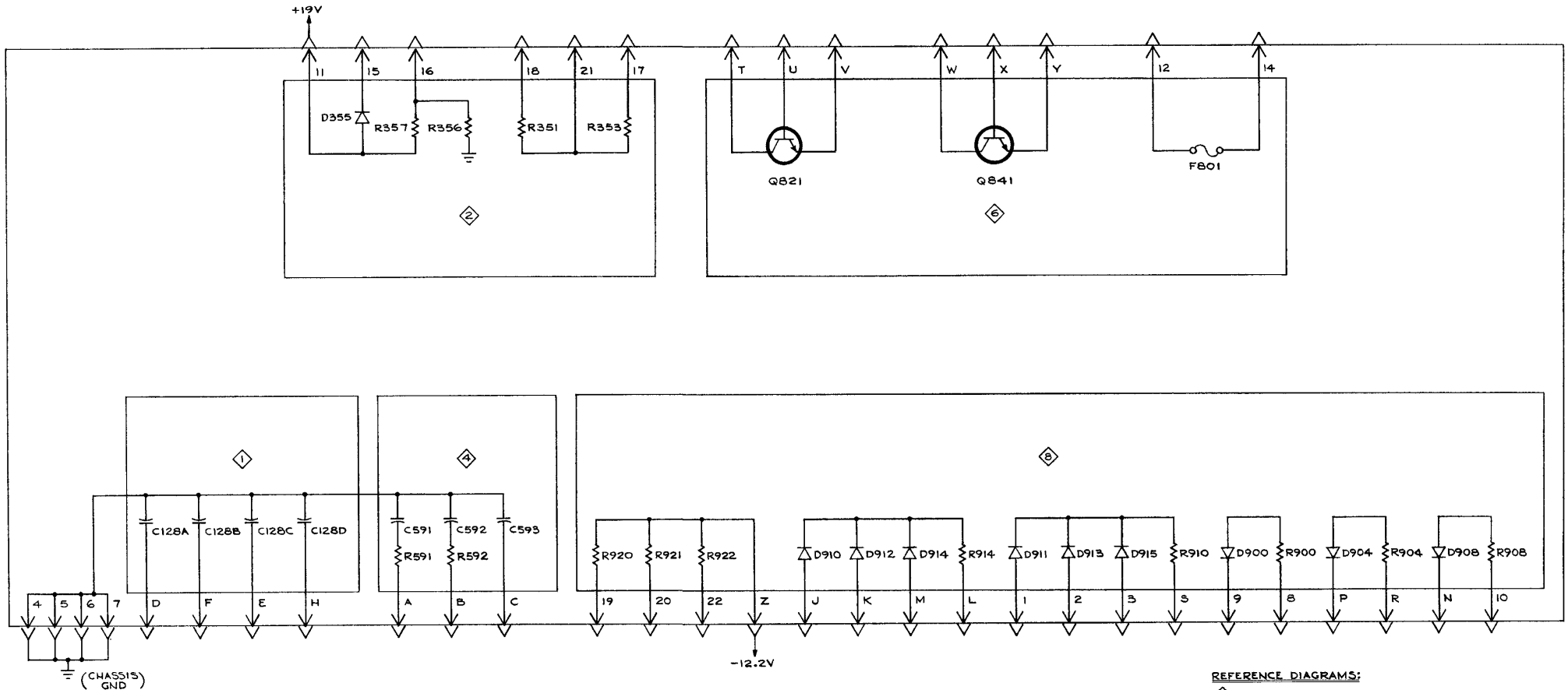
REFERENCE DIAGRAMS:

- 1 TRIGGER & HOLDOFF
- 2 RAMP GENERATORS
- 3 STAIRCASE GENERATOR
- 4 HORIZ MEMORY & RATE METER
- 7 DISTRIBUTION DIAGRAM
- 8 READOUT SWITCHING

+ TYPE 5T2 RANDOM SAMPLING SWEEP

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

DIGITAL SWITCHING 9 1069



REFERENCE DIAGRAMS:

- 1 TRIGGER & HOLDOFF
- 2 RAMP GENERATORS
- 4 HORIZ MEMORY & RATE METER
- 6 POWER SUPPLY
- 8 READOUT SWITCHING

TYPE 3T2 RANDOM SAMPLING SWEEP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z

J24

READOUT RESISTOR CARD 10 MRH 567

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

TYPE 3T2

TEXT CORRECTION

Section 1 Characteristics

Page 1-3 Horizontal Deflection System

CHANGE: SWP OUT connector signal to read:

SWP OUT Connector signal (SN B080970-up)	1 V/Div, ±5% (through 10 kΩ) 1X MAG 0.1 V/Div, ±5% (through 10 kΩ) 10X MAG	
SWP OUT Connector signal (SN B010100-B070969)	1 V/Div, ±5%	Through 10 kΩ

Page 1-3 Electrical Characteristics

CHANGE: first Performance Requirement line under "Pulse, External (50 Ω Input)" to:

External (50 Ω Input)	
With Trigger	30 ps or less trigger jitter with 50 mV, 2 ns duration pulse. 20 ps or less trigger jitter with 150 mV, 2 ns duration pulse.
Before Trigger	50 ps or less trigger jitter with 50 mV, 2 ns duration pulse.

Diagrams Block Diagram

DELETE: Q373 and Q393 from the Timing Ramp Amplifier block.

C6/1169

TEXT CORRECTIONS

Section 3 Operating Instructions

Page 3-5 DISPLAY MAG Switch

DELETE: the last sentence.

Page 3-8 2nd column, 9th line from the bottom

ADD: a period after the word waveform, and DELETE: the remainder of the sentence.

Section 5 Maintenance

Page 5-12 Fig. 5-8A

REPLACE: the existing Figure with the one included in this insert.

ADD: a Figure 5-10 included in this insert.

Section 7 Calibration

ADD: the following between the present Step 25 and Step 26.

25. Check Variable Samples/Div (SN B080970 and up)

a. Set the DISPLAY MODE switch to NORMAL, the START POINT switch to WITH TRIGGER, the RANGE switch to 10 µs and the SAMPLES/DIV control fully clockwise.

b. Check that the trace consists of 12 dots/div or less. See Fig. 7-30.

c. Set the SAMPLES/DIV control counterclockwise and adjust R453, located on X10 Magnifier board, so the spot requires one second to cross the graticule. This adjustment is on the X10 Magnifier board, which is mounted just behind the bottom portion of the 3T2 front panel.

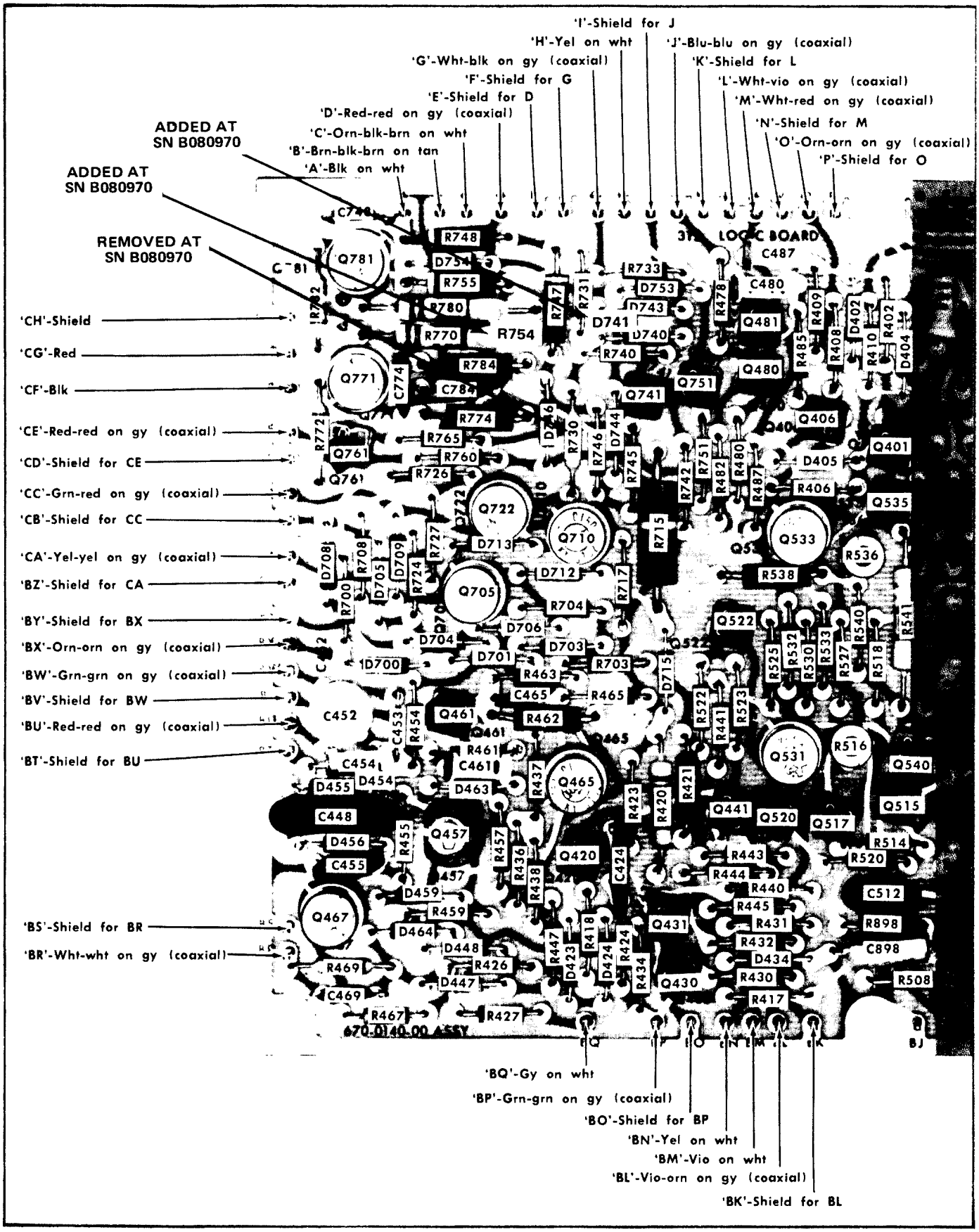


Fig. 5-8A. Logic Board, Left.

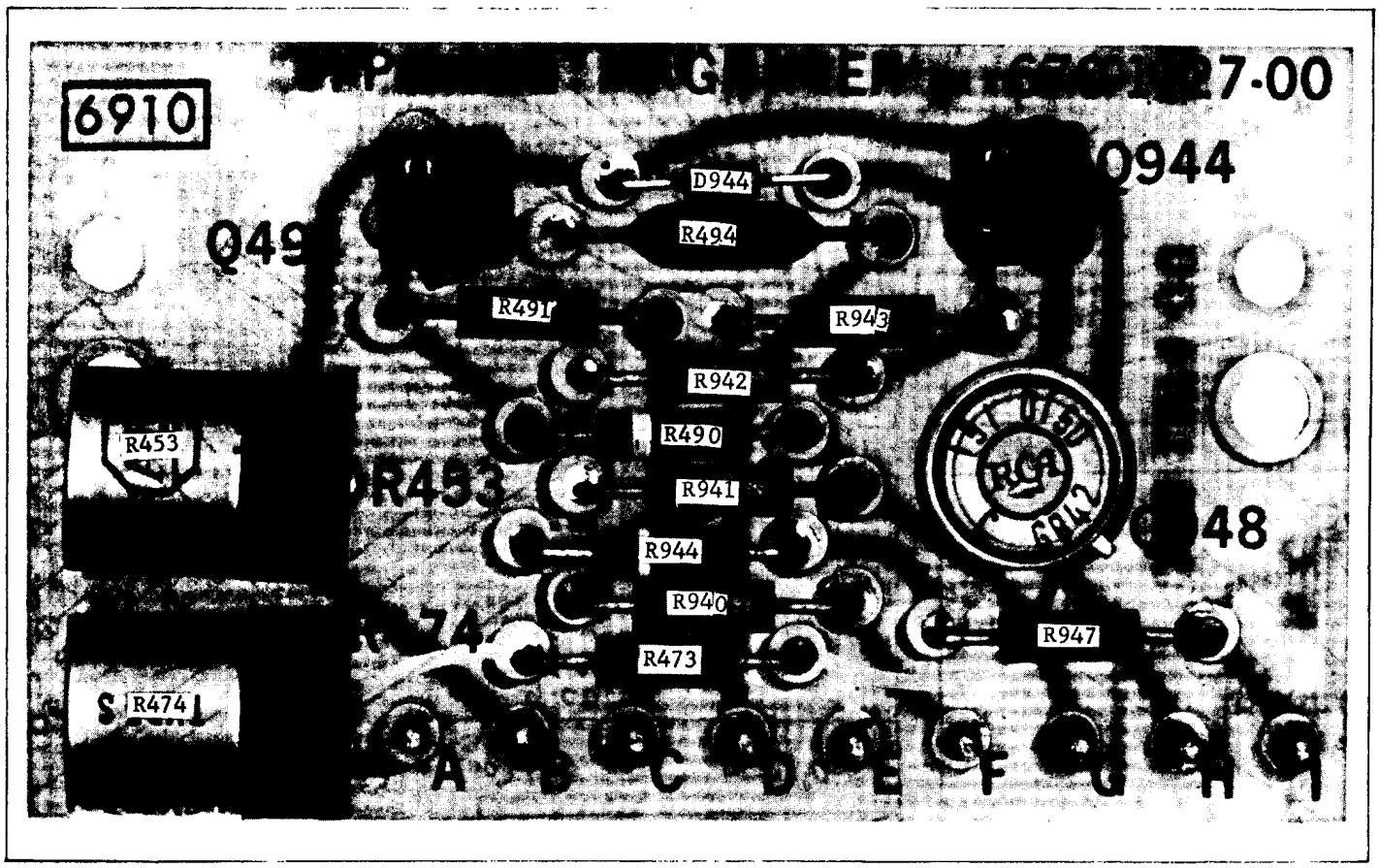


FIG. 5-10. X10 Magnifier Board.

The following are the connections for the Magnifier Board.

'A'- Orn on wht
'B'- Vio on wht
'C'- Blk on wht
'D'- Red on wht
'E'- Wht
'F'- Brn on wht
'G'- Blk-red on wht
'H'- Blk-brn on wht
'I'- Blk-orn on wht

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

REMOVE:

R451	315-0132-00	1.3 kΩ	1/4 W	5%
R730	321-0268-00	6.04 kΩ	1/8 W	1%

CHANGE TO:

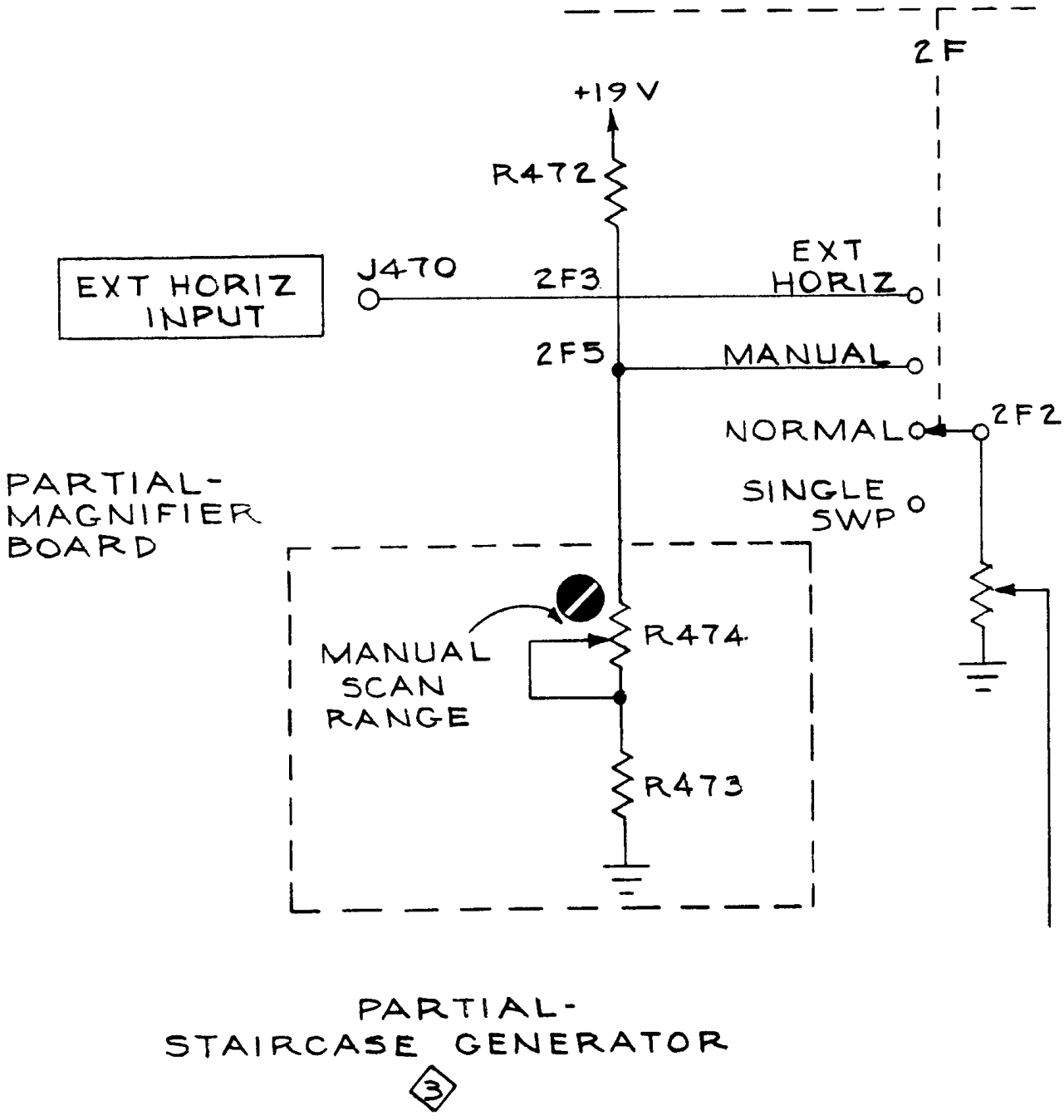
Q12	151-0221-00	Silicon	2N4258	
Q20	151-0271-00	Silicon	Tek Spec	
Q30	151-0271-00	Silicon	Tek Spec	
Q41	151-0269-00	Silicon	Hi-Frequency	
Q51	151-0269-00	Silicon	Hi-Frequency	
Q74	151-0220-00	Silicon	2N4122	
Q102	151-0271-00	Silicon	Tek Spec	
R66	321-0256-00	4.53 kΩ	1/4 W	5%
R200A, R200B (5)	311-0962-00	2x10 kΩ, Var		
R351	315-0304-00	300 kΩ	1/4 W	5%
R354, R355	311-0965-00	2x10 kΩ, Var		
R474	311-0940-00	2.5 kΩ, Var		
R731	315-0114-00	110 kΩ	1/4 W	5%
R733	315-0104-00	100 kΩ	1/4 W	5%
R737	321-0251-00	4.02 kΩ	1/8 W	1%
R738	321-0347-00	40.2 kΩ	1/8 W	1%
SW200A, SW200B (9)	311-0962-00			
SW205	262-0803-01	Rotary	TIME MAGNIFIER	

ADD:

D741	152-0185-00	Silicon	Replaceable by 1N4152
D944	152-0185-00	Silicon	Replaceable by 1N4152

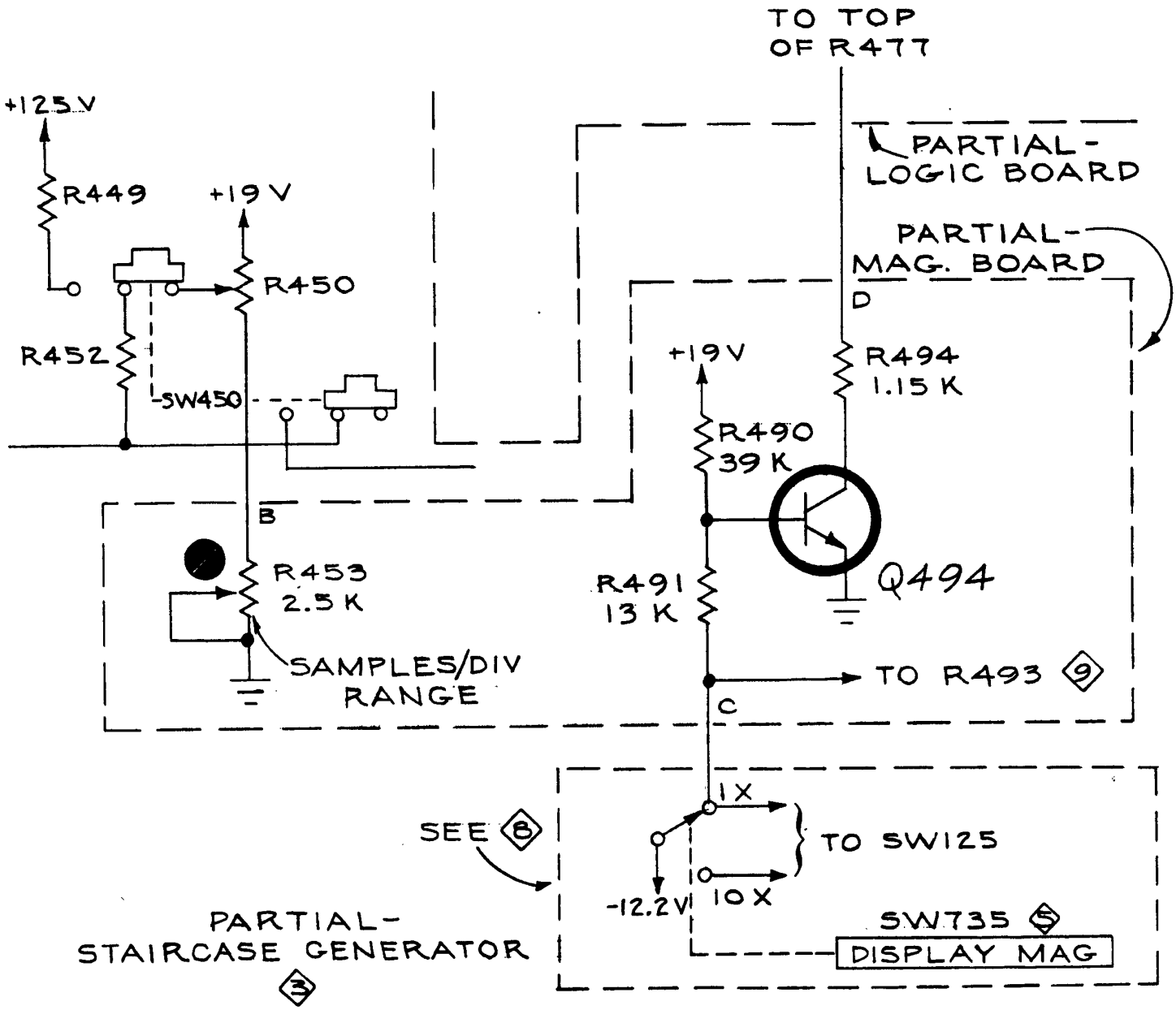
ADD (cont'd):

Q494	151-0190-01	Silicon	Tek Spec	
Q944	151-0190-01	Silicon	Tek Spec	
Q948	151-0150-00	Silicon	2N3440	
R453	311-0940-00	2.5 kΩ, Var		
R490	315-0393-00	39 kΩ	1/4 W	5%
R491	315-0133-00	13 kΩ	1/4 W	5%
R494	321-0199-00	1.15 kΩ	1/8 W	1%
R754	321-0330-00	26.7 kΩ	1/8 W	1%
R940	315-0513-00	51 kΩ	1/4 W	5%
R941	315-0104-00	100 kΩ	1/4 W	5%
R942	315-0513-00	51 kΩ	1/4 W	5%
R943	315-0124-00	120 kΩ	1/4 W	5%
R944	315-0393-00	39 kΩ	1/4 W	5%
R947	315-0133-00	13 kΩ	1/4 W	5%

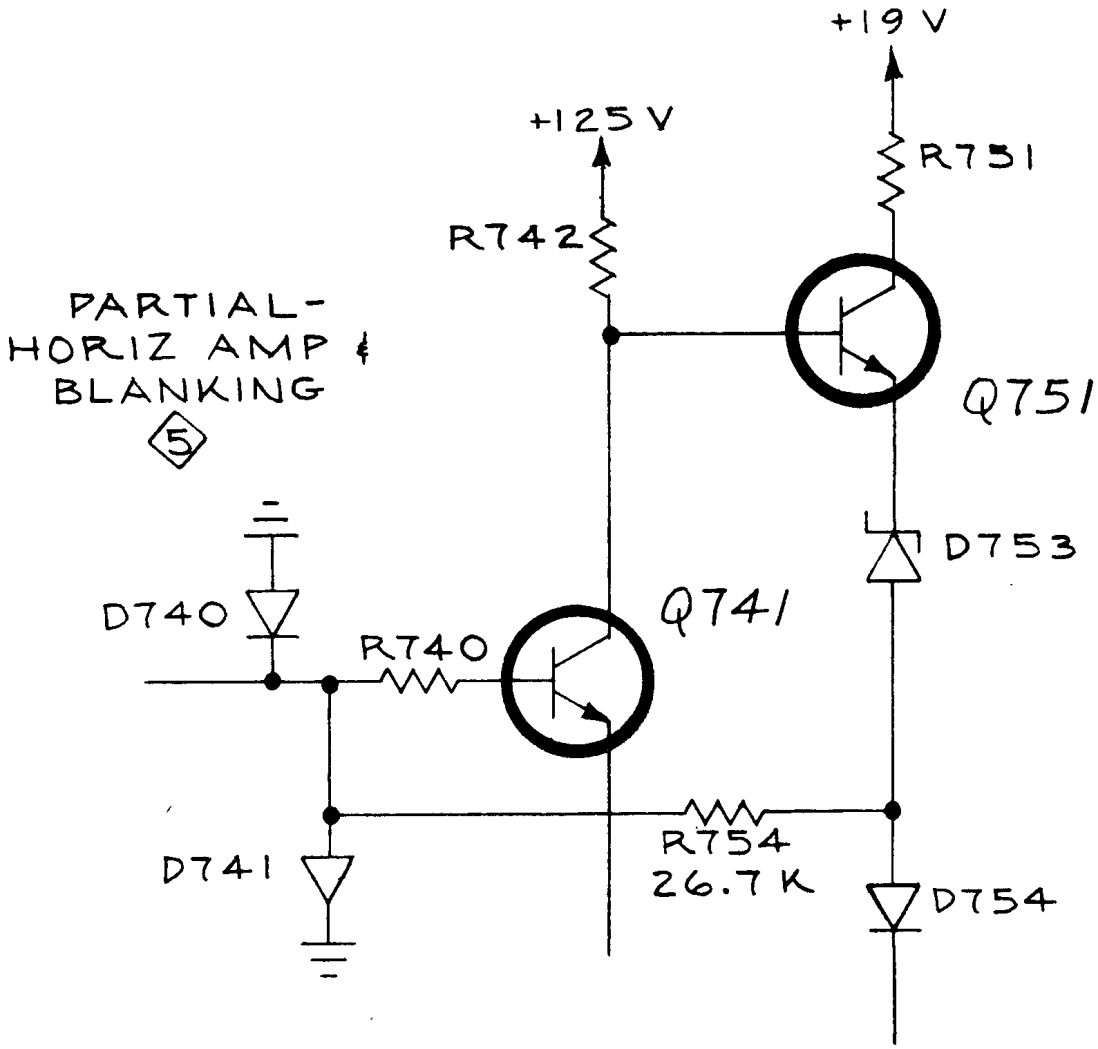


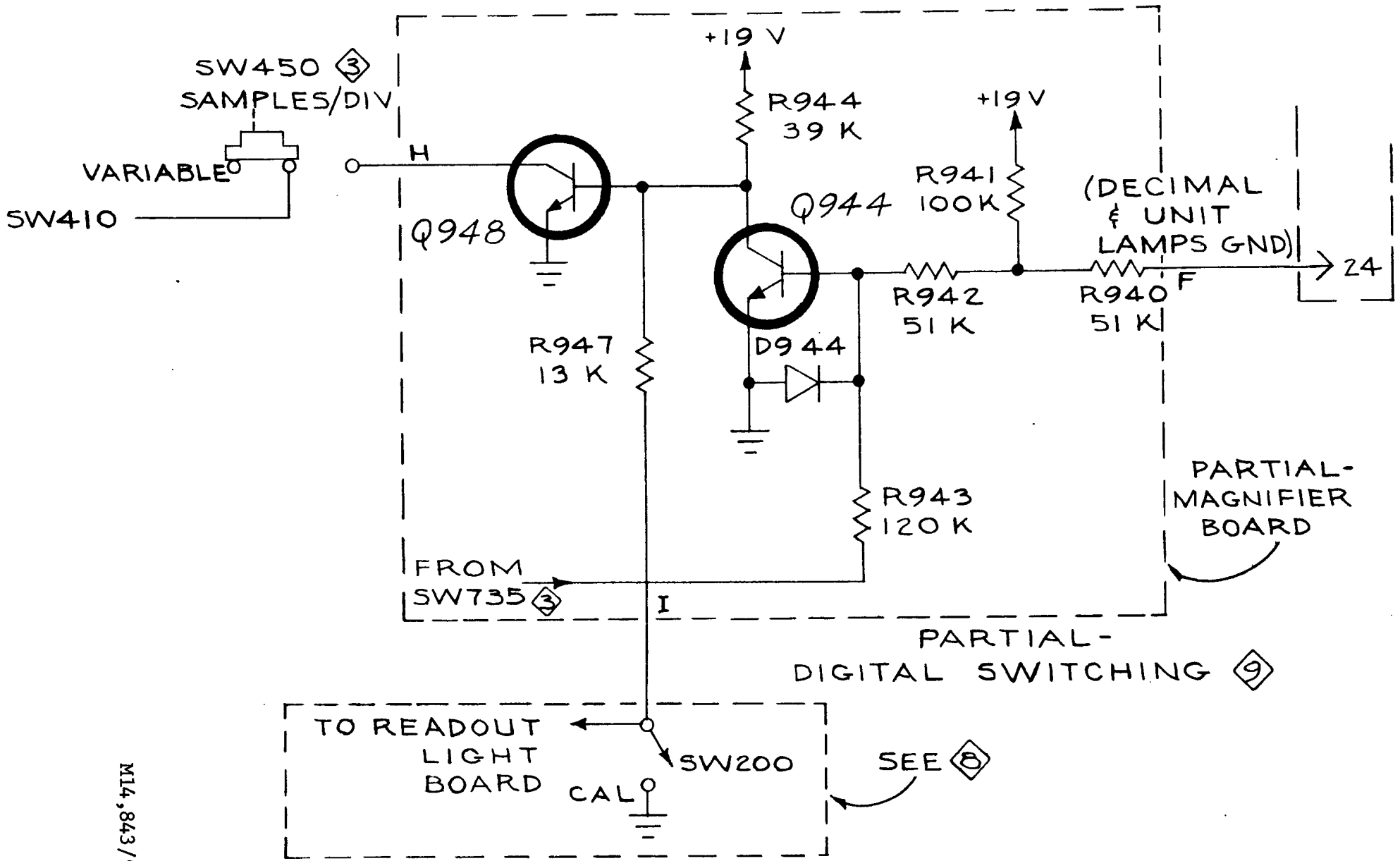
PARTIAL-STAIRCASE GENERATOR

③


TO TOP
OF R477
+125 V
R449
+19 V
R450
R452
SW450
PARTIAL-
LOGIC BOARD
PARTIAL-
MAG. BOARD
D
+19 V
R494
1.15 K
R490
39 K
B
R453
2.5 K
SAMPLES/DIV
RANGE
R491
13 K
Q494
TO R493 9
C
1 X
SEE 8
TO SW125
-12.2 V
10 X
SW735 5
DISPLAY MAG
PARTIAL-
STAIRCASE GENERATOR
3

M14,843/969


+19 V
+125 V
R751
R742
PARTIAL-
HORIZ AMP &
BLANKING
5
Q751
D753
D740
Q741
R740
D741
R754
26.7 K
D754


SW450 ③
SAMPLES/DIV
VARIABLE
SW410
H
+19 V
R944
39 K
+19 V
R941
100K
(DECIMAL & UNIT LAMPS GND)
24
F
Q948
Q944
R942
51 K
R940
51 K
R947
13 K
D944
R943
120 K
PARTIAL-MAGNIFIER BOARD
FROM SW735 ③
I
PARTIAL-DIGITAL SWITCHING ⑨
TO READOUT LIGHT BOARD
SW200
CAL
SEE ⑧

TYPE 3T2 TENT SN B060890

STANDARD ACCESSORIES CORRECTION

FIG. 3 ACCESSORIES

CHANGE and ADD to Fig. & Index No. 3-1:

3-1	011-0059-00	B010100	B059999	1 50 Ω 10X attenuator BNC
	011-0059-01	B060000		1 50 Ω 10X attenuator BNC

TYPE 3T2 TENT SN B091060

ELECTRICAL PARTS LIST CORRECTION

CHANGE TO:

D225	152-0141-02	Silicon	1N4152
D228	152-0141-02	Silicon	1N4152
D236	152-0141-02	Silicon	1N4152
D277	152-0233-00	Silicon	Tek Spec
D284	152-0141-02	Silicon	1N4152
D282	152-0141-02	Silicon	1N4152
D311	152-0141-02	Silicon	1N4152
D314	152-0141-02	Silicon	1N4152

TYPE 3T2 TENT SN B101110

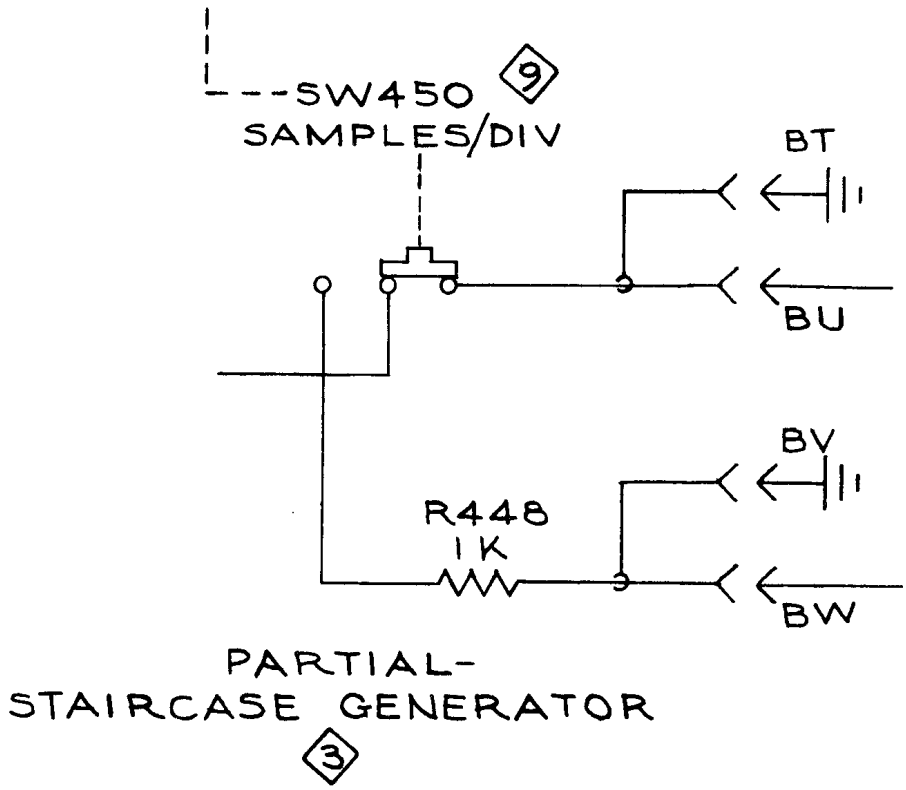
ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

CHANGE TO:

C453	283-0144-00	33 pF	Cer	500 V	1%
D454	152-0324-00	Silicon		Tek Spec	
D456	152-0324-00	Silicon		Tek Spec	
Q371A,B	151-0236-00	Silicon		Dual, Tek Spec	
Q391A,B	151-0236-00	Silicon		Dual, Tek Spec	

ADD:

R448	315-0102-00	1 kΩ	1/4 W		5%



PARTIAL-
STAIRCASE GENERATOR
3

TYPE 3T2 TENT SN B101110

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTION

CHANGE TO:

R213	321-0333-00	28.7 kΩ	1/8 W	1%

M15,651/1069

TYPE 3T2 TENT SN B121240

ELECTRICAL PARTS LIST CORRECTION

CHANGE TO:

Q791	151-0292-00	Silicon	NPN
Q793	151-0292-00	Silicon	NPN

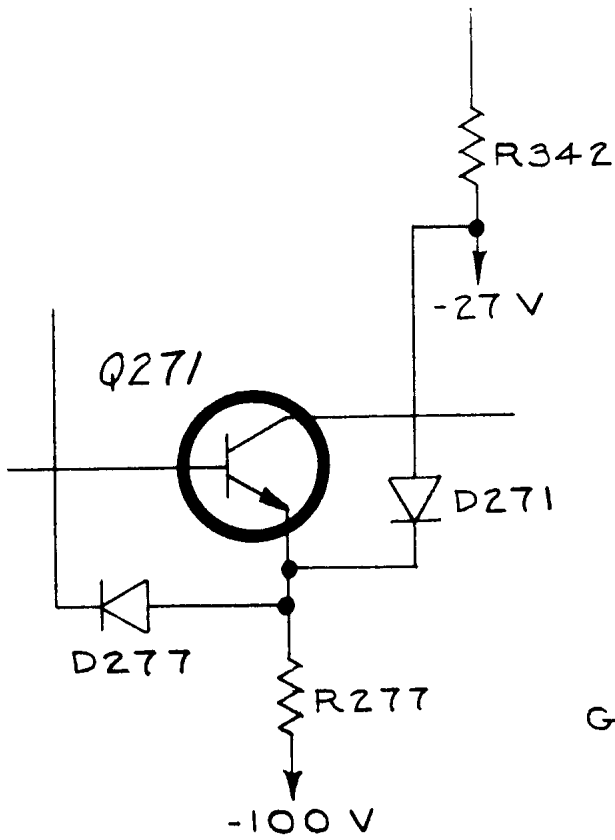
ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

CHANGE TO:

D277	152-0246-00	Silicon	250 mW, 40 V, Low-leakage

ADD:

D271	152-0185-00	Silicon	Replaceable by 1N4152



PARTIAL-RAMP GENERATORS
(2)