# INSTRUCTION MANUAL

Serial Number B030187

# TYPE 3S6 PROGRAMMABLE SAMPLING UNIT

MAY 1969

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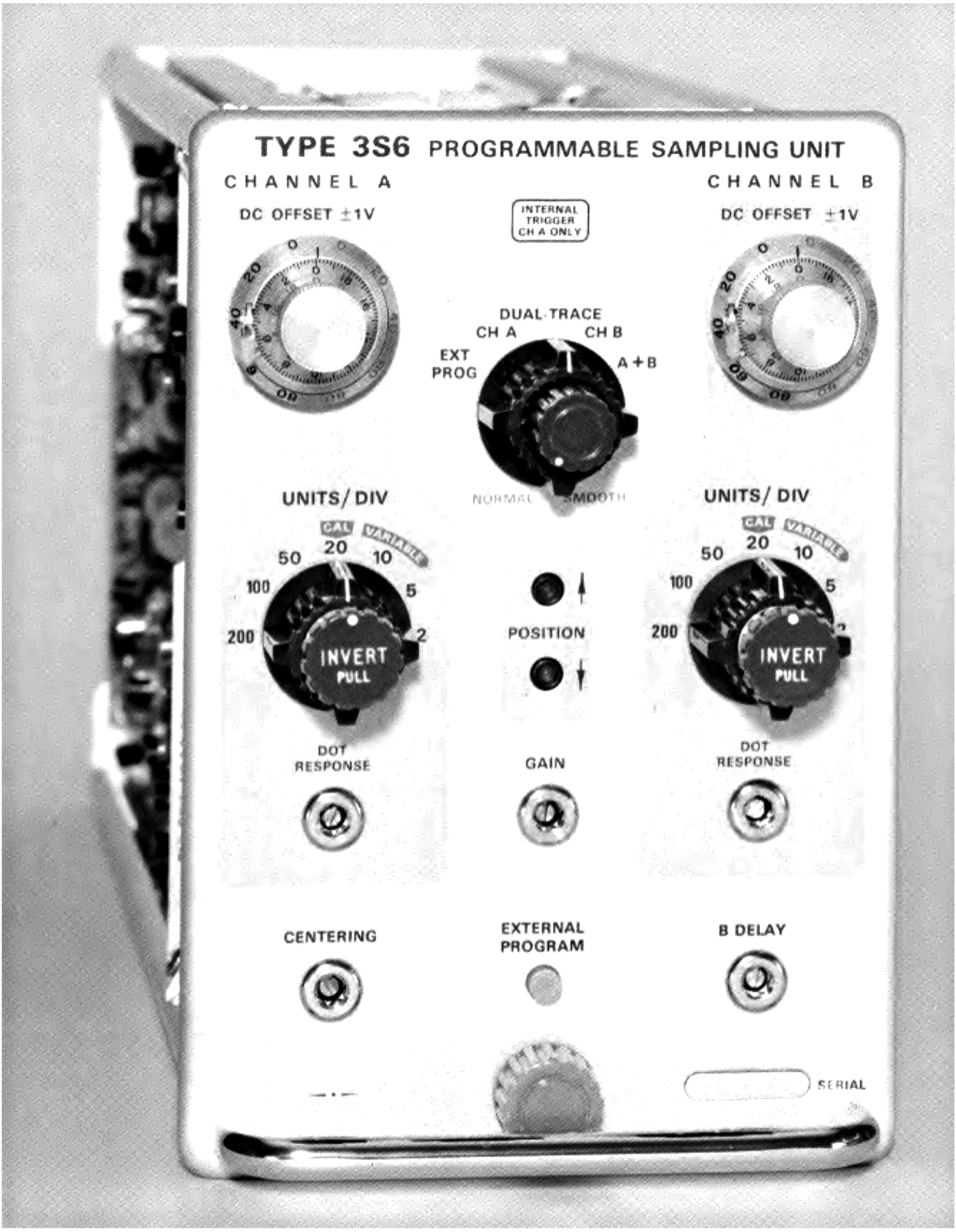

TYPE 3S6 PROGRAMMABLE SAMPLING UNIT
CHANNEL A
CHANNEL B
DC OFFSET ±1V
DC OFFSET ±1V
INTERNAL TRIGGER CH A ONLY
DUAL-TRACE
CH A
CH B
EXT PROG
A+B
NORMAL
SMOOTH
UNITS/DIV
UNITS/DIV
CAL
VARIABLE
50
20
10
100
5
200
2
INVERT PULL
POSITION
DOT RESPONSE
GAIN
DOT RESPONSE
CENTERING
EXTERNAL PROGRAM
B DELAY
SERIAL

# SECTION 1
# SPECIFICATION

**Change information, if any, affecting this section will be found at the rear of the manual.**

## General Information

The Type 3S6 Programmable Sampling Unit is a dual-channel vertical amplifier plug-in unit designed for operation in the Tektronix Type 568 Oscilloscope. The Type 3S6 accepts S-series sampling heads. The sampling heads determine the input characteristics of the sampling unit and the availability of trigger pickoff for internal triggering from Channel A.

The Type 3S6 will operate with any Tektronix 3T-series sampling unit. It is recommended that it normally be used with 3T6 Programmable Sampling Sweep. Both the Type 3S6 and the Type 3T6 can be externally programmed through a rear panel connector that is accessible through J214 of a Type 568 or R568 Oscilloscope. (Conventional or real-time time-base plug-in units do not operate with the Type 3S6.) The Type 3S6 provides the vertical signal information for amplitude measurements by a Tektronix digital readout system (Type 568-Type 230). Decimal and units control of the digital unit readout is also provided by the 3S6 including a sampling head deflection factor multiplier for sampling heads with sensitivities requiring the numbers around the Type 3S6 Units/Div control to have a decimal shift.

One or two S-series sampling heads can be used remotely on an interconnecting cable provided with the Type 3S6. This cable connects the sampling heads to J113 on the rear panel of the Type 568 Oscilloscope. Interconnecting wiring within the Type 568 connects J113 to J13 at the rear of the Type 3S6. The Type 3S6 provides the power for the sampling heads.

NOTE

**Earlier models of the Type 568 Oscilloscope require installation of Field Modification Kit Tektronix Part No. 040-0492-00, to provide an interconnecting path from the sampling heads to the Type 3S6 input circuits.**

Sampled signals are presented to the oscilloscope CRT vertical deflection plates. The two Type 3S6 channels may be displayed either individually, simultaneously, or in a combined mode, A + B, producing algebraic addition of two input signals. External programming of the Type 3S6 produces only simultaneous displays (Dual Trace) of the two channels. Individual channel displays are possible by offsetting the unused channel just outside the graticule area by external programming of DC Offset to the unused channel. A + B displays are not possible when externally programming the Type 3S6.

## ELECTRICAL CHARACTERISTICS

### Digital Unit Compatibility

The Type 3S6 is compatible for operation with all Type 230 (or R230) Digital Units.

### Characteristics

The following characteristics apply over an ambient temperature range of 0° C to +50° C and after a five minute warmup, providing the instrument was calibrated at a temperature between +20° C and +30° C.

Characteristics listed below apply for either front panel operation or external programming only after the Type 3S6 front panel GAIN control has been properly adjusted for the particular oscilloscope in which the unit is operating.

For particular system warmup requirements, refer to the Type 568 instruction manual.

A procedure for mating the Type 3S6 to the oscilloscope can be found in the Operating Instruction section.

## ELECTRICAL CHARACTERISTICS

| Characteristics | Performance Requirement |
|---|---|
| Deflection Factor | |
| UNITS/DIV Range | 2 to 200 in seven steps in a 1-2-5 sequence with Units/Div labeled on the sampling head. |
| Accuracy | Within 3%, when NORMAL-SMOOTH function is NORMAL, including sequential and random sampling. Within 4% when NORMAL-SMOOTH function is SMOOTH. (Not used with random sampling.) |
| Units/Div VARIABLE Range | Increases any display deflection at least 2.5 times when control is turned fully CW from CAL position. (Control also alters signal sent to digital unit. Control is inoperative when Vertical Mode switch is at EXT PROG.) |
| B DELAY Range | $\geq$ 10 ns |
| Interchannel Delay Range | At least +5 to −5 ns, with two of same type sampling heads; either both in Type 3S6 or both on identical length extender cables, and only when using time-coincident signals. |

## ELECTRICAL CHARACTERISTICS Cont'd

| Characteristics | Performance Requirement |
|---|---|
| Loop Gain<br>At NORMAL | Can be set to be < 0.90 to > 1.10 using the DOT RESPONSE control. |
| At SMOOTH | 0.3 X Unity Loop Gain (DOT RESPONSE control inoperative). |
| Low Frequency Trigger Rate Dot Slash | Vertical dot drift is 50.1 div when sampling sweep unit is triggered at 20 Hz. |
| Vertical GAIN control | Adjusts a post Memory amplifier gain so all deflection factors match the oscilloscope CRT deflection factor. |
| DC OFFSET<br>External Program controlled:<br>Range | —995 mV to +995 mV in 5 mV steps, programmed by a modified BCD code. |
| Accuracy | Within 2% of the programmed value, or 5 mV, whichever is greater. |
| Front Panel (Internal) Dial control:<br>Range | +1 V to —1 V. |
| Accuracy, expressed as relationship between dial number and the same voltage when externally programmed | Within 10 mV of the same offset voltage obtained in the external program mode. |
| Source resistance | 10 kΩ, within 1%. |
| Accuracy (referred to Input) | Within 2%. |
| Deflection Factor (Referred to CRT) | 200 mV per display division, within 3% at both positions of INVERT switch. |
| Source resistance | 10 kΩ, within 0.5%. |
| Accuracy of Vertical Signal to Digital Unit | Within 2% at NORMAL (typically 1%). Within 3% at SMOOTH. When Units/Div VARIABLE is at its CAL detent position. |
| CENTERING control Range | Control can move free-run trace at least +2 to —2 divisions from graticule centerline. |
| Position Indicator Lamps | One indicator lamp will be on and the other off when CRT dot is more than 4 divisions away from graticule centerline. |
| Programmable Functions | Both Channel Units/Div, DC Offset, and Smoothing. |
| Units/Div Multiplier | A digital unit readout decimal and units multiplier (milli) automatically responds to any sampling head multiplier of X0.1, X1, or X10 that may require the numbers around the Units/Div switches to have a decimal shift. |
| Type of Units | The Type 3S6 automatically controls a digital unit readout to indicate the Volts and Amps units of either channel sampling head. |
| External Programming Logic | Negative |
| Logical 1 (True) | Ground, or a voltage from 0 V to +2 V. See the operating instructions for current value required of the external closure circuit (Fig. 2-10). |
| Logical 0 (False) | Open circuit, or a voltage from +6 V to +15 V. See the Operating Instructions for leakage current values allowable when external closure circuit is a cut-off transistor (Fig. 2-10). |

## ENVIRONMENTAL CHARACTERISTICS

Storage

Temperature— —40° C to +65° C.

Altitude—to 50,000 feet.

Operating

Temperature—As stated above Electrical Characteristics table.

Altitude—to 15,000 feet.

## MECHANICAL CHARACTERISTICS

Dimensions—Height 6¼ inches

Width 4¼ inches

Length 14½ inches

Approximate dimensions including knobs and connectors.

Construction—Aluminum alloy chassis with epoxy laminated circuit boards. All circuit boards are removable without using a soldering iron. Two center-located circuit cards are of the plug-in type. The front panel is anodized aluminum.

Accessories—An illustrated list of the accessories supplied with the Type 3S6 is at the end of the Mechanical Parts list pullout pages.

# SECTION 4
# CIRCUIT DESCRIPTION

**Change information, if any, affecting this section will be found at the rear of the manual.**

## Introduction

This section of the manual contains a block diagram description and circuit description of the Type 3S6 Sampling Unit. The block diagram description is an expansion of Section 3, Basic Sampling Principles. The circuit description follows the sequence of diagrams at the back of this manual.

The Digital Unit Control circuits are described in Section 5, Digital Unit Control Description.

## BLOCK DIAGRAM

Refer to Fig. 4-1 and the complete block diagram at the back of this manual during the following description. Since most of Channel A and Channel B are identical, no reference is made to either channel except where they differ. Channel A occupies the top half of the block diagram.

Fig. 4-1 includes a simplified block diagram of a typical sampling head. The Type 3S6 Sampling Unit serves no useful purpose by itself, but functions as part of a sampling system only when a sampling head is connected. Therefore, the sampling head simplified blocks are included.

## Feedback Loop and Pulse Amplifier Chain

Fig. 4-1 relates to Fig. 3-4 and Fig. 3-7. The reconstructed signal of the Memory block (Fig. 4-1) is the first point in the Type 3S6 at which the amplitude is always a standard value of 0.5 volt per CRT vertical division. The signal between the sampling head output and the Memory output bears no similarity to the signal at the Memory output. Under ideal conditions, there is no signal between those two points whenever the sampling head input signal is at a steady value. The Post Amplifier, AC Amplifier and Memory Gate all are part of a pulse amplifier chain that amplifies the sampling head output signal just after each sample is taken. The pulse chain signals are greatest in amplitude when the sampled signal is at its full amplitude difference from the last sample (as in using the random sampling process in the Type 3T2 Random Sampling Sweep unit).

The smoothing, DC Offset, and the Units/Div circuit can be externally programmed when the Vertical Mode Switch is in the EXT PROG position. Programming is accomplished by connecting the program lines to ground at Pin A (rear panel) through saturated transistors or other closure types of programmers described in the Operating Instructions, Section 2.

Type 3S6 provides connections at J13 rear connector for all connections to the sampling head. From J13, connections are made to the logic control circuits to select the Units/Div Multiplier and the units of measure (Volts or Amps). These connections provide information to an external digital unit as described in Section 5, Digital Unit Control Description.

To complete the association in Fig. 4-1 with Section 3, the following describes the operating cycle:

a. The sampling head bridge applies an error signal to the head preamp whenever there is a voltage difference at the bridge input and output terminals at sampling time. The error-signal voltage amplitude is just a few per cent of the difference (sampling efficiency), and the pulse duration out of the bridge is equal to the bridge conduction time. A small storage capacitance at the head preamp input time-stretches the pulse so the pulse chain can amplify the error signal pulses at moderate rates of rise.

b. The time-stretched signal is amplified by the Type 3S6 Post Amplifier. Its gain is affected by the Smoothing circuit which operates in either the smooth or normal modes. The SMOOTH or NORMAL operation can be programmed externally in the EXT PROG position of the vertical Mode switch, or controlled from the front panel by the SMOOTH-NORMAL switch. In the Normal mode, the DOT RESPONSE control allows a small adjustment of the Post Amplifier gain to obtain unity loop gain. In the Smooth mode, the DOT RESPONSE control is disconnected. This reduces the Post Amplifier gain so that the sampling loop operates at about 0.3 of the gain in the Normal mode. The output of the Post Amplifier is capacitively coupled to the AC Amplifier and Forward Attenuator.

c. The AC Amplifier and Forward Attenuator block is an AC amplifier with its gain determined by the ratio of the feedback resistance to the selected input resistance. The Units/Div switch or external program, (through the Attenuator Decoder block) selects the input resistance and feedback circuit of the AC Amplifier. The attenuated or amplified pulse is applied to the Memory circuit during conduction time of the Memory Gate.

d. The Memory circuit applies its output voltage to both the vertical amplifier and the Feedback Attenuator block.

e. The Feedback Attenuator block attenuates the standard 0.5 Volt/Div signal from the Memory circuit and feeds it to the sampling head. Here the feedback voltage is combined with the DC Offset voltage and applied to the output side of the sampling bridge through the bridge balance circuit. The Units/Div switch or external program (through the Attenuator Decoder block) selects the attenuation of the Feedback Attenuator. The forward Attenuator operates concurrently with the Feedback Attenuator to maintain constant loop gain.

Fig. 4-1. Type 356 and sampling head feedback loop diagram.

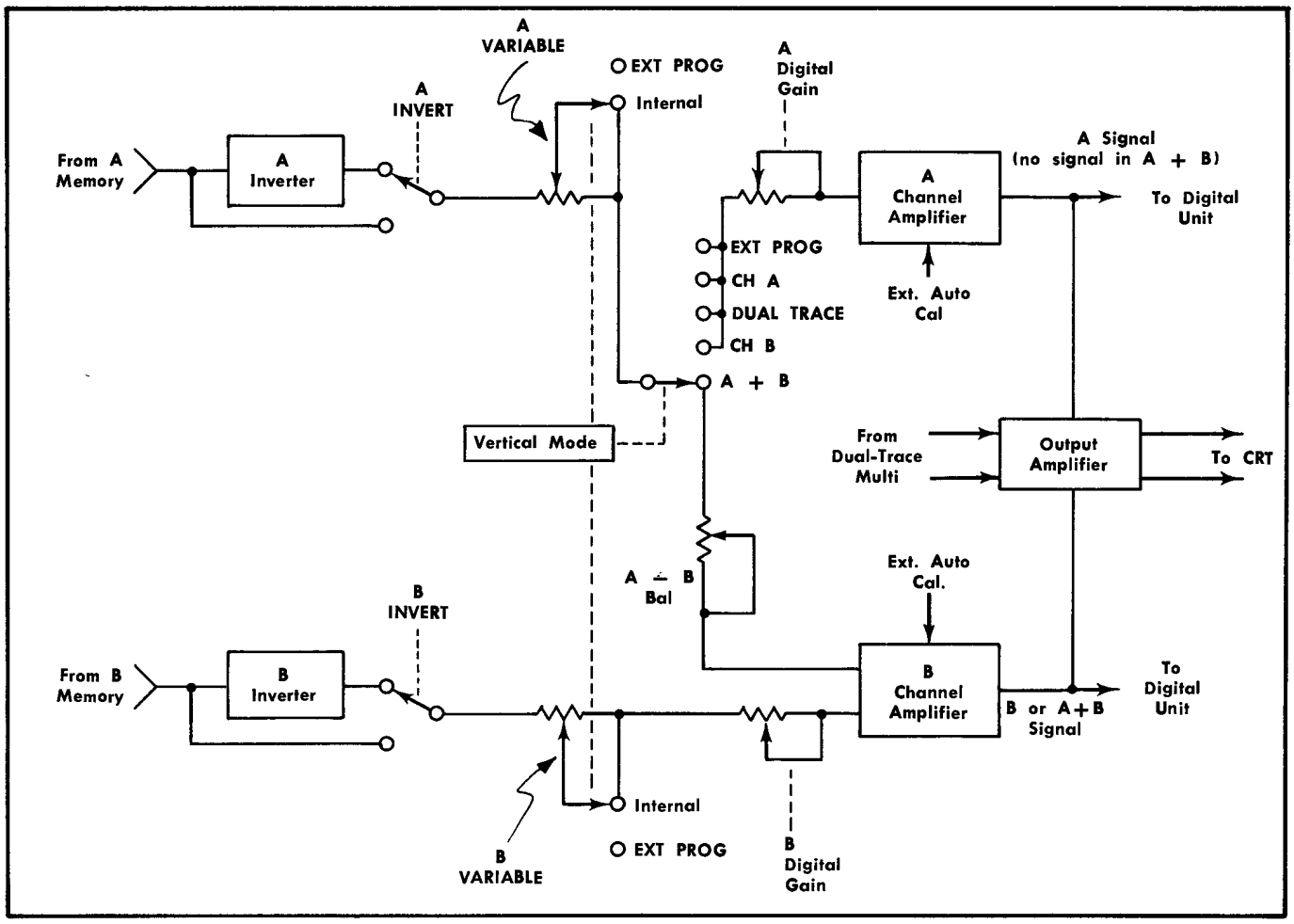



Fig. 4-2. A and B Vertical Channel block diagrams following the Memory showing A + B mode signal connections.

## Vertical Channel Following Memory

Blocks between the Memory and the CRT (see Fig. 4-2) include the inverter and the INVERT switch, the Units/Div VARIABLE control and internal Digital Gain control, the Channel Amplifier and the Output Amplifier with its input controlled by the Dual-Trace Multi. The Output Amplifier drives the indicator oscilloscope CRT vertical deflection plates directly.

The Inverter is a ×1 gain inverting amplifier that is normally in the circuit. The Inverter is by-passed when the INVERT switch is pulled out to invert the display.

The Channel Amplifier is a ×2 gain inverting amplifier with both the Units/Div VARIABLE and Digital Gain controls in series with the signal input.

During external program operation, the Units/Div VARIABLE control center arm is disconnected and does not operate. With external automatic calibration equipment connected to the proper pins of the external program connectors, the Channel Amplifier gain can be changed over a small range for calibration to a standard input signal. Except in A+B operation, the A and B Digital Gain controls allow the gain to be adjusted for a digital readout unit. (Channel A signal is disconnected in A+B operation.)

In the A+B position of the Vertical Mode switch, the B Channel Amplifier is driven by both Channel A and Channel B signals, providing algebraic addition displays. The A-B Bal control allows the Channel A signal to be balanced with the B signal in the A+B position.

NOTE

**The Channel Amplifiers drive the Output Amplifier and provide a signal output for a digital readout amplitude measurement.**

The Output Amplifier is a high gain inverting amplifier that drives the CRT vertical deflection plates directly. The input is from either Channel A or Channel B, selected by the Dual-Trace multi. The multi control circuit selects one channel continuously (CH A or CH B), alternates between channels after each sample (Dual-Trace and EXT PROG), or selects Channel B for algebraic addition (A+B).

The Position Lamp Driver circuit (not shown on the block diagram) monitors the DC voltage of the Output Amplifier lines and turns on the appropriate neon lamp to indicate whether the deflection voltage has placed the trace above or below the graticule center.

## Gate Generators

The Type 3S6 Gate Generator blocks consist of a Blocking Oscillator, Dual-Trace Driver, and two Strobe and Memory Gate Drivers. The Sampling Drive pulse from the sweep unit drives the Blocking Oscillator, which then drives the Dual-Trace Driver and both Strobe and Memory Gate Driver blocks.

Since the Type 3S6 will operate with several different sampling sweep units, the Gate Generator is designed to operate from slightly different Sampling Drive pulses. The Blocking Oscillator converts the normal variations in amplitude, risetime and duration of the Sampling Drive pulses to a standardized drive pulse with always the same amplitude, risetime and duration.

The Blocking Oscillator output pulse is converted to an RC ramp signal at both Delay circuits, and the (internal) A Delay and (front-panel) B Delay controls select a point along each ramp at which the Strobe Drive is generated. As the individual channel Strobe Drive is generated, the Memory Gate Driver causes the same channel Memory Gate to conduct. The duration of Memory Gate conduction is controlled by the Memory Gate Width control. Thus, a few nanoseconds after the arrival of the Sampling Drive pulse, a Strobe Pulse is sent to the sampling head, and the Memory Gate is driven into conduction. The instrument is calibrated so the B DELAY control alters the time of the Channel B Strobe Drive pulse approximately $\pm 5$ ns with respect to the Channel A Strobe Drive pulse (when both sampling heads are the same type).

The Dual-Trace Driver circuit drives both the CRT blanking circuit (to extinguish the CRT beam while the dot is being moved between samples) and the Dual-Trace Multi. If the Vertical Mode switch is at DUAL-TRACE or at EXT PROG, the Dual-Trace Driver causes the Dual-Trace Multi to change state at the time each sample is taken.

## Internal Trigger

The Type 3S6 couples a Channel A sampling head internal trigger pickoff signal directly from J13 (rear panel sampling head interconnector) to P11 (indicator oscilloscope horizontally mounted interconnector) through a short section of coaxial cable. P11 couples the Channel A internal trigger signal through the indicator oscilloscope J11 directly to the sampling sweep unit rear panel interconnector. The Channel B sampling head trigger pickoff circuit is terminated in 51 Ω at the Type 3S6 rear panel J13 connector. Internal triggering is thus possible only from Channel A sampling heads that contain trigger pickoff circuitry.

# CIRCUIT DESCRIPTION

The following circuit description sequence follows the order of the diagrams in Section 10.

## Programmed Amplifiers and Attenuators

The Programmed Amplifiers and Attenuators diagram for each channel includes the Post Amplifier, Smoothing, AC Amplifier, Forward and Feedback Attenuators, and Attenuator Decoder circuits. The Forward Attenuator is described as part of the AC Amplifier. The Feedback Attenuator circuits include a $\times 2$ gain operational amplifier. Where the two channels are identical, the operation of only one is described. Differences between the channels are discussed in detail.

**The Post Amplifier** is a two-stage non-inverting operational amplifier with complementary emitter followers at the output. Low output impedance drives the Forward Attenuator resistors of the AC Amplifier. The input resistance of R13 (CH A) terminates the coaxial cable feed from the sampling head preamplifier. The coaxial cable shield is DC isolated from ground to provide a Units/Div Multiplier control connection from the sampling head to the Digital Unit Control circuits. The gain of the Post Amplifier is changed by varying the resistance of R9 or disconnecting R9 to change the feedback. The Smoothing circuit has two modes of operation, Normal and Smooth. In the Normal mode Q8 is saturated, allowing the DOT RESPONSE control to adjust the gain of the Amplifier. In the Smooth mode, the DOT RESPONSE control is disconnected by cutting off Q8. This increases the feedback and decreases the gain of the Post Amplifier. Total Post Amplifier AC gain (in Normal mode) with unity loop gain is approximately 11, producing a 2.2 volt output signal at TP25 for a 0.2 volt input signal at Q15 base. DC gain is about two, and DC feedback keeps the Amplifier within its proper dynamic range.

Q15 and Q16 provide voltage gain while Q19 and Q22 are the output emitter followers. Q19 assures low output impedance for positive output signals, and Q22 provides low output impedance for negative output signals. Each emitter follower has a resistor in the collector for parasitic oscillation suppression. C20 permits the output emitters to be at different DC voltages.

The Smoothing function is either internally or externally controlled, depending upon the position of the Vertical Mode switch. For front-panel operation of the NORMAL/SMOOTH switch, the switch is an open circuit at NORMAL and grounds the Smoothing circuit input at SMOOTH.

At NORMAL, R3, R4 and R5 bias Q6 to cutoff and R7 biases Q8 on to saturation. The low saturation resistance of Q8 connects one end of the DOT RESPONSE control (R9) to ground. This connects R9 in parallel with R10 in the Post Amplifier AC feedback circuit. C11 is allowed to bypass more signal, thereby reducing the AC feedback. Thus, the Post Amplifier gain can be adjusted over a small range by the DOT RESPONSE control.

When the NORMAL/SMOOTH switch is at SMOOTH, D3 conducts and R4 biases Q6 to saturation. Q6 collector voltage turns Q8 off, disconnecting the DOT RESPONSE control from ground. With R9 disconnected, R10 resistance in series with R11 and C11 increases the Post Amplifier AC feedback voltage and thus decreases the gain. This reduces the sampling loop gain of the Type 3S6 to 0.3 or less compared to the loop gain at NORMAL.

External programming of the Smoothing circuit merely duplicates the NORMAL/SMOOTH switch functions when the Vertical Mode switch is at EXT PROG. A logical ONE or a ground closure programs the SMOOTH mode and a logical ZERO or an open circuit programs the NORMAL mode.

**The AC Amplifier and Forward Attenuators** consist of an inverting operational amplifier with complementary emitter follower output circuit. The AC Amplifier gain is changed whenever the Units/Div switch (or external program) is changed. Control is by FET switched input resistors together with a transistor-switched feedback circuit.

The gain change function of the amplifier is called the Forward Attenuator because it affects the signal amplitude

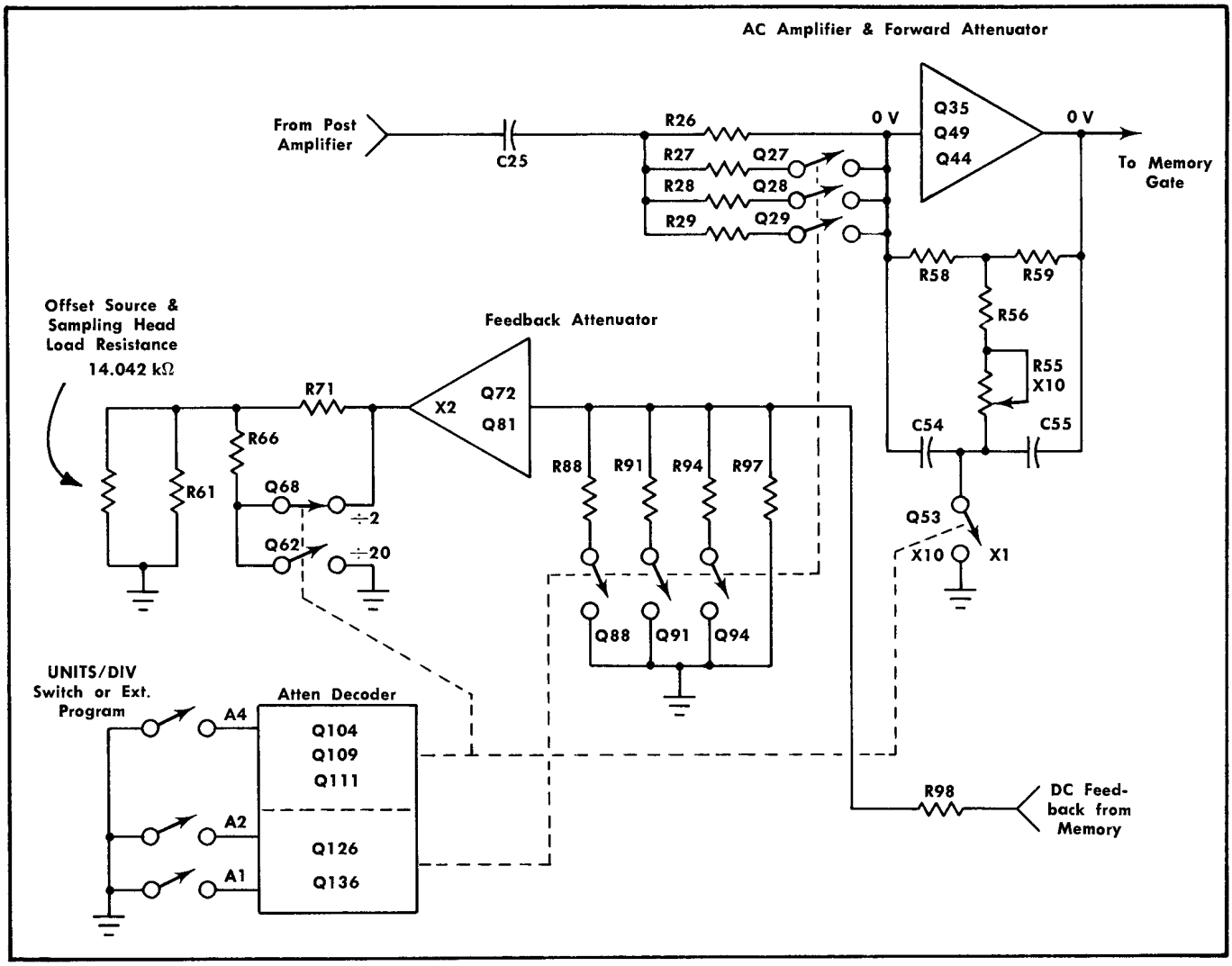



**Fig. 4-3. Simplified Programmed Amplifiers and Attenuator diagram.**

through the circuitry from the Post Amplifier to the Memory input. Fig. 4-3 shows the AC Amplifier input resistors R26 through R29. R27, R28 and R29 are connected into the circuit by Q27, Q28 and Q29 (shown as switches in Fig. 4-3) to change the input resistance and thereby the gain. These FET's are held at low resistance conduction (less than 30 Ω) or at cutoff by the Attenuator Decoder circuit (from logic lines A1 and A2). The A4 line (through the Attenuator Decoder block) controls the AC Amplifier feedback network by turning Q53 on or off. Q53 saturation increases the gain of the amplifier ten times by reducing the feedback to 0.1 its normal value. The feedback circuit consists of R59-C55, R58-C54 and R55-R56. The Decoder circuits operate the Feedback Attenuator circuits simultaneously so that the sampling loop gain is maintained constant. (See Section 3 for loop gain relationship between forward and feedback attenuators).

Schematic diagram 1 has truth tables in the AC Amplifier section showing the relationship between the lines A1, A2 and A4, and the transistors' on-off states.

At quiescence, the base of Q35 in the AC Amplifier is at 0 volts. Temperature compensation for Q35 is provided by D37. Q35 collector voltage is about +10 volts, and Q49 emitter follower output is slightly negative (between —0.25 V and ground). 0 volts input (at Q35 base) allows Q27, Q28 and Q29 to be biased off or on by the Attenuator Decoder circuits. When Q53 is turned on to change the gain of the AC Amplifier, Q53 connects the center of the feedback circuit to ground with about 125 Ω (R55 and R56). This causes only about 0.2 volt shift in the output quiescent voltage. R55 is adjusted for a gain increase of exactly ×10 when Q53 is saturated.

Two possible Q111 collector voltages of —24 or +7 V control Q52 and turn Q53 on or off. Operation is as follows: When the collector of Q111 is at +7 volts, R51 and D51 back bias Q52 by about 0.5 volt. With Q52 off, R53 turns Q53 on. The —24 volts from Q111 collector saturates Q52. This sets Q53 base positive and turns off Q53.

The summing input of the AC Amplifier (at Q35 base) receives both the input signal from the Post Amplifier (through C25 and the FET-selected input resistors) and the feedback signal from the feedback network. Q35 amplifies the signal and drives the bases of emitter followers Q49

and Q44. Q49 provides a low output impedance for positive signals and Q44 provides a low output impedance for negative signals. Q44 is AC-coupled to the output by C47. R48-C48 and R45-C45 are power supply decoupling networks in the collector circuits of Q44 and Q49. D42 protects Q44 base-emitter junction if Q35 is removed from its socket. The low output impedance of the AC Amplifier is required to drive the Memory Gate circuit for full screen transitions.

**The Feedback Attenuator** circuit consists of a selectable attenuator network at the input of a non-inverting ×2 gain operational amplifier (Q81-Q72) and a divide-by-two or divide-by-twenty divider network between Q72 and the sampling head. See Fig. 4-3. Attenuator resistors are changed by special low resistance FET transistors, drawn as switches in Fig. 4-3. The ×2 amplifier low output impedance drives the divider network R71, R66, R61 and 14.042 kΩ. The 14.042 kΩ consists of the Offset circuit output resistance in parallel with the sampling head bridge volts circuit resistance.

The CH A (CH B) Programmed Amplifier and Attenuators diagram shows truth tables listing the feedback attenuation as a percentage of the Memory DC output voltage. The input to the Feedback Attenuator at point (A) is the Memory signal at the standard deflection factor of 0.5 volt per displayed division. The truth table shows the percentage of memory output signal that reaches Q81 base at point (B). Q88-Q91 and Q94 turn on and ground appropriate attenuator resistors as a function of the program applied to the A1 and A2 lines, altering the signal at point (B). The output signal at point (C) is also included in the truth tables as a percentage of the voltage at (A). Q62 and Q68 turn on alternately and ground appropriate attenuator resistors as a function of the program applied to the A4 line. Point (C) voltage provides current through R71 and/or R66 to the DC Offset and sampling head circuits so that the voltage across R61 is held at about zero with no sampling head input signal.

Q72 and Q81 operate as a ×2 gain, non-inverting operational amplifier between the two attenuator networks. R75 and R79 (both 0.1% tolerance resistors) set the gain at ×2. The amplifier has high input resistance at Q81 base, and very low output impedance at Q72 collector. This low output impedance drives the 2×/20× divider network.

The collector signal of Q81B drives Q72 base. Q72 collector drives the output and provides a feedback signal to Q81A base through R75 and R79. The common emitters of Q81 complete the feedback path and provide temperature compensation. All quiescent base current of Q81B passes through R85, and all quiescent base current of Q81A passes through R78. Base currents from both halves of Q81 pass through Attenuator Zero control, R86. R86 is adjusted during calibration so that Q81 base currents do not offset the Memory output signal as it passes through the Feedback Attenuator networks. The Attenuator Zero control requires adjustment only if Q81 or Q72 is replaced. The adjustment assures that when the Memory output voltage is zero, the output voltage at Q72 collector is nearly zero. R73 and C73 comprise a power supply decoupling network. C72 slows the amplifier risetime, preventing self oscillations.

**The Attenuator Decoder** circuit has two sections; 1) Q104, Q109 and Q111 controlled by the condition at the A4 line and 2) Q126, Q136, D129 and D136 controlled by the conditions at the A1 and A2 lines. The circuits work together to turn on or cut off field effect transistors (FET) in the Feedback Attenuator and the Forward Attenuator circuits according to the Units/Div (deflection factor) programmed. The Units/Div can be controlled from the front panel, or externally programmed depending on the setting of the Vertical Mode switch. Conditions required at the A1, A2 and A4 lines are identical for either internal or external control. A "true" logic state ONE must place A1, A2 or A4 between 0 V and +2 V or at ground. A "false" logic state ZERO must place A1, A2 or A4 between +6 V and +15 V or be an open circuit. The Programmed Amplifier and Attenuator diagrams show truth tables listing the correct circuit voltages for both logic states of the input lines.

The A4 decoder circuit controls Q62 and Q68 in the Feedback Attenuator and Q53 in the AC Amplifier circuit. When the A4 line is grounded the decoder and the attenuator respond as follows:

When A4 = ONE: D101 conducts by current in R101 permitting R102 and R103 to forward bias Q104. Q104 positive collector voltage forward biases Q109, setting Q109 collector voltage at approximately —25 volts. This voltage forward biases D110 and D69. D69 conduction couples the —25 volts to Q68 gate, causing Q68 to cut off. At the same time D110 conduction couples the —25 volts to Q111 base, reverse biasing Q111. With Q111 off, its collector voltage is set at +7 volts (caused by conduction through R111, R51 and D51) reverse biasing D64. Q62 gate is zero biased by R63. Zero bias to Q62 sets its channel resistance to less than 30 Ω, in effect grounding one end of R66. Conduction of D51 in the AC Amplifier reverse biases Q52 and protects Q52 from excessive reverse bias. With Q52 off, R53 turns on Q53. Therefore, with a logical ONE at A4, Q62 and Q53 are on and Q68 is OFF. If A4 condition is a logical ZERO, Q62 and Q53 will be off and Q68 will be on.

The A1, A2 decoder circuit controls six attenuator FET's. Q136 is controlled by the A1 line and Q126 is controlled by the A2 line. Both transistors drive attenuator FET's and the OR gate, D129-D136. Q136 controls both Q94 in the Feedback Attenuator and Q27 in the Forward Attenuator. Q126 controls Q88 in the Feedback Attenuator and Q29 in the Forward Attenuator. The OR gate circuit controls Q91 in the Feedback Attenuator and Q28 in the Forward Attenuator.

When either or both of the Units/Div logic lines A1 and A2 are grounded (for a logical ONE), the decoder and attenuator networks respond as follows:

1. When A1 = ONE: D131 conducts, causing R132 and R133 to forward bias Q136. With Q136 saturated, its collector voltage of +3.4 to +3.5 volts back biases D139. This causes R139 to zero bias both Q94 and Q27.

2. When A2 = ONE: D121 conducts, causing R122 and R123 to forward bias Q126. With Q126 saturated, its collector voltage of +3.4 to +3.5 volts back biases D128, which causes R128 to zero bias both Q88 and Q29.

3. When A1 and A2 both = ONE: the +3.4 volts at the OR gate inputs (D129 and D136 cathodes) reverse biases both gate diodes so their common anode voltage is held at zero by R137. R137 applies zero bias to both Q91 and Q28.

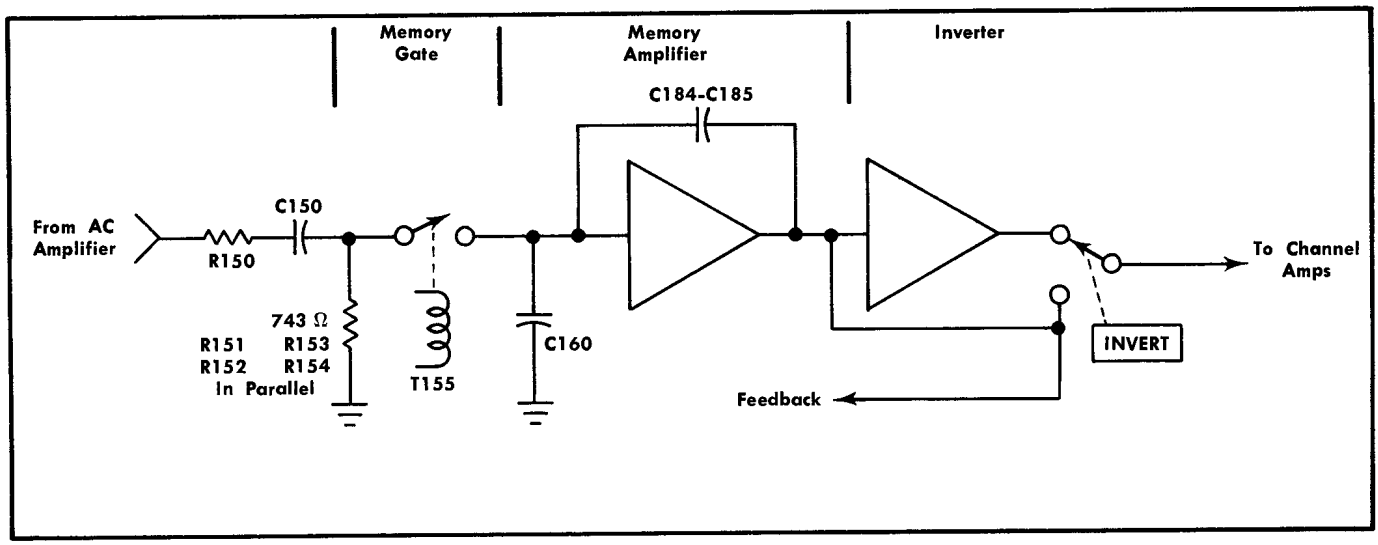



**Fig. 4-4. Detailed block of Memory diagram showing basic Memory Gate circuit.**

If only A1 or only A2 is grounded, the OR gate holds both Q91 and Q28 in heavy reverse bias (by conduction of D137), and they are both open circuits. Only two positions of the Units/Div switch (or two externally programmed deflection factors) 20 and 2, cause all three feedback attenuator input sections and all three AC Amplifier input sections to be active.

D137 conduction limits the negative voltage to —26 volts and thus protects both Q126-Q136 and the FET's from the —100 volts supply when Q126 and/or Q136 are at cutoff.

## Memory Diagram

The Memory diagram of each channel includes the Memory Gate, the Memory Amplifier and the Inverter. The AC Amplifier signal pulse is applied to the Memory circuit during the conduction time of the Memory Gate. The resulting DC signal from the Memory circuit output drives the Feedback Attenuator, the Inverter and the INVERT switch. The Inverter is normally in the circuit to drive the Channel Amplifier circuits through the INVERT switch. The Inverter is by-passed when the INVERT switch is pulled out to invert the display.

The Memory Gate is a pulse-driven diode gate that assures a very high input resistance to the Memory Amplifier except for about 0.15 to 0.2 $\mu$s at the time of each sample. During conduction time, the Memory Gate is a low impedance that allows the AC Amplifier to introduce charge to the Memory input through R150, C150 and the gate diodes' conduction resistance.

Fig. 4-4 is a detailed block diagram of the circuits on the Memory diagram. The Memory Gate is represented by a resistor, a coil and a relay switch. The resistor is the parallel value of the four biasing resistors which assure that the four gating diodes are normally not conducting. This equivalent circuit shows that the Memory Amplifier input is zero volts when there is no error signal at sample time.

Looking from the Memory Gate toward its input, the four gating diodes are normally reverse biased by the voltage of Zener diode D151. (Two of the four diodes provide very high reverse biased leakage resistance, although they don't turn off very fast. The other two turn off fast at the end of the gating pulse, although they don't provide high resistance when reverse biased). D151 voltage is balanced to ground by R153 and R154 so D156 cathode rests at +2.5 volts and D158 anode rests at —2.5 volts. C151 assures that the AC Amplifier output signal drives both sides of the Memory Gate diodes.

The gate diodes are forward biased into conduction by T155 at the time of each sample due to the drive pulse from the Memory Gate Driver. T155 is a toroidal transformer specially wound to balance capacitive and inductive coupling to the two secondary windings. The winding with only one end connected provides the capacitive balance. The magnetic toroid core provides the inductive balance. Thus, the drive pulse is converted to identical drive signals to assure that the output junction of the four diodes accurately divides the 5 volts of D151-C151. This places the junction of D157-D159 at ground when no error signal is applied from the AC Amplifier. The functions of the two limiting diodes D153-D154, and the Memory Gate, are discussed in the Memory Amplifier description next. R156, R158 and D155 are shunt damping loads to T155 which minimize self inductance ringing when the memory gate drive pulse ends.

**The Memory Amplifier** is an integrating operational amplifier with special low leakage (high DC resistance) input circuit. The input and feedback components are capacitors, making the AC input impedance very low. The internal high gain assures a very low output resistance, so that as long as there is no change at the input, the output DC voltage remains stable. The input low leakage circuit has no DC connection to ground except during the time the Memory Gate conducts.

The Memory Amplifier is specially decoupled from the power supplies because the output stage (Q181 and Q182) can require a current pulse as great as 30 mA for a 20 volt output change at sample time. The decoupling networks are: R161-C161, R180-C180 and R183-C183. L197 in the output lead to the INVERT switch, presents a high impedance to the Memory output for high frequency (fast change) sig-

nals. The inductor assures that the output amplifier does not have to provide high current to the output load. L197 slows the output signal response, but at a time when the CRT is blanked.

A dual junction FET (Q162) is the input stage. It is biased for essentially no leakage at the input gate, and the stage has high voltage gain at the in-phase output drain lead. Any voltage change at Q162 gate lead is amplified and applied to the inverting amplifier Q174. Q174 collector circuit applies proper bias to both bases of the output complementary emitter follower pair Q181-Q182, and restores the DC level so a zero input signal (at Q162A) causes a zero output signal. Q174 collector and Q181-Q182 outputs operate linearly through the range of +10 to —10 volts.

Positive feedback is supplied through R178 to Q162B gate to increase the open-loop gain and thereby reduce the input resistance of the Memory Amplifier. The Memory Amplifier has a slower risetime than the Post and AC Amplifiers. C160 and Q162 input gate lead accepts some of the charge from the AC Amplifier, temporarily storing it until the Memory Amplifier can respond.

A cycle of operation at sample time takes the following sequence:

a. The Memory Gate drive pulse arrives at essentially the same time the Sampling Bridge is strobed into conduction. Propagation delay through the three AC coupled amplifiers is quite short. The CRT is blanked at the same time. The fact that the Memory Amplifier input is always at zero volts, and the Memory Gate is balanced around zero volts, prevents any false changes in C184-C185 charge. Therefore, there is no change in the Memory Amplifier output voltage during the time the Memory Gate conducts ahead of the arrival of the AC Amplifier output signal.

b. The AC Amplifier applies a pulse signal through R150-C150 and the Memory Gate to the Memory Amplifier input. C160 accepts some of the charge until the amplifier begins to respond, driving an equal and opposite current back to the input through the feedback capacitors.

c. Since the AC Amplifier output signal is applied to the Memory Amplifier "virtual signal ground" input, C150 receives about 10% of the total error signal charge before the Memory Gate stops conducting. Thus, as the AC Amplifier output returns to its quiescent voltage, the output side of C150 overshoots. The 743 Ω (resistance of R151, R152, R153, R154 in parallel) of the Memory Gate discharges C150 well in advance of the next error signal.

If the Type 3S6 is displaying a single transition step over the full graticule with the display starting at the lower left and ending at the upper right, the error signal is very large during retrace. Such large error signals (even during random process sampling) apply a significant charge to C150. Then the overshoot at the end of the error signal pulse is large enough to cause one side of the Memory Gate to conduct, and remove some of the intended charge in the feedback capacitors. Two normally non-conducting clamp diodes prevent such undesired removal of memory charge. D153 and D154 help to discharge C150 if it receives too large a charge during the Memory Gate conduction time, thus preventing false amplitude displays. These two diodes do not conduct at any other time.

d. As the Memory Gate drive pulse ends, C160 charge is removed by the Memory Amplifier feedback. This causes the Memory output voltage to continue changing toward proper amplitude for a short period after the Memory Gate stops conducting. As soon as C160 charge is returned to normal, the output voltage remains fixed until the next sample.

The actual resting voltage at Q162A gate may not be precisely zero, but it is within a few millivolts of zero. Any deviation from zero can be due to several things: slight differences in conduction of the Memory Gating diodes; slight differences in resistance of the four Memory Gate biasing resistors; some small error signal being generated at each sample time even when the sampling head input signal is zero. Q162B gate voltage is adjusted over a small range to allow the above normal variations. Adjustment of Q162B gate voltage is called the Smoothing Balance adjustment, because it is set so there is no change in Memery Amplifier output when the forward attenuation or gain is changed. The Post Amplifier gain is changed (through the smoothing circuit) by changing the NORMAL/SMOOTH switch from because it is set so there is no change in Memory Amplifier output when the forward attenuation or loop gain is changed. one position to the other or doing the equivalent by external programming. Whatever small zero-input error signal may exist in the system, it always has an average value that will not alter the memory stored charge. Changing the forward attenuation or loop gain changes the peak amplitude of the residual error signal, but not its average voltage zero value. Therefore, Q162B gate voltage is adjusted to equal the average voltage zero value of the residual error signal, and the trace does not move when changing the NORMAL-SMOOTH switch position.

Memory output voltage limits of about +10 and —10 are set by two diodes in parallel with the feedback capacitors. The diodes, D187 and D188 are reverse biased by 9 volts each. If the output tries to go more positive than about +10 volts, D188 conducts (9 + 0.6 = 9.6 volts) reducing the amplifier gain to much less than 1. If the output tries to go more negative than about —10 volts D187 conducts, reducing the amplifier gain to much less than 1. The clamping diodes prevent the amplifier output transistors from saturating at the time of an overdrive signal, and thus assure fast response away from the clamped voltage at the next sample.

The amplifier contains two protective diodes that conduct only when a transistor is removed from its socket. D163 prevents Q162 source leads from having to withstand —100 volts when it is plugged into its socket while the power is on. D173 protects Q174 base-emitter junction in the event Q162 is removed from its socket while the power is on.

Temperature compensation of the amplifier is accomplished effectively by the source-coupled FET input amplifier and D176 and D177. The two identical halves of Q162 compensate each other so their total current does not change with temperature change. D176 and D177 have junction-drop temperature coefficients similar to Q181 and Q182 base-emitter junctions, and thus stabilize the output circuit.

The Memory Amplifier output signal drives the feedback attenuator circuit. The signal is the standard deflection signal mentioned in Section 3, 0.5 volt/CRT division. The memory also drives a X1 gain inverting amplifier (the Inverter) because the rest of the vertical amplifier stages (Channel Amplifier and Output Amplifier) invert the signal to the CRT.

NOTE

**The Memory output limit of +10 volts at 0.5 V/div equals 40 CRT divisions of displayed area, required to keep amplitude limiting off screen. The whole pulse amplifier chain is designed for full response and fast recovery so that on-screen displays have accurate deflection factors and DC offset reference.**

**The Inverter Amplifier** is a temperature compensated DC coupled operational amplifier with a gain of 1. R194 and R190 (0.1% tolerance resistors) set the gain. Q190 and Q192 emitter-coupled stage provides both the temperature compensation and high internal gain. Q195 provides the inversion and negative signal offset so the input and output can both be at zero volts at the same time. Q195 collector has the same +10 volt operating range as the Memory output. L195 raises the load resistance during fast changes at sample time to limit the pulse current amplitude required of the —12.2 volt supply at Q195 emitter.

Protective components are D190, which conducts when Q195 is removed from its socket and protects Q190 base emitter junction from excessive reverse bias; D195, which conducts when Q192 is removed from its socket and protects Q195 base-emitter junction from excessive reverse bias; and C195, which stabilizes the amplifier against self-oscillation.

The Inverter drives the Channel Amplifier through the INVERT switch and the VARIABLE and Digital Gain controls.

## A and B Channel Amps

The two Channel Amplifiers are ×2 gain inverting operational amplifiers. The input circuit switching by the Vertical Mode Switch disconnects the Units/Div VARIABLE controls, so that they are at maximum resistance at EXT PROG. The switch also connects the A signal into the B Channel Amplifier in the A+B position. The gain is adjusted by the Digital Gain control (with the Units/Div VARIABLE control at maximum resistance, and the Vertical Mode switch not in the A+B position) so that the output to the Digital Unit is the required 1 V/Div. A center-screen zero signal input produces an output of about +10 volts. The output voltage can swing through approximately a 20-volt range, corresponding to ±10 CRT divisions.

The input summing point of both amplifiers is referenced at zero volts at the base of Q413 (Q433). Q413 biasing is set by D414. D414 also provides temperature compensation. The input signal divider network R401 (Units/Div VARIABLE control), R404 (Digital Gain control) and R405 in series with R407 to ground, divide the signal before it feeds through R408 (499 Ω input resistor) to the summing input point at Q413 base.

The Digital Gain control varies the series resistance of the divider network as does the Units/Div VARIABLE control. To use **Auto Cal** disconnect R407 by removing the strap diagrammed directly above R407, and provide a remote resistor that substitutes for R407. Varying the external resistance above and below the value of R407 (from 7.9 kΩ to open circuit) changes the amplifier input current division and the amplifier gain is changed accordingly. A similar arrangement using R427 is provided in Channel B. See the Operating Instructions for additional information on Auto Cal.

Placing the Vertical Mode switch at A+B disconnects the A signal from the A Channel Amplifier input and feeds it to the B Channel Amplifier through the A-B Bal control R430 and R431. Thus the A and B signal currents are combined at the B Channel Amplifier input current summing point, Q433 base. The B Channel Amplifier then provides the algebraic sum of the two signals at its output to the Output Amplifier and the Digital Unit.

Q413 is the inverting amplifier and Q418 is the current gain emitter follower output. When a positive signal overdrives the amplifier, both Q413 and Q418 turn on hard, and both transistors may saturate. When a negative drive signal overdrives the amplifier, Zener diode D417 and D416 limit Q418 emitter voltage to about +20.7 volts, stopping any increase in feedback current. Once the feedback current stops following the input current, the summing input point becomes a higher impedance and starts negative. Q413 is completely cut off. D418 catches its collector at +21.3 volts, and D405 catches its base at less than —1 volt. The amplifier remains in this condition until the negative overdrive ceases.

D405 and D406 limit the input signal drive to the amplifier. C413 slows the amplifier risetime, preventing high frequency oscillations. D416 disconnects Zener diode D417 until the diode is required to clamp a positive excursion at approximately +20 V.

## Output Amplifier

The Output Amplifier diagram contains circuits for three blocks of the complete block diagram: The Dual-Trace Multi, the Output Amp and the Position Lamp Driver.

The Dual-Trace Multi selects which Channel Amplifier drives the Output Amplifier. Dual-Trace Multi operation is programmed by the Vertical Mode switch on the front panel. The Dual-Trace Multi is actually a multivibrator when the Vertical Mode switch is placed in the DUAL-TRACE or EXT PROG position. At the other modes of operation, the Dual-Trace Driver signal is diode-disconnected, and only one of the two transistors may conduct. A conducting transistor takes the signal current of the channel not displayed, and a non-conducting transistor permits its associated channel to be displayed. Multi transistor Q450 controls Channel B, and Q455 controls Channel A.

The signals of the Channel Amplifiers are coupled to the digital output connector (P12) by L465 and L460. L465 and L460 prevent oscillation in the A and B Channel Amplifiers by isolating the capacitance load of the digital unit. The Channel Amplifier signals are also coupled into two grounded base amplifiers. These amplifiers share the collector load resistance of R463, R467 and R470 in parallel. Only one of the common base amplifiers (either Q461 or Q466) is connected to the collector load resistance at a time. The Output Amplifier diagram lists DC voltages for displaying Channel A.

Q450 conduction (controlled by the Vertical Mode switch set to CH A) forward-biases D461 so that Q461 collector volt-

age reverse-biases D462. This disconnects the Channel B signal from the Output Amplifier. Q455 non-conduction permits R459 to reverse bias D466. Thus Q466 collector current path is through D467 and the Channel A signal reaches the Output Amplifier input.

Dual-Trace operation forward biases D441 so the —50 V to 0 V Dual-Trace Driver signal can reach the Dual-Trace Multi and switch it at each sample time. Each time a sample is taken, the Dual-Trace Multi changes on the positive portion of the drive pulse. Each time the multi changes states, the Output Amplifier is driven by the other channel. The multi divides the sampling rate by two and delivers a Digital Intensified Zone Enable signal (up = logical ZERO at about +1 volt = CH A; down = logical ONE at about —1 volt = CH B) to the digital unit from Q450 collector.

**The Output Amplifier** consists of the high gain stage Q477 and Q478, and a ×1 inverting amplifier Q487 and Q488. The high gain stage drives the inverter. Both circuits are DC coupled operational amplifiers with a common negative point at Zener diode D480.

Signals arrive from the common-base stages Q461 and/or Q466 and pass through the front panel GAIN control to the summing input at the base of Q477. The front panel CENTERING control also applies a DC signal to the same summing point, permitting positioning of the trace on the screen.

Signals are amplified by Q477 and given current gain by emitter follower Q478. (All four Output Amplifier transistors have $BV_{CBO}$ ratings of 300 volts). D479 connects Q477 collector to the output if Q478 base falls faster than its emitter for fast full screen positive-going changes. Q478 emitter also drives the ×1 inverter input.

The inverter amplifier is identical to that just described, except that the gain is 1. D489 connects Q487 collector to the output if Q488 base falls faster than its emitter for fast full screen negative-going changes. Both sides of the Output Amplifier drive the Position Lamp Driver stage.

**The Position Lamp Driver** is a floating current switch that operates the two position-indicating neons on the front panel.

The average voltage at the CRT deflection plates is about +180 volts, which sets the total emitter current of Q495 and Q496 at 0.3 mA. When the two deflection plate voltages are equal, the two transistors share the 0.3 mA and both neons are lighted. If either deflection plate goes more positive than the other, the transistor on that side takes all the 0.3 mA and the other transistor cuts off. Each transistor has a $BV_{CBO}$ rating of 85 volts, so R497 prevents the turned off-transistor collector from going all the way to +300 volts. The dark neon has some voltage across it, but not enough to cause it to glow. D492 and D493 assure that the two transistor base voltages are never more than 0.6 volt apart.

## Gate Generators

The Gate Generators diagram contains circuits for the Blocking Oscillator, Dual-Trace Driver, both Delay and Strobe Drivers and both Memory Gate Drivers. The Blocking oscillator starts the sampling process when driven by the sampling sweep unit.

The Blocking Oscillator output drives the two Delay and Strobe Driver circuits, and the Dual-Trace Driver circuit. The Dual-Trace Driver circuit drives the Dual-Trace Multivibrator and CRT cathode circuit for interdot blanking of the display.

**The Blocking Oscillator** can be thought of as a risetime improving circuit. When driven by the sampling sweep unit drive pulse, Q503 always delivers a signal of the same amplitude and same risetime at its output. The stage is a simple amplifier until T503 builds up enough positive feedback for regeneration. After regeneration, the circuit ignores the drive pulse shape, amplitude and energy content. Q503 is normally biased to cutoff, causing the output signal to go from +15 volts to ground each time it is driven. D502 disconnects T503 backswing pulse from Q503 base and also makes certain T503 does not load the drive pulse.

**The Dual-Trace Driver** is a monostable multivibrator Neither transistor conducts until driven. —12 volts is applied through L516 to R515 and R518, placing Q515 at zero bias. Q522 is reverse biased by the junction drop of D520 and current in R520. Normally, neither transistor is conducting.

A negative drive pulse from the Blocking oscillator is coupled through R505, C505 and C513 to Q522 base. (D506 is reverse-biased 15 volts while Q515 is off, so it doesn't stop the drive pulse from reaching Q522.) Q522 turns on hard and D519-C519 couples the drive to Q515 base. Q515 turns on and applies more drive to Q522. D506 turns on and keeps Q515 from saturating. Thus a heavy regeneration causes a 50 volt output pulse to drive both the Dual-Trace Multi and the CRT blanking circuit. C513 charges very rapidly, but C511 does not. C511 holds base drive current applied to Q522 for a longer period. When C511 is charged, Q522 cuts off and its falling collector signal is AC coupled by C519 alone to Q515 base, turning it off. The turn-off is also regenerative, with D520 limiting the reverse bias on Q522 and helping to recharge C513 for the next cycle.

**The Delay and Strobe Driver and the Memory Gate Driver** circuits are unusual multivibrators. The A and B Channel circuits are identical except for R530, a power supply isolation resistor located between +15 volts and the B DELAY control. The Channel B circuit is explained below.

The complete circuit, from Blocking Oscillator output to the two pulse outputs, consists of: A two-diode comporator that compares a negative-going ramp with a fixed DC voltage variable by the Delay control; a very low-current amplifier that follows the Delay control voltage without affecting its output to the next stage; and a monostable multivibrator with two output terminals.

Quiescent circuit conditions are: Q538 base voltage rests between +15 and +11 volts, as set by the B DELAY control. Q538 current is limited to about 1 mA by R537 which leaves the collector clamped by D539 at —12.8 volts, assuring that there is no change in output voltage when the Delay control position is changed. Q541 is reverse biased 0.6 volt by D539, and Q555 is reverse biased 0.6 volt by current in D555, D552, R551 and the Memory Gate Width control. Q555 collector voltage is at —12.2 volts through T355.

As the Blocking Oscillator fires, R536-C536 form a negative-going ramp signal that soon causes D536 to conduct. When D536 conducts, the ramp turns on Q538. C537 contains enough charge for Q538 collector to clear D539 of carriers, and to forward bias Q541. As Q541 conducts, the negative signal is coupled through C541 and C543 back to Q538 base in a regenerative turn-on. The feedback signal also reverse

biases D534 and D536 so as not to disturb the other channel Delay circuit.

The —27 volt signal from Q541 collector drives Q555 through C547 and C548. C548 couples a fast turn-on pulse to Q555 while C547 signal current reverse biases D552, allowing R553 to keep Q555 turned on. Q555 collector signal is coupled through R549 back to Q541 base and holds Q541 in steady conduction. R557 applies a steady 40 mA current to the Memory Gate transformer primary (T355) for the pulse duration of about 180 ns.

C543 regenerative turn-on to Q538 does not last as long as Q555 turn-on to Q541, but since Q541 is saturated, Q538 is not disturbed. The duration of Q555 conduction is therefore controlled only by the position of the Memory Gate Width control which adjusts C547 charge rate. The smaller the resistance, the shorter the gate duration. As C547 charges toward +15 volts, D552 again conducts and turns Q555 off, stopping the Memory Gate pulse and the drive to Q541 base. However, Q541 was in saturation, so it does not stop conducting immediately. Q541 collector signal rises positive about 350 ns after it is driven negative. This RC rise is slow and does not couple much energy through either C541 or C543. Q541 total negative step is coupled by C541 as a Strobe Drive pulse to the sampling head.

The sampling drive pulse from the sampling sweep unit is slewed in time from the initial trigger event to each sample. An additional time positioning is accomplished in the two Delay (ramp comparator) circuits. The additional time slewing of the strobe drive pulses require an identical time slewing of the Memory Gate drive pulses in order to maintain proper processing of the error signals into the Memory Amplifier. This is accomplished since the Memory Gate Driver is driven by the Delay and Strobe Driver.

## Programmed Offset

The Programmed Offset diagrams for each channel include the Offset Current Selector, Offset Amplifier, Offset Inverter, Electronic Switch and Polarity Decoder circuits. The offset circuits provide a DC voltage which is combined with the signal feedback voltage in the sampling head and applied to the sampling bridge. The circuit operates in two modes; external, with the Vertical Mode switch in the EXT PROG position; and internal, with the Vertical Mode switch in any position other than the EXT PROG position.

In the external mode, the DC Offset voltage is externally programmed by external voltages or connections made to the proper pins at the rear program connector. The program operates the Offset Current Selector block and the Polarity Decoder block. The Offset Current Selector circuit provides a programmed current to the Offset Amplifier. This current causes the Offset Amplifier to produce an output voltage from 0 to +9.95 volts in 0.05 volt increments. The voltage is fed to the Offset Inverter (a ×1 inverting amplifier) and the Electronic Switch circuits. The Electronic Switch circuit, operated by the Polarity Decoder circuit, selects the positive (or the inverted negative) offset voltage which is coupled through J13 (rear panel) to the sampling head.

In the internal mode, the Offset Amplifier block provides an analog voltage output with a range of —10 to +10 volts as set by the DC OFFSET control. The Polarity Decoder circuit operates the Electronic Switch circuit (Q677 conducting) to couple the output voltage to the sampling head. The Offset Inverter circuit is not used in the internal mode. Also the Offset Current Selector is not programmable in this mode, but does supply input current to the Offset Amplifier.

When the DC OFFSET is front-panel controlled, the Vertical Mode switch connects emitter return resistors of Q602, Q610, Q616, Q620 and Q622 to ground. This reverse biases these transistors, since their bases are connected to decoupled +3.6 volts. With these transistors off, a current path is provided from the —50 V supply through each collector resistor and coupling diode to Q633A base. This supplies a total of 2 mA to the Offset Amplifier summing point at Q633A base.

**The Offset Current Selector** circuit supplies a programmed current in the external mode to the Offset Amplifier. Each of the nine current selector transistor circuits supplies a different amount of current. The output currents are added through diodes to the Offset Amplifier summing input at Q633A base. In the external mode, each transistor can be turned on or off by the external program.

The mV of Offset voltage controlled by each input line is labeled at the left of diagram 8. For further programming information see the Operating Instructions, Section 2.

In external program, the Offset Current Selector circuit operates as follows (since both Channels are the same, only Channel A is described):

1. +15 volts is connected by the Vertical Mode switch to the emitter return resistors of Q602, Q610, Q616, Q620 and Q622. +3.6 volts is connected to the bases of Q604, Q608, Q614 and Q626 through decoupling resistor R628. Each transistor collector is connected to the Offset Amplifier summing input through a diode. Each transistor circuit can provide current for the Offset Amplifier circuit, but only when externally programmed to do so.

2. (Using the Q626 circuit as an example). With a logical ONE at connector A of the logic card, D625 is forward biased by current in R625. This sets Q626 emitter at about +0.6 volt, cutting off Q626 (because its base voltage is at +3.6 volts). With Q626 off, R626 current forward biases D626. This applies the current into the Offset Amplifier summing input at Q633A base.

3. When connector A of the logic card is left on open circuit (logical ZERO), D625 cannot conduct R625 current. Instead, Q626 is forward biased and its collector takes all of the R626 current away from D626 and the Offset Amplifier input.

4. The other transistors in the Offset Current Selector circuit operate as just described for Q626, except that the output current path is from the —50 volt supply, and the current values are different due to different resistance values for the collector resistors. It is the sum of all currents out of the Offset Current Selector circuits that sets the final programmed DC OFFSET voltage. The accuracy of the current for the Offset Amplifier is affected by the collector resistors and the —50-volt supply voltage.

**Offset Amplifier.** The Offset Amplifier is a DC coupled inverting (operational) amplifier consisting of Q633, Q642 and Q645. Both the input and feedback components differ in internal operation as compared to external programming

of the DC OFFSET voltage. The input summing terminal is at the base of dual transistor Q633A. The output terminal is at the emitter of emitter follower Q645. Internal gain is very high due to large collector load resistors for both Q633B and Q642. The high gain assures that the variable current input is converted to a variable voltage output with very low output resistance.

Internal operation connects R648 and the Offset Zero control as one of the input elements to the amplifier, and the DC OFFSET control (R647) is a variable resistance feedback element.

Externally programmed control of the Offset output voltage connects various resistors of the Offset Current Selector circuits as the input elements, and R646 as the fixed resistance feedback element.

Output voltage swing is from —10 to +10 volts when internally controlled, and from 0 V to +9.95 V when externally programmed. The two different voltage ranges require that the high gain input comparator amplifier, Q633, operate at different reference voltages for the two modes of operation. The reference voltage is applied to the base of Q633B, and is —10 V for internal operation, and ground for externally programmed operation. The large emitter return voltage, —100 V, prevents the stage static current from changing very much between the two conditions.

Internal operation produces an output voltage as a function of Ohm's law. The voltage varies based upon the fixed 2 mA input and feedback current and the resistance value of the variable DC OFFSET control R647. Assume R647 is zero ohms (fully clockwise at Black scale = —10 V Offset). Whatever the current value through R647, zero ohms causes zero volts difference between the amplifier summing input and the output at Q645 emitter. Since Q633B base is at —10 V, the output is also at —10 V. Turning the DC OFFSET control so it introduces resistance in the feedback path causes the output voltage to change in a positive direction. By the time the control is fully counterclockwise, the feedback current and the resistance cause the output at Q645 emitter to be at +10 V.

Externally programmed operation uses a fixed feedback resistor and different amounts of input current as selected by the Offset Current Selector circuits and the external program. R646 is the fixed feedback resistor, and even through the front panel DC OFFSET control is not completely disconnected, its current load on the output does not alter the output voltage as controlled by the feedback amplifier. The reference voltage for external control at Q633B base is ground. With all the input resistors connected to a negative voltage, it is not possible to program an output voltage that passes through zero and changes polarity. Thus, the Offset Inverter ×1 gain amplifier is used when a negative Offset output voltage is required. Protection diodes are D634, D641, D643 and D645.

C647 connected across the DC OFFSET control minimized the effect of wiper contact noise on the output voltage when the control setting is changed. C634 prevents AC pickup in the Vertical Mode switch lead by providing low impedance to any AC signals at Q633B base.

**The Offset Inverter Amplifier** is a temperature-compensated DC coupled amplifier with a gain of 1. Feedback resistor R660 and input resistor R650, both 0.1% tolerance resistors, set the gain. Q653 dual-transistor is an emitter-coupled stage providing both temperature compensation and high internal gain. Q658 operates as an inverting amplifier feeding Q660 emitter follower output circuit.

Any input voltage other than zero causes a current in the input resistor R650. Any change in Q653A base voltage changes Q653B collector voltage to Q658 base in the same direction. Q658 amplifies and inverts the signal, applying it to Q660 emitter follower. Q660 voltage output produces an equal and opposite current to Q653A base, making the output voltage equal and opposite to the amplifier input voltage.

Two diodes provide protection when transistors are removed from their sockets. D658 conducts when Q658 is removed. D657 conducts when Q653 is removed. R657 and C657 comprise a decoupling network in Q658 emitter circuit.

**The Electronic Switch** circuit operates during external programming as a single pole double throw switch consisting of field effect transistors Q663 and Q677. One transistor is on while the other is off as set by the Polarity Decoder circuit. The transistor drain leads are connected together (TP663) to provide whichever polarity output voltage is desired by the external program. When Q677 is on, it connects the Offset Amplifier output voltage (0 to +10 V) to the output circuits. When Q633 is on, it connects the Inverter Amplifier output voltage (0 to —10 V) to the output circuits. Conduction of either transistor is set by the Polarity Decoder circuit. R678 connected at TP663 is not used, but is in the circuit to make the Offset card usable in a Type 3S5.

**The Polarity Decoder** circuit operates the two transistors Q663 and Q677 in the Electronic Switch circuit, turning one transistor on while holding the other off.

The circuit holds Q677 on (exclusively) during internal operation. Q670, Q673 and Q675 are the decoder transistors. An external program that places a logical ONE at the front panel connector J15 pin 4 will cause the Decoder circuit to turn Q663 off and Q677 on. See the Operating Instructions for programming this circuit through the rear panel connector.

An external program of a logical ONE to the Decoder input causes D667 to conduct R667 current. Then R668 and R669 forward bias Q70 into saturation. R670 turns Q673 on to saturation, placing Q663 gate lead at about —25 V and assuring that it remains cut off. Q673 collector voltage also reverse biases Q675, causing R675 to reverse bias D676 and set Q677 gate lead at zero bias, turning Q677 on. D675 in Q675 emitter circuit provides an equal junction drop to that of D674, assuring that Q675 can be placed at cutoff when the external program is a logical ONE.

An external program of a logical ZERO to the Decoder input reverses the conditions, causing Q663 to conduct and Q677 to be at cut off. At that time, D674 reverse biases, and prevents Q673 high collector voltage from overdriving Q675 base circuit.

## Power Supplies

The Power Supply diagram contains the internal power supplies power connections from the indicator oscilloscope and power connections to J13 (rear connector) for the sampling heads. Power from the indicator oscilloscope enters through P11 at the left edge of the diagram. P11 and J13 also show pin connections to other circuits within the Type 3S6.

Internal power supplies obtain power from the indicator oscilloscope at 6.3 VAC and from the —12.2-volt, +125-volt, and —100-volt supplies. The 6.3 VAC is fed to T950 primary. T950 secondary windings feed the +15 and +3.6 volt supplies.

**The +15-volt Supply** is fed from T950 secondary winding at terminals 5, 6 and 7. The secondary voltage of approximately 52 VAC is rectified by D951-D953, filtered by C950, and regulated by D955, Q957, Q959, Q966 and Q969. The regulator circuit is of the series type, with Q969 the series pass (variable resistance) transistor. Q957 and Q959 form a temperature compensated comparator circuit, and Q966 inverts and amplifies the comparator output which controls Q969. The output voltage is compared with the reference Zener diode D955. Assume a positive change in the output voltage. The correcting action that follows causes Q969 series resistance to increase, restoring the output voltage to its correct value. The positive change at the output is directly coupled to Q957 base, and attenuator-coupled to Q959 base. Q959 emitter is driven by Q957 emitter and follows the change all the way. Q959 base does not follow the change 100%, and therefore the transistor receives a forward bias signal. Q959 increases its current, and applies a positive signal to Q966 base, causing Q966 to reduce its collector current. Current reduction in Q966 causes Q969 base and emitter to go more negative. Or more properly stated, Q969 increases the voltage across it, restoring the output to its proper value.

If the +15 volt supply is accidentally shorted to ground, excessive current through R951 and R953 will cause these resistors to overheat and open up, protecting Q969 and rectifiers, and the transformer.

**The —50-Volt Supply** consists of the comparator, Q901-Q907 and shunt regulator Q903. (The —50 volt supply is one of two voltage references for the +50 V supply.)

The circuit changes the resistance of Q903 to take more current when the load current reduces, and to take less current when the load current increases. D905 protects Q903 from damage in the event the output is shorted to a voltage more positive than —12.2 volts.

Comparator transistors Q901-Q907 compare a voltage near ground at the junction of R908-R909 with zero volts at ground. If the output load current increases (output voltage goes positive), Q907 base and emitter follow the change. Q907 emitter drives Q901 emitter positively, which is an increase in forward bias and turns Q901 on harder. Q901 collector voltage change decreases Q903 turn-on bias increasing Q903 resistance and permitting a negative return in voltage at the supply output.

**The +50-volt Supply** uses one transistor as an emitter follower and the other transistor as both a comparator and as the shunt regulating element. R917-R918 presents a voltage near +15 volts to the base of emitter follower Q911. Q911 provides current gain to the signal and applies it to the base of comparator-regulator transistor Q915.

If the output load current increases (voltage goes negative), Q911 emitter takes Q915 base negative, reducing Q915 current. As Q915 current reduces, the output voltage rises back to its proper value.

A short circuit that places the +50-volt line less positive than +15 volts will reverse-bias D915 and protect Q915 from damage. The large resistance value of R917 and R918 protects Q911 from damage. A short circuit on the +50-volt line will cause the +50-volt output to be a few volts low. Again, no transistors will be damaged.

**The +3.6-volt Supply** is fed from T950 secondary connections 3 and 4. The secondary voltage of approximately 6.7 VAC is rectified by the bridge rectifier D930A-B-C-D, filtered by C931 and fed to the output through Q938. Q936 emitter follower controls Q938. R933 and R934 set Q936 base at +3.6 volts. Through equal and opposite base-emitter junction drops of Q936 and Q938, the output voltage is +3.6 volts. The circuit transforms the input impedance at Q936 base to less than one ohm at Q938 emitter, so load changes do not significantly affect the output voltage.

**The —25-Volt Supply** is fed from the —100-volt Supply from the indicator oscilloscope through R946 and Q944 emitter follower. R941 and R942 set Q944 base at about —25.6 V, which provides a low impedance —25 volts output at Q944 emitter. R946 limits the current from the —100-volt supply and limits power dissipation in Q944.

## Card Connectors and Decoupling Networks

The Card Connectors and Decoupling Networks diagram contains the Offset and Logic Card connectors, and the power supply decoupling networks on the Output and Vertical boards.

The Offset card connector J600 and the Logic Card connector J800 show the signal contained at each pin, and the number of the schematic where it can be found.

Decoupling networks are drawn within outlined areas that represent particular diagrams already described.

## Vertical Mode Switch and Program Connectors

The Vertical Mode Switch and Program Connectors diagram contains information on the Vertical Mode Switch, the rear external program connectors and the digital readout connector.

All of the Vertical Mode Switch connections are shown with references to the other schematic diagrams where sections of the switch are shown. Each section or wafer of the switches is coded to indicate its position in the switch assembly. The numbered portion of the code refers to the wafer number counting from the front (the mounting end of the switch) toward the rear. The letters F and R indicate whether the front or rear of the wafer performs the particular switching function.

When the Vertical Mode switch is in the EXT PROG position, the front panel EXTERNAL PROGRAM light, B999 is lighted. B999 is then connected to —12.2-Volt supply and ground through R999.

# SECTION 5
# DIGITAL UNIT CONTROL DESCRIPTION

**Change information, if any, affecting this section will be found at the rear of the manual.**

## General Definition

This section of the manual describes the circuits and logic of the Type 3S6 Digital Unit Control diagram. A logic diagram titled Digital Unit Control Logic is included at the back of the manual following the Digital Unit Control diagram.

The Digital Unit Control circuits operate exclusively to program the readout logic circuits of a Tektronix Type 230 Digital Unit. The Type 3S6 controls the digital unit only when it is programmed by the digital unit. The type of units (either volts or amperes) programmed into the digital unit is controlled by the type of sampling head operated with the Type 3S6.

Description of the Digital Unit Control circuits is separate from the description of other Type 3S6 circuits. This is because the Digital Unit Control circuits do not contribute to the Type 3S6 operation. Only the Type 230 Digital Unit uses the Digital Unit Control outputs. All outputs pass out the rear of the Type 3S6, through P12, through the Type 568 ocilloscope, and into the associated digital unit.

Three types of signal sources control the circuit functions: (1) the deflection factor selected by either the front panel Units/Div switch or an external program, (2) the sampling head units (Volts or Amps) and its units decade (multiplier: X0.1, X1 or X10) and (3) the digital unit amplitude measurement program. If the digital unit is programmed to make a time measurement, all of the Digital Unit Control outputs are inhibited. If the digital unit is programmed to make an amplitude measurement, the Digital Unit Control circuits function as instructed by the other two sources.

NOTE

**Both the Digital Unit Control circuit diagram and its Digital Unit Control diagram include logic symbols. Logic symbols used are based on the ASA Y32.14-1962 Standards, and are drawn using negative logic symbols only.**

Three types of outputs control the digital unit: (1) the type of units, Volts or Amps, (2) the readout number decimal point, including an "M" for mV or mA and (3) the digital unit counter circuit divide command (see the digital unit instruction manual for use of the counter divide outputs).

All input and output lines are considered to be a logical ONE when grounded, and a logical ZERO when left open circuit. (Grounding is accomplished in both cases by saturating transistors in the digital unit, saturating transistors at the Digital Unit Control output leads, and by solid ground connections by the Units/Div switches.)

## Block Diagram

The main Block diagram includes the Digital Unit Control blocks at the lower left corner. Each block name agrees with areas outlined on both the Digital Unit Control diagram and the Digital Unit Control Logic diagram. The general layout of all blocks on all three diagrams is the same, with input lines at the left and output lines at the right.

Comparing the block diagram to the Digital Unit Control Logic diagram during the following block description may prove useful in understanding the Digital Unit Control circuits.

The eight blocks of the Digital Unit Control circuits show that the input lines from both CH A and CH B are always connected, but that only one set of output lines drives the digital unit circuits. Two pairs of channel selection lines from the digital unit tell the Digital Unit Control circuits which channel is being used. One pair carries the channel selection instructions for the decimal and units output, and the other pair carries the channel selection instructions for the digital unit counter divide output. When the digital unit is programmed to make an amplitude measurement, one of each pair of channel select lines is grounded. If the measurement is being made on Channel A, the three input sources from Channel B are inhibited by the digital unit grounding the "A D, U, GND" and "A ÷ GND" lines. When the digital unit is programmed to make a time measurement, none of the channel select lines is grounded, and all outputs are inhibited.

NOTE

**This description does not indicate the point from which digital unit programming originates. The circuits in the Type 3S6 operate the same whether the digital unit is externally programmed or controlled from its own front panel. However, externally programming the Type 3S6 does make the plug-in's circuits operate in a slightly different manner than controlling it from the Type 3S6 front panel. Front panel control of the Type 3S6 permits the VARIABLE control CAL switches to inhibit the decimal and units section of the Digital Unit Control circuits; externally programming the Type 3S6 causes both the VARIABLE control and its CAL switch to be removed from operation, so that turning the control will neither affect the CRT deflection factor, nor inhibit the decimal and units outputs.**

Input lines from the Units/Div switches are labeled A1, A2 and A4, and B1, B2 and B4. The Units/Div lines are grounded according to Truth Table 5-1. The 1's digit and the 2's digit lines go to both the 200 UNITS/DIV DECODER block and the COUNTER DIVIDE CONTROL block. The 4's digit lines go to only the 10, 5, 2 UNITS/DIV DECODER block. Output from the 200 UNITS/DIV DECODER block is a logical ONE only when 200 Units/Div is programmed. Output from the 10, 5, 2 UNITS/DIV DECODER block is a logical ONE only when the 10, 5 and 2 Units/Div deflection factor is programmed. Outputs from the COUNTER DIVIDE

CONTROL block are logical ONE according to Table 5-1; only one output line is a logical ONE at any particular time and the other two lines are then a logical ZERO.

**TABLE 5-1**

Units/Div Truth Table

| Units/ Div | A4 B4 | A2 B2 | A1 B1 | ÷[1] |
|---|---|---|---|---|
| 200 | 0 | 0 | 0 | 5 |
| 100 | 0 | 0 | 1 | 1 |
| 50 | 0 | 1 | 0 | 2 |
| 20 | 0 | 1 | 1 | 5 |
| 10 | 1 | 0 | 1 | 1 |
| 5 | 1 | 1 | 0 | 2 |
| 2 | 1 | 1 | 1 | 5 |

[1] ÷ = **Output line at Logical 1.**

NOTE

**Logical 1 means the line is grounded, Logical 0 means an open circuit; not grounded.**

Two other input line pairs (to the Digital Unit Control circuits) come from the sampling heads. One pair, to the UNITS CONTROL block gives instructions to the digital unit to indicate that the readout units are either Volts or Amperes. The other pair, to the UNITS/DIV MULTIPLIER DECODE block gives instructions regarding the sampling head deflection factor in relation to the Type 3S6 Units/Div control. The sampling head may require that the numbers around the Units/Div switch be multiplied by X0.1, X1 or X10, indicating the need for a decimal shift in the digital unit readout. The Units/Div multiplier instructions are ternary (three levels) rather than binary (two levels) as are all the other instructions given.

Both the UNITS CONTROL and the UNITS/DIV MULITPLIER DECODER blocks receive information from both Channel A and Channel B. These blocks use the Channel Select lines from the digital unit to inhibit information from the channel not in use.

Included in the UNITS/DIV MULTIPLIER DECODER block is a Ternary to Binary decoder that converts one-line ternary information to three-line binary information at the lines labeled X0.1, X1 and X10.

Outputs from all four of the Units/Div Decoder blocks feed the DECIMAL CONTROL block. The DECIMAL CONTROL block decodes both the Units/Div number programmed and the sampling head Units/Div multiplier to operate the digital unit decimal neons and the "milli" readout lamp. The M lamp control line is part of the Decimal Control block because lighting the M (for "milli") affects the location of the readout decimal.

## Logic Voltages

Negative logic is used throughout this manual to describe the operation of the Type 3S6 circuits. By the standards of negative logic, a TRUE state, or logical ONE (1) exists at a lead which is at or very near ground. A FALSE state or logical ZERO (0) is present at a lead which is either open-circuit or more positive with respect to ground. External control line voltage limits are stated in Section 1, Specification, to be logical ONE (TRUE) 0 V to +2 V; logical ZERO (FALSE) +6 V to +15 V, or open circuit. Externally controlled logic lines can be operated either by saturating transistors that do not completely ground the line, or by using cut off transistors that exhibit some $I_{CBO}$ leakage and do not really leave the line open.

Voltage levels of logic states produced within the Type 3S6 are different than the voltage levels of logical ONES or ZEROS in externally controlled logic. This results because the principal voltage supply for integrated circuits in the Type 3S6 is 3.6 volts rather than 15 volts.

Output voltage limits for a logical ONE or ZERO may also vary because those limits are set by the digital unit in use. However, it can be noted that a logical ONE is always accomplished by a saturated transistor.

Internal logic voltages that relate to the integrated circuits are stated at the bottom of Fig. 5-1. Other voltage values, such as the ternary voltages out of the Units/Div Multiplier Decoder are given later on in this section.

Logic states throughout the Digital Unit Control Logic diagram (without giving the voltage values) are included in the four truth Tables 5-2, 5-3, 5-4 and 5-5. The first three truth tables give the output logic states of all significant gates for three conditions of a sampling head Units/Div multiplier, X0.1, X1 and X10. The truth tables are of primary value when searching for a failure.

Control settings for using the first three truth tables are: the digital unit operating to make a Channel A amplitude measurement; the sampling head multiplier as stated at the top of the Table; the Units/Div as stated at the left of the Table; and if not externally programming the Type 3S6, the Units/Div VARIABLE control at CAL. The tables also apply to Channel B if all controls are properly set for an amplitude measurement on Channel B.

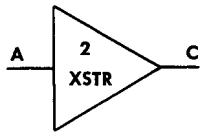
Table 5-5 applies to the circuits of the Counter Divide Control block, and is altered only by the Units/Div switch(es). If not externally programming the Type 3S6, the Units/Div VARIABLE control must be at CAL.

## Digital Unit Control Logic Diagram

Fig. 5-1 is a key to the logic symbols used in the Digital Unit Control Logic Diagram. If you are not experienced with logic symbols, it is recommended that this area on the Logic Diagram be read after reading the circuit description later in this section.

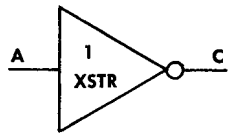
Symbols in the lower portions of Tables 5-2, 5-3, 5-4 and 5-5 differ slightly from the symbols on the Logic Diagram. Specifically, the column headed "M Q806" has a 3 input NAND gate symbol with a logic negation at one input. This symbol is equivalent to a group of symbols on the Logic Diagram; U805B inverter; R804, R805 and R806 3 input AND gate; and the (non-inhibited) 2 input NOR gate Q806, D806. The logical ONE in this column indicates that Q806 is saturated and the digital unit M lamp will be lighted. A second symbol difference includes the logic symbols leading to and including the DEC 3 column. Q839 is shown in a manner that ignores D839. This is justified by the fact htat there will be an output only when the last gate is not inhibited. The truth tables, and the symbols used, do not apply when the digital unit inhibits the outputs.

ANALOG CIRCUIT BLOCK




NON-INVERT (HI TO LO Z)

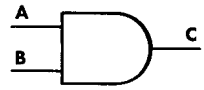
| A = C | |
|---|---|
| 1 | 1 |
| 0 | 0 |




INVERTER

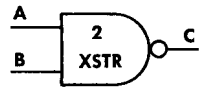
| A ≠ C | |
|---|---|
| 1 | 0 |
| 0 | 1 |

TRUTH TABLES IN THIS FIGURE ARE ALL BASED UPON NEGATIVE LOGIC:
1 = 0 V; 0 = +VOLTS
(LOW) (HIGH)




2 INPUT AND GATE

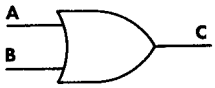
| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |




2 INPUT NAND GATE

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

2 DIODES




OR GATE (NON-INVERT)

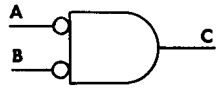
| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

2 TRANSISTORS


NOR GATE (INVERTER)

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

1 DIODE 1 TRANSISTOR

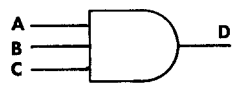



Inverted Input AND GATE

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

INHIBIT

3 DIODES OR 3 RESISTORS

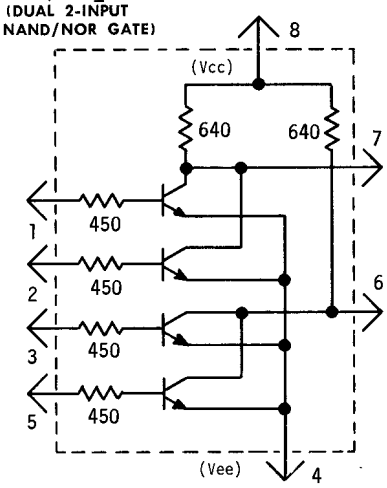


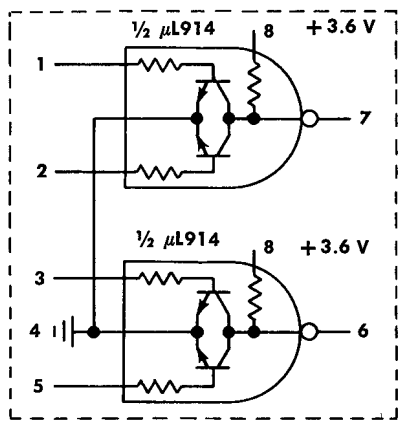

3 INPUT AND GATE

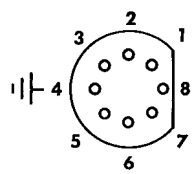
| A | B | C | D |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

INTEGRATED CKT DETAILS

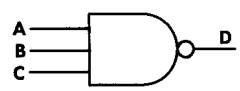
TYPE $\mu$L914[1] (DUAL 2-INPUT NAND/NOR GATE)




μL914 SOCKET TOP VIEW




3 INPUT NAND GATE

| A | B | C | D |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

[1]Data furnished courtesy of Fairchild Camera and Instrument Corporation.

**IC INPUT VOLTAGES**
LOGICAL 1 = 0 V TO +0.2 V.
LOGICAL 0 = +1 V TO +1.3 V.

**IC OUTPUT VOLTAGES**
LOGICAL 1 = 0 V TO +0.2 V.
LOGICAL 0 = +2.8 V TO +3.5 V.

A small circle ○ = a logic negation, not always an inverter.

Fig. 5-1. Digital Unit Control Logic diagram symbols and truth tables.

TABLE 5-2

Decimal & M Output Logic States When Units/Div Multiplier = X0.1

| Units/ Div | Input Logic A4 B4 | A2 B2 | A1 B1 | Q814 Coll | Q826 Coll | Q816 Q828 | Ternary Decoder X10 | X1 | X0.1 | U805A | U834A | U834B | U835A | U835B | U833A | U833B | U838B | M Q806 | DEC4 Q836 | DEC5 Q843 | D833 D834 D835 | D840 D841 D842 | U838A | DEC3 Q839 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 200 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 100 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 50 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 20 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 10 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 5 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

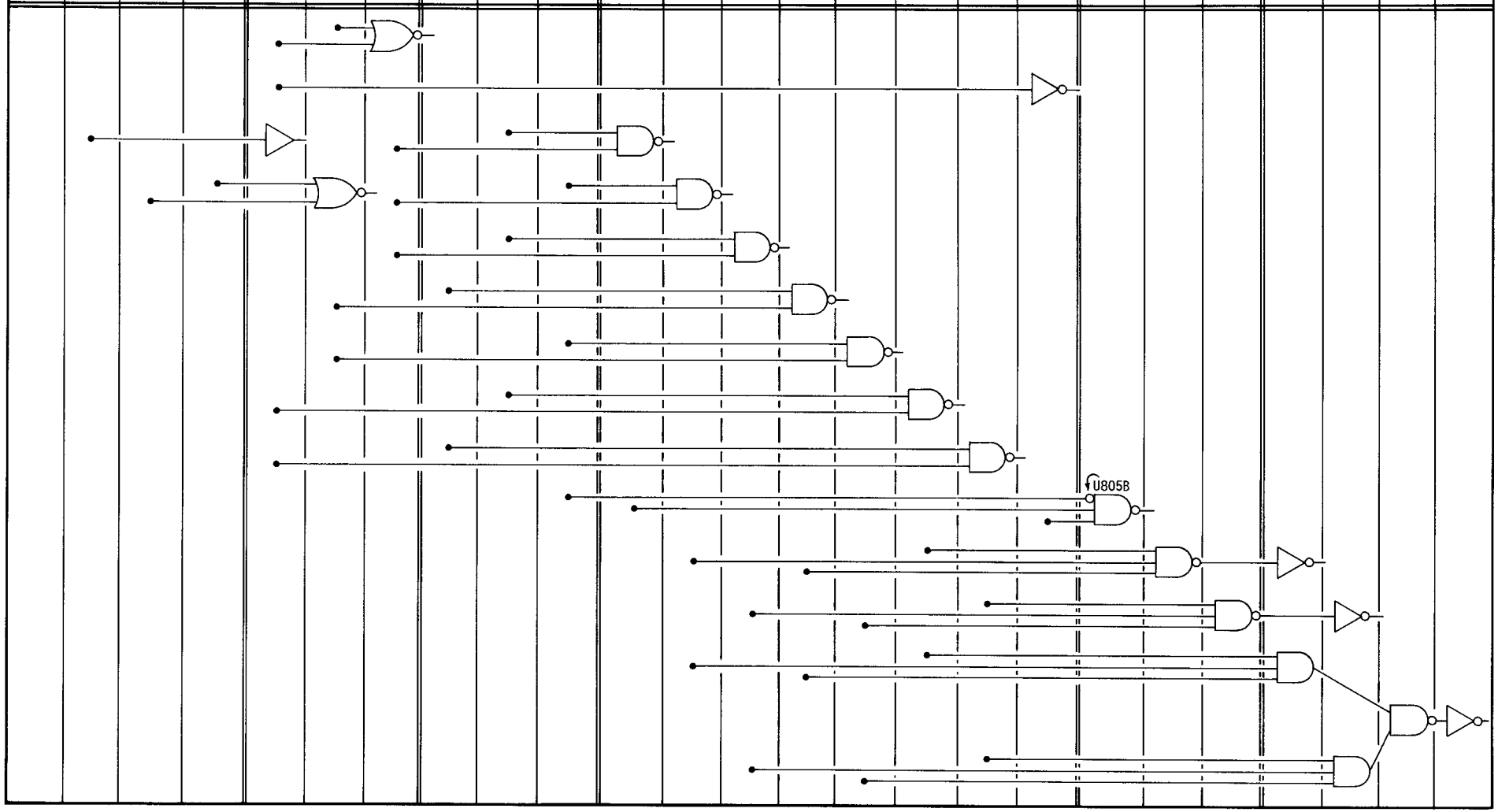


TABLE 5-3

Decimal & M Output Logic States When Units/Div Multiplier = X1

| Units/ Div | Input Logic A4 B4 | A2 B2 | A1 B1 | Q814 Coll | Q826 Coll | Q816 Q828 | Ternary Decoder X10 | X1 | X0.1 | U805A | U834A | U834B | U835A | U835B | U833A | U833B | U838B | M Q806 | DEC4 Q836 | DEC5 Q843 | D833 D834 D835 | D840 D841 D842 | U838A | DEC3 Q839 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 200 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 100 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 50 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 20 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 10 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 5 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

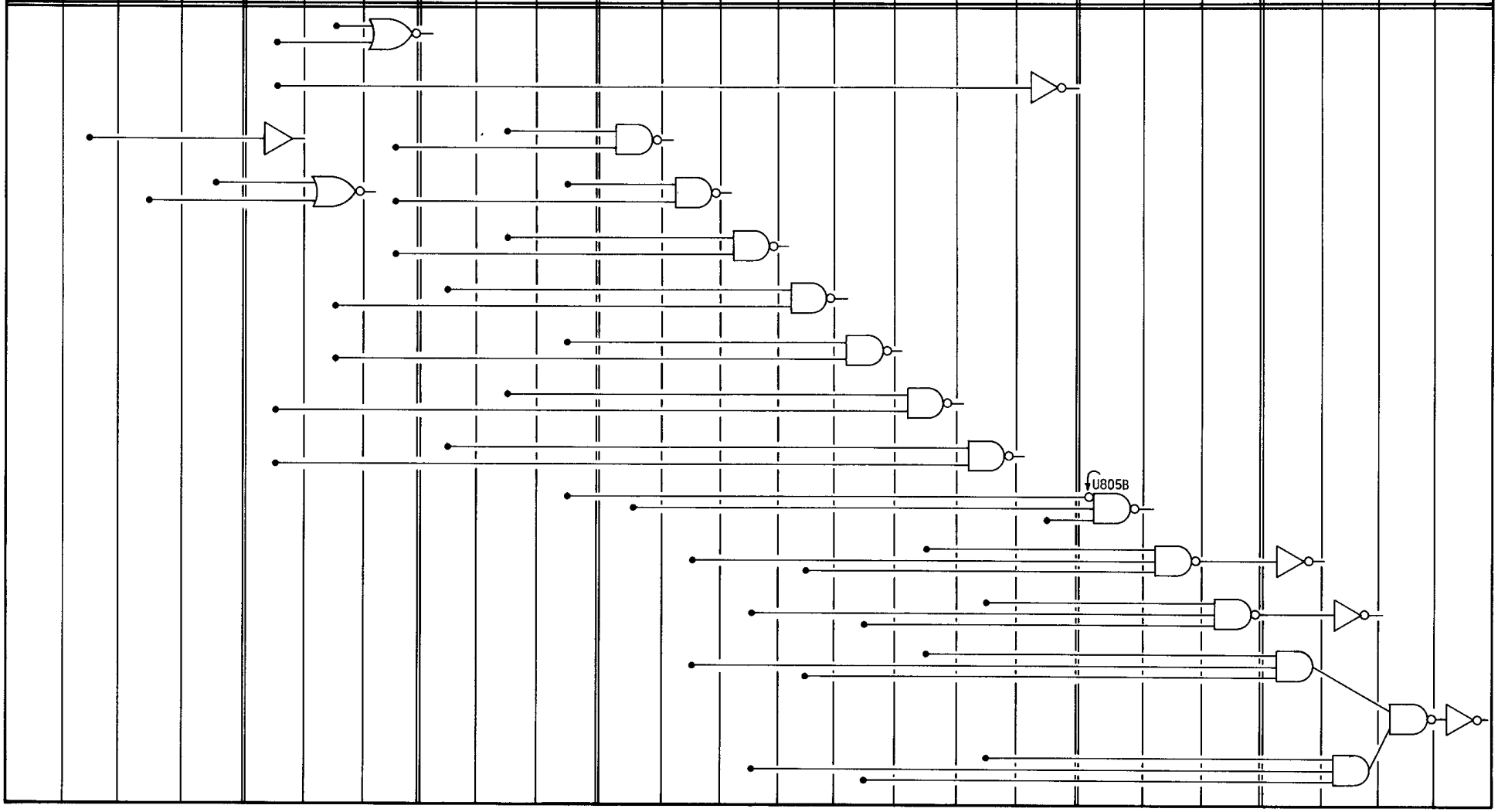
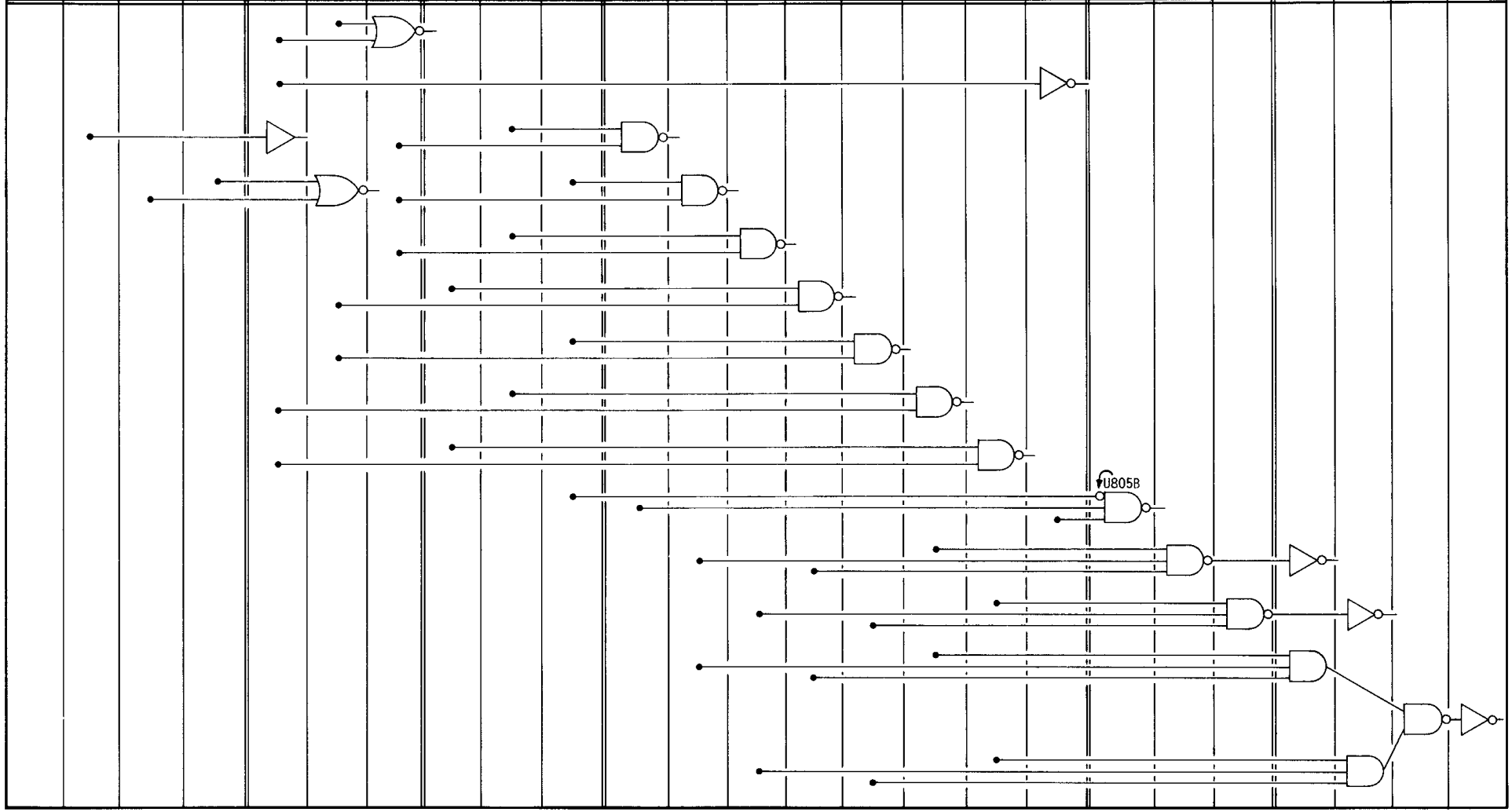


TABLE 5-4

Decimal & M Output Logic States When Units/Div Multiplier = X10

| Units/ Div | Input Logic A4 B4 | A2 B2 | A1 B1 | Q814 Col1 | Q826 Col1 | Q816 Q828 | Ternary Decoder X10 | X1 | X0.1 | U805A | U834A | U834B | U835A | U835B | U833A | U833B | U838B | M Q806 | DEC4 Q836 | DEC5 Q843 | D833 D834 D835 | D840 D841 D842 | U838A | DEC3 Q839 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 200 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 100 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 50 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 20 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 10 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 5 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 2 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |



All symbols used in this manual are negative logic symbols, regardless of the "active" state of the input or output lines. This applies even to the logic symbols on the circuit diagram. Thus, the function of any gate can be defined independently of the circuit's intended function, and all symbols on the circuit diagram or Logic diagram have truth tables found in Fig. 5-1.

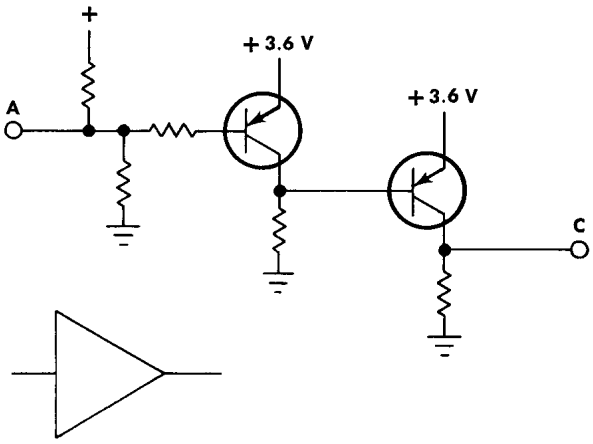
Abbreviations on the Logic Diagram include D for Decimal; U signifying Unit; GND, ground; A, Not A; and CH, channel.

## Basic Logic Symbols

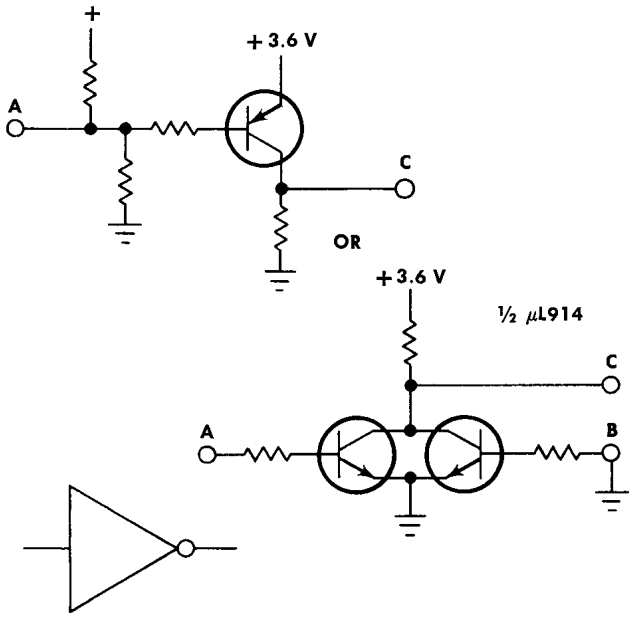
The logic symbols used in the Type 3S6 are presented in diagram form below. The sequence relates to Fig. 5-1 in a right-to-left and top-to-bottom sequence.

### 1 Input, 1 Output Non-Inverter

(High Z to Low Z, or voltage changing)

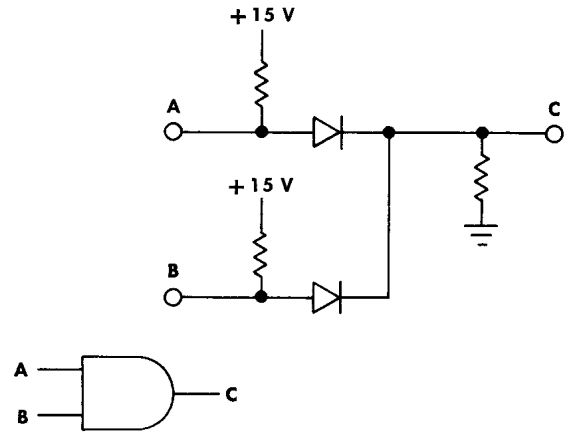



### 1 Input, 1 Output Inverter



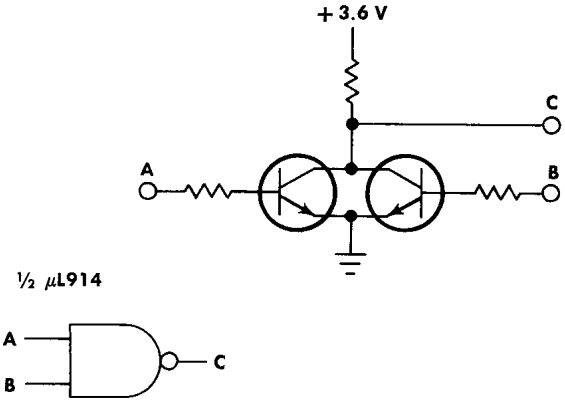

### 2 Input AND Gate

Both input leads must be grounded for the output to be at a logical 1.



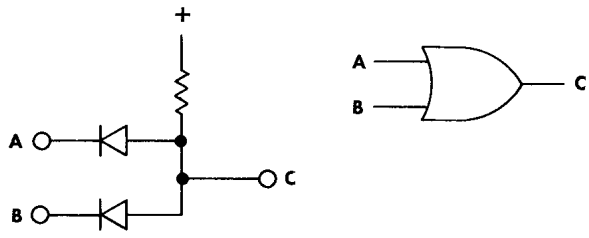

### 2 Input NAND Gate

If either input is pulled up to a logical ZERO, the output will be at a logical ONE. Both inputs must be at ONE for the output to be at ZERO.




### 2 Diode OR Gate

Either input at ONE makes the output at ONE.




### 2 Transistor NOR Gate (Inverting)

Neither input at ONE; output is at ONE.

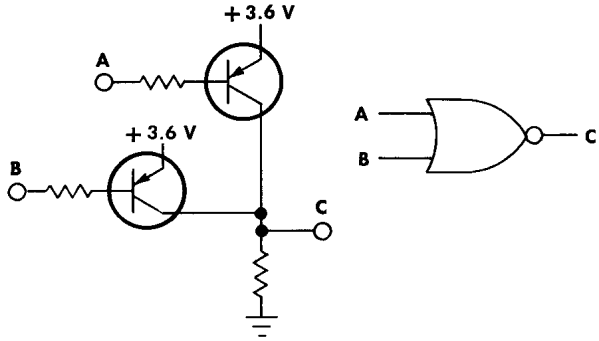
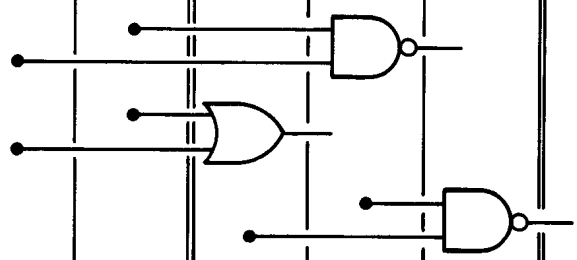


TABLE 5-5

Digital ÷ GND Output Logic States

| Units/ Div | INPUT A2 | LOGIC A1 | Q884 Coll | Q874 Coll | D886 D885 | U887A | U887B | Q891 Coll | Q892 Coll | Q893 Coll | ÷ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 200 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 5 |
| 100 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 50 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 2 |
| 20 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 5 |
| 10 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 5 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 2 |
| 2 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 5 |



Q899 Out = 0

## NOTES

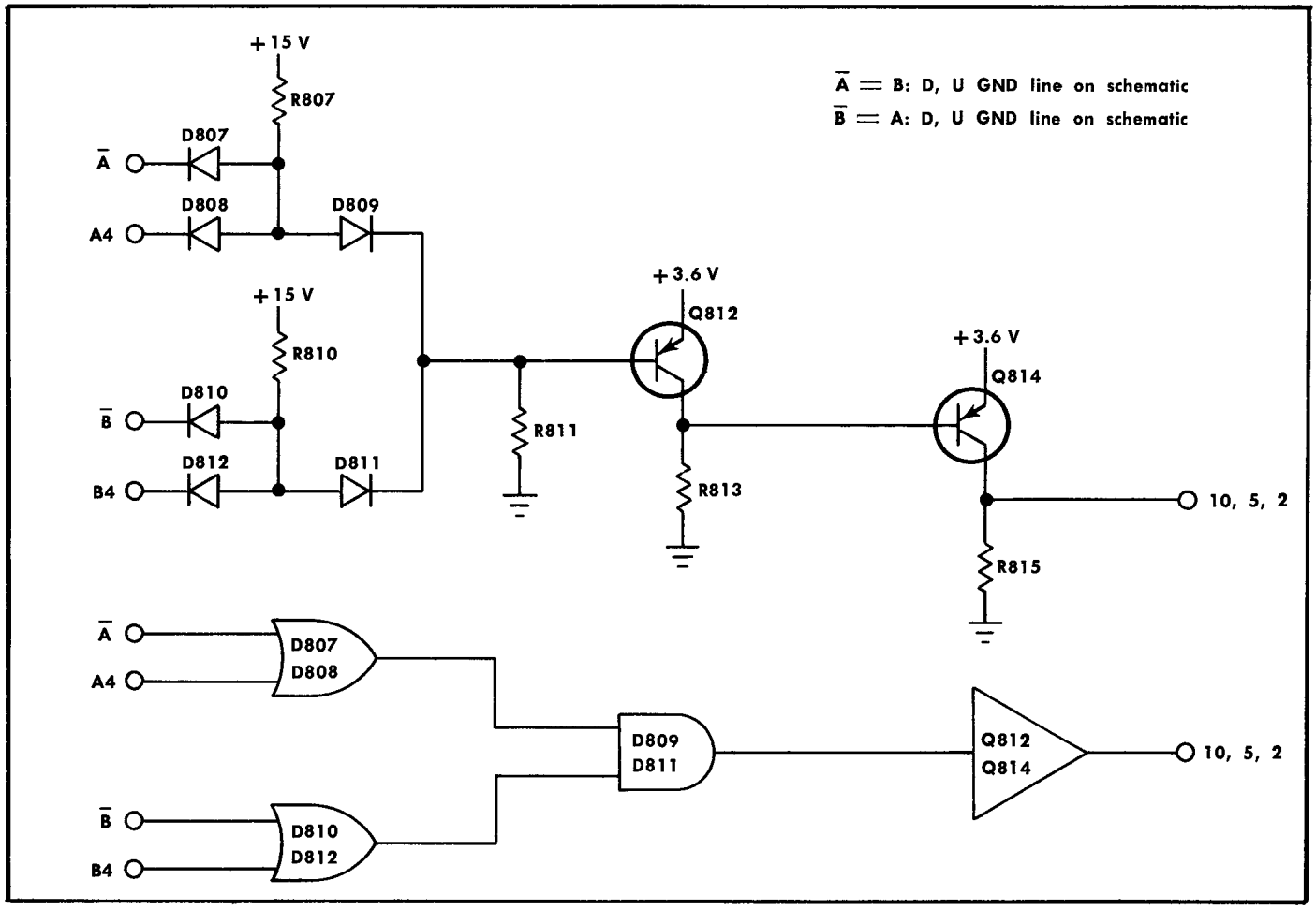
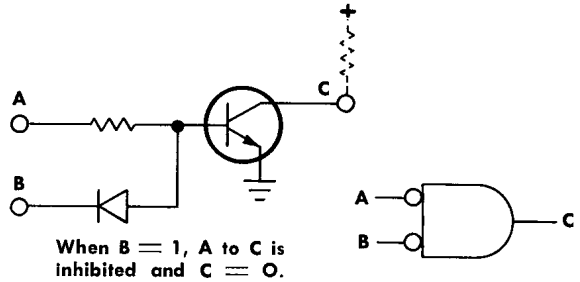


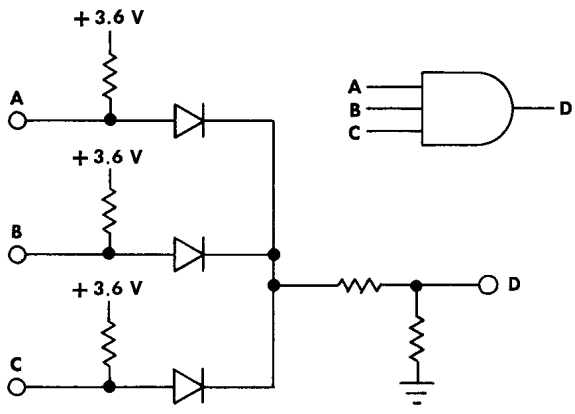

Fig. 5-2. Circuit and Logic diagrams of the 10, 5, 2 UNITS/DIV DECODER block.

### 1 Diode, 1 Transistor Inverted Input AND Gate



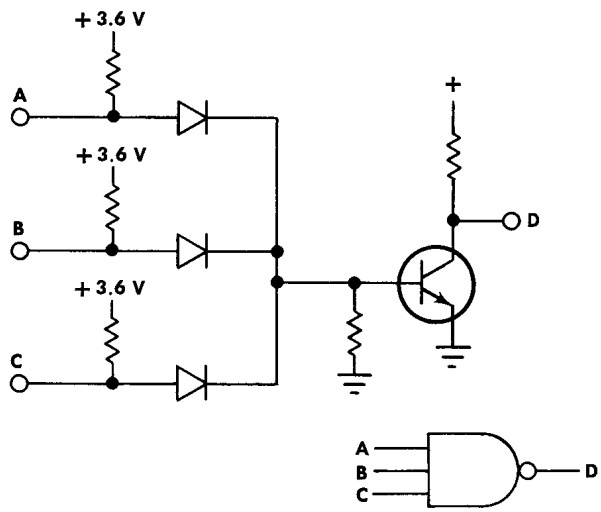

### 3 Input AND Gate

If all three inputs are at ONE, the output will be at ONE.




### 3 Input NAND Gate

The above gate with an inverter before terminal D. Only if all three inputs are at ONE, will the output be at ZERO.




## CIRCUIT DESCRIPTION

One block from the Digital Unit Control portion of the complete Block Diagram is drawn in detailed schematic and basic logic form in Fig. 5-2. Fig. 5-2 should be useful

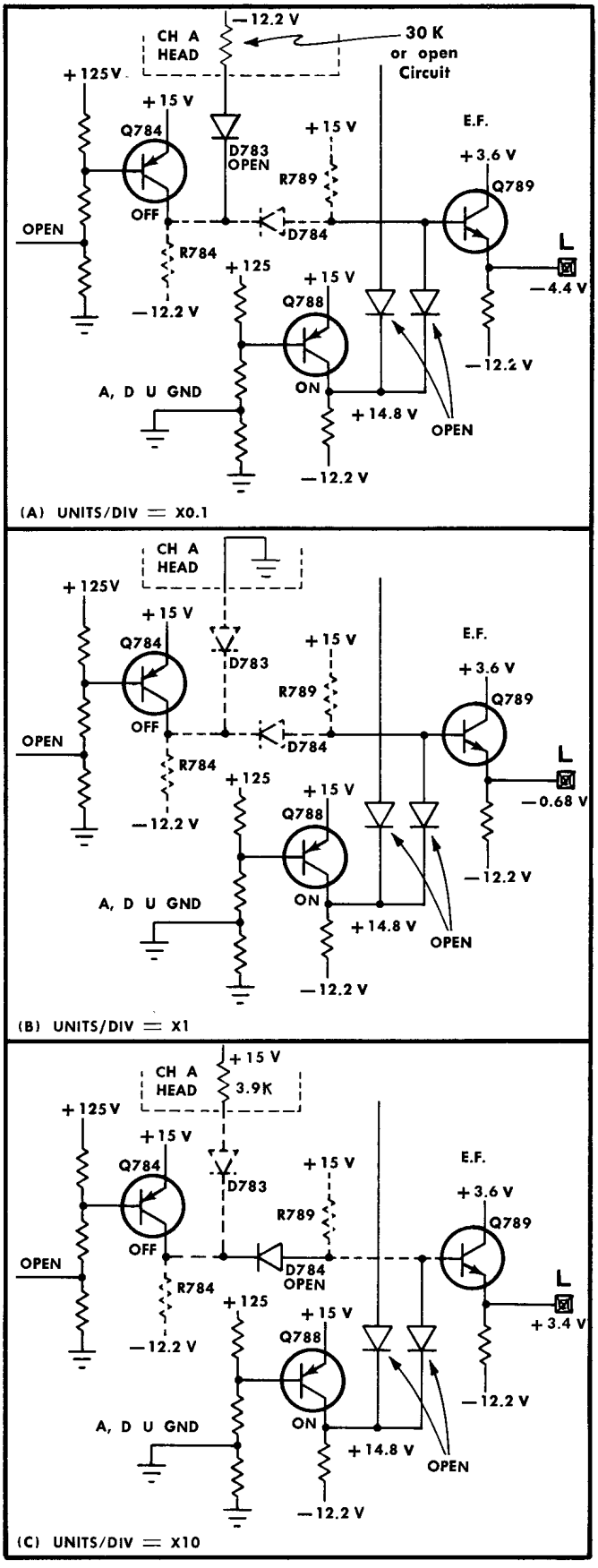



Fig. 5-3. Units/Div Multiplier Decoder circuit showing the ternary voltages for ×0.1, ×1 and ×10 Units/Div multipliers of the sampling head.

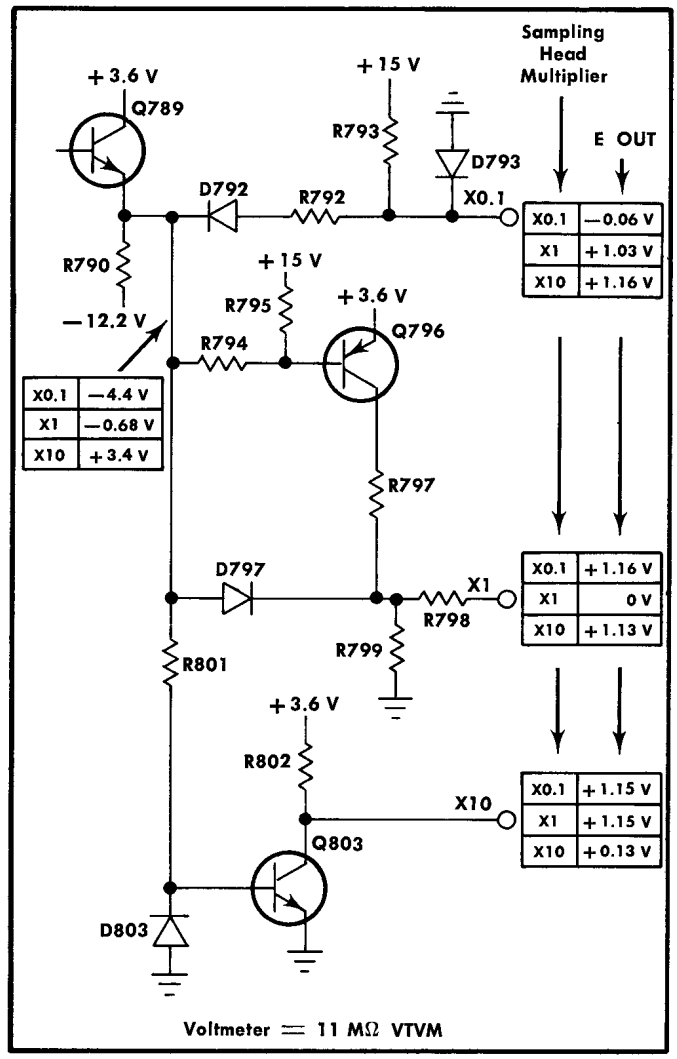



Fig. 5-4. Ternary to Binary Decoder circuit voltages.

in understanding the relationship between formal block diagram, circuit diagram and logic diagram. The block shown in Fig. 5-2 is the 10, 5, 2 UNITS/DIV DECODER.

To program the 10, 5, 2 UNITS/DIV Decoder circuit for a Channel A measurement, B is grounded. (B is the line labeled on the schematic diagram as A: D, U, GND.) At the same time, the A (not A = B: D, U, GND) line must be at a logical ZERO. This leaves only one line into the decoder circuit, the A4 line, which can affect the output at Q814 collector.

If A4 is a logical ZERO, R807 reverse-biases Q812. Q812 at cutoff lets R813 apply forward bias to Q814, saturating Q814. The circuit output is then a logical ZERO in agreement with the logical ZERO at the A4 input. This operation then agrees with the statement earlier in the block diagram description, that the 10, 5 or 2 Units/Div is programmed. Table 5-1 shows that the A4 (or B4) is a logical ONE at only 10, 5 and 2 Units/Div.

No other logic circuits will be detailed, but the simple principles stated for Fig. 5-2 apply through the rest of the Decimal Unit Control circuits that can be diagrammed into logic symbols.

Analog circuits of the Type 3S6 Digital Unit Control circuit are in the UNITS/DIV MULTIPLIER DECODER block. These are described in detail.

## Units/Div Multiplier Decoder

The Units/Div Multiplier Decoder circuits (outlined on both the schematic and logic diagrams) consist of a Channel Select circuit and a Ternary to Binary Decoder. A secondary function of the Channel Select circuit is to limit the amplitude of the X0.1 and X10 Units/Div multiplier signals from the sampling head to voltage values usable at the Ternary To Binary Decoder. The multiplier signal for X1 Units/Div is not limited, but is instead a ground connection in the sampling head.

Fig. 5-3 shows the circuit changes to the input circuits of the Units/Div Multiplier Decoder for the three sampling head multiplier settings. The Channel Select portion is shown, including the current paths and output voltages for X0.1, X1 and X10 multiplier conditions. Output voltage is controlled within the Channel Select circuit for both the X0.1 and X10 condition. For the X1 condition, output voltage is determined by the ground connection in the sampling head. Thus, the circuit does not depend upon a stable current source from the sampling head except at the 1 condition.

## Ternary to Binary Decoder

Fig. 5-4 shows the Ternary to Binary Decoder circuit with input and output voltages. This part of the circuit is similar to the Channel Select section, in that they both translate certain input voltage values to other output voltage values. Component conduction conditions that generate (translate) the output voltages are listed in Table 5-6.

**TABLE 5-6**

Ternary to Binary Conduction Paths

| MULTI Units/Div | Electron Path |
|---|---|
| X0.1 | Logical 1<br>—4.4 V at Q789 emitter, through D792, R792 and D793 to give —0.06 V at X0.1 out. |
| | Logical 0<br>—4.4 V at Q789 emitter saturates Q796. R797-R798 current into load drops Q796 collector voltage to +1.6 V at X1. |
| | Logical 0<br>Q803 is at cutoff. Current in R802 and load gives +1.15 V at X10 out. |
| X1 | Logical 0<br>—0.68 V at Q789 emitter causes electron current in D792-R792-R793 to set +1.03 V at X0.1 out. |
| | Logical 1<br>R794-R795 reverse-bias Q796. No current in R797-R798 gives 0 V at X1 out. |
| | Logical 0<br>Q803 still at cutoff. Current in R802 and load gives +1.15 V at X10 out. |
| X10 | Logical 0<br>+3.4 V at Q798 emitter reverse biases D792. R793 current into load gives +1.15 V at X0.1 out. |
| | Logical 0<br>D797 conducts. Current in R798 and load gives +1.13 V at X1 out. |
| | Logical 1<br>Q803 saturates to give +0.13 V at X10 out. |

# OUTPUTS TO DIGITAL UNIT

## Decimal Control

All Units/Div Decoder and Units Multiplier Decoder signals are processed by the Decimal Control circuits as two-level binary logic. The 10, 5, 2 Units/Div Decoder, the 100, 50, 20 Units/Div Decoder, and the 200 Units/Div Decoder each feed two dual-input NAND gates of the Decimal Decoder. The X0.1, X1 and X10 input lines inhibit one gate of each pair of gates, allowing each Units/Div decoder to control only one decimal. Actually, only Decimal 4 and Decimal 5 are controlled by the decoders because the 200 Units/Div Decoder is combined with the 100, 50, 20 Units/Div Decoder output. Thus there are only two Units/Div categories controlling Decimal 4 or Decimal 5 (200, 100-50-20 and 10-5-2). Decimal 3 is programmed only when Decimal 4 or Decimal 5 are not asked for (by the combination of Units/Div decoders and Units multiplier). Table 5-7 identifies each Units/Div category control (200, 100-50-20, and 10-5-2) in the columns marked with an "X"; the Type 230 modifies the Decimal Control outputs when it receives a ÷5 command from the Counter Divide Control circuits.

Use Tables 5-2, 5-3 and 5-4 if the circuits require maintenance. Set the digital unit controls for an amplitude measurement and use an 11 MΩ VTVM to check for proper gate voltages. Voltage values for the truth tables are given at the bottom of Fig. 5-1.

## Units Control

The Units Control block contains logic-type circuits that cause Q855 to conduct (for Volts) when the sampling head input logic line is at a logical ONE. Q857 conducts (for Amps) when the sampling head input line is at a logical ZERO (+15 volts through 30 kΩ). This simple mode of operation is possible whenever one of the digital unit D, U, GND lines is at a logical ONE. If both D, U, GND lines are at a logical ZERO, the output tries to program Volts, but the D, U INHIBIT signal from Q859 makes both outputs a logical ZERO. Both D, U, GND lines will be at logical ZERO when the digital unit is programmed to take a time measurement.

## Counter Divide Control

All states of the Counter Divide Control block are shown in Table 5-5. The circuits are not described. Use the truth table of Table 5-5, and the voltages at the bottom of Fig. 5-1 when servicing the circuits.

## Outputs Summary

Table 5-8 lists all the Digital Unit Control circuit inputs and outputs (except the V or A units) in summary form related to the digital unit readout display. The Type 230 interprets the outputs internally. On a decimal output line that is a logical ZERO, a 230 will place the output voltage at about +6 or +8 volts. The Units Mult column of Table 5-8 indicates whether the digital unit "M" lamp is lighted.

**TABLE 5-7**

Digital Unit Decimal Numbering

| | |
|---|---|
| Type 230: | 0 . 0 . 0 . 0 . 0 . 0 |
| DEC: | 1 2 3 4 5 |

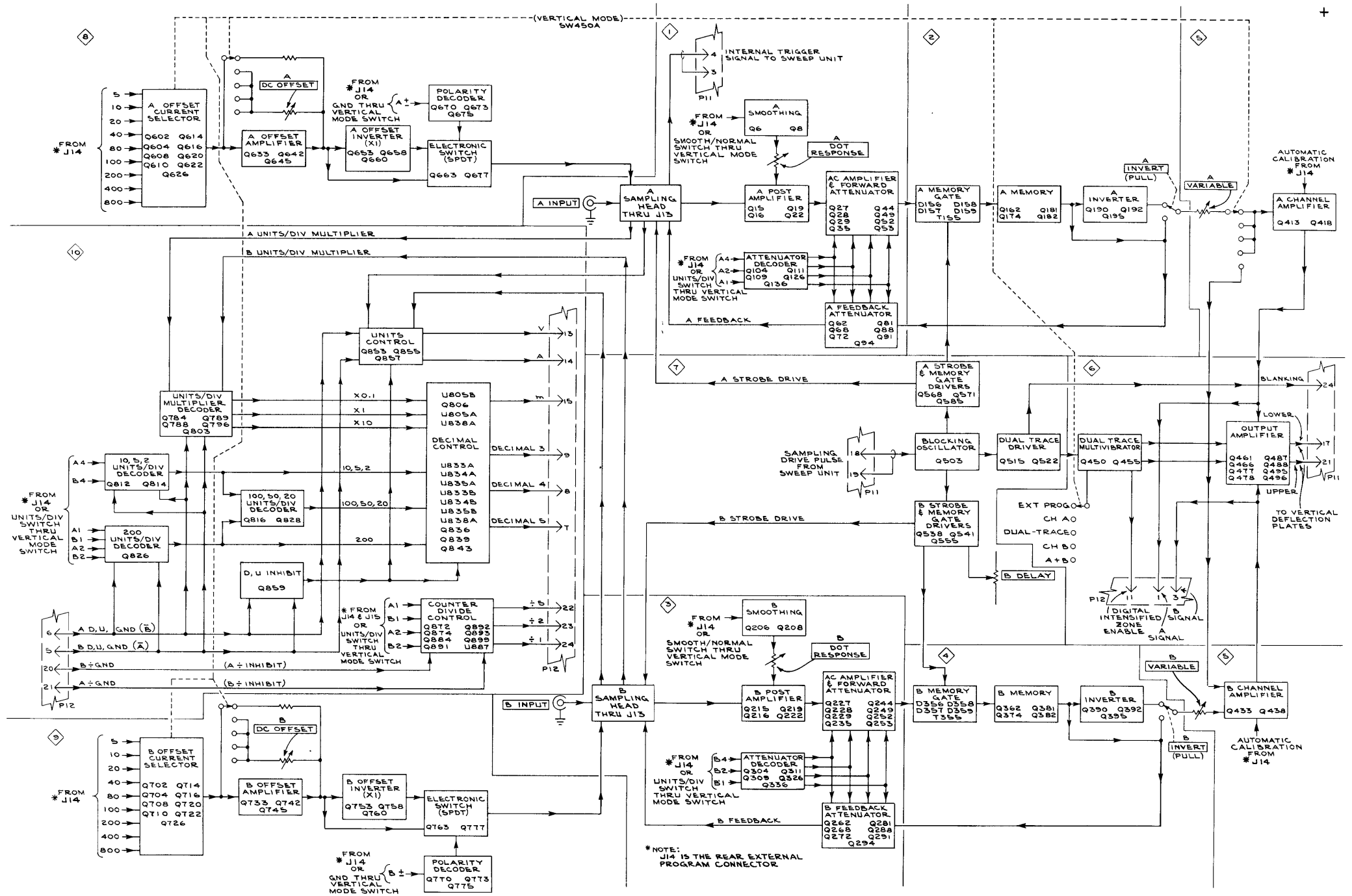
**TABLE 5-8**

Digital Unit Control circuit outputs related to Digital Unit readout display

| | Sampling Head Units/Div Multiplier | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | X0.1 20/Div to 0.2/Div | | | | | X1 200/Div to 2/Div | | | | | X10 2000/Div to 20/Div | | | | |
| Units/ Div | Dec 2 | Dec 3 | Dec 4 | Dec 5 | Units Mult | Dec 2 | Dec 3 | Dec 4 | Dec 5 | Units Mult | Dec 2 | Dec 3 | Dec 4 | Dec 5 | Units Mult |
| 200 | | | 230 | | m | 230 | | | | None | | 230 | | | None |
| 100 | | | 230 | | m | | | | 230 | m | | 230 | | | None |
| 50 | | | 230 | | m | | | | 230 | m | | 230 | | | None |
| 20 | | 230 | | | m | | | 230 | 6R1A | m | 230 | | | | None |
| 10 | | 230 | | | m | | | 230 | | m | | | | 230 | m |
| 5 | | 230 | | | m | | | 230 | | m | | | | 230 | m |
| 2 | 230 | | | | m | | 230 | | | m | | | 230 | | m |

The Type 230 contains 5 number readout lamps and one polarity readout lamp. Table 5-7 identifies the lighted decimal neon.

When the Type 3S6 is front panel controlled and the VARIABLE control is turned from its CAL detent position the units lamps of the Type 230 go out, and the decimal neons shift around in a random manner, dependent upon the position of the Units/Div switches. This is normal.

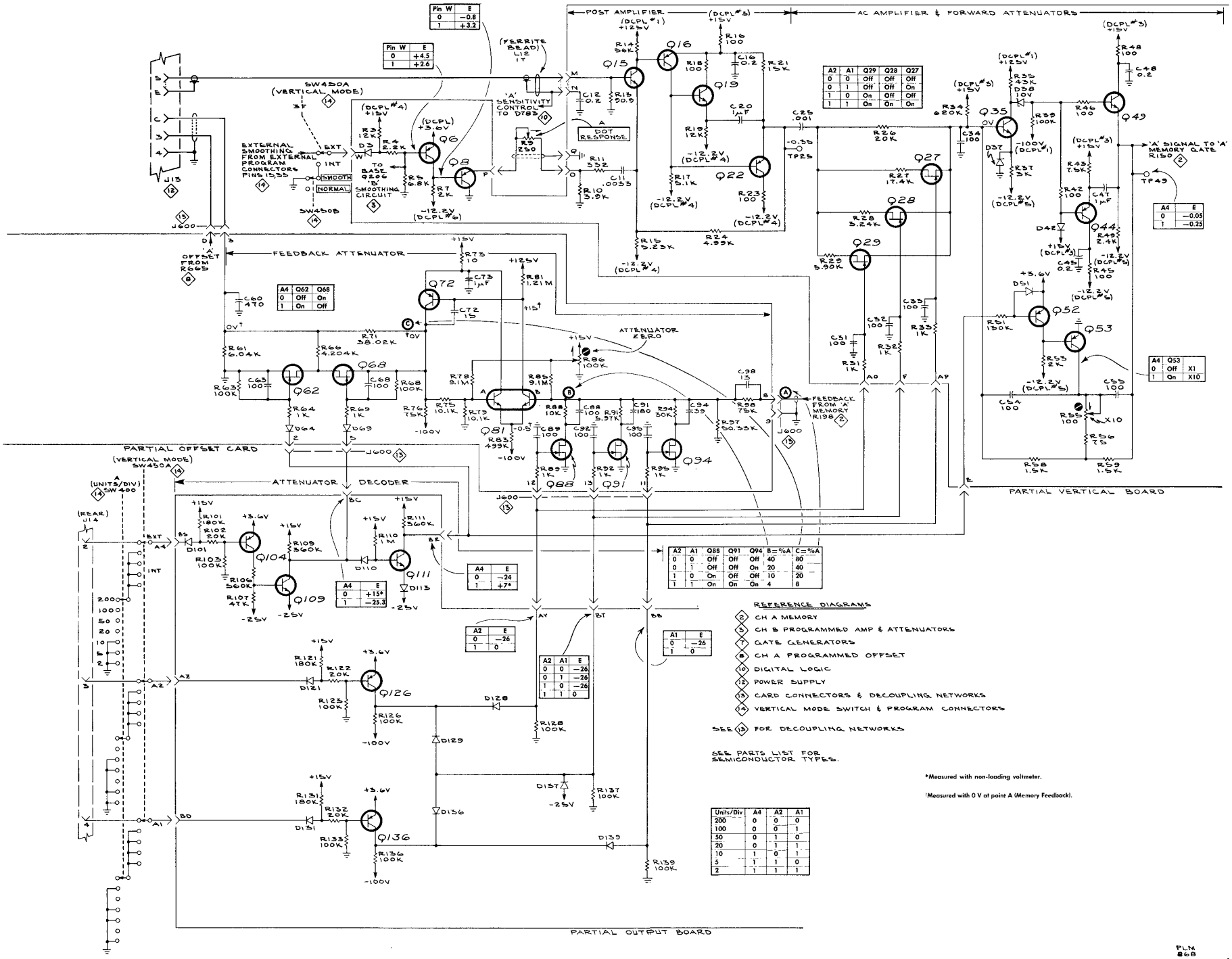



TYPE 356

A

BLOCK DIAGRAM

PLM 868




| Pin W | E |
|---|---|
| 0 | −0.8 |
| 1 | +3.2 |

| Pin W | E |
|---|---|
| 0 | +4.5 |
| 1 | +2.6 |

| A2 | A1 | Q29 | Q28 | Q27 |
|---|---|---|---|---|
| 0 | 0 | Off | Off | Off |
| 0 | 1 | Off | Off | On |
| 1 | 0 | On | Off | Off |
| 1 | 1 | On | On | On |

| A4 | E |
|---|---|
| 0 | −0.05 |
| 1 | −0.25 |

| A4 | Q53 |
|---|---|
| 0 | Off X1 |
| 1 | On X10 |

| A4 | Q62 | Q68 |
|---|---|---|
| 0 | Off | On |
| 1 | On | Off |

| A4 | E |
|---|---|
| 0 | +15* |
| 1 | −25.3 |

| A4 | E |
|---|---|
| 0 | −24 |
| 1 | +7* |

| A2 | E |
|---|---|
| 0 | −26 |
| 1 | 0 |

| A2 | A1 | E |
|---|---|---|
| 0 | 0 | −26 |
| 0 | 1 | −26 |
| 1 | 0 | −26 |
| 1 | 1 | 0 |

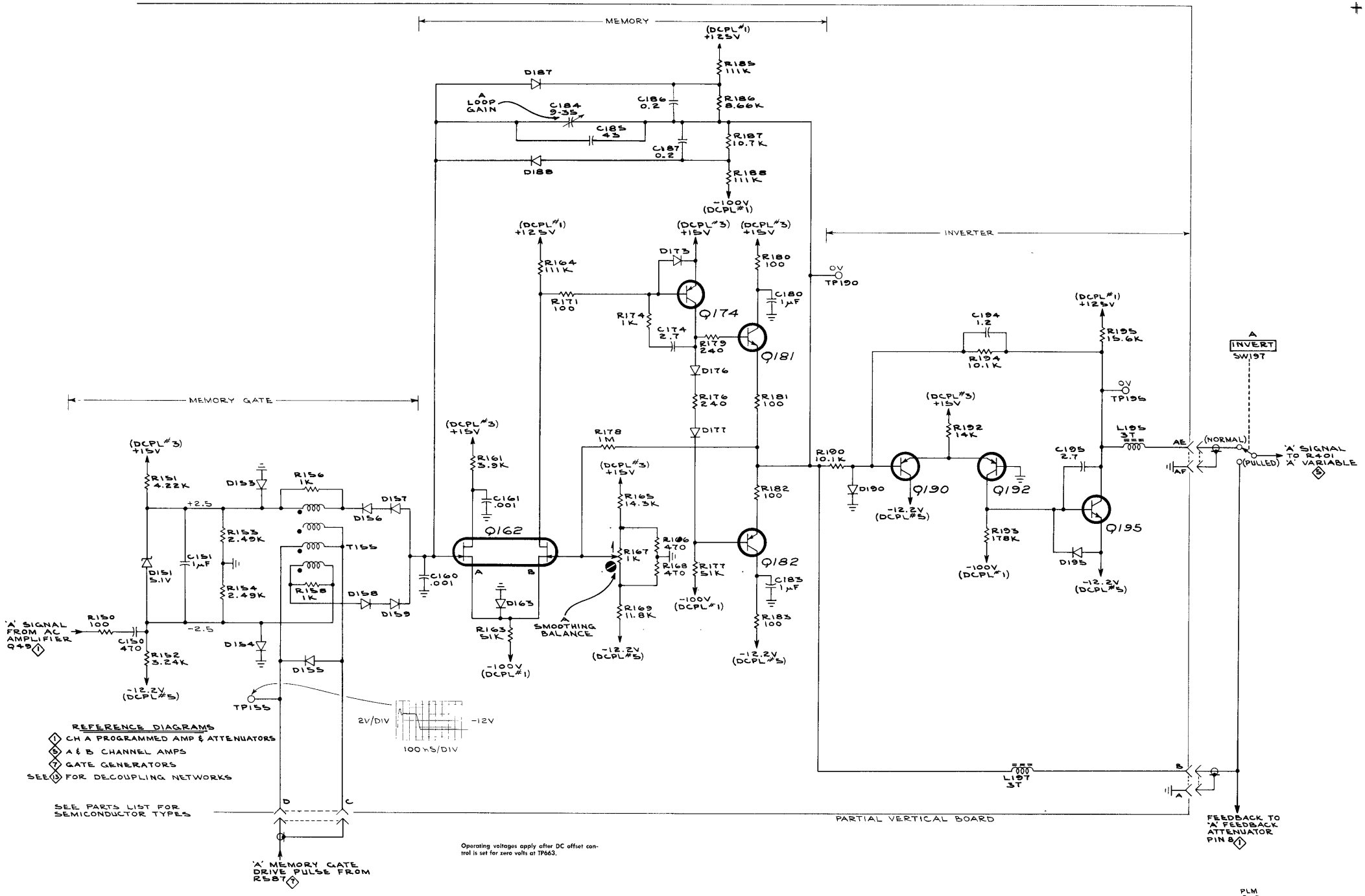
| A1 | E |
|---|---|
| 0 | −26 |
| 1 | 0 |

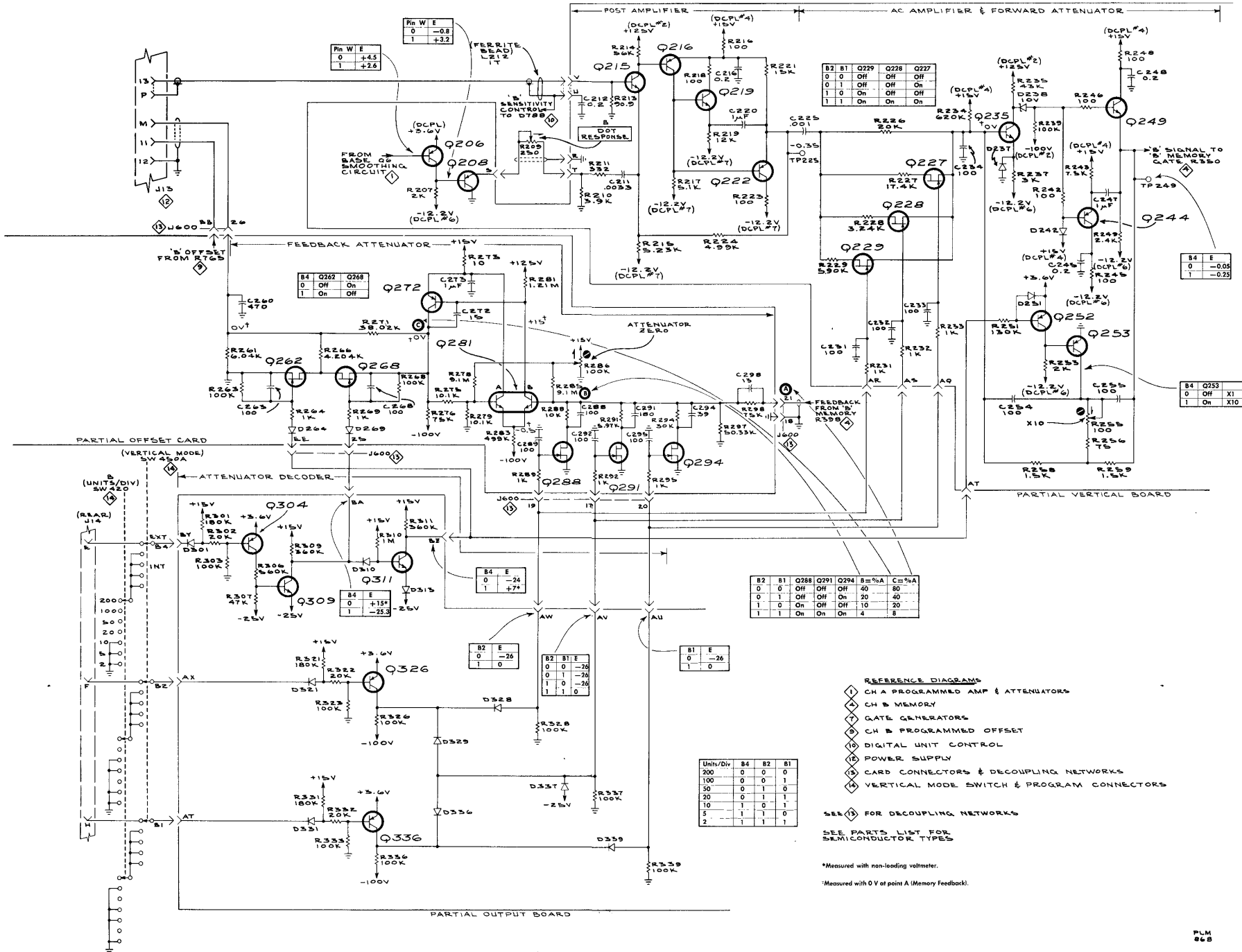
| A2 | A1 | Q88 | Q91 | Q94 | B=%A | C=%A |
|---|---|---|---|---|---|---|
| 0 | 0 | Off | Off | Off | 40 | 80 |
| 0 | 1 | Off | Off | On | 20 | 40 |
| 1 | 0 | On | Off | Off | 10 | 20 |
| 1 | 1 | On | On | On | 4 | 8 |

| Units/Div | A4 | A2 | A1 |
|---|---|---|---|
| 200 | 0 | 0 | 0 |
| 100 | 0 | 0 | 1 |
| 50 | 0 | 1 | 0 |
| 20 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 |
| 5 | 1 | 1 | 0 |
| 2 | 1 | 1 | 1 |



# CH A PROGRAMMED AMP & ATTENUATORS (1)


MEMORY
INVERTER
MEMORY GATE
(DCPL#1) +125V
(DCPL#3) +15V
-100V (DCPL#1)
-12.2V (DCPL#5)
D187
D188
R185 111K
R186 8.66K
R187 10.7K
R188 111K
C184 9-35
C185 43
C186 0.2
C187 0.2
A LOOP GAIN
R164 111K
R171 100
R174 1K
C174 2.7
D173
Q174
R179 240
Q181
D176
R176 240
D177
R178 1M
R180 100
C180 1μF
R181 100
R182 100
C183 1μF
R183 100
0V TP190
R161 3.9K
C161 .001
Q162
A
B
D163
R163 51K
SMOOTHING BALANCE
R165 14.3K
R166 470
R167 1K
R168 470
R177 51K
Q182
R169 11.8K
R190 10.1K
D190
Q190
Q192
R192 14K
R193 178K
C194 1.2
R194 10.1K
R195 15.6K
0V TP195
C195 2.7
Q195
D195
L195 3T
AE
AF
(NORMAL)
(PULLED)
A INVERT SW197
'A' SIGNAL TO R401 'A' VARIABLE (5)
L197 3T
B
A
FEEDBACK TO 'A' FEEDBACK ATTENUATOR PIN 8 (1)
R151 4.22K
+2.5
-2.5
D153
R156 1K
D157
D156
R153 2.49K
T155
R154 2.49K
C151 1μF
D151 5.1V
R158 1K
D158
D159
D154
D155
R150 100
'A' SIGNAL FROM AC AMPLIFIER Q49 (1)
C150 470
R152 3.24K
C160 .001
TP155
2V/DIV
-12V
100 nS/DIV
REFERENCE DIAGRAMS
(1) CH A PROGRAMMED AMP & ATTENUATORS
(5) A & B CHANNEL AMPS
(7) GATE GENERATORS
SEE (13) FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
D
C
PARTIAL VERTICAL BOARD
'A' MEMORY GATE DRIVE PULSE FROM R587 (7)
Operating voltages apply after DC offset control is set for zero volts at TP663.




| Pin W | E |
|---|---|
| 0 | −0.8 |
| 1 | +3.2 |

| Pin W | E |
|---|---|
| 0 | +4.5 |
| 1 | +2.6 |

| B2 | B1 | Q229 | Q228 | Q227 |
|---|---|---|---|---|
| 0 | 0 | Off | Off | Off |
| 0 | 1 | Off | Off | On |
| 1 | 0 | On | Off | Off |
| 1 | 1 | On | On | On |

| B4 | Q262 | Q268 |
|---|---|---|
| 0 | Off | On |
| 1 | On | Off |

| B4 | E |
|---|---|
| 0 | −0.05 |
| 1 | −0.25 |

| B4 | Q253 | |
|---|---|---|
| 0 | Off | X1 |
| 1 | On | X10 |

| B4 | E |
|---|---|
| 0 | −24 |
| 1 | +7* |

| B4 | E |
|---|---|
| 0 | +15* |
| 1 | −25.3 |

| B2 | E |
|---|---|
| 0 | −26 |
| 1 | 0 |

| B2 | B1 | E |
|---|---|---|
| 0 | 0 | −26 |
| 0 | 1 | −26 |
| 1 | 0 | −26 |
| 1 | 1 | 0 |

| B1 | E |
|---|---|
| 0 | −26 |
| 1 | 0 |

| B2 | B1 | Q288 | Q291 | Q294 | B=%A | C=%A |
|---|---|---|---|---|---|---|
| 0 | 0 | Off | Off | Off | 40 | 80 |
| 0 | 1 | Off | Off | On | 20 | 40 |
| 1 | 0 | On | Off | Off | 10 | 20 |
| 1 | 1 | On | On | On | 4 | 8 |

| Units/Div | B4 | B2 | B1 |
|---|---|---|---|
| 200 | 0 | 0 | 0 |
| 100 | 0 | 0 | 1 |
| 50 | 0 | 1 | 0 |
| 20 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 |
| 5 | 1 | 1 | 0 |
| 2 | 1 | 1 | 1 |

REFERENCE DIAGRAMS

1. CH A PROGRAMMED AMP & ATTENUATORS
4. CH B MEMORY
7. GATE GENERATORS
9. CH B PROGRAMMED OFFSET
10. DIGITAL UNIT CONTROL
12. POWER SUPPLY
13. CARD CONNECTORS & DECOUPLING NETWORKS
14. VERTICAL MODE SWITCH & PROGRAM CONNECTORS

SEE 13 FOR DECOUPLING NETWORKS

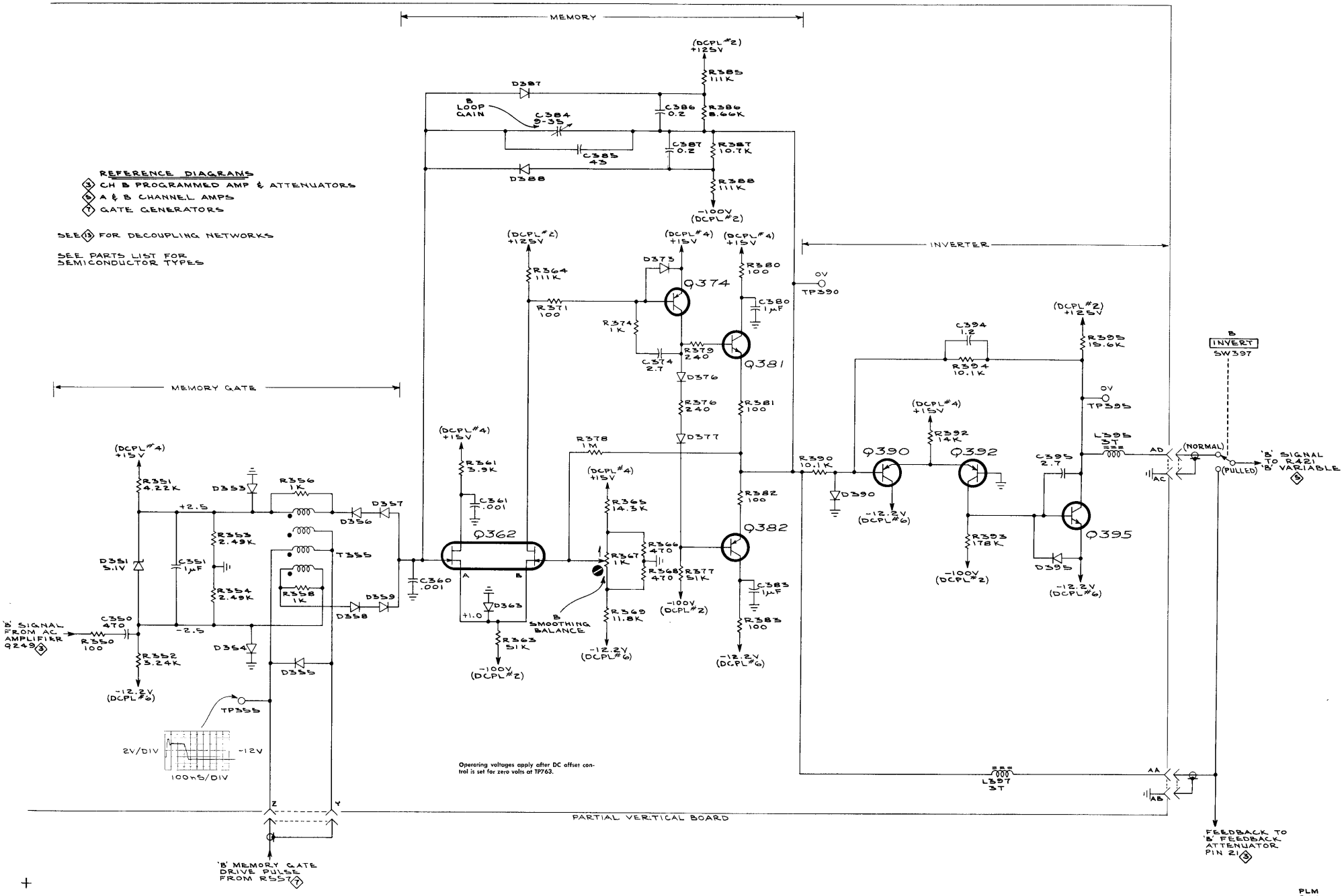
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

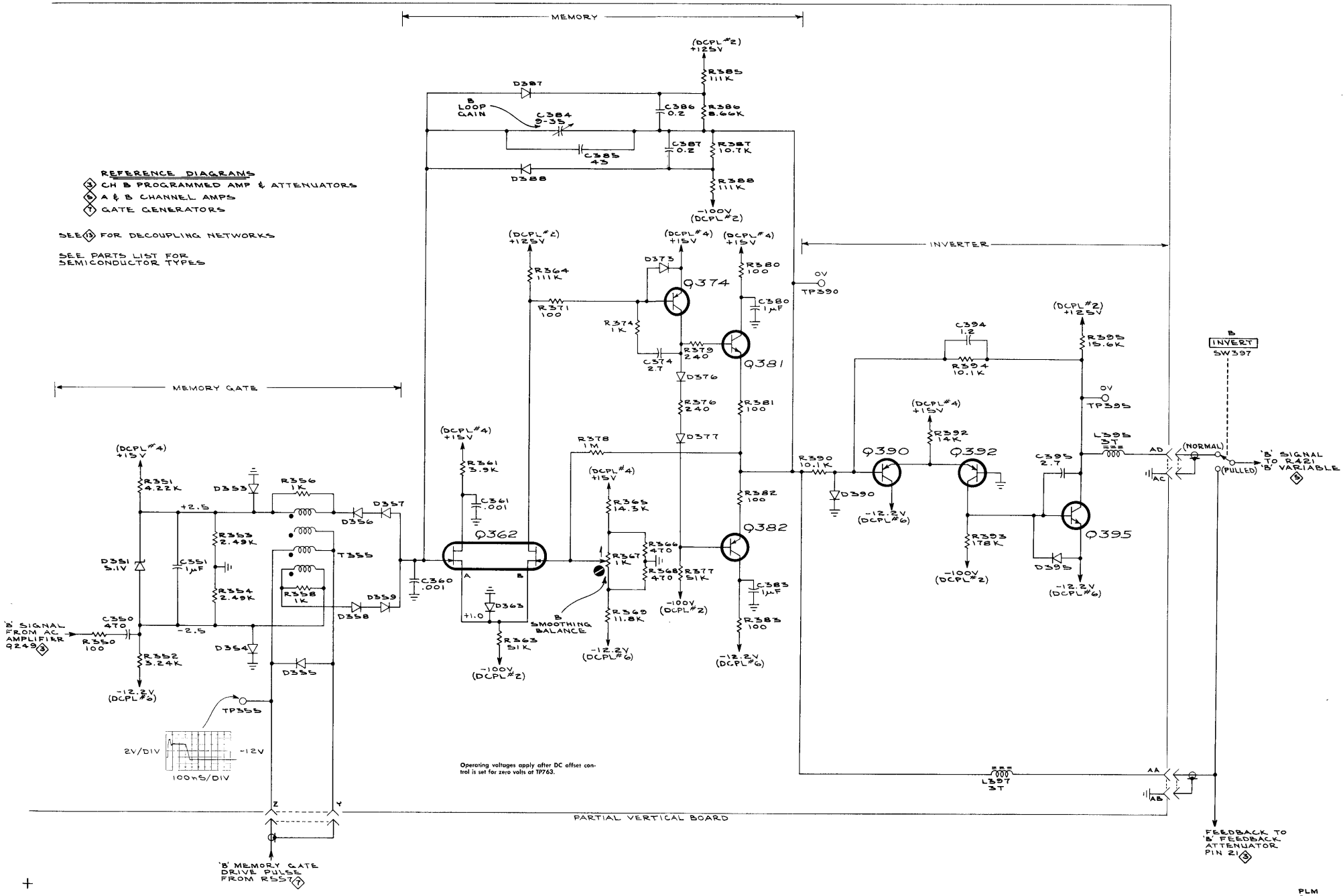
*Measured with non-loading voltmeter.

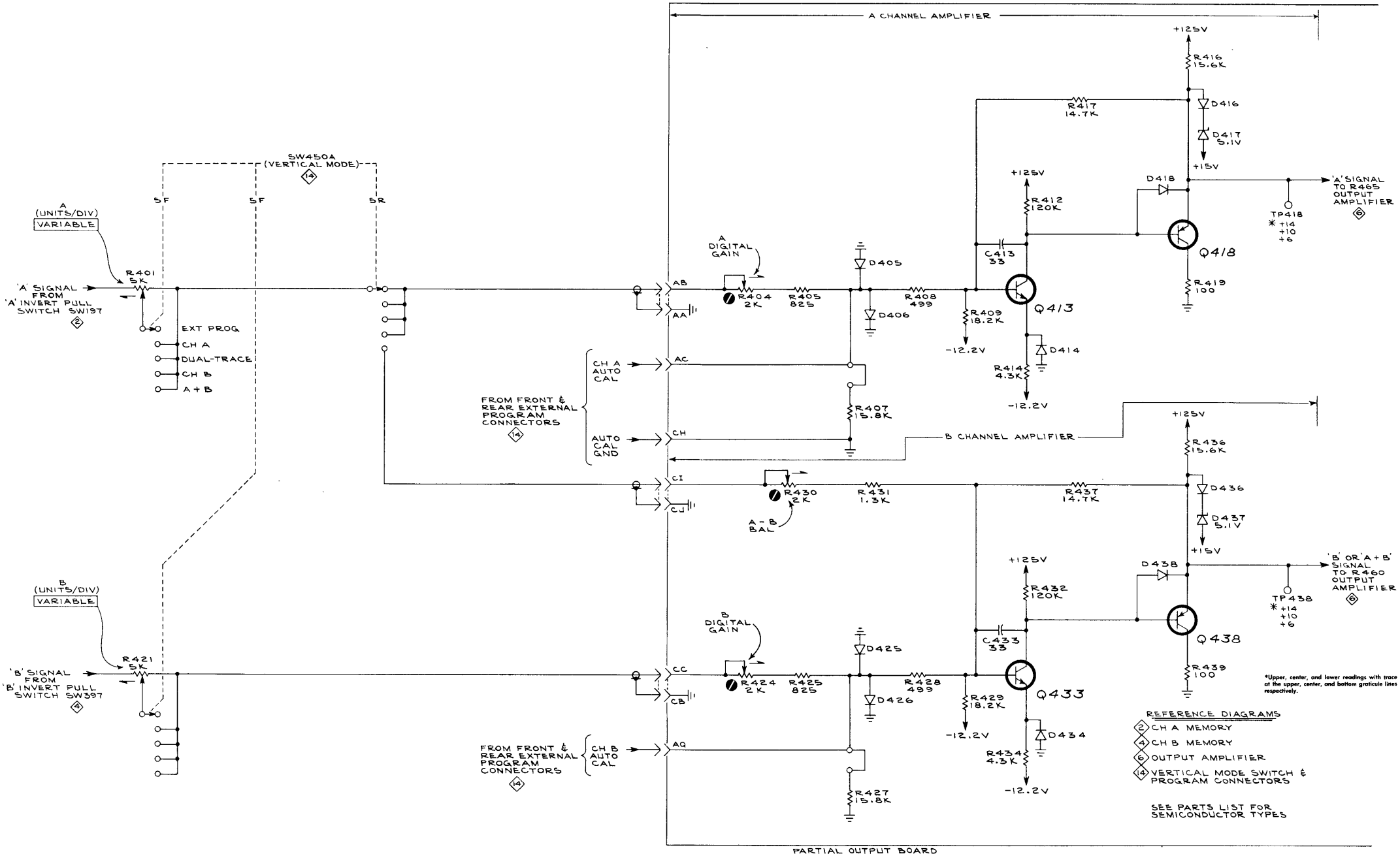
†Measured with 0 V at point A (Memory Feedback).

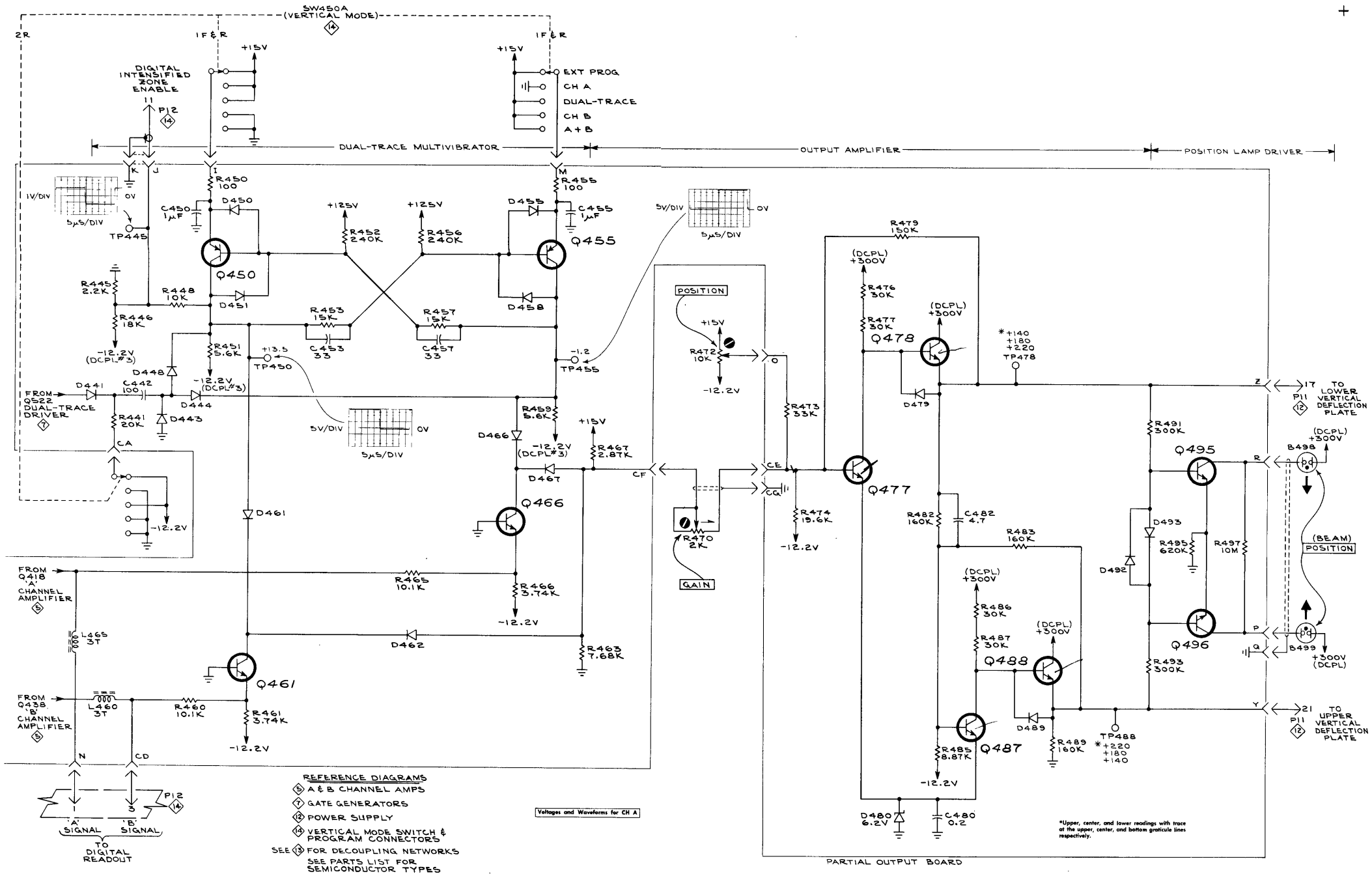
PLM 868

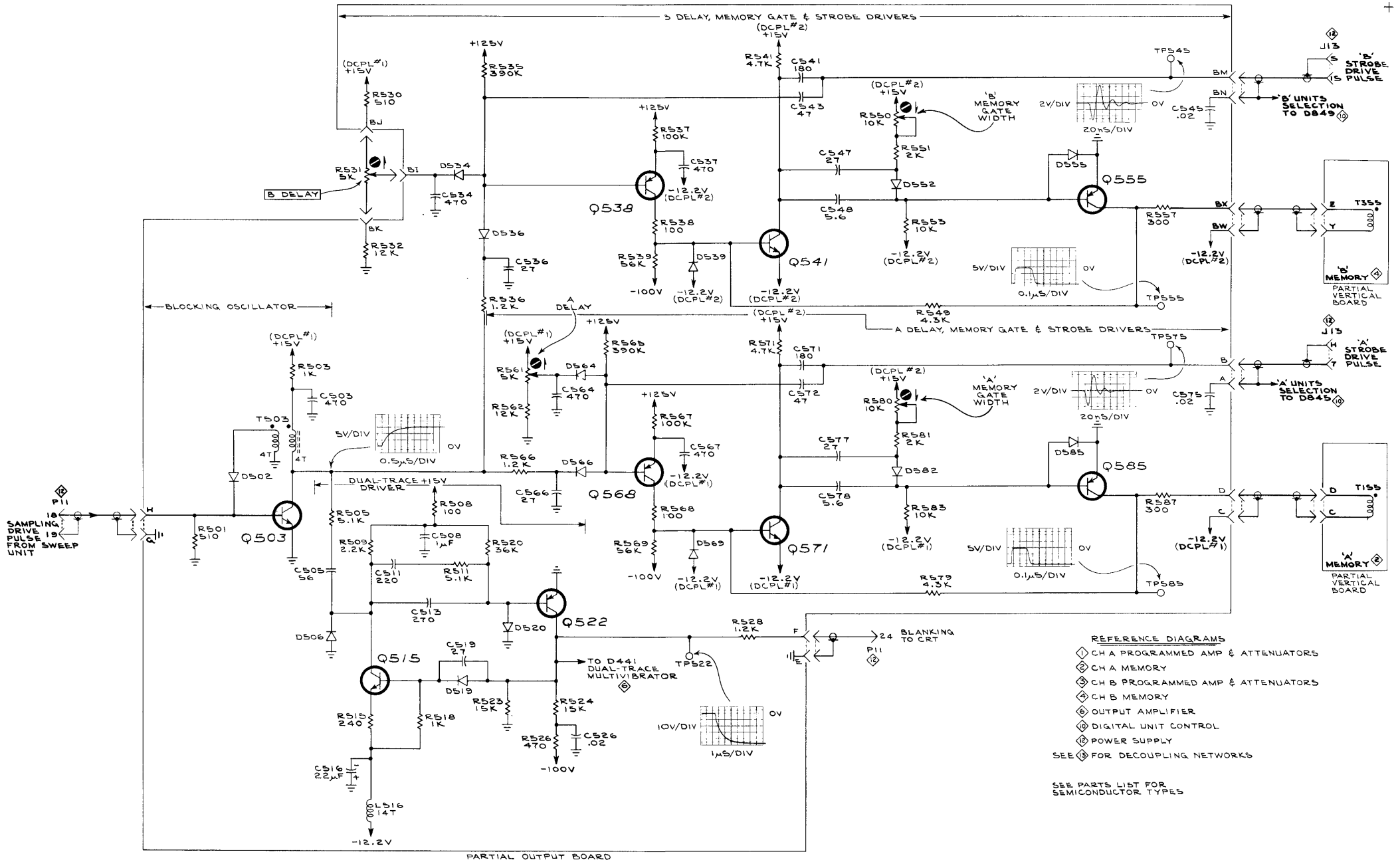
# CH B PROGRAMMED AMP & ATTENUATORS 3


MEMORY
INVERTER
MEMORY GATE
REFERENCE DIAGRAMS
3 CH B PROGRAMMED AMP & ATTENUATORS
5 A & B CHANNEL AMPS
7 GATE GENERATORS
SEE 13 FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
(DCPL #2) +125V
R385 111K
D387
B LOOP GAIN
C384 9-35
C386 0.2
R386 8.66K
C385 43
C387 0.2
R387 10.7K
D388
R388 111K
-100V (DCPL #2)
(DCPL #4) +15V
R364 111K
R371 100
D373
Q374
R380 100
C380 1μF
R374 1K
C374 2.7
R379 240
Q381
D376
R376 240
R381 100
D377
0V TP390
C394 1.2
R394 10.1K
R395 15.6K
0V TP395
B INVERT SW397
(NORMAL)
(PULLED)
'B' SIGNAL TO R421 VARIABLE 5
L395 3T
AD
AC
R390 10.1K
D390
Q390
Q392
R392 14K
-12.2V (DCPL #6)
R393 178K
-100V (DCPL #2)
C395 2.7
Q395
D395
R378 1M
R361 3.9K
C361 .001
Q362
R365 14.3K
R366 470
R367 1K
R368 470
R377 51K
R382 100
Q382
C383 1μF
R383 100
R369 11.8K
R363 51K
D363
+1.0
B SMOOTHING BALANCE
-100V (DCPL #2)
-12.2V (DCPL #6)
R351 4.22K
+2.5
D353
R356 1K
D357
D356
R353 2.49K
T355
D351 5.1V
C351 1μF
R354 2.49K
R358 1K
D359
D358
C360 .001
C350 470
'B' SIGNAL FROM AC AMPLIFIER 9249 3
R350 100
-2.5
D354
R352 3.24K
D355
-12.2V (DCPL #6)
TP355
2V/DIV
-12V
100nS/DIV
Z
Y
'B' MEMORY GATE DRIVE PULSES FROM R557 7
Operating voltages apply after DC offset control is set for zero volts at TP763.
PARTIAL VERTICAL BOARD
L397 3T
AA
AB
FEEDBACK TO 'B' FEEDBACK ATTENUATOR PIN 21 3


MEMORY
INVERTER
MEMORY GATE
REFERENCE DIAGRAMS
3 CH B PROGRAMMED AMP & ATTENUATORS
6 A & B CHANNEL AMPS
7 GATE GENERATORS
SEE 13 FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
B LOOP GAIN
B SMOOTHING BALANCE
B INVERT SW397
(NORMAL)
(PULLED)
'B' SIGNAL TO R421 VARIABLE 5
'B' SIGNAL FROM AC AMPLIFIER Q249 3
'B' MEMORY GATE DRIVE PULSE FROM R557 7
FEEDBACK TO 'B' FEEDBACK ATTENUATOR PIN 21 3
TP355
TP390
TP395
2V/DIV
100nS/DIV
-12V
Operating voltages apply after DC offset control is set for zero volts at TP763.
PARTIAL VERTICAL BOARD
Q362
Q374
Q381
Q382
Q390
Q392
Q395
T355
L395 5T
L397 3T
(DCPL#2) +125V
(DCPL#4) +15V
-100V (DCPL#2)
-12.2V (DCPL#6)

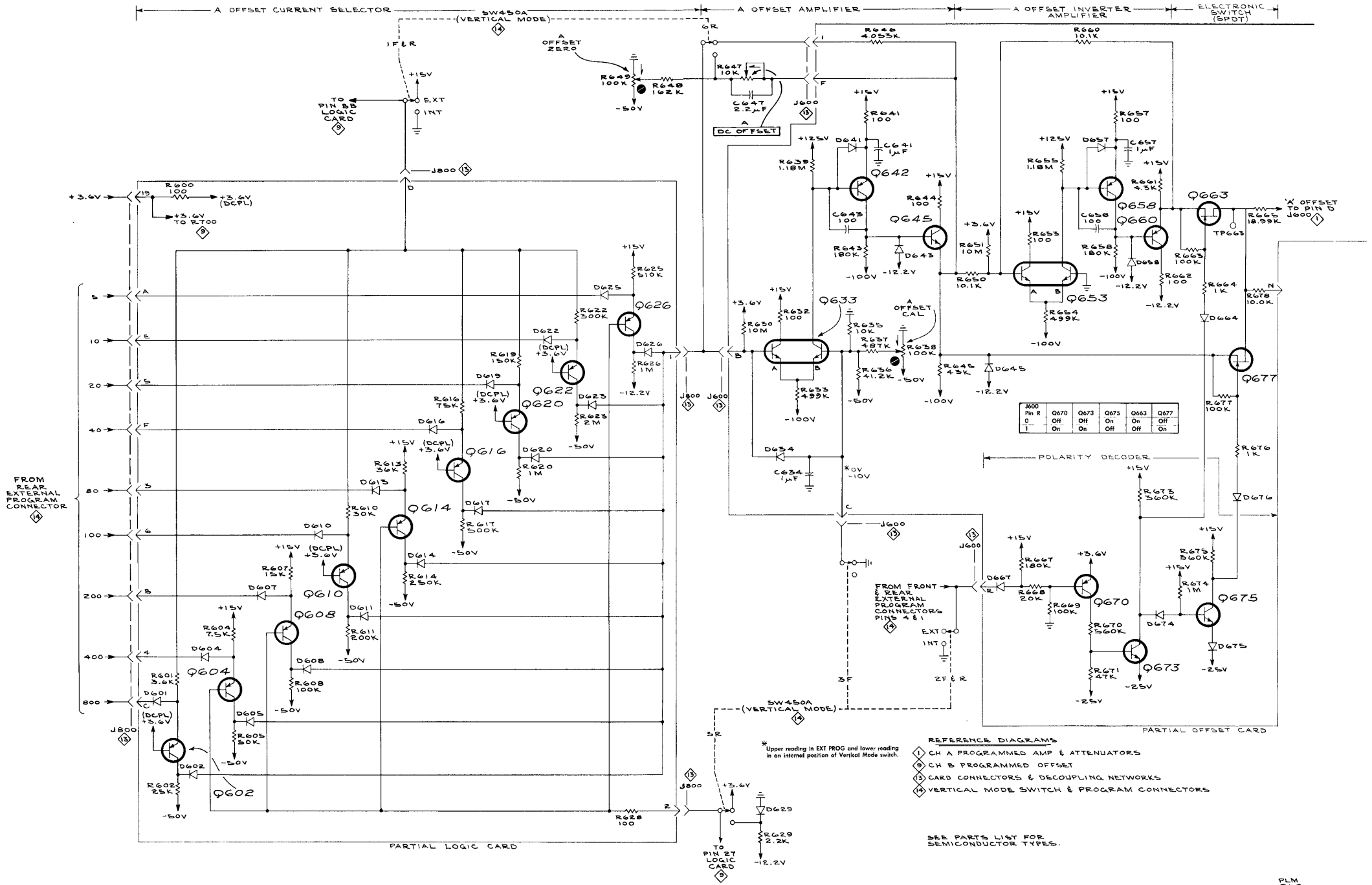

A CHANNEL AMPLIFIER
B CHANNEL AMPLIFIER
PARTIAL OUTPUT BOARD
SW450A (VERTICAL MODE) 14
5F
5F
5R
A (UNITS/DIV) VARIABLE
R401 5K
'A' SIGNAL FROM 'A' INVERT PULL SWITCH SW197 2
EXT PROG
CH A
DUAL-TRACE
CH B
A+B
A DIGITAL GAIN
R404 2K
R405 825
R408 499
D405
D406
AB
AA
AC
CH A AUTO CAL
FROM FRONT & REAR EXTERNAL PROGRAM CONNECTORS 14
AUTO CAL GND
CH
R407 15.8K
+125V
R416 15.6K
R417 14.7K
D416
D417 5.1V
+15V
D418
R412 120K
C413 33
Q413
Q418
R409 18.2K
-12.2V
D414
R414 4.3K
R419 100
TP418 *+14 +10 +6
'A' SIGNAL TO R465 OUTPUT AMPLIFIER 6
CI
CJ
R430 2K
A-B BAL
R431 1.3K
R437 14.7K
R436 15.6K
D436
D437 5.1V
D438
R432 120K
C433 33
Q433
Q438
R429 18.2K
D434
R434 4.3K
R439 100
TP438 *+14 +10 +6
'B' OR 'A+B' SIGNAL TO R460 OUTPUT AMPLIFIER 6
B (UNITS/DIV) VARIABLE
R421 5K
'B' SIGNAL FROM 'B' INVERT PULL SWITCH SW397 4
B DIGITAL GAIN
R424 2K
R425 825
R428 499
D425
D426
CC
CB
CQ
FROM FRONT & REAR EXTERNAL PROGRAM CONNECTORS 14
CH B AUTO CAL
R427 15.8K
*Upper, center, and lower readings with trace at the upper, center, and bottom graticule lines respectively.
REFERENCE DIAGRAMS
2 CH A MEMORY
4 CH B MEMORY
6 OUTPUT AMPLIFIER
14 VERTICAL MODE SWITCH & PROGRAM CONNECTORS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES


SW450A (VERTICAL MODE) 14
2R
1F & R
+15V
DIGITAL INTENSIFIED ZONE ENABLE
11
P12 14
EXT PROG
CH A
DUAL-TRACE
CH B
A+B
DUAL-TRACE MULTIVIBRATOR
OUTPUT AMPLIFIER
POSITION LAMP DRIVER
1V/DIV
5μS/DIV
TP445
R450 100
R455 100
C450 1μF
C455 1μF
D450
D455
+125V
R452 240K
R456 240K
Q450
Q455
D451
D458
R445 2.2K
R446 18K
R448 10K
R453 15K
R457 15K
C453 33
C457 33
-12.2V (DCPL#3)
R451 5.6K
+13.5
TP450
-1.2
TP455
D448
D441
C442 100
D444
D443
R441 20K
FROM Q522 DUAL-TRACE DRIVER 7
CA
5V/DIV
5μS/DIV
R459 5.6K
D466
R467 2.87K
D467
CF
Q466
D461
D462
R465 10.1K
R466 3.74K
R463 7.68K
FROM Q418 'A' CHANNEL AMPLIFIER 5
L465 3T
Q461
FROM Q438 'B' CHANNEL AMPLIFIER 5
L460 3T
R460 10.1K
R461 3.74K
N
CD
P12 14
'A' SIGNAL
'B' SIGNAL
TO DIGITAL READOUT
POSITION
R472 10K
GAIN
R470 2K
CE
CG
R473 33K
R474 19.6K
Q477
R479 150K
(DCPL) +300V
R476 30K
R477 30K
Q478
D479
*+140 +180 +220
TP478
R482 160K
C482 4.7
R483 160K
R486 30K
R487 30K
Q488
D489
R485 8.87K
Q487
R489 160K
TP488
*+220 +180 +140
D480 6.2V
C480 0.2
R491 300K
Q495
Q496
D492
D493
R495 620K
R497 10M
R493 300K
B498
B499
(BEAM) POSITION
+300V (DCPL)
Z
R
P
Q
Y
17 P11 12 TO LOWER VERTICAL DEFLECTION PLATE
21 P11 12 TO UPPER VERTICAL DEFLECTION PLATE
REFERENCE DIAGRAMS
5 A & B CHANNEL AMPS
7 GATE GENERATORS
12 POWER SUPPLY
14 VERTICAL MODE SWITCH & PROGRAM CONNECTORS
SEE 13 FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
Voltages and Waveforms for CH A
*Upper, center, and lower readings with trace at the upper, center, and bottom graticule lines respectively.
PARTIAL OUTPUT BOARD


B DELAY, MEMORY GATE & STROBE DRIVERS
A DELAY, MEMORY GATE & STROBE DRIVERS
BLOCKING OSCILLATOR
DUAL-TRACE +15V DRIVER
PARTIAL OUTPUT BOARD
PARTIAL VERTICAL BOARD
'B' MEMORY GATE WIDTH
'A' MEMORY GATE WIDTH
'B' STROBE DRIVE PULSE
'A' STROBE DRIVE PULSE
'B' UNITS SELECTION TO D849
'A' UNITS SELECTION TO D845
SAMPLING DRIVE PULSE FROM SWEEP UNIT
TO D441 DUAL-TRACE MULTIVIBRATOR
BLANKING TO CRT
Q503
Q515
Q522
Q538
Q541
Q555
Q568
Q571
Q585
REFERENCE DIAGRAMS
1 CH A PROGRAMMED AMP & ATTENUATORS
2 CH A MEMORY
3 CH B PROGRAMMED AMP & ATTENUATORS
4 CH B MEMORY
6 OUTPUT AMPLIFIER
10 DIGITAL UNIT CONTROL
12 POWER SUPPLY
SEE 13 FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES



PLM 868

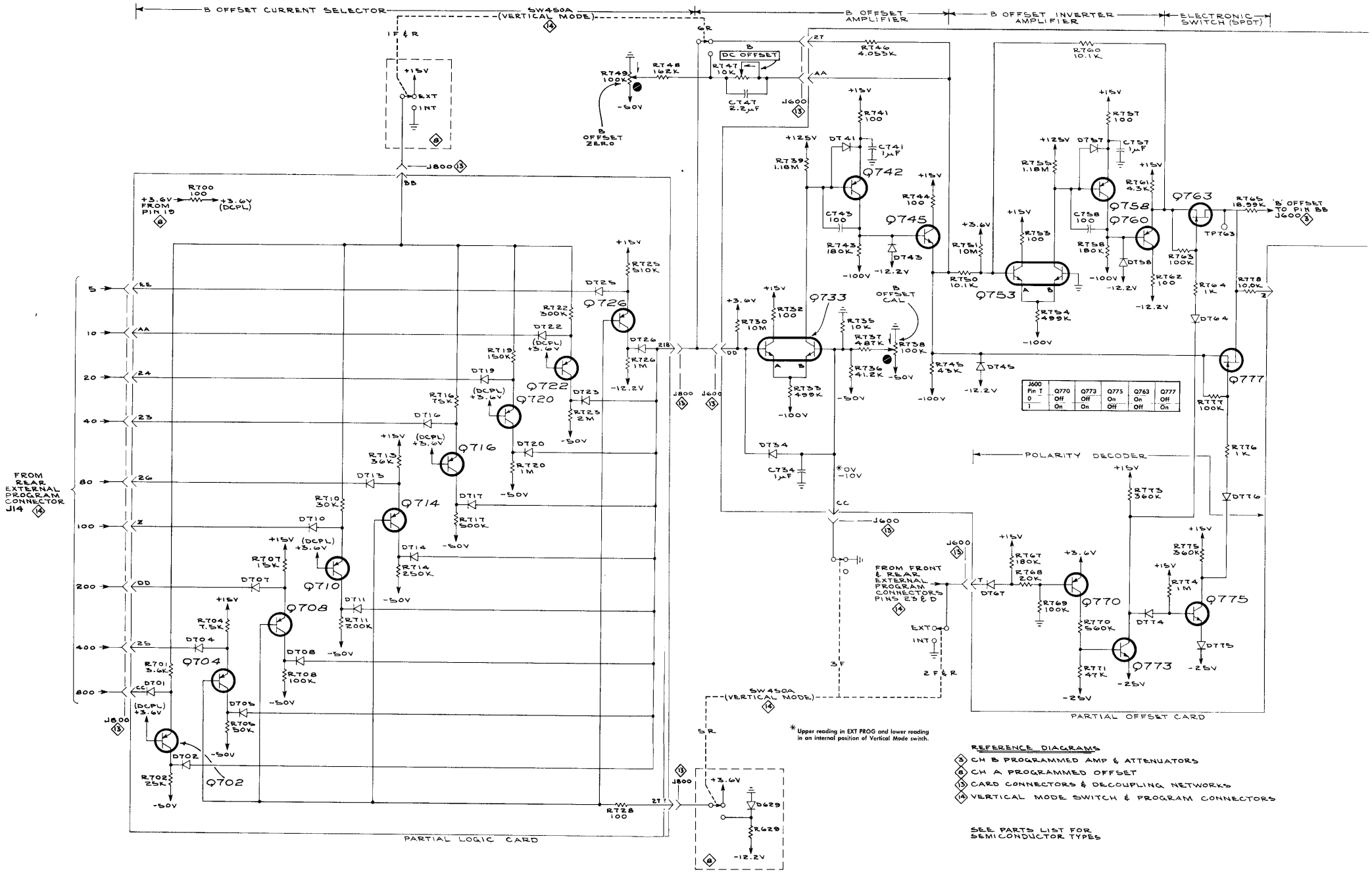



TYPE 356

A

CH A PROGRAMMED OFFSET 8

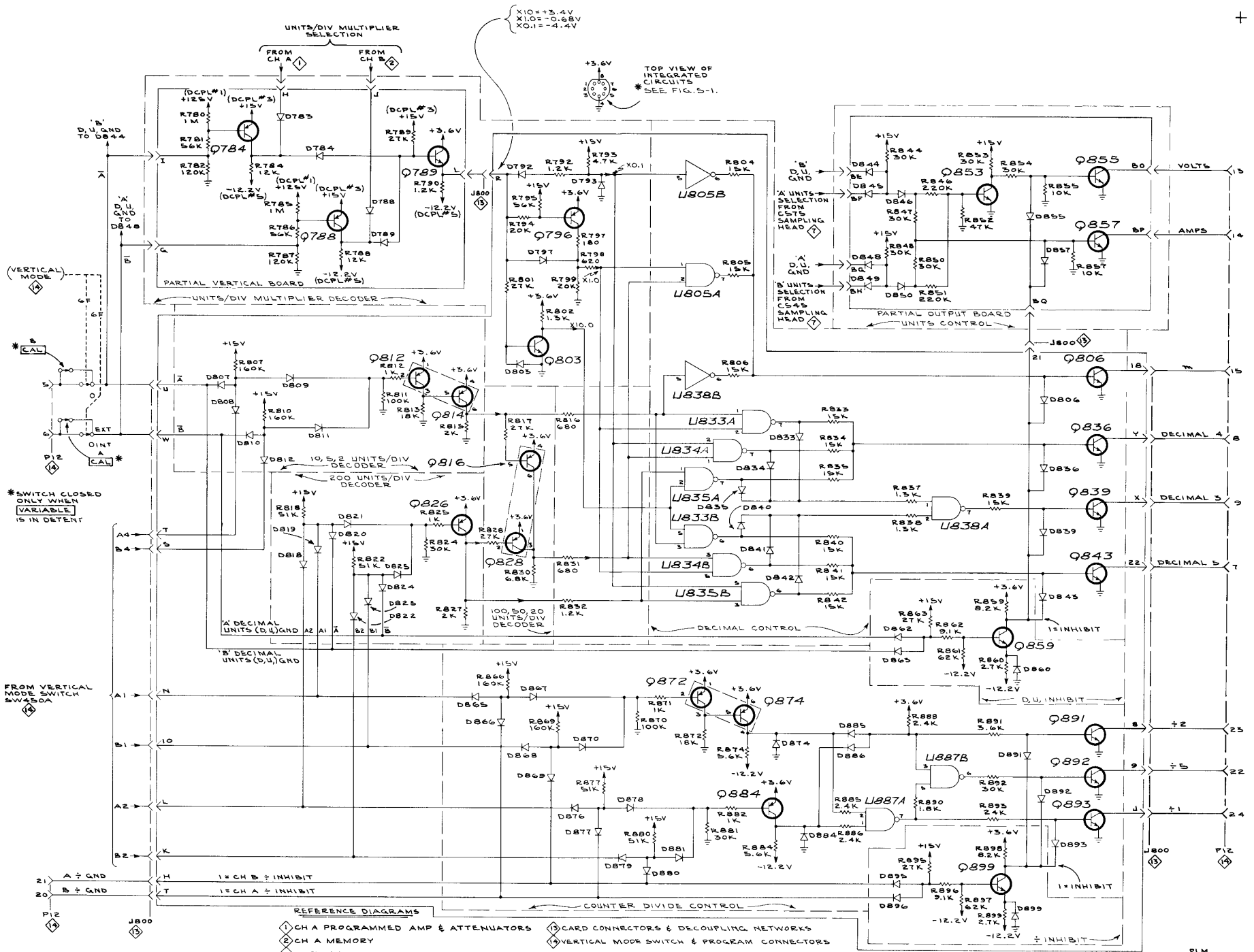
PLM 868

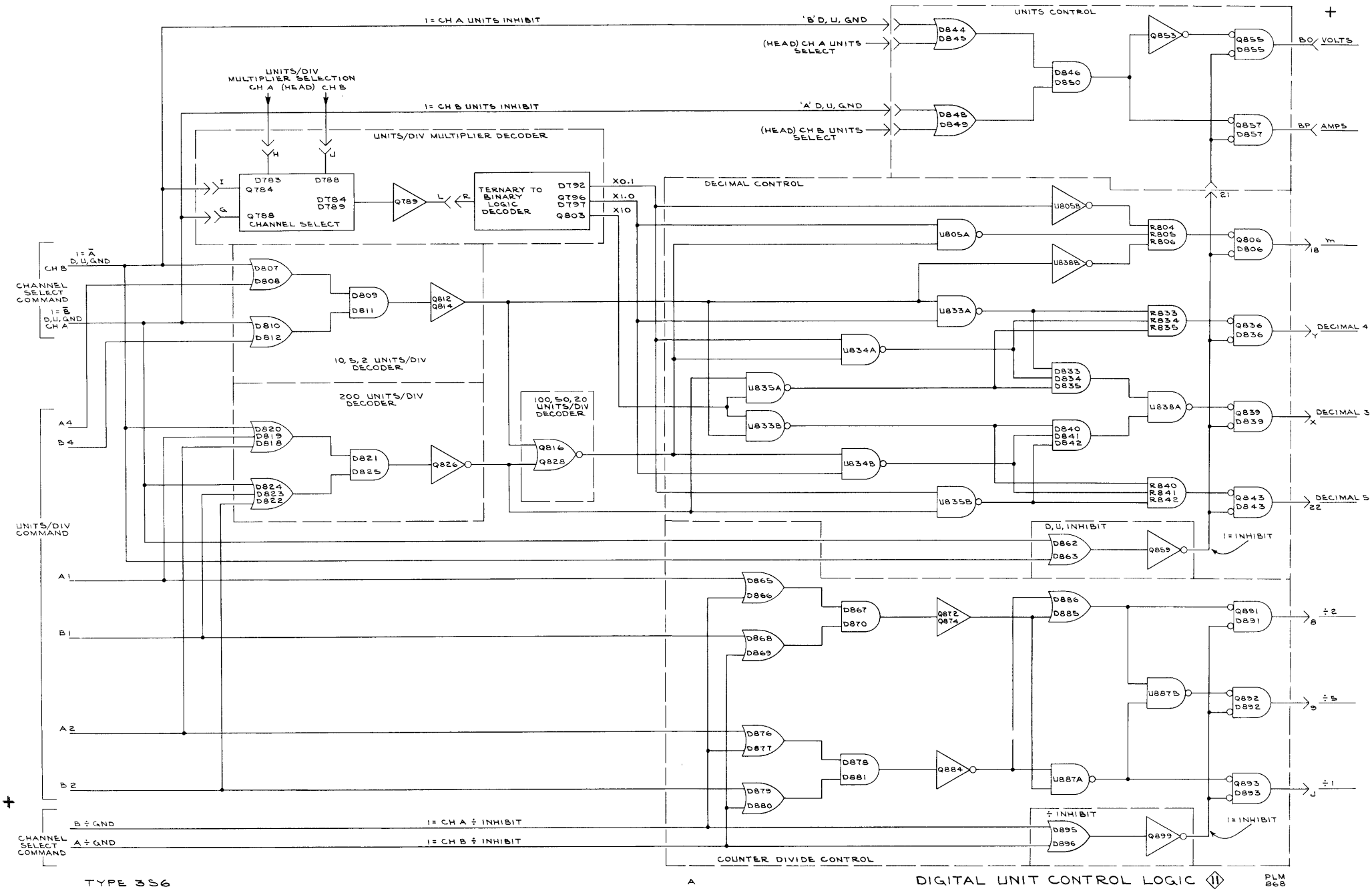



TYPE 356

CH B PROGRAMMED OFFSET 9

PLM 868


UNITS/DIV MULTIPLIER SELECTION
FROM CH A
FROM CH B
X10 = +3.4V
X1.0 = -0.68V
X0.1 = -4.4V
TOP VIEW OF INTEGRATED CIRCUITS
* SEE FIG. 5-1.
PARTIAL VERTICAL BOARD
UNITS/DIV MULTIPLIER DECODER
PARTIAL OUTPUT BOARD
UNITS CONTROL
10, 5, 2 UNITS/DIV DECODER
200 UNITS/DIV DECODER
100, 50, 20 UNITS/DIV DECODER
DECIMAL CONTROL
COUNTER DIVIDE CONTROL
PARTIAL LOGIC CARD
VOLTS
AMPS
DECIMAL 4
DECIMAL 3
DECIMAL 5
D, U, INHIBIT
÷INHIBIT
1=INHIBIT
1=CH B ÷ INHIBIT
1=CH A ÷ INHIBIT
FROM VERTICAL MODE SWITCH SW450A
* SWITCH CLOSED ONLY WHEN VARIABLE IS IN DETENT
REFERENCE DIAGRAMS
1 CH A PROGRAMMED AMP & ATTENUATORS
2 CH A MEMORY
7 GATE GENERATORS
13 CARD CONNECTORS & DECOUPLING NETWORKS
14 VERTICAL MODE SWITCH & PROGRAM CONNECTORS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 356
A
DIGITAL UNIT CONTROL 10
PLM 868

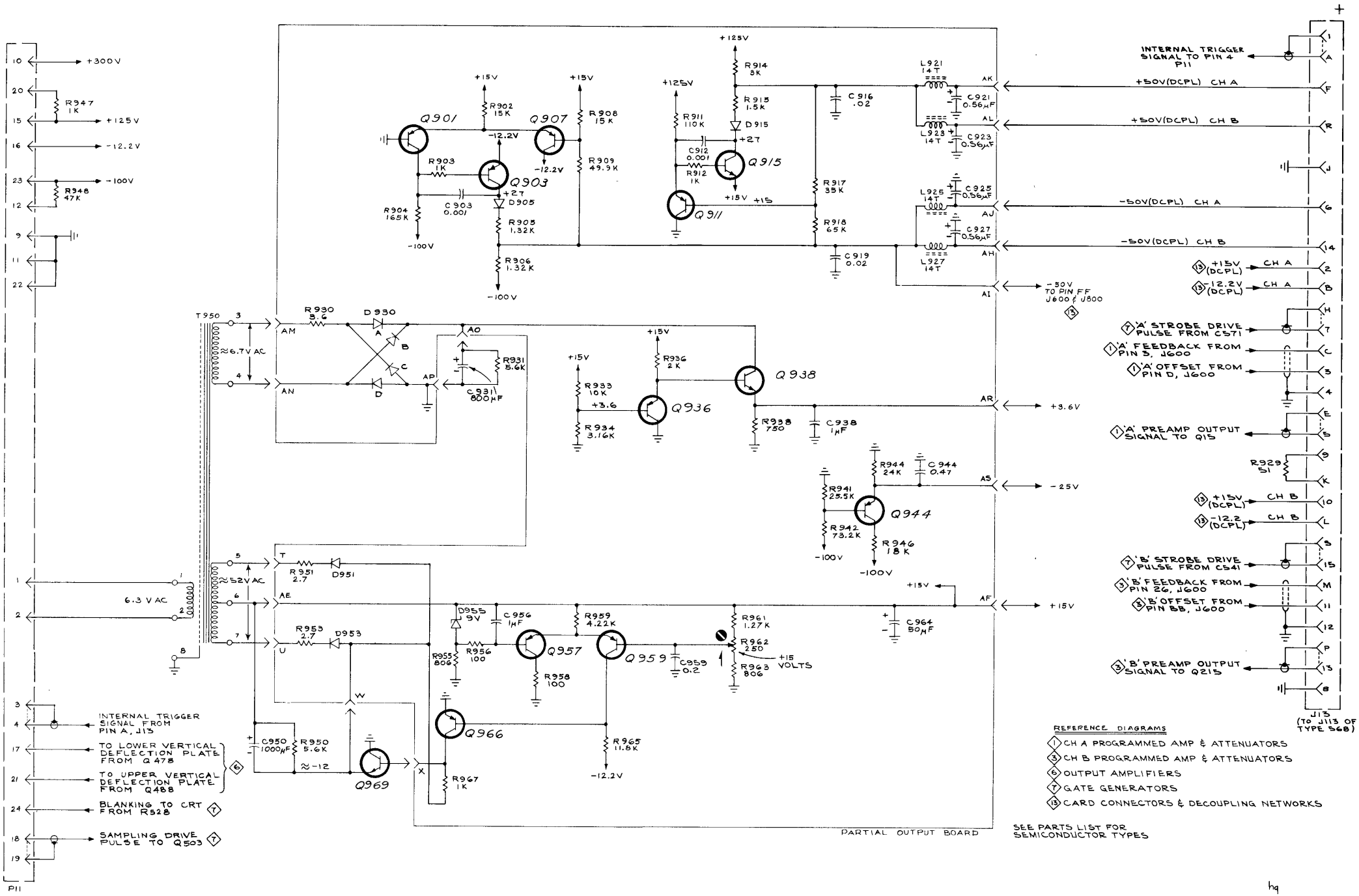


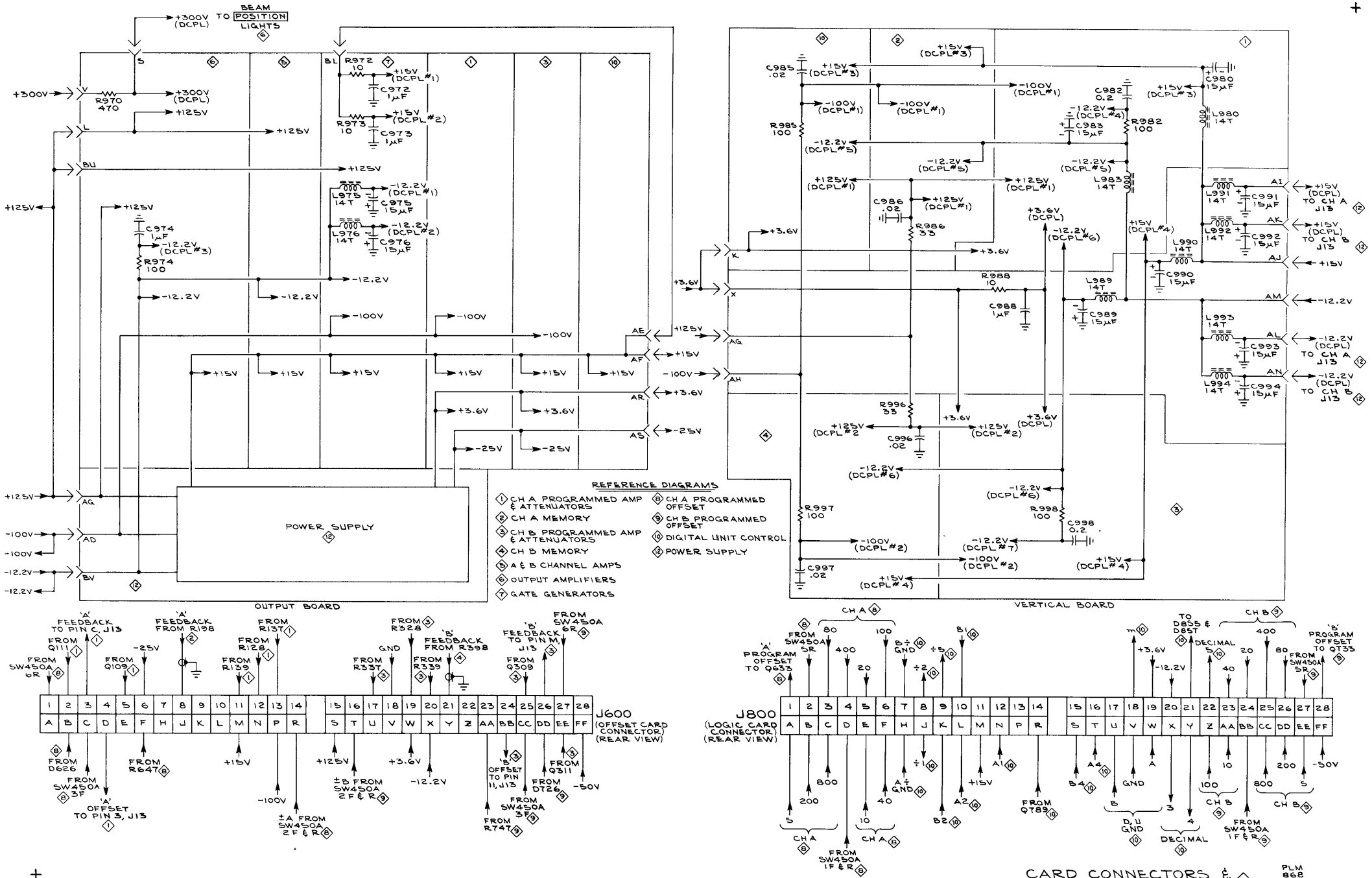

TYPE 356

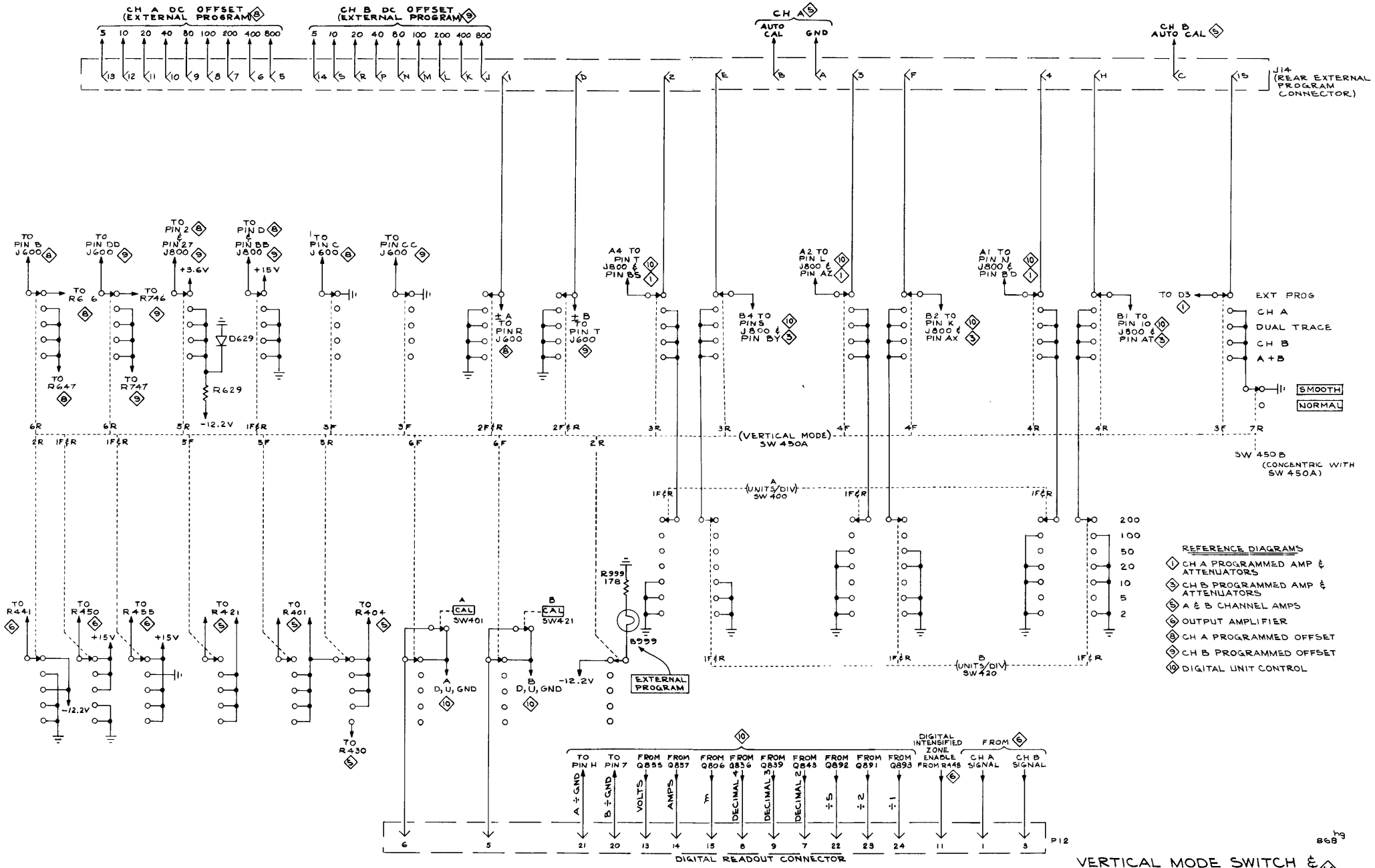
A

DIGITAL UNIT CONTROL LOGIC

PLM 868


+300V
+125V
-12.2V
-100V
R947 1K
R948 47K
Q901
Q903
Q907
Q911
Q915
R902 15K
R903 1K
R904 165K
C903 0.001
D905
R905 1.32K
R906 1.32K
R908 15K
R909 49.9K
R911 110K
R912 1K
C912 0.001
D915
R914 3K
R915 1.5K
R917 35K
R918 65K
C916 .02
C919 0.02
L921 14T
L923 14T
L925 14T
L927 14T
C921 0.56µF
C923 0.56µF
C925 0.56µF
C927 0.56µF
INTERNAL TRIGGER SIGNAL TO PIN 4 P11
+50V(DCPL) CH A
+50V(DCPL) CH B
-50V(DCPL) CH A
-50V(DCPL) CH B
-50V TO PIN FF J600 & J800
+15V (DCPL) CH A
-12.2V (DCPL) CH A
'A' STROBE DRIVE PULSE FROM C571
'A' FEEDBACK FROM PIN 3, J600
'A' OFFSET FROM PIN D, J600
'A' PREAMP OUTPUT SIGNAL TO Q15
+15V (DCPL) CH B
-12.2 (DCPL) CH B
'B' STROBE DRIVE PULSE FROM C541
'B' FEEDBACK FROM PIN 26, J600
'B' OFFSET FROM PIN BB, J600
'B' PREAMP OUTPUT SIGNAL TO Q215
J13 (TO J113 OF TYPE S68)
T950
≈6.7V AC
≈52V AC
6.3 V AC
R930 3.6
D930
R931 5.6K
C931 800µF
R933 10K
R934 3.16K
Q936
R936 2K
Q938
R938 750
C938 1µF
+3.6V
R941 25.5K
R942 73.2K
Q944
R944 24K
C944 0.47
R946 18K
-25V
R951 2.7
D951
R953 2.7
D953
D955 9V
C956 1µF
R955 806
R956 100
R958 100
Q957
R959 4.22K
Q959
C959 0.2
R961 1.27K
R962 250
R963 806
+15 VOLTS
C964 50µF
+15V
Q966
Q969
R965 11.8K
R967 1K
C950 1000µF
R950 5.6K
≈-12
INTERNAL TRIGGER SIGNAL FROM PIN A, J13
TO LOWER VERTICAL DEFLECTION PLATE FROM Q478
TO UPPER VERTICAL DEFLECTION PLATE FROM Q488
BLANKING TO CRT FROM R528
SAMPLING DRIVE PULSE TO Q503
P11
PARTIAL OUTPUT BOARD
REFERENCE DIAGRAMS
1 CH A PROGRAMMED AMP & ATTENUATORS
3 CH B PROGRAMMED AMP & ATTENUATORS
6 OUTPUT AMPLIFIERS
7 GATE GENERATORS
13 CARD CONNECTORS & DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES


BEAM POSITION LIGHTS
+300V (DCPL)
R970 470
+125V
R972 10
+15V (DCPL#1)
C972 1µF
R973 10
+15V (DCPL#2)
C973 1µF
L975 14T
-12.2V (DCPL#1)
C975 15µF
L976 14T
-12.2V (DCPL#2)
C976 15µF
C974 1µF
-12.2V (DCPL#3)
R974 100
-12.2V
-100V
AE
AF
AR
AS
+3.6V
-25V
AG
AD
AV
POWER SUPPLY
OUTPUT BOARD
REFERENCE DIAGRAMS
1 CH A PROGRAMMED AMP & ATTENUATORS
2 CH A MEMORY
3 CH B PROGRAMMED AMP & ATTENUATORS
4 CH B MEMORY
5 A & B CHANNEL AMPS
6 OUTPUT AMPLIFIERS
7 GATE GENERATORS
8 CH A PROGRAMMED OFFSET
9 CH B PROGRAMMED OFFSET
10 DIGITAL UNIT CONTROL
12 POWER SUPPLY
C985 .02
+15V (DCPL#3)
-100V (DCPL#1)
R985 100
-12.2V (DCPL#5)
+125V (DCPL#1)
C986 .02
R986 33
+3.6V (DCPL)
C982 0.2
-12.2V (DCPL#4)
C983 15µF
R982 100
L980 14T
L983 14T
+15V (DCPL#4)
L990 14T
C990 15µF
L989 14T
C989 15µF
R988 10
C988 1µF
L991 14T
C991 15µF
+15V (DCPL) TO CH A J13
L992 14T
C992 15µF
+15V (DCPL) TO CH B J13
L993 14T
C993 15µF
-12.2V (DCPL) TO CH A J13
L994 14T
C994 15µF
-12.2V (DCPL) TO CH B J13
R996 33
C996 .02
R997 100
C997 .02
R998 100
C998 0.2
VERTICAL BOARD
J600
(OFFSET CARD CONNECTOR) (REAR VIEW)
'A' FEEDBACK TO PIN C, J13
FROM Q111
FROM SW450A 6R
FROM Q109
-25V
'A' FEEDBACK FROM R198
FROM R128
FROM R137
FROM R139
FROM R328
GND
FROM R337
'B' FEEDBACK FROM R398
FROM R339
'B' FEEDBACK TO PIN M, J13
FROM Q309
FROM SW450A 6R
FROM D626
FROM SW450A 3F
'A' OFFSET TO PIN 3, J13
FROM R647
+15V
-100V
±A FROM SW450A 2F & R
+125V
±B FROM SW450A 2F & R
+3.6V
-12.2V
'B' OFFSET TO PIN 11, J13
FROM R747
FROM SW450A 3F
FROM DT26
FROM Q311
-50V
J800
(LOGIC CARD CONNECTOR) (REAR VIEW)
'A' PROGRAM OFFSET TO Q655
FROM SW450A 5R
80
400
20
100
B÷ GND
÷2
÷5
B1
FROM SW450A 5R
200
800
5
CH A
FROM SW450A 1F & R
40
÷1
A÷ GND
B2
A2
+15V
A1
FROM Q789
10
CH A
TO D855 & D85T
DECIMAL
CH B
400
20
80
FROM SW450A 5R
'B' PROGRAM OFFSET TO Q735
+3.6V
-12.2V
A4
B4
GND
A
B
D, U GND
3
4
DECIMAL
100
CH B
800
5
CH B
FROM SW450A 1F & R
-50V
CARD CONNECTORS & DECOUPLING NETWORKS 13
PLM 868
TYPE 356
A




TYPE 356

A

868 hg

VERTICAL MODE SWITCH & PROGRAM CONNECTORS 14