INSTRUCTION MANUAL

Serial Number B0 40856

TYPE 3S2 SAMPLING UNIT

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070-0759-00

Fig. 1-1. Type 3S2 Sampling Unit.

SECTION 1
SPECIFICATION

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

The Type 3S2 Sampling Unit is a dual-channel vertical amplifier plug-in unit designed for operation in any one of the Tektronix Type 560-Series Oscilloscopes except the Type 561 (it will operate in the Type 561A). The Type 3S2 accepts "S" Series sampling heads. The sampling heads determine the input characteristics of the sampling unit and the availability of the trigger pickoff.

The Type 3S2 will operate with any Tektronix 3T-series sampling unit. The Type 3T2 Random Sampling Sweep is recommended, because it can display the triggering event without a pretrigger or signal delay line. Conventional or real time 2B- or 3B-series time-base units include the Types 2B67, 3B1, 3B4 and the 3B5 non-digital time bases, and the Type 3B2 Analog/Digital Time Base Unit. The Type 3S2 provides the vertical information needed for voltage measurements by Tektronix digital readout systems, such as the Type 567-Type 6R1A, or the Type 568-Type 230.

One or two "S" Series sampling heads can be plugged into the Type 3S2, or used remotely on an optional extender cable unit. The Type 3S2 provides the power for the sampling heads.

Interconnections to the circuits in the sampling heads are provided by connectors in the sampling head compartments of the Type 3S2.

If a trigger pickoff is provided in the sampling head, the Type 3S2 provides a trigger selection circuit and returns a portion of the input signal to the front panel for externally triggering a sampling sweep unit. An internal reconstructed signal is provided to trigger the real-time time-base.

Sampled signals are presented to both the oscilloscope CRT and to the front panel connectors for external use with auxiliary equipment such as pen recorders. The two Channels may be displayed either individually or in one of three combined modes: DUAL-TRACE, A+B (Algebraic addition), or a VERT/B HORIZ (X-Y). The A VERT/B HORIZ (X-Y) mode does not apply in real time operation.

ELECTRICAL CHARACTERISTICS

Digital Unit Compatibility

The Type 3S2 is compatible for operation with all Type 230 Digital Units and all Type 6R1A Digital Units. It is compatible with all Type 6R1 Digital Units SN 695 and up. The Type 6R1 Digital Units SN 101-694 require the installation of Tektronix Modification Kit 040-0342-00 when operating with a Type 3S2.

The following characteristics apply over an ambient temperature range of 0°C to + 50°C. These characteristics apply only after the Type 3S2 VERT GAIN control has been properly adjusted for the oscilloscope and after a sufficient warm-up time. For particular system warm-up requirements, refer to the main frame oscilloscope instruction manual. A procedure for mating the Type 3S2 to each oscilloscope can be found in the Operating Instructions section.

The Type 3S2 meets the tolerances stated below after a 5-minute warmup.

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Deflection Factors		
Units/Div Switch Range	2 to 200 in 7 steps in a 1-2-5 sequence with Units/Div labeled on the sampling head.	
Accuracy	Within 3%, NORMAL; 6% SMOOTH	Normal sequential sampling with at least 20 samples per cycle of displayed square wave.
Units/Div VARIABLE Range	Reduction in deflection to 0.7 or less when control is turned CCW from CAL position, and 2.5 times or more increase in deflection when control is turned CW from CAL position.	
Interchannel Delay Range	At least +5 ns to −5 ns.	With two same type sampling heads plugged in, using time-coincident signals.
Loop Gain		
NORMAL	Can be set to unity with DOT RESPONSE control.	Range of DOT RESPONSE control is $\leq$0.95 to $\geq$1.05.

ELECTRICAL CHARACTERISTICS *(cont'd)*

Characteristic	Performance Requirement	Supplemental Information
SMOOTH	Loop gain is reduced to be $\leq$0.3.	Random noise in display reduced to approx ½.
Dot Slash	Vertical dot drift is $\leq$ 0.1 div when sampling sweep unit is triggered at 20 Hz.	Measure with Units/Div switch at 200 with no signal input to the sampling head.
OFFSET Output Voltage Range	+10 to −10 volts.	
Accuracy	Actual DC OFFSET Voltage is 0.1× OFFSET Output voltage within 2%.	Source Resistance 10 kΩ within 1%.
DC OFFSET Range	+1 to −1 volt[1].	
A Output, B Output Amplitude in Volts (Referred to Input)	Signal input times $\left(\frac{200}{\text{Units/Div Setting}}\right)$	Maximum output voltage ±4 V. Source Resistance 10 kΩ, within 0.5%.
Accuracy (Referred to Input)	Within 2%.	
Accuracy (Referred to CRT)	Within 3%. (200 mV/Div).	
Accuracy of Vertical Signal to Digital Unit	Within 3%.	
TRIG OUT (SN B040250-up) (with Type S-1, S-2) Amplitude (referred to the Type S-1, S-2 input)	Approximately 1× inut signal voltage into 50 Ω for AC. Approximately .1× input signal voltage into 50 Ω for DC. Coupling time constant is 5 μs. Approximately 1× for both AC and DC signals into 1 MΩ.	
Risetime	2 ns or less, 10% to 90%, into 50 Ω using 70 ps risetime input pulse	
Strobe signal in Trig Out Signal	$\leq$50 mV peak into 50 Ω	
TRIG OUT, SN B010101 to SN B030249 (with Type S-1, S-2) Amplitude (Referred to the Type S-1, S-2 input)		Approximately 0.1 × input signal voltage DC coupled into 50 Ω. Approximately 2½× input signal voltage into 1 MΩ.
Risetime	0.6 ns or less, 10% to 50%, into 50 Ω using 70 ps risetime input pulse.	
Strobe signal in Trig Out signal	$\leq$10 mV peak into 50 Ω.	
Position Indicator Lamps	One indicator lamp will be on and the other off when CRT dot is more than 4 divisions away from the graticule centerline.	
POSITION Range	$\geq$ +5 to −5 vertical divisions from the graticule center.	When DC OFFSET is set to deliver 0 V to OFFSET output jack.

[1]**Unless otherwise stated on the sampling head front panel.**

ENVIRONMENTAL CHARACTERISTICS

Storage

Temperature— −40°C to +65°C.

Altitude— To 50,000 feet.

Operating

Operating Temperature— 0°C to +50°C.

Operating Altitude— To 15,000 feet.

MECHANICAL CHARACTERISTICS

Dimensions— Height 6¼ inches

Width 4¼ inches

Length 14½ inches

Approximate dimensions including knobs and connectors.

Construction— Aluminum alloy chassis with epoxy laminated circuit boards. Front panel is anodized aluminum.

Accessories— An illustrated list of the accessories supplied with the Type 3S2 is at the end of the Mechanical Parts List pullout pages.

SECTION 4
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual contains a block diagram description and circuit description of the Type 3S2 Sampling Unit. The block diagram description is an expansion of Section 3, Basic Sampling Principles. The circuit description follows the sequence of diagrams at the back of this manual.

BLOCK DIAGRAM

Refer to Fig. 4-1 and the complete block diagram at the back of this manual during the following description. Since most of Channel A and Channel B are identical, no reference is made to either channel except where they differ. Channel A occupies the top half of the block diagram.

Both Fig. 4-1 and the complete block diagram include a simplified block of a typical sampling head. The Type 3S2 Sampling Unit serves no useful purpose by itself, but functions as part of a sampling system only when a sampling head is installed. Thus, the sampling head simplified blocks are included.

Feedback Loop and Pulse Amplifier Chain

Fig. 4-1 relates to Fig. 3-4 and Fig. 3-7. The reconstructed signal out of the Memory block (Fig. 4-1) is the first point in the Type 3S2 at which the amplitude is always a standard value of 0.5 volt per CRT vertical division. The signal between the sampling head output (TP121) and the Memory input bears no similarity to the signal at the Memory output. Under ideal conditions, there is no signal between those two points whenever the sampling head input signal is at a steady value. The Post Amplifier, AC Amplifier and Memory Gate all are part of a pulse amplifier chain that amplifies the sampling head output signal just after each sample is taken. The pulse chain signals are greatest in amplitude when the sampled signal is at its full amplitude difference from the last sample (as in using the random sampling process in the Type 3T2 Random Sampling Sweep unit).

To complete the association of Fig. 4-1 with Section 3, the following describes the operating cycle:

a. The sampling head bridge applies an error signal to the head preamp whenever there is a voltage difference at the bridge input and output terminals at sampling time. The error-signal voltage amplitude is just a few per cent of the difference (sampling efficiency), and the pulse duration out of the bridge is equal to the bridge conduction time. A small storage capacitance at the head Preamp input time-stretches the pulse so the pulse chain can amplify the error signal pulses at moderate rates of rise.

b. The time-stretched pulse is amplified by the Type 3S2 Post Amplifier and sent forward into the attenuating network made up of the NORMAL-SMOOTH switch, the DOT RESPONSE control and the Forward Attenuator portion of the Units/Div switch.

c. The AC Amplifier again amplifies the pulse and applies it to the Memory circuit during conduction time of the Memory Gate. In effect, the error signal charge applied to the head Preamp is then transferred to the feedback capacitor of the Memory circuit.

d. The Memory circuit applies its error signal-determined output voltage to both the vertical amplifier and to the feedback attenuator and sampling head bridge output terminal. Control of the input deflection factor by the Forward and Feedback Attenuators is described near the end of Section 3. The DOT RESPONSE control is also described in Section 3.

Vertical Channel Following Memory

Blocks between the Memory and the CRT include: the Inverter and the INVERT switch, the Units/Div VARIABLE control and internal Digital Gain control, the Channel Amplifier and the Output Amplifier with its input controlled by the Dual-Trace Multi. The Output Amplifier drives the indicator oscilloscope CRT vertical deflection plates directly.

The Inverter is a $\times 1$ gain inverting amplifier that is normally in the circuit. The inverter is by-passed when the INVERT switch is pulled out to invert the display.

The Channel Amplifier is a $\times 2$ gain inverting amplifier with both the Units/Div VARIABLE and Digital Gain controls in series with the signal input. The Channel Amplifier drives both the Output Amplifier and the real-time time-base unit. The signal to the real-time time-base unit is for internal triggering of a real-time sampling display.

Channel B Channel Amplifier drives the same output line to the sampling sweep unit during A VERT-B HORIZ operation. The signal then drives the horizontal deflection plate amplifier in the sampling sweep unit.

Both of the above functions require that the Horiz Plug-In Compatibility switch be placed at the correct position. See the Operating Instructions.

The Output Amplifier is a high gain inverting amplifier that drives the CRT vertical deflection plates directly. The input is from either Channel A or Channel B, selected by the Dual-Trace Multi. The multi control circuit selects one channel continuously (CH A or CH B), alternates between channels after each sample (DUAL-TRACE), or parallels the two channels and adds their signals algebraically at the summing input circuit.

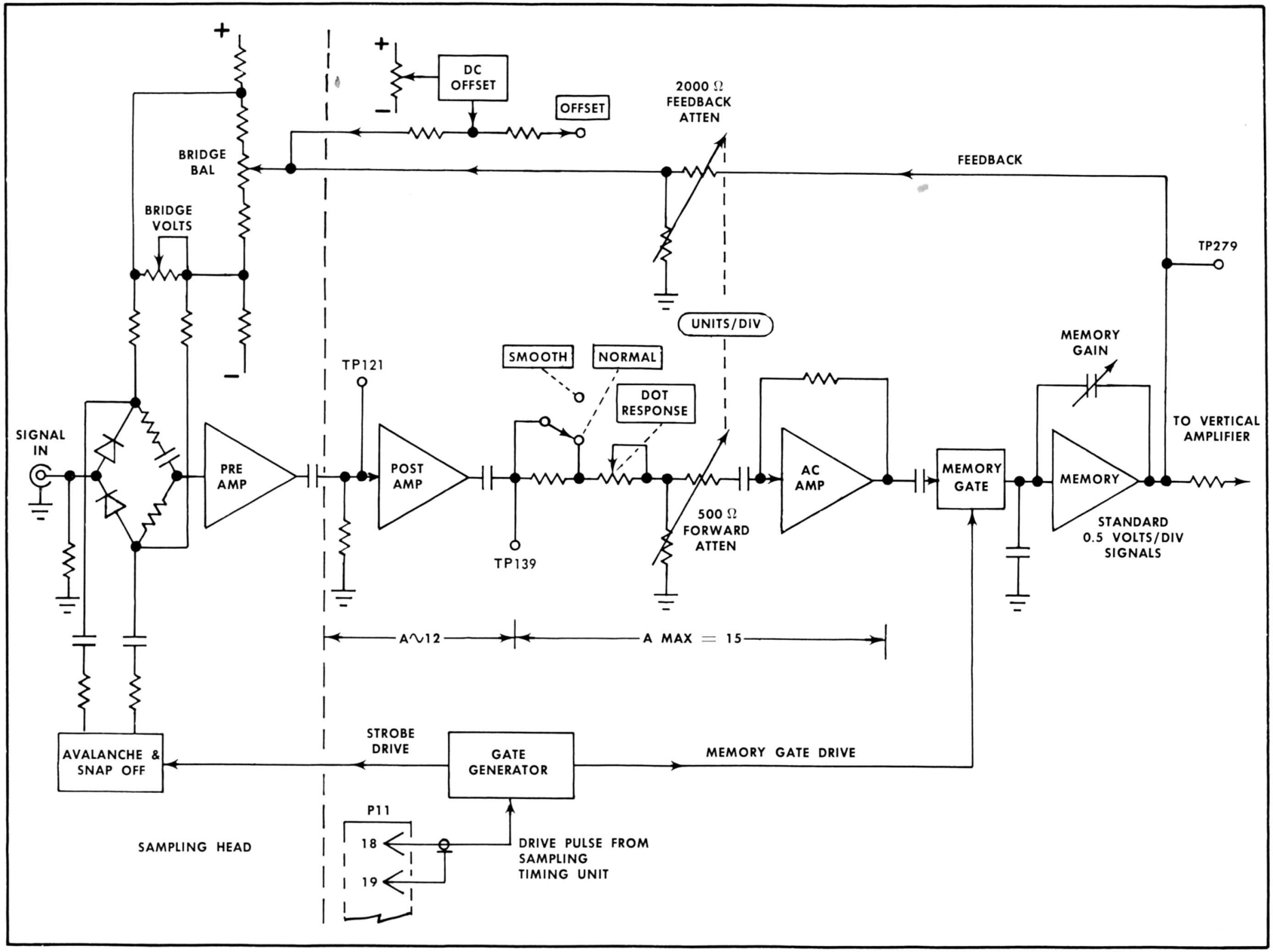


Fig. 4-1. Type 352 and sampling head feedback loop block diagram.

The Position Lamp Driver circuit monitors the DC voltage of the Output Amplifier lines and turns on the appropriate neon lamp to indicate whether the deflection voltage has placed the trace above or below the graticule.

Gate Generators

The Type 3S2 Gate Generator blocks function in two different modes: driven by the associated 3T-series sampling sweep unit, or self excited at a 100 kHz rate when the associated time base is of the 2B- or 3B-series. The function is selected by the internally mounted Horiz Plug-In Compatibility switch, SW6. When SW6 is at the Sampling position, the sampling sweep unit drives the Blocking Oscillator, which then drives the Dual-Trace Driver and both Delay & Strobe Driver blocks. When SW6 is at the Non-Sampling position, the Dual-Trace Driver oscillates and drives the Blocking Oscillator, which again drives both Delay & Strobe Driver blocks.

Sampling; 3T-Series Operation

Since the Type 3S2 will operate with several different sampling sweep units, the Gate Generator is designed to operate from slightly different Sampling Drive pulses. The Blocking Oscillator converts the normal variations in amplitude, risetime and duration of the Sampling Drive pulses to a standardized drive pulse with always the same amplitude, risetime and duration.

The Blocking Oscillator output pulse is converted to an RC ramp signal at both Delay circuits, and the (internal) A Delay and (front-panel) B Delay controls select a point along each ramp at which the Strobe Drive is generated. As the individual channel Strobe Drive is generated, the Memory Gate Driver causes the same channel Memory Gate to conduct. The duration of Memory Gate conduction is controlled by the Memory Gate Width control. Thus, a few nanoseconds after the arrival of a Sampling Drive pulse, a Strobe Drive pulse is sent to the sampling head, and the Memory Gate is driven into conduction. The instrument is calibrated so the B DELAY control alters the time of the Channel B Strobe Drive pulse approximately ± 5 ns with respect to the Channel A Strobe Drive pulse (when both sampling heads are the same type).

The Dual-Trace Driver circuit drives both the CRT blanking circuit (to extinguish the CRT beam while the dot is being moved between samples) and the Dual-Trace Multi. The Dual-Trace Multi mode of operation is not controlled by the Dual-Trace Driver, but by the Vertical Mode Switch, SW730A. If the Vertical Mode switch is at DUAL-TRACE, the Dual-Trace Driver causes the Dual-Trace Multi to change state at the time each sample is taken.

Non-Sampling; 2B, 3B-Series Operation

Non-Sampling real-time time-base units do not provide a Sampling Drive pulse to the Blocking Oscillator. Since the Type 3S2 will operate with linear sawtooth time base units, the Gate Generator must provide its own sampling Strobe Drive control.

The Dual Trace Driver is made to oscillate at 100 kHz and to drive the Blocking Oscillator, the CRT blanking circuit and the Dual-Trace Multi.

The remainder of the Gate Generator circuits function as when operating with a sampling sweep unit. The operational differences between the two types of time bases are explained in the Operating Instructions, Section 2.

Trigger Amplifier

SN B040250-Up. A trigger amplifier block shown at the left of the block diagram near the sampling heads, couples an amplified portion of the sampling head input signal to a front panel connector. The amplifier is not connected to any of the Type 3S2 sampling process circuits. The front panel TRIG OUT switch selects the head from which the trigger pickoff signal is sent to the front panel connector.

The same TRIG OUT switch selects the internal Channel Amplifier signal for internal triggering of real-time time-base units.

SN B010101-B030249. Trigger amplifiers in this serial number range deliver a signal approximately 0.1 times the sampling head input signal.

A trigger amplifier block shown at the left of the block diagram near the sampling heads, couples a portion of the sampling head input signal to a front panel connector. The amplifier is not connected to any of the Type 3S2 sampling process circuits. The front panel TRIG OUT switch selects the head from which the trigger pickoff signal is set to the front panel connector.

The same TRIG OUT switch selects the internal Channel Amplifier signal for internal triggering of real-time time base units.

CIRCUIT DESCRIPTION

The following circuit description sequence follows the order of the diagrams in section 9.

Post Amplifiers & Attenuators

The Post Amplifier and Attenuators diagram includes Post Amplifiers for both channels, as well as Forward and Feedback attenuators, DC Offset and the common Trigger Amplifier. Where the two channels are identical, the operation of only one is described. Differences between the channels are discussed in detail.

The Trigger Amplifier SN B040250-Up, consists of the front panel TRIG OUT switch and TRIG OUT connector, transistors Q103, Q104, Q113 and Q114, and associated components. Q103 and Q113 are connected as common-base, amplifiers, with only one conducting at a time. The TRIG OUT switch selects the conducting transistors, Q103 for Channel A or Q113 for Channel B.

The signal input at J101 and J111 from a sampling head trigger pickoff circuit is approximately 0.1 of the input signal to the sampling head. A total AC gain of about 10 in the trigger amplifier causes the TRIG OUT connector signal to be about equal in amplitude to the sampling head input signal, within the bandpass limitations of the amplifier and when loaded by 50 Ω. Total DC gain into 50 Ω is about 0.075, and into 1 MΩ it is about 1.

Assume the TRIG OUT switch is at A. Then all the current from the channel B sampling head tirgger pickoff circuit

and R113 passes through D113 and R115 to ground; Q113 is cut off because its base voltage is +1.7 V and its emitter voltage is +1.5 V, 0.2 volt reverse biased.

The signal entering at J101 is in phase with the sampling head input signal. Q103 does not invert the signal, but both Q103 and Q114 do invert it (total of two invertions), making the TRIG OUT signal in phase with the sampling head input signal. D103 is reverse biased because C106 charges to a positive value equal to the most positive signal value that enters J101, minus about 0.5 V drop across D103. C106 charge has no leakage path, thus D103 reverse bias effectively disconnects R105, C106 and the lead to the TRIG OUT switch from the trigger amplifier input.

R101 raises Q103 emitter input resistance to provide a nominal 50 Ω termination to the coaxial cable feed line from the sampling head. Q103 collector circuit is DC coupled to Q104 base, with the main current path through R104, L104 and D104 which is bypassed by C104. D104 serves to temperature compensate Q104 so its collector DC voltage does not shift appreciably with temperature changes.

Q104 and Q114 form a stabilized feedback amplifier that has its DC gain set by the potentiometric ratio of R108-R109. The AC gain is higher for high frequencies due to the feedback bypass capacitor C108. (Both C108 and L104 aid to assure the total amplifier high frequency gain-bandwidth product is at high as possible.)

Q114 emitter has two bypass capacitors that aid to keep the gain high. C118 bypasses the very high frequencies and C117 bypasses the lower frequencies.

Q114 collector output is RC coupled to the TRIG OUT connector by R110 and C110. C110 assures that the low AC impedance at Q114 collector is coupled to the output connector. The output RC circuit has a 5 μs time constant. Low AC impedance occurs at Q114 collector due to the feedback path through R109. When Q114 collector moves (due to the signal) a current through R109 limits the gain. However, if some of Q114 collector signal current is required by the TRIG OUT load, that current does not get back through R109 effectively turning the output current on harder. Thus Q104-Q114 feedback amplifier output at Q114 is a very low impedance signal source.

The amplifier contains two power supply decoupling networks. R110-C110 decouple the +15-V supply from current pulses within the amplifier. R119-C119 decouple the −12.2 V supply from current pulses at the amplifier output. R114 isolates the decoupled +15-V supply from the Q104-Q114 feedback amplifier.

The active transistor will be forced to conduct significant base current when the sampling head is removed from the Type 3S2, but no damage occurs. The open circuit output voltage rises from about +0.1 V (no signal value) to about +0.8 V when there is no sampling head connected to the active trigger amplifier.

The Trigger Amplifier, SN B010101-B030249 consists of front panel TRIG OUT switch and TRIG OUT connector, transistors Q103 and Q113, and associated components. The transistors are connected as a common-base amplifier, but only one conducts at a time. The TRIG OUT switch selects the conducting transistor, Q103 for Channel A or Q113 for Channel B.

Fig. 4-2 is a schematic of only the Channel B portion of the Trigger Amplifier. Included is the signal input connection from a sampling head trigger pickoff circuit (Q17), and operating voltages. The supply voltages listed are values at the output side of power supply decoupling circuits located on the Trigger Amplifier circuit board.

Approximately 6 mA of current passes through the active transistor, as selected by the TRIG OUT switch. If the TRIG OUT switch is placed at A, D113 in series with R115 take all the current otherwise taken by Q113. Note the two voltages at Q113 emitter. Note also that when inactive, the transistor is reverse biased 0.2 volt. When the TRIG OUT switch is at B, Q113 is active and delivers an in-phase signal to the TRIG OUT connector through R114.

Fig. 4-2 shows −2.5 volts at the TRIG OUT connector. This is true only when the connector is loaded by 1 MΩ. When loaded by 50 Ω, the output voltage is −0.1 volt, but the static state DC currents within the circuit are not significantly altered.

Total circuit gain includes the characteristics of the associated sampling head. When the head is either a Type S-1

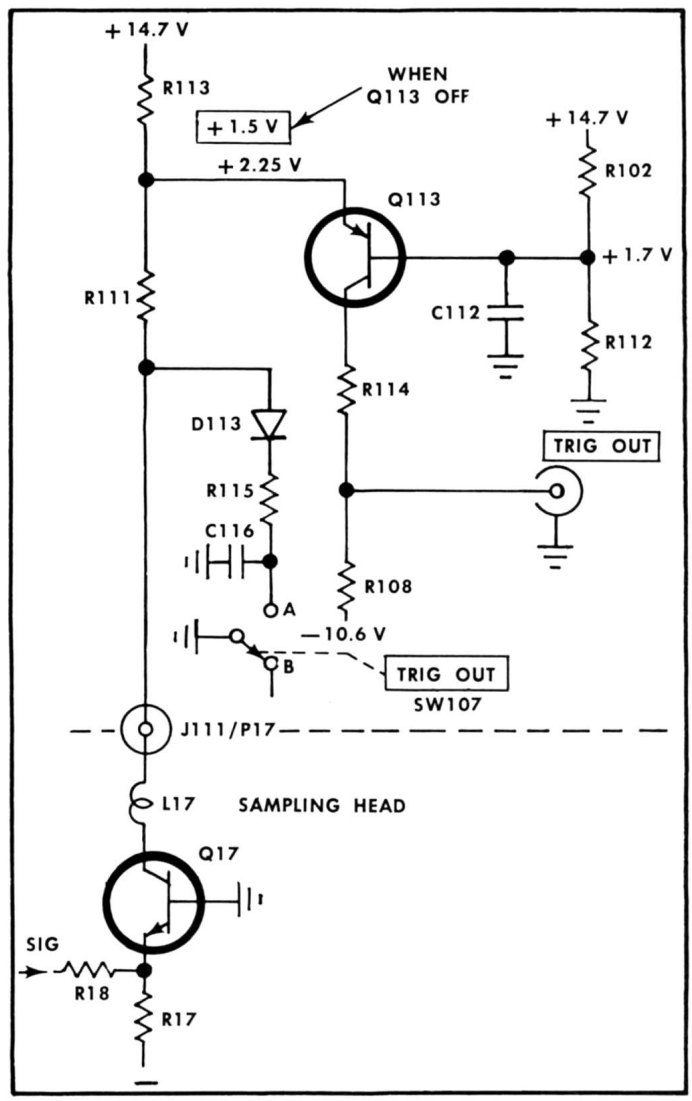


Fig. 4-2. Channnel B Trigger circuit connections.

or Type S-2, and when the TRIG OUT connector is loaded by 50 Ω, the gain is approximately 0.1, so signal output amplitude is 10% of that at the sampling head input connector. When the TRIG OUT connector is loaded by 1 MΩ, the gain is about 2.5 times the signal at the sampling head input connector. The frequency response is related to typical gain-bandwidth product, and the amplifier upper frequency limit is the highest when loaded by 50 Ω.

The active transistor will be forced to conduct significant base current when the sampling head is removed from the Type 3S2, but no damage occurs.

The Post Amplifiers are two-stage non-inverting operational amplifiers with AC coupled complementary emitter followers between the second stage and the output. The input impedance is 90 Ω, which properly terminates the coaxial cable feed from the sampling head. Output impedance is very low to provide signal current to the 50 Ω Forward Attenuator. Total AC gain is approximately 12, producing a 2.4 volt output signal for a 0.2 volt input signal. DC gain is essentially unity and feedback keeps the amplifier within its proper dynamic range.

Q123 and Q128 (channel A) are the amplifier transistors, and Q133 and Q136 are the output emitter followers. Q133 assures low output impedance for positive output signals, and Q136 assures low output impedance for negative output signals. Each emitter follower has a resistor in the collector for parasitic oscillation suppression. C134 permits the output emitters to be at different DC voltages and also assures that the emitter of the non-driving transistor follows the output voltage.

Output of the Post Amplifier is AC coupled to the NORMAL-SMOOTH switch, the DOT RESPONSE control and the Forward Attenuator (part of the Units/Div switch).

The Forward Attenuation Network consists of the NORMAL-SMOOTH switch, the DOT RESPONSE control, and the Forward Attenuator portion of the Units/Div switch.

Changing the NORMAL-SMOOTH switch to SMOOTH introduces R141 in series with the Post Amplifier output signal, reducing the loop gain to 0.3 or less compared to loop gain in the NORMAL Position.

The Forward Attenuator, made up of resistors R145A through R145G, presents a constant 500 Ω load to the driving side. The output resistance to the AC Amplifier changes from 1 kΩ to 100 kΩ in seven steps. Six of the seven resistors are always in parallel connection to ground, with the seventh in series with the signal to the AC Amplifier input. Signal pulse amplitude across the 500 Ω to ground does not change when the Units/Div switch position is changed. No attenuation occurs because the output series resistor is actually the input resistor to the feedback type AC Amplifier. The Forward Attenuator is called an attenuator because it affects the signal amplitude as it passes through the pulse chain from Post Amplifier to Memory input. Fig. 4-3 shows the full forward attenuator network and identifies the AC Amplifier input terminal. Change in signal amplitude at the AC Amplifier output is thus not actually attenuation, but a change in gain. The gain is controlled by the ratio of feedback resistor R215 to the value of the series element of R145. The AC Amplifier gain changes from 15 at 2 units/div to 0.15 at 200 units/div.

The Forward Attenuator portion of the Units/Div switch is ganged with the Feedback Attenuator portion. The result is that changing the Units/Div switch does not change the dot response (or loop gain). Changing either the NORMAL-SMOOTH switch or the DOT RESPONSE control changes only the forward signal, and thus does change the loop gain.

The Feedback Attenuator and DC Offset are connected together within the sampling head where they are combined and applied to the Sampling Bridge output terminals. The Feedback Attenuator receives the Memory circuit output signal from a very low impedance. The attenuator places one of seven resistors in series with the Memory output signal, and the other six resistors paralleled to ground as slightly more than 2000 Ω. Maximum attenuation (at 2 Units/Div) allows 0.42% of the Memory signal to pass to the Sampling Bridge circuit. Mimimum attenuation (at 200 Units/Div) allows 42% of the Memory signal to pass to the Sampling Bridge Circuit. The attenuation of 0.42% and 42% is corrected to exactly 0.40% and 40% by the parallel value of R148, R149 and 53 kΩ to ground inside the sampling head. (The Forward Attenuator ratio or AC Amplifier gain ratio of 100:1, and the feedback attenuator ratio of 1:100 assure that the loop gain is not altered throughout the Units/Div switch range).

Each channel DC Offset circuit is a single transistor emitter follower that converts the fairly high resistance of the DC OFFSET control to a fairly low resistance at the emitter. Q155 emitter voltage follows the voltage of the arm of the DC OFFSET control, offset by —0.6 volt. Q155 drives a 22.4 kΩ resistive load, consisting of Q155 output resistance, R158 19.1 kΩ and 2000 Ω of the Feedback Attenuator. Thus the DC OFFSET voltage at Q155 emitter develops a fixed voltage across the Feedback Attenuator 2000 Ω regardless of the Units/Div switch setting.

Memory Diagram

The Memory diagram applies to both channels of the Type 3S2. The diagram shows the 200-series circuit numbers of Channel A. Corresponding components in Channel B are numbered 500 through 599. Channel B pin connectors are lettered in blue. The diagram includes the AC Amplifier, the Memory Gate, the Memory Amplifier and the Inverter.

The AC Amplifier (whose gain is described above with the Forward Attenuation Network) is an inverting operational amplifier with AC coupled complementary emitter followers at the output. Q203 is the voltage amplifier, Q211 emitter follower adds current gain to Q203 collector signal, and Q223-Q224 provide the very low output resistance.

The amplifier input is AC coupled by C201 to permit the amplifier DC operating voltages to be independent of the changes made in input resistance by the Units/Div switch. Q203 base is the summing input terminal of the operational amplifier. As a signal arrives and changes the base voltage, the collector voltage changes in the opposite direction and Q211 emitter drives current of the opposite polarity through R215 back to the Q203 base. The input and feedback signal currents are equal, keeping the base voltage almost constant. The output signal is coupled to the Memory Gate by Q223, Q224 and R229, C229. R229 limits the signal output current assuring that C229 does not receive a significant charge for output signals of high pulse amplitude.

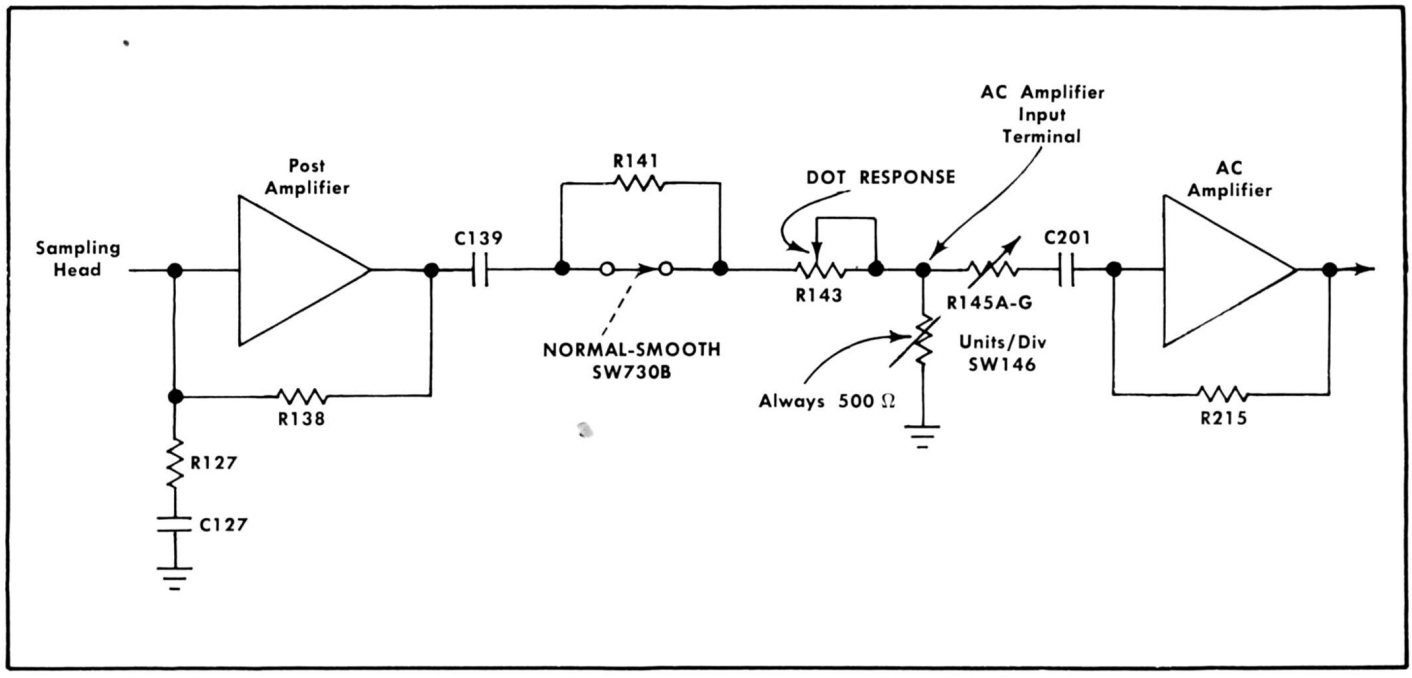


Fig. 4-3. Forward Attenuation network, showing that the output resistor of the Units/Div Forward Attenuator is actually the AC Amplifier input resistor.

The two diodes provide protection when transistors are removed from their sockets. D201 conducts if Q211 is removed, and D209 conducts if Q203 is removed. Parasitic suppressing resistors include R207, R210, R219, R221 and R225.

The Memory Gate is a special pulse driven diode gate that assures a very high input resistance to the Memory Amplifier except for about 0.15 to 0.20 μs at the time of each sample. During the conduction time, the Memory Gate is a low impedance that allows the AC amplifier to introduce a charge into the Memory Amplifier.

Fig. 4-4 is a detailed block diagram of the circuits on the Memory diagram. The Memory Gate is represented by a resistor, a coil and a relay switch. The resistor is the parallel value of the four biasing resistors which assure that the four gating diodes are normally not conducting. This equivalent circuit shows that the Memory Amplifier input is zero volts when there is no error signal at sample time.

Looking from the Memory Gate output toward its input, the four gating diodes are normally reverse biased by the voltage of Zener diode D231. (Two of the four diodes provide very high reverse biased leakage resistance, although they don't turn off very fast. The other two turn off fast at the end of the gating pulse, although they don't provide high resistance when reverse biased). D231 voltage is balanced to ground by R232 and R233 so D236 cathode rests at +2.5 volts and D238 anode rests at —2.5 volts. C231 assures that the AC Amplifier output signal drives both sides of the memory gate diodes.

The gate diodes are forward biased into conduction by T235 at the time of each sample due to the drive pulse from the Memory Gate Driver. T235 is a toroidal transformer specially wound to balance capacitive and inductive coupling to the two secondary windings. The winding with only one end connected provides the capacitive balance. The magnetic toroid core provides the inductive balance. Thus, the drive pulse is converted to identical drive signals to assure that the output junction of the four diodes accurately divides the 5 volts of D231-C231. This places the junction of D237-D239 at ground when no error signal is applied from the AC Amplifier. The Functions of the two limiting diodes D232-D233, and the Memory Gate, are discussed in the Memory Amplifier description next. R236, R238 and D234 are shunt damping loads to T235 which minimize self-inductance ringing when the memory gate drive pulse ends.

The Memory Amplifier is an integrating operational amplifier with special low leakage (high DC resistance) input circuit. The input and feedback components are capacitors, making the AC input impedance very low. The internal high gain assures a very low output resistance; so that as long as there is no change at the input, the output DC voltage remains stable. The input low leakage circuit has no DC connection to ground except during the time the Memory Gate conducts.

The Memory Amplifier is specially decoupled from the power supplies because the output stage (Q261 and Q266) can require a current pulse as great as 30 mA for a 20 volt output change at sample time. The decoupling networks are: R241-C241, R261-C261 and R267-C267. L298, in the output lead to the INVERT switch, presents a high impedance to the Memory output for high frequency (fast change) signals. The inductor assures that the output amplifier does not have to provide high current to the output load. L298 slows the output signal response, but at a time when the CRT is blanked.

A dual junction FET (Q243) is the input stage. It is biased for essentially no leakage at the input gate, and the stage has high voltage gain at the in-phase output drain lead. Any

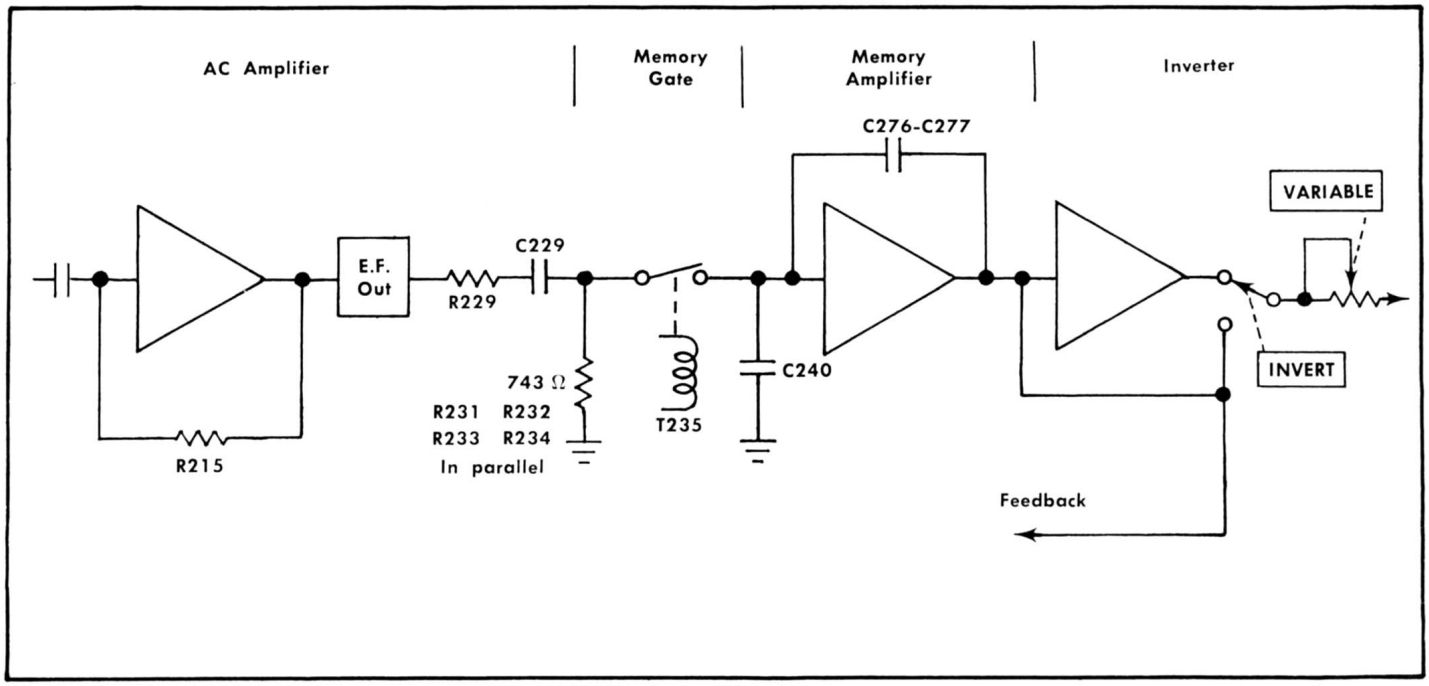


Fig. 4-4. Basic Memory Gate circuit between AC Amplifier and Memory Amplifier. (Detailed block of Memory diagram.)

voltage change at Q243A gate lead is amplified and applied to the inverting amplifier Q252. Q252 collector circuit applies proper bias to both bases of the output complementary emitter follower pair, Q261-Q266 and restores the DC level negatively so a zero input signal (at Q243A) is also a zero output signal. Q252 collector and Q261-Q266 output lead operate linearly through the range of +10 to −10 volts.

Because of the high open-loop gain, the Memory Amplifier does not have the fast risetime that the prior amplifiers have. The AC Amplifier output pulse duration is shorter than the Memory Amplifier risetime. C240 at Q243 input gate lead accepts some of the charge from the AC Amplifier, stores it until the Memory Amplifier can respond, and then loses the charge again due to feedback current.

A cycle of operation at sample time takes the following sequence:

a. The Memory Gate drive pulse arrives at essentially the same time the Sampling Bridge is strobed into conduction. Propagation delay through the three AC coupled amplifiers is quite short. The CRT is blanked at the same time. (The fact that the Memory Amplifier input is always at zero volts, and the Memory Gate is balanced around zero volts, prevents any false changes in C276-C277 charge. Therefore, there is no change in the Memory Amplifier output voltage during the time the Memory Gate conducts ahead of the arrival of the AC Amplifier output signal).

b. The AC Amplifier applies a pulse signal through R229-C229 and the Memory Gate to the Memory Amplifier input. C240 accepts some of the charge until the amplifier begins to respond, driving an equal and opposite current back to the input through the feedback capacitors.

c. Since the AC Amplifier output signal is applied to the Memory Amplifier "virtual signal ground" input, C229 receives about 10% of the total error signal charge before the Memory Gate stops conducting. Thus, as the AC Amplifier output returns to its quiescent voltage, the output side of C229 overshoots. The 743 Ω of the Memory Gate discharges C229 well in advance of the next error signal.

If the Type 3S2 is displaying a single transition step over the full graticule with the display starting at the lower left and ending at the upper right, the error signal is very large during retrace. Such large error signals (even during random process sampling) apply a significant charge to C229. Then the overshoot at the end of the error signal pulse is large enough to cause one side of the Memory Gate to conduct, and remove some of the intended charge in the feedback capacitors. Two normally non-conducting clamp diodes prevent such undesired removal of memory charge. D232 and D233 help to discharge C229 if it receives too great a charge during the Memory Gate conduction time, thus preventing false amplitude displays. These two diodes do not conduct at any other time.

d. As the Memory Gate drive pulse ends, C240 charge is removed by the Memory Amplifier feedback. This causes the Memory output voltage to continue changing toward proper amplitude for a short period of time after the Memory Gate stops conducting. As soon as C240 charge is returned to normal, the output voltage remains fixed until the next sample.

The actual resting voltage at Q243A gate may not be precisely zero, but it is within a few millivolts of zero. Any deviation from zero can be due to several things: slight differences in conduction of the Memory Gating diodes; slight differences in resistance of the four Memory Gate biasing resistors; some small error signal being generated at each sample time even when the sampling head input signal is zero. Q243B gate voltage is adjusted over a small range to allow the above normal variations. Adjustment of Q243B gate voltage is called the Smoothing Balance adjustment, because it is set so there is no change in Memory

Amplifier output when the forward attenuation is changed. The forward attenuation is changed by changing the NORMAL-SMOOTH switch between its two positions. Whatever small zero-input error signal may exist in the system it always has an average value that will not alter the memory stored charge. Changing the forward attenuation changes the peak amplitude of the residual error signal, but not its average voltage zero value. Therefore, Q243 gate voltage is adjusted to equal the average voltage zero value of the residual error signal, and the trace does not move when changing the NORMAL-SMOOTH switch position.

Memory output voltage limits of about +10 and —10 are set by two diodes in parallel with the feedback capacitors. The diodes, D276 and D277 are reverse biased by 9 volts each. If the output tries to go more positive than about +10 volts, D277 conducts (9 + 0.6 = 9.6 volts) reducing the amplifier gain to much less than 1. If the output tries to go more negative than about —10 volts D276 conducts, reducing the amplifier gain to much less than 1. The clamping diodes prevent the amplifier transistors from saturating at the time of an overdrive signal, and thus assure fast response away from the clamped voltage at the next sample.

The amplifier contains two protective diodes that conduct only when a transistor is removed from its socket. D243 prevents Q243 source leads from having to withstand —100 volts when it is plugged into its socket while the power is on. D252 protects Q252 base-emitter junction in the event Q243 is removed from its socket while the power is on.

Temperature compensation of the amplifier is accomplished effectively by the source-coupled FET input amplifier and D254 and D256. The two identical halves of Q243 compensate each other so their total current does not change with temperature change. D254 and D256 have junction-drop temperature coefficients similar to Q261 and Q266 base-emitter junctions, and thus stabilize the output circuit.

The Memory Amplifier drives the front panel vertical output jack through a resistive attenuator that delivers 40% of the memory signal through 10 kΩ. The jack is labeled A or B VERT OUTPUT, 0.2 V/DIV, 10 kΩ. The memory output signal is the standard deflection signal mentioned in Section 3, and is 0.5 volt/CRT division. The memory also drives an ×1 gain inverting amplifier, the Inverter, because the rest of the vertical amplifier stages (Channel Amplifier and Output Amplifier) invert the signal to the CRT.

NOTE

The Memory output limits of ±10 volts at 0.5 V/div equals 40 CRT divisions of display area, required when operating at high sensitivity and many divisions of DC OFFSET. The whole pulse amplifier chain is designed for full response and fast recovery so that on-screen displays have accurate deflection factors and DC offset reference. Such operation provides accurate signals at the front panel Vert Output jacks, even through much of the signal is not displayed on the 8 division CRT.

The Inverter Amplifier is a temperature compensated DC coupled operational amplifier with a gain of 1. R280 and R288 (0.1% tolerance resistors) set the gain. Q282 and Q284 emitter-coupled stage provides both the temperature compensation and high internal gain. Q287 provides the inversion and negative signal offset so the input and output can both be at zero volts at the same time. Q287 collector has the same ±10 volt operating range as the Memory output. L287 raises the load resistance during fast changes at sample time to limit the pulse current amplitude required of the — 12.2-volt supply at Q287 emitter.

Protective components are D282 which conducts when Q287 is removed from its socket and protects Q282 base-emitter junction from excessive reverse bias; D287 which conducts when Q284 is removed from its socket and protects Q287 base-emitter junction from excessive reverse bias; and C286-R286 which stabilize the amplifier against self-oscillation.

The Inverter drives the Channel Amplifier through the INVERT switch and the VARIABLE and Digital Gain controls.

A & B Channel Amps

The two Channel Amplifiers are approximately 2× gain inverting operational amplifiers. The gain is adjusted by the Digital Gain control (while the Units/Div switch VARIABLE control is at its CAL position) so the output to the Digital Unit is the required 1 V/Div. A center-screen zero signal input produces an output of +10 volts when the POSITION control is centered in its range. The output voltage can swing through approximately a 20 volt range, thus limiting the Memory output to 20 divisions of CRT display. The input current summing point is referenced approximately 0.6 volt above ground at the base of Q307 (Q607).

Q307 is the inverting amplifier and Q312 is the current gain emitter follower output. When a positive signal overdrives the amplifier, both Q307 and Q312 turn on hard, and both transistors may saturate. When a negative drive signal overdrives the amplifier, Zener diode D317 and D316 limit Q312 emitter voltage to about +21.8 volts, stopping any increase in feedback current. Once the feedback current stops following the input current, the summing input point becomes a higher impedance and starts negative. Q307 is completely cut off. D310 catches its collector at +22.4 volts, and D306 catches its base at —0.6 volt. The amplifier remains in this condition until the negative overdrive ceases.

D316 is in series with D317 to isolate D317 junction capacitance from the output terminal. C307, C315 and R315 all serve to stabilize the amplifier against self-oscillation. L313 presents a high impedance to Q312 emitter during fast signal changes so all the circuit current can be used for feedback; then, the inductor connects the load when the output voltage has stabilized. This reduces the amplitude of pulse currents required of the power supply during high amplitude fast changes.

The Channel Amplifiers always drive both the Output Amplifier and the Digital Unit. Either one may also drive the real-time time-base unit, depending upon the position of the TRIG OUT switch and the Horiz Plug-in Compatibility switch. Channel B Channel Amplifier can also drive a sampling sweep unit for the A VERT-B HORIZ mode of operation. R641 is in the circuit to simplify the construction of the Vertical Mode switch, and ground Q612 emitter at all other switch positions except A VERT-B HORIZ.

The circuit associated with the TRIG OUT switch offsets the +10-volt center-screen Channel Amplifier output signal to

zero at the junction of R332 and R334. This allows proper operation of the Non-Sampling time base DC coupled internal triggering circuit. D331 is a catching diode to stop the trigger output from going to —100 volts between positions of the TRIG OUT switch.

Output Amplifier

The Output Amplifier diagram contains circuits for three blocks of the complete block diagram: the Dual-Trace Multi, the Output Amp and the Position Lamp Driver.

The Dual Trace Multi programs the selection of the Channel Amplifier which drives the Output Amplifier, and the Dual Trace Multi operation is programmed by the Vertical Mode switch on the front panel. The Dual Trace Multi is actually a multivibrator only when the Vertical Mode switch is placed in the DUAL-TRACE position. At the other modes of operation, the Dual Trace Driver drive signal is diode-disconnected, and only one of the two transistors may conduct. A conducting transistor takes the signal current of the channel not displayed, and a non-conducting transistor permits its associated channel to be displayed. Multi transistor Q714 controls Channel B, and Q724 controls Channel A.

The signals of both Channel Amplifiers enter the Output Amplifier diagram into the emitter circuits of two common base amplifiers. These amplifiers share the collector load resistance of R753 in parallel with R762. With the exception of A + B operation, only one of the common base amplifiers (Q749 or Q759) is connected to the collector load resistance. The Output Amplifier diagram lists DC voltages for displaying Channel A. Q714 conduction (controlled by the Vertical Mode switch) forward-biases D750 so that Q749 collector voltage reverse-biases D751. This disconnects the Channel B signal from the Output Amplifier. Q724 nonconduction permits R725 to reverse bias D760, so that Q759 collector current passes through D761 and the Channel A signal reaches the Output Amplifier input. There is essentially no current in R753, but D782-C782 assure that the resistor is in parallel with R762 so far as signals are concerned.

A + B operation turns off both Q714 and Q724, permitting both Q749 and Q759 to be connected to R753-R762. Both channel signals are thus added algebraically. R753 is now connected to +15 volts. This doubles the DC current in the collector load resistance, so the current of both common base stages added together does not alter the DC level into the Output Amplifier. There will probably be a vertical shift in the display when changing the vertical mode switch from CH B to A + B, the amount of shift depending upon the voltage tolerance of Zener diode D782.

Dual-Trace operation forward biases D701 so the —50 V to 0 V Dual-Trace Driver signal can reach the Dual-Trace Multi and switch it at each sample time. Each time a sample is taken, the Dual-Trace Multi changes states on the positive portion of the drive pulse. Each time the multi changes states the Output Amplifier is driven by the other channel. The multi divides the sampling rate by two and delivers a Digital Intensified Zone Enable signal (up = logical 0 at about +1 volt = CH A; down = logical 1 at about —1 volt = CH B) to the digital unit from Q714 collector.

The Output Amplifier consists of the high gain stage Q771 and Q775, and a ×1 inverting amplifier Q781 and Q785. The high gain stage drives the inverter. Both circuits are DC coupled operational amplifiers with a common negative point at Zener diode D782.

Signals arrive from the common-base stages Q749 and/or Q759, and pass through the front panel GAIN control to the summing input at the base of Q771. The internal Vertical Centering control also applies a DC signal to the same summing point, permitting adjustment for differences in the center-screen voltage that appears at the common-base switching stages, and the tolerance range of D782. Signals are amplified by Q771 and given current gain by emitter follower Q775. (All four Output Amplifier transistors have BV_{CBO} ratings of 300 volts). D774 connects Q771 collector to the output if Q775 base falls faster than its emitter for fast full screen positive-going changes. Q775 emitter also drives the ×1 inverter input.

The inverter amplifier is identical to that just described, except that the gain is 1. D784 connects Q781 collector to the output if Q785 base falls faster than its emitter for fast full screen negative-going changes. Both sides of the Output Amplifier drive the Position Lamp Driver stage.

The position Lamp Driver is a floating current switch that operates the two position-indicating neons on the front panel.

The average voltage at the CRT deflection plates is about +180 volts, which sets the total emitter current of Q793 and Q795 at 0.3 mA. When the two deflection plate voltages are equal, the two transistors share the 0.3 mA and both neons are lighted. If either side neon goes more positive than the other, the transistor on that side takes all the 0.3 mA and the other transistor cuts off. Each transistor has a BV_{CBO} rating of 85 volts, so R797 prevents the turned off-transistor collector from going all the way to +300 volts. The dark neon has some voltage across it, but not enough to cause it to glow. D791 and D792 assure that the two transistor base voltages are never more than 0.6 volts apart.

Gate Generators

The Gate Generators diagram contains circuits for the Blocking Oscillator, Dual-Trace Driver, both Delay & Strobe Drivers and both Memory Gate Drivers. The Blocking oscillator starts the sampling process when driven by the Sampling sweep unit with the Horiz Plug-In Compatibility switch at Sampling 3T-Series. When the Horiz Plug-In Compatibility switch is at Non-Sampling 2B, 3B-Series, the Dual-Trace Driver oscillates at 100 kHz and drives the Blocking Oscillator. The Blocking Oscillator always drives the two Delay & Strobe Driver circuits. The Dual-Trace Driver always drives the Dual-Trace Multivibrator and CRT cathode for interdot blanking of the display.

The Blocking Oscillator can be thought of as a risetime improving circuit. If the sampling sweep unit drive pulse risetime changes from one type of time base to another, the Blocking Oscillator cancels the difference. Q3 always delivers a signal of the same amplitude and same risetime at its output. The stage is a simple amplifier until T3 builds up enough positive feedback for regeneration. After regeneration, the circuit ignores the drive pulse shape, amplitude and energy content. Q3 is normally biased to cutoff, causing the output signal to go from +15 volts to ground each time it is driven. D2 disconnects T3 backswing pulse from Q3 base and also makes certain T3 does not load the drive pulse.

The Dual-Trace Driver is a monostable multivibrator during Sampling 3T-Series operation, and a free running 100 kHz Colpitts oscillator during Non-Sampling 2B, 3B-Series operation.

As a monostable multivibrator, neither transistor conducts until driven. — 12.2 volts is applied to R10 and R19, placing Q17 at zero bias. Q24 is reverse biased by the junction drop of D24 and current in R21.

A negative drive pulse from the Blocking oscillator is coupled through C15 and C23 to Q24 base. (D15 is reverse-biased 15 volts while Q17 is off, so it doesn't stop the drive pulse from reaching Q24.) Q24 turns on hard and D25-C25 couples drive to Q17 base. Q17 turns on and applies more drive to Q24, limited at ground by D15. Thus a heavy regeneration causes a 50 volt output pulse to drive both the Dual-Trace Multi and the CRT cathode circuit. C23 charges rapidly, but C22 does not. C22 holds base drive current applied to Q24 for a longer period. When C22 is charged, Q24 cuts off and its falling collector signal is AC coupled by C25 alone to Q17 base turning it off. The turn-off is also regenerative, with D24 limiting the reverse bias on Q24 and helping to recharge C23 for the next cycle. (R22 in series with C22 causes the positive portion of the output signal to be stable at essentially ground. The time of conduction is independent of drive because Q17 keeps D15 conducting until the regenerative turn-off starts.)

Placing the Horiz Plug-In Compatibility switch to Non-Sampling 2B, 3B-Series converts Q17 to a Colpitts oscillator. Now the Blocking Oscillator receives no signal from the real-time time-base unit. Instead, it is driven by the oscillator through C4. The Dual Trace Multi still produces a 50 volt output pulse because D25 is reverse biased most of the time. The oscillator frequency is controlled by L8, C9 and C10.

The Delay & Strobe Driver and Memory Gate Width circuits are actually one circuit. The A and B channel circuits are identical except for R32, located between +15 volts and the B DELAY control. R32 is a power supply isolation resistor. The Channel B circuit is explained below.

The complete circuit, from Blocking Oscillator output to the two pulse outputs, consists of: A two-diode comparator that compares a negative-going ramp with a fixed DC voltage variable by the Delay control; a very low-current amplifier that follows the Delay control voltage without affecting its output to the next stage; and a monostable multivibrator with two output terminals.

Quiescent circuit conditions are: Q36 base voltage rests between +15 and +11 volts, as set by the B DELAY control. Q36 current is limited to about 1 mA by R36, which does not pull the collector up to —12.2 volts. Instead, D38 clamps the collector at —12.8 volts assuring that there is no change in output voltage when the Delay control position is changed. Q41 is reverse biased 0.6 volt by D38, and Q54 is reverse biased 0.6 volt by current in D54, D52, R51 and the Memory Gate Width control. Q54 collector voltage is —12.2 volts.

As the Blocking Oscillator fires, R34-C34 form a negative-going ramp that soon causes D34 to conduct. When D34 conducts, the ramp turns Q36 on. C36 contains enough charge for Q36 collector to clear D38 of carriers, and to forward-bias Q41. As Q41 conducts, the negative signal is coupled through C41 and C33 back to Q36 base in a regenerative turn-on. The feedback signal also reverse-biases D31 and D34 so as not to disturb the other channel Delay circuit.

The —27 volt signal from Q41 collector drives Q54 through C45. C45 signal current reverse-biases D52, allowing R53 to turn on just into saturation. Q54 collector signal couples through R48 back to Q41 base and holds Q41 in steady conduction. R59 applies a steady 50 mA current to the Memory Gate transformer primary (T535) for the pulse duration of about 180 ns.

C33 regenerative turn-on to Q36 does not last as long as Q54 turn-on to Q41, but since Q41 base voltage cannot go more positive than about —11.6 volts, Q36 collector is not disturbed. The duration of Q54 conduction is therefore controlled only by the position of the Memory Gate Width control which adjusts C45 charge rate. The smaller the resistance, the shorter the gate duration. As C45 charges toward +15 volts, D52 again conducts and turns Q54 off, stopping the Memory Gate pulse and the drive to Q41 base. However, Q41 was in saturation, so it does not stop conducting immediately. Q41 collector signal rises positive about 350 ns after it is driven negative. This RC rise is slow and does not couple much energy through either C41 or C33. Q41 total negative step is coupled by C41 as a Strobe Drive pulse to the sampling head.

The sampling drive pulse from the sampling sweep unit is slewed in time from the initial trigger event of each sweep. An additional time positioning is accomplished in the two Delay (ramp comparator) circuits. The additional time slewing of the strobe drive pulses requires an identical time slewing of the Memory Gate drive pulses in order to maintain proper processing of the error signals into the Memory Amplifier. Therefore, the Memory Gate Driver is driven by the Delay & Strobe Driver.

Power Distribution & Connectors

The Power Distribution & Connectors diagram contains many power supply decoupling networks and the internal power supplies. Power from the indicator oscilloscope enters through P11 at the left edge of the diagram. P11 also shows pin connections of other circuits within the Type 3S2.

Decoupling networks are drawn within outlined areas that represent particular diagrams already described. At the page right are the decoupling networks that are located on the left side Vertical Board.

One section of the Vertical Mode switch shows the biasing voltage change sent to the sampling sweep unit horizontal amplifier during A VERT B HORIZ operations. Function of the bias change is discussed in the sweep unit instruction manual.

Internal Power Supplies obtain power from the indicator oscilloscope at 6.3 VAC, and from the +125-volt and —100-volt supplies.

The +15-Volt Supply is fed 6.3 VAC at T821. T821 secondary voltage of approximately 51 VAC is rectified by D823-D825, filtered by C824, and regulated by D827, Q828, Q830, Q836 and Q839. The regulator circuit is of the series type, with Q839 the series pass (variable resistance) transistor. Q828 and Q830 form a temperature compensated comparator circuit, and Q836 inverts and amplifies the compar-

ator output which controls Q839. The output voltage is compared with the reference Zener diode D827.

Assume a positive change in the output voltage. The correcting action that follows causes Q839 series resistance to increase, restoring the output voltage to its correct value. The positive change at the output is directly coupled to Q828 base, and attenuator-coupled to Q830 base. Q830 emitter is driven by Q828 emitter and follows the change all the way. Q830 base does not follow the change 100% and therefore the transistor receives a forward bias signal. Q830 increases its current and applies a positive signal to Q836 base, causing Q836 to reduce its collector current. (In normal operation all Q836 collector current is Q839 base current, and none passes through R837-D837). Current reduction in Q836 causes Q839 base and emitter to go more negative. Or more properly stated, Q839 increases its series resistance so the load current increases the voltage across it, restoring the output to its proper value. R837-D837 take all Q836 collector current if the +15 volts output is shorted, permitting Q839 emitter to go positive with respect to the base, and thus become a very high series resistance. Such high resistance of Q839 protects the transformer and rectifiers from damage.

The —50 Volt Supply consists of the comparator, Q842-Q844, and shunt regulator Q848. (The —50-Volt supply is one of two voltage references for the +50 V supply).

The supply changes the resistance of Q848 to take more current when the load current reduces, and to take less current when the load current increases. D848 protects Q848 from damage in the event the output is shorted to a voltage more positive than —12.2 volts.

Comparator transistors Q842-Q844 compare a voltage near ground at the junction of R845-R846 with zero volts at ground. If the output load current increases (output voltage goes positive), Q844 base and emitter follow the change. Q844 emitter drives Q842 emitter positively, which is an increase in forward bias and turns Q842 on harder. Q842 collector voltage change decreases Q848 turn-on-bias, increasing Q848 resistance and permitting a negative return in voltage at the supply output.

The +50-Volt Supply uses one transistor as an emitter follower and the other transistor as both a comparator and as the shunt regulating element. R857-R858 presents a voltage near +15 volts to the base of emitter follower Q856. Q856 provides current gain to the signal and applies it to the base of comparator-regulator transistor Q853.

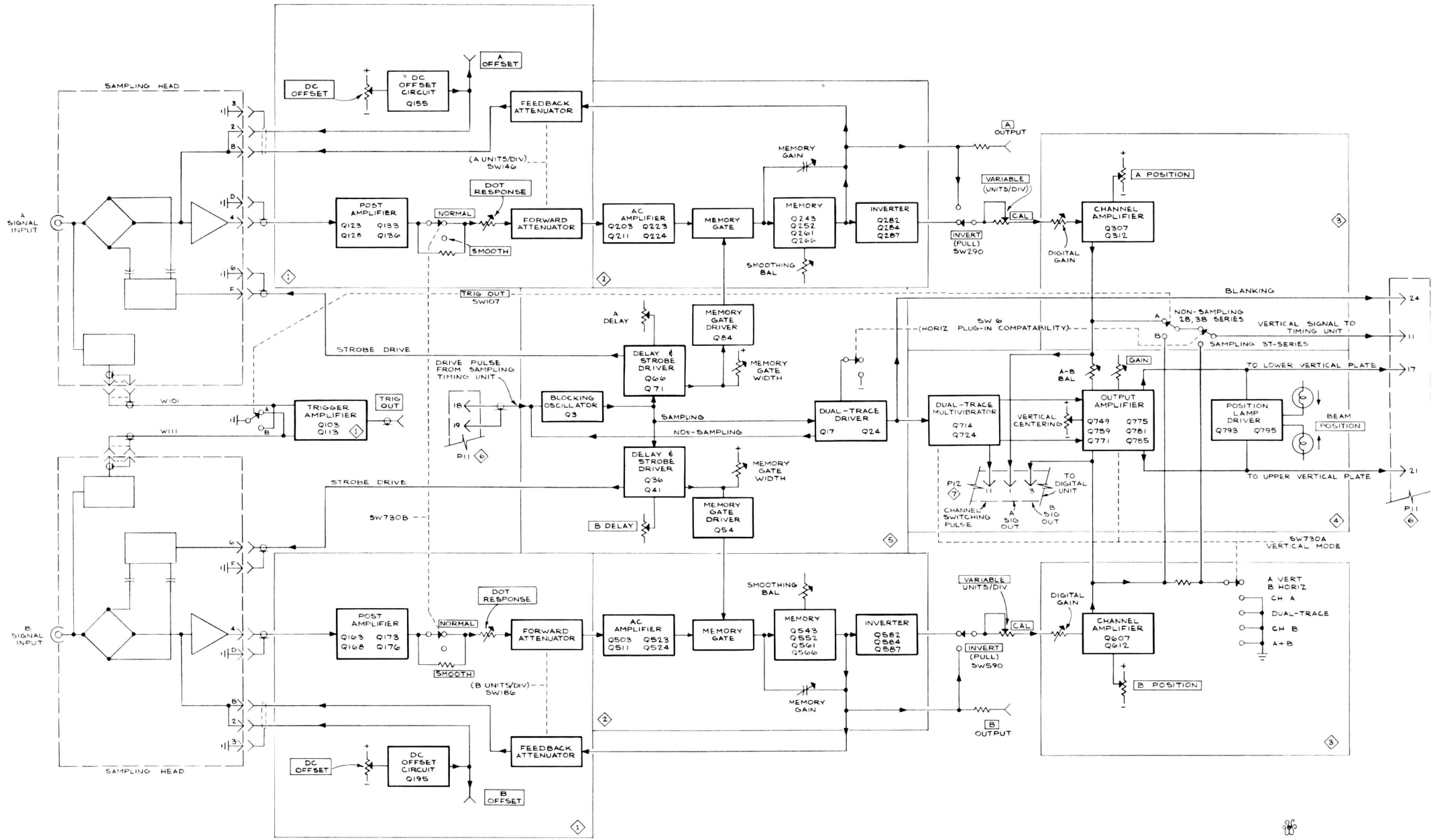
If the output load current increases (voltage goes negative), Q856 emitter takes Q853 base negative, reducing Q853 current. As Q853 current reduces, the output voltage rises back to its proper value.

A short circuit that places the +50-Volt line less positive than +15 volts will reverse-bias Q853 and protect Q853 from damage. The large resistance value of R857 and R858 protects Q856 from damage.

A short circuit on the —50-Volt line will cause the +50-Volt output to be a few volts low. Again, no transistors will be damaged.

Digital Switching

The Digital Switching diagram contains information on the Units/Div and VARIABLE CAL switches, and their connections out to the Digital Unit. The Units/Div switch selects the Digital Unit decimal neon and units nixie operation for both Channels when the VARIABLE controls are at CAL. Diodes in some of the lines prevent logic interactions when the associated digital unit is externally programmed.



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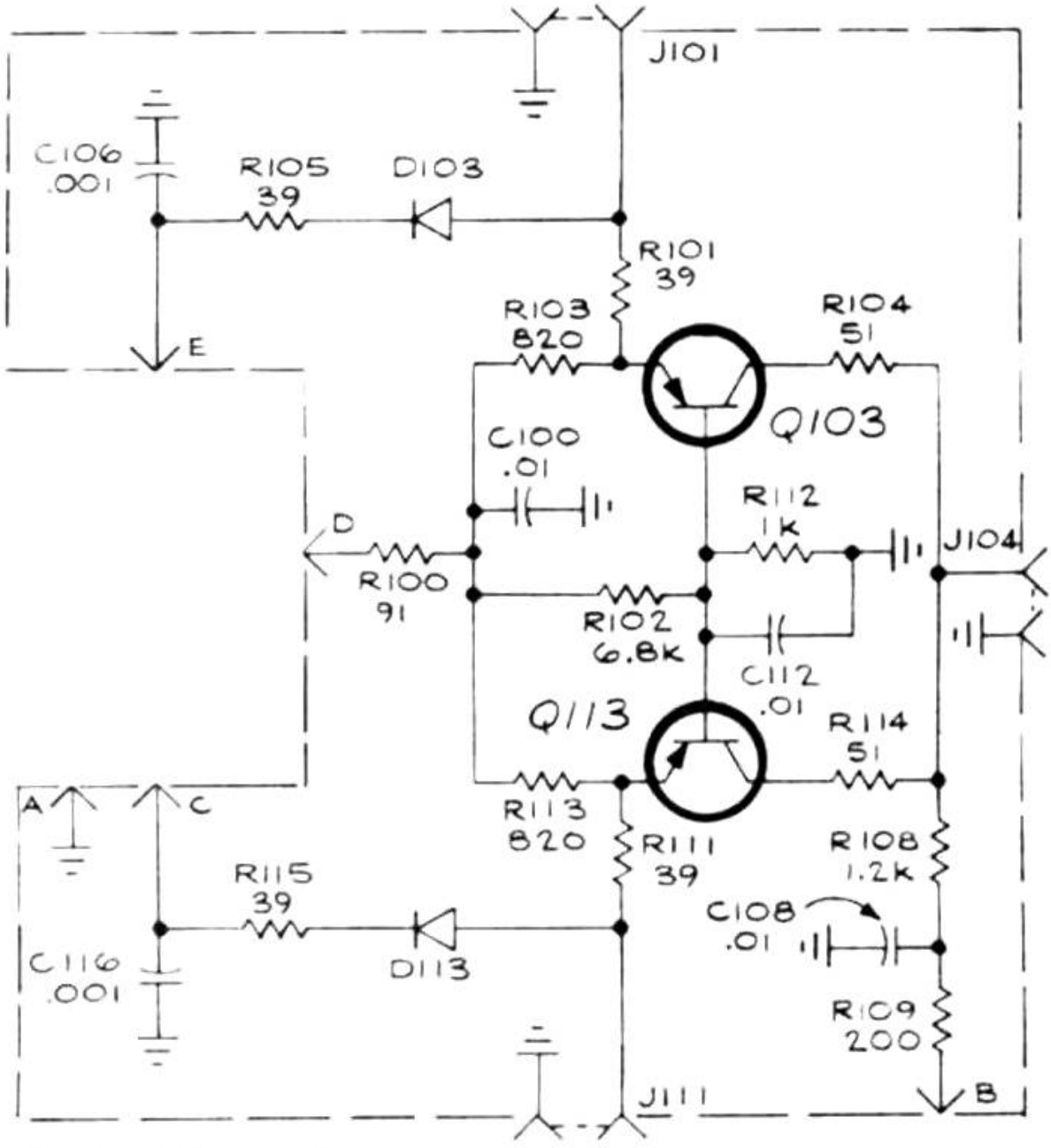
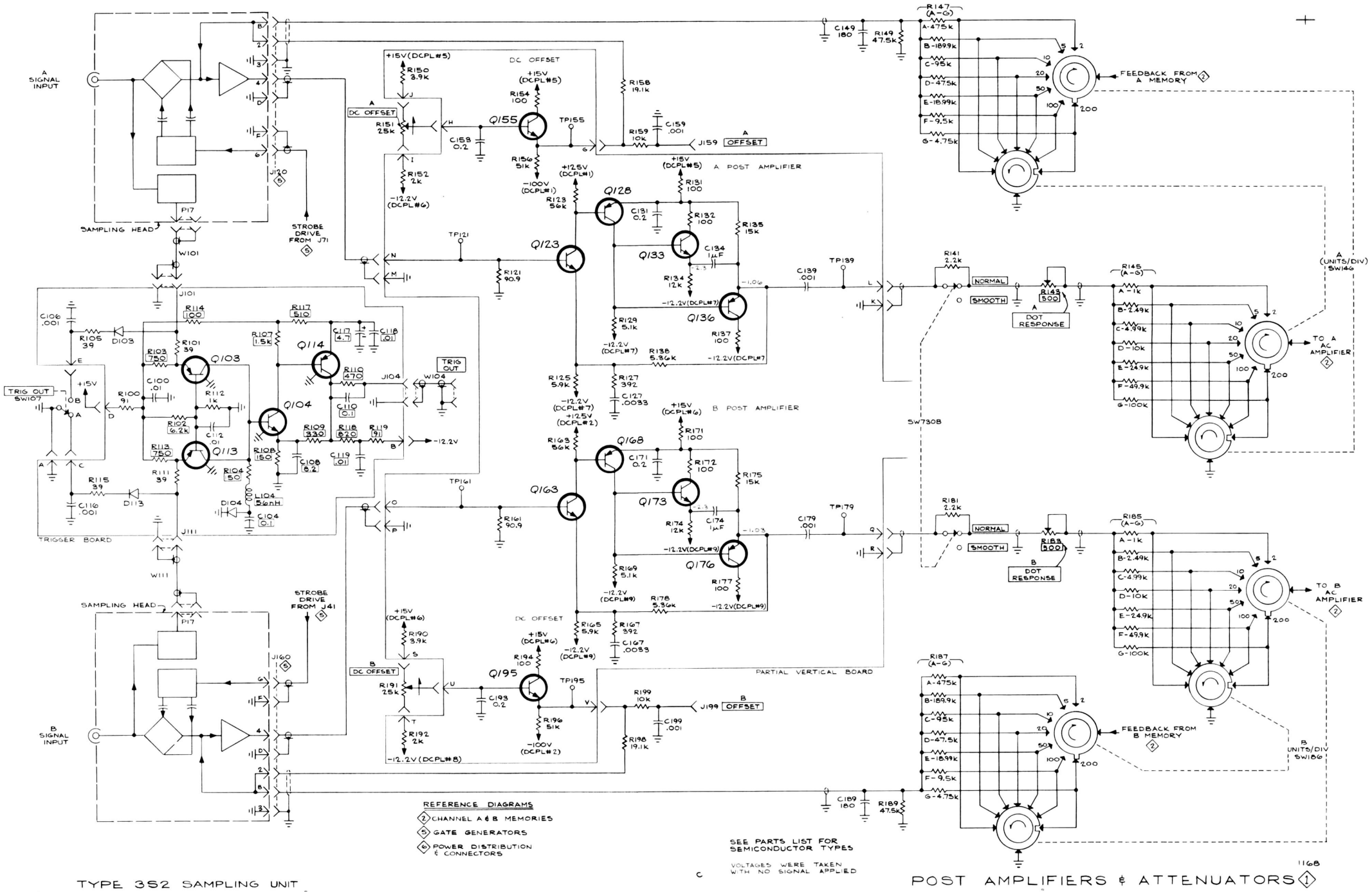
BLOCK DIAGRAM

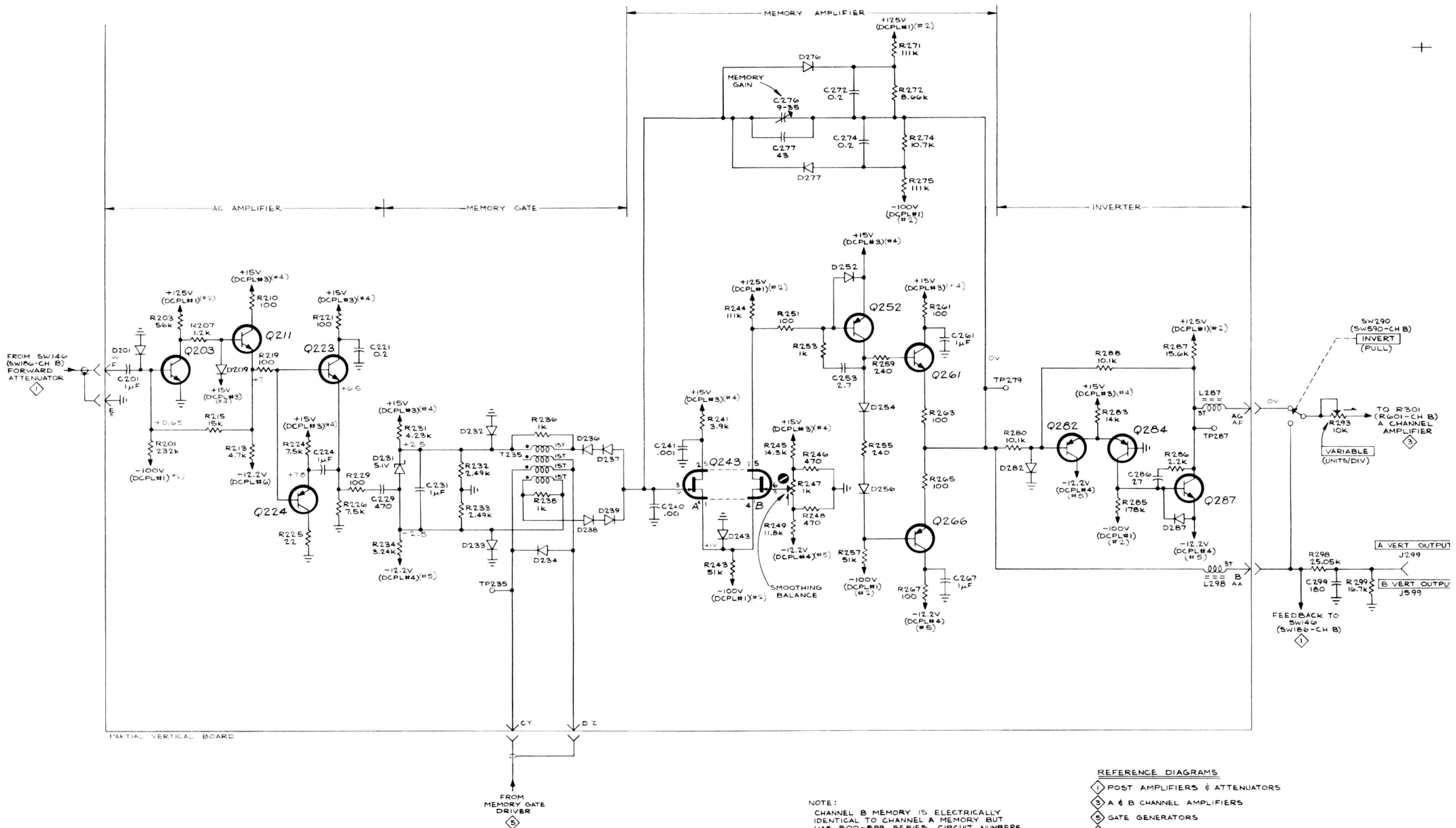
A

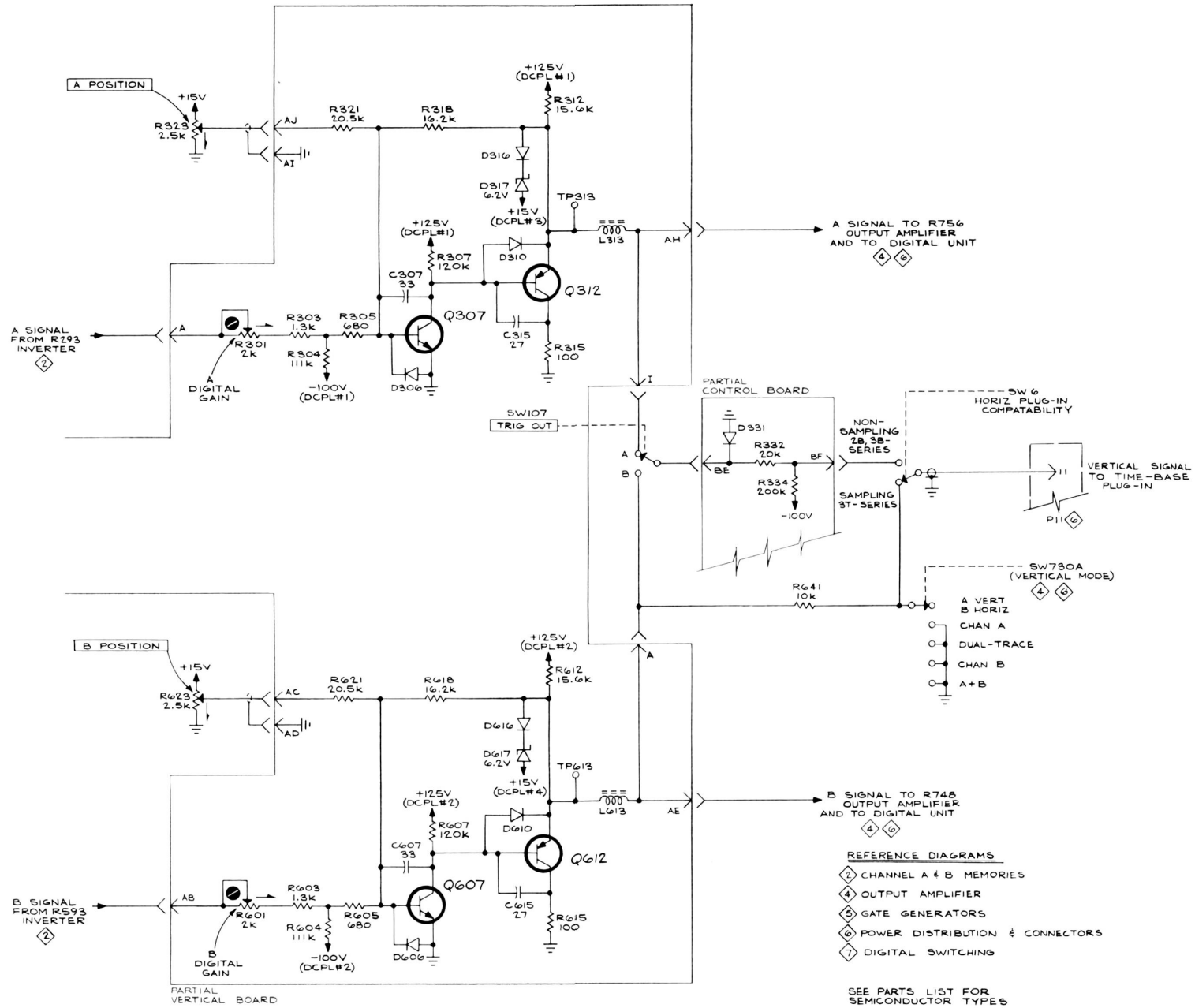
TYPE 3S2 SAMPLING UNIT

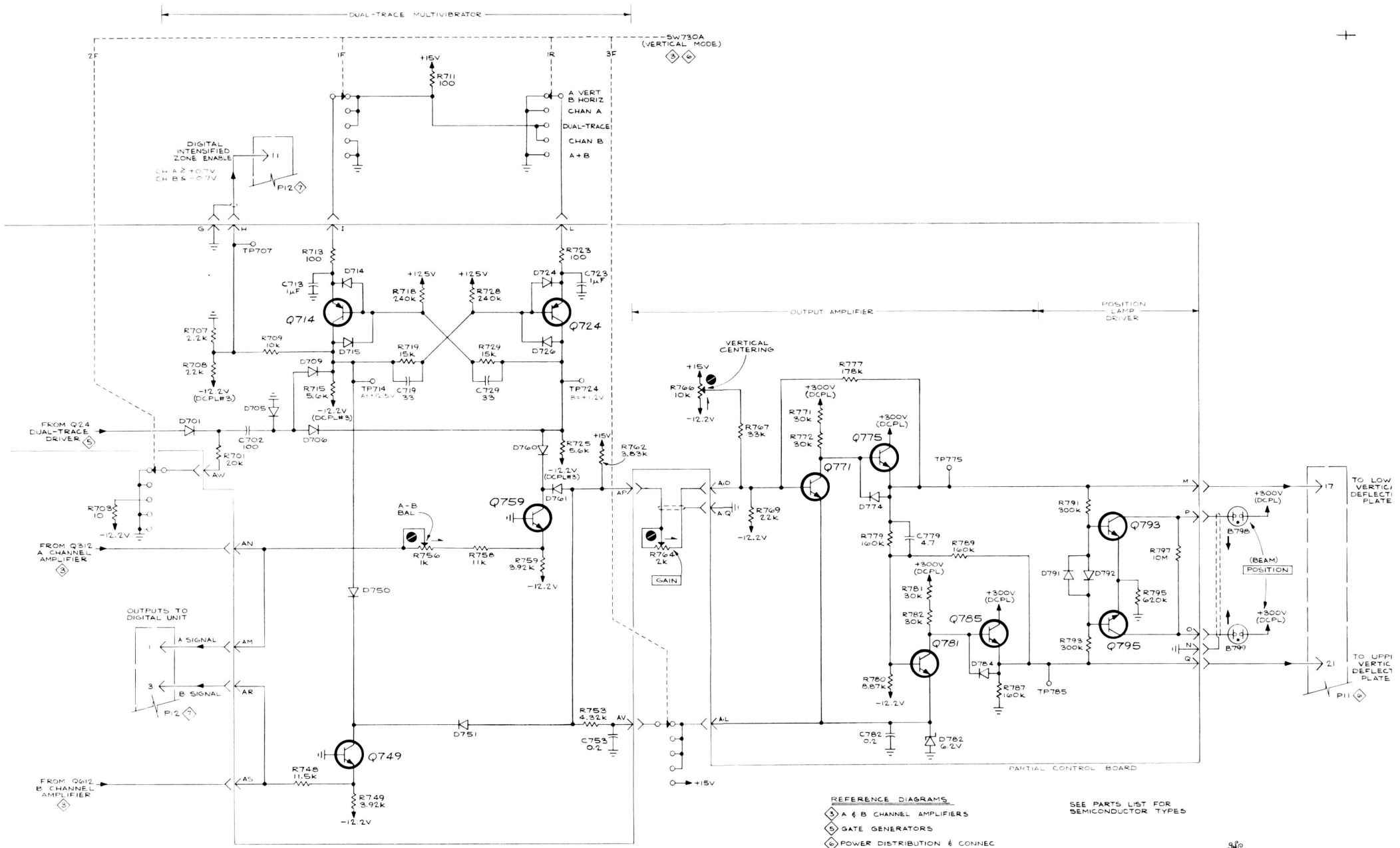


TRIGGER BOARD
(EFF S/N 100-250)


A SIGNAL INPUT
SAMPLING HEAD
P17
W101
J101
J120
STROBE DRIVE FROM J71
TRIGGER BOARD
J111
W111
B SIGNAL INPUT
STROBE DRIVE FROM J41
J160
DC OFFSET
A DC OFFSET
B DC OFFSET
A OFFSET
B OFFSET
A POST AMPLIFIER
B POST AMPLIFIER
PARTIAL VERTICAL BOARD
TRIG OUT SW107
TRIG OUT
SW730B
NORMAL
SMOOTH
A DOT RESPONSE
B DOT RESPONSE
FEEDBACK FROM A MEMORY
FEEDBACK FROM B MEMORY
TO A AC AMPLIFIER
TO B AC AMPLIFIER
A (UNITS/DIV) SW146
B UNITS/DIV SW186
Q103
Q104
Q113
Q114
Q123
Q128
Q133
Q136
Q155
Q163
Q168
Q173
Q176
Q195
REFERENCE DIAGRAMS
2 CHANNEL A & B MEMORIES
5 GATE GENERATORS
6 POWER DISTRIBUTION & CONNECTORS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
VOLTAGES WERE TAKEN WITH NO SIGNAL APPLIED
1168
TYPE 352 SAMPLING UNIT
POST AMPLIFIERS & ATTENUATORS 1


MEMORY AMPLIFIER
AC AMPLIFIER
MEMORY GATE
INVERTER
PARTIAL VERTICAL BOARD
FROM SW146 (SW186-CH B) FORWARD ATTENUATOR
FROM MEMORY GATE DRIVER
MEMORY GAIN
SMOOTHING BALANCE
Q203
Q211
Q223
Q224
Q243
Q252
Q261
Q266
Q282
Q284
Q287
D276
D277
D252
D254
D256
D232
D233
D234
D235
D236
D237
D238
D239
D243
TP235
TP279
TP287
SW290 (SW590-CH B) INVERT (PULL)
VARIABLE (UNITS/DIV)
TO R301 (R401-CH B) A CHANNEL AMPLIFIER
A VERT OUTPUT J299
B VERT OUTPUT J599
FEEDBACK TO SW146 (SW186-CH B)
CY
DZ
NOTE:
CHANNEL B MEMORY IS ELECTRICALLY IDENTICAL TO CHANNEL A MEMORY BUT HAS 500-599 SERIES CIRCUIT NUMBERS
CHANNEL B PIN CONNECTORS & SUPPLY VOLTAGES ARE LETTERED IN BLUE
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
OPERATING VOLTAGES APPLY AFTER DC OFFSET CONTROL IS SET FOR ZERO VOLTS AT OFFSET JACK.
REFERENCE DIAGRAMS
1 POST AMPLIFIERS & ATTENUATORS
3 A & B CHANNEL AMPLIFIERS
5 GATE GENERATORS
6 POWER DISTRIBUTION & CONNECTORS


A POSITION
+15V
R323 2.5k
AJ
AI
R321 20.5k
R318 16.2k
+125V (DCPL#1)
R312 15.6k
D316
D317 6.2V
+15V (DCPL#3)
TP313
L313
AH
A SIGNAL TO R756 OUTPUT AMPLIFIER AND TO DIGITAL UNIT
4 6
+125V (DCPL#1)
R307 120k
C307 33
D310
Q312
Q307
R303 1.3k
R305 680
R301 2k
R304 111k
C315 27
R315 100
A SIGNAL FROM R293 INVERTER
2
A DIGITAL GAIN
-100V (DCPL#1)
D306
I
PARTIAL CONTROL BOARD
SW107 TRIG OUT
A
B
D331
R332 20k
BE
BF
R334 200k
-100V
NON-SAMPLING 28,38- SERIES
SAMPLING 3T-SERIES
SW 6 HORIZ PLUG-IN COMPATABILITY
VERTICAL SIGNAL TO TIME-BASE PLUG-IN
P11 6
SW730A (VERTICAL MODE)
4 6
R641 10k
A VERT
B HORIZ
CHAN A
DUAL-TRACE
CHAN B
A+B
B POSITION
+15V
R623 2.5k
AC
AD
R621 20.5k
R618 16.2k
+125V (DCPL#2)
R612 15.6k
D616
D617 6.2V
+15V (DCPL#4)
TP613
L613
AE
B SIGNAL TO R748 OUTPUT AMPLIFIER AND TO DIGITAL UNIT
4 6
+125V (DCPL#2)
R607 120k
C607 33
D610
Q612
Q607
R603 1.3k
R605 680
R601 2k
R604 111k
C615 27
R615 100
B SIGNAL FROM R593 INVERTER
2
B DIGITAL GAIN
-100V (DCPL#2)
D606
PARTIAL VERTICAL BOARD
REFERENCE DIAGRAMS
2 CHANNEL A & B MEMORIES
4 OUTPUT AMPLIFIER
5 GATE GENERATORS
6 POWER DISTRIBUTION & CONNECTORS
7 DIGITAL SWITCHING
SEE PARTS LIST FOR SEMICONDUCTOR TYPES



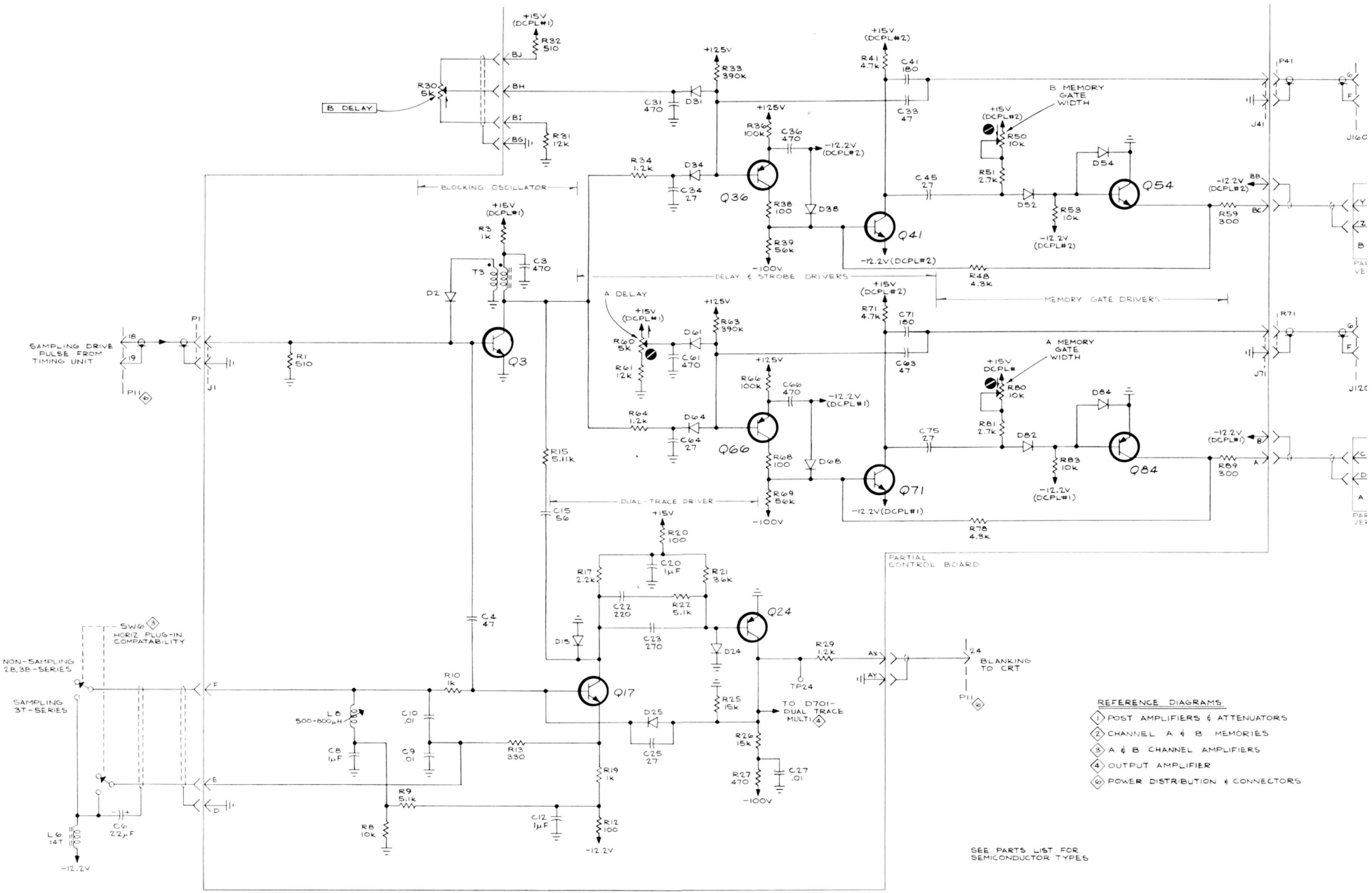
REFERENCE DIAGRAMS

- 3 A & B CHANNEL AMPLIFIERS
- 5 GATE GENERATORS
- 6 POWER DISTRIBUTION & CONNEC
- 7 DIGITAL SWITCHING

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

2-68

OUTPUT AMPLIFIER 4

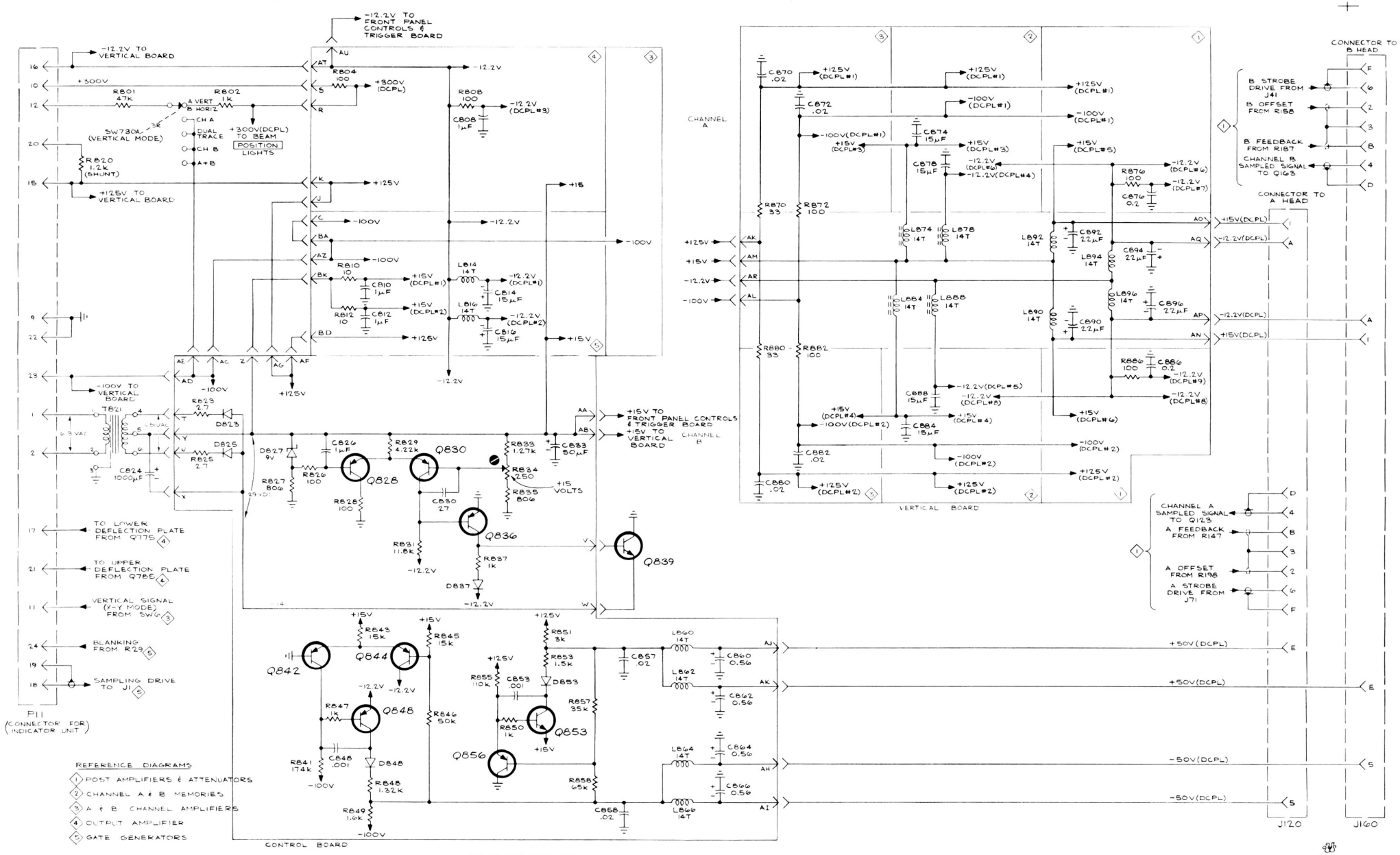


2-68

GATE GENERATORS ⟨5⟩

TYPE 3S2 SAMPLING UNIT

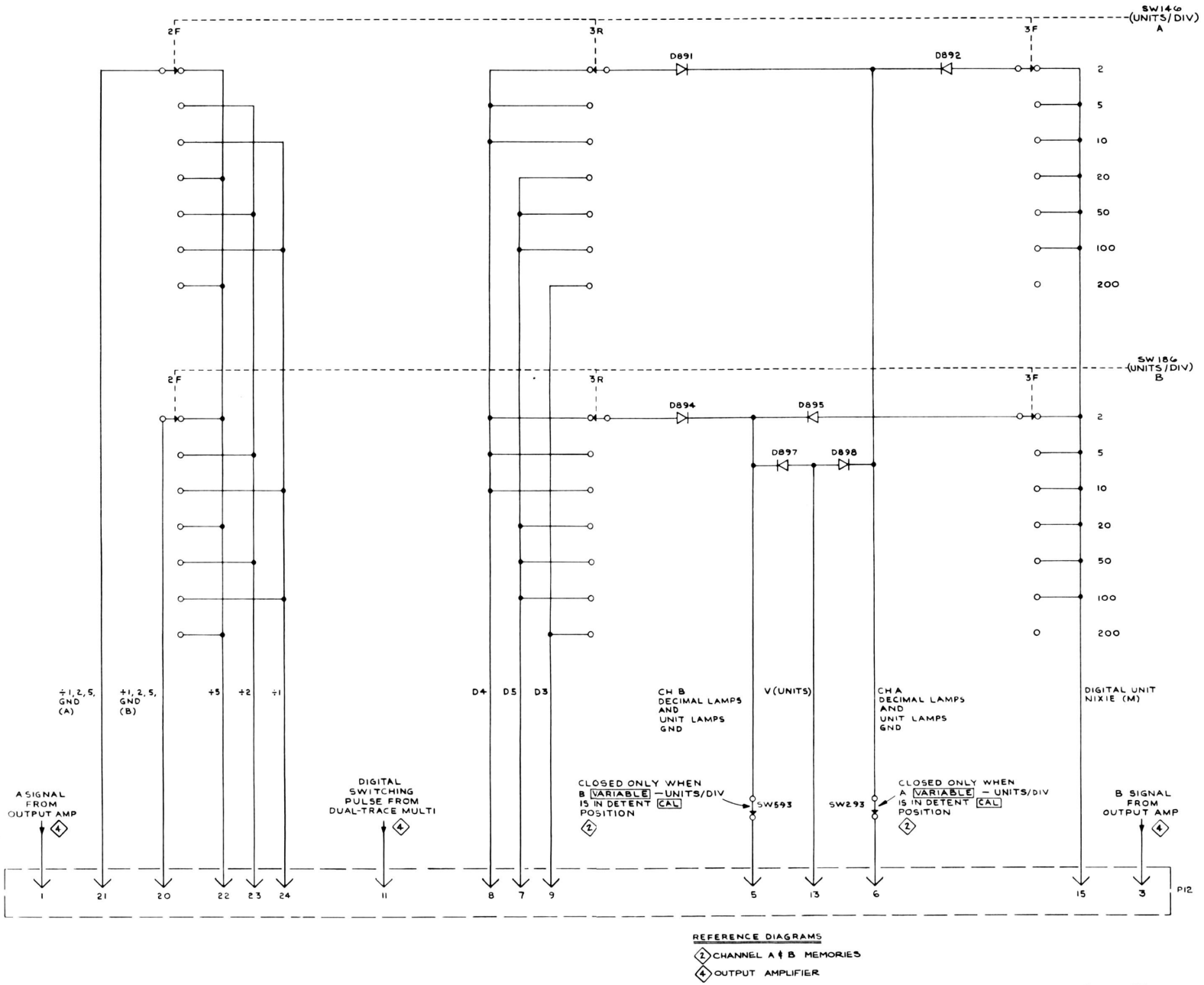
A



TYPE 3S2 SAMPLING UNIT

A

POWER DISTRIBUTION & CONNECTORS 6



TYPE 3S2 SAMPLING UNIT

DIGITAL SWITCHING 7