

INSTRUCTION MANUAL

Serial Number _____

TYPE 3S3 **SAMPLING-PROBE** **UNIT**

Tektronix, Inc.

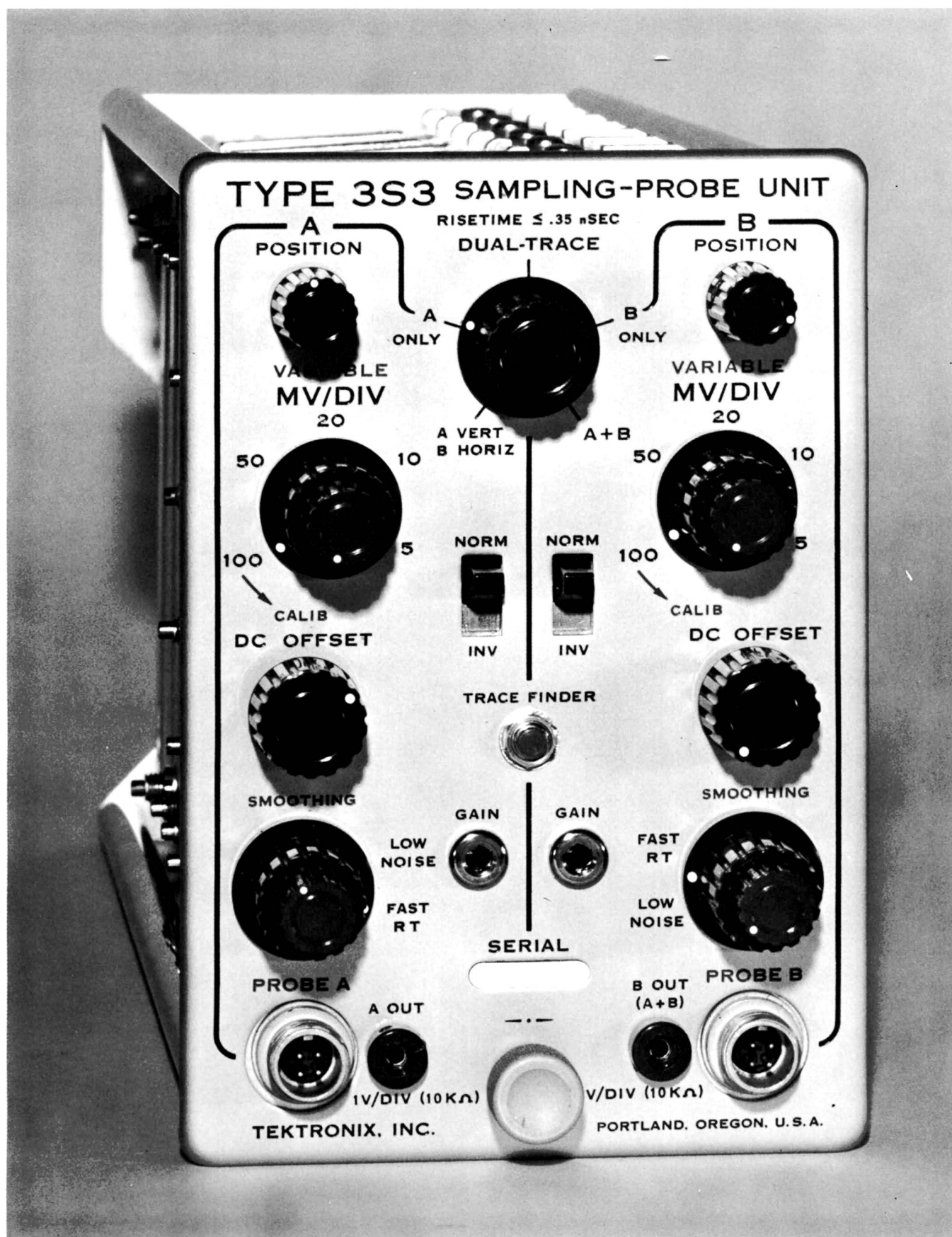
S.W. Millikan Way • P. O. Box 500 • Beaverton, Oregon • Phone MI 4-0161 • Cables: Tektronix

Tektronix International A.G.

Terrassenweg 1A • Zug, Switzerland • PH. 042-49192 • Cable: Tekintag, Zug Switzerland • Telex 53.574

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Type 353

Type 353 Sampling-Probe Unit.

SECTION 1

CHARACTERISTICS

General Information

The Tektronix Type 3S3 Sampling-Probe Unit is a dual-trace vertical channel plug-in unit for Tektronix Types 561A, 564, and 567 Oscilloscopes. The Type 3S3, operated with P6038 Direct Sampling Probes, has a basic risetime of 0.35 nsec or less when the signal source impedance is 50 ohms and the Noise-Risetime switch is at FAST RT. The LOW NOISE position of the switch gives the system a risetime of approximately 0.8 nsec. The P6038 sampling probe has a low-frequency input resistance of 100 k paralleled by about 2 pf capacitance. The system is capable of presenting accurate single- or dual-trace displays of repetitive high-speed signals with fractional-nanosecond risetime. By taking successive samples of a repetitive signal, each sample at a slightly later time with respect to the previous sample, the system reconstructs the signal on an equivalent time base.

ELECTRICAL AND MECHANICAL CHARACTERISTICS

Input Resistance

Probe only	100 k $\pm 1\%$
Probe and 10 \times Attenuator	1 meg $\pm 1.5\%$
Probe and Response Normalizer	100 k $\pm 1.5\%$

Input Capacitance

Probe only	2 pf $\pm 10\%$
Probe and 10 \times Attenuator	1.8 pf $\pm 10\%$
Probe and Response Normalizer	4 pf $\pm 10\%$

Ac Coupling Capacitor

Capacitance	1000 pf minimum, 100 volts
Approximate low-frequency 3 db point:	
Probe only	1.5 kc
Probe and 10 \times Attenuator	150 cycles
Probe and Response Normalizer	1.5 kc

Maximum Signal Input

	Linear Display (Dc Plus Peak Ac)		Momentary Dc or Ac Peak Overload
	Low Noise	Fast RT	
Probe Only	± 1.5 v	± 3 v	10 v
Probe and 10 \times Attenuator	± 15 v	± 30 v	100 v
Probe and Response Normalizer	± 1.5 v	± 3 v	10 v
Probe and Ac Coupling Capacitor	1.5 v ac	3 v ac	100 v dc

Signal Performance

See Table 1-1.

TABLE 1-1

Input	Source Impedance	Risetime in nsec	Overshoot in %	Noise in mv	Risetime in nsec	Overshoot in %	Noise in mv
		FAST RISETIME			LOW NOISE		
Probe Only	50 Ω	≤ 0.35	3	≤ 2	0.8	2	≤ 0.5
	*300 Ω	* 1.5	* 0	* ≤ 2	1.7	0	≤ 2
Probe and Coupling Capacitor	50 Ω	0.38	5	≤ 2	0.8	4	≤ 0.5
	300 Ω	* 2.5	* 0	* ≤ 2	3.0	0	≤ 2
Probe and 10 \times Attenuator	50 Ω	0.37	4	2	0.8	3	0.5
	300 Ω	* 1.5	* 0	* 2	1.7	0	0.5
Probe and Response Normalizer	50 Ω	* 1.5	* 0	* 2	1.7	0	2
	300 Ω	* 5	* 0	* 2	5	0	2

Risetime is 10% to 90%.

Overshoot is peak aberration of first 1 nsec of a square pulse display.

Noise is for single-channel operation at unity loop gain; multiply figures by 1.5 for combined-trace operation.

*SMOOTHING control fully counterclockwise. Dot transient response less than unity.

Deflection Factors

Calibrated steps of 5, 10, 20, 50, and 100 mv/div. Accuracy at unity loop gain: $\pm 3\%$ for all positions of MV/DIV switch with NORM-INV switch at NORM; $\pm 5\%$ for all positions of the MV/DIV switch with NORM-INV switch at INV. A VARIABLE control with about a 3:1 range permits uncalibrated sensitivity increase, thus decreasing the deflection factor of each setting of the MV/DIV switch. Accuracy at full smoothing: $\pm 3\%$ to $\pm 6\%$ for all positions of the MV/DIV switch with NORM-INV switch at NORM; $\pm 5\%$ to $\pm 8\%$ for all positions of the MV/DIV switch with NORM-INV switch at INV.

Triggering

External to Timing Unit. Pretrigger must arrive at Timing Unit external trigger input connector about 60 nsec prior to arrival of signal at input to P6038 Probe when sweep rate is 1 nsec/div or faster. Pretrigger can arrive at Timing Unit more than 60 nsec ahead of signal to P6038 Probe when using slower sweep rates.

Operating Modes

A Only, B Only, Dual-Trace, A + B, and A Vertical — B Horizontal (X-Y operation). The dual-trace switching frequency is one-half the sampling rate.

Rejection ratio for A + B mode is 40:1 or better when each channel is driven with a 0.5-volt flat-top pulse and the deflection factor is 50 mv/div, each channel. At 100 mv/div, A + B, a 4-division identical signal in each channel will produce an 8-division display, ± 0.15 division.

Display

Normal or Inverted, permitting the addition or subtraction of dual-trace displays. Valuable in X-Y displays for observation of hysteresis loops, or for inverting the phase of signals into or out of an amplifier for phase comparison. Inverted operation can add an additional 2% error to the deflection factors.

Smoothing

Each channel SMOOTHING control permits adjustment of the dot transient response. Clockwise rotation reduces time jitter and random noise. Valuable when operating at lowest deflection factors. The dot transient response can be made correct for source impedances from at least $50\ \Omega$ to approximately $300\ \Omega$ when the Noise-Risetime switch is at LOW NOISE; from about $50\ \Omega$ to some higher value (dependent upon source capacitance) when the Noise-Risetime switch is at FAST RT.

Dc Offset

The dc component of a signal may be offset up to ± 0.5 volt (with a ten-turn control) to either bring a display back onto the crt, or to make an incremental measurement.

Signal Outputs

Signal output jacks, A OUT and B OUT (A + B) are provided. The signal output of each is 1 volt/div, $\pm 3\%$, on a dc level of about +10 volts when the trace is centered vertically. Output impedance is 10 k.

Trace Finder

Pushing the TRACE FINDER button reduces the vertical amplifier gain by 5, allowing off-screen displays to be located and returned to view.

Dot Slash

The sampling dot vertical stability is such that no slash is visible when triggering at a rate above about 150 cps. At a triggering rate of 50 cps, the dot slash will not exceed 0.2 division.

Co-Channel Time Coincidence

Dual-trace display of a fast-rise pulse will produce no more than a 60-picosecond time difference between channels.

Construction

Aluminum-alloy chassis with six plug-in subchassis. Photo-etched anodized panel.

Dimensions

Height $6\frac{1}{4}$ inches, width $4\frac{1}{4}$ inches, depth $12\frac{1}{2}$ inches.

Weight

6 lbs, 1 oz.

Accessories

	Tektronix Part No.
2 — Instruction Manuals	070-374
2 — P6038 Probe Packages	010-156

SECTION 3

CIRCUIT DESCRIPTION

General Information

Most circuits in the Type 3S3 are on plug-in subchassis. The main frame contains only the preamplifier circuits, controls, interconnections, and cables. You may wish to refer to the Tektronix publication "Sampling Notes", publication number 061-557, during the following discussion.

Block Diagram

The Type 3S3 simplified block diagram of Fig. 3-1 shows each circuit in block form, with all front-panel controls identified. Since the two channels are nearly identical, only the Channel A circuits are shown. A detailed block diagram is included with the schematics at the back of this manual.

External trigger information to the Timing Unit starts the sampling cycle. The Timing Unit sends command pulses to the Type 3S3 Gate Generator. The Gate Generator sends very short duration push-pull pulses to both P6038 Probes, and longer duration pulses to both Memory circuits. The

pulses from the Gate Generator first connect the signal to the preamplifiers, and then each preamplifier to its Memory.

Input signals arrive at the P6038 Probe sampling gate. The sampling gate is biased to conduction by the Gate Generator as command pulses arrive from the timing unit. The sampling gate output signal is a series of pulses, amplified by the preamplifier, and coupled through the MV/DIV switch to the Memory. The Memory input circuit is an Ac Amplifier that raises the signal level for the Memory. The Gate Generator biases a two-diode gate at the Memory input to conduction as the signal arrives.

The Memory amplifies and stores the signal. The Memory output is sent to the Inverter, and to the probe and input circuit to set the voltage equal to the signal at the time of the sample. (The next sample only corrects for any signal change since the last sample.) The Memory output signal can be inverted by the unity gain Inverter. The output of both channels then pass to the Dual-Trace electronic switch where either or both are sent on to the Vertical Amplifier, and each is available for the oscilloscope Digital Unit.

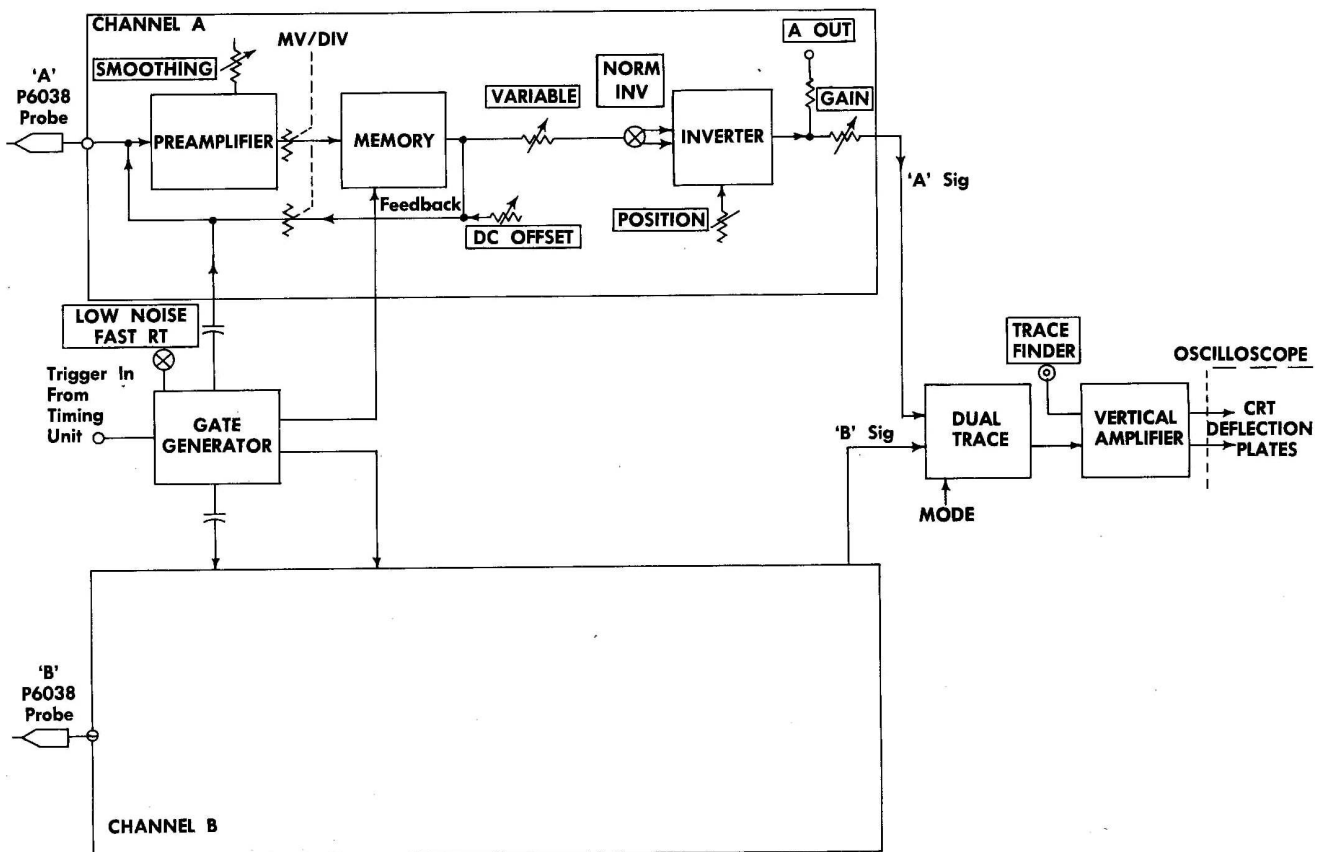


Fig. 3-1. Type 3S3 simplified block diagram, Channel B is essentially the same as Channel A.

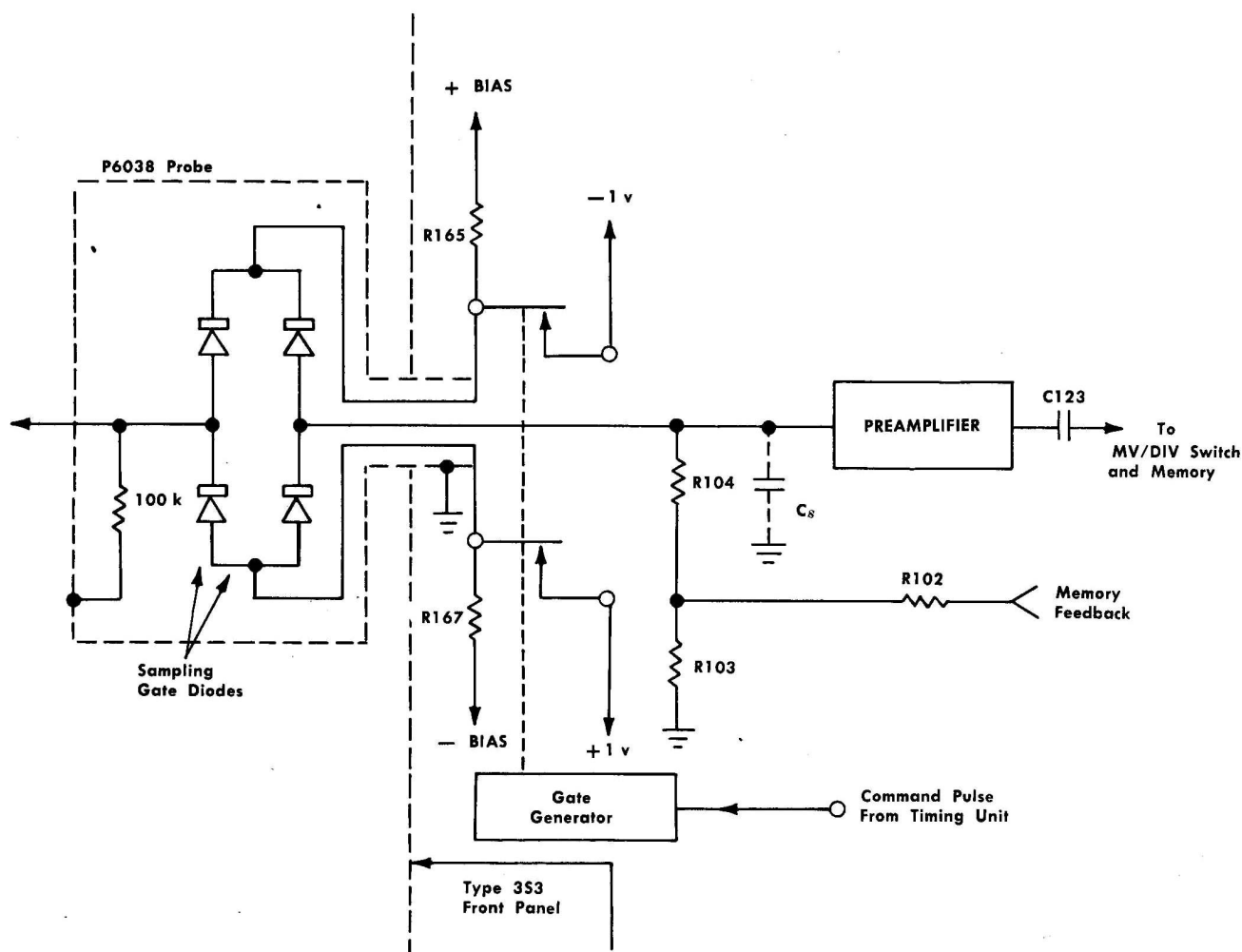


Fig. 3-2. Simplified Channel A input.

P6038 Probe

The Type 353 input is via the P6038 Probe shown in simplified form in Fig. 3-2. The probe is the heart of the sampling system where the 0.35-nsec risetime performance is established. The input impedance is 100 k paralleled by about 2 pf.

Fig. 3-2 shows the probe sampling gate is normally reverse biased (about 4 to 5 volts). The relay contacts represent an equivalent method of applying forward bias to the sampling gate. If the relay is closed momentarily, the gate is forward biased and connects the signal to the Pre-amplifier. The duration of forward biasing is slightly less than 0.35 nsec; so fast that the probe cable and Pre-amplifier shunt capacitance (C_s) limit the signal to the Pre-amplifier grid to about 2% of the input amplitude. C_s is stray input capacitance that increases the signal duration at the Pre-amplifier input. Because only about 2% of the signal

gets to the Pre-amplifier, the sampling efficiency is about 2%.

Gate Generator (Series A, Model 1)

The pulses that gate the sampling diodes into conduction are formed by a snap-off diode and clipping line, driven by a blocking oscillator, Q200. The blocking oscillator also drives the Memory input gates via the memory gate width amplifier, Q214.

The Gate Generator quiescent state is as follows: Q200 is held cut-off by reverse bias developed across D202. The emitter and base rest at +20 volts. The collector of Q200 rests slightly below ground due to about 20 ma of current flowing in the snap-off diode D200. The memory-gate amplifier Q214 is cut off with its base at about +0.3 volt due to the drop across D212.

As the positive trigger pulse arrives from the Timing Unit, the following action takes place:

The Timing Unit command pulse passes through coupling capacitor C209 and diode D207 to the collector of Q200. Q200 is a common-emitter type blocking-oscillator. When the positive trigger pulse is received, signal current passes through the collector winding of T200. Signal current in the collector winding induces a voltage in the base winding that overcomes the back-bias at the base and turns the transistor on for a blocking-oscillator cycle. The fast current rise which then occurs in the collector of Q200 is directly coupled to the snap-off circuit. During turn-on, Q200 base-emitter junction is forward biased by the feedback winding of T200. C202 receives a charge that will aid in stopping any self oscillation after the trigger pulse is gone.

After the collector voltage of Q200 rises to the saturation point, the normal blocking-oscillator back swing tries to occur. At the same time the charge on C202 back-biases the base of Q200, allowing a quick return to equilibrium.

The quiescent condition of snap-off diode D200 is set by the SNAP-OFF CURRENT control, R205. The circuit typically carries about 20 ma of forward current through D200. This forward current assures that D200 has many carriers within its junction region. As the forward current is suddenly reversed, the carriers require a short time to clear out and open the diode in a normal reverse bias condition. Snap-off diode D200 is reverse biased by the pulse from Q200 but does not become a high impedance immediately.

As the pulse from Q200 arrives at D200, a high reverse current builds up in the clipping line and D200. As the carriers clear out of the D200 junction, the reverse current stops suddenly, sending a fast-rise voltage pulse into the 50 Ω clipping line and toward each probe.

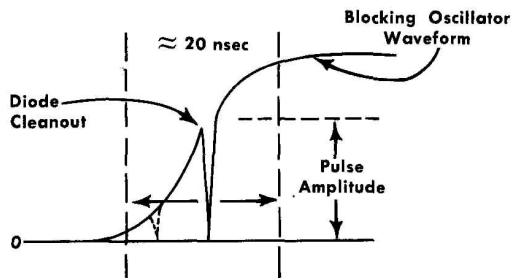


Fig. 3-3. Principle of snap-off diode action as SNAP-OFF CURRENT control is adjusted.

The blocking oscillator output pulse has a finite risetime. The snap-off diode reverse-cleanout delay is proportional to the forward bias applied (SNAP-OFF CURRENT adjustment). Thus, the interrogate pulse amplitude is set by the SNAP-OFF CURRENT control position. See Fig. 3-3.

The sharp step that appears at the clipping line input at snap-off is propagated down the line. The line acts as a balanced transmission line, terminated in a short circuit. The step travels to the short circuit in a finite time. When it reaches the short, it is reflected, equal in amplitude and opposite in polarity, back to the snap-off diode and the

probes. The reflection reverses the initial fast-pulse polarity, limiting the pulse duration to a very short time, and the snap-off diode returns to its normal forward bias condition. T160 balances the fast sampling pulses that are sent to the probe. The sampling pulse (Gate Generator output pulse to probes) is of triangular form with a duration greater than 1 nsec at its base and less than 0.35 nsec at the peak.

Low Noise—Fast Risetime

The system risetime is altered by changing the peak value of the Gate Generator pulse that causes the sampling gates to conduct. The Type 353 uses a switch that changes the value of the bridge volts (reverse bias) instead of changing the pulse amplitude. By this method, the peak value of gate pulse is effectively changed as shown in Fig. 3-4, thus changing the length of time the sampling gates conduct and the system risetime.

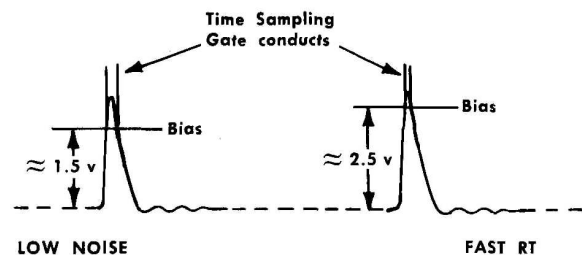


Fig. 3-4. Two conditions of Low Noise-Fast Risetime switch, idealized waveforms.

When the Low Noise-Fast Risetime switch is at LOW NOISE, R181 and R189 are placed in parallel with the BRIDGE VOLTS control. This reduces the amount of sampling bridge reverse bias. The sampling diodes' balance changes slightly with a change of bridge volts. The combination of the BRIDGE BAL and RISE TIME BAL controls allows each probe gate to be balanced for both bias conditions of the Low Noise-Fast Risetime switch.

Memory Gate Width

The memory is allowed to receive signals only when a sample is taken. Because the feedback loop contains positive feedback, the output of the Preamplifier must be disconnected from the memory input while the feedback loop is shifting the level at the input to the Preamplifier. The Gate Generator subchassis has a memory gate driver that controls the memory gates.

Memory gate amplifier Q214 is normally biased to cut-off due to drop across D212 and current through the MEMORY GATE WIDTH control R215 and R213. Q214 collector rests at -12.2 volts. The collector current path is through the two windings of the two Memory gates, not through D216 and R216. As Q200 pulses, a third winding of T200 couples a negative signal through D212 to the base of Q214, causing Q214 to saturate. Q214 collector rises nearly to ground and its current flows through the two Memory gates. Car-

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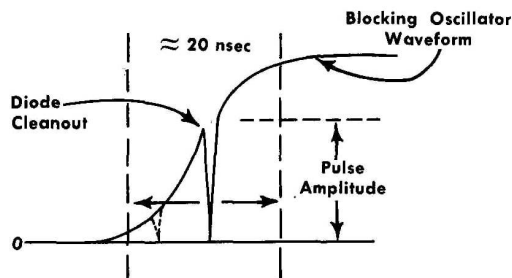


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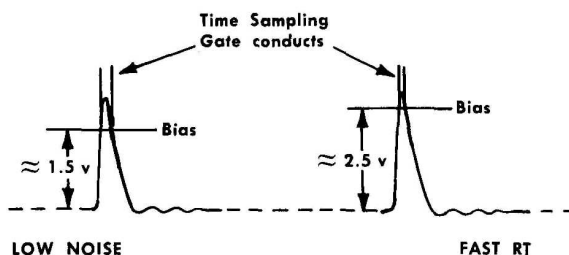


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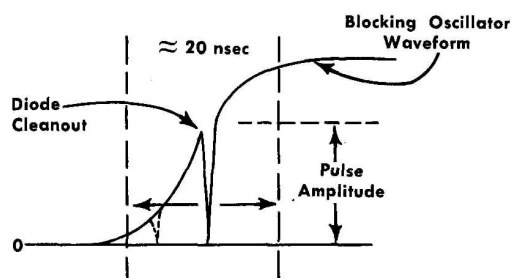


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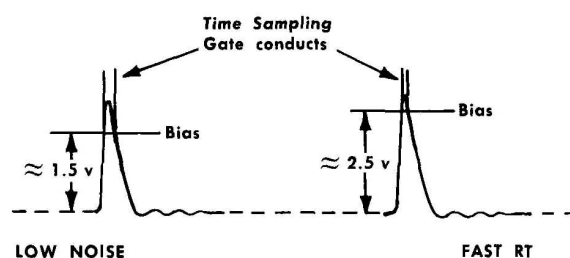


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Circuit Description—Type 3S3

rier storage, variable by the MEMORY GATE WIDTH control, assures that Q214 will stay at saturation for typically 0.4 μ sec. As the collector of Q214 falls, D216 and R216 critically damp the Memory gate transformers to prevent ringing.

Sampler Controls

The Gate Generator subchassis contains nearly all internal adjustments that control the sampling efficiency and loop gain; they are: SNAP-OFF CURRENT, MEMORY GATE WIDTH, A BRIDGE VOLTS, A and B BRIDGE BAL, and A and B RISETIME BAL controls. Note that there is no B BRIDGE VOLTS control. The bridge bias volts of Channel B is fixed, and the A BRIDGE VOLTS control allows the bridge bias volts of Channel A to be adjusted so both channels perform with the same risetime.

Two other controls in each channel affect the system operation. Each Memory subchassis has a LOOP GAIN and a SMOOTHING BALANCE control. Their functions are described with the Memory circuit description.

Preamplifier

The Preamplifier consists of two cascaded amplifiers, V114A, and the combination of V114B, Q124, and Q123. V114A is a voltage amplifier with a variable plate load, the SMOOTHING control. V114B, Q124, and Q123 form an operational amplifier with a high voltage gain. The supply voltage for V114A, and the first two elements of the operational amplifier, is double decoupled from the +125-volt supply. The entire amplifier negative return is to the -12.2-volt supply, and the collector supply of Q123 is decoupled from the +20-volt supply.

Preamplifier gain is best described as voltage input and current output. If the input grid of V114A receives 0.1 volt, its plate will drive 0.5 ma to the operational amplifier (if the SMOOTHING control is fully counterclockwise at full gain). The operational amplifier has a virtual ground input impedance due to the feedback from the emitter of Q123. The internal-loop of the operational amplifier drives the base of Q123 about 2 volts for each input 0.1 ma at the grid of V114B. (2 volts across R123 equals 0.1 ma through R123 to the grid of V114B.) With 0.1-volt input, the preamplifier output will be 10 volts.

Sampling efficiency of the P6038-Type 3S3 is about 10% or less. Under ideal conditions, about 10% of the signal at the probe tip reaches the grid of V114A. Signal source capacitance, and/or operation for fast-rise signals, can reduce the sampling efficiency to about 2%. Thus, with a 1-volt signal at the probe tip, the input signal to V114A can be between about 20 mv and 100 mv.

Signals from the probe are fast pulses, one each time a sample is taken. Right after the grid of V114A has responded to the signal, feedback from the Memory sets the input voltage level equal to the true signal value.

The bypass capacitor C117 in the cathode circuit of V114A, and the coupling circuit between V114A and V114B, differentiate both the signal and the feedback, thus allowing the circuit to return to equilibrium before the next sample is taken.

Fast positive input signals turn on Q123 in normal forward bias fashion. Fast negative going signals may turn Q123 off faster than its emitter can fall, in which case D123 conducts and drives the emitter negative at the signal rate.

The Preamplifier output is ac coupled to the Memory subchassis through a section of the MV/DIV switch. The system, including the Preamplifier output, the MV/DIV switch and the Ac Amplifier (Memory subchassis), is shown in Fig. 3-5.

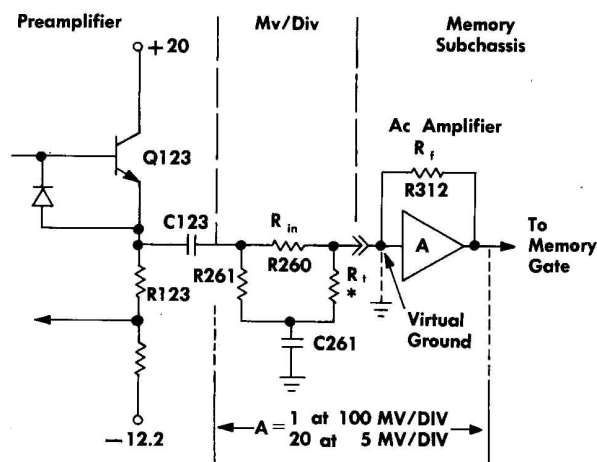


Fig. 3-5. Simplified connections from Preamplifier output to (Memory) Ac Amplifier input. * R_T = Parallel value of all other R260 and R261 resistors.

AC Amplifier

The Input circuit of the Memory subchassis is a two-transistor operational amplifier with its gain controlled by the MV/DIV switch resistance in series with the base of Q304. The input signal from the Preamplifier always looks into a 1 k load. The series resistor, R_{in} of Fig. 3-5, sets the Ac Amplifier voltage gain according to R_T/R_{in} . When the MV/DIV switch is at 5, R260E (1 k) sets the voltage gain at 30. When the MV/DIV switch is at 100, R260A (21 k) sets the voltage gain at 1.5. The resistor R_T of Fig. 3-5 has no significant effect upon the circuit because it is in parallel with the virtual ground input resistance of the Ac Amplifier.

The input of the Ac Amplifier rests about -0.3 volt from ground which requires ac coupling of the 1 k resistance to ground of the MV/DIV switch (C261). Thus, the signal differentiation by C123 and the 1 k value of the MV/DIV switch is accomplished at the voltage of the Ac Amplifier input.

The Ac Amplifier output is set by R313, the LOOP GAIN control. R313 is adjusted during calibration so the system loop gain (dot transient response) is correct for 50 Ω source impedance signals at the tip of the P6038 Probe when the SMOOTHING control is fully counterclockwise and the Noise-Risetime switch is at FAST RT.

The signal pulses handled by the Ac Amplifier are about 0.5 to 1 μ sec in duration. The amplifier output voltage can

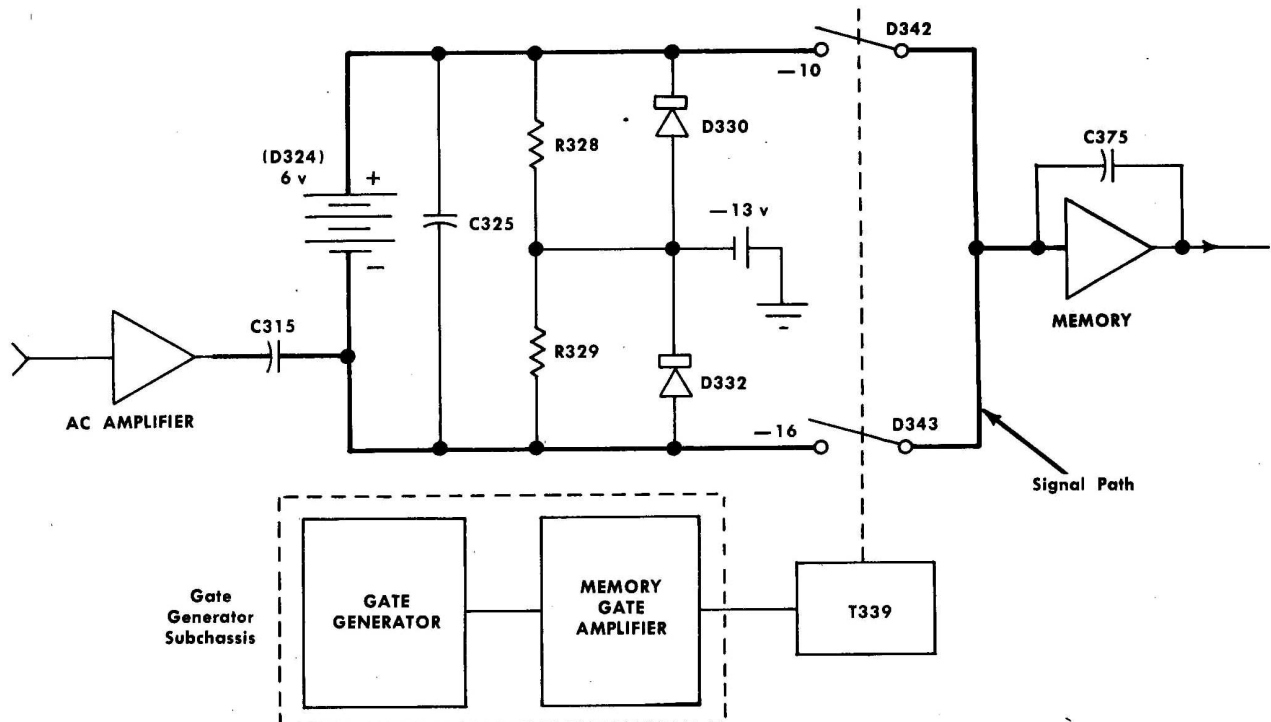


Fig. 3-6. Simplified memory gate.

change a maximum of about 2 volts in about 0.1 μ sec. Normally the system causes the output pulses to be less than 1 volt, but if the display moves 8 divisions in one sample, the output pulse will be about 1.6 volts peak. The output impedance of the circuit is low enough to charge C315 during the time the Memory Gate conducts.

Memory (Series B, Model 1)

A simplified schematic of the Memory circuit is shown in Fig. 3-6. Refer also to the Memory schematic at the back of this manual. The Gate Generator closes the Memory input gate diodes D342 and D343 at the correct time of each sampling cycle. The Memory circuit is a feedback amplifier (integrator) with input and feedback elements both capacitors. The input capacitor is C315, the feedback capacitor is C375. V353 is an input cathode follower, Q364 is the amplifier, and Q374 is an output emitter follower.

The input impedance at the grid of V353 acts as a virtual ground because as the input signal changes the grid voltage, the signal is amplified and applied back to the input as negative feedback to cancel the original change.

The action of the Memory is to transfer a charge from C315 to C375. The circuit between the Ac Amplifier output and the grid of V353 looks like 200 Ω and 510 pf in series (when the Memory gate is conducting). Thus, as a signal appears at the Ac Amplifier output, C315 is charged. C315

tries to couple the signal to the grid of V353, but feedback prevents the grid voltage from changing significantly; the result is for both C315 and C375 to receive a charge.

When the Memory gate is not conducting, the grid of V353 has a very high impedance to ground, and at this time the only possible discharge path for C375 is by V353 grid current or stray leakage current. The grid current and total leakage current is so low that there is essentially no change in the output voltage between samples even when sampling at the low rate of 150 times a second.

The circuit elements between C315 and the grid of V353 serve several purposes:

1. D330 and D332 are amplitude-limiting diodes. They normally do not conduct.
2. D324 is a 6-volt Zener to provide back-bias for the gating diodes D342 and D343.
3. The resistors all aid in setting the input quiescent voltage level.
4. T339 is a pulse transformer that allows rapid turn-on of the gating diodes to connect the input circuit to V353.
5. C325 assures that both sides of D324 follow the signal equally.

Within the Memory amplifier:

1. C365 corrects for transistor phase shift.

Circuit Description—Type 353

2. D362 is positive signal overload protection for Q364.
3. D372 assures that fast negative signals at the base of Q374 will be coupled to C375 and the output, even if Q374 is momentarily cut off.
4. The maximum positive swing of the output lead can be about +20 volts. The maximum negative output can be about -12 volts.

Between samples, the Ac Amplifier output returns to its quiescent level, and any C315 charge (that was gained at the last sample) is cancelled. At the next sample (if there is any change at the Preamplifier input), C315 will receive a new charge and can add to or subtract from the residual charge of C375. C315 is charged by the Ac Amplifier only when the memory gate is conducting.

System Operation With No Signal

Items to remember when examining signals at various points between the Preamplifier output and the Memory output:

1. It is impossible to install perfectly balanced sampling gate diodes, so at each Gate Generator pulse there will be some small error signal sent into the system.
2. The Memory circuit does not retain a perfectly stable output voltage because C375 cannot hold a charge permanently.

3. The Memory output is coupled back to the Preamplifier input (with proper attenuation).

4. Theoretically, if there is no input at the sampling gate, there will be no Ac Amplifier signal, and the Memory output will be zero. The Memory output will be essentially zero, but there will always be a small pulse at the Ac Amplifier output.

5. The SMOOTHING BALANCE control (R355) sets the quiescent dc level at the Memory input and if incorrectly adjusted will cause an offset voltage that looks like a continuous signal. For example, assume the SMOOTHING BALANCE control is off by +1 mv. If the Memory amplifier internal gain is 500 (it isn't actually), the Memory output will now be off by -500 mv. The -500-mv feedback to the input bridge creates an error signal which will drive the Memory output nearly back to zero. After several dots the Memory output will stabilize near zero, but slightly off from zero to provide enough error signal to correct for the original 1-mv error. Thus, a continuous minor error signal is amplified to place the output level near zero. If the Preamplifier gain is reduced by the SMOOTHING control, the Memory output must now be larger so the error signal fed into the Ac Amplifier is larger, restoring again the -1-mv correction at the Memory input. A trace shift seen when the SMOOTHING control is rotated is the increased Memory output to make up for the reduced amplifier gain. Thus, the Memory input balance control is called the SMOOTHING BALANCE because its effect is seen by rotation of the SMOOTHING control.

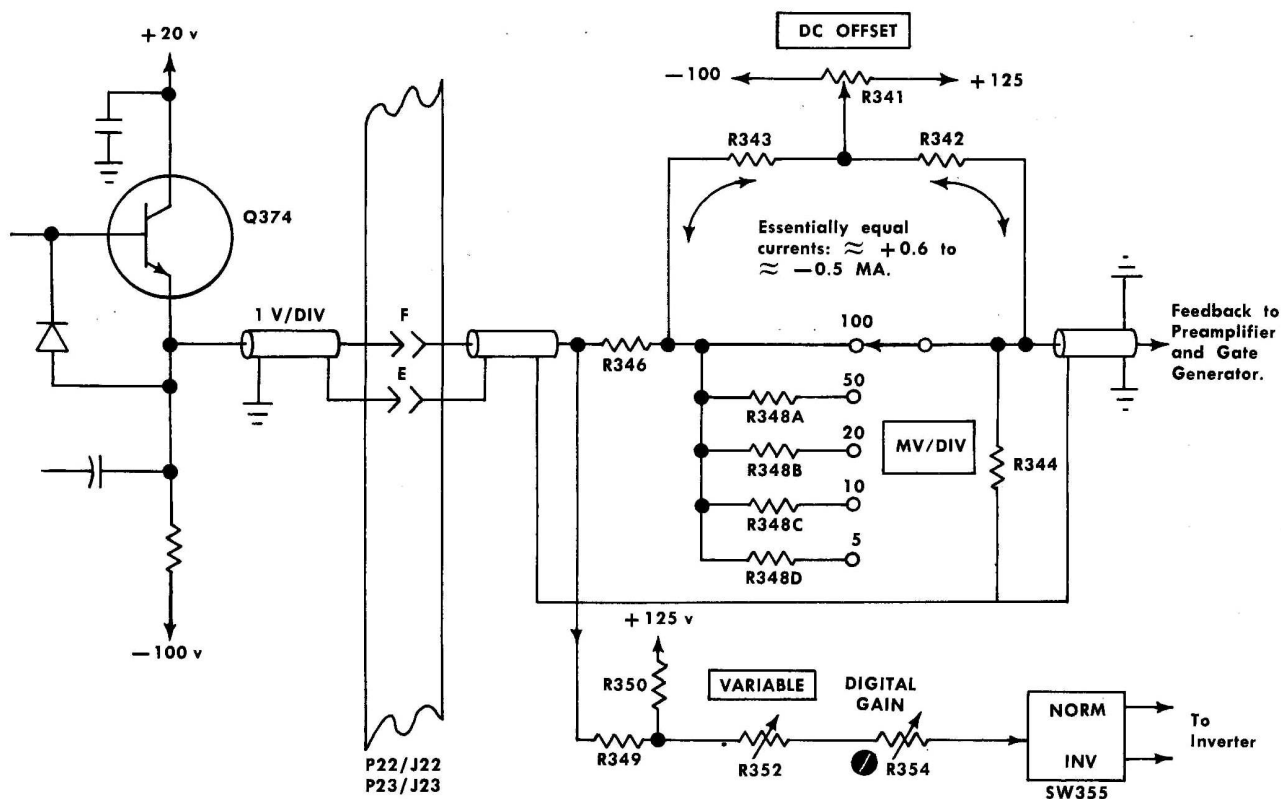


Fig. 3-7. DC OFFSET and MV/DIV circuit from Memory output to feedback and Inverter circuits.

DC Offset

The Memory output of Q374 is fed to the Inverter circuit. It is also fed to a voltage divider of the MV/DIV switch that controls the feedback signal sent to the Preamplifier and Gate Generator. The feedback attenuator resistors (R348, A through D, Attenuator Switching diagram), set the feedback amplitude to keep the basic Memory output at 1 volt/division while the feedback voltage just matches the input signal.

The Dc Offset circuit adds a dc shift to the feedback loop. It includes a current cancelling system that prevents offset current from flowing in R348; see Fig. 3-7. Rotating the DC OFFSET control from one end to the other causes equal currents to be injected at both sides of the MV/DIV feedback

divider. The resulting voltage drop of ± 0.5 volt across both R344 and R346 is the offset voltage sent to the Preamplifier and Gate Generator. The two points of offset injection assures there is essentially no offset current in R348 so that the offset system is not affected by changing the setting of the MV/DIV switch.

The DC OFFSET control may be used to extend the range of the POSITION control for signals with a dc component up to ± 0.5 volt.

Inverter (Series C, Model 1)

The Inverter includes two operational amplifiers for each channel. The function is to invert the display when the front-panel NORM-INV switch is in the INV position. When

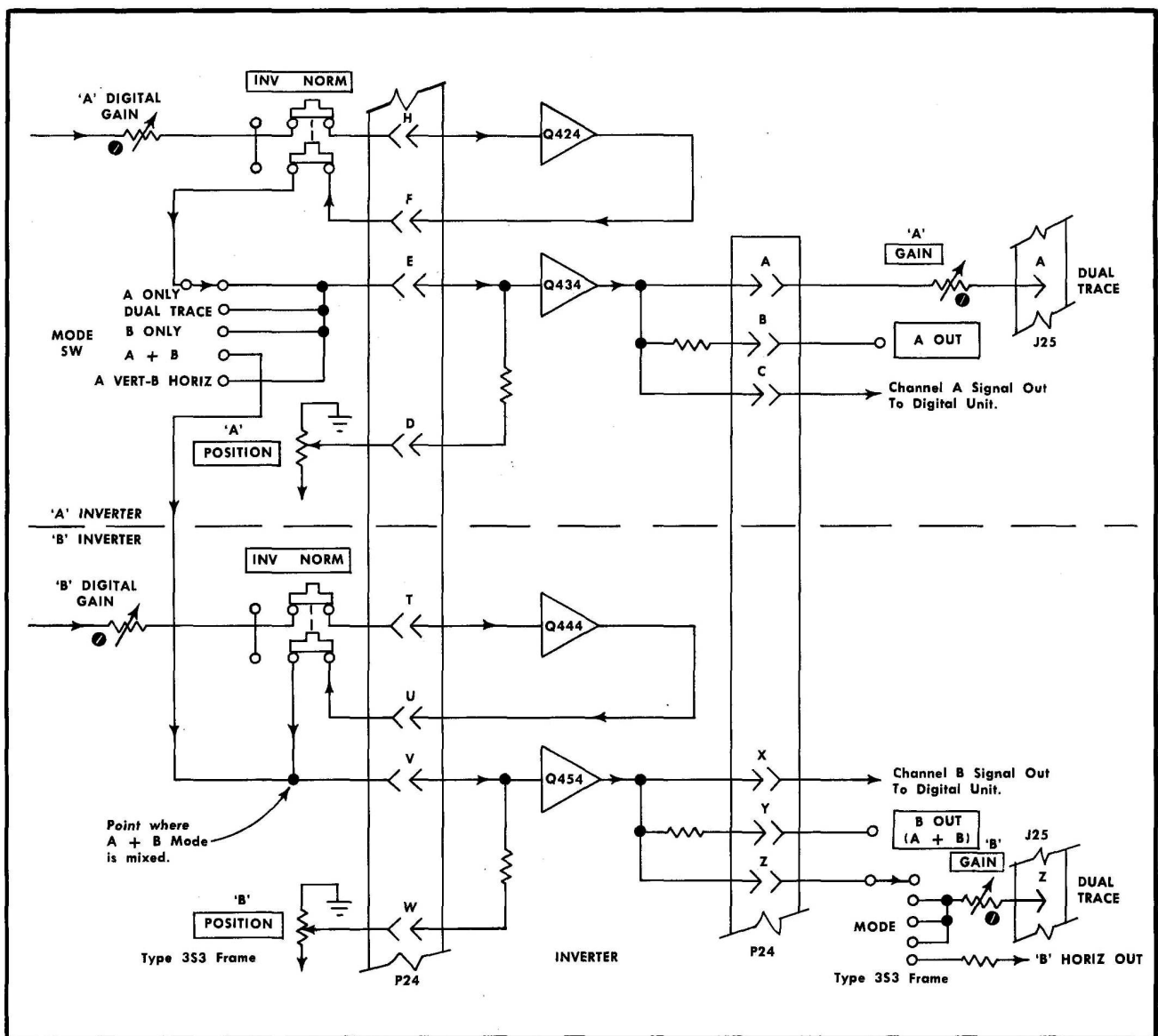


Fig. 3-8. Interconnections for Inverter subchassis.

Circuit Description—Type 353

the switch is in the NORM position, both amplifiers are used in cascade. Switching and interconnections are shown in Fig. 3-8 and on the Interconnector Diagram at the back of this manual.

Each amplifier has a current injection system at the transistor base for changing the dc level of the output signal. The INVERTER ZERO control is the current injection of the first amplifier. It is used to set the input and output voltage equal (essentially zero). As an example, Q424 collector rests at about +20 volts. Zener diode D424 lowers the voltage to near zero without attenuation. Then the INVERTER ZERO control injects a small current at the base of Q424 to alter the output voltage a bit to allow for variation in components and input voltage. Thus, the first amplifier can be switched in or out of the circuit without changing the vertical position of a centered display. The current injection of the second amplifier is the front-panel POSITION control. The output voltage of each second amplifier (Q434 and Q454) is at about +10 volts.

All four amplifiers are simple operational amplifiers. The gain is set by the ratio of the feedback resistance to the input resistance. Each stage has essentially 12.1 k input and feedback resistance. The signal input current is equal to the feedback current, and the base impedance of each transistor is then a virtual ground. Thus, the resistance of the current injection circuits just discussed does not affect the signal source impedance and therefore does not affect the stage gain.

The gain of the first amplifier (Q424 and Q444) may not be unity. The gain is set by the 12.5 k feedback resistor and the series value of R349 at the Memory output (1 k), R352 (VARIABLE control at CALIB, 10 k), and the DIGITAL GAIN control. The total of these three resistors will be between about 11 k and about 13.5 k depending upon the Memory output at unity loop gain.

The gain of the second amplifier (Q434 and Q454) is unity when fed from the first amplifier. Channel A gain is set by R429 and R435. The gain of the second amplifier will be the same as the first amplifier when the NORM-INV switch is at INV because its source resistance is then the input system from the Memory.

The DIGITAL GAIN control allows setting the system gain, from the probe tip to the Inverter output, to the correct value for operation with a digital plug-in unit in the Type 567 Oscilloscope. It also affects the display amplitude, but the display amplitude is then adjusted to match the digital unit readout by the front-panel GAIN control.

Operational amplifiers can be used as signal adders. More than one input can be paralleled at the virtual ground base impedance of Q454. When the Mode switch is set to A + B, both channel signals enter the base of Q454 and are added. If one channel NORM-INV switch is at INV, then the signals subtract. Under this mode of operation, the Channel A POSITION control does not affect the display (see Fig. 3-8). Both switches operate, and the single-trace algebraic display is positioned by the Channel B POSITION control.

Output of both channel Inverters at Q434 and Q454 goes to three 10 k loads. They are the Dual Trace subchassis, the front-panel output terminal, and the digital unit.

Each output can work into a very low impedance because the feedback within the operational amplifier makes its collector output impedance very low.

Dual Trace (Series D, Model 1)

The Dual Trace subchassis determines which channel is displayed, or that both are displayed. Because of the various modes of operation possible, both the A and B channels will be discussed.

The signal of both channels enter the emitter circuits of separate common-base stages Q514 and Q524 that have a single and shared collector load at the input to the Vertical Amplifier. Which channel is displayed is determined by the Mode switch and the conduction of Q545 or Q555. Q514 and Q524 always conduct the same current, and the signal is either passed to the Vertical Amplifier or bypassed to the clamping circuit of Q545 or Q555.

During single-channel displays (A ONLY, B ONLY, A + B or A VERT B HORIZ), only one clamping transistor conducts. Q555 conducts for the A ONLY and A VERT B HORIZ modes, Q545 conducts for the B ONLY and A + B modes, and Q545 and Q555 become a bistable multivibrator, triggered by Q570 for DUAL-TRACE operation.

The output voltages of the INVERTER subchassis rests at +10 volts and are 'modulated' by signal currents. Each Dual-Trace common-base stage has about 10 k between the Inverter and the emitter of the stage (front-panel GAIN control in series with R513). Thus, each common-base stage conducts 1 ma steady dc and 100 μ a/div signal current. (Memory output is 1 volt/div; Inverter output is 1 volt/div into 10 k. Thus, signal current is 0.1 ma or 100 μ a/div at the input to the common-base stages.)

Fig. 3-9 shows dc current flow paths for the common-base amplifiers for A ONLY operation. Voltages for A ONLY operation are included on the Dual Trace Schematic. The transistor for the channel not displayed, Q514 of Fig. 3-9, does not saturate when its output is channeled through D516. It must not saturate or dual-trace switching transients would be sent back to the Inverter and cause excessive display noise. The combined voltage drops across D557 (at the collector of Q555) and D516 assure that the collector voltage of Q514 will always be negative with respect to its base, therefore not saturated. B ONLY operation current flow is the reverse of that shown in Fig. 3-9.

Dual-Trace Operation

The Type 353 switches between channels at every sample when operated in the Dual-Trace mode. Q545 and Q555 operate as a nonsaturating bistable multivibrator that switches at the sampling rate. Basically its frequency is about 50 kc if the timing unit triggering signal is 100 kc or greater; less than 50 kc if the triggering signal is less than 100 kc.

The multivibrator is switched by triggers from the blanking oscillator Q570. The triggers are negative pulses from the grounded winding of T570, each time the blanking oscillator is triggered by the Gate Generator. The trigger pulses are ac coupled to the base of the off transistor (Q545 or Q555) to turn it on and cause the multivibrator to switch.

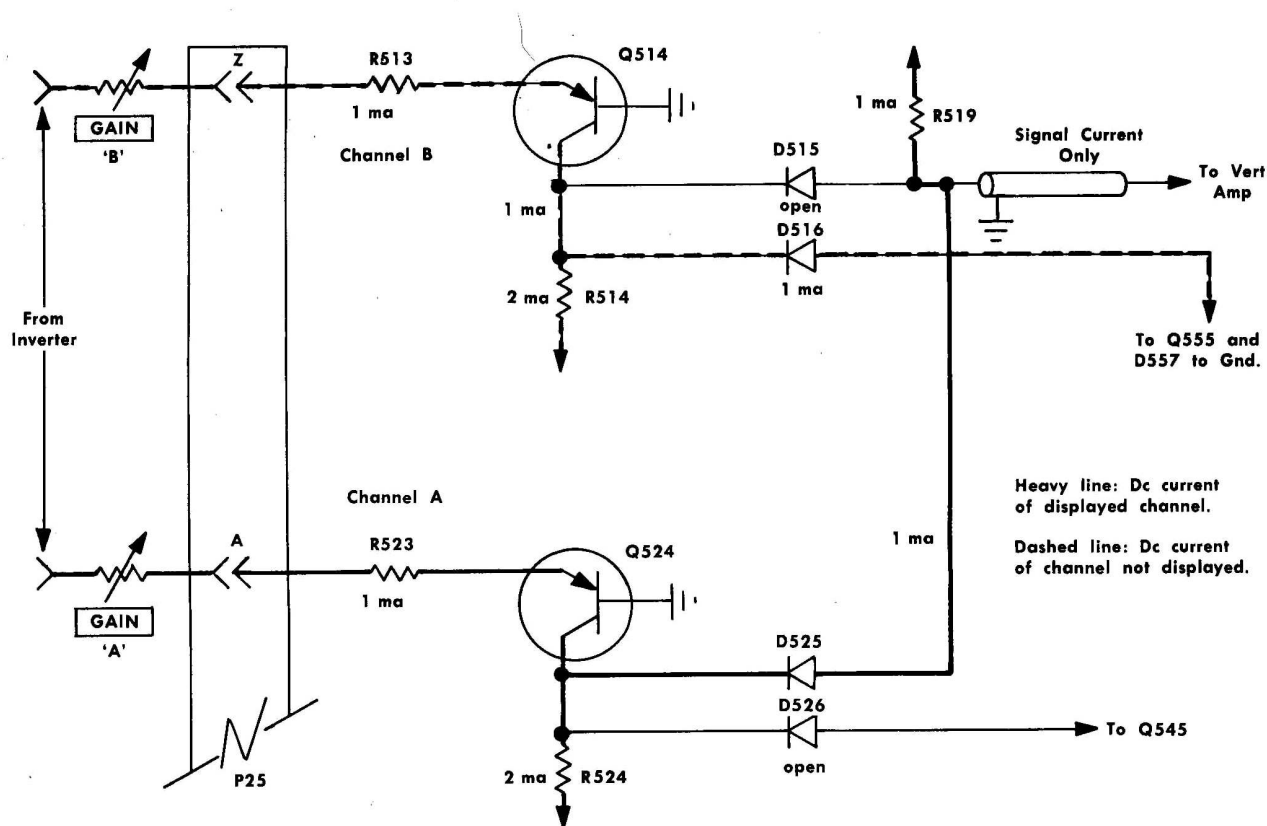


Fig. 3-9. Current flow of Dual Trace common base amplifiers for A ONLY operation.

Blanking Oscillator

The blanking oscillator is active in all modes of operation to blank the oscilloscope crt each time a sample is taken and the display dot is moved. Thus it serves well as the blanking system for Dual-Trace operation.

The blanking oscillator is triggered into conduction by the memory gate width circuit of the Gate Generator. The Gate Generator pulse does not last long enough to properly blank the crt so the blanking oscillator pulse lasts about 4 μ sec.

Before Q570 is triggered it is cut off by about +0.2 volts at the base. The collector voltage is -38 volts. As the positive trigger pulse arrives, the following takes place.

1. The trigger is transformer coupled (and inverted) to the base to turn on Q570.
2. Regenerative blocking oscillator action follows and the transistor saturates.
3. As the trigger signal stops, the base of Q570 is negative due to stored charge in the emitter-base junction. R571 removes the stored charge slowly, allowing Q570 to come out of saturation slowly and prevent any back-swing of T570. Thus a steady blanking signal of about +38 volts is sent to the oscilloscope crt circuit.
4. At the time the trigger arrives, a sharp negative pulse is sent to the Dual-Trace multivibrator. If the MODE switch

is at DUAL-TRACE, the multivibrator will switch states. Otherwise the trigger has no effect.

Digital Readout Channel Information

Digital Readout amplifier Q564 sends a +2-volt steady signal to the Digital Plug-In Unit when the Type 3S3 displays Channel A and a -1-volt steady signal when Channel B is displayed. It also switches at the Dual-Trace switching rate.

Vertical Amplifier (Series E, Model 1)

The Vertical Amplifier is composed of two operational amplifiers. The first, Q614, Q624 and Q634, has a gain of 110 volts output per ma input. The second, Q654, Q664, and Q674 has a voltage gain of -1.

The output voltage of the Dual Trace subchassis and the input of the Vertical Amplifier is set by the emitter voltage of Q614. The base of Q614 is the collector load for the two common-base dual-trace amplifiers.

The input circuit of Q614 includes a $\div 5$ TRACE FINDER push button. The Trace Finder switches the Dual-Trace output from a direct connection to the base of Q614, to a 5:1 resistive divider R607 and R608. Since both sides of the divider are at -12.2 volts, no dc current flows in the divider.

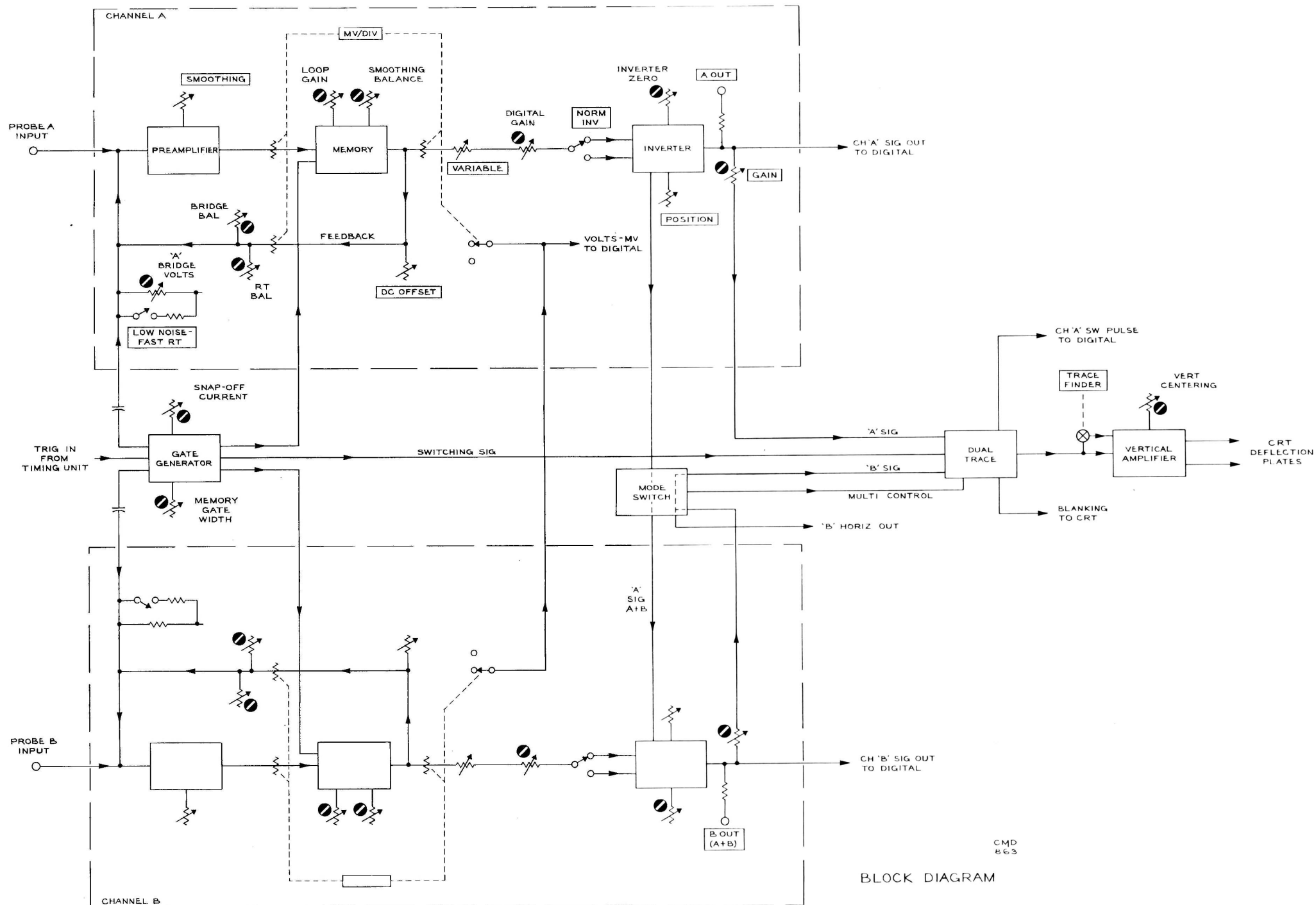
Circuit Description—Type 353

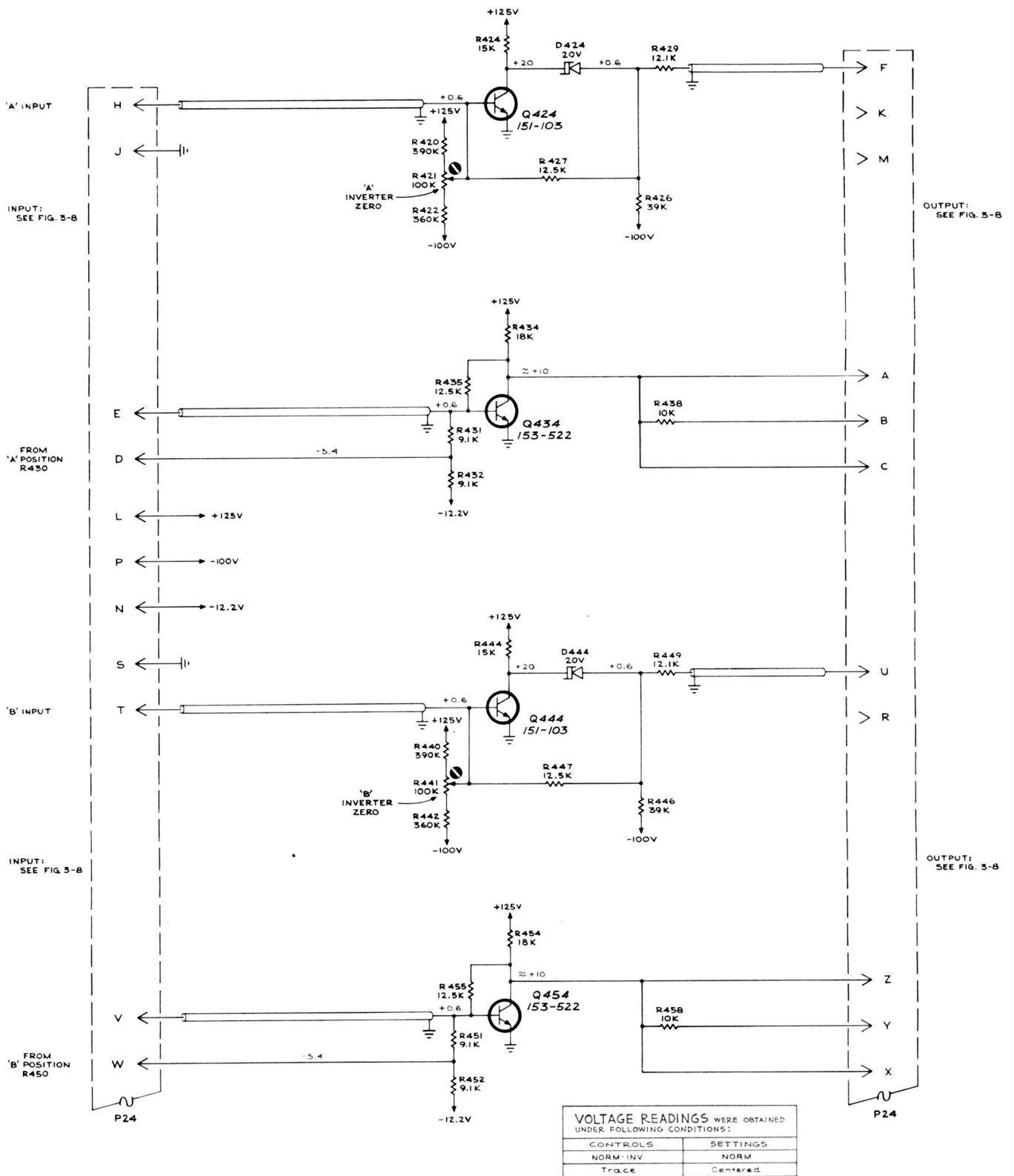
The input voltage level of the Vertical Amplifier is a combination of two silicon junction drops, D612 and the emitter-base junction of Q614. The Vertical Centering circuit, R610 and R611, set the current at the base of Q614 so that zero current from the Dual Trace circuit centers the trace. The current path is from the emitter of Q634, through R619, D612, and the Vertical Centering resistance. The total current with the trace centered is about 1.8 ma, enough to make the voltage drop across D612 equal and opposite the forward voltage drop of the emitter-base junction of Q614.

In making voltage measurements within the Vertical

Amplifier, all but one (as listed in the schematics) remain very stable with a stable trace position. However, the voltage at the collector of Q614 drifts nearly 0.5 volt if the trace is moved from center to either the top or bottom of the graticule. The drift is due to a thermal change in D615, but since it is at the high-impedance collector of Q614, there is essentially no change in current drive to the emitter of Q624. The drift is normal and should not be considered.

The Vertical Amplifier push-pull output is about 185 volts peak-to-peak for 8 divisions of trace shift. The signal input current for 8 divisions of trace shift is slightly less than 1 ma.

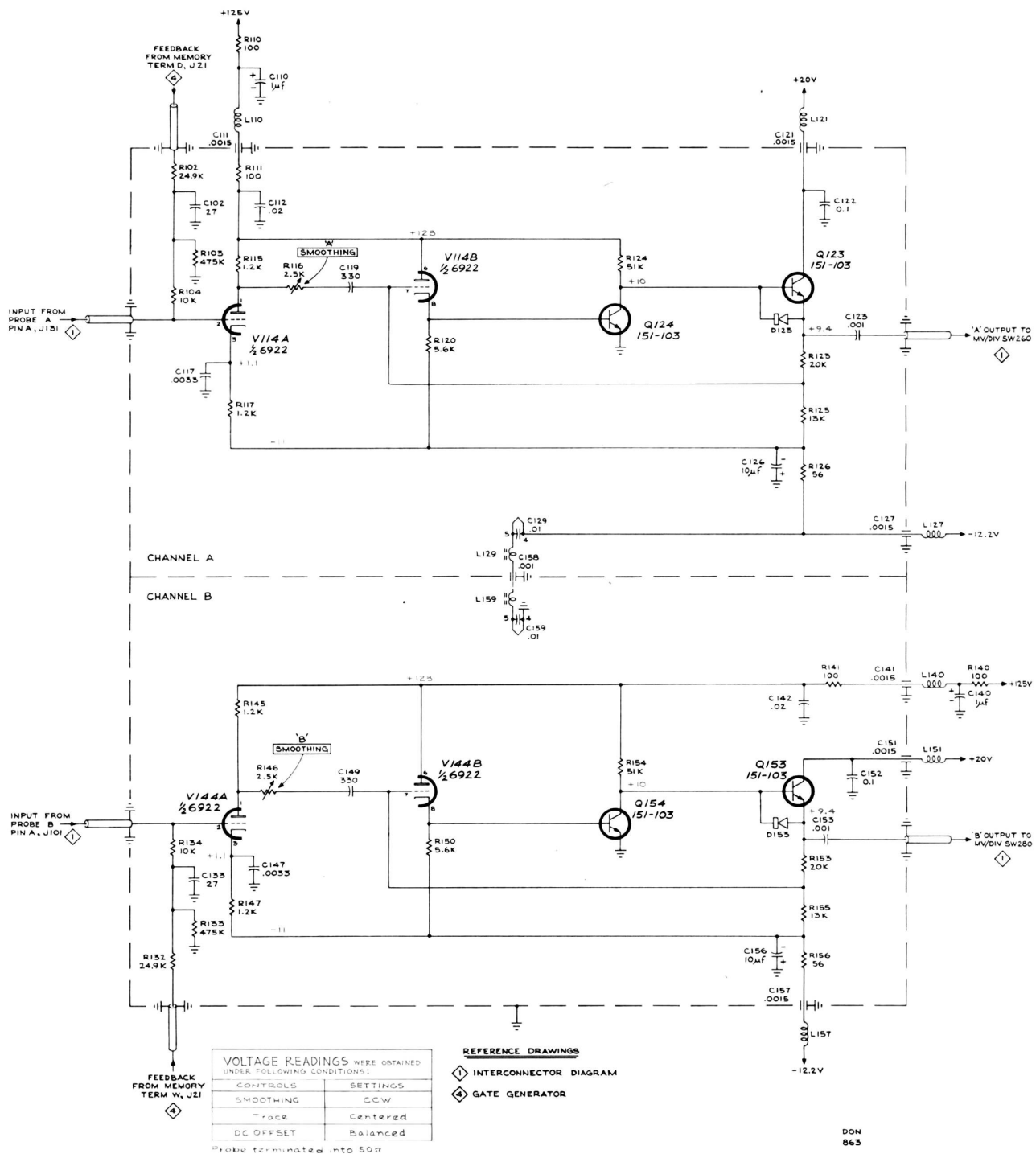


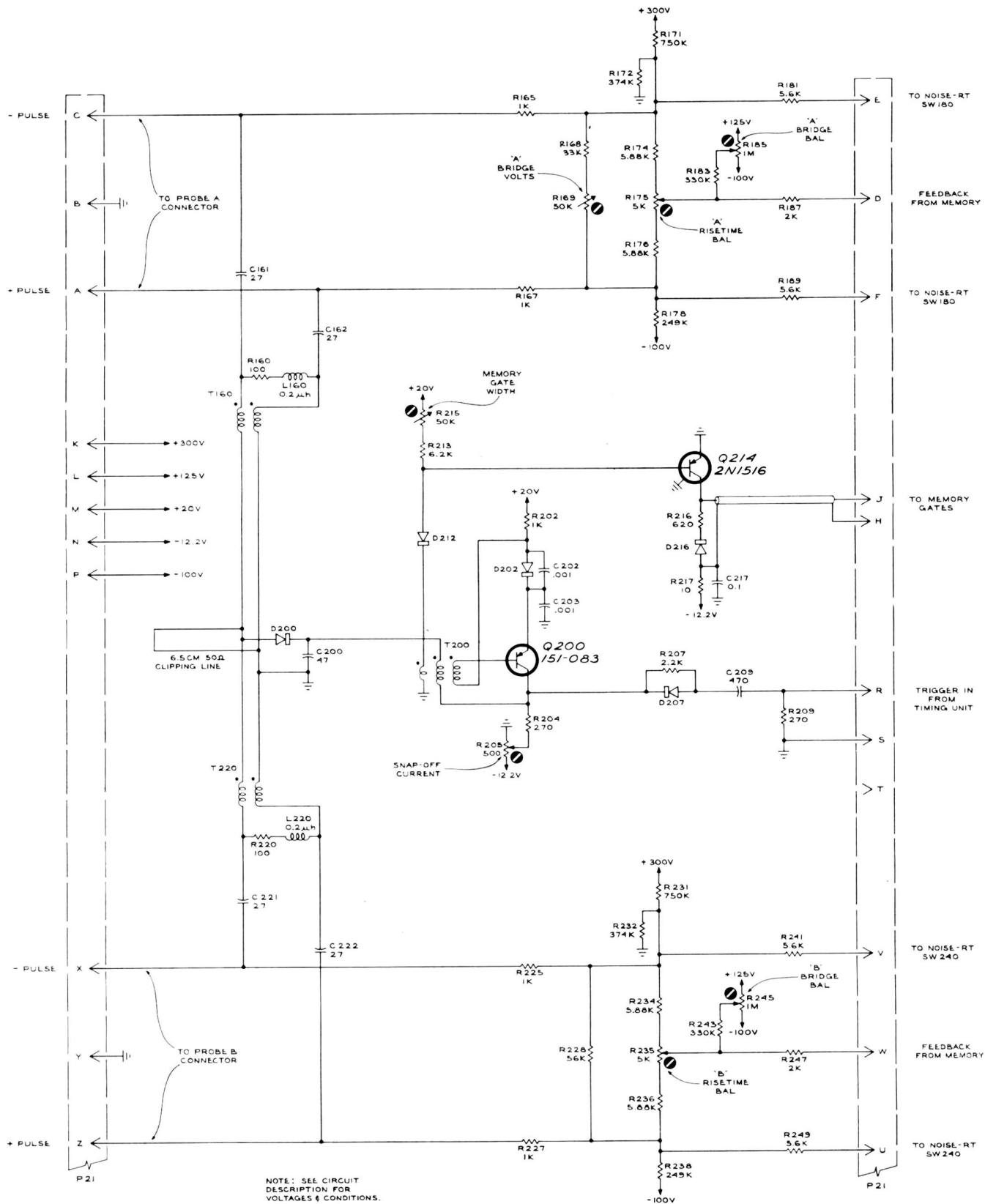


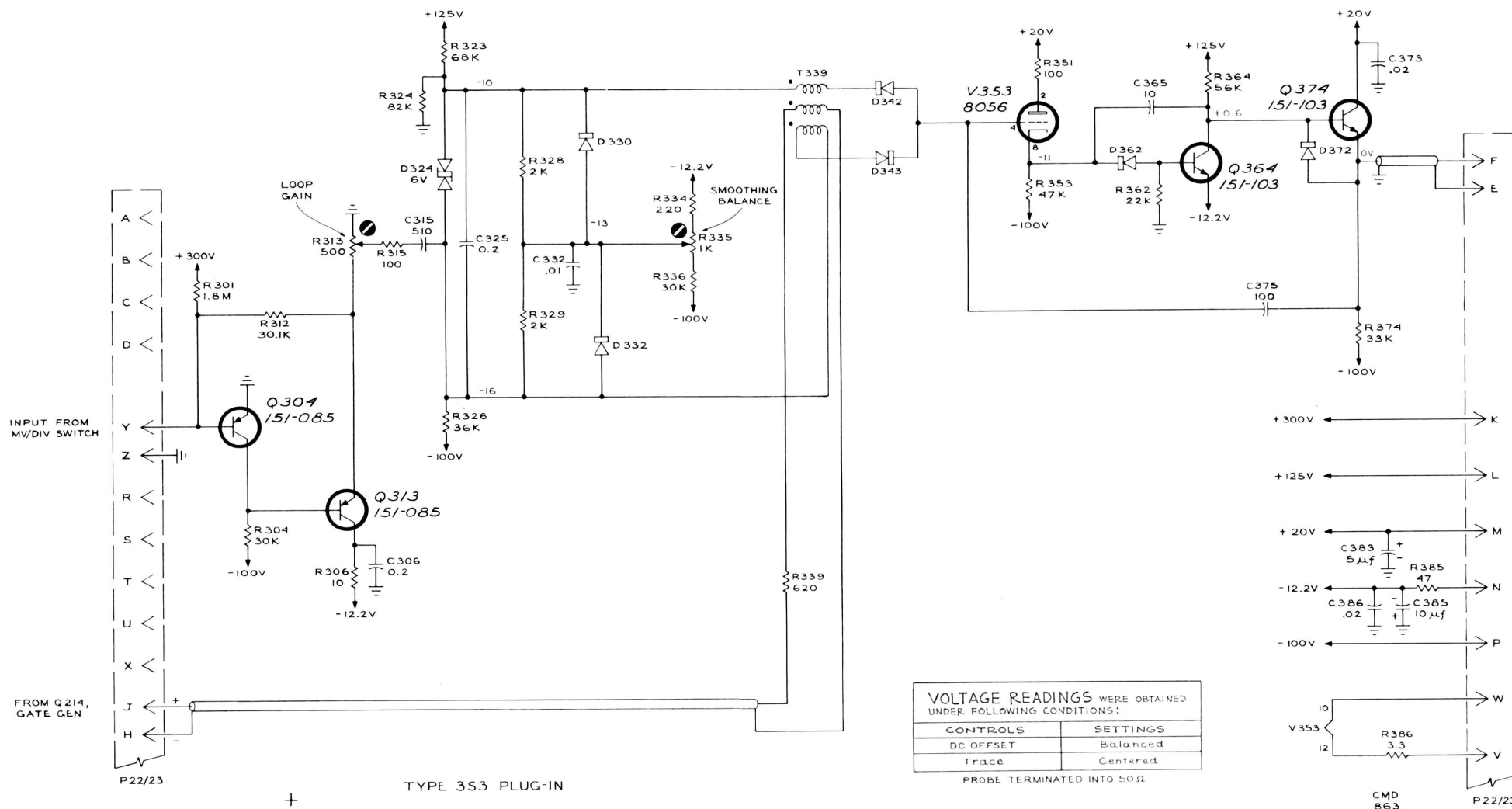
TYPE 3S3 PLUG-IN

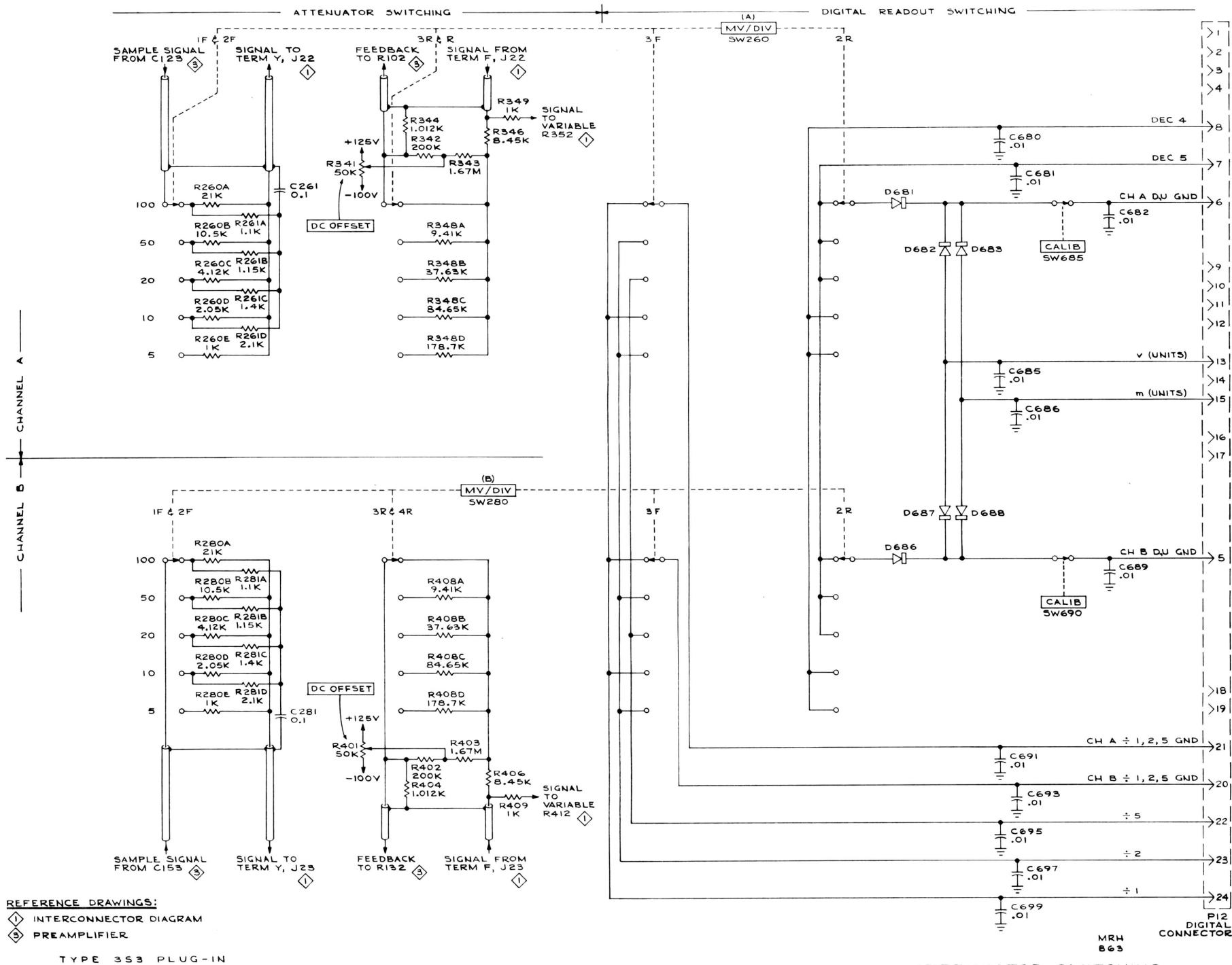
A

INVERTER
SERIES-C
MODEL-I







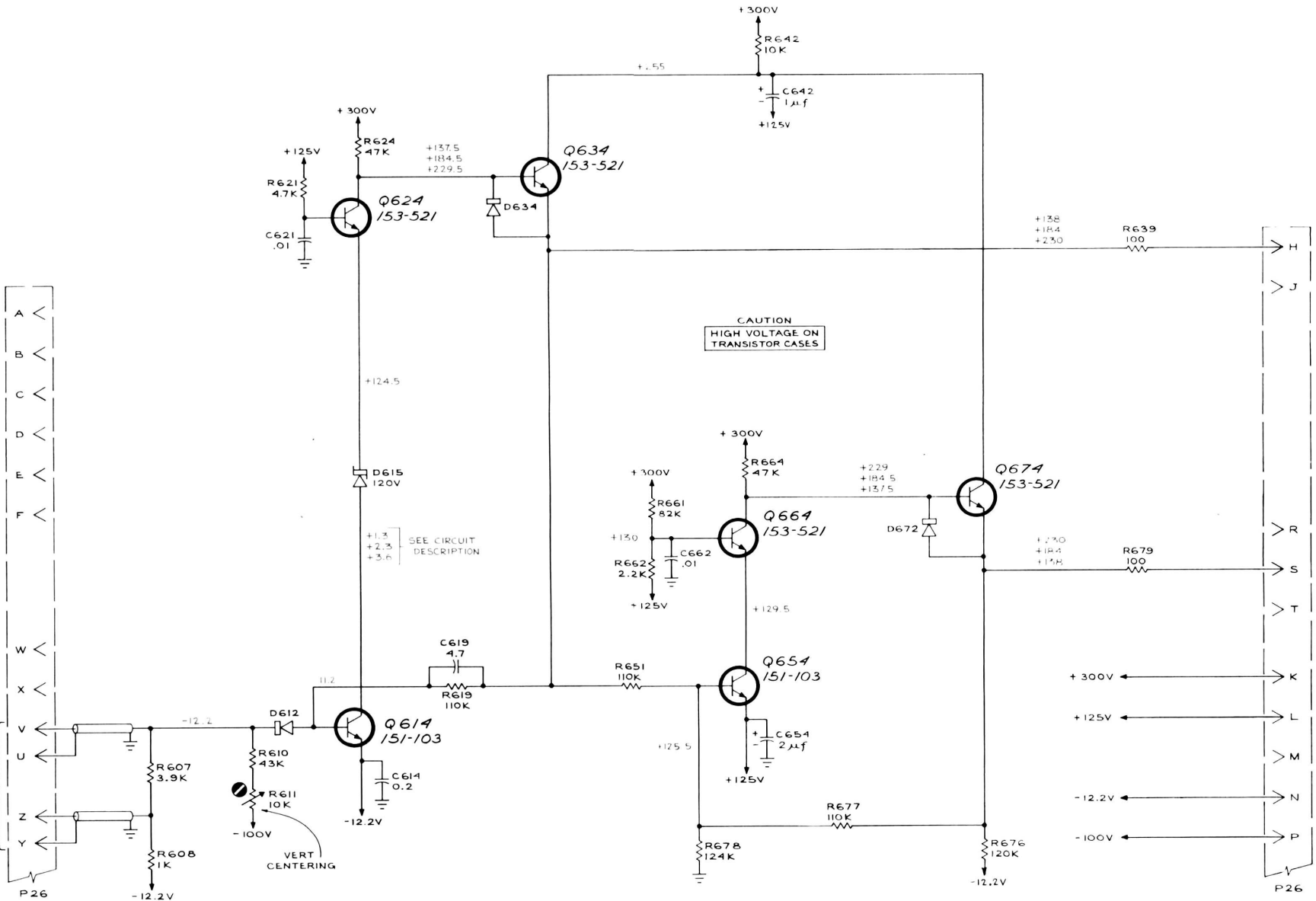




A

INPUT FROM
DUAL-TRACE
& TRACE FINDER
SW 605

A <
B <
C <
D <
E <
F <
W <
X <
V <
U <
Z <
Y <
P26



VOLTAGE READINGS WERE OBTAINED
UNDER FOLLOWING CONDITIONS:

CONTROLS	SETTINGS		
Trace	UPPER + 4 div	MID centered	LOWER - 4 div

CMD
863

VERTICAL AMPLIFIER
SERIES-E
MODEL-1

TYPE 3S3 PLUG-IN

TYPE 3S3

PARTS LIST CORRECTIONS

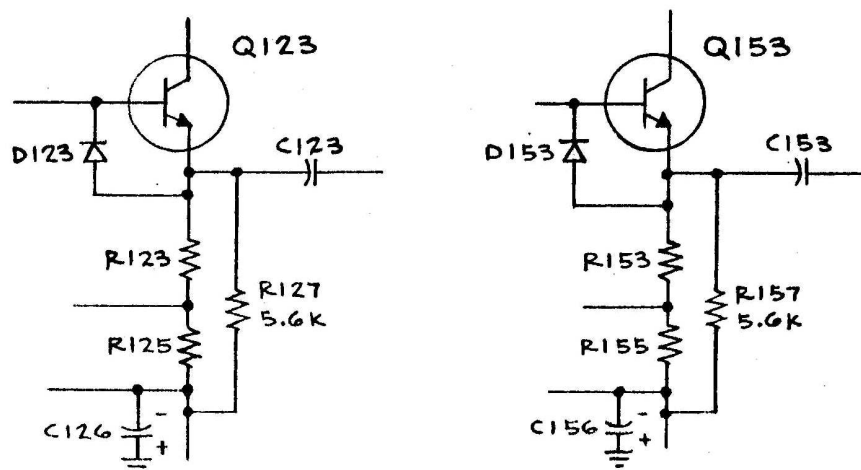
CHANGE TO:

C200	281-504	10pf	Cer	500v	(GATE GENERATOR BOARD)
R124	301-223	22k	1/2w	5%	
R154	301-223	22k	1/2w	5%	
R204	308-231	220Ω	3w	5%	(GATE GENERATOR BOARD)

ADD:

R127	315-562	5.6k	1/4w	5%	
R157	315-562	5.6k	1/4w	5%	
R433	315-102	1k	1/4w	5%	(INVERTER BOARD)
R453	315-102	1k	1/4w	5%	(INVERTER BOARD)

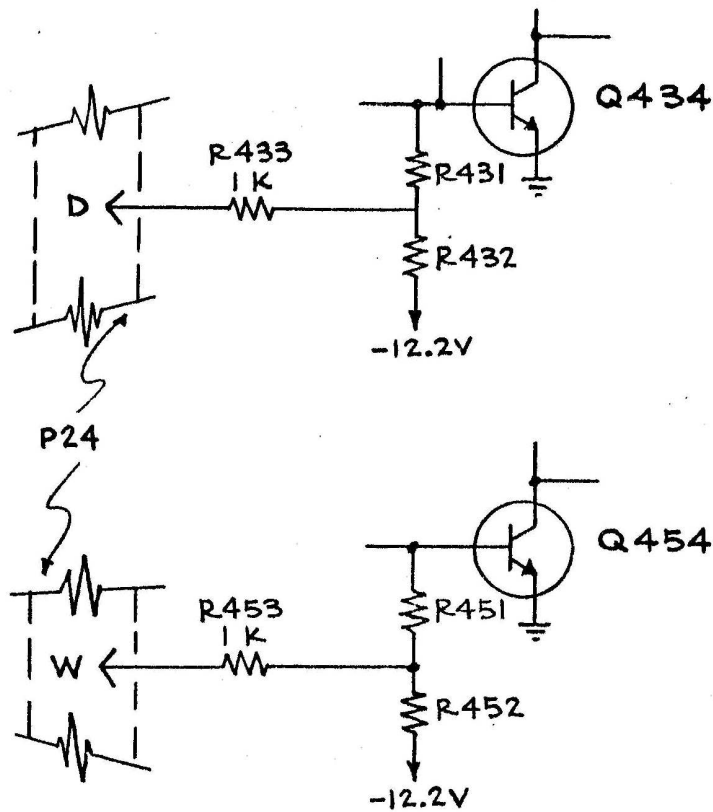
SCHEMATIC CORRECTION



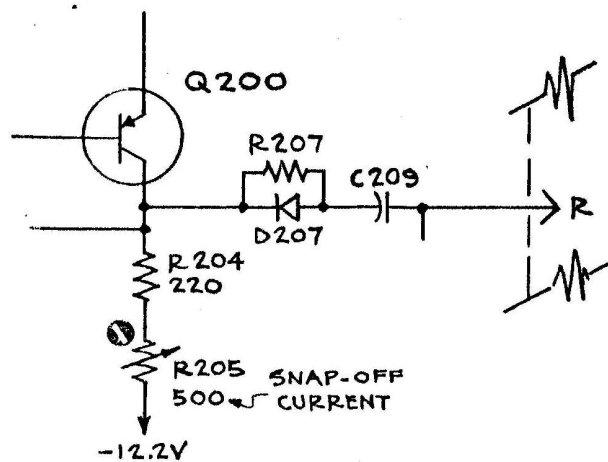
PART. PREAMP. DIAG.

TYPE 3S3

SCHEMATIC CORRECTIONS



PART. INVERTER DIAG.



PART. GATE GEN. DIAG.