INSTRUCTION MANUAL

Serial Number 307

TYPE 3B2
TIME BASE

Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon ● Phone MI 4-0161 ● Cables: Tektronix

Tektronix International A.G.
Terrassenweg 1A ● Zug, Switzerland ● PH. 042-49192 ● Cable: Tekintag, Zug Switzerland ● Telex 53.574

070-355 1063


TYPE 3B2 TIME BASE
TRIGGER
LEVEL
COUPLING
AC SLOW
AC FAST
DC
SLOPE
SOURCE
INT
LINE
EXT
EXT TRIG IN
RUN
DELAY TIME
DEL'D TRIG OUT
DELAY
SWEEP DELAY
IN
OUT
SWEEP + GATE OUT
DIGITAL RESOLUTION
SWEEP
TIME/DIV
mSEC
POSITION
SEC
SWEEP CAL
SERIAL
TEKTRONIX, INC
ORTLAND, OREGON, U.S.A.

SECTION 1
CHARACTERISTICS

General Information

The Type 3B2 Time Base Unit is used to generate sweeps for the Type 560-Series oscilloscopes. The sweeps may be initiated immediately by the trigger pulses or they may be delayed a selected time (from 5 μsec to 10.5 sec) after the trigger pulses. The unit provides outputs for digital unit displays as well as the usual analog displays. The unit can be used with any of the Type 560-Series oscilloscopes except the Types 560, 565, and RM565.

Sweep Rates

Sweeps from 2 μsec/div to 1 sec/div in 18 calibrated steps. Accurate to ±3%.

Delay Time

A 6-position delay-time switch and precision dial multiplier provide sweep delay from 5 μsec to 10.5 sec. Accurate to 1.0%.

Triggering Modes

Ac slow, ac fast, or dc coupled: + or — slope, internal, line, or external source.

Trigger Signal Requirements

Internal Triggering: Minimum signal amplitude of 2 minor divisions on the crt.

External Triggering: 0.5-volt minimum signal.

Trigger Frequency

Dc to 30 mc. (Internal trigger frequency limited to 500 kc when used with Type 3A2 Dual-Trace Amplifier plug-in unit.)

Internal Clock

Clock pulses for the digital readout unit are supplied from a 1-mc crystal-controlled oscillator. Frequency tolerance is ±0.01%.

Sweep Gate Out: +15-volt signal.

Delayed Trigger Out: +6-volt pulse ≈ 0.5-μsec width.

Jitter: Less than 1:20,000.

Mechanical

Construction: Aluminum-alloy chassis.

Finish: Photo-etched, anodized panel.

Weight: 5 lbs.

SECTION 4
CIRCUIT DESCRIPTION

General Information

A block diagram of the Type 3B2 is shown in Fig. 4-1. The Type 3B2 Time Base Unit contains a Trigger Generator, Delay Generator, Sweep Generator, and a Clock Pulse Generator.

The Trigger Generator accepts a signal from one of three sources and converts it (regardless of shape) into a string of fast-rise constant-amplitude pulses that pass to the Delay Generator (see Fig. 4-1).

Usually, not all the pulses passing to the Delay Generator are used. Gating signals prevent pulses from entering the gated multivibrator circuit while the delay-ramp generator or sweep-ramp generator are producing a ramp voltage. Each pulse that enters the multivibrator switches the circuit to produce a square wave. The square wave is coupled to the SWEEP DELAY switch through an integrator that produces a nondelayed trigger pulse. The square wave also passes to the delay-ramp generator. With each square-wave input, the ramp generator produces an output ramp with a rate of rise that depends on the DELAY TIME switch setting. The ramp output is applied to one side of the delay comparator which has a voltage (set by the DELAY TIME dial) on the other side. When the rise of the delay ramp equals the voltage set by the DELAY TIME dial, the comparator switches and a delayed trigger pulse is generated. The delayed trigger pulse passes to the DEL'D TRIG OUT connector and to the SWEEP DELAY switch.

The Delay Generator produces trigger pulses for the Sweep Generator. If the SWEEP DELAY switch is set to OUT, the pulses are not delayed; if set to IN, the pulses are delayed by an amount determined by both the delay-ramp rate of rise (set by the DELAY TIME switch) and the value of the comparison voltage (set by the DELAY TIME dial).

Each trigger pulse passing to the Sweep Generator triggers one sweep. With each trigger pulse, the sweep multivibrator passes a square wave to the sweep-ramp generator producing a ramp that passes to the output amplifier and on to the crt. The Sweep Generator also supplies sweep and + gate signals for the digital unit.

The Clock Pulse Generator operates independently of the other circuits in the Type 3B2. The outputs to the digital unit are controlled by the DIGITAL RESOLUTION switch that determines which of five clock-pulse frequencies is used in the digital unit. The DIGITAL RESOLUTION switch selects the signals needed for setting the decimal point and unit of measure displayed in the digital unit.

TRIGGER GENERATOR

SOURCE switch SW3 selects one of three triggering sources (see foldout schematic): INT (internal triggering), LINE (internal triggering from the line frequency), and EXT (triggering from a signal applied to the EXT TRIG IN connector).

COUPLING switch SW5 selects the type of coupling in the input circuit of the trigger generator. In the DC position, the Trigger Generator can be triggered with a very slowly changing dc level. The two AC positions of SW5 block the dc and very low-frequency ac components of the trigger signal. The AC FAST position uses a high-pass network to trigger on only the high-frequency component of a signal that contains both high and low frequencies.

V13 is a cathode follower that isolates the input from the remaining sweep trigger circuitry. B10 is a neon lamp that protects V13 from excessive input voltage. The output of V13 passes through diode D15 to SLOPE switch SW19 and then to sweep trigger comparator Q24 and Q34. The position of SLOPE switch SW19 determines the connections to the base of Q24 and Q34 and thus determines whether the circuit responds to the negative- or positive-going portion of the input signal.

The signal is applied to one base of the comparator circuit, and an adjustable dc voltage (set by the LEVEL control R23) is applied to the opposite base. Without a signal input, Q34 is turned off. When the signal input reaches a value in excess of the value set by the LEVEL control, Q34 turns on and switches D35 rapidly to its high-voltage state to generate the trigger pulse.

To understand the operation of the comparator circuit, assume that the SLOPE switch is set at + and the LEVEL control is set for about +4 volts. This places +4 volts on the base of Q24. With no input signal present, the base of Q34 normally rests at about +2.2 volts. Under these voltage conditions Q34 will be turned on, and Q24 will be turned off. Q34 turns off when the incoming signal arrives at its base and becomes more positive than the +4 volts on the base of Q24. When Q34 turns off, tunnel diode D35 switches rapidly to its higher-voltage state. The fast transient generated by D35 is coupled to Q44. From Q44 the signal is transformer coupled to the delay generator circuit.

DELAY GENERATOR

The Delay Generator consists of a gated multivibrator circuit, a Miller runup circuit, a delay comparator, and a delayed-trigger generator. The delay generator circuit is always in operation, although it has no affect on the sweep generator when the SWEEP DELAY switch is set to OUT.

Incoming pulses from the Trigger Generator are coupled to the gated multivibrator through T51. The multivibrator is switched only by pulses arriving when Q123 is able to conduct and D55 is set to its low-voltage state. Any pulse arriving under different conditions will not affect the circuit. The output of the multivibrator (collector of Q64) is a negative-going square wave.

Delay Ramp Starts

With D55 set to its low-voltage state, Q64 is not conducting and its collector voltage is high. The incoming pulse switches D55 to its high-voltage state; Q64 is turned on to

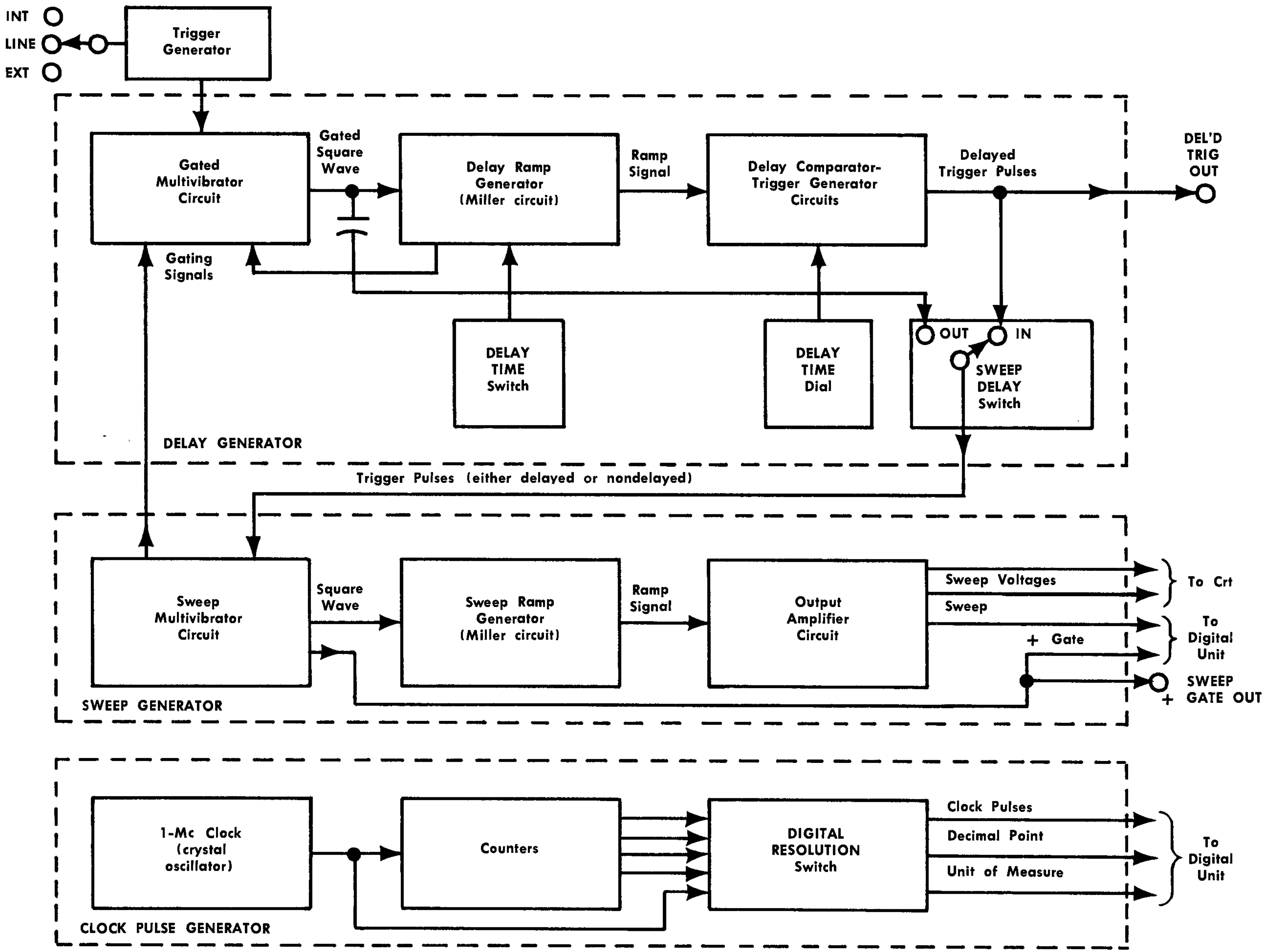


Fig. 4-1. Type 3B2 block diagram.

saturation and continues to conduct until the multivibrator is reset. When Q64 goes into saturation, its collector moves negative to produce a negative signal that passes to SWEEP DELAY switch SW170 and to the Miller circuit.

As long as the Miller circuit has a negative input, it generates a delay-ramp signal. Such a negative input turns off disconnect diode V72, and Miller capacitor C80 starts charging through timing resistor R80. As C80 charges, the grid voltage of Miller tube V91A moves in a negative direction. However, as this happens, the plate of V91A goes positive and the positive change is coupled through cathode follower V91B to the upper plate of C80. This increasing voltage on C80 serves to keep the charging current of C80 constant, thus providing a linear rather than exponential voltage change across C80 and at the cathode of V91B. Therefore, the output of the Miller circuit (V91B cathode) is a linear ramp that passes on to the delay-comparator circuit and back to the gated multivibrator.

Delay Ramp Stops

The Miller ramp is coupled to the gated multivibrator through D99 to the base of Q123. When the ramp exceeds +15 volts, Q123 is back biased and turns off (emitter cannot exceed +15 volts because of D116). When Q123 turns off, it ends the ramp by switching D55 to its low-voltage state which turns Q64 off. With Q64 off, its collector moves positive. This positive change brings disconnect diode V72 into conduction and Miller capacitor C80 discharges, thus stopping the delay ramp rise.

At times, the sweep produced on the crt may end before the delay ramp reaches +15 volts to stop the delay ramp rise. When this occurs, the delay generator reset signal turns the delay ramp off. This reset signal is coupled through R115 and C115 to the emitter of Q123. When the reset signal goes negative at the end of the crt sweep, the negative pulse formed turns Q123 off and thus stops the delay-ramp rise.

The next delay ramp cannot be started by a pulse from the trigger generator until Q123 is allowed to conduct so that D55 can be switched back to its high-voltage state. As long as the ramp signal to Q123 through D99 is +15 volts or greater, Q123 will not conduct. However, when the ramp stops, the signal reduces and will allow Q123 to conduct. Two other signals, however, can prevent Q123 from conducting. One signal, the negative trigger lockout, is applied to the emitter of Q123 through D114 to prevent conduction during the time the Sweep Generator produces sweep voltages for the crt. The second signal, from the holdoff circuit, appears at D98 to keep Q123 from conducting for a short time after the sweep is generated to allow the Sweep Generator circuits to stabilize before the next sweep is started.

The holdoff-circuit signal applies back bias to D98 to hold Q123 cut off. D98 is back biased through D96 and D97 with positive charges on holdoff capacitors C100 and C270. When the positive charges on the holdoff capacitors discharge to a low level, D98 is forward biased to allow Q123 to conduct.

Holdoff capacitor C270 is charged by the positive ramp produced in the Sweep Generator and is discharged at the end of the ramp. Holdoff capacitor C100 is charge to —12.2 volts through R103 as the delay ramp starts. When the delay ramp stops with SWEEP DELAY switch SW170 set to IN, Q103 conducts bringing one end of C100 to ground and C100 provides a positive charge of about 10 volts at D96 (+12.2 volts minus the negative starting voltage of the ramp). Thus, with the SWEEP DELAY switch set to IN, the holdoff signal from C100 is a minimum of +10 volts and may be increased depending on the value of delay-ramp voltage generated. With the SWEEP DELAY switch set to OUT, C100 remains connected to —12.2 volts through R103 and in some cases may never be charged to a positive value by the delay ramp. Any positive charges developed on C100 are discharged at the end of the delay ramp.

Delayed-Trigger Pulse Generator

The linear ramp output of the delay Miller circuit at pin 8 of V91B is applied to the grid of voltage comparator V134A. A variable dc voltage, set by DELAY TIME control R149, is on the other grid of the comparator (V134B). During quiescence, V134A is cut off and V134B is conducting. As the delay Miller circuit starts running up, the grid of V134A gets progressively more positive. When the ramp voltage on the grid of V134A reaches and exceeds the voltage on the grid of V134B, the comparator circuit switches states (V134A conducts and V134B turns off). As the current falls, V134B switches D135 to its low-voltage state. The switching signal of D135 is coupled directly to the base of Q164 where it is amplified. The amplified signal is the delayed-trigger pulse coupled to the DEL'D TRIG OUT connector through Q174 and to the SWEEP DELAY switch.

The amount of delay produced by the delay circuit depends on how long it takes for the delay Miller circuit to run up to the voltage set by the DELAY TIME control. Hence, this time can be changed either by varying the rate of rise of the delay Miller circuit with DELAY TIME switch SW80, or by varying the comparator switching voltage with DELAY TIME control R149.

V138 in the delay comparator circuit supplies a relatively constant current to V134 to permit V134 to operate linearly over a wide range. V149 regulates the voltage supplied to the DELAY TIME control to increase the stability of the delay circuit.

SWEEP GENERATOR

The sweep generator operation starts with a trigger pulse input from the Delay Generator. The incoming trigger turns Q214 on. When Q214 turns on, tunnel diode D215 switches to its high-voltage state. When D215 switches, Q224 turns on. This, in turn, places a more-negative voltage on the plates of disconnect diode V252. With the disconnect diodes turned off, Miller capacitor C260 starts charging through timing resistor R260. When C260 starts charging, the control grid of Miller tube V261A attempts to move negative. With its grid moving negative, the plate of V261A moves positive. This positive change is coupled through a cathode follower and back to the upper plate of Miller capacitor C260. This increasing voltage across the Miller capacitor serves to keep the charging current of C260 constant—thus providing a linear rather than exponential voltage change across C260 and at the cathode of V261B.

The Miller circuit stops running up and resets when D271 becomes forward biased and transistor Q273 becomes back biased. The exact point where this occurs is set by SWEEP LENGTH control R268. When Q273 turns off, tunnel diode D215 resets to its low-voltage state. At the same time, Q224 turns off, causing disconnect diode V252 to conduct and discharge Miller capacitor C260. Also, the positive change on the collector of Q224 is coupled to emitter follower Q233.

After the Miller capacitor is discharged, Q273 is brought into conduction and supplies the proper amount of current (about 4.1 ma) to make D215 triggerable.

TIME/DIV switch SW260 selects the resistors and capacitors used to set the sweep rate and holdoff period for the Sweep Generator. Transistors Q233 and Q244 supply sweep-gating signals to the Delay Generator and various points in the indicator unit as well as to the companion vertical plug-in unit.

The output of the Miller circuit (pin 8 of V261B) couples to the horizontal output amplifier through R301 and R303. The sweep takeoff for the digital unit is also at this point.

The output amplifier is a cathode-coupled paraphase amplifier with fixed gain. SWEEP CAL potentiometer R303 varies the amplitude of the sawtooth at the input of the output amplifier. Positioning is accomplished by changing the dc level on the grid of V314B with potentiometer R319 (POSITION control).

CLOCK PULSE GENERATOR

This circuit develops the clock-pulse signals used in the digital readout unit. The circuit also contains the DIGITAL RESOLUTION switch used to select time measurement units for the digital display unit.

The clock (Q490) is a crystal-controlled 1-mc oscillator. The signal from the collector of Q490 couples through C492 to the base of Q494. This transistor is an over-driven amplifier that produces pulses at 1-μsec intervals. These pulses are coupled to the DIGITAL RESOLUTION switch and to the first Counter board.

There are four Counter boards. Each board is a divide-by-ten device; that is, for every ten pulses in, there is one pulse out. Thus, with the output of one counter fed to the next, four successive divisions-by-ten occur. Outputs from the clock, and from the counters provide pulses at intervals of 1 μsec, 10 μsec, 0.1 msec, 1 msec, and 10 msec. Each of these outputs is connected to the DIGITAL RESOLUTION switch where it selects which of the five pulse intervals is sent to the digital unit.

With the DIGITAL RESOLUTION switch in the .1 μS position, pin 16 of P22 is connected to the 1-MC clock oscillator. This signal may pass from pin 16 to the digital unit where it can be used to generate pulses with 0.1-μsec intervals. Note, however, that not all digital units can use this signal.

The DIGITAL RESOLUTION switch also selects the position of the decimal point and unit of measure (S, MS, μS) when the digital unit is displaying time measurements. When the digital unit displays time measurements, pin 24 of P22 in the Type 3B2 is connected to ground. This ground is then used to light the S unit of measure through D287 and through the DIGITAL RESOLUTION switch to light the correct decimal point and additional unit of measure.

COUNTER BOARDS

Each of the four counter boards consists of a divide-by-two circuit followed by a divide-by-five circuit. The divide-by-two circuit is a bistable multivibrator that produces one output pulse for each two input pulses. The divide-by-five circuit contains three bistable multivibrators that produce an output pulse for each five input pulses. Divide-by-ten operation is accomplished by coupling the output of one divider circuit to the input of the other.

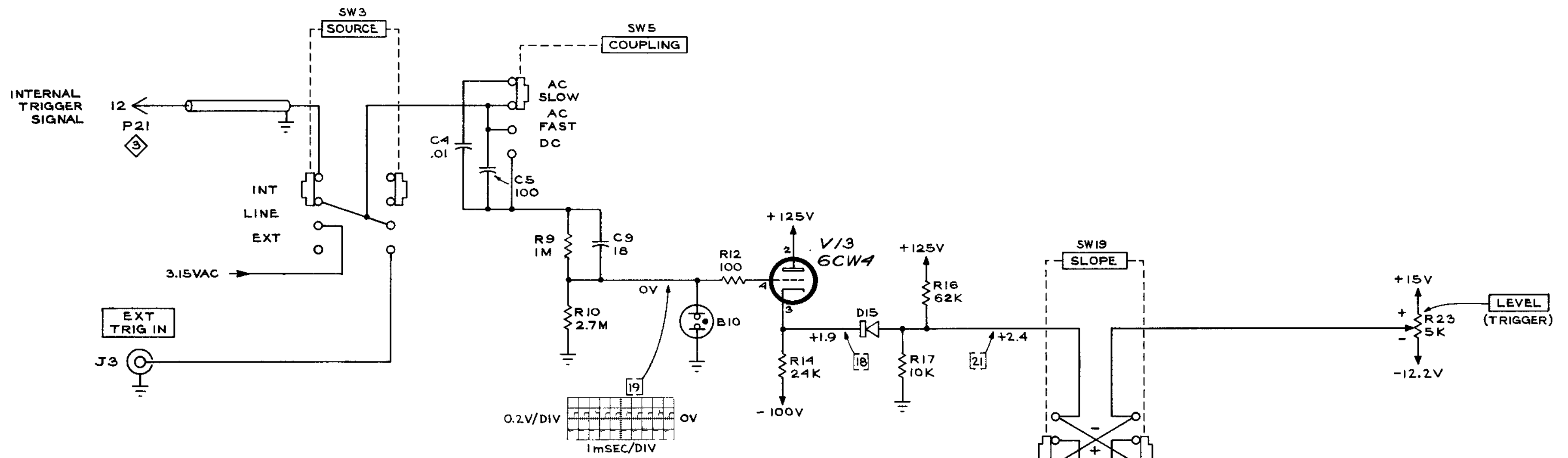
Each bistable multivibrator has two transistors and must set in one of two states. One state has the first transistor on with the second off. The other state has the first transistor off with the second on. The multivibrator is switched from one state to the other by a positive pulse applied through diodes to the bases of the transistors. The positive pulse switches the "on" transistor off which forces the "off" transistor on.

Q405 and Q415 are the two transistors in the divide-by-two multivibrator. When the instrument is turned on, the circuit will settle in one state; for example, Q415 turned on, and Q405 turned off. Diode D402 is highly back biased while D412 is slightly back biased. The positive-going portion of the input pulse from pin 6 is coupled through C407 and C417, and will find a path through D412, but be blocked by D402. This positive pulse through D412 turns Q415 off. When this happens, the collector of Q415 becomes more negative, and this change coupled to the base of Q405, turns Q405 on. Thus, the multivibrator has changed state. The multivibrator changes state again when the next input pulse finds a path through D402 to turn Q405 off. Each input pulse from pin 6 changes the state of the divide-by-two circuit.

Each time Q415 turns on, its collector moves in a positive direction and generates the positive input pulse for the next multivibrator.

In the cycle of operation of the divide-by-five circuit, Q465 turns on with one input pulse, turns off with the next input pulse, and then remains off for three input pulses before it turns on again. Thus, Q465 turns from off to on once for every five input pulses and turns from 'on' to 'off' once for every five input pulses. When Q465 switches from off to on, it generates the positive output pulse coupled to the digital unit through pin 4. When Q465 switches from on to off, Q475 switches on and generates the positive input pulse coupled to the next counter board through pin 11.

Each of the three multivibrators in the divide-by-five circuit operate the same as the one in the divide-by-two circuit. The only difference is that each time a digital unit pulse is generated (when Q465 turns on), a reset pulse through D430 and D450 turns Q435 and Q455 from on to off for divide-by-five operation.



IMPORTANT:

ALL CIRCUIT VOLTAGES WERE OBTAINED WITH A 20,000Ω/V VOM. ALL READINGS ARE IN VOLTS.

VOLTAGE & WAVEFORM AMPLITUDE MEASUREMENTS ARE NOT ABSOLUTE. THEY MAY VARY BETWEEN INSTRUMENTS AS WELL AS WITHIN THE INSTRUMENT ITSELF DUE TO NORMAL MANUFACTURING TOLERANCES AND TRANSISTOR AND VACUUM TUBE CHARACTERISTICS.

ACTUAL PHOTOGRAPHS OF WAVEFORMS ARE SHOWN.

TEST SCOPE TRIGGERED -EXT FROM 3B2 SWEEP +GATE OUT UNLESS OTHERWISE NOTED

3B2 TRIGGERED EXT WITH 1KC, 0.5V P-P SQUARE WAVE APPLIED

TYPE 3B2 CONTROL SETTINGS FOR ALL MEASUREMENTS ARE AS FOLLOWS:

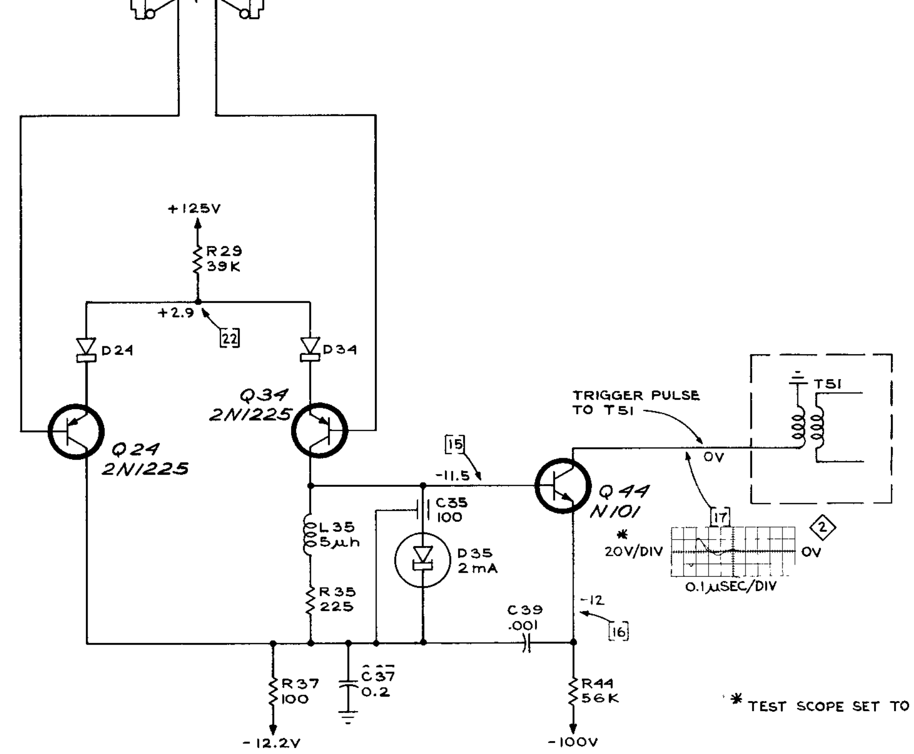
TRIGGER	
LEVEL	Centered
COUPLING	AC SLOW
SLOPE	+
SOURCE	EXT
DELAY	
SWEEP DELAY	OUT
DELAY TIME	1mSX50
SWEEP	
TIME/DIV	.2 mS

REFERENCE DRAWINGS

2 DELAY GENERATOR

3 SWEEP GENERATOR

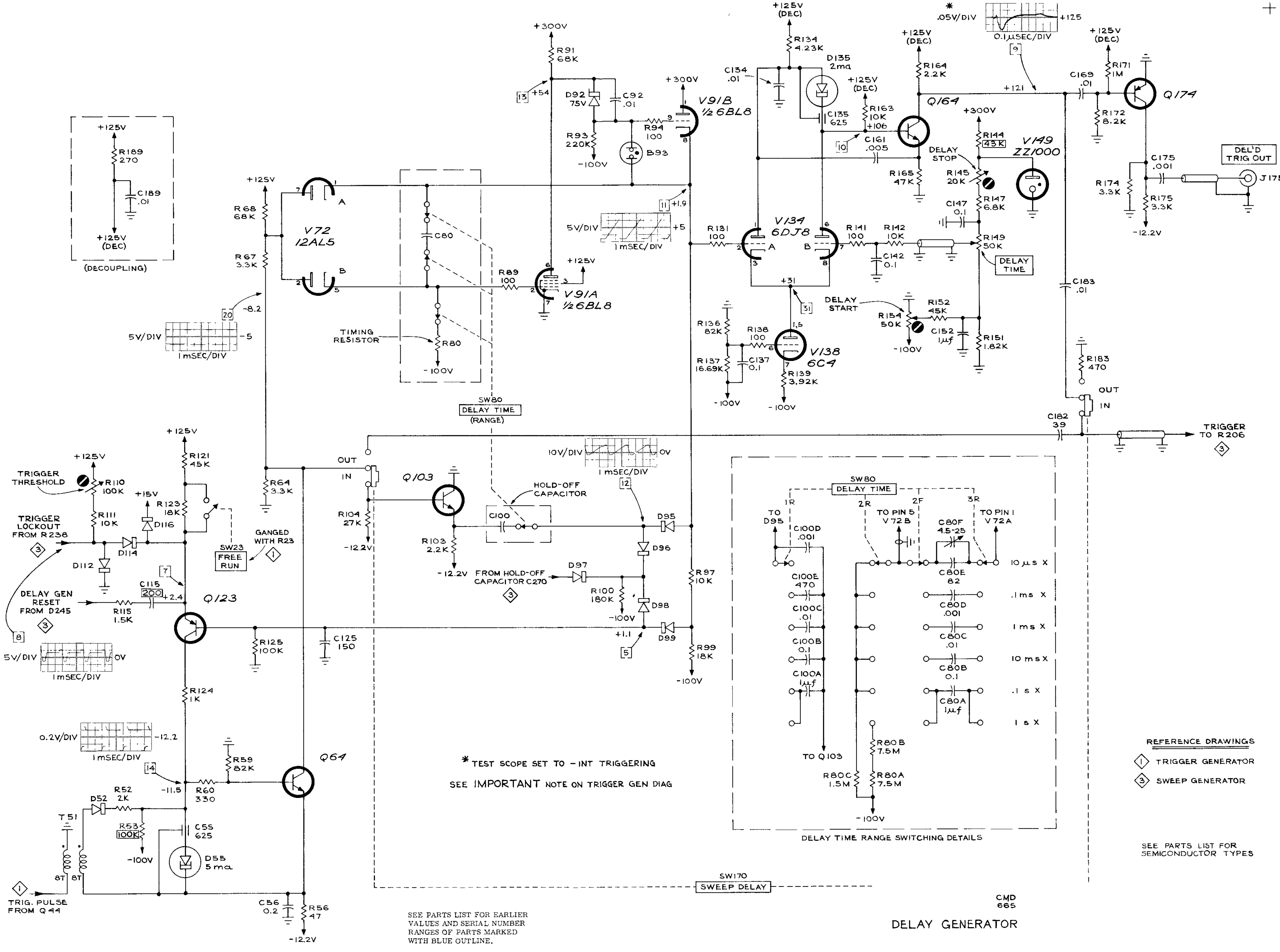
TYPE 3B2 PLUG-IN



* TEST SCOPE SET TO - INT TRIGGERING

CMD 963

TRIGGER GENERATOR



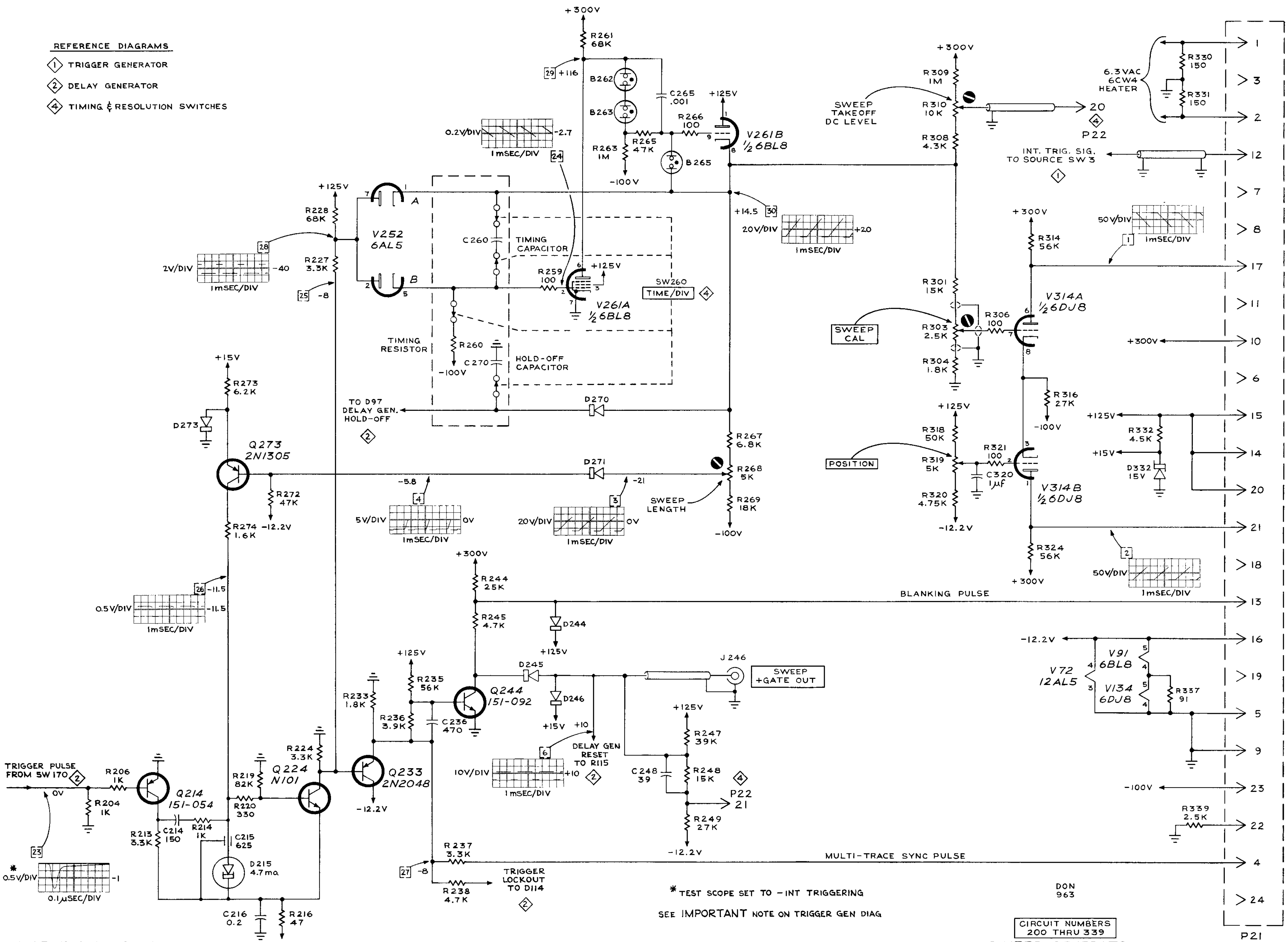
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

CMD
665

DELAY GENERATOR

TYPE 3B2 PLUG-IN

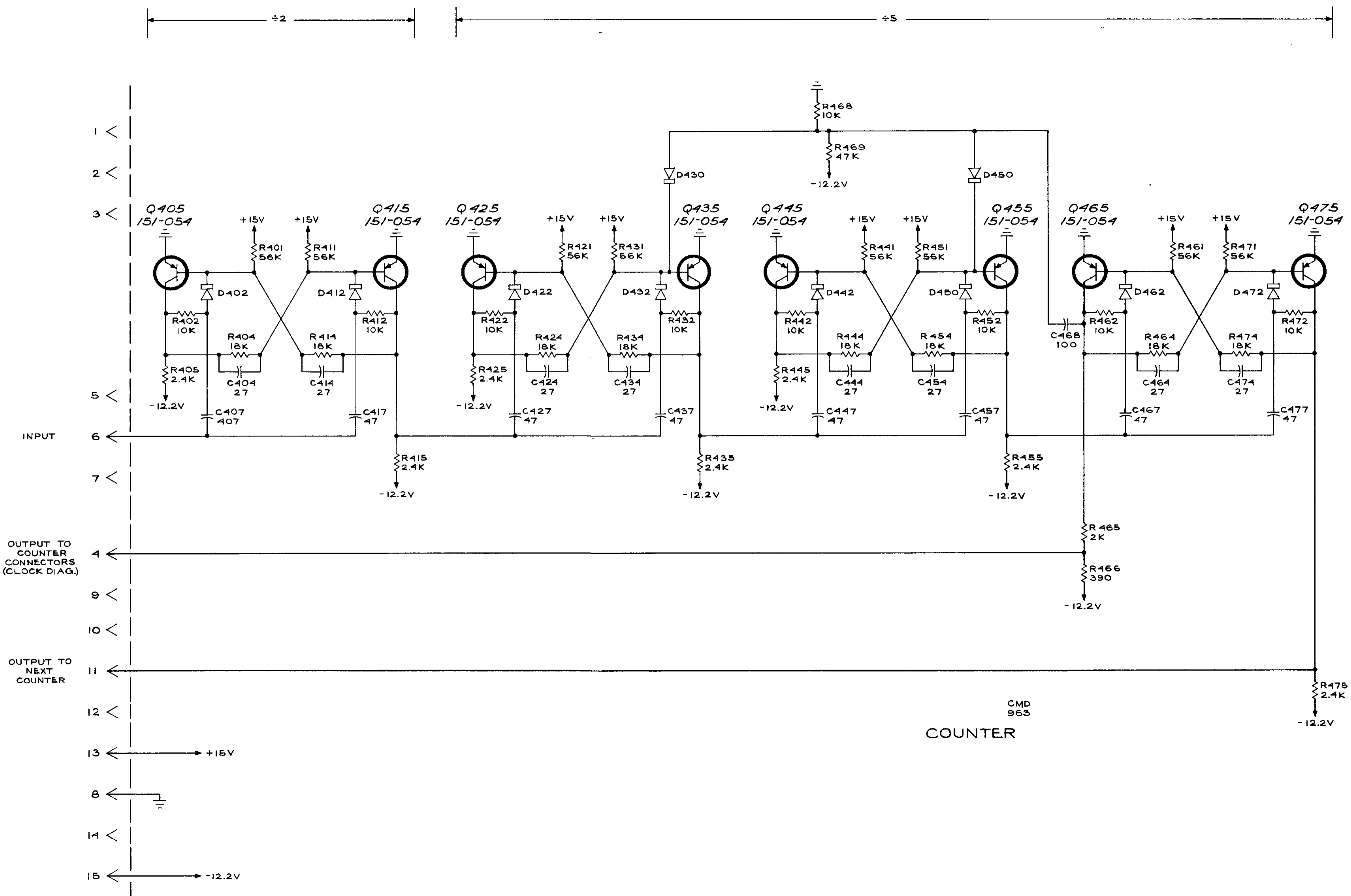
D



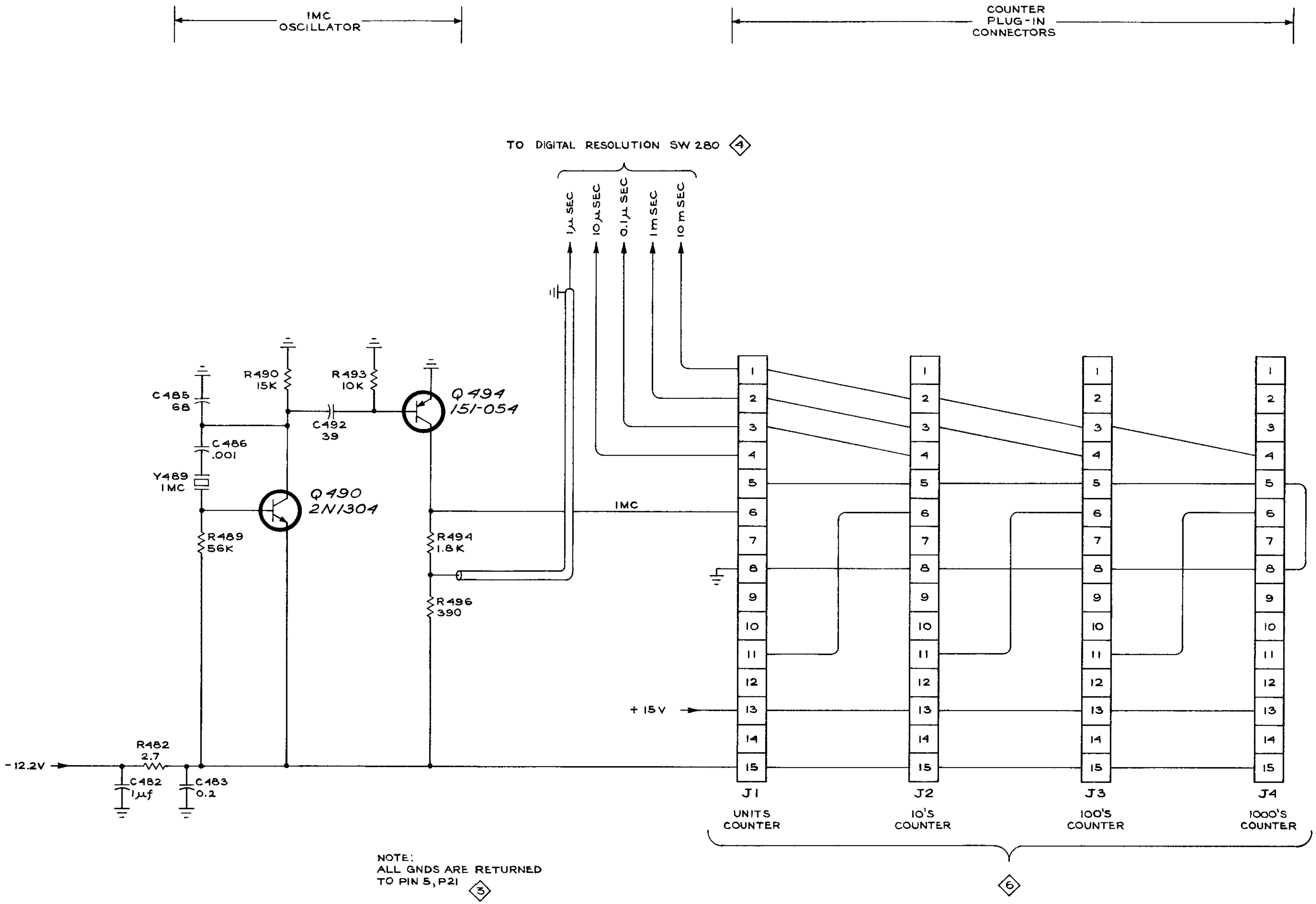
TYPE 3B2 PLUG-IN

A1

SWEEP GENERATOR



TYPE 3B2 PLUG-IN



TYPE 3B2 PLUG-IN

REFERENCE DRAWINGS

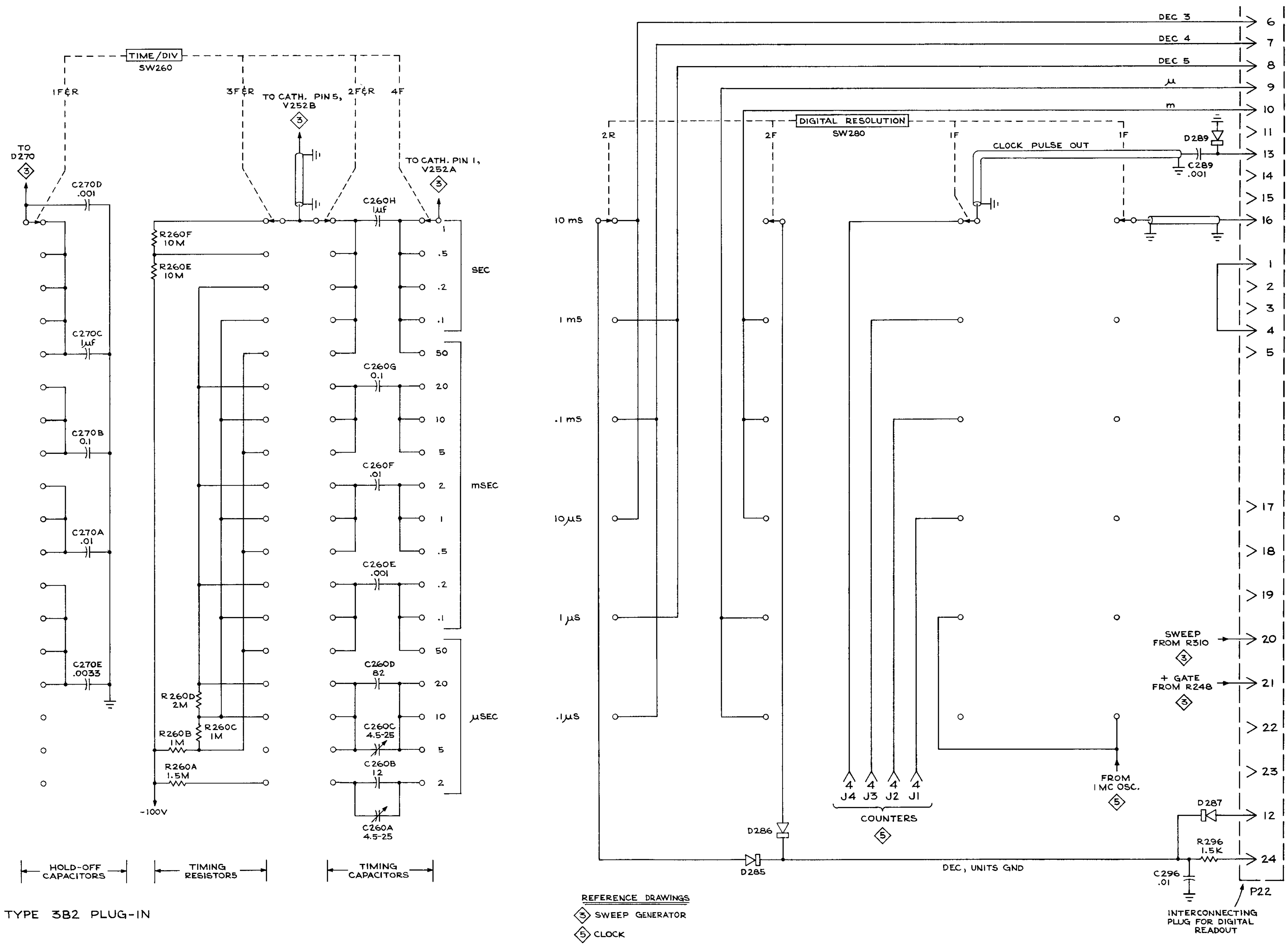
3 SWEEP GENERATOR

4 TIMING & RESOLUTION SWITCHES

6 COUNTER

CMD 963

CLOCK



TYPE 3B2 PLUG-IN

TIMING & RESOLUTION SWITCHES

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages. If it does not, your manual is correct as printed.

TYPE 3B2

PARTS LIST CORRECTION

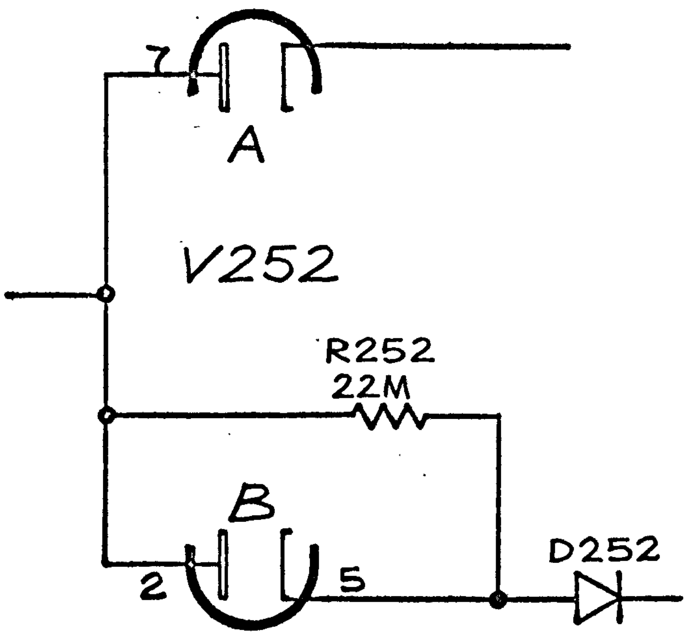
CHANGE TO:

Q123	151-0188-00	2N3906		
R52	316-0471-00	470 Ω	1/4 W	10%

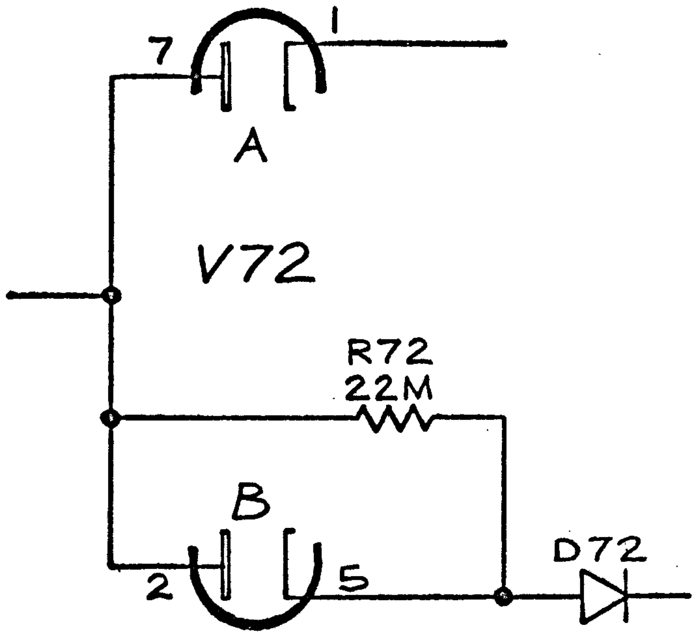
ADD:

R72, R252	316-0226-00	22 MΩ	1/4 W	10%

SCHEMATIC CORRECTION



PARTIAL SWP GEN. DIAG.



PARTIAL DELAY GEN. DIAG.

M11,546/966