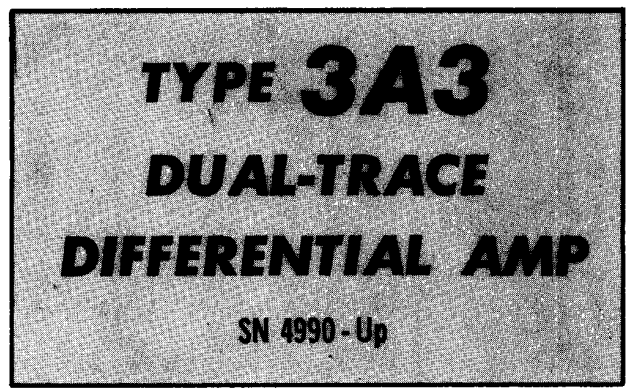
INSTRUCTION MANUAL

Serial Number _____



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070-0787-00

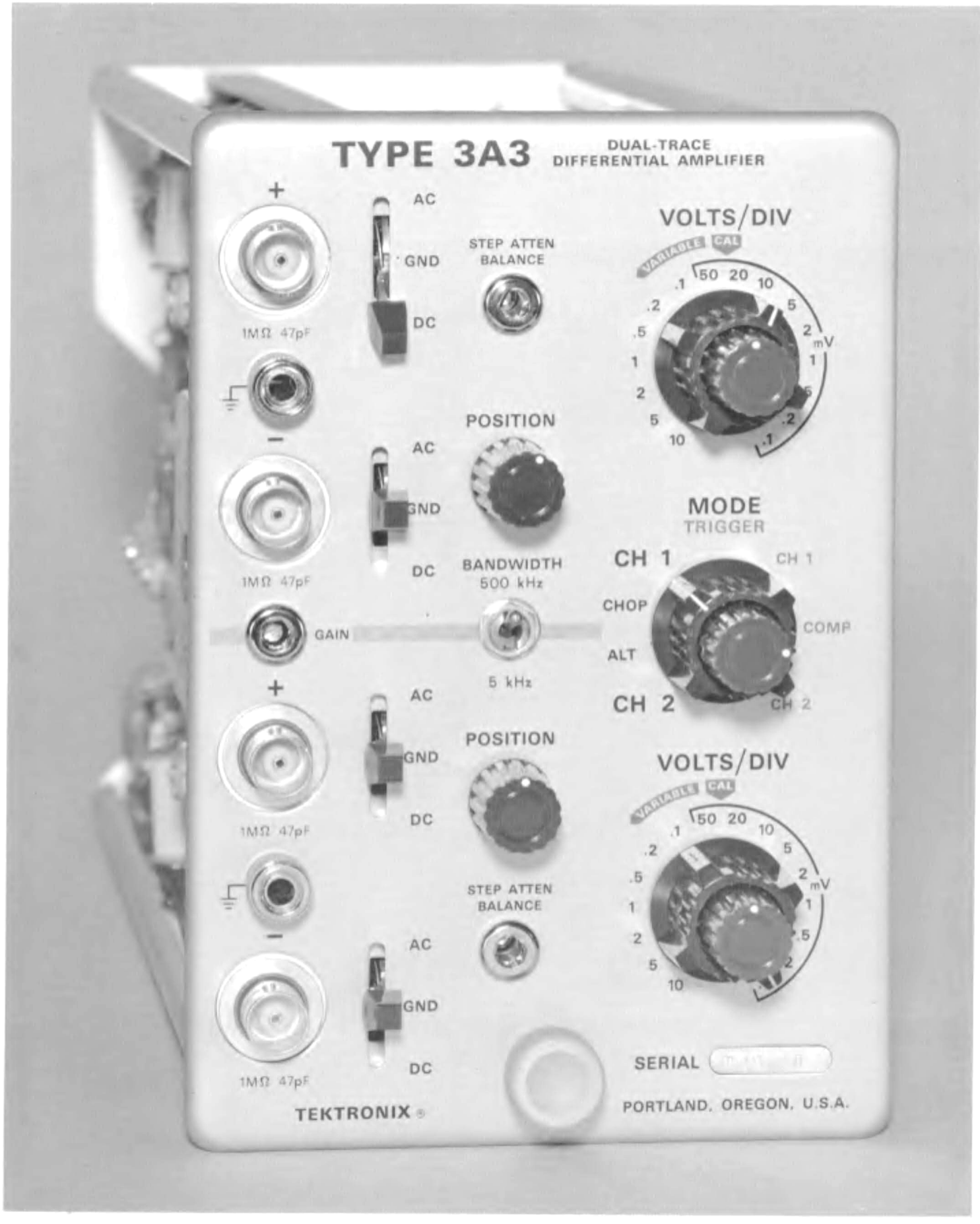


Fig. 1-1. Type 3A3 Dual-Trace Differential amplifier plug-in.

SECTION 1
CHARACTERISTICS

Change information, if any, affecting this section will be found at the rear of the manual.

The Type 3A3 is a Dual-Trace Differential Amplifier plug-in unit, designed to be used with Tektronix 560-series Oscilloscopes except the Type 560. The unit contains two independent high-gain differential amplifier channels. Either or both channels may be operated to produce a display. When both channels are used, a dual display is produced through alternate channel switching, or by chopping between channels during the sweep time.

In addition to the above, the Type 3A3 contains a low impedance Trigger Output circuit that provides trigger signal from either channel or a composite signal from both channels. The selected trigger signal is coupled through the oscilloscope plug to the companion time-base unit for internal trigger operation. Jacks may be installed in the oscilloscope to provide access to this trigger signal, so it may be used to drive a slave oscilloscope or X-Y plotters.

Characteristics described in this section are valid over the stated environmental range for instruments calibrated at an ambient temperature of +20°C to +30°C. A 30 minute warm-up is required for certain temperature-dependent characteristics as noted.

DUAL-TRACE AMPLIFIERS

Characteristic	Performance Requirement	Supplemental Information
Deflection Factor		
Calibrated Range	0.1 mV/div to 10 V/div, 16 steps in a 1-2-5 sequence	
Accuracy	Within ±3%	
Uncalibrated (Variable)	Continuously variable; extends deflection factor to at least 25 V/div	≥2.5:1
GAIN Range		At least +8% to −8% from calibrated setting
Bandwidth Limit Frequency (−3 dB points)		
500 kHz	500 kHz or more	
5 kHz	Not less than 5 kHz or more than 6.25 kHz	
AC (Capacitive) Coupled Input, Lower Bandwidth Frequency	1.6 Hz within 20%	
Step Response		
Risetime (500 kHz Bandwidth)	≤0.7 μs	
Common-Mode Rejection Ratio		
DC (Direct) Coupled		
0.1 mV/Div to 10 mV/Div, for signals within + and − 5 V of ground	≥50,000:1; DC to 100 kHz ≥1,000:1; 100 kHz to 500 kHz	
20 mV/Div to 0.1 V/Div for signals within + and − 50 V of ground	Equal to or adjustable to 5,000:1; DC to 1 kHz. Equal or adjustable to 1,000:1; 1 kHz to 100 kHz	
0.2 V/Div to 10 V/Div for signals within + and − 350 V from ground.	Equal to or adjustable to 500:1; 100 kHz to 500 kHz.	
AC (Capacitive) Coupled	≥500:1 at 15 Hz ≥2,000:1 at 60 Hz	
Input R and C		
Resistance	1 MΩ within 1%	

DUAL-TRACE AMPLIFIERS (Cont.)

Characteristic	Performance Requirement	Supplemental Information
Capacitance	47 pF within 2 pF	
Time Constant	47 μs within 4%. CH 1 + input and CH 1 — input; CH 2 + input and CH 2 — input matched to within 1.5%	
Input Gate Current		
Each Input	0°C to +35°C: ±100 pA or less; +35°C to +50°C: ±500 pA or less	
Uncompensated Input Current		≤200 pA at 25°C (0 V at wiper arm of Input Current Zero adjustment for each channel)
Variable Balance	≤0.2 div, shift with VARIABLE control turned from fully CW to CCW position at 10 mV/div	Adjustable to 0 using internal VAR DC BAL control
STEP ATTEN BALANCE	Adjustable for no position change while switching VOLTS/DIV selector	
POSITION Control Range		≥6 cm above and below the graticule center line
Displayed Noise (Tangentially measured)	≤15 μV at 500 kHz bandwidth with 25 Ω source	A figure of noise amplitude that approximately equals twice the RMS noise value and about 1/3 of the apparent trace width
DC drift		
Drift with Ambient Temperature (Line Voltage Constant)	≤50 μV/°C	
Interchannel Isolation		
Attenuator Isolation	≥10^6: 1, DC to 500 kHz	
Channel Isolation	≥10^5: 1, DC to 100 kHz	
Dual Trace Isolation	≥100:1, DC to 100 kHz	
Maximum Non-Destructive Input Voltage		
0.1 mV/Div to 10 mV/Div	350 V, DC to 1 kHz	See Fig. 1-2
20 mV/Div to 10 V/Div	350 V, DC to 500 kHz	DC (Direct) coupled; DC + peak AC.
AC (Capacitive) Coupled Input DC Rejection		600 V max when precharge circuit is used

TRIGGER OUTPUT CIRCUIT

Trig Output (Pins 11 & 12 of P-11)		
Amplitude		
Single Ended		2.5 V/div within 40%
Push Pull		5 V/div within 40%
Output Resistance		≤500 Ω
Bandwidth		≥400 kHz when connected to a 2B- or 3B-series Plug-In Unit.
Chopped Mode		
Chopped Repetition Rate	200 kHz within 25%	
Chopped Line Segment	2 μs to 3.3 μs	
Display Factor	≥60%	

GENERAL

Characteristic	Performance Requirement	Supplemental Information
Phase Difference Between Two Similar Type 3A3's		
0.1 mV/Div to 10 mV/Div	≤2°, DC to 100 kHz	Adjustable to zero internally

MECHANICAL CHARACTERISTICS

Characteristic	Information
Construction	
Chassis	Aluminum
Front-panel	Aluminum with anodized finish
Circuit Boards	Glass-epoxy laminate

ENVIRONMENTAL CHARACTERISTICS

The following environmental test limits apply when tested in accordance with the recommended test procedure. This instrument will meet the electrical performance requirements given in this section following environmental test. Complete details on environmental test procedures, including failure criteria, etc., may be obtained from Tektronix, Inc. Contact your local Tektronix Field Office or representative.

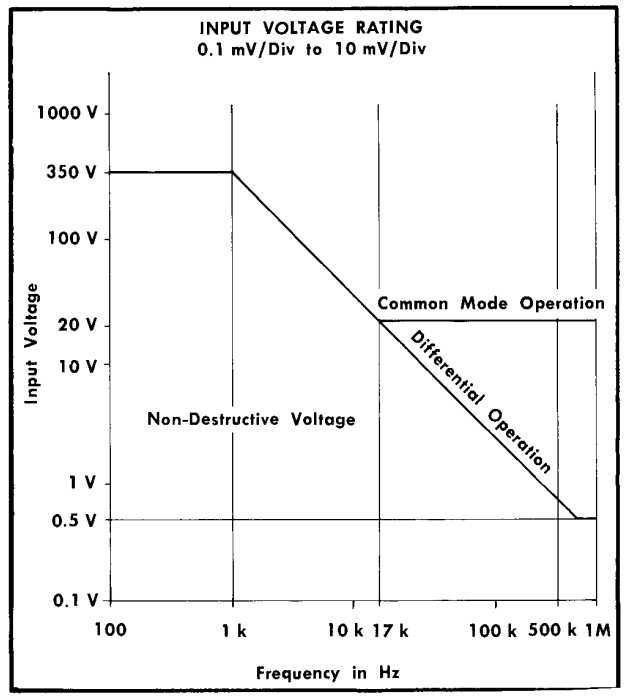


Fig. 1-2. Input Voltage rating of the Type 3A3, 0.1 mV/Div. to 10 mV/Div.

Characteristic	Operating Requirements	Supplemental Information
Temperature		
Non-operating	+4°C to +65°C	
Operating	0°C to +50°C	
Altitude		
Non-operating	To 50,000 feet	
Operating	To 15,000 feet	

SECTION 3
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual presents a description of the Type 3A3 circuitry, keyed to the block diagram and circuit schematics in Section 9. Detailed circuit analysis include some simplified drawings of the circuits to enable the reader to readily follow signal or current paths as the description is read. Changes or corrections to this section may be found at the rear of the manual.

General Description and Functional Block Diagram

A functional block diagram of the Type 3A3 is located in Section 9 of the manual, and in Fig. 3-1. The unit contains two independent differential amplifier channels, with each channel providing either differential or single-ended input signal application. Either channel may be selected to produce the display, or the two channels may be electronically switched to produce a dual trace display.

A trigger output circuit provides three selections of trigger signal (CH 1, CH 2, or the composite of both channels) to the plug-in connector as an internal trigger source to the companion Time-Base Plug-in Unit.

Signals applied to any input connector of the Type 3A3 are either AC or DC coupled via the input selector switch to the input attenuator. A GND position on the input selector grounds the attenuator input and connects the coupling capacitor through a resistor to the BNC input (+ or —) connector. Therefore, the coupling capacitor is charged to the DC level of an applied signal. Thus, there is no surge current from the capacitor charge when the input selector is switched from the GND position to the AC position, and only the AC component is coupled to the amplifier input.

Attenuation for both sides of each channel is provided by RC type attenuators with attenuation steps of 1×, 10×, 100×, and 1000×.

The output of the attenuator connects to the input amplifier, which contains a constant-current supply plus balanced input and output circuits that provide a high common-mode rejection ratio (CMRR).

The differential output from the input stage is then DC coupled to a gain-switching amplifier. This amplifier provides seven gain selections and when operated in conjunction with the four input attenuator steps, provides the .1 mV/div to 10 V/div deflection factors in a 1, 2, 5 sequence. The 500 kHz or 5 kHz bandwidth of the unit is also selected in this stage.

The differential output signal from the gain switching amplifier drives the trigger amplifier, plus an emitter-coupled differential amplifier. Vertical POSITION adjustment and a VARIABLE gain control are provided in this amplifier. A range of at least 2.5:1 variation in gain by this control provides continuous adjustment through each step of the VOLTS/DIV selector and increases the 10 VOLTS/DIV position to at least 25 V/div uncalibrated.

The output signal from the channel gain balancing amplifiers is then DC coupled through a switching circuit to the output amplifier for both channels. This switching circuit provides the four modes of operation. When the MODE selector is switched to either CH 1 or CH 2 position the driver multivibrator is disabled and the switching circuit connects the signal from the selected channel amplifier to the input of the composite output amplifier. Setting the MODE switch to the CHOP position causes the driver multivibrator to free run at an approximate 400 kHz rate. This output drives the switching circuit so that it chops between Channels 1 and 2 and the unit presents a display of both channels. When the MODE switch is in the ALT position, the driver multivibrator becomes a monostable multivibrator and requires an input pulse to cycle. This pulse is generated at the end of each horizontal sweep by the companion time-base plug-in unit. Therefore, the switching circuit alternates between channels to display both at a rate determined by the position of the Time/Div selector.

In the sequence with the drive signals to the mode switching circuit, the driver multivibrator provides both a chop blanking pulse to the plug-in oscilloscope CRT circuit, and a synchronizing pulse to the companion time-base plug-in unit.

The chop blanking pulses are applied via pin 24 of the interconnecting plug (J21) to the CRT cathode, when the CRT Cathode Selector switch on the back panel of the oscilloscope is in the Chopped Blanking position. This pulse blanks the CRT beam during switching time to eliminate the undesirable vertical transit lines between the dual display.

The dual X-Y sync pulse output is applied via pin 4 of the left hand interconnecting plug, to pin 3 of the right hand interconnecting plug. This provides dual X-Y display capability using the Type 3A3 and a companion vertical plug-in.

Differential signal voltages from the selected channel amplifiers are converted to push-pull signal currents by the output amplifier. This output drives the high impedance of the vertical deflection plates for the CRT. A GAIN adjustment in the emitter of the push pull amplifier provides a gain calibration adjustment for the unit.

The output signal from the amplifier is also connected through the TRIGGER selector, when it is switched to the COMP position, to the trigger output amplifier. This provides a composite trigger signal from either or both channels to internally trigger the time base unit.

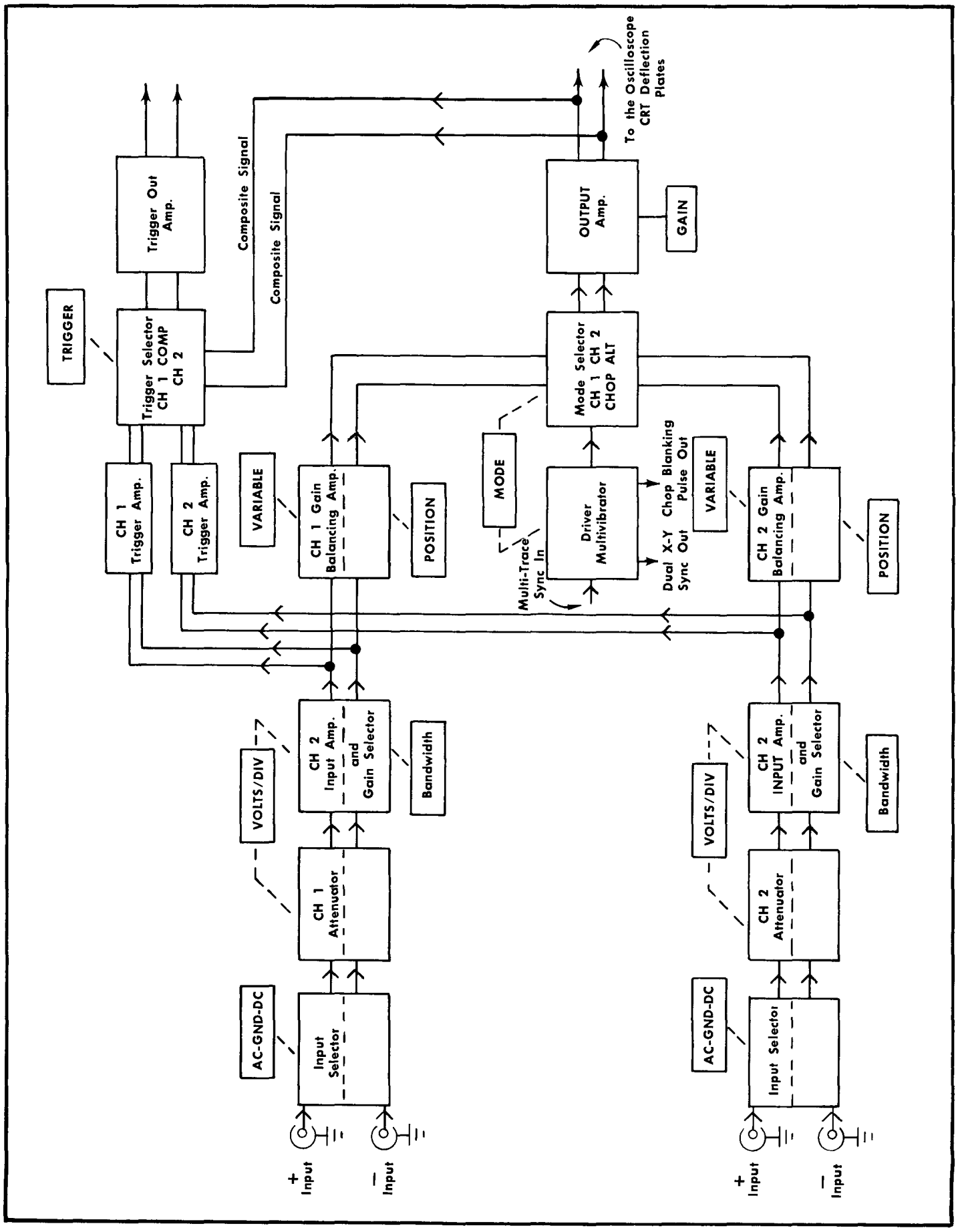


Fig. 3-1. Functional block diagram of the Type 3A3.

The trigger output amplifier is a cathode follower amplifier which provides a high current low impedance output signal with a DC reference adjustable to zero volts. This provides the trigger to the companion time base unit. It also provides a low impedance signal source to drive auxiliary equipment if provisions such as jacks, are installed in the oscilloscope main-frame and connected to pins 11 and 12 of the interconnecting plug.

DETAILED CIRCUIT DESCRIPTION

The illustrations in this section are provided as an aid in understanding the circuit descriptions. For electrical values and the complete circuit, refer to the schematics in section 9.

The input coupling, attenuator and channel amplifier circuits are identical except for circuit and component numbers. Therefore, the circuit description of Channel 1 is applicable to Channel 2. The + side of Channel 1 is described.

Input Coupling

A three-position selector SW101 and associated circuitry (Fig. 3-2) provide the following functions:

In the DC position, signals applied to the input connector are directly coupled through the input attenuator to the gate of the input amplifier transistor Q114.

In the GND position, the input to the amplifier is grounded through the attenuator and the switch. Signals applied to the + input connector charge the coupling capacitor C101 through R101 to the DC or average level of the applied signal. By precharging the coupling capacitor C101, no gate current flows when the Input selector is switched to the AC position and the trace remains on screen.

In the AC position, frequencies below 1.6 Hz are attenuated.

When the input selector is placed in either the AC or DC position and the VOLTS/DIV switch is in the 1× (.1 mV to 10 mV) attenuator position, input R and C for CH 1 is established by R113 (1 MΩ) and the stray circuit capacitance in shunt with C109. Input time constant for the 1× attenuator range is normalized at 47 μs by adjusting C109. The variable capacitors C105A, C106A or C107A are adjusted so all attenuator ranges maintain a standard input time constant through each position of the VOLTS/DIV selector.

Input Attenuator

An attenuation factor of 1×, 10×, 100× or 1000× is selected simultaneously for both the + and — Inputs with the VOLTS/DIV selector. These attenuators have the following characteristics:

1. The input R and C are normalized for all settings of the VOLTS/DIV switch for both input connectors. Adjustable capacitors C109-C209 (1×), C105A-C205A (10×), C106A-

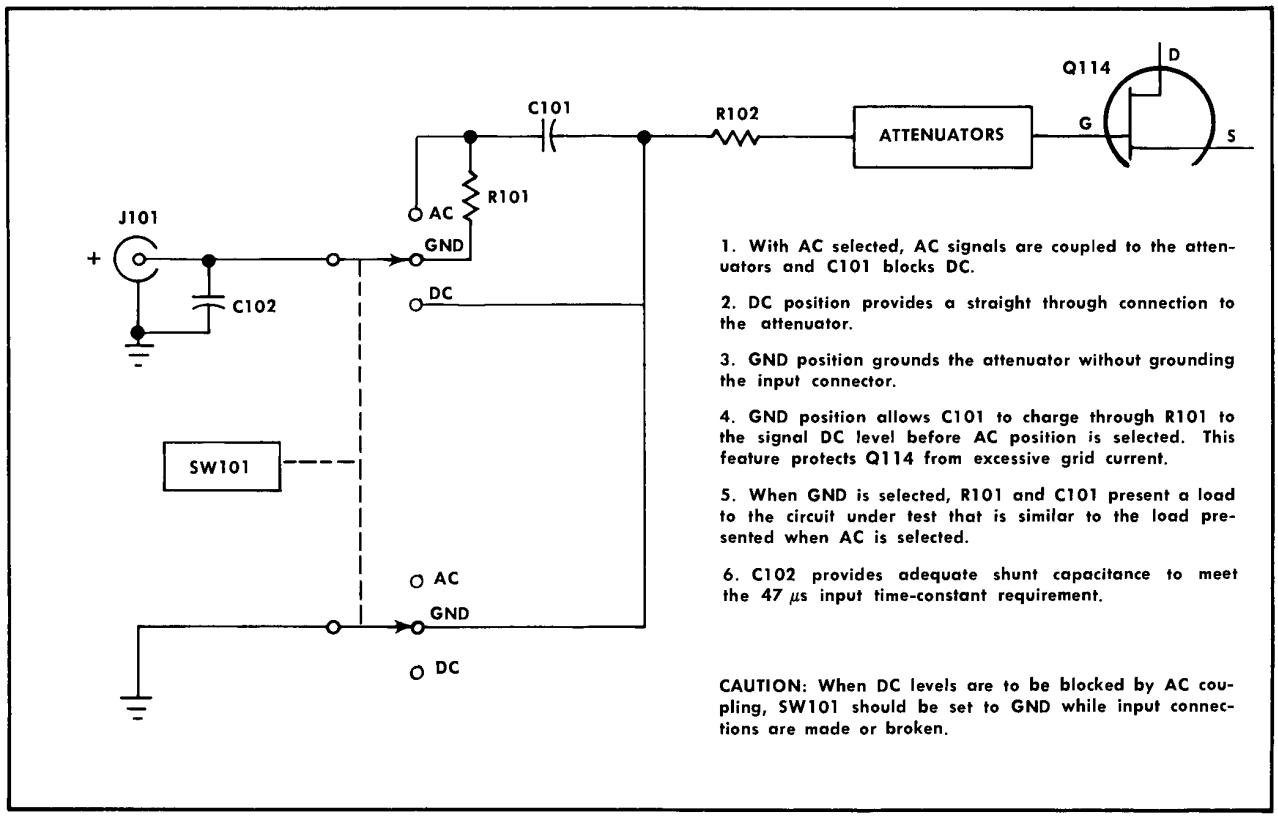


Fig. 3-2. Partial diagram showing the Input Coupling circuit with SW101 set to GND.

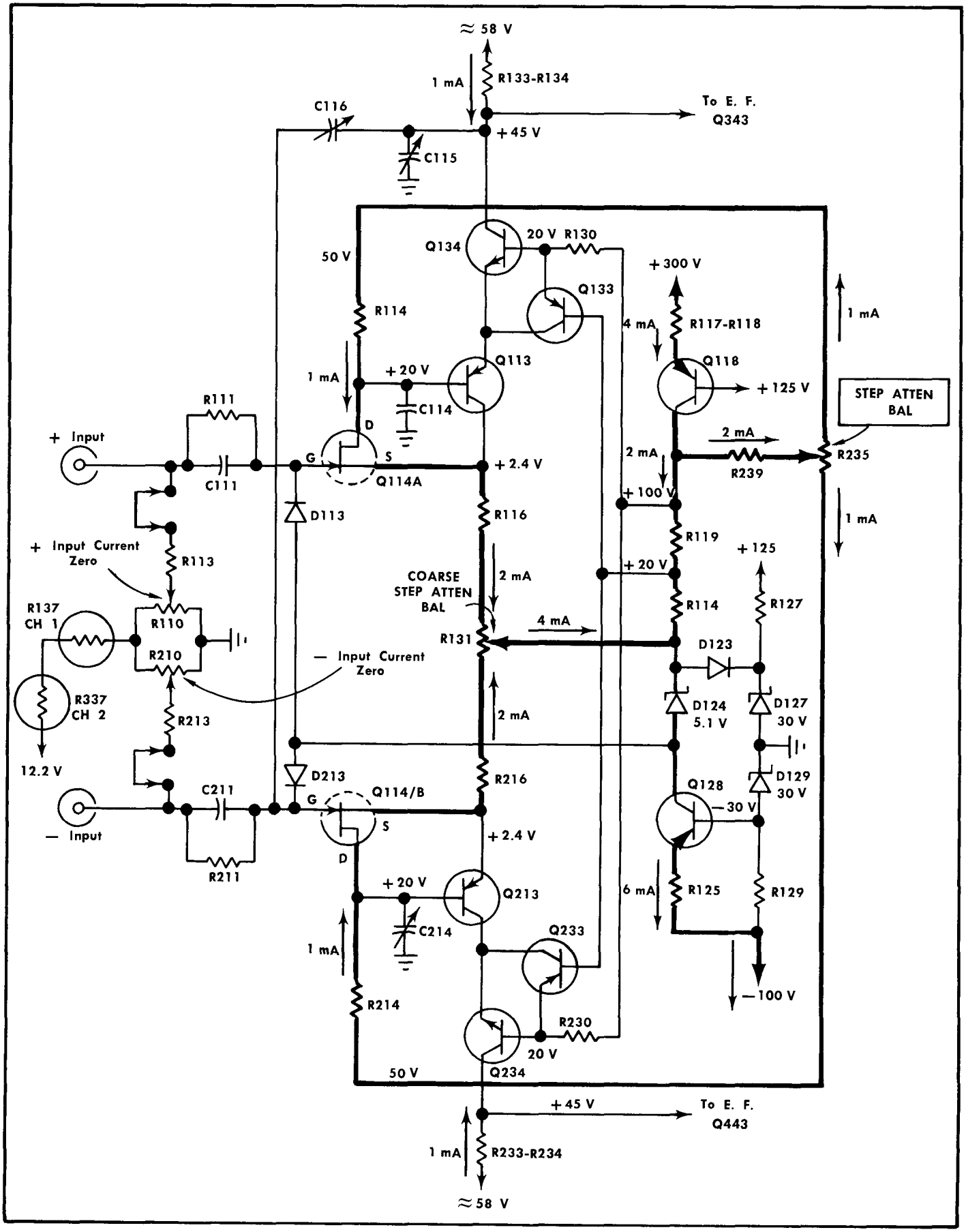


Fig. 3-3. Simplified (partial) diagram of the input amplifier with approximate current and voltage values. *Heavy lines indicate bootstrap circuit.* Voltage values are with input grounded.

C206A (100×) and C107A-C207A (1000×) provide this normalization adjustment.

2. The resistance (DC or low frequency) attenuation ratios of the attenuator are equalized by adjusting R105F, R106F, and R107F in each attenuator network for the + input. With these adjustments accurately set, optimum common mode rejection through the attenuators is achieved.

3. The reactance (AC or high frequency) attenuation ratio of the attenuator is calibrated by adjusting C105C-C205C, C106C-C206C and C107C-C207C.

4. High frequency compensation for the gain switching amplifier stage is provided by adjustments C251B, C251D, C251F, C251H, C251K, C251L, and C251M.

A maximum common mode signal range of ±20 volts (40 volts peak to peak, AC) is provided over the 1× range of the attenuator (.1 mV to 10 mV range of the VOLTS/DIV switch). This increases to ±200 volts (400 volts peak to peak, AC) for the 10× range (20 mV to .1 V range of the VOLTS/DIV switch) and ±350 volts (700 volts peak to peak, AC) for the remaining 100× and 1000× ranges of the attenuator (.2 V to 10 V range of the VOLTS/DIV switch). Common mode signal amplitudes up to ±20 volts peak to peak, AC at the gate input will produce essentially no change in the division of the common source current between the FET's. Signals in excess of this cause deterioration of the common-mode rejection ratio.

Input Amplifier

The input amplifier is basically a cascode paraphase or cascode differential amplifier, depending on the signal application, with a constant current source. Circuit differences between the + and — sides of the amplifier are minimized by incorporating the following features in the input amplifier circuit:

1. Constant current sources (Q118, Q128) for the amplifier. They establish the amplifier's operating current and greatly reduce differential signal currents that might otherwise appear in the amplifier when subjected to common mode voltage signals.

2. A g_m multiplier stage around the FET Q114, to offset gain variation due to temperature changes (about 0.35%/°C) and stabilize the forward transconductance (g_{fs}) of the FET.

3. Close tolerance (within 1/4%) load resistors set the drain current through each section of Q114, such that the current through each half of the input amplifier is closely balanced.

4. A collector impedance multiplier Q133-Q233, reduces the common mode error current developed by the h_{oe} of the transistors Q134-Q234.

A simplified diagram of Channel 1 Input amplifier is shown in Fig. 3-3. A constant source of floating power supply, consisting of Q118, Q128 and the associated circuitry, provide a constant current of approximately 2 mA for each half of the input amplifier. The voltage developed across R124 sets the voltage across each section of the dual FET Q114, and R119 sets the constant 2 mA current through the input amplifier. The 1/4% tolerance of the drain load resistors R114 and R214 plus the Step Atten Balance potentiometer R235, balance the current distribution through each half of the amplifier. The additional 2 mA is external current which flows from the external + 125 V power supply, through the cascode amplifier Q113-Q213 and Q134-Q234 to the floating power supply.

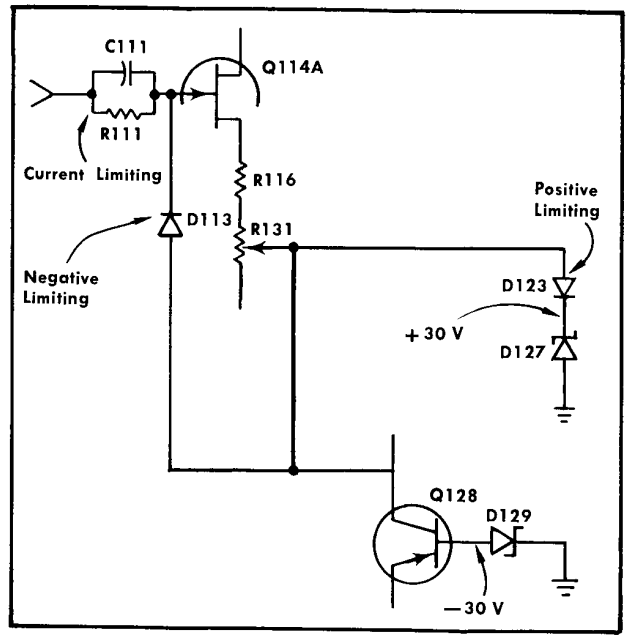


Fig. 3-4. Simplified diagram of input circuit, to illustrate, input signal limiting.

Changes in common mode signal level at the amplifier input are reflected through the gate-to-source junction of Q114 to the common source point of the FET. (The center point of R131). Since the current is constant through R124 and R119, a unit of voltage at the input is bootstrapped through the floating power supply to the base-emitter junctions of the transistors (Q133, Q134, Q233, Q234) and through R239 plus R235, to the drain-source voltage for Q114. The operating voltages and currents of the transistors and the FET are therefore held constant and the circuit remains balanced through variations of common mode input signal level within the maximum input limits of the amplifier. An approximate 6 mA source current through Q128 in the floating power supply is distributed as shown in Fig. 3-3.

Another determining factor in the CMRR of the input amplifier is the collector current stability of Q134-Q234. A small error current is generated through the collector to base impedance of Q134-Q234 when the common mode input signal shifts. This error is returned via Q133-Q233 to the emitters of Q134-Q234. Therefore, the effective collector to base impedance of Q134-Q234 is multiplied or increased by the beta of transistor Q133-Q233 to minimize the error current effect and increase the amplifier CMRR.

Signal current flow and circuit operation for the input stage is as follows: Signal applied to the + input is amplified by Q114A and applied to the base of Q113. This produces a signal current through the cascode paraphase

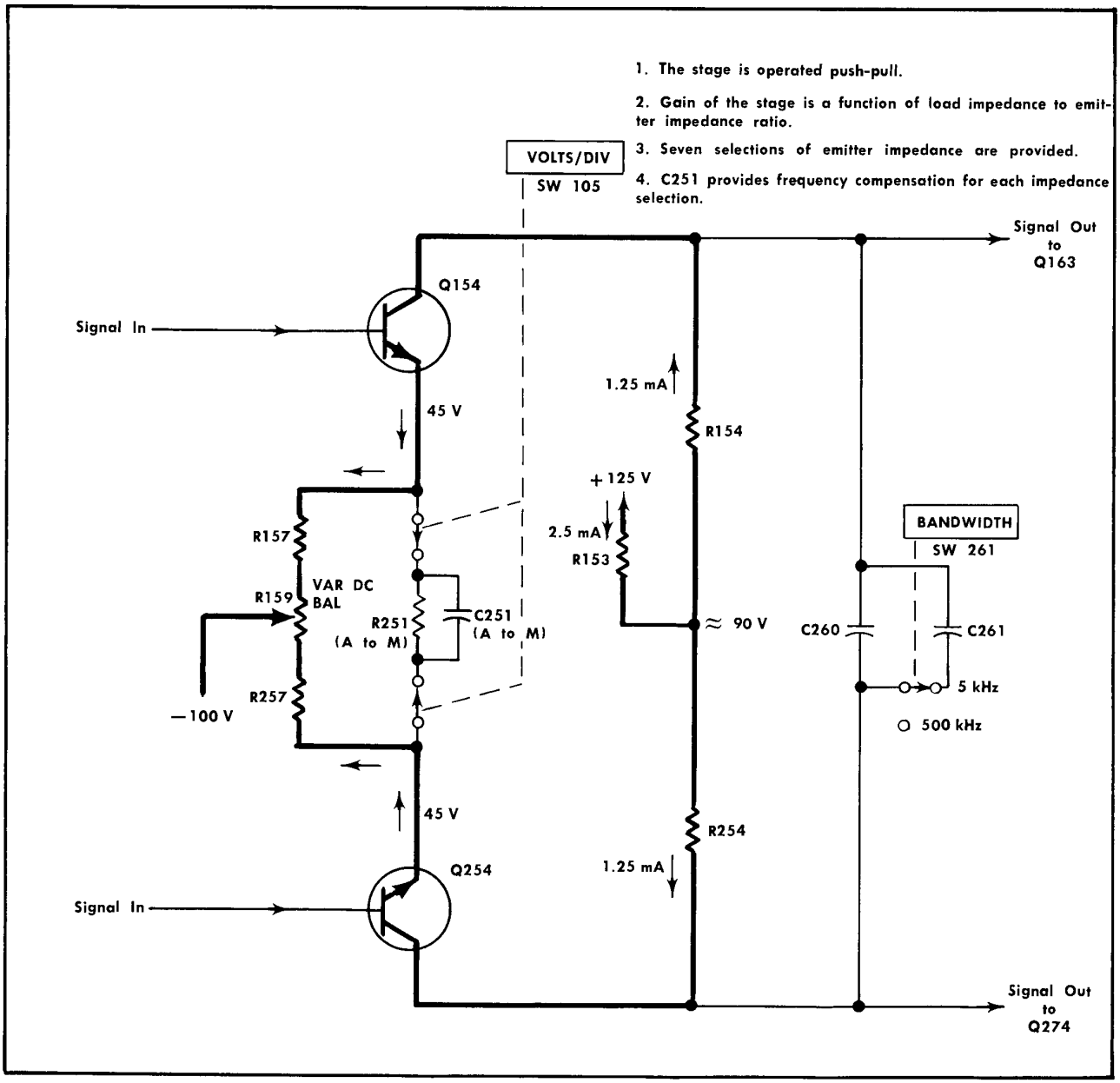


Fig. 3-5. Partial diagram of the gain switching stage. Heavy lines indicate path for constant current. (Currents and voltage figures are approximate with the inputs grounded.)

amplifier that develops an output signal voltage across the collector load impedance (about 12.9 kΩ) for Q134 and Q234. This signal is then applied as a push-pull signal to the emitter followers Q143 and Q243.

Gain of the input amplifier is a function of the ratio of the collector load impedance for Q134-Q234 to the total resistance R116, R216 and R131 or approximately

$$\frac{2\ (12.9\ \text{k}\Omega)}{\text{R116} + \text{R216} + \text{R131}}.$$

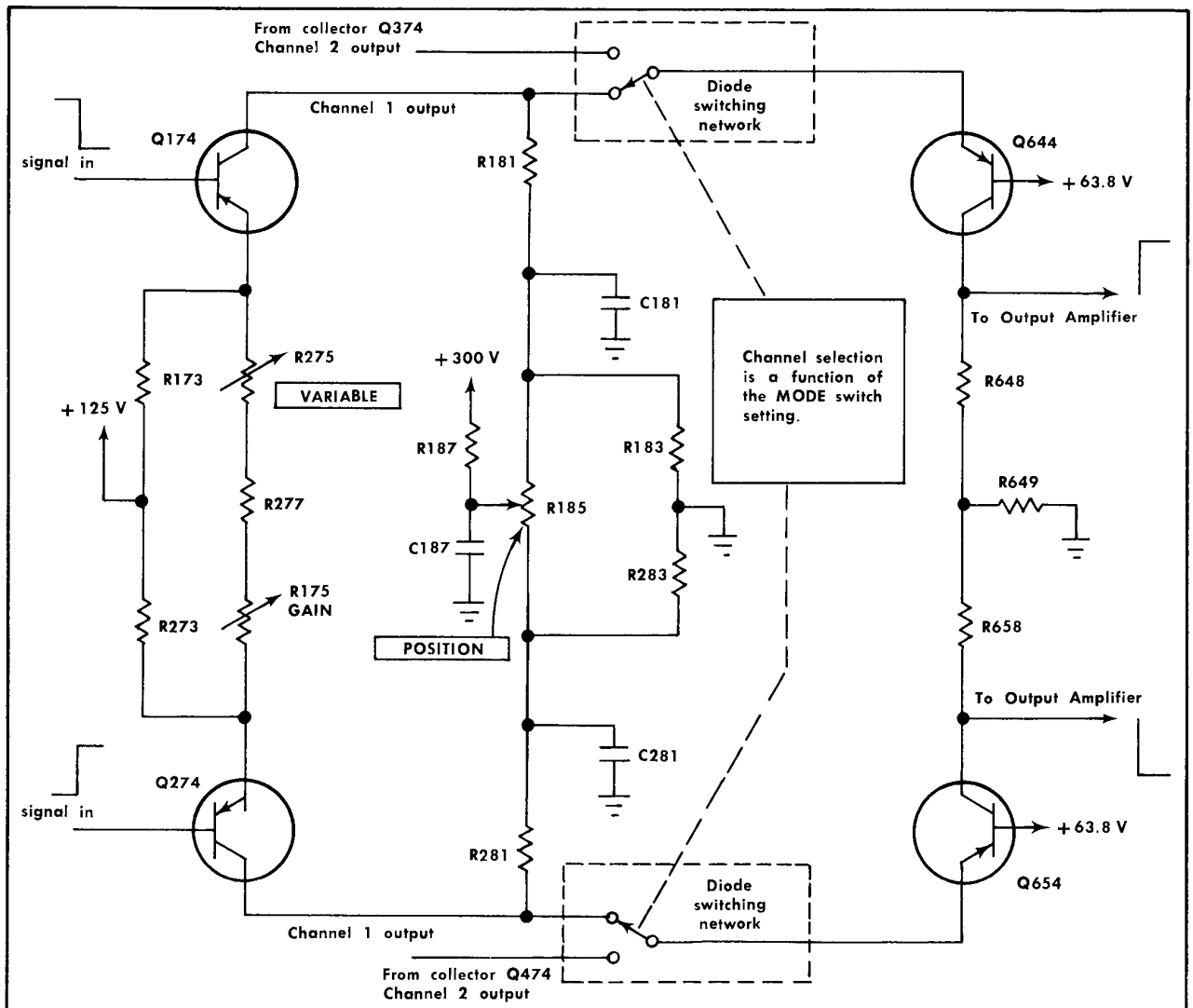
Transistors Q113 and Q213 serve as transconductance (g_{fs}) multipliers for the FET Q114A and Q114B. Q113 samples a small portion of Q114A drain current (I_d) and applies approximately beta times this sampled amount back to the source terminal of Q114A. Therefore, changes in I_d become independent of the dynamic characteristics of the field effect transistor, and effects of temperature variations on the FET transconductance are minimized by a factor that approaches the beta of Q113.

Gate leakage current (I_{gss}) for the input amplifier is temperature dependent; therefore, a temperature tracking compensation circuit is used to balance and offset the effects of this leakage current. The series connected thermistors R137 and R337 are part of a voltage divider circuit from

ground through R110-R210, to the —12.2 V supply. A voltage is set by the input current zero adjustments R110 and R120 that is equal but opposite in polarity to the voltage developed at the amplifier input by the I_{gss} through the input resistors R113 and R213. The voltage at the input to the amplifier remains at 0 V with respect to ground. For example: A gate-to-source leakage current of approximately 100 pA will develop about ±0.1 mV at the input. Adjusting R110 for —0.1 mV will shift the input or gate of Q114A to 0 V with respect to ground and the effect of I_{gss} is eliminated. The thermistors are mounted on each side of the input amplifier board. The temperature compensation is therefore an average of the temperature change for each side of the input amplifier circuit board.

The wire link in series with the gate return to ground can be removed if desired. This provides a floating input or a substantially higher input resistance. The signal source must provide the DC return path for the input leakage current and only DC coupled signals within the range of the .1 mV/DIV to 10 mV/DIV deflection factors can be accurately measured with the floating input.

Circuit protection from input voltages that may exceed ±30 V is provided by the following:



1. Front panel VARIABLE control provides continuously variable attenuation between calibrated deflection factors.

2. Internal GAIN control R175 provides a means of adjusting the gain of Channel 1 to the proper magnitude, and equal to the gain of Channel 2.

3. Front panel POSITION control provides CRT display positioning.

Fig. 3-6. Partial diagram showing the output of channel 1 selected by the electronic switching circuit. The combined circuit is two convential cascode amplifiers operated as a conventional emitter coupled push-pull amplifier.

1. Negative signals whose amplitudes are greater than —30 V are limited through D113, the collector-to-base junction of Q128 and D129 to ground. See Fig. 3-4.

2. Positive signals, above +30 V are limited through the gate-to-source junction of Q114A, R116, R131, D123 and D127 to ground.

3. The series elements composed of R111-C111 limit the input current to protect the gate-to-source or diode junctions when the limiting action is occurring.

C116 and C216 provide a cross neutralization adjustment to compensate for the capacitance between the input leads to the amplifier.

C115 provides a differential adjustment to equalize the collector load time constants of the output transistors, Q134 and Q234. It is adjusted for maximum CMRR at the high input signal frequency range.

C214 provides a differential equalizing adjustment for the dynamic output impedance of the FET, Q114.

Gain Switching Stage

Signal outputs at the collectors of Q134-Q234 are DC coupled through an emitter follower Q143-Q243.

Gain of the stage is determined by the ratio of the total collector load impedances (essentially R154-R254) to the effective common emitter impedance (essentially R251). Seven values of emitter impedances are selected with the VOLTS/DIV switch, to provide the selectable gain feature. These impedance components (R251A, R251C, R251E, R251G, R251J, R251L, and R251M, with their associated capacitors) parallel the current balancing circuit R157, R159 and R257. Inspection of the collector load and effective emitter resistance values show ratios ranging from about 25:1 to 0.25:1 at the lower sensitivity settings of the VOLTS/DIV switch. (To check these ratios refer to the Attenuator schematic in section 9 for the selectable component values).

The Var DC Bal R159 adjusts the current through R157 and R257 for 0 V, between the emitters of Q174 and Q274, so there will be no current through the VARIABLE control or Gain adjustments.

The bandwidth of the amplifier is limited to approximately 500 kHz and 5 kHz by the bandwidth selector SW261, which adds or removes an additional capacitor C261 across the collector load of the gain switching amplifiers Q154-Q254. The 5 kHz position of the BANDWIDTH selector attenuates high frequency noise, so low frequency measurements may be more easily performed.

Gain Balancing and Output Driver Stage

The push-pull signal from the gain switching stage is applied through emitter followers Q163-Q263 to the gain balancing stage or driver amplifiers Q174-Q274, plus the trig-

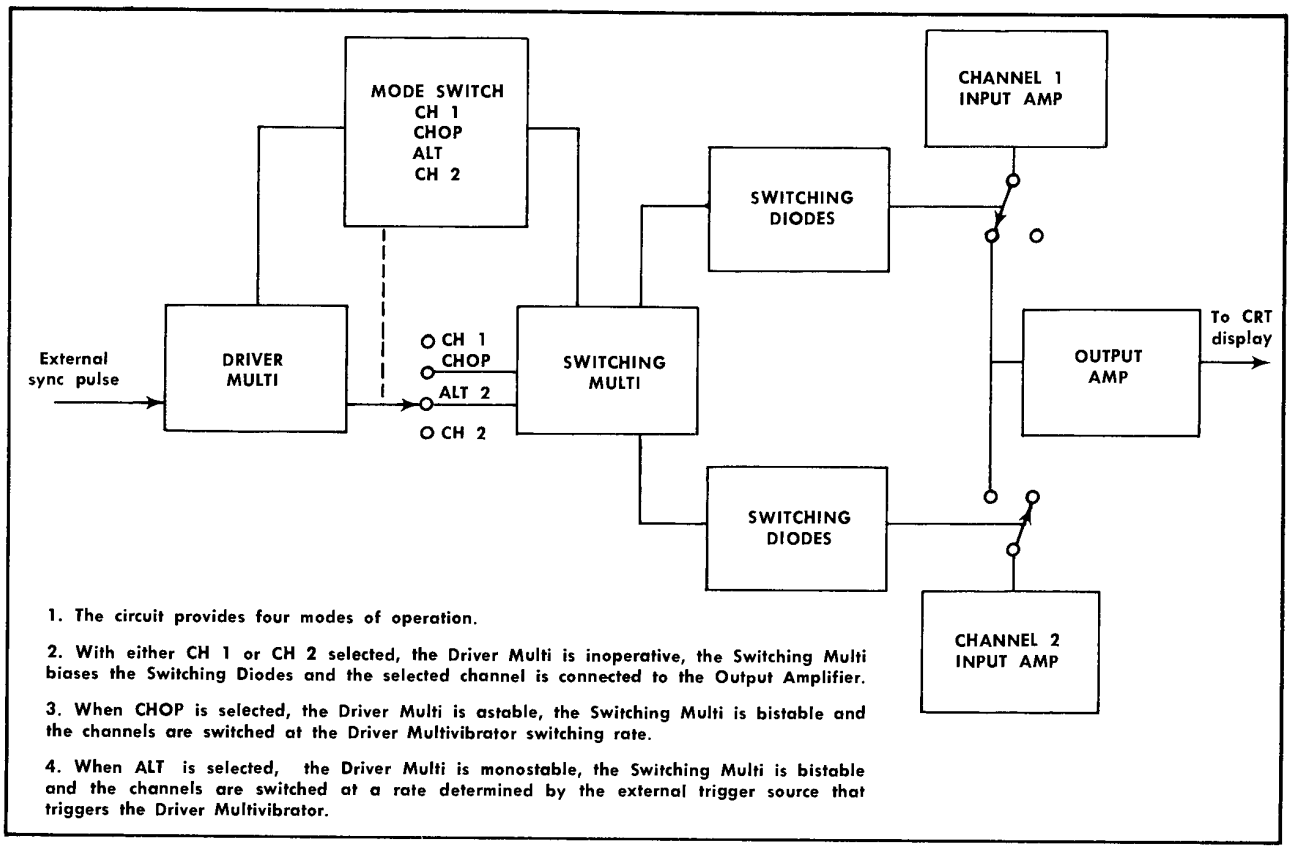


Fig. 3-7. Block diagram of the Electronic Switching circuit.

ger amplifiers Q504-Q514. The emitter followers provide the isolation between the gain switching stage and the variable gain adjusting stage. They also provide the signal drive to the trigger amplifier stage Q504-Q514.

Q174 and Q274 with associated circuitry provide CRT display vertical positioning, gain adjustment to calibrate the VOLTS/DIV selector positions, continuously variable attenuation between calibrated deflection factors and gain balancing between Channel 1 and Channel 2.

The MODE switch SW602 electronically selects either the output of this stage or its counterpart from Channel 2, to current-drive the emitters of Q644 and Q654. With either channel selected, the combined circuitry is two cascode amplifiers connected and operated as conventional emitter coupled push-pull amplifiers (see Fig. 3-6).

The emitters of Q174 and Q274 are returned to +125 volts through R173 and R273 establishing a DC operating current of about 3 mA for each side. (An emitter voltage of about +75 volts is set by preceding circuitry.)

The voltage divider network (between Q174-Q274 collectors) provide CRT display positioning. This is accomplished by diverting current from one side of the circuit to the other with the front panel POSITION control R185.

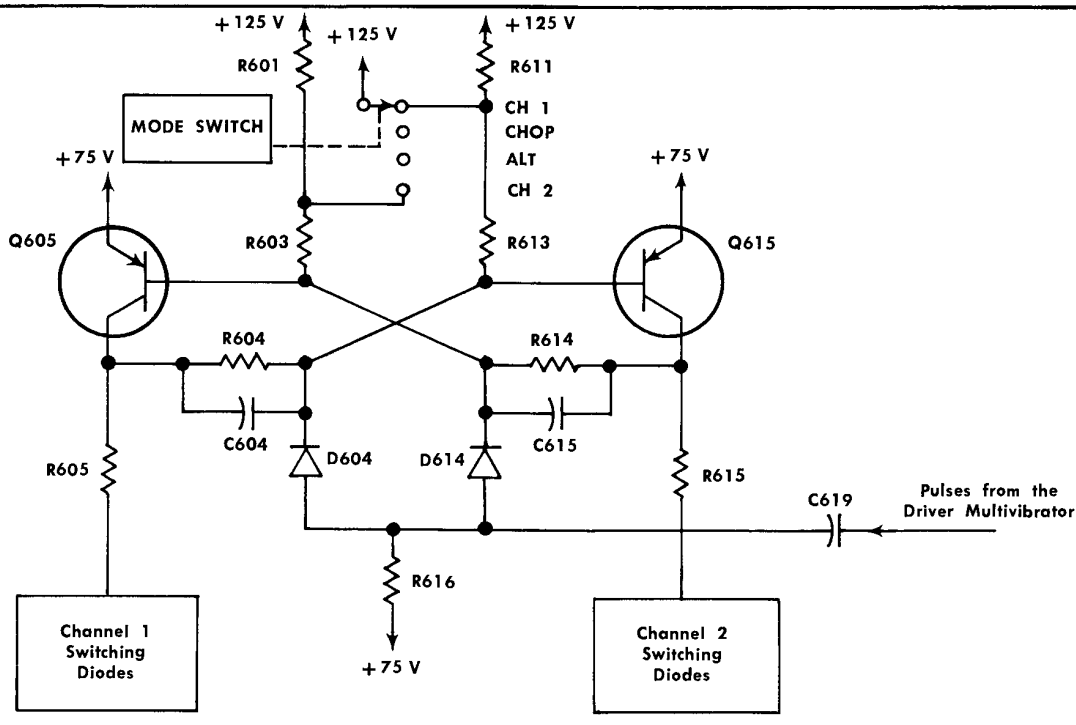
Since the combined circuit is two cascode amplifiers connected and operated as a conventional push-pull amplifier, the voltage gain of the circuit can be derived as a function of the ratio of output impedance to input impedance. In this circuit, the output impedance is the Q644-Q654 collector impedance, and the input impedance is the Q174-Q274 emitter impedance. Since VARIABLE control R274 and Int Gain R175 set the effective emitter impedance, they control the gain of the combined circuit.

VARIABLE control R275 is a front-panel control. It provides continuously variable attenuation between the calibrated deflection factors and extends the attenuation range to at least 25 volts per division.

Int Gain R175 provides a means of balancing the gain of Channel 1 with the gain of Channel 2 at the proper magnitude.

Electronic Switching Circuit

The electronic switching circuit provides four operating modes that are selected by the MODE switch SW620. The circuit contains a switching multivibrator, a driver multivibrator and switching diodes for each channel. See Fig. 3-7.



1. When the MODE switch is set to CH 1, Q605 is forward biased and Q615 is reverse biased.

2. When the MODE switch is set to CH 2, Q615 is forward biased and Q605 is reverse biased.

3. When the MODE switch is set to either CHOP or ALT, the circuit is bistable. The conduction state of Q605 and Q615 is switched by pulses from the Driver Multivibrator.

Fig. 3-8. Partial diagram showing the Switching Multivibrator circuit.

When the MODE selector is positioned to either CH 1 or CH 2, the driver multivibrator is inoperative. The switching multivibrator is held in a state with either of the two sides turned on. The on side of the switching multivibrator opens the circuit through the switching diodes and connects the selected CH 1 or CH 2 amplifier to the output amplifier through Q644 and Q654.

When the MODE switch is set to either CHOP or ALT positions, the driver multivibrator is activated, the switching multivibrator becomes bistable and electronically turns the switching diodes on and off. The CH 1 and CH 2 amplifiers are thus alternately connected to the output amplifier. This switching between the two channels produces the dual display.

Q605 and Q615 with their associated circuitry form the switching multivibrator. The circuit determines which channel is coupled to the output amplifier by controlling the bias of the switching diodes.

With the MODE switch set to CH 1, the junction of R611 and R613 is returned to +125 volts (see Fig. 3-8). This applies sufficient reverse bias to Q615 to hold it in cutoff. Q605 is forward biased. Its conduction biases the switching diodes so the signals from the channel 1 amplifier are coupled to the output amplifier.

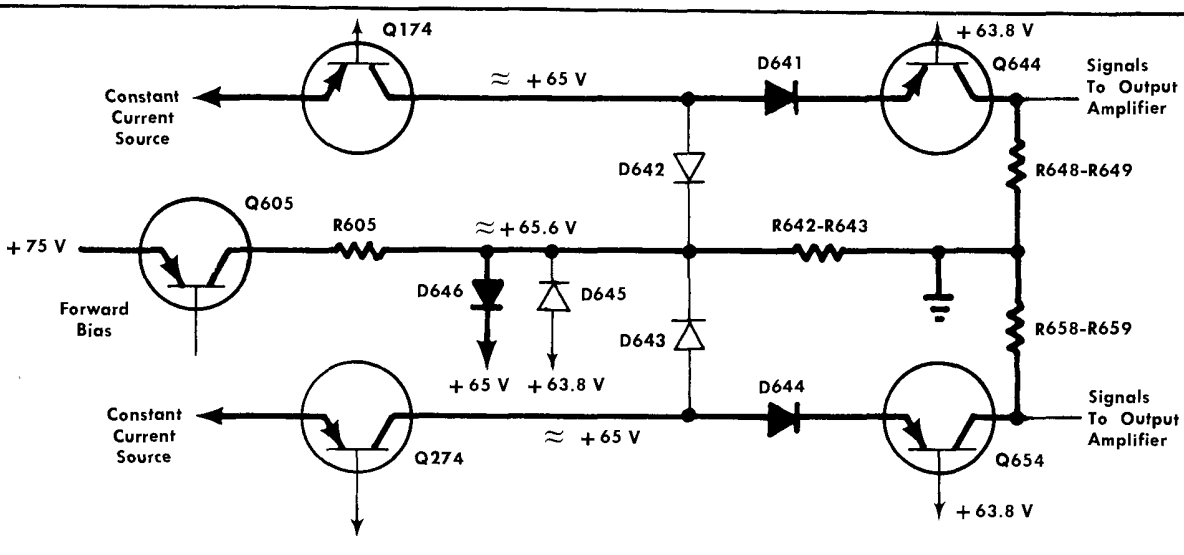
With the MODE switch set to CH 2, the junction of R601 and R603 is returned to +125 volts. Q605 is cut off and Q615 conducts. This biases the switching diodes so the signals of channel 2 are coupled to the output amplifier and channel 1 is decoupled or disconnected.

When the MODE switch is set to either CHOP or ALT positions, the switching multivibrator is a bistable circuit. The conduction state of Q605 and Q615 are switched by pulses from the driver multivibrator. The positive portions of the pulses are steered to the base of the conducting transistor by diodes D604 and D614.

Two sets of silicon diodes form the switching diode circuits that couple and decouple the input amplifier channels with the output amplifier. The conduction state of the switching multivibrator transistors controls the bias of the switching diodes and determines which channel is coupled or decoupled to the output amplifier.

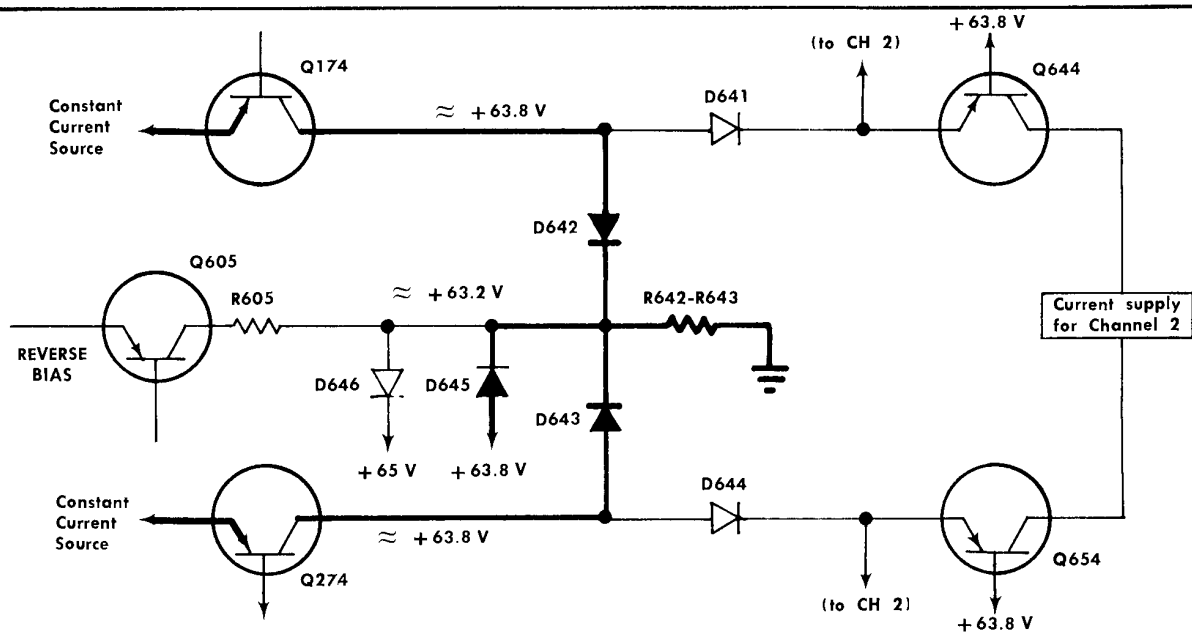
When Q605 conducts (see Fig. 3-9), D646 is turned on and a voltage of about +65.6 volts is established at its anode. This voltage reverse biases D642, D643, and D645. With these diodes reverse biased, R642 and R643 are decoupled from the Q174-Q274 collector circuits and D641-D644 are forward biased. With D641 and D644 forward biased, the collectors of Q174 and Q274 are coupled to the emitters of Q644 and Q654. Signals from channel 1 are now applied to the output amplifier.

When Q605 is in cutoff (see Fig. 3-10), D645 is forward biased and a voltage of about +63.2 volts is established at its cathode. This voltage will forward bias D642 and D643, which connects R642 and R643 to the Q174-Q274



1. Heavy lines indicate current paths, solid diodes indicate forward biased diodes.
2. Q605 is forward biased. Its required current is supplied through R605 from D646 and parallel resistors R642 and R643.
3. D646 is forward biased and the voltage at its anode is clamped at about +65.6 volts.
4. D646, D643 and D645 are reverse biased.
5. The current required by Q174 is supplied through D641, Q644, R648 and R649.
6. The current required by Q274 is supplied through D644, Q654, R658 and R659.
7. With D641 and D644 forward biased, the Channel 1 Input Amplifier is coupled to the Output Amplifier.

Fig. 3-9. Partial diagram showing the channel 1 set of Switching Diodes when Q605 is forward biased.



1. Heavy lines indicate current path, solid diodes indicate forward bias.
2. Q605 is reverse biased.
3. Current through D645 and parallel resistors R642 and R643 sets the voltage at the cathodes of D642, D643 and D645 to about +63.2 volts.
4. With D642 and D643 forward biased, the current required by Q174 and Q274 is supplied by parallel resistors R642 and R643.
5. With D641 and D644 reverse biased, Channel 1 signal currents are decoupled from the Output Amplifier.
6. Q644 and Q654 supply current to Q374 of Channel 2.

Fig. 3-10. Partial diagram showing the Channel 1 set of Switching Diodes when Q605 is reverse biased.

collector circuits. D641, D644 and D646 are reverse biased and disconnect the collector output of Q174-Q274 to the output amplifier.

The conduction state of Q615 controls the bias of the diodes in the channel 2 diode set in the same manner as Q605 controls their counterparts in the channel 1 set.

R642 and R643 provide the collector load and current return path for Q174 and Q274 when channel 1 is decoupled from the output amplifier. R652 and R653 provide the same function for Q374 and Q474 when channel 2 is decoupled.

Since the coupling and decoupling action of the diodes is dependent on the voltage developed across a conducting silicon diode, the voltage difference between the voltage supplies for this circuit is critical (see Switching and Output Amplifier schematic). A voltage divider circuit consisting of Q684, Zener diode D687, the two silicon diodes D688 and D689 and their associated circuitry, insure that the correct difference voltage is maintained between the supply voltages.

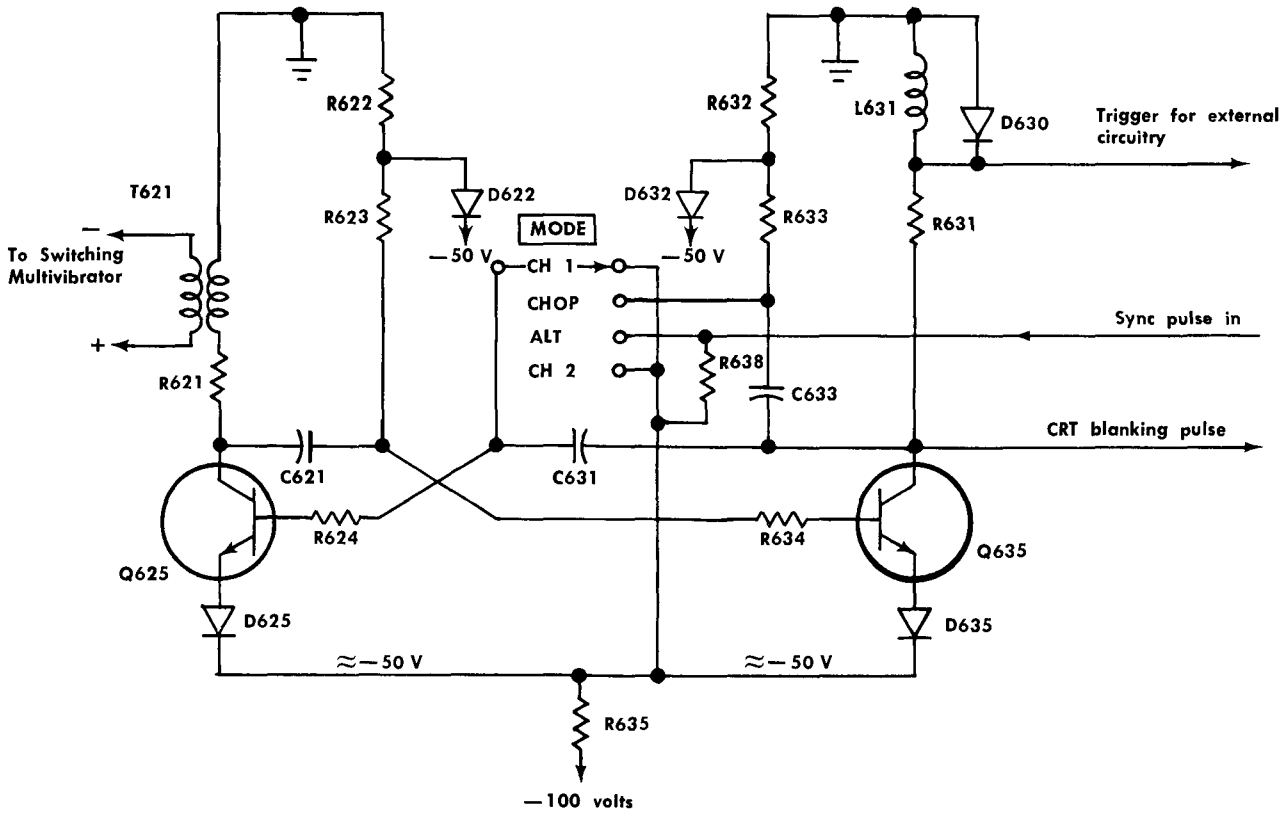
The driver multivibrator consists of Q625-Q635 and the associated circuitry (Fig. 3-11). When operating, the circuit provides three output pulses. A positive pulse to the switching multivibrator, a positive pulse to synchronize the companion plug-in unit, and a chop blanking pulse for the CRT circuit to blank the beam during channel switching time when operating in the CHOP mode. The multivibrator frequency can be synchronized to an external sync pulse, from the companion plug-in unit through pin 3 of the interconnecting plug P11.

With the Mode switch in CH 1 or CH 2 positions, the base of Q625 is returned through the switch contacts to the junction of R635 and the cathode side of diodes D625-D635. This sets the potential on the base of Q625 to approximately −51 volts, which is sufficient to reverse-bias the base emitter junction so the multivibrator is inoperative.

When the MODE switch is placed in the CHOP position, the base of Q625 is connected through the switch to the junction of R633-C633 which duplicates the voltage to the base of Q635. The multivibrator is now stable and switches at about 2 or 3 μs intervals.

When the MODE switch is set to ALT, the circuit is a monostable multivibrator. In the quiescent state, Q625 is reverse biased and Q635 forward biased. A positive pulse applied to the base of Q625 will cycle the circuit.

Each time the driver multivibrator cycles, pulses are coupled through T621 to the switching multivibrator. With the MODE switch in CHOP or ALT, the CRT display alternates between channel 1 and channel 2 at the driver multivibrator cycling rate. In CHOP mode, the channel switching rate is 2 to 3 μs. In ALT mode, the channel switching rate is



1. When the MODE switch is set to either CH 1 or CH 2, the base of Q625 is returned to the junction of R635 and the D625, D635 cathodes. This circuit inoperative.
2. When the MODE switch is set to CHOP, the circuit is astable.
3. When the MODE switch is set to ALT, the base of Q625 is returned to the junction of R635 and the D625, D635 cathodes through R638. The circuit is monostable and positive sync pulses will switch the circuit.
4. T621 couples pulses from the Driver Multivibrator to the Switching Multivibrator.
5. CRT blanking pulses are coupled from the collector of Q635.
6. Trigger pulses for external circuitry are coupled from the junction of R631, L631 and D630.

Fig. 3-11. Partial diagram showing the Driver Multivibrator.

determined by the pulse of the external signal used to cycle the driver multivibrator.

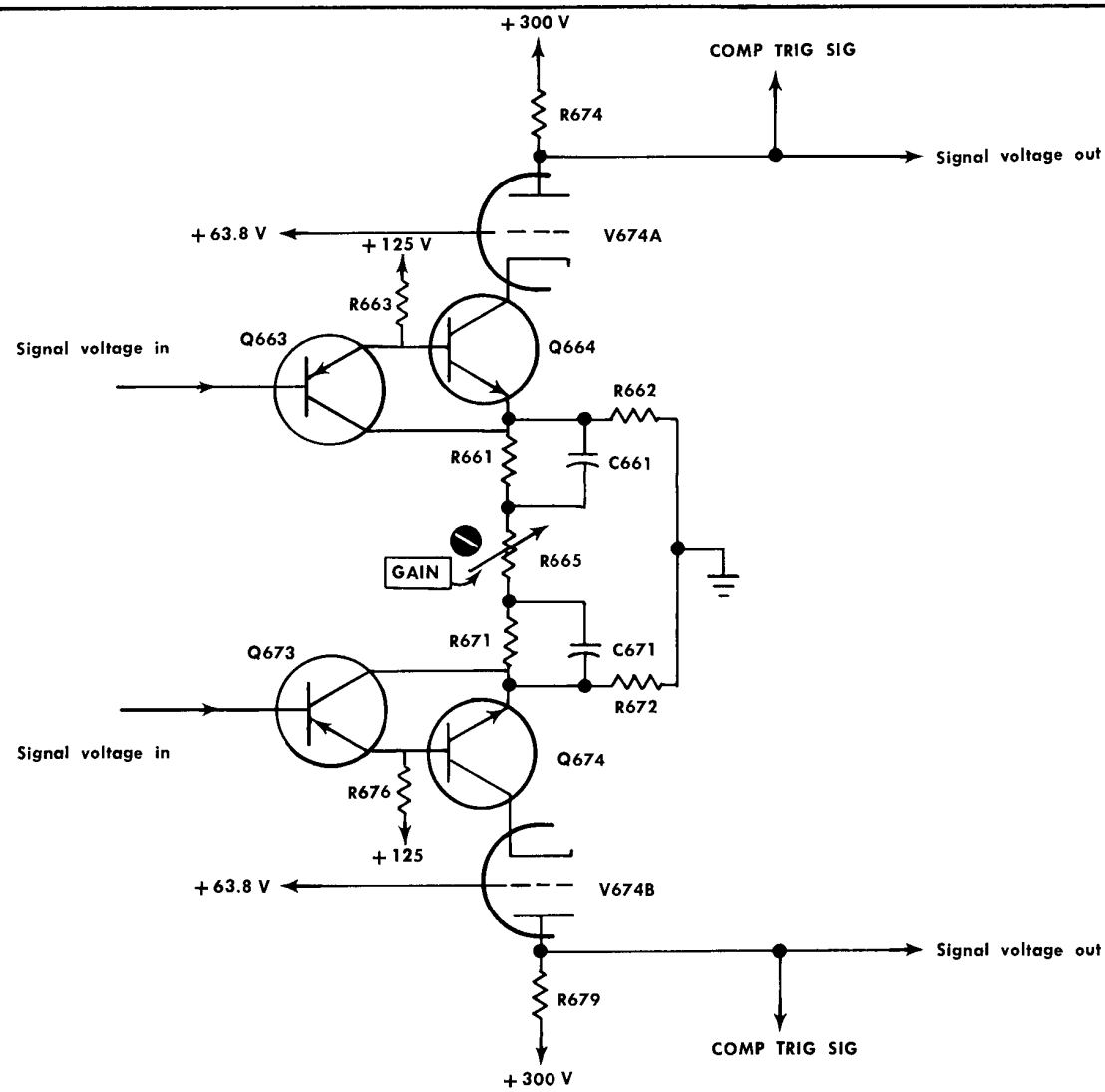
D625 and D635 provide base-to-emitter reverse-bias breakdown protection.

Output Amplifier

The output amplifier is common to both channel input amplifiers and is connected to the output of one channel or the other by means of the switching circuit. The amplifier provides the gain and power output to drive the CRT deflection plates with a high impedance push-pull signal. See Fig. 3-12.

Q644 and Q654 plus their circuitry convert output signal current, from the channel amplifier output stage, to signal voltage to drive the output amplifier stage.

The output amplifier contains emitter followers driving two cascode amplifiers with their input sections sharing a common emitter circuit. Gain of the stage is set by the plate-to-emitter load impedance ratio which can be calibrated by the front panel GAIN adjustment R665.



1. Q664 and V674A form a cascode amplifier and Q674 and V674B form a cascode amplifier.

2. Since Q644 and Q674 share a common emitter impedance and push-pull signals are applied to their bases, the combined circuitry is operated as a push-pull amplifier.

3. Gain control R665, adjusts the voltage gain of the stage.

Fig. 3-12. Parital diagram showing the Output Amplifier.

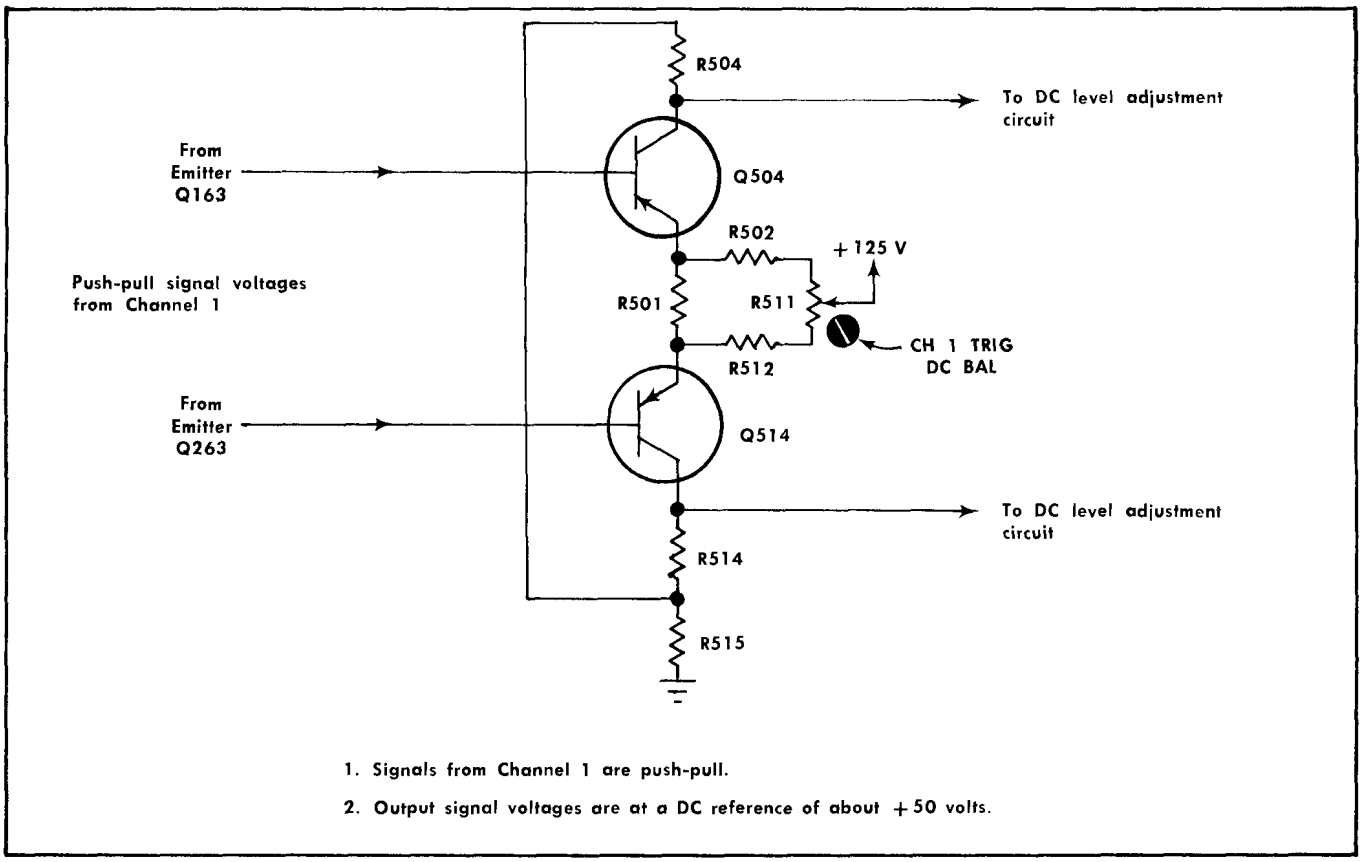
Q663 and Q673 stabilize the gain of the amplifier over a temperature range and increase the apparent input impedance to the cascode amplifier.

A composite trigger signal (output signal) is available to the trigger amplifier circuit at the plates of V674A and V674B.

Trigger Circuit

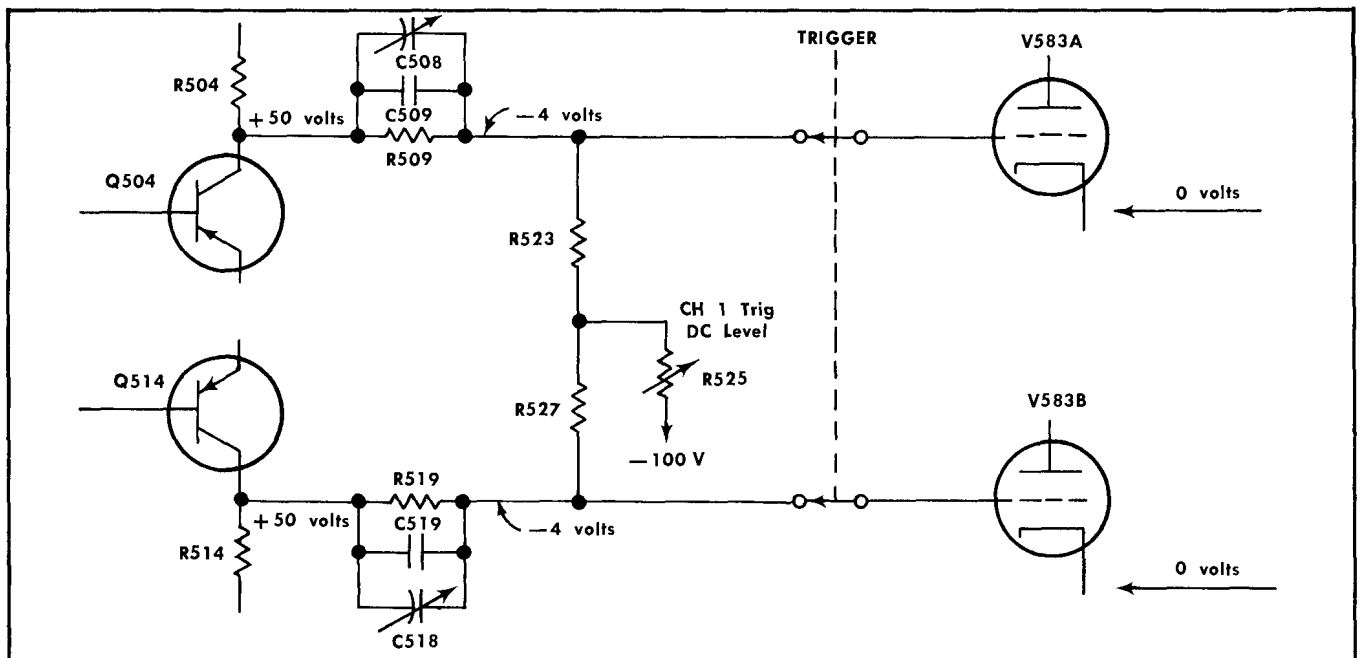
The trigger circuit contains a trigger DC level adjustment circuit for each selection of the TRIGGER selector, a trigger amplifier for each channel and two output cathode followers. The circuit provides three selections of trigger information, channel 1 (CH 1), composite (COMP) and channel 2 (CH 2). The DC reference level of the output trigger signals is adjustable to zero volts. The output of the circuit is applied through the plug in connector (P11) to provide a companion time base unit with internal trigger information.

When the TRIGGER switch is set to either CH 1 or CH 2 positions, the input to the cathode followers V583A-V583B, are connected through a coupling circuit to the output of the selected trigger amplifiers Q504, Q514 or Q534, Q544. Since the trigger amplifiers are driven by signals from their respective input amplifiers, the output trigger signal of the



1. Signals from Channel 1 are push-pull.
2. Output signal voltages are at a DC reference of about +50 volts.

Fig. 3-13. Partial diagram showing the Channel 1 Trigger Amplifier.



1. The DC reference at the collectors of Q504 and Q514 is about +50 volts.
2. With R525 properly adjusted, the DC reference at the R509, R523 and R519, R527 junctions is about −4 volts.
3. Cathode followers V583A and V583B operate with about 4 volts of bias.
4. With the TRIGGER switch set to CH 1, R525 sets the DC reference of the output trigger signals to zero volts.

Fig. 3-14. Partial diagram showing the Channel 1 Trigger DC Level adjustment circuit.

common cathode followers originate from the selected channel. The DC level of each trigger amplifier is balanced by adjustments R525 and R555.

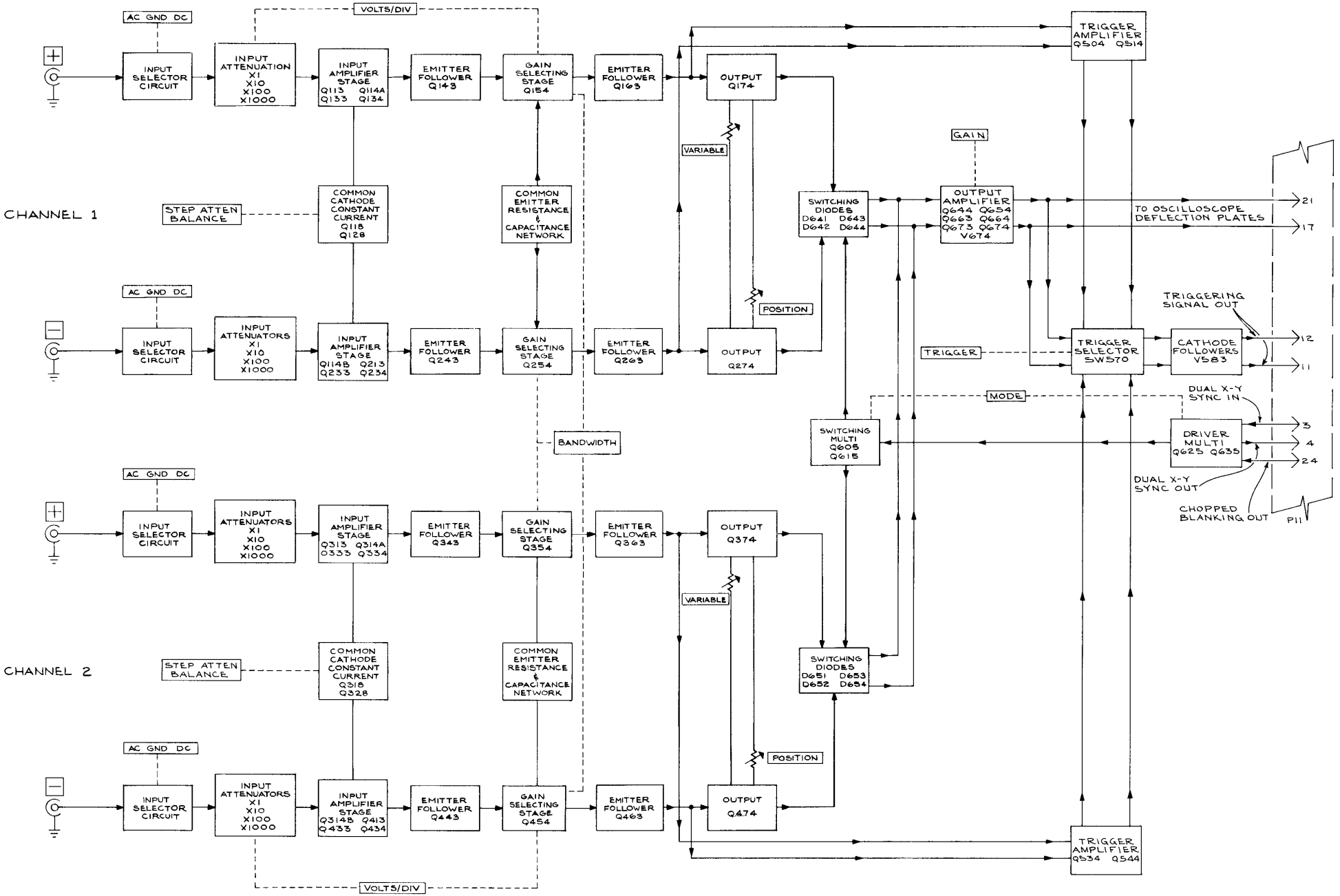
When the COMP position is selected, the input to the cathode followers is coupled to the plates of V674 in the output amplifier. Since the drive to the output amplifier is a function of the MODE switch setting, the origin of the trigger signals is the channel that is displayed. The DC level of the trigger signal to the time base unit is again set by the Comp Trig DC Level R565.

Q504 and Q514 with their associated circuitry form the channel 1 trigger amplifier (Fig. 3-13). The circuit is a conventional emitter coupled amplifier operated push-pull. The constant DC operating current of the circuit is set and balanced by returning the emitters to +125 volts through R502 and CH 1 Trig DC Bal adjustment R511.

Push-pull signal voltages from the channel 1 emitter followers, Q163 and Q263, are coupled to the bases of Q504 and Q514. The amplifier push-pull signal voltage at the collectors of Q504 and Q514 is at a DC level of about +50 volts.

A trigger DC Level adjustment circuit for each trigger selection provides a means of setting the DC output reference voltage at the cathodes of V583 to zero volts. A voltage divider network to the —100 volt supply that includes the respective CH or Comp Trig DC Level adjustments R525, R555 or R565, sets the DC level at the grids of the cathode follower V583, so the output level at the cathodes is 0 V. See Fig. 3-14.

High frequency compensation is provided by adjustments C508 and C518 for CH 1, C538 and C548 for CH 2, C561 and C569 for the composite signal.

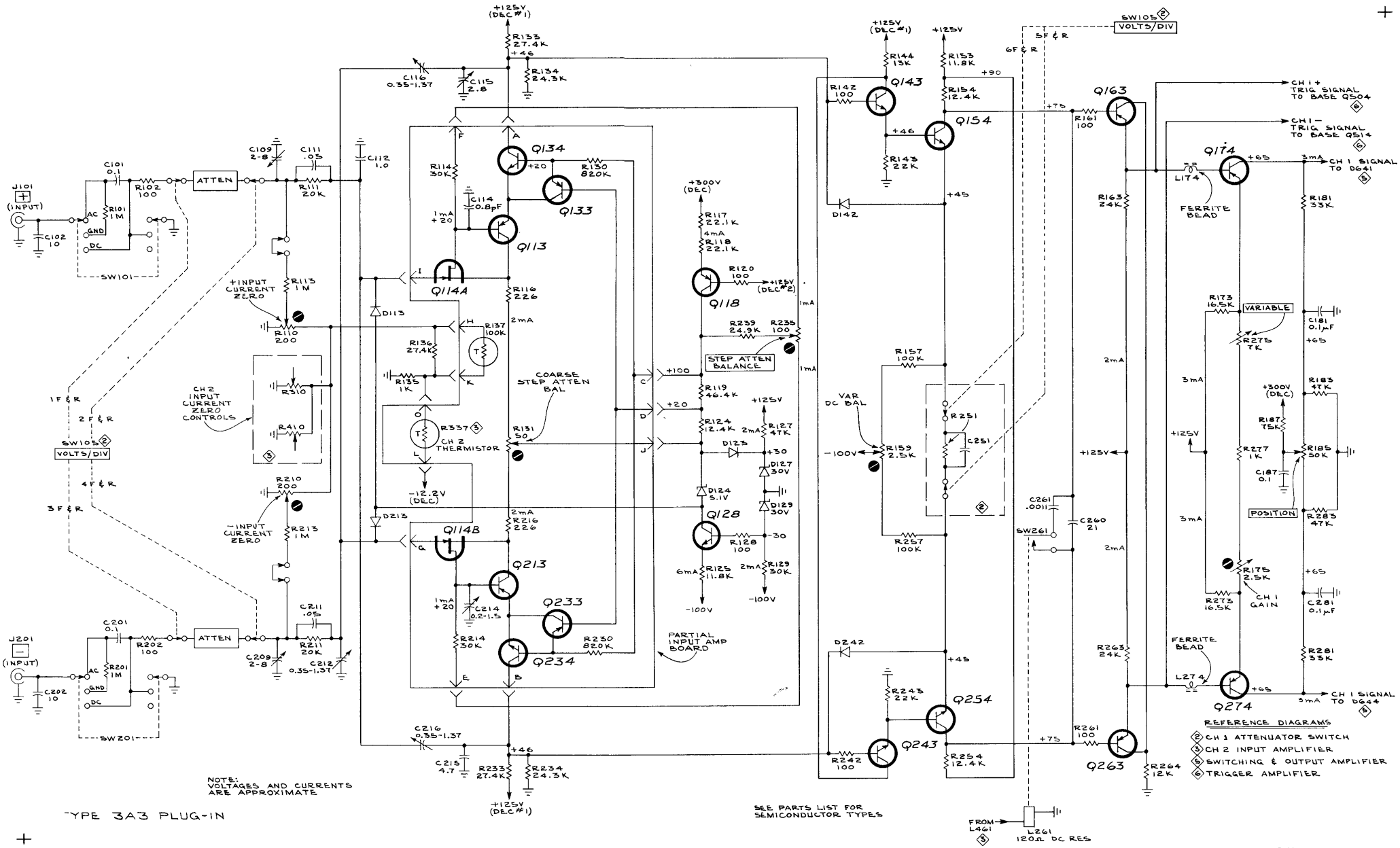


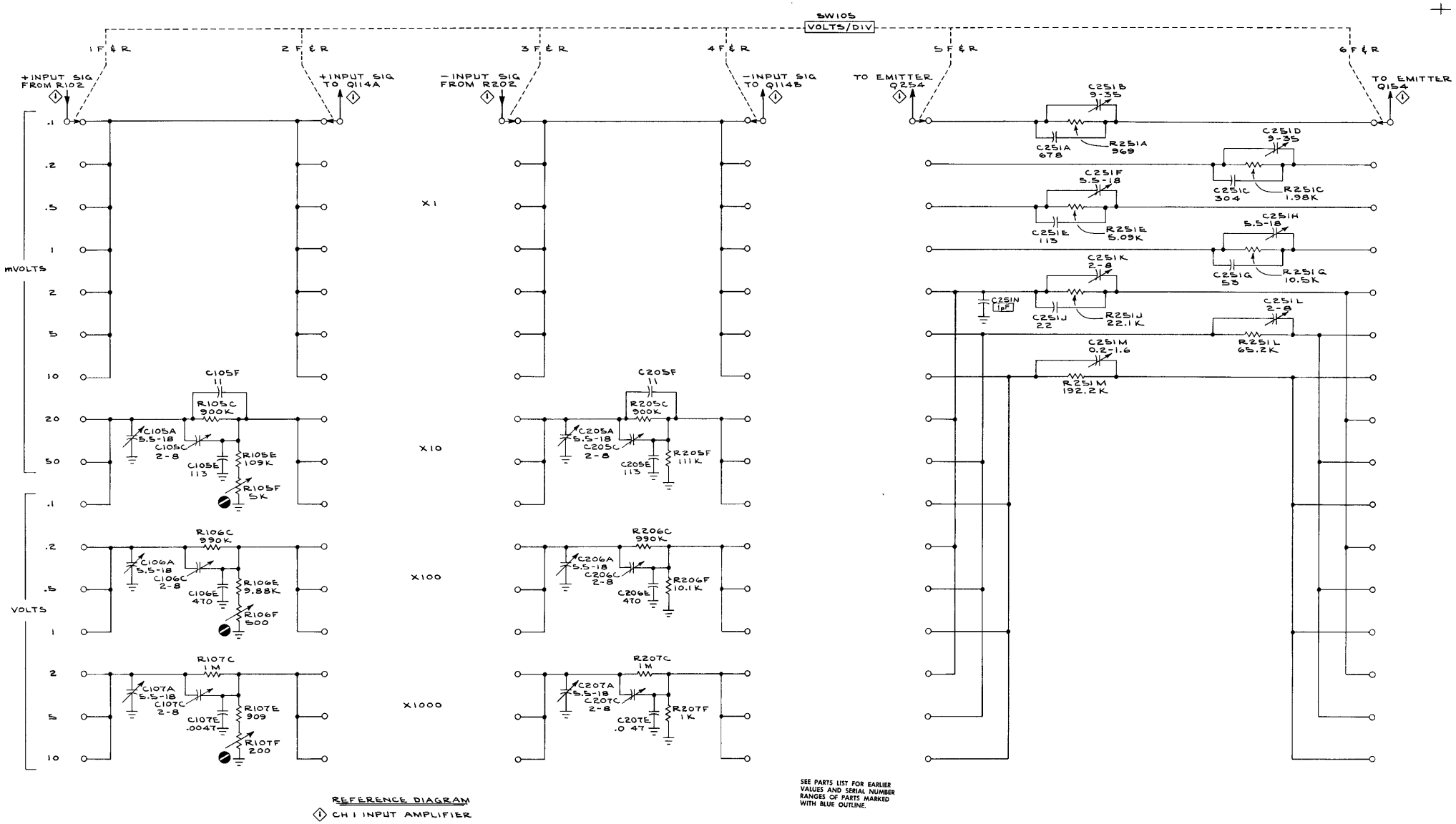
PLM
268

TYPE 3A3 PLUG-IN

BLOCK DIAGRAM

(S/N 4990-UP)


J101 (INPUT)
C101 0.1
R102 100
ATTEN
C109 2-8
C111 .05
C112 1.0
R111 20K
AC
R101 1M
GND
DC
C102 10
SW101
+INPUT CURRENT ZERO
R113 1M
R110 200
CH 2 INPUT CURRENT ZERO CONTROLS
R310
R410
1F & R
2F & R
SW105 VOLTS/DIV
4F & R
3F & R
R210 200
-INPUT CURRENT ZERO
R213 1M
J201 (INPUT)
C201 0.1
R202 100
R201 1M
C202 10
SW201
C209 2-8
C211 .05
C212 0.35-1.3pF
+125V (DEC #1)
R133 27.4K
+46
R134 24.3K
C116 0.35-1.3pF
C115 2.8
Q134
R130 820K
Q133
R114 30K
C114 0.8pF
1mA +20
Q113
Q114A
R116 226
D113
2mA
R137 100K
R136 27.4K
R135 1K
COARSE STEP ATTEN BAL
R337
CH 2 THERMISTOR
R131 50
-12.2V (DEC)
D213
Q114B
R216 226
Q213
Q233
Q234
C214 0.2-1.5
R214 30K
R230 820K
PARTIAL INPUT AMP BOARD
C216 0.35-1.3pF
C215 4.7
R233 27.4K
R234 24.3K
+125V (DEC #1)
+300V (DEC)
R117 22.1K
4mA
R118 22.1K
Q118
R120 100
+125V (DEC #2)
1mA
R239 24.9K
R235 100
STEP ATTEN BALANCE
+100
+20
+30
R119 46.4K
R124 12.4K
2mA
R127 47K
D123
D127 30V
D124 5.1V
D129 30V
Q128
R128 100
-30
6mA
R125 11.8K
R129 30K
-100V
+125V (DEC #1)
R144 13K
Q143
R142 100
D142
+46
R143 22K
+125V
R153 11.8K
+90
R154 12.4K
Q154
+45
R157 100K
VAR DC BAL
-100V
R159 2.5K
R251
C251
R257 100K
D242
R243 22K
Q254
Q243
R242 100
R254 12.4K
SW105 VOLTS/DIV
5F & R
6F & R
Q163
+75
R161 100
R163 24K
2mA
+125V
C261 .0011
SW261
C260 21
R261 100
Q263
R264 12K
CH 1 + TRIG SIGNAL TO BASE Q504
CH 1 - TRIG SIGNAL TO BASE Q514
Q174
+65
3mA
L174
FERRITE BEAD
CH 1 SIGNAL TO D641
R181 33K
R173 16.5K
VARIABLE
R275 TK
C181 0.1μF
R183 47K
+300V (DEC)
R187 TSK
R277 1K
R185 50K
C187 0.1
POSITION
R283 47K
R175 2.5K
CH 1 GAIN
R273 16.5K
C281 0.1μF
R263 24K
FERRITE BEAD
L274
Q274
R281 33K
CH 1 SIGNAL TO D644
REFERENCE DIAGRAMS
2 CH 1 ATTENUATOR SWITCH
3 CH 2 INPUT AMPLIFIER
5 SWITCHING & OUTPUT AMPLIFIER
6 TRIGGER AMPLIFIER
FROM L461
L261 120Ω DC RES
NOTE: VOLTAGES AND CURRENTS ARE APPROXIMATE
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3A3 PLUG-IN
PLM 268
CH 1 INPUT AMPLIFIER 1
(S/N 4990 -UP)



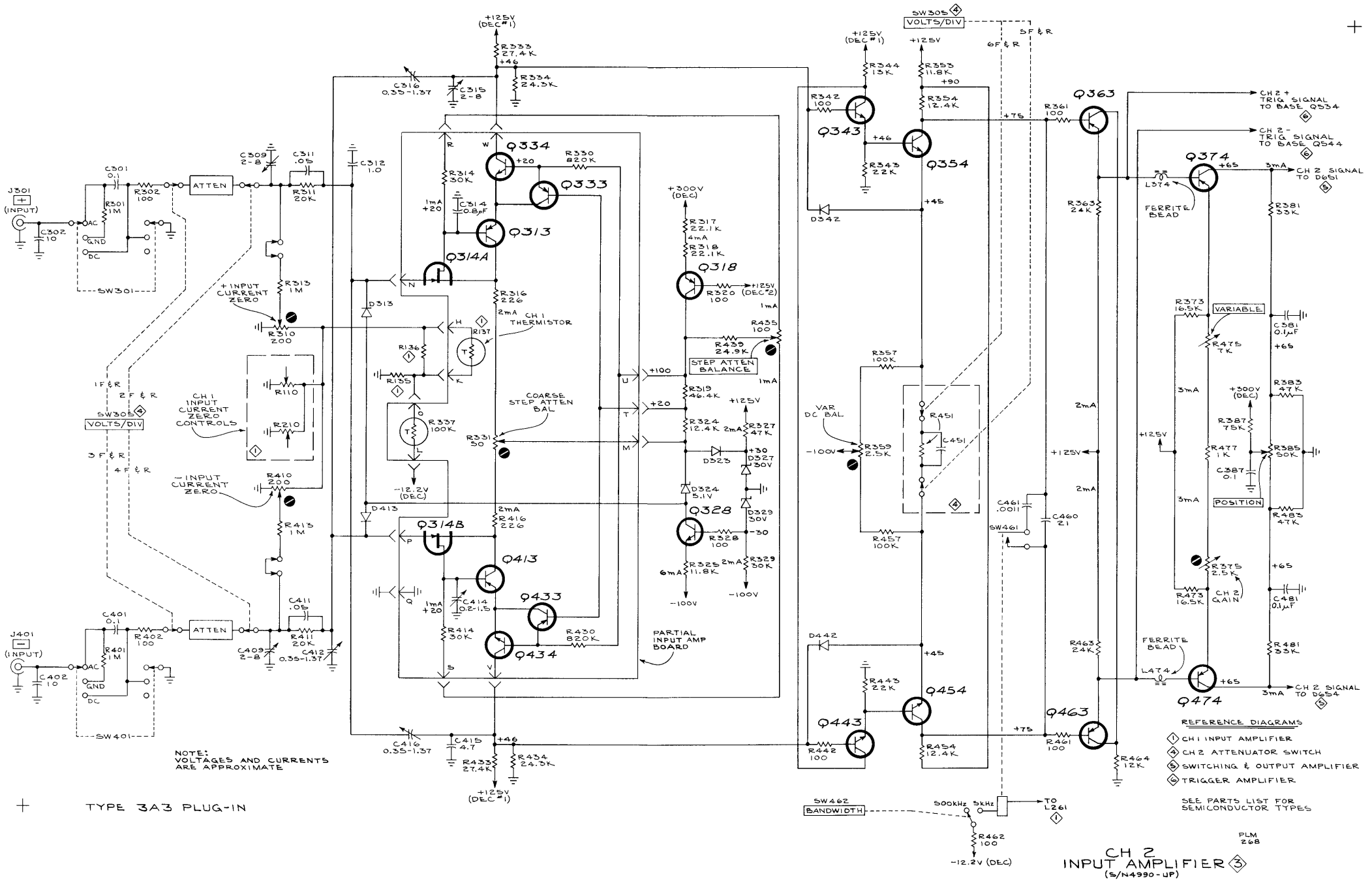
REFERENCE DIAGRAM
① CH 1 INPUT AMPLIFIER

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

TYPE 3A3 PLUG-IN

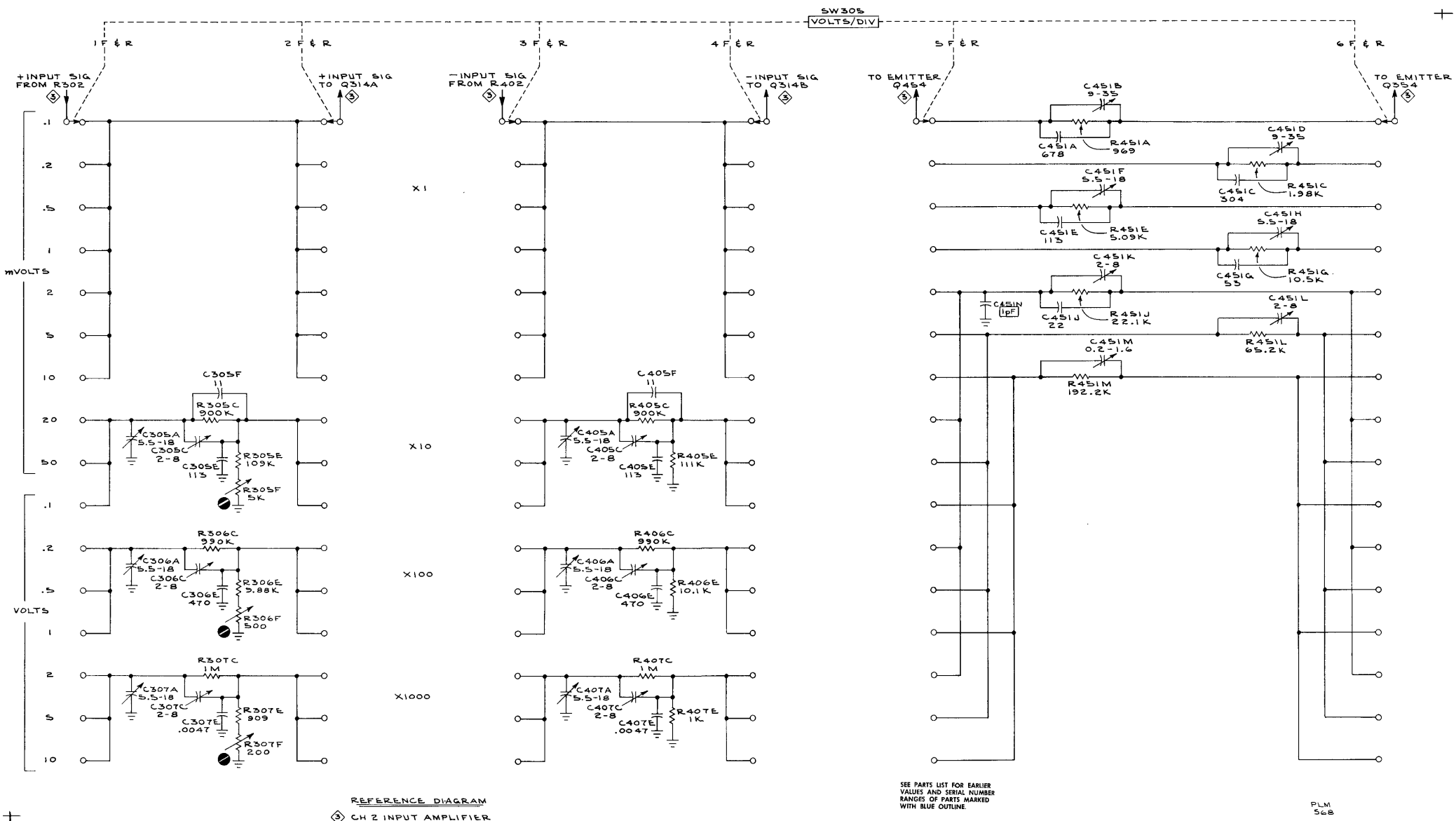
PLM
568

CH 1 ATTENUATOR SWITCH ②
(S/N 4990-UP)



CH 2 INPUT AMPLIFIER 3

(S/N 4990 - UP)



REFERENCE DIAGRAM

③ CH 2 INPUT AMPLIFIER

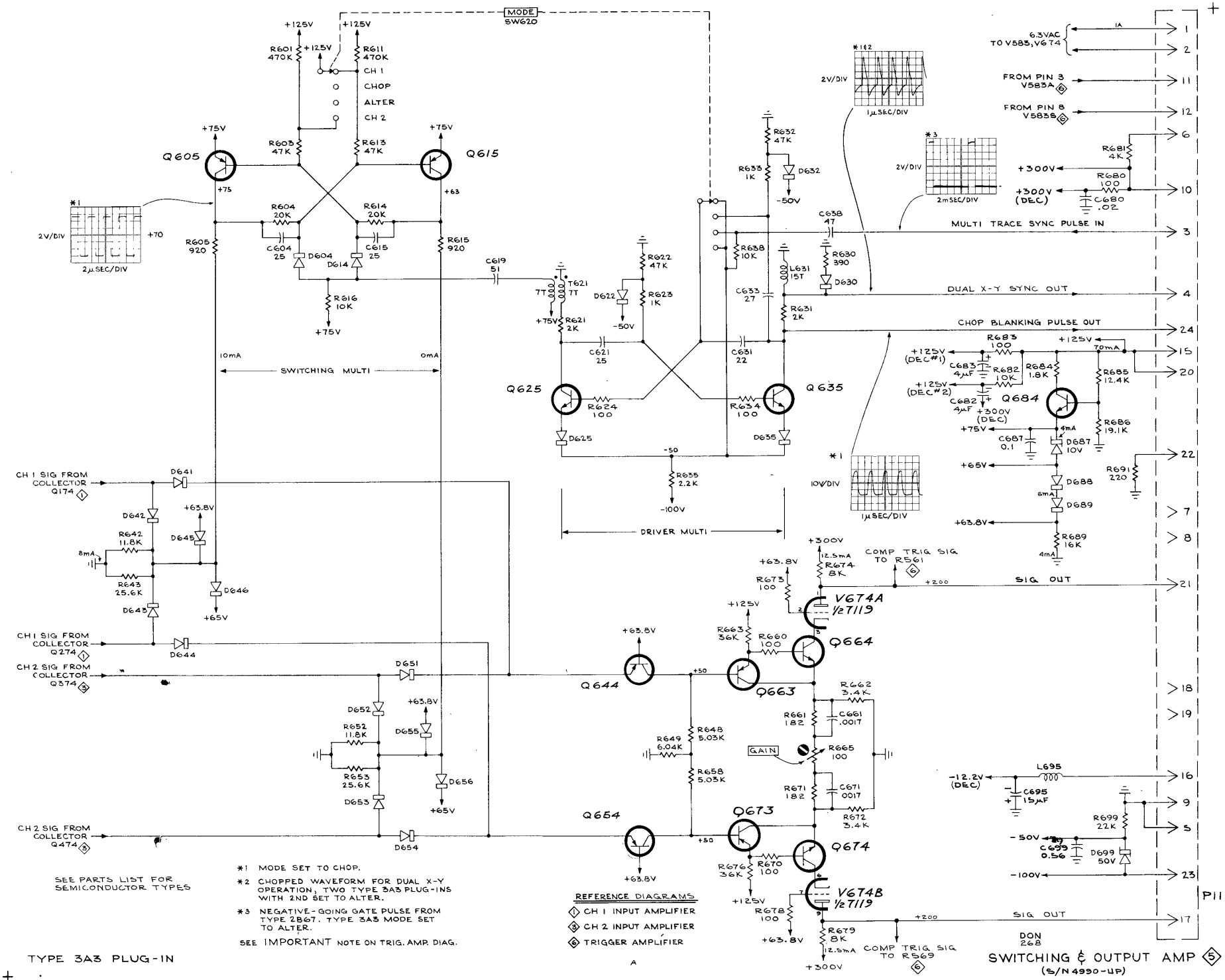
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

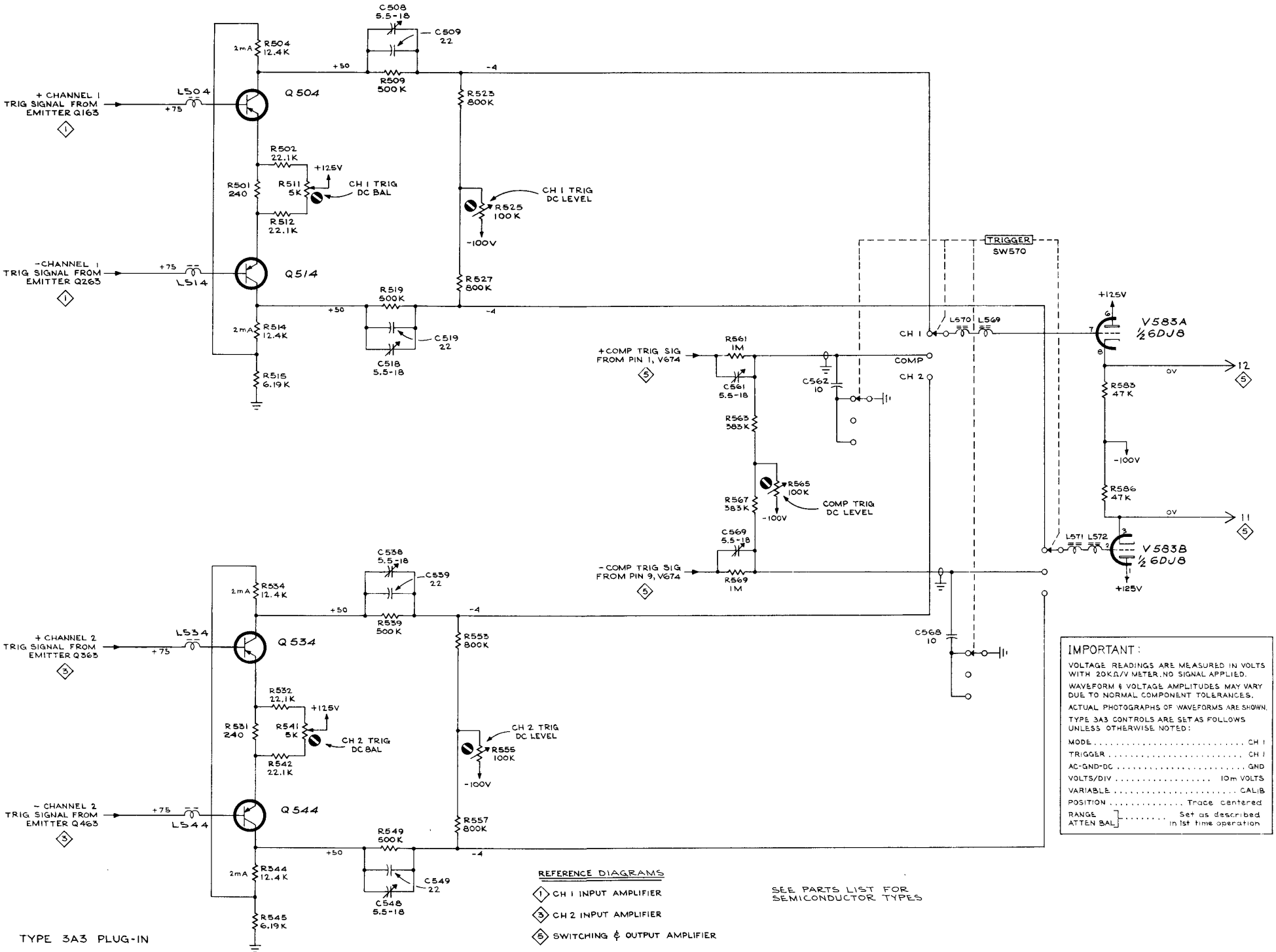
PLM 568

CH 2 ATTENUATOR SWITCH ④

(S/N 4990-UP)

TYPE 3A3 PLUG-IN


MODE SW620
+125V
R601 470K
R611 470K
CH 1
CHOP
ALTER
CH 2
Q605
Q615
R603 47K
R613 47K
R604 20K
R614 20K
C604 25
C615 25
D604
D614
R605 920
R615 920
R616 10K
+75V
+70
+63
*1
2V/DIV
2μSEC/DIV
C619 51
T621
7T
R621 2K
R622 47K
R623 1K
D622
-50V
C621 25
C631 22
Q625
Q635
R624 100
R634 100
D625
D635
R635 2.2K
-100V
10mA
0mA
SWITCHING MULTI
DRIVER MULTI
R632 47K
R633 1K
D632
R638 10K
L631 15T
C638 47
R630 390
D630
C633 27
R631 2K
*2
2V/DIV
1μSEC/DIV
*3
2mSEC/DIV
6.3VAC TO V583, V674
FROM PIN 3 V583A
FROM PIN 8 V583B
MULTI TRACE SYNC PULSE IN
DUAL X-Y SYNC OUT
CHOP BLANKING PULSE OUT
R681 4K
R680 100
+300V
+300V (DEC)
C680 .02
R683 100
+125V (DEC#1)
C683 4μF
R682 10K
R684 1.8K
R685 12.4K
+125V (DEC#2)
C682 4μF
Q684
R686 19.1K
C687 0.1
D687 10V
D688
D689
R691 220
R689 16K
+65V
+63.8V
10V/DIV
CH 1 SIG FROM COLLECTOR Q174
CH 1 SIG FROM COLLECTOR Q274
CH 2 SIG FROM COLLECTOR Q374
CH 2 SIG FROM COLLECTOR Q474
D641
D642
D643
D644
D645
D646
R642 11.8K
R643 25.6K
8mA
D651
D652
D653
D654
D655
D656
R652 11.8K
R653 25.6K
Q644
Q654
R648 5.03K
R649 6.04K
R658 5.03K
+50
+63.8V
+65V
R674 8K
12.5mA
COMP TRIG SIG TO R561
R673 100
V674A ½T119
Q664
Q663
R663 36K
R660 100
R662 3.4K
R661 182
C661 .0017
GAIN
R665 100
R671 182
C671 0017
R672 3.4K
Q673
Q674
R676 36K
R670 100
V674B ½T119
R678 100
R679 8K
COMP TRIG SIG TO R569
SIG OUT
+200
L695
-12.2V (DEC)
C695 15μF
R699 22K
C699 0.56
D699 50V
-50V
-100V
1
2
11
12
6
10
3
4
24
15
20
22
7
8
18
19
16
9
5
23
17
P11
DON 268
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
*1 MODE SET TO CHOP.
*2 CHOPPED WAVEFORM FOR DUAL X-Y OPERATION, TWO TYPE 3A3 PLUG-INS WITH 2ND SET TO ALTER.
*3 NEGATIVE-GOING GATE PULSE FROM TYPE 2B67. TYPE 3A3 MODE SET TO ALTER.
SEE IMPORTANT NOTE ON TRIG. AMP. DIAG.
REFERENCE DIAGRAMS
1 CH 1 INPUT AMPLIFIER
3 CH 2 INPUT AMPLIFIER
6 TRIGGER AMPLIFIER
TYPE 3A3 PLUG-IN
SWITCHING & OUTPUT AMP 5
(S/N 4990-UP)
A


+ CHANNEL 1 TRIG SIGNAL FROM EMITTER Q163
- CHANNEL 1 TRIG SIGNAL FROM EMITTER Q263
+ CHANNEL 2 TRIG SIGNAL FROM EMITTER Q363
- CHANNEL 2 TRIG SIGNAL FROM EMITTER Q463
L504
L514
L534
L544
+75
Q504
Q514
Q534
Q544
2mA
R504 12.4K
R514 12.4K
R534 12.4K
R544 12.4K
R515 6.19K
R545 6.19K
C508 5.5-18
C509 22
R509 500K
C518 5.5-18
C519 22
R519 500K
C538 5.5-18
C539 22
R539 500K
C548 5.5-18
C549 22
R549 500K
+50
-4
R502 22.1K
R501 240
R511 5K
R512 22.1K
+125V
CH 1 TRIG DC BAL
R532 22.1K
R531 240
R541 5K
R542 22.1K
CH 2 TRIG DC BAL
R523 800K
R525 100K
-100V
CH 1 TRIG DC LEVEL
R527 800K
R553 800K
R555 100K
CH 2 TRIG DC LEVEL
R557 800K
+COMP TRIG SIG FROM PIN 1, V674
-COMP TRIG SIG FROM PIN 9, V674
R561 1M
C561 5.5-18
R569 1M
C569 5.5-18
C562 10
C568 10
R563 383K
R567 383K
R565 100K
COMP TRIG DC LEVEL
COMP
CH 1
CH 2
TRIGGER SW570
L570 L569
L571 L572
V583A ½6DJ8
V583B ½6DJ8
R583 47K
R586 47K
0V
12
11
IMPORTANT:
VOLTAGE READINGS ARE MEASURED IN VOLTS WITH 20KΩ/V METER, NO SIGNAL APPLIED.
WAVEFORM & VOLTAGE AMPLITUDES MAY VARY DUE TO NORMAL COMPONENT TOLERANCES.
ACTUAL PHOTOGRAPHS OF WAVEFORMS ARE SHOWN.
TYPE 3A3 CONTROLS ARE SET AS FOLLOWS UNLESS OTHERWISE NOTED:
MODE ..... CH 1
TRIGGER ..... CH 1
AC-GND-DC ..... GND
VOLTS/DIV ..... 10m VOLTS
VARIABLE ..... CALIB
POSITION ..... Trace centered
RANGE, ATTEN BAL ..... Set as described in 1st time operation
REFERENCE DIAGRAMS
1 CH 1 INPUT AMPLIFIER
3 CH 2 INPUT AMPLIFIER
5 SWITCHING & OUTPUT AMPLIFIER
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
TYPE 3A3 PLUG-IN