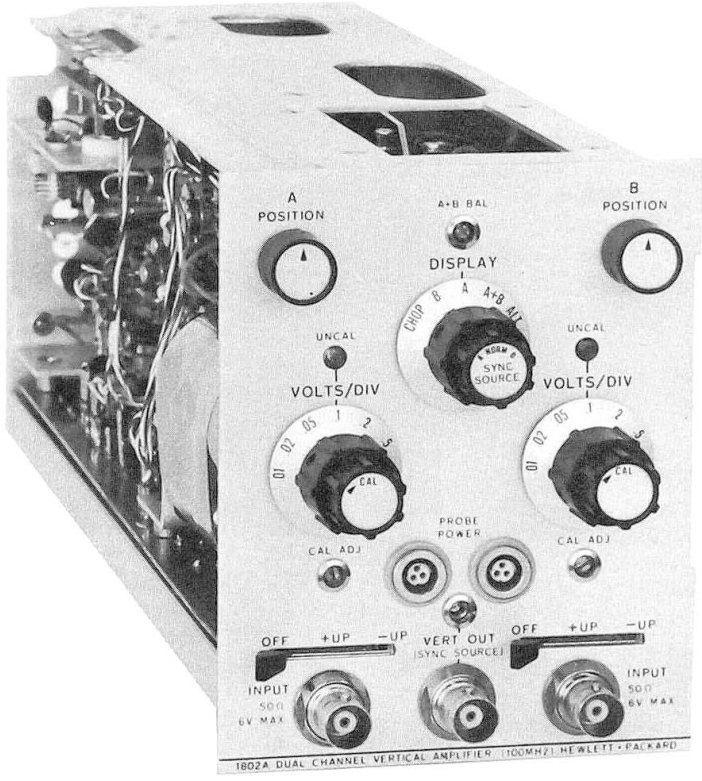


Figure 1-1. Model 1802A Dual Channel Vertical Amplifier

Table 1-1. Specifications

MODES OF OPERATION

Channel A alone; Channel B alone; Channels A and B displayed alternately on successive sweeps (ALT); Channels A and B displayed by switching at approx. 400 kHz rate between channels (CHOP), with blanking during switching; Channel A plus Channel B (algebraic addition). Vertical output allows cascading of channels.

EACH CHANNEL

BANDWIDTH

DIRECT: DC to greater than 100 MHz (3 dB down from 8 div reference signal); with channels cascaded, dc to greater than 75 MHz.

WITH MODEL 1123A ACTIVE PROBE: Same as Direct for source resistances from 0 to 150 ohms.

WITH MODEL 10020A RESISTIVE DIVIDER PROBES: Same as Direct for source resistances from 0 to 750 ohms.

WITH MODEL 10201A-D RESISTIVE DIVIDER PROBES: Same as Direct for source resistances from 0 to 1000 ohms.

RISETIME

DIRECT: Less than 3.5 ns (10% to 90% with 6 div input step); with channels cascaded, less than 4.5 ns.

WITH MODEL 1123A ACTIVE PROBE: Same as Direct for source resistances from 0 to 150 ohms.

WITH MODEL 10020A RESISTIVE DIVIDER PROBES: Same as Direct for source resistances from 0 to 750 ohms.

WITH MODELS 10201A-D RESISTIVE DIVIDER PROBES: Same as Direct for source resistances from 0 to 1000 ohms.

PULSE RESPONSE

(6 div reference at 25° C) overshoot,<3% perturbations,<3%; tilt, <2%. With channels cascaded: overshoot,<5%; perturbations,<5%; tilt,<3%.

DEFLECTION FACTOR

RANGES: From 0.01 V/div to 1 V/div (7 positions) in a 1, 2, 5 sequence. ±3% accuracy with Vernier in calibrated position; calibration adjustment provided on front panel. Channels may be cascaded using vertical output to obtain 1, 2, or 5 mV/div.

VERNIER: With UNCAL (uncalibrated) light, continuously variable between all ranges; extends maximum deflection factor to at least 2.5 V/div.

POLARITY

+UP or -UP, selectable; OFF position disconnects signal input from amplifier, terminates input

SECTION I
GENERAL INFORMATION

1-1. GENERAL DESCRIPTION.

1-2. The Model 1802A is a dual channel vertical amplifier (see Figure 1-1) designed to operate as an integral part of the HP Model 180-Series Oscilloscopes. Its unique design features fixed input impedance (50 ohms), wide band pass (dc to 100 MHz), and a higher sensitivity when operated in cascade than most standard vertical plug-ins (see detailed theory in Section IV). Refer to Table 1-1 for instrument specifications.

1-3. During operation, the Model 1802A can be direct-coupled (by 50-ohm coax) to examine signals originating from 50-ohm sources, or with the use of an active probe (e.g., the Model 1123A) it can be used to examine high frequency signals within an operating circuit. For low level signals, the vertical and sync amplifiers can be operated in cascade to produce a higher gain, thereby increasing overall instrument sensitivity; and, in this configuration, bandwidth is 75 MHz. The DISPLAY control permits the selection

Table 1-1. Specifications (Cont'd)

signal in 50 ohms, and grounds amplifier input for reference.

SIGNAL DELAY

Input signals are delayed sufficiently to view leading edge of input pulse without advance external trigger.

DYNAMIC RANGE

6 divisions for signals to 100 MHz, increasing to 8 div at 50 MHz.

POSITIONING RANGE

Allows positioning top of a 6 div pulse to center graticule line.

DRIFT

Less than ±1 div over environmental temperature range (except for cascaded operation).

INPUT IMPEDANCE

50 ohms ±2 ohms.

MAXIMUM INPUT

6V rms.

VSWR

Less than 1.35:1 at 100 MHz on 0.01 V/div; less than 1.1:1 at 100 MHz on all other deflection factors.

REFLECTION COEFFICIENT

Less than 15% at 100 MHz on 0.01 V/div; less than 5% at 100 MHz on all other deflection factors.

PROBE POWER

Provides power to operate Model 1123A Active Probe.

A + B OPERATION

AMPLIFIER

Bandwidth and deflection factor are unchanged; either channel may be inverted to give ±A±B operation.

DIFFERENTIAL INPUT (A-B)

Common mode rejection ratio greater than 40 dB for frequencies to 1 MHz, greater than 20 dB to 100 MHz; common mode signal, up to amplitude equivalent of 6 div deflection.

TRIGGERING

MODE

Normal, on the signal displayed as selected by DISPLAY switch; A, on Channel A signal; B, on Channel B signal.

FREQUENCY

DC to greater than 120 MHz on 1 div pk-pk signal for Models 1820B or 1822A time base plug-ins; or from DC to greater than 75 MHz on 1 div pk-pk signal for Models 1820A or 1821A time base plug-ins.

VERTICAL SIGNAL OUTPUT

AMPLITUDE

100 mV/div of displayed signal into 50-ohm load, adjustable with front panel control; usable amplitude, 600 mV pk-pk.

BANDWIDTH

DC to greater than 100 MHz.

RISETIME

Less than 3.5 ns.

GENERAL

WEIGHT

Net, 4 1/2 pounds (2,0 kg); shipping, 7 pounds (3,2 kg).

ENVIRONMENT

Same as Model 180A/AR except temperature which is 0° C to +55° C.

ACTIVE COMPONENTS

All solid-state.

ACCESSORIES FURNISHED

Calibrator adapter (HP Part No., 01802-63201).

of CHOP, B, A, A + B, and ALT, which increases the versatility of the system.

1-4. INSTRUMENT IDENTIFICATION.

1-5. Hewlett-Packard uses an eight-digit serial number (000-00000) for unit identification. The first three digits are referred to as the "serial prefix" and separated from the rest of the digits by a hyphen. Succeeding digits identify a particular instrument within the series. The instrument serial number is located on a plate riveted to the rear panel.

1-6. MANUAL CHANGES.

1-7. A "serial prefix" number is printed on the title page to associate this manual with a specific series of instruments. Since it is readily known what instrument is covered by the manual, it is relatively easy to provide backdating for earlier instruments and updating by the use of "Manual Change" sheets for later instruments. Refer to Section VII for backdating information. All updating information is incorporated as insert sheets entitled "Manual Changes". All questions concerning the instrument or manual should be directed to your nearest Hewlett-Packard Sales/Service Office. Be sure to include the instrument model and complete HP serial number in all correspondence.

1-8. ACCESSORY PROBE.

1-9. The Model 1123A Voltage Probe was designed for use with the Model 1802A to ensure maximum versatility. Probe input impedance is 100k ohms paralleled by 3.5 picofarads of capacitance. Output impedance is 50 ohms which furnishes a matched source for the 50-ohm input of the Model 1802A.

1-10. SCOPE OF MANUAL.

1-11. This section contains general information about the Model 1802A instrument and manual. Each subsequent section provides detailed facts concerning the particular area being dealt with; e.g., Section III furnishes detailed operation instructions for specific measurement functions. To ensure a thorough understanding of the Model 1802A, its operation is discussed at four different levels of complexity: (1) General Description (in this section), (2) Functional Description (in Section IV), (3) Detailed Theory of Operation (in Section IV), and (4) Simplified Circuit Theory (preceeding both the Functional Description and the Detailed Theory of Operation) also in Section IV.

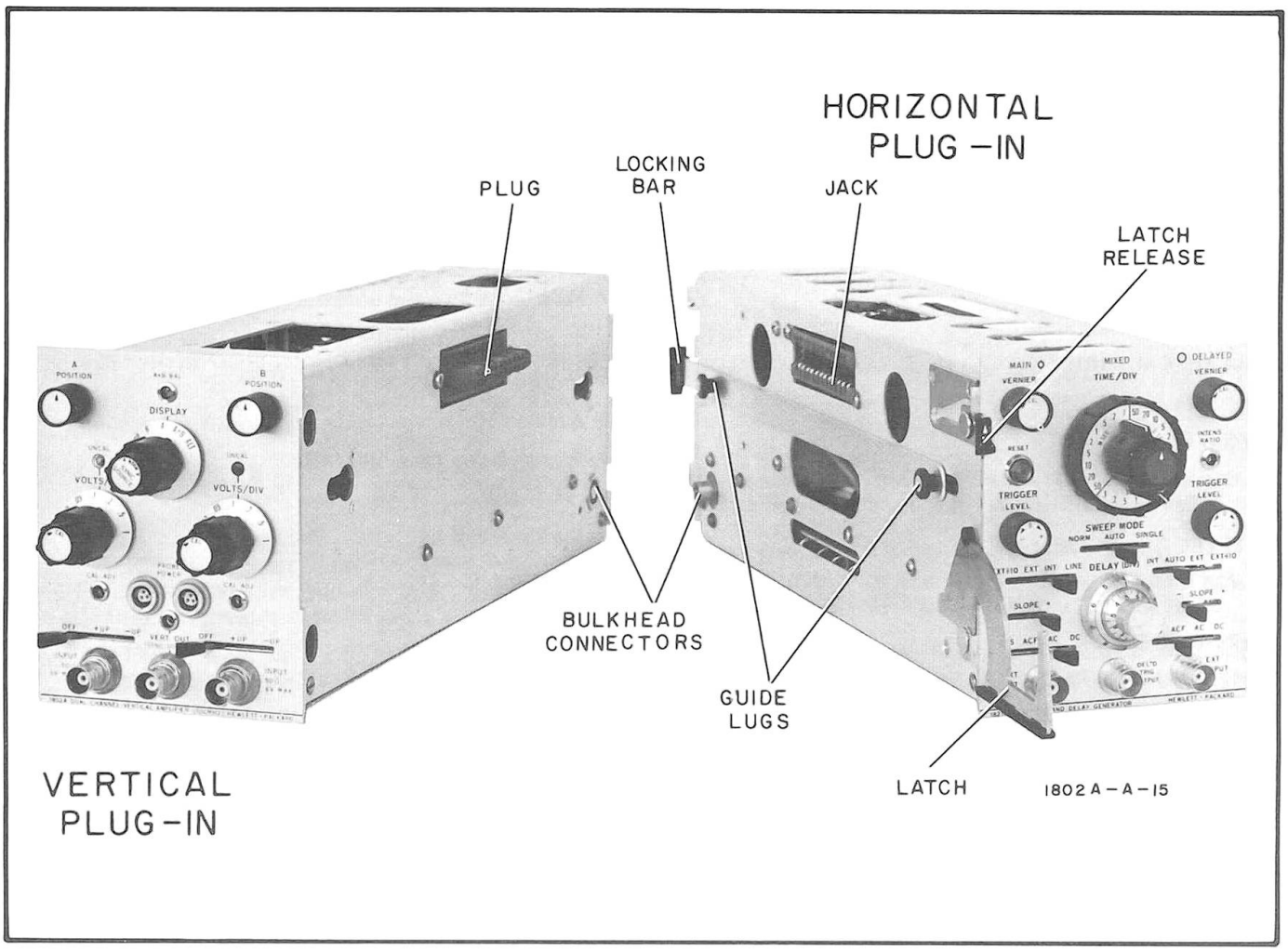


Figure 2-1. Plug-In Mating

4-18. FUNCTIONAL DESCRIPTION.

4-19. Figure 4-7 is a functional block diagram designed to show the signal flow through the Model 1802A.

4-20. This amplifier is designed to accept vertical signals at INPUT A and B. To accommodate a wide dynamic range of voltage, each input has an attenuator which reduces the signal amplitude to the Input Amplifier. Each channel is attenuated separately; therefore, vertical signals with wide voltage differences can be accepted simultaneously. Also, each channel has a polarity switch which allows the user to view either positive (+) signals up or negative (-) signals up. In the OFF position, these switches disconnect their respective inputs and terminate the inputs with 50 ohms.

4-21. After attenuation and desired polarity selection, the input signals are amplified and distributed to both Vertical Channel Amplifiers and the Sync Channel Amplifiers. Position controls connected to the Vertical Amplifiers provide positioning of the two signals to any desired screen location. Immediately following the Input Amplifiers are diode gating networks which determine which signal or combination of signals is displayed on the CRT. The selected vertical signal is routed through a delay line, amplified by the Vertical Output Amplifier and applied to the CRT vertical deflection plates.

4-22. The vertical signal is delayed approximately 160 ns by the delay line, giving the Sync Amplifier sufficient time to provide a sync output before the vertical signal is applied to the deflection plates. This allows the sweep to be started slightly before the vertical signal reaches the plates and permits viewing of the leading edge of the signal.

4-23. Following the Input Amplifier is a gating network for the Sync Amplifier which allows the operator to select a sync output which is independent of the displayed vertical signal. The selected signal is amplified and used as a sync signal to the time base plug-in and also applied to the front panel as an inverted vertical output.

4-24. MODES OF OPERATION.

4-25. The DISPLAY control lets the operator select any of five modes of display operation: (1) CHOP, used for reducing flicker while simultaneously viewing displays of two signals having slow repetition rates, (2) B Channel alone, (3) A Channel alone, (4) A + B, used for summing both channels or eliminating the common mode components from the two inputs (A - B) and (5) ALT, used for the apparent simultaneous display of two signals having fast rep-rates. When only one channel is selected, the switching multivibrator is forced to one stable state which produces a switching signal to the diode gating network for the desired signal. For ALTERNATE operation, the multivibrator is triggered by the CRT blanking pulse, causing the vertical signal to be selected alternately from Channel A or Channel B. During CHOP operation, however, the multivibrator is allowed to free run causing small segments of each channel to be displayed during each sweep. Due to the nature of CHOP operation, it is necessary to provide a blanking signal to turn off the beam during the transitions between Channel A and Channel B.

4-26. DETAILED THEORY OF OPERATION.

4-27. The following paragraphs discuss detailed theory of circuits as they appear in the main signal path. This instrument contains two identical Vertical channels and two identical Sync channels; therefore, only one of each typical circuit is discussed.

4-28. VERTICAL INPUT ATTENUATORS.

4-29. To insure maximum frequency response in the Vertical Amplifier, impedance matching between the source and input is necessary. The Vertical Amplifier is designed with a 50-ohm input impedance to facilitate direct observation of systems which have 50-ohm input/output impedances. Maximum range is maintained by switching the attenuator for inputs up to ±6.0V.

4-30. Three pi sections and one variable bridged T attenuator are used in various combinations to furnish desired attenuations. Figure 8-6 shows this switching arrangement. The bridged T attenuator is in series with the selected pi section combination, and provides the calibration adjustment (CAL-ADJ) necessary when changing the plug-in from one mainframe (Model 180-Series) to another. By the use of two ganged logarithmic tapered potentiometers (A1R12 and R13), it is possible to vary the attenuation for UNCAL operation, yet maintain a constant 50-ohm impedance match from input connector to Input Amplifier.

4-31. The bridged T attenuator keeps input/output impedance constant by causing R12 to increase in value while R13 decreases in value. Although the input/output impedance is constant, the variations in value of R12 and R13 change the overall attenuation of the input signal. To calibrate the Model 1802A, the CAL ADJ moves the detent of the Vernier, thereby making use of part of the range of the bridge T attenuator. It is necessary to readjust the CAL ADJ to compensate for differences in CRT deflection from one mainframe to another.

4-32. POLARITY SWITCH.

4-33. To provide the option of viewing positive or negative up, or to disconnect the signal from the Vertical Input Amplifier, a Polarity Switch is added in series with each channel's signal path. When "+" is selected, positive signals are displayed up, and when "-" is selected, negative signals are displayed up. In the OFF position the signal input from the attenuator and each side of the Input Amplifier is terminated with 50 ohms. This is to maintain a constant impedance match and, thereby, eliminate possible reflections due to mismatch.

4-34. VERTICAL INPUT AMPLIFIER.

4-35. Dual transistor A3Q1A/B receives the attenuated vertical input signal from the polarity network (see Figure 8-9). A dual transistor is used here because of its closely matched gain characteristics and close temperature tracking which insures minimum offset. Both A3Q1A and B are one-half of two Cas-

code Amplifiers; e.g., in conjunction with A3Q2A and B, each forms a Cascode Amplifier for the Sync B Channel and A4Q1A and B form the Vertical B Channel.

4-36. Although the vertical signal is traced through the vertical channels in the following paragraphs, the Cascode Amplifiers consisting of A3Q1A/B and A3Q2A/B are discussed here because they are identical. (Figure 8-9).

4-37. POWER MATCHING. Transistors A3Q1A and B are at the front end of both Sync and Vertical Amplifiers; therefore, and offset introduced at this point is amplified causing erroneous display. As previously mentioned, A3Q1A and A3Q1B have matched gain and are contained in a single case. Dual transistors tend to operate at approximately the same temperature; however, when connected in a differential configuration, one or the other usually conducts more, thus raising its power dissipation and causing thermal drift. To prevent this, power matching networks are added to the collector circuit of each transistor.

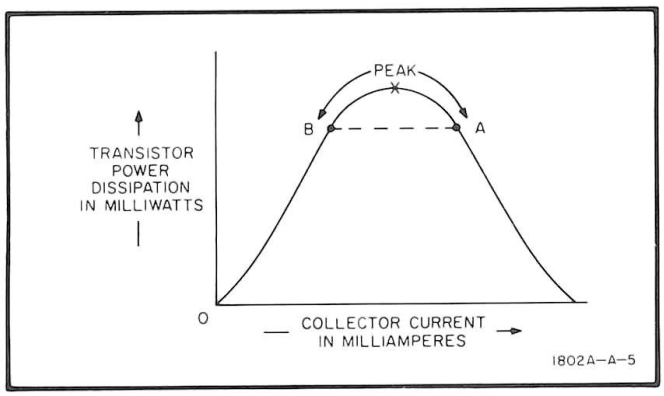


Figure 4-6. Transistor Power Curve

4-38. In order to obtain a power match between A3Q1A and Q1B, it is necessary to set up a condition where each transistor is operating at its power peak while in the quiescent state (see Figure 4-6). To accomplish this, resistors A3R15 and R16 and A3R11 and R12 are selected so that an increase or decrease in current through either A3Q1A and A3Q1B causes transistor power dissipation to decrease. For example, when current increases in Q1A its power dissipation moves forward and down the power curve, while simultaneously the decrease in current in Q1B causes its power dissipation to move backward and down the power curve. Since these power points essentially track each other in magnitude, transistors Q1A and Q1B always operate at equal powers, thus, minimizing thermal drift.

4-39. IMPEDANCE MATCHING. To maintain maximum response at high frequencies, the impedances at the common base stages of A3Q2A and B, and those of A4Q1A and B in the Vertical Channel, are carefully matched to provide 50 ohms of resistance in each leg of the 100-ohm line. Resistors A3R17/18 in series with the emitter/base resistance of A3Q2A and B furnish the right value in the Sync Channel, and resistors A4R3 and A4R4 in series with the emitters A4Q1A and B and accomplish it in the Vertical Channel (Figure 8-12).

4-40. GAIN DETERMINATION. The voltage gain of either Cascode Amplifier stage is approximately equal to the ratio of its collector and emitter resistances. For example, in the Cascode Amplifier consisting of A3Q3 and A3Q9A, the gain is set essentially by the ratio of A3R80 to one-half the value of A3R32. The resistors in series with the collector current of A3Q3 (R33 and R106) have virtually no effect on stage gain.

4-41. VERTICAL POSITIONING. Positioning of the Channel B signal is controlled by potentiometer R10 which is mounted on the front panel. This control simply introduces an offset bias current which in turn causes the VERTICAL OUTPUT and CRT trace to move up or down (see Figure 8-12). To insure that the POSITION control is centered with CRT trace centered, balance control A3R6 is used. To assure that the VERTICAL OUTPUT is at zero when the position and CRT trace are centered, sync balance adjust (A3R30), is used.

4-42. VERTICAL AMPLIFICATION. The amplified vertical signal is direct-coupled to the base of Differential Amplifier, A4Q2 and A4Q3, enroute to the delay line and vertical output stages. Voltage gain in this stage is kept low to prevent amplification of the Miller effect. As with the first Cascode Amplifier stage this too has emitter peaking (C7 and R16) to compensate for gain changes at high frequencies.

4-43. CHANNEL SWITCHING.

4-44. The vertical signal is amplified by a second cascode Differential Amplifier (A4Q4/A4Q11 and A4Q5/A4Q12) immediately following the Differential Amplifier stage just discussed (see Figure 8-12). This time, however, the second half (common base amplifier) is common to both Vertical Channels A and B. Since the input to a Common Base Amplifier is a low impedance, it is an ideal location to insert the channel switching diodes, A4CR1 through A4CR8.

4-45. Examine the connections of diodes A4CR1 through A4CR4. Notice that CR3 and CR4 are connected in series with the signal flow and will pass the vertical signal to A4Q11 and A4Q12. The bases of Q11 and Q12 are at approximately +5 volts due to VR1. The emitters of these transistors are near +5.7 volts; i.e., during operation the anodes of CR3 and CR4 are approximately +5.7 volts. When these diodes are conducting, they drop 0.7 volts causing their cathodes to assume about +5 volts. If Channel B switching input (90 wire) to the junction of CR1 and CR2 is at 0V, these diodes are reverse-biased, effectively removing them from the circuit. All vertical signals applied to Channel B are amplified and directed to the Output Amplifiers. However, when the switching input goes positive, CR1 and CR2 are forward biased, clamping the signal path to a positive voltage. Transistors Q4 and Q5 continue to conduct; but, due to the reverse-bias on CR3 and CR4, the signal path is open beyond this stage for Channel B. Switching is controlled so that when one channel is off the other will be on.

4-46. A + B OPERATION. It was previously mentioned that when CR1 and CR2 were forward-biased, Channel B signal path was opened. Due to the arrangement of the channel switching circuitry, Channel A would be on during this time. For A + B operation, however,

both Channels A and B are on simultaneously. In this instance, both channel signals are summed at the emitters of Q11 and Q12. To compensate for offset caused by the bias of both channels operating simultaneously, A + B BAL potentiometer R11 is used to compensate the bias on Q11 and Q12.

4-47. DELAY LINE.

4-48. The Delay Line is inserted in series with the vertical signal path to delay the vertical signal. The delay in the Vertical Channel is enough to allow the sweep to start before the signal arrives at the vertical deflection plates. Without this delay, it would be impossible to observe leading edge of single pulses or transitions.

4-49. The Delay Line used in the Model 1802A has an impedance of 180 ohms and delays the signal 160 nanoseconds. Impedance matching is important; therefore, resistors A4R62 and R63 are used to provide proper matching on the input side of the Delay Line. Resistors R13 and R14 provide matching at the output to insure impedance matching and minimum reflection.

4-50. VERTICAL OUTPUT. (CRT)

4-51. Subsequent Differential and Cascode Amplifier stages, similar to those already discussed, are used prior to the output transistors Q1 and Q2. Each of these stages provides gain, and each common emitter stage contains emitter peaking to compensate for high frequency roll-off. In addition, amplifier stage A4Q21 and Q22 is controlled by the BEAM FINDER connection at the junction of A4CR9/CR10. The BEAM FINDER lead normally supplies -12.6V to this junction. When the BEAM FINDER is depressed this point is disconnected, decreasing the gain and current in amplifier A4Q21/Q22. This restricts the CRT display regardless of input signal. Transistors A4Q23 and A4Q25 provide a voltage step up to attain the high DC level required at the base of Q1. Transistors A4Q24 and A2Q26 operate identical for Q2.

4-52. SYNC AMPLIFIER.

4-53. The Sync Amplifier contains circuits which are essentially the same as the Vertical Amplifier; therefore, only the differences are discussed (see Figure 8-9). A major difference is in the sync output stages. Each half of the differential sync signal is amplified and supplied to a separate output driver stage.

4-54. SYNC OUTPUT DRIVER. Transistor A3Q15 is an Emitter Follower which supplies a sync signal to the horizontal trigger generator via connector J6. Diode A3CR13 in the base bias circuit provides temperature compensation to minimize thermal drift. Emitter resistor A3R99 and inductor A3L4 maintain an impedance match to the cable in the horizontal plug-in. Collector resistor A3R101 minimizes the change in power dissipation for A3Q15, thereby helping to decrease thermal drift.

4-55. VERTICAL OUTPUT DRIVER. This output Driver works identical to the Horizontal Sync Output driver, except the VERTICAL OUTPUT is connected to front panel connector J5 through a variable attenuator and provides a signal for use with other related instruments. Peaking circuits in the sync amplifier insure good response to both the horizontal sync output and the VERTICAL OUTPUT. Good response is necessary in the sync amplifier to insure good results when the VERTICAL OUTPUT is cascaded with the Vertical Amplifier and for stable triggering.

4-56. CASCADE OPERATION.

4-57. When additional sensitivity is required, Channels A and B may be cascaded to use the gain available from both in series. Figure 3-8 gives the recommended cascade connection.

4-58. During normal operation, the signal levels dealt with at the inputs of Channel A and B Input Amplifiers are relatively small; however, when using the cascade mode, the amplifier signal applied to Channel B INPUT from the VERTICAL OUTPUT has been amplified by Channel A Sync Amplifier. Since Channel B Sync Amplifier is not used during this operation, its channel switching diodes are reverse-biased.

4-59. CHANNEL SWITCHING.

4-60. Channel Switching Assembly A5 (see Figure 8-18) performs two important functions: (1) it furnishes switching voltages to the Vertical and Sync Channel switching diodes, and (2) it produces a chopped blanking signal for use in the associated horizontal time base.

4-61. SWITCHING MULTIVIBRATOR. (Refer to Figure 8-18 for the following discussion.) Due to the various switching modes required in the Model 1802A Switching Multivibrator A5Q1/Q2 functions as a bistable multivibrator during ALT, A, and B operation and as an astable multivibrator during CHOP operation. For A + B operation, it acts as two separate saturated Common Emitter Amplifiers.

4-62. The various switching modes are initiated by DISPLAY switch S1 which controls the action of the multivibrator (A5Q1 and A5Q2). For example, in the position shown (ALT) switch S3-1F furnishes a negative operating voltage to the collector circuits of A5Q1 and A5Q2, switches S3-1R and S3-2R connect positive-bias to the base circuits of A5Q1 and A5Q2, and switch S3-2F provides ground to the trigger input circuitry. Under the above conditions, the multivibrator is ready to accept alternate trigger pulses via instrument connector P1 and cable W8.

4-63. As explained in the simplified circuit theory, each negative going trigger pulse causes the multivibrator to change state. Multivibrator outputs are amplified by Differential Amplifier A5Q3/Q4. The resulting output voltages at the emitters of A5Q5 and A5Q6 are used to control the channel switching diodes in the Vertical and Sync Amplifiers.

4-64. VERTICAL SWITCHING. The vertical channel switching diodes are connected directly to the switching voltages, therefore always providing switching as indicated on the DISPLAY switch.

4-65. SYNC SWITCHING. Switching voltages for the Sync Channel switching diodes are taken from the SYNC SOURCE switch (S4) and depend on the switch setting. Regardless of the mode selected by the DISPLAY

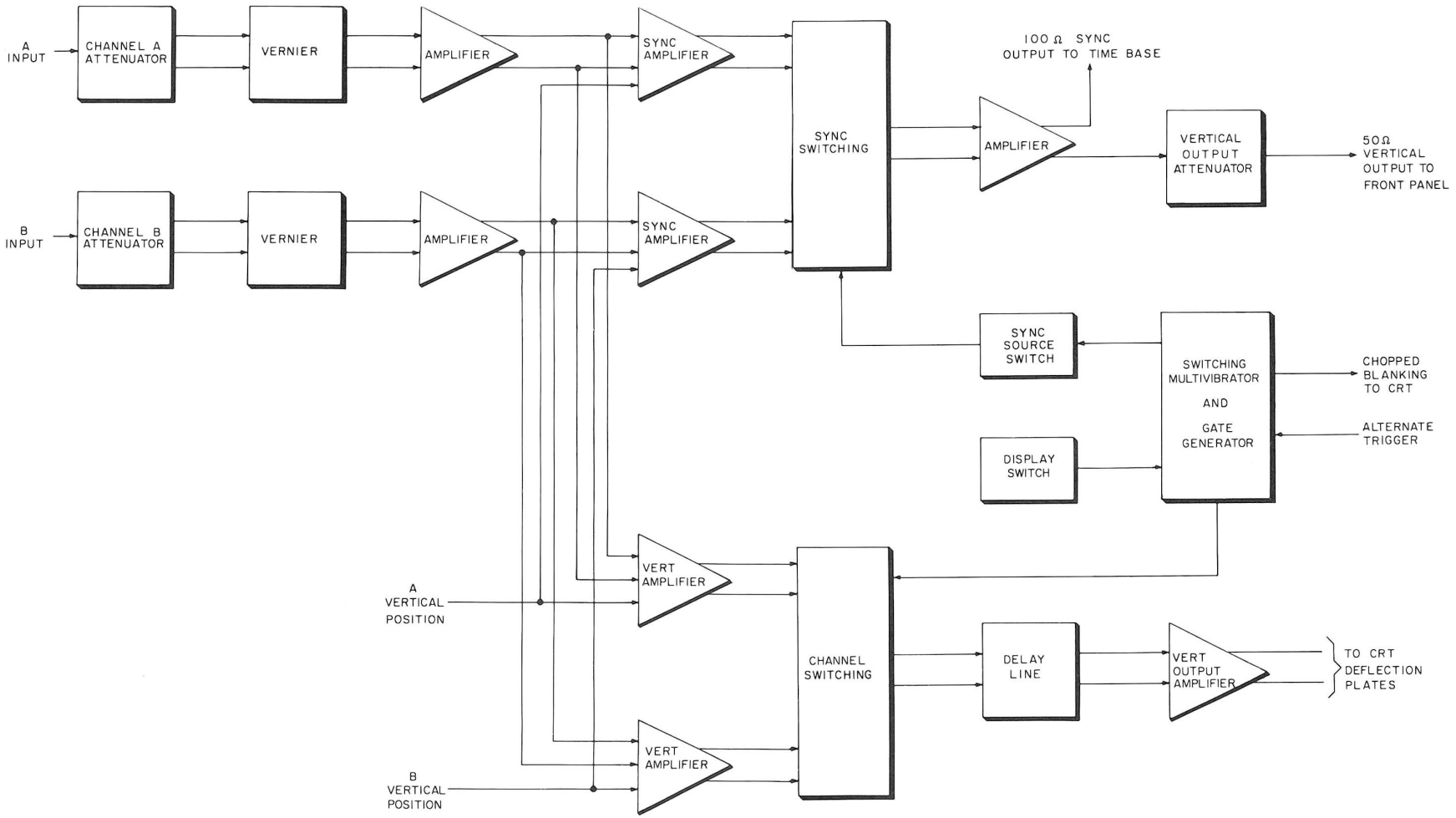
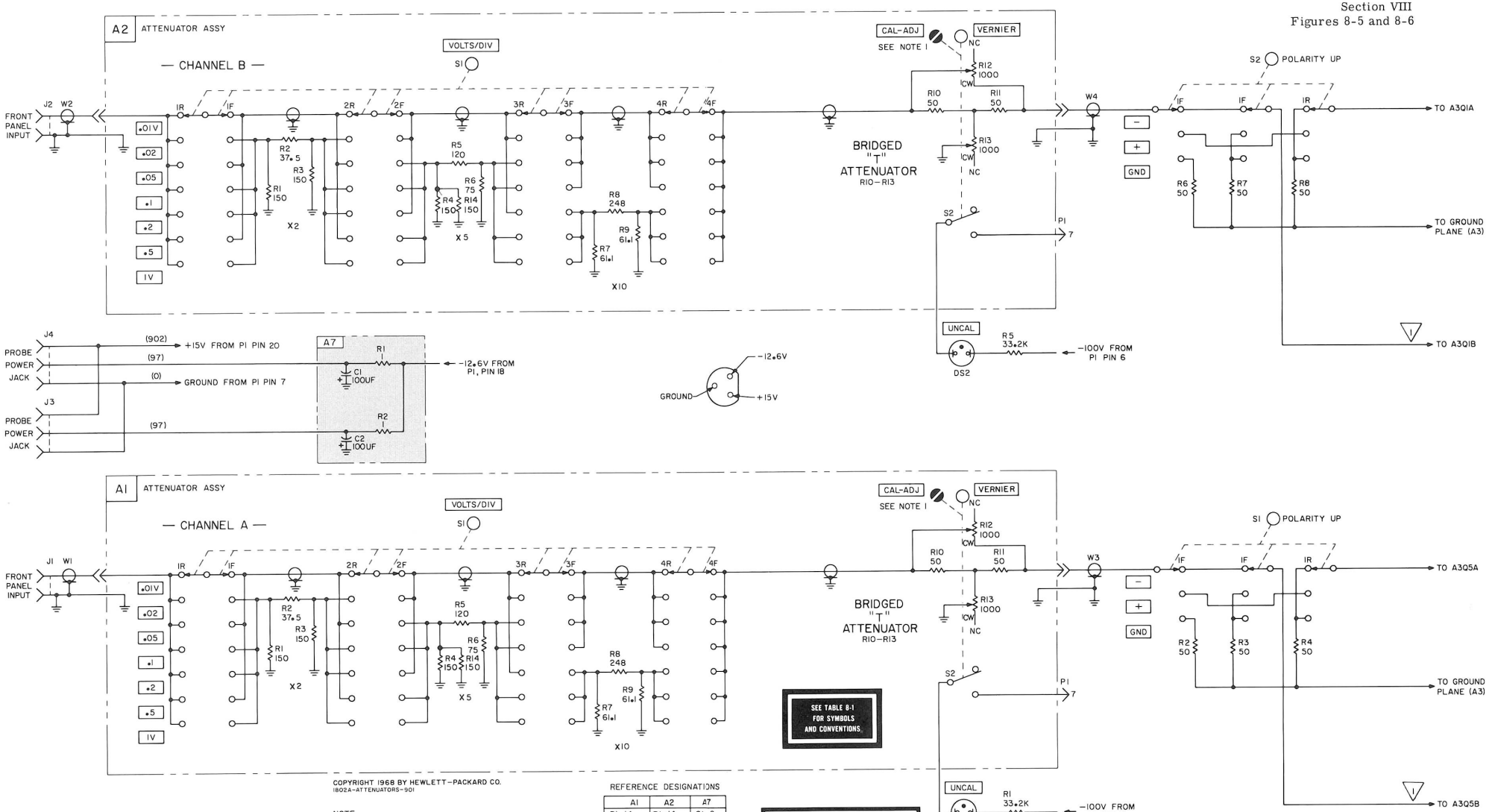


Figure 4-7. Overall Block Diagram



NOTE

1. CAL ADJUST IS A FINE VERNIER ADJUSTMENT WHICH MOVES THE DETENT, THUS CHANGING THE ATTENUATION FOR THE CALIBRATED POSITION OF THE CAL (VERNIER) CONTROL.

REFERENCE DESIGNATIONS

A1	A2	A7
R1-14 S1, 2	R1-14 S1, 2	C1, 2 R1, 2
CHASSIS		
DS1, 2 J1-4 R1-8	S1, 2 W1-4	

DELETED

Reference designations within assemblies are abbreviated. Add assembly designation as prefix to form complete designation (e.g., R1 on assembly A2 is A2R1).

Figure 8-6. Attenuator Assemblies Schematic Diagram

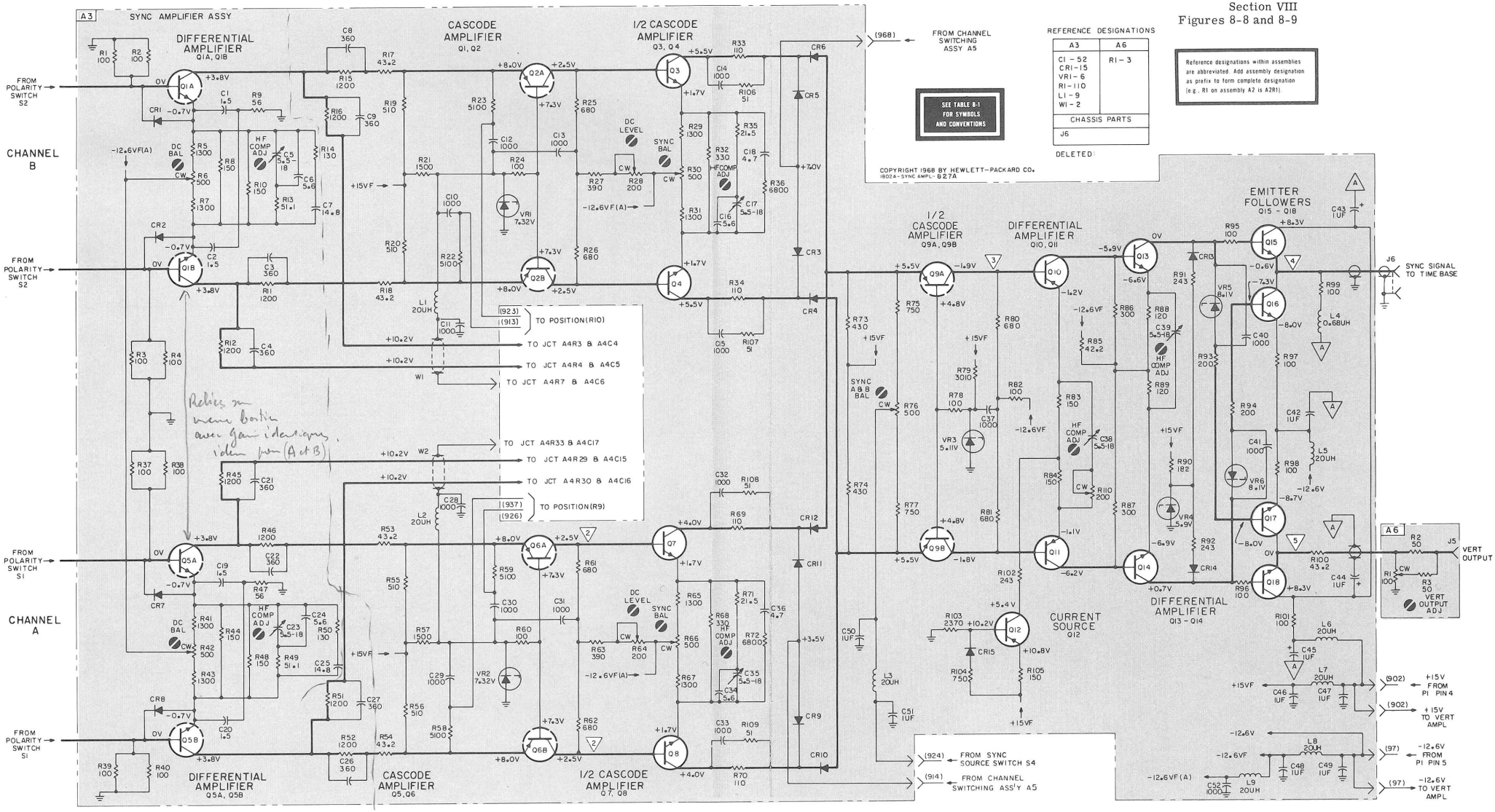


Figure 8-9. Sync Amplifier Schematic Diagram

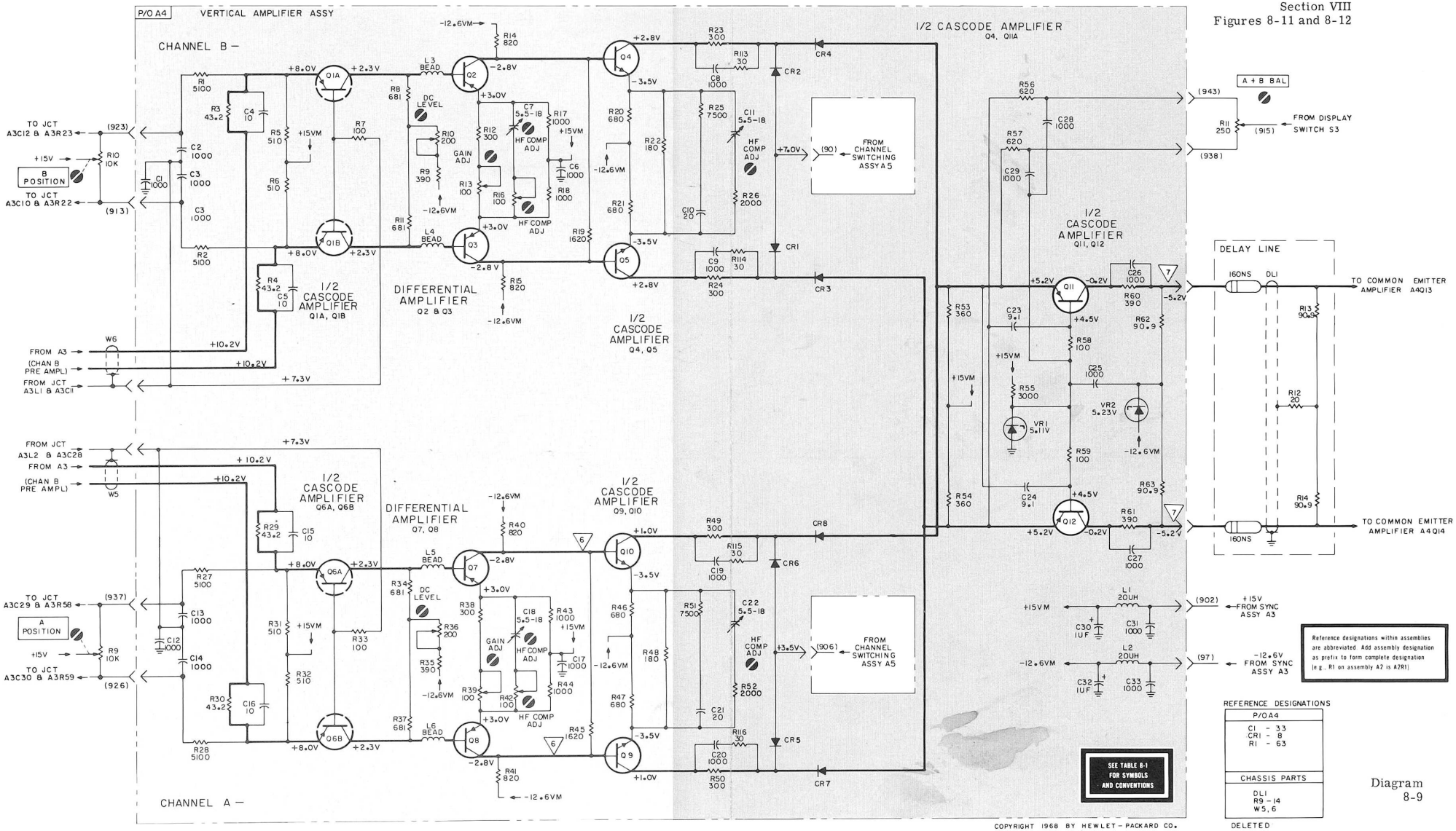


Figure 8-12. Vertical Amplifier Schematic

Diagram 8-9

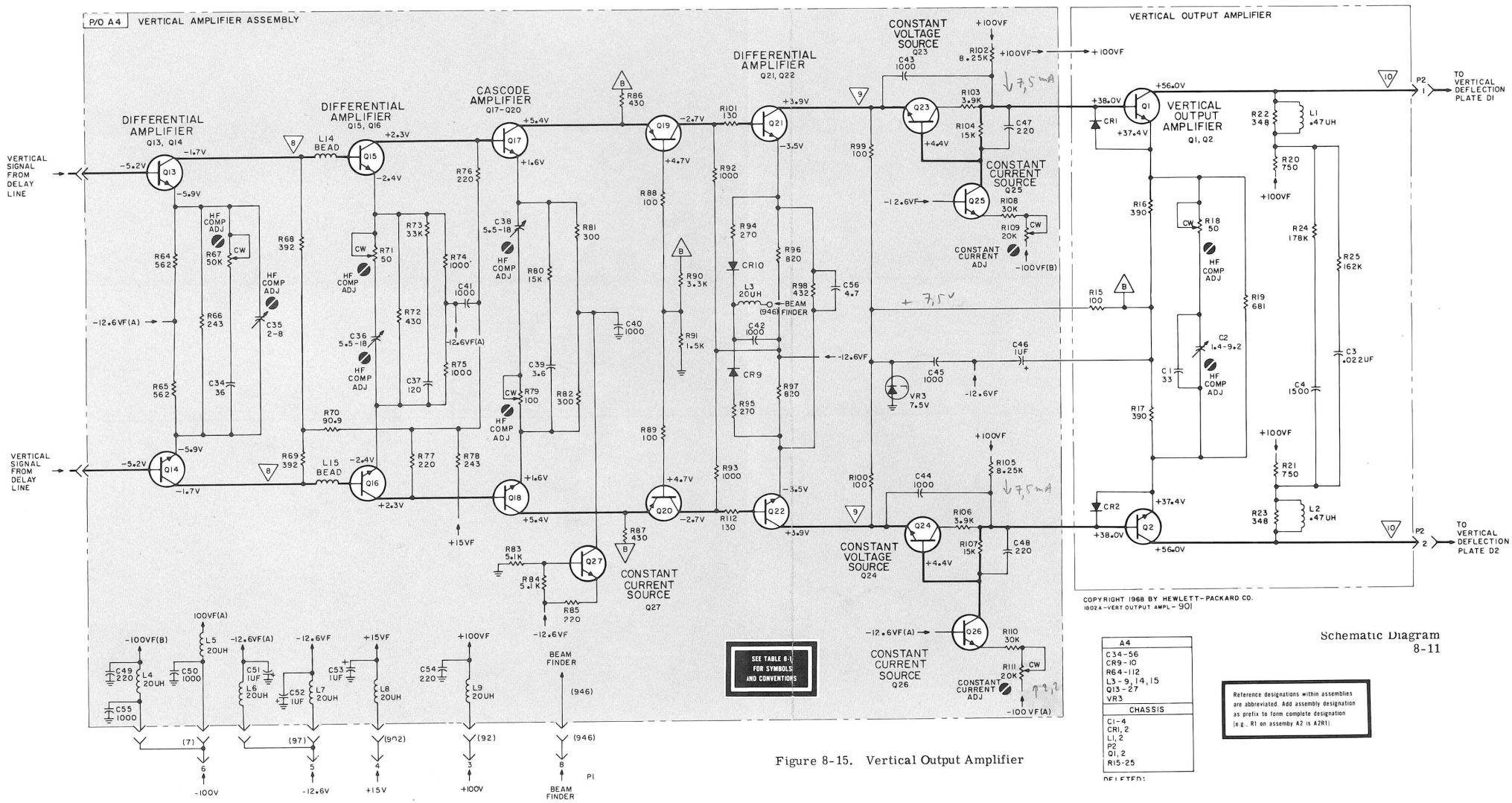


Figure 8-15. Vertical Output Amplifier

A4
C34-56
CR9-10
R64-112
L3-9, 14, 15
Q13-27
VR3
CHASSIS
C1-4
CR1, 2
L1, 2
P2
Q1, 2
R15-25
DELETED:

Reference designations within assemblies are abbreviated. Add assembly designation as prefix to form complete designation (e.g., R1 on assemby A2 is A2R1).

Schematic Diagram
8-11

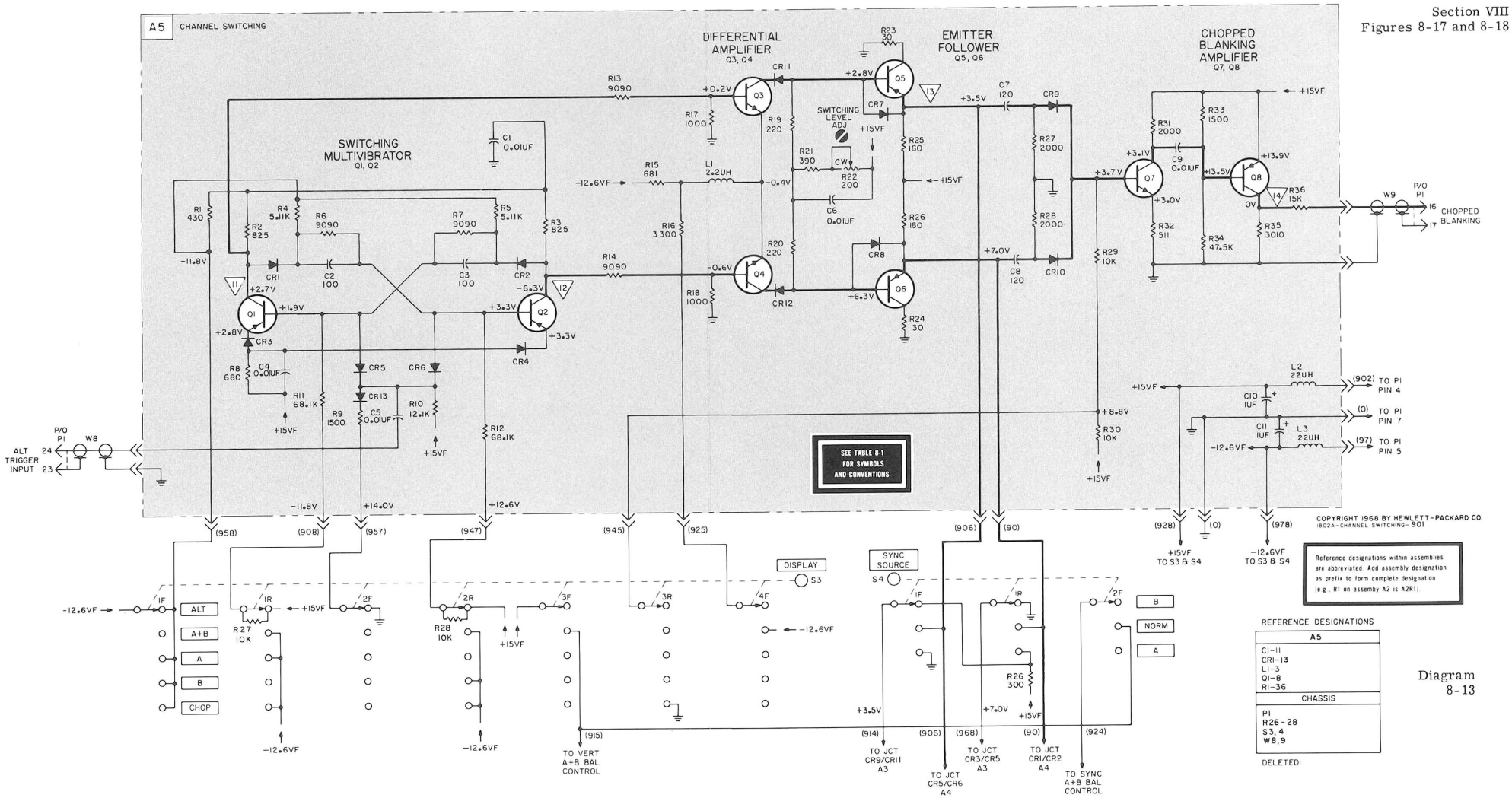


Figure 8-18. Channel Switching Schematic Diagram 8-13