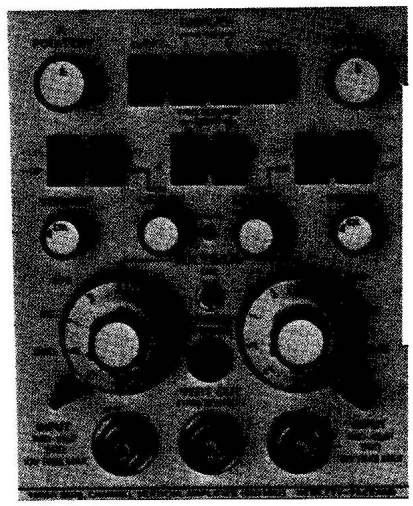
OPERATING AND SERVICE MANUAL

DUAL CHANNEL VERTICAL AMPLIFIER

1805A



HEWLETT hp PACKARD

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The Hewlett-Packard Model 1805A plug-in is a dual-channel vertical amplifier designed to operate with a horizontal time base in an HP 180-series oscilloscope mainframe. Each channel provides accurate measurements of high-frequency signals and fast rise time pulses with 5 mV/div vertical deflection capability over the full 100-MHz bandwidth. Selectable input impedance of either 50 ohms or 1 megohm permits impedance selection that best meets measurement applications. Its low shunt capacitance of approximately 13 pF reduces phase shift and signal loss in pulse or cw measurements. In addition, the dc offset capability of ±200 divisions allows low-level, biased logic pulses to be positioned on screen for accurate measurements.

1-3. This manual contains installation and operating instructions, as well as maintenance information for the 1805A. Instrument specification and procedures for verifying proper operation are included. Procedures are also included for adjusting the instrument to its performance specifications. Schematic diagrams, the theory of operation, and troubleshooting information are provided for use in maintaining the instrument.

1-4. This section of the manual contains the performance specifications for the 1805A, and a list of available options. It also lists the accessories that are available. Instrument and manual identification information are also included.

1-5. SPECIFICATIONS.

1-6. Table 1-1 is a complete list of the 1805A critical specifications that are controlled by tolerances. Any changes in specifications due to manufacturing, design, or traceability to the U.S. National Bureau of Standards will be listed on a manual change sheet included with this manual. The manual and manual change sheet supersede all previous information concerning specifications of the 1805A.

1-7. ACCESSORIES SUPPLIED.

1-8. The following accessories are supplied with the 1805A:

Two Voltage Divider Probes, HP Model 10014A

1-9. ACCESSORIES AVAILABLE.

1-10. The following accessories are available for the 1805A:

Model 10016A Voltage Divider Probes
Model 10020A Resistive Divider Probe Kit
Model 1120A 500 MHz Active Probe
Model 1125A Impedance Converter Probe

1-11. OPTIONS.

1-12. OPTION 003. This option provides the basic instrument without the two HP Model 10014A Voltage Divider Probes.

1-13. INSTRUMENT AND MANUAL IDENTIFICATION.

1-14. Instrument identification by serial number is located on the rear panel. Hewlett-Packard uses a two-section serial number consisting of a four-digit prefix and a five-digit suffix, separated by a letter designating the country in which the instrument was manufactured. (A=U.S.A.; G=West Germany; J=Japan; U=United Kingdom.)

1-15. This manual applies to instruments with a serial prefix number as shown on the title page. If changes have been made in the instrument since this manual was printed, a "Manual Changes" supplement supplied with the manual will define these changes. Be sure to record these changes in your manual. Backdating information in Section VII adapts the manual to instruments with serial numbers lower than that shown on the title page. Part numbers for the manual and the microfiche copy of the manual are also shown on the title page.

Table 1-1. Specifications

MODES OF OPERATION

Channel A; channel B; channels A and B displayed alternately on successive sweeps (ALT); channel A and B displayed by switching between channels at approx 400 kHz rate (CHOP) with blanking during switching; channel A plus channel B (algebraic addition).

EACH CHANNEL (2)

BANDWIDTH: (measured with or without 10014A probe, 3 dB down from 8 div reference signal from a terminated 50-ohm source.)

DC-coupled: dc to 100 MHz.

AC-coupled: approx 10 Hz to 100 MHz (lower limit is approx 1 Hz with 10014A probe).

RISE TIME: <3.5 ns (measured with or without 10014A probes, 10% to 90% points of 6 div input step from a terminated 50-ohm source).

DEFLECTION FACTOR

Ranges: 5 mV/div to 5 V/div (10 calibrated positions) in 1, 2, 5 sequence. ±2% attenuator accuracy.

Vernier: provides continuous adjustment between deflection factor settings and extends maximum deflection factor to at least 12.5 V/div. Front panel light indicates when vernier is not in CAL position.

POLARITY: + or — up, selectable.

SIGNAL DELAY: input signals are delayed sufficiently to view leading edge of input pulse without advanced trigger.

INPUT COUPLING: AC, DC, 50 ohms (dc), or ground. Ground position disconnects input connector and grounds amplifier input.

INPUT RC

AC and DC: 1 megohm ±1% shunted by approx 13 pF. Constant on all ranges.

50 ohm: 50 ohms ±2%. VSWR <1.2:1 at 100 MHz on all ranges.

MAXIMUM INPUT

AC and DC: ±300 V (dc + peak ac) at 1 kHz or less. ±150 V (dc + peak ac) on 5 mV/div range at 1 kHz or less.

50 ohm: 10 V rms.

DYNAMIC RANGE: 6 div at 100 MHz increasing to 16 div at ≤15 MHz.

POSITIONING RANGE: 16 div.

A+B OPERATION

Amplifier: bandwidth and deflection factors are unchanged; either channel may be inverted for ±A ±B operation.

Differential Input (A—B) Common Mode: CMRR is at least 40 dB from dc to 1 MHz for common mode signals of 16 div or less. CMRR is at least 20 dB at 50 MHz for common mode signals of 6 div or less.

TRIGGERING

SOURCE: selectable from channel A, channel B or a composite (Comp) signal from A and B in any display mode. Composite is channels A and B signals switched for Alt and Chop modes and added for A and B mode. Vernier and position controls do not affect A, B, or composite trigger signals. A and B signals are independent of polarity selection.

FREQUENCY

Time Base Plug-in	Trigger Frequency*	Required Vertical Deflection
1820C, 1824A	dc - 50 MHz	1/2 div
1825A, 1840A, 1841A	dc - 100 MHz	1 div
1820B, 1822A	dc - 50 MHz	1/2 div
	dc - 100 MHz	2 div
1820A, 1821A	dc - 50 MHz	1 div

*All display modes except Chop, dc to 100 kHz in Chop.

OFFSET

±200 div of offset. Allows offset of dc or ac signals up to the dynamic range and maximum input.

VERTICAL SIGNAL OUTPUT (selected by trigger source switch)

Bandwidth: >50 MHz into 50 ohms.

Amplitude: >50 mV for each division of display into 50 ohms with usable amplitudes up to 500 mV p-p.

Source Impedance: approx 50 ohms.

GENERAL

OPERATING ENVIRONMENT

Temperature: 0 to +55°C.

Humidity: to 95% relative humidity at +40°C.

Altitude: to 4600 m (15 000 ft).

Vibration: vibrated in three planes for 15 min. each with 0.254 mm (0.010 in.) excursion, 10 to 55 Hz.

WEIGHT: net, 2.3 kg (5 lb); shipping 3.6 kg (8 lb).

SECTION IV

PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains functional descriptions keyed to an overall troubleshooting block diagram located in Section VIII. Detailed circuit descriptions are keyed to schematics that are also located in Section VIII.

4-3. BLOCK DIAGRAM.

4-4. Because operation of both channels are identical, the following discussion of channel A is also applicable to channel B.

4-5. ATTENUATOR. The input signal is applied to the attenuator through the front-panel INPUT connector. The attenuator controls the type of input coupling (50Ω, DC, GND, AC) and it establishes the vertical deflection factor (5 mV/div to 5 V/div) as selected by the front-panel VOLTS/DIV control.

4-6. IMPEDANCE CONVERTER. The attenuator output is applied to differential impedance converter A6Q1A/Q1B. Field-effect transistor (FET) A6Q1A converts the single-ended, high-impedance input signal to a low-impedance, single-ended output. FET A6Q1B provides the dc-offset and channel-balance capabilities.

4-7. PREAMPLIFIER. Differential amplifier A6Q2/Q3 converts the single-ended input signal to a differential signal. This stage also provides a means for adjusting the gain of channel A to equal that of channel B which is fixed.

4-8. CHANNEL A CONTROL. The main amplifier consists primarily of control chip A6U1. This integrated circuit (IC) accepts a differential input and provides two differential outputs: (1) the main signal which after amplification, will be displayed on the CRT, and (2) the output that is applied to sync amplifier A6Q9-A6Q12. The IC also provides all functions necessary for the front-panel controls of the vertical system.

4-9. SYNC AMPLIFIER. Channel A and channel B sync signals are combined at the outputs of A6U1 and A6U2. The summed output is applied to sync amplifier A6Q9-Q12. The sync amplifier stage provides a gain of at least 10.

4-10. The sync amplifier output is separated into two signals. One signal is fed into a complementary emitter follower (A6Q13/Q14) that provides a low impedance source for the time base plug-in. The other signal is fed into emitter follower A6Q15/Q16 which is used to compensate for dc drift. The output of A6Q15/Q16 is also applied to the front-panel VERT OUT connector. Output impedance of A6Q15/Q16 is 50 ohms.

4-11. DELAY LINE. The output from channel control A6U1 is applied through delay line drivers A6Q7/Q8 to the delay line. This line delays the input signal for 160 nanoseconds to allow the sweep to trigger before the signal reaches the CRT deflection plates.

4-12. MAIN AMPLIFIER. Main amplifier A7 consists primarily of integrated circuit A7U1. The remainder of the circuit provides high-frequency and gain adjustments. Gain is adjusted by two variable resistors, R6 and A7R8. In addition, the main amplifier provides current gain for output amplifiers Q1/Q2 and Q3/Q4.

4-13. OUTPUT AMPLIFIER. Integrated circuit A7U1 provides two outputs. One drives output amplifier Q1/Q2 and the other drives output amplifier Q3/Q4. Each amplifier is compensated by a feedback signal that is adjustable by A8C1. Outputs from Q1/Q2 and Q3/Q4 are applied to the CRT vertical deflection plates.

4-14. CONTROL CIRCUIT. Control circuit A3 selects the type of display to be presented on the CRT: channel A, channel B, channels A and B, ALT, or CHOP.

4-15. Pulse shaper A3U1A receives the ALT TRIGGER signal from the oscilloscope mainframe. The ALT TRIGGER signal indicates that the gate pulse has ended. The output of A3U1A is applied to J-K flip-flop A3U2 which changes state after the completion of each sweep. The flip-flop action causes the trace on the CRT to alternate between channel A and channel B. In ALT mode of operation, chop oscillator A3U1B is disabled.

4-16. In CHOP mode, the chop oscillator is enabled and the pulse shaper is disabled, inhibiting the ALT TRIGGER signal from the oscilloscope mainframe. The chop oscillator switches the trace between channels at a 400-kHz rate. The oscillator also drives chop blanking circuit A3Q1/Q2. This circuit blanks the CRT during transition between channels.

4-17. The J-K flip-flop is connected to two current switches. A3Q3/Q4 is the on-off control for the main signal path. A3Q5 through A3Q8 is the on-off control for the sync signal path. The current switches control on-off circuits in A6U1 and A6U2.

4-18. Channel control current switch A3Q3/Q4 always follows the J-K flip-flop, but can be overridden by TRIG SOURCE pushbutton A or B.

4-19. POWER SUPPLY. The 1805A power supply operates on 115-Vac line from the oscilloscope mainframe. The power supply rectifies and filters the line voltage into +20 Vdc. The +20 Vdc is added to +15 Vdc from the mainframe to provide the +35 Vdc operating power.

4-20. Transformer T1 is connected to the mainframe transformer which provides proper operating voltage to the 1805A whether the oscilloscope is being operated from either 115 Vac or 230 Vac.

4-21. DETAILED CIRCUITRY.

4-22. The following paragraphs provide detailed explanations of individual circuits in the 1805A. Circuits that are identical for both channels are explained for channel A.

4-23. ATTENUATORS A10 and A11. (See schematic 1.) The 1805A employs a two-section, cam-actuated attenuator consisting of 17 in-line cams. The first three cams form coupling switch A10S1. The other 14 cams form VOLTS/DIV switch A10S2. These cams actuate pushrods which close spring-switch contacts A10A1S1 through A10A1S17 on thick-film substrate A10A1.

4-24. The first three cams form coupling switch A10S1 and actuate spring-switch contacts A10A1S1 through A10A1S3. A table located on schematic 1 explains the switch closure sequence for each of the front-panel coupling switch positions.

4-25. The last 14 cams form VOLTS/DIV switch A10S2 and actuate spring-switch contacts A10A1S4 through A10A1S17. A table on schematic 1 explains the switch closure sequence for each front-panel VOLTS/DIV setting.

4-26. The VOLTS/DIV switch is a compensated RC type attenuator consisting of two sections. Each section contains a group of attenuation networks. The first section contains X1, X10, and X100 networks. The second section has X1, X2, X4, and X10 networks. Each switch position cascades a network from the first section with a network from the second section. Different network combinations provide attenuation ranges from 5 mV/div to 5 V/div vertical deflection.

4-27. Each attenuator network has input capacitance adjustments. The straight-through range, .005 V/div, is not adjustable. The input capacitance for each range is matched to the input capacitance of the straight-through range to achieve a uniform input capacitance over the entire range of inputs. The other attenuator adjustments provide for high-frequency compensation.

4-28. PREAMPLIFIER. (See schematic 2.) Dual FET A6Q1 is an impedance converter that provides a high-input impedance to the attenuator and a low-output impedance to differential amplifier A6Q2/Q3.

4-29. The impedance converter has two inputs. One input is from attenuator A10 and is applied to the gate of A6Q1A. The other input is the sum of the voltages from the front-panel OFFSET control and the internal channel A balance control. The dual input provides a ±1-volt offset shift.

4-30. Differential amplifier A6Q2/Q3 converts the single-ended input signal from the impedance converter to a differential output. Resistors A6R23/R24 cross couple the input signal from A6Q2 to A6Q3. Capacitor A6C23 provides high-frequency compensation. Channel B has a fixed gain and channel A gain is adjusted by A6R35 to equal channel B gain.

4-31. Channel A control A6U1 is a medium scale IC that controls all vertical functions necessary for oscilloscope operation. The differential output from A6Q2/Q3 is fed into A6U1 where it is converted into two differential outputs. One is the main signal which, after amplification, is displayed on the CRT; the second output drives the sync amplifier.

4-32. Channel A and channel B signals are combined at the outputs of A6U1 and A6U2. The signal displayed on the CRT (channel A, channel B, or channels A+B) is determined by the IC's that are turned on.

4-33. The summed outputs of A6U1/U2 is the input to delay-line drivers A6Q7/Q8. A6Q7/Q8 is a differential amplifier that is temperature compensated. Temperature variations within the 1805A cause a resistance change in thermistor A6RT1. The resulting voltage change causes the capacitance in varactors A6C66 and A6C67 to change. The change in capacitance on emitters of A6Q7/Q8 maintains constant frequency response throughout the 100-MHz range of the 1805A.

4-34. Delay-line drivers A6Q7/Q8 also incorporate the oscilloscope find beam function. When the find beam pushbutton is pressed, —12.6 V is removed from the junction of A6R94/R95 (through A6R96). The resulting change in bias voltage reduces the amplifier gain sufficiently to return the vertical display to the viewing area of the CRT.

4-35. DELAY LINE. (See schematic 4.) The delay line provides 160 nanoseconds of delay to the input signal to allow sufficient time for the sweep circuit to trigger.

4-36. MAIN AMPLIFIER. (See schematic 4.) Main amplifier A7 contains an integrated circuit that provides the current gain for the entire system. The gain of A7U1 is adjusted by A7R8 and front-panel CAL

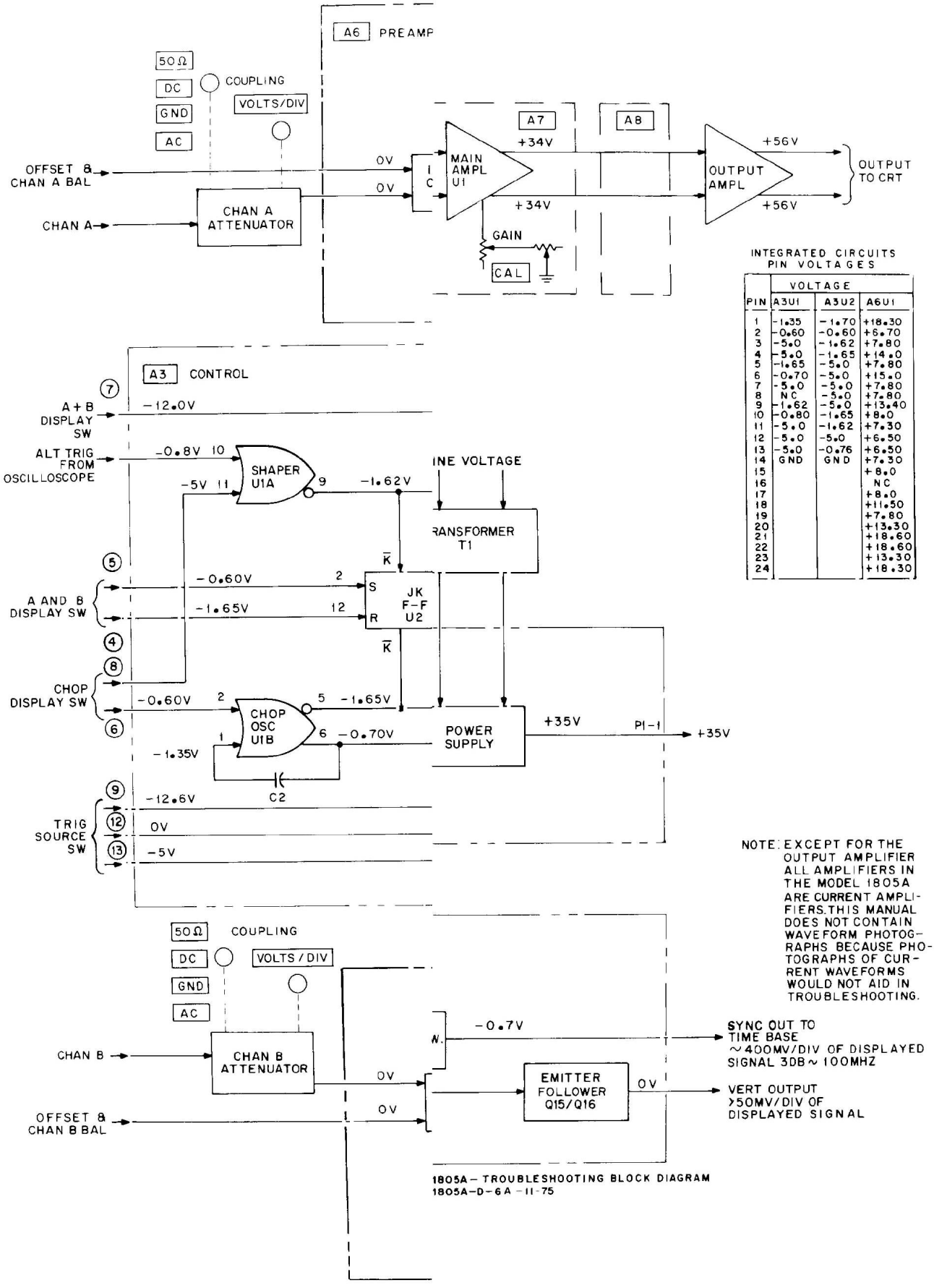
control, R6. These adjustments are used to calibrate the 1805A for different mainframes.

4-37. OUTPUT AMPLIFIER. (See schematic 4.) Signals from the main amplifier drive shunt-output amplifiers Q1/Q2 and Q3/Q4 which provide the voltage gain to drive the CRT. Each amplifier feeds a portion of its output back to its input through a compensation network. Amplifier Q3/Q4 has a high-frequency corner adjustment HF1. The vertical deflection signal from the output amplifier is applied to the CRT deflection plates in the oscilloscope mainframe.

4-38. SYNC AMPLIFIER. (See schematic 3.) The sync signals from channel A and channel B are combined at the output of channel control A6U1. The combined signal is applied to amplifier A6Q9-Q12.

4-39. The sync amplifier consists of series feedback pair A6Q9/Q10 followed by a shunt-feedback pair A6Q11/Q12. Feedback amplifier A6Q11/Q12 is the last gain stage for the internal trigger signal.

4-40. The amplified signal is applied to two paths. One path is by way of complementary emitter followers A6Q13/Q14 to J2. At J2 there will be 400 mV/div of displayed signal (3 dB down at 100 MHz). The after path provides 50-mV/div of display signal to the front-panel vertical output connector by way of emitter follower A6Q15.



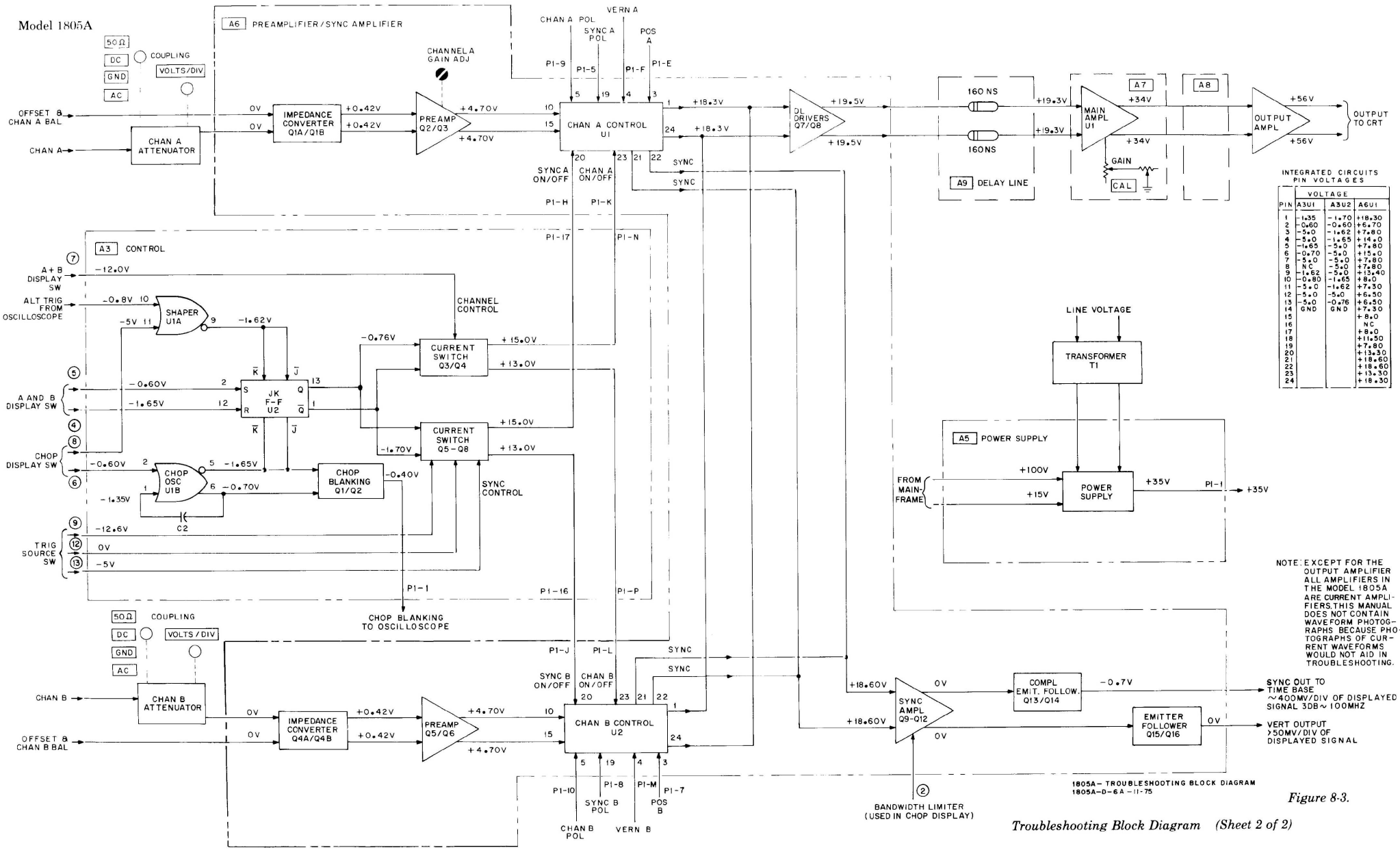
INTEGRATED CIRCUITS PIN VOLTAGES

PIN	VOLTAGE A3U1	A3U2	A6U1
1	-1.35	-1.70	+18.30
2	-0.60	-0.60	+6.70
3	-5.0	-1.62	+7.80
4	-5.0	-1.65	+14.0
5	-1.65	-5.0	+7.80
6	-0.70	-5.0	+15.0
7	-5.0	-5.0	+7.80
8	NC	-5.0	+7.80
9	-1.62	-5.0	+13.40
10	-0.80	-1.65	+8.0
11	-5.0	-1.62	+7.30
12	-5.0	-5.0	+6.50
13	-5.0	-0.76	+6.50
14	GND	GND	+7.30
15			+8.0
16			NC
17			+8.0
18			+11.50
19			+7.80
20			+13.30
21			+18.60
22			+18.60
23			+13.30
24			+18.30

NOTE: EXCEPT FOR THE OUTPUT AMPLIFIER ALL AMPLIFIERS IN THE MODEL 1805A ARE CURRENT AMPLIFIERS. THIS MANUAL DOES NOT CONTAIN WAVEFORM PHOTOGRAPHS BECAUSE PHOTOGRAPHS OF CURRENT WAVEFORMS WOULD NOT AID IN TROUBLESHOOTING.

1805A-TROUBLESHOOTING BLOCK DIAGRAM
1805A-D-6A-11-75

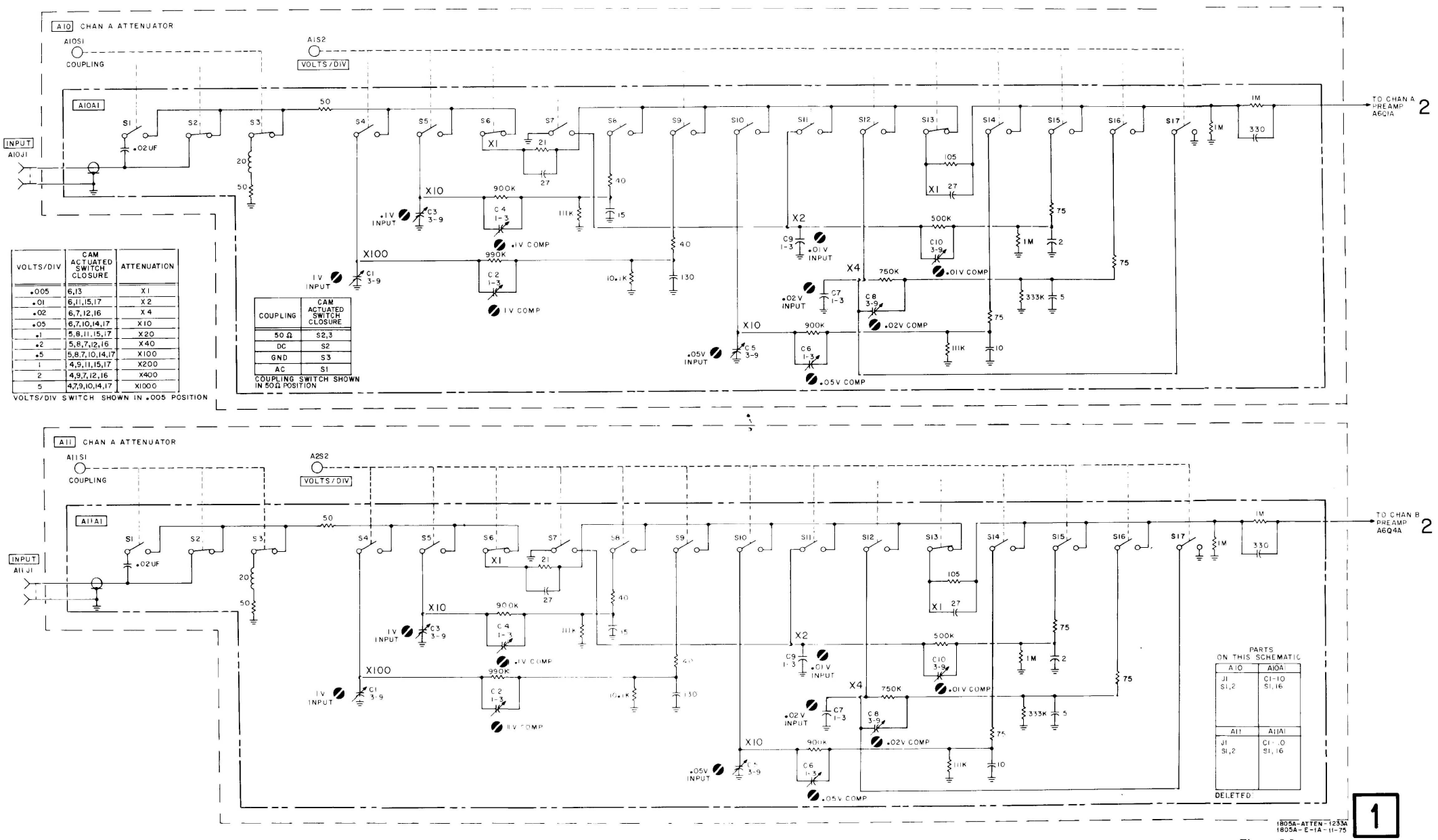
Troubleshooting Block Diagram



PIN	VOLTAGE A3U1	VOLTAGE A3U2	VOLTAGE A6U1
1	-1.35	-1.70	+18.30
2	-0.60	-0.60	+6.70
3	-5.0	-1.62	+7.80
4	-5.0	-1.65	+14.0
5	-1.65	-5.0	+7.80
6	-0.70	-5.0	+15.0
7	-5.0	-5.0	+7.80
8	NC	-5.0	+7.80
9	-1.62	-5.0	+13.40
10	-0.80	-1.65	+8.0
11	-5.0	-1.62	+7.30
12	-5.0	-5.0	+6.50
13	-5.0	-0.76	+6.50
14	GND	GND	+7.30
15			+8.0
16			NC
17			+8.0
18			+11.50
19			+7.80
20			+13.30
21			+18.60
22			+18.60
23			+13.30
24			+18.30

Figure 8-3.

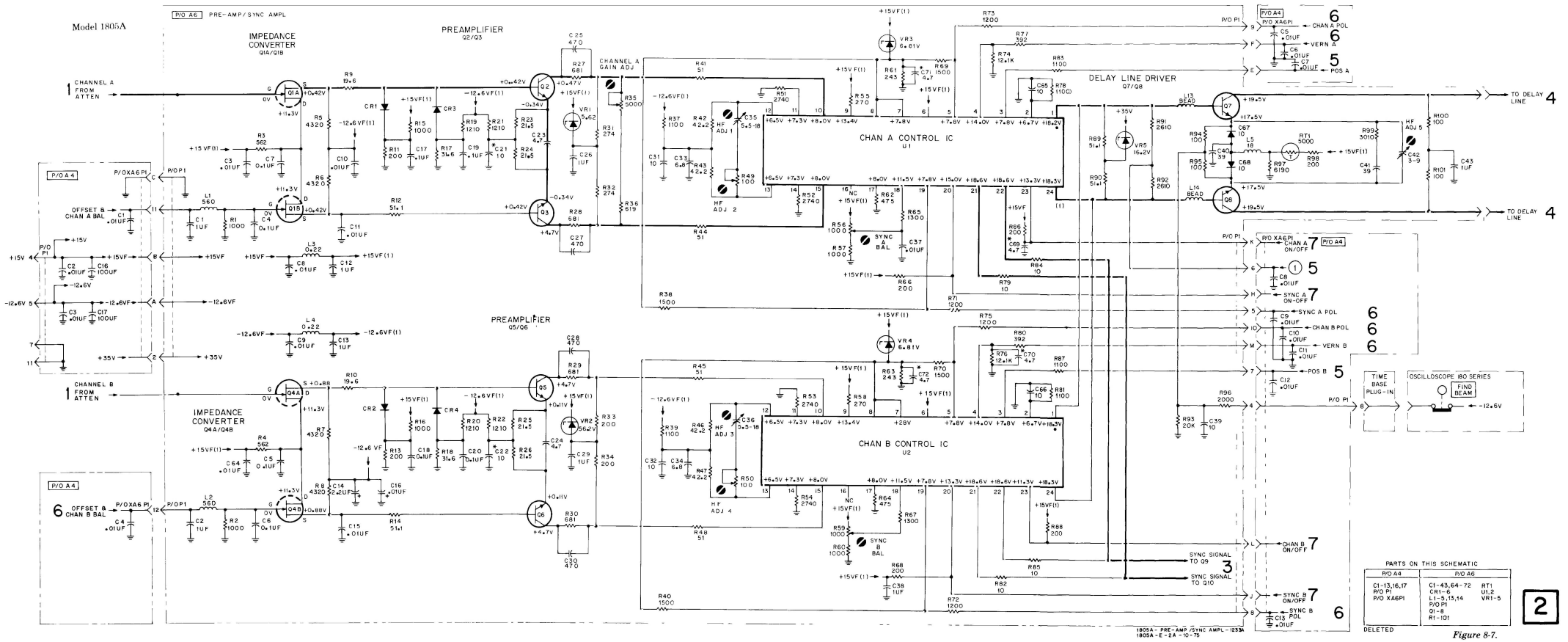
Troubleshooting Block Diagram (Sheet 2 of 2)



Attenuator Schematic

Figure 8-5.

Model 1805A



PARTS ON THIS SCHEMATIC

P/O A4	P/O A6
C1-13,16,17	C1-43,64-72
P/O P1	CR1-6
P/O XA6P1	L1-5,13,14
	P/O P1
	Q1-8
	R1-101
	RT1
	U1,2
	VR1-5

DELETED

Figure 8-7. Preamplifier and Sync Amplifier Schematic

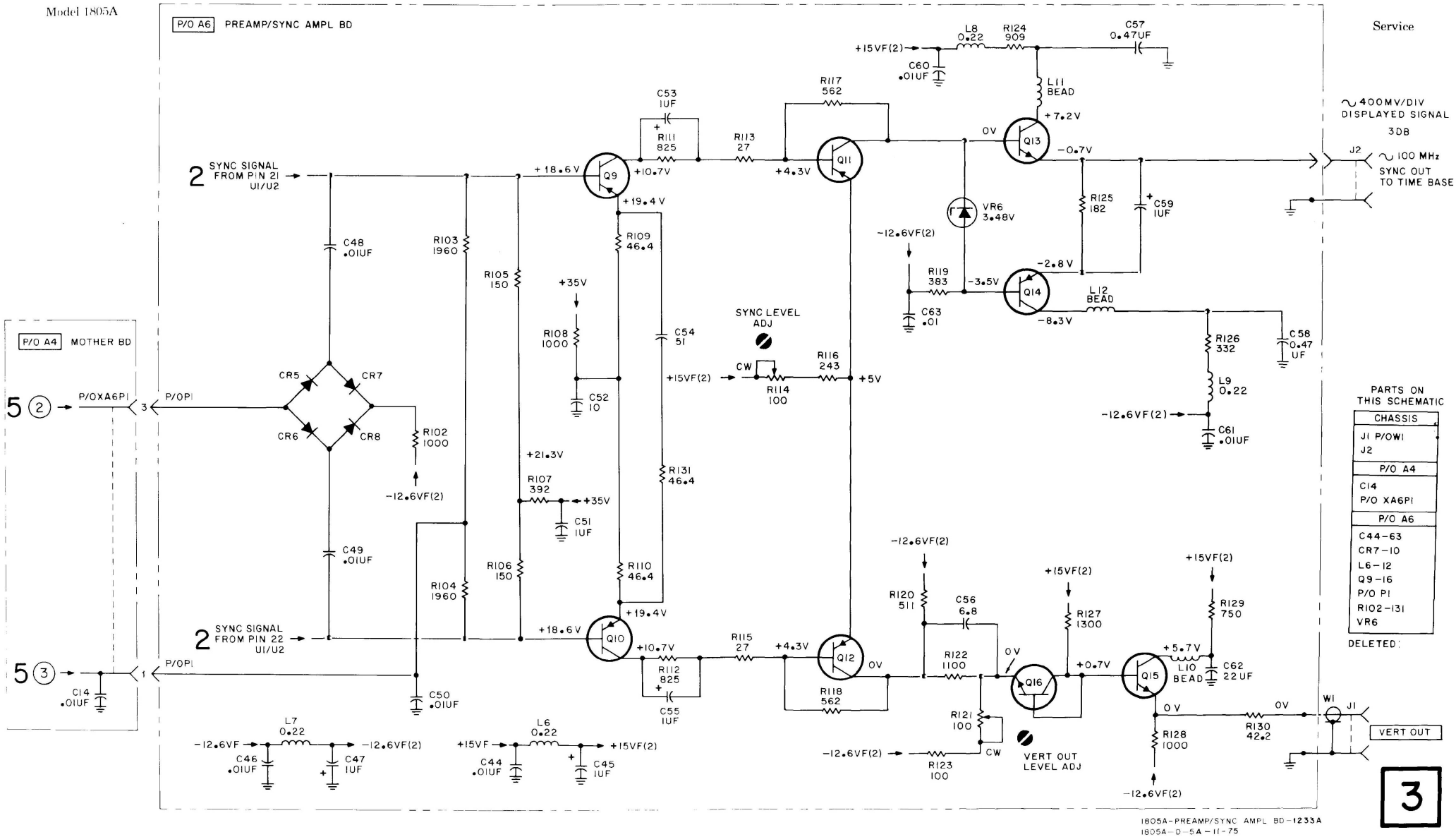
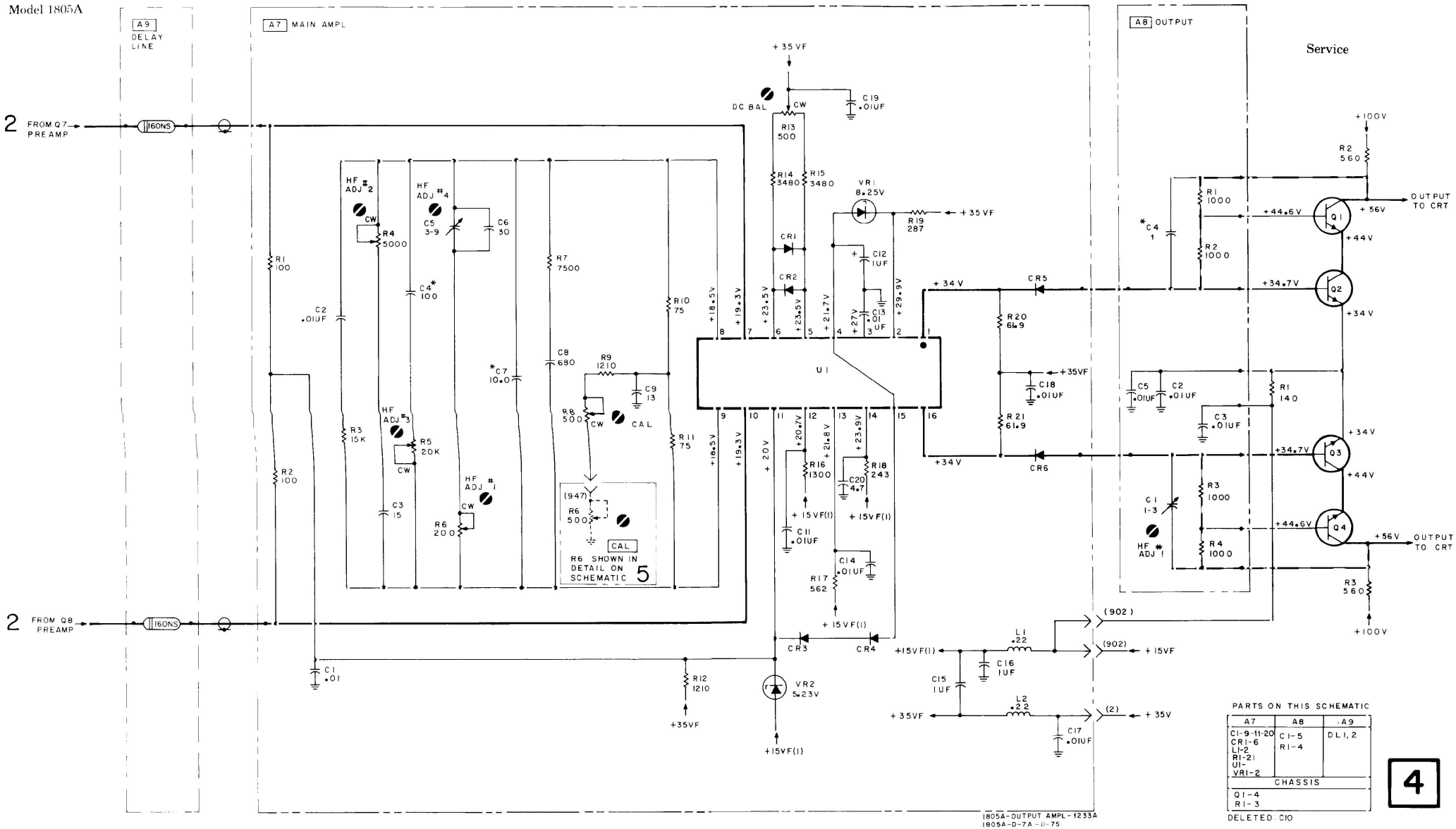

P/O A6 PREAMP/SYNC AMPL BD
P/O A4 MOTHER BD
2 SYNC SIGNAL FROM PIN 21 U1/U2
2 SYNC SIGNAL FROM PIN 22 U1/U2
5 2
5 3
P/OXA6P1
P/OP1
+15VF(2)
L8 0.22
R124 909
C57 0.47UF
C60 .01UF
L11 BEAD
+7.2V
0V
Q13
-0.7V
J2
400MV/DIV DISPLAYED SIGNAL
3DB
100 MHz SYNC OUT TO TIME BASE
C53 1UF
R111 825
R117 562
R113 27
Q9
Q11
+18.6V
+10.7V
+4.3V
+19.4V
VR6 3.48V
R125 182
C59 1UF
-12.6VF(2)
R119 383
C63 .01
Q14
-2.8V
-3.5V
-8.3V
L12 BEAD
R126 332
C58 0.47 UF
L9 0.22
C61 .01UF
C48 .01UF
R103 1960
R105 150
+35V
R108 1000
C52 10
R109 46.4
C54 51
SYNC LEVEL ADJ
CW
R114 100
R116 243
+5V
+15VF(2)
R131 46.4
+21.3V
R107 392
C51 1UF
R106 150
R110 46.4
R104 1960
C49 .01UF
C50 .01UF
CR5
CR6
CR7
CR8
R102 1000
-12.6VF(2)
C14 .01UF
P/OP1
L7 0.22
C46 .01UF
C47 1UF
L6 0.22
C44 .01UF
C45 1UF
Q10
Q12
R112 825
C55 1UF
R115 27
R118 562
R120 511
C56 6.8
R122 1100
R121 100
R123 100
VERT OUT LEVEL ADJ
Q16
R127 1300
+0.7V
Q15
R129 750
+5.7V
L10 BEAD
C62 22 UF
R128 1000
R130 42.2
W1
J1
VERT OUT
PARTS ON THIS SCHEMATIC
CHASSIS
J1 P/OW1
J2
P/O A4
C14
P/O XA6P1
P/O A6
C44-63
CR7-10
L6-12
Q9-16
P/O P1
R102-131
VR6
DELETED:
1805A-PREAMP/SYNC AMPL BD-1233A
1805A-D-5A-11-75
3

Figure 8-9.



PARTS ON THIS SCHEMATIC

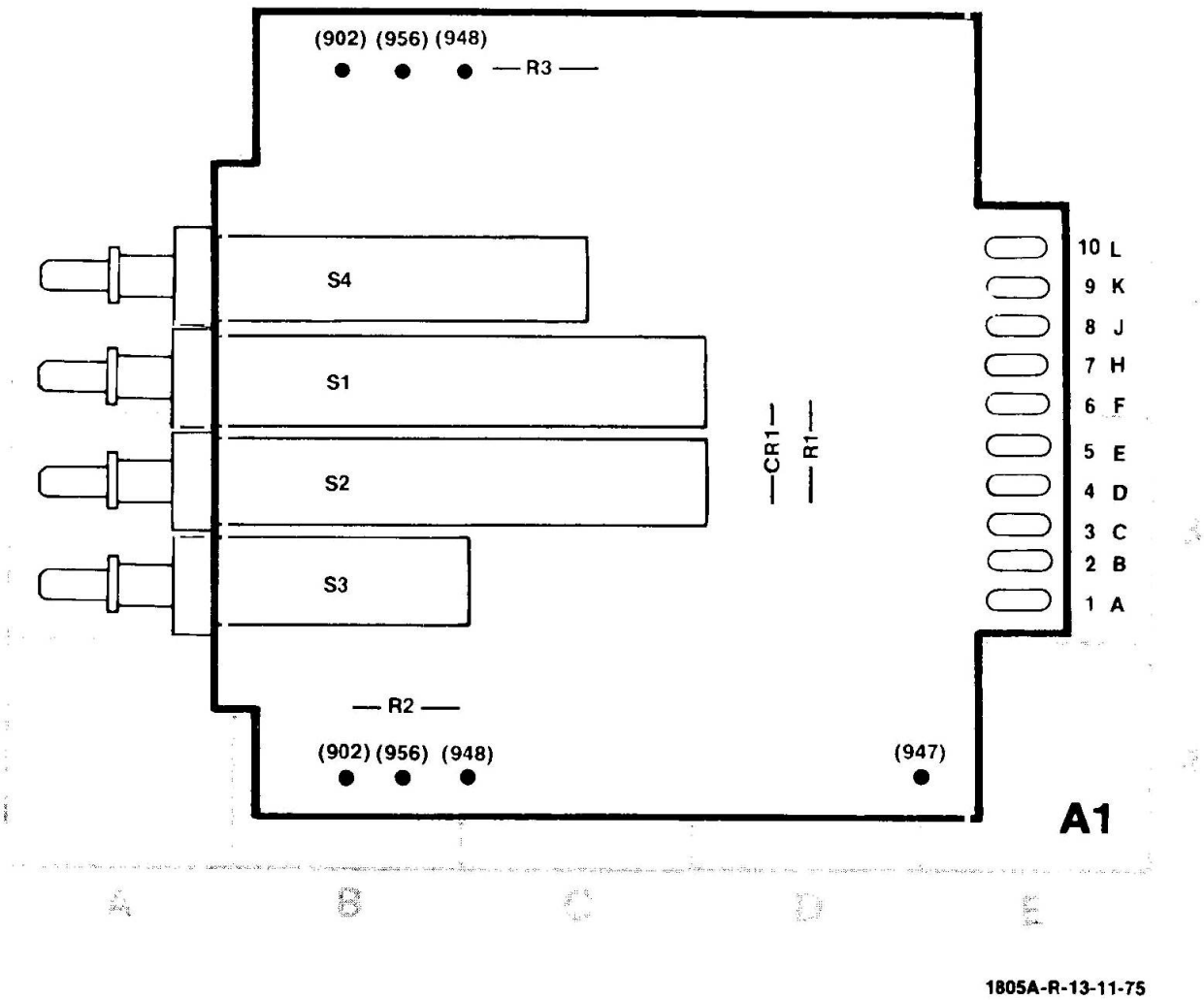
A7	A8	A9
C1-9-11-20 CR1-6 L1-2 R1-21 U1 VR1-2	C1-5 R1-4	D L 1, 2
CHASSIS		
Q1-4 R1-3		

DELETED: C10

4

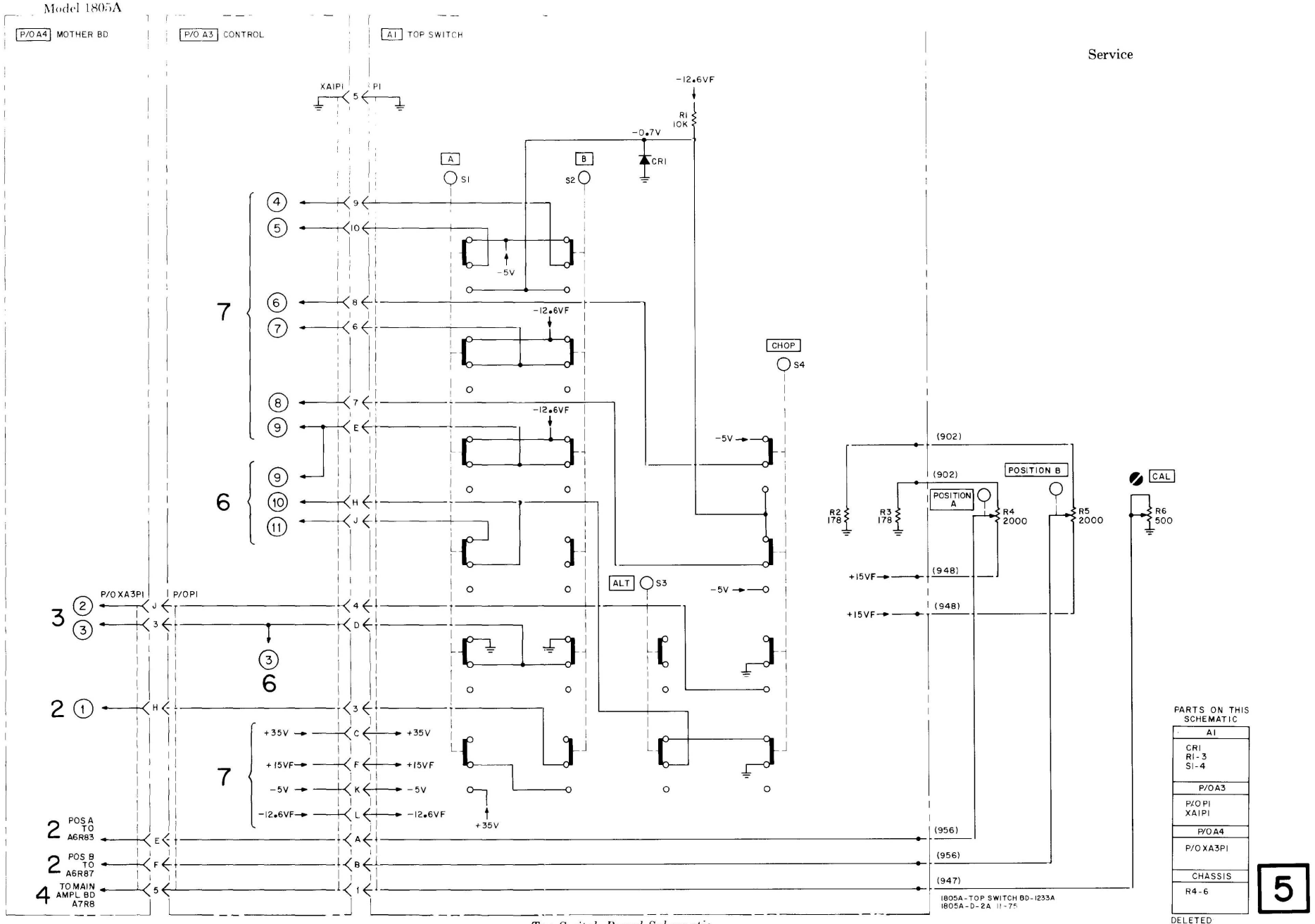
Output Amplifier Schematic

Figure 8-12.



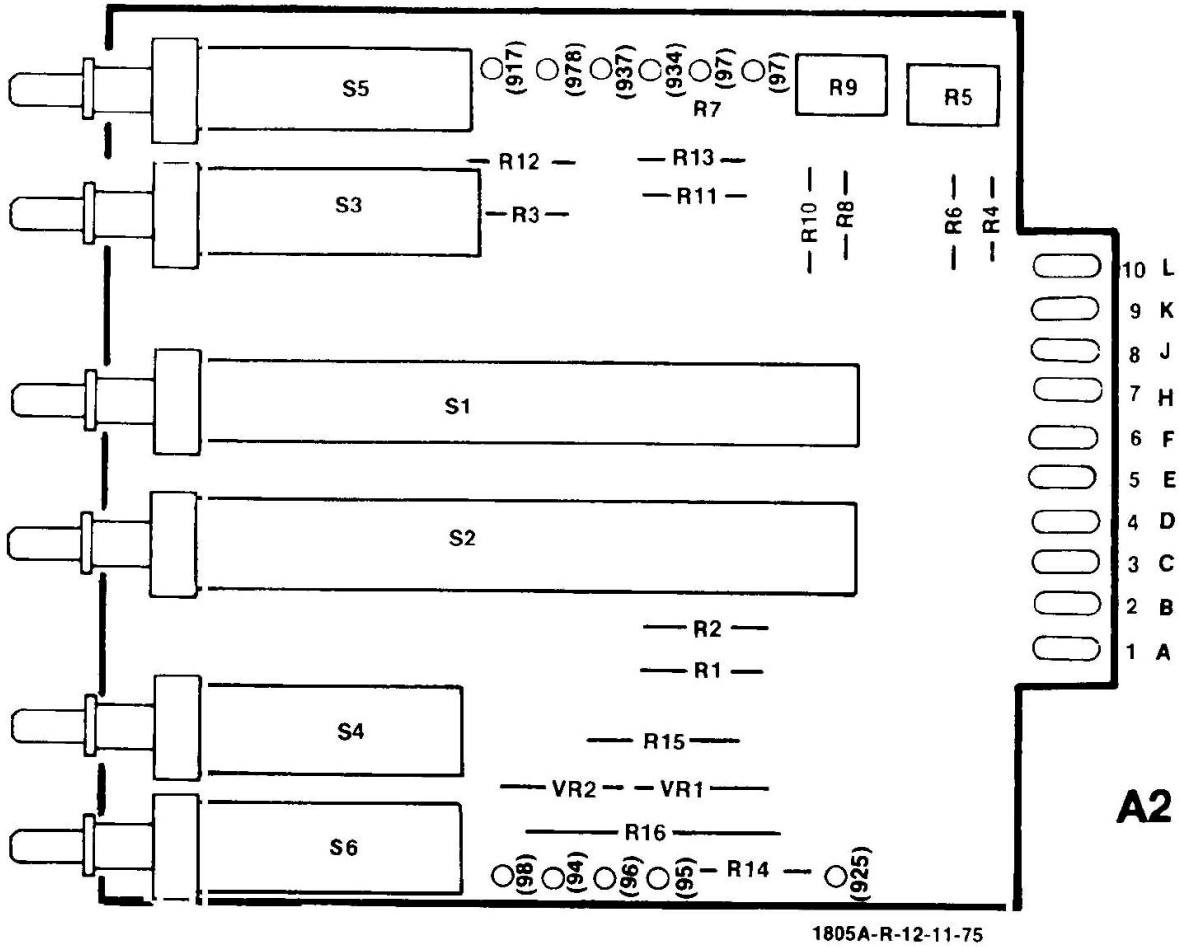
REF DESIG	GRID LOC	REF DESIG	GRID LOC
CR1	D-3	S1	B-2
R1	D-3	S2	B-3
R2	B-4	S3	B-3
R3	C-1	S4	B-2

Figure 8-13. Top Switch Board A1, Component Identification



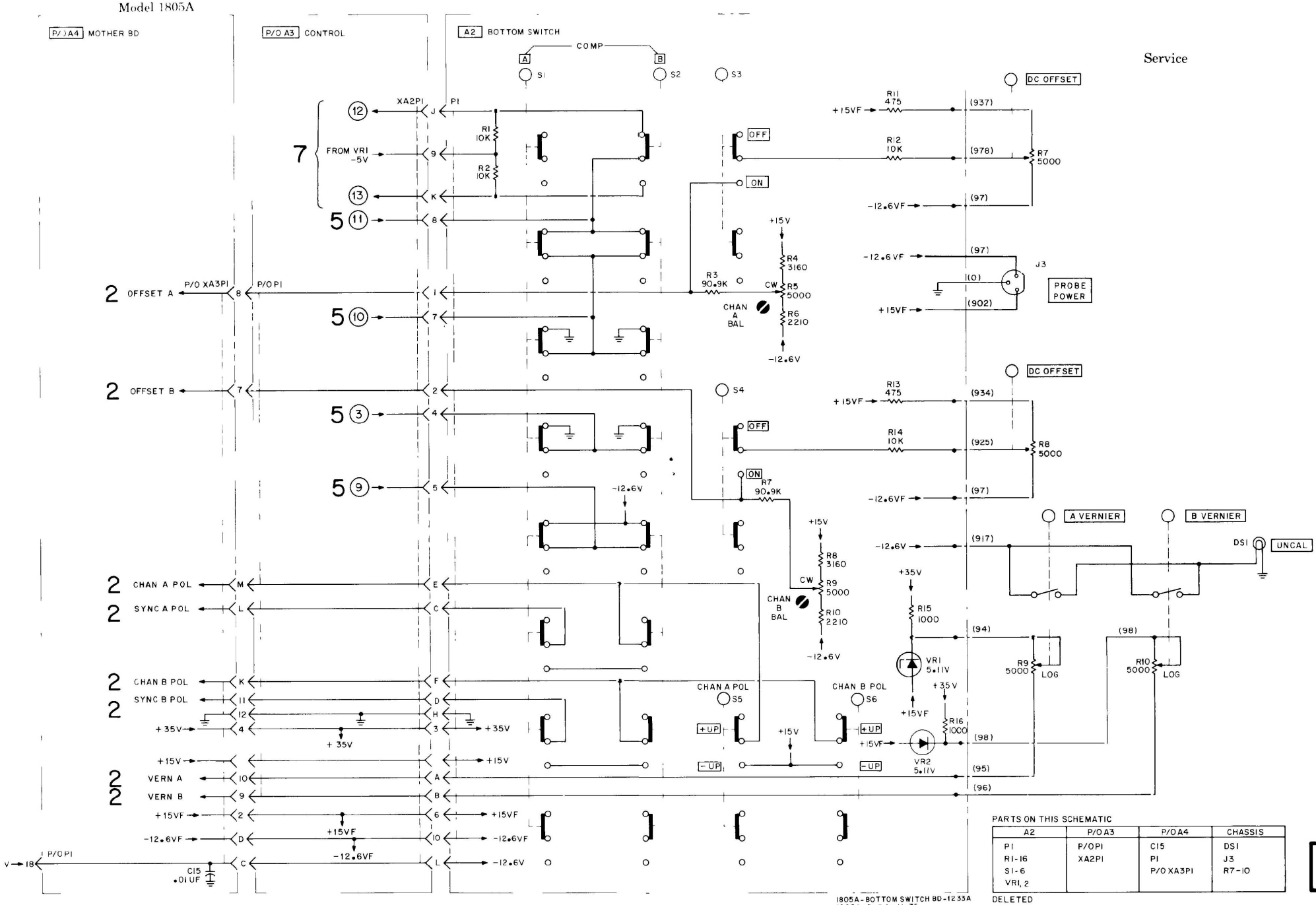
Top Switch Board Schematic

Figure 8-14.



REF DESIG	GRID LOC	REF DESIG	GRID LOC
R1	D-3	R13	D-1
R2	D-3	R14	D-4
R3	C-1	R15	D-4
R4	E-1	R16	D-4
R5	E-1	S1	C-2
R6	E-1	S2	C-3
R7	D-1	S3	C-1
R8	E-1	S4	C-4
R9	E-1	S5	C-1
R10	E-1	S6	C-4
R11	D-1	VR1	D-4
R12	C-1	CR2	D-4

Figure 8-15. Bottom Switch Board A2, Component Identification



PARTS ON THIS SCHEMATIC

A2	P/O A3	P/O A4	CHASSIS
P1	P/O P1	C15	DS1
R1-16	XA2P1	P1	J3
S1-6		P/O XA3P1	R7-10
VR1, 2			

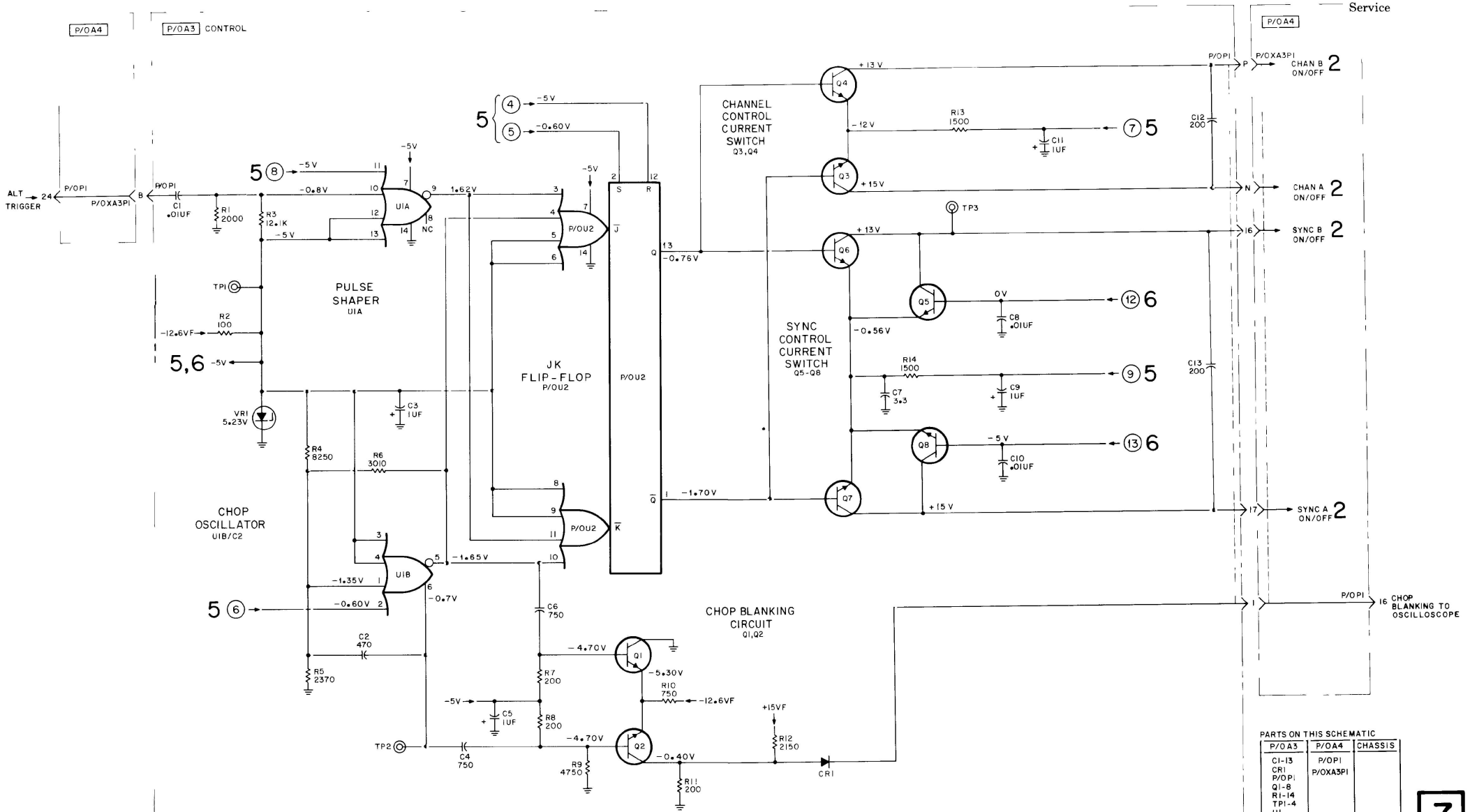
DELETED

1805A-BOTTOM SWITCH BD-1233A
1805A-D-3A-11-75

6

Figure 8-16.

Bottom Switch Board Schematic

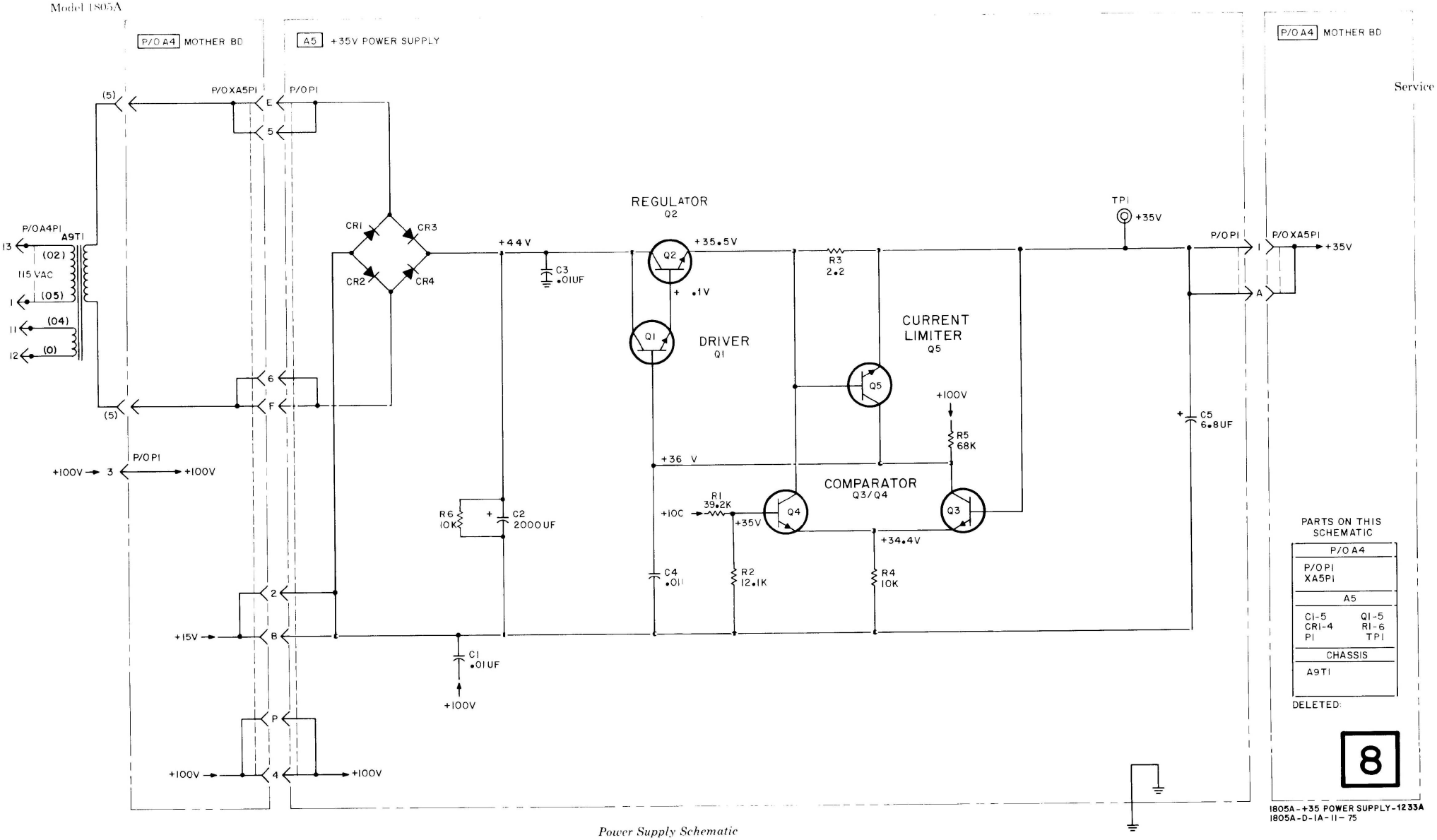


PARTS ON THIS SCHEMATIC		
P/OA3	P/OA4	CHASSIS
C1-13 CR1 P/OP1 Q1-8 R1-14 TP1-4 U1 P/OU2 VR1	P/OPI P/OXA3PI	
DELETED:		

1805A-CONTROL BD-1233A
1805A-D-4A-11-75

Control Board Schematic

7



Power Supply Schematic