



## OPERATING AND SERVICE MANUAL

# MODEL 1840A TIME BASE

SERIALS PREFIXED: 963—

Refer to Section VII for instruments with other Serial Prefixes.

HEWLETT-PACKARD COMPANY/COLORADO SPRINGS DIVISION  
1900 GARDEN OF THE GODS ROAD, COLORADO SPRINGS, COLORADO, U.S.A.

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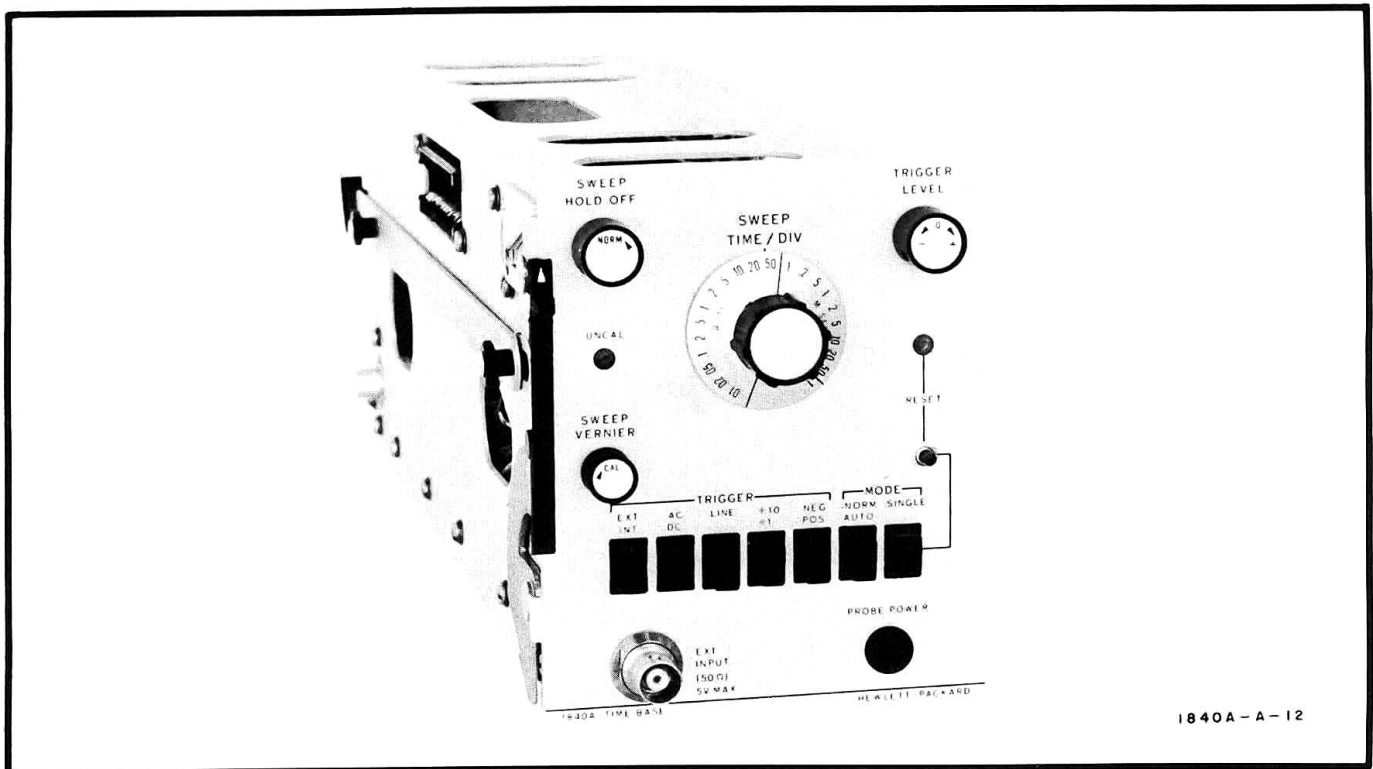


Figure 1-1. Model 1840A Time Base

Table 1-1. Model 1840A Specifications

**SWEEP**

**RANGES:** from 10 ns/div to 0.1 sec/div in 1, 2, 5 sequence;  $\pm 3\%$  accuracy with vernier in calibrated position. Mainframe magnifier extends fastest speed to 1 ns/div with  $\pm 5\%$  accuracy.

**VERNIER:** continuously variable between all ranges, extends slowest sweep to at least 0.25 sec/div.

**TRIGGERING****NORMAL:**

Internal: dc to  $>250$  MHz with 1830A plug-in and signals producing 1.0 div or more vertical deflection.

External: dc to  $>250$  MHz with signals of 20 mV pk-pk or more, increasing to 50 mV at 500 MHz. Input impedance 50 ohms.  $\div 10$  trigger attenuator allows wider dynamic ranges of INT and EXT trigger input.

**AUTOMATIC:** bright baseline displayed in absence of trigger signal. Triggering is same as normal except low frequency limit is 5 Hz for internal and external triggering.

**SINGLE SWEEP:** selectable with front-panel switch; reset pushbutton with armed indicator light. Rear-panel input provides remote arming.

**TRIGGER LEVEL AND SLOPE:**

Internal: any point on the vertical waveform displayed.

External: trigger level continuously variable from +0.1V to -0.1V on either slope of sync signal; from +1.0V to -1.0V in  $\div 10$  setting.

**COUPLING:** front-panel selection of ac or dc. AC attenuates signals below approximately 5 kHz.

**VARIABLE HOLD OFF:** time between sweeps continuously variable, exceeding one full sweep on all ranges.

**GENERAL**

**WEIGHT:** net, 3 lb (1,4 kg); shipping 6 lb (2,7 kg).

## SECTION IV

## PRINCIPLES OF OPERATION

## 4-1. INTRODUCTION.

4-2. Descriptions of basic circuits used in Model 1840A are covered at the beginning of this section. A block diagram, Figure 4-7, with a brief overall functional explanation is given following the basic circuit paragraphs. The last paragraphs give detailed circuit descriptions (keyed to the schematics) of the Model 1840A.

## 4-3. BASIC CIRCUIT DESCRIPTIONS.

## 4-4. COMPARATOR.

4-5. Comparators are used in this instrument to reference a signal to a dc level. A basic comparator is shown in Figure 4-1. Bias for both transistors is adjusted by R4. If the arm of R4 is moved toward the positive supply voltage, current increases through Q2 and decreases through Q1. Moved in a negative direction, R4 reverse biases Q2 and forward biases Q1. Since R4 controls the quiescent dc voltage levels of this circuit, it is called a LEVEL control.

4-6. When the positive excursion of an input signal applied to the base of Q1 reaches an amplitude sufficient to overcome the bias set by R4, Q1 increases conduction. A voltage is dropped across R1, and output A moves in a negative direction. At the same time, a voltage is dropped across R3, making the emitter of Q2 more positive. Therefore, Q2 conduction decreases, and output B moves in a positive direction. During the negative excursion of an input signal, conditions reverse. Conduction decreases for Q1 and output A moves positive; conduction increases for Q2 and output B moves negative. Thus, as input signal polarity alternates, so does the amount of conduction for the two transistors.

4-7. The Model 1840A has two comparator circuits. First is the trigger comparator which produces two

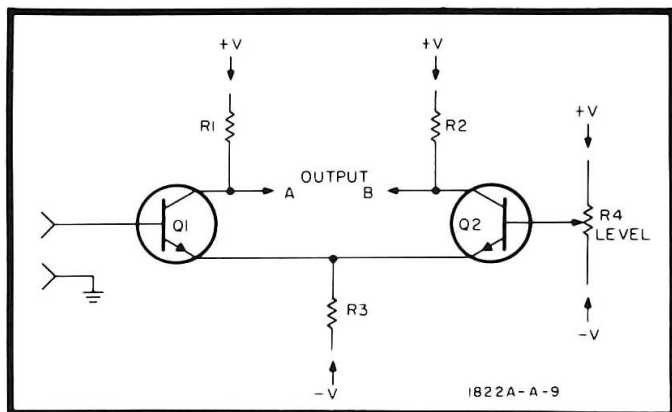


Figure 4-1. Basic Comparator

differential output signals for further amplification. Second, a comparator is used in the sweep reader circuit where one output is required. The output is the dc voltage level at the collector of A1Q14B which restores a dc level to the sweep signal.

## 4-8. DIFFERENTIAL AMPLIFIER.

4-9. Figure 4-2 shows a basic differential amplifier. Only out-of-phase (difference) signals are amplified by this circuit. In-phase waveforms applied to both inputs are called common-mode signals. These, often in the form of unwanted noise and stray pick-up, are rejected.

4-10. Input signals of opposite polarity cause one transistor to increase conduction and the other to decrease conduction. Since the output is taken across the two collectors, input signals are amplified and voltage drops across R2 and R3 are summed.

4-11. When common-mode signals are applied, both transistors either increase or decrease conduction and cause equal current changes through R2 and R3. Thus, no output is developed with common-mode signals.

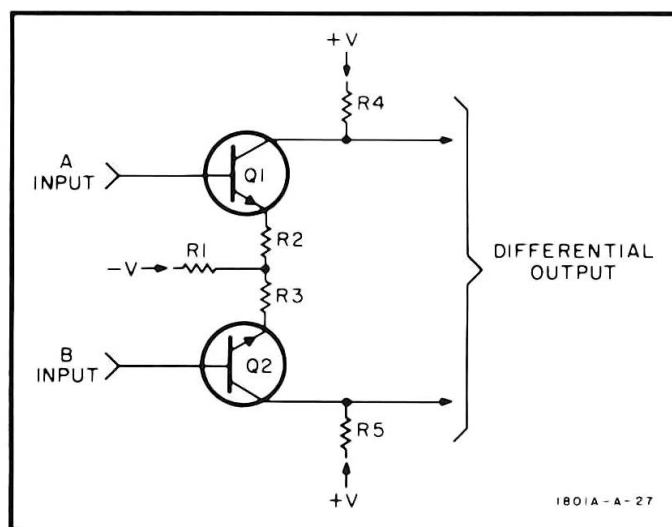


Figure 4-2. Basic Differential Amplifier

## 4-12. SCHMITT TRIGGER.

4-13. A Schmitt trigger circuit (Figure 4-3) is a type of triggered multivibrator. This circuit is characterized by two stable states and a fast risetime and falltime. Initially Q1 is cutoff and Q2 is in saturation. Current through Q2 develops a voltage drop across R4, reverse biasing Q1 and ensuring no Q1 conduction. If a positive trigger is applied

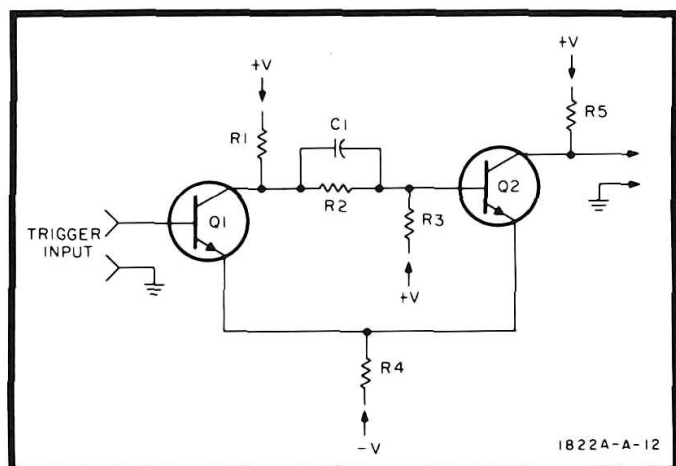


Figure 4-3. Basic Schmitt Trigger

to the base of Q1, forward bias is aided and Q1 starts to conduct. As current flows through R1, a voltage is dropped across it, and the collector of Q1 goes negative. This negative voltage is coupled through R2 to the base of Q2. Conduction for Q2 decreases, removing the voltage drop across R4 and removing the reverse bias from Q1. Now Q1 saturates and Q2 goes into cutoff. The circuit remains in this state until the input trigger to Q1 goes sufficiently negative to remove the forward bias from Q1.

#### 4-14. MONOSTABLE MULTIVIBRATOR.

4-15. A simple emitter-coupled monostable multivibrator is shown in Figure 4-4. This circuit has only one stable state, that is, one transistor is normally saturated and the other is cut off. Operation reverses temporarily when an input signal is applied, then the circuit reverts back to the stable state by itself. The time necessary for the monostable multivibrator to revert back to the stable state is established by the timing capacitor (C1) and timing resistor (R4). This cycle repeats for each trigger pulse applied. Another name for this circuit is one-shot multivibrator.

4-16. During quiescence, Q2 is saturated and Q1 is cut off due to supply voltages. This is the stable state. A negative-going trigger applied to the base of Q1 forward biases the transistor and starts conduction. A voltage is dropped across R2, and the collector of Q1 goes positive. At this point C1 discharges through R4, driving the base of Q2 positive and reverse biasing it. Now Q1 saturates and Q2 cuts off. After C1 discharges through R4, Q2 is again forward biased by the supply voltage and starts conducting. As Q2 draws current through R5, a negative-going voltage at the top of R5 reverse biases the emitter of Q1 with respect to base and Q1 cuts off. The circuit has now returned to the stable state and will remain in this condition until another trigger signal is applied.

4-17. The HP Model 1840A uses a pulse to control the monostable multivibrator. The period of the pulse is equal to the sweep gate period. The sweep gate signal will keep the multivibrator in the unstable state. After the gate ends,

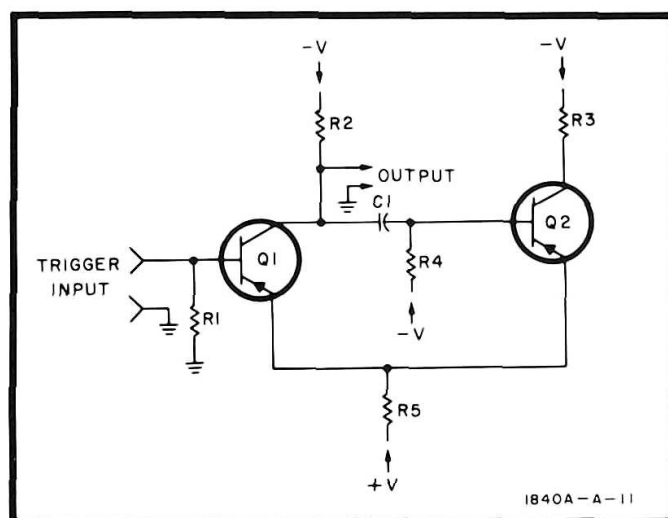


Figure 4-4. Basic Monostable Multivibrator

the multivibrator will continue in the unstable state for a period determined by the timing capacitor (C1) and timing resistor (R4).

#### 4-18. OVERALL CIRCUIT DESCRIPTION.

4-19. The HP Model 1840A Time Base consists of trigger, gate, and sweep circuits. Refer to the block diagram, Figure 4-7, for the following description. The time base can be triggered or set to free run. When triggered operation is used, the required trigger signal is coupled to the trigger comparator and amplifiers through the trigger selection and conditioner circuits. The trigger signal is coupled from one of three inputs: external (EXT) input, internal (INT) input, or line frequency (LINE) from power transformer. Free-run operation is selected by setting the MODE switch to AUTO. In this position, the Model 1840A operates without a trigger signal. However, if a trigger signal is applied, it will override the free-run operation and generate the sweep. The trigger-coupling switch determines the type of coupling for the incoming trigger signal while the TRIGGER LEVEL control selects the voltage point on the selected slope where sweep generation starts. Selection of positive or negative slope of trigger signal for sweep generation is accomplished in the polarity selection circuit.

4-20. In NORM operation, the dual tunnel diode trigger circuit produces a negative rectangular pulse which is applied to the oscilloscope CRT through the gate output circuit for unblanking the trace. Also, the negative pulse is applied to the sweep integrator circuit. The sweep integrator circuit is normally clamped so that the output is a constant dc voltage. The negative gate signal unclamps the sweep integrator circuit which generates a positive-going sawtooth signal. This sweep signal is coupled through the sweep reader circuit to the oscilloscope for horizontal deflection. The sweep signal is also applied to length Schmitt and hold-off circuits through the hold-off driver. At approximately 10 volts, the length Schmitt circuit switches to the other state, turning the dual tunnel diode trigger circuit off to end the sweep ramp in



the sweep integrator. After the sweep ramp ends, the sweep integrator will return to the quiescent level. At the same time, the hold-off capacitor will begin to discharge to 0 volt. At approximately 1 volt, the length Schmitt circuit will switch back to the pre-trigger state. The length Schmitt resets the control reset and the dual tunnel diode trigger circuit for the next trigger pulse. The dual tunnel diode trigger circuit will again start the sweep gate signal and repeat the sweep cycle.

4-21. When operating in AUTO MODE, the input from the control reset to the dual input gate circuit is biased so that when the control reset is rearmed, the dual input gate circuit generates a new gate and sweep. At the end of the hold-off time, the control reset changes states. The control reset will be rearmed and a new gate will be generated, resulting in a new sweep. The sweep period is determined by the SWEEP TIME/DIV switch which also determines the frequency of free-run operation. If, however, a signal of 5 hertz or greater is applied to the dual tunnel diode trigger circuit, it will override the AUTO circuit and lockout free run operation.

4-22. When the MODE switch is set to SINGLE, the sweep reset circuit overrides the hold-off circuit in the length Schmitt circuit and controls the reset operation. The gate generator can then be reset by manually switching the length Schmitt to the pre-trigger state or by an EXT input from the rear panel of the Model 183A/B Oscilloscope.

#### 4-23. CIRCUIT DETAILS.

4-24. The following paragraphs explain the theory of operation of the Model 1840A. See the block diagram, Figure 4-7, and the schematics in Section VIII while reading the text. An explanation of the reference designator system used in this manual is located in Section VIII.

#### 4-25. NORMAL SWEEP OPERATION.

#### 4-26. TRIGGER INPUT CIRCUIT.

4-27. Three trigger sources can be selected by the front-panel switches EXT/INT, A1A1S1, and LINE, A1A1S3. The internal trigger signal can be received from connector P2 or P3. When the Model 1840A is used with the vertical amplifier of the HP 183-series oscilloscopes, the internal signal is applied through P3 and supplied directly to A1A1S1. The Model 1840A can also be used with vertical amplifiers in the HP 180-series oscilloscopes and the trigger signal is supplied through P2. The trigger signals from HP 180-series vertical amplifiers are ac-terminated into 100 ohms, and are terminated by A1R2 at all times into the 50-ohm system of the Model 1840A. The position of A1A1S1 determines the trigger signal to be used and the other trigger signal is terminated into 50 ohms. The termination prevents coupling of unwanted signals into the time base.

4-28. AC/DC Switch A1A1S2 selects the coupling desired. DC couples the selected trigger directly to the LINE switch. AC removes the dc portion of the trigger signal and attenuates frequencies below approximately 5 kilohertz. The trigger signal is then supplied to LINE TRIGGER switch A1A1S3. If LINE is selected, the previously selected trigger signal is terminated into 50 ohms by resistor, A1R6. The LINE trigger is a 3-volt ac peak-to-peak signal obtained from the power transformer. After the coupling switch (AC/DC), the selected trigger signal is supplied to the  $\div 1/\div 10$  switch, A1A1S4. In  $\div 1$ , the trigger signal is supplied directly to the trigger comparator and is terminated by the 50-ohm input of the trigger comparator. If  $\div 10$  is selected, the trigger signal is attenuated by a factor of 10 and is also terminated by the 50-ohm input of the trigger comparator.

#### 4-29. TRIGGER AMPLIFIER.

4-30. The trigger signal is applied to the trigger amplifier where the trigger level point and polarity are selected. Diodes A1CR2 and A1CR3 are overload protection diodes for the base-emitter junctions of transistors A1U1Q1 and Q2. TRIGGER LEVEL control R1 sets the trigger point where gate generation starts. The trigger level is applied to the trigger comparator circuit at A1U1Q2. Transistor A1U1Q2 has an input impedance of 50 ohms which is established by resistor A1R15. The trigger level range of the Model 1840A is  $\pm 100$  millivolts for the  $\div 1$  input and  $\pm 1$  volt for the  $\div 10$  input. The trigger signal is converted to a differential voltage signal by A1U1Q1 and Q2. Resistor A1R19 is the trigger amplifier balance which is used to balance any dc offset in A1U1Q1 and Q2. Also, the trigger amplifier balance adjustment sets the TRIGGER LEVEL potentiometer zero to center of range.

4-31. The trigger signal is amplified and converted to a current signal by the first stage of the trigger amplifier for the polarity function. Diodes A1CR4-7, in association with polarity switch A1S5, make up the polarity-selection circuit. When + (positive) slope is selected, a positive voltage is applied to the anode of A1CR6 and a negative voltage is applied to the cathode of A1CR7. The trigger signal is coupled from A1U1Q3 to A1U2Q1 and from A1U1Q4 to A1U2Q2. If - (negative) slope is selected, a positive voltage is applied to A1CR5 and a negative voltage is applied to A1CR4. The trigger signal is coupled from A1U1Q3 to A1U2Q1 and from A1U1Q4 to A1U2Q3. The signal current through A1R28 develops a signal voltage across A1R28. The trigger signal is voltage amplified by A1U2Q1 and Q2. The trigger signal is coupled to A1U2Q3 and A1U2Q4, part of the dual tunnel diode trigger circuit.

#### 4-32. DUAL TUNNEL DIODE TRIGGER CIRCUIT.

4-33. Transistors A1U2Q3 and U2Q4 along with diodes A1CR8 and CR9, form the dual tunnel diode trigger circuit. Tunnel diode A1CR8 receives current from the negative supply through transistor A1U2Q3 and resistor R34. Tunnel diode A1CR9 receives current from the same

negative supply through transistor A1U2Q4 and resistor A1R34. Initially current is supplied to A1CR9 from the collector of Q3 in the control reset circuit. However, the current is insufficient to switch A1CR9 to the high voltage state. The current supplied to A1CR8 by A1R43 and R44 is insufficient to switch tunnel diode CR8 to the high-voltage state.

4-34. The sync signal is applied differentially to the dual tunnel diode trigger circuit. During the positive portion of the trigger signal applied to the base of A1U2Q4, there will be a signal level that will supply enough additional current to A1CR9 to switch A1CR9 to the high-voltage state. When the next positive portion of the input signal arrives at the base of A1U2Q3, sufficient current will flow through A1CR8 to switch A1CR8 to the high-voltage state. With A1CR8 and A1CR9 conducting, the bias established across A1R35 is that bias required to keep A1CR8 and CR9 in the high-voltage states. When A1CR8 is in the high-voltage state, a negative gate pulse is generated and lasts as long as A1CR8 is in that state.

4-35. When hold-off time starts, A1Q4 is driven into conduction and current flow through A1Q3 is cut off. The reduction in current through A1Q3 causes A1CR8 and CR9 to switch to the low-voltage states. After hold-off time ends, the current flow through A1Q3 is restored but is not adequate to turn on A1CR9.

4-36. In order for the dual tunnel diode trigger circuit to respond to the next trigger pulse, A1CR9 must be switched to the high-voltage state before A1CR8. When the positive portion of the sync signal arrives at the base of A1U2Q4, the current through A1U2Q4 will increase and supply the additional current required to switch A1CR9 to the high-voltage state. The point where A1CR9 turns on is the lower hysteresis limit. When the dual tunnel diode trigger circuit passes through the lower hysteresis limit, the circuit is rearmed and ready to produce a new gate. The next positive portion of the trigger signal at the base of A1U2Q3 will switch A1CR8 to the high-voltage state and start a new gate. The voltage level required is the upper hysteresis limit. Thus the dual tunnel diode trigger circuit must pass through the lower then upper hysteresis limits before a new gate is generated.

#### 4-37. GATE CIRCUIT.

4-38. The negative gate from A1CR8 is applied to the dual input gate circuit at the base of transistor A1U1Q1, resulting in a differential gate output from the collectors of A1U4Q1 and Q2. Throughout normal operation, transistor A1U4Q3 is biased off. The differential gate signal is coupled to another differential amplifier (transistors A1Q5 and Q6) which increases the amplitude of the gate signal to ensure rapid signal currents at A1Q7 and Q9. The differential gate signal from the collectors of A1U4Q1 and Q2 is at an average level of +15 volts. The average level of +15 volts must be shifted to an average level of about -9 volts before the gate signal can be

applied to the bases of A1Q7 and Q9. Zener diodes A1VR2 and VR3 accomplish the shift to approximately -9 volts as well as limit power dissipation in A1Q5 and Q6.

4-39. The negative-going gate pulse at the base of transistor A1Q7 produces two outputs. First, the alternate trigger output is supplied to J1, pin 22 from the collector of transistor A1Q7. The alternate trigger signal is opposite the polarity of the base of transistor A1Q7. Second, the gate output is supplied to P1, pin 17 from the collector of transistor A1Q8. The gate output signal is the same polarity as the base of transistor A1Q7. The alternate trigger signal is supplied to the vertical amplifier for ALT operation of the vertical amplifier. For 180-series vertical amplifiers, the alternate trigger signal is supplied by the HP Model 183A/B Oscilloscope and is coupled from P1, pin 6 to J1, pin 24. The alternate trigger signal for a 183-series vertical amplifier is coupled directly to the vertical amplifier to avoid time delay of the alternate trigger signal. The time delay would limit the alternate switching rate.

4-40. The positive-going gate pulse at the base of A1Q9 also produces two functions. First, a gate output of opposite polarity is supplied to the rear panel of the Model 183A/B Oscilloscope. The gate signal is coupled through P1, pin 13. Second, the gate signal determines the time allowed for selected integrator capacitor to develop a positive charge.

4-41. Prior to the gate signal at the base of transistor A1Q9, the sweep current for transistor A1Q33 was supplied by transistor A1Q10. When the gate signal arrives, transistors A1Q10 and Q11 are turned off. The sweep current through diode A1CR17 is then supplied by the selected sweep timing capacitor. During the ramp sequence, transistor A1Q20 is biased off.

4-42. The current source for the sweep timing capacitor must have high output impedance. The collector circuit of transistor A1Q33 provides the required impedance. Because of the common-base configuration of transistor A1Q33 and because the base current is held constant, the current flow to the sweep timing capacitor will be constant. Voltage drop across the selected sweep timing resistor determines the current into the emitter of transistor A1Q33. The voltage drop is constant and is established by the potential difference between the emitter of transistor A1Q33 and the base of transistor A1Q35. By changing the sweep timing resistor, the current flow to the sweep timing capacitor will also change. The potential at the base of transistor A1Q35 is equal to the potential at the base of transistor A1Q36 and is set by R3. Transistor A1Q35, connected as a diode, provides an offset compensation so that the voltage at the base of transistor A1Q35 is at approximately the same voltage as the base of transistor A1Q36.

4-43. When the SWEEP VERNIER is switched out of the detent position and is rotated in a counterclockwise

direction, the level at the bases of transistors A1Q36 and Q35 decreases. This decreases the current flow through transistors A1Q36 and Q34. The sweep timing capacitor requires more time to reach approximately +10 volts and the longer charge time results in slower sweep speeds. Also the UNCAL indicator lights when this operation is used to indicate when the time base is not in calibrated operation.

#### 4-44. SWEEP READER CIRCUIT.

4-45. The ramp voltage developed on the sweep timing capacitor is applied to the gate of field-effect transistor (FET) A1Q13 of the sweep reader circuit. Transistors A1Q12, Q13, Q14, Q16, and Q17 make up the sweep reader circuit. The high input impedance of transistor A1Q16 allows the drain of transistor A1Q13 to follow the gate within 1%. Transistor A1Q13 has unity gain because of the source-follower configuration. The ramp signal is capacitively coupled to transistor A1Q16 to remove the dc component of the signal. The ramp signal again passes through a unity-gain amplifier consisting of A1Q16 and Q17 with a resulting sweep ramp from 0 to +10 volts.

4-46. The dc level of the sweep is established by comparator transistors A1Q14A and Q14B and is coupled back to the sweep ramp signal at the base of transistor A1Q16. The sweep ramp at the base of A1Q13 couples through the high frequency roll-off circuit (resistor A1R92 and capacitor A1C15) to the base of transistor A1Q14A in the comparator. The output sweep ramp at the emitter of A1Q17 is also coupled through a high frequency roll-off circuit (resistor A1R97 and capacitor A1C17) to the base of A1Q14B. The resultant level of the comparator at the collector of A1Q14B is restored to a sweep ramp signal at the base of transistor A1Q16. This function ensures a constant dc level of the sweep ramp. The sweep signal from the emitter of A1Q17 is then supplied to the horizontal amplifier in the Model 183A/B oscilloscope through P1, pin 1. The input impedance at the horizontal amplifier, with resistor A1R99, converts the sweep ramp from a 0-to-+10-volt signal to a 0-to-2.5-milliampere signal.

#### 4-47. SWEEP TERMINATION.

4-48. The hold-off driver circuit, transistors A1Q18 and Q19, is an emitter follower of low dc offset with thermal compensation whose purpose is to isolate the length Schmitt circuit and the hold-off circuit from the sweep reader circuit. As the sweep ramp develops on the emitter of transistor A1Q19, diode A1CR36 turns on at approximately 8 volts. The base of transistor A1Q32 is drawn positive, causing the length Schmitt to change states at approximately 10 volts. When the length Schmitt changes state, a positive pulse is developed at the collector of transistor A1Q31 which is coupled to control reset transistors A1Q3 and Q4. The control reset changes state, turning off transistor A1Q3 and removing the current supply to tunnel diodes A1CR8 and CR9. Both A1CR8

and CR9 turn off and end the gate. Turning off the sweep gate results in a positive transition that turns on transistors A1Q10 and Q11. The current for transistor A1Q33 is again supplied by A1Q10. Transistor A1Q11 supplies a discharge path for the sweep timing capacitor. During the positive transition at the collector of transistor A1Q31, current is supplied through resistor A1R108 to the base of transistor A1Q20. Transistor A1Q20 is turned on and aids in rapidly discharging the sweep timing capacitors.

#### 4-49. HOLD-OFF CIRCUIT.

4-50. As the sweep voltage increases, diode A1CR24 turns on and the hold-off capacitor charges positively. When the sweep resets, diode A1CR24 becomes reverse-biased and the hold-off capacitors discharge because of the current supplied by the collector of transistor A1Q27. The hold-off signal is applied to the hold-off reader circuit, transistors A1Q21 and Q22, a thermal-compensated emitter-follower pair. The hold-off circuit discharges from +10 volts to 0 volt. At approximately 5 volts, the voltage divider resistors A1R110 and R109 apply about 0 volt to the anode of diode A1CR23. This hold-off voltage level turns off diode A1CR23. The current supplied by A1R107 now flows through diode A1CR22 which establishes a bias on transistor A1Q20, fast reset circuit. The bias will turn off transistor A1Q20 approximately half way through the hold-off period. Transistor A1Q20 must be turned off half way through the hold-off period to ensure that all base charge is removed from A1Q20 when the new sweep starts.

4-51. During the sweep period, the collector of A1Q31 is at its low level. The current that flows through transistor A1Q31 also flows through resistor A1R108. The current develops a voltage level at the cathode of diode A1CR21 that will forward bias diode A1CR21. Capacitor A1C19 will charge to approximately -0.6 volt. At the end of a sweep, the collector of transistor A1Q31 will switch to the high-voltage level and will permit transistor A1Q20 to conduct. Transistor A1Q20 will permit rapid discharge of the sweep timing capacitor. However, the discharge operation is delayed by the time required for capacitor A1C19 to discharge and permit transistor A1Q20 to conduct. This ensures that the discharge current through transistor A1Q20 does not start before the gate turns off in the integrator circuit.

4-52. The hold-off ramp on the emitter of transistor A1Q21 continues to decrease. When the emitter of transistor A1Q21 reaches approximately 1.0 volt, enough current is generated in resistor A1R111 to supply current to resistors A1R112 and A1R141. The current flow will cause the base voltage of transistor A1Q32 to decrease enough to switch the length Schmitt to the stable state. The change in level on the collector of transistor A1Q31 causes the control reset to change states and transistor A1Q3 again supplies arming current to tunnel diode A1CR9.



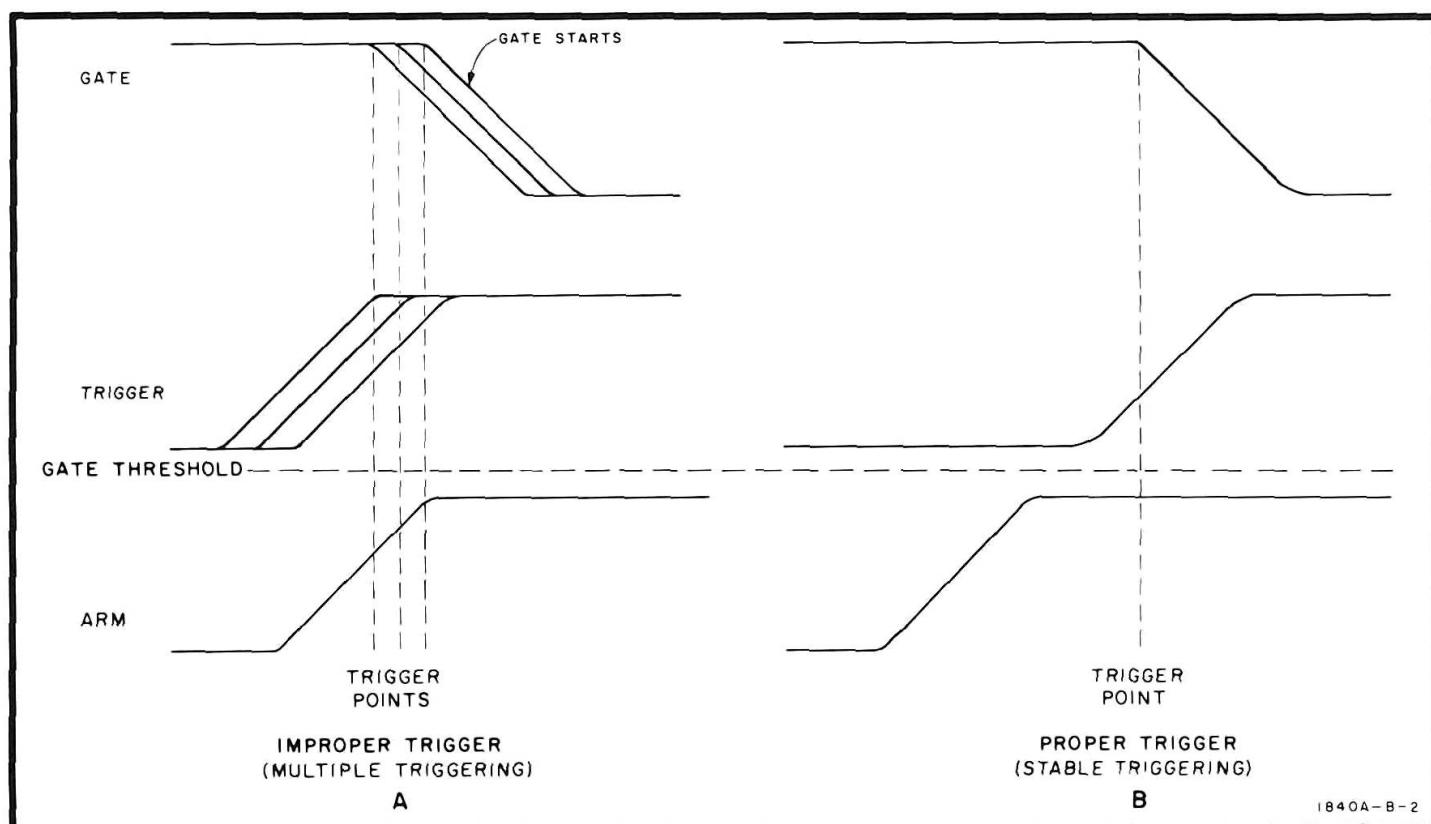


Figure 4-5. Sweep Trigger Level Analysis

#### 4-53. AUTOMATIC HIGH-FREQUENCY STABILITY CIRCUIT.

4-54. It is possible for the arming pulse to occur at about the same time as the trigger pulse and cause unstable triggering on the screen of the CRT. To avoid the various combinations of triggering time illustrated in Figure 4-5A, the hold-off time is shortened to ensure that the arming current is present and stabilized before the trigger pulse arrives in the dual tunnel diode trigger circuit.

4-55. The sweep stability is established in the automatic high frequency stability circuit of transistors A1Q23-Q25. The negative-going sweep gate is applied to the base of transistor A1Q23. The current signal that is developed on the emitter of transistor A1Q23 is combined with the inverse arming current signal in "and" gate A1R120, CR27, and CR28 and the resultant signal (combined signal of the gate signal and inverse arming signal) is applied to the base of transistor A1Q25. The current signal is inverted by A1Q25 and the resultant signal is a negative-going voltage pulse.

4-56. The voltage signal that is developed on the emitter of transistor A1Q23 is differentiated by resistor A1R118 and capacitor A1C20. The resultant negative voltage is inverted by transistor A1Q24. The two signals from transistors A1Q24 and A1Q25 produce a positive voltage charge on capacitor A1C21. The two signals are of opposite polarity and the resultant voltage is analogous to the difference. The analog voltage is applied to source

follower transistor A1Q26. The signal at the source of transistor A1Q26 is dc coupled to transistor A1Q27, hold-off current source, and causes a change in hold-off time.

4-57. For normal operation, the differentiated gate signal and the combined gate and inverse arming signals are equal in width and amplitude. This results in constant hold-off current through transistor A1Q27. If the arming signal occurs closer in time to the trigger signal, the combined gate and inverse arming pulse becomes narrower. This causes a more positive voltage charge on capacitor A1C21 which increases the hold-off discharge rate and decreases the hold-off time. Decreasing the hold-off time assures that the arming current is present and stable before a new trigger pulse arrives.

4-58. Figure 4-5 illustrates the necessity for the automatic high frequency stability circuit. Part A shows three conditions that can occur and Part B shows an ideal situation. When the sum of the levels of the trigger and arming signals reaches gate threshold in the dual tunnel diode trigger circuit, a new gate will be produced. If the trigger signal varies in time in relation to the arming signal, different sums of levels will reach gate threshold and start a new gate. However, if the leading edge of the arming signal is advanced in time or hold-off time shortened, as in Part B of Figure 4-5, the arming signal will be at maximum level and be stabilized before the trigger signal arrives. The additional level required to produce a new gate will be the same from trigger signal to trigger signal.

## 4-59. AUTO OPERATION.

4-60. When AUTO MODE is selected (with SINGLE MODE pushbutton out), approximately 200 microamperes are applied to the collector of transistor A1U3Q3 and base of transistor A1Q1. Transistor A1Q1 will turn on and cause transistor A1U3Q5 to turn off, establishing a bias on the base of transistor A1U4Q3. With the bias, a small shift in signal at the collector of transistor A1Q4 will turn on transistor A1U4Q3. Transistor A1U4Q3 will produce a gate signal at the end of the hold-off time. The negative transition on the base of transistor A1Q4 of the control reset circuit changes the state of the control reset, turning off transistor A1Q4. With transistor A1Q4 off, a positive transition at the collector will also turn on transistor A1U4Q3 and generate a gate to permit a sweep ramp to be generated.

4-61. When a trigger signal is supplied to tunnel diode A1CR8, the gate signal is generated and applied to the base of transistors A1U3Q1 and A1U4Q1. The resultant gate signal on the collector of transistor A1U3Q1 is a positive transition applied to the monostable multivibrator. The multivibrator will switch states and apply a negative transition to the base of transistor A1Q1 which will turn off transistor A1Q1 and turn on transistor A1U3Q5. The negative transition on the collector of transistor A1U3Q5 will cause transistor A1U4Q3 to go further into cutoff. No transition on the collector of transistor A1Q4 will produce a new gate in the dual input gate circuit. Hence, the free-run operation is locked out.

4-62. To override free-run operation, the trigger signal must make a 20-millivolt excursion in EXT or 1-division excursion in INT during the sweep period as set by the SWEEP TIME/DIV switch. This satisfies the requirement that the trigger signal will pass through the lower and upper threshold levels of the dual tunnel diode trigger circuit during the same arming period. If the trigger signal does not pass through the two threshold levels within the

sweep time necessary, the time base will automatically return to free-run operation.

4-63. If the trigger signal period is less than 0.2 second or a frequency greater than 5 hertz, the monostable multivibrator cannot switch states. The free-run lock out circuit will continue to lock out free-run operation. If the trigger signal period is greater than 0.2 second or a frequency less than 5 hertz, the monostable multivibrator will switch states. This will establish a voltage level on the collector of transistor A1U3Q5 so that transistor A1U4Q3 will turn on when hold off ends, restoring free-run operation.

4-64. Figure 4-6 illustrates AUTO operation. If the period between trigger pulses at tunnel diode A1CR8 is 1 second, the sweep gate generator will not free run during the first 800 milliseconds but will free run during the remaining 200 milliseconds until another trigger pulse is present. If the period between trigger pulses is less than approximately 800 milliseconds, the sweep-gate generator will respond to each trigger. The period of the free-running ramp is determined by the SWEEP TIME/DIV switch (sweep time plus hold-off).

## 4-65. SINGLE OPERATION.

4-66. When SINGLE MODE is selected, the emitter of transistor A1Q30 will change to approximately +15 volts. This prevents the length Schmitt circuit from switching to the unstable state at the end of the sweep ramp. There are two means available to switch the length Schmitt circuit and rearm the time base. Manual RESET with a front-panel pushbutton, electrical reset with a rear-panel input (EXT RESET on Model 183A/B oscilloscope). When a positive pulse is applied to the reset regenerative switch, a negative transition occurs at the emitter of transistor A1Q28 which produces a negative transition at the emitter of transistor A1Q30. This transition will reverse bias diode A1CR33 and current through resistor R111 will switch the length Schmitt circuit and rearm the dual tunnel diode trigger circuit.

4-67. When the dual tunnel diode trigger circuit is reset, the RESET indicator is turned on. Prior to reset, transistor A1Q3 is turned off and no current will flow through transistor A1Q3. The bias on the base of transistor A1Q3 is the same as on the base of transistor A1Q2 and no current will flow through transistor A1Q2. When the control reset circuit is armed, the bias on the base of transistors A1Q3 and Q2 will permit current to flow in both transistors. With transistor A1Q2 conducting, the current will bypass resistor A1R63 through transistor A1Q2 and will cause the voltage level at the collector of A1Q2 to decrease. The voltage drop across A1R61 will increase until DS1 lights. Indicator DS1 will stay on during the arming time and gate time. This indication occurs in all modes but is particularly useful in SINGLE MODE. The indicator will light when the circuit is rearmed and ready to accept a new trigger.

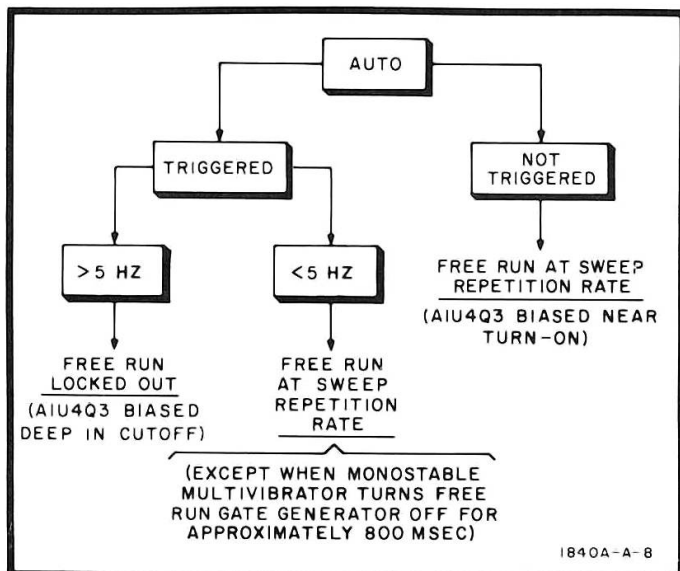


Figure 4-6. AUTO Operation

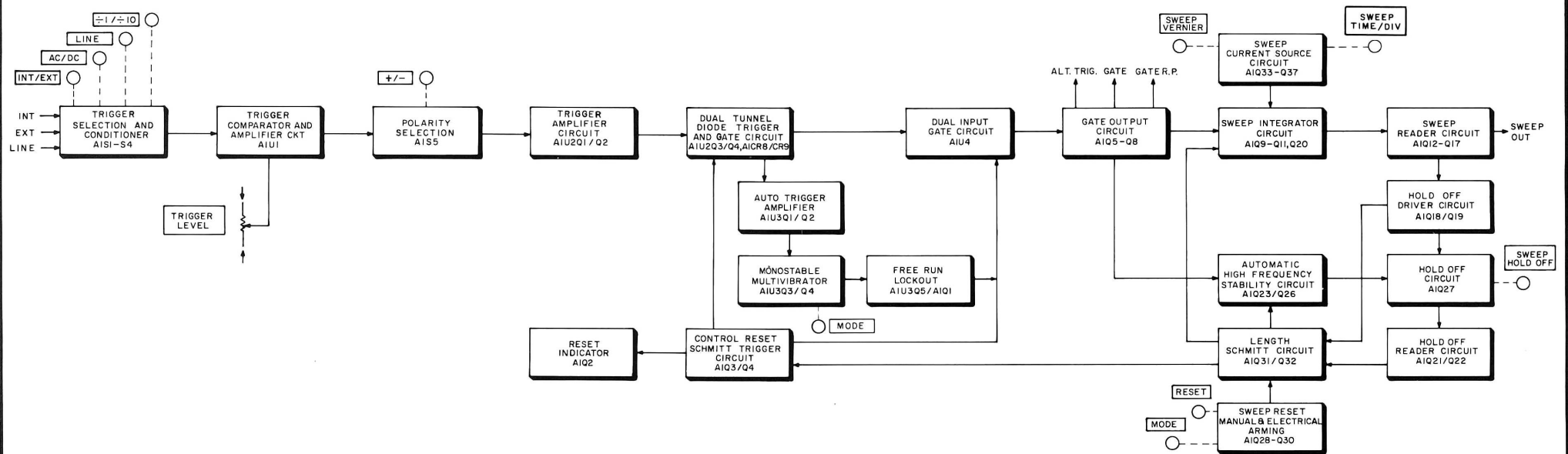


Figure 4-7. Overall Block Diagram





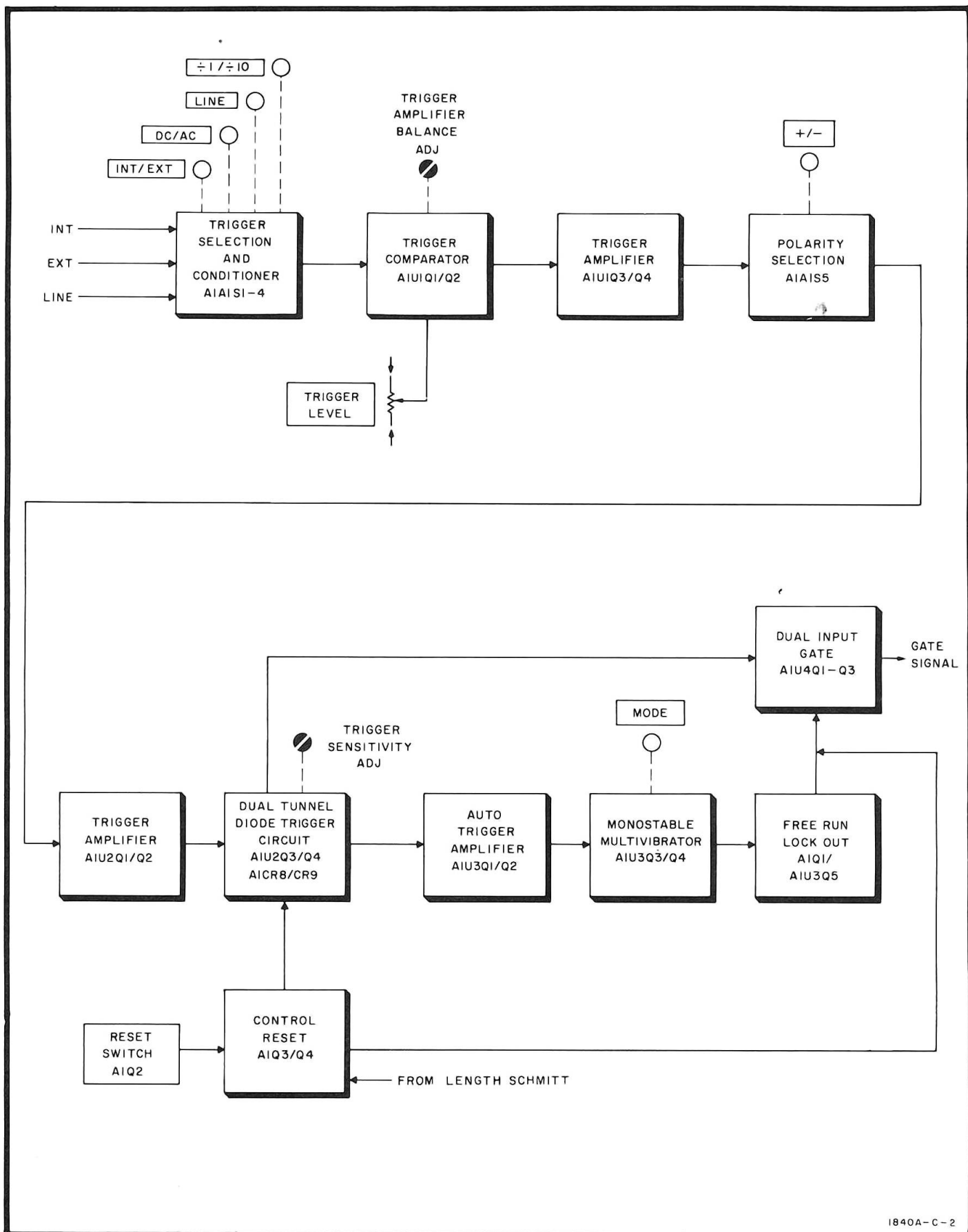
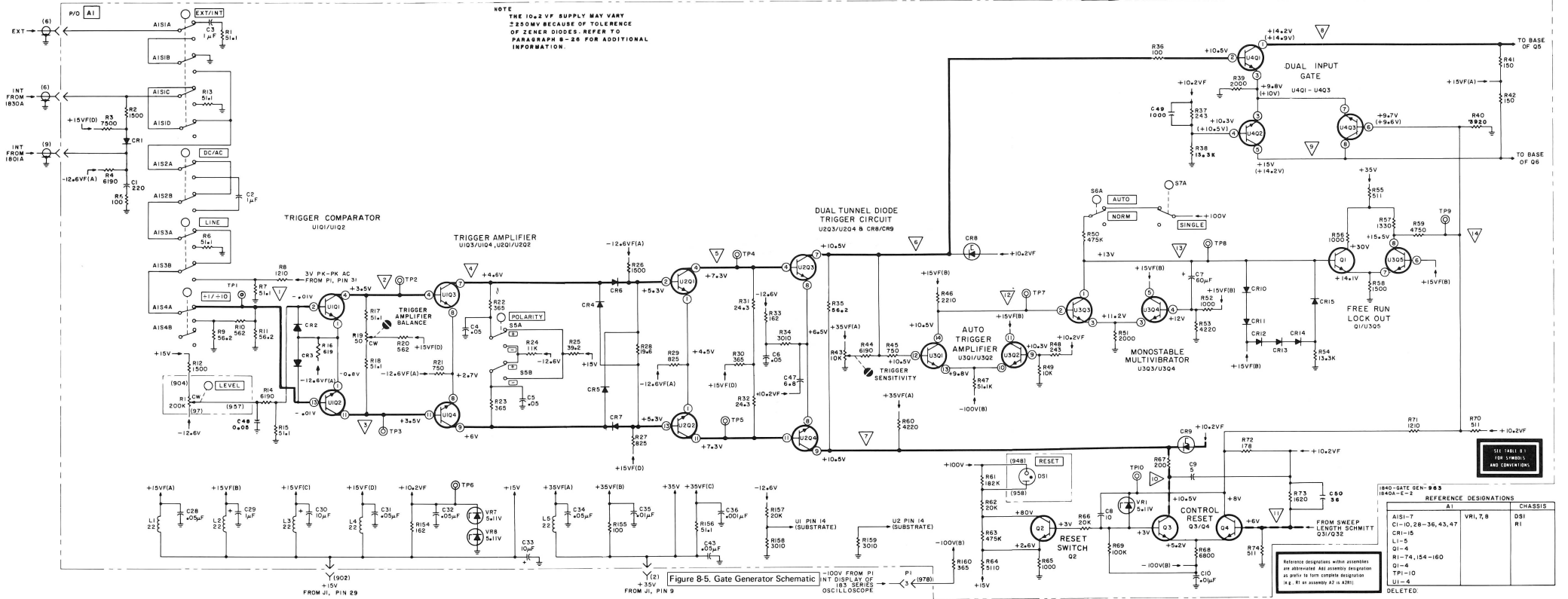


Figure 8-4. Gate Generator Block Diagram



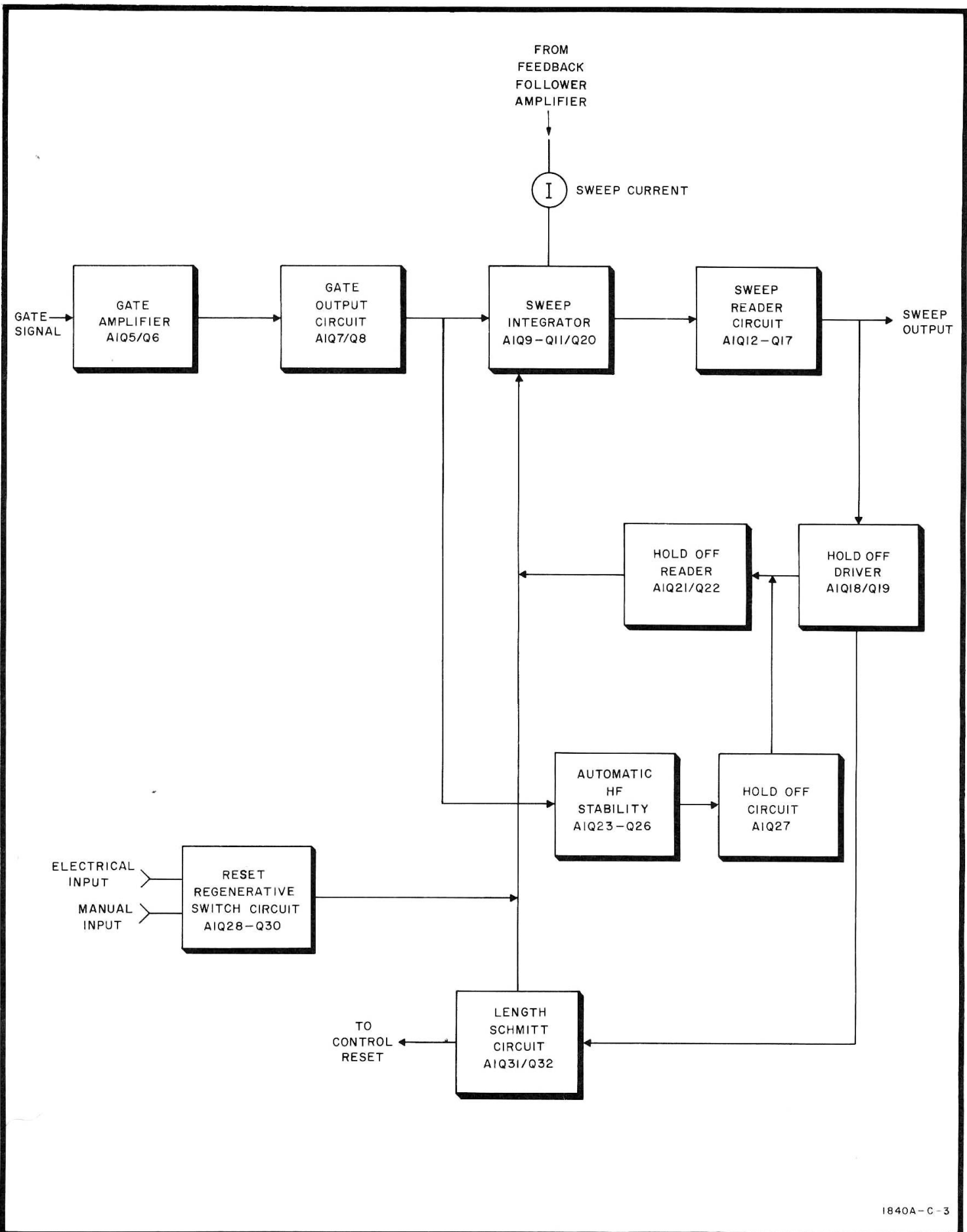


Figure 8-7. Sweep Generator Block Diagrams

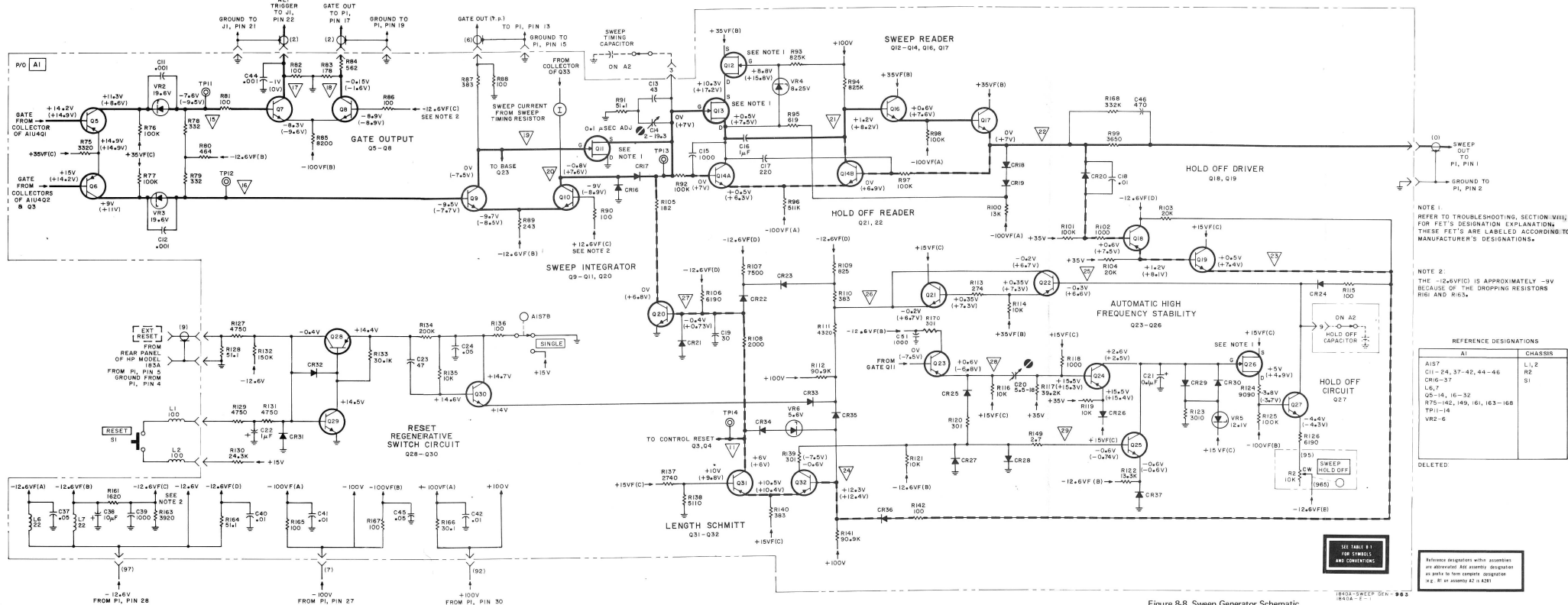


Figure 8-8. Sweep Generator Schematic  
8-7

1840A-SWEEP GEN - 983  
1840A-E-1

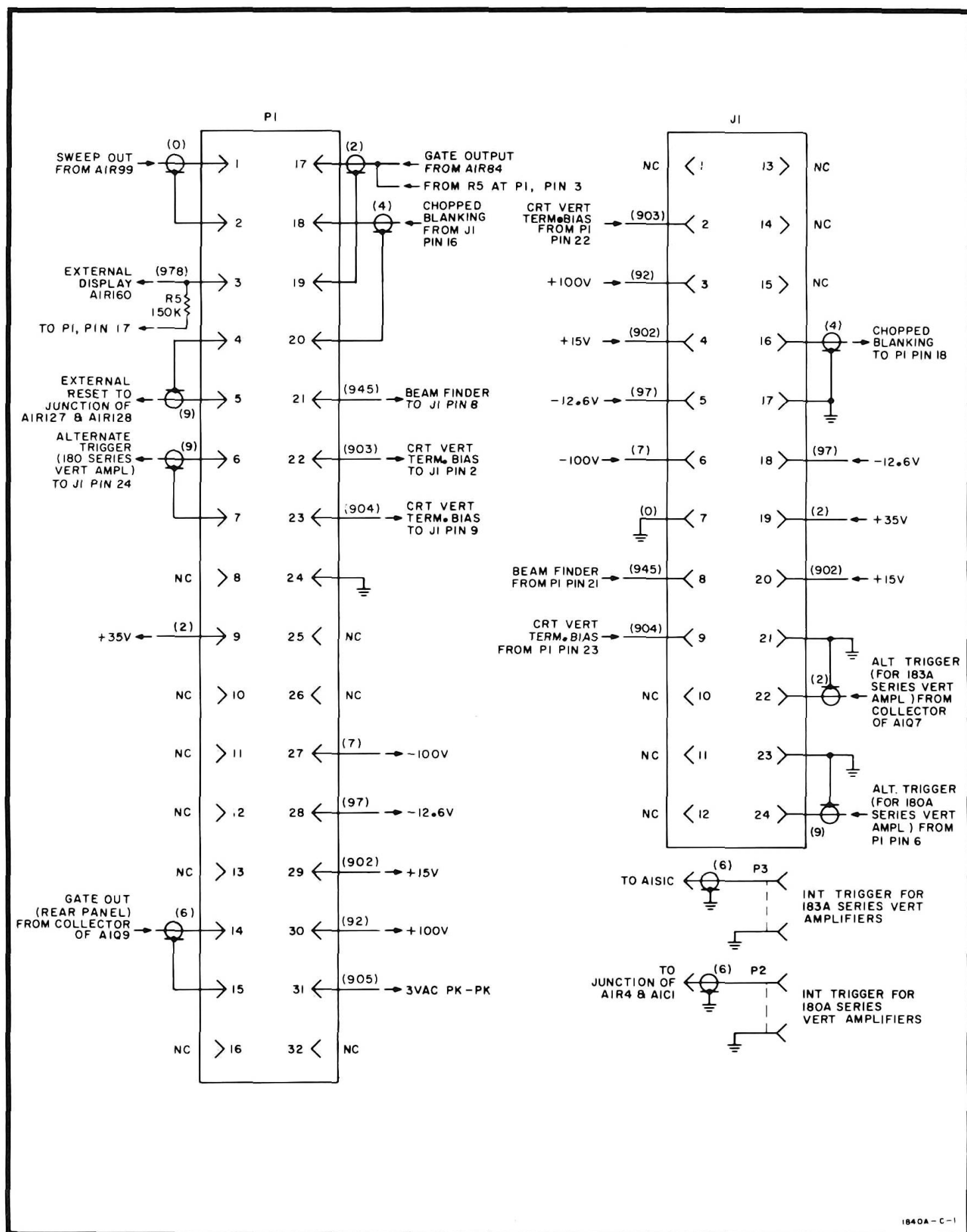


Figure 8-9. Plug and Jack Connections

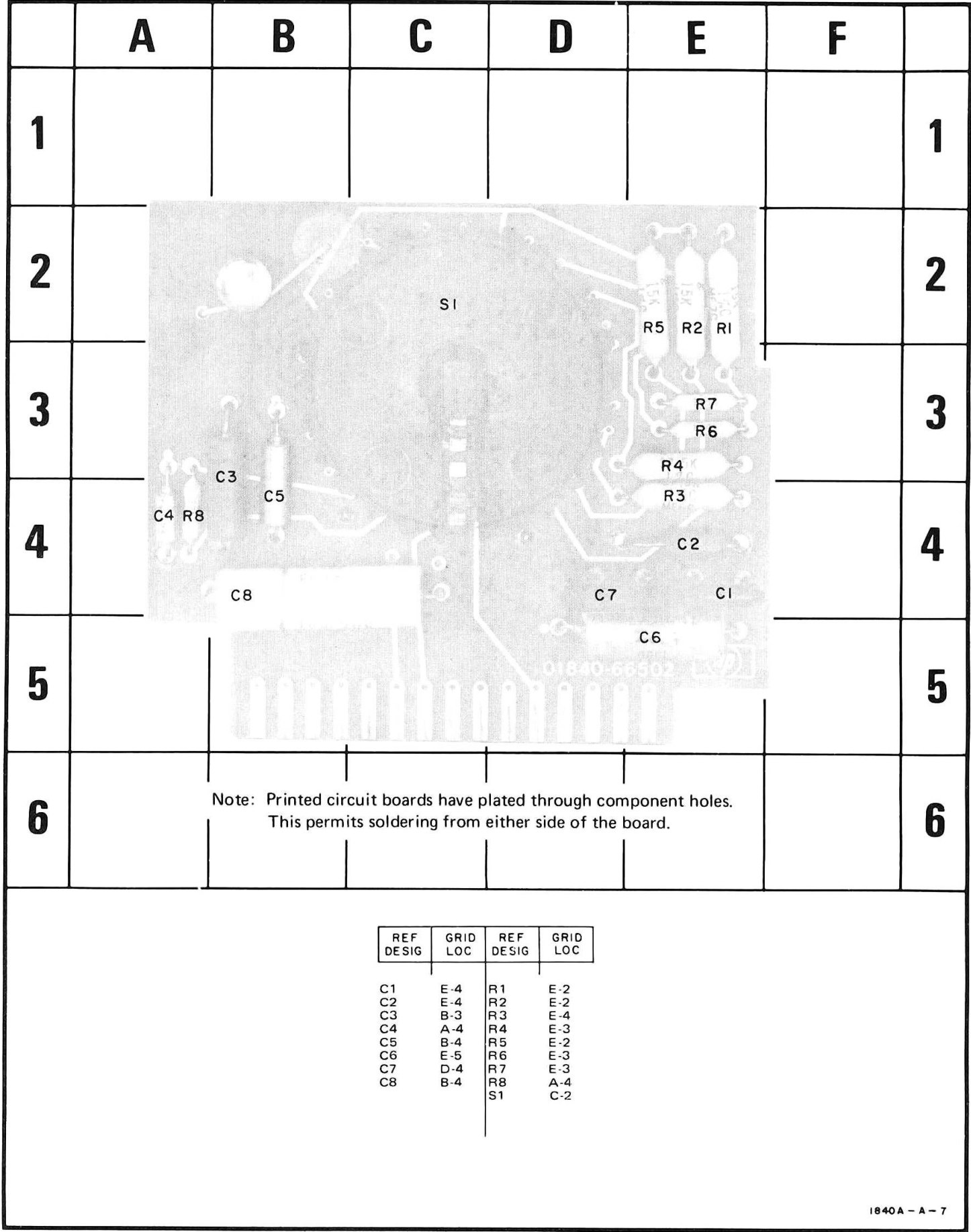


Figure 8-10. A2 Component Locations

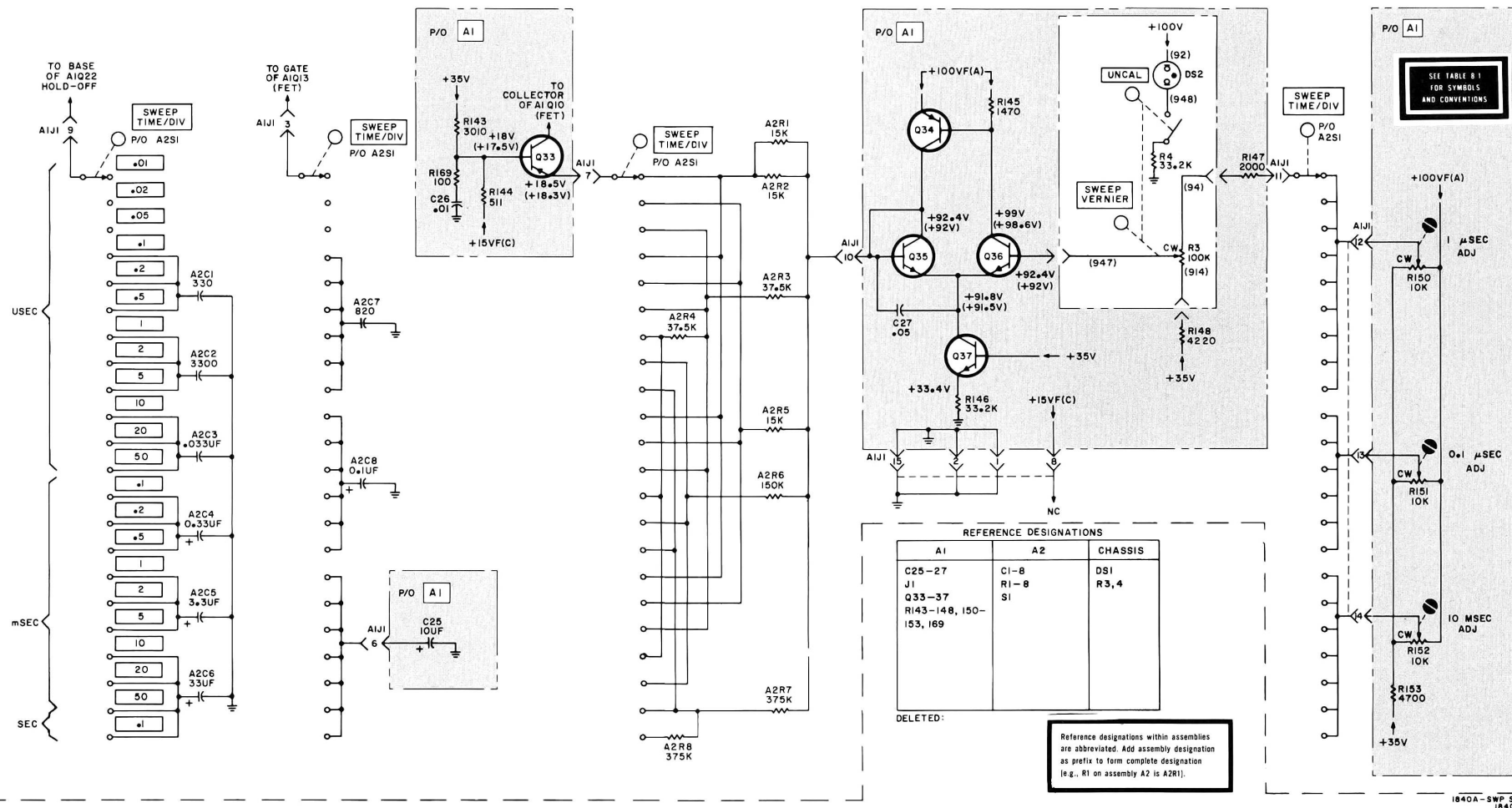


Figure 8-11. Sweep Time Switch and Sweep Current Source Schematic  
8-9/8-10