CIRCUIT DESCRIPTION

Introduction

This section of the manual contains a description of the circuitry used in the 7603 Oscilloscope. The description begins with a discussion of the instrument using the basic block diagram shown in Fig. 4-1. Then, each circuit is described in detail using detailed block diagrams to show the interconnections between the stages within each major circuit and the relationship of the external controls and connectors to the individual stages.

A complete block diagram is located in the Diagrams section at the back of this manual. This block diagram shows the overall relationship between all of the circuits. Complete schematics of each circuit are also given in the Diagrams section. Refer to these diagrams throughout the following circuit description for electrical values and relationship.

BLOCK DIAGRAM

The following discussion is provided to aid in understanding the overall concept of the 7603 before the individual circuits are discussed in detail. A basic block diagram of the 7603 is shown in Fig. 4-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each block represents a major circuit within the instrument. The number on each block refers to the complete circuit diagram located at the rear of the manual.

Vertical signals to be displayed on the CRT are applied to the Vertical Interface circuit from both vertical plug-in compartments. The Vertical Interface circuit determines whether the signal from the left and/or right vertical unit is displayed. The selected vertical signal is then amplified by the Vertical Amplifier circuit to bring it to the level necessary to drive the vertical deflection plates of the CRT.

Horizontal signals for display on the CRT are connected to the Horizontal Amplifier circuit from the horizontal plug-in compartment. The Horizontal Amplifier circuit amplifies this signal to provide the horizontal deflection for the CRT.

The internal trigger signals from the vertical plug-in units are connected to the Trigger Selector circuit. This circuit selects the trigger signal which is connected to the horizontal plug-in unit. The Calibrator circuit produces a square-wave output signal with accurate amplitude which can be used to check the calibration of this instrument and the compensation of probes.

The Logic circuit develops control signals for use in other circuits within this instrument and the plug-in units. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and 7603 control settings. The CRT circuit produces the voltages and contains the controls necessary for operation of the cathode-ray tube. It also contains the Z-Axis Amplifier which provides the drive signal to control the intensity level of the CRT display.

The power necessary for the operation of this instrument is produced by the Low-Voltage Power Supply circuit. These voltages are connected to all circuits within the instrument.

CIRCUIT OPERATION

This section provides a detailed description of the electrical operation and relationship of the circuits in the 7603. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits which are commonly used in the electronics industry are not described in detail. If more information is desired on these commonly used circuits, refer to the following textbooks (also see books under Logic Fundamentals):

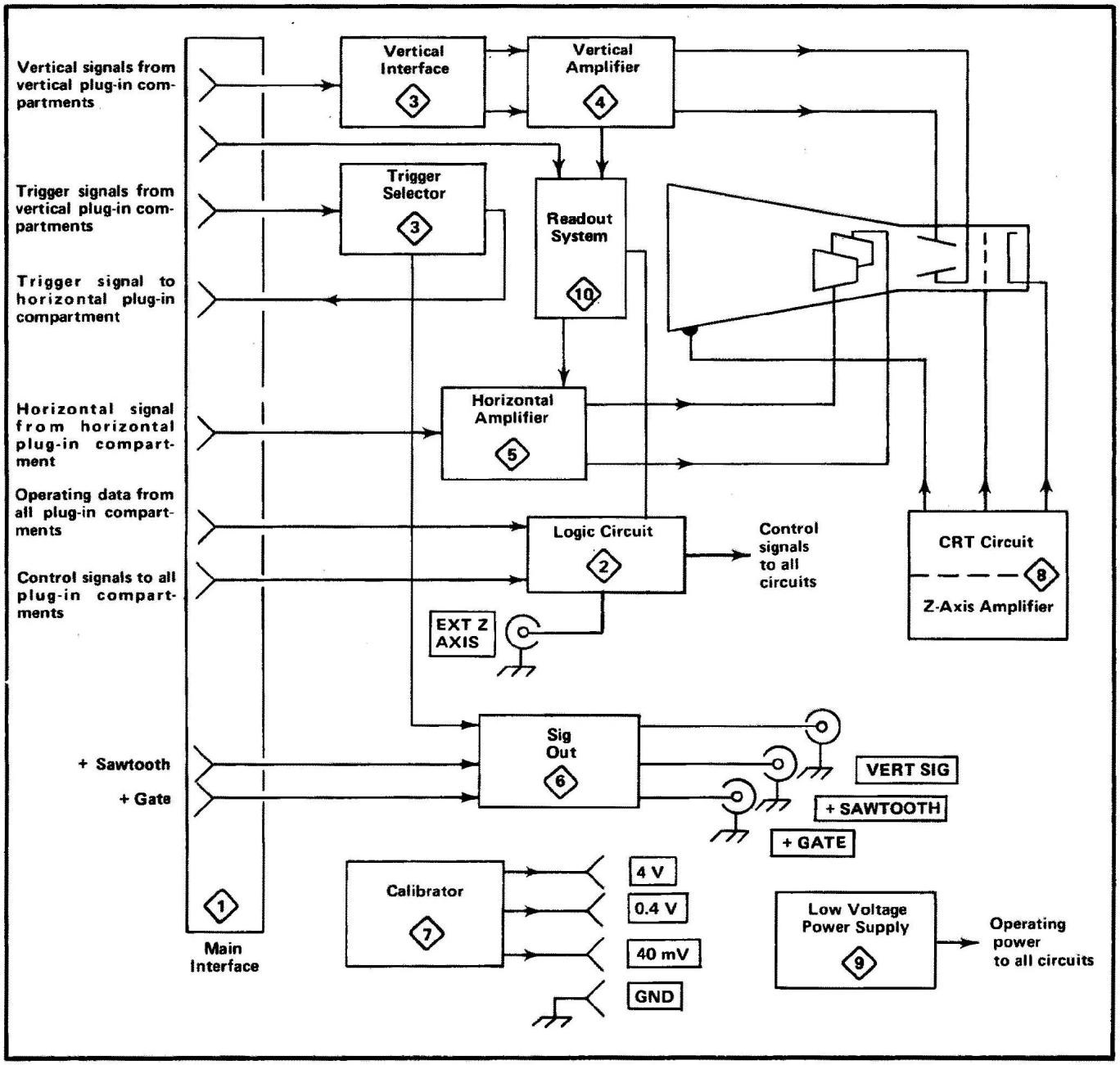


Fig. 4-1. Basic block diagram of 7603 Oscilloscope.

Phillip Cutler, "Semiconductor Circuit Analysis", McGraw-Hill, New York, 1964.

Lloyd P. Hunter (Ed.), "Handbook of Semiconductor Electronics", second edition, McGraw-Hill, New York, 1962.

Jacob Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, 1965.

The following circuit analysis is written around the detailed block diagrams which are given for each major circuit. These detailed block diagrams give the names of the individual stages within the major circuits and show how they are connected together to form the major circuit. The block diagrams also show the inputs and outputs for each circuit and the relationship of the external controls and connectors to the individual stages. The circuit diagrams from which the detailed block diagrams are derived are shown in the Diagrams section.

NOTE

All references to direction of current in this manual are in terms of conventional current; i.e., from plus to minus.

LOGIC FUNDAMENTALS

Digital logic techniques are used to perform many functions within this instrument. The function and operation of the logic circuits are described using logic symbology and terminology. This portion of the manual is provided to aid in the understanding of these symbols and terms. The following information is a basic introduction to logic concepts, not a comprehensive discussion of the subject. For further information on binary number systems and the associated Boolean Algebra concepts, the derivation of logic functions, a more detailed analysis of digital logic, etc., refer to the following textbooks:

Robert C. Baron and Albert T. Piccirilli, "Digital Logic and Computer Operation", McGraw-Hill, New York, 1967.

Thomas C. Bartee, "Digital Computer Fundamentals", McGraw-Hill, New York, 1966.

Yaohan Chu, "Digital Computer Design Fundamentals" McGraw-Hill, New York, 1962.

Joseph Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, Chapters 9 – 11, 1965.

Symbols

The operation of circuits within the 7603 which use digital techniques is described using the graphic symbols set forth in military standard MIL-STD-806B. Table 4-1 provides a basic logic reference for the logic devices used within this instrument. Any deviations from the standard symbology, or devices not defined by this standard will be described in the circuit description for the applicable device.

TABLE 4-1

Basic Logic Reference

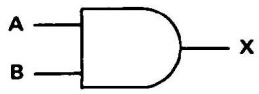
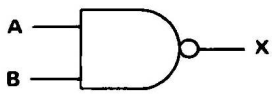
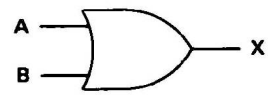
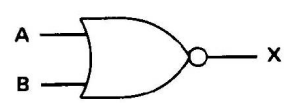
Device	Symbol	Description	Input/Output Table
AND gate		A device with two or more inputs and one output. The output of the AND gate is HI if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI LO HI LO LO HI HI HI
NAND gate		A device with two or more inputs and one output. The output of the NAND gate is LO if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI HI HI LO HI HI HI LO
OR gate		A device with two or more inputs and one output. The output of the OR gate is HI if one or more of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI HI HI LO HI HI HI HI
NOR gate		A device with two or more inputs and one output. The output of the NOR gate is LO if one or more of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI LO HI LO LO HI HI LO

TABLE 4-1 (cont)

Basic Logic Reference

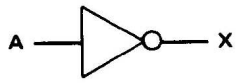
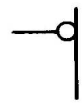
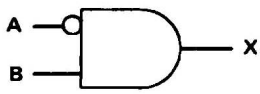
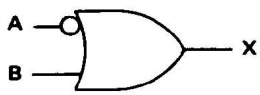
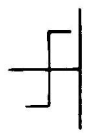
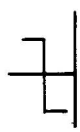
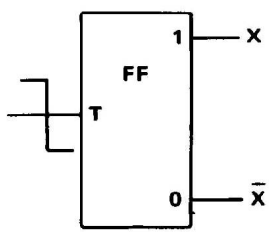
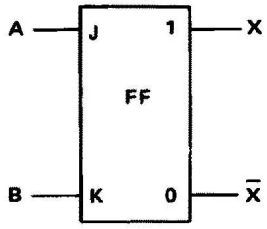
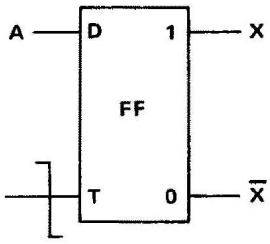
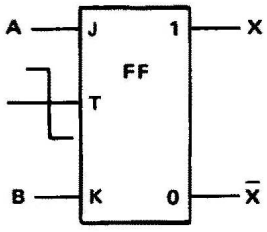
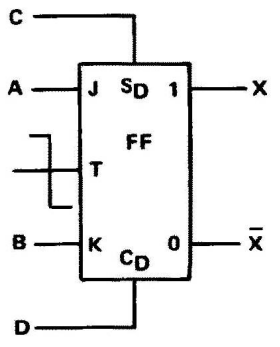
Device	Symbol	Description	Input/Output Table
Inverter		A device with one input and one output. The output state is always opposite to the input state.	Input / Output A: LO, HI X: HI, LO
LO-state indicator		A small circle at the input or output of a symbol indicates that the LO state is the significant state. Absence of the circle indicates that the HI state is the significant state. Two examples follow:	
		AND gate with LO-state indicator at the A input. The output of this gate is HI if and only if the A input is LO and the B input is HI.	Input / Output A: LO, LO, HI, HI B: LO, HI, LO, HI X: LO, HI, LO, LO
		OR gate with LO-state indicator at the A input: The output of this gate is HI if either the A input is LO or the B input is HI.	Input / Output A: LO, LO, HI, HI B: LO, HI, LO, HI X: HI, HI, LO, HI
Edge symbol		Normally superimposed on an input line to a logic symbol. Indicates that this input (usually the trigger input of a flip-flop) responds to the indicated transition of the applied signal.	
			
Triggered (toggle) Flip-Flop		A bistable device with one input and two outputs (either or both outputs may be used). When triggered, the outputs change from one stable state to the other stable state with each trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	Input / Output Condition before trigger pulse: X, $\bar{X}$ Condition after trigger pulse: X, $\bar{X}$ LO, HI, HI, LO HI, LO, LO, HI

TABLE 4-1 (cont)

Basic Logic Reference

Device	Symbol	Description	Input/Output Table
Set-Clear (J-K) Flip-Flop		A bistable device with two inputs and two outputs (either or both outputs may be used). The outputs change state in response to the states at the inputs. The outputs are complementary (i.e., when one output is HI the other is LO).	Input / Output A: LO, LO, HI, HI B: LO, HI, LO, HI X: No change, LO, HI, Changes state $\overline{X}$: HI, LO
D (data) Type Flip-Flop		A bistable device with two inputs and two outputs (either or both outputs may be used). When triggered the state of the "1" output changes to the state at the data (D) input prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity, depending on the device.	Input / Output A: LO, HI X: LO, HI $\overline{X}$: HI, LO Output conditions shown after trigger pulse
Triggered Set-Clear (J-K) Flip-Flop		A bistable device with three or more inputs and two outputs (either or both outputs may be used). When triggered, the outputs change state in response to the states at the inputs prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	Input / Output A: LO, LO, HI, HI B: LO, HI, LO, HI X: No change, LO, HI, Changes state $\overline{X}$: HI, LO Output conditions shown after trigger pulse
Flip-flop with direct inputs (may be applied to all triggered flip-flops)		For devices with direct-set (S_D) or direct-clear (C_D) inputs, the indicated state at either of these inputs over-rides all other inputs (including trigger) to set the outputs to the states shown in the input/output table.	Input / Output A: 1, Φ, Φ, Φ B: 1, Φ, Φ, Φ C: LO, LO, HI, HI D: LO, HI, LO, HI X: No change[1], LO, HI, Undefined $\overline{X}$: HI, LO Φ = Has no effect in this case [1]Output state determined by conditions at triggered inputs

NOTE

Logic symbols used on the diagrams depict the logic function and may differ from the manufacturer's data.

Logic Polarity

All logic functions are described using the positive logic. Positive logic is a system of notation where the more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false or 0-state. The HI-LO method of notation is used in this logic description. The specific voltages which constitute a HI or LO state vary between individual devices.

NOTE

The HI-LO logic notation can be conveniently converted to 1-0 notation by disregarding the first letter of each step. Thus:

HI = 1

LO = 0

Wherever possible, the input and output lines are named to indicate the functions that they perform when at the HI (true) state. For example, the line labeled, "Display B Command" means that the B Time-Base unit will be displayed when this line is HI or true. Likewise, the line labeled "X-Compensation Inhibit" means that the X-Compensation function is inhibited or disabled when this line is HI.

Input/Output Tables

Input/output (truth) tables are used in conjunction with the logic diagrams to show the input combinations which are of importance to a particular function, along with the resultant output conditions. This table may be given either for an individual device or for a complete logic stage. For examples of input/output tables for individual devices, see Table 4-1.

Non-Digital Devices

It should be noted that not all of the integrated circuit devices in this instrument are digital logic devices. The function of non-digital devices will be described individually using operating waveforms or other techniques to illustrate their function.

MAIN INTERFACE

Diagram 1 shows the plug-in interface and the interconnections between the plug-in compartments, circuit boards, etc. of this instrument.

LOGIC CIRCUIT

The Logic Circuit develops control signals for use in other circuits within this instrument and in the associated plug-in units. These output signals automatically determine the correct instrument operation in relation to the plug-in installed and/or selected, plug-in control settings, and the 7603 control settings. A schematic of this circuit is shown on diagram 2 at the rear of this manual.

Logic Block Diagram

A block diagram of the Logic Circuit is shown in Fig. 4-2. This diagram shows the source of the input control signals, the output signals produced by this circuit, and the basic interconnections between blocks. The interconnections shown are intended only to indicate inter-relation between blocks and do not indicate a direct connection or that only a single connection is made between the given blocks. Details of the inter-relationship between stages within this circuit are given in the circuit description which follows.

The operation of each of these stages is discussed relating the input signals and/or levels to the output, with consideration given to the various modes of operation that may affect the stage. A logic diagram is also provided where applicable. These diagrams are not discussed in detail, but are provided to aid in relating the function performed by a given stage to standard logic techniques. It should be noted that these logic diagrams are not an exact representation of the circuit but are only a logic diagram of the function performed by the stage. An input/output table is given, where applicable, for use along with this circuit description and logic diagram. These input/output tables document the combination of input conditions which are of importance to perform the prescribed function of an individual stage.

Z-Axis Logic

The Z-Axis Logic stage produces an output current which sets the intensity of the display on the CRT. The level of this output current is determined by the setting of the front-panel INTENSITY control, an external signal from the rear panel EXT Z AXIS input connector, or signals from the plug-in compartments. The Vertical Chopped Blanking from U55 is applied to this stage to blank the CRT display during vertical trace switching. The Intensity Limit input from the horizontal plug-in compartment provides protection for the CRT phosphor at slow sweep rates.

The Z-Axis Logic stage consists of transistor 108, dual-transistor Q90 and integrated circuit U99, which is a five-transistor array. A simplified schematic of the Z-Axis

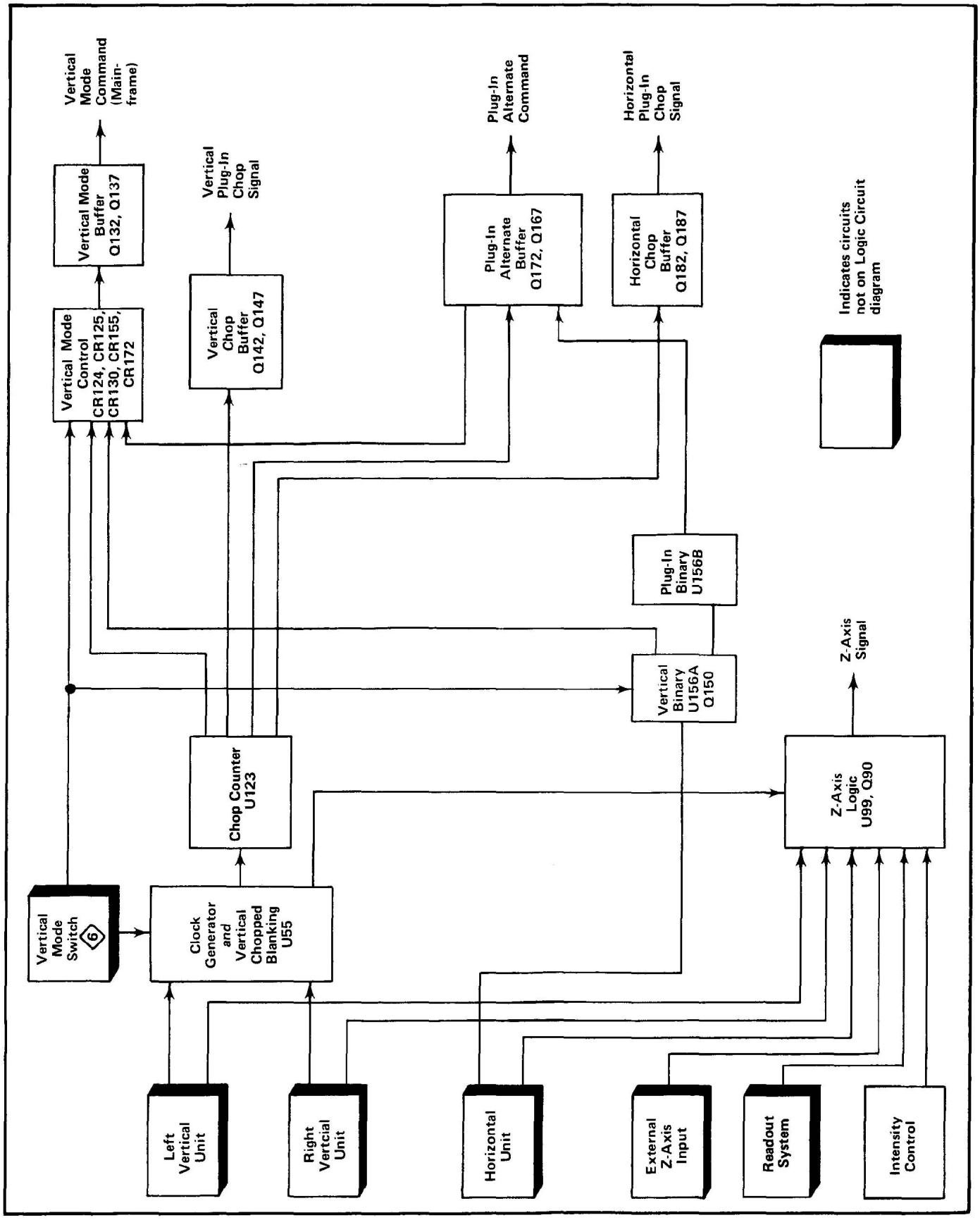


Fig. 4-2. Block diagram of Logic circuit.

Logic stage is shown in Fig. 4-3. Only the components essential to operation of this stage are shown in this simplified schematic.

Transistor U99C is connected in the common-base configuration to provide the output for this stage. The collector load for U99C is provided by the Z-Axis Amplifier in the CRT Circuit. Transistors U99D and U99E provide a current-limiting action for this stage. The collector current of U99D, represented by I_t, is the maximum amount of current that can flow in the circuit. The amount of this current is determined by the relationship between the Intensity Limit and Vertical Chopped Blanking. When both of these inputs are HI the collector current of U99D, I_t, is maximum. This maximum level of I_t is determined by current I_1 in the base circuit of U99D established by networks R76-R77 and R62-R63 into R110 and the collector of U99E. During Vertical Chopped Blanking, the respective input level goes LO. This shunts the current I_1 from the base of U99D so the collector current of U99D, I_t, drops to minimum to blank the CRT display during vertical trace switching.

The Intensity Limit function limits the output current of this stage to protect the CRT phosphor whenever the time-base unit is set to a slow sweep rate. For conditions that do not require limiting, quiescent current is added to I_1 from the +15-volt supply through R76-R77. When the time-base unit is set to a sweep rate which requires intensity

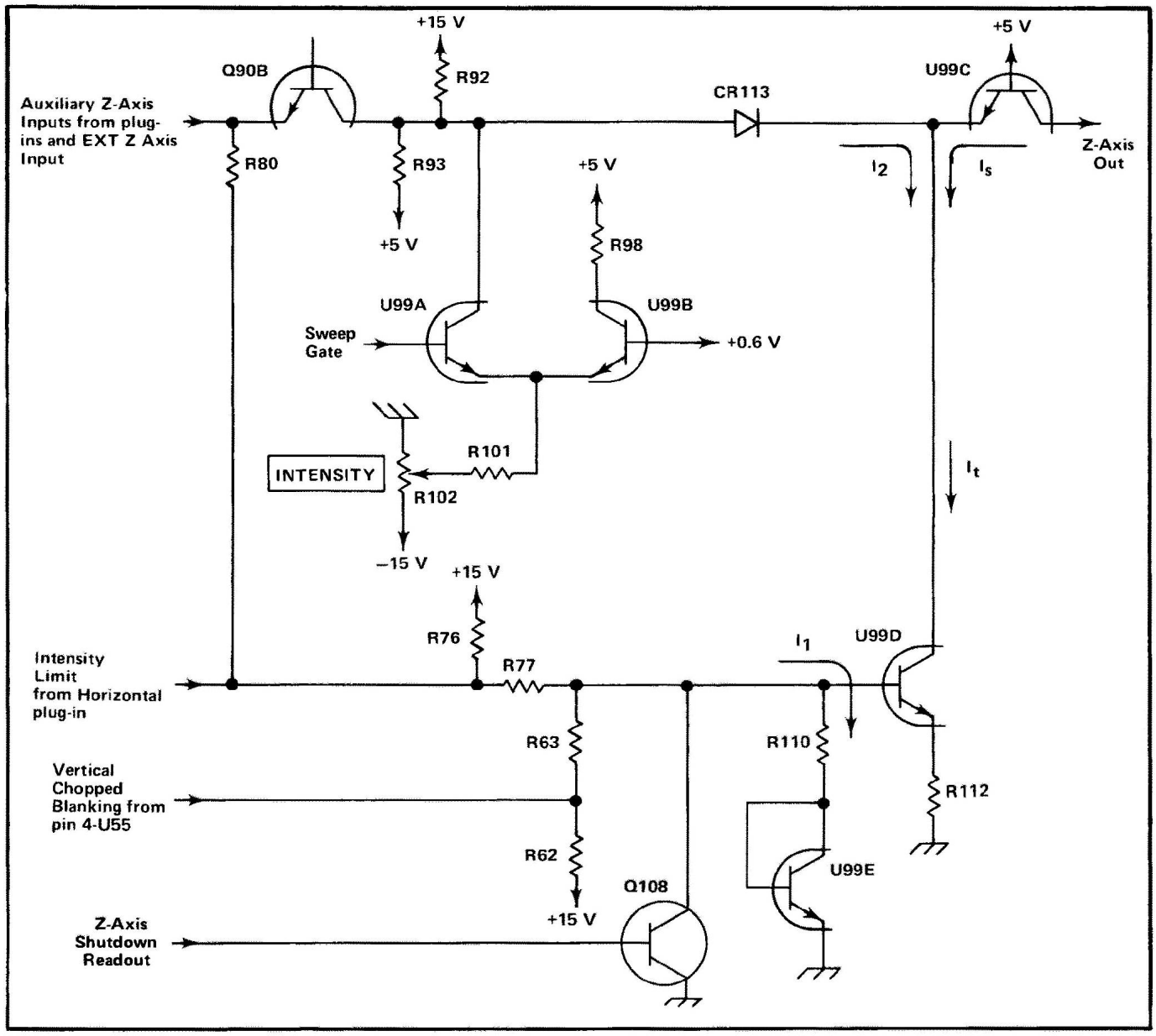


Fig. 4-3. Simplified schematic of Z-Axis Logic stage.

limiting, the Intensity Limit input goes to ground level in the plug-in unit. This reduces the level of I_1 at the base of U99D and therefore reduces I_t and the output current to reduce the intensity of the display. At the same time, the ground level from the Intensity Limit input is connected to the emitter of Q90B through R80. This connection limits the maximum level to which the INTENSITY control can be set to aid in obtaining intensity limiting at slow sweep rates.

The collector current of U99D is made up of two currents; I_s and I_2 is determined by divider R92 and R93. When the Sweep Gate level at the base of U99A is LO (no sweep in progress), I_2 is at its maximum level so that I_s is minimum to provide minimum intensity of the display ($I_s + I_2$ is always equal to I_t). During sweep time, the Sweep Gate level at the base of U99A as established by INTENSITY control R102 determines the output current. As the INTENSITY control is turned toward maximum, the level of I_2 decreases. This allows I_s to increase to produce a brighter display. The Auxiliary Z-Axis Inputs from the plug-in compartments and the intensity modulating signal from the EXT Z-AXIS input connector are connected to the emitter of Q90B. These signals modulate the level of I_2 to, in turn, modulate the intensity of the display.

When readout information is to be displayed on the CRT, the Z-Axis shutdown goes LO. This forward biases Q180, and it saturates, shunting I_1, through Q108 to ground. This reduces the output current to zero during the readout time.

Clock Generator

One half of integrated circuit U55 along with the external components shown in Fig. 4-4A make up the Clock Generator stage. R1, Q1, Q2, and Q3 represent an equivalent circuit contained within U55A. This circuit along with discrete components C59, R56, R57, and R59 comprise a two-megahertz free-running oscillator to provide a timing signal (clock) for mainframe vertical and plug-in chopping.

The stage operates as follows: Assume that Q2 is conducting and Q1 is off. The collector current of Q2 produces a voltage drop across R1 which holds Q1 off. This negative level at the collector of Q2 is also connected to pin 14 through Q3 (see waveforms in Fig. 4-4B at time T_0). Since there is no current through Q1, C59 begins to charge towards −15 volts through R56-R57. The emitter of Q1 goes negative as C59 charges until it reaches a level about 0.6 volt more negative than the level at its base. Then, Q1 is forward biased and its emitter rapidly rises positive. Since

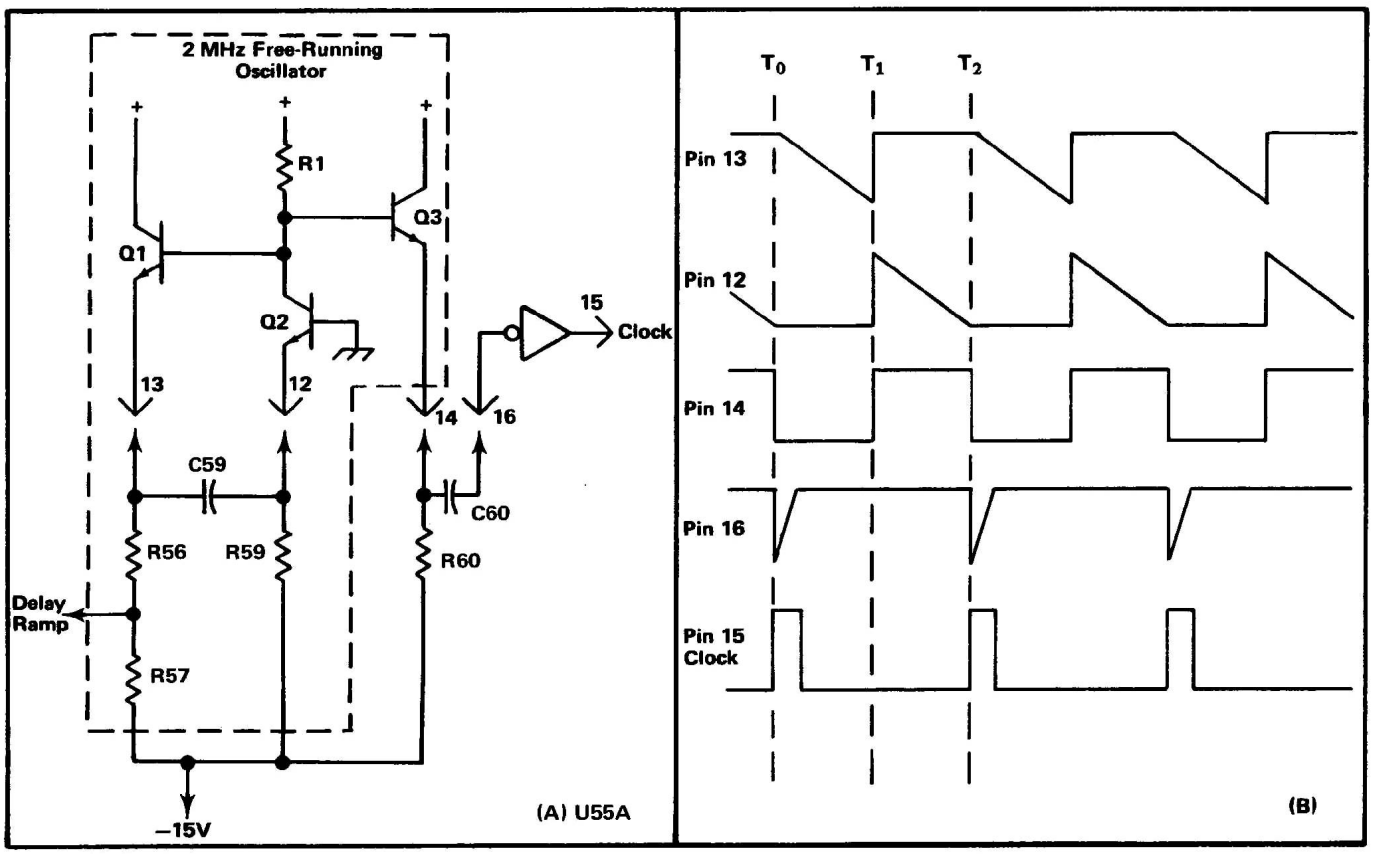


Fig. 4-4. (A) Diagram of Clock Generator stage. (B) Idealized waveforms from Clock Generator stage.

C59 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q1 pulls the emitter of Q2 positive also, to reverse-bias it. With Q2 reverse biased, its collector rises positive to produce a positive output level at pin 14 (see time T_1 on the waveforms).

Now, conditions are reversed. Since Q2 is reverse biased, there is no current through it. Therefore, C59 can begin to discharge through R59. The emitter level of Q2 follows the discharge of C59 until it reaches a level about 0.6 volt more negative than its base. Then Q2 is forward biased and its collector drops negative to reverse-bias Q1. The level at pin 14 drops negative also, to complete the cycle. Once again, C59 begins to charge through R56-R57 to start the second cycle.

Two outputs are provided from this oscillator. The Delay Ramp signal from the junction of R56-R57 is connected to the Vertical Chopped Blanking stage. This signal has the same waveshape as shown by the waveform at pin 13, with its slope determined by the divider ratio between R56-R57. A square-wave output is provided at pin 14. The frequency of this square wave is determined by the RC relationship between C59 and R1. The duty cycle is determined by the ratio of R56-R57 to R59.

The square wave at pin 14 is connected to pin 16 through C60. C60, along with the internal resistance of U55A, differentiates the square wave at pin 14 to produce a negative-going pulse coincident with the falling edge of the square wave (positive-going pulse coincident with rising edge has no effect on circuit operation). This negative-going pulse is connected to pin 15 through an inverter-shaper which is also part of U55A. The output at pin 15 is a positive-going Clock pulse at a repetition rate of about two megahertz.

Vertical Chopped Blanking

The Vertical Chopped Blanking stage is made up of the remaining half of integrated circuit U55B, Fig. 4-5A. This stage determines if Vertical Chopped Blanking pulses are required, based upon the operating mode of the vertical system or the plug-in units (dual trace units only). Vertical Chopped Blanking pulses are produced if: (1) VERT MODE switch is set to CHOP; (2) dual-trace vertical unit is operating in the chopped mode and that unit is being displayed; (3) dual-trace vertical unit is operating in the chopped mode with the VERT MODE switch set to ADD. The repetition rate of the negative-going Vertical Chopped Blanking pulse output at pin 4 is always two megahertz as determined by the Clock Generator stage.

The Delay Ramp signal from the Clock Generator stage determines the repetition rate and pulse width of the Vertical Chopped Blanking pulses. The Delay Ramp applied to pin 10 starts to go negative from a level of about +1.1 volts coincident with the leading edge of the Clock pulse (see waveforms in Fig. 4-5B). This results in a HI quiescent condition for the Vertical Chopped Blanking pulse. The slope of the negative-going Delay Ramp is determined by the Clock Generator stage. As it reaches a level slightly negative from ground, the Vertical Chopped Blanking pulse output level changes to the LO state. This signal remains LO until the Delay Ramp goes HI again. Notice the delay between the leading edge of the Clock pulse generated by U55A and the leading edge of the Vertical Chopped Blanking pulses (see Fig. 4-5B). The amount of delay between the leading edges of these pulses is determined by the slope of the Delay Ramp applied to pin 10. This delay is necessary due to the delay line in the vertical deflection system. Otherwise, the trace blanking resulting from the Vertical Chopped Blanking pulse would not coincide with the switching between the displayed traces. The duty cycle of the square wave produced in the Clock Generator stage determines the pulse width of the Vertical Chopped Blanking pulses (see Clock Generator discussion for more information).

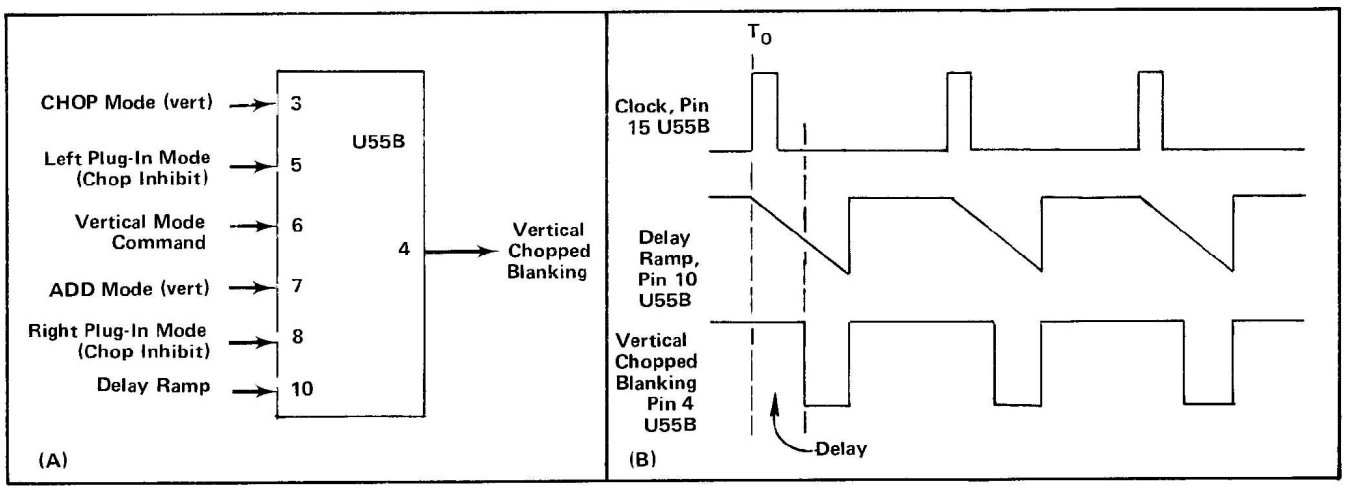


Fig. 4-5. (A) Input and output pins for Vertical Chopped Blanking stage, (B) Idealized waveforms for Vertical Chopped Blanking stage.

Whenever this instrument is turned on, the Vertical Chopped Blanking pulses are being produced at a two-megahertz rate. However, these pulses are available as an output at pin 4 only when the remaining inputs to U55B are at the correct levels. The following discussions give the operating conditions which produce Vertical Chopped Blanking pulses to blank the CRT during vertical trace switching. Fig. 4-5A identifies the functions of the pins of U55B.

1. CHOP VERTICAL MODE

When the VERT MODE switch is set to CHOP, Vertical Chopped Blanking pulses are available at pin 4 at all times. The input conditions necessary are:

PIN 3 HI—VERT MODE switch set to CHOP.

Pin 7 LO—VERT MODE switch set to any position except ADD.

Pin 10 LO—Delay Ramp more negative than about 0 volts.

2. LEFT VERTICAL UNIT SET FOR CHOPPED OPERATION

If the Left Vertical unit is set for chopped operation, the setting of the VERT MODE switch determines whether the Vertical Chopped Blanking pulses are available. If the VERT MODE switch is set to the CHOP position, conditions are as described in No. 1 above. Operation in the ADD position of the VERT MODE switch is given later. For the LEFT position of the VERT MODE switch, or when the left vertical unit is to be displayed in the ALT mode, Vertical Chopped Blanking pulses are available at all times (two-megahertz rate). The input conditions are:

Pin 3 LO—VERT MODE switch set to any position except CHOP.

Pin 5 LO—Left vertical unit set to chopped mode.

Pin 6 LO—Left vertical unit to be displayed (Vertical Mode Command LO).

Pin 7 LO—VERT MODE switch set to any position except ADD.

Pin 10 LO—Delay Ramp more negative than about 0 volts.

Notice that the Vertical Mode Command at pin 6 must be LO for output pulses to be available at pin 4. This means that when the VERT MODE switch is set to ALT, Vertical Chopped Blanking pulses are produced only during the time that the left vertical unit is to be displayed (unless right vertical unit is also set for chopped operation).

3. RIGHT VERTICAL UNIT SET FOR CHOPPED OPERATION

If the right vertical unit is set for chopped mode, operation is the same as described previously for the left vertical unit except that Vertical Chopped Blanking pulses are produced when the VERT MODE switch is set to RIGHT or when the Vertical Mode Command is HI in the ALT mode. The input conditions are:

Pin 3 LO—VERT MODE switch set to any position except CHOP.

Pin 6 HI—Right vertical unit to be displayed (Vertical Mode Command HI).

Pin 7 LO—VERT MODE switch set to any position except ADD.

Pin 8 LO—Right vertical unit set to chopped mode.

Pin 10 LO—Delay Ramp more negative than about 0 volts.

4. ADD VERTICAL MODE

When the VERT MODE switch is in the ADD position and either or both of the vertical units are operating in the chopped mode, Vertical Chopped Blanking pulses must be available to block out the transition between traces of the vertical units. The input conditions are:

Pin 3 LO—VERT MODE switch set to any position except CHOP.

Pin 5 LO—Left vertical unit set to chopped mode (can be HI if pin 8 is LO).

Pin 7 HI—VERT MODE switch set to ADD.

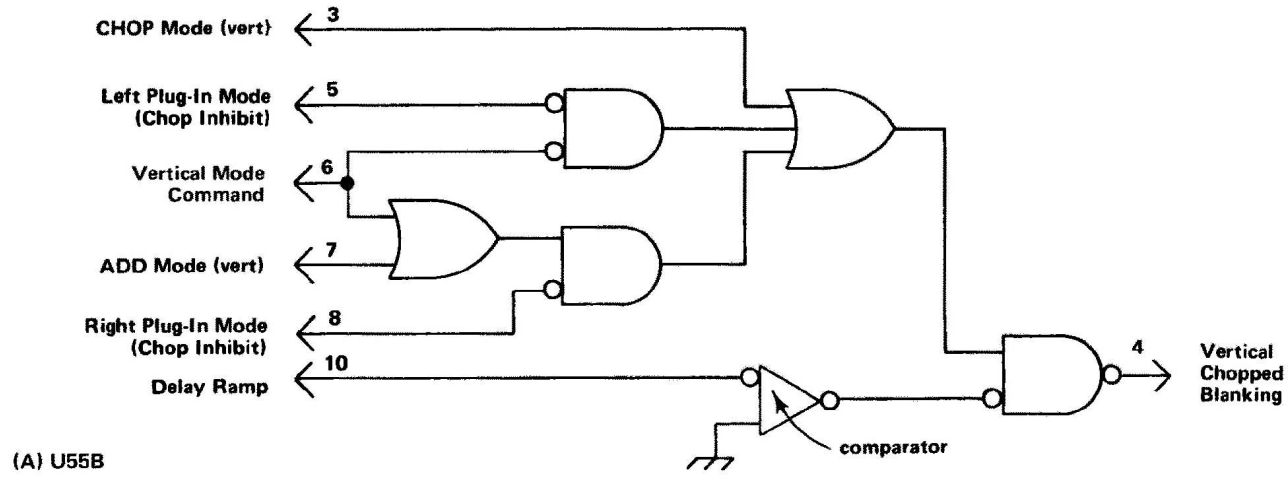
Pin 8 LO—Right vertical unit set to chopped mode (can be HI if pin 5 is LO).

Pin 10 LO—Delay Ramp more negative than about 0 volt.

Fig. 4-6A shows a logic diagram of the Vertical Chopped Blanking stage. Notice the comparator block on this diagram (one input connected to pin 10). The output of this comparator is determined by the relationship between the levels at its inputs. If pin 10 is more positive (HI) than the grounded input, the output is HI also; if it is more negative (LO), the output is LO. An input/output table for this stage is given in Fig. 4-6B.

Chop Counter

The Chop Counter stage produces the Mainframe Chop Signal and the Vertical Plug-In Chop Signal. The Clock



(A) U55B

(B)

Input						Output	
CHOP Mode (vert) 3	Left Plug-In Mode (Chop Inhibit) 5	Vertical Mode Command 6	Add Mode (vert) 7	Right Plug-In Mode (Chop Inhibit) 8	Delay Ramp 10^1	Vertical Chopped Blanking 4^2	Conditions
HI	Φ	Φ	LO	Φ	LO	LO	CHOP Mode (vert)
LO	LO	LO	LO	Φ	LO	LO	Left Plug-in Chopped
LO	Φ	HI	LO	LO	LO	LO	Right Plug-in Chopped
LO	LO[3]	Φ	HI	LO[3]	LO	LO	ADD Mode, Left or Right Plug-in Chopped
All other combinations						HI	No Vertical Chopped Blanking pulses at output.

Φ = Has no effect in this case.

[1] Ramp signal; considered LO when more negative than about zero volts.

[2] Negative-going pulse at two megahertz rate.

[3] Pin 5 can be HI and not affect operation if pin 8 is LO, and vice versa.

Fig. 4-6. (A) Logic diagram for Vertical Chopped Blanking stage, (B) Table of input/output combinations for Vertical Chopped Blanking stage.

pulse produced by the Clock Generator stage provides the timing signal for this stage. A logic diagram of the Chop Counter, identifying the inputs and outputs, is shown in Fig. 4-7.

The Chop Counter stage consists of integrated circuit U123, a dual D-type flip-flop with direct-set, direct-clear inputs (see Table 4-1 for operation of D-type flip-flip). As connected in this circuit, these D-type flip-flops operate as triggered (toggle) flip-flops.

The two-megahertz clock pulses from the Clock Generator stage are connected to the trigger (T) input of U123B. As connected, U123B changes output states with each positive-going Clock pulse, and the signal at its "1" output is a square wave which switches between the HI and LO levels at a one-megahertz rate. This signal is connected to the Vertical Mode Control stage to provide the Vertical Mainframe Chop Signal. It is also connected to the trigger input of U123A. U123A also changes output states with each positive-going pulse at its trigger input to produce a 500 kilohertz square wave at its "1" output. The output from U123A provides the Vertical Plug-In Chop Signal to

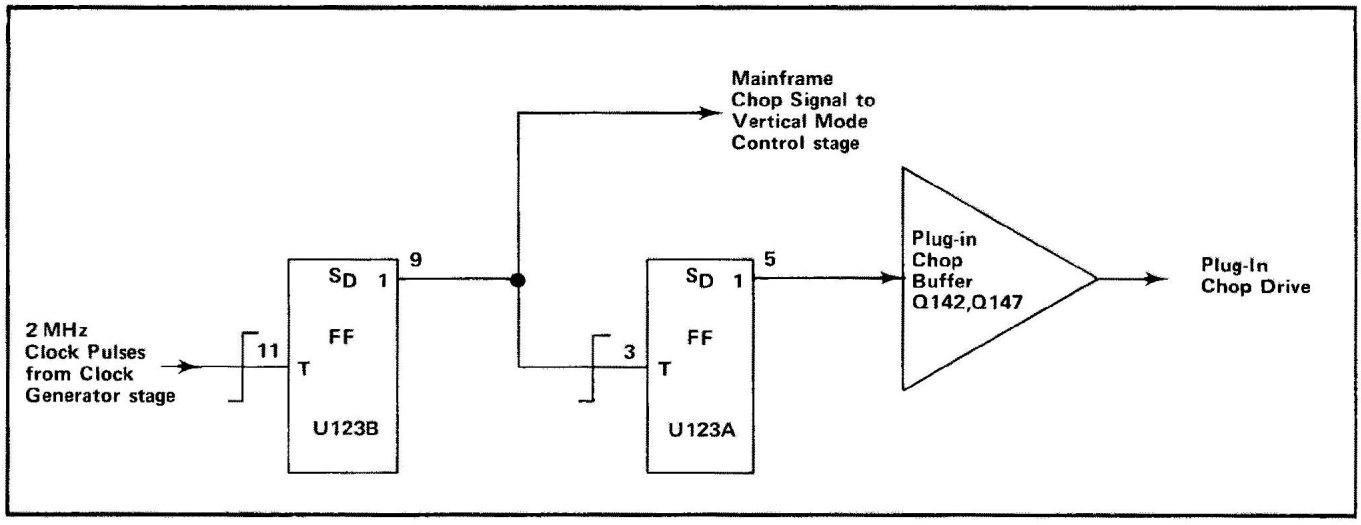


Fig. 4-7. Detailed logic diagram of Chop Counter stage.

the Plug-In Chop Buffer stage. Idealized waveforms showing the timing relationship between the input and output signals for this stage are shown in Fig. 4-8.

Vertical Mode Control

The Vertical Mode Control stage is made up of discrete components CR124-CR125, CR126, CR130-CR155, CR172, and buffer amplifier Q132-Q137. These components develop the Mainframe Vertical Mode Command which is connected to the Main Interface circuit (vertical plug-in compartments and trigger selection circuitry) and the Vertical Interface circuit to indicate which vertical unit is to be displayed. When this output level is HI, the right vertical unit is displayed and when it is LO, the left vertical unit is displayed.

The VERT MODE switch located on diagram 7 provides control levels for this stage. This switch provides a HI level on only one of four output lines to indicate the selected vertical mode; the remaining lines are LO. The fifth mode, LEFT, is indicated when all four output lines are LO. Operation of this stage in all positions of the VERT MODE switch is as follows:

Right. When the VERT MODE switch is set to RIGHT, a HI level is connected to the Buffer Amplifier through R126 and CR126. The LO level at the anodes of diodes CR125 and CR130 holds them reverse biased. The resultant Vertical Mode Command output from the Vertical Mode Buffer Amplifier is a HI level to indicate that the right vertical unit is to be displayed.

Chop. In the CHOP position of the VERT MODE switch, a HI level is applied to the anodes of diodes CR124-CR125 through R125. Both diodes are forward biased so the Vertical Chop Signal from pin 9 of U123B can pass to the emitter of Q132. This signal switches between the HI and LO levels at a one-megahertz rate and it produces a corresponding Mainframe Vertical Mode Command output at the emitter of Q137. When this output is

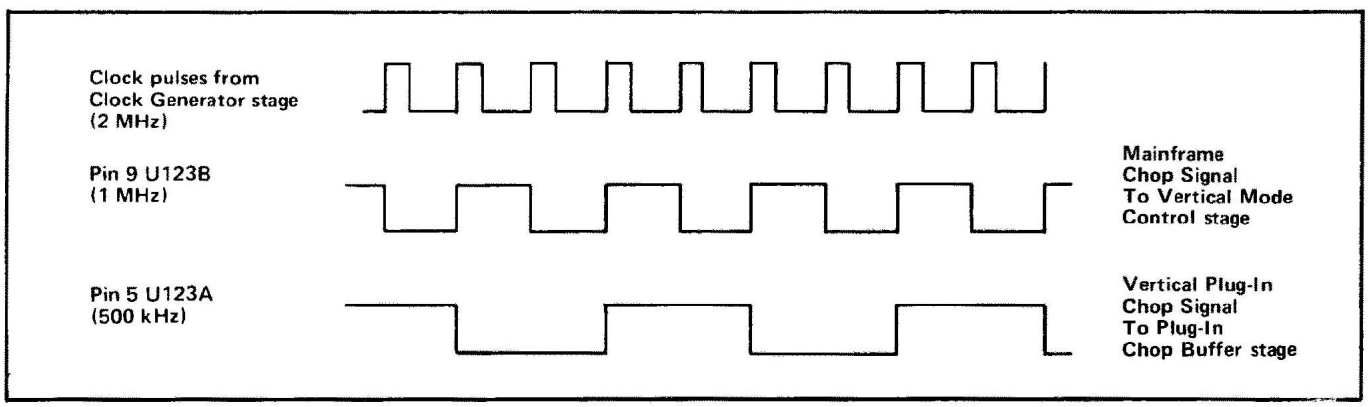


Fig. 4-8. Idealized input and output waveforms for Chop Counter stage.

HI, the right vertical unit is displayed and when it switches to LO, the left vertical unit is displayed.

Alt. In the ALT mode, the VERT MODE switch applies a HI level to the anodes of diodes CR130-CR155 through R130. These diodes are forward biased so the Display Right Command from pin 5 of U156A can pass to the emitter of Q132 to determine the Mainframe Vertical Mode Command level. The Display Right Command switches between its HI and LO levels at a rate determined by the Vertical Binary stage.

Add and Left. The control levels in the ADD and LEFT positions of the VERT MODE switch are not connected to this stage. However, since only the line corresponding to the selected vertical mode can be HI, the RIGHT, CHOP, and ALT lines must remain at their LO level when either LEFT or ADD are selected. Therefore, the emitter of Q132 remains LO to produce a LO Mainframe Vertical Mode Control output level. Final control of LEFT or ADD mode is made by the Vertical Interface circuit.

A logic diagram of the Vertical Mode Control stage is shown in Fig. 4-9. The discrete components which make up each logic function are identified. The gate connected to the input of the Vertical Mode Buffer Amplifier is a phantom-OR gate. A phantom-OR gate performs the OR logic function merely by interconnection of the three inputs.

Vertical Binary

The Vertical Binary stage consists of integrated circuit U156A and transistor Q150. U156A is a D-type flip-flop with direct-set and direct-clear inputs (see Table 4-1 for operating details). The connection between the "0" output and the data (D) input enables this flip-flop to operate in the triggered mode. A logic diagram of the Vertical Binary stage is shown in Fig. 4-10.

The operation of the Vertical Binary stage is controlled by the level of the ALT Mode line from the VERT MODE switch. When this switch is set to ALT, a HI level is connected to the emitter of Q150 through R152. This HI level disables Q150 so its collector remains HI. As a result, Q150 has no effect upon operation of the Vertical Binary stage and the direct-clear input of U156A remains HI so it does not affect the operation of U156A. Therefore, U156A operates as a basic triggered flip-flop which changes output states with each positive-going Sweep Holdoff pulse at the trigger (T) input. The Sweep Holdoff pulse goes positive at the end of each sweep. The signal at the "1" output of U156A switches between the HI and LO level at one-half the rate of the Sweep Holdoff signal from the horizontal plug-in unit. Fig. 4-11 shows the time relationship between the input and output signals for this stage, and gives the resultant display with each signal combination.

For any other position, the emitter of Q150 is pulled LO by the ALT Mode command from the VERT MODE switch. This enables Q150, but it does not change output state unless the level at the "1" output of U156A is HI. Quiescently, the output of Q150 is LO. Therefore, when the positive-going Sweep Hold-off pulse is received at the end of the sweep, the "1" output of U156A goes HI. This activates Q150 and its output goes LO to provide a direct-clear reset to U156A. The "1" output of U156A is reset to its LO level, and Q150 is again disabled so its output returns to the HI level. The stage is now ready for

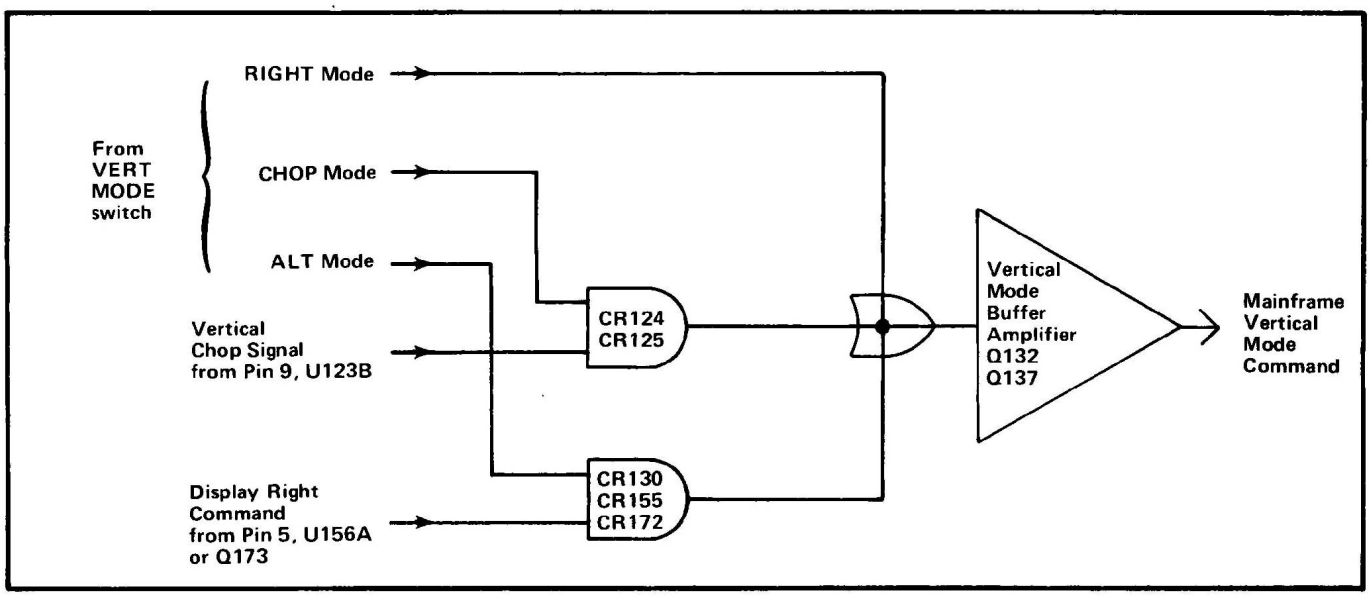


Fig. 4-9. Logic diagram of Vertical Mode Control and Vertical Mode Buffer Amplifier stages.

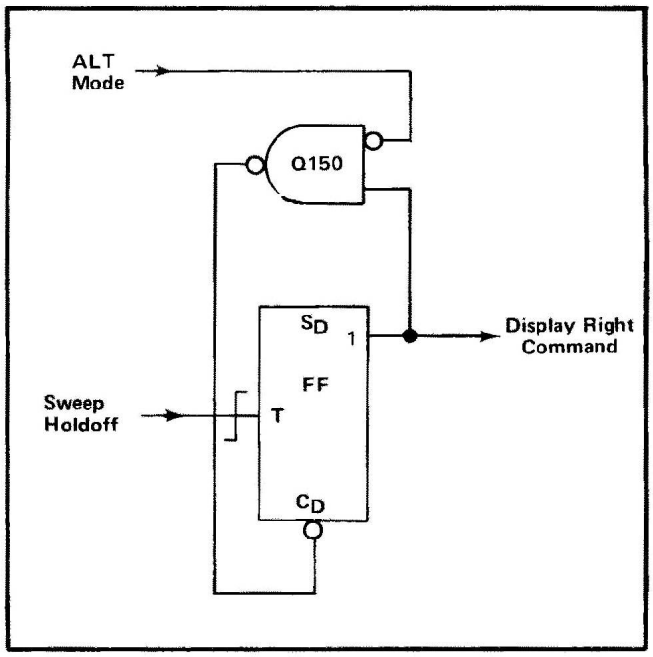


Fig. 4-10. Logic diagram of Vertical Binary stage.

the next positive-going Sweep Hold-off pulse. The action is the same with each pulse, so the signal at the output of this stage is at the same repetition rate as the Sweep Holdoff input. Therefore, this stage is now operating as a divide-by-one counter rather than a divide-by-two counter as described previously. The output under this condition is used only by the Plug-In Binary stage.

Since the Vertical Binary stage can change output states only at the end of each sweep, there will be no Alternate Drive signal for either the mainframe or vertical plug-in units if a sweep is not being produced by the horizontal plug-in unit.

Plug-In Binary

The Plug-In Binary stage consists of U156B, which is connected as a triggered flip-flop with direct-set input. The trigger input for this stage is the Display Right Command from the Vertical Binary stage. When the VERT MODE switch is set to ALT, the repetition rate of the Display Channel 2 Command output of this stage is one-fourth of the Sweep Holdoff input (see waveforms in Fig. 4-11). For any position of the VERT MODE switch except ALT, the repetition rate of the output signal from this stage is one-half of the Sweep Holdoff input. A logic diagram of the Plug-In Binary stage is shown in Fig. 4-12.

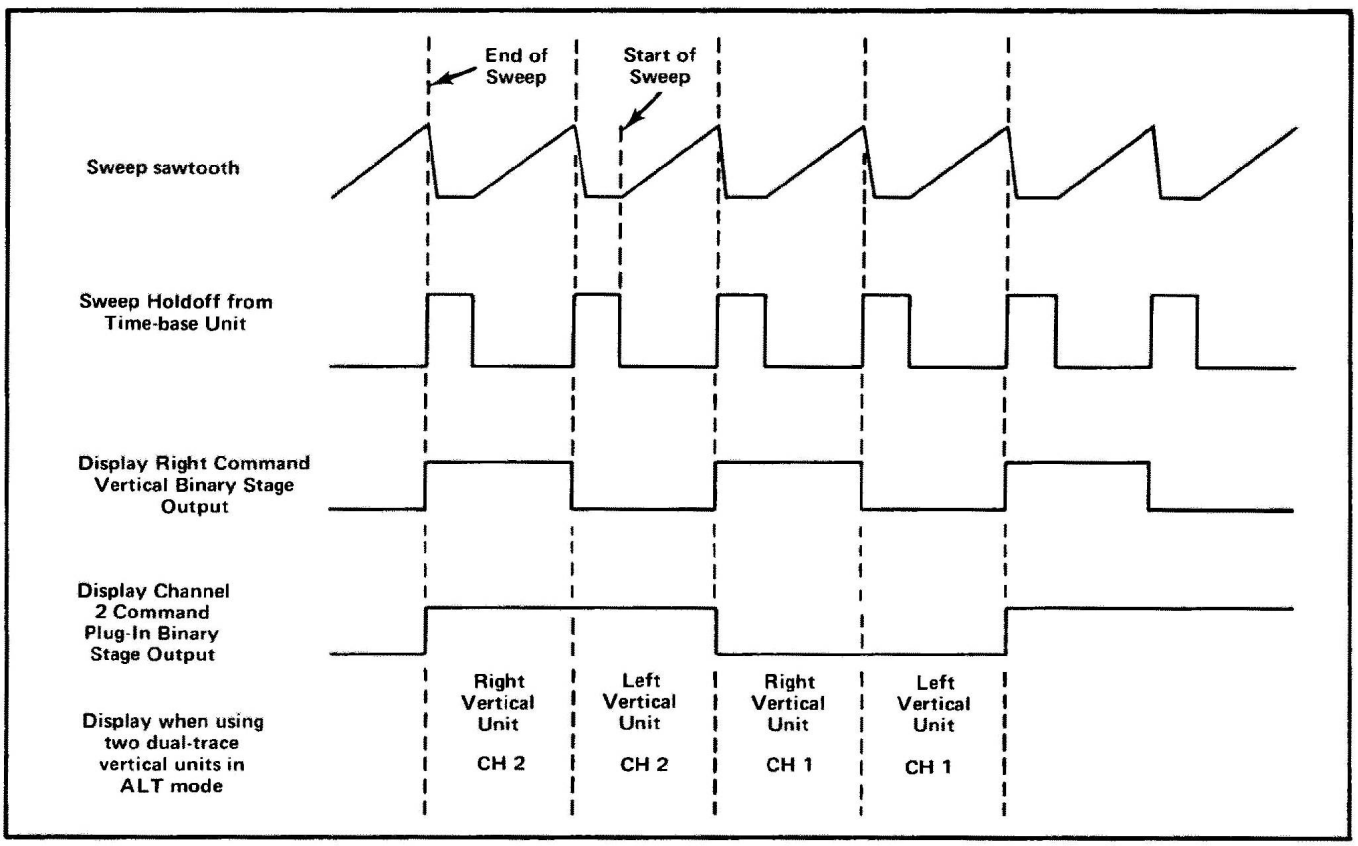


Fig. 4-11. Idealized waveforms showing relationship between input and output waveforms for Vertical Binary and Plug-In Binary stages when operating in ALT mode.

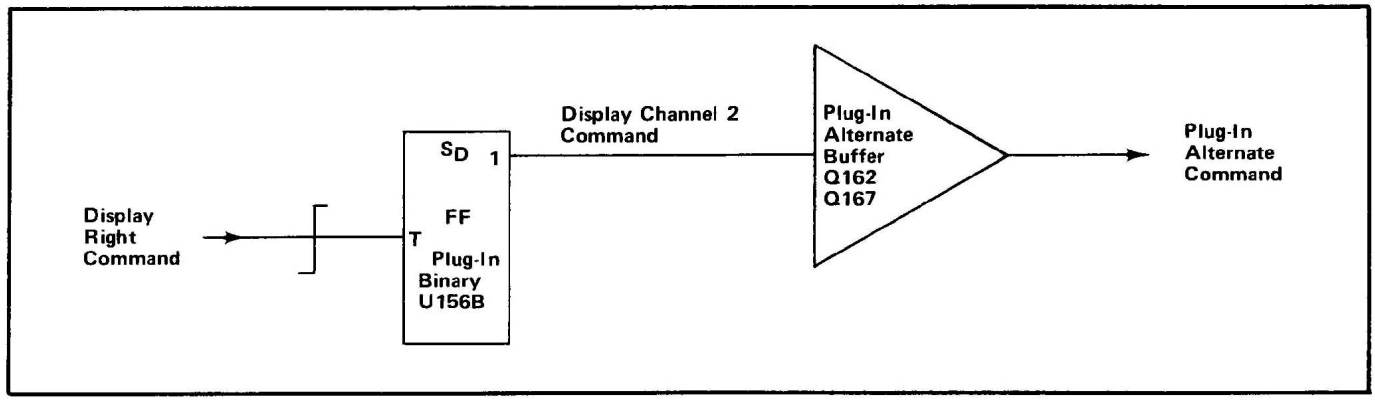


Fig. 4-12. Logic diagram of Plug-In Binary and Plug-In Alternate Buffer stages.

Output Buffers

The output switching commands from the Logic circuit are provided through buffer stages Q142-Q137, Q142-Q147, Q162-Q167, and Q182-Q187. Each of these stages includes a common-base input transistor to provide a low-impedance load for the associated driving stages. The output transistor is connected as an emitter-follower to provide isolation between the Logic circuit and other circuits within this instrument or the plug-in units.

TRIGGER SELECTOR

The Trigger source switch determines which vertical signal is connected to the time-base unit, and which vertical signal, that is provided at VERT SIG/OUT connector on the rear panel. Fig. 4-13 shows a detailed block diagram of the Trigger Selector circuit, along with a simplified diagram of all the circuitry involved in selection of the trigger source. A schematic of the Trigger Selector circuit is shown on diagram 3 at the rear of this manual. Also, see diagrams 6 and 7 for the signal selection circuitry not shown on diagram 3.

Trigger Mode and Add Signals

General. The circuitry shown on the left side of the simplified diagram in Fig. 4-13 determines the operation of the Trigger Channel Switch stage. TRIG SOURCE switch S1011 controls Trigger Channel Switch U324 through Q314. When the TRIG SOURCE switch is set to the VERT MODE position, the setting of the VERT MODE switch determines the trigger selection. In the LEFT or RIGHT positions, the trigger signal is obtained from the indicated vertical unit. The following discussions give detailed operation in each position of the TRIG SOURCE switch.

Vert Mode. In the VERT MODE position of the TRIG SOURCE switch, the setting of the VERT MODE switch determines the operation of the Trigger Channel Switch stage. In the LEFT position of the VERT MODE switch, the base of Q314 is connected to ground through the ALT and RIGHT sections of S1021, CR1021 and CR1026, and S1011. This holds Q314 reverse biased to provide a LO level to pin 4 of U324 (see Fig. 4-14).

When the VERT MODE switch is set to ALT, +5 volts is applied to the base of Q314 through CR1021 and S1011. Q314 is forward biased and its emitter level is determined by the Mainframe Vertical Mode Command signal from the Logic circuit applied to its collector. This signal switches between the HI level (Right Vertical unit to be displayed) and the LO level (Left Vertical unit to be displayed) at the end of each sweep. When the Mainframe Vertical Mode Command is HI, it provides a positive collector voltage to Q314. Q314 is saturated due to CR1021, and its emitter level is very near the collector level. This provides a HI output level to the Trigger Channel Switch stage. As the Mainframe Vertical Mode Command goes LO, the collector supply for Q314 also goes negative. Q314 remains saturated and the output again follows the collector level to supply a LO output level to U324.

For ADD and CHOP vertical mode operation, +5 volts is connected to pin 14 of U324 through CR1023 or CR1024 and S1011. At the same time, the base of Q314 is held LO by the ground connection through the ALT and RIGHT section of S1021 so the level at pin 4 of U324 is LO also (produces an ADD mode in Trigger Channel Switch; see description of this circuit which follows). In the RIGHT position of the VERT MODE switch, +5 volts is connected to the base of Q314 through CR1026 and S1011 to forward-bias the transistor. The Mainframe Vertical Mode Command signal connected to the collector of Q314 is also HI in this mode, and a HI output level is produced at the emitter of Q314.

Left. When the LEFT trigger source is selected, the VERT MODE switch is disconnected from the trigger selector circuitry. Now the ground connection through the

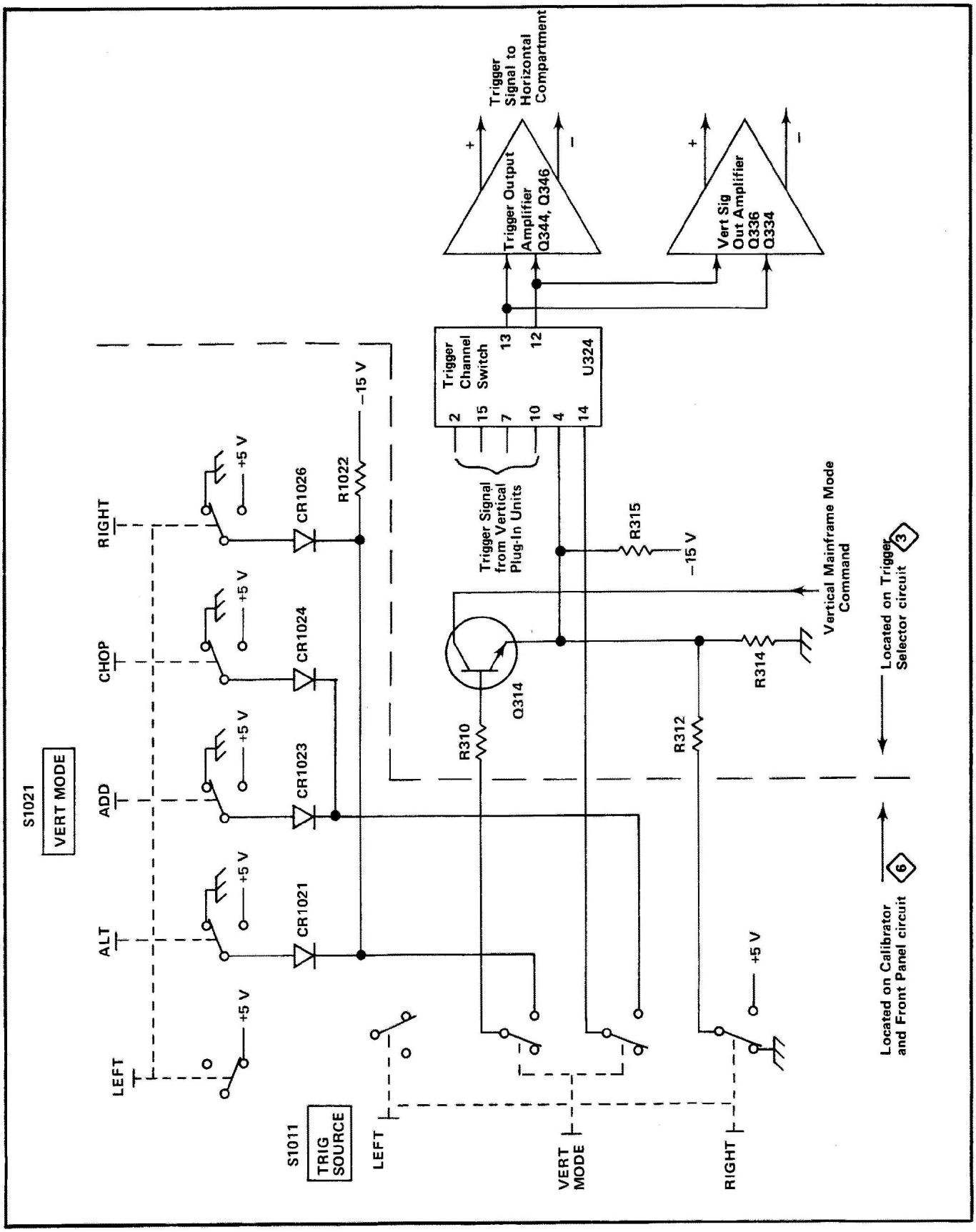
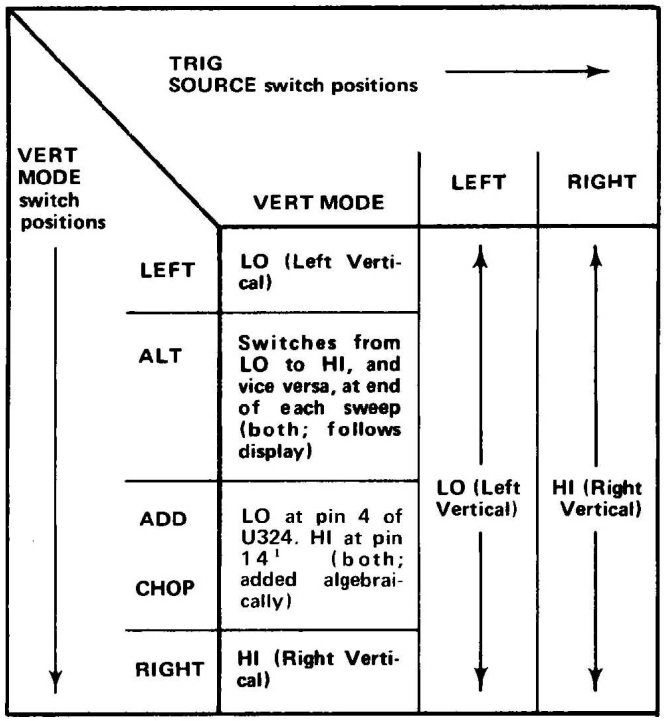


Fig. 4-13. Detailed block diagram of Trigger Selector circuit along with simplified diagram of trigger source selection circuitry.



[1] Pin 14 LO for all other conditions.

Fig. 4-14. Input levels at pin 4 of U324 (source of triggering is shown in parenthesis).

RIGHT section of S1011 establishes a LO output level at the emitter of Q314.

Right. In the RIGHT position of the TRIG SOURCE switch, +5 volts is connected to the emitter of Q314 through S1011 and R312. This produces a HI output level to the Trigger Channel Switch stage.

Trigger Channel Switch

The Trigger Channel Switch stage determines which input signal provides the trigger signal to the horizontal compartment as controlled by the Trigger Mode and ADD signals from the trigger selection circuitry. Refer to diagram 3 during the following discussion.

Resistors R317-R319 establish the input resistance and provide a load for the trigger signal from the right vertical plug-in unit. Resistors R307 and R308, provide the input resistance and load for the left vertical plug-in unit. R321-R323-R324 and R326-R327-R328 establish the operating level of the Trigger Channel Switch; R321-R323 and R326-R328 set the current gain for each channel. This stage is made up primarily of integrated circuit U324. An input/output table for U324 is shown in Fig. 4-15. U324 provides a high impedance differential input for the trigger signal from the left vertical unit at pins 2 and 15, and for the trigger signal from the right vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9, and 16 in all modes. This provides a constant DC bias to the stages which follow as the TRIG SOURCE or the VERT MODE switches are changed.

When the level at pin 4 is LO (see Trigger Mode and ADD Signals discussion and Fig. 4-15), the trigger signal from the left vertical unit passes to the output, while the trigger signal from the right vertical unit is blocked. A HI level at pin 4 connects the trigger signal from the right vertical unit to the output and the trigger signal from the left vertical unit is blocked. For VERT MODE operation in the ALT position of the VERT MODE switch, the level at pin 4 switches between the LO and HI level at a rate determined by the Vertical Binary stage (see Logic circuit description). This action obtains the trigger signal from the left vertical unit when the left vertical unit is being displayed and from the right vertical unit when it is being displayed.

When the level at pin 4 is LO and the level at pin 14 is HI, the trigger signal from both the left and right vertical units passes to the output pins. This condition occurs only when the TRIG SOURCE switch is set to VERT MODE and the VERT MODE switch is set to either ADD or CHOP. Under this operating mode, the trigger output signal is the algebraic sum of the trigger input signals from the left and right vertical units to prevent triggering on the vertical chopping transition, or only on one signal of an added display.

Trigger Output Amplifier

The trigger output at pins 12 and 13 of U324 is connected to the bases of Q344-Q346 to provide the internal trigger signal for the horizontal unit (via the Main Interface circuit). The horizontal unit provides a 50-ohm differential load for this stage. If it is removed from its compartment, the collector load for Q344-Q346 changes and the voltage at their collectors increases. This stage prevents this change from affecting the vertical signal for the Output Signals board. CR341-CR349 clamp the collectors of Q344 and Q346 at about +0.6 volt to prevent these transistors from saturating under this no-load condition.

Vertical Signal Buffer

The trigger output signal at pin 12 and 13 of U324 is also connected to the emitter of a common-base amplifier Q336 and Q334. The output signal at the collector of Q336 and Q334 is connected to the signals out board.

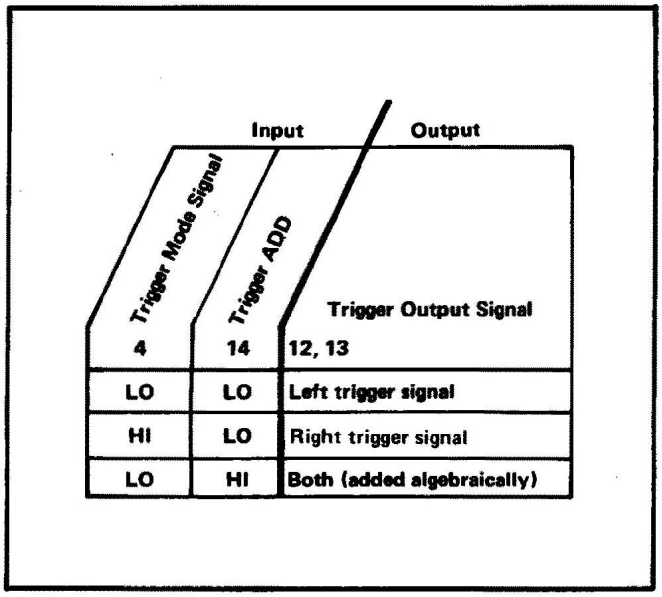


Fig. 4-15. Input/output table for Trigger Channel Switch stage.

VERTICAL INTERFACE

The Vertical Interface circuit selects the vertical deflection signal from the output of the left vertical and/or the right vertical plug-in unit. Fig. 4-16 shows a detailed block diagram of the Vertical Interface circuit. A schematic of this circuit is shown on diagram 3 at the rear of this manual.

Vertical Channel Switch

The Vertical Channel Switch stage determines which input signal provides the vertical signal to the Delay-Line Driver stage as controlled by the Mainframe Vertical Mode Command from the Logic circuit. Resistors R200-R202 and R204-R206 establish the input resistance of this stage and provide a load for the left and right vertical units. Resistors R209-R211-R212 and R216-R218-R219 establish the operating levels for this stage. R209-R212 and R216-R219 set the current gain for each channel. C208-R208 and C215-R215 provide frequency compensation.

This stage is made up primarily of integrated circuit U214, which is the same type as used for the Trigger Channel Switch. An input/output table for U214 is shown in Fig. 4-17. U214 provides a high impedance differential input for the signal from the left vertical unit at pins 2 and 15, and the signal from the right vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal which is connected to the Delay-Line Driver stage through R222-R224. The sum of the DC output currents at

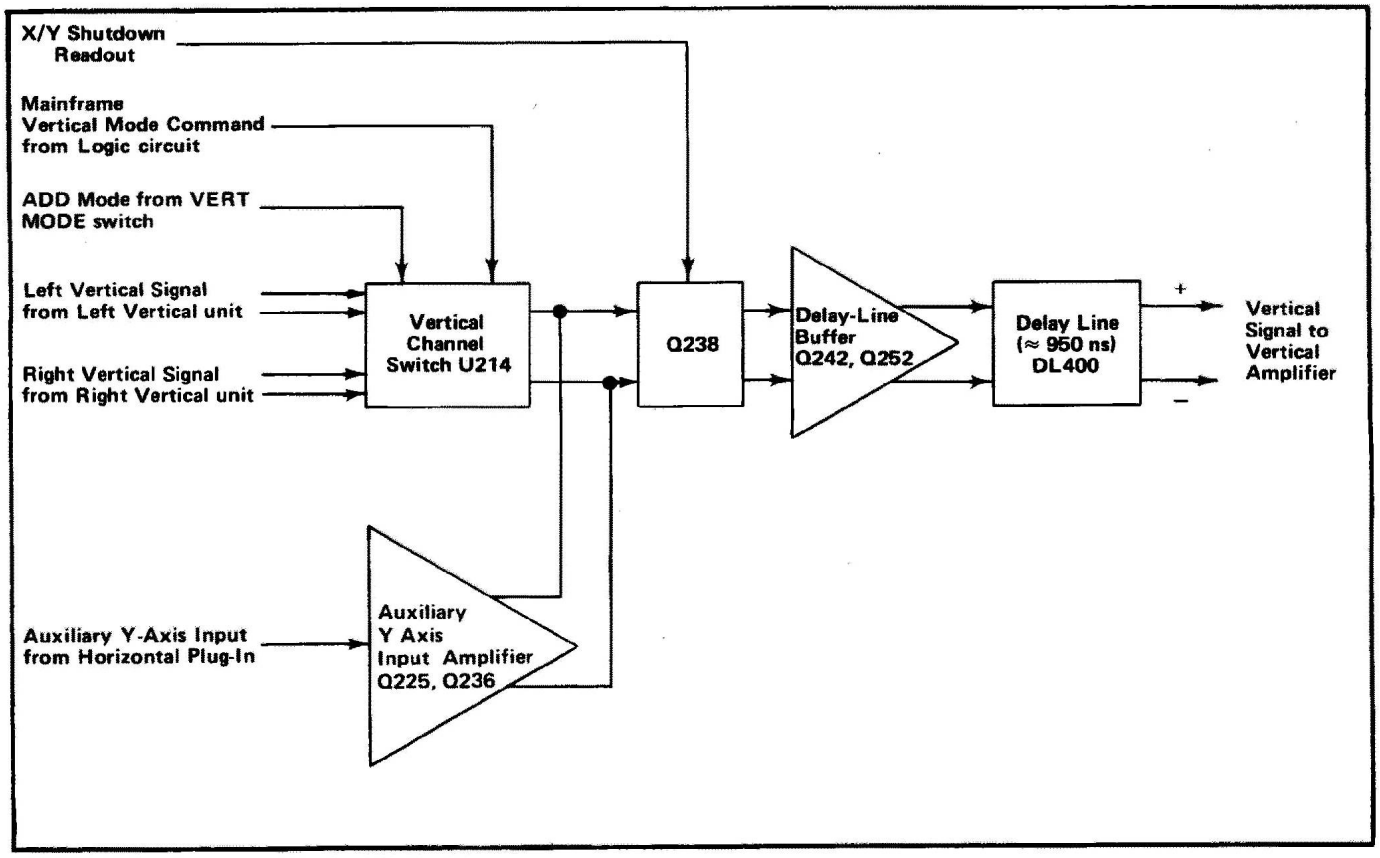


Fig. 4-16. Vertical Interface detailed block diagram.

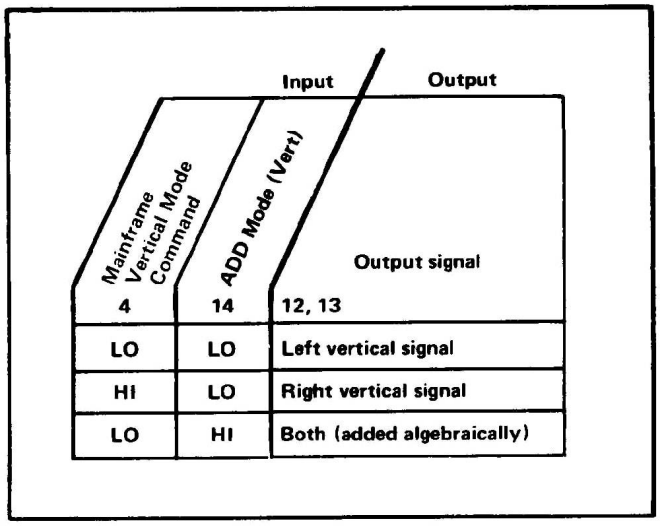


Fig. 4-17. Input/output table for Vertical Channel Switch.

pins 12 and 13 is always equal to the sum of the DC input currents at pins 1, 8, 9, and 16 in all modes. This provides a constant DC bias to the following stage as the VERT MODE switch is changed.

When the VERT MODE swich is set to LEFT, the level at pin 4 is LO. This level allows the signal from the left vertical unit to pass to the output while the signal from the right vertical unit is blocked. In the RIGHT position of the VERT MODE switch, the level at pin 4 is HI. Now, the signal from the right vertical unit is connected to the output while the signal from the left vertical unit is blocked.

When the VERT MODE switch is set to either ALT or CHOP, the Mainframe Vertical Mode Command at pin 4 switches between the LO and HI levels at a rate determined by either the Chop Counter or the Vertical Binary stages (see Logic circuit description). This action allows the signal from the left vertical unit to be displayed when the Mainframe Vertical Mode Command is LO and the signal from the right vertical unit is displayed when the Mainframe Vertical Mode Command is HI. When ADD vertical mode operation is selected, a HI level is applied to pin 14 and the level at pin 4 is LO as determined by the Vertical Mode Control stage in the Logic Circuit. This allows both the right and left vertical signals to pass to the output pins. Now, the signal from both vertical units is algebraically added and the resultant signal determines the vertical deflection.

The X/Y Shutdown signal from the Readout system is applied to pin 6 of U214. It has final control over the output signal from U214. Quiescently, the X/Y Shutdown signal is LO and the signal from the selected vertical can pass to the output pins 12 and 13. However, when the Readout system is ready to display Readout information, the level at pin 6 goes HI. This level blocks the signals from both vertical compartments and there is no output from U214 under this condition. Transistor Q238 will conduct and provide about the same current for the output stage as under normal conditions. This limits any change in positioning that would otherwise occur when the X/Y Shutdown signal from the Readout system is applied.

Auxiliary Y-Axis Input Amplifier

The Auxiliary Y-Axis Input Amplifier accepts an input from horizontal plug-in units having compatible features. Normally, this input is a positioning voltage to offset the display. The single-ended signal connected to the input of this stage is converted to a push-pull signal at the collectors of Q225 and Q236. This signal is connected to the Delay-Line Buffer stage along with the output from the Vertical Channel Switch.

Delay-Line Buffer

The output of the Vertical Channel Switch stage, along with any signal from the Auxiliary Y-Axis Input Amplifier, is connected to the emitters of Q242-Q252. These transistors are connected as common-base amplifiers to provide a low-impedance current-summing point. The signal at the collectors of Q242-Q252 is connected to Delay Line DL400. Resistor R260 provides reverse termination for the Delay Line.

Delay Line

Delay Line DL400 provides approximately 150 nanoseconds delay for the vertical signal, to allow the horizontal circuits time to initiate a sweep before the vertical signal reaches the vertical deflection plates of the CRT. This allows the instrument to display the leading edge of the signal originating the trigger pulse when using internal triggering. The delay line used in this instrument has a characteristic impedance of about 50 ohms per side, or about 100 ohms differentially. It is of the coaxial type, which does not produce preshoot or phase distortion in the CRT display.

VERTICAL AMPLIFIER

The Vertical Amplifier circuit provides final amplification for the vertical signal before it is applied to the vertical deflection plates of the CRT. This circuit includes an input from the BEAM FINDER switch to compress an overscanned display within the viewing area of the CRT. Fig. 4-18 shows a detailed block diagram of the Vertical Amplifier circuit. A schematic of this circuit is shown on diagram 4 at the rear of this manual.

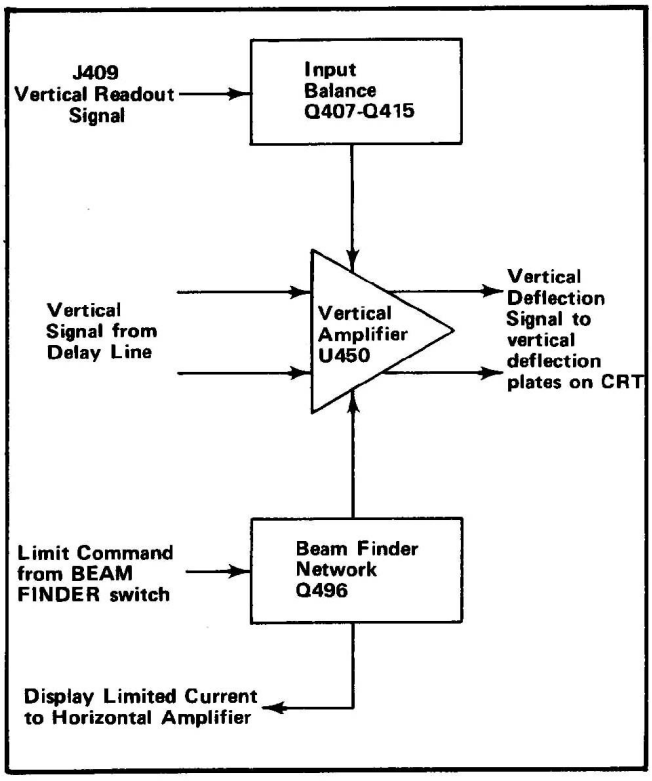


Fig. 4-18. Vertical Amplifier detailed block diagram.

Input Balance

Q407-Q415 comprise a paraphase amplifier to provide input balance for the Vertical Amplifier by changing the DC levels at pins 2 and 4 of U450. Vertical Centering adjustment R403 determines the bias at the base of Q407. As this bias is changed, the levels at the collectors of Q407 and Q415 change due to paraphase action. This DC level is connected to pin 2 of U450 through R408-R423 and to pin 4 through R414-R424. R403 is adjusted so the trace is displayed at the center of the CRT when the inputs to this circuit are at the same potential.

The input to the base of Q407 through J409 is used for Vertical readout signal.

Output Amplifier

Amplification of the vertical signal is accomplished by integrated circuit U450. The circuit shown within the shaded area is a representation of the circuit contained within U450. Notice that the circuit is made up of three similar push-pull stages. Each stage has a pair of common emitter transistors driving a pair of low input impedance common base transistors. Frequency compensation is provided by the networks connected between pins 2 and 4 in the first amplifier stage and pins 7 and 8, 13 and 14 in the third amplifier stage. The resistive network connected to pins 3, 6, and 16 determines the gain of the Vertical Amplifier. Vertical Gain adjustment R447 sets the gain of the second amplifier stage to determine the overall gain of the vertical deflection system and thereby provide a calibrated deflection factor. Bias adjustment R486 sets the voltage level at pin 10 of U450 (nominally 4.3 volts) to balance the third amplifier stage for maximum gain-bandwidth operation.

Beam Finder Network

The Beam Finder Network, consisting of transistor Q496 and associated components, provides a means of locating a display which overscans the graticule area. Under normal operation, −15 volts is connected to the base of Q496 from the BEAM FINDER switch (see diagram 7) to reverse bias it. Therefore, the normal operating levels for U450 are determined by the resistive network connected to pins 3, 6, and 16. When the BEAM FINDER switch is pressed, the −15 volts is interrupted and the base of Q496 rises positive to turn it on. The resulting change in current of U450 unbalances the second amplifier stage so as to limit its gain. This action compresses the display vertically within the display area.

HORIZONTAL AMPLIFIER

The Horizontal Amplifier circuit amplifies the push-pull horizontal deflection signals from the plug-in unit in the horizontal compartment and connects it to the horizontal deflection plates of the CRT. Fig. 4-19 shows a detailed block diagram of the Horizontal Amplifier circuit. A schematic of this circuit is shown on diagram 5 at the rear of this manual.

Horizontal Channel Switch

The horizontal signals from the plug-in unit in the horizontal compartment are connected to pin 2 and pin 15 of U510. The Readout signal is connected to pin 7 of U510. Integrated circuit U510 determines which input signal will provide the signal for the Horizontal amplifier circuit as controlled by the X/Y Shutdown signal from the Readout system. When the X/Y Shutdown is LO, the signal from horizontal compartment is passed to the output of U510. When the X/Y Shutdown is high, the Readout signal is passed to the output of U510. Resistors R514, R515, R521, and R522 establish the operating levels for this circuit. R512 adjusts the circuit gain. R511 and R513 establish the range for the gain adjustment (see Trigger Channel Switch under TRIGGER SELECTOR in this section).

For normal operation, the gain and current level resistors are connected to the Display Limit Command line. The

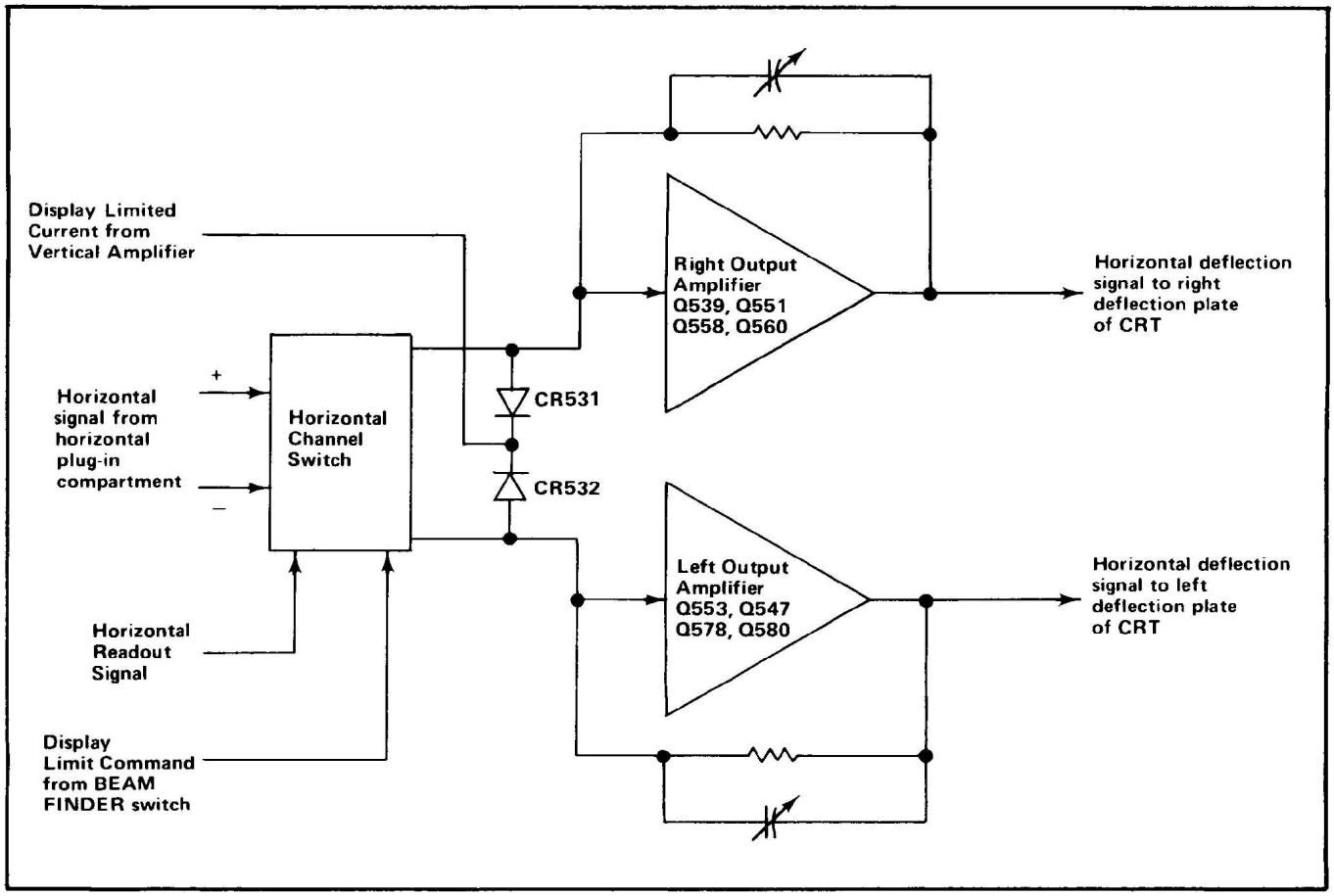


Fig. 4-19. Horizontal Amplifier detailed block diagram.

Display Limit Command is connected to the −15 supply through the BEAM FINDER switch. When the BEAM FINDER switch is actuated, the −15 volt is interrupted to limit the current to U510. At the same time, current is added through CR531 and CR532 from the display limited current line. This added current maintains about the same DC currents through the output circuit in both positions of the BEAM FINDER switch. The signal at the output is connected to the right and left amplifier inputs. Resistor R525 adjusts the amplifier for center screen deflection in the absence of an input signal to U510.

Output Amplifier

Transistors Q539, Q551, Q558, and Q560 function as a current driven feedback amplifier. The input current is converted to a voltage output signal to drive the right horizontal CRT deflection plate. R558 establishes the quiescent current level for series connected transistors Q558 and Q560.

The CRT deflection plates present a capacitive load to the amplifier, which requires additional current during fast transients. Extra current for positive excursions is provided by Q551 via R555, C555, and Q558; for negative excursions, by Q560 via R563.

Resistor R556 reduces the power dissipation in Q558. Resistors R566, R567, and R569 provide DC feedback and establish low frequency gain. Capacitors C566 and C588 (C568 for lower serial numbers) are adjusted for correct gain at fastest sweep rates (in later serial numbered instruments, C588 replaces C568 and a differently located C588, a thermal compensation network C584-R584 is added).

Basic operation of the Left Output Amplifier stage is the same as described for the Right Output Amplifier. C586 and C588 set the gain for the fastest sweep rates (C588 is relocated for later serial numbers and affects both Right and Left Output Amplifiers). The output signal at the collectors of Q578-Q580 connects to the left deflection plate of the CRT through R585.

The series circuit CR549 and R549 stabilize the output amplifier during fast retrace intervals. R535 is adjusted to balance the negative excursions of the right and left sides of the amplifier when the time base plug-in is used in X10 Magnified mode.

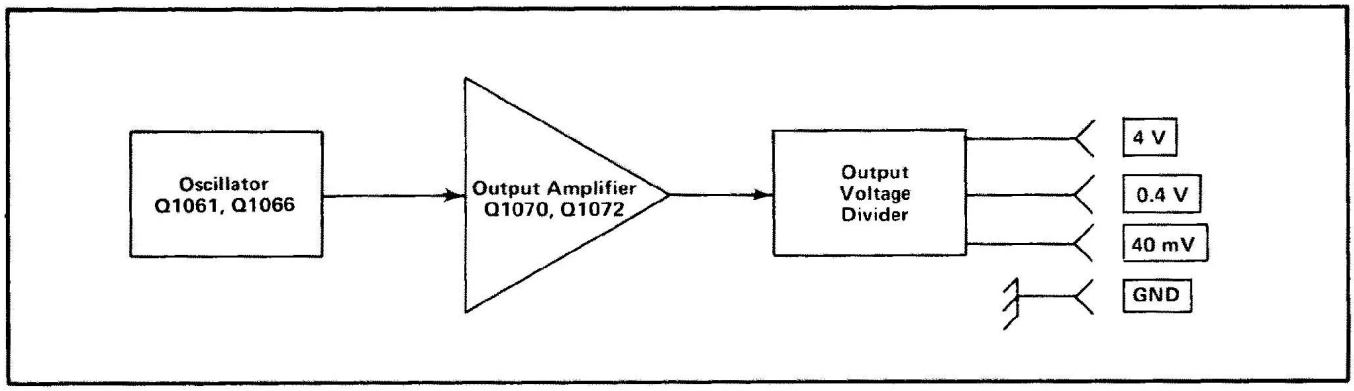


Fig. 4-20. Calibrator detailed block diagram.

CALIBRATOR AND FRONT PANEL SWITCHING

The Calibrator and Front Panel Switching circuit provides output voltage to the front-panel Calibrator pin-jacks and includes the front-panel switches and controls. Fig. 4-20 shows a detailed block diagram of the Calibrator portion of this circuit. A schematic of this circuit is shown on diagram 7 at the rear of this manual.

Mode Switch Logic

The VERT MODE switch determines the operating mode of the Vertical Interface circuit. The levels established by this switch are also used in various other circuits throughout this instrument. This switch is designed so it is self-cancelling (i.e., only one button can be pressed at a time). Specific operation of this switch is described in connection with the circuits that it controls.

The TRIG SOURCE switch controls the operation of the Trigger Selector circuit. This switch is also self-cancelling so only one of the buttons can be pressed at a time. Operation of this switch is discussed in connection with the Trigger Selector circuit.

Calibrator

General. The Calibrator circuit provides accurate voltage output at the front-panel Calibrator pin-jacks. Repetition rate of the output signal is about one kilohertz.

Oscillator. Q1061 and Q1066 are connected as a square-wave oscillator to determine the repetition rate of the Calibrator circuit. Oscillation occurs as follows: Assume that Q1061 is conducting and Q1066 is off. The collector current of Q1061 through R1061 produces a voltage level which holds the base of Q1066 low. This keeps Q1066 turned off, and since there is no current through it, its collector goes positive to produce the positive portion of the square wave. At the same time, C1064 begins to charge toward −15 volts through R1069. The emitter of Q1066 goes negative also as C1064 charges, until it reaches a level about 0.6 volt more negative than the level at its base. Then, Q1066 is forward biased and its emitter rapidly rises positive. Since C1064 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q1066 pulls the emitter of Q1061 positive also, to reverse bias it. The current through Q1066 produces a voltage drop at its collector to produce the negative portion of the square wave.

Now, conditions are reversed. Since Q1061 is reverse biased, there is no current through it. Therefore, C1064 can begin to discharge through R1063. The emitter level of Q1061 follows the discharge of C1064 until it reaches about −0.6 volt. Then, Q1061 is forward biased and its collector drops negative to reverse bias Q1066. This interrupts the current through Q1066, and its collector goes positive again to complete the square wave. Once again, C1064 begins to charge through R1069 to start the second cycle. The signal produced at the collector of Q1066 has a repetition rate of about one kilohertz.

The Oscillator stage can be changed by jumper P1066. When this jumper is installed in the DC position, the Oscillator is disabled and the collector of Q1066 rises positive. This produces a positive DC voltage output to the front-panel Calibrator pin-jacks.

Output Amplifier. Transistors Q1070 and Q1072 are connected as a comparator with the reference level at the base of Q1072 determined by the network R1073-R1074-R1076-R1077. The 4 Volts adjustment R1077, is set to provide accurate output voltage at the 4 V Calibrator pin-jack.

The output of the Oscillator stage is connected to the base of Q1070. This signal controls the conduction of comparator Q1070-Q1072. When the base of Q1070 is high, it is off and Q1072 is conducting. This produces a positive output voltage at the Calibrator pin-jacks. When the level at the base of Q1070 is switched low, Q1070 conducts and Q1072 is reverse biased. Now, the voltage level at the Calibrator pin-jacks drops to zero.

Output Voltage Divider. The collector current of Q1072 in the Output Amplifier stage is applied across the voltage divider made up of resistors R1079 through R1085. This divider is designed to provide a low output resistance in the 40 mV and 0.4 V positions while providing accurate output voltages. The output resistance at the 4 V pin-jack is about 450 ohms and at the 0.4 V and 40 mV pin-jacks is about 50 ohms.

CRT CIRCUIT

The CRT Circuit produces the high-voltage potentials and provides the control circuits necessary for the operation of the cathode-ray tube (CRT). This circuit also includes the Z-Axis Amplifier stage to set the intensity of the CRT display and the Auto Focus amplifier to assure

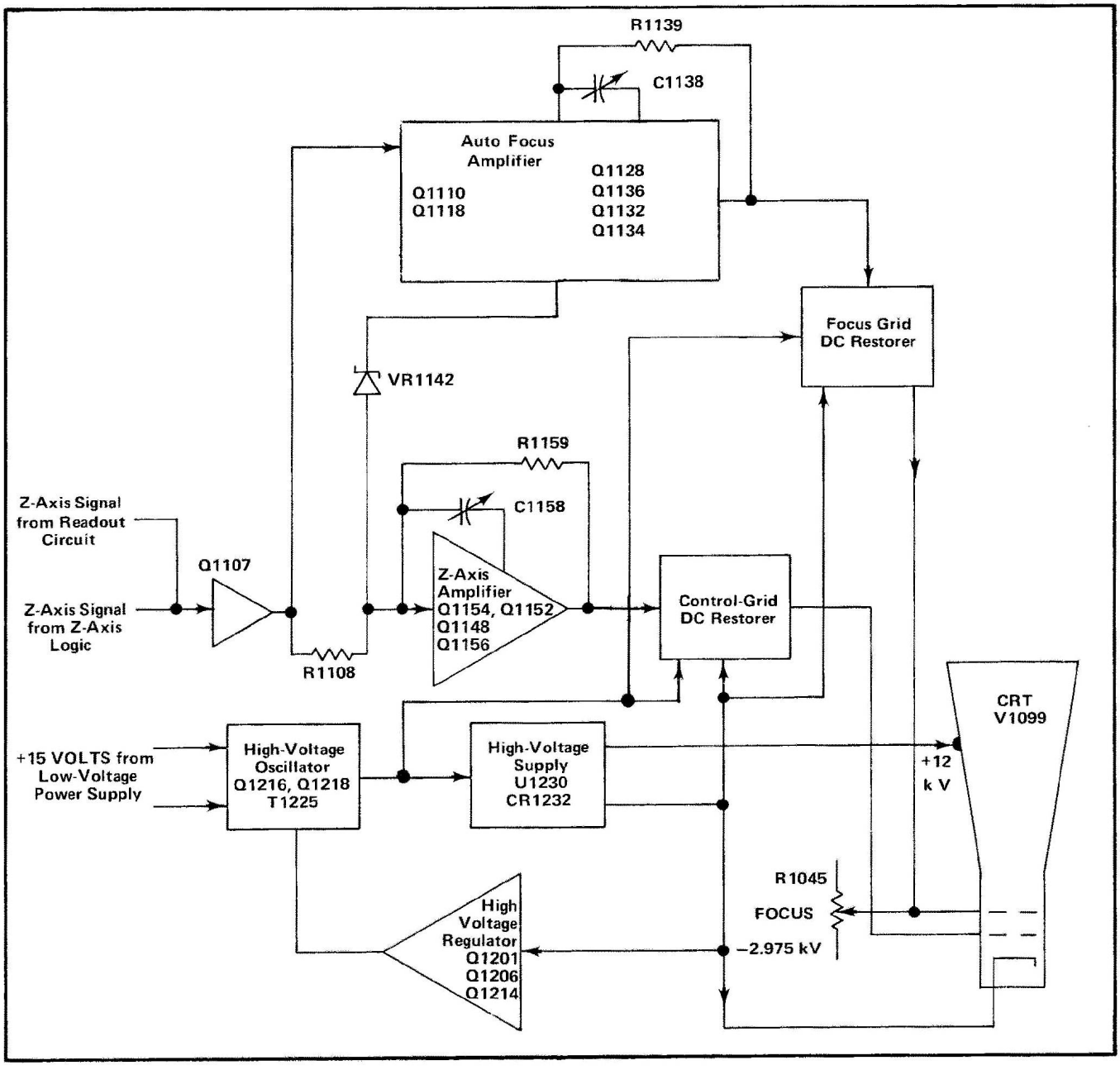


Fig. 4-21. CRT Circuit detailed block diagram.

optimum focus. Fig. 4-21 shows a detailed block diagram of the CRT Circuit. A schematic of this circuit is shown on diagram 8 at the rear of this manual.

Z-Axis Amplifier

The Z-Axis signal from the Logic circuit and the Z-Axis signal from the Readout system are connected to the emitter of Q1107. Transistor Q1107 is a common-base amplifier to establish a low input impedance for the input signals. Transistors Q1148, Q1152, Q1154, and Q1156 form a current driven operational amplifier. The input and output transistors are complementary to provide a fast rise-time and a fast fall-time response. The amplifier input is through resistor R1108. Resistor R1152 establishes a low current in the series connected output transistors. Transistor Q1148 supplies additional current through C1151 for the positive transients, and transistor Q1156 supplies additional current through C1158 for negative transients. Capacitor C1158 is adjusted for optimum square-wave output, resistors R1158 and R1159 along with capacitor C1158 form the feedback network. Zener diode VR1142 provides the necessary change of voltage from the collector of Q1107 to the base of Q1156.

Auto Focus Amplifier

The voltage developed across R1108 by the Z-Axis amplifier driving current is inverted and amplified non-linearly by Q1110 and Q1118, to conform to the requirements of the CRT focus electrode. As the base of Q1110 is driven negative CR1115 is forward biased, producing a knee in the amplifier response. The Level where the knee occurs is determined by the adjustment R1121. The operation of the remaining amplifier is identical to the Z-Axis amplifier.

High-Voltage Oscillator

Power for operation of the high-voltage supply is provided from the +15-Volt Supply. At the time of turn-on, CR1215 is reversed biased holding the collector of Q1214 positive. This allows the starting base bias current for the High-Voltage Oscillator to be supplied from the +5-Volt Supply through R1214, Q1214, and the base feedback windings of T1225 while the emitter potential of Q1216-Q1218 is established by the negative side of the +15-Volt Supply. As the output of the high-voltage supply increases to its required output level, the collector of Q1214 goes negative until CR1215 is forward biased. Then the collector level of Q1214 is clamped about 0.6 volt more negative than the negative side of the +15-Volt Supply. This configuration provides a controlled starting current for the High-Voltage Oscillator at turn-on, and at the same time allows the High-Voltage Regulator stage to control the current for the High-Voltage Oscillator after the stage reaches operating potentials to provide a regulated high-voltage output.

Q1216-Q1218 and the associated circuitry comprise an oscillator to drive high-voltage transformer T1225. When the instrument is turned on, assume that Q1216 comes into conduction first. The collector current of Q1216 produces a corresponding current increase in the base-feedback winding of T1225 to further increase the conductivity of Q1216. At the same time, the voltage developed across the base-feedback winding connected to Q1216 holds Q1218 reverse biased.

As long as the collector current of Q1216 continues to increase, voltage is induced into the base-feedback windings of T1225 which holds Q1216 forward biased and Q1218 reverse biased. However, when the collector current of Q1216 stabilizes, the magnetic field built up in T1225 begins to collapse. This induces an opposite current into the base windings which reverse biases Q1216, but forward biases Q1218. When the induced voltage at the base of Q1218 exceeds the bias set by the High-Voltage Regulator, Q1218 conducts and the amplified current at its collector adds to the current flowing through T1225 due to the collapsing field. Then, as the current through T1225 stabilizes again, the magnetic field around it once more begins to collapse. This reverses the conditions to start another cycle.

The signal produced across the primary of T1225 is a sine wave at a frequency of 35 to 45 kilohertz. The amplitude of the oscillations in the primary of T1225 is controlled by the High-Voltage Regulator to set the total accelerating potential for the CRT. Filter network C1222-L1222 decouples high peak operating current from the +15-Volt Supply.

High-Voltage Regulator

A sample of the secondary voltage from T1225 is connected to the High-Voltage Regulator stage through divider R1245A-R1245B. Q1201 and Q1206 are connected as an error amplifier to sense any change in the voltage level at the base of Q1201. The ground reference for the emitter of Q1201 through R1202, establishes the reference level for this stage. The output voltage is set by the fixed values of the components in this circuit.

Regulation occurs as follows: If the output voltage at the −2975 V test point starts to go positive (less negative), a sample of this positive-going change is connected to the base of Q1201 through R1245B. Both Q1201 and Q1206

are forward biased by this positive change, which in turn increases the conduction of Q1214. This results in a greater bias current delivered to the bases of Q1216-Q1218 through Q1214. Now, the bases of both Q1216 and Q1218 are biased closer to their conduction level so the feedback voltage induced into their base-feedback windings produces a larger collector current. This results in a larger induced voltage in the secondary of T1225 to produce a more negative level at the −2975 V test point to correct the original error. In a similar manner, the circuit compensates for output changes in a negative direction. Since the amplitude of the voltage induced into the secondary of T1225 also determines the output level of the positive High-Voltage Supply and the Control-Grid Supply, the total high-voltage output is regulated by sampling the output of the negative High-Voltage Supply.

High-Voltage Supplies

High-voltage transformer T1225 has two output windings. One winding provides filament voltage for the cathode-ray tube. The other winding provides the negative and positive accelerating potential for the CRT and the bias voltage for the control grid. All of these voltages are regulated by the High-Voltage Regulator stage to maintain a constant output voltage as previously described.

Positive accelerating potential for the CRT anode is supplied by the voltage quadrupler U1230. The applied voltage from the secondary of T1225 is about six kilovolts peak-to-peak. This results in an output voltage of about +12 kilovolts at the CRT anode. The negative accelerating potential for the CRT cathode is also obtained from this same secondary winding. Half-wave rectifier CR1232 provides an output voltage of about −2.975 kilovolts which is connected to the CRT cathode through R1234. The cathode and filament are connected together through R1275 to prevent cathode-to-filament breakdown due to a large difference in potential between these CRT elements. A sample of the negative accelerating voltage is connected to the High-Voltage Regulator to maintain a regulated high-voltage output.

The network consisting of diodes CR1269-CR1268-CR1270-CR1264-VR1264 provides the negative voltage for the control grid of the CRT. Output level of this supply is set by CRT Grid Bias adjustment R1261. Approximately 800 volts peak-to-peak from the secondary of T1225 is connected to the Control-Grid Supply through C1266 and R1266. Diodes CR1268 and CR1264 clip this signal to determine the operating level at the control grid. CR1268 limits the negative excursion of the signal; quiescently when the CRT is blanked, the anode of CR1268 is set at about +15 volts by the Z-Axis Amplifier stage. The positive clipping level at the cathode of CR1264 is set by CRT Grid Bias adjustment R1261. R1261 is adjusted to bias the control grid of the CRT just enough negative so the trace is blanked between sweeps. Under normal conditions, this biases the control grid about 80 volts more negative than the cathode.

The negative level at the CRT cathode is connected to the cathode of CR1270. This level is held constant by the High-Voltage Regulator as described previously. The clipped voltage developed by diodes CR1264 and CR1268 is peak to peak rectified by diodes CR1269 and CR1270 and super-imposed on this negative voltage to result in a level at the grid of the CRT which is more negative than the CRT cathode level. C1269 acts as a filter to provide a constant voltage output level. The unblanking gate level developed by the Z-Axis Amplifier stage is applied to the anode of CR1268 through R1157. The fast rising and falling portions of this signal are coupled directly to the output through C1269. The overall effect of the unblanking gate is to further clip the negative excursions thereby reducing the voltage difference between grid and cathode of the CRT. This allows the cathode current of the CRT to pass to the anode so the display can be viewed.

CRT Control Circuits

The focus of the display is determined by the FOCUS control R1045. This control and the Auto Focus amplifier maintains a well-defined display for fast changes in the intensity of the display. The network consisting of CR1255, CR1254, CR1253, CR1258, and VR1258 provide the negative voltage for the focus grid of the CRT. Approximately 800 volts peak to peak from the secondary of T1225 is connected to the focus grid supply through C1257 and R1257. The positive clipping level at the anode of CR1258 is set by the FOCUS control setting. This determines the operating level at the focus grid. Under normal operating conditions the voltage applied to the focus grid is more positive (less negative) than the control grid or the cathode of the CRT. The signal developed by the Auto Focus amplifier is coupled to the focus grid by C1254. When there is a sudden change in intensity levels the focus grid level will change to maintain a well-defined display. Astigmatism adjustment R1193, which is used in conjunction with the FOCUS control to obtain a well-defined display, varies the positive level on the astigmatism grid. Geometry adjustment R1184 varies the positive level on the horizontal deflection-plate shield to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field induced by coils around the CRT. Y-Axis Alignment R1190 controls the current through L1098, which affects the CRT beam after vertical deflection, but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. Beam Rotation adjustment R1181 controls the current through L1099 and affects both the vertical and horizontal rotation of the display.

LOW-VOLTAGE POWER SUPPLY

The Low-Voltage Power Supply circuit provides the operating power for this instrument from six regulated supplies. Electronic regulation is used to provide stable, low-ripple output voltages. Each supply (except the +130 V supply, which is fused) contains a short-protection circuit to prevent instrument damage if a supply is inadvertently over-loaded or shorted to ground. Fig. 4-22 shows a detailed block diagram of the Low-Voltage Power Supply circuit. A schematic of this circuit is shown on diagram 9 at the rear of this manual.

Power Input

Power is applied to the primary of transformer T801 through line fuse F1000, thermal cutout S1000, and POWER switch S1001. The Voltage-Selector Jumper, P1001, connects the two halves of the primary of T801 in parallel for 110-volt (nominal) operation. Voltage-Selector Jumper P1002 connects the two halves of the primary in series for 220-volt (nominal) operation. The line fuse, F1000, must be changed to provide the correct protection for 220-volt nominal operation.

Each half of the primary of T801 has taps above and below the 110-volt (220-volt) nominal point. When the Voltage Selector Jumper is moved from LOW to MED to HI, more turns are effectively added to the primary winding and the turns ratio is decreased to compensate for the increased primary voltage. This configuration extends the regulating range of the 7603.

For the R7603 a fan provides forced-air cooling. The fan is connected in parallel with one half of the primary winding of T801. Therefore, it always has the same voltage applied regardless of the position of the Voltage-Selector Jumper.

Thermal cutout S1000 provides thermal protection for this instrument. If the internal temperature of the instrument exceeds a safe operating level, S1000 opens to interrupt the applied power. When the temperature returns to a safe level, S1000 automatically closes to re-apply the power.

−50-Volt Supply

The following discussion includes the description of the 50 V Rectifier, −50 V Series Regulator, −50 V Feedback Amplifier, −50 V Reference, and −50 V Current Limiting stages. Since these stages are closely related in the operation of the −50-volt regulated output, their performance is most easily understood when discussed as a unit.

The 50 V Rectifier assembly CR808 rectifies the output at the secondary of T801 to provide the unregulated voltage source for both the −50- and +50-volt supplies. CR808 is connected as a bridge rectifier and its output is filtered by C808-C809. Transistors Q886, Q896, Q900 operate as a feedback-stabilized regulator circuit to maintain a constant −50-volt output level. Q886 is connected as a differential amplifier to compare the feedback voltage at the base of Q886B against the reference voltage at the base of Q886A. The error output at the collector of Q886B reflects the difference, if any, between these two inputs. The change in error-output level at the collector of Q886B is always opposite in direction to the change in the feedback input at the base of Q886B (out of phase).

Zener diode VR890 sets a reference level of about −9 volts at the base of Q886A. A feedback sample of the output voltage from this supply is connected to the base of Q886B through divider R880-R881-R882. R881 in this divider is adjustable to set the output level of this supply. Notice that the feedback voltage to this divider is obtained from a line labeled −50 V Sense. Fig. 4-23 illustrates the reason for this configuration. The inherent resistance of the interconnecting wire between the output of the −50-Volt Supply and the load produces a voltage drop which is equal to the output current multiplied by the resistance of the interconnecting wire. Even though the resistance of the wire is small, it results in a substantial voltage drop due to the high output current of this supply. Therefore, if the feedback voltage were obtained ahead of this drop, the voltage at the load might not maintain close regulation. However, the −50 V Sense feedback configuration overcomes this problem since it obtains the feedback voltage from a point as close as practical to the load. Since the current in the −50 V Sense line is small and constant, the feedback voltage is an accurate sample of the voltage applied to the load.

Regulation occurs as follows: If the output level of this supply decreases (less negative) due to an increase in load, or a decrease in input voltage (as a result of line voltage changes or ripple), the voltage across divider R880-R881-R882 decreases also. This results in a more positive feedback level at the base of Q886B than that established by the −50 V Reference stage at the base of Q886A. Since the transistor with the more positive base controls the conduction of the differential amplifier, the output current at the collector of Q886B increases. This increase in output from Q886B allows more current to flow through Q896 and Q900 to result in increased conduction of −50 V Series Regulator Q903. The load current increases and the output voltage of this supply also increases (more negative). As a result, the feedback voltage from the −50 V Sense line increases and the base of Q886B returns to the same level as the base of Q886A. Similarly, if the output level of this supply increases (more negative), the output current of Q886B decreases. The feedback through Q896 and Q900 reduces the conduction of the −50 V Series Regulator to decrease the output voltage of this supply.

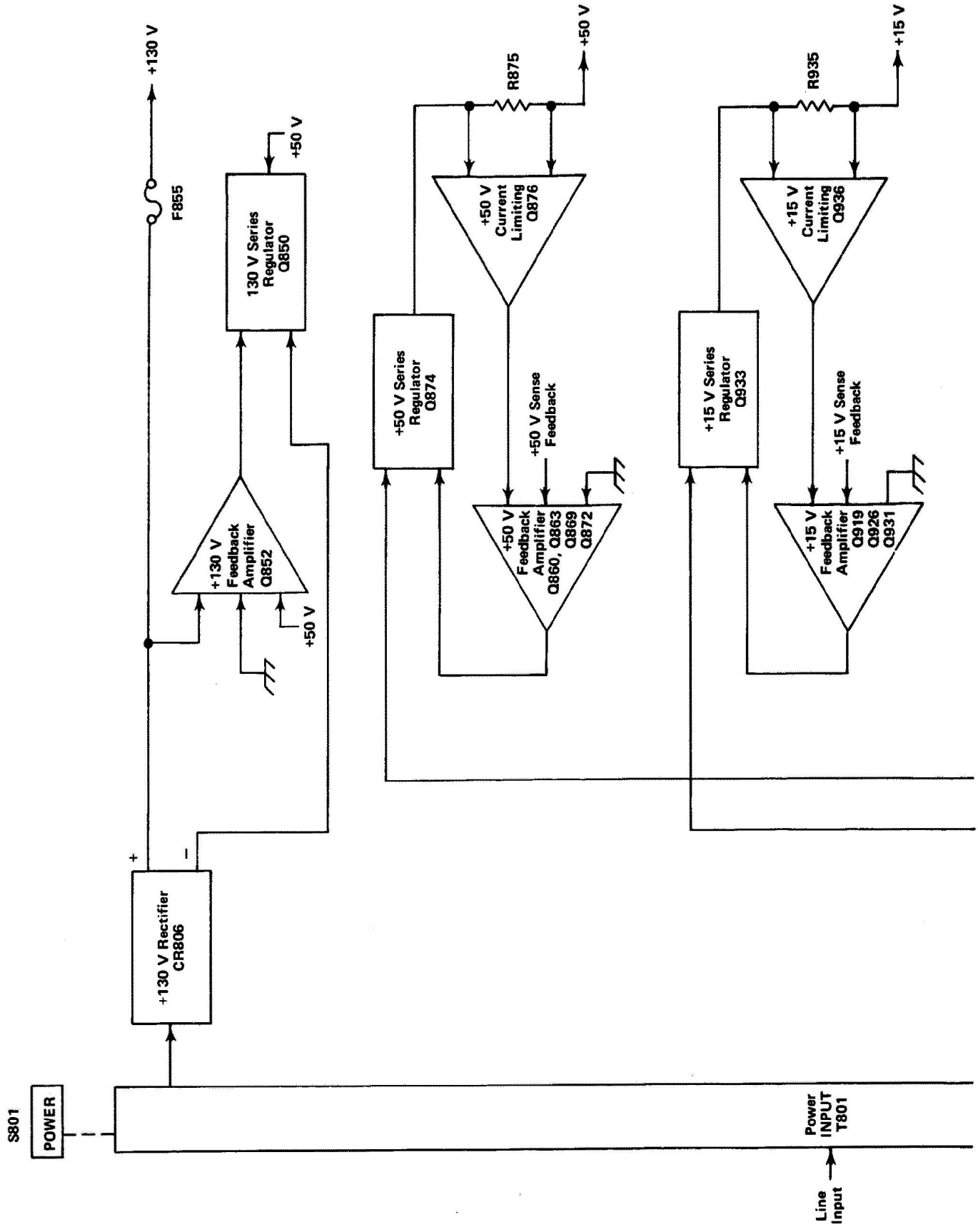


Fig. 4-22. Low-Voltage Power Supply detailed block diagram.

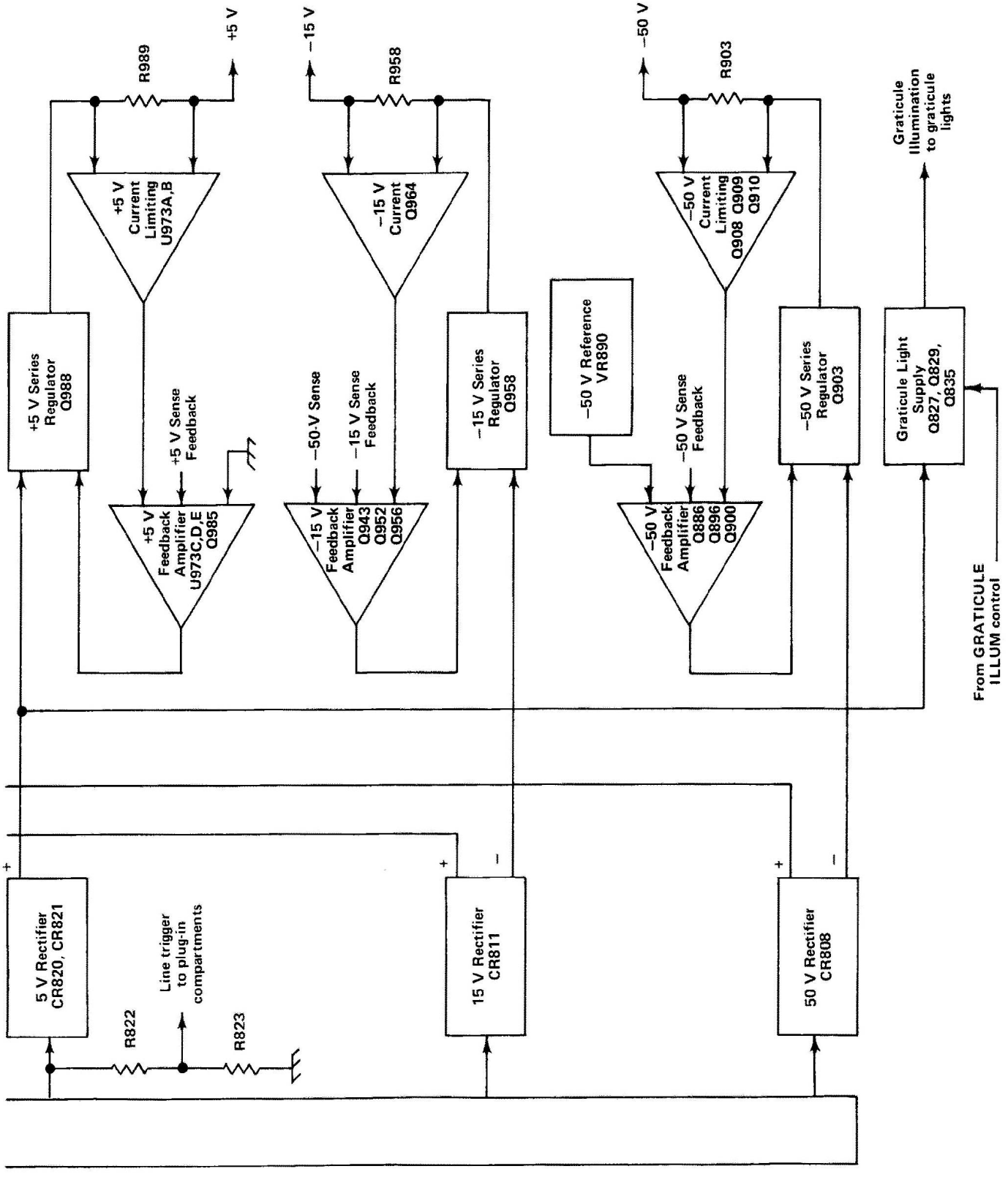


Fig. 4-22. Low-Voltage Power Supply detailed block diagram (cont).

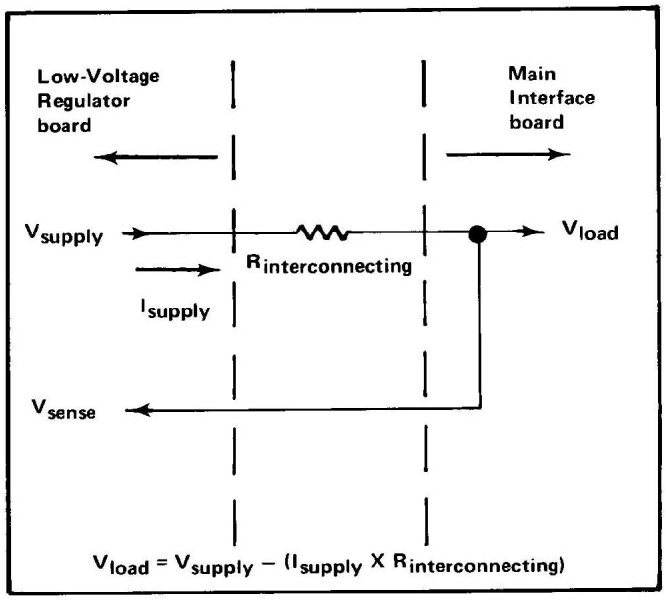


Fig. 4-23. Schematic illustrating voltage drop between power supply output and load due to resistance of interconnecting wire.

−50 Volts adjustment R881 determines the divider ratio to the base of Q886B and thereby determines the feedback voltage. This adjustment sets the output level of the supply in the following manner: If R881 is adjusted so the voltage at its variable arm goes less negative (closer to ground), this appears as an error signal at the base of Q886B. In the same manner as described previously, this positive-going change at the feedback input of the differential amplifier increases the conduction of the −50 V Series Regulator to produce more current to the load, and thereby increase the output voltage of this supply. This places more voltage across divider R880-R881-R882 and the divider action returns the base of Q886B to about −9 volts. Notice that the feedback action of this supply forces a change in the output level which always returns the base of Q886B to the same level as the base of Q886A. In this manner, the output level of the −50-Volt Supply can be set to exactly −50 volts by correct adjustment of R881.

The −50 V Current Limiting stage Q908-Q909-Q910 protects the −50-Volt Supply if excess current is demanded from this supply. All of the output current from the −50-Volt Supply flows through R903. Transistor Q908 senses the voltage at the collector of the −50 V Series Regulator Q903 and compares it against the −50 V output level at the base of Q909 which is obtained from the other side of R903. Under normal operation, Q908 is held in conduction and Q909 is off. However, when excess current is demanded from the −50 V Series Regulator due to a short circuit or similar malfunction at the output of this supply, the voltage drop across R903 increases until the base of Q908 goes more negative than the level at the base of Q909. Then Q909 takes over conduction of the comparator. The collector current of Q909 increases the voltage drop across R896 to reduce the conduction of Q896 in the −50 V Feedback Amplifier and limit the conduction of Q903. Q910 is connected as a constant-current source for Q908-Q909.

−15-Volt Supply

Basic operation of all stages in the −15-V Supply is the same as for the −50-Volt Supply. Reference level for this supply is established by divider R945-R946 between ground and the −50 V Sense voltage. The divider ratio of R945-R946 sets a level of −15 volts at the base of Q943A. The level on the −50 V Sense line is held stable by the −50-Volt Supply as described previously. The −15 V Sense voltage is connected to the base of Q943B through R940. Any change at the output of the −15-Volt Supply appears at the base of Q943B as an error signal. The output voltage is regulated in the same manner as described for the −50-Volt Supply.

+5-Volt Supply

Basic operation of the +5-Volt Supply is the same as described for the previous supplies. The +5 V Current Limiting and +5 V Feedback Amplifier (except for Q985) is made up of a five-transistor array U973. Notice that both U973C and Q985 in the +5 V Feedback Amplifier are connected as emitter followers, since inversion is not necessary in the feedback path for positive output voltages. Reference voltage for the +5 V Feedback Amplifier stage is established by divider R970-R971 between the +5 V Sense and −50 V Sense feedback voltages. This divider establishes a quiescent level of about 0 volt at the base of U973E.

+15-Volt Supply

The +15-Volt Supply operates in the same manner as described for the previous supplies. The unregulated +15-Volt Supply provides the source voltage for the High-Voltage Oscillator stage in the CRT circuit through fuse F814 and P870.

+50-Volt Supply

Operation of the +50-Volt Supply is the same as described for the previous supplies. The unregulated +50 volts, from 50 V Rectifier CR808, is used to provide a positive starting voltage for the −50-Volt Supply.

+130-Volt Supply

The +130-V Rectifier CR806 provides the rectified voltage for the +130-Volt Supply. However, this secondary winding of T801 does not supply the full potential necessary to obtain the +130-volt output level. To provide the required output level, the +50-Volt Supply is connected in series with this supply through Q850. Basic regulation of

the output voltage is provided by +130 V Feedback Amplifier Q852, and +130 V Series Regulator Q850.

The output voltage of this supply is connected across divider R855-R856. This divider provides a quiescent level of about +50 volts at the base of Q852. The reference level for this supply is provided by the +50-Volt Supply connected to the emitter of Q852. If the output of this supply changes, this change is sensed by Q852 and an amplified error signal is connected to the base of Q850. This error signal changes the conduction of the +130 V Series Regulator Q850 to correct the output error. Fuse F855 protects this supply if the output is shorted. However, since the response time of F855 is slow to a shorted condition, VR851 provides additional current to the base of Q850 to protect it from damage due to overvoltage. Diode CR852 limits the reverse bias on Q852 to about 0.6 volt when F855 is blown.

Graticule Light Supply

Power for the graticule lights is supplied by the Graticule Light Supply. Rectified voltage for this supply is provided by 5 V Rectifier CR820-CR821. Q835 operates as a series regulator transistor. Emitter follower Q829 determines the conduction of this series regulator as controlled by front panel GRATICULE ILLUM Control R1095. Current-limiting to protect this supply is provided by Q827. Under normal operation, divider R830-R831-R833 sets the base of Q827 below its conduction level. However, if excess current is demanded from this supply, the voltage drop across R837-R838 increases until Q827 comes into conduction. The collector of Q827 then limits the conduction of this supply to limit its output current.

Divider R822-R823 provides a sample of the line voltage in the secondary of T801 to the plug-in unit. This provides a line-frequency reference to the plug-in units for internal triggering at line frequency or for other applications.

DC Fan (R7603 only)

The DC fan (Option 5) uses a brushless, Hall-effect motor. The Hall-effect devices, located inside the motor housing, control the base current to motor-driving transistors Q1034-Q1035-Q1037-Q1038 depending upon the magnitude and polarity of the magnetic field around them. A permanent magnet, located in the rotor, changes the magnetic field as the rotor turns, causing the Hall-effect devices to turn on the appropriate transistors to drive the motor windings.

Transistor Q1041 provides a constant current source for the Hall-effect devices, responding to voltage changes at the emitters of the driving transistors, thus controlling the motor current. Transistor Q1030, along with R1203, provides a biasing arrangement to make the Hall-effect devices compatible with the silicon driving transistors.

SIGNAL OUT BOARD

VERT SIG OUT

The vertical signal is selected by the TRIG SOURCE switch. The vertical signal selected is applied to the bases of a differential amplifier Q606 and Q618. A single-ended signal is taken off the collector of Q618 and connected to an output buffer Q620. CR621 and CR622 provide protection against a high voltage inadvertently applied to the output connector.

+ GATE OUT

The gate signal is connected to a comparator circuit Q662 and Q666 through resistor R660. From the comparator the gate signal is connected to the emitter of an output buffer Q672. Gate Selector switch connects one of the gate signals to R660, the input of the Gate Amplifier. Possible gate signals are MAIN gate and, with a dual-sweep time-base unit, a DELAY or an AUXILIARY gate signal can be selected. CR674 and CR676 provide protection against a high voltage inadvertently applied to the output connector.

+ SAWTOOTH OUT

The sawtooth signal is connected to the Sawtooth Amplifier through R36. Q631, Q634, and Q640 comprise a negative feedback amplifier with a gain of two, determined by the ratio of feedback resistor R645 to the combined input resistance of R630 and R63. CR635 and CR676 provide protection against a high voltage inadvertently applied to the output connector.

READOUT SYSTEM

The Readout System in the 7603 provides alphanumeric display of information encoded by the plug in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis. Schematics for the total Readout System are shown on diagrams at the rear of this manual.

The definitions of several terms must be clearly understood to follow this description of the Readout System. These are:

Character—A character is a single number, letter, or symbol which is displayed on the CRT, either alone or in combination with other characters.

Word—A word is made up of a related group of characters. In the 7603 Readout System, a word can consist of up to ten characters.

Frame—A frame is a display of all words for a given operating mode and plug-in combination. Up to six words can be displayed in one frame. Fig. 4-24 shows one complete frame (simulated readout) and the position at which each of the six words is displayed.

Column—One of the vertical lines in the Character Selection Matrix (see Fig. 4-25). Columns C-0 (column zero) to C-10 (column 10) can be addressed in the 7603 system.

Row—One of the horizontal lines in the Character Selection Matrix (Fig. 4-25). Rows R-1 (row 1) to R-10 (row 10) can be addressed in the 7603 system.

Time-slot—A location in a pulse train. In the 7603 Readout System, the pulse train consists of 10 negative-going pulses. Each of these time-slots is assigned a number between one and ten. For example, the first time-slot is TS-1.

Time-multiplexing—Transmission of data from two or more sources over a common path by using different time intervals for different signals.

Display Format. Up to six words of readout information can be displayed on the 7603 CRT. The position of each word is fixed and is directly related to the plug-in unit from which it originated. Fig. 4-24 shows the area of the graticule where the readout from each plug-in unit is displayed. Notice that channel 1 of each plug-in unit is displayed within the top division of the CRT and channel 2 is displayed directly below within the bottom division. Fig. 4-26 shows a typical display.

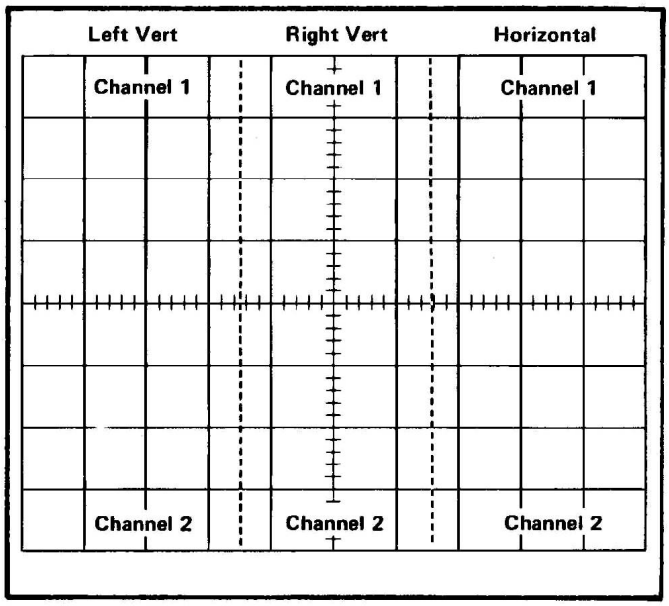


Fig. 4-24. Location of readout words on the CRT identifying the originating plug-in unit and channel (one complete frame shown, simulated readout).

Each word in the readout display can contain up to 10 characters, although the typical display will contain between two and seven characters per word. The characters are selected from the Character Selection Matrix shown in Fig. 4-25. Any one of the 50 separate characters can be addressed and displayed on the CRT. In addition, 12 operational addresses are provided for special instructions to the Readout System. The unused locations in the Matrix (shaded areas) are available for future expansion of the Readout System. The method of addressing the locations in the Character Selection Matrix is described in the following discussion.

Developing the Display. The following basic description of the Readout System uses the block diagram shown in Fig. 4-27. This description is intended to relate the basic function of each stage to the operation of the overall Readout System. Detailed information on circuit operation is given later.

The key block in the Readout System is the Timer stage. This stage produces the basic signals which establish the timing sequences within the Readout System. Period of the timing signal is about 250 microseconds (drops to about 210 microseconds when Display-Skip is received; see detailed description of Timing stage for further information). This stage also produces control signals for other stages within this circuit and interrupt signals to the Vertical Interface, Horizontal Interface, CRT Circuit, and Z-Axis Logic stage which allow a readout display to be presented. The Time-Slot Counter stage receives a trapezoidal voltage signal from the Timer stage and directs it to one of ten output lines. These output lines are labeled TS-1 through TS-10 (time-slots one through ten) and are connected to the vertical and horizontal plug-in compartments as well as to various stages within the Readout System. The output lines are energized sequentially so there is a pulse on only one of the 10 lines during any 250 microsecond timing period. When the Time-Slot Counter stage has completed time-slot 10, it produces an End-of-Word pulse which advances the system to the next channel.

Two output lines, row and column, are connected from each channel of the plug-in units back to the Readout System. Data is encoded on these output lines by connecting resistors between them and the time-slot input lines. The resultant output is a sequence of ten analog

ROW NUMBER \ COLUMN NUMBER →	CURRENT (MILLI-AMPERES)	C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	⩾ 1.0
R-1	0	SKIP[1]	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*
R-2	0.1		*ϟ*	*<*	*I*	*/*	*+*	*−*	*+*	*C*	*Δ*	*>*
R-3	0.2		ADD[1] ONE ZERO	ADD[1] TWO ZEROS	SHIFT[1] PREFIX ←	SHIFT[1] PREFIX ← AND ADD ONE ZERO						*IDENTIFY*[1]
R-4	0.3		*m*	*μ*	*n*	*p*	*X*	*K*	*M*	*G*	*T*	*R*
R-5	0.4		*S*	*V*	*A*	*W*	*H*	*d*	*B*	*c*	*Ω*	*E*
R-6	0.5		*U*	*N*	*L*	*Z*	*Y*	*P*	*F*	*J*	*Q*	*D*
R-7	0.6				DECIMAL[1] POINT LOCATION NO. 3	DECIMAL[1] POINT LOCATION NO. 4	DECIMAL[1] POINT LOCATION NO. 5	DECIMAL[1] POINT LOCATION NO. 6	DECIMAL[1] POINT LOCATION NO. 7			
R-8	0.7										DECIMAL[2] POINT	
R-9	0.8											
R-10	0.9	ADD SPACE IN DISPLAY[1]										

UNUSED LOCATIONS. AVAILABLE FOR FUTURE EXPANSION OF READOUT SYSTEM

[1] OPERATIONAL ADDRESS.

[2] DECIMAL POINT CHARACTER. SEE DECIMAL POINT CHARACTER DESCRIPTION IN TEXT.

Fig. 4-25. Character Selection Matrix for 7603 Readout System.

1195-25A

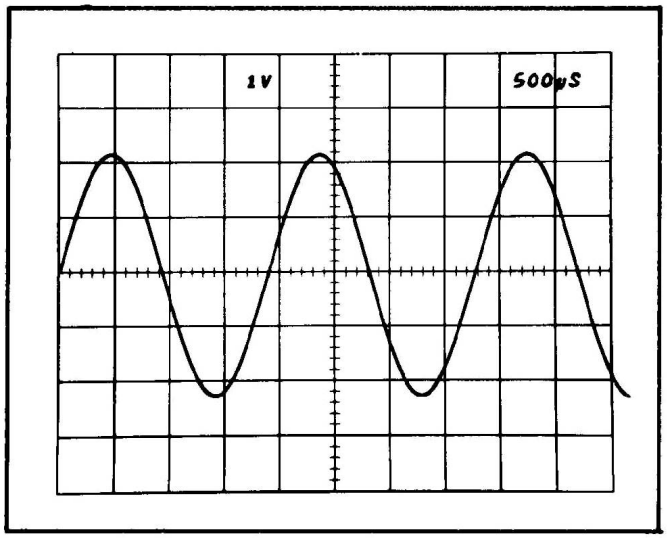


Fig. 4-26. Typical readout display where only channel 1 of the Right Vertical and Horizontal units is displayed.

current levels which range from zero to one milliampere (100 microamperes/step) on the row and column output lines. This row and column correspond to the row and column of the Character Selection Matrix in Fig. 4-25. The standard format in which information is encoded onto the output lines is given in Table 4-2 (special purpose plug-in units may have their own format for readout; these special formats will be defined in the manuals for these units).

The encoded column and row data from the plug-in units is selected by the Column Data Switch and Row Data Switch stages respectively. These stages take the analog currents from the six data lines (two channels from each of the three plug-in compartments) and produce a single time-multiplexed analog voltage output which contains all of the column or row information from the plug-ins. The Column Data Switch and Row Data Switch are sequenced by the binary Channel Address No. 1 code from the Channel Counter.

The time multiplexed output of the Column Data Switch is monitored by the Display-Skip Generator to determine if it represents valid information which should be displayed. Whenever information is not encoded in a time-slot, the Display-Skip Generator produces an output level to prevent the Timer stage from producing the control signals which normally interrupt the CRT display and present a character.

The analog outputs of the Column Data Switch and Row Data Switch are connected to the Column Decoder and Row Decoder stages respectively. These stages sense the magnitude of the analog voltage input and produce an output current on one of ten lines. The outputs of the Column Decoder stage are identified as C-1 to C-10 (column 1 to 10) which correspond to the column information encoded by the plug-in unit. Likewise, the outputs of the Row Decoder stage are identified as R-1 to R-10 (row 1 to 10) which correspond to the row information encoded by the plug-in unit. The primary function of the row and column outputs is to select a character from the Character Selection Matrix to be produced by the Character Generator stage. However, these outputs are also used at other points within the system to indicate when certain information has been encoded. One such stage is the Zeros Logic and Memory. During time-slot 1 (TS-1), this stage checks if zero-adding or prefix-shifting information has been encoded by the plug-in unit and stores it in memory until time-slots 5, 6, or 8. After storing this information, it triggers the Display-Skip Generator stage so there is no display during this time slot (as defined by Standard Readout Format; see Table 4-2). When time-slots 5, 6, and 8 occur, the memory is addressed and any information stored there during time-slot 1 is transferred out and connected to the input of the Column Decoder stage to modify the analog data during the applicable time-slot.

TABLE 4-2

Standard Readout Format

Time-Slot Number	Description
TS-1	Determines decimal magnitude (number of zeros displayed or prefix change information) or the IDENTIFY function (no display during this time-slot).
TS-2	Indicates normal or inverted input (no display for normal).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control (no display for calibrated condition).
TS-4	1-2-5 scaling.
TS-5 TS-6 TS-7	Not encoded by plug-in unit. Left blank to allow addition of zeros by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Define the units of measurement of the plug-in unit. May be standard units of measurement (V, A, S, etc.,) or special units selected from the Character Selection Matrix.

Another operation of the Zeros Logic and Memory stage is to produce the IDENTIFY function. When time-slot 1 is encoded for IDENTIFY (column 10, row 3), this stage produces an output level which connects the Column Data Switch and Row Data Switch to a coding network within the Readout System. Then, during time-slots 2 through 9, an analog current output is produced from the Column Data Switch and Row Data Switch which addresses the correct points in the Character Selection Matrix to display the word "IDENTIFY" on the CRT. The Zeros Logic and Memory stage is reset after each word by the Word Trigger pulse.

The Character Generator stage produces the characters which are displayed on the CRT. Any of the 50 characters shown on the Character Selection Matrix of Fig. 4-24 can be addressed by proper selection of the column and row current. Only one character is addressable in any one time-slot; a space can be added into the displayed word by the Decimal Point Logic and Character Position Counter stage when encoded by the plug-in. The latter stage counts how many characters have been generated and produces an output current to step the display one character position to the right for each character. In addition, the character position is advanced once during each of time-slots 1, 2, and 3 whether a character is generated during these time-slots or not. This action fixes the starting point of the standard-format display such that the first digit of the scaling factor always starts at the same point within each word regardless of the information encoded in time-slot 2 (normal/invert) or time-slot 3 (cal/uncal) which precedes this digit. Also, by encoding row 10 and column 0 during any time-slot, a blank space can be added to the display. Decimal points can be added to the display at any time by addressing row 7 and columns 3 through 7 (see Character Selection Matrix for location of these decimal points). The Decimal Point Logic and Character Position Counter stage is reset after each word by the Word Trigger pulse.

The Format Generator stage provides the output signals to the vertical and horizontal deflection systems of the instrument to produce the character display. The binary Channel Address No. 2 code from the Channel Counter stage is connected to this stage so that the display from each channel is positioned to the area of the CRT which is associated with the plug-in and channel originating the word (see Fig. 4-24). The positioning current or decimal point location current generated by the Decimal Point Logic and Character Position Counter stage is added to the horizontal (X) signal at the input to the Format Generator stage to provide horizontal positioning of the characters within each word. The X- and Y-output signals are connected to the Horizontal Amplifier and Vertical Amplifier through the Horizontal Output and Vertical Output stages respectively.

The Word Trigger stage produces a trigger from the End-of-Word pulse generated by the Time-Slot Counter stage after the tenth time-slot. This Word Trigger pulse advances the Channel Counter to display the information from the next channel or plug-in. It also provides a reset pulse to the Zeros Logic and Memory stage and the Decimal Point Logic and Character Position Counter stage. The Word Trigger stage can also be advanced to jump a complete word or a portion of a word when a Jump command is received from the Row Decoder stage.

The Single-Shot Lockout stage allows the display sequence of the Readout System to be changed. Normally, the Readout System operates in a free-running mode so the waveform display is interrupted randomly to display characters. However, under certain conditions (such as single-shot photography), it is desirable that the Readout System operate in a triggered mode where the readout portion of the display is normally blanked out but can be presented on command. The Readout Mode switch determines the operating mode of the readout system.

Circuit Analysis of Readout System

The following analysis of the Readout System describes the operation of each stage in detail. Complete schematics of the Readout System are shown on diagram 10 at the read of this manual.

Timer

Timer U2126 establishes the timing sequence for all circuits within the Readout System This stage produces seven time-related output waveforms (see Fig. 4-28). The triangle waveform produced at pin 6 forms the basis for the remaining signals. The basic period of this triangle waveform is about 250 microseconds as controlled by RC network C1214-R1214. The triangle waveform is clipped and amplified by U1210 to form the trapezoidal output signal at pin 10. The amplitude of this output signal is exactly 15 volts as determined by V2126 (exact amplitude necessary to accurately encode data in plug-in units; see Encoding the Data). The Trigger output at pin 5 provides the switching signal for the Time-Slot Counter and Word Trigger stages.

The signals at pins 12, 13, 14, and 16 are produced only when the triangle waveform is on its negative slope and the trapezoidal waveform has reached the lower level. The timing sequence of these waveforms is very important to the correct operation of the Readout System (see expanded waveforms in Fig. 4-29). The Z-Axis Logic OFF Command at pin 14 is produced first. This negative-going signal provides a blanking pulse to the Z-Axis Logic stage (see diagram 2) to blank the CRT before the display is switched to the Readout System. It also produces the Strobe pulse through R2137, Q2138, and CR2142 to signal other stages within the Readout System to begin the sequence necessary

Circuit Description—7603/R7603 Service

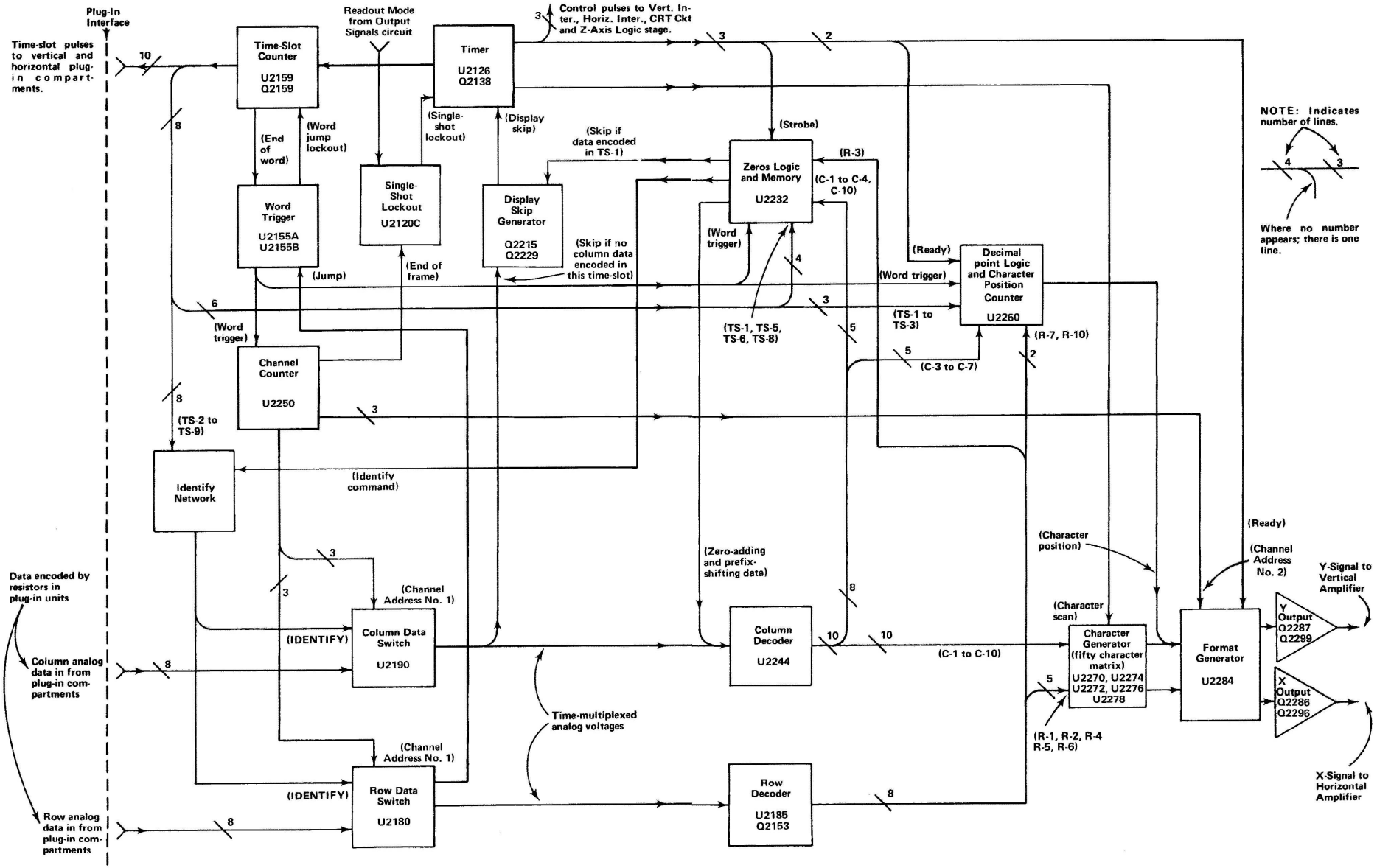


Fig. 4-27. Detailed block diagram of Readout System.

Fig. 4-27. Detailed block diagram of Readout System (cont).

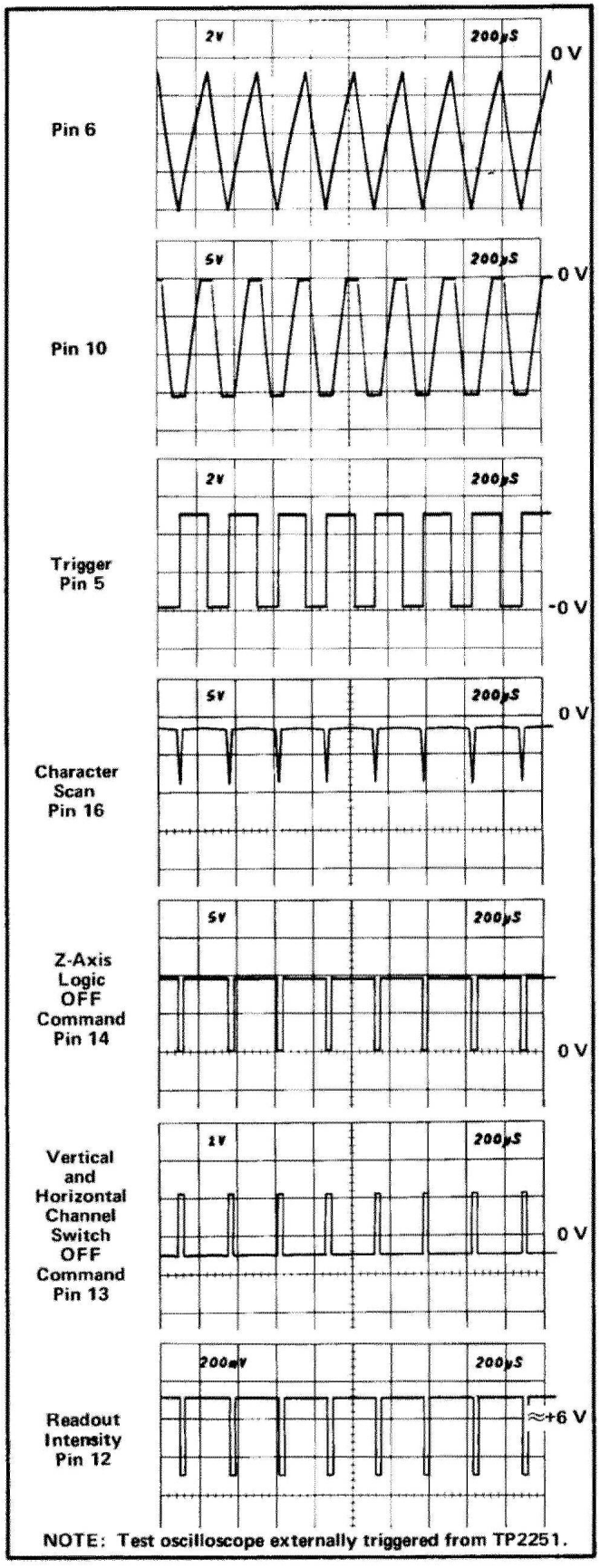


Fig. 4-28. Output waveforms of Timer stage.

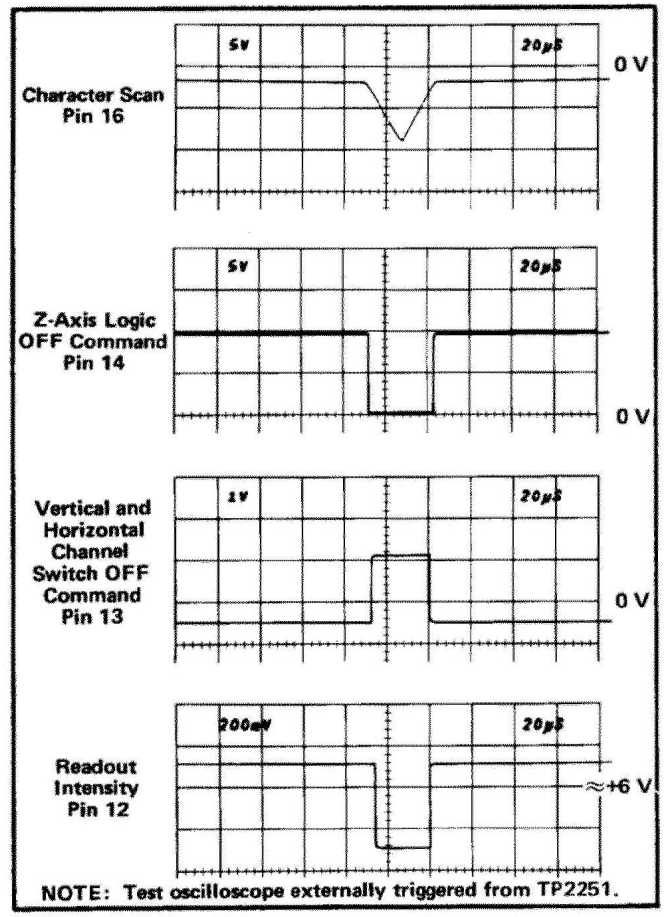


Fig. 4-29. Detail of outputs at pins 12, 13, 14, and 16 of U2126.

to produce a character. The collector of Q2138 is also connected to Character Generator No. 2, U2272 through C2140, CR2140. This activated U2272 during the quiescent period of the Strobe pulse (collector of Q2138 negative) and diverts the output current of Row Decoder U2185 to row 2. The purpose of this configuration is to prevent the Zeros Logic and Memory stage U2232 from storing incorrect data during the quiescent period of the Strobe pulse. When the Strobe pulse goes positive, CR2140 is reverse biased to disconnect Q2138 from U2272 and allow the Row Decoder stage to operate in the normal manner.

The next signal to be produced is the Vertical/Horizontal Channel Switch OFF Command at pin 13. This positive-going signal disconnects the plug-in signals in the vertical and horizontal deflection systems so the plug-in units do not control the position of the CRT beam during the readout display. The Ready signal derived from this output is connected to the Decimal Point Logic and Character Position Counter stage and the Format Generator stage (see diagram 10). The Readout Intensity output at pin 12 is produced next. This current is connected to the CRT Circuit to unblank the CRT to the intensity level determined by READOUT intensity control R2124. The Character Scan ramp at pin 16 started to go negative as this

timing sequence began. However, character-generation does not start until the readout intensity level has been established. The triangular Character Scan ramp runs negatively from about −2 volts to about −8.5 volts and then returns back to the original level. This waveform provides the scanning signal for the Character Generator stages (see diagram 10). The Full Character Scan adjustment R2128 sets the DC level of the Character Scan ramp to provide complete characters on the display.

The Timer stage operates in one of two modes as controlled by the Display-Skip level at pin 4. The basic mode just described is a condition which does not occur unless all ten characters of each word (60 characters total) are displayed on the CRT. Under typical conditions only a few characters are displayed in each word. The Display-Skip level at pin 4 determines the period of the Timer output signal. When a character is to be generated, pin 4 is LO and the circuit operates as just described. However, when a character is not to be displayed, a HI level is applied to pin 4 of U2126 through CR2125 from the Display-Skip Generator stage. This signal causes the Timer to shorten its period of operation to about 210 microseconds. The waveforms shown in Fig. 4-30 show the operation of the Timer stage when the Display-Skip condition occurs for all positions in a word. Notice that there is no output at pin 12, 13, 14, and 16 under this condition. This means that the CRT display is not interrupted to display characters. Also notice that the triangle waveform at pin 6 does not go as far negative and that the negative portion of the trapezoidal waveform at pin 10 is shorter. Complete details on operation of the Display-Skip Generator are given later.

The Single-Shot Lockout level at pin 2 determines the operating mode of U2126. If this level is LO, the Timer operates as just described. However, if the Single-Shot Lockout stage sets a HI level at this pin, the Timer stage is locked out and can not produce any output signals (see Single-Shot Lockout description for further information).

The READOUT intensity control R2124 sets the intensity of the readout display independently of the INTENSITY control. The READOUT intensity control also provides a means of turning the Readout System off when a readout display is not desired. When R2124 is turned fully counterclockwise, switch S102 opens. The current to pin 11 of U2126 is interrupted and at the same time a positive voltage is applied to pin 4 through R2122 and CR2124. This positive voltage switches the stage to the same conditions as were present under the Display-Skip condition. Therefore, the CRT display is not interrupted to present characters. However, time-slot pulse continue to be generated.

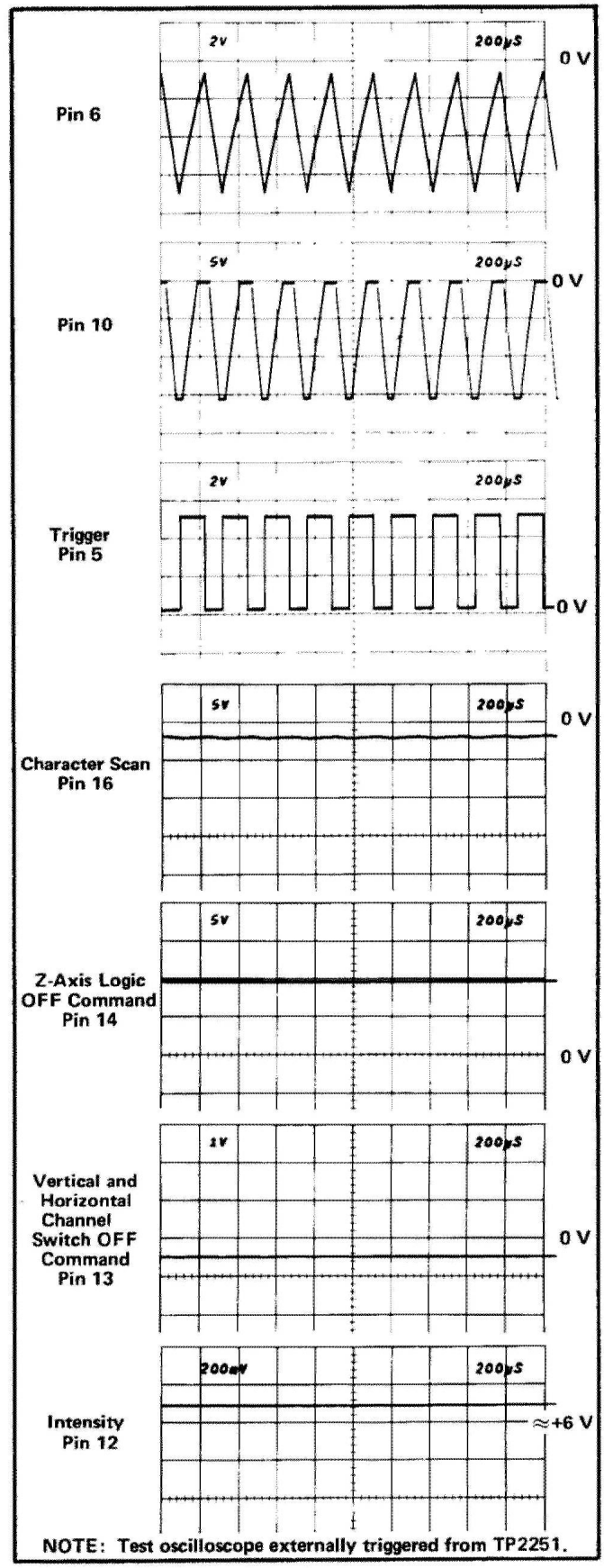


Fig. 4-30. Timer stage operation when Display-Skip condition occurs.

Time-Slot Counter

Time-Slot Counter U2126 is a sequential switch which directs the trapezoidal waveform input at pin 8 to one of its 10 output lines. These time-slot pulses are used to interrogate the plug-in units to obtain data for the Readout System. The Trigger pulse at pin 15 switches the Time-Slot Counter to the next output line; the output signal is sequenced consecutively from time-slot 1 through time-slot 10. Fig. 4-31 shows the time-relationship of the time-slot pulses. Notice that only one of the lines carries a time-slot pulse at any given time. When time-slot 10 is completed, a negative-going End-of-Word pulse is produced at pin 2. The End-of-Word pulse provides a drive pulse for the Word Trigger stage and also provides an enabling level to the Display-Skip Generator during time-slot 1 only.

Pin 16 is a reset input for the Time-Slot Counter. When this pin is held LO, the Time-Slot Counter resets to time-slot 1. The Time-Slot Counter can be reset in this manner only when a Jump signal is received by U2155C (see following discussion).

Word Trigger

The Word Trigger stage is made up of the 4 two-input NOR gates contained in U2155. Quiescently, pin 2 of U2155A is LO as established by the operating conditions of U2155D and U2155C. Therefore, the LO End-of-Word pulse produced by the Time-Slot Counter results in a HI level at pin 1 of U2155A. This level is inverted by U2155B to provide a negative-going advance pulse to the Channel Counter.

An advance pulse is also produced by U2155A when a Jump signal is received at pin 8 of U2155C. This condition can occur during any time-slot (see Row Decoder for further information on origin of the Jump signal). U2155D and U2155C are connected as a bistable flip-flop. The positive-going Jump signal at pin 8 of U2155C produces a LO at pin 10. This LO is inverted by U2155D to produce a HI at pin 13, which allows pin 9 of U2155C to be pulled HI through R2155. The flip-flop has now been set and it remains in this condition until reset, even though the Jump signal at pin 8 returns to its LO level. The HI output level at pin 13 turns on Q2159 through R2158 to pull pin 16 of the Time-Slot Counter LO. This resets the Time-Slot Counter to time-slot 1 and holds it there until U2155C is reset. At the same time, a HI level is applied to pin 4 of the Timer through CR2125 and CR2124. This HI level causes the Timer to operate in the display-skip mode so that a character is not generated.

The next Trigger pulse is not recognized by the Time-Slot Counter since U2159 is locked in time-slot 1 by U2155. However, this Trigger pulse resets the Word Trigger

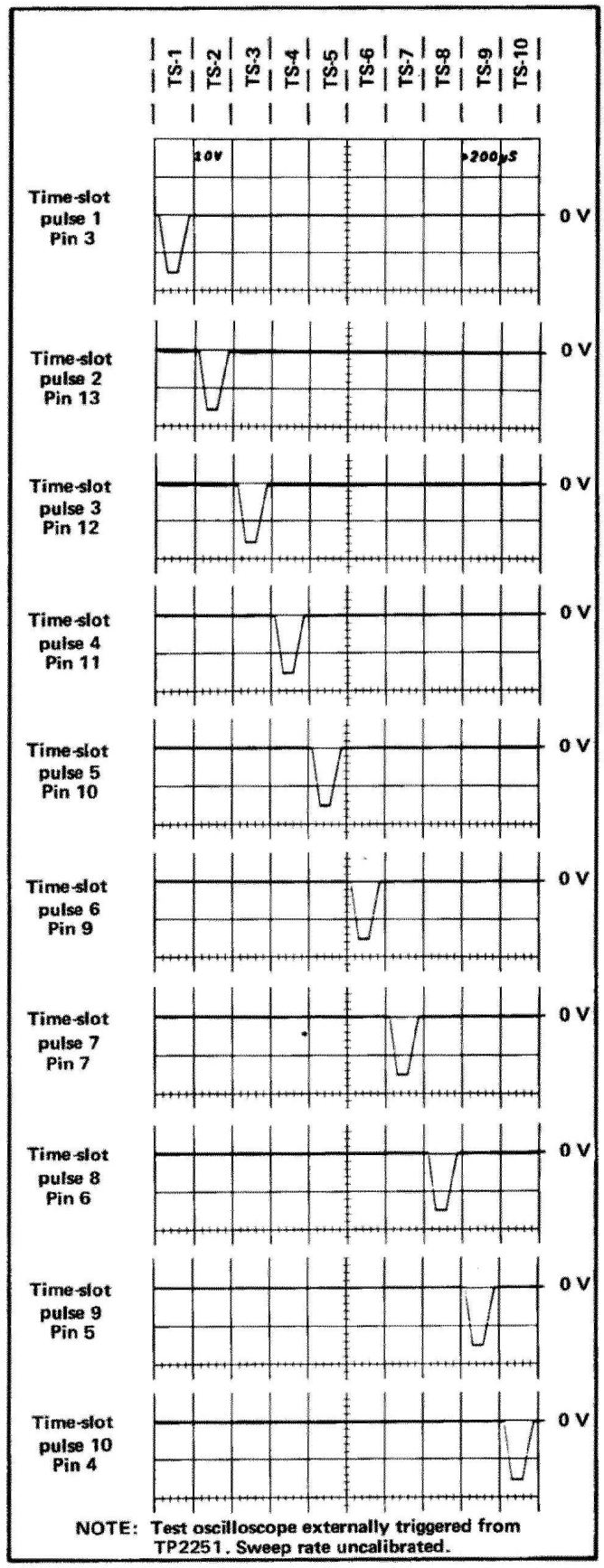


Fig. 4-31. Time relationship of the time-slot (TS) pulses produced by U2126.

stage through C2155. Pin 13 of U2155D goes LO to enable the Time-Slot Counter and Timer stages for the next time-slot pulse. At the same time, the negative-going edge produced at U2155D switches output states which is connected to pin 3 of U2155D. This results in a negative-going Word Trigger output at pin 4 of U2155B to advance the Channel Counter to the next word. When the next Trigger pulse is received at pin 15, the Time-Slot Counter returns to the normal sequence of operation and produces an output on the time-slot 1 line.

Channel Counter

The Channel Counter, made up of integrated circuit U2250 is a binary counter which produces the Channel Address code for the Column and Row Decoder stages and the Format Generator stage. This code instructs these stages to sequentially select and display the six channels of data from the plug-in units. The input channel which is displayed with each combination of the Channel Address code is given in the discussion of the applicable stages.

Single-Shot Lockout

Q2108, Q2117, and U2120 makes up the Single-Shot Lockout stage. This stage allows a single readout frame (Six complete words) to be displayed on the CRT, after which the Readout System is locked out so further readout displays are not presented until the circuit is reset. U2120C and U2120B are connected to form a bistable flip-flop. For normal operation, pin 3 of U2120 is pulled HI through R2108. This activates U2120C to result in a LO output level at pin 10. This level enables the Timer stage so it can operate in the free-running manner as described previously. The LO at pin 10 of U2120C is also applied to pin 5 of U2120B. Since pin 6 of U2120A is LO, U2120B is disabled and its output goes HI.

The output of this stage remains LO to allow U2126 to operate in the free-running mode until a LO is received at pin 8 of U2120C. When this occurs, the output level at pin 10 of U2120C does not change immediately. However, the Readout System is now enabled as far as the single-shot lockout function is concerned. If the Channel Counter has not completed word six (Channel 2 of the Horizontal unit), the Readout System continues to operate in the normal manner. However, when word six is completed, a positive-going End-of-Frame pulse is produced at pin 9 of U2120B as the Channel Counter shifts to the code necessary to display word one. This pulse is coupled to pin 3 of U2120A and pin 12 of U2120D. The momentary HI at pin 3 activates U2120B and its output goes LO to disable U2120C (pin 3 already LO). The output of U2120C goes HI to disable the Timer so it operates in the display-skip mode. The HI at pin 10 of U2120C also holds U2120B enabled so it maintains control of the flip-flop.

The Single-Shot Lockout stage remains in this condition until a positive-going trigger pulse is applied to pin 8 of U2120C. This trigger pulse produces a LO at pin 10 of U2120C which enables U2120B and disables U2120C. Now, the Timer can operate in the normal manner for another complete frame. When word six is completed, the Channel Counter produces another End-of-Frame pulse to again lock out the Timer stage.

Encoding the Data

Data is conveyed from the plug-in units to the Readout System in the form of an analog code having up to 11 current levels (from zero to one milliampere in 100 microampere steps). The characters which can be selected by the encoded data are shown on the Character Selection Matrix (see Fig. 4-25). Each character requires two currents to define it; these currents are identified as the column current and the row current which correspond to the column and row of the matrix. The column and row data is encoded by resistive programming in the plug-in units. Fig. 4-32 shows a typical encoding scheme for a voltage-sensing amplifier plug-in unit. Notice that the 10 time-slot (TS) pulses produced by the Time-Slot Counter stage are connected to the plug-in unit. However, time-slots 5, 6, 7, and 10 are not used by the plug-in unit to encode data when using the Standard Readout Format (see Table 4-2 for Standard Readout Format). The amplitude of the time-slot pulses is exactly −15 volts as determined by the Timer stage. Therefore, the resultant output current from the plug-in units can be accurately controlled by the programming resistors in the plug-in units.

For example, in Fig. 4-32, resistors R10 through R90 control the row analog data which is connected back to the Readout System. These resistors are of fixed value and define the format in which the information will be presented by the Readout System. Fig. 4-33A shows an idealized output current waveform of row analog data which results from the 10 time-slot pulses. Each of the steps of current shown in these waveforms corresponds to 100 microamperes of current. The row numbers on the left-hand side of the waveform correspond to the rows in the Character Selection Matrix shown in Fig. 4-35. The row analog data is connected back to the Readout System via terminal B37 of the plug-in interface.

The Column analog data is defined by resistors R110 through R190. The program resistors are connected to the time-slot lines by switch closures to encode the desired data. The data as encoded by the circuit shown in Fig. 4-32 indicates a 100 microvolt sensitivity with the display inverted and calibrated vertical deflection factors. This results in the idealized output current waveforms shown in Fig. 4-33B at the column analog data output, terminal A37 of the plug-in interface. Resistor R111, connected between time-slot 1 and the column analog data output, encodes two units of current during time-slot 1. Referring to the

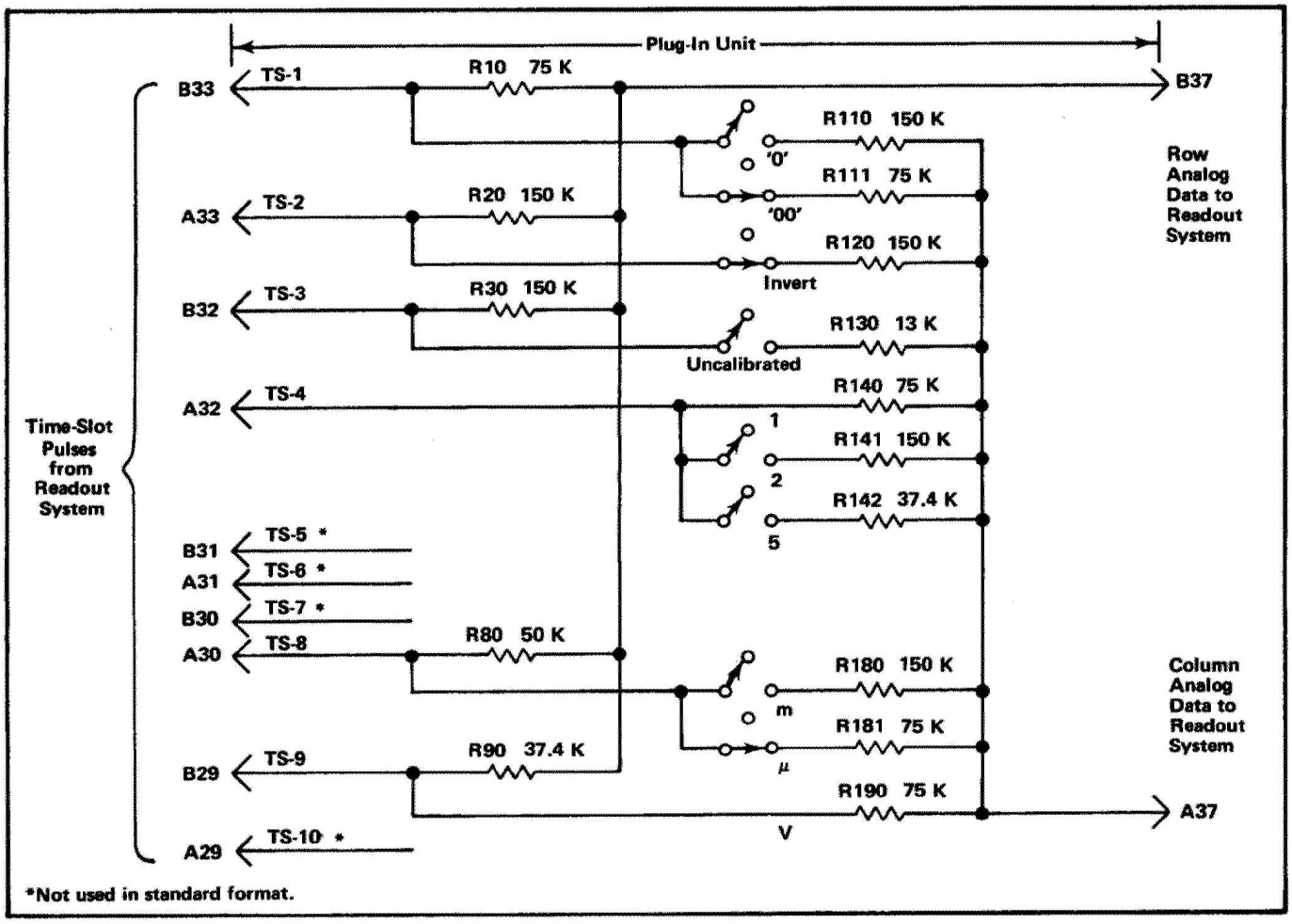


Fig. 4-32. Typical encoding scheme for voltage-sensing amplifier plug-in unit. Coding shown for deflection factor of 100 microvolts.

Character Selection Matrix, two units of column current along with the two units of row current encoded by R10 (row 3) indicates that two zeros should be added to the display. Resistor R120 adds one unit of column current during time-slot 2 and along with the one unit of current from the row output, the Readout System is instructed to add an invert arrow to the display. R130 is not connected to the time-slot 3 line since the vertical deflection factors are calibrated. Therefore, there is no column current output during this time-slot and there is no display on the CRT (see Display-Skip Generator for further information). During time-slot 4, two units of column current are encoded by R140. There is no row current encoded during this time-slot and this results in the numeral 1 being displayed on the CRT. Neither row nor column analog data is encoded during time-slots 5, 6, and 7 as defined by the Standard Readout Format. During time-slot 8, two units of column current and three units of row current are encoded by resistors R181 and R80 respectively. This addresses the μ prefix in the Character Selection Matrix. The final data output is provided from time-slot 9 by R190 connected to the column output and R90 to the row output. These resistors encode three units of column current and four units of row current to cause a V (volts) to be displayed. Time-slot 10 is not encoded in accordance with the Standard Readout Format. The resultant CRT readout will be ↓ 100 μV.

In the above example, the row analog data was programmed to define which row of the Character Selection Matrix was addressed to obtain information in each time-slot. The column data changes to encode the applicable readout data as the operating conditions change. For example, if the variable control of the plug-in unit was activated, R130 would be connected between time-slot 3 and the column analog data output lines. This encodes 10 units of column current (see shaded area in time-slot 3 of the waveform shown in Fig. 4-33B). Since one unit of row current is also encoded during this time-slot by R30, a > symbol is added to the display. The CRT readout will now say ↓ >100 μV. In a similar manner, the other switches can change the encoded data for the column output and thereby change the readout display. See the descriptions which follow for decoding this information.

The column analog data encoded by the plug-in can be modified by attenuator probes connected to the input

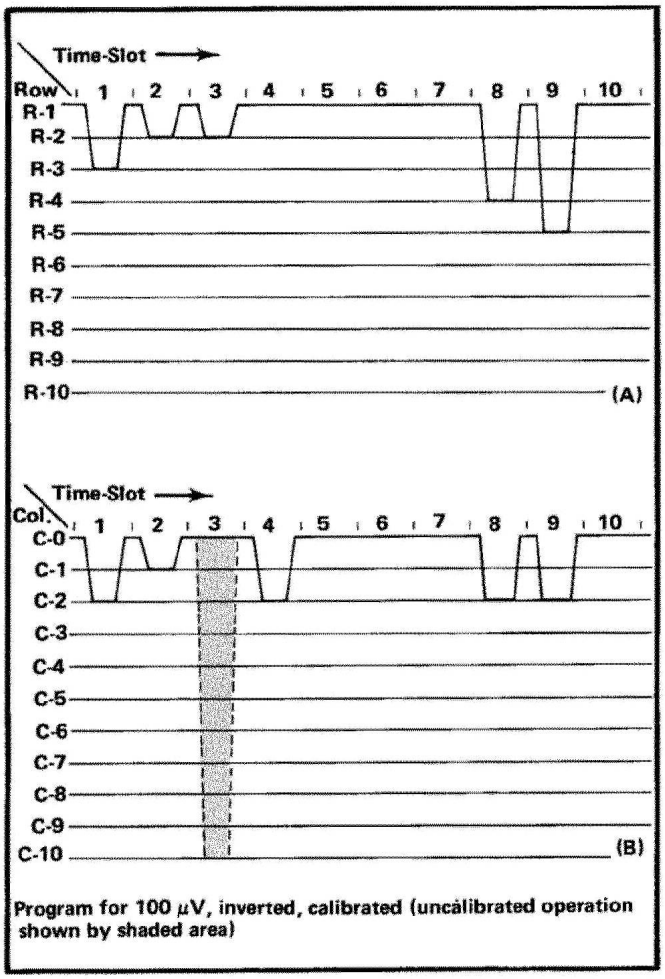


Fig. 4-33. Idealized current waveforms of: (A) Row analog data, (B) Column analog data.

connectors of vertical plug-in units. A special coding ring around the input connector of the plug-in unit senses the attenuation ratio of the probe (with readout-coded probes only). The probe contains a resistor which results in additional column current. For example, if a 10X attenuator probe is connected to a plug-in with the coding for 100 microvolts as shown in Fig. 4-32, an additional unit of current is added to the column analog data during time-slot 1. Since two units of current were encoded by R111 (see Fig. 4-32), this additional current results in a total of three units of column analog current during this time-slot. Referring to the Character Selection Matrix, three units of column current along with the two units of row current encoded by R10 indicates that the prefix should be reduced. Since this instruction occurs in the same time-slot which previously indicated that two zeros should be added to the display and only one instruction can be encoded during a time-slot, the zeros do not appear in the display. The CRT readout will now be changed to 1 mV (readout) program produced by plug-in same as for previous example.

Likewise, if a 100X readout-coded probe is connected to the input of the plug-in unit, the column current during time-slot 1 will be increased two units for a total of four units of column current. This addresses an instruction in the Character Selection Matrix which reduces the prefix and adds one zero to the display. The resultant CRT readout with the previous program is 10 mV.

Three other lines of information are connected from the plug-in compartments to the Readout System. The column and row analog data from channel 2 of a dual-channel plug-in are connected to the Readout System through terminals A38 and B38 of the plug-in interface, respectively. Force readout information is encoded on terminal A35; function of this input is described under Column and Row Data Switches.

The preceding information gave a typical example of encoding data from an amplifier plug-in unit. Specific encoding data and circuitry is shown in the individual plug-in unit manual.

Column and Row Data Switches

The readout data from the plug-in units is connected to the Column and Row Data Switch stages in the Readout System. A column-data line and a row-data line convey analog data from each of the eight data sources (two channels from each of the four plug-in compartments).

TABLE 4-3

Channel Address

Pin 1 U2232 "Identify" Command	Pin 11 U2250	Pin 8 U2250	Pin 9 U2250	Channel Selected
HI	HI	HI	HI	Channel 1 Left Vertical
HI	HI	HI	LO	Channel 2 Left Vertical
HI	HI	LO	HI	Channel 1 Right Vertical
HI	HI	LO	LO	Channel 2 Right Vertical
HI	LO	HI	HI	Channel 1 Horizontal
HI	LO	HI	LO	Channel 2 Horizontal

The Column Data Switch U2190 and the Row Data Switch U2180 receive the Channel Address No. 1 code from the Channel Counter. This binary code directs the Column Data Switch and the Row Data Switch as to which channel should be the source of the readout data. Table 4-3

gives the eight combinations of the Channel Address No. 1 code and the resultant channel which is selected with each combination. These stages have nine inputs and provide a single time-multiplexed output at pin 7 which includes the information from all of the input channels. Eight of the nine inputs to each stage originate in the plug-in units; the ninth input comes from a special data-encoding network composed of resistors R2201 through R2209 and R2191 through R2199 (see Zeros Logic and Memory description for further information on ninth channel).

In addition to the data inputs from the plug-in units, channel-inhibit inputs are provided from each of the plug-in units. The channel inhibit lines are LO only when the associated plug-in unit has been selected for display. When a plug-in unit is not selected, the respective line is HI which forward biases the associated diode CR2162, CR2163, CR2167, CR2166, CR2171, CR2170, CR2175, or CR1174 to by-pass the encoded data from this plug-in. However, since it may be desired to display information from special-purpose plug-ins even though they do not produce a normal waveform display on the CRT, a feature is provided to over-ride the channel inhibit. This is done by applying a LO to the associated forcing over-ride input. The LO level diverts the HI channel inhibit current and allows the data from this plug-in unit to reach the Column Data Switch, even though it has not been selected for display by the mode switches.

Display-Skip Generator

The Display-Skip Generator, Q2215, Q2223, Q2229, and Q2225 monitors the time-multiplexed column data at the output of the Column Data Switch during each time-slot to determine if the information at this point is valid data which should result in a CRT display. The voltage at the base of Q2215B is set by divider R2219, R2220, and R2221. Quiescently, there is about 100 microamperes of current flowing through R2213 and R2214 from Q2240 and the Zeros Logic and Memory stage (purpose of this quiescent current will be discussed in connection with the Zeros Logic and Memory stage). This current biases Q2215A so its base is about 0.2 volt more positive than the base of Q2215B in the absence of column data. Therefore, since Q2215A and Q2215B are connected as a comparator, Q2215A will remain on unless its base is pulled more negative than the base of Q2215B. The analog data output from the Column Data Switch produces a 0.5 volt change at the base of Q2215A for each unit of column current that has been encoded by the plug-in unit. Therefore, whenever any information appears at the output of the Column Data Switch, the base of Q2215A is pulled more negative than the base of Q2215B resulting in a negative (LO) Display-Skip output to the Timer stage through Q2225. Recall that a LO was necessary at the skip input of the Timer so it could perform the complete sequence necessary to display a character.

Q2223-Q2229 also provide display-skip action. The End-of-Word level connected to their emitters through R2229 is LO only during time-slot 1. This means that Q2223-Q2229 are enabled only during time-slot. These transistors allow the Zeros Logic and Memory stage to generate a display-skip signal during time-slot 1 when information has been stored in memory which is not to be displayed on the CRT (further information given under Zeros Logic and Memory discussion).

Column and Row Decoder

The Column Decoder U2244 and Row Decoder U2185 sense the magnitude of the analog voltages at their inputs and produce a binary output on one of ten lines corresponding to the column or row data which was encoded by the plug-in. These outputs provide the Column Digital Data and Row Digital Data which is used by the Character Generator stages to select the desired character for display on the CRT. The column and row data is also used throughout the Readout System to perform other functions. The input current at pin 9 of the Column Decoder stage is steered to only one of the ten Column Digital Data outputs. The size of the character which will be displayed on the CRT is determined by the value of R2227. When a display-skip signal is present (collector of Q2225 is HI), pin 9 is pulled HI through CR2226. This ensures that no current is connected to the Character Generator stage under this condition. Notice the corresponding input on the Row Decoder. This input is connected to ground and causes only one of the ten row outputs to saturate to ground.

The network at the input of the Row Decoder, made up of Q2153 and its associated components, is a Row 13 detector which produces the Jump command. This row current is encoded by special-purpose plug-ins to cause all or part of a word to be jumped. Whenever row 13 (thirteen units of row current; 1.3 milliamperes) is encoded, the base of Q2153 is pulled negative enough so that this transistor is reverse biased to produce a HI Jump output at its collector. This Jump command is connected to the Word Trigger stage (diagram 10) to advance the Channel Counter stage to the next word and to reset the Time-Slot Counter to time-slot 1.

Zeros Logic and Memory

The Zeros Logic and Memory stage U2232 stores data encoded by the plug-in units to provide zeros-adding and prefix-shifting logic for the Readout System. The Strobe pulse at pin 15 goes positive when the data has stabilized and can be inspected. This activates the Zeros Logic and Memory stage so it can store the encoded data. A block representation of the memory sequence is shown in Fig. 4-34. Typical output waveforms for the five possible input conditions that can occur are shown in Fig. 4-35. When time-slot 1 occurs, a store command is given to all of the

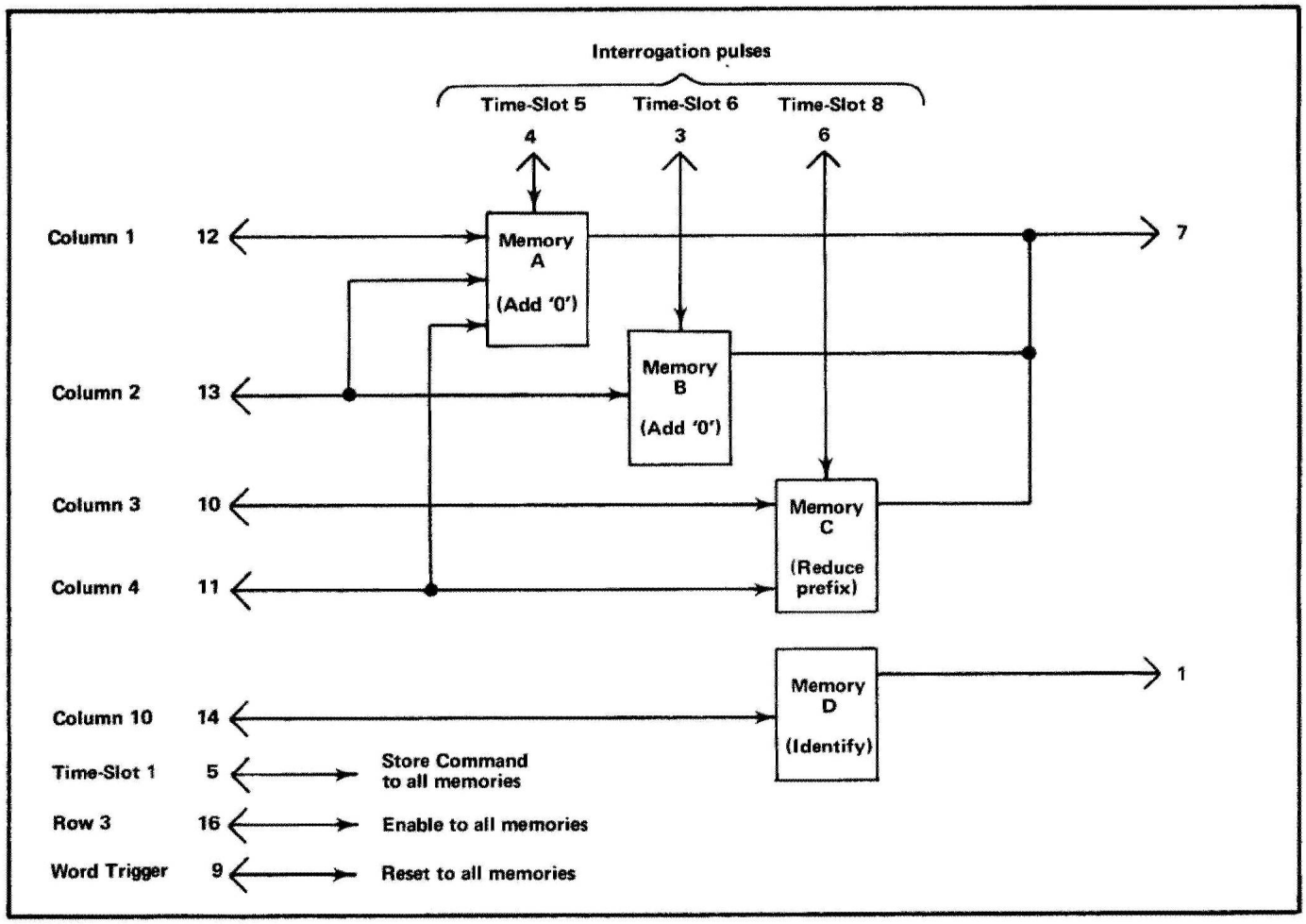


Fig. 4-34. Block representation of memory sequence in U2232.

memories. If the plug-in unit encoded data for column 1, 2, 3, 4, or 10 during time-slot 1, the appropriate memory (or memories) is set. Notice that row 3 information from the Row Decoder must also be present at pin 16 for data to be stored in the memory of U2232. If data was encoded during time-slot 1, a negative-going output is produced at pin 7 as the memories are being set. This negative-going pulse is connected to the base of Q2229 in the Display-Skip Generator to produce a Display-Skip output. Since the information that was encoded during time-slot 1 was only provided to set the memories and was not intended to be displayed on the CRT at this time, the display-skip output prevents a readout display during this time-slot.

During time-slot 5, memory A is interrogated. If information was stored in this memory, a positive-going output is produced at pin 7. This pulse is connected to pin 10 of the Column Decoder through Q2240 to add one unit of current at the input of the Column Decoder. This produces a zero after the character displayed on the CRT during time-slot 4. During time-slot 6, memory B is interrogated to see if another zero should be added. If another zero is necessary, a second positive output is produced at pin 7 which again results in a column 1 output from the Column Decoder and a second zero in the CRT display.

Finally, memory C is interrogated during time-slot 8 to obtain information on whether the prefix should be reduced or left at the value which was encoded. If data has been encoded which calls for a reduction in prefix, a negative-going output level is produced at pin 7. This negative level subtracts one unit of column current from the data at the input to the Column Decoder. Notice on the Character Selection Matrix of Fig. 4-24 that a reduction of one column when row 4 is programmed results in a one unit reduction of the prefix. For example, with the 100 μV program shown in Fig. 4-31, if the data received from the plug-in called for a reduction in prefix, the CRT readout would be changed to 1 mV (zeros deleted by program; see Encoding the Data).

The 100 microamperes of quiescent current through R2213 and R2214 that was provided by Q2240 (see Display-Skip Generator) allows the prefix to be reduced

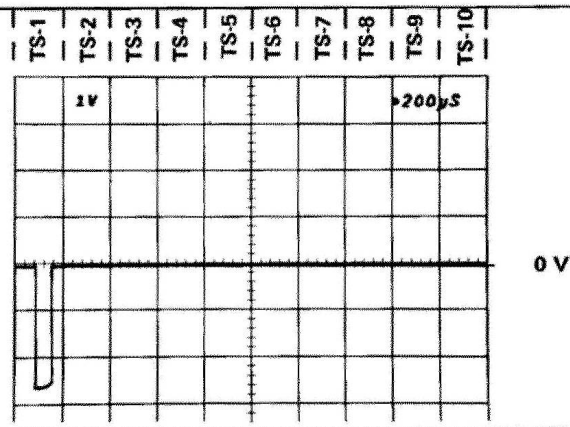
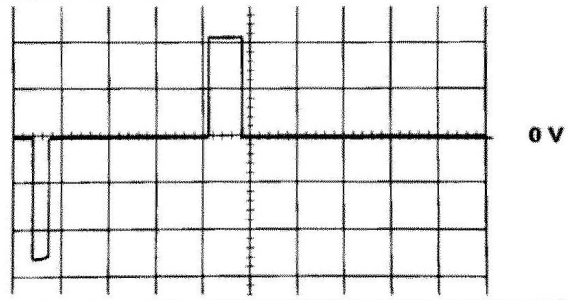
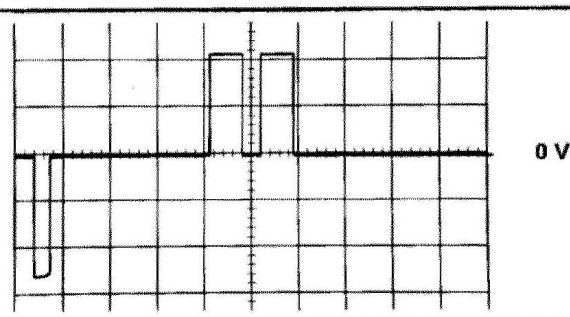
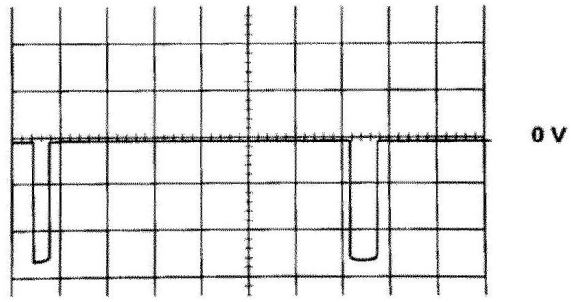
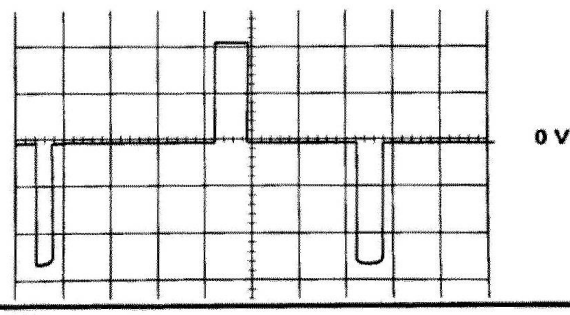
Input Pins of Zeros Logic & Memory	Command	Time Slot
14	IDENTIFY	
12	Add one zero	
13	Add two zeros	
10	Decrease prefix	
11	Decrease prefix and add one zero	

Fig. 4-35. Typical output waveforms for Zeros Logic and Memory stage operation (at pin 7 of U2232).

from m (100 microamperes column current; column 1) to no prefix (zero column current; column zero) so only the unit of measurement encoded during time-slot 9 is displayed. Notice that reducing the prefix program from column 1 to column 0 programs the Readout System to not display a character at this readout location.

A further feature of the Zeros Logic and Memory is the Identify function. If 10 units of column current are encoded by the plug-in unit along with row 3 during time-slot 1, the Zeros Logic and Memory produces a negative-going output pulse at pin 1 which switches the Column Data Switch and Row Data Switch to the ninth channel. Then, time-slot pulses 2 through 9 encode an output current through resistors R2191-R2199 for column data and R2201-R2209 for row data. This provides the currents necessary to display the word IDENTIFY on the CRT in the word position allotted to the channel which originated the Identify command. After completion of this word, the Column Data Switch and Row Data Switch continue with the next word in the sequence.

The Word Trigger signal from the Word Trigger stage is connected to pin 9 of U2232 through C2242. At the end of each word of readout information, this pulse goes LO. This erases the four memories in the Zeros Logic and Memory in preparation for the data to be received from the next channel.

Character Generators

The Character Generator stage consists of five similar integrated circuits U2270, U2272, U2274, U2276, and U2278, which generate the X (horizontal) and Y (vertical) outputs at pins 16 and 1 respectively to produce the character displayed on the CRT. Each integrated circuit can produce 10 individual characters. U2270, which is designated as the "Numerals" Character Generator, can produce the numerals 0 through 9 shown in row 1 of the Character Selection Matrix (Fig. 4-24). U2272 can produce the symbols shown in row 2 of the Character Selection Matrix and U2274 produces the prefixes and some letters of the alphabet which are used as prefixes in row 4. U2276 and U2278 produce the remaining letters of the alphabet shown in rows 5 and 6 of the Character Selection Matrix. All of the stages receive the column digital data from Column Decoder U2244 in parallel. However, only one of the character generators receives row data at a particular time; only the stage which receives both row and column data is activated. For example, if column 2 is encoded by a plug-in unit, the five Character Generators are enabled so that either a 1, < μ, V, or an N can be produced. However, if at the same time row 4 has also been encoded by the plug-in unit, only the Prefix Character Generator U2274 will produce an output to result in a μ displayed on the screen. This integrated circuit provides current outputs to the Format Generator which produce the selected character on the CRT. In a similar manner, any of the 50 characters shown in the Character Selection Matrix can be displayed by correct addressing of the row and column.

Decimal Point Logic and Character Position Counter

The Decimal Point Logic and Character Position Counter stage U2260 performs two functions. The first function is to produce a staircase current which is added to the X (horizontal) signal to space the characters horizontally on the CRT. After each character is generated, the negative-going edge of the Ready signal at pin 5 advances the Character Position Counter. This produces a current step output at pin 3 which, when added to the X signal, causes the next character to be produced one character space to the right. This stage can also be advanced when a Space instruction is encoded by the plug-in unit so that a space is left between the displayed characters on the CRT. Row 10 information from the Row Decoder is connected to pin 4 of U2260 through R2265. When row 10 and column 0 are encoded, the output of this stage advances one step to move the next character another space to the right. However, under this condition, no display is produced on the CRT during this time-slot.

Time-slot pulses 1, 2, and 3 are also connected to pin 4 of U2260 through VR2262, VR2263, and VR2264 respectively and R2262-R2265. This configuration adds a space to the displayed word during time-slots 1, 2, and 3 even if information is not encoded for display during these time-slots. With this feature, the information which is displayed during time-slot 4 (1-2-5 data) always starts in the fourth character position whether data has been displayed in the previous time-slots or not. Therefore, the resultant CRT display does not shift position as normal/invert or cal/uncal information is encoded by the plug-in. The Word Trigger pulse connected to pin 8 of U2260 through C2255 resets the Character Position Counter to the first character position at the end of each word.

The Decimal Point Logic portion of this stage allows decimal points to be added to the CRT display as encoded by the plug-in units. When row 7 is encoded in coincidence with columns 3 through 7 (usually encoded during time-slot 1), a decimal point is placed at one of the five locations on the CRT identified in row 7 of the Character Selection Matrix (Fig. 4-24). This instruction refers to the decimal point location in relation to the total number of characters that can be displayed on the CRT (see Fig. 4-36). For example, if column 3 and row 7 are encoded during time-lost 1, the system is instructed to place a decimal point in location No. 3. As shown in Fig. 4-36, this displays a decimal point before the third character that can be displayed on the CRT (first three time-slots produce a space whether data is encoded or not; see previous paragraph). The simultaneous application of row 7 data to the Y-input

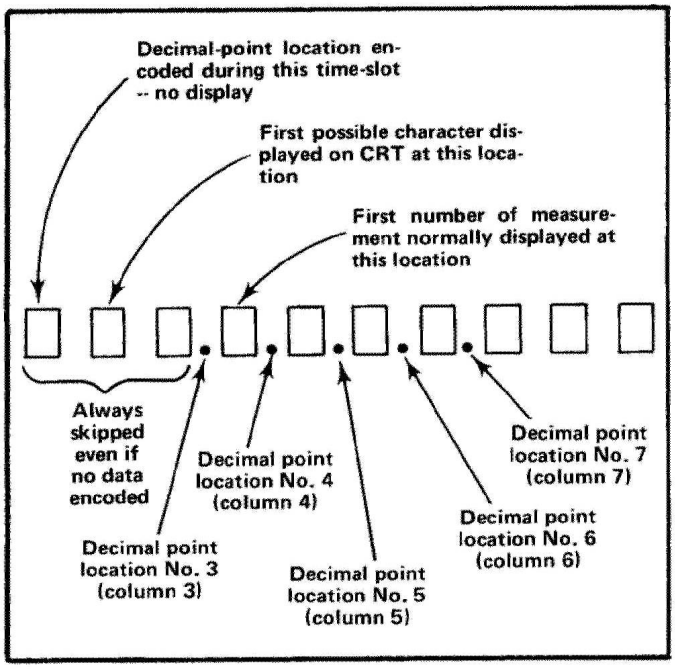


Fig. 4-36. Readout word relating 10 possible character locations to the decimal-point instructions that can be encoded and the resulting display.

of the Format Generator through R2280 raises the decimal point so it appears between the displayed characters.

When decimal-point data is encoded, the CRT is unblanked so a readout display is presented. However, since row 7 does not activate any of the five Character Generators, the CRT beam is not deflected but instead remains in a fixed position to display a decimal point between the characters along the bottom line of the readout word. After the decimal point is produced in the addressed location, the CRT beam returns to the location indicated by the Character Position Counter to produce the remainder of the display.

Format Generator

The X- and Y-deflection signals produced by the Character Generator stage, are connected to pins 2 and 7 respectively of Format Generator U2284. The Channel Address No. 2 code from the Channel Counter is also connected to pins 1, 8, and 15 of this stage. The Channel Address No. 2 code directs the Format Generator to add current to the X and Y signals to deflect the CRT beam to the area of the CRT which is associated with the plug-in channel that originated the information (see Fig. 4-24). The Channel Address No. 2 Code and the resultant word positions are shown in Table 4-4. In addition, the character position current from the Decimal Point Logic and Character Position stage is added to the X (horizontal) input signal to space the characters horizontally on the CRT (see previous discussion). The Ready signal at pin 13 (coincident with Vertical/Horizontal Channel Switch OFF Command) activates this stage when a character is to be displayed on the CRT.

TABLE 4-4

Channel Address

Pin 11 U2250	Pin 8 U2250	Pin 9 U2250	Channel Displayed
LO	LO	LO	Channel 1 Left Vertical
LO	LO	HI	Channel 2 Left Vertical
LO	HI	LO	Channel 1 Right Vertical
LO	HI	HI	Channel 2 Right Vertical
HI	LO	LO	Channel 1 Horizontal
HI	LO	HI	Channel 2 Horizontal

Y-Output Amplifiers

The Y-output signal at pin 6 of U2284 is connected to the Y-Output Amplifier Q2287-Q2299. This stage provides a low impedance load for the Format Generator while providing isolation between the Readout System and the Vertical Amplifier. Vertical Separation adjustment R2291 changes the gain of this stage to control the vertical separation between the readout words displayed at the top and bottom of the graticule area.

X-Output Amplifier

The X-Output Amplifier Q2286-Q2296 operates similarly to the Y-Output Amplifier to provide the horizontal deflection from the readout signal available at pin 4 of U2284. The gain of this stage is fixed by the values of the resistors in the circuit.

Display Sequence

Fig. 4-37 shows a flow chart for the Readout System. This chart illustrates the sequence of events which occurs in the Readout System each time a character is generated and displayed on the CRT.