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**TECHNICAL MANUAL**

**OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT,  
AND GENERAL SUPPORT MAINTENANCE MANUAL  
INCLUDING REPAIR PARTS AND SPECIAL TOOLS LISTS  
FOR  
OSCILLOSCOPE, TEKTRONIX MODEL R7704  
(NSN 6625-00-007-8487)**

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**HEADQUARTERS, DEPARTMENT OF THE ARMY**

**8 SEPTEMBER 1980**

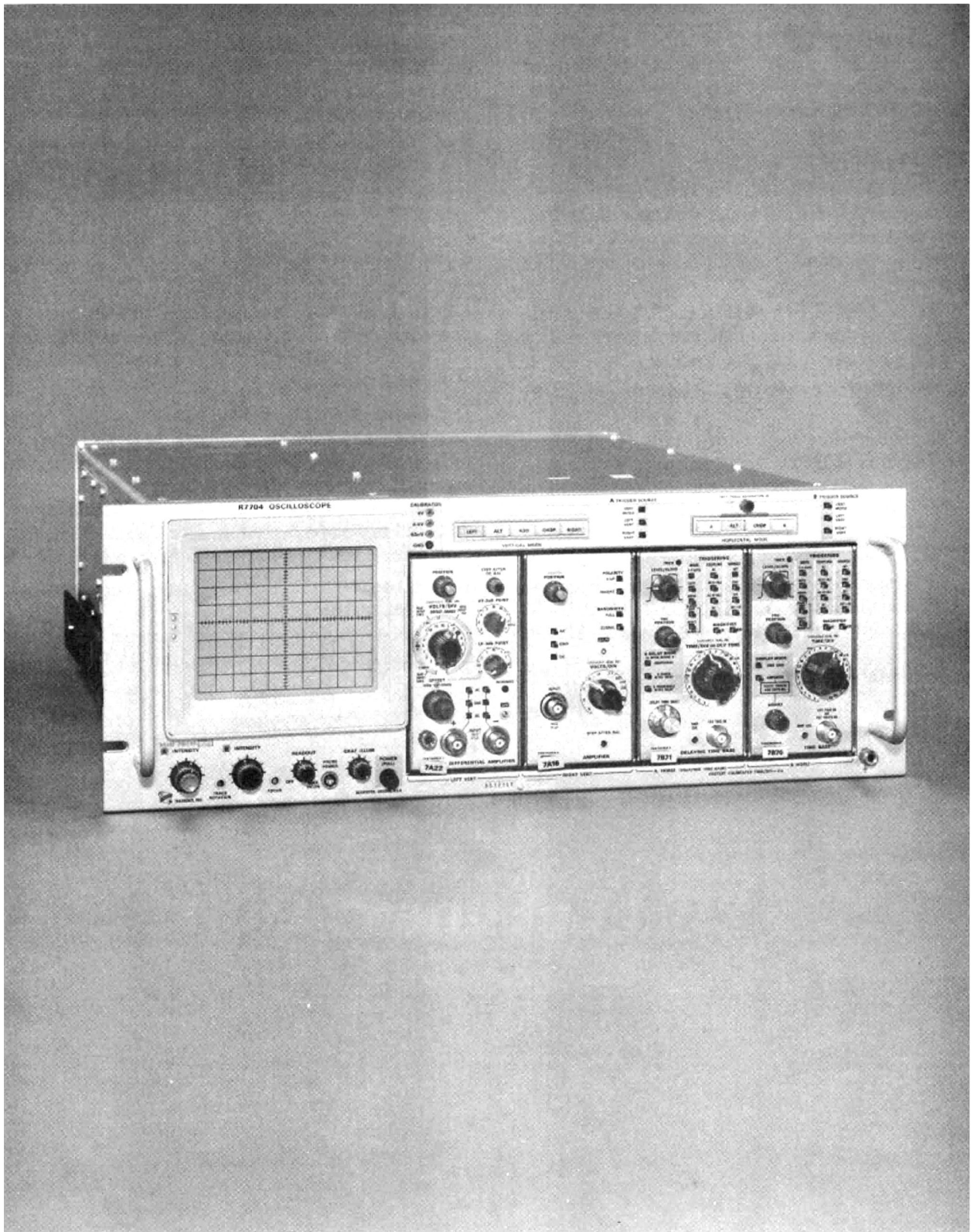


Fig. 1-1. The R7704 Oscilloscope

R7704

(A)



## SECTION 1 R7704 SPECIFICATION

*Change information, if any, affecting this section will be found at the rear of the manual.*

### Introduction

The Tektronix R7704 Oscilloscope is a solid-state, high performance instrument designed for mounting in a 19-inch rack (complete rackmounting information is given in Section 6). This instrument accepts Tektronix 7-series plug-in units to form a complete measurement system. The flexibility of this plug-in feature and the variety of plug-in units available allow the system to be used for many measurement applications.

The R7704 has four plug-in compartments. The left pair of plug-ins is connected to the vertical deflection system. The right pair is connected to the horizontal deflection system. Electronic switching between the plug-in units connected to each deflection system allows a dual-trace vertical display and/or a dual-sweep horizontal display. This instrument features regulated DC power supplies to assure that performance is not affected by variations in line voltage and frequency, or by changes in load due to the varying power requirements of the plug-in units. Maximum power consumption of this instrument is about 225 watts (60 hertz, 115-volt line).

The R7704 features a CRT with small spot size and high writing speed. Graticule area is 8 X 10 centimeters. In addition, the instrument contains a readout system to provide CRT display of alpha-numeric information from the plug-in units; data such as deflection factor, sweep rate, etc. can be encoded.

This instrument will meet the electrical characteristics listed in Table 1-1 following complete calibration as given in Section 5. The performance check procedure included in Section 5 provides a convenient method of checking instrument performance without making internal checks or adjustments. The following electrical characteristics apply over a calibration interval of 1000 hours and an ambient temperature range of 0°C to +50° C, except as otherwise indicated. Warmup time for given accuracy is 20 minutes.

### NOTE

**Many of the measurement capabilities of this instrument are determined by the choice of plug-in units. The following characteristics apply to the R7704 Oscilloscope only. See the system specification later in this section for characteristics of the complete system.**

TABLE 1-1.  
ELECTRICAL

Characteristic	Performance
<b>VERTICAL DEFLECTION SYSTEM</b>	
Deflection Factor	Compatible with all 7-series plug-in units.
Deflection Accuracy	Less than 1% difference between vertical compartments.
Low-Frequency Linearity	0.1 division or less compression or expansion of a center-screen two-division signal when positioned anywhere vertically within the graticule area.
Bandwidth	Varies with vertical plug-in selected.
Risetime	See System Specifications.

Characteristic	Performance Requirement
Isolation Between Vertical Compartments	At least 100:1 from DC to 150 megahertz.
Chopped Mode Repetition rate	One megahertz $\pm 20\%$ .
Time segment from each compartment	0.4 to 0.6 microsecond.
Delay Line	Permits viewing of leading edge of triggering signal
Difference in Delay Between Compartments	0.2 nanosecond or less.

TABLE 1-1. (cont)

Characteristic	Performance
Vertical Display Modes (selected by front-panel VERTICAL MODE switch)	LEFT: Left vertical unit only. ALT: Dual-trace, alternate between vertical units. ADD: Added algebraically. CHOP: Dual-trace, chopped between vertical units. RIGHT: Right vertical unit only.
Trace Separation Range for Dual-Sweep Modes	B trace can be positioned +4 to +6 or -4 to -6 divisions from the A trace.

**TRIGGERING**

Trigger Source (selected by front-panel A TRIGGER SOURCE and B TRIGGER SOURCE switches)	VERT MODE: Determined by vertical mode.  LEFT VERT: From left vertical unit only. RIGHT VERT: From right vertical unit only.
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**HORIZONTAL DEFLECTION SYSTEM**

Deflection Factor	Compatible with all 7-series plug-in units.
Deflection Accuracy	Less than 1% difference between compartments.
Fastest Calibrated Sweep Rate	Two nanoseconds/division.
Bandwidth at 10% Down	DC to at least three megahertz (10-division reference). DC to at least six megahertz (five-division reference).
Without phase correction	
With phase correction	DC to at least three megahertz (10-division reference).
Phase Shift Between Vertical and Horizontal Deflection Systems	2° or less from DC to at least 35 kilohertz.
Without phase correction	
With phase correction	Adjustable to less than 2° from DC to two megahertz.

TABLE 1-1. (cont)

Characteristic	Performance Requirement
Chopped Mode Repetition rate	200 kilohertz $\pm 20\%$ .
Time segment from each compartment	2.0 to 3.0 microseconds
Horizontal Display Modes (selected by front-panel HORIZONTAL MODE switch)	A: A horizontal unit only. ALT: Dual-sweep, alternate between horizontal units. ADD: Added alphabetically CHOP: Dual-sweep, chopped between horizontal units B: B horizontal unit only.

**CALIBRATOR**

Wave Shape	Square wave.
Polarity	Positive going with baseline at zero volts.
Output Voltage Open circuit	40 mV, 0.4 V, 4 V at front-panel pin jacks.  4 mV and 40 V available at internal circuit board connections.
Into 50 ohms	20 mV, 0.2 V, 0.4 V at front-panel pin jacks.
Output Current	40 milliamperes with current-loop accessory (012-0259-00) connected between 4 V pin jack and ground.
Repetition Rate	One kilohertz.
Accuracy	+15 ° C to +35°C 0°C to +50°C
Voltage and current	Within 1%. Within 2%.
Repetition rate	Within 0.25%. Within 0.5%.
Risetime and Fall-time	0.25 microsecond or less.
Duty Cycle	50% $\pm 0.1\%$ .

**EXTERNAL Z-AXIS INPUTS**

High Sensitivity Input Sensitivity	Two volts peak to peak provides trace modulation over full intensity range.
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TABLE 1-1. (cont)

Characteristic	Performance Requirement
Useful input volt-ages versus repetition frequency	Two volts peak to peak, DC to two megahertz; reducing to 0.4 volt peak to peak at 20 meqahertz.
Polarity of operation	Positive-going signal decreases trace intensity; negative- going signal increases trace intensity.
Minimum pulse width that provides intensity modulation	30 nanoseconds at two volts.
Input resistance at DC	500 ohms $\pm$ 10%.
Maximum input voltage	15 volts (DC + peak AC).
High Speed Input Sensitivity	60 volts peak to peak provides trace modulation over full intensity range.
Useful input voltage versus repetition frequency	60 volts peak to peak, DC to 100 megahertz.
Polarity of operation	Positive-going signal decreases trace intensity; negative-going signal increases trace intensity.
Minimum pulse width that provides intensity modulation	3.5 nanoseconds at 60 volts.
Input resistance at DC	18 kilohms $\pm$ 20%.
Maximum input voltage	60 volts (DC + peak AC); 60 volts peak to peak AC.

**SIGNAL OUTPUTS**

+Sawtooth Source (selected by SWEEP switch)	A HORIZ time-base unit or B HORIZ time-base unit.
Polarity	Positive-going with baseline at zero volts $\pm$ 1 volt (into one megohm).

TABLE 1-1. (cont)

Characteristic	Performance Requirement
Output voltage	
Rate of rise	
Into 50 ohms	50 millivolts/unit of time $\pm$ 15%. <sup>1</sup>
Into one megohm	One volt/unit of time $\pm$ 10%. <sup>1</sup>
Peak voltage	
Into 50 ohms	Greater than 500 millivolts.
Into one megohm	Greater than 10 volts.
Output resistance	950 ohms $\pm$ 2%.
+Gate Source (selected by GATE switch)	A HORIZ time-base unit. B HORIZ time-base unit.  Delaying time-base unit (in A HORIZ compartment).
Output voltage	
Into 50 ohms	0.5 volt $\pm$ 10%.
Into one megohm	10 volts $\pm$ 10%.
Risetime into 50 ohms	20 nanoseconds or less.
Output resistance	950 ohms $\pm$ 2%.
Vertical Signal Output	
Bandwidth	Varies with vertical plug-in selected. See System Specification.
Risetime	
Source	Determined by B TRIGGER' SOURCE switch.
Output voltage	
Into 50 ohms	25 millivolts/division of vertical deflection $\pm$ 25%.
Into one megohm	0.5 volt/division of vertical deflection $\pm$ 25%.
Output resistance	950 ohms $\pm$ 2%.

<sup>1</sup> Unit of time selected by time-base time/division switch.

TABLE 1-1. (cont)

Characteristic	Performance Requirement
<b>CHARACTER GENERATOR</b>	
Word Location	See Fig. 2-5
<b>POWER SUPPLY</b>	
Line Voltage Range AC, RMS (Selected by Line Selector assembly on rear panel).	
115-volts nominal	90 to 136 volts.
230-volts nominal	180 to 272 volts.
Line Frequency	48 to 66 hertz (48 to 66 and 360 to 440 hertz with special MOD 101K).
Maximum Power Consumption	225 watts, 2.8 amperes at 60 hertz, 115-volt line.
<b>DISPLAY</b>	
Graticule Type	Internal with variable edge lighting.
Area	Eight divisions vertical by 10 divi- sions horizontal. Each division equals one centimeter.
Phosphor	P31 standard. Others available on special order.
Resolution Horizontal	At least 12 lines/division.
Vertical	At least 12 lines/division.
Geometry	0.1 division or less total bowing or tilt of a display horizontal or vertical line.
Beam Finder	Limits display within graticule area when actuated.
Photographic Writing Speed (without film fogging techniques)	
Tektronix C-51 Camera with f1.2 lens and 1:0.5 object-to-image ratio	At least 3300 centimeters/micro- second with Polaroid <sup>2</sup> Type 410 film (10,000 ASA) and P31 CRT phosphor.
	At least 7000 centimeters/micro- second with Polaroid Type 410 film (10,000 ASA) and P11 CRT phosphor.

<sup>2</sup> Registered trademark of the Polaroid Corporation.

TABLE 1-1. (cont)

Tektronix C-27 Camera with f1.3 lens and 1:0.5 object-to-image ratio	At least 2200 centimeters/micro- second with Polaroid Type 410 film(10,000 ASA) and P31 CRT phosphor.
	At least 5500 centimeters/micro- second with Polaroid Type 410 film (10,000 ASA) and P11 CRT phosphor.

TABLE 1-2.

**ENVIRONMENTAL CHARACTERISTICS**

Characteristic	Performance
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**NOTE**

This instrument will meet the electrical characteristics given in Table 1-1 over the following environmental limits. Complete details on environmental test procedures, including failure criteria, etc., can be obtained from Tektronix, Inc. Contact your local Tektronix Field Office or representative

Temperature Range Operating	0°C to +50°C.
Non-operating	-55°C to +75°C.
Altitude Operating	15,000 feet.
Non-operating	Test limit 50,000 feet.
Electro-magnetic Interference (EMI) as tested in MIL-I- 6181D (when equip- ped with Option 3 only)	
Radiated inter- ference	Interference radiated from the instrument under test within the given limits from 150 kilohertz to 1000 megahertz.
Conducted interference	Interference conducted out of the instrument under test through the power cord within the given limits from 150 kilohertz to 25 mega- hertz.
Transportation(pack aged instrument, without plug-ins)	Qualifies under National Safe Transit Committee test procedure 1A, Category II.

TABLE 1-3.  
PHYSICAL CHARACTERISTICS

Characteristic	Performance
Ventilation	Safe operating temperature is maintained by forced-air cooling. Automatic resetting thermal cutout protects instrument from over-heating.
Warm-up Time	20 minutes for rated accuracy.
Finish	Anodized front panel and cabinet.
Overall Dimensions (measured at maximum points)	
Height	7.0 inches (17.7 centimeters).
Width	19.0 inches (48.3 centimeters).
Length	22.4 inches (56.9 centimeters) behind front panel. 24.2 inches (61.7 centimeters) over-all.
Net Weight (instrument only)	44 pounds (19.7 kilograms).

### STANDARD ACCESSORIES

Standard accessories supplied with the R7704 are given in the Mechanical Parts List illustrations. For optional accessories available for use with this instrument, see the Tektronix, Inc. catalog.

### INSTRUMENT OPTIONS

#### General

The following options are available for the R7704 and can be installed as part of the instrument when ordered, or they can be installed at a later time. Complete information on all options for this instrument is given in this manual. For further information on instrument options, see your Tektronix, Inc. catalog, or contact your local Tektronix Field Office or representative.

#### Option 1

This option deletes the Readout System. Operation of the instrument is unchanged except that there is no alphanumeric display on the CRT and the READOUT control is non-functional. The Readout System can be added at any time by ordering the readout conversion kit.

#### Option 2

The X-Y Delay Compensation Network can be added to the instrument to equalize the signal delay between the vertical and horizontal deflection systems. When this network is installed and activated, the phase shift between the vertical and horizontal channels is adjustable to less than 20 from DC to two megahertz.

#### Option 3

With option 3 installed, the instrument will meet the EMI interference specifications given in Table 1-2.

## SYSTEM SPECIFICATIONS

Your Tektronix 7700-series oscilloscope system provides exceptional flexibility in operation with a wide choice of general and special purpose plug-in units. The type number of a particular plug-in unit identifies its usage as follows: The first digit (7) denotes the oscilloscope system for which the plug-in unit is designed (7000-series).

The second letter describes the purpose of the plug-in unit:

A - Amplifier unit.

B - "Real time" time-base unit.

D - Digital unit.

J - Spectrum analyzer, single width.

K - Spectrum analyzer, single width.

L - Spectrum analyzer, double width.

M - Miscellaneous.

S - Sampling unit.

T - Sampling time-base unit.

The third and fourth digits of the plug-in type number are sequence numbers and do not carry any special connotation.

An "N" suffix letter added to the normal four digit type number identifies a unit not equipped with the circuitry necessary to encode data for the 7000-series readout system.

## 7700-SERIES OSCILLOSCOPE SYSTEM VERTICAL SPECIFICATIONS

This table lists the vertical specifications which are system dependent. For more complete specifications on plug-in units for the 7000-Series Oscilloscope System, refer to the Tektronix Catalog.

Amplifier Plug-In				Vertical System Deflection Factor Accuracy*			SIG OUT	
				EXT CAL	INT CAL	INT CAL		
Unit	Probe	BW	Tr	0 to 50 ° C	15 to 35°C	0 to 50°C	BW	Tr
7A11	Integral	150 MHz	2.4 ns	2%	3%	4%	60 MHz	5.9 ns
	None	105 MHz	3.4 ns	2%	3%	4%	55 MHz	6.4 ns
	P6053	105 MHz	3.4 ns	3%	4%	5%	55 MHz	6.4 ns
	None	100 MHz	3.5 ns	1.5%	2.5%	3.5%	55 MHz	6.4 ns
7A13	P6053	100 MHz	3.5 ns	1.5%	2.5%	3.5%	55 MHz	6.4 ns
	P6055	65 MHz	5.4 ns	1.5%	2.5%	3.5%	45 MHz	7.8 ns
7A14	P6021	50 MHz	7.0 ns	2%	3%	4%	40 MHz	8.8 ns
	P6022	105 MHz	3.4 ns	2%	3%	4%	50 MHz	7.0 ns
7A15	None	75 MHz	4.7 ns	2%	3%	4%	50 MHz	7.0 ns
	P6053	75 MHz	4.7 ns	3%	4%	5%	50 MHz	7.0 ns
7A16	None	150 MHz	2.4 ns	2%	3%	4%	60 MHz	5.9 ns
	P6053	150 MHz	2.4 ns	3%	4%	5%	60 MHz	5.9 ns
7A18	None	75 MHz	4.7 ns	2%	3%	4%	50 MHz	7.0 ns
	P6053	75 MHz	4.7 ns	3%	4%	5%	50 MHz	7.0 ns
7A22	None or any	1.0 MHz ± 10%	350 ns ± 9%	2%	3%	4%	1.0 MHz ± 10%	350 ns ± 9%

\*Deflection Factor accuracy is checked as follows:

EXT CAL 0° C to 50°C-Plug-in gain set at a temperature within 10°C of operating temperature, using an external calibrator whose accuracy is within 0.25%.

INT CAL 15°C to 35°C-Plug-in gain set while operating within a temperature range of +15°C to +35°C, using the oscilloscope calibrator.

INT CAL 0°C to 50°C-Plug-in gain set using the oscilloscope calibrator (within 10°C of the operating temperature) in a temperature range between 0°C and +50°C.

## SECTION 3 CIRCUIT DESCRIPTION

*Change information, if any, affecting this section will be found at the rear of this manual.*

### Introduction

This section of the manual contains a description of the circuitry used in the R7704 Oscilloscope. The description begins with a discussion of the instrument using the basic block diagram shown in Fig. 3-1. Then, each circuit is described in detail using detailed block diagrams to show the interconnections between the stages in each major circuit and the relationship of the front-panel controls to the individual stages.

A complete block diagram is located in the Diagrams section at the back of this manual. This block diagram shows the overall relationship between all of the circuits. Complete schematics of each circuit are also given in the Diagrams section. Refer to these diagrams throughout the following circuit description for electrical values and relationship.

### BLOCK DIAGRAM

#### General

The following discussion is provided to aid in understanding the overall concept of the R7704 before the individual circuits are discussed in detail. A basic block diagram of the R7704 is shown in Fig. 3-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each block represents a major circuit within the instrument. The number on each block refers to the complete circuit diagram which is located at the rear of this manual.

Vertical signals to be displayed on the CRT are applied to the Vertical Interface circuit from both vertical plug-in compartments. The Vertical Interface circuit determines whether the signal from the left and/or right vertical unit is displayed. The selected vertical signal is then amplified by the Vertical Amplifier circuit to bring it to the level necessary to drive the vertical deflection plates of the CRT. This circuit also includes an input to produce the vertical portion of an alpha-numeric readout display.

Horizontal signals for display on the CRT are connected to the Horizontal Interface circuit from both horizontal plug-in compartments. The X-Y Delay Compensation network (optional feature) provides a delay for the horizontal (X) portion of an X-Y display to match the delay of the

vertical (Y) signal due to the delay line. The Horizontal Channel Switch determines whether the signal from the A and/or B horizontal unit is displayed. The horizontal signal selected by the Horizontal Channel Switch is connected to the Horizontal Amplifier circuit which amplifies it to provide the horizontal deflection for the CRT. This circuit also accepts the X-signal from the Readout System to produce the horizontal portion of the readout display. The Readout System provides alpha-numeric display of information encoded by the plug-in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis with the analog waveform display.

The internal trigger signals from the vertical plug-in units are connected to the Trigger Selector circuit. This circuit selects the trigger signal which is connected to the horizontal plug-in units. It also provides the drive signal for the Output Signals circuit to provide an output which is a sample of the vertical signal. The Output Signals circuit also provides a sawtooth and a gate output signal. The Calibrator portion of this circuit produces a square-wave output with accurate amplitude which can be used to check the calibration of this instrument and the compensation of probes.

The Logic Circuit develops control signals for use in other circuits within this instrument and the plug-in units. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and R7704 control settings.

The CRT Circuit contains the Z-Axis Amplifier which provides the drive signal to control the intensity level of the display. The CRT Circuit also contains the controls necessary for operation of the cathode-ray tube.

The Line to DC Converter/Regulator and Low-Voltage Regulator circuits provide the power necessary for operation of this instrument. This voltage is connected to all circuits within the instrument. The Controls and Cabling circuit shows the switching logic of the front-panel controls. It also includes the rear-panel REMOTE CONTROL connector and the output connectors to supply power to active probe systems.

(A)



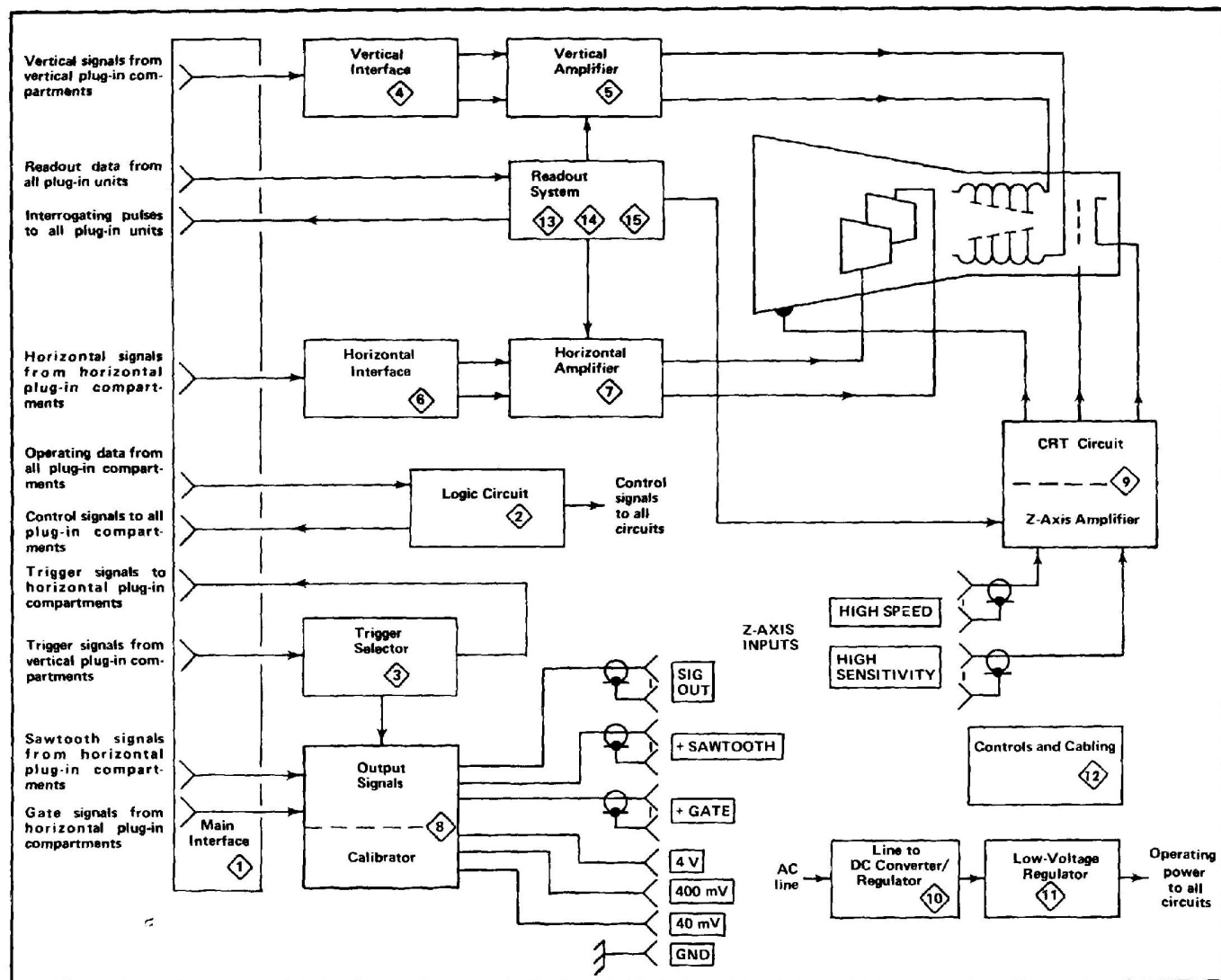


Fig. 3-1. Basic block diagram of R7704 Oscilloscope

## CIRCUIT OPERATION

### General

This section provides a detailed description of the electrical operation and relationship of the circuits in the R7704. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits which are commonly used in the electronics industry are not described in detail. If more information is desired on these commonly used circuits, refer to the following textbooks (also see books under Logic Fundamentals):

Phillip Cutler, "Semiconductor Circuit Analysis", McGraw-Hill, New York, 1964.

Lloyd P. Hunter (Ed.), "Handbook of Semiconductor Electronics", second edition, McGraw-Hill, New York, 1962.

Jacob Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, 1965.

The following circuit analysis is written around the detailed block diagrams which are given for each major circuit. These detailed block diagrams give the names of the individual stages within the major circuits and show how they are connected together to form the major circuit. The block diagrams also show the inputs and outputs for each circuit and the relationship of the front-panel controls to the individual stages. The circuit diagrams from which the detailed block diagrams are derived are shown in the Diagrams section.

### NOTE

**All references to direction of current in this manual are in terms of conventional current, - i.e., from plus to minus.**

## LOGIC FUNDAMENTALS

### General

Digital logic techniques are used to perform many functions within this instrument. The function and  
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### Circuit Description-R7704

operation of the logic circuits are described using logic symbology and terminology. This portion of the manual is provided to aid in the understanding of these symbols and terms. The following information is a basic introduction to logic concepts, not a comprehensive discussion of the subject. For further information on binary number systems and the associated Boolean Algebra concepts, the derivation of logic functions, a more detailed analysis of digital logic, etc., refer to the following textbooks:

Robert C. Baron and Albert T. Piccirilli, "Digital Logic and Computer Operation", McGraw-Hill, New York, 1967.

Thomas C. Bartee, "Digital Computer Fundamentals", McGraw-Hill, New York, 1966.

Yaohan Chu, "Digital Computer Design Fundamentals", McGraw-Hill, New York, 1962.

Joseph Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, Chapters 9-11, 1965.

### Symbols

The operation of circuits within the R7704 which use digital techniques is described using the graphic symbols set forth in military standard MIL-STD-806B. Table 3-1 provides a basic logic reference for the logic devices used within this instrument. Any deviations from the standard symbology, or devices not defined by the standard will be described in the circuit description for the applicable device.

### NOTE

**Logic symbols used on the diagrams depict the logic function and may differ from the manufacturer's data.**

### Logic Polarity

All logic functions are described using the positive logic convention. Positive logic is a system of notation where the

more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false or 0-state. The HI-LO method of notation is used in this logic description. The specific voltages which constitute a HI or LO state vary between individual devices.

NOTE

The HI-LO logic notation can be conveniently converted to 1-0 notation by disregarding the first letter of each step. Thus:

HI= 1  
LO = 0

Wherever possible, the input and output lines are named to indicate the function that they perform when at the HI (true) state. For example, the line labeled, "Display B Command" means that the B Time-Base unit will be displayed

when this line is HI or true. Likewise, the line labeled "X-Compensation Inhibit" means that the X-Compensation function is inhibited or disabled when this line is HI.

Input/Output Tables

Input/output (truth) tables are used in conjunction with the logic diagrams to show the input combinations which are of importance to a particular function, along with the resultant output conditions. This table may be given either for an individual device or for a complete logic stage. For examples of input/output tables for individual devices, see Table 3-1.

Non-Digital Devices

It should be noted that not all of the integrated circuit devices in this instrument are digital logic devices. The function of non-digital devices will be described individually using operating waveforms or other techniques to illustrate their function.

TABLE 3-1.  
Basic Logic Reference


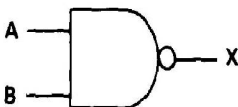
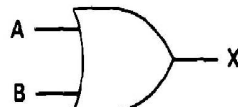
Device	Symbol	Description	Input/Output Table																		
AND gate		A device with two or more inputs and one output. The output of the AND gate is HI if and only if all of the inputs are at the HI state.	<table><tr><th colspan="2">Input</th><th>Output</th></tr><tr><td>A</td><td>B</td><td>X</td></tr><tr><td>LO</td><td>LO</td><td>LO</td></tr><tr><td>LO</td><td>HI</td><td>LO</td></tr><tr><td>HI</td><td>LO</td><td>LO</td></tr><tr><td>HI</td><td>HI</td><td>HI</td></tr></table>	Input		Output	A	B	X	LO	LO	LO	LO	HI	LO	HI	LO	LO	HI	HI	HI
Input		Output																			
A	B	X																			
LO	LO	LO																			
LO	HI	LO																			
HI	LO	LO																			
HI	HI	HI																			
NAND gate		A device with two or more inputs and one output. The output of the NAND gate is LO if and only if all of the inputs are at the HI state.	<table><tr><th colspan="2">Input</th><th>Output</th></tr><tr><td>A</td><td>B</td><td>X</td></tr><tr><td>LO</td><td>LO</td><td>HI</td></tr><tr><td>LO</td><td>HI</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>HI</td><td>LO</td></tr></table>	Input		Output	A	B	X	LO	LO	HI	LO	HI	HI	HI	LO	HI	HI	HI	LO
Input		Output																			
A	B	X																			
LO	LO	HI																			
LO	HI	HI																			
HI	LO	HI																			
HI	HI	LO																			
OR gate		A device with two or more inputs and one output. The output of the OR gate is HI if one or more of the inputs are at the HI state.	<table><tr><th colspan="2">Input</th><th>Output</th></tr><tr><td>A</td><td>B</td><td>X</td></tr><tr><td>LO</td><td>LO</td><td>LO</td></tr><tr><td>LO</td><td>HI</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>HI</td><td>HI</td></tr></table>	Input		Output	A	B	X	LO	LO	LO	LO	HI	HI	HI	LO	HI	HI	HI	HI
Input		Output																			
A	B	X																			
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LO	HI	HI																			
HI	LO	HI																			
HI	HI	HI																			

TABLE 3-1. (cont.)

Basic Logic Reference

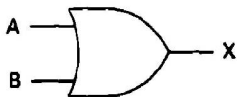
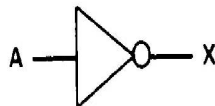



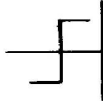
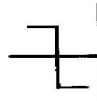
Device	Symbol	Description	Input/Output Table																		
NOR gate		A device with two or more inputs and one output. The output of the NOR gate is LO if one or more of the inputs are at the HI state	<table><tr><th colspan="2">Input</th><th>Output</th></tr><tr><td>A</td><td>B</td><td>X</td></tr><tr><td>LO</td><td>LO</td><td>HI</td></tr><tr><td>LO</td><td>HI</td><td>LO</td></tr><tr><td>HI</td><td>LO</td><td>LO</td></tr><tr><td>HI</td><td>HI</td><td>LO</td></tr></table>	Input		Output	A	B	X	LO	LO	HI	LO	HI	LO	HI	LO	LO	HI	HI	LO
Input		Output																			
A	B	X																			
LO	LO	HI																			
LO	HI	LO																			
HI	LO	LO																			
HI	HI	LO																			
Inverter		A device with one input and one output. The output state is always opposite to the input state.	<table><tr><th>Input</th><th>Output</th></tr><tr><td>A</td><td>X</td></tr><tr><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>LO</td></tr></table>	Input	Output	A	X	LO	HI	HI	LO										
Input	Output																				
A	X																				
LO	HI																				
HI	LO																				
LO-state indicator		A small circle at the input or output of a symbol indicates that the LO state is the significant state. Absence of the circle indicates that the HI state is the significant state. Two examples follow:	<table><tr><th colspan="2">Input</th><th>Output</th></tr><tr><td>A</td><td>B</td><td>X</td></tr><tr><td>LO</td><td>LO</td><td>LO</td></tr><tr><td>LO</td><td>HI</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>HI</td><td>HI</td></tr></table>	Input		Output	A	B	X	LO	LO	LO	LO	HI	HI	HI	LO	HI	HI	HI	HI
	Input			Output																	
	A	B		X																	
LO	LO	LO																			
LO	HI	HI																			
HI	LO	HI																			
HI	HI	HI																			
		AND gate with LO-state indicator at the A input.  The output of this gate is HI if and only if the A input is LO and the B input is HI.																			
		OR gate with LO-state indicator at the A input:  The output of this gate is HI if either the input is LO or the B input is HI.	<table><tr><th colspan="2">Input</th><th>Output</th></tr><tr><td>A</td><td>B</td><td>X</td></tr><tr><td>LO</td><td>LO</td><td>LO</td></tr><tr><td>LO</td><td>HI</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>HI</td><td>HI</td></tr></table>	Input		Output	A	B	X	LO	LO	LO	LO	HI	HI	HI	LO	HI	HI	HI	HI
Input		Output																			
A	B	X																			
LO	LO	LO																			
LO	HI	HI																			
HI	LO	HI																			
HI	HI	HI																			
Edge symbol		Normally superimposed on an input line to a logic symbol. Indicates that this input (usually the trigger input of a flip-flop) responds to the indicated transition of the applied signal.																			
																					

TABLE 3-1. (cont.)

Basic Logic Reference

Device	Symbol	Description	Input/Output Table																																				
Triggered (toggle) Flip-Flop		A bistable device with one input and two outputs (either or both outputs may be used). When triggered, the outputs change from one stable state to the other stable state with each trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	<table><tr><th colspan="2">Input</th><th colspan="2">Output</th></tr><tr><td colspan="2">Condition before trigger pulse</td><td colspan="2">Condition before trigger pulse</td></tr><tr><td>X</td><td><math>\overline{X}</math></td><td>X</td><td><math>\overline{X}</math></td></tr><tr><td>LO</td><td>HI</td><td>HI</td><td>LO</td></tr><tr><td>HI</td><td>LO</td><td>LO</td><td>HI</td></tr></table>	Input		Output		Condition before trigger pulse		Condition before trigger pulse		X	$\overline{X}$	X	$\overline{X}$	LO	HI	HI	LO	HI	LO	LO	HI																
Input		Output																																					
Condition before trigger pulse		Condition before trigger pulse																																					
X	$\overline{X}$	X	$\overline{X}$																																				
LO	HI	HI	LO																																				
HI	LO	LO	HI																																				
Set-Clear (J-K) Flip-Flop		A bistable device with two inputs and two outputs (either or both outputs may be used). The outputs change state in response to the states at the inputs. The outputs are complementary (i.e., when one output is HI the other is LO).	<table><tr><th colspan="2">Input</th><th colspan="2">Output</th></tr><tr><td>A</td><td>B</td><td>X</td><td><math>\overline{X}</math></td></tr><tr><td>LO</td><td>LO</td><td colspan="2">No change</td></tr><tr><td>LO</td><td>HI</td><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>HI</td><td>LO</td></tr><tr><td>HI</td><td>HI</td><td colspan="2">Changes state</td></tr></table>	Input		Output		A	B	X	$\overline{X}$	LO	LO	No change		LO	HI	LO	HI	HI	LO	HI	LO	HI	HI	Changes state													
Input		Output																																					
A	B	X	$\overline{X}$																																				
LO	LO	No change																																					
LO	HI	LO	HI																																				
HI	LO	HI	LO																																				
HI	HI	Changes state																																					
Triggered Set-Clear (J-K) Flip-Flop		A bistable device with three or more inputs and two outputs (either or both outputs may be used). When triggered, the outputs change state in response to the states at the inputs prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	<table><tr><th colspan="2">Input</th><th colspan="2">Output</th></tr><tr><td>A</td><td>B</td><td>X</td><td><math>\overline{X}</math></td></tr><tr><td>LO</td><td>LO</td><td colspan="2">No change</td></tr><tr><td>LO</td><td>HI</td><td>LO</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>HI</td><td>LO</td></tr><tr><td>HI</td><td>HI</td><td colspan="2">Changes state</td></tr></table>	Input		Output		A	B	X	$\overline{X}$	LO	LO	No change		LO	HI	LO	HI	HI	LO	HI	LO	HI	HI	Changes state													
Input		Output																																					
A	B	X	$\overline{X}$																																				
LO	LO	No change																																					
LO	HI	LO	HI																																				
HI	LO	HI	LO																																				
HI	HI	Changes state																																					
Flip-flop with direct inputs (may be applied to all triggered flip-flops)		For devices with direct-set ( $S_D$ ) or direct-clear ( $C_D$ ) inputs, the indicated state at either of these inputs overrides all other inputs (including trigger) to set the outputs to the states shown in the input/output table.	<table><tr><th colspan="4">Input</th><th colspan="2">Output</th></tr><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>X</td><td><math>\overline{X}</math></td></tr><tr><td>1</td><td>1</td><td>LO</td><td>LO</td><td colspan="2">NO change<sup>1</sup></td></tr><tr><td><math>\Phi</math></td><td><math>\Phi</math></td><td>LO</td><td>HI</td><td>LO</td><td>HI</td></tr><tr><td><math>\Phi</math></td><td><math>\Phi</math></td><td>HI</td><td>LO</td><td>HI</td><td>LO</td></tr><tr><td><math>\Phi</math></td><td><math>\Phi</math></td><td>HI</td><td>HI</td><td colspan="2">Unde-fined</td></tr></table> <p><math>\Phi</math> = Has no effect in this case <sup>1</sup>Output state determined by conditions at triggered inputs</p>	Input				Output		A	B	C	D	X	$\overline{X}$	1	1	LO	LO	NO change <sup>1</sup>		$\Phi$	$\Phi$	LO	HI	LO	HI	$\Phi$	$\Phi$	HI	LO	HI	LO	$\Phi$	$\Phi$	HI	HI	Unde-fined	
Input				Output																																			
A	B	C	D	X	$\overline{X}$																																		
1	1	LO	LO	NO change <sup>1</sup>																																			
$\Phi$	$\Phi$	LO	HI	LO	HI																																		
$\Phi$	$\Phi$	HI	LO	HI	LO																																		
$\Phi$	$\Phi$	HI	HI	Unde-fined																																			

## MAIN INTERFACE

### General

Diagram 1 shows the plug-in interface and the interconnections between the plug-in compartments, circuit boards, etc. of this instrument. The circuitry shown on this diagram associated with Q24 and Q28 is described in connection with the Trigger Selector circuit.

## LOGIC CIRCUIT

### General

The Logic Circuit develops control signals for use in other circuits within this instrument. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and R7704 control settings. A block diagram of the Logic Circuit is shown in Fig. 3-2. This diagram shows the source of the input control signals, the output signals produced by this stage, and the basic interconnections between blocks. The interconnections shown are intended only to indicate inter-relation between blocks and do not indicate a direct connection or that only a single connection is made between the given blocks. Details of the inter-relation between stages in this circuit are given in the circuit description which follows. A schematic of this circuit is shown on diagram 2 at the rear of this manual.

This circuit description for the Logic Circuit is written with the approach that each of the integrated circuits and its associated discrete components comprises an individual stage as shown by the block diagram (Fig. 3-2). The operation of each of these stages is discussed relating the input signals and/or levels to the output, with consideration given to the various modes of operation that may affect the stage. A logic diagram is also provided for each stage. These diagrams are not discussed in detail but are provided to aid in relating the function performed by a given stage to standard logic techniques. It should be noted that these logic diagrams are not an exact representation of the internal structure of the integrated circuit but are only a logic diagram of the function performed by the stage. An input/output table is given, where applicable, for use along with the circuit description and logic diagram. These input/output tables document the combination of input conditions which are of importance to perform the prescribed function of an individual stage.

### Horizontal Logic

General. The Horizontal Logic stage performs three separate logic functions. These functions are: A Sweep Inhibit, B Sweep Inhibit, and Alternate Pulse Generator. Fig. 3-3 identifies the three individual stages and the input and out-

put terminals associated with each. Notice that some of the input levels are used in several or all of the individual stages.

**A Sweep Inhibit.** The A Sweep Inhibit stage produces an output level at pin 14 which determines if the A Time-Base unit can produce a sweep. If this level is HI, the A Time-Base unit is locked out (disabled) so it cannot produce a sweep. If the level is LO, the A Time-Base unit is enabled and can produce a sweep when triggered.

Only two combinations of input conditions produce an A Sweep Inhibit level (HI); if any one of the prescribed conditions is not met, the A Sweep Inhibit level is LO and the A Time-Base unit is enabled. These conditions are:

1. Pin 1 HI-HORIZONTAL MODE switch set to ALT.

Pin 4 HI-A Horizontal unit operated in time-base mode.

Pin 5 HI-B Horizontal unit operated in time-base mode.

Pin 12 LO-A Time-Base unit in independent (non-delayed) mode.

Pin 16 HI-B Sweep is being displayed in the horizontal-alternate mode.

2. Pin 2 LO-A Time-Base unit is not already producing a sweep.

Pin 12 HI-A Time-Base unit in delayed mode.

Pin 13 HI-B Time-Base unit has just completed a sweep and is in holdoff condition.

The first combination disables the A Sweep while the B Sweep is being displayed in the horizontal ALT mode (both units must be in time-base mode) if non-delayed operation is being used. The second combination disables the A Sweep during delayed-sweep operation so the B Sweep can complete its holdoff before the next A Sweep begins.

A logic diagram for the A Sweep Inhibit stage is shown in Fig. 3-4A. A table of input/output combinations for this stage is shown in Fig. 3-4B. This table shows the level at each input for the two combinations that produce a HI output level.

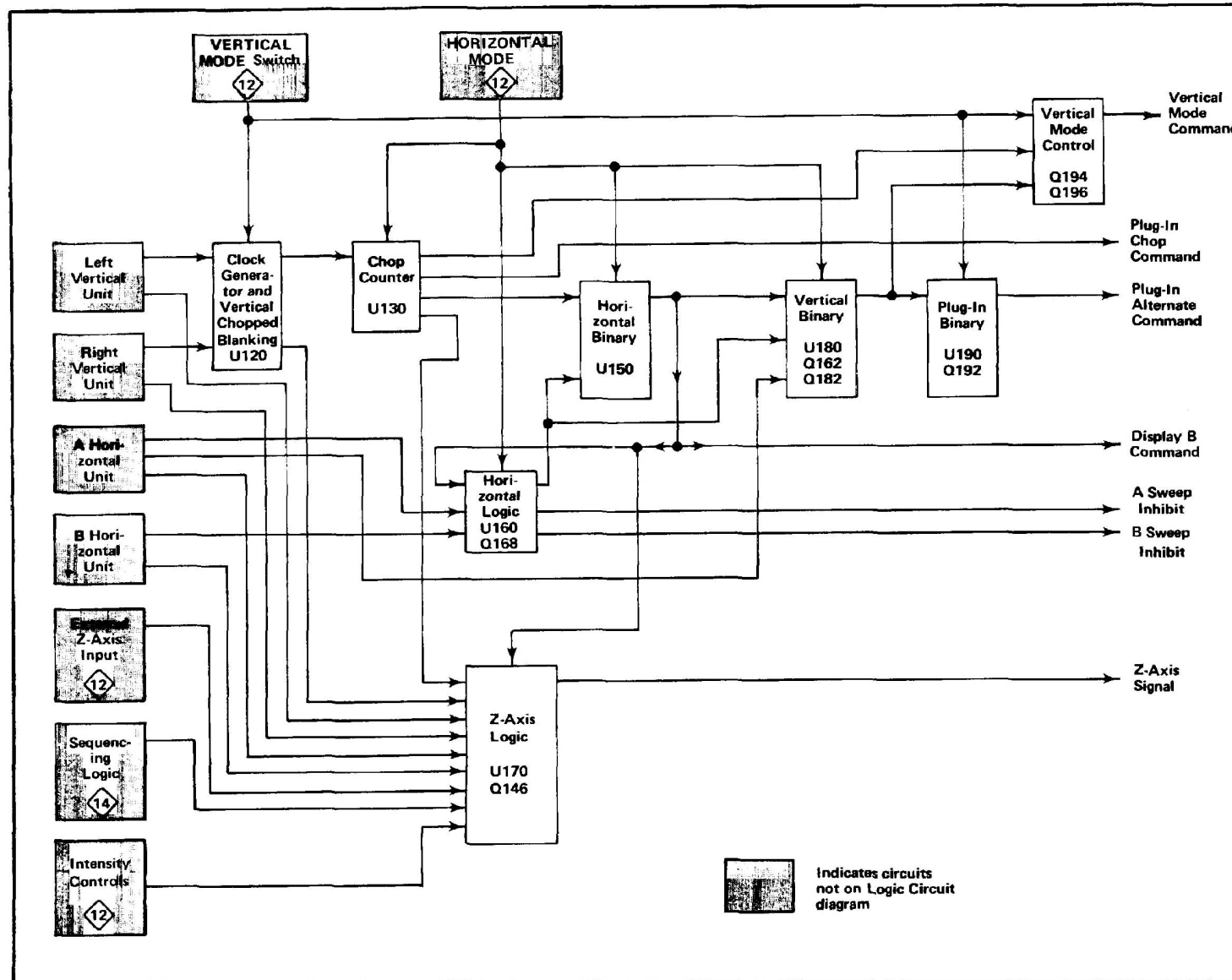


Fig. 3-2. Block diagram of Logic Circuit



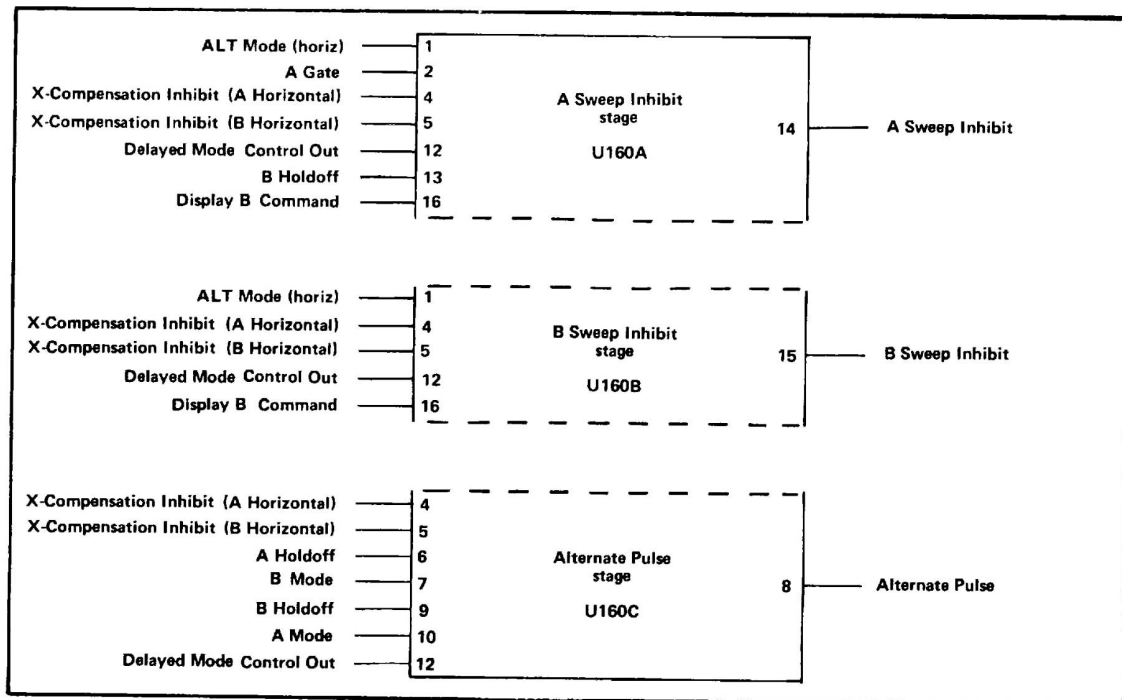


Fig. 3-3. Breakdown of separate stages within Horizontal Logic (U160) showing inputs and outputs for each stage

**B Sweep Inhibit.** The B Sweep Inhibit stage produces an output level at pin 15 of U160B which determines if the B Time-Base unit can produce a sweep. A HI level at this pin disables the B Sweep and a LO level provides an enabling level to the B Time-Base unit. The output at pin 15 is HI only under one set of input conditions. These conditions are:

- Pin 1 HI-HORIZONTAL MODE switch set to ALT.
- Pin 4 HI-A Horizontal unit operated in time-base mode.
- Pin 5 HI-B Horizontal unit operated in time-base mode.
- Pin 12 LO-A Time-Base unit in independent (non-delayed) mode.
- Pin 16 LO-A Sweep is being displayed in the horizontal-alternate mode.

These conditions disable the B Sweep while the A Sweep is being displayed in the horizontal ALT mode (both units must be in time-base mode) if non-delayed sweep is used. For any other combination of input conditions, the B Sweep Inhibit level at pin 15 is LO. However, the inhibit level to the B Time-Base unit is determined by both the

Delay Gate from the A Time-Base unit and the B Sweep Inhibit level produced by this stage. The B Sweep is enabled only when both of these levels are LO.

Fig. 3-5A shows the logic diagram of the B Sweep Inhibit stage. The gate connected to the output of this stage is a phantom-OR gate located on the Main Interface diagram (a phantom-OR gate performs the OR-logic function merely by interconnection of the two signals). An input/output table for the B Sweep Inhibit stage is shown in Fig. 3-5B.

**Alternate Pulse Generator.** The third function performed by U160 is to produce alternate pulses for use by the horizontal and vertical alternate systems. The conditions that exist at the inputs to the Alternate Pulse Generator stage determine which time base provides the Alternate Pulse. The Alternate Pulse is a positive-going pulse (falling edge only used by following-stages) which is coincident with the leading edge of the holdoff gate from the time-base units. The holdoff gate is produced at the end of the sweep by the respective time-base unit, and differentiated by either C165 or C166 to provide a positive-going pulse to pins 6 or 9. The Alternate Pulse is produced at the end of either the A Sweep or the B Sweep, or both, depending upon the operating conditions. The following discussions describe the

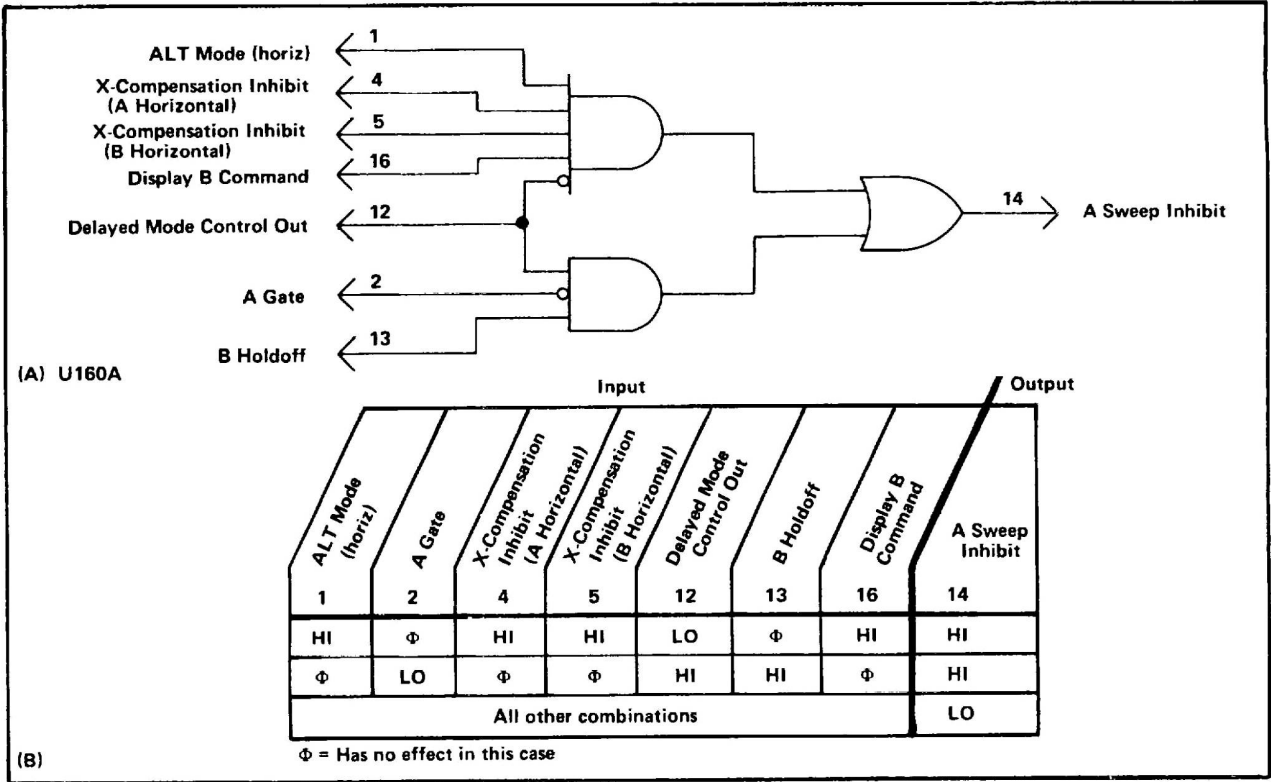


Fig. 3-4. (A) Logic diagram for A Sweep Inhibit stage, (B) Table of input/output combinations for A Sweep Inhibit stage.

operation of the Alternate Pulse Generator stage in relation to various combinations of input conditions that can occur.

1. A (ONLY) MODE

The Alternate Pulse is produced only at the end of the A Sweep when the HORIZONTAL MODE switch is set to the A position. The input conditions are:

- Pin 4 HI-A Horizontal unit operated in time-base mode.
- Pin 6 HI-Holdoff pulse produced at end of A Sweep.
- Pin 7 LO-HORIZONTAL MODE switch set to any position except B.
- Pin 10 HI-HORIZONTAL MODE switch set to A.

2. B (ONLY) MODE-NON-DELAYED

In the B position of the HORIZONTAL MODE switch, the Alternate Pulse is produced only at the end of the B Sweep (A Time-Base must be in independent, non-delayed, mode). The input conditions are:

- Pin 5 HI-B Horizontal unit operated in time-base mode.

- Pin 7 HI-HORIZONTAL MODE switch set to B.
- Pin 9 HI-Holdoff pulse produced at end of B Sweep.
- Pin 10 LO-HORIZONTAL MODE switch set to any position except A.
- Pin 12 LO-A Time-Base unit in independent (non-delayed) mode.

3. ALTERNATE OR CHOPPED OPERATION-NON-DELAYED

When the HORIZONTAL MODE switch is set to ALT or CHOP (A Time-Base unit must be in independent, non-delayed, mode), an Alternate Pulse is produced at the end of each sweep. For example, an Alternate Pulse is produced first at the end of the A Sweep, then at the end of the B Sweep, again at the end of the A Sweep, etc. Although Alternate Pulses are produced in the CHOP horizontal mode, they are not used in this instrument. The input conditions for this mode of operation are:

- Pin 4 HI-A Horizontal unit operated in time-base mode.
- Pin 5 HI-B Horizontal unit operated in time-base mode.

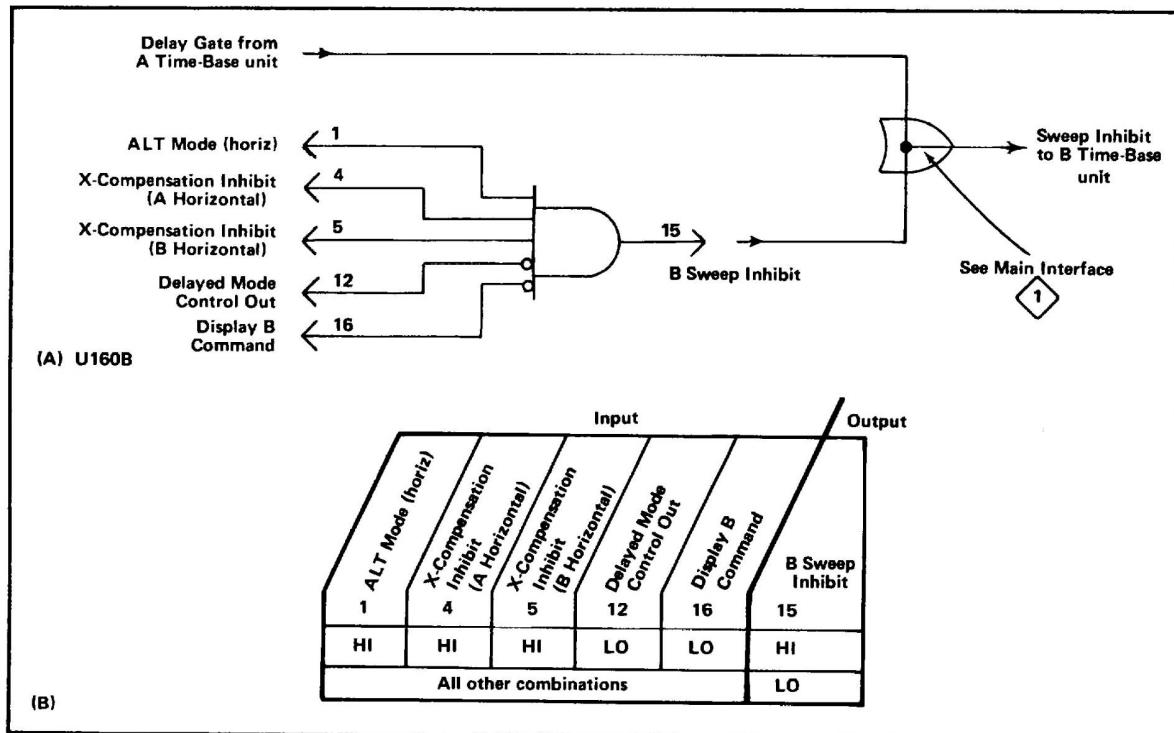


Fig. 3-5. (A) Logic diagram for B Sweep Inhibit stage, (B) Table of input/output combinations for B Sweep Inhibit stage

Pin 6 HI-Holdoff pulse produced at end of A Sweep'.  
 Pin 7 LO-HORIZONTAL MODE switch set to any position except B.  
 Pin 9 HI-Holdoff pulse produced at end of B Sweep'.  
 Pin 10 LO-HORIZONTAL MODE switch set to any position except A.  
 Pin 12 LO-A Time-Base unit in independent (non-delayed) mode.

#### 4. DELAYED SWEEP

When the A Time-Base unit is set for delayed operation, the operation of the stage is changed so an Alternate Pulse is produced only at the end of the A Sweep even when the HORIZONTAL MODE switch is set to B. This is necessary since the A Time-Base establishes the amount of delay time for the B Time-Base whenever it is displayed. The input conditions for this mode of operation are:

Pin 4 HI-A Horizontal unit operated in time-base mode.

<sup>1</sup>Simultaneous HI at pins 6 and 9 are not required; a HI at either input produces an Alternate Pulse if other conditions are met.

(A)

Pin 5 HI-B Horizontal unit operated in time-base mode.  
 Pin 6 HI-Holdoff pulse produced at end of A Sweep.  
 Pin 12 HI-A Time-Base unit in delayed mode.

#### 5. VERTICAL UNIT IN HORIZONTAL COMPARTMENT

When a vertical unit is installed in either of the horizontal plug-in compartments, the Alternate Pulse can be produced only from the remaining time-base unit. If vertical units are installed in both horizontal plug-in compartments, an Alternate Pulse is not produced under normal operating conditions since there are no time-base units to produce a holdoff pulse.

#### NOTE

The conditions of the Alternate Pulse Generator with vertical units in both horizontal plug-in compartments are such that an Alternate Pulse could be produced if positive-going pulses are applied to pins 6 and 9. Although not used for normal operation, this mode may be used in special purpose plug-ins.

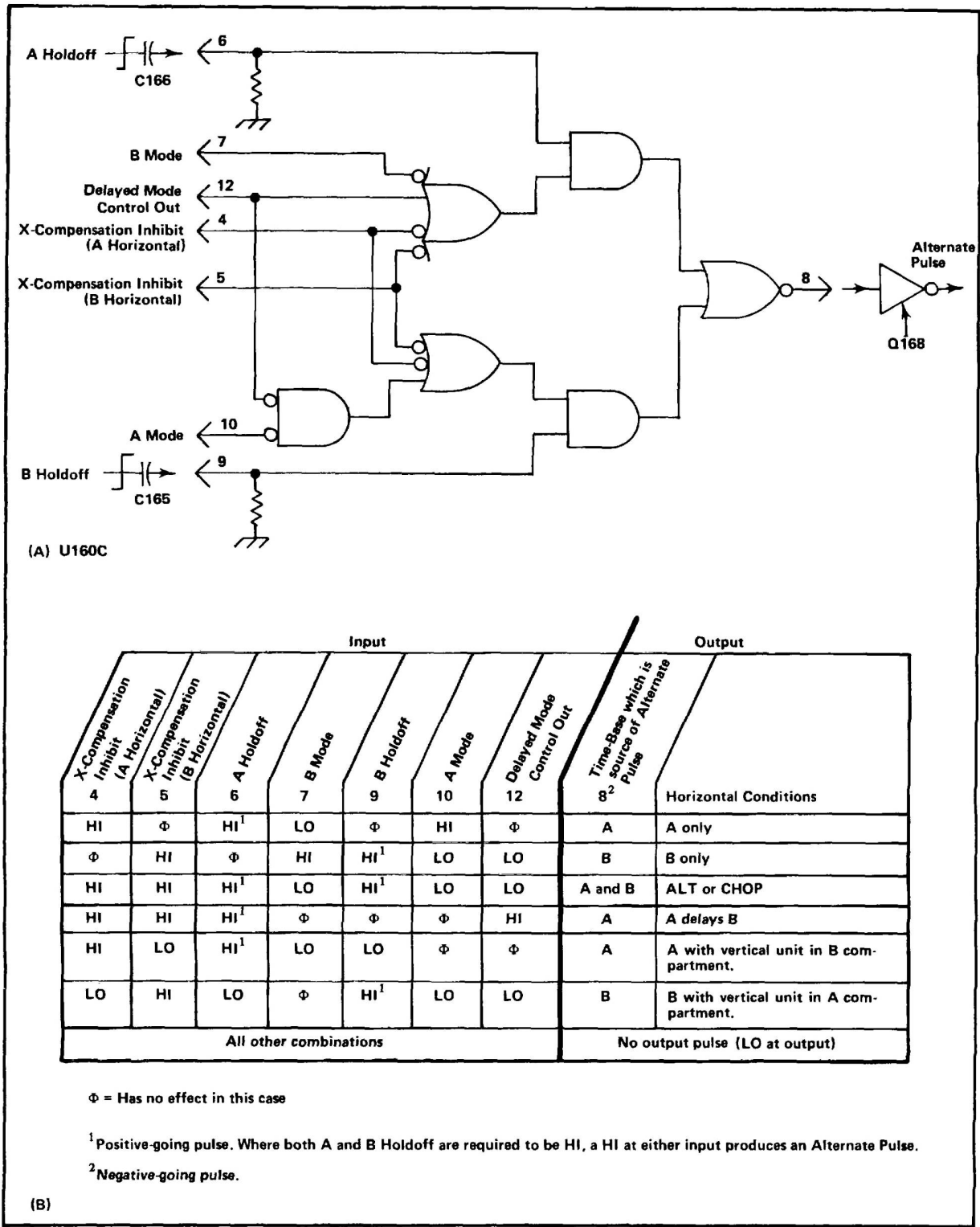


Fig. 3-6. (A) Logic diagram for Alternate Pulse Generator stage, (B) Table of input/output combinations for the Alternate Pulse Generator stage.

## 6. ONE TIME-BASE REMOVED

If either time-base unit is removed from its compartment and the compartment is left vacant, an Alternate Pulse can not be produced. Although the input levels to the Alternate Pulse Generator stage will allow an output pulse to be produced by the remaining time-base unit, further operation is prevented by the A or B Sweep Inhibit stages.

A logic diagram for the Alternate Pulse Generator stage is shown in Fig. 3-6A. Note the resistors shown connected to pins 6 and 9 of U160C. These resistors, which are internal to the device, hold the level at pins 6 and 9 LO unless a HI level is applied to the corresponding input. Since the holdoff gate is capacitively coupled to pins 6 and 9, these inputs are at the LO level except when a differentiated A or B Holdoff Gate is received from the respective time base. Fig. 3-6B shows an input/output table for the Alternate Pulse Generator stage.

### Z-Axis Logic

The Z-Axis Logic stage produces an output current which sets the intensity of the display on the CRT. The level of this output current is determined by the setting of the A or B INTENSITY controls, by a current added during B Sweep time to provide an intensified zone on the A Sweep for delayed-sweep operation, or by an external signal. The input current from the A and B INTENSITY controls is switched so the output current matches the horizontal display. The Vertical Chopped Blanking, Horizontal Chopped Blanking, and Readout Blanking are applied to this stage to block the output current and blank the CRT display for vertical chopping, horizontal chopping, or during a readout display.

Fig. 3-7 identifies the inputs to the Z-Axis Logic circuit. This circuit is current-driven at all inputs except pins 5 and 15. The current at pins 1, 2, 9, and 16 is variable from 0 to 4 milliamperes and is determined by the applicable current source to control the output current at pin 8.

The Vertical Chopped Blanking connected to pin 6, and the Horizontal Chopped Blanking connected to both pins 6 and 7 through CR145-CR146, enables or disables this stage to control all output current. Quiescently, the level at pins 6 and 7 is HI so that the intensity current from pins 1, 2, 9, and 16 can pass to the output. However, pin 6 goes LO during Vertical Chopped Blanking and both pins 6 and 7 go LO for Horizontal Chopped Blanking or during a readout display. This blocks the output current and the CRT is blanked. The Vertical Chopped Blanking signal is connected to pin 6 of U170 directly from pin 4 of U120. The Horizontal Chopped Blanking signal is connected to U170 from pin 4 of U130 through LR134, Q146, and CR145-CR146 (see diagram 2). Notice that this signal is connected to the

(A)

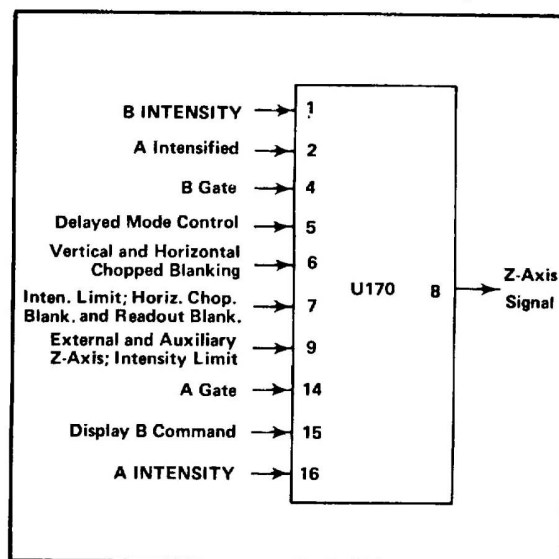


Fig. 3-7. Input and output pins for Z-Axis Logic stage

collector of Q146. This transistor is normally operating in the saturated condition and the HI Horizontal Chopped Blanking level from U130 is the collector source voltage. When the Horizontal Chopped Blanking level goes LO, the current through Q146 drops to produce a corresponding LO level at its emitter. This level is connected to both pins 6 and 7 of U170 through CR145 and CR 146.

Q146 also controls the levels at pins 6 and 7 for readout displays. The Z-Axis Logic OFF Command from the Readout Circuit is connected to the base of Q146 through VR148 and R147. This level is normally HI so Q146 operates as controlled by the Horizontal Chopped Blanking level at its collector. When a readout display is to be presented, the Z-Axis Logic OFF Command drops LO and this level is coupled to the base of Q146 through VR148 with very little voltage attenuation. Q146 is reverse-biased to produce a LO level at its emitter. This level is coupled to pins 6 and 7 of U170 through CR145 and CR146 to block the Z-Axis Logic output current during the readout display (intensity of readout display determined by a separate Readout Intensity level connected directly to the Z-Axis Amplifier; see CRT Circuit description). Diode CR147 clamps the emitter of Q146 at about -0.6 volts when this transistor is off.

The Intensity Limit input at pins 7 and 9 provides protection for the CRT phosphor at slow sweep rates or when the BEAM FINDER is actuated. For conditions that do not require limiting, R140-R141-R142-R143R144-R145-R175 establish the operating current at pins 7 and 9. When either of the time-base units is set to a sweep rate which requires intensity limiting the junction of

R143-R144-R145 is connected to ground in the time-base unit. This drops the current level at pins 7 and 9 to limit the output current from this stage. Limiting the output current of this stage in turn limits the maximum trace intensity for all CRT displays whenever either of the time-base units is set to a sweep rate that requires intensity limiting. The Max Intensity adjustment R140 is set to provide optimum writing rate on the CRT when the INTENSITY controls are set fully clockwise.

The A INTENSITY control sets the output current level when the A Gate at pin 14 is HI and the Display B Command at pin 15 is LO. Whenever the A Gate level goes LO indicating that the A Sweep is complete or the Display B Command goes HI indicating that the B Sweep is being displayed, the A INTENSITY current is blocked. The current from the A INTENSITY control (see diagram 12) is connected to pin 16 through R176.

In the delayed mode, current is added to the A INTENSITY current during the A Sweep time to intensify a portion of the trace. This intensified portion is coincident with the B Sweep time to provide an indication of the portion of the A sweep which will be displayed in the delayed mode. The A Intensified current is supplied to pin 2 of U170 from the A INTENSITY control through R178. With this configuration, the intensified current increases as the A INTENSITY control setting is advanced to provide a proportional intensity increase in the intensified zone as the overall A Sweep intensity increases. Therefore, the intensified zone is more readily visible at high intensity levels. The intensified current is added to the A INTENSITY current to produce an intensified zone on the A SWEEP under the following conditions: HI A Gate level at pin 14, LO Display B Command at pin 15, HI B Gate level at pin 4, and HI Delayed Mode Control Out level at pin 5.

The B INTENSITY control determines the output current when the B Gate level at pin 4 and the Display B Command at pin 15 are both HI. The current from the B INTENSITY control (see diagram 12) is connected to the Z-Axis Logic stage through R179.

The current level established by the intensity controls can be altered by the External and Auxiliary Z-Axis current level at pin 9. The current at this pin can come from the Z AXIS INPUT connectors on the rear panel through R112 or from any of the plug-in compartments through R110, R 11 1, R 113, or R 114. This current either increases or decreases (depending on polarity) the output current to modulate the intensity of the display. Input from the Z AXIS INPUT connectors allows the trace to be modulated by external signals. The auxiliary Z-Axis inputs from the plug-in compartments allow special purpose plug-in units to modulate the display intensity. Diodes CR175 and CR176 limit the maximum voltage change at pin 9 to about + and

-0.6 volt to protect the Z-Axis Logic Stage if an excessive voltage is applied to the Z AXIS INPUT connectors.

Fig. 3-8A shows a logic diagram of the Z-Axis Logic stage. Notice the current-driven inputs as indicated by the current-generator symbols at the associated inputs. An input/output table for the Z-Axis Logic stage is given in Fig. 3-8B.

### Horizontal Binary

The Horizontal Binary stage produces the Display B Command to determine which horizontal unit is to be displayed on the CRT. When this level is HI, the B Horizontal unit is displayed and when it is LO, the A Horizontal unit is displayed. The Display B Command is used in the following stages within the Logic Circuit: Horizontal Logic (A and B Lockout), Z-Axis Logic, and Vertical Binary. In addition, it is connected to the following circuits elsewhere in the instrument to indicate which horizontal unit is to be displayed: Main Interface circuit (A and B Horizontal plug-in compartments), Vertical Interface circuit (for trace separation), and Horizontal Interface circuit (for horizontal channel selection). Fig. 3-9 identifies the function of the input pins for this stage. The following discussions describe the operation of the Horizontal Binary stage in each position of the HORIZONTAL MODE switch. Notice that the levels at pins 3, 4, 7, and 10 are determined by the HORIZONTAL MODE switch (see diagram 12). This switch indicates which horizontal mode has been selected by providing a HI output level on only one of four output lines; the remaining lines are LO. Therefore, for U150 either pin 3, pins 4 and 7 (notice that pins 4 and 7 are tied together at U150), or pin 10 can be HI and the two unselected lines from the HORIZONTAL MODE switch remain LO.

#### 1. A MODE

When the HORIZONTAL MODE switch is set to A, the Display B Command is LO to indicate to all circuits that the A Horizontal unit is to be displayed. The input conditions are:

Pin 3 HI-HORIZONTAL MODE switch set to A.

Pin 4 and 7 LO-HORIZONTAL MODE switch set to any position except B.

Pin 10 LO-HORIZONTAL MODE switch set to any position except CHOP.

#### 2. B MODE

Selecting the B horizontal mode provides a HI Display B

Command to all circuits. The input conditions are:

Pin 3 LO-HORIZONTAL MODE switch set to any position except A.

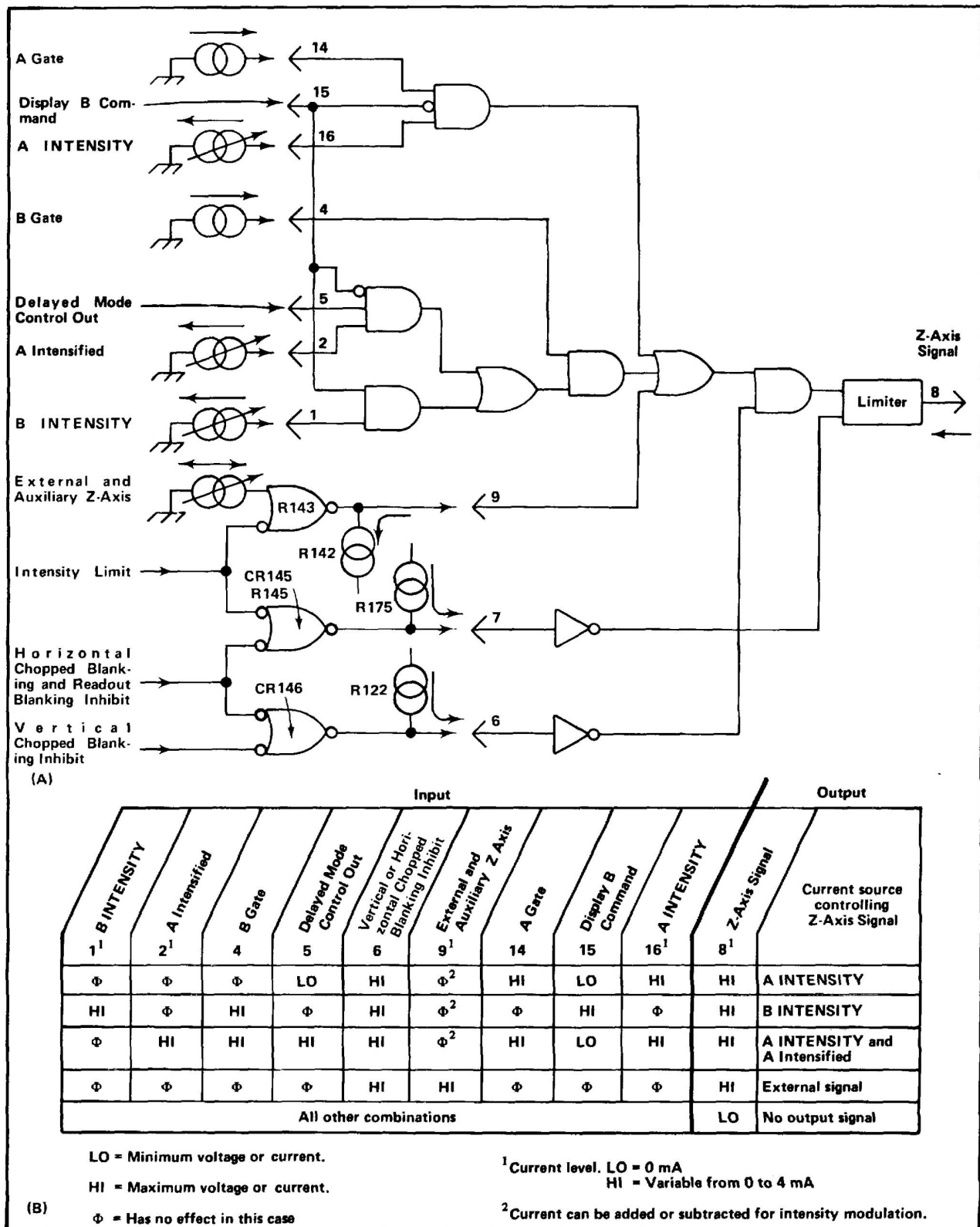


Fig. 3-8. (A) Logic diagram for Z-Axis Logic circuit, (B) Table of input/output combinations for Z-Axis Logic circuit



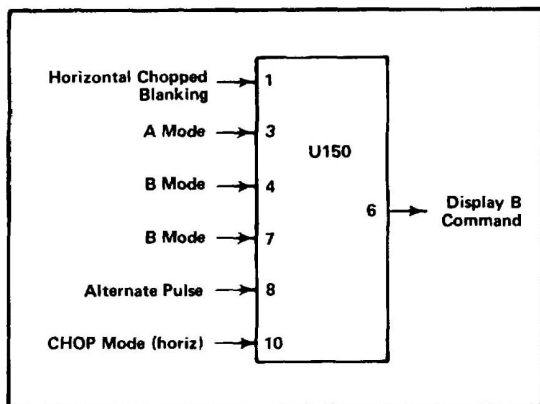


Fig. 3-9. Input and output pins for Horizontal Binary stage

Pin 4 and 7 HI-HORIZONTAL MODE switch set to B.  
Pin 10 LO-HORIZONTAL MODE switch set to any position except CHOP.

### 3. CHOP MODE

In the CHOP position of the HORIZONTAL MODE switch, the Display B Command switches between the HI and LO levels to produce a display which switches between the A and B Horizontal units at a 0.2 megahertz rate. The repetition rate of the Display B Command in this mode is determined by the Horizontal Chopped Blanking pulse (see Chop Counter stage for further information on this pulse). Each time the Horizontal Chopped Blanking Pulse at pin 1 drops LO, the output at pin 6 switches to the opposite state. The input conditions which cause the output to change states are:

Pin 1 LO-Horizontal Chopped Blanking pulse generated by Chop Counter stage goes negative.  
Pin 3 LO-HORIZONTAL MODE switch set to any position except A.  
Pin 4 and 7 LO-HORIZONTAL MODE switch set to any position except B.  
Pin 10 HI-HORIZONTAL MODE switch set to CHOP.

### 4. ALT MODE

For ALT horizontal operation, the Display B Command switches to the opposite state each time the negative portion of the Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Display B Command in this mode is one-half the repetition rate of the Alternate Pulse. The input conditions which cause the output to change states are:

Pin 3 LO-HORIZONTAL MODE switch set to any position except A.  
Pin 4 and 7 LO-HORIZONTAL MODE switch set to any position except B.  
Pin 8 LO-Alternate Pulse generated by Horizontal Logic stage goes negative.  
Pin 10 LO-HORIZONTAL MODE switch set to any position except CHOP.

Fig. 3-10A shows a logic diagram of the Horizontal Binary stage. An input/output table showing the conditions for each position of the HORIZONTAL MODE switch is shown in Fig. 3-10B.

### Vertical Binary

The Vertical Binary stage produces the Display Right Command to determine which vertical unit is to be displayed on the CRT. When this output level is HI, the Right Vertical unit is displayed and when it is LO, the Left Vertical unit is displayed. In the ALT or CHOP positions of the HORIZONTAL MODE switch, (non-delayed operation only), the output of this stage is slaved to the output of the Horizontal Binary stage so that the Display Right Command is always HI when the Display B Command is LO, and vice versa. This action allows independent pairs operation in the ALT position of the VERTICAL MODE switch and the ALT or CHOP positions of the HORIZONTAL MODE switch whereby the Left Vertical unit is always displayed at the sweep rate of the B Time-Base unit and the Right Vertical unit at the sweep rate of the A Time-Base unit to simulate dual-beam operation for repetitive sweeps.

When the A Time-Base unit is set to the delayed mode, the repetition rate of the Display Right Command is one-half the repetition rate of the Display B Command input. This results in each vertical unit being displayed first against the A Time-Base unit (delaying) and the B Time-Base unit (delayed) before the display is switched to the other vertical unit. The Display Right Command is used in the following stages within the Logic Circuit: Plug-In Binary, Vertical Chopped Blanking, and Vertical Mode Control. It is also connected to the following circuits elsewhere in the instrument (through Vertical Mode Control stage, ALT vertical mode only) to indicate which vertical unit is to be displayed: Main Interface circuit (Left and Right Vertical plug-in compartments and trigger selection circuitry) and Vertical Interface circuit.

Fig. 3-11 identifies the function of the input pins for the Vertical Binary stage. This stage uses the same type of integrated circuit as the Horizontal Binary stage. Notice the Display A level at pin 7. This input is the inverse of the Display B level at pin 8. Therefore the Display A level is always HI when the Display B level is LO, and vice versa. The following discussions describe the operation of the Vertical

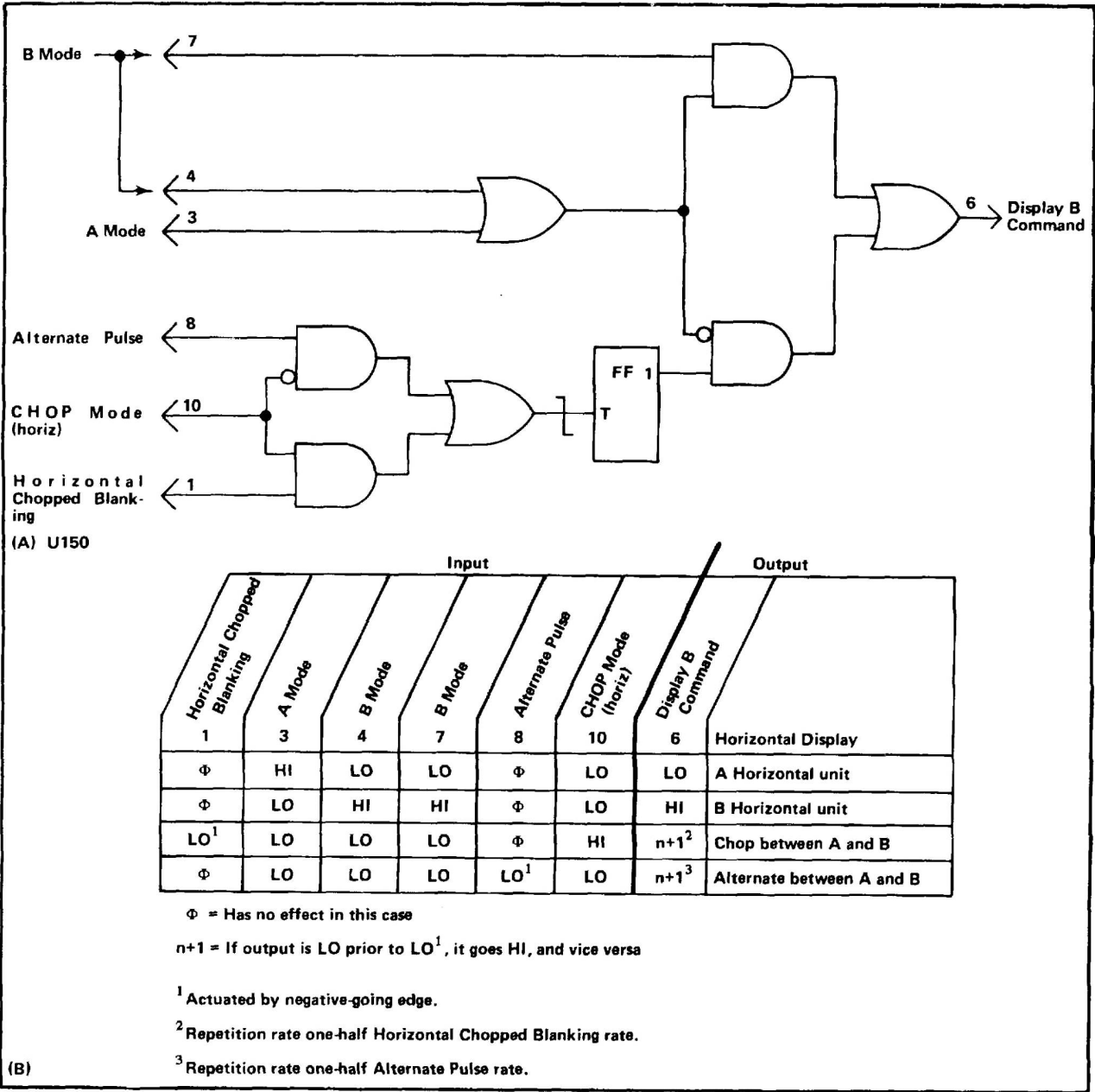


Fig. 3-10. (A) Logic diagram for Horizontal Binary stage, (B) Table of input/output combinations for the Horizontal Binary stage.

tical Binary stage in relation to the modes of operation that can occur.

NOTE

Although the output at pin 6 of U180 is always controlled by the HORIZONTAL MODE switch as described here, this level determines the Vertical Mode control level at the collector of 0196 only in

(A)

the A L T position of the VERTICAL MODE switch due to AND gate CR 183-CR 184. See the discussion on the Vertical Mode Logic stage in this section for further information.

1. A ORB MODE

When the HORIZONTAL MODE switch is set to either A or B, the Display Right Command switches to the

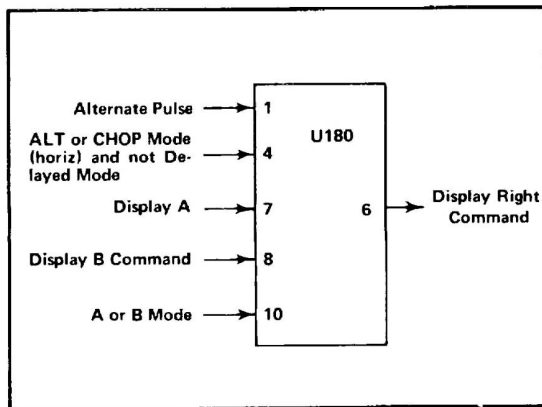


Fig. 3-11. Input and output pins for Vertical Binary stage

opposite state each time an Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Display Right Command in this mode is one-half the repetition rate of the Alternate Pulse. The input conditions for these modes are:

Pin 1 LO-Alternate Pulse generated by Horizontal Logic stage goes negative.

Pin 4 LO-HORIZONTAL MODE switch in any position except ALT or CHOP, or the A Time-Base unit is set for delayed sweep.

Pin 10 HI-HORIZONTAL MODE switch set to A or B.

## 2. ALT OR CHOP MODE (HORIZ)-NON-DELAYED

In the ALT or CHOP positions of the HORIZONTAL MODE switch, the output level at Pin 6 is the same as the Display A level at pin 7. The Display A level is produced by inverting the Display B Command from the Horizontal Binary stage. Therefore, the repetition rate of the output signal is the same as the Display B Command. The result with the VERTICAL MODE switch set to ALT and the A Time-Base unit set for non-delayed operation is that the Right Vertical unit is always displayed at the sweep rate of the A Time-Base unit and the Left Vertical unit at the sweep rate of the B Time-Base unit (independent-pairs operation). The input conditions to provide a HI output level so that the Right Vertical unit can be displayed at the A Sweep rate are:

Pin 4 HI-HORIZONTAL MODE switch set to ALT or CHOP with non-delayed sweep.

Pin 7 HI-A Sweep is to be displayed (Display B Command LO).

Pin 10 LO-HORIZONTAL MODE switch set to any position except A or B.

The input conditions to provide a LO output level so the Left Vertical unit can be displayed at the B Sweep rate are:

Pin 4 HI-HORIZONTAL MODE switch set to ALT or CHOP with non-delayed sweep.

Pin 7 LO-B Sweep is to be displayed (Display B Command HI).

Pin 10 LO-HORIZONTAL MODE switch set to any position except A or B.

The Display Right Command switches from HI to LO along with the Display A level at pin 7 (inverse of Display B Command). However, notice that the Display Right Command changes from HI to LO as the Display B Command changes from LO to HI, and vice versa.

## 3. ALT OR CHOP MODE (HORIZ)-DELAYED

If the A Time-Base unit is set to the delayed mode when the HORIZONTAL MODE switch is set to either ALT or CHOP, the operation of the stage is changed from that discussed above. Now, the Display Right Command switches between the HI and LO states at a rate which is one-half the repetition rate of the Display B Command. The resultant CRT display in the ALT position of the VERTICAL MODE switch allows the Right Vertical unit to be displayed first against the A Sweep (delaying) and then against the B Sweep (delayed). Then the display switches to the Left Vertical unit and it is displayed consecutively against the A and B Sweeps in the same manner. The input conditions for this mode of operation are:

Pin 4 LO-A Time-Base unit set for delayed operation.

Pin 8 LO-Display B Command generated by Horizontal Binary stage goes negative.

Pin 10 LO-HORIZONTAL MODE switch set to any position except A or B.

A logic diagram of the Vertical Binary stage is shown in Fig. 3-12A. Several Logic functions in this stage are performed by logic devices made up of discrete components. The components that make up these logic devices are identified on the logic diagram. An input/output table for the Vertical Binary stage is given in Fig. 3-12B.

## Plug-In Binary

The Plug-In Binary stage produces the Display Channel 2 Command to provide a Plug-In Alternate Command to dual-trace vertical units. Fig. 3-13 identifies the function of the input pins for the Plug-In binary stage. This stage uses the same type of integrated circuit as the Horizontal Binary and Vertical Binary stages.

(A)

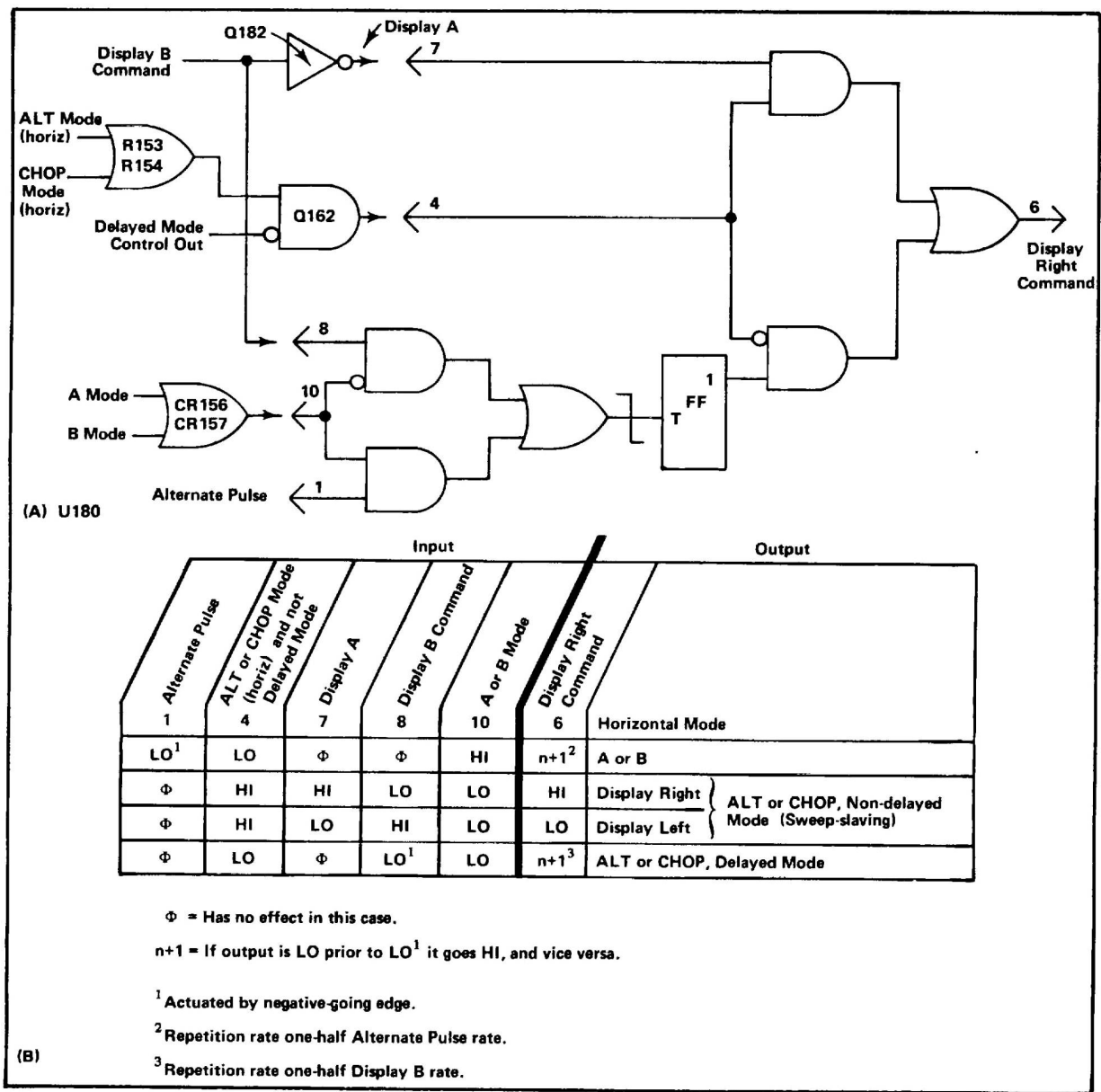


Fig. 3-12. (A) Logic diagram for Vertical Binary stage, (B) Table of input/output combinations for the Vertical Binary stage

When the Display Channel 2 Command level is HI and the vertical plug-ins are set for alternate operation, Channel 2 of the dual-trace unit is displayed. When it is LO, Channel 1 is displayed. The repetition rate of the Display Channel 2 Command is determined by the setting of the VERTICAL MODE switch. For all positions of the VERTICAL MODE switch except ALT, the Display Channel 2 Command is the same as the Display Right Command from the Vertical Binary stage. Since the Display Right Command was

(A)

derived directly from the Display B Command, this allows the two channels of a dual-trace vertical unit to be slaved to the time-base units (non-delayed, dual-sweep horizontal modes only) in the same manner as previously described for independent-pairs operation between the vertical and time-base units. The resultant CRT presentation when the dual-trace unit is set for alternate operation displays the Channel1 trace at the sweep rate of the B Time-Base unit and the Channel 2 trace at the sweep rate of the A Time Base unit.

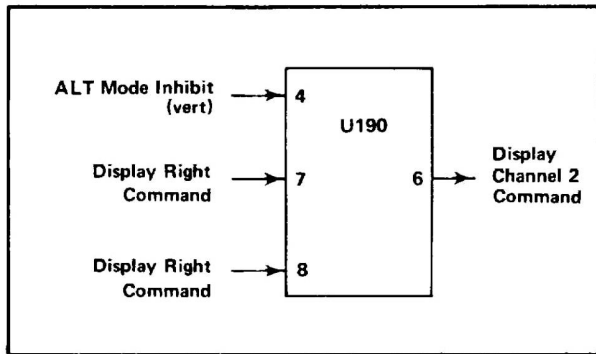


Fig. 3-13. Input and output pins for Plug-In Binary stage

Input conditions for a LO output level so that Channel 1 of the vertical plug-in can be displayed at the B Sweep rate are:

Pin 4 HI-VERTICAL MODE switch set to any position except ALT.

Pin 7 LO-B Sweep to be displayed (Display Right Command and Display B Command HI).

The input conditions to provide a HI output level so that Channel 2 of the plug-in can be displayed at the A Sweep rate are:

Pin 4 HI-VERTICAL MODE switch set to any position except ALT.

Pin 7 HI-A Sweep to be displayed (Display Right Command and Display B Command LO).

The Display Channel 2 Command switches from HI to LO as the Display B Command from the Horizontal Binary stage switches from LO to HI, and vice versa.

When the VERTICAL MODE switch is set to ALT, the Display Right Command from the Vertical Binary stage switches the vertical display between the two vertical units. However, if either or both of the vertical plug-in units are dual-trace units, they can be operated in the alternate mode also. To provide a switching command to these units, the Plug-In Binary stage produces an output signal with a repetition rate one-half the repetition rate of the Display Right Command. The sequence of operation when two dual-trace vertical units are installed in the vertical plug-in compartments and they are both set for alternate operation, is as follows (VERTICAL MODE and HORIZONTAL MODE switches set to ALT): 1) Channel 1 of Left Vertical unit at sweep rate of B Time-Base units, 2) Channel 1 of Right Vertical unit at sweep rate of A Time-Base unit, 3) Channel 2 of Left Vertical unit at sweep rate of B Time-Base unit, 4) Channel 2 of Right Vertical unit at sweep rate

of A Time-Base unit. Notice that under these conditions, both channels of the Left Vertical unit are displayed at the B Sweep rate and that both channels of the Right Vertical unit are displayed at the A Sweep rate. The repetition rate at the output of this stage is one-half the Display Right Command rate. Input conditions when the VERTICAL MODE switch is set to ALT are:

Pin 4 LO-VERTICAL MODE switch set to ALT.

Pin 8 LO-Display Right Command generated by Vertical Binary stage goes negative.

Fig. 3-14A shows a logic diagram of the Plug-In Binary stage. An input/output table for this stage is given in Fig. 3-14B.

### Clock Generator

One half of integrated circuit U120 along with the external components shown in Fig. 3-15A make up the Clock Generator stage. R1, Q1, Q2, and Q3 represent an equivalent circuit which is contained within U120A. This circuit along with discrete components C117-R116-R117-R118 comprise a two-megahertz free-running oscillator to provide a timing signal (clock) for vertical, horizontal, and plug-in chopping.

The stage operates as follows: Assume that Q2 is conducting and Q1 is off. The collector current of Q2 produces a voltage drop across R1 which holds Q1 off. This negative level at the collector of Q2 is also connected to pin 14 through Q3 (see waveforms in Fig. 3-15B at time T). Since there is no current through Q1, C117 begins to charge towards -15 volts through R116-R117. The emitter of Q1 goes negative as C117 charges until it reaches a level about 0.6 volt more negative than the level at its base. Then, Q1 is forward biased and its emitter rapidly rises positive (see time T, on waveforms). Since C117 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q1 pulls the emitter of Q2 positive also, to reverse-bias it. With Q2 reverse biased, its collector rises positive to produce a positive output level at pin 14.

Now, conditions are reversed. Since Q2 is reverse biased, there is no current through it. Therefore, C117 can begin to discharge through R118. The emitter level of Q2 follows the discharge of C117 until it reaches a level about 0.6 volt more negative than its base. Then, Q2 is forward biased and its collector drops negative to reverse-bias Q1. The level at pin 14 drops negative also, to complete the cycle. Once again, C117 begins to charge through R116-R117 to start the second cycle.

Two outputs are provided from this oscillator. The Delay Ramp signal from the junction of R1 16-R1 17 is con-

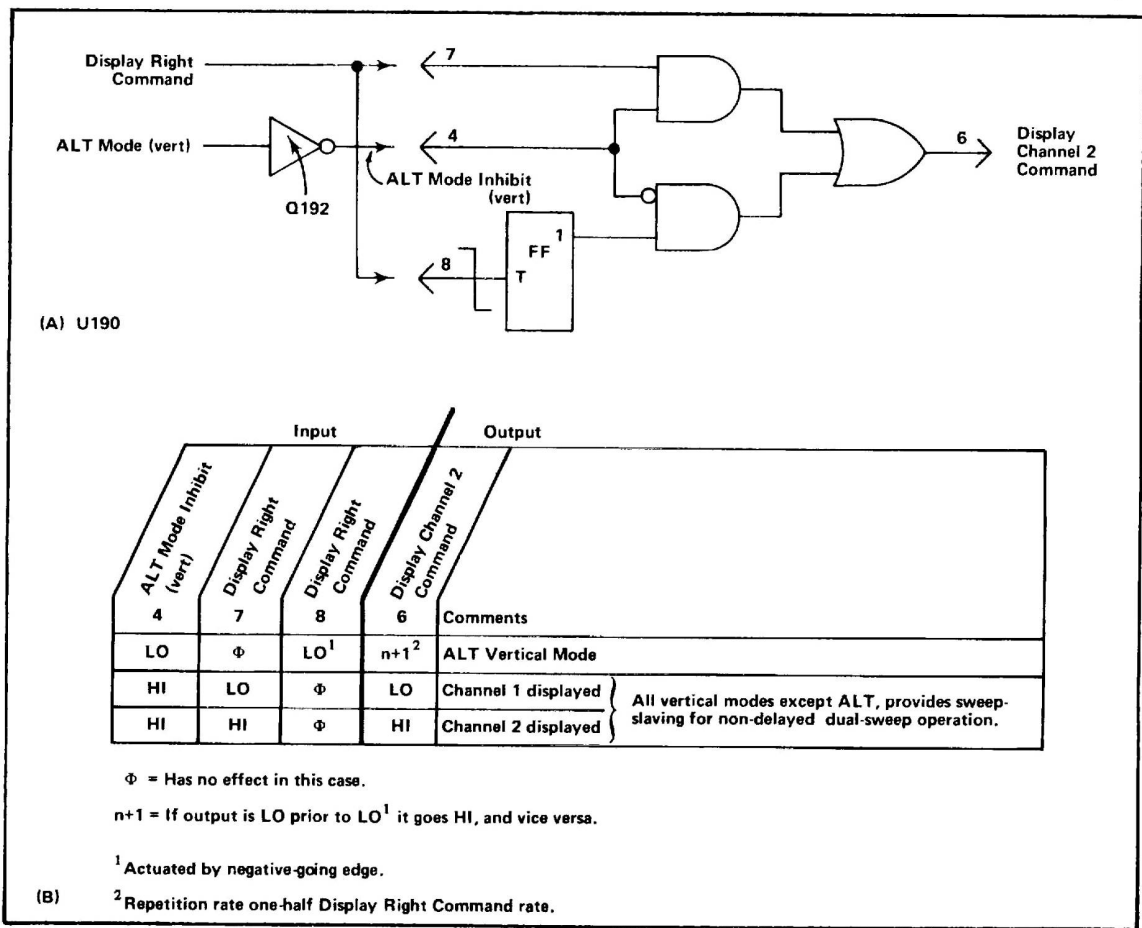


Fig. 3-14. (A) Logic diagram for Plug-In Binary stage, (B) Table of input/output combinations for the Plug-In Binary stage

to the Vertical Chopped Blanking stage. This signal has the same waveshape as shown by the waveform at pin 13, with its slope determined by the divider ratio between R116-R117. A square-wave output is provided at pin 14. The frequency of this square wave is determined by the overall RC relationship between C117-R116-R117-R118, and its duty cycle is determined by the ratio of R 116-R 117 to R118.

The square wave at pin 14 is connected to pin 16 through C1 19. C119, along with the internal resistance of U120A, differentiates the square wave at pin 14 to produce a negative-going pulse coincident with the falling edge of the square wave (positive-going pulse coincident with rising edge has no effect on circuit operation). This negative-going pulse is connected to pin 15 through an inverter-shaper which is also part of U120A. The output at pin 15 is a positive-going Clock pulse at a repetition rate of about two megahertz.

(A)

Vertical Chopped Blanking

The Vertical Chopped Blanking stage is made up of the remaining half of integrated circuit U120. This stage determines if Vertical Chopped Blanking pulses are required based upon the operating mode of the vertical system or the plug-in units (dual-trace units only). Vertical Chopped Blanking pulses are produced if: 1) VERTICAL MODE switch is set to CHOP; 2) Dual-trace vertical unit is operating in the chopped mode and that unit is being displayed; 3) Dual-trace vertical unit is operating in the chopped mode with the VERTICAL MODE switch set to ADD. The repetition rate of the negative-going Vertical Chopped Blanking pulse output at pin 4 is two megahertz for all of the above conditions as determined by the Clock Generator stage.

The Delay Ramp signal from the Clock Generator stage determines the repetition rate and pulse width of the Vertical Chopped Blanking pulses. The Delay Ramp applied to

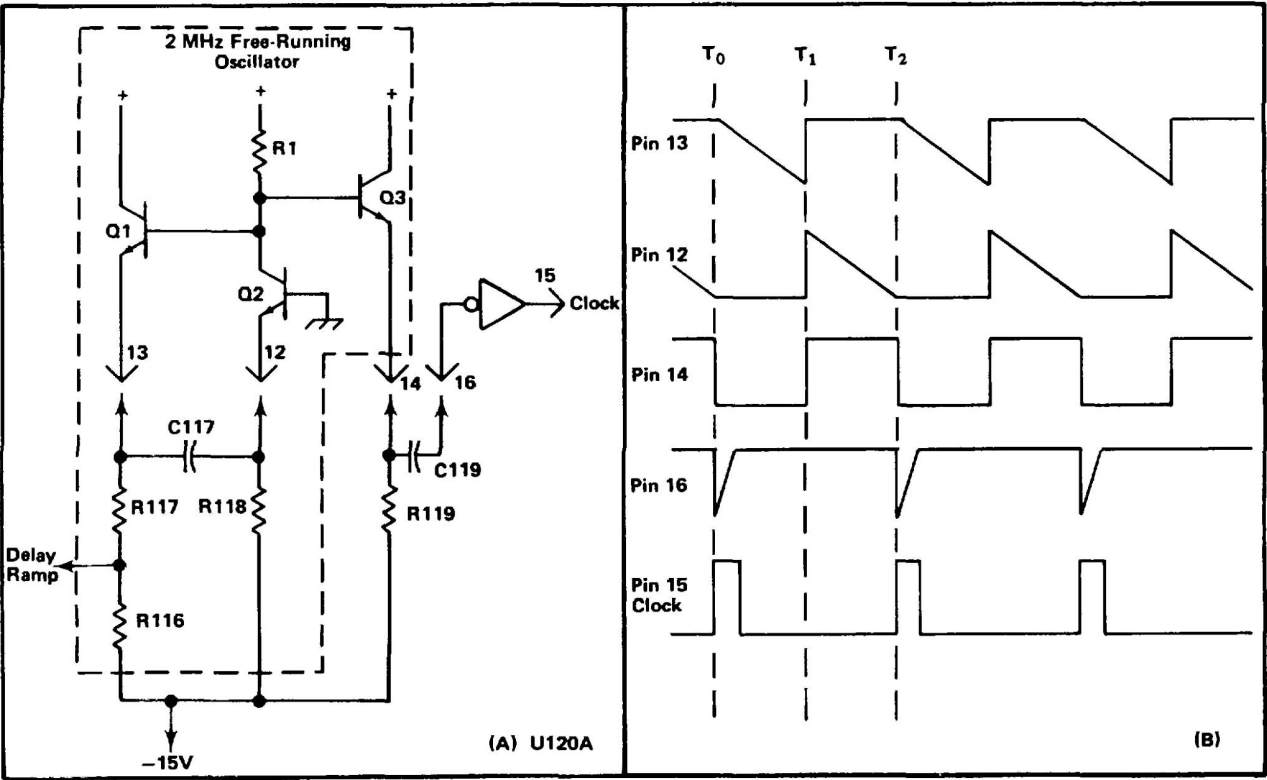


Fig. 3-15. (A) Diagram of Clock Generator stage, (B) Idealized waveforms for Clock Generator stage.

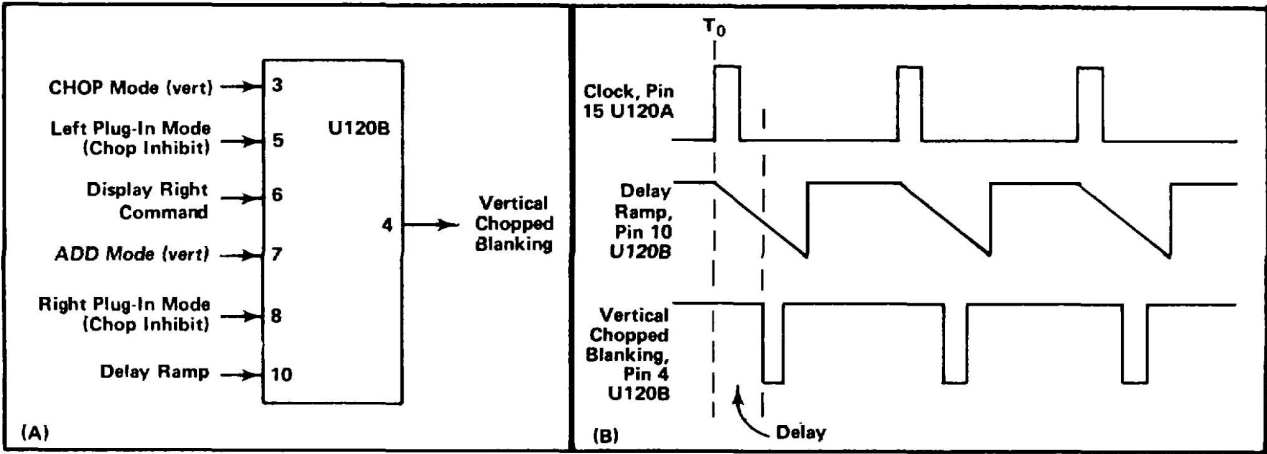


Fig. 3-16. (A) Input and output pins for Vertical Chopped Blanking stage, (B) Idealized waveforms for Vertical Chopped Blanking stage.

pin 10 starts to go negative from a level of about +1.1 volts coincident with the leading edge of the Clock pulse (see waveforms in Fig. 3-16B). This results in a HI quiescent condition for the Vertical Chopped Blanking pulse. The slope of the negative-going Delay Ramp is determined by the Clock Generator stage. As it reaches a level slightly negative from ground, the Vertical Chopped Blanking pulse

output level changes to the LO state. This signal remains LO until the Delay Ramp goes HI again. Notice the delay between the leading edge of the Clock pulse generated by U120A and the leading edge of the Vertical Chopped Blanking pulses (see Fig. 3-16B). The amount of delay between the leading edges of these pulses is determined by the slope of the Delay Ramp applied to pin 10. This delay is



necessary due to the delay line in the vertical deflection system. Otherwise, the trace blanking resulting from the Vertical Chopped Blanking pulse would not coincide with the switching between the displayed traces. The duty cycle of the square wave produced in the Clock Generator stage determines the pulse width of the Vertical Chopped Blanking pulses (see Clock Generator discussion for more information).

Whenever this instrument is turned on, Vertical Chopped Blanking pulses are being produced at a two-megahertz rate. However, these pulses are available as an output at pin 4 only when the remaining inputs to U 120B are at the correct levels. The following discussions give the operating conditions which produce Vertical Chopped Blanking pulses to blank the CRT during vertical chopping. Fig. 3-16A identifies the function of the pins of U120B.

### 1. CHOP VERTICAL MODE

When the VERTICAL MODE switch is set to CHOP, Vertical Chopped Blanking pulses are available at pin 4 at all times. The input conditions necessary are:

Pin 3 HI-VERTICAL MODE switch set to CHOP.

Pin 7 LO-VERTICAL MODE switch set to any position except ADD.

Pin 10 LO-Delay Ramp more negative than about zero volts.

### 2. LEFT VERTICAL UNIT SET FOR CHOPPED MODE

If the Left Vertical unit is set for chopped operation, the setting of the VERTICAL MODE switch determines whether Vertical Chopped Blanking pulses are available. If the VERTICAL MODE switch is set to the CHOP position, conditions are as described in No. 1 above. Operation in the ADD position of the VERTICAL MODE switch is given later. For the LEFT position of the VERTICAL MODE switch or when the Left Vertical unit is to be displayed in the ALT mode, Vertical Chopped Blanking pulses are available at all times (two-megahertz rate). The input conditions are:

Pin 3 LO-VERTICAL MODE switch set to any position except CHOP.

Pin 5 LO-Left Vertical unit set to chopped mode.

Pin 6 LO-Left Vertical unit to be displayed (Display Right Command LO).

Pin 7 LO-VERTICAL MODE switch set to any position except ADD.

Pin 10 LO-Delay Ramp more negative than about zero volts.

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Notice that the Display Right Command at pin 6 must be LO for output pulses to be available at pin 4. This means that when the VERTICAL MODE switch is set to ALT, Vertical Chopped Blanking pulses will be produced only during the time that the Left Vertical unit is to be displayed (unless Right Vertical unit is also set for chopped operation).

### 3. RIGHT VERTICAL UNIT SET FOR CHOPPED OPERATION

If the Right Vertical unit is set for the chopped mode, operation is the same as described above for the Left Vertical unit except that Vertical Chopped Blanking pulses are produced when the VERTICAL MODE switch is set to RIGHT or when the Display Right Command is HI in the ALT mode. The input conditions are: Pin 3 LO-VERTICAL MODE switch set to any position except CHOP.

Pin 6 HI-Right Vertical unit to be displayed (Display Right Command HI).

Pin 7 LO-VERTICAL MODE switch set to any position except ADD.

Pin 8 LO-Right Vertical unit set to chopped mode.

Pin 10 LO-Delay Ramp more negative than about zero volts.

### 4. ADD VERTICAL MODE

When the VERTICAL MODE switch is in the ADD position and either or both of the vertical units are operating in the chopped mode, Vertical Chopped Blanking pulses must be available to block out the transition between the traces of the vertical units. The input conditions are: Pin 3 LO-VERTICAL MODE switch set to any position except CHOP.

Pin 5 LO-Left Vertical unit set to chopped mode (can be HI if pin 8 is LO).

Pin 7 HI-VERTICAL MODE switch set to ADD.

Pin 8 LO-Right Vertical unit set to chopped mode (can be HI if pin 5 is LO).

Pin 10 LO-Delay Ramp more negative than about zero volts.

Fig. 3-17A shows a logic diagram of the Vertical Chopped Blanking stage. Notice the comparator block on this diagram (one input connected to pin 10). The output of this comparator is determined by the relationship between the levels at its inputs. If pin 10 is more positive (HI)

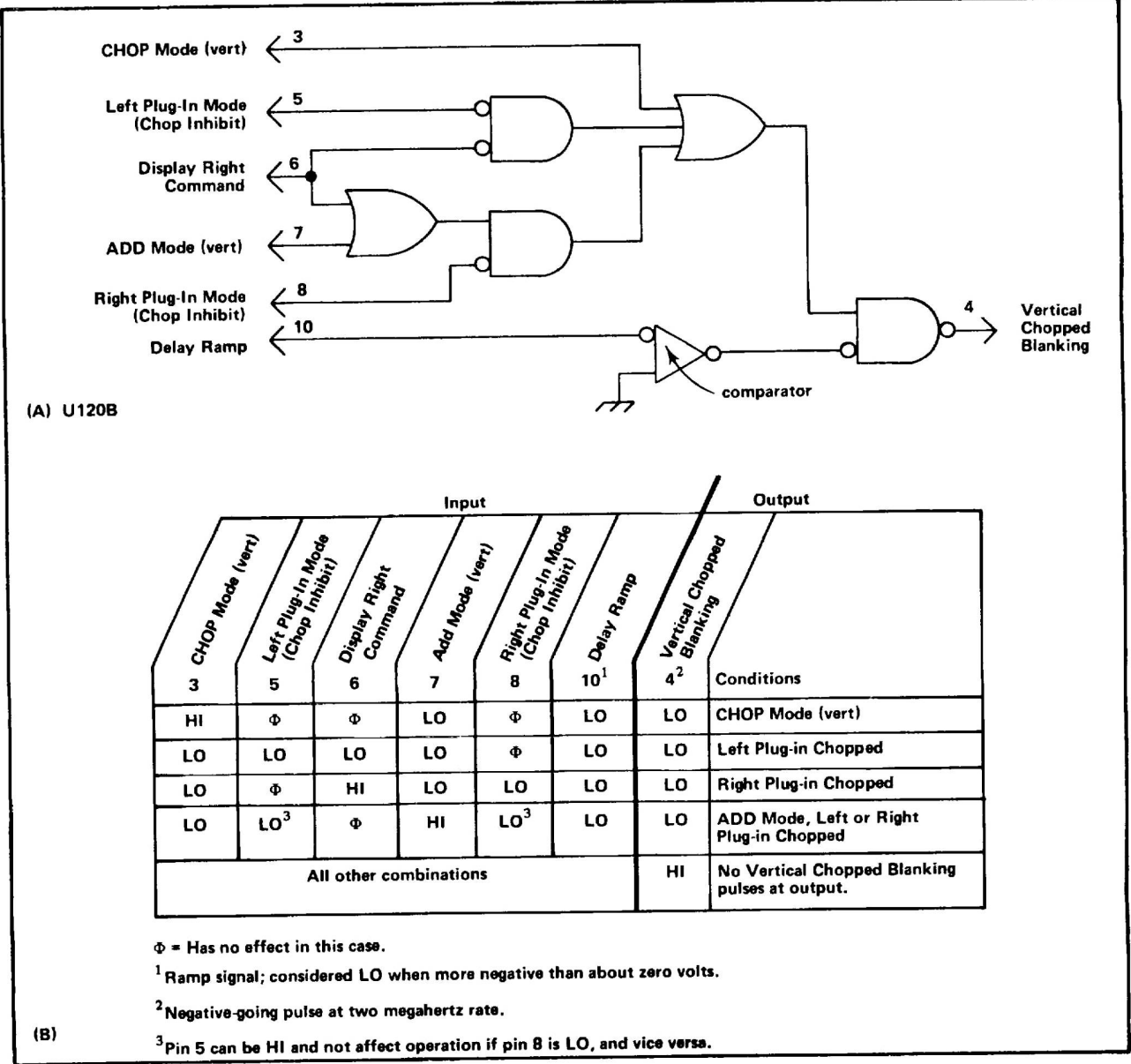


Fig. 3-17. (A) Logic diagram for Vertical Chopped Blanking stage, (B) Table of input/output combinations for Vertical Chopped Blanking stage

than the grounded input, the output is HI also; if it is more negative (LO), the output is LO. An input/output table for this stage is given in Fig. 3-17B.

Chop Counter

The Chop Counter stage produces the Vertical Chopping Signal, the Plug-In Chop Command, and the Horizontal Chopped Blanking signal. The Clock pulse produced by the Clock Generator stage provides the timing signal for this stage. The functions of the input and output pins for the

Chop Counter stage are identified in Fig. 3-18A. Idealized waveforms showing the timing relationship between the input and output signals for this stage are shown in Fig.3-18B.

The repetition rate of the output signals from this stage is determined by the setting of the HORIZONTAL MODE switch. When the HORIZONTAL MODE switch is set to any position except CHOP, the repetition rate of the Vertical Chopping Signal output at pin 1 is one megahertz (onehalf Clock rate). This determines the switching between the

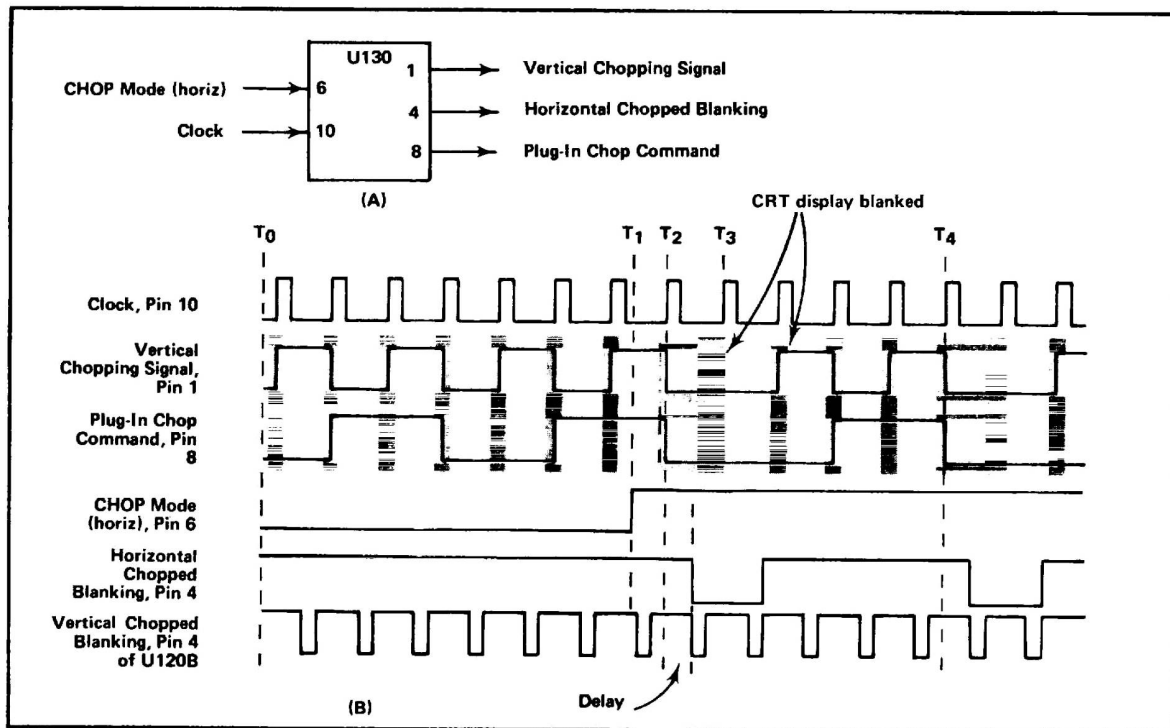


Fig. 3-18. (A) Input and output pins for Chop Counter stage, (B) Idealized waveforms for Chop Counter stage.

Left and Right Vertical units when the VERTICAL MODE switch is set to CHOP. At the same time, the repetition rate of the Plug-In Chop Command at pin 8 is 0.5 megahertz (one-fourth Clock rate). This provides a chopping signal to dual-trace vertical units to provide switching between the two channels. The relationship between these output signals and the Clock input is shown by the waveforms in Fig. 3-18B in the area between T<sub>0</sub> and T<sub>1</sub>. During this time, the level at pin 4 remains HI.

When the HORIZONTAL MODE switch is set to CHOP, the basic repetition rate of the Vertical Chopping Signal and the Plug-In Chop Command is altered. For example, if the HORIZONTAL MODE switch is changed to the CHOP position at time T<sub>1</sub> (see Fig. 3-18B), a HI level is applied to pin 6. This stage continues to produce outputs at pins 1 and 8 in the normal manner until both outputs are at their HI level (see time T<sub>2</sub>; this condition only occurs once every fifth Clock pulse when the HORIZONTAL MODE switch is set to CHOP). When both of these outputs are at their HI level, the next Clock pulse switches both outputs LO and at the same time switches the Horizontal Chopped Blanking to the LO level. However, this change does not appear at pin 4 immediately due to a delay network in the circuit. The delay is necessary so the Horizontal Chopped Blanking coincides with the Vertical Chopped Blanking produced by

(A)

U120A and the switching between the displayed signals (compare bottom two waveforms of Fig. 3-18B; also see Vertical Chopped Blanking for further information). After the delay time, the output level at pin 4 goes LO where it remains for about 0.5 microsecond which is equal to the period of the Clock pulse (two megahertz repetition rate). The Horizontal Chopped Blanking time must be longer than the Vertical Chopped Blanking time since it takes more time for the display to switch between horizontal units than between vertical units. During the time that the level at pin 4 is LO, the CRT is blanked and the Vertical Chopping Signal and the Plug-In Chop Command cannot change levels. The Clock pulse at T<sub>3</sub> changes only the Horizontal Chopped Blanking output at pin 4. The level on this pin goes HI after the delay time to unblank the CRT.

For the next three trigger pulses, the Vertical Chopping Signal output and Plug-In Chop Command operate in the normal manner. However, just prior to the fourth clock pulse (time T<sub>4</sub>) both outputs are again at their HI level. The fourth Clock pulse at T<sub>4</sub> switches the output at pin 1, pin 8, and pin 4 (after delay) to the LO level to start the next cycle. Notice that a Horizontal Chopped Blanking pulse is produced at pin 4 with every fifth Clock pulse. Also notice that with the HORIZONTAL MODE switch set to CHOP, two complete cycles of the Vertical Chopping Signal are produced with each five Clock pulses (repetition rate two

fifths Clock rate) and one complete cycle of the Plug-In Chop Command for every five Clock pulses (one fifth Clock rate). Notice that the large shaded area produced by the Horizontal Chopped Blanking pulse (see Fig. 3-18B) is not part of the display time (CRT display blanked). However, about the same time segment is displayed from the vertical signal source with or without Horizontal Chopped Blanking due to the change in repetition rate when in the CHOP horizontal mode.

The Vertical Chopping Signal at pin 1 of U130 is connected to the Vertical Mode Logic stage (see following description) through L138-R138. This signal is HI when the Right Vertical unit is to be displayed and it is LO when the Left Vertical unit is to be displayed. The Plug-In Chop Command at pin 8 is connected to the plug-in units in the vertical compartments through L136-R136 via the Main Interface board. When this signal is HI, Channel 2 of the plug-in units can be displayed and when this level is LO, Channel 1 can be displayed. The Horizontal Chopped Blanking signal at pin 4 is connected through LR134 to the Horizontal Binary stage U150, and to the Z-Axis Logic stage U170 by way of Q146. When this signal is HI, the CRT is unblanked to display the selected signal. When it is LO, the CRT is blanked to allow switching between the time-base units.

A logic diagram of the Chop Counter stage is shown in Fig. 3-19. Details of operation for the flip-flops (FF) are shown in Table 3-1 at the front of this section. Use the waveforms given in Fig. 3-18B along with this diagram.

### Vertical Mode Logic

The Vertical Mode Logic stage is made up of discrete components CR128-CR139, CR183-CR184, and Q194-0196. These components develop the Vertical Mode Command which is connected to the Main Interface circuit (vertical plug-in compartments and trigger selection circuitry) and the Vertical Interface circuit to indicate which vertical unit is to be displayed. When this output level is HI, the Right Vertical unit is displayed and when it is LO, the Left Vertical unit is displayed.

The VERTICAL MODE switch located on diagram 12 provides control levels to this stage. This switch provides a HI level on only one of five output lines to indicate the selected vertical mode; the remaining lines are LO (notice that only four of the lines from the VERTICAL MODE switch are used on this schematic). Operation of this stage is as follows:

When the VERTICAL MODE switch is set to RIGHT, a HI level is connected to the base of Q194 through R127. This forward biases Q194 and the positive-going level at its emitter is connected to the emitter of Q196. The collector of Q196 goes HI to indicate that the Right Vertical unit is to be displayed. For the CHOP position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR128-CR139 through R128. Both diodes are forward biased so that the Vertical Chopping Signal from pin 1 of U130 can pass to the base of Q194. This signal switches between the HI and LO levels at a one-megahertz rate and it produces a corresponding Vertical Mode Command output

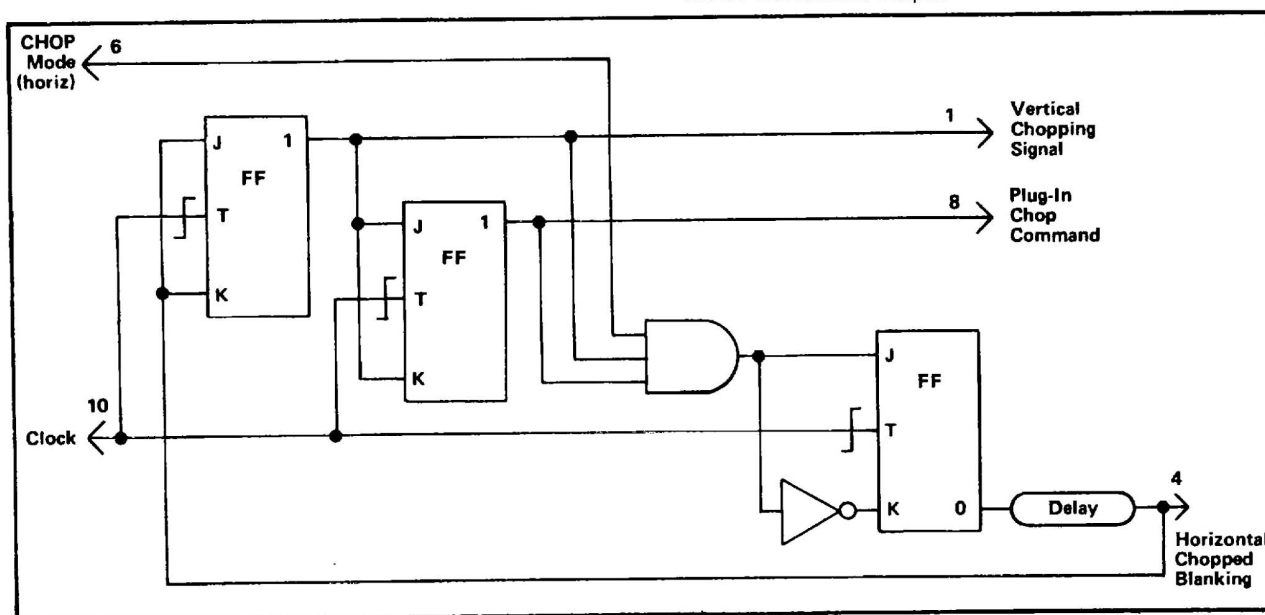


Fig. 3-19. Logic diagram of Chop Counter stage

at the collector of Q196. When the output is HI, the Right Vertical unit is displayed and when it switches to LO, the Left Vertical unit is displayed.

In the ALT position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR183-CR184 through R 183. These diodes are forward biased so the Display Right Command from pin 6 of the Vertical Binary stage can pass to the base of Q194 to determine the Vertical Mode Command level. The Display Right Command switches between its HI and LO levels at a rate determined by the Vertical Binary stage.

The control levels in the LEFT and ADD positions of the VERTICAL MODE switch are not connected to this stage. However, since only the line corresponding to the selected vertical mode can be HI, the RIGHT, CHOP, and ALT lines must remain at their LO level when either LEFT or ADD are selected. Therefore, the base of Q194 remains LO to produce a LO Vertical Mode Control output level at the collector of Q196.

A logic diagram of the Vertical Mode Logic stage is shown in Fig. 3-20. The discrete components which make up each logic function are identified.

### TRIGGER SELECTOR

#### General

The Trigger Selector circuit determines the trigger signal which is connected to the A and B time-base units as controlled by the A TRIGGER SOURCE and B TRIGGER

SOURCE switches. This circuit also provides the drive signal for the Vertical Signal Amplifier stage as controlled by the B TRIGGER SOURCE switch. Fig. 3-21 shows a detailed block diagram of the Trigger Selector circuit along with a simplified diagram of all the circuitry involved in selection of the trigger source. A schematic of the Trigger Selector circuit is shown on diagram 3 at the rear of this manual. Also see diagrams 1 and 12 for the trigger selection circuitry not shown on diagram 3.

#### Trigger Mode and ADD Signals

**General.** The circuitry shown on the left side of the simplified diagram in Fig. 3-21 determines the operation of the A and B Trigger Channel Switch stages. The A TRIGGER SOURCE switch S1011 controls the A Trigger Channel Switch U304 through Q24; the B TRIGGER SOURCE switch S1001 controls the B Trigger Channel Switch U324 through Q28. When the front-panel A or B TRIGGER SOURCE switches are set to the VERT MODE positions, the setting of the VERTICAL MODE switch determines the trigger selection. In the LEFT VERT or RIGHT VERT positions, the trigger signal is obtained from the indicated vertical unit. The following discussions give detailed operation in each position of the A and B TRIGGER SOURCE switches. It is written assuming that both of these switches are set to the same position. However, the A and B TRIGGER SOURCE switches can be operated independently to control the operation of the A and B Trigger Channel Switch stages, respectively, and select the trigger output signal for the associated time-base unit.

**VERT MODE.** In the VERT MODE position of either the A or B TRIGGER SOURCE switch, the setting of the VERTICAL MODE switch determines the operation of the

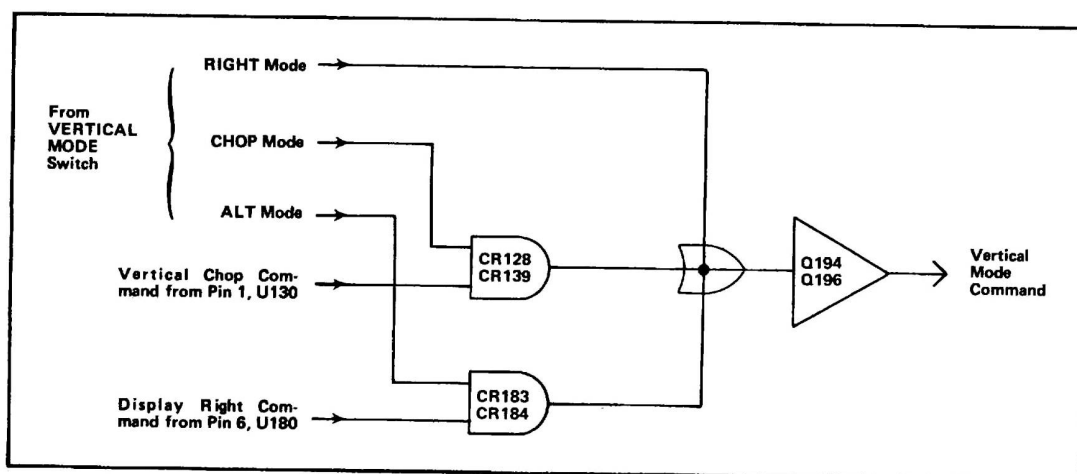


Fig. 3-20. Logic diagram of Vertical Mode Logic stage.

(A)

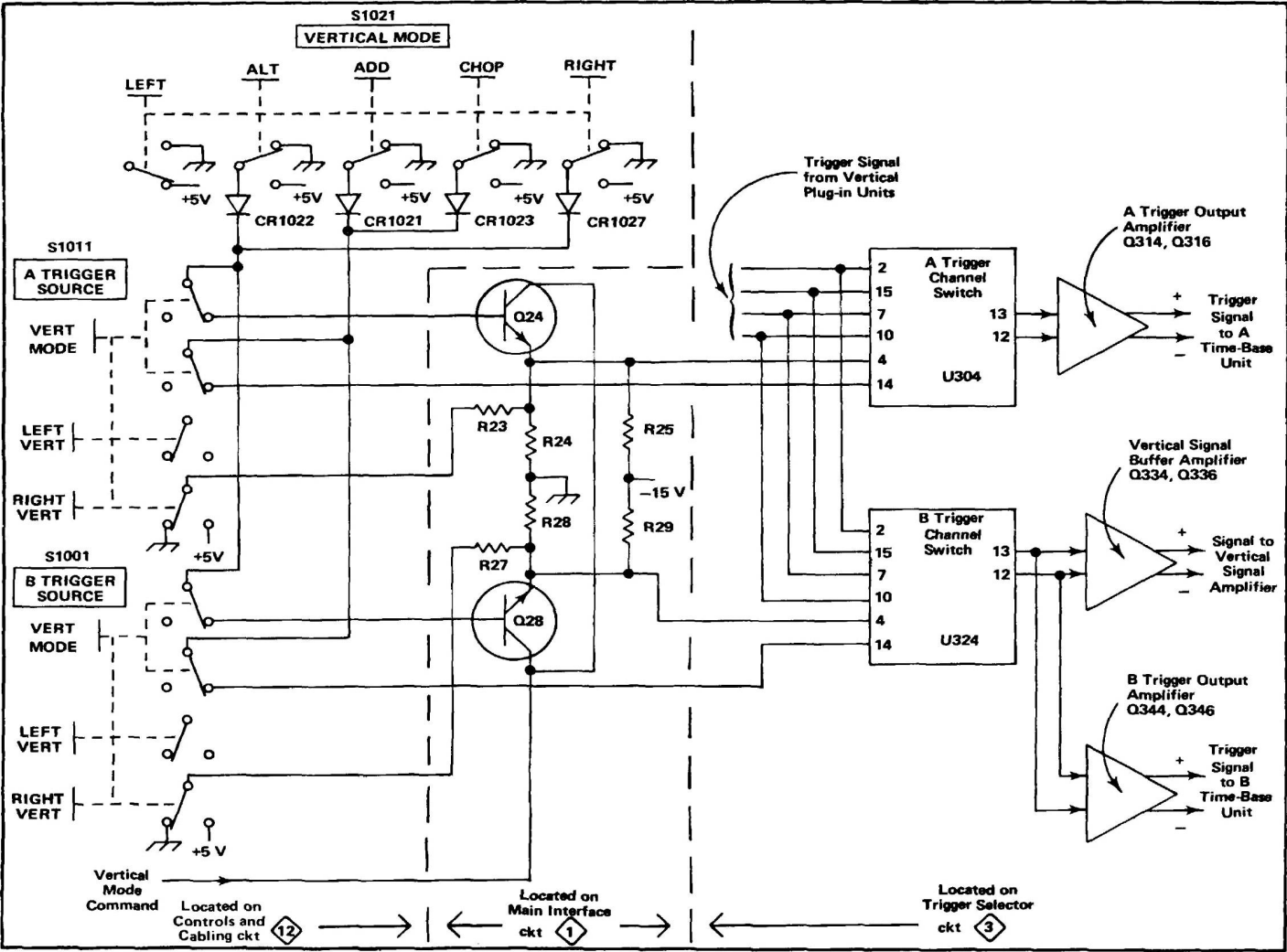


Fig. 3-21. Simplified schematic of trigger selector circuitry.



A and B Trigger Channel Switch stages (A TRIGGER SOURCE, B TRIGGER SOURCE, and VERTICAL MODE switches shown on diagram 12). In the LEFT position of the VERTICAL MODE switch, the base of Q24 or Q28 (see Main Interface schematic) is connected to ground through the ALT and RIGHT sections of S1021, CR1022 and CR1027, and S1001 or S1011. This holds Q24 or Q28 reverse biased to provide a LO level to pin 4 of U304 or U324 (see Fig. 3-22).

When the VERTICAL MODE switch is set to ALT, +5 volts is applied to the base of Q24 or Q28 through CR 1022 and S1001 or S1011. Q24 and Q28 are forward biased and their emitter level is determined by the Vertical Mode Command from the Logic Circuit applied to their collectors. This signal switches between the HI level (Right Vertical unit to be displayed) and the LO level (Left Vertical unit to be displayed) at the end of each sweep. When the Vertical Mode Command is HI, it provides a positive collector voltage to Q24 and Q28. Q24 and Q28 are saturated due to CR 1022, and their emitter levels are very near the collector level. This provides a HI output level to the Trigger Channel Switch stages. As the Vertical Mode Signal goes LO, the collector supply for Q24 and Q28 also goes negative. Q24 and Q28 remain saturated and the output again follows the collector level to supply a LO output level to U304 and U324.

VERTICAL MODE switch positions		A and B TRIGGER SOURCE switch positions	
		VERT MODE	
VERTICAL MODE switch positions	LEFT	LO (Left Vertical)	↑
	ALT	Switches from LO to HI, and vice versa, at end of each sweep (both; follows display)	↑
	ADD	LO at pin 4 of U304 and U324.	LO (Left Vertical)
	CHOP	HI at pin 14 <sup>1</sup> (both; added algebraically)	HI (Right Vertical)
	RIGHT	HI (Right Vertical)	↓

<sup>1</sup> Pin 14 LO for all other conditions.

Fig. 3-22. Input levels at pin 4 of U304 and U324 (source of triggering signal is shown in parenthesis).

For ADD and CHOP vertical mode operation, +5 volts is connected to pin 14 of U304 or U324 through CR1021 or CR1023 and S1001 or S1011. At the same time, the base of Q24 or Q28 is held LO by the ground connection through the ALT and RIGHT sections of S1021 so the level at pin 4 of the Trigger Channel Switch stages is LO also (produces an ADD mode in Trigger Channel Switches; see description of these circuits which follows). In the RIGHT position of the VERTICAL MODE switch, +5 volts is connected to the bases of Q24 or Q28 through CR1027 and S1001 or S1011 to forward bias these transistors. The Vertical Mode Command connected to the collectors of Q24 and Q28 is also HI in this mode and a HI output level is produced at the emitters of Q24 or Q28.

**LEFT VERT.** When the LEFT VERT trigger source is selected, the VERTICAL MODE switch is disconnected from the trigger selector circuitry. Now, the ground connection through the RIGHT VERT section of S1001 or S1011 establishes a LO output level at the emitters of Q24 and Q28.

**RIGHT VERT.** In the RIGHT VERT position of the A or B TRIGGER SOURCE switches, +5 volts is connected to the emitters of Q24 or Q28 through S1011-R23 or S1001-R27. This produces a HI output level to the A and B Trigger Channel Switch stages.

#### A and B Trigger Channel Switch

The A and B Trigger Channel Switch stages determine which input signal provides the trigger signal to the time base units as controlled by the trigger mode and ADD signals from the trigger selection circuitry. Resistors R301-R321 and R302-R322 (refer to diagram 3) establish the input resistance of this stage and provide a load for the trigger output of the Left and Right Vertical plug-in units. Resistors R303-R304-R305 and R307-R308-R309 establish the operating levels for the A Trigger Channel Switch; R303-R305 and R307-R309 set the current gain for each channel. Resistors R323-R324-R325 and R327-R328-R329 establish the operating levels for the B Trigger Channel Switch; R323-R325 and R327-R329 set the current gain for each channel. These stages are made up primarily of integrated circuits U304 and U324. An input/output table for U304 and U324 is shown in Fig. 3-23. U304-U324 provide a high impedance differential input for the trigger signal from the Left Vertical unit at pins 2 and 15 and for the trigger signal from the Right Vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9, and 16 in all modes. This provides a constant DC bias to the stages which follow as the A or B TRIGGER SOURCE switches or the VERTICAL MODE switch are changed.

When the level at pin 4 is LO (see Trigger Mode and ADD Signals discussion and Fig. 3-23), the trigger signal

(A)

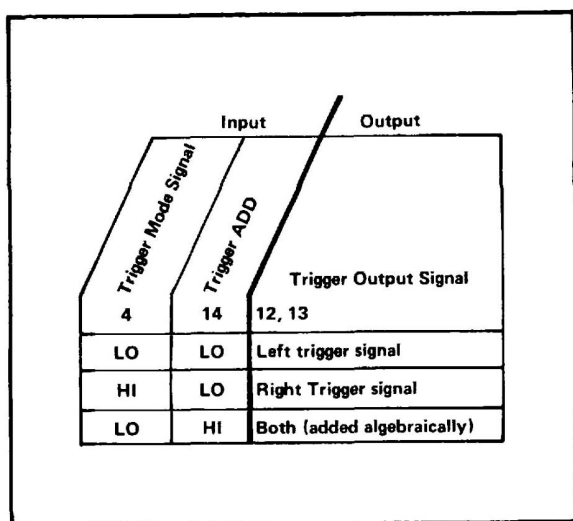


Fig. 3-23. Input/output table for A and B Trigger Channel Switch stages.

from the Left Vertical unit passes to the output while the trigger signal from the Right Vertical unit is blocked. A HI level at pin 4 connects the trigger signal from the Right Vertical unit to the output and the trigger signal from the Left Vertical unit is blocked. For VERT MODE operation in the ALT position of the VERTICAL MODE switch, the level at pin 4 switches between the LO and HI level at a rate determined by the Vertical Binary stage (see Logic Circuit description). This action obtains the trigger signal from the Left Vertical unit when the Left Vertical unit is being displayed and from the Right Vertical unit when it is being displayed.

When the level at pin 4 is LO and the level at pin 14 is HI, the trigger signal from both the Left and Right Vertical units passes to the output pins. This condition occurs only when the A or B TRIGGER SOURCE switches are set to VERT MODE and the VERTICAL MODE switch is set to either ADD or CHOP. Under this operating mode, the trigger output signal is the algebraic sum of the trigger input signals from the Left and Right Vertical units to prevent triggering on the vertical chopping transition or only on one signal of an added display.

### A Trigger Output Amplifier

The trigger output signal at pins 12 and 13 of the A Trigger Channel Switch is connected to the emitters of common-base amplifier Q314-Q316 through R311-R312. These transistors provide a low-resistance load for the A Trigger Channel Switch while providing a high output impedance to the circuits which follow. The signal at the collectors of Q314 and Q316 is connected to the A Horizontal unit via the Main Interface circuit. The A Horizontal unit

provides a 50-ohm differential load for this stage. If it is removed from its compartment, the voltage-swing at the collectors of Q314-Q316 will increase substantially.

### Vertical Signal Buffer Amplifier

The trigger output signal at pins 12 and 13 of the B Trigger Channel Switch is connected to the emitters of common-base amplifier Q334-Q336. The output signal at the collectors of Q334 and Q336 is connected to the Vertical Signal Amplifier (see Output Signals description) through R337 and R338. R339 provides a differential output resistance of about 100 ohms.

### B Trigger Output Amplifier

The signal at pins 12 and 13 of the B Trigger Channel Switch is also connected to the bases of Q344-Q346 to provide the internal trigger signal for the B Horizontal unit (via the Main Interface circuit). This stage provides isolation between the B Horizontal unit and the Vertical Signal Buffer Amplifier stage. The B Horizontal unit provides a 50-ohm differential load for this stage. If it is removed from its compartment, the collector load for Q344-Q346 changes and the voltage swing at their collectors increases. The action of this stage prevents this change from affecting the Vertical Signal Buffer Amplifier stage. CR342-CR346 clamp the collectors of Q344 and Q346 at about +0.6 volts to prevent these transistors from saturating under this no load condition.

## VERTICAL INTERFACE

### General

The Vertical Interface circuit selects the vertical deflection signal from the output of the Left Vertical and/or the Right Vertical plug-in unit. This stage also accepts an input from the Readout System to block the vertical signal while readout information is displayed on the CRT. In addition, this stage contains the Trace Separation Circuit to shift the vertical position of the B-Sweep portion of a dual-sweep display. Fig. 3-24 shows a detailed block diagram of the Vertical Interface circuit. A schematic of this circuit is shown on diagram 4 at the rear of this manual.

### Vertical Switching

Transistors Q202-Q206 and Q212-Q216 form differential amplifiers which determine if the signal from the left vertical plug-in or the right vertical plug-in, or both, provides the vertical deflection signal to the Vertical Amplifier. Transistor Q218 provides a constant voltage source of about -8.7 volts for the collector circuits of Q202-Q206 and Q212-Q216. The operation of this stage is controlled by the Vertical Mode Command, the ADD Mode signal, and the Vertical Channel Switch OFF Command. Fig. 3-25 shows an input/output table for the overall Vertical Interface circuit to show the output signal for the applicable input conditions.



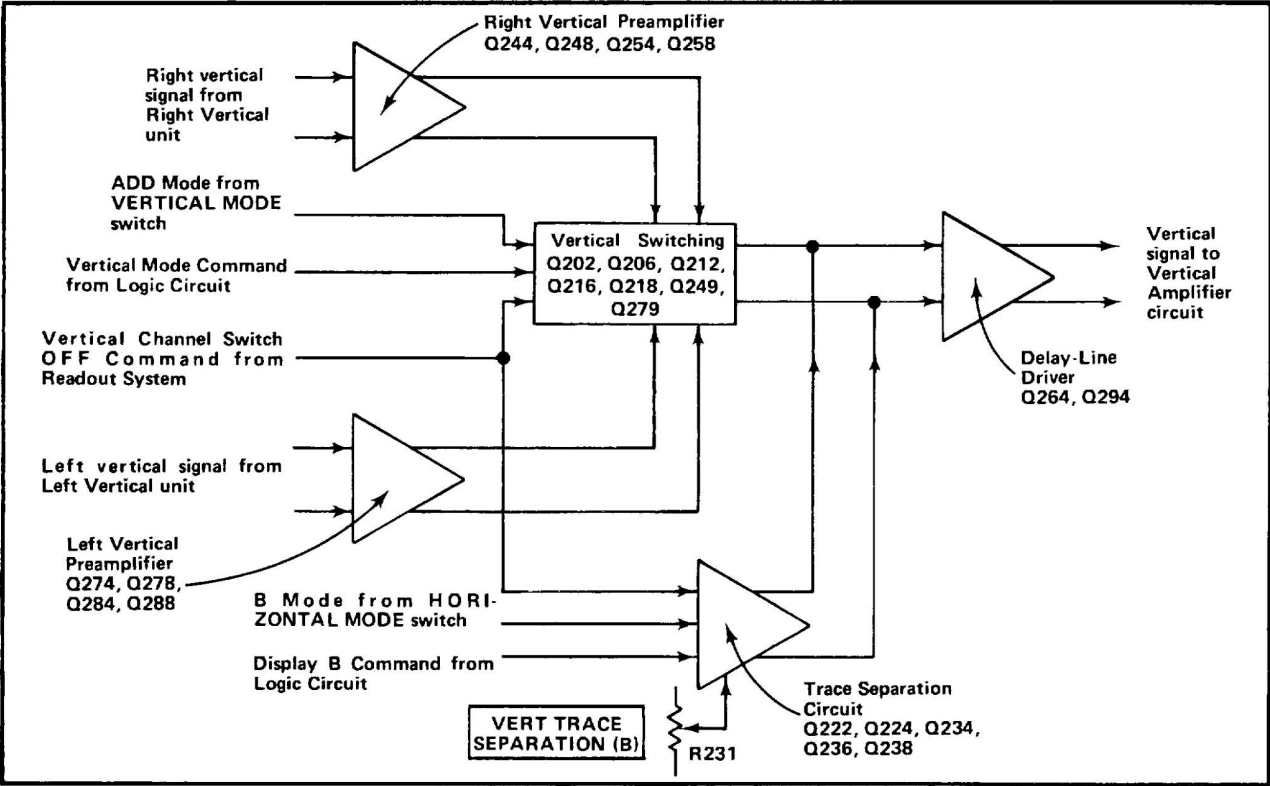


Fig. 3-24. Vertical Interface detailed block diagram.

Input			Output
Vertical Mode Command	ADD Mode (Vert)	Vertical Channel Switch OFF Command	Output signal
LO	LO	LO	Left vertical signal
HI	LO	LO	Right vertical signal
LO	HI	LO	Both (added algebraically)
Φ	Φ	HI	Neither (blocked by Readout System)

Φ = Has no effect in this case

Fig. 3-25. Input/output table for Vertical Interface circuit.

When the VERTICAL MODE switch is set to LEFT, the Vertical Mode Command is LO. This level allows the bases of Q202 and Q212 to go negative so that these transistors are forward biased. The resulting positive-going change at the collectors of Q202 and Q212 produce different results for the Left and Right Vertical Preamplifier stages. The positive-going signal at the collector of Q212 is connected to the bases of the series transistors Q278-0288 in the Left Vertical Preamplifier stage through R212. At the same time, the other transistor in this differential amplifier, Q216, is reverse biased. The negative level at its collector reduces the conduction of Q279 to reverse bias shunt diodes CR279-CR289. As a result, the signal from the Left Vertical plug-in can pass to the Delay-Line Driver stage. The positive-going change at the collector of Q202 forward biases transistor Q249 and shunt diodes CR249-CR259 in the Right Vertical Preamplifier stage. Q206 is reverse biased and the negative level at its collector holds series transistors Q248-Q258 reverse biased to block the signal from the Right Vertical plug-in. Instead, the signal is shunted through CR249-CR259 and Q249 to the junction of R262-R292. This arrangement provides a constant DC current to the Delay-Line Driver stage as the VERTICAL MODE switch is changed by providing a signal current

either through the applicable series transistors or an equivalent DC current through the shunt diodes via R262-R292.

In the RIGHT position of the VERTICAL MODE switch, the Vertical Mode Command is HI. Now, diodes CR200 and CR209 are forward biased and the positive signal at the base of Q202-Q212 reverse biases these transistors. The previous conditions are now reversed. The collector of Q212 is negative so that series transistors Q278-Q288 are reverse biased. At the same time Q216 is forward biased to hold Q279 and the shunt diodes CR279-CR289 forward biased also. This action blocks the signal from the Left Vertical plug-in unit. On the Right Vertical side of the circuit, the negative level at the collector of Q202 reduces the conduction of Q249 to reverse bias shunt diodes CR249-CR259. The positive level at the collector of Q206 forward biases series transistors Q248-Q258 to allow the signal from the Right Vertical plug-in unit to pass to the Delay-Line Driver stage.

For either the ALT or CHOP position of the VERTICAL MODE switch, the Vertical Mode Command switches between the LO and HI levels at a rate determined by either the Chop Counter or the Vertical Binary stages (see Logic Circuit description). This action allows the signal from the Left Vertical unit to be displayed when the Vertical Mode Command is LO and the signal from the Right Vertical unit is displayed when the Vertical Mode Command is HI.

When ADD vertical mode operation is selected, a HI Vertical Mode Command level is applied to the base of Q202 through R200. The level at the collector of Q202 goes negative to reverse bias the Right Vertical shunt diodes and the positive level at the collector of Q206 forward biases the series transistors to allow the Right Vertical signal to pass to the Delay-Line Driver stage. At the same time, the Vertical Mode Command level is LO as determined by the Vertical Mode Control stage in the Logic Circuit. This allows Q212 to conduct to forward bias the Left Vertical series transistors; the shunt diodes are reverse biased by the negative level at the collector of Q216. Therefore, the signal from the Left Vertical plug-in unit can pass to the Delay-Line Driver stage. Now, the signal from both vertical units is algebraically added by the Delay-Line Driver stage and the resultant signal determines the vertical deflection.

The Vertical Channel Switch OFF Command from the Readout System has final control over the output signal from this stage. Quiescently, this signal is LO and the signal from the selected vertical unit can pass to the Delay-Line Driver stage. However, when the Readout System is ready to display readout information, the Vertical Channel Switch OFF Command goes HI. Transistor Q212 is reverse biased through CR210 and Q206 is reverse biased through R208. This reverse biases the series transistors Q248-Q258

#### **Circuit Description-R7704**

and Q278-Q288 to block the signal from both vertical units. At the same time the remaining transistor in each differential amplifier is forward biased to shunt the vertical signal. Therefore, the signal from neither plug-in unit is displayed on the CRT so the CRT deflection can be determined by the Readout System.

#### **Left Vertical Preamplifier**

The vertical signal from the Left Vertical plug-in unit is connected to the Left Vertical Preamplifier stage by way of the strip lines on the Vertical Interconnect board. These strip lines provide an impedance of 50 ohms. The applied signal is amplified by transistors Q274-Q284. C274-C282-R274-R284 in the emitter circuit of Q274-Q284 provide high-frequency compensation; C274-R274 are variable to provide high-frequency response adjustment for this stage. The Left Vertical Centering adjustment R277 balances the quiescent DC levels at the output of the Left Vertical Preamplifier stage so the trace from the Left Vertical unit is displayed at the center of the CRT when the inputs to this stage are at the same potential. Transistors Q278-Q288 operate along with the Vertical Switching stage to determine if the Left Vertical signal is displayed on the CRT.

#### **Right Vertical Preamplifier**

The components in the Right Vertical Preamplifier stage serve the same function as the corresponding components in the Left Vertical Preamplifier stage. The only difference between the two circuits is the presence of the Right Vertical Gain adjustment, R242, in this circuit. The overall gain of the Vertical Amplifier circuit is set when the Left Vertical signal is displayed. The Right Vertical Gain adjustment compensates for any differences in gain between the Right Vertical Preamplifier stage and the Left Vertical Preamplifier stage. Gain is controlled by changing the emitter degeneration between transistors Q244-Q254.

#### **Trace Separation Circuit**

The Trace Separation Circuit provides a variable positioning voltage to offset the B Sweep display when operated in either the ALT or CHOP dual-sweep modes (horizontal). The display B Command from the Logic Circuit controls the operation of this stage through Q234. When the B Sweep is being displayed (for ALT or CHOP horizontal operation), the Display B Command is HI to forward bias Q234. The collector of Q234 goes negative to reverse bias shunt diodes CR233-CR234. Under this condition, the VERT TRACE SEPARATION (B) control determines the bias at the base of transistors Q236-Q238 through R230-R232 and the series diodes CR230-CR232. The output current at the collectors of Q236-Q238 is connected to the Delay-Line Driver stage through R261-R291 to offset the B Sweep display up to about four divisions above or below the A Sweep display. This prevents a confusing

display when using dual-sweep operation, as the A and B Sweeps would be displayed on top of each other without this feature.

When the Display B Command is LO (A Sweep displayed), Q234 is reverse biased and the shunt diodes CR233-CR234 are forward biased through R233. This applies a DC bias of about +5.1 volts to the bases of transistors Q236-Q238 to provide a quiescent DC output current from this stage to the Delay-Line Driver stage. Since the series diodes CR230-CR232 are reverse biased, the VERT TRACE SEPARATION (B) control is disconnected while the A Sweep is being displayed.

Two other signals also control the current through this stage. When the HORIZONTAL MODE switch is set to B (only), a HI level is connected to the base of Q224 through CR224 and R224. This forward biases Q224 and, since Q224-Q234 share emitter resistor R227, transistor Q234 is reverse biased even though the Display B Command at its base is HI for this mode. Therefore, the VERT TRACE SEPARATION (B) control has no effect. The Vertical Channel Switch OFF Command from the Readout System is connected to the base of Q222 through R221. This signal is quiescently LO so that Q222 is conducting through R222 to hold Q224 reverse biased by way of R223 (except when HORIZONTAL MODE switch is in B position described above). When the Readout System is ready to display readout information, the Vertical Channel Switch OFF Command goes HI to reverse bias Q222. The base of Q224 goes positive through R222-R223 and it is forward biased. Now, Q224 controls conduction and Q234 is off to disconnect the VERT TRACE SEPARATION (B) control. The output of this stage goes to its quiescent DC level so that the

## Circuit Description-R7704

Readout System has full control of the trace position (see Readout System description for more information).

### Delay-Line Driver

Output of the Left Vertical Preamplifier and the Right Vertical Preamplifier stages, along with any positioning current from the Trace Separation Circuit is connected to the bases of Q264-Q294. This stage provides amplification for the selected signal as well as providing a reverse termination for the delay line. Diodes CR264-CR295 decrease the feedback resistance for Q264-Q294 as the signal is deflected towards the edges of the display area. This action reduces the gain of the stage to compensate for the inherent expansion characteristic of the CRT. The output signal from the Delay-Line Driver stage is connected to the Vertical Amplifier circuit through C266-R266 and C296-R296.

### VERTICAL AMPLIFIER

#### General

The Vertical Amplifier circuit provides the final amplification for the vertical signal before it is applied to the vertical deflection plates of the CRT. This circuit includes the delay line and an input to produce the vertical portion of a readout display. The BEAM FINDER switch limits the dynamic range of this circuit to compress an over-scanned display within the viewing area of the CRT. Fig. 3-26 shows a detailed block diagram of the Vertical Amplifier circuit. A schematic of this circuit is shown on diagram 5 at the rear of this manual.

#### Delay Line

Delay Line DL400 provides approximately 120 nanoseconds delay for the vertical signal to allow the horizontal

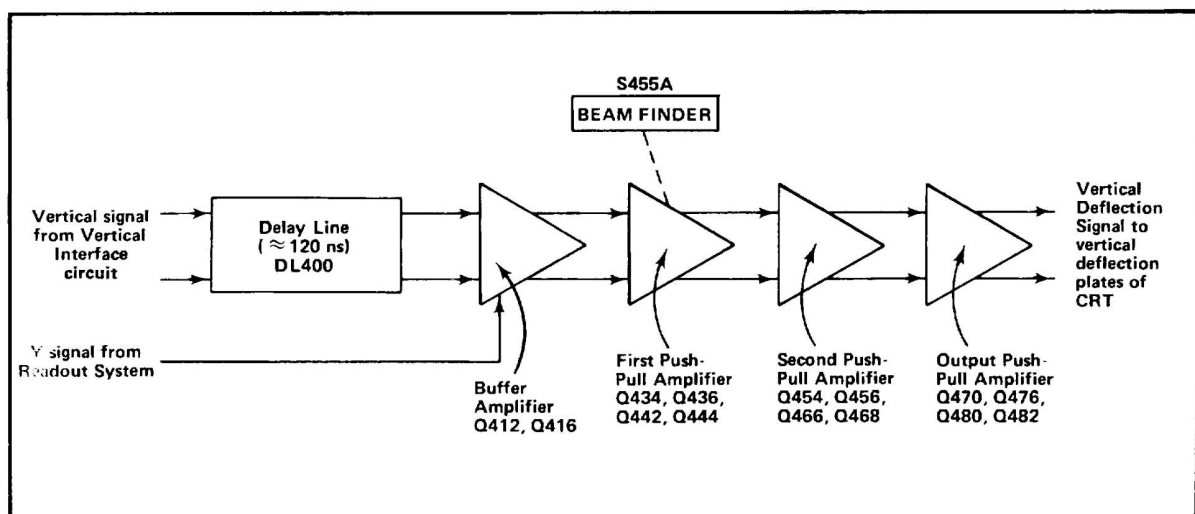


Fig. 3-26. Vertical Amplifier detailed block diagram.

circuits time to initiate a sweep before the vertical signal reaches the vertical deflection plates of the CRT. This allows the instrument to display the leading edge of the signal originating the trigger pulse when using internal triggering. The delay line used in this instrument has a characteristic impedance of about 50 ohms per side, or about 100 ohms differentially. It is of the coaxial type which does not produce preshoot or phase distortion in the CRT display.

#### **Buffer Amplifier**

The Buffer Amplifier stage Q412-Q416 provides a low input impedance for the Vertical Amplifier circuit to permit accurate delay-line termination. C401-R401 and C408-R408 provide the forward termination for the delay line. The output signal from the Buffer Amplifier stage is connected to the First Push-Pull Amplifier stage through C411-R411-VR411 and C417-R417-VR417. Zener diodes VR411 and VR417 limit the voltage swing across R411 and R417 to keep Q412 and Q416 out of saturation. R405 and the operating bias of Q412-Q416 provide compensation for thermal distortion produced in Q470-Q476.

For readout displays, the Y-signal from the Readout System is connected to the emitter of Q412 through R402. Since the signal from the vertical units is blocked in the Vertical Interface circuit, the readout signal provides the only vertical deflection. Although this signal is connected to the emitter of Q412 as a single-ended signal, it is converted to a push-pull signal in the following stages.

#### **First Push-Pull Amplifier**

Q434-Q442 and Q436-Q444 are connected as a pushpull cascode amplifier stage. The network C426-L421L422-L423-R420-R421-R422-R423-R424-R425-R426 provides compensation for the delay line. R421-R422-R423 in this network are adjustable to provide mid-frequency compensation. C430-R430, connected between the emitters of Q434-Q436, provide high-frequency compensation adjustment for this stage. The network CR431-CR432-RT433 provides thermal compensation for this stage. As the temperature increases, the resistance of RT433 decreases and the capacitance of varactors CR431-CR432 increases. The output signals at the collectors of Q434-Q436 are connected to the common-base transistors Q442-Q444 through C435-R435-R436 and C438-R437-R438. The low input resistance of the Q442-Q444 common-base transistors allows this stage to provide maximum high-frequency performance. The Vertical Centering adjustment R443 balances the quiescent DC levels in the Vertical Amplifier circuit so the trace is displayed at the center of the CRT when the inputs to this circuit are at the same potential. The output signal from the First Push-Pull Amplifier stage is connected to the next stage through C447-L447 and C448-L448. Zener diode VR449 establishes a collector source voltage of about -6.2 volts for Q442-Q444.

#### **Second Push-Pull Amplifier**

The Second Push-Pull Amplifier, Q454-Q466 and Q456-Q468, operates in the same manner as the previous stage. The main difference between the stages is the compensation networks and the BEAM FINDER switch located in this circuit. C458-R458 in the emitter circuit of Q454-Q456 provide adjustable high-frequency compensation for this stage.

BEAM FINDER switch S455A switches the emitter current source for Q454-Q456 to provide the beam finder function. Normally, the emitter current for Q454-Q456 is supplied through S455A-L452. However, when S455A is pressed in, the current source through L452 is interrupted and the only emitter-current source for Q454-Q456 is through R451. This limits the dynamic range of this stage by limiting its current, so the display is compressed vertically within the graticule area. The BEAM FINDER switch can also be pulled out to lock it in the "find" position to aid in locating the traces of several plug-in units.

The signal at the collectors of Q454-Q456 is connected to common-base transistors Q466-Q468 through C460-R460-R461-R462 and C465-R463-R464-R465. Transformer T466 reduces the common-mode signal components in the push-pull signal applied to the following stages. The output signal from this stage at the collectors of Q466-Q468 is connected to the Output Push-Pull Amplifier through VR467-VR469 and LC networks C470-L470 and C471-L471. VR467-VR469 provide DC voltage matching without appreciable current loss. Vertical Gain adjustment R468 sets the resistance between the bases of Q470-Q476 in the following stage to control the current gain of this stage. This adjustment sets the overall gain of the Vertical Amplifier stage.

#### **Output Push-Pull Amplifier**

Q470-Q480 and Q476-Q482 operate in the same manner as the previous stages to provide amplification for the vertical deflection signal. The output signal from this stage provides the vertical deflection on the CRT. C472 and thermistor RT472 provide frequency compensation to maintain high-frequency response with temperature changes. Thermistor RT480 and R480 provide gain compensation with changes in temperature. The output signal is connected to the vertical deflection plates of the CRT through buffer transistors Q480-Q482. A distributed deflection plate system is used in this instrument for maximum frequency response and sensitivity. The output signal at the collectors of Q480-Q482 is connected to the integral inductors in the CRT and then to the deflection-plate termination network C483-L481-L483-R483-R485 and C484-L482-L484-R484-R487. As the signal passes through the integral inductors in the CRT, its velocity is essentially the same as the velocity of the electron beam passing between the vertical deflection plates. The synchronism of the deflection signal and the

electron beam reduces the loss in high-frequency sensitivity due to electron transit time through the deflection plates. Inductors L483-L484 and capacitors C483-C484 are adjusted to minimize signal reflections by providing the correct termination for the vertical deflection plate structure.

## HORIZONTAL INTERFACE

### General

The Horizontal Interface circuit is made up of the X-Y Delay Compensation Network and the Horizontal Channel Switch stage. The X-Y Delay Compensation Network (optional) provides a delay for the horizontal (X) portion of an X-Y display to match the delay of the vertical (Y) signal due to the Delay Line. The Horizontal Channel Switch portion of the circuit selects the horizontal deflection signal from the output of the A Horizontal and/or the B Horizontal plug-in unit. Fig. 3-27 shows a detailed block diagram of this circuit. A schematic of this circuit is shown on diagram 6 at the rear of this manual.

### X-Y Delay Compensation

**Time-Base Operation.** When the plug-in unit installed in the A or B horizontal compartment is operated as a standard time-base unit to produce a horizontal sweep for deflection of the CRT beam, the A

or B Delay Compensation Networks are effectively disabled. The X Compensation Inhibit command is HI and relays K50-K60 or K70-K80 are not actuated. Therefore, the relay contacts remain in the normally closed position so the horizontal signal passes directly through this network to the Horizontal Channel Switch without delay.

**X-Y Operation.** If the time-base unit installed in the A or B horizontal compartment is operated as an amplifier or if a vertical unit is installed in a horizontal compartment, the X-Compensation Inhibit command to the applicable Delay Compensation Network drops to the LO level (zero volts). This provides an actuating level to relays K50-K60 or K70-K80 to connect the Delay Compensation Network into the circuit. For example, if the X-Compensation Inhibit command from the A Horizontal Unit goes LO, K50 and K60 close to route the A Horizontal Signal through the A Delay Compensation Network. Diodes CR50 and CR70 shunt the voltage produced across the relays when the actuating level is removed. LR networks L51-R51 and L61-R61 along with capacitors C53 and C55 provide a constant input impedance. The LC network made up of C56-C58-C66-C68-L55-L56-L65-L66 provides a fixed delay from DC to about two megahertz to provide minimum phase shift between the X and Y portions of the CRT

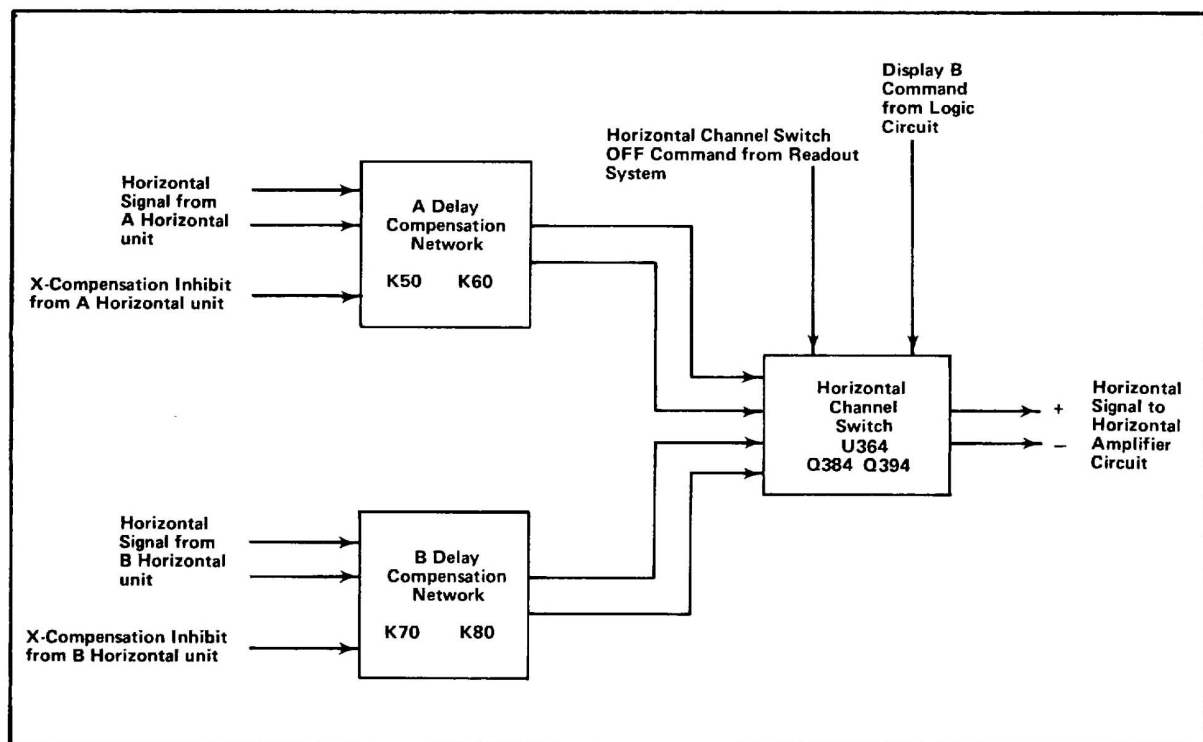


Fig. 3-27. Horizontal Interface detailed block diagram.



display. C55 is adjusted to match the horizontal and vertical signal delay up to at least two megahertz.

The Delay Compensation Network normally produces negative preshoot distortion along with some corner rounding of fast step functions. The A Delay Disable switch S50 allows selection of a display with either minimum phase-shift characteristics or optimum step response. When this switch is set to Out (down), the X Compensation Inhibit command from the A Horizontal Unit is disconnected from relays K50-K60. Now, the signal from the A Horizontal Unit passes directly to the Horizontal Channel Switch without delay to provide a horizontal display with optimum step response.

The B Delay Compensation Network operates in the same manner as described above. The X-Y Delay Compensation Network is an optional feature. For instruments which are not equipped with this feature, the horizontal signals from the plug-in units are connected directly to the Horizontal Channel Switch stage by the Horizontal Interconnect board.

Horizontal Channel Switch

The Horizontal Channel Switch determines which input signal provides the horizontal signal to the Horizontal Amplifier circuit as controlled by the Display B Command from the Logic Circuit. Resistors R352-R354 and R356-R358 establish the input resistance of this stage and provide a load for the A and B Horizontal units. Resistors R363-R365-R367 and R373-R375-R377 establish the operating levels for this stage. R363-R365 and R373-R375 set the current gain for each channel. C361-R361 and C371-R371 provide frequency compensation.

This stage is made up primarily of integrated circuit U364 which is the same type as used for the Trigger Channel Switch stage. An input/output table for U364 is shown in Fig. 3-28. U364 provides a high-impedance differential input for the signal from the A Horizontal unit at pins 2 and 15 and the signal from the B Horizontal unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal which is connected to the Horizontal Amplifier circuit. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9, and 16 in all modes. This provides a constant DC output current level to the following stage as the HORIZONTAL MODE switch is changed.

When the HORIZONTAL MODE switch is set to A, the level at pin 4 is LO. This level allows the signal from the A Horizontal unit to pass to the output while the signal from the B Horizontal unit is blocked. In the B position of the HORIZONTAL MODE switch, the level at pin 4 is HI. Now, the signal from the B Horizontal unit is connected to the output while the signal from the A Horizontal unit is blocked.

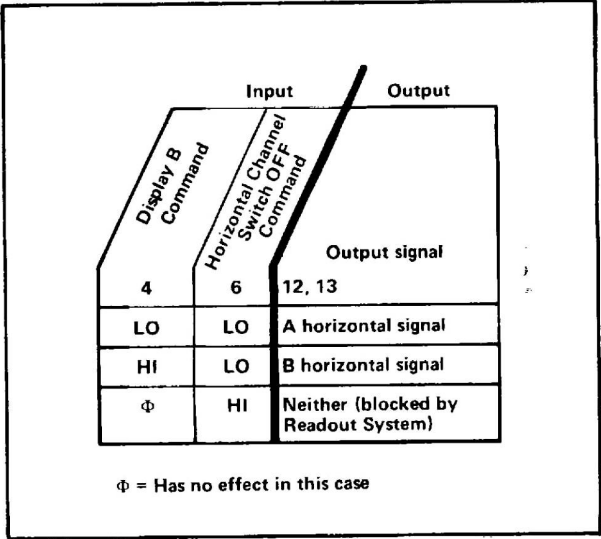


Fig. 3-28. Input/output table for Horizontal Channel Switch.

For ALT or CHOP positions of the HORIZONTAL MODE switch, the Display B Command at pin 4 switches between the LO and HI levels at a rate determined by the Horizontal Binary stage in the Logic Circuit. This action allows the signals from the A Horizontal unit to be displayed when the Display B Command is LO and the signal from the B Horizontal Unit is displayed when the Display B Command is HI.

The Horizontal Channel Switch OFF Command from the Readout System which is applied to pin 6 has final control over the output signal from this stage. Quiescently, this signal is LO and the signal from the selected horizontal unit can pass to output pins 12 and 13. However, when the Readout System is ready to display readout information, the level at pin 6 goes HI. This level blocks the signal from both horizontal units so there is no signal output from this stage under this condition.

The output signal at pins 12 and 13 is connected to the Horizontal Amplifier circuit through Q384-Q394. Resistors R381-R383 and R391-R393 establish the correct operating DC levels for U364. Buffer amplifier Q384-Q394 provides a low load impedance for U364 as well as providing DC voltage matching between the Horizontal Interface and Horizontal Amplifier circuits.

HORIZONTAL AMPLIFIER

General The Horizontal Amplifier circuit amplifies the push-pull horizontal deflection signal from the Horizontal Interface circuit and connects it to the horizontal deflection plates of

the CRT. This circuit also accepts the X-signal from the Readout System to produce the horizontal portion of a readout display. Fig. 3-29 shows a detailed block diagram of the Horizontal Amplifier circuit. A schematic of this circuit is shown on diagram 7 at the rear of this manual.

### Input Amplifier

The horizontal signal from the Horizontal Interface circuit is connected to the bases of Q526 and Q536. The Input Amplifier is driven from an equivalent 100-ohm source. The resistive network R521-R522-R524-R531-R532-R533-RT534 between the emitters of Q526-Q536 controls the emitter degeneration of this stage to perform several functions. Horizontal Gain adjustment R522 is variable to determine the amount of emitter degeneration between Q526-Q536 to set the overall gain of the Horizontal Amplifier circuit. Thermistor RT534 provides thermal gain compensation for this circuit. As the temperature increases, the resistance of RT534 decreases resulting in less emitter degeneration between Q526-Q536. Therefore, the overall gain of this stage increases to compensate for the opposite characteristic of the transistors in the Horizontal Amplifier circuit.

Transistor Q514 is normally supplying current to the emitters of Q526-Q536 through R521-R531. However,

### Circuit Description-R7704

when the BEAM FINDER switch is actuated, Q514 is no longer forward biased so the current supplied to R521-R531 is determined only by R515. This results in less current to Q526-Q536 so their dynamic range is limited. When the BEAM FINDER switch S455B is actuated, a ground level is also connected to the Logic Circuit to provide an intensity limit. This action prevents damage to the CRT phosphor when the display is compressed.

The Horizontal Centering adjustment R529 provides adjustment for differential unbalance in the Horizontal Amplifier circuit and the CRT. The network CR528-CR538-CR544-CR554 limits the input to the next stages so they always operate within their dynamic range and are not overdriven by excessive current from the Input Amplifier stage. Since the output signal from the Input Amplifier stage is a current signal, very little voltage change occurs across the limiting network. With horizontal deflection signals which produce an on-screen display, CR544 and CR554 remain forward biased and CR528-CR538 are reverse biased. However, if high-amplitude horizontal deflection signals are applied to this circuit as a result of sweep magnification or high-amplitude external horizontal signals, either CR544 or CR554 is reverse biased, depending on the polarity of the overdrive signal. This results in a sufficient voltage change at the anode of either CR528 or CR538 to forward bias it. The shunt diodes provide a current path for

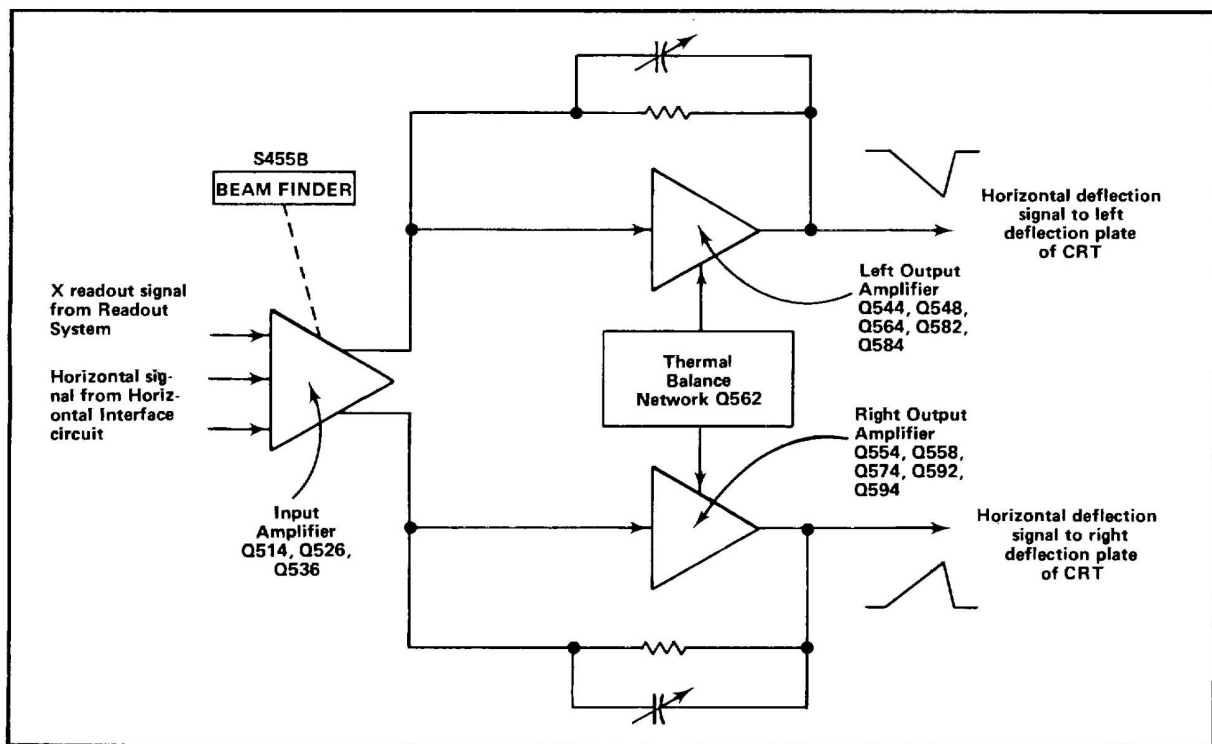


Fig. 3-29. Horizontal Amplifier detailed block diagram.

the signal current to limit the current change at the bases of Q544-Q554 during the overdrive condition.

For readout displays, the X readout signal from the Readout System is connected to the base of Q526 through R525. The signal from the A HORIZ and B HORIZ plug-in units is blocked in the Horizontal Interface circuit so the only horizontal deflection is provided by the Readout System. Q526 and Q536 operate as a paraphase amplifier to convert the single-ended readout signal at the base of Q526 to a push-pull signal at the collectors of both Q526 and Q536. For instruments which are not equipped with a Readout System, R525 is connected to ground at the Readout System chassis.

#### **Left Output Amplifier**

Transistors Q544, Q548, Q564, Q584, and Q582 are connected as a current-driven feedback amplifier. The input current is converted to a voltage output signal to drive the left horizontal deflection plate of the CRT. Input transistor Q544, an NPN transistor, responds best to positive-going input signals. The signal at the collector of Q544 is connected to the emitters of output transistors Q582-Q584 through two parallel paths. High-frequency signals are connected through capacitor C544. Low-frequency signals are connected to the output transistors through R544-Q548-R549. The output transistors Q582 and Q584 are connected in the complementary configuration to provide less resistive loading at the output. The output signal at the collector of Q582-Q584 is connected to the left deflection plate of the CRT through L589-R589.

Negative feedback is provided from the collectors of Q582-Q584 to the base of Q544 through feedback network C569-R569-Q564-C563-R563. Emitter follower Q564 in the feedback network provides current gain for the feedback signal. With this configuration, the input impedance of the Left Output Amplifier is low since the feedback network beyond the emitter followers is effectively reduced in impedance as far as the input signal is concerned. Variable capacitor C569 adjusts the transient response of the feedback network to provide good linearity at fast sweep rates. C568-R568 provide adjustment for correct high-frequency gain versus frequency response in the amplifier.

#### **Right Output Amplifier**

Basic operation of the Right Output Amplifier stage is the same as just described for the Left Output Amplifier stage. Notice that the input transistor in this stage is complementary to the corresponding transistor in the Left Output Amplifier stage. Therefore, this stage provides the best response to negative-going input signals. C579 provides linearity adjustment for the Right Output Amplifier at fast sweep rates. The output signal at the collectors of Q592-Q594 is connected to the right deflection plate of the CRT through L599-R599.

#### **Thermal Balance Network**

Q562 provides thermal balance for the Horizontal Amplifier circuit. The Thermal Balance adjustment R571 sets the bias on Q562 and thereby determines the operating voltage for Q544-Q554. This adjustment provides DC shift in the CRT display and reduces low-frequency signal cross talk. Diode CR562 provides reverse-voltage breakdown protection for Q562 when the instrument is first turned on. Diodes CR560 and CR570 establish the operating bias for Q544-Q554.

### **OUTPUT SIGNALS**

#### **General**

The Output Signals circuit provides output voltages to the front-panel Calibrator jacks and output signals to the connectors located on the rear panel. These output signals are either generated within this instrument or are samples of signals from the associated plug-in units. Fig. 3-30 shows a detailed block diagram of the Output Signals circuit. A schematic of this circuit is shown on diagram 8 at the rear of this manual.

#### **Vertical Signal Amplifier**

The vertical signal selected by the B Trigger Channel Switch (see Trigger Selector description for more information) is connected to the bases of differential amplifier Q684-Q694. Resistors R681-R692 establish an input resistance of about 50 ohms for this stage. The amplified signal at the collectors of Q684 and Q694 is connected to buffer amplifier Q686-Q696 through RC networks C686-R686 and C695-R695. These networks provide thermal balance for this stage. The single-ended signal at the collector of Q686 is connected to the rear-panel SIG OUT connector J699. The signal at the collector of Q696 is connected to ground. CR696 and CR699 protect this stage if high-level voltages are accidentally applied to the SIG OUT connector. CR696 provides protection from positive voltages and CR699 provides protection from negative voltages.

#### **Sawtooth Amplifier**

The sawtooth signals from the A Time-Base unit and the B Time-Base unit are connected to the Sawtooth Amplifier stage through series resistors R4 and R5 respectively (on Main Interface board). The SWEEP switch S666 (on top panel) determines which sawtooth signal provides the output signal. The other sawtooth signal is terminated by R667 to provide a similar load to the signal source. Transistors Q670, Q672, and Q675 comprise an inverting feedback amplifier. Gain of this stage is about two as determined by the ratio of feedback resistor R678 to the input resistance made up of R669 and either R4 or R5, depending on which sawtooth source is selected. The signal at the collector of Q675 is connected to the rear-panel +SAWTOOTH connector J679 through R679. RC network C675-R675 provides



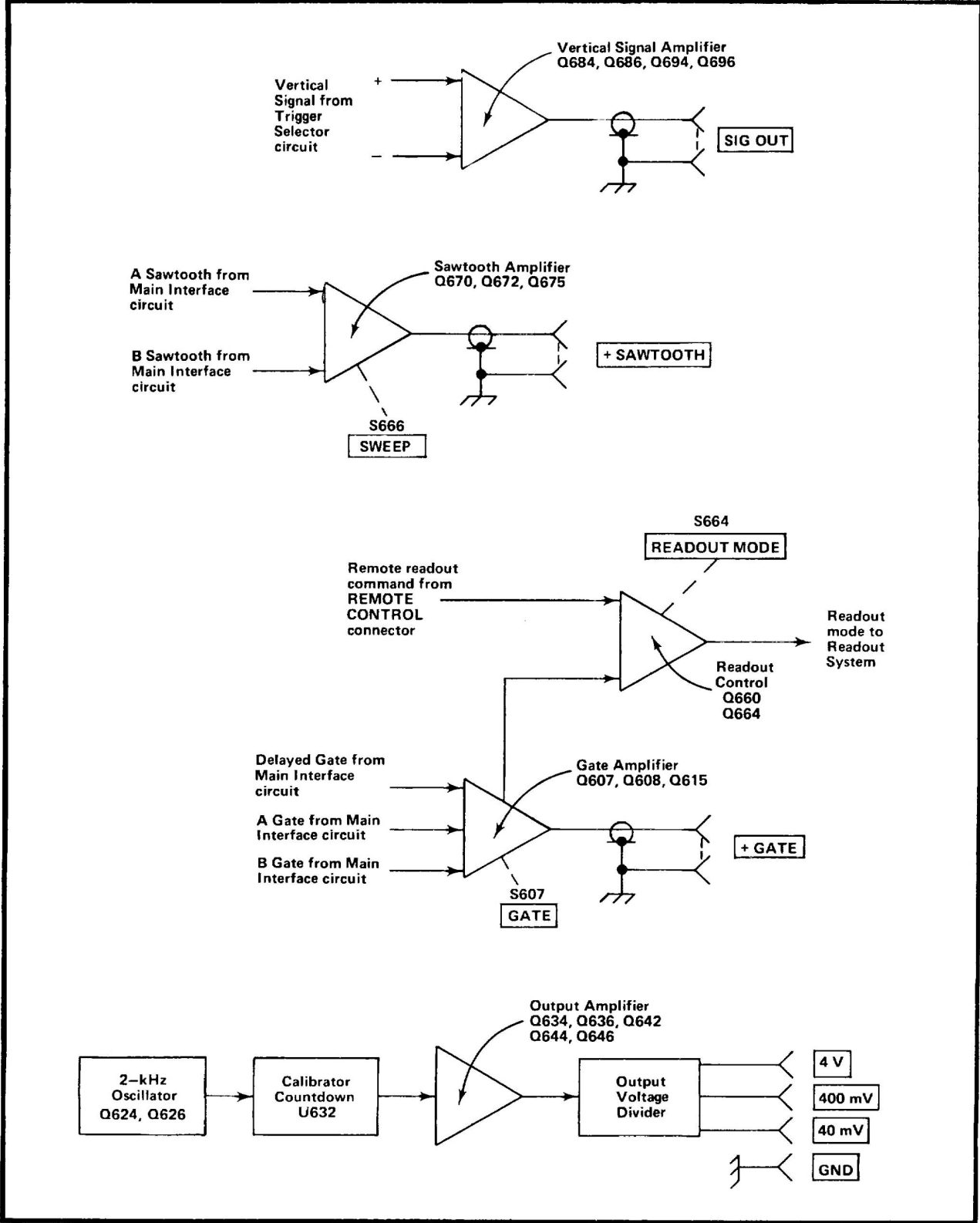


Fig. 3-30. Output Signals detailed block diagram.

(A)

frequency response stabilization for this stage. Diode CR674 provides protection from high-level positive voltages inadvertently connected to the output connector by providing a current path to the +15-volt supply through the collector-base junction of Q675. When CR674 is forward biased it clamps the base of Q675 at this level. CR676 provides protection from high-level negative voltages at the +SAWTOOTH connector by clamping the output if it attempts to go more negative than about -15.6 volts.

#### Gate Amplifier

The output signal at the rear-panel +GATE connector J618 is selected from three input gate signals by GATE switch S607 (on top panel). In the A position, the A Gate signal from the A Time-Base unit is connected to the base of emitter-follower Q607 through R607. The base of Q608 is connected to ground by S607 in this position so it operates as a common-base stage. Q607 provides a high input impedance for the stage while the emitter coupling between Q607-Q608 provides temperature compensation. Operation is the same in the B position of S607 except that the B Gate signal from the B Time-Base unit provides the input signal. In the DLY'D position, S607 connects the base of Q607 to ground through R607 and disconnects both the A and B Gate signals. Now, the Delayed Gate signal from the delaying time base (in A HORIZ compartment) can pass to the base of Q608 through R602. Q608 inverts this negative going input signal so the gate output signals at the +GATE connector are all positive going.

The input gate signal selected by S607 is connected to the emitter of Q615 through C612-R612. Diode CR614 provides temperature compensation for Q615. The signal at the collector of Q615 is connected to the +GATE connector through CR615 and R617. CR615 protects Q615 if a high-level positive voltage is applied to the +GATE connector and CR616 clamps the output at about -0.6 volt if a negative signal is applied to this connector.

#### Readout Control

Q660 and Q664 along with S664 control the operating mode of the Readout System. When READOUT MODE switch S664 is in the FREE RUN-REMOTE position, the Readout System runs continuously in a free-running manner. The emitter of Q664 has no ground return, so Q664 can not conduct and its collector rises positive (through circuitry in the Readout System) to enable the Readout System. However, in this position, the readout mode can be controlled remotely through rear-panel REMOTE CONTROL connector J1075. If a remote readout lockout command (ground level) is connected to pin E of J1075, a ground return is provided for the emitter circuit of Q664 through the shield of the interconnecting cable. The positive voltage connected to the base of Q664 through R663-R664 results in a LO level at the collector of

#### Circuit Description-R7704

Q664. This LO level disables the Readout System (see Readout System for complete details). Now, the operation of the Readout System can be controlled remotely through pin F of J1075. If pin F is connected to ground, a negative-going pulse is connected to the base of Q664 through C661. The collector of Q664 momentarily rises positive to enable the Readout System so it can present one complete frame (eight words).

In the GATE TRIG'D position, the emitter of Q664 is connected to ground through R666 and S664. The base of Q664 is pulled positive through R663-R664 to produce a LO lockout level to the Readout System. The gate signal selected by GATE switch S607 is connected to the Readout Control stage from the emitter of Q615. At the end of the selected gate, a negative level is applied to the base of emitter-follower Q660. This negative level is differentiated by C660-R660, and the resultant negative-going pulse reverse biases Q664 to allow its collector to go HI momentarily. This enables the Readout System so it can produce one complete frame (eight words) each time the selected gate goes negative.

#### Calibrator

**General.** The Calibrator circuit provides accurate voltage output at the front-panel calibrator pin-jacks. Repetition rate of the output signal is one kilohertz. 2-kHz Oscillator. Q624 and Q626 are connected as a two-kilohertz square-wave oscillator to provide the drive signal for the Calibrator Countdown stage. Oscillation occurs as follows: Assume that Q624 is conducting and Q626 is off. The collector current of Q624 through R624-R625 produces a voltage level which holds the base of Q626 low. This keeps Q626 turned off, and since there is no current through it, its collector goes positive to produce the positive portion of the square wave. At the same time, C621 begins to charge toward -50 volts through R627. The emitter of Q626 goes negative also as C621 charges, until it reaches a level about 0.6 volt more negative than the level at its base. Then, Q626 is forward biased and its emitter rapidly rises positive. Since C621 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q626 pulls the emitter of Q624 positive also, to reverse bias it. The current through Q626 produces a voltage drop at its collector to produce the negative portion of the square wave.

Now, conditions are reversed. Since Q624 is reverse biased, there is no current through it. Therefore, C621 can begin to discharge through R621. The emitter level of Q624 follows the discharge of C621 until it reaches about -0.6 volt. Then, Q624 is forward biased and its collector drops negative to reverse bias Q626. This interrupts the current through Q626 and its collector goes positive again to complete the square wave. Once again, C621 begins to charge through R627 to start the second cycle. The signal

produced at the collector of Q626 is a two-kilohertz square wave. C628 differentiates this signal to produce positive and negative-going output pulses, coincident with the rise and fall of the square wave, which provides negative-going trigger pulses for the Calibrator Countdown stage (positive going pulses have no effect on circuit operation). The 1 kHz adjustment, R625, sets this stage so an accurate one kilohertz square-wave is produced at the output of the Calibrator circuit.

**Calibrator Countdown.** Integrated circuit U632 is a triggered set-clear (J-K) flip-flop. An input/output table for this device is shown in Fig. 3-31. U632 is connected so it only operates in one mode; the output changes state with each trigger. The two-kilohertz signal from the 2-kHz Oscillator stage is connected to the trigger input of U632. This results in a one-kilohertz square-wave output signal at pin 7.

**Output Amplifier.** Transistors Q642 and Q644 are connected as a comparator with the reference level at the base of Q644 determined by the network R638-R646R647-R648-R649-Q646. The 0.4 V adjustment R649 is set to provide accurate output voltage at the 0.4 V Calibrator pin-jack J651.

The output of the Calibrator Countdown stage is connected to the base of Q634 through R634. Q634 acts as a switch to control the current through Q636, and the output of Q636 controls the conduction of comparator Q642-Q644. The level at the base of Q634 is switched between the LO and HI levels at the two-kilohertz rate. When the base of Q634 is LO, Q642 is off and Q644 is conducting. This produces a positive output voltage at the Calibrator pin-jacks. When the level at the base of Q634 is switched to HI, Q644 conducts and Q646 is reverse biased. Now, the voltage level at the Calibrator pin-jacks drops to zero.

Input		Output
3	1	Condition at pin 7 after trigger pulse
LO	LO	Output changes state with each trigger pulse
LO	HI	HI
HI	LO	LO
HI	HI	No change

Fig. 3-31. Input/output table for U632.

**Output Voltage Divider.** The collector current of Q644 in the Output Amplifier stage is applied across the voltage divider made up of resistors R652 through R659. This divider is designed to provide a low output

## Circuit Description-R7704

resistance in all positions except 40 V, while providing accurate output voltages between 4 mV and 40 V (4 mV and 40 V levels available at internal board connections and can be connected to the front-panel by changing board connections). The output resistance in the 40 V position is about 15 kilohms as determined by R651 and the equivalent resistance of divider network R652-R659. This means that a 1.5 megohm load will produce about 1% error in output voltage for this position; error increases as the load resistance decreases. The remaining four output voltages are accurate with a one-megohm load or, at reduced output, a 50-ohm load. Output voltages into a 50-ohm load are: 4 V pin-jack, 0.4 V; 0.4 V pin-jack, 0.2 V; 40 mV pin-jack, 20 mV; 4 mV (internal), 2 mV.

## CRT CIRCUIT

### General

The CRT Circuit produces the high-voltage potentials and provides the control circuits necessary for the operation of the cathode-ray tube (CRT). This circuit also includes the Z-Axis Amplifier stage to set the intensity of the CRT display and the Auto-Focus Amplifier to maintain optimum focus of the CRT display. Fig. 3-32 shows a detailed block diagram of the CRT Circuit. A schematic of this circuit is shown on diagram 9 at the rear of this manual.

### Z-Axis Amplifier

**General.** The Z-Axis Amplifier stage is a current driven, shunt-feedback amplifier with voltage output. The output voltage provides the drive signal to control the CRT intensity level through the Control-Grid Supply. Details of operation for the individual stages within this circuit follow.

**Turn-On Delay.** Transistors Q706, Q708, and Q712 provide a delay for the CRT Circuit to prevent it from coming into operation until the other circuits within the instrument have reached operating levels. When the instrument is turned on, C711 begins to charge through R709R71 1-R712. However, since C71 1 is completely discharged when the instrument is turned on, the base of Q712 is at -15 volts. As C711 charges, it pulls the base of Q712 positive and its emitter follows. C711 continues to charge until the emitter level of Q712 reaches about +50 volts (Q712 saturated). The emitter voltage of Q712 supplies the positive voltage for the feedback divider in the High-Voltage Regulator stage. The delay provided by the charging of C711 prevents CRT beam current for about four seconds. This protects the CRT phosphor from damage due to a high-intensity display as the instrument is first turned on.

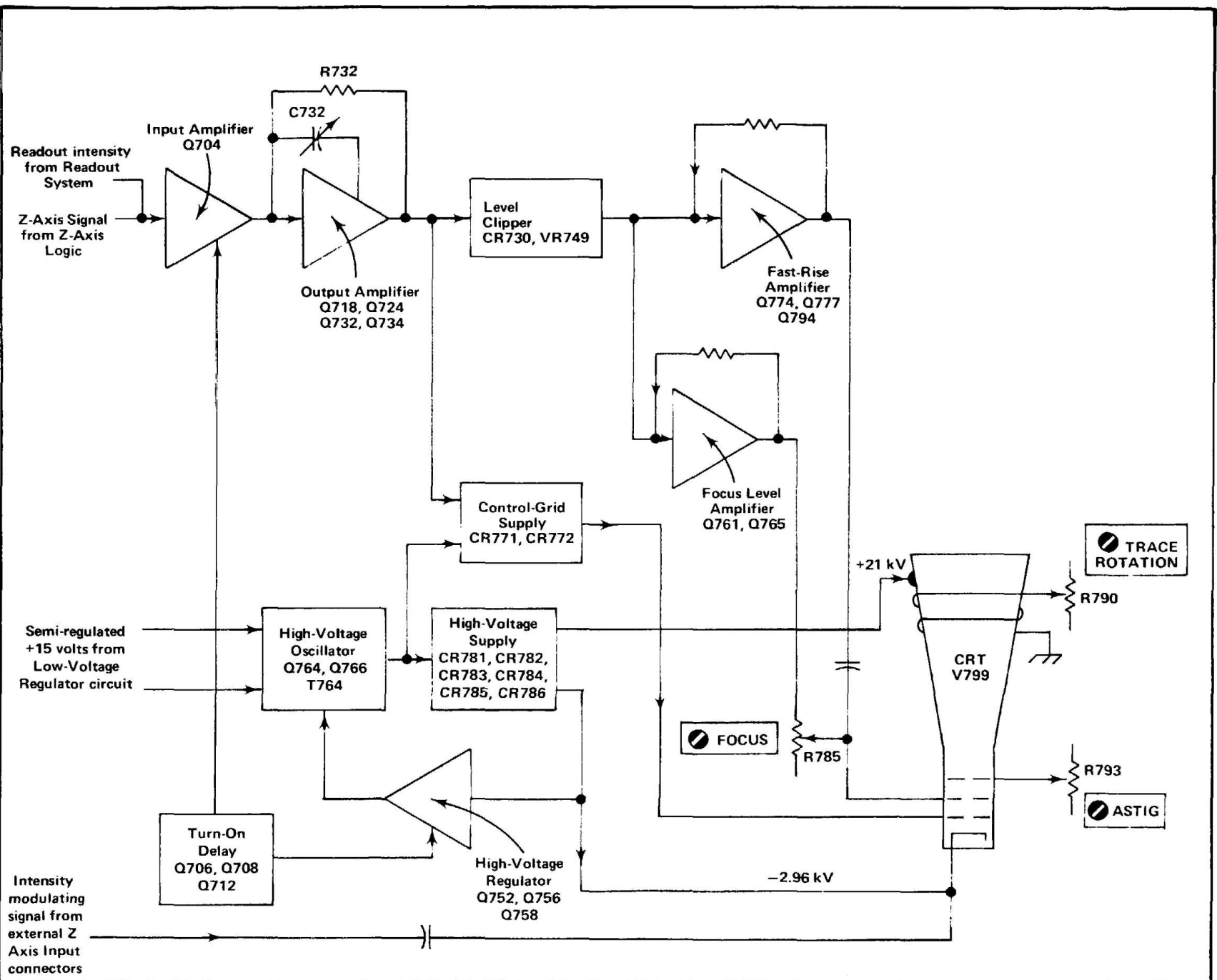


Fig. 3-32. CRT Circuit detailed block diagram.

The current flow through R709 as C711 charges also forward biases transistor Q708. This holds Q706 reverse biased so it does not supply current to Input Amplifier Q704. The result of this reduction in current to Q704 is that the Z-Axis Amplifier output remains at its low level regardless of the input from either the Z-Axis Logic stage or the Readout System. When C711 reaches full charge, the current flow through R709 ceases and Q708 is reverse biased. Q706 is now forward biased and it supplies about four milliamperes of bias current to Q704. Diode CR708 protects Q708 as C711 discharges when the instrument is turned off.

**Input Amplifier.** Transistor Q704 is a common-base amplifier to establish a low input impedance for the Z-Axis Amplifier. The operating bias for Q704 is established by Q706 as described in the previous paragraph. The output level of this stage is determined by the input current from either of two circuits. For normal operation, the Z-Axis Signal from the Logic Circuit sets the input current as determined by the front-panel A and B INTENSITY controls, the chopped blanking logic, or an external signal connected to either of the rear-panel Z-Axis Inputs (see Logic Circuit description for details). For readout displays, the Z-Axis Signal is blocked in the Logic Circuit. Now, the input current is provided from the Readout System as determined by the READOUT intensity control on the front panel.

**Output Amplifier.** The output stage is a shunt-feedback operational amplifier with feedback connected from the output to the input through C732-R732. The output voltage is determined by the input current multiplied by the feedback resistor and is expressed by the formula:  $E_{out} = I_{in} \times R_{fb}$  where R732 is  $R_{fb}$ . The signal current change at the base of Q704 for maximum intensity is about four milliamperes. The maximum output voltage change is set for 64 volts (about 4 mA  $\times$  15.4 k $\Omega$ ). AC feedback is provided from the output to the base of Q718 by C732. This capacitor is adjusted for optimum step response to provide a fast rise unblanking gate output signal with minimum overshoot or ringing. Otherwise, the CRT display would vary in intensity level following sudden changes in blanking.

The signal from the Input Amplifier stage is amplified by Q718-Q724. Variable resistor R719 in the collector circuit of Q718 provides transient response adjustment for this stage. The signal at the collector of Q724 is connected to the base of transistor Q732 through C730 and to the base of Q734 through R722-C723-R723. These transistors are connected as a collector-coupled complementary amplifier to provide a linear, fast output signal while consuming minimum quiescent power. The signal at the collector of Q724 is connected to the base of Q734 through R722. This transistor maintains the low-frequency response of the input signal and provides a fast falling edge on the output signal.

(A)

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Only the fast-changing portions of the input signal are coupled to the base of Q732 through C730. Since Q732 is a PNP-type transistor, it responds faster to negative-going changes at its base than to positive-going changes. This action provides a fast rising edge on the output signal (fast falling edge provided by Q734, an NPN-type transistor). The signal at the collectors of Q732-Q734 is connected to the Control Grid Supply stage through R735-R736.

Diodes CR718, CR734, and CR735 provide protection for the Z-Axis Amplifier circuit. CR735 protects this stage from damage due to high-voltage surges connected back into this circuit from the high-voltage supply. CR734 protects Q734 by clamping its base at -0.6 volt if Q724 fails or is removed from its socket while the instrument is on. CR718 protects Q718 against excess reverse base-emitter voltage.

## Auto Focus

**General.** The Auto Focus stage develops control voltages to maintain optimum focus of the CRT display. When the FOCUS control is set for best definition of the CRT display at low to medium settings of the INTENSITY controls, this stage will maintain optimum focus for all portions of the display as it switches between readout, A sweep, B sweep, and high or low intensity displays.

**Level Clipper.** The voltage requirements at the Focus Grid of the CRT to maintain a focused display are fairly constant for low and medium intensity level settings. However, for displays which require intensity control settings beyond midrange, the voltage requirement at the Focus Grid increases linearly with the increase in intensity drive at the output of the Z-Axis Amplifier stage. CR730 and zener diode VR749 clip the output level of the Z-Axis Amplifier stage so the Auto Focus stage is not activated for low or medium intensity displays. Quiescently, the anode of VR749 rests near zero volts. The positive voltage applied to VR749 through R730 sets the cathode of VR749 at about +30 volts. Therefore, CR730 is held reverse biased until its anode rises above about +30.5 volts. Then, the portion of the Z-axis drive signal which exceeds the 30-volt level is coupled to the Auto-Focus amplifier stages.

**Fast-Rise Amplifier.** The portion of the Z-axis drive signal which exceeds the clipping level is coupled to the base of Q774 through C767-R767-R768-R769. Focus Gain adjustment R769 determines the amount of signal connected to the base of Q774 to set the overall gain of the Fast-Rise Amplifier. C767 adjusts the high-frequency attenuation of the input signal to determine the step response of the stage. Q774, Q777, and Q794 are connected as a feedback amplifier to provide fast response to the high-frequency components of the auto-focus control signal. The output signal at the emitter of Q794 is connected to the Focus Grid of



the CRT through R798 and C798. This capacitor blocks the DC component so only the fast changing portions of the signal at the emitter of Q794 are coupled to the Focus Grid.

**Focus Level Amplifier.** Q761 and Q765 make up a DC-coupled amplifier to determine the amplitude of the low-frequency components of the auto-focus control signal. The portion of the Z-axis drive signal which exceeds the clipping level is also coupled to the base of Q761 through R760 and R761. Focus Level adjustment R761 determines the gain of this stage to provide optimum focus at all intensity levels. Typical gain of this stage is about 10.

The output at the collector of Q765 is coupled to the Focus Grid through R740E, R785, and R784. Therefore, this stage determines the source voltage for the FOCUS adjustment. The FOCUS adjustment is adjusted for best focus for low to medium intensity displays (if the instrument is equipped with readout, the FOCUS adjustment should be set for best definition of the readout display). Then, the auto-focus stages automatically control the voltage at the Focus Grid to maintain optimum focus of the remaining portions of the display.

### High-Voltage Oscillator

Unregulated voltage for operation of the high-voltage supply is provided from the semi-regulated +15 volts in the Low-Voltage Regulator circuit. The starting bias current for the High-Voltage Oscillator is supplied from the positive side of the +15 volt input through R759. As the High Voltage Oscillator begins to operate, the emitter of Q758 goes negative and further bias current is available through CR759 from the negative side of the semi-regulated +15 volts. This configuration provides a controlled starting current for the High-Voltage Oscillator at turn-on and at the same time allows the High-Voltage Regulator stage to control the current of the High-Voltage Oscillator to regulate the output level after the stage reaches operating potential.

Q764-Q766 and the associated circuitry comprise an oscillator to drive high-voltage transformer T764. When the instrument is turned on, assume that Q764 comes into conduction first. The collector current of Q764 produces a corresponding current increase in the base-feedback winding of T764 to further increase the bias on Q764. At the same time, the voltage developed across the base feedback winding connected to Q766 reverse biases it.

As long as the collector current of Q764 continues to increase, a voltage is induced into the base-feedback windings of T764 which holds Q764 forward biased. However, when the collector current of Q764 stabilizes, the magnetic field built up in T764 begins to collapse. This induces an opposite current into the base windings

### Circuit Description-R7704

which reverse biases Q764, but forward biases Q766. When the induced voltage at the base of Q766 exceeds the bias set by Q758, Q766 is forward biased and the amplified current at its collector adds to the current flowing through T764 due to the collapsing field. Then, as the current through T764 stabilizes again, the magnetic field around it once more begins to collapse. This reverses the conditions to start another cycle.

The signal produced across the primary of T764 is a sine wave at a frequency of 35 to 45 kilohertz. C764-L764 shape the signal in the primary of T764 to improve regulation of the high-voltage supply. The amplitude of the oscillations in the primary of T764 is controlled by the High Voltage Regulator stage to set the total accelerating potential for the CRT. Filter network C762-L762 decouples high peak operating currents from the +15-Volt Supply.

### High-Voltage Regulator

A sample of the secondary voltage from T764 is connected to the High-Voltage Regulator stage through divider R740A-R740B-R740C. Q752 and Q756 are connected as an error amplifier to sense any change in the voltage level at the base of Q752. The -15-Volt Supply, connected to the emitter of Q752 through R753-R755, and the +50 volts connected to R740A from the emitter of Q712 provide the reference level for this stage. High Voltage adjustment R743 sets the quiescent level at the base of Q752 to a level which establishes a -2.96 kilovolt operating potential at the CRT cathode. CR747 protects Q752 from excessive reverse emitter-base voltage.

Regulation occurs as follows: If the output voltage at the -2960 V test point starts to go positive (less negative), a sample of this positive-going change is connected to the base of Q752. Both Q752 and Q756 are forward biased by this positive change which in turn increases the conduction of Q758. This results in a greater bias current delivered to the bases of Q764-Q766 through Q758. Now, the bases of both Q764 and Q766 are biased closer to their conduction level so that the feedback voltage induced into their base feedback windings produces a larger collector current. This results in a larger induced voltage in the secondary of T764 to produce a more negative level at the -2960 V test point to correct the original error. In a similar manner, the circuit compensates for output changes in a negative direction. Since the amplitude of the voltage induced into the secondary of T764 also determines the output level of the positive High-Voltage Supply and the Control-Grid Supply, the total high-voltage output is regulated by sampling the output of the negative High-Voltage Supply.

### High-Voltage Supplies

High-voltage transformer T764 has three output windings. One winding provides filament voltage for the

cathode-ray tube. Two high-voltage windings provide the negative and positive accelerating potential for the CRT and provide the bias voltage for the control grid. All of these outputs are regulated by the High-Voltage Regulator stage to maintain a constant output voltage as previously described.

Positive accelerating potential for the CRT anode is supplied by voltage quintupler C782-C783-C784-C785-C786-CR782-CR783-CR784-CR785-CR786. This rectified voltage is filtered by C787-R786-R787 to provide an output of about +21 kilovolts. All of these components are included in encapsulated assembly U786. The negative accelerating potential for the CRT cathode is also obtained from the same secondary winding. Half-wave rectifier CR781 provides an output voltage of about -2.96 kilovolts which is connected to the CRT cathode through L781 and L788. The cathode and filament are connected together through L788 to prevent cathode-to-filament breakdown due to a large difference in potential between these CRT elements. Neon bulbs DS781 and DS785 protect L781 and L788 if the CRT cathode is shorted to chassis ground. Diode CR780 and neon bulb DS780 protect the +50-Volt Supply from damage under this condition. A sample of the negative accelerating voltage is connected to the High-Voltage Regulator stage to maintain a regulated high-voltage output.

Half-wave rectifier CR772 provides a negative voltage for the control grid of the CRT. Output level of this supply is set by the CRT Grid Bias adjustment R739. Rectifier CR771 provides rectified low-potential voltage to R739 so that it can perform its function without being enclosed in the high-voltage compartment. Neon bulbs DS786-DS787-DS788 protect the CRT by limiting the voltage difference between the cathode and control grid to a maximum of about 165 volts. The unblanking gate from the Z-Axis Amplifier circuit is connected to the positive side of the Control-Grid Supply. As the unblanking gate level changes, it shifts the overall supply level to change the bias on the CRT which controls the intensity of the display.

High speed intensity modulating signals from the rear panel HIGH SPEED connector J1055 are applied to the CRT cathode through C790-C791-R788. This signal changes the CRT bias, and thereby the intensity of the display, by changing the level of the cathode. RC divider C 1056-C 1057-R 1056-R 1057 provides a cross-over network between the HIGH SPEED and HIGH SENSITIVITY inputs. The HIGH SENSITIVITY connector provides an input for low-frequency, low-amplitude intensity modulating signals. This signal is connected to the Z-Axis Logic stage through R 1060 (see Logic Circuit description for further information).

#### **CRT Control Circuits**

The ASTIG adjustment R793, which is used in conjunction with the FOCUS adjustment to obtain a well

#### **Circuit Description-R7704**

defined display, varies the positive level on the astigmatism grid. Geom adjustment R792 varies the positive level on the horizontal deflection plate shield to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field around the CRT. Y Axis Align adjustment R795 controls the current through L795 which affects the CRT beam after vertical deflection but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. TRACE ROTATION adjustment R790 controls the current through L790 and affects both the vertical and horizontal rotation of the beam.

#### **LINE TO DC CONVERTER/REGULATOR**

##### **General**

The Line to DC Converter/Regulator circuit provides the operating power for this instrument from an AC line voltage source. This circuit also includes the Line Selector assembly to allow selection of the nominal operating voltage for the instrument. Fig. 3-33 shows a detailed block diagram of the Line to DC Converter/Regulator circuit. A schematic of this circuit is shown on diagram 10 at the rear of this manual.

##### **Line Input**

Power is applied to this circuit through Line fuse F800, EMI (electro-magnetic interference) filter FL801, POWER switch S800, and thermal cutout S801. The EMI filter is made up of C800-C801-C803-L800-L801-T800. This filter is designed primarily to filter out the 25 kilohertz interference originating within this circuit. L800-L801 provide differential and common-mode inductance; T800 provides additional common-mode inductance. C803 along with the differential inductance of L800-L801 provides differential EMI filtering. R803 provides differential resonance damping for C803-L800-L801. R804 provides a discharge path for C803 when the POWER switch is turned off. Common-mode EMI filtering is provided by C800-C801 along with the common-mode inductance of T800. R801 provides common-mode resonance damping for C800-C801 - T800.

Thermal cutout S801 provides thermal protection for this instrument. If the internal temperature of the instrument exceeds a safe operating level, S801 opens to interrupt the applied power. When the temperature returns to a safe level, S801 automatically closes to re-apply the power. Cooling is provided by fan B801. Line power is connected directly to B801 in the 115 V position of the Line Selector switch. In the 230 V position, power is connected to B801 through step-down auto-transformer T801 to provide the required 115-volts operating potential for B801.

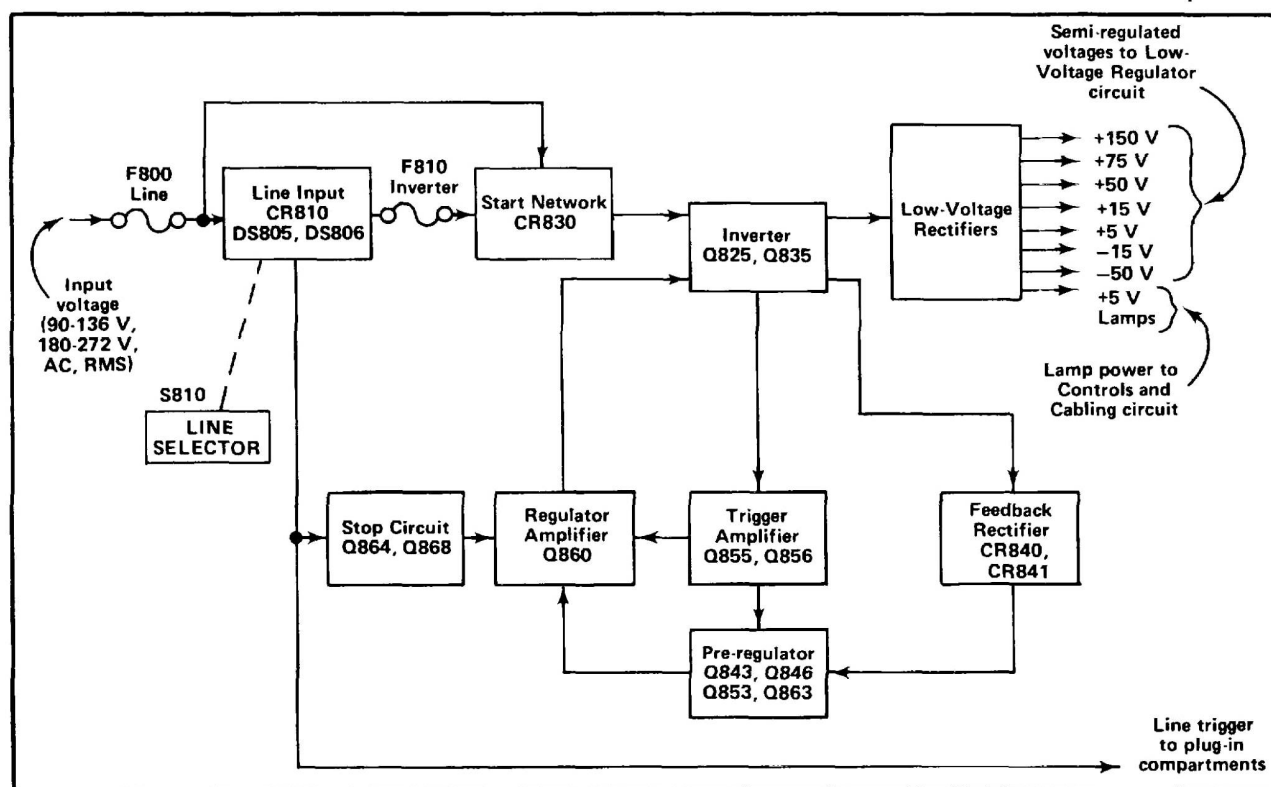


Fig. 3-33. Detailed block diagram of Line to DC Converter/Regulator circuit.

Line Selector switch S810 allows this instrument to operate from either a 115-volt nominal line or a 230-volt nominal line. In the 115 V position, rectifier CR810 operates as a full-wave doubler along with capacitors C813-C814. For 230 V operation, S810 connects rectifier CR810 in the bridge configuration and C813-C814 operate as series energy-storage capacitors. With this configuration, the output voltage applied to the Inverter stage from the Line Input stage is about the same for either 115-volt or 230-volt operation.

C810-L810 and C811-L811 form a 25 kilohertz filter to provide further EMI filtering. Thermistors RT810 and RT811 limit the surge current demanded by the power supply when it is first turned on. After the instrument is in operation, the resistance of the thermistors drops so they have very little power loss and have little effect on the operation of this stage. The stored charge on C813 and C814 limits the surge current if the POWER switch is quickly turned off and back to ON after the resistance of these thermistors has dropped to their low value. The discharge of capacitors C813-C814 is controlled by R813, and it is so designed that the discharge time constant of C813-C814-R813 is about equal but opposite to the thermal time constant of RT810-RT811. This arrangement provides surge-current limiting for the Line Input stage at all

times. Since C813-C814 discharge slowly, dangerous potentials can exist within this supply for several minutes after the POWER switch is turned off. C812-DS812-R812 form a relaxation oscillator to indicate the presence of voltage across C813-C814. Neon bulb DS812 will blink until the potential across these capacitors drops to about 80 volts.

The rectified output voltage from this stage is connected to the Start Network through Inverter fuse F810. This fuse protects the Inverter stage if it demands too much current due to a malfunction.

DS805 and DS806 are surge voltage protectors. When the Line Selector switch is in the 115 V position, only DS805 is connected across the line input. If a peak voltage surge in excess of about 230 volts is present on the line, DS805 will break down and demand high current. This excess current will quickly open Line fuse F800 to interrupt the input power before the circuit can be damaged. In the 230 V position, DS805 and DS806 are connected in series across the line input to provide surge voltage protection for peak voltage surges in excess of about 460 volts.

Transformer T805 provides a sample of the line voltage to the plug-in connectors in the Main Interface circuit for



internal triggering at line frequencies or for other applications. In the 115 V position of S810, the line input voltage is connected across the primary of T805 and R805. For the 230 V position, the line voltage is connected across the primary of T805 and R805-R806 in series. This arrangement provides an output line trigger signal of about one volt RMS for both nominal line voltages. This trigger signal is also connected to the Stop Circuit to indicate when line voltage is connected to the Line Input stage and the POWER switch is ON.

### Start Network

Rectified DC power for the Inverter stage is supplied through EM I filter C820-C821-C822-T820. C820-C822-T820 provide common-mode filtering and C821 provides differential filtering. Resistors R820 and R821 provide common-mode and differential resonance damping respectively. The positive input voltage is connected directly to power transformer T870. The negative input voltage provides the negative reference for the Inverter stage; the negative voltage to the power transformer is determined by the Inverter stage.

The input line voltage to this instrument is connected to divider R823-R824. This voltage charges C824 on each half cycle. When the charge on C824 reaches about 32 volts, trigger diode CR830 conducts to provide a turn-on trigger current to transistor Q835 through C835. This current allows the Inverter stage to start operating. After the Inverter stage is operating, the recurrent waveform at the collector of Q835 keeps C824 discharged through CR831.

### Inverter

A simplified schematic of the Inverter stage is shown in Fig. 3-34. After the circuit has been placed into operation by the Start Network, LC circuit C1-L1 oscillates at its resonant frequency. The resulting current through the one turn winding of T1 induces a bias current into the base circuit of either Q1 or Q2, depending upon the polarity. The 1:4 turns ratio of T1 results in a current in the transistor base circuits which is one-fourth the current in the one turn feedback winding. Since the current in the feedback winding must flow through the conducting transistor, the transistors operate at a forced beta of four. A sine-wave current is produced across the primary of power transformer T2; the voltage is a square-wave with a peak-to-peak amplitude equal to the input DC voltage. The voltage induced into the secondary of T2 is rectified by diodes CR1 and CR2, filtered by capacitor C2 and applied across load R2.

Now, refer to the complete Line to DC Converter/Regulator diagram. The LC circuit is made up of C870 and L870. After the circuit has been started by the Start Network as discussed previously, C870-L870 resonate at a frequency of 25 kilohertz. The feedback to the base circuits of Q825-Q835 through T825 alternately turns Q825 and Q835 on. These transistors operate at a forced beta of four due to the turns ratio of T825, and their output current sustains resonance in C870-L870. The 60-turn center tapped winding of T825 is used to delay the turn-on of Q825 or Q835 to provide pre-regulation of the voltages produced in the secondary of T870. This operation will be discussed in more detail under Pre-Regulator.

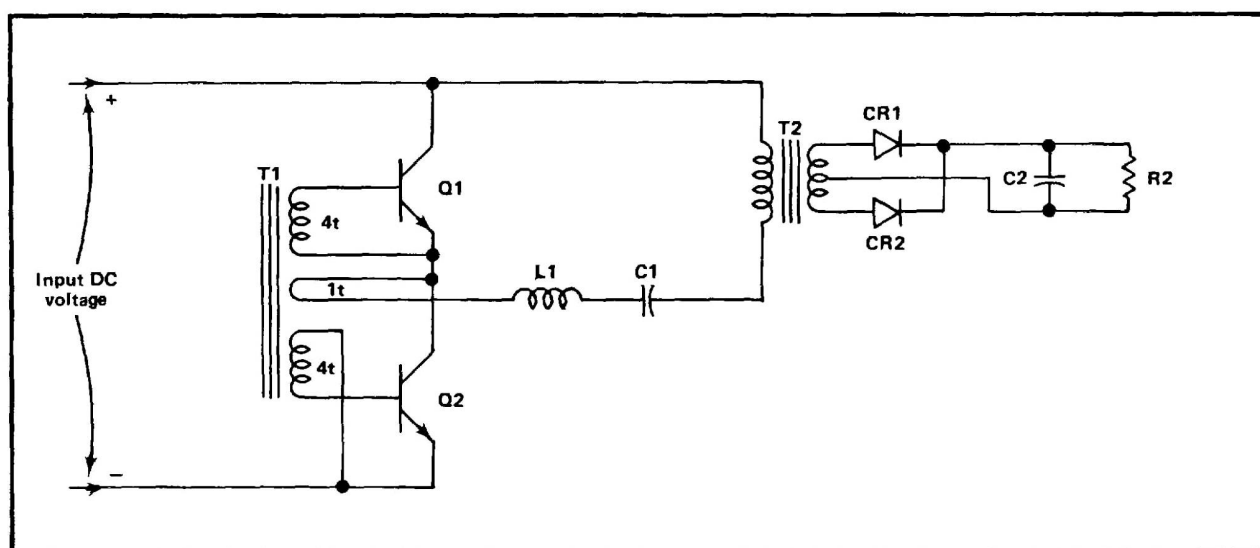


Fig. 3-34. Simplified schematic of Inverter stage.

Diodes CR828 and CR838 provide reverse conduction paths across Q825 and Q835 respectively when these transistors are held off for pre-regulation purposes. Inductors L826-L836 minimize turn-on losses in the transistors by reducing the voltage on Q825-Q835 during their turn-on interval. CR826-R826 and CR836-R836 protect Q825 and Q835 from excessive voltage due to stored energy in the associated inductors when the transistors are turned off. Diodes CR825 and CR835 aid in the turn off of the associated transistors by connecting the collector potential back to the base of each transistor. This feedback does not turn the transistor off but eliminates excess base current to reduce the turn-off time when the current from feedback transformer T825 reverses. The networks C825-R825 and C835-R835 develop voltage biases in response to the average base currents of Q825 and Q835 which help to hold Q825 and Q835 in cutoff during their respective off intervals.

#### **Trigger Amplifier**

The primary current of power transformer T870 also flows through the one-turn primary winding of T839. The voltage induced into the secondary of T839 is differentiated by C855-R855 and C856-R856 and connected to the bases of Q855 and Q856. Notice that the differentiated signals at the bases of these transistors is opposite in polarity and this polarity changes on each half-cycle of the induced voltage. Therefore, on each half-cycle the transistor which receives a positive-going pulse at its base is momentarily forward biased. This results in a negative-going pulse at the collector of either Q855 or Q856 which is connected to the Pre-Regulator multivibrator.

CR857 and CR858 rectify the voltage in the secondary of T839. Under normal conditions, the rectified voltage developed across C858-R858 is not sufficient to forward bias CR859. However, if excess current is demanded from the Inverter stage, the current through the primary of T839 increases to result in a larger current in its secondary. This results in a larger voltage drop across R858 and, when it is sufficient to forward bias CR859, Q860 in the Regulator Amplifier circuit is turned on to limit the output current of the Inverter stage.

#### **Feedback Rectifier**

Diodes CR840 and CR841 form a center-tapped fullwave rectifier. The rectified output of these diodes is filtered by C840-R840 to provide a feedback voltage of about +16 volts to the Pre-Regulator stage. The exact output level depends upon the voltage applied to the primary of transformer T870. This feedback is used to provide preregulation of the output voltage from T870.

#### **Pre-Regulator**

Q853 and Q863 form a monostable multivibrator. The circuit conditions are such that Q863 is conducting in the stable state. When a negative-going trigger pulse is received

#### **Circuit Description-R7704**

from the Trigger Amplifier stage, Q863 turns off and Q853 turns on. The amount of time that Q853 remains in conduction is determined by the recharge time of C852. This time is, in turn, determined by Q843-Q846 and the feedback voltage from the Feedback Rectifier. Q843 and Q846 are connected as a comparator. Zener diode VR848 sets a level of about +9 volts at the base of Q846. The output voltage of the Feedback Rectifier stage is connected across divider R842-R843-R844. The +75 Volts adjustment R843 in this divider is adjustable to set the output voltages produced by this circuit. If the feedback voltage from the Feedback Rectifier stage should increase after R843 has been adjusted properly, the collector current of Q843 will decrease. Therefore, C852 will recharge more slowly and Q863 will remain off for a longer period of time (further explanation of regulation will be given under Regulator Amplifier, which follows). Likewise, if the feedback voltage decreases, the collector current of Q843 increases and C852 recharges more rapidly so Q863 is off for a shorter period of time.

#### **Regulator Amplifier**

The actual pre-regulation of the voltages produced by this circuit is controlled by transistor Q860. This transistor is connected so it is always on when Q863 is off (note exceptions for current limiting and Stop Circuit operation). Therefore, when multivibrator Q853-Q863 has been triggered so Q863 is off, Q860 is on. The collector of Q860 drops negative and it conducts current away from the secondary of T825 through CR823 and CR824. Due to the turns ratio of T825, this action does not allow any current from the feedback winding of T825 to reach the bases of either Q825 or Q835. As a result, the inverter transistors remain off as long as Q860 is on, and they do not conduct current through the primary of T870. When the Pre Regulator multivibrator resets so Q863 is again conducting, Q860 turns off. Now, Q860 no longer conducts current away from T825 so feedback current can reach the base windings of this transformer. As a result, the Inverter transistors operate as described previously for the remainder of this half cycle. By controlling the amount of time that Q860 is in conduction, the voltage that is delivered to power transformer T870 can be controlled. The amount of time that Q860 conducts is controlled by comparator Q843-Q846 and the feedback voltage as described under Pre-Regulator.

The network C860-CR860-R860-R861 in the collector circuit of Q860 protects this transistor from the positive voltage which is developed across the 60-turn winding of T825 when Q860 is turned off. C858-CR857-CR858-CR859-R858 in the Trigger Amplifier stage, provide a current limiting network to protect the supply when excess current is demanded from the inverter stage. When this condition occurs, the base of Q860 is pulled positive so that it conducts to limit the output current from this circuit as long as excess current is flowing through the primary of T839.

### Stop Circuit

Transistors Q864 and Q868 provide a circuit to stop the operation of the Inverter stage when the POWER switch is turned off or the line voltage is disconnected from this instrument. When the POWER switch is turned on and line voltage is available, line-trigger pulses from transformer T805 in the Line Input stage are connected to the base of Q868 through R868. Each time a trigger pulse is received, Q868 conducts and its collector goes negative to discharge C867. However, when there are no line triggers at the base of Q868, C867 begins to charge towards the feedback voltage through R867. As C867 charges, the base of Q864 is pulled positive to a level where it conducts. Then, the emitter of Q864 pulls the base of Q860 positive also to bring it into conduction. The conduction of Q860 takes all of the feedback current away from T825 so the Inverter stage ceases operation.

### Low-Voltage Rectifiers

The rectifiers and associated filter components in the secondaries of T870 provide rectified, pre-regulated voltages for re-regulation by the Low Voltage Regulator circuit for operation of this instrument or for connection to the plug-in compartments. Zener diode VR876 and silicon controlled rectifier Q876, connected from the +150 Volt output to ground, provide over-voltage protection for this circuit. If the output voltage across this secondary of T870 increases to about 180 volts, VR876 conducts to turn on Q876. This effectively provides a direct short across this winding of T870 and demands high current from the circuit. A high current demand in the secondary of T870 results in Inverter fuse F810 opening to interrupt the power to the Inverter stage.

## LOW-VOLTAGE REGULATOR

### General

The Low-Voltage Regulator circuit contains five regulated supplies. Electronic regulation converts the semiregulated input voltages from the Line to DC Converter/ Regulator circuit to stable, low-ripple output voltages. Each supply contains a short-protection circuit to prevent instrument damage if a supply is inadvertently shorted to ground or to another supply. Fig. 3-35 shows a detailed block diagram of the Low-Voltage Regulator circuit. A schematic of this circuit is shown on diagram 11 at the rear of this manual.

### -50-Volt Supply

The following discussion includes the description of the -50 V Series Regulator, -50 V Feedback Amplifier, -50 V Reference, and -50 V Current Limiting stages. Since these stages are closely regulated in the production of the -50-volt regulated output voltage, their operation is most easily understood when discussed as a unit.

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Semi-regulated -50 volts from the Line to DC Converter/Regulator circuit provides the unregulated voltage source for this supply. Transistors Q984, Q992, Q994, and Q998 operate as a feedback-stabilized regulator circuit to maintain a constant -50-volt output level. Q984 is connected as a differential amplifier to compare the feedback voltage at the base of Q984B against the reference voltage at the base of Q984A. The error output at the collector of Q984A reflects the difference, if any, between these two inputs. The change in error-output level at the collector of Q984A is always in the same direction as the change in the feedback input at the base of Q984B (in phase).

Zener diode VR982 sets a reference level of about -9 volts at the base of Q984A. A sample of the output voltage from this supply is connected to the base of Q984B through divider R985-R986-R987. R986 in this divider is adjustable to set the output level of this supply. Notice that the feedback voltage to this divider is obtained from a line labeled -50 V Sense. Fig. 3-36 illustrates the reason for this configuration. The inherent resistance of the interconnecting wire between the output of the -50-Volt Supply and the load produces a voltage drop which is equal to the output current multiplied by the resistance of the interconnecting wire. Even though the resistance of the wire is small, it results in a substantial voltage drop due to the high output current of this supply. Therefore, if the feedback voltage were obtained ahead of this drop, the voltage at the load might not maintain close regulation. However, the -50 V Sense configuration overcomes this problem since it obtains the feedback voltage from a point as close as practical to the load. Since the current in the -50 V Sense line is small and constant, the feedback voltage is an accurate sample of the voltage applied to the load.

Regulation occurs as follows: If the output level of this supply decreases (less negative) due to an increase in load, or a decrease in input voltage (as a result of line voltage changes or ripple), the voltage across divider R985-R986-R987 decreases also. This results in a more positive feedback level at the base of Q984B than established by the -50 V Reference stage at the base of Q984A. Since the transistor with the more positive base controls the conduction of the differential amplifier, the output current at the collector of Q984A decreases. This decrease in output from Q984A allows more current to flow through Q992 and Q994 to result in increased conduction of the -50 V Series Regulator Q998. The load current increases and the output voltage of this supply also increases (more negative). As a result, the feedback voltage from the -50 V Sense line increases and the base of Q984B returns to the same level as the base of Q984A. Similarly, if the output level of this supply increases (more negative), the output current of Q984A increases. The feedback through Q992 and Q994 reduces the conduction of the -50 V Series Regulator to decrease the output voltage of this supply.

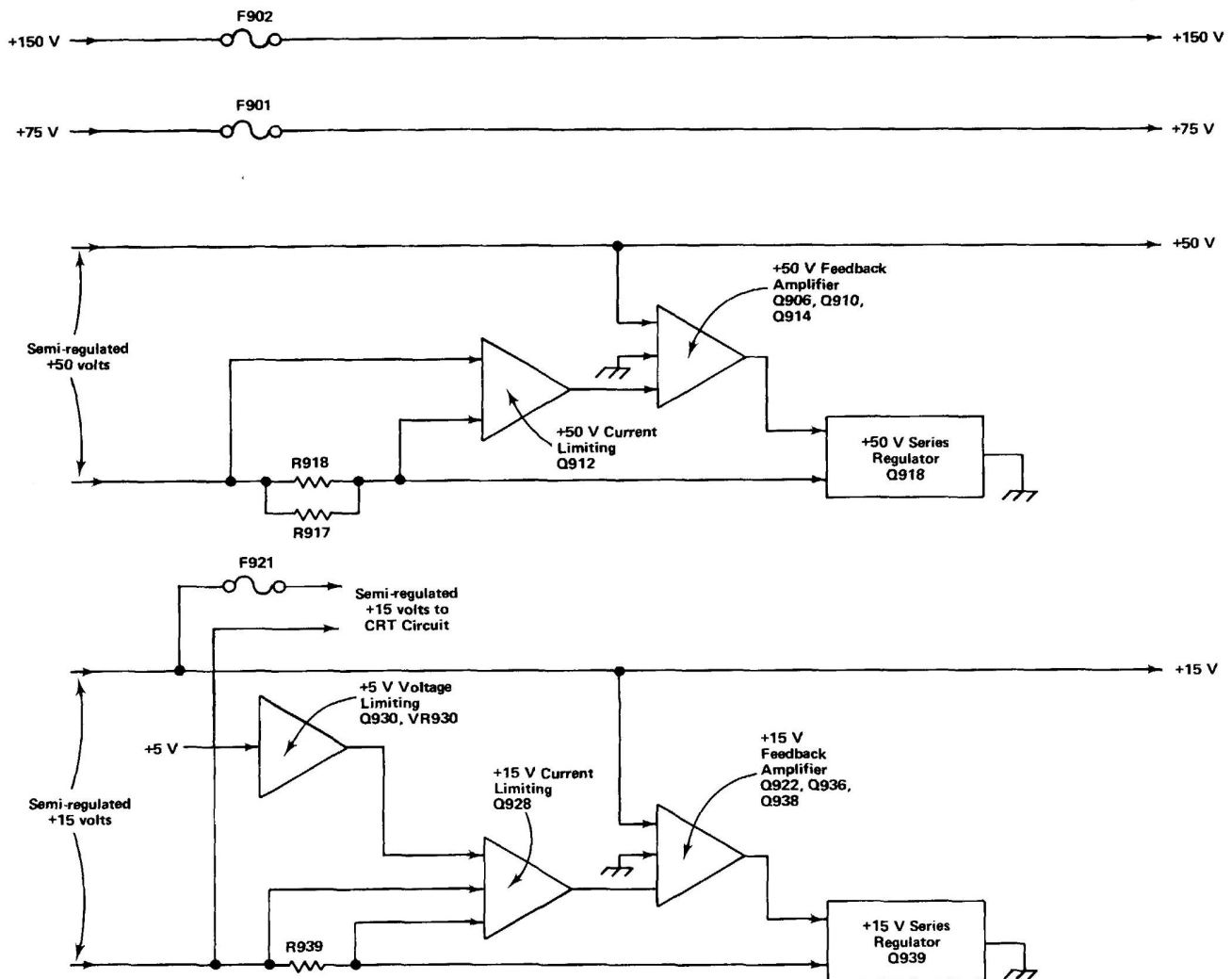


Fig. 3-35. Detailed block diagram of Low-Voltage Regulator circuit.

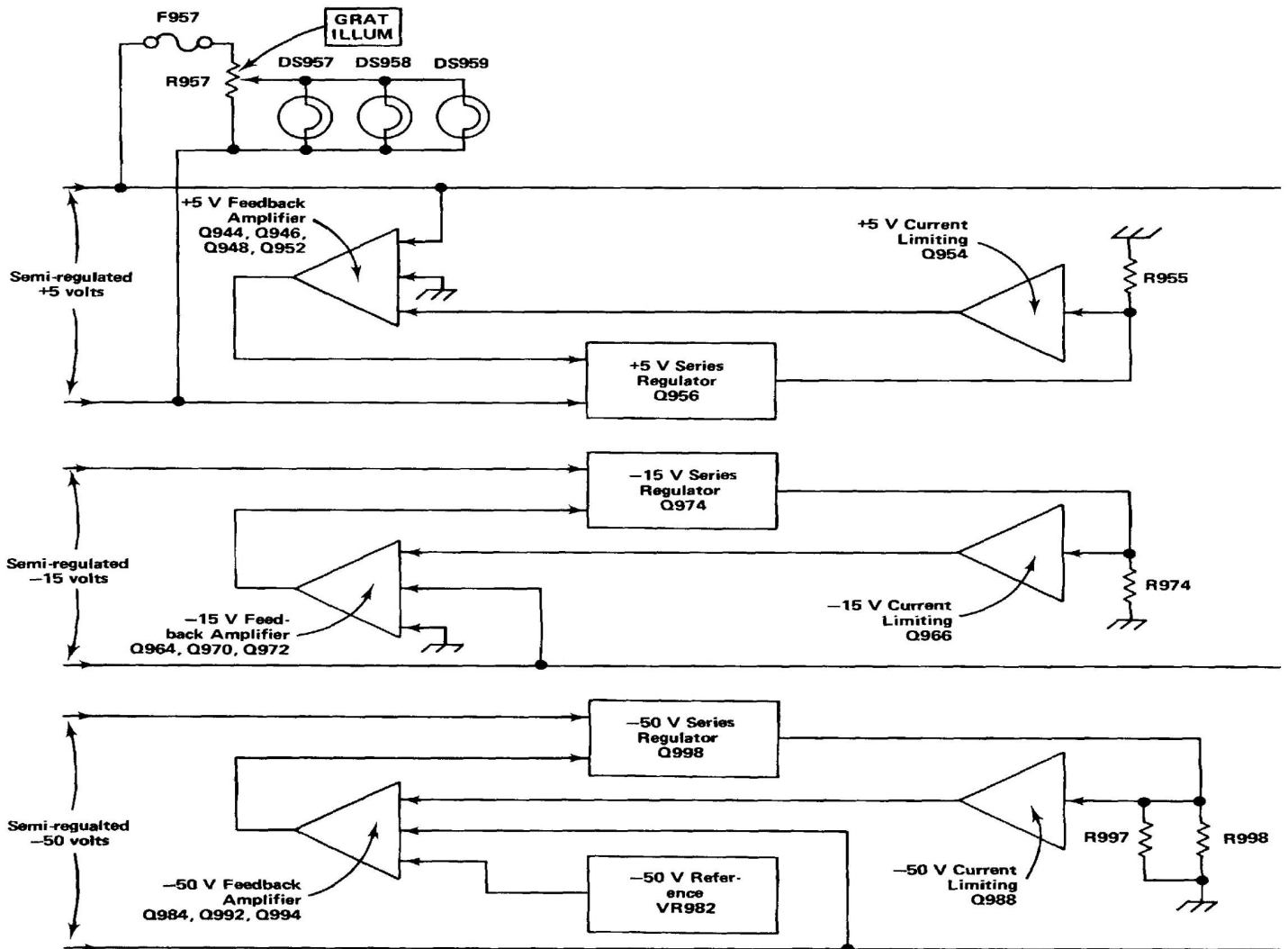


Fig. 3-35. (cont).

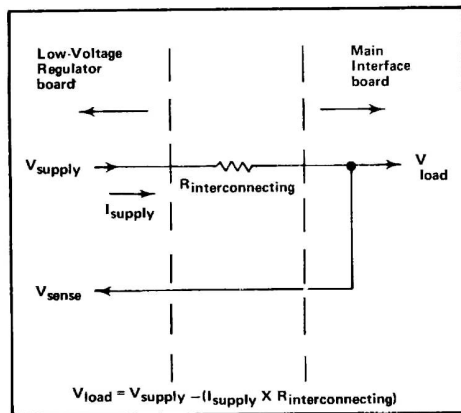


Fig. 3-36. Schematic illustrating voltage drop between power supply output and load due to resistance of interconnecting wire.

C990-R990 and C992-R992 provide stabilization for the feedback network by reducing the response time of the feedback network so it can not oscillate.

The -50 Volts adjustment R986 determines the divider ratio to the base of Q984B and thereby determines the feedback voltage. This adjustment sets the output level of the supply in the following manner: If R986 is adjusted so the voltage at its variable arm goes less negative (closer to ground), this appears as an error signal at the base of Q984B. In the same manner as described previously, this positive-going change at the feedback input of the differential amplifier increases the conduction of the -50 V Series Regulator to produce more current through the load and thereby increase the output voltage of this supply. This places more voltage across divider R985-R986-R987 and the divider action returns the base of Q984B to about -9 volts. Notice that the feedback action of this supply forces a change in the output level which always returns the base of Q984B to the same level as the base of Q984A. In this manner, the output level of the -50-Volt Supply can be set to exactly -50 volts by correct adjustment of R986.

The -50 V Current Limiting stage Q988 protects the -50-Volt Supply if excess current is demanded from this supply. Since the ground return for the -50 Volt Supply is through R997-R998, all current from the -50-Volt Supply must flow through these resistors. Transistor Q988 senses the voltage drop across R997-R998. Under normal operation, there is about 0.3-volt drop across R997-R998 which is not sufficient to forward bias Q988. However, when excess current is demanded from the -50 V Series Regulator due to a short circuit or similar malfunction at the 3-52

output of this supply, the voltage drop across R997-R998 increases until it is sufficient to forward bias Q988. The

collector current of Q988 results in a reduction of current through Q992 and Q994 to limit the conduction of Q998. As the output voltage of this supply decreases due to current limiting, the level of the positive semi-regulated voltage increases. More current flows through R988-R989 to increase the voltage drop across R989. As a result, the bias on Q998 increases so the Series Regulator supplies less current. This current limiting protects Q998 from damage due to excess power dissipation.

Several protection diodes are also included in this circuit. CR981 prevents the output of this supply from going more positive than about +0.6 volt if it is shorted to a positive supply. CR984 protects Q984A from reverse voltage breakdown. CR991 protects transistor Q994 by disconnecting the +50-Volt Supply if it is more negative than the base of Q994, such as when the instrument is turned on, or if the +50-Volt Supply is shorted to a less positive supply. CR994 protects Q994 from reverse-voltage breakdown.

#### -15-Volt Supply

Basic operation of all stages in the -15-Volt Supply is the same as for the -50-Volt Supply. Reference level for this supply is established by divider R962-R963 between ground and the -50 V Sense voltage. The divider ratio of R962-R963 sets a level of -15 volts at the base of Q964A. The level on the -50 V Sense line is held stable by the -50 Volt Supply. Any change at the output of the -15-Volt Supply appears at the base of Q964B as an error signal. The output voltage is regulated in the same manner as described for the -50-Volt Supply. Diode CR972 insures a conduction path between the collector of -15 V Current Limiting transistor Q966 and the -15 V Series Regulator Q974 when current limiting is required. CR961 limits the output of this supply from going more positive than about +0.6 volts when it is shorted to one of the positive supplies. Diode CR964 and CR965 provide reverse-voltage protection for transistors Q964A and Q964B respectively.

#### +5-Volt Supply

Basic operation of the +5 V Series Regulator and +5 V Current Limiting stages are the same as described for the previous supplies. The +5 V Feedback Amplifier operates in the same manner as described previously except that Q948 provides inversion in the feedback path. The reference level for this supply is established by the ground connection at the base of Q944. Feedback voltage to the base of Q946 is provided by divider R946-R947 between the +5 V Sense line and the -50 V Sense line. The divider ratio of R946-R947 is 10:1 so that the base of Q946 is at zero volts when the supply is operating properly. The level on the -50 V Sense line is held stable by the -50-Volt Supply. Therefore, any change at the output of the +5-Volt Supply ®



appears at the base of Q946 as an error signal. The output voltage is regulated in the manner described previously for the -50-Volt Supply. Diode CR941 limits the output of this supply to about -0.6 volt if it is shorted to one of the negative supplies. Diode CR942 provides a current path to limit the output of the +5-Volt Supply to about +7.6 volts if this supply is shorted to the +50-Volt Supply. Diode CR948 establishes a level of about +0.6 volt at the emitter of Q948. CR949 along with the forward drop across the base-emitter junction of Q948 establishes sufficient voltage drop for correct operation of the +5 V Current Limiting stage Q954.

The output of this supply is also connected across the GRAT ILLUM control R957 through fuse F957. R957 controls the current through the graticule illumination lights DS957, DS958, DS959 to change the illumination of the graticule lines. Fuse F957 protects the +5-Volt Supply if a short-circuit condition occurs in the graticule light network.

Elapsed-time meter M941 is connected to the +5-volt output. This meter records the amount of time that this instrument has been operating. R941 establishes the current through M941 which determines the rate at which the meter records time.

#### **+15-Volt Supply**

The semi-regulated voltage applied to the +15-Volt Supply is also connected to the High-Voltage Oscillator stage in the CRT Circuit through F921. This fuse protects the +15-Volt Supply from damage due to failures in the High-Voltage Oscillator stage. The +15 V Series Regulator and +15 V Current Limiting stages operate in the same manner as described for the previous supplies. The +15 V Feedback Amplifier stage is connected in the inverting configuration. The ground connection at the base of Q922A provides the reference for this supply. Feedback voltage to the base of Q922B is provided through divider R925-R926 between the +15 V Sense line and the -50 V Sense line. The divider ratio of R925-R926 sets the base of Q922B to zero volts. Any change in the output level of the +15-Volt Supply appears at the base of Q922B as an error signal. This results in an opposite change at the collector of Q922B which is connected to the base of Q936 through zener diode VR927. This diode provides voltage-level shifting between Q922B and Q936. The change at the base of Q936 is connected to the +15 V Series Regulator stage through Q938 to correct the error in the output voltage.

Diodes CR922 and CR924 provide reverse-voltage breakdown protection for transistors Q922A and Q922B respectively. Diode CR923 protects Q922B against negative voltages when the +15-Volt Supply is shorted to ground. CR938 provides a connection between the +15 V Current Limiting stage Q954 and the +15 V Series Regulator stage Q930.

Limiting stage and the +15 V Series Regulator stage when current limiting is required. Diode CR935 disconnects the emitter circuit of Q936 from the -50-Volt Supply if the -50-Volt Supply is shorted to a positive supply.

The +5 V Voltage Limiting stage Q930 provides protection for the integrated circuits which are powered from the +5-Volt Supply if the +5-Volt and +15-Volt supplies are shorted together. The output of the +5-Volt Supply is connected across zener diode VR930 through R929 and R930. Under normal conditions, Q930 does not conduct. However, if the output of the +5-Volt Supply rises positive because it is shorted to the +15-Volt Supply, the base of Q930 is clamped at about +5.1 volts by zener diode VR930. As the output voltage of the +5-Volt Supply increases to about +5.7 volts, Q930 is forward biased and its collector current turns on the +15 V Current Limiting stage through R931. This limits the output level of the +15-Volt Supply so it drops to about +5.7 volts. Since the output level of the +15-Volt Supply is now limited, it can not pull the +5-Volt Supply more positive than about +5.7 volts.

#### **+50-Volt Supply**

Operation of the +50 V Series Regulator and the +50 V Current Limiting stages are the same as described previously for the other supplies. The +50 V Feedback Amplifier operates in the same manner as described previously except that Q910 provides inversion in the feedback path. Reference voltage for this supply is established by the ground connection at the base of Q906A. Feedback voltage to the base of Q906B is provided by divider R907-R908 between the +50 V Sense line and -50 V Sense line. The divider ratio of R907-R908 sets the base level of Q906B to zero volts when the output of this supply is correct. The protection diodes in this circuit operate similarly to the other supplies.

#### **+75 and +150-Volt Supply**

The +75-Volt and +150-Volt levels produced by the Line to DC Converter/Regulator circuit are connected to fuses F901 and F902, respectively, in this circuit. These fuses protect the Line to DC Converter/Regulator circuit if the output of these supplies is shorted.

### **CONTROLS AND CABLING**

#### **General**

Diagram 12 shows the front-panel switches and controls of the R7704 and the interconnections between these controls and the circuits within this instrument. To use the cabling diagram, note the number on the wire at the point where an individual wire joins the cable. Then follow the cable around until a break-out is found with the same number. This is the source/location of the desired wire.

## Circuit Description-R7704 READOUT SYSTEM

### Switch Logic

The VERTICAL MODE and HORIZONTAL MODE switches determine the operating mode of the Vertical Interface and Horizontal Interface circuits respectively. Each of these switches is designed so that it is self-canceling (i.e., only one button can be pressed at a time). Specific operation of these switches is described in connection with the circuits that they control.

The A TRIGGER SOURCE and B TRIGGER SOURCE switches control the operation of the Trigger Selector circuit. These switches are also self-canceling so that only one of the buttons can be pressed at a time. Operation of these switches is discussed in connection with the Trigger Selector circuit.

### Indicator Lights

The indicator lights shown in connection with the VERTICAL MODE and HORIZONTAL MODE switches indicate which mode has been selected. When one of the buttons of these switches is pressed, it completes the circuit between the associated bulb and the lamp-common line. Notice that a separate bulb is used for each mode switch position. Bulbs DS1035 and DS1037, located beside the B INTENSITY and A INTENSITY controls respectively, are actuated by the HORIZONTAL MODE switch to indicate which of the intensity controls is active for the selected horizontal mode. The selected button of the A TRIGGER SOURCE and B TRIGGER SOURCE switches is also illuminated to indicate the trigger source. Notice that only one bulb is associated with each of the trigger source switches. The source switches are mechanically designed so that the button which is pressed receives light from the bulb, but the remaining buttons remain un-illuminated.

The CONTROL ILLUM switch S1040B determines the illumination level of the pushbutton switches on the R7704 and the associated plug-in units. In the HIGH position of this switch, lamp power from the Line to DC Converter/Regulator circuit is connected directly to the light bulbs. In the LOW position, lamp power is connected to the bulbs through diodes CR1040 and CR1041. The forward drop across these diodes reduces the current available to the bulbs so they operate at a lower intensity level. In the OFF position, lamp power to all of the pushbutton switches is disconnected. However, lamp power is still connected to the bulbs associated with the A and B INTENSITY controls through CR1040 and CR1041 to provide an indication that the POWER switch is ON. Fuse F1040 protects the +5-Volt Lamp Supply if the lamp power circuit is shorted to ground.

This diagram also shows the wiring for the Camera Power Connector on the CRT bezel, the PROBE POWER connectors J1080-J1085, and the REMOTE CONTROL connector J1075.

### Introduction to Readout System

**General.** The Readout System in the R7704 provides alpha-numeric display of information encoded by the plug-in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis with the analog waveform display. Schematics for the total Readout System are shown on diagram 13, 14, and 15 at the rear of this manual.

The definitions of several terms must be clearly understood to follow this description of the Readout System. These are:

**Character-A** character is a single number, letter, or symbol which is displayed on the CRT, either alone or in combination with other characters.

**Word-A** word is made up of a related group of characters. In the R7704 Readout System, a word can consist of up to ten characters.

**Frame-A** frame is a display of all words for a given operating mode and plug-in combination. Up to eight words can be displayed in one frame. Fig. 3-37 shows one complete frame (simulated readout) and the position at which each of the eight words is displayed.

**Column-One** of the vertical lines in the Character Selection Matrix (see Fig. 3-38). Columns C-0 (column zero) to C-10 (column 10) can be addressed in the R7704 system .

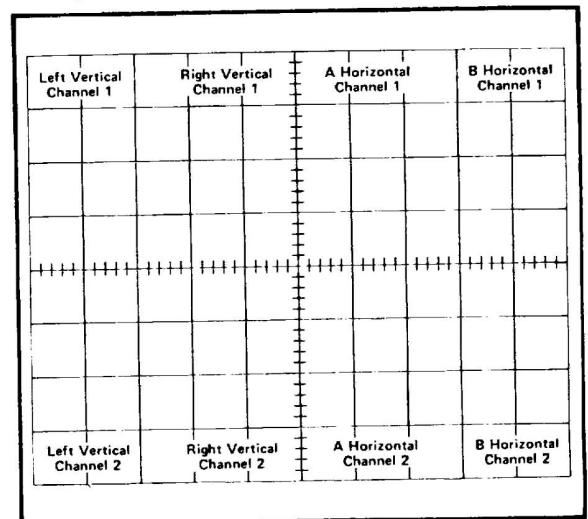


Fig. 3-37. Location of readout words on the CRT identifying the originating plug-in and channel (one complete frame shown, simulated readout).



Column Number →		C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
Row Number ↓	Current (Milli-amperes)	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	≥1.0
R-1	0	SKIP* ↑ ↓	0	1	2	3	4	5	6	7	8	9
R-2	0.1		/	<	I	/	+	-	+	C	Δ	>
R-3	0.2		Add* one zero	Add* two zeros	Reduce* prefix	Reduce* prefix and add one zero						IDENTIFY*
R-4	0.3		m	μ	n	p	X	K	M	G	T	R
R-5	0.4		S	V	A	W	H	d	B	c	Ω	E
R-6	0.5		U	N	L	Z	Y	P	F	J	Q	D
R-7	0.6				Decimal* point location No. 3	Decimal* point location No. 4	Decimal* point location No. 5	Decimal* point location No. 6	Decimal* point location No. 7			
R-8	0.7	Add Space In Display*										
R-9	0.8											
R-10	0.9											



Unused locations. Available for future expansion of Readout System

Operational address.

Fig. 3-38. Character Selection Matrix for R7704 Readout System.

Row-One of the horizontal lines in the Character Selection Matrix (Fig. 3-38). Rows R-1 (row 1) to R-10 (row 10) can be addressed in the R7704 system.

Time-Slot-A location in a pulse train. In the R7704 Readout System, the pulse train consists of 10 negative-going pulses. Each of these time-slots is assigned a number between one and ten. For example, the first time-slot is TS-1.

Time-multiplexing-Transmission of data from two or more sources over a common path by using different time intervals for different signals.

**Display Format.** Up to eight words of readout information can be displayed on the R7704 CRT. The position of each word is fixed and is directly related to the plug-in unit from which it originated. Fig. 3-37 shows the area of the graticule where the readout from each plug-in unit is displayed. Notice that channel 1 of each plug-in unit is displayed within the top division of the CRT and channel 2 is displayed directly below within the bottom division. Fig. 3-39 shows a typical display where only channel 1 of the Right Vertical and B Horizontal units is selected for display.

Each word in the readout display can contain up to 10 characters, although the typical display will contain between two and seven characters per word. The characters are selected from the Character Selection Matrix shown in Fig. 3-38. Any one of the 50 separate characters can be addressed and displayed on the CRT. In addition, 12 operational addresses are provided for special instructions to the

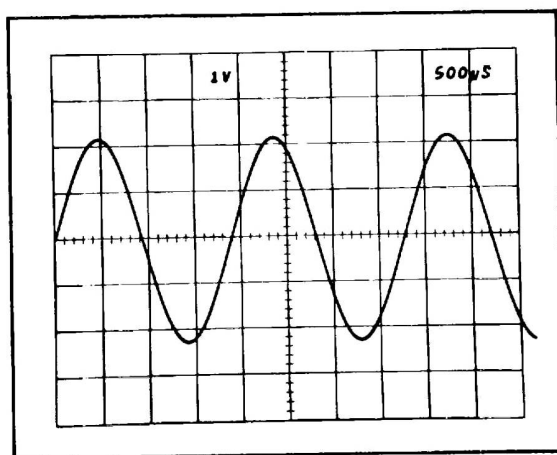


Fig. 3-39. Typical readout display where only channel 1 of the Right Vertical and B Horizontal units is displayed.

### Circuit Description-R7704

3-56 Readout System. The unused locations in the Matrix (shaded area) are available for future expansion of the Readout System. The method of addressing the locations in the Character Selection Matrix is described in the following discussion.

**Developing the Display.** The following basic description of the Readout System uses the block diagram shown in Fig. 3-40. This description is intended to relate the basic function of each stage to the operation of the overall Readout System. Detailed information on circuit operation is given later.

The key block in the Readout System is the Timer stage. This stage produces the basic signals which establish the timing sequences within the Readout System. Period of the timing signal is about 250 microseconds (drops to about 210 microseconds when Display-Skip is received; see detailed description of Timing stage for further information). This stage also produces control signals for other stages within this circuit and interrupt signals to the Vertical Interface, Horizontal Interface, CRT Circuit, and Z-Axis Logic stage which allow a readout display to be presented.

The Time-Slot Counter stage receives a trapezoidal voltage signal from the Timer stage and directs it to one of ten output lines. These output lines are labeled TS-1 through TS-10 (time-slots one through ten) and are connected to the vertical and horizontal plug-in compartments as well as to various stages within the Readout System. The output lines are energized sequentially so there is a pulse on only one of the 10 lines during any 250 microsecond timing period. When the Time-Slot Counter stage has completed time-slot 10, it produces an End-of-Word pulse which advances the system to the next channel.

Two output lines, row and column, are connected from each channel of the plug-in unit back to the Readout System. Data is typically encoded on these output lines by connecting resistors between them and the time-slot input lines. The resultant output is a sequence of ten analog current levels which range from zero to one milliamper (100 microamperes/step) on the row and column output lines. This row and column correspond to the row and column of the Character Selection Matrix in Fig. 3-38. The standard format in which information is encoded onto the output lines is given in Table 3-2 (special purpose plug-in units may have their own format for readout; these special formats will be defined in the manuals for these units).

The encoded column and row data from the plug-in units is selected by the Column Data Switch and Row Data Switch stages respectively. These stages take the analog currents from the eight data lines (two channels from each of the four plug-in compartments) and produce a single time multiplexed analog voltage output which contains all of the

**TABLE 3-2**  
**Standard Readout Format**

Time-Slot Number	Description
TS-1	Determines decimal magnitude (number of zeros displayed or prefix change information) or the IDENTIFY function (no display during this time-slot).
TS-2	Indicates normal or inverted input (no display for normal).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control (no display for calibrated condition).
TS-4	1-2-5 scaling.
TS-5 TS-6 TS-7 TS-8	Not encoded by plug-in unit. Left blank to allow addition of zeros by Readout System. Defines the prefix which modifies
TS-9 TS-10	the units of measurement. Define the units of measurement of the plug-in unit. May be standard units of measurement (V, A, S, etc.) or special units selected from the Character Selection Matrix.

column or row information from the plug-ins. The Column Data Switch and Row Data Switch are sequenced by the binary Channel Address No. 1 code from the Channel Counter.

The time multiplexed output of the Column Data Switch is monitored by the Display-Skip Generator to determine if it represents valid information which should be displayed. Whenever information is not encoded in a timeslot, the Display-Skip Generator produces an output level to prevent the Timer stage from producing the control signals which normally interrupt the CRT display and present a character.

The analog outputs of the Column Data Switch and Row Data Switch are connected to the Column Decoder and Row Decoder stages respectively. These stages sense the magnitude of the analog voltage input and produce an output current on one of ten lines. The outputs of the Column Decoder stage are identified as C-1 to C-10 (column 1 to 10) which correspond to the column information encoded by the plug-in unit. Likewise, the outputs of the Row De®

coder stage are identified as R-1 to R-10 (row 1 to 10) which correspond to the row information encoded by the plug-in unit. The primary function of the row and column outputs is to select a character from the Character Selection Matrix to be produced by the Character Generator stage. However, these outputs are also used at other points within the system to indicate when certain information has been encoded. One such stage is the Zeros Logic and Memory. During time-slot 1 (TS-1), this stage checks if zero-adding or prefix-shifting information has been encoded by the plug-in unit and stores it in memory until time-slots 5, 6, or 8. After storing this information, it triggers the Display Skip Generator stage so there is no display during this time-slot (as defined by Standard Readout Format; see Table 3-2). When time-slots 5, 6, and 8 occur, the memory is addressed and any information stored there during time-slot 1 is transferred out and connected to the input of the Column Decoder stage to modify the analog data during the applicable time-slot.

Another operation of the Zeros Logic and Memory stage is to produce the IDENTIFY function. When time-slot 1 is encoded for IDENTIFY (column 10, row 3), this stage produces an output level which connects the Column Data Switch and Row Data Switch to a coding network within the Readout System. Then, during time-slots 2 through 9, an analog current output is produced from the Column Data Switch and Row Data Switch which addresses the correct points in the Character Selection Matrix to display the word "IDENTIFY" on the CRT. The Zeros Logic and Memory stage is reset after each word by the Word Trigger pulse.

The Character Generator stage produces the characters which are displayed on the CRT. Any of the 50 characters shown on the Character Selection Matrix of Fig. 3-37 can be addressed by proper selection of the column and row current. Only one character is addressable in any one timeslot; a space can be added into the displayed word by the Decimal Point Logic and Character Position Counter stage when encoded by the plug-in. The latter stage counts how many characters have been generated and produces an output current to step the display one character position to the right for each character. In addition, the character position is advanced once during each of time-slots 1, 2, and 3 whether a character is generated during these time-slots or not. This action fixes the starting point of the standard format display such that the first digit of the scaling factor always starts at the same point within each word regardless of the information encoded in time-slot 2 (normal/invert) or time-slot 3 (cal/uncal) which precedes this digit. Also, by encoding row 10 and column 0 during any time-slot, a blank-space can be added to the display. Decimal points can be added to the display at any time by addressing row 7 and columns 3 through 7 (see Character Selection Matrix for location of these decimal points). The Decimal Point Logic and Character Position Counter stage is reset after each word by the Word Trigger pulse.

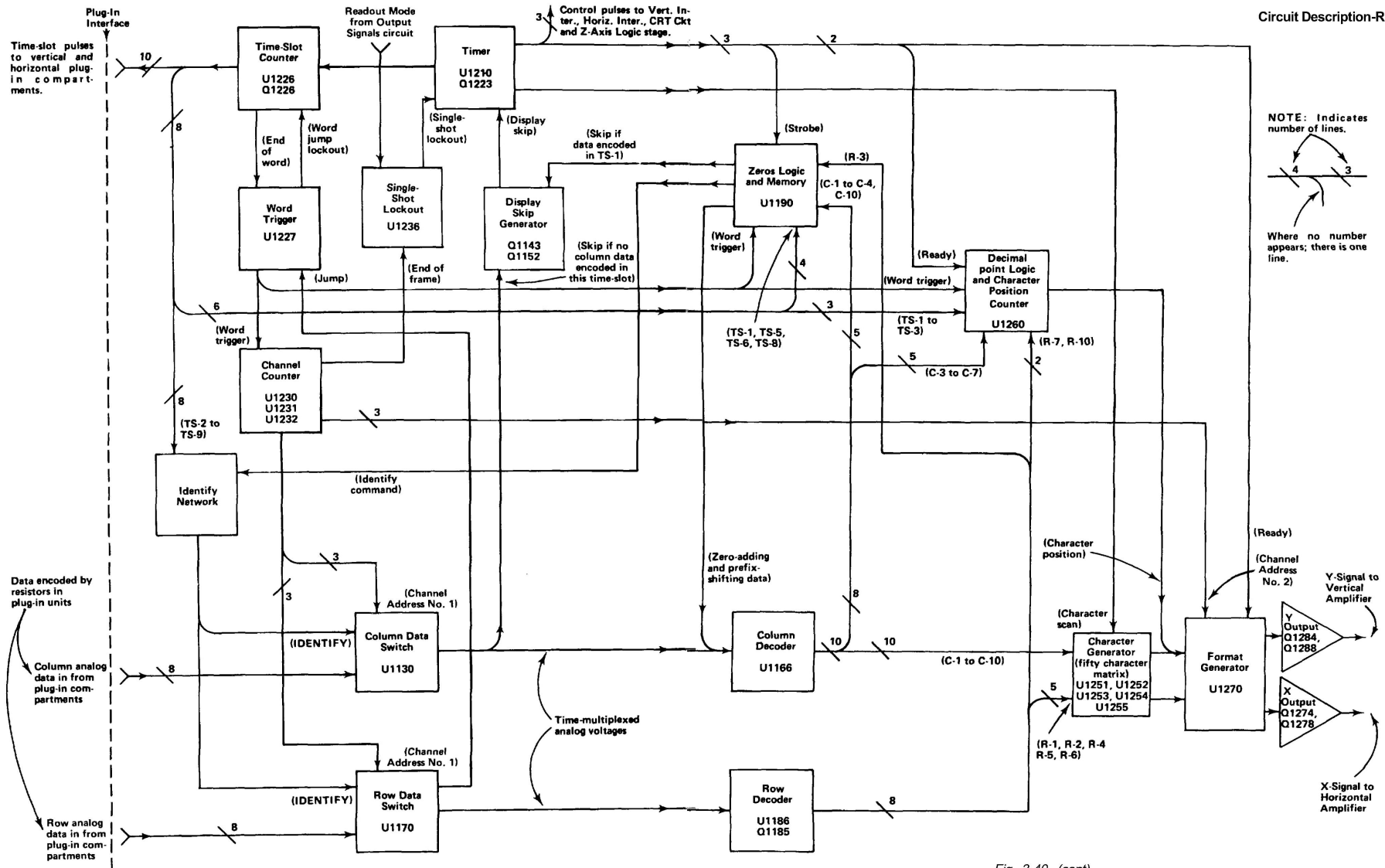


Fig. 3-40. Detailed block diagram of Readout System.

Fig. 3-40. (cont).

The Format Generator stage provides the output signals to the vertical and horizontal deflection systems of the instrument to produce the character display. The binary Channel Address No. 2 code from the Channel Counter stage is connected to this stage so the display from each channel is positioned to the area of the CRT which is associated with the plug-in and channel originating the word (see Fig. 3-36). The positioning current or decimal point location current generated by the Decimal Point Logic and Character Position Counter stage is added to the horizontal (X) signal at the input to the Format Generator stage to provide horizontal positioning of the characters within each word. The X and Y-output signals are connected to the Horizontal Amplifier and Vertical Amplifier through the Horizontal Output and Vertical Output stages respectively.

The Word Trigger stage produces a trigger from the End-of-Word pulse generated by the Time-Slot Counter stage after the tenth time-slot. This Word Trigger pulse advances the Channel Counter to display the information from the next channel or plug-in. It also provides a reset pulse to the Zeros Logic and Memory stage and the Decimal Point Logic and Character Position Counter stage. The Word Trigger stage can also be advanced to jump a complete word or a portion of a word when a Jump command is received from the Row Decoder stage.

The Single-Shot Lockout stage allows the display sequence of the Readout System to be changed. Normally, the Readout System operates in a free-running mode so the waveform display is interrupted randomly to display characters. However, under certain conditions (such as single shot photography), it is desirable that the Readout System operate in a triggered mode where the readout portion of the display is normally blanked out, but can be presented on command. The Readout Mode input from the Output Signals circuit determines the operating mode of the readout system.

### Circuit Analysis of Readout System

The following analysis of the Readout System discusses the operation of each stage in detail. Complete schematics of the Readout System are shown on diagram 13, 14, and 15 at the rear of this manual.

### Timer

Timer U1210 establishes the timing sequence for all circuits within the Readout System. This stage produces seven time-related output waveforms (see Fig. 3-41). The triangle waveform produced at pin 6 forms the basis for the remaining signals. The basic period of this triangle waveform is about 250 microseconds as controlled by RC network C1214-R1214. The triangle waveform is clipped and amplified by U1210 to form the trapezoidal output signal

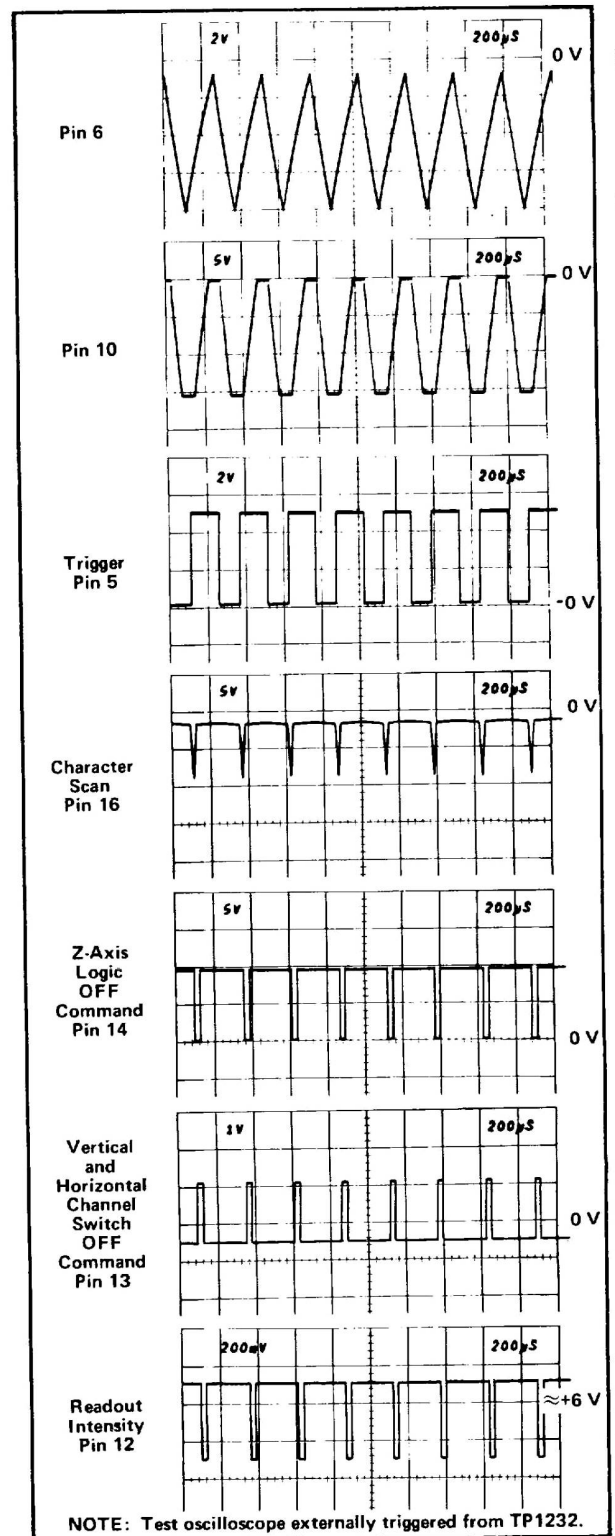


Fig. 3-41. Output waveforms of Timer stage.



at pin 10. The amplitude of this output signal is exactly 15 volts as determined by U1210 (exact amplitude necessary to accurately encode data in plug-in units; see Encoding the Data). The Trigger output at pin 5 provides the switching signal for the Time-Slot Counter and Word Trigger stages.

The signals at pins 12, 13, 14, and 16 are produced only when the triangle waveform is on its negative slope and the trapezoidal waveform has reached the lower level. The timing sequence of these waveforms is very important to the correct operation of the Readout System (see expanded waveforms in Fig. 3-42). The Z-Axis Logic OFF Command at pin 14 is produced first. This negative-going signal provides a blanking pulse to the Z-Axis Logic stage (see diagram 2) to blank the CRT before the display is switched to the Readout System. It also produces the Strobe pulse through R1221, Q1223, and CR1224 to signal other stages within the Readout System to begin the sequence necessary to produce a character. The collector level of Q1223 is also connected to Character Generator No. 2, U1252, through C1222-CR1222. This activates U1252 during the quiescent period of the Strobe pulse (collector of Q1223 negative) and diverts the output current of Row Decoder U1186 to row 2. The purpose of this configuration is to prevent the

Zeros Logic and Memory stage U1190 from storing incorrect data during the quiescent period of the Strobe pulse. When the Strobe pulse goes positive, CR1222 is reverse biased to disconnect Q1223 from U1252 and allow the Row Decoder to operate in the normal manner.

The next signal to be produced is the Vertical/Horizontal Channel Switch OFF Command at pin 13. This positive-going signal disconnects the plug-in signals in the vertical and horizontal deflection systems so the plug-in units do not control the position of the CRT beam during the readout display. The Ready signal derived from this output is connected to the Decimal Point Logic and Character Position Counter stage and the Format Generator stage (see diagram 15). The Readout Intensity output at pin 12 is produced next. This current is connected to the CRT Circuit to unblank the CRT to the intensity level determined by READOUT intensity control R1040. The Character Scan ramp at pin 16 started to go negative as this timing sequence began. However, character-generation does not start until the readout intensity level has been established. The triangular Character Scan ramp runs negatively from about -2 volts to about -8.5 volts and then returns back to the original level. This waveform provides the scanning signal for the Character Generator stages (see diagram 15). Full Character Scan adjustment R1219 sets the DC level of the Character Scan ramp to provide complete characters on the display.

The Timer stage operates in one of two modes as controlled by the Display-Skip level at pin 4. The basic mode just described is a condition which does not occur unless all ten characters of each word (80 characters total) are displayed on the CRT. Under typical conditions only a few characters are displayed in each word. The Display-Skip level at pin 4 determines the period of the Timer output signal. When a character is to be generated, pin 4 is LO and the circuit operates as just described. However, when a character is not to be displayed, a HI level is applied to pin 4 of U1210 through CR1207 from the Display-Skip Generator stage (diagram 14). This signal causes the Timer to shorten its period of operation to about 210 microseconds. The waveforms in Fig. 3-43 show the operation of the Timer stage when the Display-Skip condition occurs for all positions in a word. Notice that there is no output at pins 12, 13, 14, and 16 under this condition. This means that the CRT display is not interrupted to display characters. Also notice that the triangle waveform at pin 6 does not go as far negative and that the negative portion of the trapezoidal waveform at pin 10 is shorter. Complete details on operation of the Display-Skip Generator are given later.

The Single-Shot Lockout level at pin 2 also controls the operation of U1210. If this level is LO, the Timer operates as just described. However, if the Single-Shot Lockout stage sets a HI level at this pin, the Timer-stage is locked out and can not produce any output signals (see Single-Shot Lockout description for further information).

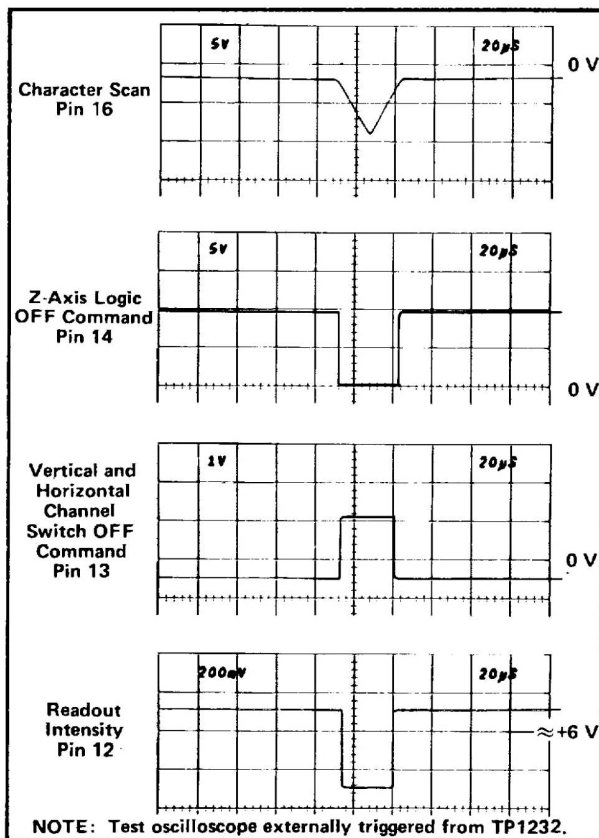


Fig. 3-42. Detail of output at pins 12, 13, 14, and 16 of U1210.

### Circuit Description-R7704

READOUT intensity control R 1040 sets the intensity of the readout display independently of the A or B INTENSITY controls. The READOUT intensity control also provides a means of turning the Readout System off when a readout display is not desired. When R 1040 is turned fully counterclockwise, switch S1040 opens. The current to pin 11 of U1210 is interrupted and at the same time a positive voltage is applied to pin 4 through R1206 and CR1206. This positive voltage switches the stage to the same conditions as were present under the Display-Skip condition. Therefore, the CRT display is not interrupted to present characters. However, time-slot pulses continue to be generated.

### Time-Slot Counter

Time-Slot Counter U1226 is a sequential switch which directs the trapezoidal waveform input at pin 8 to one of its 10 output lines. These time-slot pulses are used to interrogate the plug-in units to obtain data for the Readout System. The Trigger pulse at pin 15 switches the Time-Slot Counter to the next output line; the output signal is sequenced consecutively from time-slot 1 through time-slot 10. Fig. 3-44 shows the time-relationship of the time-slot pulses. Notice that only one of the lines carries a time-slot pulse at any given time. When time-slot 10 is completed, a negative-going End-of-Word pulse is produced at pin 2. The End-of-Word pulse provides a drive pulse for the Word Trigger stage and also provides an enabling level to the Display Skip Generator during time-slot 1 only.

Pin 16 is a reset input for the Time-Slot Counter. When this pin is held LO, the Time-Slot Counter resets to timeslot 1. The Time-Slot Counter can be reset in this manner only when a Jump Command is received by U1227A (see following discussion).

### Word Trigger

The Word Trigger stage is made up of the 4 two-input NOR gates contained in U1227. Quiescently, pin 2 of U1227C is LO as established by the operating conditions of U1227A-U1227B. Therefore, the LO End-of-Word pulse produced by the Time-Slot Counter results in a HI level at pin 1 of U1227C. This level is inverted by U1227D to provide a negative-going advance pulse to the Channel Counter.

An advance pulse is also produced by U1227D when a Jump Command is received at pin 8 of U1227A. This condition can occur during any time-slot (see Row Decoder for further information on origin of the Jump Command). U1227A and U1227B are connected as a bistable flip-flop. The positive-going Jump Command at pin 8 of U1227A produces a LO at pin 10. This LO is inverted by U1227B to produce a HI at pin 13 which allows pin 9 of U1227A to be pulled HI through R1227. The flip-flop has now been set

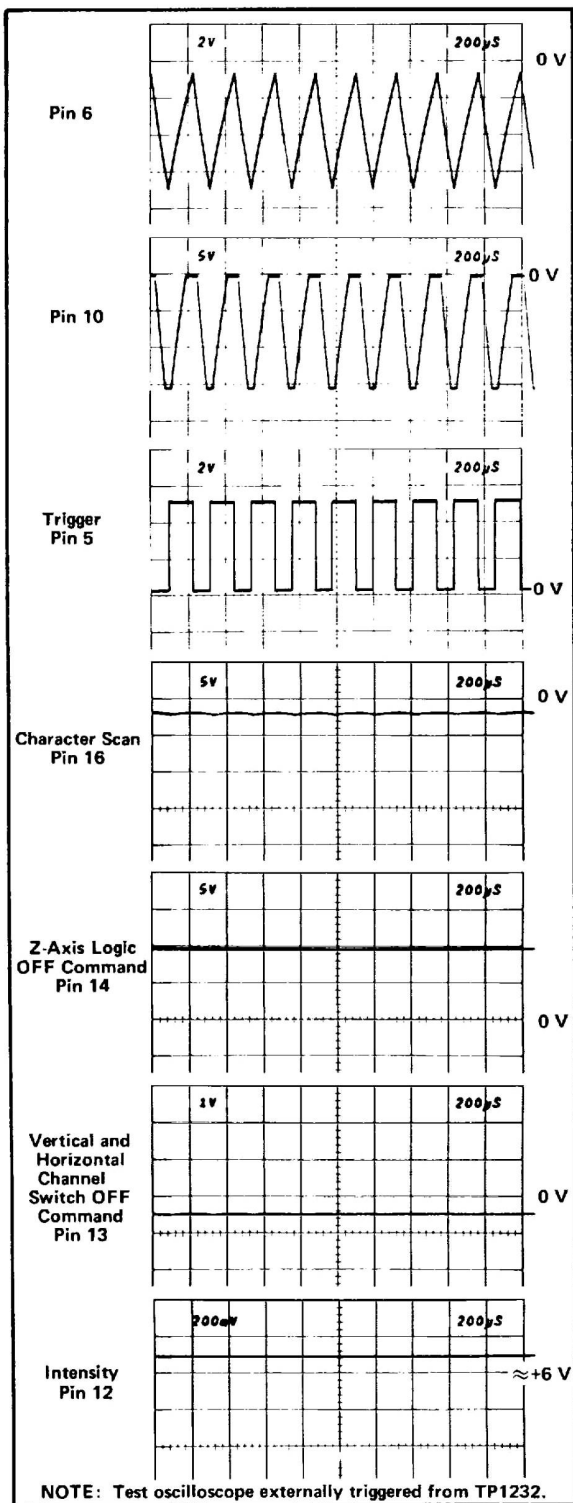


Fig. 3-43. Timer stage operation when Display-Skip condition occurs.



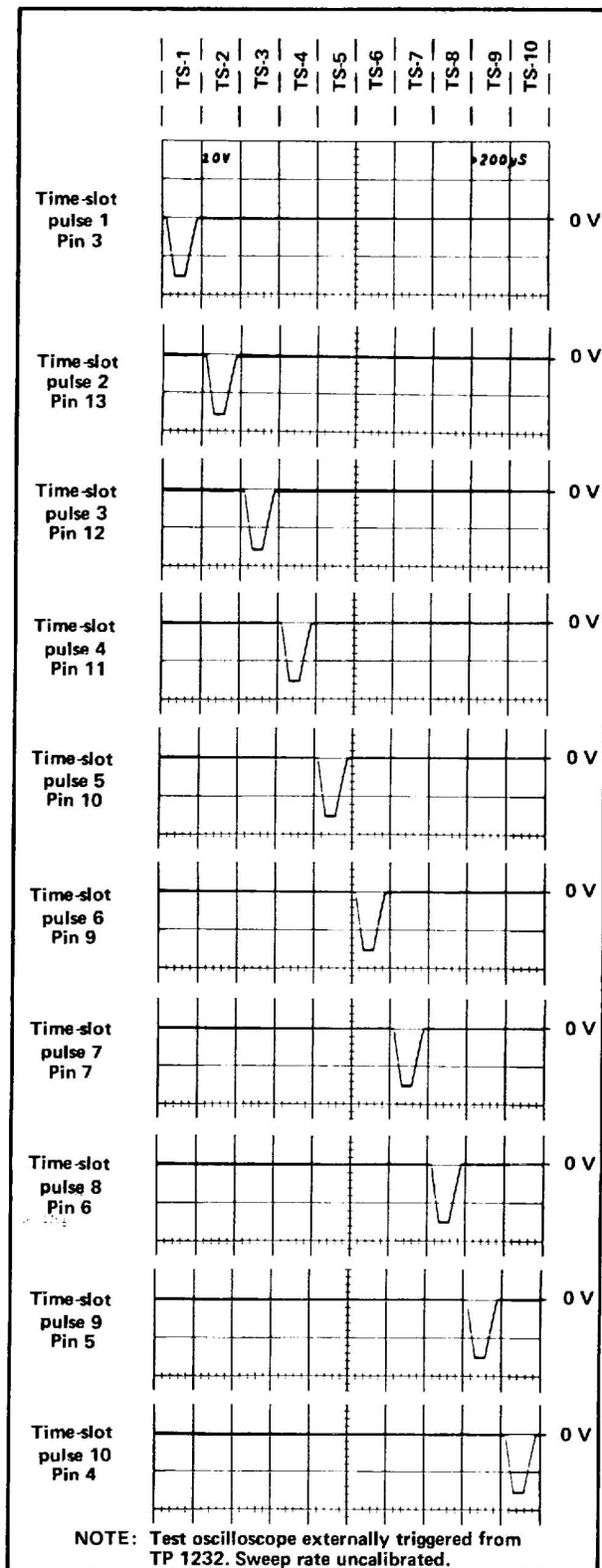


Fig. 3-44. Time relationship of the time-slot (TS) pulses produced by U1226.

and it remains in this condition until reset, even though the Jump Command at pin 8 returns to its LO level. The HI output level at pin 13 turns on Q1226 through R1226 to pull pin 16 of the Time-Slot Counter LO. This resets the Time-Slot Counter to time-slot 1 and holds it there until U1227 is reset. At the same time, a HI level is applied to pin 4 of the Timer through CR1208 and CR1207. This HI level causes the Timer to operate in the display-skip mode so that a character is not generated.

The next Trigger pulse is not recognized by the Time Slot Counter, since U1226 is locked in time-slot 1 by U1227. However, this Trigger pulse resets the Word Trigger stage through C1227. Pin 13 of U1227B goes LO to enable the Time-Slot Counter and Timer stages for the next timeslot pulse. At the same time, the negative-going edge produced as U1227B switches output states is connected to pin 2 of U1227C. This results in a negative-going Word Trigger output at pin 4 of U1227D to advance the Channel Counter to the next word. When the next Trigger pulse is received at pin 15, the Time-Slot Counter returns to the normal sequence of operation and produces an output on the timeslot 1 line.

#### Channel Counter

The Channel Counter, made up of integrated circuits U1230-U1231-U1232 is a binary counter which produces the Channel Address code for the Column and Row Decoder stages (diagram 14) and the Format Generator stage (diagram 15). This code instructs these stages to sequentially select and display the eight channels of data from the plug-ins. The input channel which is displayed with each combination of the Channel Address code is given in the discussion for the applicable stages.

#### Single-Shot Lockout

U1236 makes up the Single-Shot Lockout stage. This stage allows a single readout frame (eight complete words) to be displayed on the CRT, after which the Readout System is locked out so further readout displays are not presented until the circuit is reset. U1236A and U1236B are connected to form a bistable flip-flop. For normal operation, pin 3 of U1236A is pulled HI through R1235. This activates U1236A to result in a LO output level at pin 6 which enables the Timer stage so it can operate in the free-running manner as described previously. The LO at pin 6 of U1236A is also applied to pin 2 of U1236B. Since pin 1 is LO due to the ground connection through R1237. U1236B is disabled and its output goes HI.

The output of this stage remains LO to allow U1210 to operate in the free-running mode until a LO is received at pin 3 of U 1236A. When this occurs, the output level at pin 6 of U1236A does not change immediately. However, the Readout System is now enabled as far as the single-shot

lockout function is concerned. If the Channel Counter has not completed word eight (channel 2 of B Horizontal unit), the Readout System continues to operate in the normal manner. However, when word eight is completed, the positive-going End-of-Frame pulse is produced at pin 5 of U1232 as the Channel Counter shifts to the code necessary to display word one. This pulse is coupled to pin 1 of U1236B through C1237. The momentary HI at pin 1 activates U1236B and its output goes LO to disable U1236A (pin 3 already LO). The output of U1236A goes HI to disable the Timer so it operates in the display-skip mode. The HI at pin 6 of U1236A also holds U1236B enabled so it maintains control of the flip-flop.

The Single-Shot Lockout stage remains in this condition until a positive-going trigger pulse is applied to pin 3 of U1236A. This trigger pulse produces a LO at pin 6 of U1236A which enables U1210 and disables U1236B. Now, the Timer can operate in the normal manner for another complete frame. When word eight is completed, the Channel Counter produces another End-of-Frame pulse to again lock out the Timer stage.

For further information on the Readout Mode, see the Output Signals description.

### Encoding the Data

Data is conveyed from the plug-in units to the Readout System in the form of an analog code having up to 11 current levels (from zero to one milliampere in 100 microampere steps). The characters which can be selected by the encoded data are shown on the Character Selection Matrix (see Fig. 3-38). Each character requires two currents to define it; these currents are identified as the column current and the row current which correspond to the column and row of the matrix. The column and row data is encoded by resistive programming in the plug-in units. Fig 3-45 shows a typical encoding scheme for a voltage-sensing amplifier plug-in unit. Notice that the 10 time-slot (TS) pulses produced by the Time-Slot Counter stage are connected to the plug-in unit. However, time-slots 5, 6, 7, and 10 are not used by the plug-in unit to encode data when using the Standard Readout Format (see Table 3-2 for Standard Readout Format) The amplitude of the time-slot pulses is

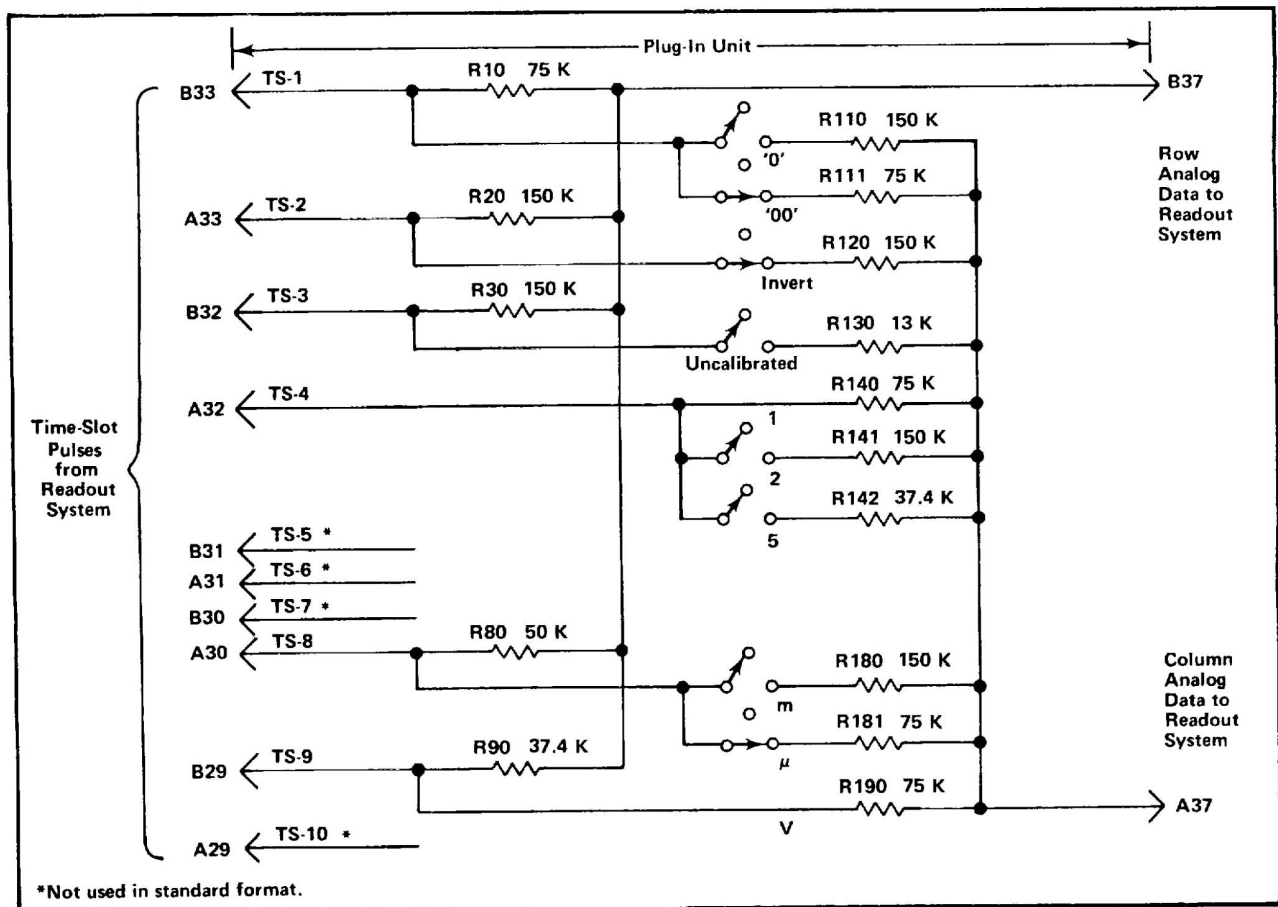


Fig. 3-45. Typical encoding scheme for voltage-sensing plug-in unit. Coding shown for deflection factor of 100 microvolts.

exactly -15 volts as determined by the Timer stage. Therefore, the resultant output current from the plug-in units can be accurately controlled by the programming resistors in the plug-in units.

For example, in Fig. 3-45 resistors R10 through R90 control the row analog data which is connected back to the Readout System. These resistors are of fixed value and define the format in which the information will be presented by the Readout System. Fig. 3-46A shows an idealized output current waveform of row analog data which results from the 10 time-slot pulses. Each of the steps of current shown in these waveforms corresponds to 100 microamperes of current. The row numbers on the left-hand side of the waveform correspond to the rows in the Character Selection Matrix shown in Fig. 3-38. The row analog data is connected back to the Readout System via terminal B37 of the plug-in interface.

The Column analog data is defined by resistors R110 through R190. The program resistors are connected to the

indicates a 100 microvolt sensitivity with the CRT display inverted and calibrated vertical deflection factors. This results in the idealized output current waveforms shown in Fig. 3-46B at the column analog data output, terminal A37 of the plug-in interface. Resistor R 111, connected between time-slot 1 and the column analog data output, encodes two units of current during time-slot 1. Referring to the Character Selection Matrix, two units of column current along with the two units of row current encoded by resistor R100 (row 3) indicates that two zeros should be added to the display. Resistor R120 adds one unit of column current during time-slot 2 and along with the one unit of current from the row output, the Readout System is instructed to add an invert arrow to the display. Resistor R130 is not connected to the time-slot 3 line since the vertical deflection factors are calibrated. Therefore, there is no column current output during this time-slot and there is no display on the CRT (see Display-Skip Generator for further information). During time-slot 4, two units of column current are encoded by R140. There is no row current encoded during this time-slot and this results in the numeral 1 being displayed on the CRT. Neither row nor column analog data is encoded during time-slots 5, 6, and 7 as defined by the Standard Readout Format. During time-slot 8, two units of column current and three units of row current are encoded by resistors R181 and R80 respectively. This addresses the p prefix in the Character Selection Matrix. The final data output is provided from time-slot 9 by R190 connected to the column output and R90 to the row output. These resistors encode three units of column current and four units of row current to cause a V (volts) to be displayed. Time-slot 10 is not encoded in accordance with the Standard Readout Format. The resultant CRT readout will be  $\downarrow 100 \mu V$ .

In the above example, the row analog data was programmed to define which row of the Character Selection Matrix was addressed to obtain information in each time-slot. The column data changes to encode the applicable readout data as the operating conditions change. For example, if the variable control of the plug-in unit was activated, R130 would be connected between time-slot 3 and the column analog data output lines. This encodes 10 units of column current (see shaded area in time-slot 3 of the waveform shown in Fig. 3-46B). Since one unit of row current is also encoded during this time-slot by R30, a> symbol is added to the display. The CRT readout will now show  $\downarrow > 100 \mu V$ . In a similar manner, the other switches can change the encoded data for the column output and thereby change the readout display. See the descriptions which follow for decoding this information.

The column analog data encoded by the plug-in unit can be modified by attenuator probes connected to the input connectors of vertical plug-in units. A special coding ring around the input connector of the plug-in unit senses the attenuation ratio of the probe (with readout-coded probes

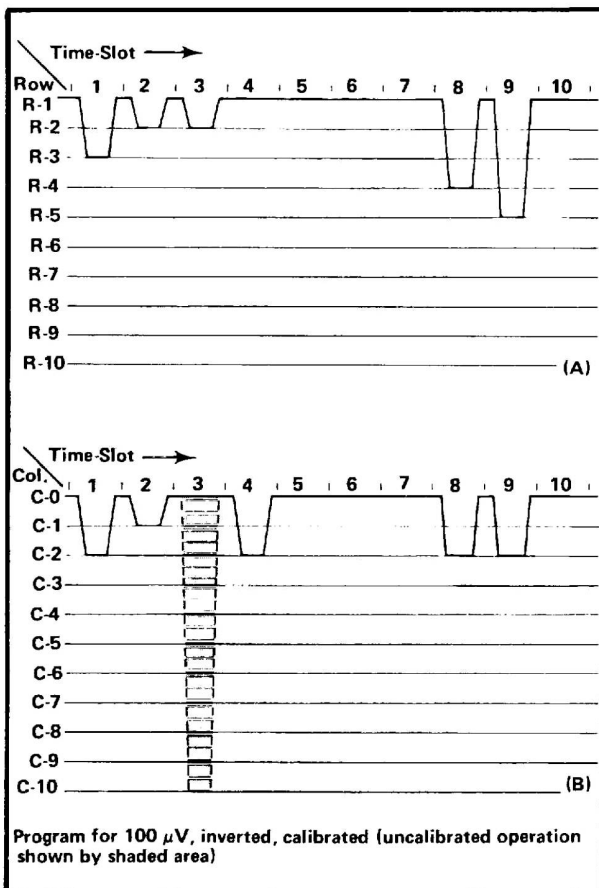


Fig. 3-46. Idealized current waveforms of: (A) Row analog data, (B) Column analog data.

time-slot lines by switch closures to encode the desired data. The data as encoded by the circuit shown in Fig. 3-45 (A)

only). The probe contains a resistor which results in additional column current. For example, if a 10X attenuator probe is connected to a plug-in with the coding for 100 microvolts as shown in Fig. 3-45, an additional unit of current is added to the column analog data during time-slot 1. Since two units of current were encoded by R 111 (see Fig. 3-45), this additional current results in a total of three units of column analog current during this time-slot. Referring to the Character Selection Matrix, three units of column analog current during this time-slot. Referring to the Character Selection Matrix, three units of column current along with the two units of row current encoded by R10 indicates that the prefix should be reduced. Since this instruction occurs in the same time-slot which previously indicated that two zeros should be added to the display and only one instruction can be encoded during a time-slot, the zeros do not appear in the display. The CRT readout will now be changed to 1 mV (readout program produced by plug-in same as for previous example).

Likewise, if a 100X readout-coded probe is connected to the input of the plug-in unit, the column current during time-slot 1 will be increased two units for a total of four units of column current. This addresses an instruction in the Character Selection Matrix which reduces the prefix and adds one zero to the display. The resultant CRT readout with the previous program is 10 mV.

Three other lines of information are connected from the plug-in compartments to the Readout System. The column and row analog data from channel 2 of a dual-channel plug-in are connected to the Readout System through terminals A38 and B38 of the plug-in interface, respectively. Force readout information is encoded on terminal A35; function of this input is described under Column and Row Data Switches.

The preceding information gave a typical example of encoding data from an amplifier plug-in unit. Specific encoding data and circuitry is shown in the individual plug in unit manuals.

Column and Row Data Switches

The readout data from the plug-in units is connected to the Column and Row Data Switch stages (Diagram 14). A column-data line and a row-data line convey analog data from each of the eight data sources (two channels from each of the four plug-in compartments).

The Column Data Switch U1130 and the Row Data Switch U1170 receive the Channel Address No. 1 code from the Channel Counter. This binary code directs the Column Data Switch and the Row Data Switch as to which channel should be the source of the readout data. Table 3-3

®

TABLE 3-3  
Channel Address No. 1 Code

Pin 1 U1190 "Identify" Command	Pin 5 U1232	Pin 5 U1231	Pin 5 U1230	Channel Selected
HI	HI	HI	HI	Channel 1 Left Vertical
HI	HI	HI	LO	Channel 2 Left Vertical
HI	HI	LO	HI	Channel 1 Right Vertical
HI	HI	LO	LO	Channel 2 Right Vertical
HI	LO	HI	HI	Channel 1 A Horizontal
HI	LO	HI	LO	Channel 2 A Horizontal
HI	LO	LO	HI	Channel 1 B Horizontal
HI	LO	LO	LO	Channel 2 B Horizontal
LO	Φ	Φ	Φ	IDENTIFY

(Φ= Has no effect in this case.

gives the eight combinations of the Channel Address No. 1 code and the resultant channel which is selected with each combination. These stages have nine inputs and provide a single time-multiplexed output at pin 7 which includes the information from all of the input channels. Eight of the nine inputs to each stage originate in the plug-in units; the ninth input comes from a special data-encoding network composed of resistors R1131 through R1138 and R1171 through R1178 (see Zeros Logic and Memory description for further information on ninth channel).

In addition to the data inputs from the plug-in units, channel-inhibit inputs are provided from each of the plug-in units. The channel inhibit lines are LO only when the associated plug-in unit has been selected for display. When a plug-in unit is not selected, the respective line is HI which forward basis the associated diode CR1112, CR1113, CR1117, CR1118, CR1122, CR1123,CR1127, orCR1128 to bypass the encoded data from this plug-in unit. However, since it may be desired to display information from special purpose plug-in units even though they do not produce a normal waveform display on the CRT, a feature is provided to over-ride the channel inhibit. This is done by applying a LO to the associated forcing over-ride input. The LO level diverts the HI channel inhibit current and allows the data from this plug-in unit to reach the Column Data Switch, even though it has not been selected for display by the mode switches.

### Display-Skip Generator

The Display-Skip Generator, Q1143-Q1150-Q1152Q1155, monitors the time-multiplexed column data at the output of the Column Data Switch during each time-slot to determine if the information at this point is valid data which should result in a CRT display. The voltage at the base of Q1143B is set by divider CR1141-R1146-R1147R1148. Quiescently, there is about 100 microamperes of current flowing through R1141 from Q1163 and the Zeros Logic and Memory stage (purpose of this quiescent current will be discussed in connection with the Zeros Logic and Memory stage). This current biases Q1143A so its base is about 0.2 volt more positive than the base of Q1143B in the absence of column data. Therefore, since Q1143A and Q1143B are connected as a comparator, Q1143A will remain on unless its base is pulled more negative than the base of Q1143B. The analog data output from the Column Data Switch produces a 0.5-volt change at the base of Q1143A for each unit of column current that has been encoded by the plug-in unit. Therefore, whenever any information appears at the output of the Column Data Switch, the base of Q1143A is pulled more negative than the base of Q1143B, resulting in a negative (LO) Display Skip output to the Timer stage through Q1155. Recall that a LO was necessary at the skip input of the Timer so it could perform the complete sequence necessary to display a character.

Q1150-Q1152 also provide display-skip action. The Endof-Word level connected to their emitters through R1152 is LO only during time-slot 1. This means that Q1150-Q1152 are enabled only during time-slot 1. These transistors allow the Zeros Logic and Memory stage to generate a displayskip signal during time-slot 1 when information has been stored in memory which is not to be displayed on the CRT (further information given under Zeros Logic and Memory discussion).

### Column and Row Decoder

The Column Decoder U1166 and Row Decoder U1186 sense the magnitude of the analog voltages at their inputs and produce a binary output on one of ten lines corresponding to the column or row data which was encoded by the plug-in unit. These outputs provide the Column Digital Data and Row Digital Data which is used by the Character Generator stages to select the desired character for display on the CRT. The column and row data is also used throughout the Readout System to perform other functions. The input current at pin 9 of the Column Decoder stage is steered to only one of the ten Column Digital Data outputs. The size of the character which will be displayed on the CRT is determined by the value of R 1156. When a display skip signal is present (collector of Q1155 HI), pin 9 is pulled HI through CR1155. This ensures that no current is connected to the Character Generator stage under this condition. Notice the corresponding input on the Row Decoder. This input is connected to ground and causes only one of the ten row outputs to saturate to ground.

The network at the input of the Row Decoder, made up of Q1185 and its associated components, is a Row 13 detector which produces the Jump Command. This row current is encoded by special-purpose plug-ins to cause all or part of a word to be jumped. Whenever row 13 (thirteen units of row current; 1.3 milliamperes) is encoded, the base of Q1185 is pulled negative enough so that this transistor is reverse biased to produce a Hi Jump Command output at its collector. This Jump Command is connected to the Word Trigger stage (diagram 13) to advance the Channel Counter to the next word and to reset the Time-Slot Counter to time-slot 1.

### Zeros Logic and Memory

The Zeros Logic and Memory stage U1190 stores data encoded by the plug-in units to provide zeros-adding and prefix-shifting logic for the Readout System. The Strobe pulse at pin 15 goes positive when the data has stabilized and can be inspected. This activates the Zeros Logic and Memory stage so it can store the encoded data. A block representation of the memory sequence is shown in Fig. 3-47. Typical output waveforms for the five possible input conditions that can occur are shown in Fig. 3-48. When time-slot 1 occurs, a store command is given to all of the memories. If the plug-in unit encoded data for column 1, 2, 3, 4, or 10 during time-slot 1, the appropriate memory (or memories) is set. Notice that row 3 information from the Row Decoder must also be present at pin 16 for data to be stored in the memory of U1190. If data was encoded during time-slot 1, a negative-going output is produced at pin 7 as the memories are being set. This negative-going pulse is connected to the base of Q1152 in the Display-Skip Generator to produce a Display-Skip output. Since the information that was encoded during time-slot 1 was only provided to set the memories and was not intended to be displayed on the CRT at this time, the display-skip output prevents a readout display during this time-slot.

During time-slot 5, memory A is interrogated. If information was stored in this memory, a positive-going output is produced at pin 7. This pulse is connected to pin 10 of the Column Decoder through Q1163 to add one unit of current at the input of the Column Decoder. This produces a zero after the character displayed on the CRT during time-slot 4. During time-slot 6, memory B is interrogated to see if another zero should be added. If another zero is necessary, a second positive output is produced at pin 7 which again results in a column 1 output from the Column Decoder and a second zero in the CRT display.

Finally, memory C is interrogated during time-slot 8 to obtain information on whether the prefix should be reduced or left at the value which was encoded. If data has been encoded which calls for a reduction in prefix, a negative-going output level is produced at pin 7. This negative level subtracts one unit of column current from the data at the input to the Column Decoder. Notice on the



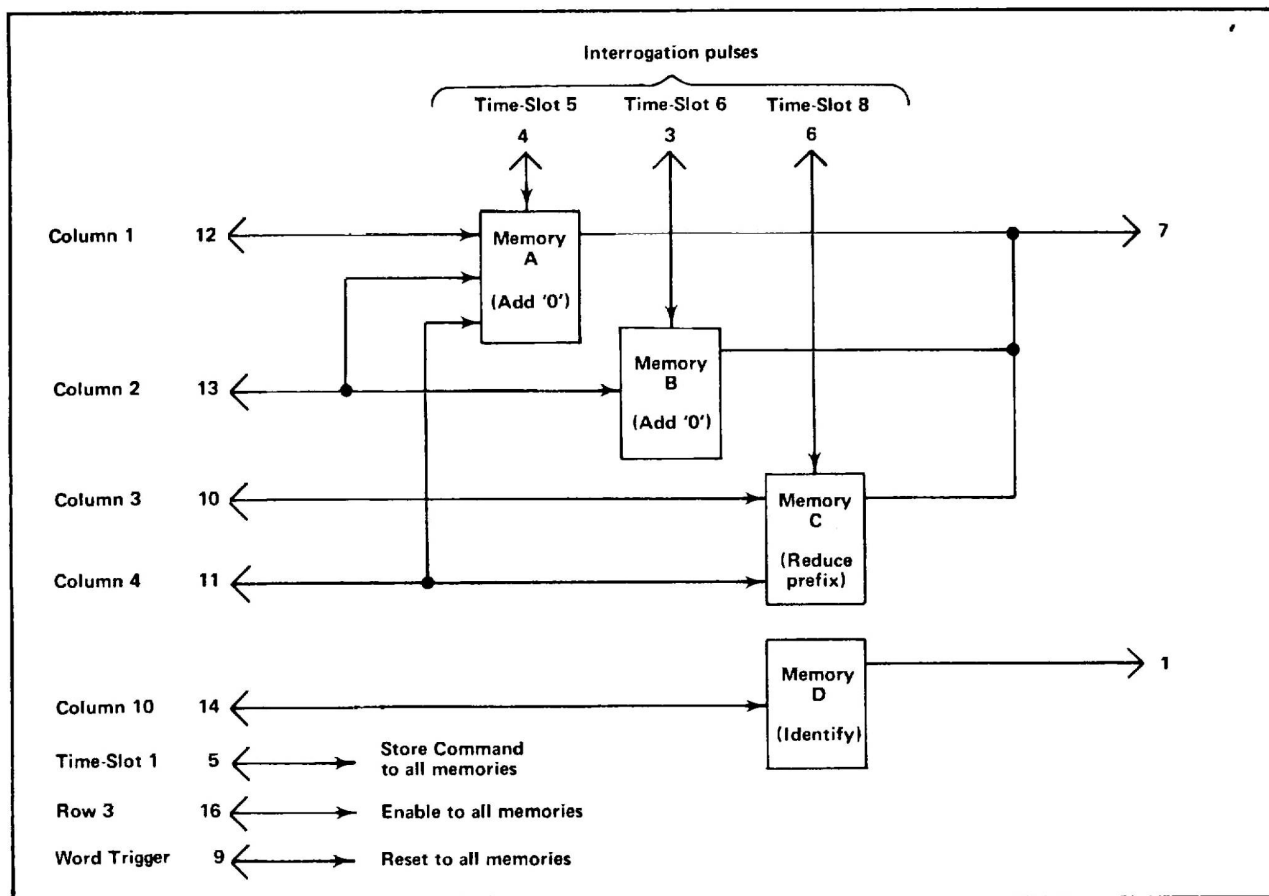


Fig. 3-47. Block representation of memory sequence in U1190.

Character Selection Matrix of Fig. 3-38 that a reduction of one column when row 4 is programmed results in a one unit reduction of the prefix. For example, with the 100  $\mu$ V program shown in Fig. 3-45, if the data received from the plug-in called for a reduction in prefix, the CRT readout would be changed to 1 mV (zeros deleted by program; see Encoding the Data).

The 100 microamperes of quiescent current through R1141 that was provided by Q1163 (see Display-Skip Generator) allows the prefix to be reduced from m (100 microamperes column current; column 1) to no prefix (zero column current; column zero) so only the unit of measurement encoded during time-slot 9 is displayed. Notice that reducing the prefix program from column 1 to column 0 programs the Readout System to not display a character at this readout location.

A further feature of the Zeros Logic and Memory is the Identify function. If 10 units of column current are encoded by the plug-in unit along with row 3 during time-slot 1, the Zeros Logic and Memory produces a negative-going output pulse at pin 1 which switches the Column Data 3-68

Switch and Row Data Switch to the ninth channel. Then, time-slot pulses 2 through 9 encode an output current through resistors R1131-R1138 for column data and R1171-R1178 for row data. This provides the currents necessary to display the word IDENTIFY on the CRT in the word position allotted to the channel which originated the Identify command. After completion of this word, the Column Data Switch and Row Data Switch continue with the next word in the sequence.

The Word Trigger signal from the Word Trigger stage is connected to pin 9 of U1190 through C1190. At the end of each word of readout information, this pulse goes LO. This erases the four memories in the Zeros Logic and Memory in preparation for the data to be received from the next channel.

### Character Generators

The Character Generator stage (Diagram 15) consists of five similar integrated circuits U1251-U1255 which generate the X (horizontal) and Y (vertical) outputs at pins 16



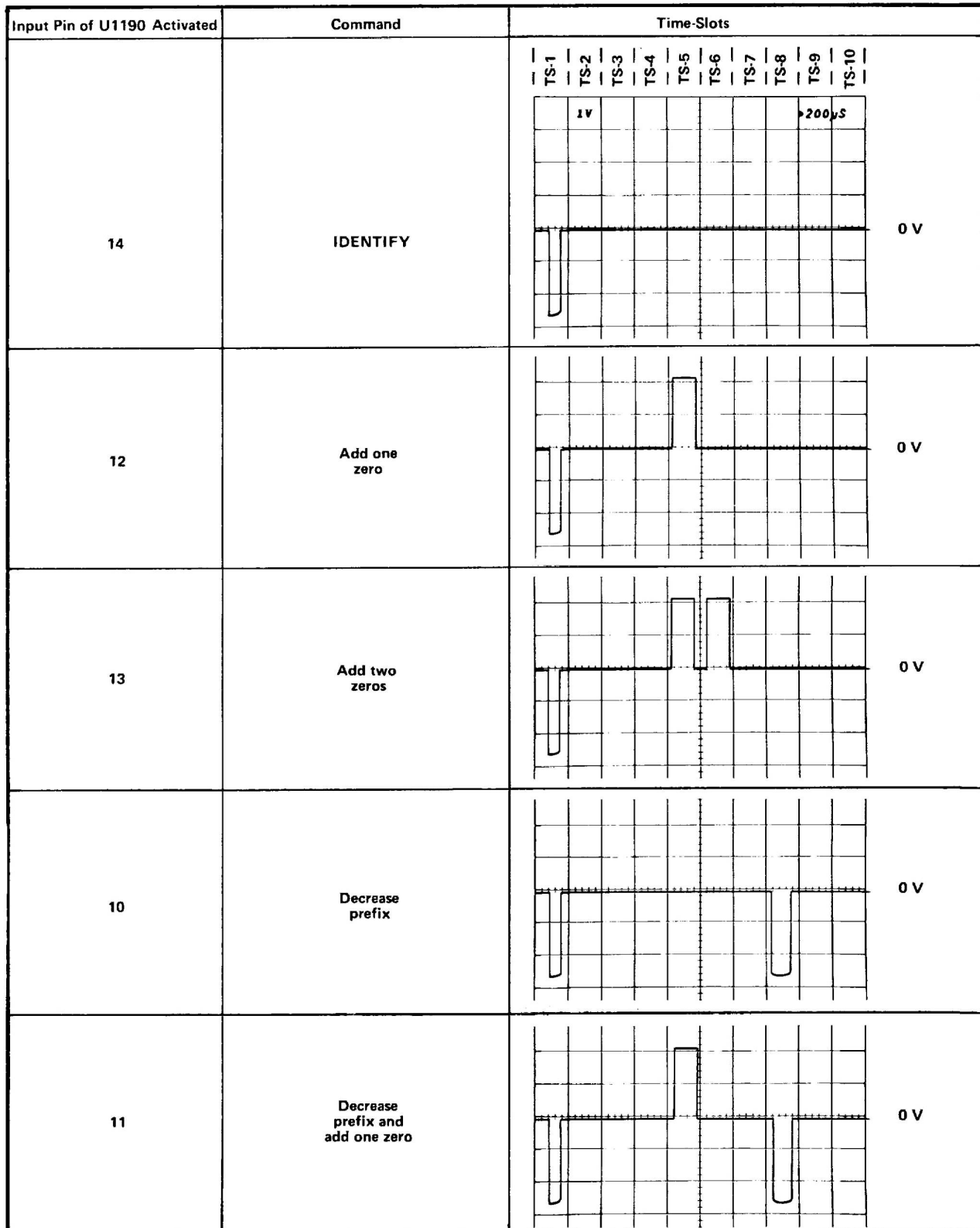


Fig. 3-48. Typical output waveforms for Zeros Logic and Memory stage operation (at pin 7 of U1190).

and 1 respectively to produce the character displayed on the CRT. Each integrated circuit can produce 10 individual characters. U1251 which is designated as the "Numerals" Character Generator can produce the numerals 0 through 9 shown in row 1 of the Character Selection Matrix (Fig. 3-38). U1252 can produce the symbols shown in row 2 of the Character Selection Matrix and U1253 produces the prefixes and some letters of the alphabet which are used as prefixes in row 4. U1254 and U1255 produce the remaining letters of the alphabet shown in rows 5 and 6 of the Character Selection Matrix. All of the Character-Generator stages receive the column digital data from Column Decoder U1166 in parallel. However, only one of the character generators receives row data at a particular time and only the stage which receives both row and column data is activated. For example, if column 2 is encoded by a plug-in unit, the five Character Generators are enabled so that either a 1, <, /, V, or an N can be produced. However, if at the same time row 4 has also been encoded by the plug-in unit, only the Prefix Character Generator U1253 will produce an output to result in a / displayed on the screen. This integrated circuit provides current outputs to the Format Generator which produce the selected character on the CRT. In a similar manner, any of the 50 characters shown in the Character Selection Matrix can be displayed by correct addressing of the row and column.

#### Decimal Point Logic and Character Position Counter

Decimal Point Logic and Character Position Counter U1260 performs two functions. The first function is to produce a staircase current which is added to the X (horizontal) signal to space the characters horizontally on the CRT. After each character is generated, the negative going edge of the Ready signal at pin 5 advances the Character Position Counter. This produces a current step output at pin 3 which, when added to the X signal, causes the next character to be displayed one character space to the right. This stage can also be advanced when a Space instruction is encoded by the plug-in unit so that a space is left between the displayed characters on the CRT. Row 10 information from the Row Decoder is connected to pin 4 of U1260 through R1265. When row 10 and column 0 are encoded, the output of this stage advances one step to move the next character another space to the right. However, under this condition, no display is produced on the CRT during this time-slot since the Character Generators are not activated.

Time-slot pulses 1, 2, and 3 are also connected to pin 4 of U1260 through VR1260, VR1261, and VR1262 respectively and R1260, R1265. This configuration adds a space to the displayed word during time-slots 1, 2, and 3 even if information is not encoded for display during these timeslots. With this feature, the information which is displayed during time-slot 4 (1-2-5 data) always starts in the fourth character position whether data has been displayed in the previous time-slots or not. Therefore, the resultant CRT

display does not shift position as normal/invert or cal/uncal information is encoded by the plug-in. The Word Trigger pulse connected to pin 8 of U1260 through C1267 resets the Character Position Counter to the first character position at the end of each word.

The Decimal Point Logic portion of this stage allows decimal points to be added to the CRT display as encoded by the plug-in units. When row 7 is encoded in coincidence with columns 3 through 7 (usually encoded during time-slot 1), a decimal point is placed at one of the five locations on the CRT identified in row 7 of the Character Selection Matrix (Fig. 3-38). This instruction refers to the decimal point location in relation to the total number of characters that can be displayed on the CRT (see Fig. 3-49). For example, if column 3 and row 7 are encoded during timeslot 1, the system is instructed to place a decimal point in location No. 3. As shown in Fig. 3-49, this displays a decimal point before the third character that can be displayed on the CRT (first three time-slots produce a space whether data is encoded or not; see previous paragraph). The simultaneous application of row 7 data to the Y-input of the Format Generator through R1269 raises the decimal point so it appears between the displayed characters.

When decimal-point data is encoded, the CRT is unblanked so a readout display is presented. However, since row 7 does not activate any of the five Character Generators, the CRT beam is not deflected but instead remains in a fixed position to display a decimal point between the characters along the bottom line of the readout word. After

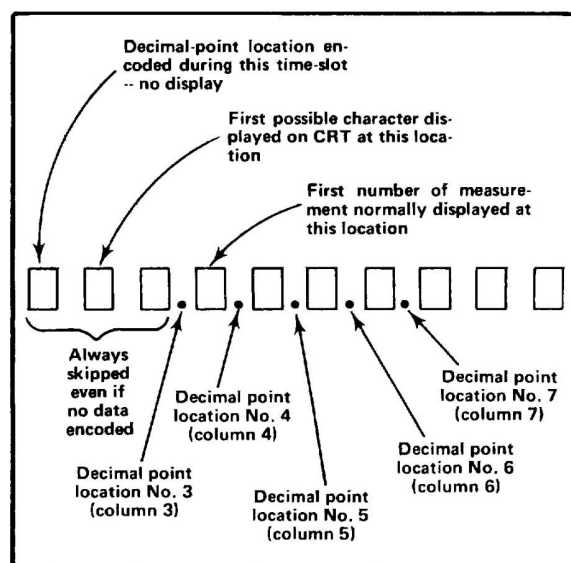


Fig. 3-49. Readout word relating 10 possible character locations to the decimal point instructions that can be encoded, and the resultant CRT display.

the decimal point is produced in the addressed location, the CRT beam returns to the location indicated by the Character Position Counter to produce the remainder of the display.

## Format Generator

The X and Y-deflection signals produced by the Character Generator stage, are connected to pins 2 and 7 respectively of Format Generator U1270. The Channel Address No. 2 code from the Channel Counter is also connected to pins 1, 8, and 15 of this stage. The Channel Address No. 2 code directs the Format Generator to add current to the X and Y signals to deflect the CRT beam to the area of the CRT which is associated with the plug-in channel that originated the information (see Fig. 3-37). The Channel Address No. 2 code and the resultant word positions are shown in Table 3-4. In addition, the character position current from the Decimal Point Logic and Character Position stage is added to the X (horizontal) input signal to space the characters horizontally on the CRT (see previous discussion). The Ready signal at pin 13 (coincident with Vertical/Horizontal Channel Switch OFF Command) activates this stage when a character is to be displayed on the CRT.

### Y-Output Amplifier

The Y-output signal at pin 6 of U1270 is connected to the Y-Output Amplifier Q1284-Q1288. This stage provides a low impedance load for the Format Generator while providing isolation between the Readout System and the Vertical Amplifier. Vertical Separation adjustment R1285 changes the gain of this stage to control the vertical separation between the readout words displayed at the top and bottom of the graticule area.

**TABLE 3-4**  
**Channel Address No. 2 Code**

Channel Address NO. 2 Code			
Pin 7 U1232	Pin 7 U1231	Pin 5 U1230	Channel Displayed
LO	LO	HI	Channel 1 Left Vertical
LO	LO	LO	Channel 2 Left Vertical
LO	HI	HI	Channel 1 Right Vertical
LO	HI	LO	Channel2 Right Vertical
HI	LO	HI	Channel 1 A Horizontal
HI	LO	LO	Channel 2 A Horizontal
HI	HI	HI	Channel 1 B Horizontal
HI	HI	LO	Channel2 B Horizontal

### X-Output Amplifier

The X-Output Amplifier Q1274-Q1278 operates similarly to the Y-Output Amplifier to provide the horizontal deflection from the readout signal available at pin 4 of U1270. The gain of this stage is fixed by the values of the resistors in the circuit.

### Display Sequence

Fig. 3-50 shows a flow chart for the Readout System. This chart illustrates the sequence of events which occurs in the Readout System each time a character is generated and displayed on the CRT.

## NOTES

(A)

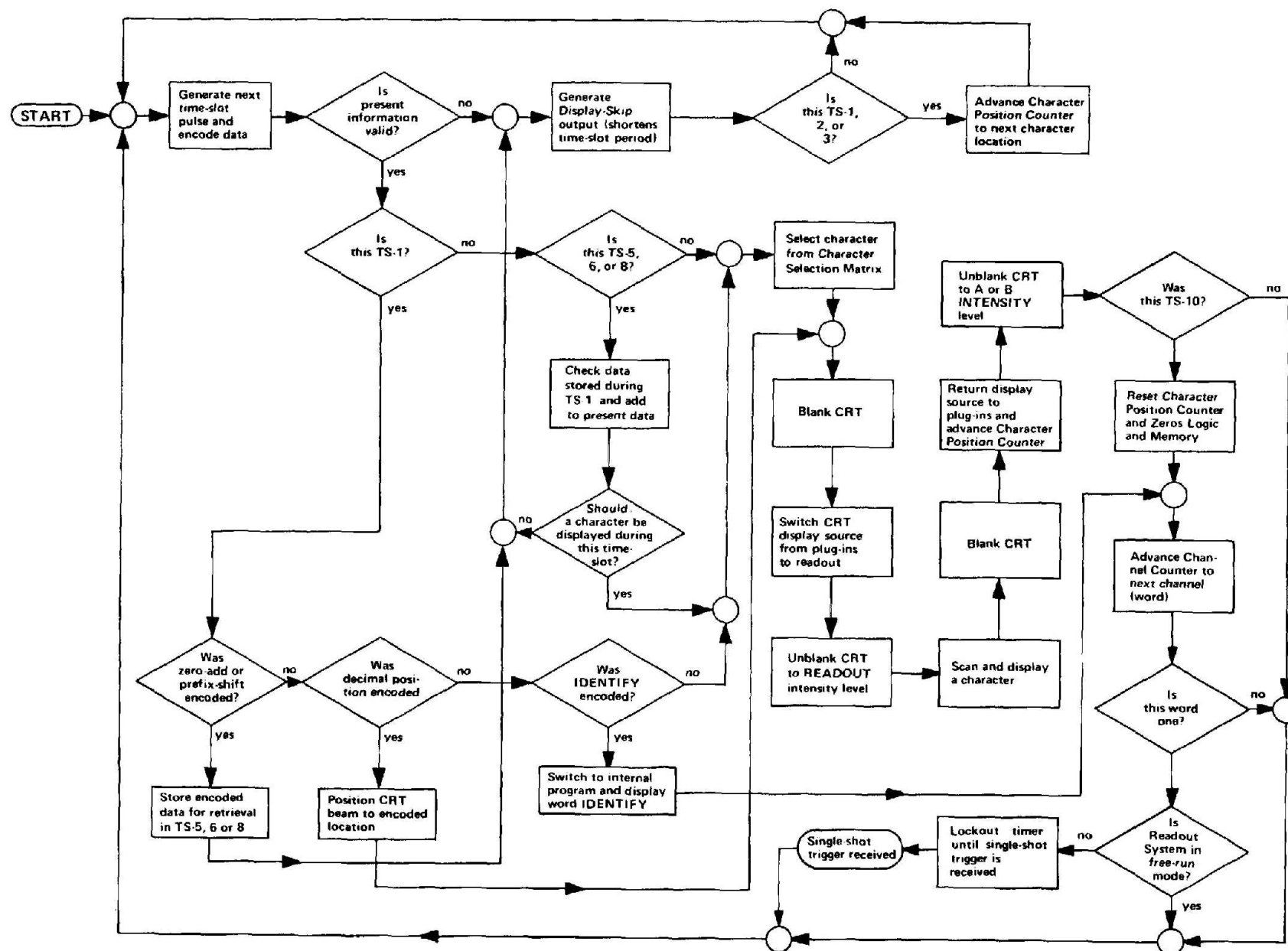


Fig. 3-50. Flow chart for character generation by the Readout System.

## SECTION 4 MAINTENANCE

*Change information, if any, affecting this section will be found at the rear of the manual.*

## Introduction

This section of the manual contains maintenance information for use in preventive maintenance, corrective maintenance, or troubleshooting of the R7704.

## Cover Removal

## WARNING

Dangerous potentials exist at several points throughout this instrument. When the instrument is operated with the covers removed, do not touch exposed connections or components. Some transistors have voltages present on their cases. Disconnect power before cleaning the instrument or replacing parts.

The top and bottom covers of the R7704 can be removed to gain access to the interior of the instrument. Remove the 12 screws in each cover to remove the covers. The top and bottom covers protect this instrument from dust in the interior, and also provide protection to personnel from the operating potentials present. In addition, they reduce the EMI radiation from the instrument or EMI interference to the display due to other equipment.

## Power Unit Removal

The power unit can be slid out of the rear of the R7704 to gain better access to the Logic, Vertical Switching, X-Y Delay Compensation or Horizontal Interconnect, and the Low-Voltage Regulator circuit boards, high-voltage oscillator transistors, and for power-unit maintenance. To remove the power unit, first remove the top cover. Then, remove the four screws (see Fig. 4-1) which hold the power unit to the rear of the instrument. Slide the power unit out of the rear of the instrument until it can be set down on the work surface (guide the power cable so it does not catch on other parts of the instrument). The power unit remains connected to the instrument so it can be operated in this position for maintenance purposes. Reverse this procedure when replacing the power unit; be careful not to pinch the power cable as the power unit is replaced. Be sure that all the securing screws are tight to hold the power unit in place properly.

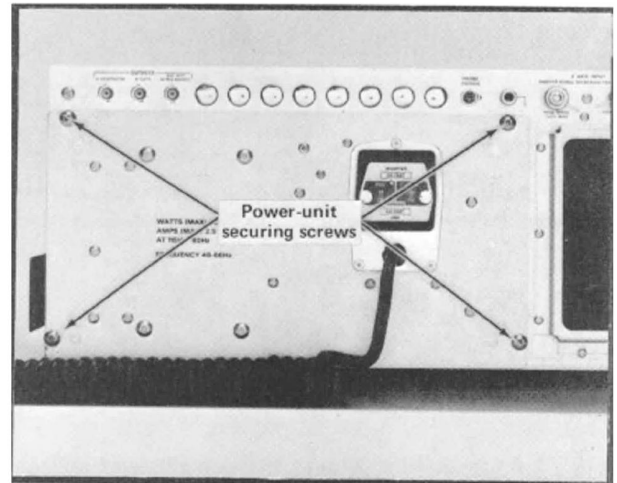
## WARNING

**Extreme caution must be used when troubleshooting in the power supply due to the line voltage and the high voltage/high current potentials present. Refer to the discussion entitled Troubleshooting the Power Supply for troubleshooting information, and Access to Components in Power Unit for information on how to remove the protective cover/shield on the power unit**

## PREVENTIVE MAINTENANCE

## General

Preventive maintenance consists of cleaning, visual inspection, lubrication, etc. Preventive maintenance performed on a regular basis may prevent instrument breakdown and will improve the reliability of this instrument. The severity of the environment to which the R7704



*Fig. 4-1. Securing screws for power unit (rear of instrument).*





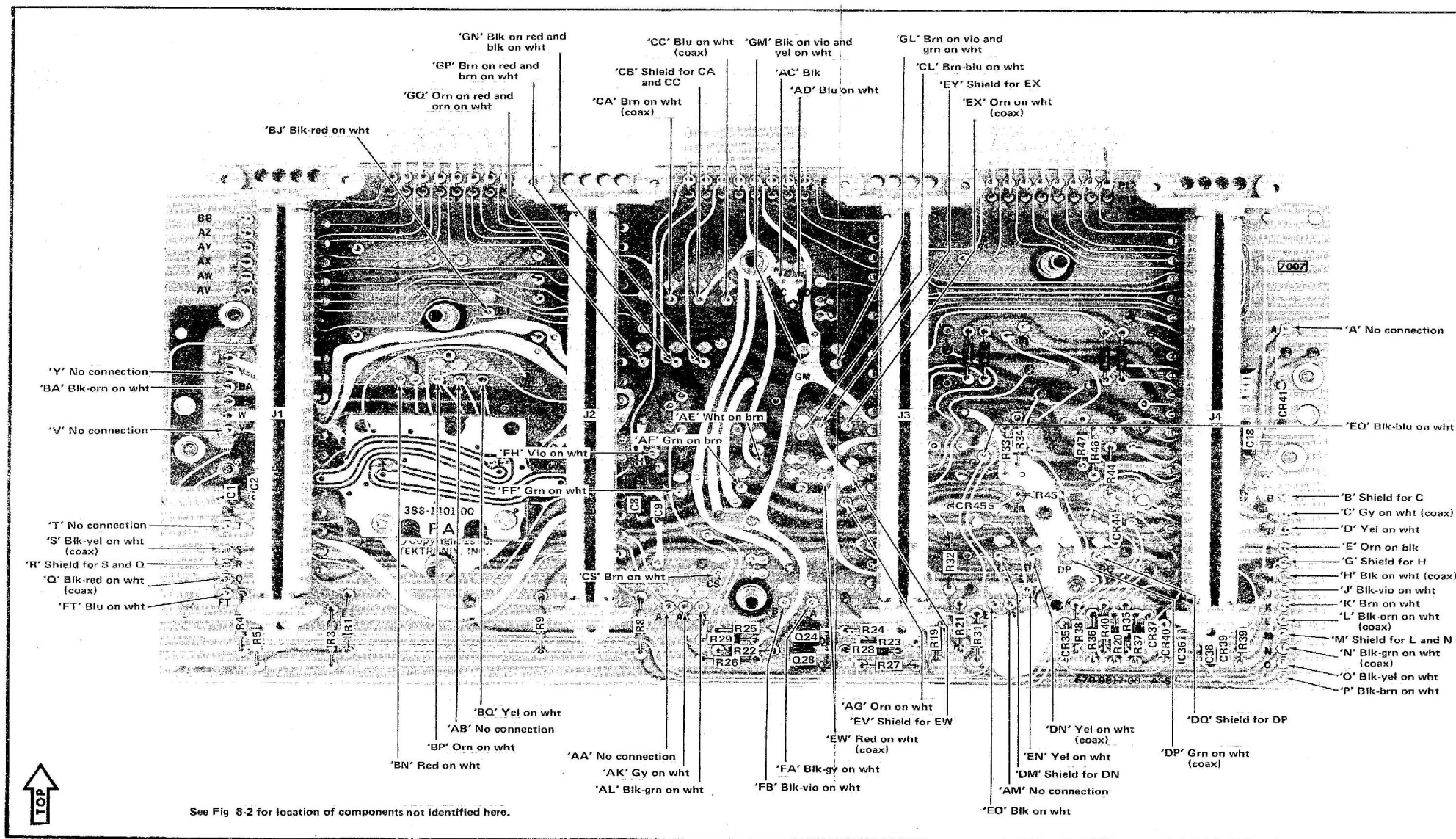
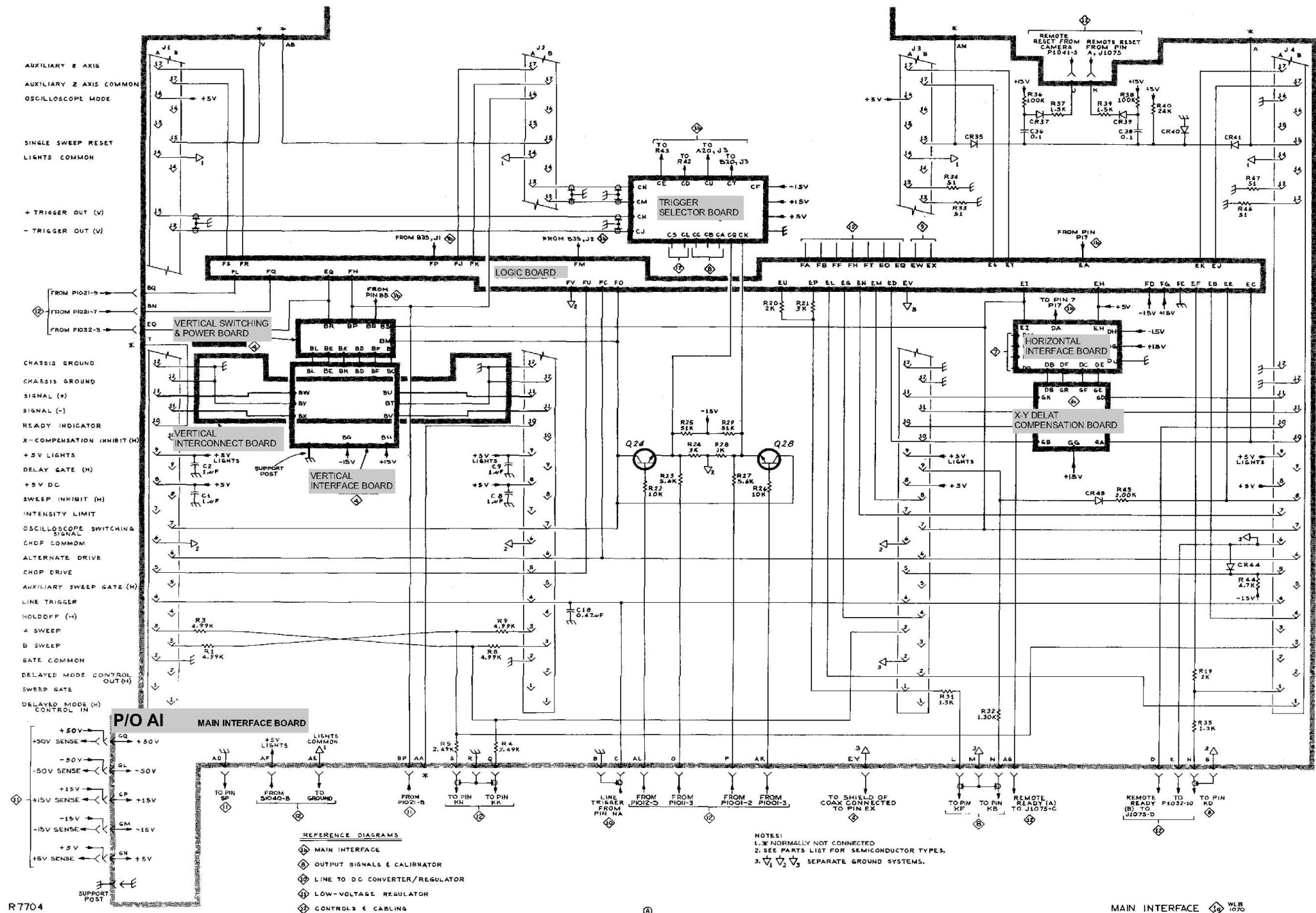
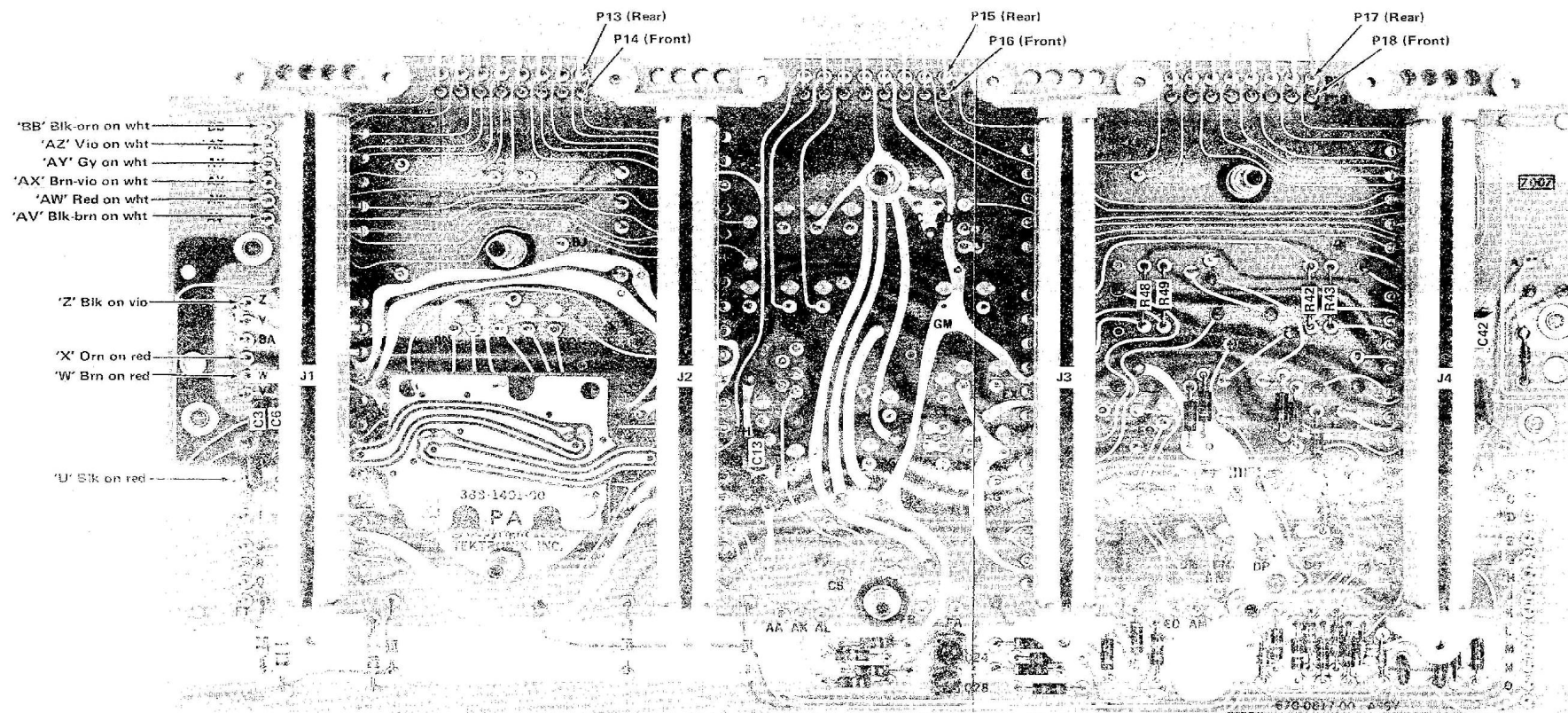


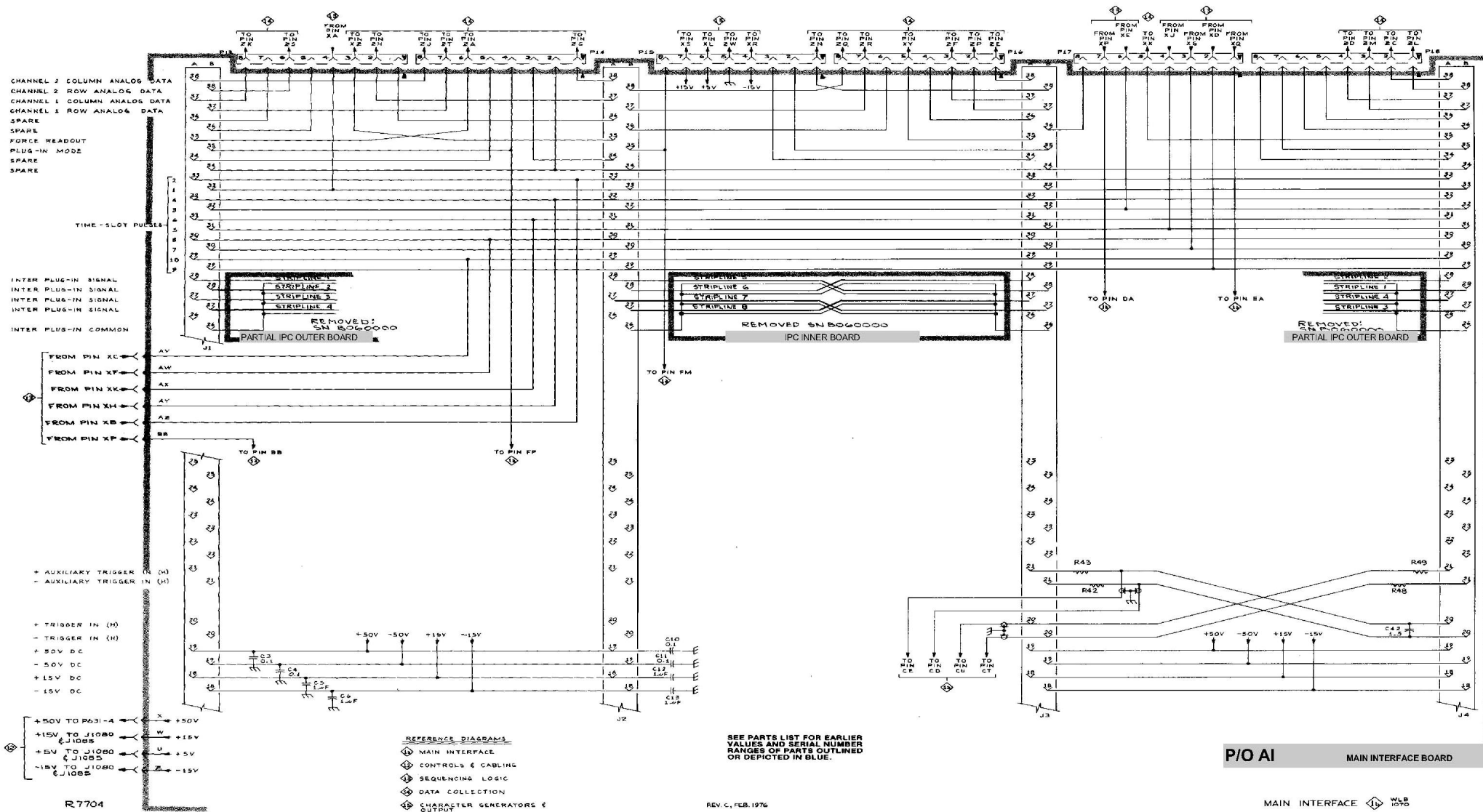
Fig. 8-1. P/O A1-Partial Main Interface circuit board.;





See Fig. 8-1 for location of components not identified here.

Fig. 8-2. P/O A1-Partial Main Interface circuit board.



R7704

REV. C, FEB. 1976



CR178 added on rear SN B040000.

Fig. 8-3. A2-Logic circuit board.



**P/OAI**



LOGIC BOARD **A2**

LOGIC CIRCUIT

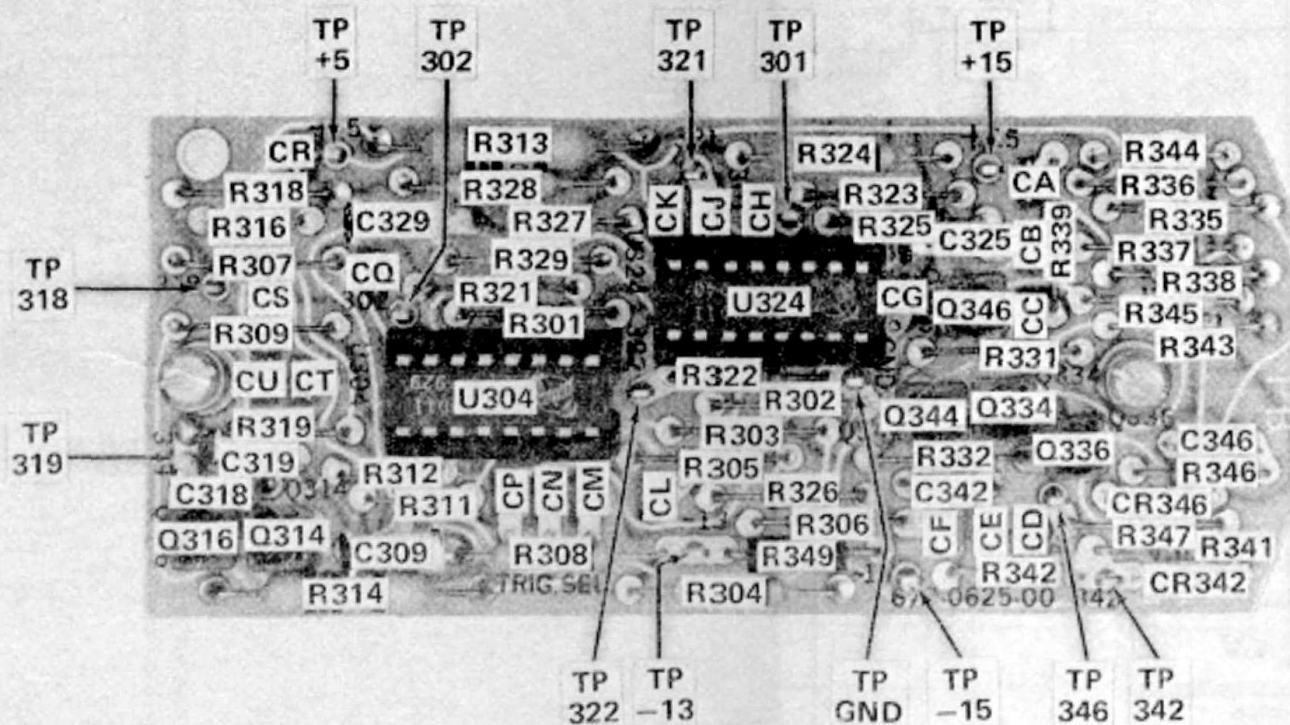
R7704

REV. D, AUG. 1977

SEE PARTS LIST FOR EARLIER  
VALUES AND SERIAL NUMBER  
RANGES OF PARTS MARKED  
WITH BLUE OUTLINE.

VOLTAGES obtained under conditions given on page 8-2.

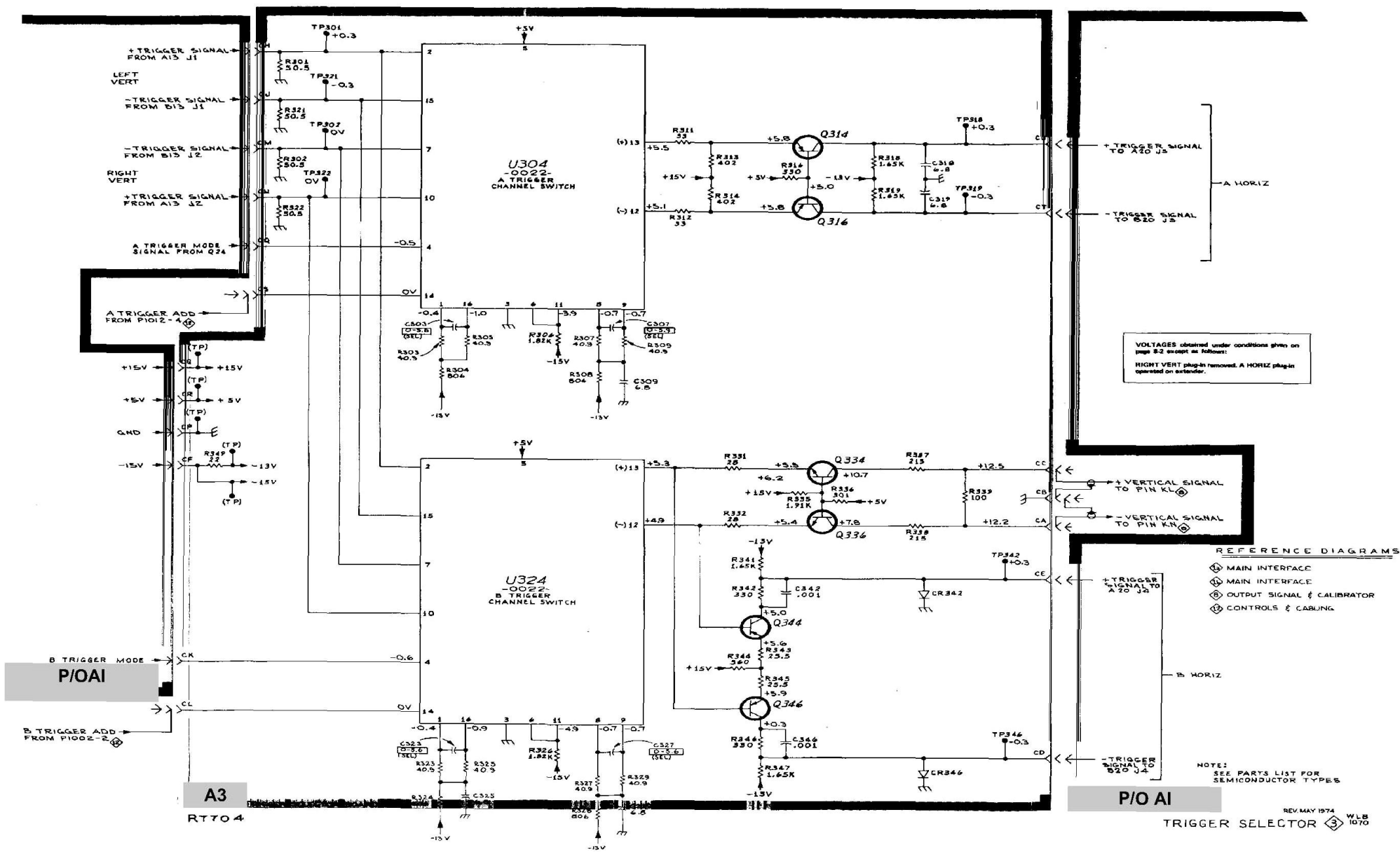




NOTE: R313 moved to rear of board SN B020000



Fig. 8-4. A3 - Trigger Selector circuit board.

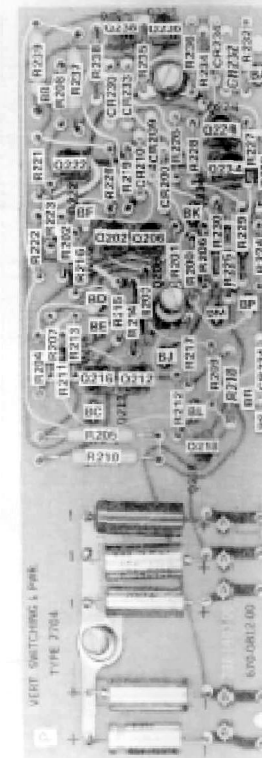




NOTE: R241, R251, R271,  
R281, R295 mounted  
on rear of board.



Fig. 8-5. A4 - Vertical Interface circuit board.

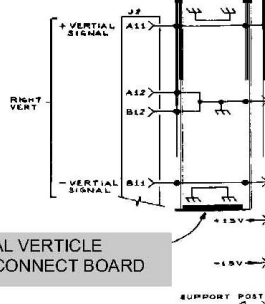


See Fig. 8-18 for location of components not identified here.



Fig. 8-6. P/O A5 - Partial Vertical Switching and Power circuit board.

P/O AI



PARTIAL VERTICLE  
INTERCONNECT BOARD

VERTICAL ADD  
MODE

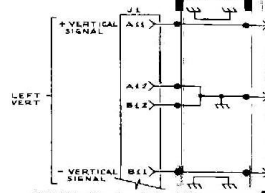
HORIZONTAL MODE  
SWITCH B MODE  
FROM PIN EQ

VERTICAL CHANNEL  
SWITCH OFF  
COMMAND

DISPLAY B COMMAND  
FROM PIN E1

VERTICAL MODE  
COMMAND FROM  
PIN F0

PARTIAL VERTICLE  
INTERCONNECT BOARD



R7704

A4

P/O A5 VERTICLE  
SWITCHING &  
POWER BOARD

VOLTAGES obtained under conditions given on  
page B2 except as follows:  
LEFT and RIGHT VERT units removed. Plastic  
cover removed from Vertical Interface board.

NOTES:  
1. \* NON-REPLACEABLE PART, INTERNAL  
PART OF CIRCUIT BOARD.  
2. SEE PARTS LIST FOR SEMICONDUCTOR  
TYPES.

REFERENCE DIAGRAMS  
◆ MAIN INTERFACE  
◆ VERTICAL AMPLIFIER

VERTICAL INTERFACE ◆ WLS  
1070

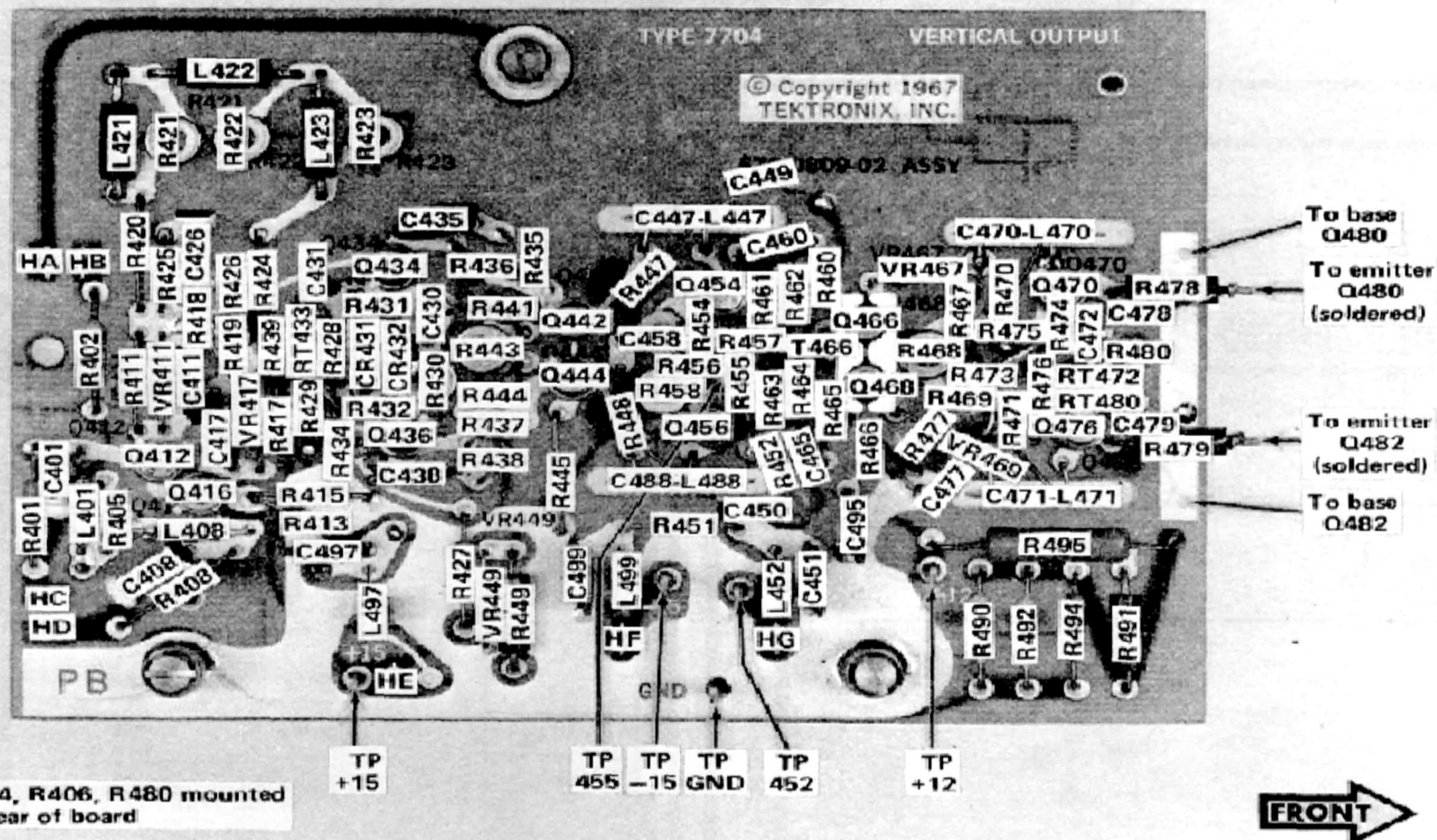
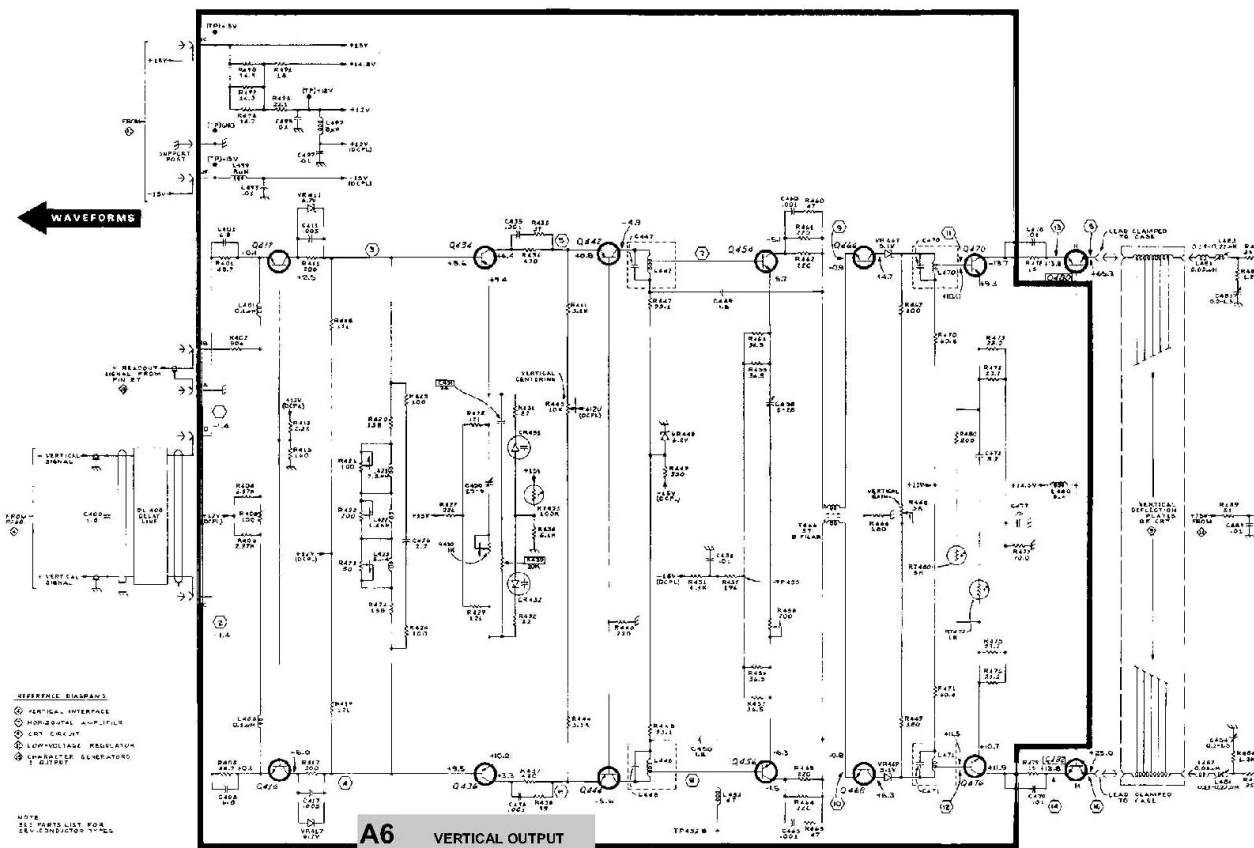
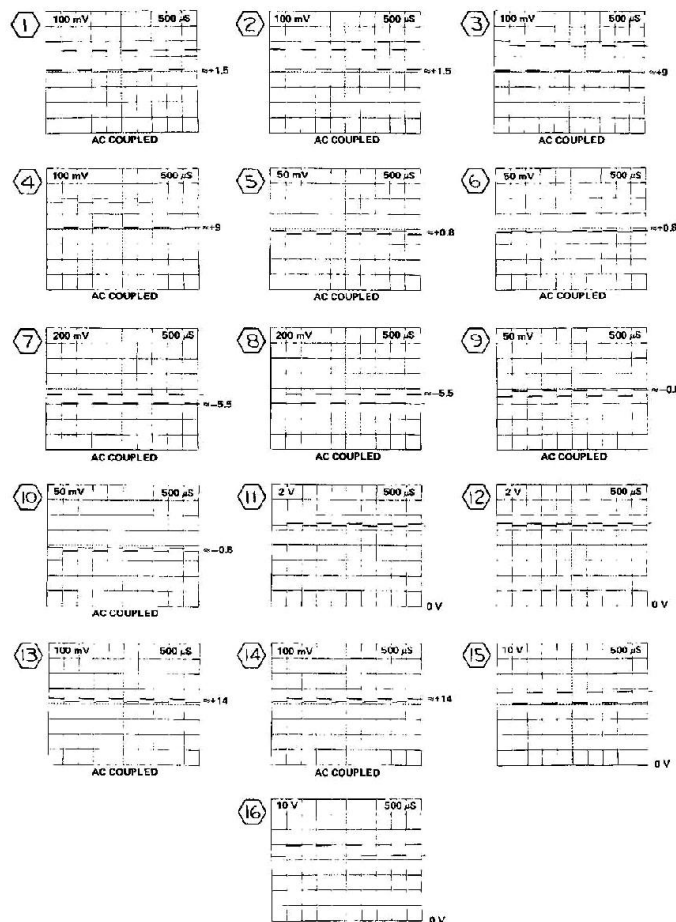
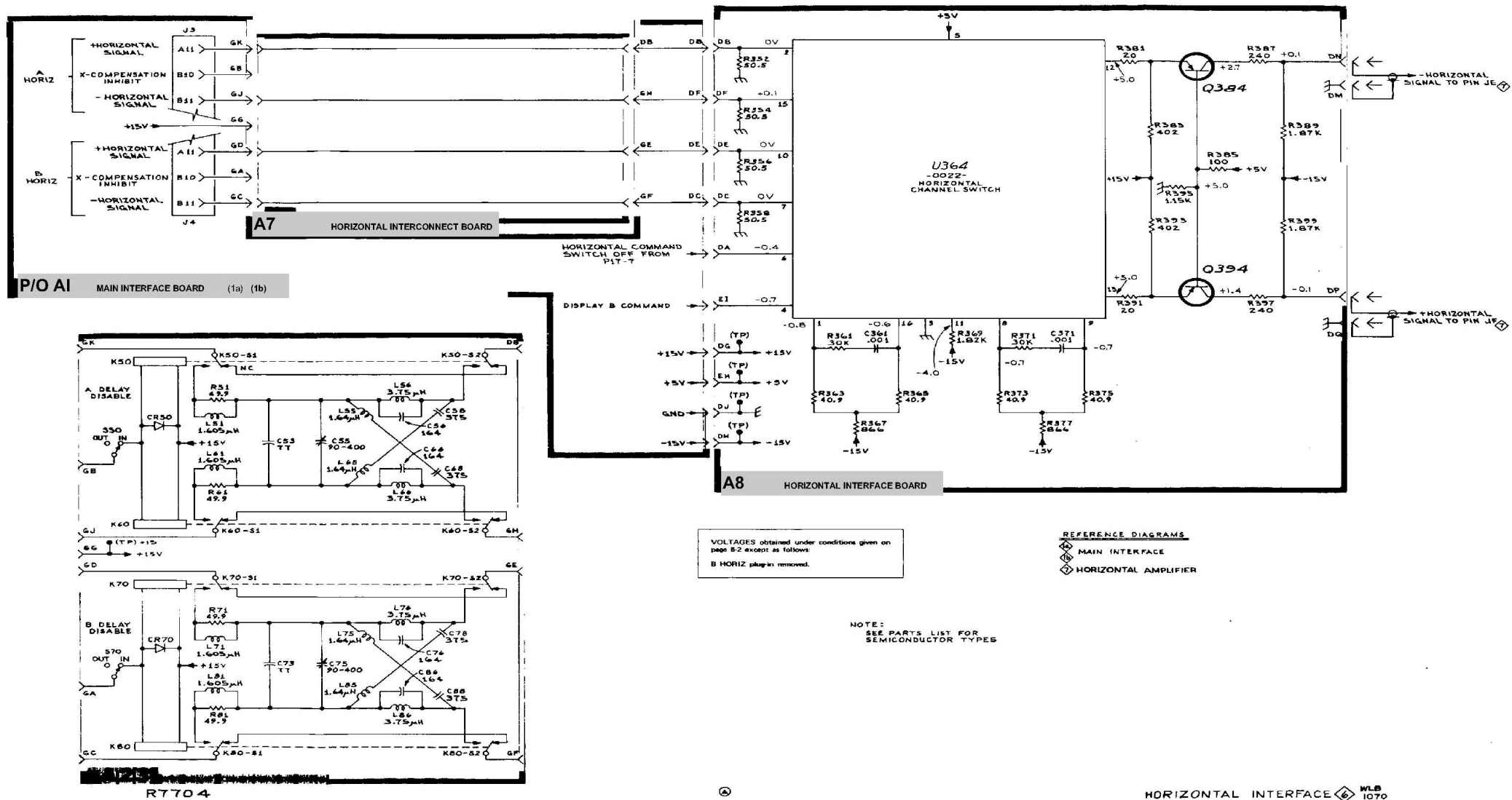


Fig. 8-7. A6 - Vertical Output circuit board.













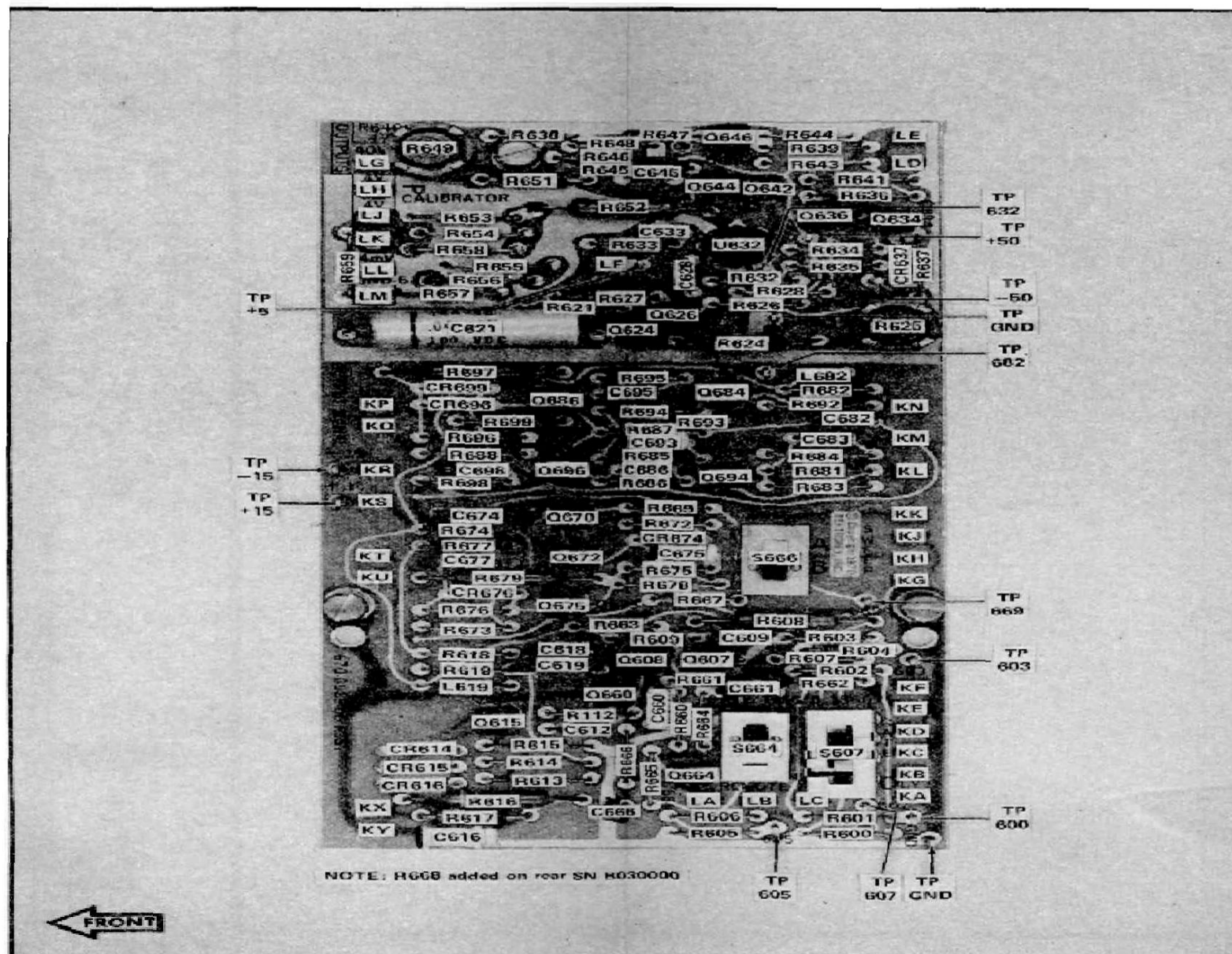


Fig. 8-12. A10-Output Signal circuit board.



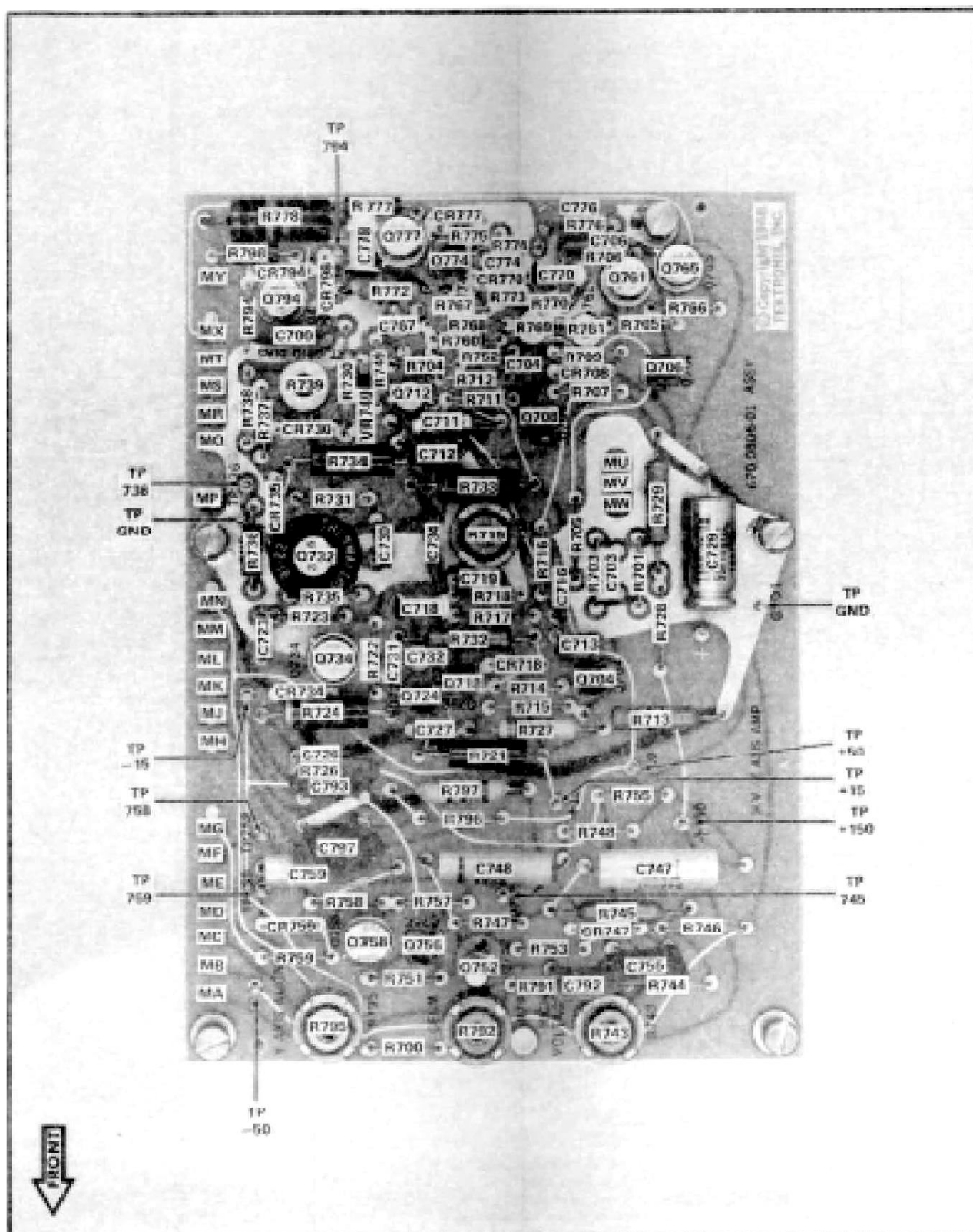
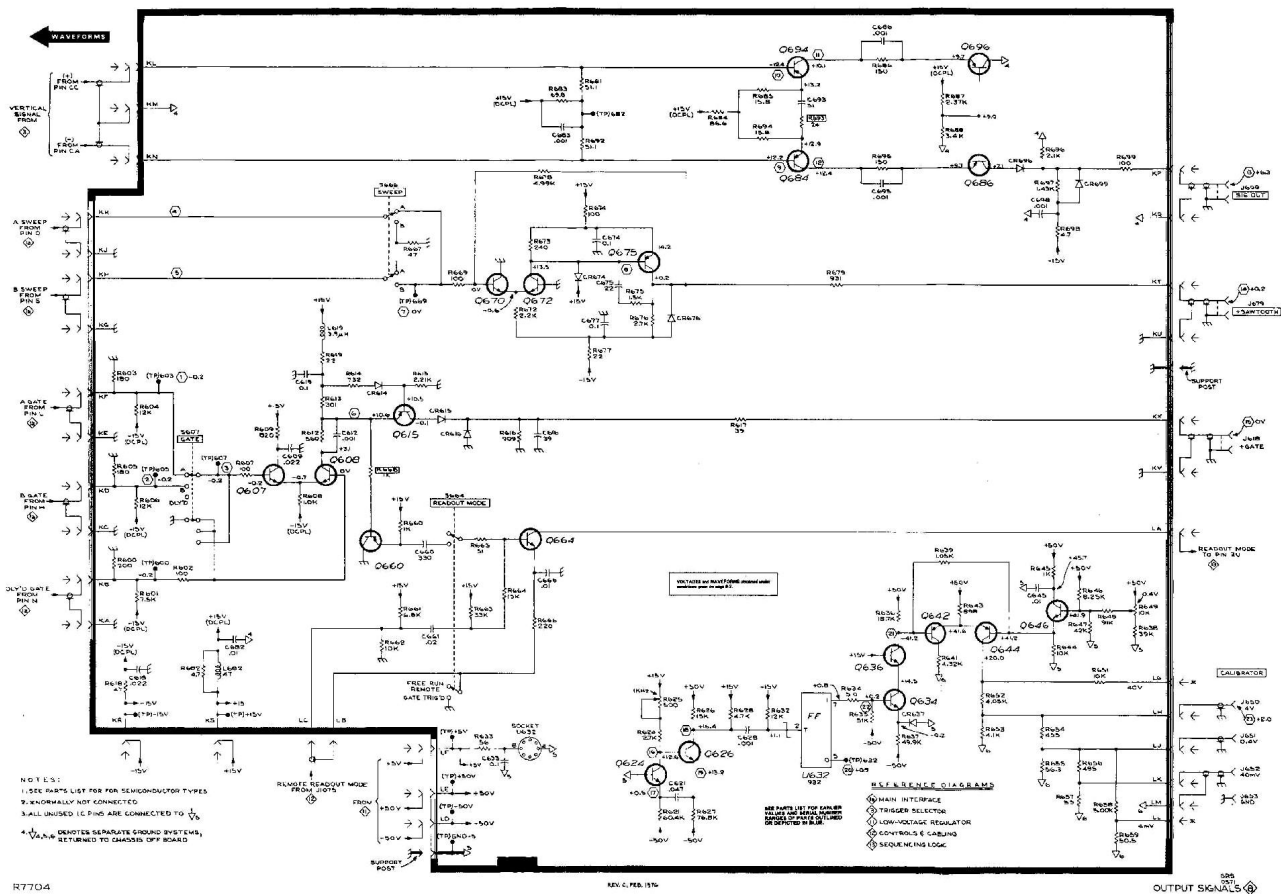
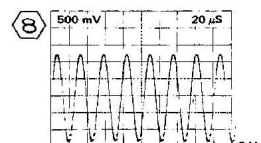
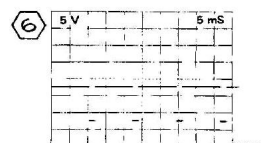
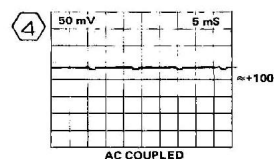
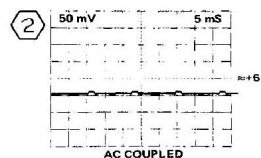


Fig. 8-13. A11 - High Voltage/Z Axis Amplifier circuit board.









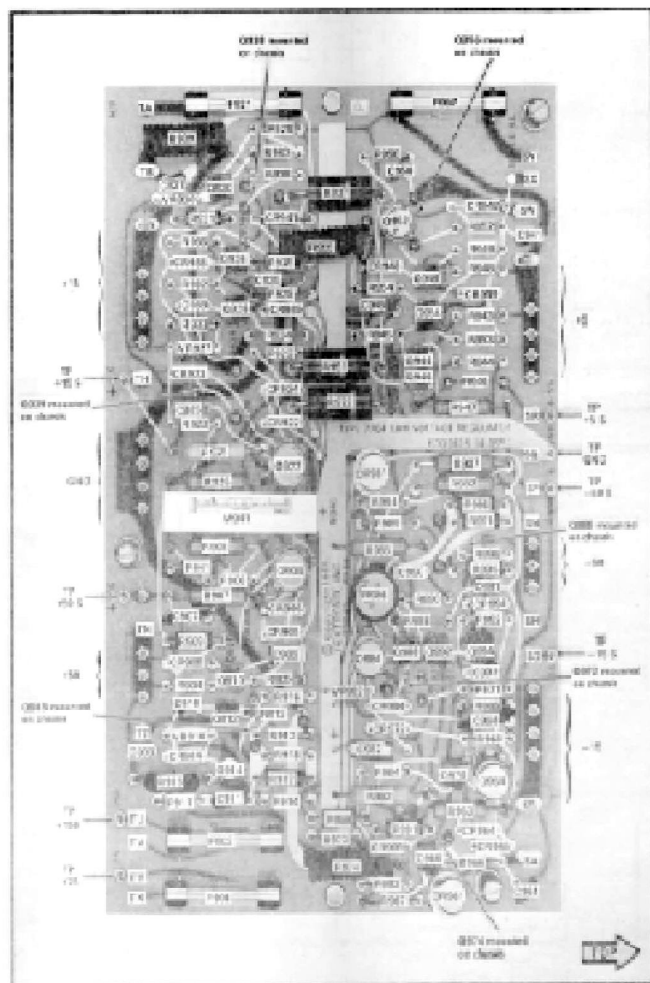


Fig 8-17. A15 - Low-Voltage Rectifier circuit board.

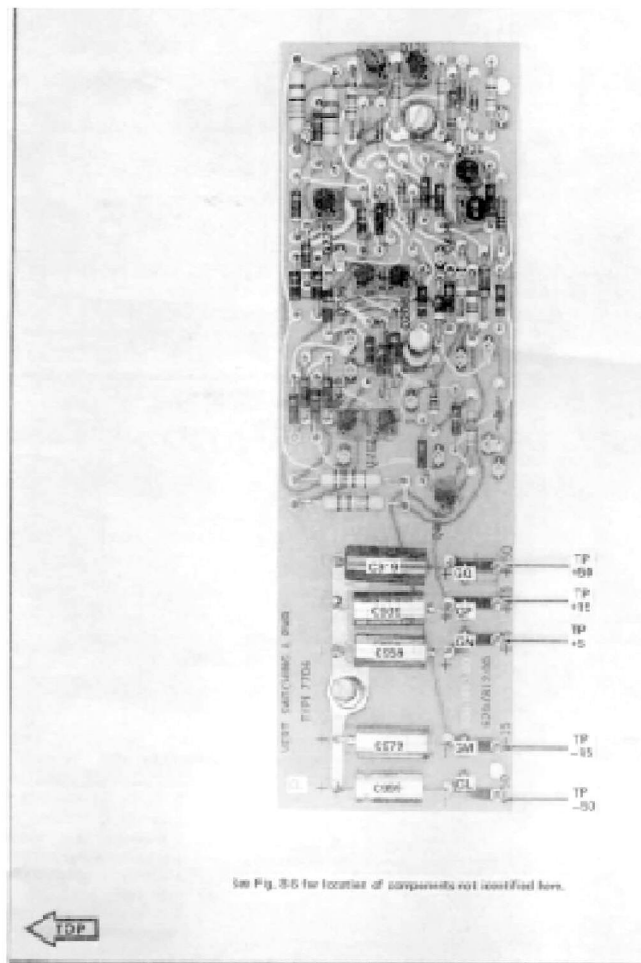


Fig 8-18. P/O A5 - Partial Vertical Switching and Power circuit board.

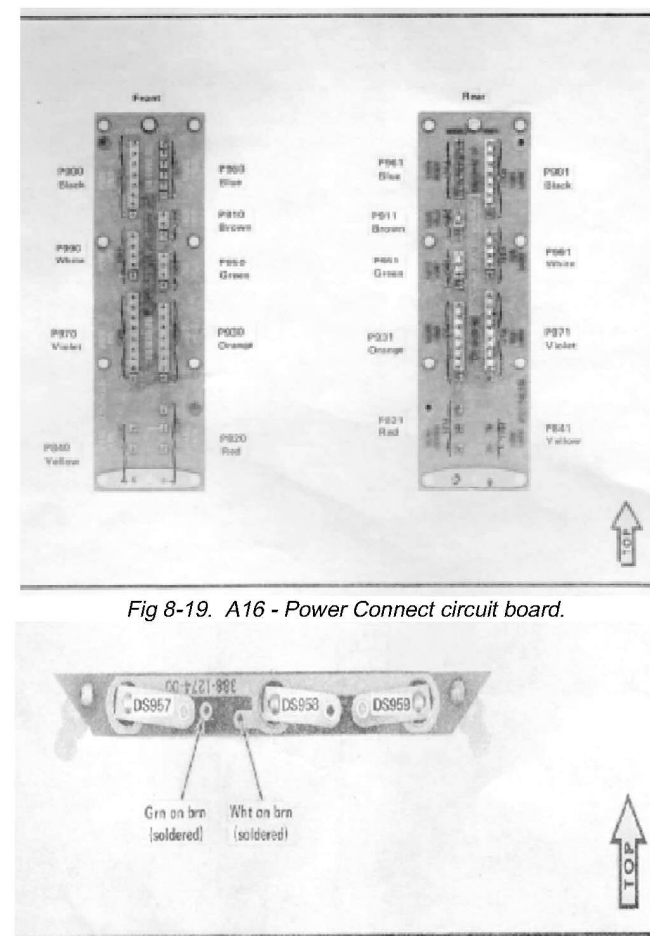


Fig 8-19. A16 - Power Connect circuit board.

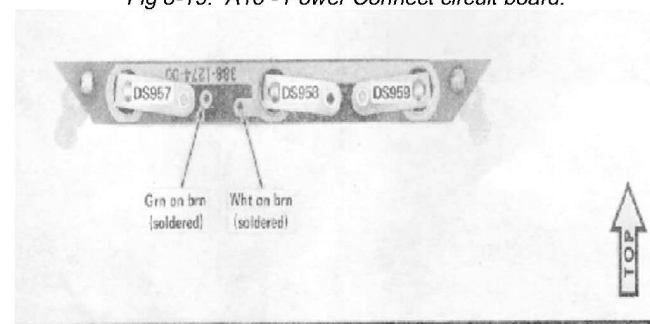
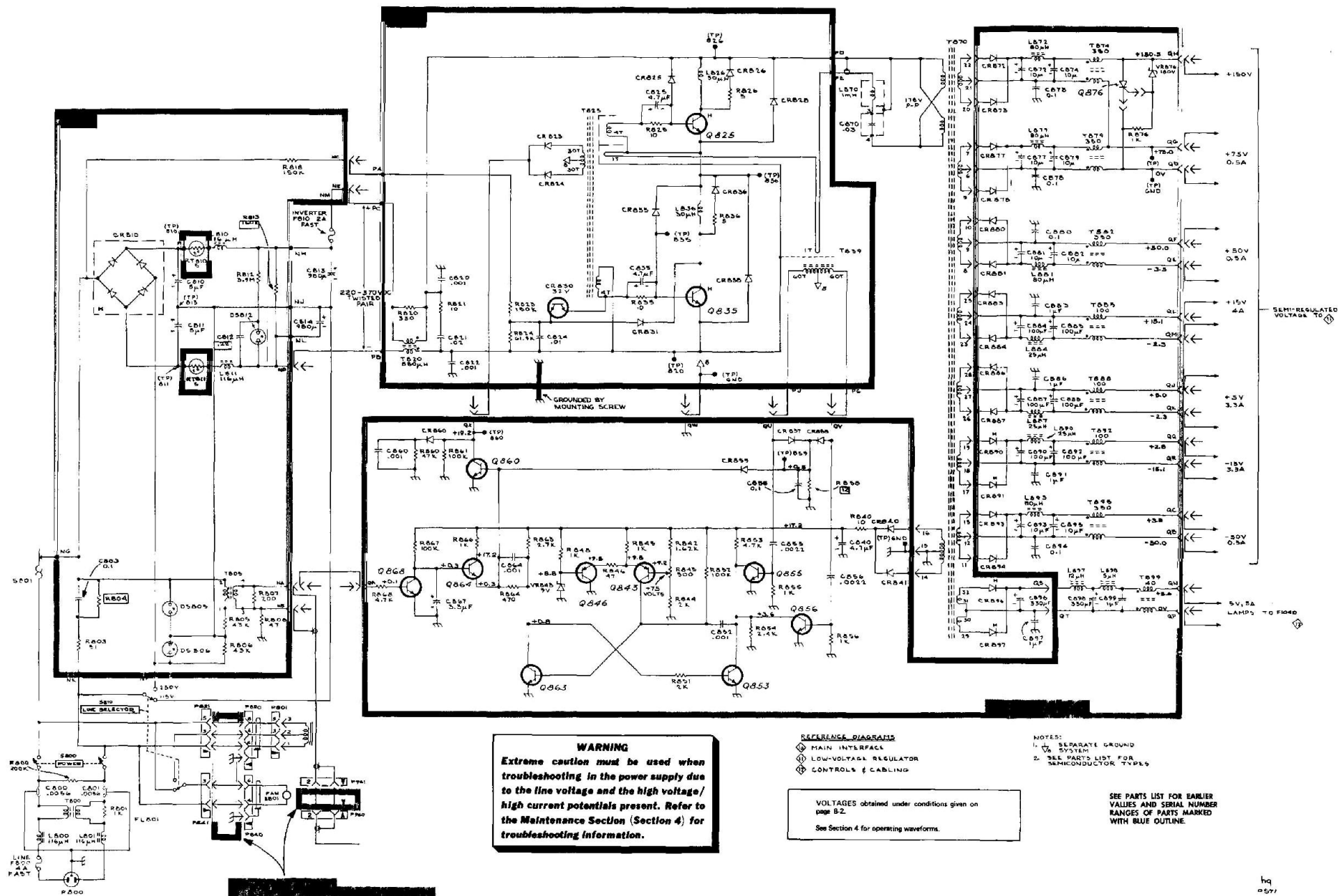


Fig 8-20. A22 - Graticule Light circuit board.



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①

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Fig. 8-21. A17 - B Trigger Source Switch circuit board.

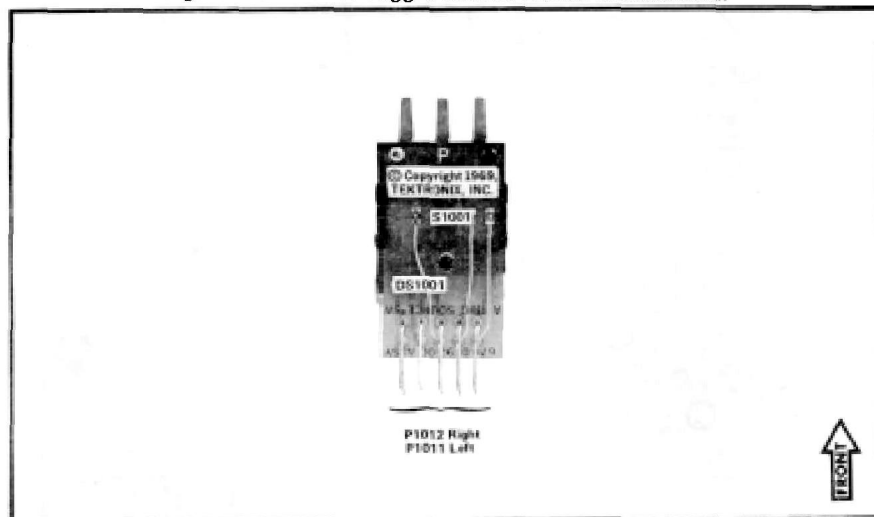


Fig. 8-22. A18 - A Trigger Source Switch circuit board.

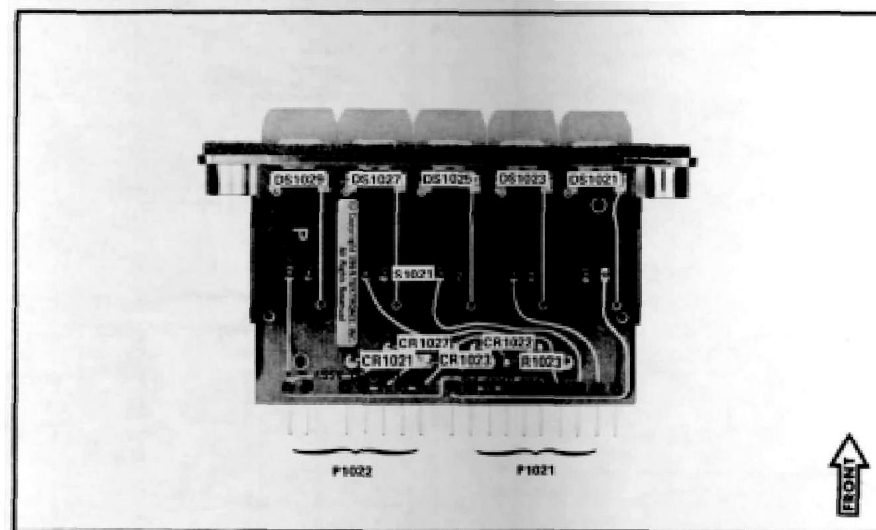


Fig. 8-23. A19 - Vertical Mode Switch circuit board.

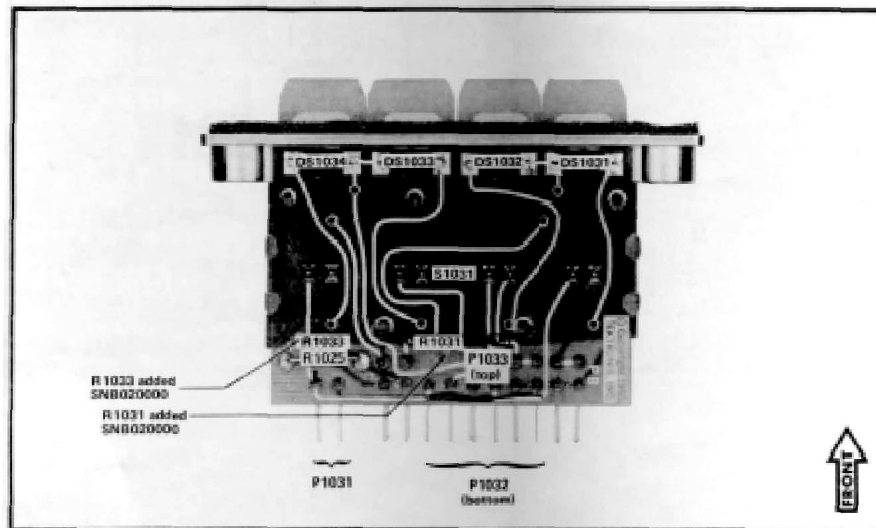
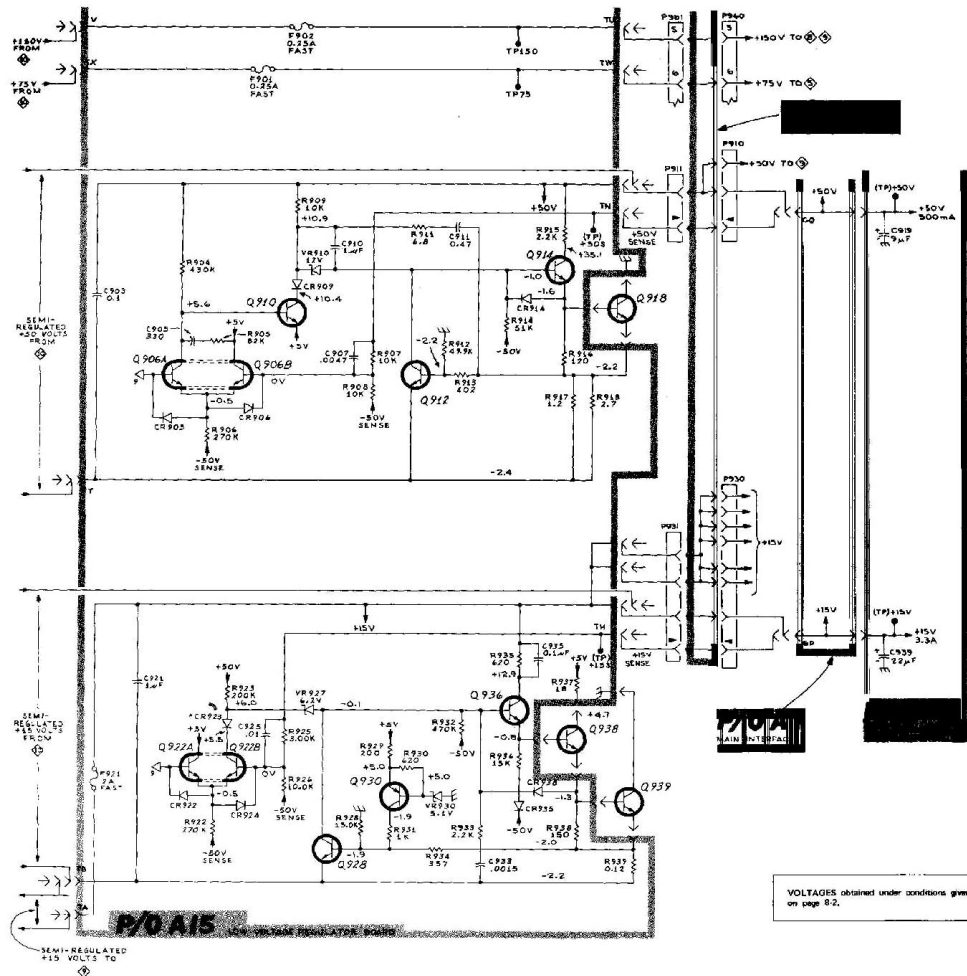


Fig. 8-24. A20 - Horizontal Mode Switch circuit board.

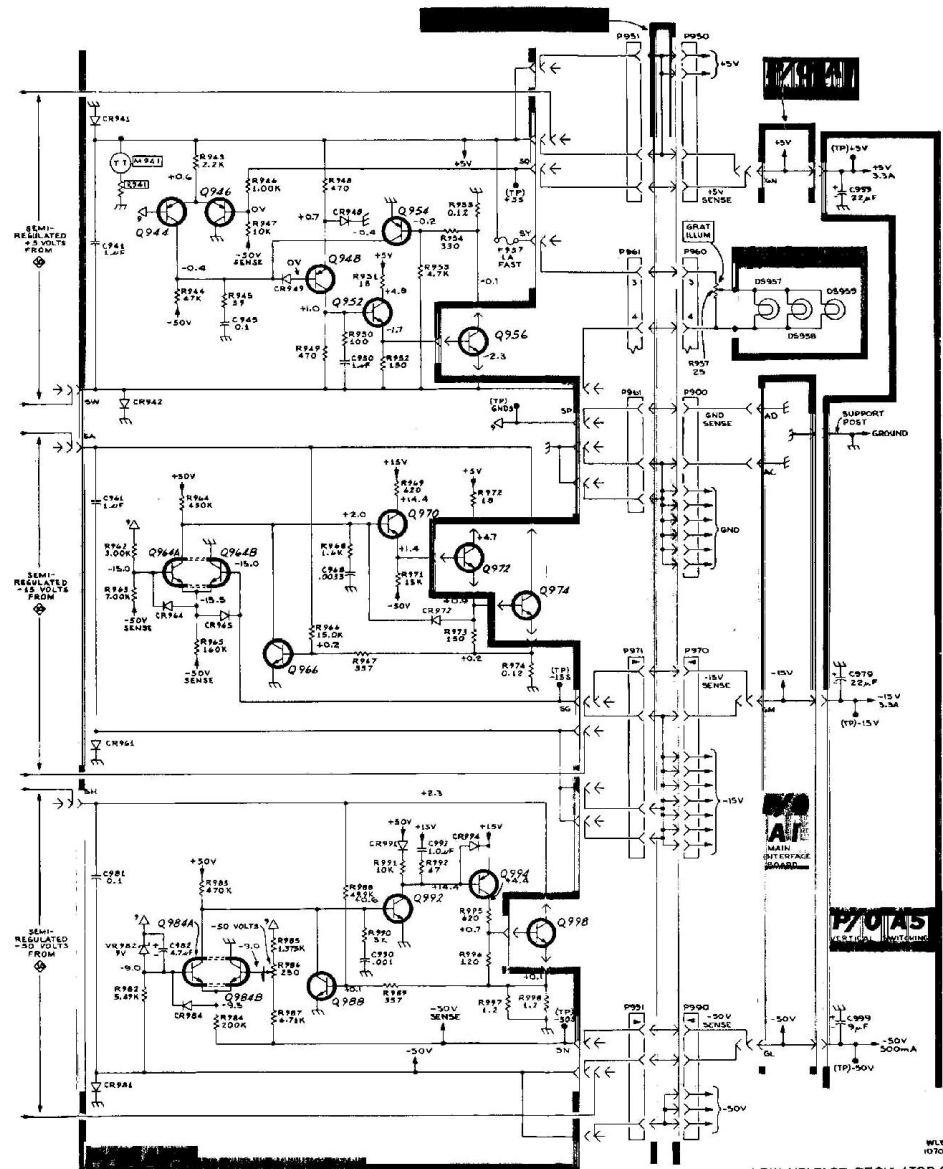




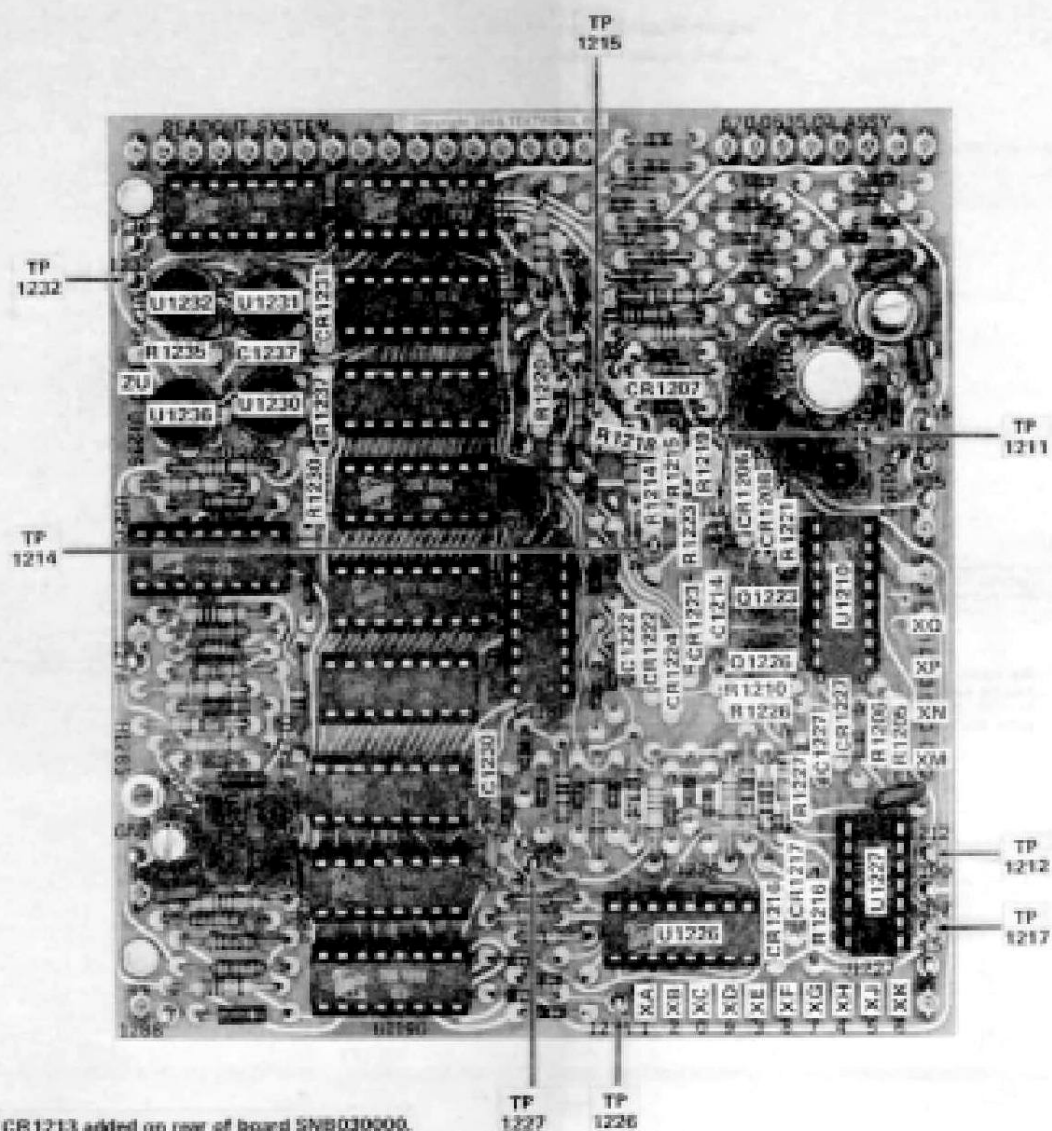
REFERENCE DIAGRAMS  
 ⊕ VERTICAL AMPLIFIER  
 ⊕ OUTPUT SIGNALS & CALIBRATOR  
 ⊕ CRT CIRCUIT  
 ⊕ LINE TO DC CONVERTER/REGULATOR

NOTES:  
 1. SEE PARTS LIST FOR SEMICONDUCTOR TYPES.  
 2. SEPARATE GROUND SYSTEM.

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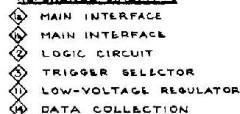
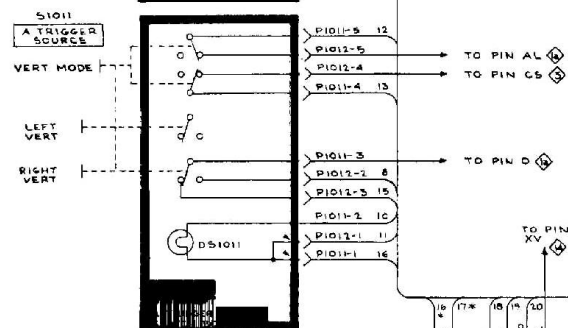


NOTES: CR1213 added on rear of board SNB030000.  
R1231 added on rear SN B040000.

See Figs. 8-26 and 8-27 for location of components not identified here.

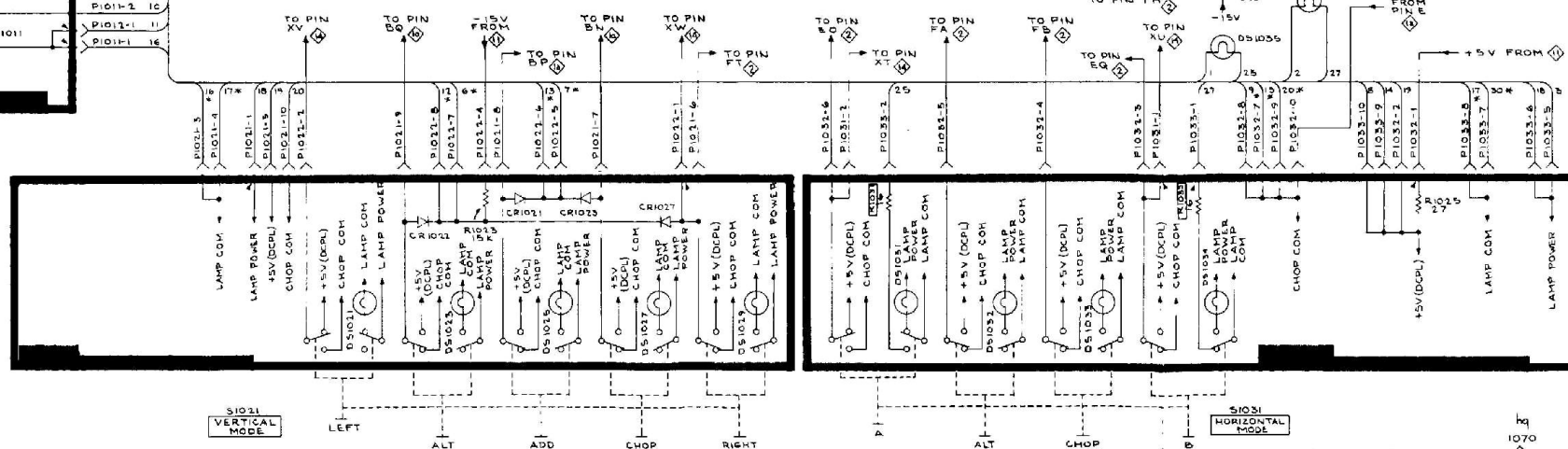
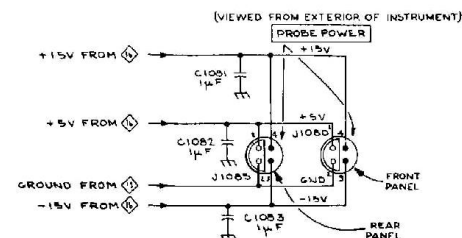


Figure 8-25. P/O A21 - Partial Readout System circuit board.



\* BREAK-OUT NUMBERS FOR REFERENCE, USE ONLY. WIRES OF THE SAME COLOR ON THE SAME CONNECTOR MAY BE INTERCHANGED IN INSTRUMENT

SEE PARTS LIST FOR EARLIER  
VALUES AND SERIAL NUMBER  
RANGES OF PARTS MARKED  
WITH BLUE OUTLINE.



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## CONTROLS & CABLING

1070  
12

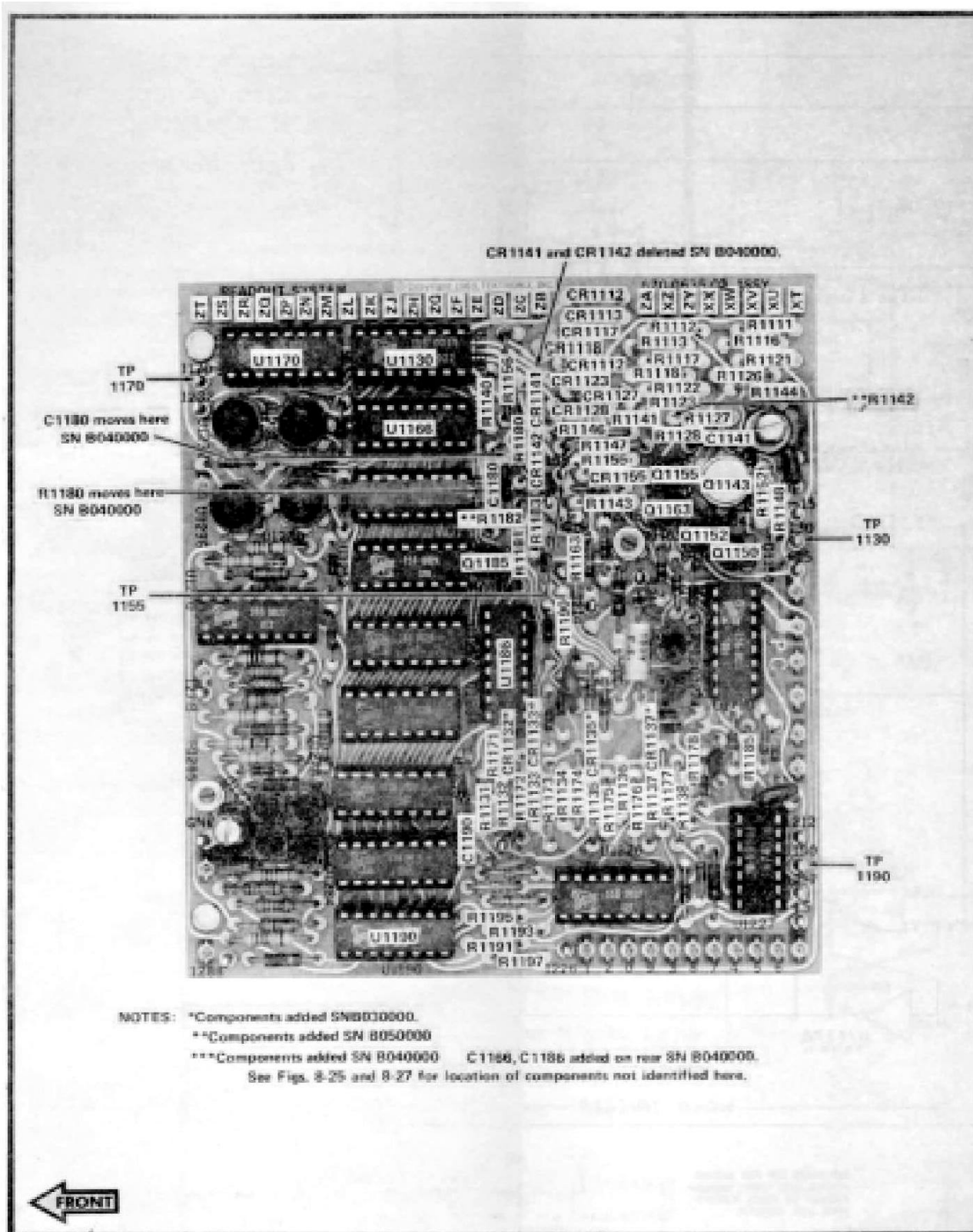
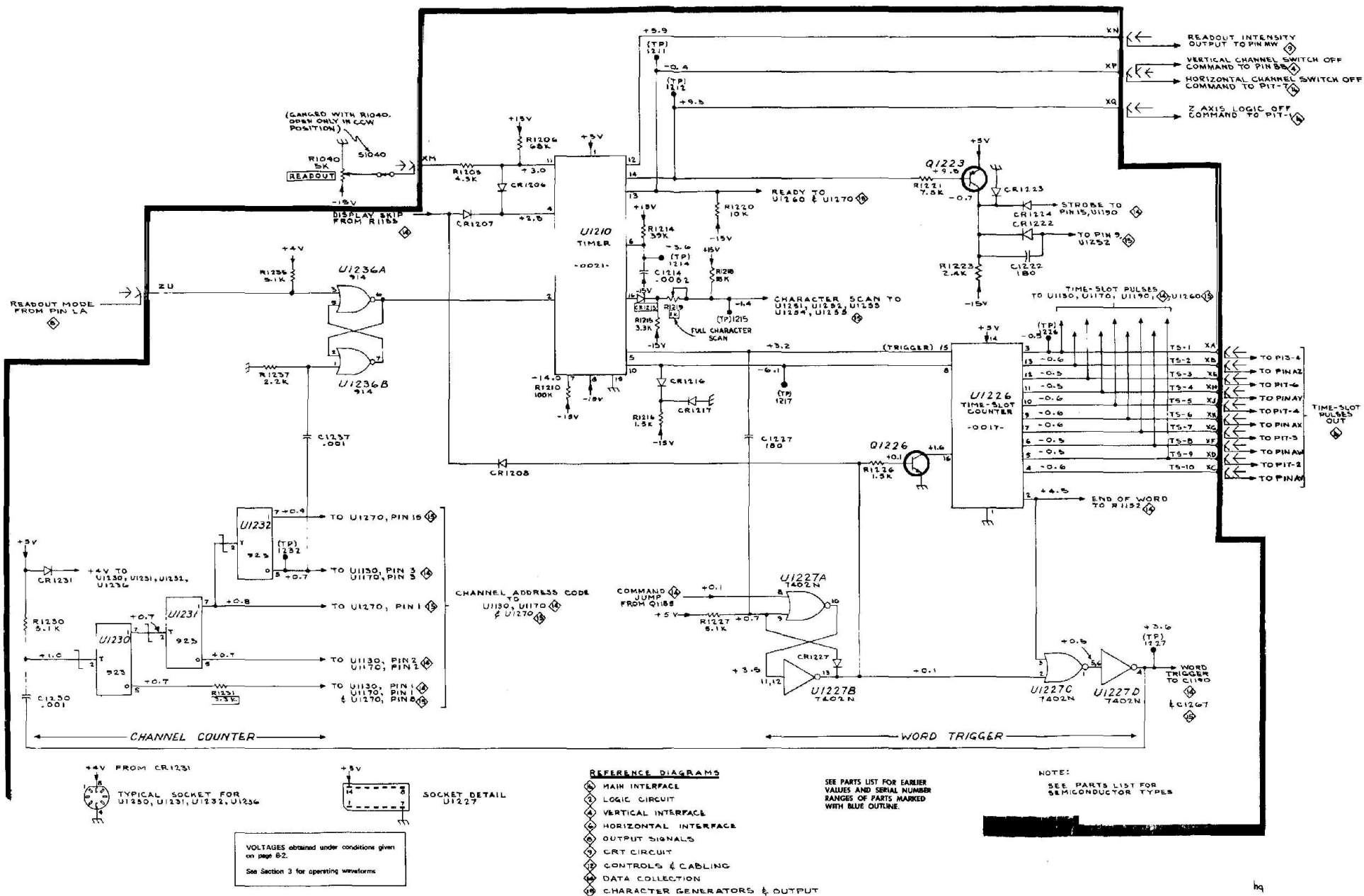
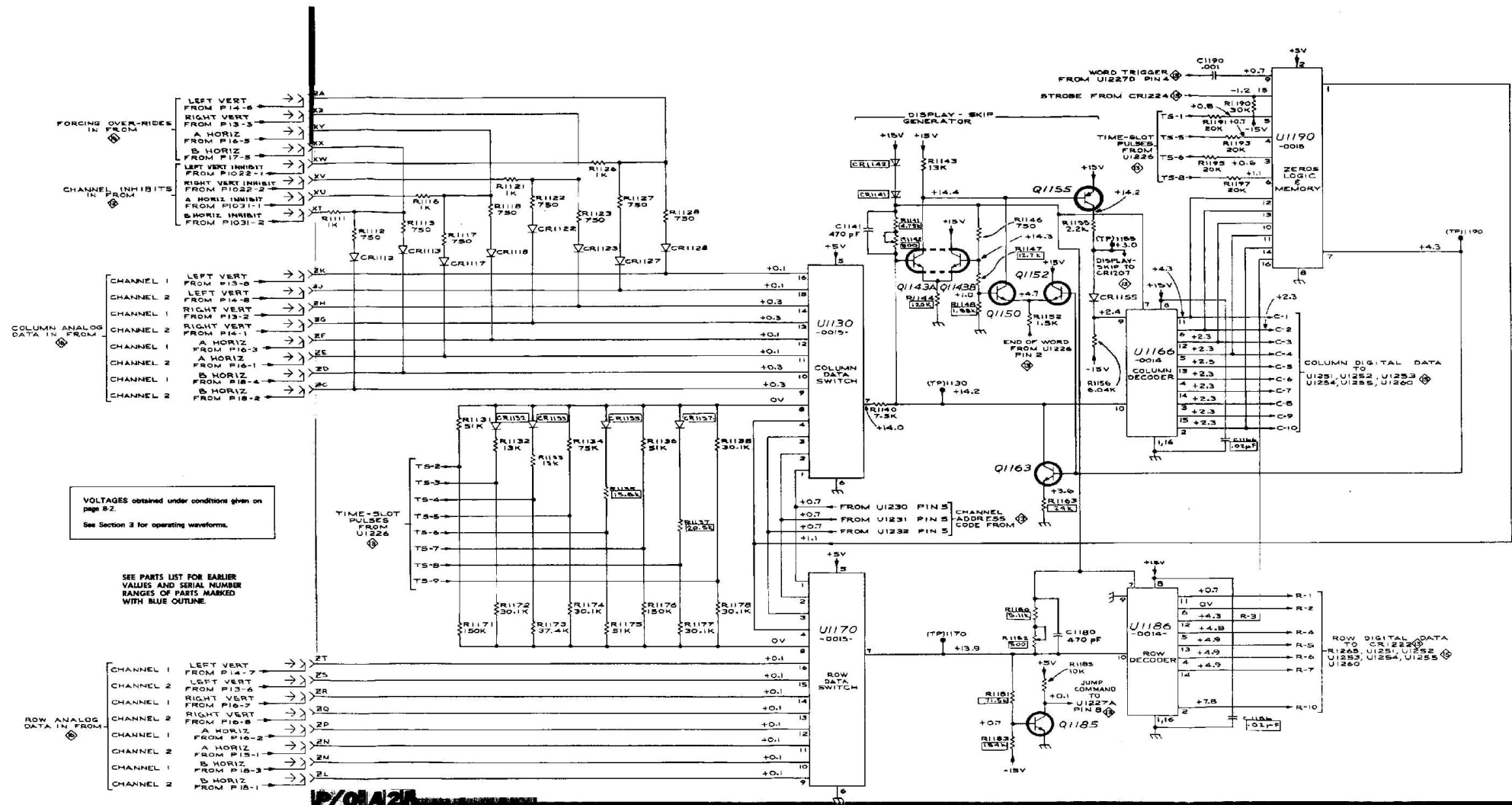
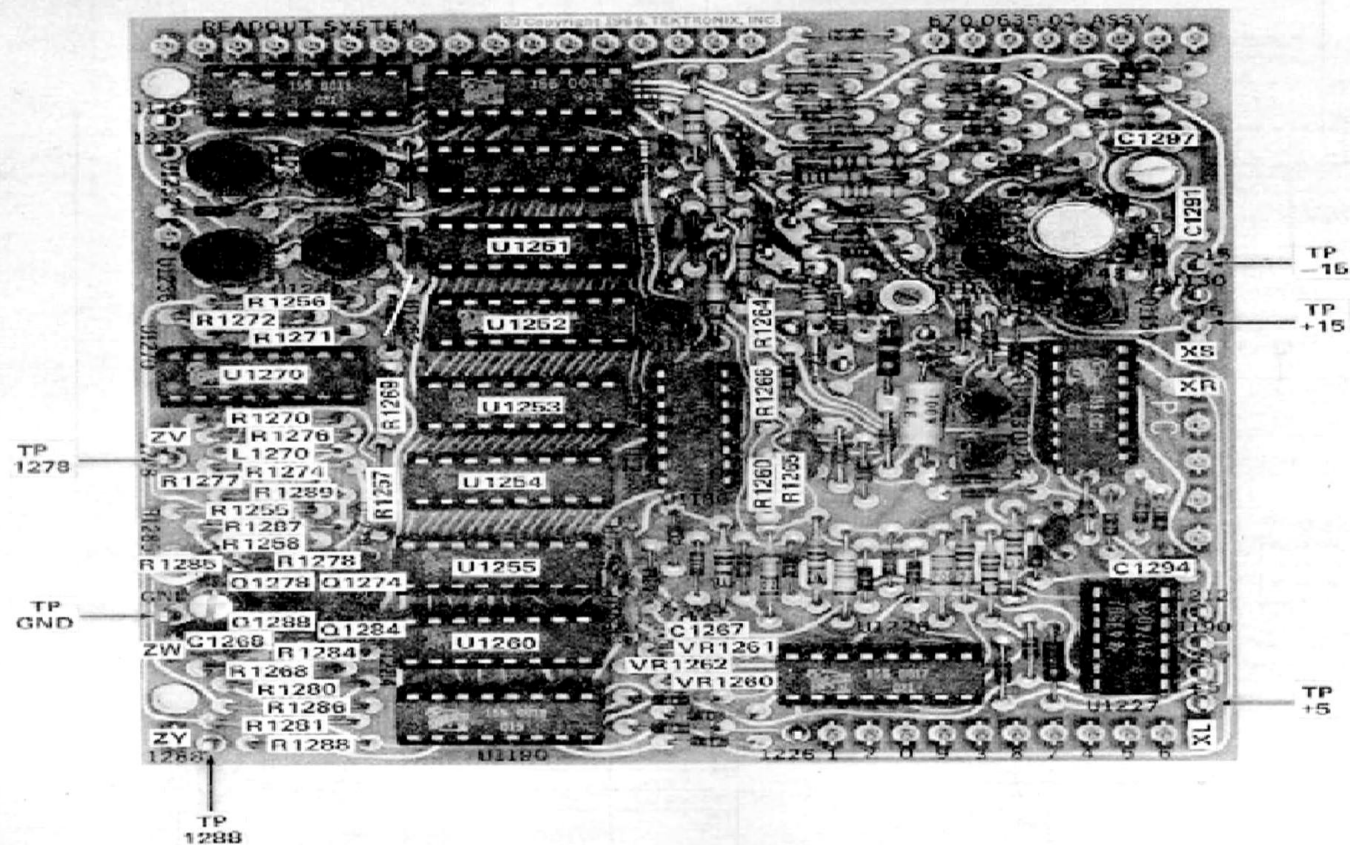


Fig. 8-26. P/O A21 - Partial Readout System circuit board.









See Figs. 8-25 and 8-26 for location of components not identified here.

Fig. 8-27. P/O A21 - partial Readout system circuit board.

