TECHNICAL MANUAL

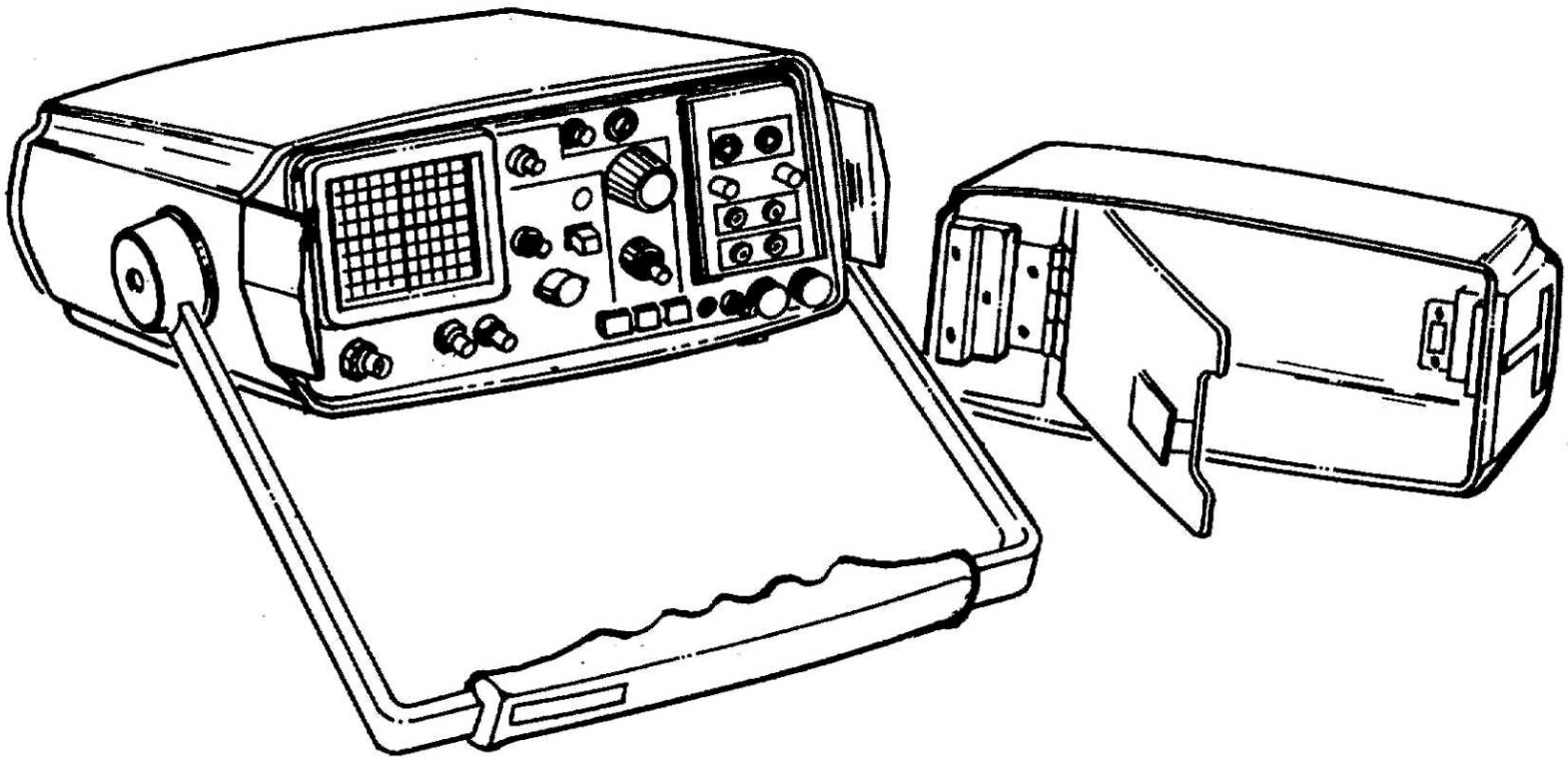
OPERATOR, ORGANIZATIONAL, AND DS/GS MAINTENANCE MANUAL

(INCLUDING REPAIR PARTS)

FOR

TEKTRONIX 1502 TIME DOMAIN REFLECTOMETER

AUGUST 1986



1792-01

1502 Time Domain Reflectometer.

REV A FEB 1980

SPECIFICATION

General Information

The Tektronix 1502 is a portable Time Domain Reflectometer that uses pulses to test cables and provides a visual display of cable faults. The test pulses are transmitted via the CABLE output jack. Reflections are received at the same jack and displayed on the Cathode-Ray Tube (crt).

NOTE

All distances are shown in feet followed by metres in parenthesis. Metric units are not direct conversions from the measurements shown in feet, but represent the calibrated ranges of the metric option 1502.

Calibrated distance controls allow an operator to examine up to 100 feet (25 metres) of cable with segments as small as 1 foot (25 cm) displayed horizontally across the 10-division crt screen. Low-loss cables as long as 2000 feet (500 metres) may be examined at 100 feet (25 metres) per division or 200 feet (50 metres) per division. The horizontal crt scale is calibrated directly in distance units from 0.1 foot (2.5 cm) per division to 200 feet (50 metres) per division in a 1-2-5 sequence (1-2.5-5 sequence).

A 3-digit, direct reading dial indicates the distance to any cable discontinuity when the dial is used to horizontally position the discontinuity's reflection to a crt reference line.

Vertical (Y-axis) deflection of the crt beam is proportional to the amplitude of the reflected signal plus the incident step. The vertical scale is calibrated in units of rho (ρ) of the transmitted pulse amplitude. For a definition of rho, refer to section 2 of this manual. The sensitivity scale can be selected in 7 calibrated steps from 5 mρ/div to 500 mρ/div.

The transmitted pulse is a step-signal having an amplitude of approximately 225 mV. The risetime of the pulse generator and the equivalent bandwidth of the deflection circuits provide a system reflected risetime of 140 ps or less.

The 1502 plug-in compartment will accept either the X-Y OUTPUT MODULE or the TEKTRONIX Y-T Chart Recorder. The X-Y OUTPUT MODULE is a standard accessory for the 1502 and provides an interface for an X-Y recorder. The TEKTRONIX Y-T Chart Recorder is an optional accessory. This recorder uses a heated stylus to record on 4 cm wide, heat-sensitive chart paper. The chart recording length represents the entire crt screen and is controlled by the 1502.

The 1502 is a ruggedized portable instrument that can be used in the field as well as in the laboratory. The requirements for a Type III, Class 3, Style A instrument as specified in MIL-T-28800 were used as a guideline for the environmental specifications. The 1502 has a ruggedized case that provides protection when the instrument is stored in exposed areas. When the instrument is not being used, the accessories, including the Operators manual, may be packed in the instrument cover and latched tightly on the front of the instrument. Table 1-1 indicates which accessories may be placed in the cover of the 1502.

The characteristics given in Table 1-2 apply over an ambient temperature range from -15°C to +55°C after the instrument has been calibrated at +25°C, ±5°C. Under these conditions, the 1502 will perform to the requirements given in the Performance Check section of this manual.

Table 1-1.
1502 ACCESSORIES

Accessories stored in the 1502 cover	
Accessory	**Tektronix Part Number**
1 50 Ω BNC Terminator	011-0123-00
1 Precision 50 Ω Cable	012-0482-00
1 Viewing Hood	016-0297-00
1 Operators Manual	070-1790-00
1 BNC Connector, Female-to-Female	103-0028-00
2 Replacement Fuses (for front panel) For 115 V ac Operation or For 230 V ac Operation (Option 6)	159-0113-00 159-0029-00
1 Power Cord	161-0066-00
1 Filter, Mesh (crt)	378-0055-00
Accessories not stored in the 1502 cover	
1 TDR Slide Rule	003-0700-00
1 X-Y Output Module	016-0606-00
1 Instruction Manual	070-1792-01

SPECIFICATION

The performance limits in this specification are valid with the following conditions:

The instrument must have been calibrated at an ambient temperature between +20°C and +30°C.

The instrument must have a warm up period of at least 20 minutes.

Table 1-2.
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
Excitation Step Pulse		Cable Dielectric set to AIR
Reflected Rise	≤0.07 feet (≤140 ps) ≤2.1 cm for metric	10% to 90%
Aberrations	±5% peak during 1st 10 feet (300 cm) after rise	
	±0.5% peak beyond 10 feet (300 cm)	Noise Filter "Out"
Jitter	≤0.02 feet (≤40 ps) ≤0.6 cm	Set at X.1 (Cable Dielectric set to AIR)
	≤0.1 feet (≤200 ps) ≤3 cm	Set at X1 (Cable Dielectric set to AIR)
Deflection Factor	5 m*p*/div to 500 m*p*/div	7 steps, 1-2-5 sequence
Accuracy	Within ±3%	
Gain	At least 3.5:1 from calibrated point	Screwdriver control
Display Noise	±5 m*p* or less, NOISE FILTER switch "Out"	Peak
Low Noise Operation	±2 m*p* or less, NOISE FILTER switch "in"	Peak
Distance Controls		0 to 2000 feet total
Distance Dial		
At X.1 Multiplier Range	0 to 100 feet 0 to 25 metres for metric	
Accuracy	Within ±2% ±0.05 feet Within ±2% ±0.05 metres for metric	from 2nd to 9th graticule lines
At X1 Multiplier Range	0 to 1000 feet 0 to 250 metres for metric	
Accuracy	Within ±2% ±0.5 feet Within ±2% ±0.5 metres for metric	from 2nd to 9th graticule lines

Table 1-2. (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
FEET/DIV Control At X.1 Multiplier Range	 To 20 feet/div To 5 metres/div for metric	
Scales	.1 feet/div to 20 feet/div 0.025 m/div to 5 m/div for metric	8 steps, 1-2-5 sequence 8 steps, 1-2.5-5 sequence
At X1 Multiplier Range	 To 200 feet/div To 50 metres/div for metric	 DISTANCE dial disabled in 200 (FIND) position
Scales	1 foot/div to 200 feet/div 0.25 m/div to 50 m/div for metric	8 steps, 1-2-5 sequence 8 steps, 1-2-5 sequence
Dielectric Scales	SOLID PTFE, V_p/V_{air}, = 0.70 SOLID POLY, V_p/V_{air} = 0.66 OTHER-VAR, V_p/V_{air}, = 0.55 to 1	$_r$= 2.04 $_r$= 2.31 VAR is calibrated for air when turned to full cw position. All buttons released causes default mode and is cal. for air
Accuracy	Within ±2%	
External Recorder Interface for X-Y Recorders Horizontal	 0.1 V/div	 Source impedance 10 kΩ
Vertical	0.09 to 0.13 V/div (adjustable)	Source impedance 10 kΩ
Pen Lift Mode 1 Source	 V_s = 5 V Nominal with R_s = 10 kΩ	
Mode 2 (inverted Mode 1) Source	 V_s = 5 V Nominal with R_s = 10 kΩ	
Y-T Plug-in Chart Recorder Interface Horizontal	 0.4 V/div	 Source impedance 200 Ω (switched)
Vertical	0.2 V/div	Source impedance 200 Ω (switched) The TEKTRONIX Chart Recorder, 016-0506-03 is designed to operate with the 1502. The chart uses a heat sensitive stylus to record on 4 cm chart paper. Chart recording length is controlled by the 1502.

Table 1-2. (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information		
Line Voltage	117 Vac ±20%, 48 to 410 Hz 234 Vac ±20%, 48 to 410 Hz	Fused at 0.5 A Fused at 0.3 A		
Battery Pack		C size 9 cell		
Operation	At least 5 hours	+20° C to +25° C charge and discharge temperature		
Full Charge Time		16 hours		
Typical Charge Capacity Charge Temperature		Discharge Temperature		
		-15°C	+20°C to +25°C	+55°C
0° C		40%	60%	50%
+20° C to +25° C		65%	100%	85%
+40° C		40%	65%	55%
Temperature Operating	-15° C to +55° C	At temperatures other than 20°C-25° C, the battery efficiency becomes restricted		
Non-Operating	-62° C to +85° C	With batteries removed. If stored with batteries storage range changed to -40° C to +55° C		
Humidity	To 100%			
Altitude Operating	10,000 feet			
Non-Operating	50,000 feet			
Vibration	3.0 g, 5 to 55 Hz; Test time 45 minutes			
Shock, Mechanical Shock, Pulse	15 g, 1/2 sine shock waveform of 11 ms duration. Total of 18 shocks			
Bench Handling Operating	4 drops each face at 4 inches or 45° with opposite edge as pivot	Case on		
Non-Operating	4 drops each face at 4 inches or 45° with opposite edge as pivot. Satisfactory operation after drops.	Case off		
Transit Drop	12 inch drop			

Table 1-2. (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
Water Resistance Operating	Splashproof and drip proof with cover off and instrument operating	
Non-Operating	Watertight with three feet of water above top of the case	Cover on
Salt Atmosphere Structural Parts	Withstand 48 hours exposure to 20% solution without corroding	
Explosive Atmosphere	Operation does not cause ignition of an ambient-explosive-gaseous mixture with air	
Sand and Dust	Operates after non-operating, cover removed, exposure to dust test of MIL-STD-810, Method 510, Proc. I	
Washability	Capable of being washed	
Electromagnetic Compatibility Electromagnetic Interference (EMI)	Meets requirements specified in Table X of MIL-T-28800A	
Magnetic Environment DC	Performs satisfactorily when 20 oersted dc applied	
AC	Performs satisfactorily when 5 oersted RMS ac applied	
Fungus Inert	Materials used are fungus inert	
Weight With Panel Cover and Accessories	18 pounds (8.2 kg)	
Without Panel Cover and Accessories	16.0 pounds (7.3 kg)	
Domestic Shipping Weight	24.4 pounds (11.1 kg)	
Export Shipping Weight	Approximately 36.0 pounds (16.4 kg)	
Height	5.0 inches (12.7 cm)	
Width With Handle	12.4 inches (31.5 cm)	
Without Handle	11.8 inches (29.9 cm)	

Table 1-2. (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
Depth Including Panel Cover	16.5 inches (41.9 cm)	
Handle Extended	18.7 inches (47.4 cm)	

THEORY OF OPERATION

This section describes the circuits of the 1502 using a combination of block and circuit diagrams on pull-outs from the back of this manual.

Block Diagrams

There are two block diagrams that show the overall functions of the 1502; Fig. 3-1, a simplified version, and the main block diagram located on a pull-out.

Circuit Operation

The 1502 uses pulses to check cable conditions. The Pulser circuits transmit the pulses down the cable under test, and the Sampler circuits sample the reflections and provide the vertical signal for display on the crt.

The Pulser is basically a tunnel diode in a 50 Ω strip line (cavity). It contains all biasing and timing circuits required for operation of tunnel diode, CR1703.

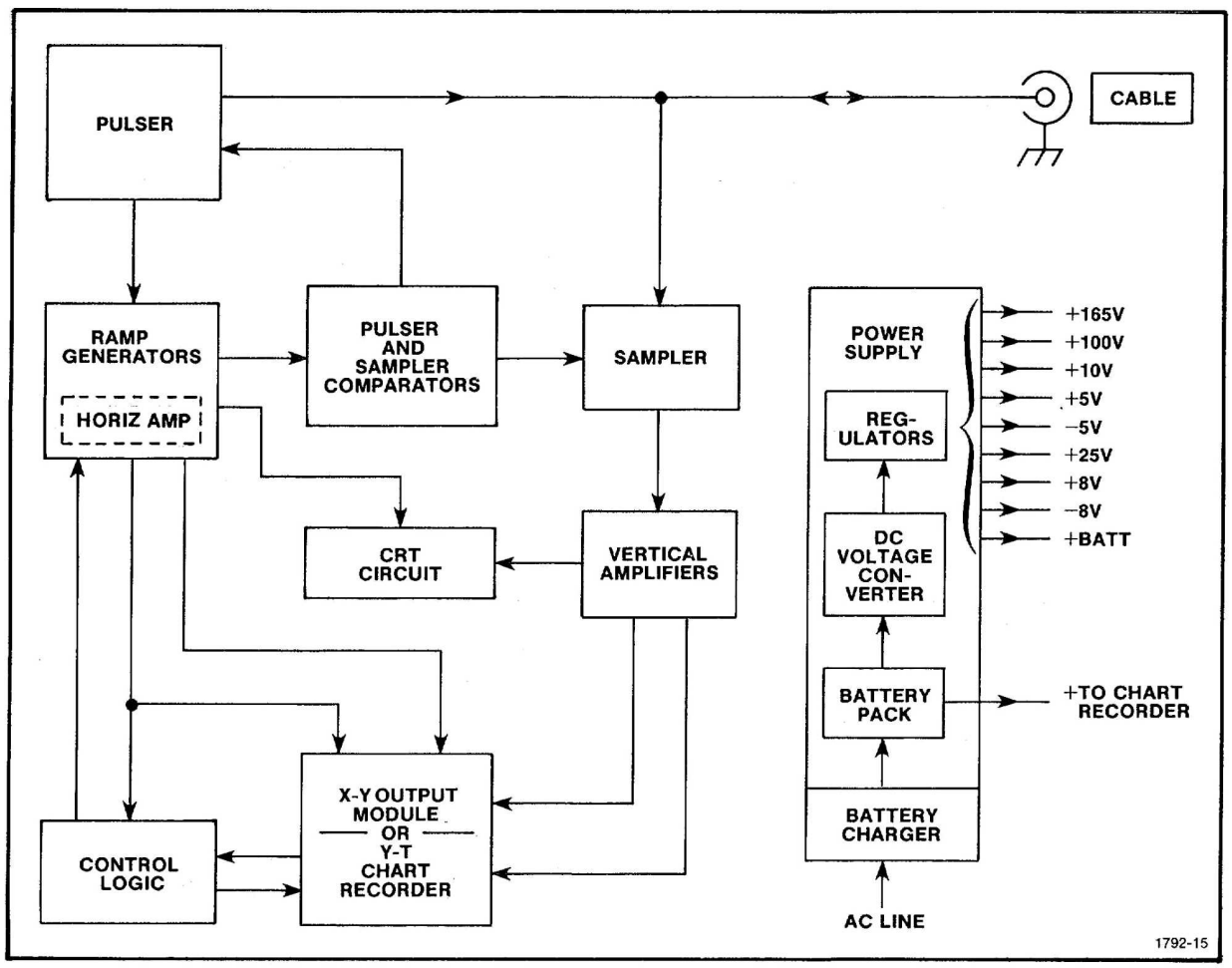


Figure 3-1. Simplified Block Diagram-1502

Sequential equivalent-time sampling is used to develop a display. Two ramps are generated, a fast ramp and a slow ramp. The fast ramp is compared to the slow ramp or a fixed reference to generate trigger pulses for the Sampler and the Pulser respectively. These comparisons are made by the Pulser and Sampler Comparators.

A short time after the Pulser transmits the step pulse into the cable under test, depending on the amplitude of the slow and fast ramps, a sampling trigger from the Sampler Comparator causes the Sampler to sample-and-hold the voltage level appearing at that time. This voltage is taken at the point where the Sampler is connected to the 50 Ω strip line. This voltage sample is amplified and sent through the vertical amplifiers to the crt.

The Slow Ramp Generator provides the horizontal sweep for the crt and, combined with the vertical sample, provides a display of the sampled value. Sampling triggers, taken later during the next fast ramp time, cause additional samples to be displayed next to the first one, until a line of very short dashes are formed across the crt, appearing as a solid line (Fig. 3-2).

The amplified vertical and ramp signals are also sent to X-Y Interface connectors. These signals, along with a pen lift control signal, provide the information for driving external X-Y recorders.

If the TEKTRONIX Y-T Chart Recorder is used, the amplified vertical signals from the Sampler are applied to the writing stylus drive circuits. The speed of the chart paper is derived by the holes along the edge of the chart paper passing between a phototransistor and a light-emitting diode providing digital information to the Control Logic. The Control Logic uses this information to control the slope of the slow ramp so as to match the speed of the chart paper. Thus, the trace and grid on the chart recording correlates to the trace and graticule displayed on the crt.

When the horizontal scan of the crt has been completed, the vertical input is automatically disconnected and the slow ramp is released to scan at its own speed. The chart paper continues to run until the entire recorded data is outside the chart recorder.

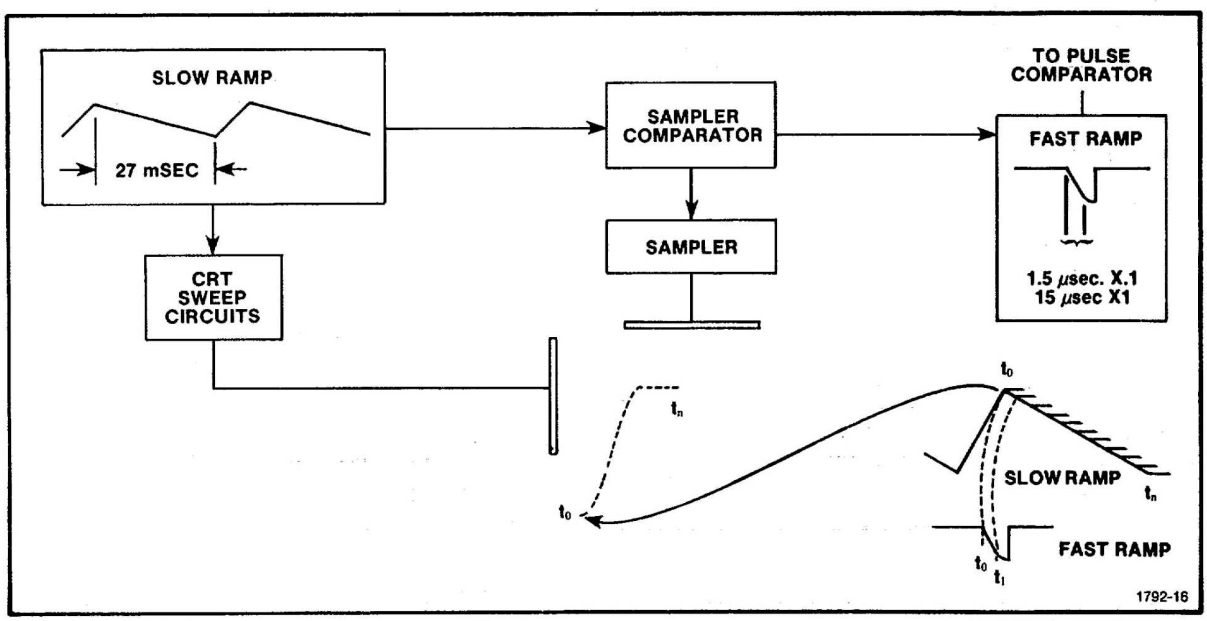


Figure 3-2. Sampling Diagram.

DETAILED CIRCUIT DESCRIPTION

Pulser

The Pulser consists of three circuits: a Clock Generator, a Logic Programmer, and a Pulse Generator. These circuits provide a signal for the fast ramp generator called the FAST RAMP START, and provide timing for firing the tunnel diode, CR1703. A complete programming cycle consists of six equally divided time slots derived from the 60 kHz Clock Generator output. The Logic Programmer develops the timing pulses from the Clock Generator output to control bias level timing on the tunnel diode and the duration of the Fast Ramp Generator.

The Pulser uses a two step process to generate a test pulse. Two steps are used to automatically bias the tunnel diode. The first step checks the peak current point of the tunnel diode then stores the firing voltage level on Memory Capacitor C1596. The second step uses the voltage stored on C1596 and an additional pulse (TD TRIGGER) to fire the tunnel diode and transmit the test pulse to the CABLE connector. This peak current check is performed for each Programming cycle. Thus, the automatic bias corrects for tunnel diode aging, thermal effects, and loading variations. Biasing action on the tunnel diode during each time slot is as shown in Fig. 3-3 and described as follows:

Time Slot 1. All current is removed from the tunnel diode to reset it to its low state. The low state is on the low voltage side of the peak current point on the voltage-current curve of the tunnel diode (Fig. 3-4).

Time Slot 2. Bias current is applied to the tunnel diode so that the current is raised to just below the minimum peak current point (depending on the tolerance of the tunnel diode characteristics).

Time Slot 3. A current ramp is added to the bias current until the tunnel diode fires. After firing, the tunnel diode current is reduced to a predetermined amount where it remains for the rest of time slot 3.

Time Slot 4. All current is removed to reset the tunnel diode to the low state. This completes the first pulse and the firing level of the tunnel diode is now just above the voltage stored in capacitor C1596.

Time Slot 5. This is a waiting period where currents are allowed to stabilize.

Time Slot 6. The tunnel diode is fired by TD TRIGGER from the Pulse Comparator. The fast ramp makes its sweep and the Sampler takes its sample during this time.

Clock Generator. The Clock Generator consists of two inverters, U1575A and U1575B, which act as an astable multivibrator. The output signal is a square wave about 60 kHz, as determined by C1572 and R1574. R1577 protects the input to U1575B. The square wave is applied to a divide-by-six counter in the Logic Programmer.

Logic Programmer. The Logic Programmer provides the needed logic sequence to allow automatic tunnel diode biasing and sampler synchronization. It consists of a divide-by-six counter, U1569, and gates U1575C, U1575D, and U1671. A cycle is completed after every six clock inputs (Fig. 3-3). $\overline{Q1}$ starts going high at the start of the clock pulse train and remains high for three clock pulses, then goes low for the next three clock pulses.

The outputs ($\overline{Q1}$ through $\overline{Q5}$) of the counter go to gates U1575C, U1575D, and U1671. The output of U1575C is called FAST RAMP START and controls the duration of the fast ramp generator. It is in the low state for the first five clock cycles and in the high state for the sixth clock cycle (see Fig. 3-3b).

The output of U1575D, MEMORY RESET, is used to reset the biasing level of tunnel diode CR1703. By turning Q1597 on, the charging current to C1596 is shunted to ground, and any voltage on this capacitor is removed. This occurs during the first 2 time slots (see Fig. 3-3c).

The output of gate U1671D resets the tunnel diode during time slots 1 and 4, accomplished by diverting the current for the tunnel diode to ground through Q1602. This causes the tunnel diode to turn off. The reset action occurs each time after the tunnel diode is fired (shown in Fig. 3-3d).

The output of U1671C is used to enable a comparator, Q1688 and Q1695, which senses when tunnel diode CR1703 goes into the high state during time slot 3 (see Fig. 3-3e).

Pulse Generator. The Pulse Generator consists of the high speed, 20 milliamp tunnel diode, CR1703, and the tunnel diode bias control circuits. It generates the test output pulses to the CABLE connector.

The voltage pulse across CR1703 is 400 mV with a risetime of about 50 ps. The low impedance of CR1703, combined with R1701, form a source impedance of 50 Ω. This circuit provides a 200 mV step pulse to the CABLE connector.

Bias current for tunnel diode CR1703 is provided by R1601 and R1693. Transistors Q1602 and Q1603 serve as a switch to direct the current through the tunnel diode via Q1603 or to divert the current to ground via Q1602. TUNNEL DIODE RESET (U1671D output), which is high during time slots 1 and 4, is used to switch between Q1602 and Q1603. When the base of Q1583 goes high, its output to Q1589 goes low. The emitter of Q1589 goes low, turning Q1595 on, which turns Q1602 on (through Q1502) and Q1603 off (through Q1504). CR1703 is then off.

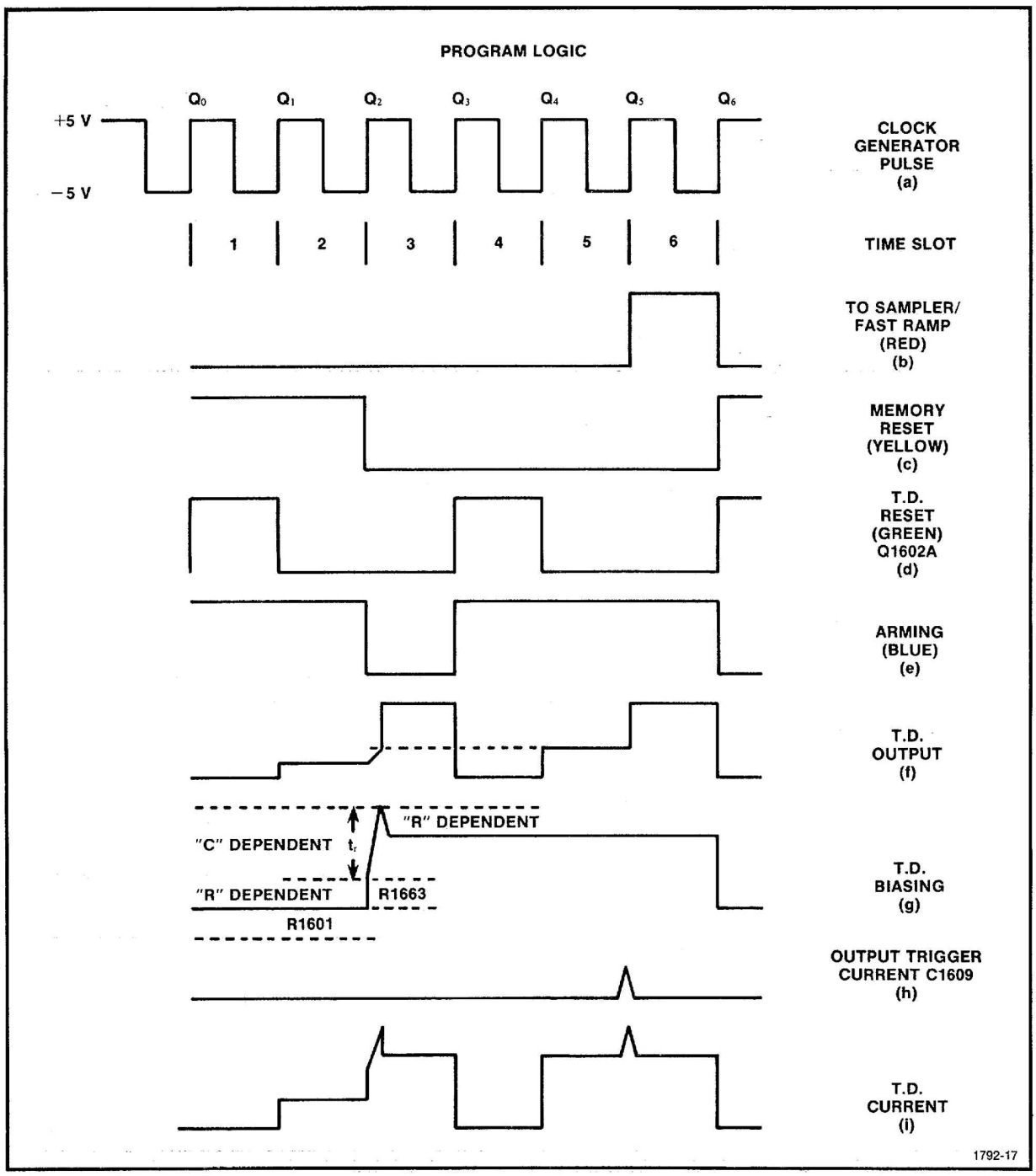


Figure 3-3. Program Logic Cycle.

During time slots 1 and 2,Q1597 is saturated, discharging memory capacitor C1596. At the start of time slot 3, Q1597 is cut off, allowing the current through CR1691 and R1691 to charge C1596 via R1692 and R1594. (C1596, R1692, and R1594 compose the memory circuit). This causes the gate voltage of Q1693 to be stepped up to a value determined by voltage divider R1691, R1692, and R1594 and then increase with a time constant rate determined by R1691, R1692, R1594, and C1596 (see Fig. 3-3g).

A current with a waveform similar to the voltage waveform at the gate of Q1693 will flow through R1693 and is added to the idle current from R1601. This current flows through Q1603 to output tunnel diode CR1703, and continues to increase until the tunnel diode goes into the high voltage state. At this point, comparator Q1695 and Q1688 cause Q1683 to remove the memory charge current. Thus, current stops flowing into C1596, causing the voltage ramp at the gate of Q1693 to stop and step-down. Similarly, the current ramp into the tunnel diode will stop and step-down.

The comparator consists of Q1695 and Q1688. Its reference is set at a negative level, except during time slot 3 when it is set at a positive 300 mV. The reference input voltage (the voltage at the base of Q1695) equals the tunnel diode voltage (which is always above ground level). These conditions cause Q1683 to saturate and remove the memory charging current. At the beginning of time slot 3, when the tunnel diode is still at its low voltage state, the comparison voltage is set at 300 mV. At this level Q1683 is not conducting, therefore, the memory charge current flows to the memory capacitor. When the tunnel diode fires, the comparator input voltage goes above the 300 mV comparison level. Q1683 becomes saturated again and the memory charge current is removed. The comparison reference levels are set by R1682, R1683, R1681, and Q1675. Factory selectable resistors R1702 and R1707, along with capacitors C1701 and C1706, are used to compensate for tunnel diode thermal time constants.

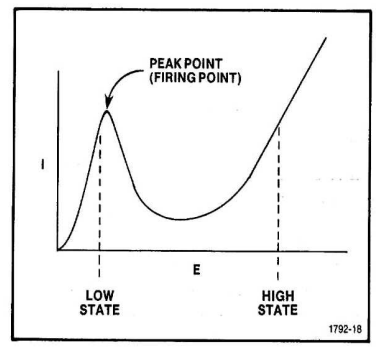


Figure 3-4. Tunnel Diode Voltage-Current Curve.

A tunnel diode, CR1609, is used to reduce jitter on the output step pulse. Q1608 conducts when TD TRIGGER is received from the pulser comparator during time slot 6. The current through Q1608 causes tunnel diode CR1609 to go to the high voltage state, producing a fast spike pulse through C1609 and R1701 to tunnel diode CR1703. This fires CR1703, sending the test pulse to the CABLE connector. Dc balance network, R1753, R1659, and C1655 provides an output of "zero" level when no test pulse is being generated, and if the CABLE terminations are not too extreme.

Sampler

The Sampler circuitry provides positive and negative strobes to strobe the sampling diodes, so that during a short time period (100 ps), a sample of the incident pulse or reflected signals can be taken. The sampling preamplifier amplifies these signals for display on the crt. The sampler consists of a Sampling Gate, Sampling Preamplifier, Strobe Generator, and Blowby Compensation.

Sampling Gate. Dual-diode Sampling Gate, CR1732, allows signals from the output terminal to appear at the preamplifier input for a short period of time. The bandwidth (or risetime) of the sampler is proportional to the conduction time of the diodes, which are controlled by the strobe width of the strobe generator.

Sampling Preamplifier. The Sampling Preamplifier consists of Q1648, Q1556, and Q1643. While strobing is occurring, a signal sample is taken from the transmission line and stored in capacitors C1635, C1636, C1637, C1638, C1646, and C1647. The preamplifier amplifies the charge stored in the capacitors. A positive feedback is provided by C1646 and C1647 to bring the sampling efficiency to unity. The sampling efficiency is adjustable by R1543.

The preamplifier has a gain of approximately 2 times, which is controlled by R1549 and R1651. R1639 and R1630 are needed to bleed off some of the reverse self-charge of C1637 and C1638. This allows the sampling gate to conduct during the peak amplitude of the strobes and thus determines the sampling aperature.

Strobe Generator. The Strobe Generator consists of preamplifier Q1553; signal-shaping amplifier Q1544 and Q1535; avalanche circuit Q1537; snap-off diode circuitry and strobe shaper, CR1632; and shorted strip lines.

A negative-going signal from the sampler comparator is amplified by Q1553 and the collector output is fed to a fast-rise one-shot multivibrator. A positive-going signal to Q1544 produces a negative-going signal on the base of Q1535, which results in a more positive-going signal on the base of Q1544. This action continues until both transistors are completely saturated, at which point TP1534 (violet test point) is at ground level. It will stay in this state as long as a charge remains on C1543. When this charge is depleted, the circuit resets and TP1534 returns to -5 volts. The fast positive edge at TP1534 is fed through C1534 into transformer T1538, which drives the avalanche circuit. Avalanche transistor Q1537 goes into its avalanche mode and the voltage across the transistor collapses very rapidly (300 ps). The collector voltage drops and the emitter voltage rises. These opposite signals are fed to the SNAP-OFF circuit by way of C1631 and C1632. The SNAP-OFF diode CR1632 is normally forward biased by a current from R1625 and R1633. This current is established by the emitter voltage of Q1539. The emitter voltage is controlled by R1538 (SNAP-OFF CURRENT). The negative-going signal of the avalanche circuit is applied to the anode of the SNAP-OFF diode and the positive-going signal is applied to the cathode to reverse bias this diode. After a small delay, the SNAP-OFF diode will become reverse biased. The reverse biasing occurs in less than 50 nanoseconds. The fast rising step from CR1632 is applied to the shorted strip lines. The width of the strobes is determined by the physical length of the shorted strip lines. The generated strobe is differentiated by capacitors C1635 and C1636 and then strobes the sampling diodes.

The avalanche voltage amplitude is controlled by R1525 with Q1529 acting as an emitter follower.

Blowby Compensation. The Blowby compensation network, Q1656, R1657, R1752, and R1656, cancels any signal component passing the gate due to diode shunt capacitance. This is accomplished by inverting the transmission line signal and adding it to the input of the preamplifier through C1648. The amount of compensation is set by R1657 and R1659 (LO FREQ COMP).

Comparators

There are two comparators; the Pulser Comparator and the Sampling Comparator. The Pulser Comparator provides the TD trigger signal to the Pulse Generator and the Sampler Comparator provides the Sampling Trigger signal to the Strobe Generator. Each comparator consists of a differential amplifier; Q1336 and Q1325 in the Sampler Comparator; and Q1347, Q1348 in the Pulser Comparator. The two comparators operate the same, therefore only the Sampler Comparator component numbers will be used in this description (see circuit diagram 1B).

The two inputs for the Sampler Comparator are the bases of Q1336 and Q1325. Depending on which input is higher, the voltage at TP1324 (green test point) will be +5 V or negative. If the base of Q1336 is high, Q1336 conducts and Q1325 is turned off. The current for Q1336 comes from Q1329 which turns Q1328 on. This puts the voltage at TP1324 high (+5 V). When the base of Q1336 is below that of Q1325, Q1336, Q1329 and Q1328 are turned off. Q1325 is conducting. The output voltage drops to the level of a conducting diode junction.

Q1425 and Q1431 form a temperature-compensated current source for the differential amplifier. The collector current of Q1431 is determined by the value of R1431 and R1422. It is approximately equal to the current of Q1425.

The second input of the Sampler Comparator is connected to the attenuated and inverted slow ramp signal. (The second input for the Pulser Comparator is a dc voltage that is controlled by the ZERO REF SET, R0151. The X.1 POSITION CAL control, R1132, compensates for unequal delays in the comparator when the speed of the Fast Ramp is changed (X1 to X.1).)

Ramp Generators

There are two ramp generators, the Fast Ramp Generator and the Slow Ramp Generator. The Fast Ramp is used for setting the X1 and X.1 distance timing. The Slow Ramp is used for the crt sweep and, when combined with the Fast Ramp, to create slewed strobes for the sampler.

Fast Ramp. The Fast Ramp Generator consists of amplifier Q1357 and Q1358; fast ramp clamp Q1338; current source Q1337 and Q1339; and timing capacitors C1325, C1237, and C1332.

Q1337 provides a constant current source for the timing capacitors to develop a linear voltage ramp across them. The magnitude of current can be precisely set with the FEET/DIV CAL, R1435. Q1339 is needed for thermal tracking. The timing capacitors are reset, at the end of time slot 6, by high speed ramp clamp Q1338. The ramp clamp is controlled by the pulse generator programmer through 01338 and Q1357. C1332 is a timing adjustment for the X.1 ramp. The Fast Ramp signal is supplied to the Sampler and Pulser Comparator.

Slow Ramp (Schematic 3). The Slow Ramp Generator consists of an integrator, a bi-level comparator, a positive current source, a negative current source, a retrace switch, and a retrace signal amplifier. A functional block diagram of the Slow Ramp Generator is shown in Fig. 3-5.

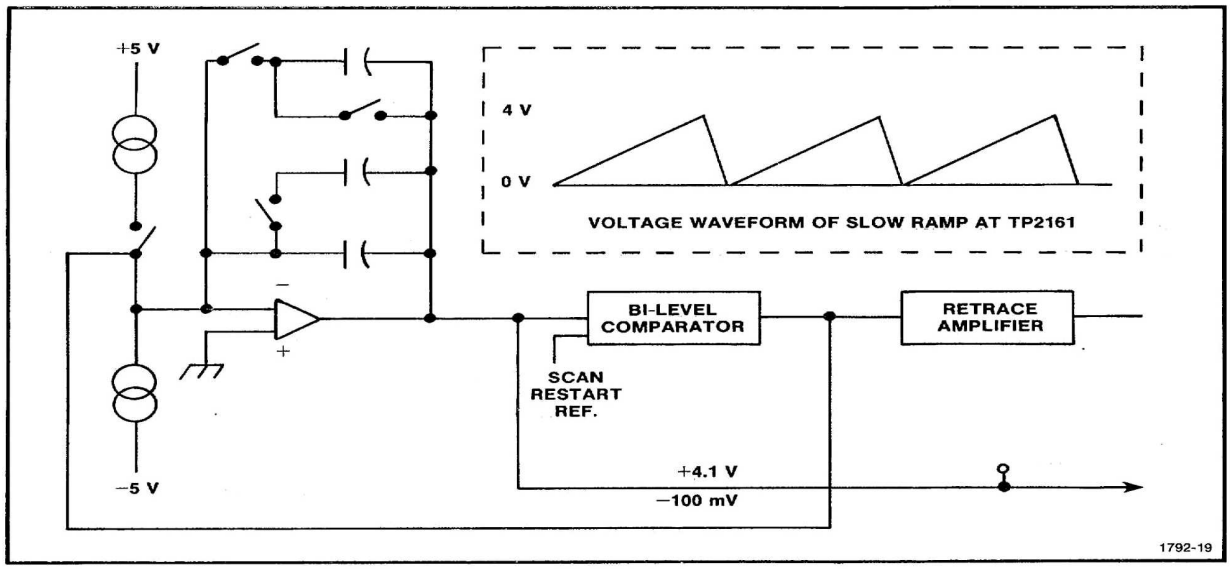


Figure 3-5. Functional Block Diagram of Slow Ramp Generator.

Integrator. An inverting amplifier circuit with an FET input is used as an integrator. Integrator capacitor C2356 is connected between the collector of Q2345 and the inverting input (gate of Q2246A). A minus current applied to the inverting input through R2353 results in a linear rising voltage on the output (see the waveform shown in Fig. 3-5). This output voltage will continue to rise until it reaches the internal comparison level of 4.1 volts. The bi-level comparator output then switches to a higher output level to close FET switch Q2257. It also changes its comparison level to -.1 V. This allows a positive current to be applied to the input of the integrator. The positive current is several times larger than the negative current and causes the output voltage of the integrator to decrease linearly. After a short period of time, the integrator output voltage approaches this comparison voltage of -0.1 V and causes the positive current into the integrator to be turned off. At this time the comparator level is switched back to the 4.1 V level and the cycle starts over.

The rise and fall time of the slow ramp can be varied by changing the integrating capacitance values. In the normal 40 Hz scan frequency, a value of 0.0013 μF is used. When NOISE FILTER switch S2254 is activated, the scan frequency is reduced by approximately 7 times by paralleling a capacitance value of 0.01 μF to the original 0.0013 μF. For recording (X-Y or chart) purposes, a value of 1 μF is used. (Q2248 acts as a FET switch and is controlled by the Record Logic.)

Bi-Level Comparator. During the positive going sequence of the Slow Ramp Generator, Q2261 is saturated and Q2262 is off. The emitter voltage of Q2261 and Q2262 is 4.1 volts. This voltage is controlled by a resistor divider, R2267 and R2158. The collector (output of the comparator) of Q2262 is at a -5 V level because the transistor is not conducting. The anode of CR2161 has to rise to 4.1 volts in order to turn off Q2261.

When Q2261 turns off, its collector level will decrease, which causes Q2262 to be turned on and saturated. The emitter voltage output switches to -0.1 volt. 02261 remains off until the anode voltage of CR2161 goes to -0.1 volt, which restarts the cycle.

The comparator can be forced into the scan cycle when the Recorder Logic turns on CR2262.

Retrace Signal Amplifier. The retrace signal amplifier uses an input FET (Q2258) to drive amplifier Q2259. The output voltage is +5 V during retrace and -5 V during the scan cycle. The output is used for Chart Recorder Logic and Record Logic.

Current Sources. The positive and negative currents for the retrace sweep are generated by applying +5 V and -5 V to the high value resistors R2251 and R2353 respectively.

Sweep Inverter with Horizontal Attenuator (Schematic 2)

The Sweep Inverter consists of an operational amplifier U1344; selectable input resistors, R1216, R1217, R1218, R1219, R1226, R1227, R1323, R1324 (which are selected by the FEET/DIV switch, S1222F) and selectable feedback resistors, R1148, R1146, R1152, which are selectable by the CABLE DIELECTRIC switch S1251.

Operational amplifier U1344 is connected in the circuit as an inverter. Its input voltage amplitude is determined by the position of FEET/DIV switch S1222F, whose input signal is the 4 volt, slow-ramp generator signal. The FEET/DIV control is selectable from 1 to 200 feet per division in a 1-2-5 sequence. The output of the FEET/DIV control is fed to the Sampler Comparator by way of voltage offset circuitry R1342 and R1239.

Feedback resistor R0472 is a variable range adjustment for the "OTHER" cable types; OTHER being any cable with a dielectric material other than solid polyethylene or solid polytetrafluoroethylene.

Distance Offset

The distance offset consists of a compensated current source Q1413, Q1317; a DISTANCE dial, R0271; and a ZERO REF CHECK switch, S0151.

The constant current of Q1413 is fed into the wiper of the variable DISTANCE resistor, R0271. The variable calibrated current of R0271 is fed into the summing junction of the Inverters operational amplifier, U1344. This occurs in all FEET/DIV settings except the 200 feet/div setting. When depressed, ZERO REF CHECK switch S0151 disables the offset current so that reference checks can be made. DISTANCE CAL resistor R1315 provides an adjustment for the calibrated current of Q1317.

Horizontal Output Amplifier (Schematic 4)

The Horizontal Output Amplifier consists of Q3221, Q3118, Q3113, and Q3114. This amplifier amplifies the 0-4 volt, slow ramp signal into a differential voltage of approximately 150 volts as well as shifting the output level to an average voltage of 85 V. This amplifier gain of approximately 37 times is achieved with a differential transistor amplifier, Q3221 and Q3118. The gain is controlled by the ratio of resistance R3122 or R3121, the parallel values of resistors R3217 and R3116, and resistors R3216 and R3212. R3217 is variable to adjust for crt deflection factor tolerances. The differential amplifier uses 0Q3113 and 0Q3114 as a current mirror current source. The thermally stable current is set by R3112, R3114, and R3115. R3213 is used for horizontal positioning.

X-Y Recorder Logic (Schematic 3)

The X-Y Recorder Logic consists of bi-stable multivibrator U2332B and U2332D; gates U2332A and U2332C and multiplex switches U3223A and U3223B. (U3223A and U3223B are on Schematics 3 and 4.)

During the normal mode of 1502 operation, the output of the multivibrator (PENLIFT: TP2157, yellow) is low and Q2248 is not conducting. Pin 10 of gate U2332C is low and Q2249 is not conducting. By pressing RECORD switch S0481B, the RECORD line goes high, the multivibrator changes level, and TP2157 becomes positive (+5 V). The output of U2332A (pin 3) goes low and the output of U2332C (pin 10) goes high. This turns Q2249 on. Q2249 keeps C2356 discharged and the output of the Slow Ramp remains at 0 V. By releasing the RECORD switch, the output of U2332C goes low, which turns Q2249 off. At the same time, Q2248 is on. This starts the Slow Ramp Generator scanning at a much slower rate due to C2252 being added to the circuit. When the scan cycle ends, the output of retrace amplifier Q2259 goes high, causing multivibrator U2332D and B to be reset. This sets the Recorder Logic back to the normal mode of operation.

Components CR2324, R2324, and C2325 are used to ensure that the Recorder Logic is in the normal mode of operation when the power supply switch is turned on.

Vertical Amplifier

The Vertical Amplifier circuit contains selectable gain amplifier U2136 with positioning control, variable gain amplifier U2143 to calibrate the instrument for different cable impedances, retrace logic with a fogging oscillator, and a vertical output amplifier.

Vertical Amplifier. This circuit consists of operational amplifier U2136, and a bank of resistors for gain selection. The required resistors are selected by switch S2126 (m*p*/DIV).

The operational amplifier is connected as a voltage follower. The non-inverting input receives its signal from the preamplifier through R2138 and the positioning signal from amplifier U2131 through R2137. High-frequency noise is filtered by 0.001 μF capacitor C2137. Additional noise filtering can be obtained by activating the NOISE FILTER switch, S2254, which adds 0.1 μF capacitor C2241 to the circuit.

Positioning. Vertical trace positioning is accomplished by offsetting the dc level of the vertical signal. Operational amplifier U2131 provides the dc offset voltage. U2131 is controlled by R0251A (POSITION) and R0251B (FINE).

Gain Amplifier. The Gain Amplifier consists of U2143 with variable gain provided by R0263. The incoming voltage is attenuated approximately 20% by R2228 and R2144. The output voltage is approximately 200 m*p* per division. The variable gain control has a range of approximately 5 times and is set by the values of R0263 and R2142. The output goes through the Retrace Logic to the Vertical Output Amplifier.

Retrace Logic (Schematic 4). The Retrace Logic consists of gate U3123C, inverter Q3137, oscillator U3123A and U3123D, and analog switches U3223C and U3223D.

The only time the vertical signal is applied to the vertical output amplifier is during the forward scanning cycle. During the retrace cycle, an offset voltage is applied to the vertical output amplifier.

During the slow ramp forward scan cycle, the retrace signal is negative, as is pin 2 of U3123A. This causes the output of U3123D to be low. Pin 6 of U3223C is also high and the vertical signal is passed through the analog gate to the output amplifier.

During the retrace cycle, the output of U3123D is high, but pin 6 of U3223C is low and pin 12 of U3223D is high. This allows the output of U3123D to be passed to the vertical output amplifier, which causes the beam to be deflected below the crt viewing area.

Vertical Output Amplifier. The Vertical Output amplifier consists of Q3236, Q3232, Q3139, and Q3235. The mode of operation is identical to that of the Horizontal Output Amplifier. In the Vertical Output Amplifier, the amplifier gain is approximately 80. Capacitor C3233 is added to increase high frequency response.

CRT Display Circuits (Schematic 4)

The crt display circuit High Voltage Supply provides the voltage for the FOCUS control, INTENSITY control, and the cathode of the crt and the crt biasing network. The crt provides a display of the conditions of the cable being checked and is also shown in the circuit.

High Voltage. The high voltage circuit consists of: an oscillator, formed by transistors Q4149 and Q4145; transformer T4141; a high voltage multiplier circuit consisting of CR4323, CR4313, CR4311, and CR4211, and a resistor divider string consisting of R4114, R4126, R4222, R4129, and R4221, INTENSITY control R0442, and FOCUS control R0432.

The self-starting oscillator is formed by R4146, R4141, and transformer T4241. The transformer has a separate feedback winding (pins 9, 10, 11), which ac couples the voltage to the bases of the transistors (Q4149 and 04145). R4146 and R4141, along with the 0.001 μF capacitors (C4135 or C4134), establish a time-constant that prevents saturation and controls the oscillator frequency.

Winding 7-8 of the transformer provides a 0.6 volt rms signal for the crt filament. This winding is high voltage insulated. Winding 4-6 provides a 500 volt square wave that is used to generate the high voltage. The high voltage multiplier circuit converts the 500 volts to 2000 volts. A resistor divider string is connected between the 2000 volt and the 1000 volt taps of the multiplier circuit. This provides the voltages for correct biasing of the crt. The FOCUS and INTENSITY controls are included in this divider string. A 150 volt zener diode, VR4117, is used to stabilize the cathode voltage.

Cathode-Ray Tube. In order to optimize the crt display, internal controls for Astigmatism, Geometry, and Trace Rotation are provided. These controls, which are located on the output board, are: R3148, R3149, R3242 (ASTIGMATISM); R3249, R3248 (GEOMETRY); and R3142, R3143 (TRACE ROTATION).

Power Supply (Schematic 6)

The Power Supply consists of a line selector, transformer T0389, a battery charger network, battery pack BT0369, and the dc voltage converters. The battery charger network contains SCR switch Q6155, SCR triggering circuit Q6143, Q6244, and Q6241, operational amplifier U6138, and the current reference resistor R6131.

In the dc voltage converters, there is an Anti-Deep Discharge circuit, Q6548, Q6549, and Q6547; a primary regulator, Q6552, Q6557, and VR6459; a controllable oscillator, Q6458, Q6445, C6551, R6545; a fly-back switch, Q6435 and Q6349; and fly-back transformer T6535. The secondary output windings of T6535 provide the +165 V, +100 V, +25 V, +10 V, +8 V, -8 V, +5 V, and -5 V supplies. The +10 V, +5 V, and -5 V circuits have secondary regulation circuitry. See Fig. 3-6 for a simplified block diagram of the power supply.

Line Selector. The line selector is composed of the input transformer's terminals and can be wired for either 110 volts or 220 volts. It is factory wired for 110 volts. If 220 volt operation is required, remove the wire straps from lugs 1-2 and 3-4 of T0389; then connect a strap from lug 2 to lug 3.

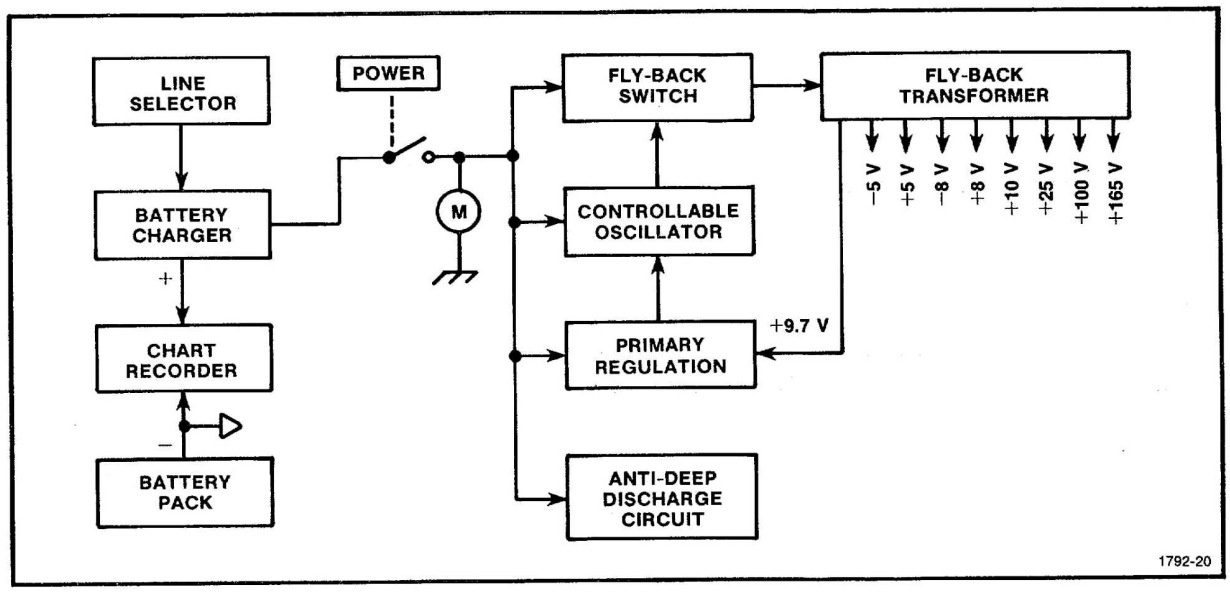


Figure 3-6. Block Diagram of 1502 Power Supply.

CAUTION

If the instrument is wired for 220 V operation, be sure that the two front panel fuses are changed. See the electrical parts list for proper fuse size.

Battery Charger. Line transformer T0389 provides battery charge current. The battery charge current is regulated for an average current of 150 mA (independent of battery load).

A reference voltage of approximately 50 mV is created across reference resistor R6132. This voltage is created by R6135 and VR6134. The battery load and charge current are always fed through R6131 and the charger will try to maintain an average current of 150 mA into the battery. This is done by comparing the voltages across two reference resistors (R6132 and R6131) using operational amplifier U6138. Depending upon the battery charge current, the output of the operational amplifier will provide more or less current into the current source input Q6244. With every new cycle, a current (of the same magnitude as the input current) will be released by Q6241 to charge capacitor C6147. Full wave rectification is provided by CR6157. The voltage across C6147 builds up every cycle until it reaches the firing threshold level of the programmable unijunction transistor (PUT) Q6143. At this moment, a triggered pulse occurs at the cathode of the PUT, which in turn fires SCR Q6155. When this occurs, a portion of the full-wave rectifier output provides a charge current for the battery during the remainder of the cycle. During this same period, C6147 gets discharged through the anode of the PUT. The point at which the triggering occurs is determined by how fast C6147 becomes charged to the reference voltage of about 4.5 V and the charging speed is determined by the average current to the battery.

Because the charge current and load currents are in the form of pulses, averaging (integration) is performed at the output of operational amplifier U6138 by a 15 μF capacitor C6233. Zener diode VR6134 provides protection in case the battery pack is removed and the line cord is plugged into a line-voltage source. Battery pack BT0369 consists of nine nickel-cadmium C cells.

NOTE

For proper operation, the battery pack must be in place at all times during operation of the instrument.

DC Voltage Converter. The controllable oscillator is an astable multivibrator (Q6458 and Q6445). Its output voltage is high for 8 us and low during the remainder of the period. The 8 μs period is set by C6551 and R6545 in parallel with R6449 and R6457. The low voltage duration at the output is controlled by the primary regulation voltage of Q6552, R6454, and C6451. Diode CR6452, R6451, and R6453 protect against base-emitter reverse breakdown voltage.

The output of the astable multivibrator is connected to the fly-back switching circuitry consisting of Q6349 (an emitter follower) and Q6435 (a high current switch). Q6435 conducts when the output of the multivibrator is high, so a magnetic field builds up in fly-back transformer T6535 by way of windings 5-6 during the 8p s period. When Q6435 turns off, the field collapses and the stored energy is transferred to the secondary windings. Diodes CR6347, CR6441 and CR6442 prevent Q6435 from saturating, causing the switch-off time to be faster. To reduce the base drive energy, a voltage source that is lower than the battery pack is used. This is supplied from terminal 3 of T6535.

The +25 V (pre-regulated) supply is used to control the primary regulation. (It is also used for the high voltage circuitry.) A voltage tap is provided by way of R6358 and Q6357 to create 9.7 V as a reference voltage for the primary regulator network. This voltage is compared against the combined voltage of 9.1 V zener diode VR6459 and the base-emitter junction of Q6557. Depending on the voltage level of the 25 volt supply, Q6557 increases or decreases conduction. The amplified collector voltage is fed to astable multivibrator Q6458 and Q6445 by way of emitter-follower Q6552. This controls the low voltage output duration of the astable multivibrator.

Anti-Deep-Discharge Circuit. The Anti-Deep Discharge circuit prevents the battery pack from going into deep discharge, which could permanently damage the batteries. Q6549 and Q6547 are connected as an SCR network. When fired, both transistors fully conduct, which forces the collector of Q6557 to ground. This removes all the input voltage to the input of the astable multivibrator, which turns it off and disables the dc voltage converter.

The SCR network can be triggered when Q6548 conducts. This happens when the battery voltage drops below 10 volts. The +25 V and +10 V power supplies are used as reference voltages by way of R6549, CR6546, and R6539. To reset this SCR network, the battery voltage must be removed by turning off the front panel POWER switch. The batteries must be charged or replaced (unless ac power is to be used) before further operation of the instrument.

Voltage Regulators. The +165 V, +100 V, +8 V, and -8 V supplies are not individually adjustable. R6358 is used to adjust the +25 V supply to the correct output voltage. The +10 V regulator provides a 10 volt reference for the +5 V and -5 V regulators.

The 5.1 V zener diode, VR7417, is used in a bridge configuration to provide a reference voltage for the +10 V supply. R6518, R6513, R6413, and R6514 are part of this bridge network. The bridge outputs are fed into operational amplifier U6515, which drives series regulator Q6427. Zener diode VR6419 is used as a start-up circuit. Capacitor C6416 provides additional power supply filtering. In order to reduce the energy or power losses, Q6427 has only a 2 volt collector-to-emitter drop.

Q6331 is the series regulator for the +5 V power supply. The +5 V is referenced against the +10 V with operational amplifier U6236. The output of U6326 drives the series regulator in an emitter-follower mode.

The -5 V power supply uses Q6227 as a series regulator. U6222 is used as a controlled current source and the minus voltage connection (VEE) is connected to the base of the series regulator. The standing amplifier current is shunted by R6222 and only the load fluctuations are used to control Q6227. R6223 is a current limiter.

Control Logic (Schematic 5)

The Logic board is only used with the TEKTRONIX Y-T Chart Recorder. This board can be removed without affecting the operation of the 1502. However, if this board is removed, the RECORD switch would have to be connected to the Vertical board by connecting the cable from the RECORD switch to P28 on the Vertical board.

The Logic board consists of pulse shaper, U5166A, U5166B, U5166C, and U5166D; binary counter U5147; a horizontal correction network; Chart Recorder Logic for controlling the paper drive motor; sytlus heat; a Chart Recorder power switch; and an anti-bounce record circuit. See Fig. 3-7 on Chart Recorder Logic.

Pulse Shaper. The Pulse Shaper is made up of U5166A, U5166B, U5166C and U5166D. When the paper is moving, a square wave signal (CHART SPEED SENS) is generated by the holes in the paper passing between a light-emitting diode and a photo-sensitive transistor. The resultant pulses are shaped to a clean square wave by a Schmitt trigger circuit, U5166B and U5166C. The output signal is capacitor-coupled by C5167 to one-shot multivibrator U5166A and U5166D. This one-shot produces an output signal at TP5145 (violet test point) which is a positive going pulse approximately 10 ms wide. This (clock) pulse is connected to binary counter U5147; and to the end of the paper-sensitizer network, R5148.

Counter. The 7-stage binary counter is integrated circuit U5147. The binary outputs are connected to a resistor ladder network, which forms a digital-to-analog converter. Outputs Q1 and Q7 are connected to AND gate U5252B so that it recognizes the count number 65. Q2 clocks multivibrator U5127B at count 2. (The signal from U5127B starts the slow ramp.)

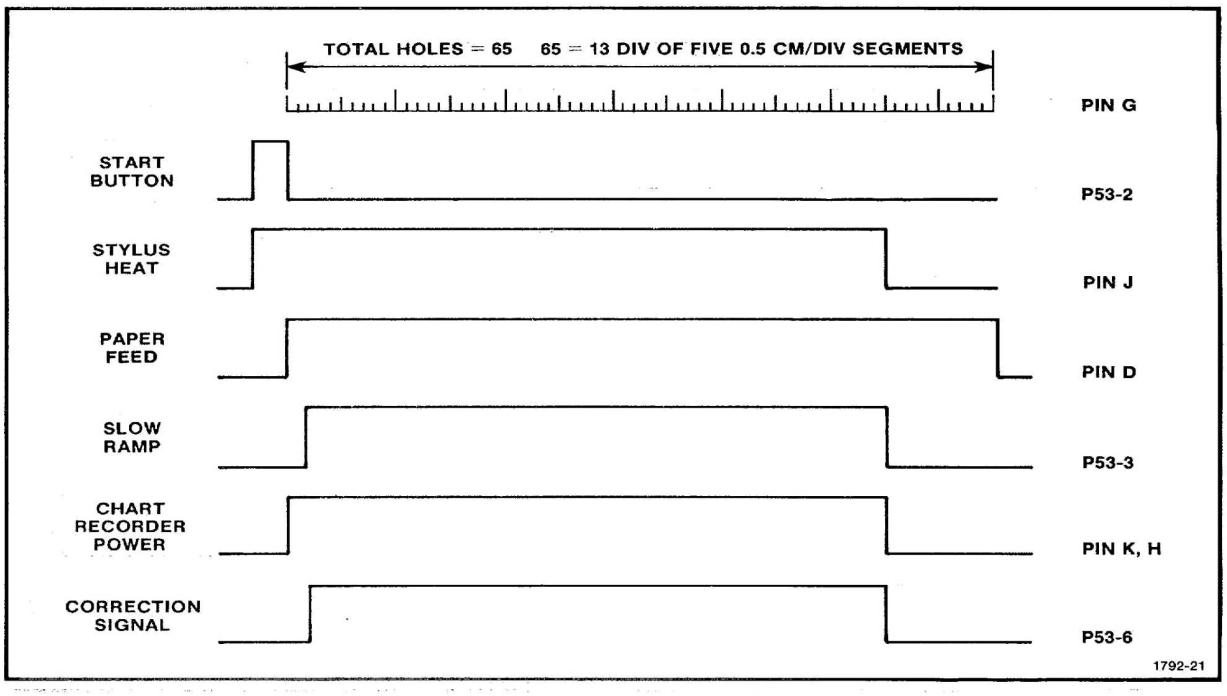


Figure 3-7. Chart Recorder Logic.

Horizontal Correction Network. The Horizontal Correction network compares the output of the digital-to-analog converter U5147 with the inverted slow ramp signal. U5227 inverts the slow ramp signal. The digital-to-analog output and inverted slow ramp signal are connected to inverting amplifier U5117, which performs summation and amplification simultaneously. This signal is fed to the Slow Ramp Generator by way of R5118 and will speed up or slow down the Slow Ramp Generator to synchronize it with the paper speed of the Strip Chart Recorder.

Chart Recorder Logic. The logic control signal that is received through pin 2 of P53 is shaped into a narrow impulse (negative going) by U5156B and U5156C. This impulse occurs at the trailing edge of the logic control signal and latches bi-stable multivibrator U5252A and U5252C. Pin 9 of U5252A goes positive and turns on Q5266, which pulls the motor control line to ground, causing the paper drive motor to start rotating. The paper drive motor turns off at count 65 by U5252B. A second signal is capable of turning the motor off. This occurs when the end of the paper is reached and the output from the pulse shaper is stopped. This causes C5249 to discharge and unlatch the multivibrator.

The multivibrator is initally latched when the inverted control signal from pin 4 of U5156B charges C5249. The impulse from pulse shaper U5166A and U5166D keeps C5249 charged. The multivibrator latch (output of pin 10) disables the reset of the counter and turns Q5144 on. This locks out the logic control input line.

Stylus heat control comes from Q5239, which is turned on by flip-flop U5127A. This flip-flop is energized by PEN LIFT signal from the Vertical board. The RETRACE signal turns the stylus heat off. This signal brings the flip-flop back to its original state (where pin 1 is low). The "Q" output also controls the chart pen motor power switch as well as providing the "J" input to flip-flop U5127B.

U5127 controls the start of the Slow Ramp Generator and controls the horizontal correction signal disable network (Q5112). The Slow Ramp Generator starts when Q2 of the Counter goes high. The output "Q" of U5127A resets U5127B to allow the Slow Ramp Generator to return to its original mode. The horizontal correction disable network Q5112 is controlled by the signal from pin 14 of U5127B, through Q5114.

Q5226 will conduct only when the Strip Chart Recorder is plugged in. Q5237 and Q5229 act as a dc level shift amplifier between flip-flop U5127B and the Slow Ramp Generator, which is on the Vertical board.

Chart Recorder Power Switch. The plus or minus 8 volts to drive the stylus movement is applied to the Strip Chart Recorder through two electronic switches, Q5273 and Q5277. Q5179 parallels Q5273 to provide more current in the +8 V line, These switches are driven by the same signal that is used to control stylus heat switch Q5239. This signal is passed through Q5173 and. Q5279 to the switches.

Anti-Bounce Record. This circuit, consisting of U5156A and Q5156D, removes switching transients from the RECORD switch. The output of this circuit goes to the Vertical board to control the X-Y Record Logic. The Record Logic in turn provides the logic control signal that is received through pin 2 of P53 on the Logic board. If the Logic board is removed from the TDR unit, the harmonica connector from the RECORD switch should be connected to P28 on the Vertical board.

X-Y Output Module (Schematic 7)

The X-Y Output Module provides an electrical interface between the 1502 and an external X-Y Chart Recorder. Three signals, PEN LIFT, X Output, and Y Output are provided for use by the external Chart Recorder. The switching mechanisms for the outputs are solid state devices, therefore care should be taken when connecting loads to them. See the specification listed in the Specification section of this manual.

Pen Lift. The Pen Lift signal level changes when the RECORD switch is activated. The normal level is either 0.0 V ±0.5 V or 5 V +0 or -1 V, depending on how the terminal link of the X-Y Output Module board is connected (positive or negative slope, see Fig. 3-8). When the RECORD switch is activated, the level will change from 0 V to 5 V or from 5 V to 0 V. The driving capability of this signal source is given in the Specification section of this manual.

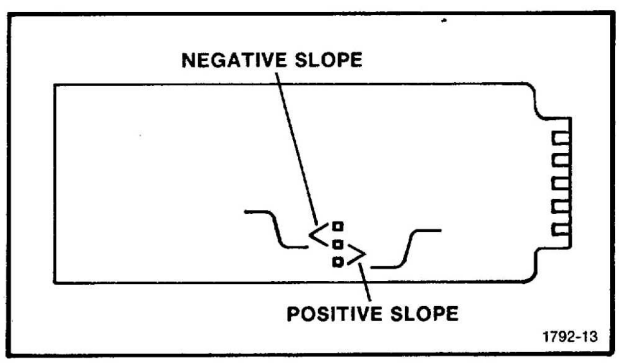


Figure 3-8. X-Y Output Module Strap.

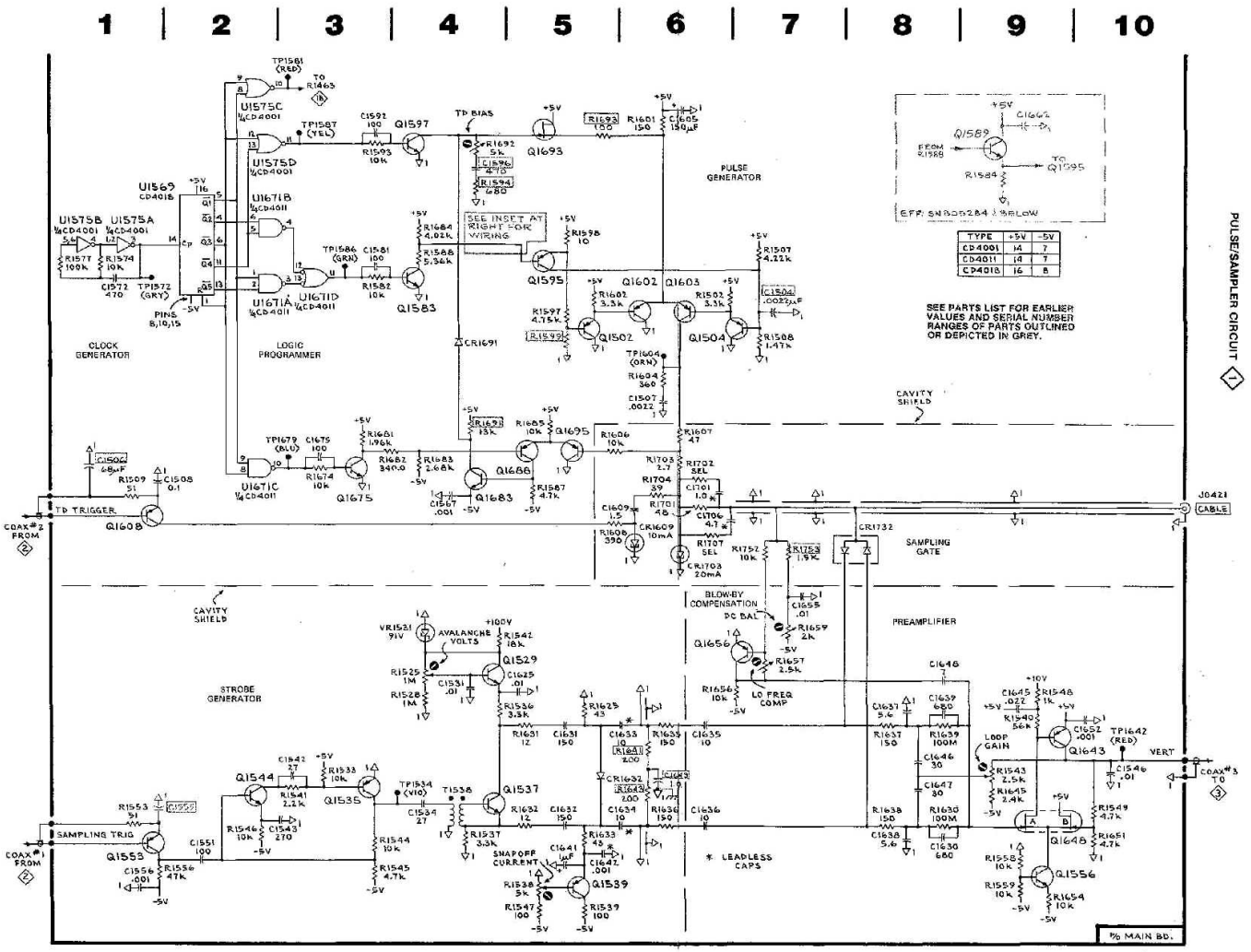
Diode CR7247 is used to clamp the negative voltage swing to -0.6 V. Q7242 provides the capabilities for the operation of units with a positive pen lift or a ground return path.

X Output. The X output is directly proportional to the horizontal position of the crt beam along the crt face. This signal is a ramp of approximately 20 seconds duration and raises at a rate of 0.1 V for each division of horizontal travel across the crt. This 0.1 V per division scale factor is set by a voltage divider network comprised of R7138, R7129 and R7122. C7132 is used to reduce noise. Source impedance is less than 13 K (9.4 K minimum).

Y Output. The Y output is directly proportional to the vertical deflection on the crt. The scale factor (volts output per division of crt deflection) is adjustable, from 0.09 V per division to 0.13 V per division (factory set for 0.1 V/div), by variable resistor R7225. The source impedance of this signal is less than 11 kΩ (8 kΩ minimum) and is determined by R7234, R7224 and R7225. C7232 is used to reduce noise.

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C1155	F12	Q1504	C6		
C1161	F12	Q1529	F4	R1542	F4
C1237	E15	Q1535	G3	R1543	G9
C1313	C13	Q1537	G4	R1544	H3
C1325	E14	Q1539	H5	R1545	H3
C1332	F15	Q1544	G2	R1546	G2
C1341	E17	Q1553	H1	R1547	H5
C1345	H17	Q1556	H9	R1548	F9
C1435	F13	Q1583	C4	R1549	G10
C1464	D12	Q1589	A9	R1553	G1
C1504	C7	Q1595	B5	R1556	H1
C1506	D1	Q1597	A4	R1558	H9
C1507	D6	Q1602	C6	R1559	H9
C1508	D2	Q1603	C6	R1574	B1
C1531	F4	Q1608	E1	R1577	B1
C1534	G4	Q1643	G9	R1582	C3
C1542	G3	Q1648	G9	R1584	B9
C1543	G3	Q1656	F7	R1587	D5
C1546	G10	Q1675	D3	R1588	B4
C1551	H2	Q1683	D4	R1593	A3
C1555	G2	Q1688	D5	R1594	B4
C1556	H1	Q1693	A5	R1597	C5
C1568	F11	Q1695	D5	R1598	B5
C1567	E4			R1599	C5
C1572	C1	R0151	H18	R1601	A6
C1581	B3	R0271	C15	R1602	C5
C1592	A3	R0472	F20	R1604	C6
C1596	B4	R1129	H15	R1606	D5
C1605	A6	R1132	H15	R1607	D6
C1609	E6	R1135	H15	R1608	E5
C1625	F5	R1138	H17	R1625	F5
C1630	H8	R1144	F19	R1630	G8
C1631	G5	R1145	F19	R1631	G5
C1632	G5	R1148	F19	R1632	G5
C1633	G6	R1152	E18	R1633	H5
C1634	G6	R1216	B16	R1635	G6
C1635	G6	R1217	B16	R1636	G6
C1636	G6	R1218	B17	R1637	G8
C1637	F8	R1219	B17	R1638	G8
C1638	H8	R1226	B18	R1639	G8
C1639	F8	R1227	B18	R1641	G6
C1641	H5	R1235	H17	R1643	G6
C1642	H5	R1239	E17	R1645	G9
C1643	G6	R1312	C14	R1651	H10
C1645	F9	R1315	C13	R1654	H9
C1646	G8	R1318	D14	R1656	F7
C1647	G8	R1319	C13	R1657	F7
C1648	F8	R1323	B19	R1659	F7
C1652	G10	R1324	B20	R1674	D3
C1655	E7	R1326	C13	R1681	D3
C1661	F11	R1333	E16	R1682	D3
C1662	B9	R1335	F15	R1683	D4
C1675	D3	R1338	F13	R1684	B4
C1701	D6	R1341	F16	R1685	D5
C1706	E6	R1342	E17	R1691	D4
		R1352	F12	R1692	A4
CR1359	D13	R1353	E12	R1693	A5
CR1609	E6	R1354	E12	R1701	E6
CR1632	G5	R1355	D13	R1702	D6
CR1691	C4	R1358	D13	R1703	D6
CR1703	E6	R1422	F16	R1704	D6
CR1732	E8	R1431	E18	R1707	E6
		R1432	F14	R1752	E7
Q1317	C13	R1434	F13	R1753	E7
Q1325	E17	R1435	F13		
Q1328	D17	R1437	F16	S0151	D14
Q1329	D16	R1441	F13	S1222	A17
Q1336	E16	R1442	H16	S1251	F18
Q1337	F14	R1443	H16		
Q1338	F13	R1445	G16	T1538	G4
Q1339	F13	R1462	D12		
Q1347	G16	R1463	D12	U1344	E19
Q1348	G16	R1502	C6	U1569	B2
Q1355	D13	R1507	B7	U1575	B1,B2
Q1357	E12	R1508	C7	U1671	B2,D2
Q1358	E12	R1509	D1		
Q1413	C14	R1525	F4	VR1531	F4
Q1425	E16	R1528	F4		
Q1431	E16	R1533	G3		
Q1443	G16	R1536	F4		
Q1444	G17	R1537	H4		
Q1447	G16	R1538	H5		
Q1448	G16	R1539	H5		
Q1502	C5	R1540	G9		
		R1541	G3		

NOTE: THIS GRID LOCATOR APPLIES TO BOTH DIAGRAMS ① AND ②



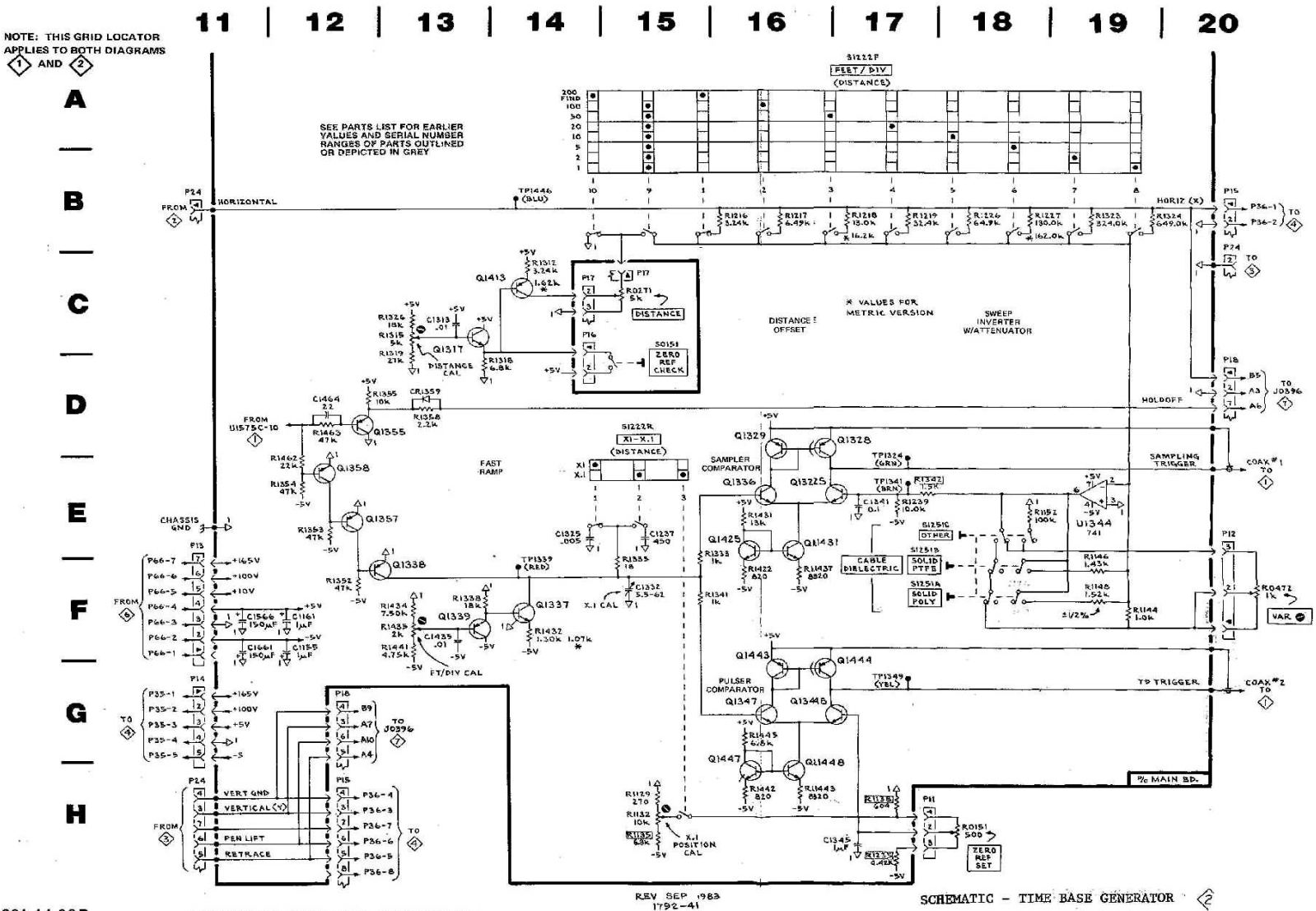
SCHEMATIC-PULSER/SAMPLER

1502

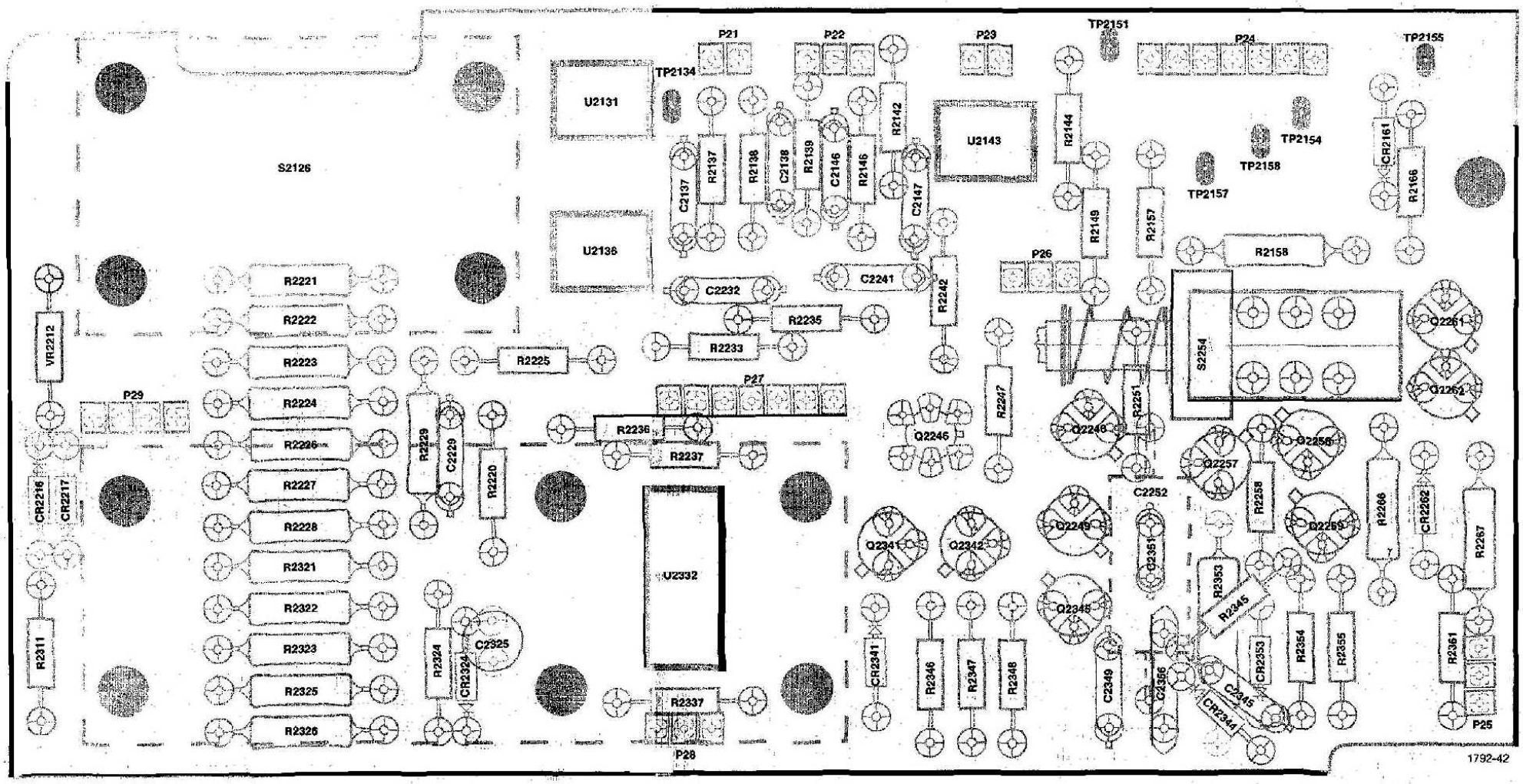
REV SEP 1983
1792-40

SCHEMATIC – PULSER/SAMPLER ①

CKT NO	GRID LOC	CKT NO	GRID LOC	CKT NO	GRID LOC
C1155	F12	Q1504	C6	R1542	F4
C1161	F12	Q1529	F4	R1543	G9
C1237	E15	Q1535	G3	R1544	H3
C1313	C13	Q1537	G4	R1545	H3
C1325	E14	Q1539	H5	R1546	G2
C1332	F15	Q1544	G2	R1547	H5
C1341	E17	Q1553	H1	R1548	F9
C1345	H17	Q1556	H9	R1549	G10
C1435	F13	Q1583	C4	R1553	G1
C1464	D12	Q1589	A9	R1556	H1
C1504	C7	Q1595	B5	R1558	H9
C1506	D1	Q1597	A4	R1559	H9
C1507	D6	Q1602	C6	R1574	B1
C1508	D2	Q1603	C6	R1577	B1
C1531	F4	Q1608	E1	R1582	C3
C1534	G4	Q1643	G9	R1584	B9
C1542	G3	Q1648	G9	R1587	D5
C1543	G3	Q1656	F7	R1588	B4
C1546	G10	Q1675	D3	R1593	A3
C1551	H2	Q1683	D4	R1594	B4
C1555	G2	Q1688	D5	R1597	C5
C1556	H1	Q1693	A5	R1598	B5
C1566	F11	Q1695	D5	R1599	C5
C1567	E4			R1601	A6
C1572	C1	R0151	H18	R1602	C5
C1581	B3	R0271	C15	R1604	C6
C1592	A3	R0472	F20	R1606	D5
C1596	B4	R1129	H15	R1607	D6
C1605	A6	R1132	H15	R1608	E5
C1609	E6	R1135	H15	R1625	F5
C1625	F5	R1138	H17	R1630	G8
C1630	H8	R1144	F19	R1631	G5
C1631	G5	R1146	F19	R1632	G5
C1632	G5	R1148	F19	R1633	H5
C1633	G6	R1152	E18	R1635	G6
C1634	G6	R1216	B16	R1636	G6
C1635	G6	R1217	B16	R1637	G8
C1636	G6	R1218	B17	R1638	G8
C1637	F8	R1219	B17	R1639	G8
C1638	H8	R1226	B18	R1641	G6
C1639	F8	R1227	B18	R1643	G6
C1641	H5	R1235	H17	R1645	G9
C1642	H5	R1239	E17	R1651	H10
C1643	G8	R1312	C14	R1654	H9
C1645	F9	R1315	C13	R1656	F7
C1646	G8	R1318	D14	R1657	F7
C1647	G8	R1319	C13	R1659	F7
C1648	F8	R1323	B19	R1674	D3
C1652	G10	R1324	B20	R1681	D3
C1655	E7	R1326	C13	R1682	D3
C1661	F11	R1333	E16	R1683	D4
C1662	B9	R1335	F15	R1684	B4
C1675	D3	R1338	F13	R1685	D5
C1741	D8	R1341	F16	R1691	D4
C1706	E6	R1342	E17	R1692	A4
		R1352	F12	R1693	A5
CR1359	D13	R1353	E12	R1701	E6
CR1609	E6	R1354	E12	R1702	D6
CR1632	G5	R1355	D13	R1703	D6
CR1691	C4	R1358	D13	R1704	D6
CR1703	E6	R1422	F18	R1707	E6
CR1732	E8	R1431	E16	R1752	E7
		R1432	F14	R1753	E7
Q1317	C13	R1434	F13		
Q1325	E17	R1435	F13	S0151	D14
Q1328	D17	R1437	F16	S1222	A17
Q1329	D16	R1441	F13	S1251	F18
Q1336	E16	R1442	H16		
Q1337	F14	R1443	H16	T1538	G4
Q1338	F13	R1445	G16		
Q1339	F13	R1462	D12	U1344	E19
Q1347	G16	R1463	D12	U1569	B2
Q1348	G16	R1502	C6	U1575	B1,B2
Q1355	D13	R1507	B7	U1671	B2,D2
Q1357	E12	R1508	C7		
Q1358	E12	R1509	D1	VR1531	F4
Q1413	C14	R1525	F4		
Q1425	E16	R1528	F4		
Q1431	E16	R1533	G3		
Q1443	G16	R1536	F4		
Q1444	G17	R1537	H4		
Q1447	G16	R1538	H5		
Q1448	G16	R1539	H5		
Q1502	C5	R1540	G9		
		R1541	G3		

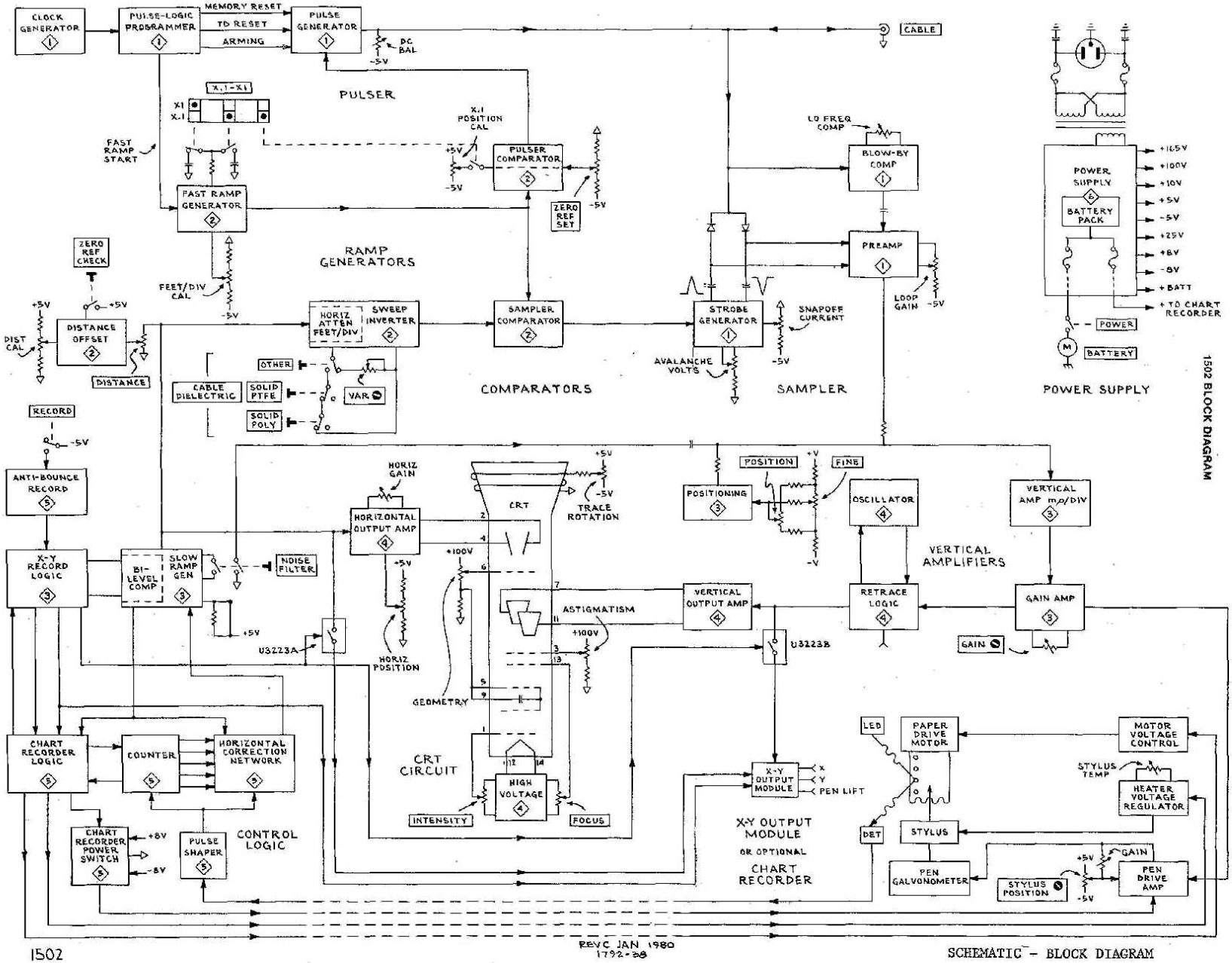


SCHEMATIC-TIME BASE GENERATOR

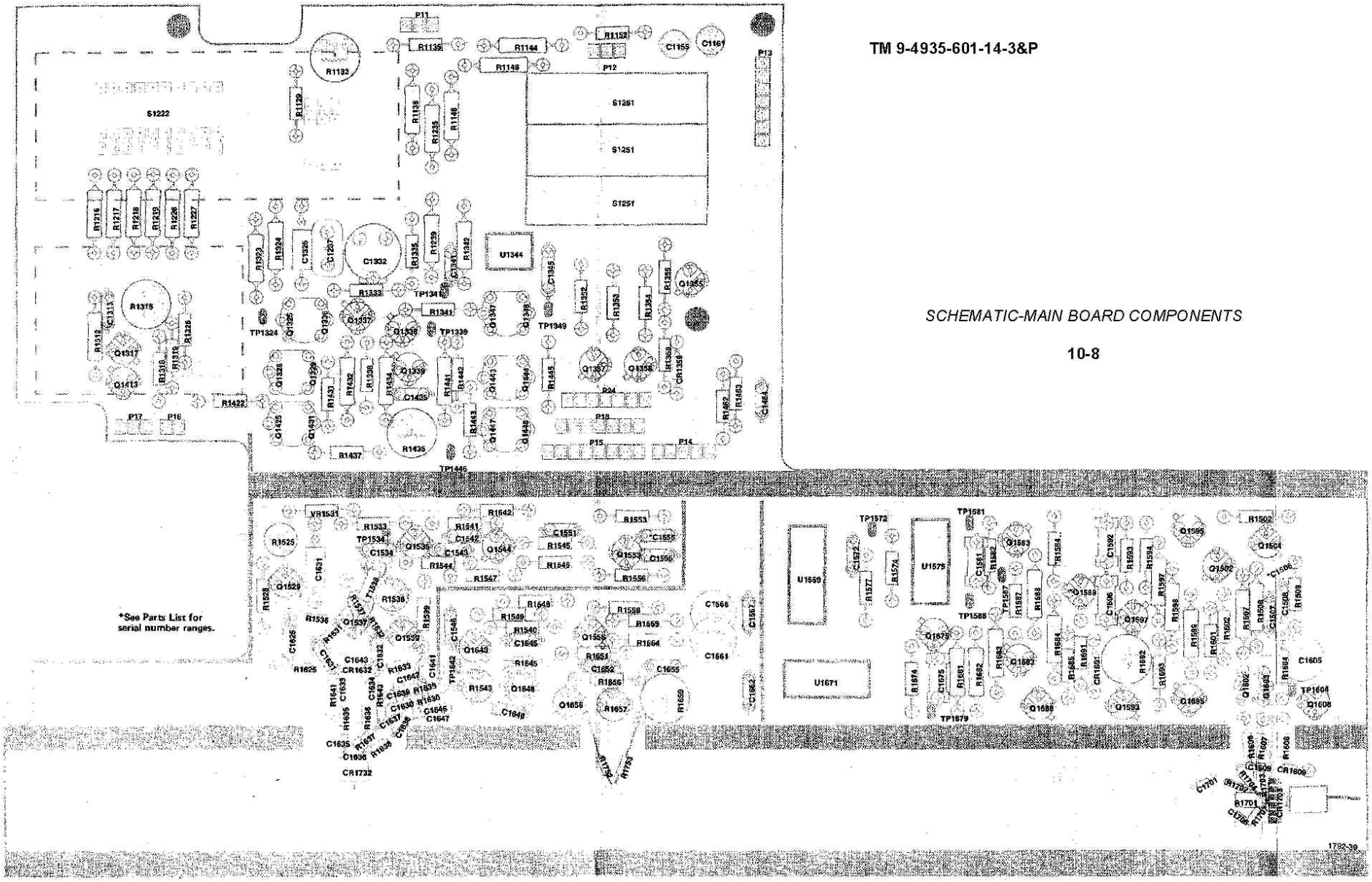


Vertical Amplifier/Slow Ramp Board

SCHEMATIC-VERT AMPL/SLOW RAMP COMPONENT



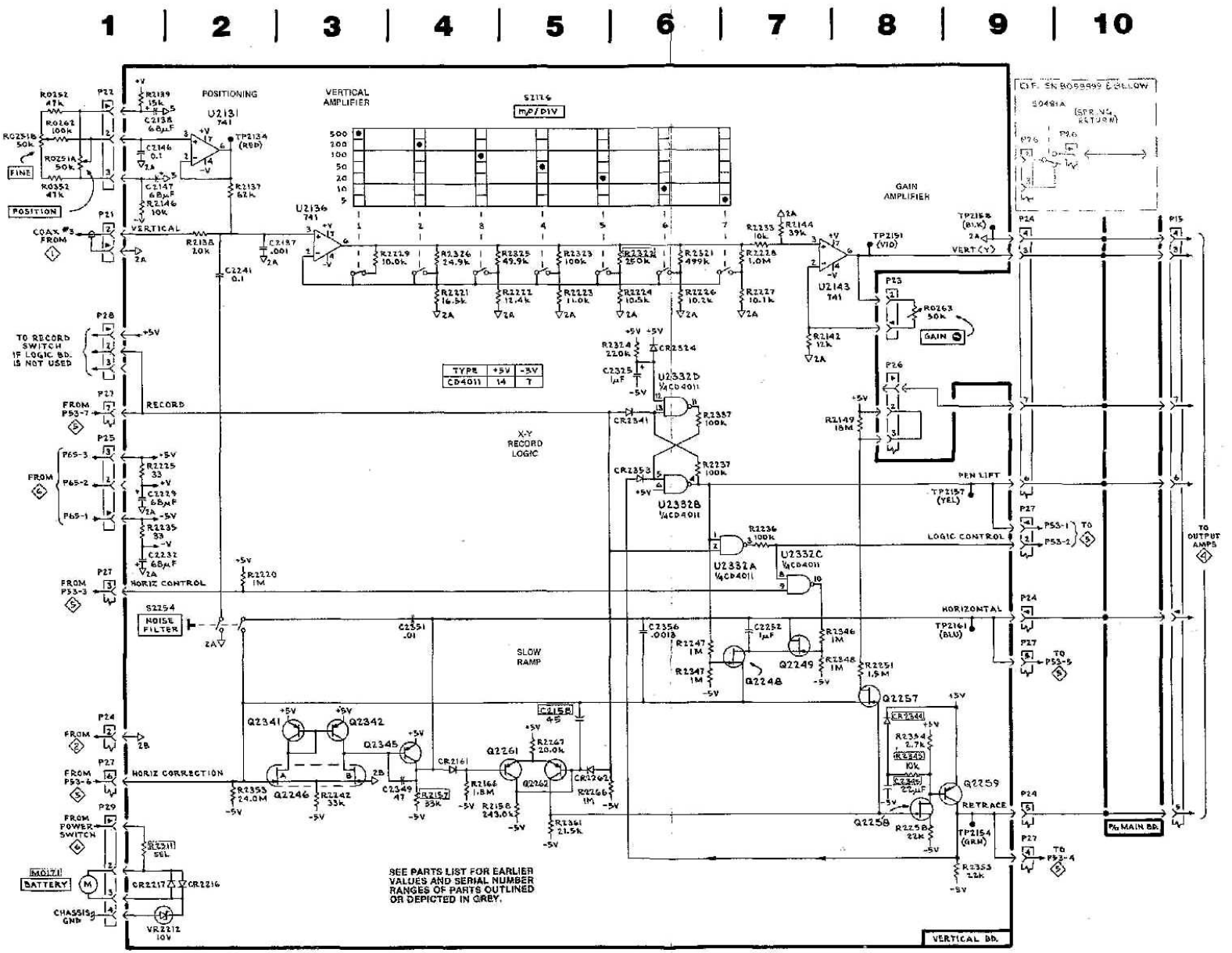
SCHEMATIC-BLOCK DIAGRAM



SCHEMATIC-MAIN BOARD COMPONENTS

10-8

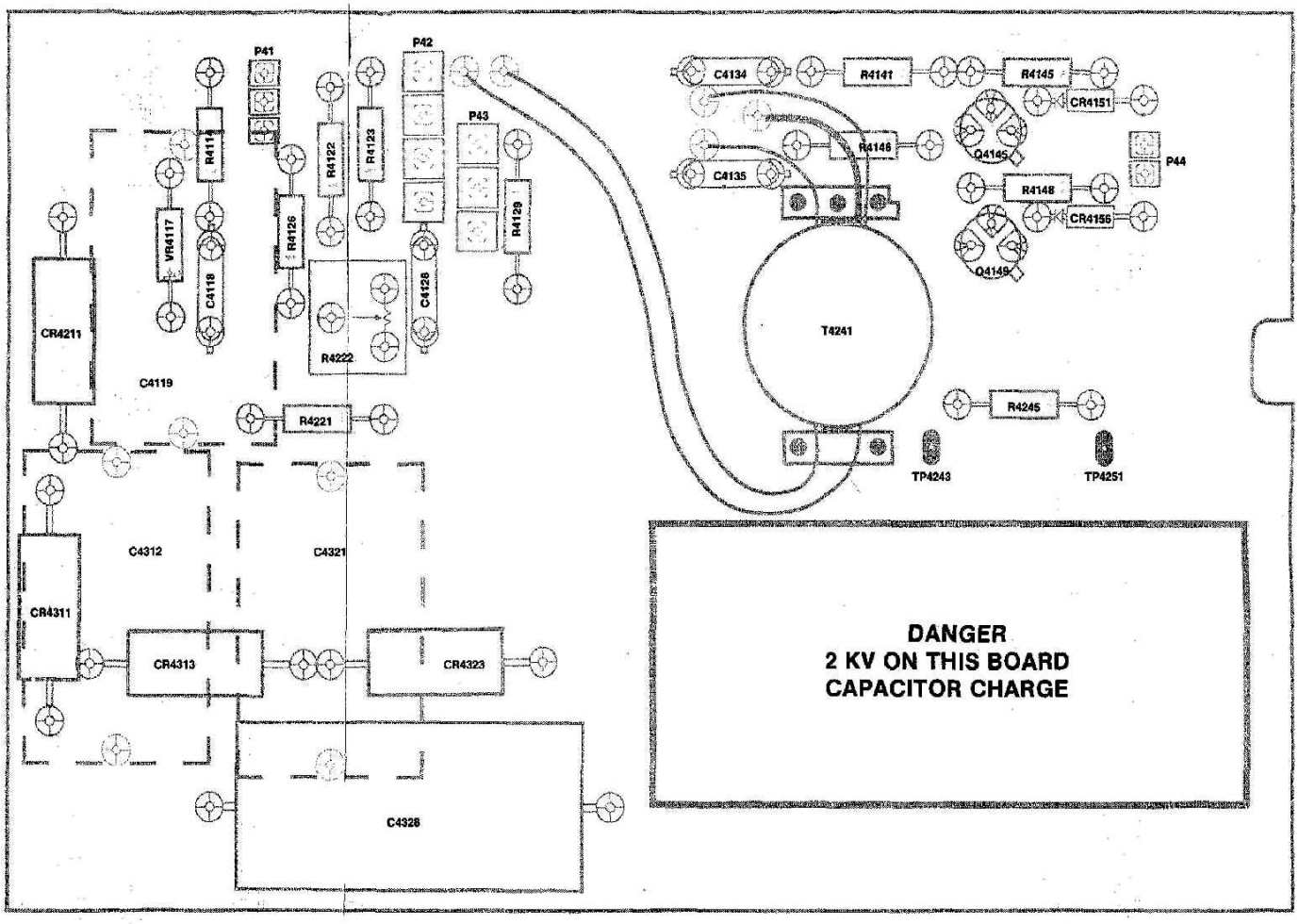
CKT NO	GRID LOC
C2137	B3
C2138	A2
C2146	A2
C2147	B2
C2158	G5
C2229	E2
C2232	E2
C2241	C2
C2252	F7
C2325	C6
C2345	G8
C2349	G4
C2351	F4
C2352	F7
C2356	F6
CR2161	G4
CR2216	H2
CR2217	H2
CR2262	G6
CR2324	C6
CR2341	D6
CR2344	F8
CR2345	G8
CR2353	D6
M0171	H1
Q2246A	G6
Q2246B	G6
Q2248	F7
Q2249	F7
Q2257	F8
Q2258	G8
Q2259	G9
Q2261	G5
Q2262	G5
Q2341	G3
Q2342	G3
Q2345	G4
R0251A	A1
R0251B	A1
R0252	A1
R0262	A1
R0263	C9
R0352	B1
R2137	B2
R2138	B2
R2139	A2
R2142	C8
R2144	B7
R2146	B2
R2149	D8
R2157	G4
R2158	G5
R2166	G4
R2220	E3
R2221	C4
R2222	C3
R2223	C5
R2224	C6
R2225	D2
R2226	C7
R2227	C7
R2228	B7
R2229	B4
R2233	B7
R2235	E2
R2236	E7
R2237	D7
R2242	G3
R2247	F7
R2251	F8
R2258	H9
R2266	G5
R2267	G5
R2311	H2
R2321	B6
R2322	B6
R2323	B5
R2324	C6
R2325	B5
R2326	B4
R2337	D7
R2345	G8
R2346	F8
R2347	F7
R2348	F8
R2353	G2
R2354	G9
R2355	H9
R2361	G5
S0481A	D8
S2125	A5
S2254	F2
U2131	A2
U2136	B3
U2143	B8
U2332	D6,E7
VR2212	H2



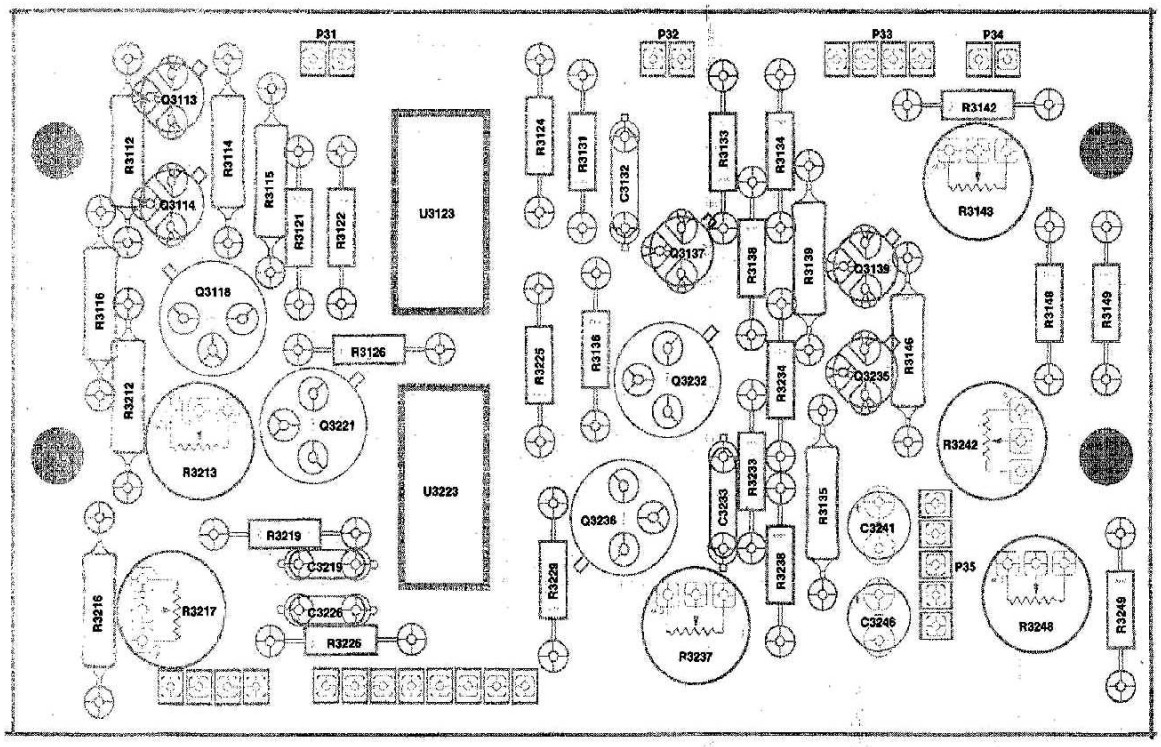
SCHEMATIC-VERTICAL AMP/SLOW RAMP

10-9

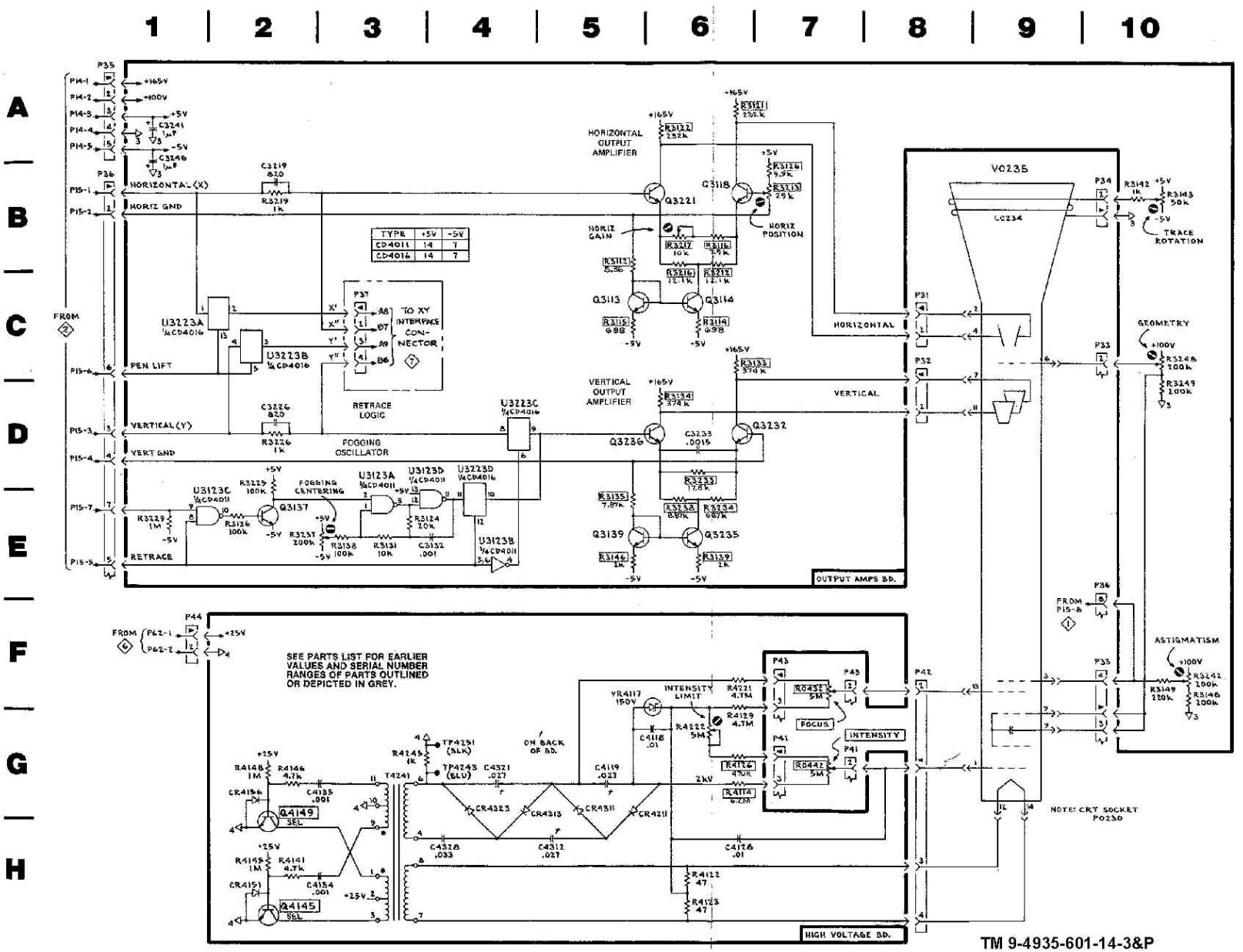
TM 9-4935-601-14-3&P



SCHEMATIC-OUTPUT AMPL & HIGH VOLTAGE COMPONENTS

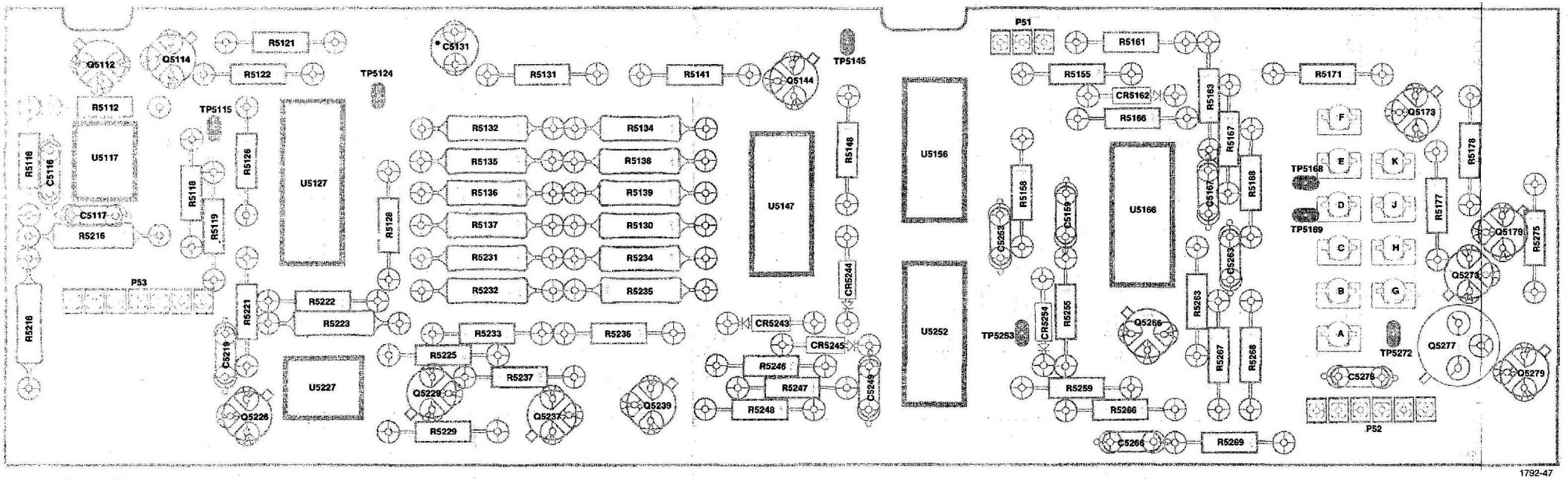


CKT NO	GRID LOC	CKT NO	GRID LOC
C3132	E2	R4114	G6
C3219	B2	R4122	H6
C3226	D2	R4123	H6
C3233	D6	R4126	G6
C3241	A1	R4129	G6
C3246	A1	R4141	H2
		R4145	H2
C4118	G5	R4146	G2
C4119	G5	R4148	G2
C4128	H6	R4221	F6
C4134	H2	R4222	G6
C4135	G2	R4245	G3
C4312	H4		
C4321	G4		
C4328	H3	T4241	G3
CR4151	H2	U3123	E1,E3
CR4156	G2	U3223	C1,D4
CR4211	G5		
CR4311	G5		
CR4313	G4	V0235	B9
CR4323	G4		
		VR4117	F5
L0234	B9		
P0230	G9		
Q3113	C5		
Q3114	C6		
Q3118	B6		
Q3137	E2		
Q3139	E5		
Q3221	B6		
Q3232	D6		
Q3235	E6		
Q3236	D6		
Q4145	H2		
Q4149	G2		
R0432	F7		
R0442	G7		
R3112	B5		
R3114	C6		
R3115	C5		
R3116	B6		
R3121	A6		
R3122	A6		
R3124	E3		
R3126	B7		
R3131	E3		
R3133	C6		
R3134	D6		
R3135	E5		
R3136	E2		
R3138	E3		
R3139	E6		
R3142	B10		
R3143	B10		
R3146	E5		
R3148	F10		
R3149	F10		
R3212	B6		
R3213	B7		
R3216	B6		
R3217	B6		
R3219	B2		
R3225	D2		
R3226	D2		
R3229	E1		
R3233	D6		
R3234	E6		
R3237	E2		
R3238	E6		
R3242	F10		
R3248	C10		
R3249	C10		



TM 9-4935-601-14-3&P

SCHEMATIC-OUTPUT AMPLIFIERS & HIGH VOLTAGE



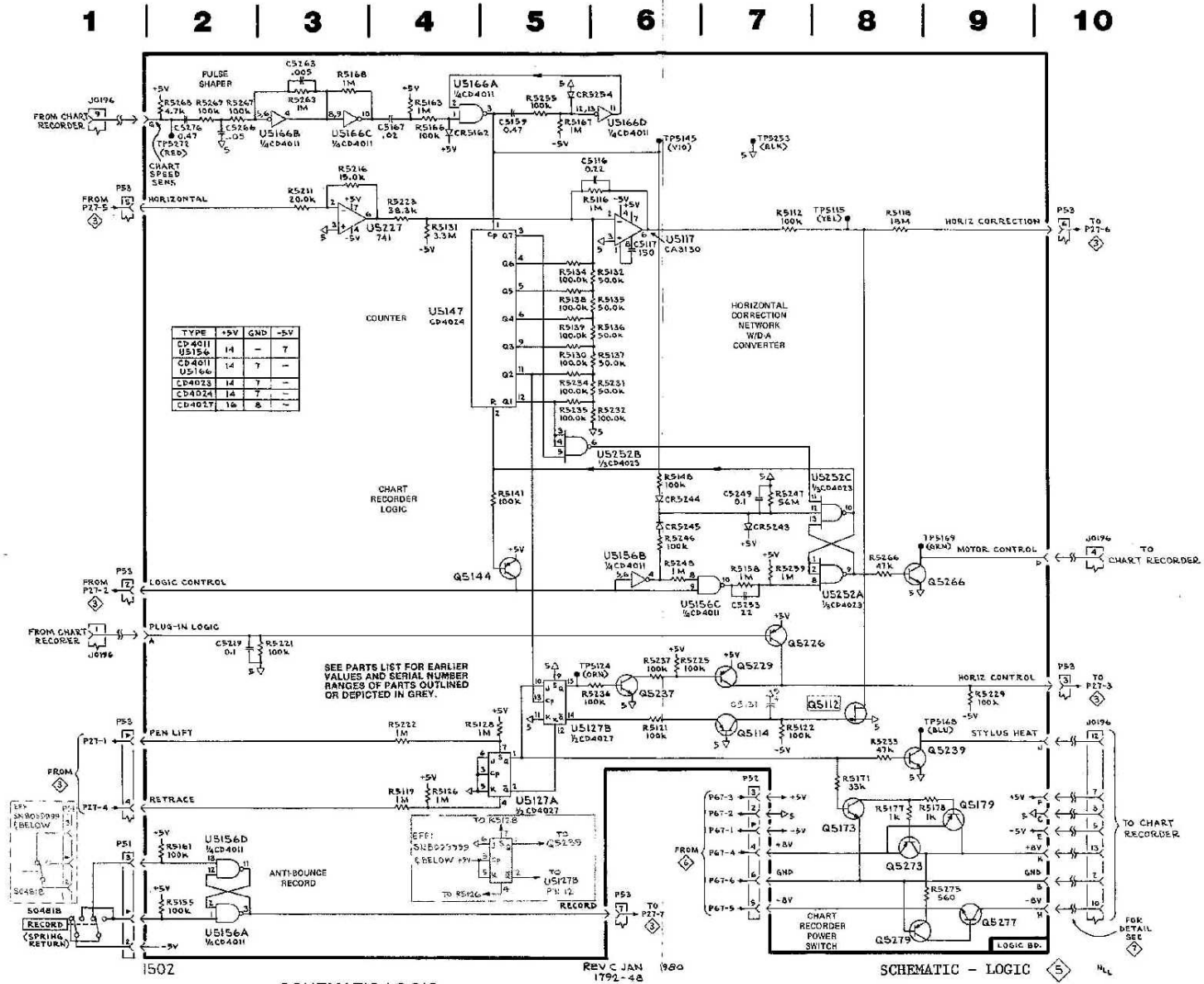
1792-47

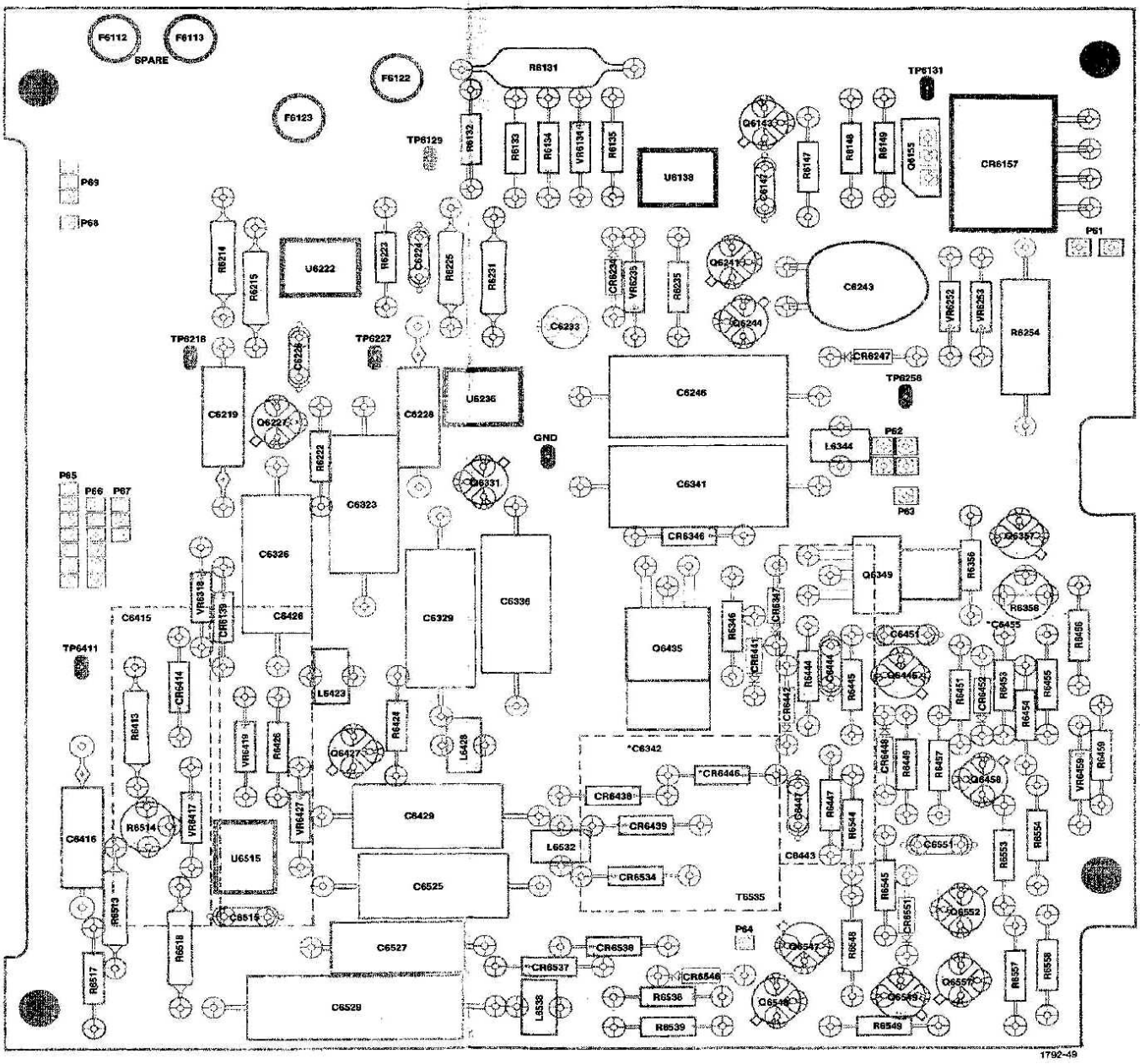
*See Parts List for serial number ranges.

Logic Board

SCHEMTAIC-LOGIC BOARD COMPONENTS

CKT NO	GRID LOC	CKT NO	GRID LOC
C5116	B5	R5246	E6
C5117	B6	R5247	E7
C5131	G7	R5248	E6
C5159	A5	R5255	A5
C5167	A4	R5259	E7
C5219	F2	R5263	A3
C5249	D7	R5266	E8
C5253	F7	R5267	A2
C5263	A3	R5268	A2
C5266	A2	R5269	A2
C5276	A2	R5275	H9
CR5162	A4	S0481B	H1
CR5243	E7		
CR5244	E6		
CR5245	E6	U5117	B6
CR5254	A6	U5127	G5
		U5147	C4
		U5156	E6
Q5112	F8	U5166	A3,A5,A6
Q5114	G7	U5227	B4
Q5144	E4	U5252	D5,D8,E8
Q5173	G7		
Q5179	G9		
Q5226	F7		
Q5229	F7		
Q5237	F6		
Q5239	G9		
Q5266	E9		
Q5273	H8		
Q5277	H9		
Q5279	H8		
R5112	B7		
R5116	B5		
R5118	B8		
R5119	G4		
R5121	G6		
R5122	G7		
R5126	G4		
R5128	G5		
R5130	C5		
R5131	B4		
R5132	C6		
R5134	C5		
R5135	C6		
R5136	C6		
R5137	C6		
R5138	C5		
R5139	C5		
R5141	D5		
R5148	D6		
R5155	H2		
R5158	E7		
R5161	H2		
R5163	A4		
R5166	A4		
R5167	A5		
R5168	A3		
R5171	G8		
R5177	G8		
R5178	G9		
R5211	B3		
R5216	B2		
R5221	F3		
R5222	G4		
R5223	B4		
R5225	F6		
R5229	F9		
R5231	D6		
R5232	D6		
R5233	G8		
R5234	D5		
R5235	D6		
R5236	F5		
R5237	F6		



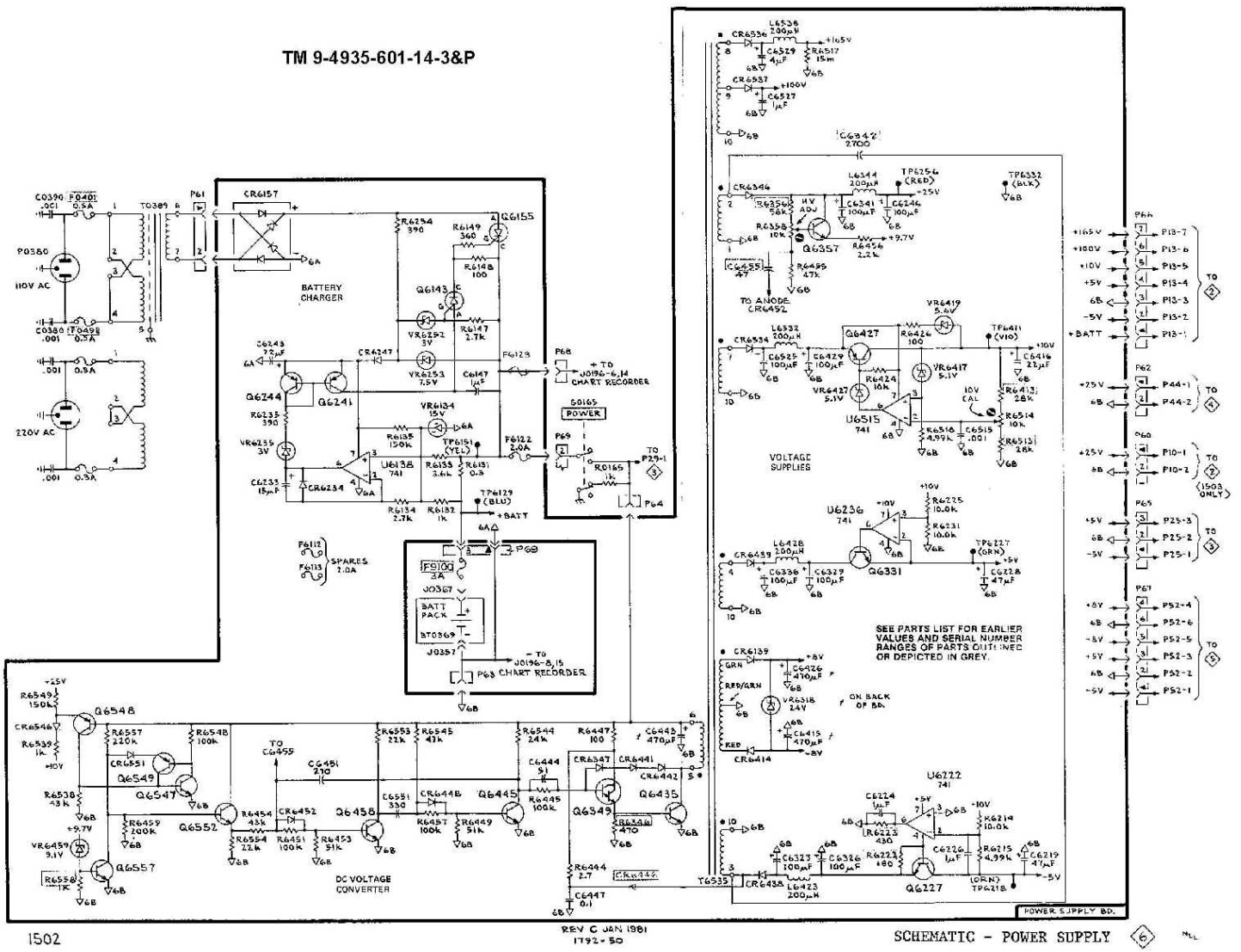


*See Parts List for serial number ranges.

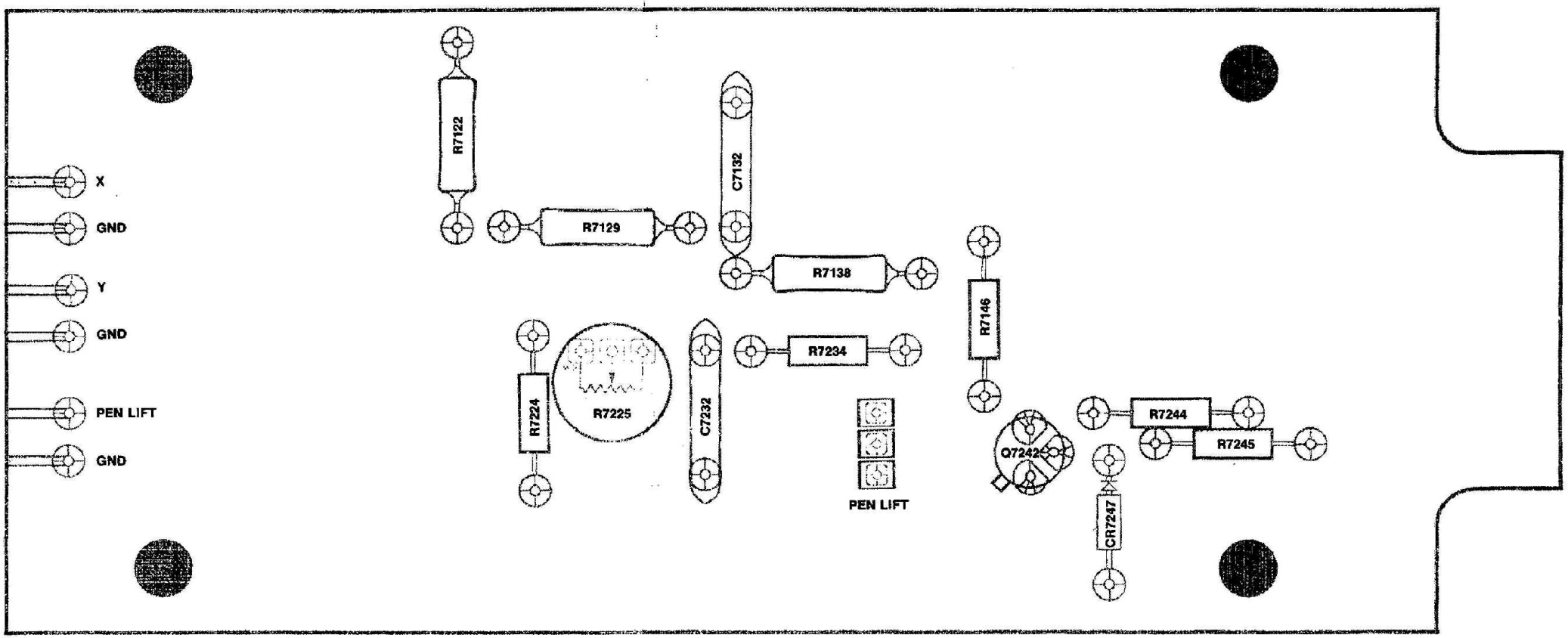
Power Supply

SCHEMATIC-POWER SUPPLY

CKT NO	GRID LOC	CKT NO	GRID LOC
BT0369	F4	Q6458	H3
C0380	D1	Q6547	H2
C0390	C1	Q6548	G1
C6147	D5	Q6549	G2
C6219	H10	Q6552	H2
C6224	H8	Q6557	H1
C6226	H9		
C6228	F9	R6131	E5
C6233	E3	R6132	E4
C6243	D3	R6133	E4
C6246	B8	R6134	E4
C6323	H7	R6135	D4
C6326	H8	R6147	C5
C6329	F8	R6148	C5
C6336	F7	R6149	C5
C6341	B8	R6214	H9
C6342	B8	R6215	H9
C6415	G8	R6222	H8
C6416	D10	R6223	H8
C6426	G8	R6225	E9
C6429	D8	R6231	E9
C6443	G7	R6235	D3
C6444	G5	R6254	C4
C6447	H6	R6346	H6
C6451	G3	R6356	B8
C6455	C7	R6358	C7
C6515	D9	R6413	D9
C6525	D7	R6424	D8
C6527	A7	R6426	D8
C6529	A7	R6444	H6
C6551	H4	R6445	H5
		R6447	G6
		R6449	H5
CR6139	F7	R6451	H3
CR6157	B3	R6453	H3
CR6234	E3	R6454	H3
CR6247	D4	R6455	C8
CR6346	B7	R6456	C8
CR6347	G6	R6457	H4
CR6414	G7	R6459	H2
CR6438	H7	R6513	E9
CR6439	F7	R6514	D9
CR6441	G6	R6517	A8
CR6442	G6	R6518	D9
CR6446	H6	R6538	H1
CR6448	H4	R6539	G1
CR6452	H3	R6544	G5
CR6534	D7	R6545	G4
CR6536	A7	R6548	G2
CR6537	A7	R6549	G1
CR6546	G1	R6553	G4
CR6551	G2	R6554	H3
		R6557	G2
		R6558	H1
F0401	B1		
F0401	B1		
F0491	C1	S0165	E6
F0491	C1		
F6112	F3		
F6113	F3	T6535	H8
F6122	E5		
		U6138	E4
		U6222	H9
L6344	B8	U6236	E8
L6423	H7	U6515	D8
L6428	F7		
L6532	D7		
L6538	A7		
		VR6134	D4
		VR6235	E3
Q6143	C4	VR6252	D4
Q6155	C5	VR6253	D4
Q6227	H9	VR6318	G7
Q6241	D3	VR6417	D9
Q6244	D3	VR6419	C9
Q6331	F8	VR6427	D8
Q6349	H6	VR6459	H1
Q6357	C8		
Q6427	D8		
Q6435	H6		
Q6445	H5		



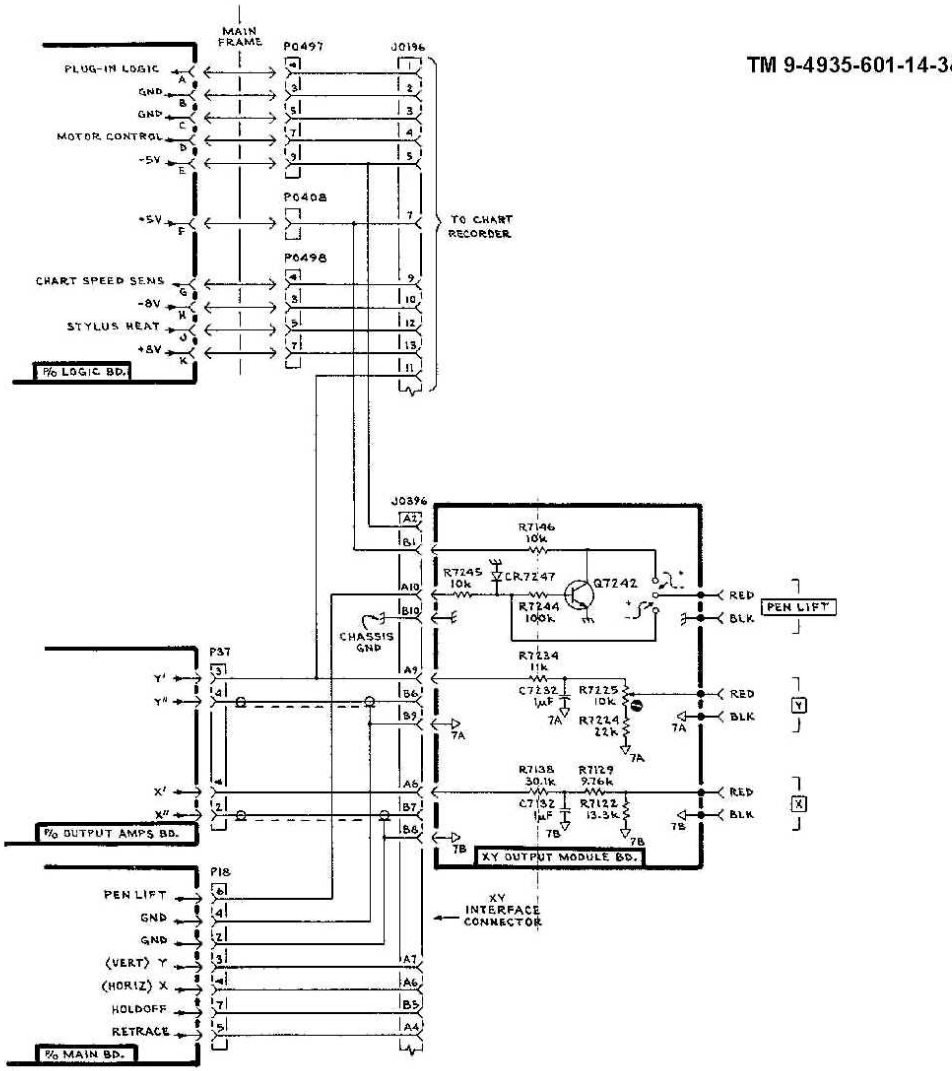
SCHEMATIC-POWER SUPPLY



X-Y Output Module

SCHEMATIC-POWER SUPPLY COMPONENTS

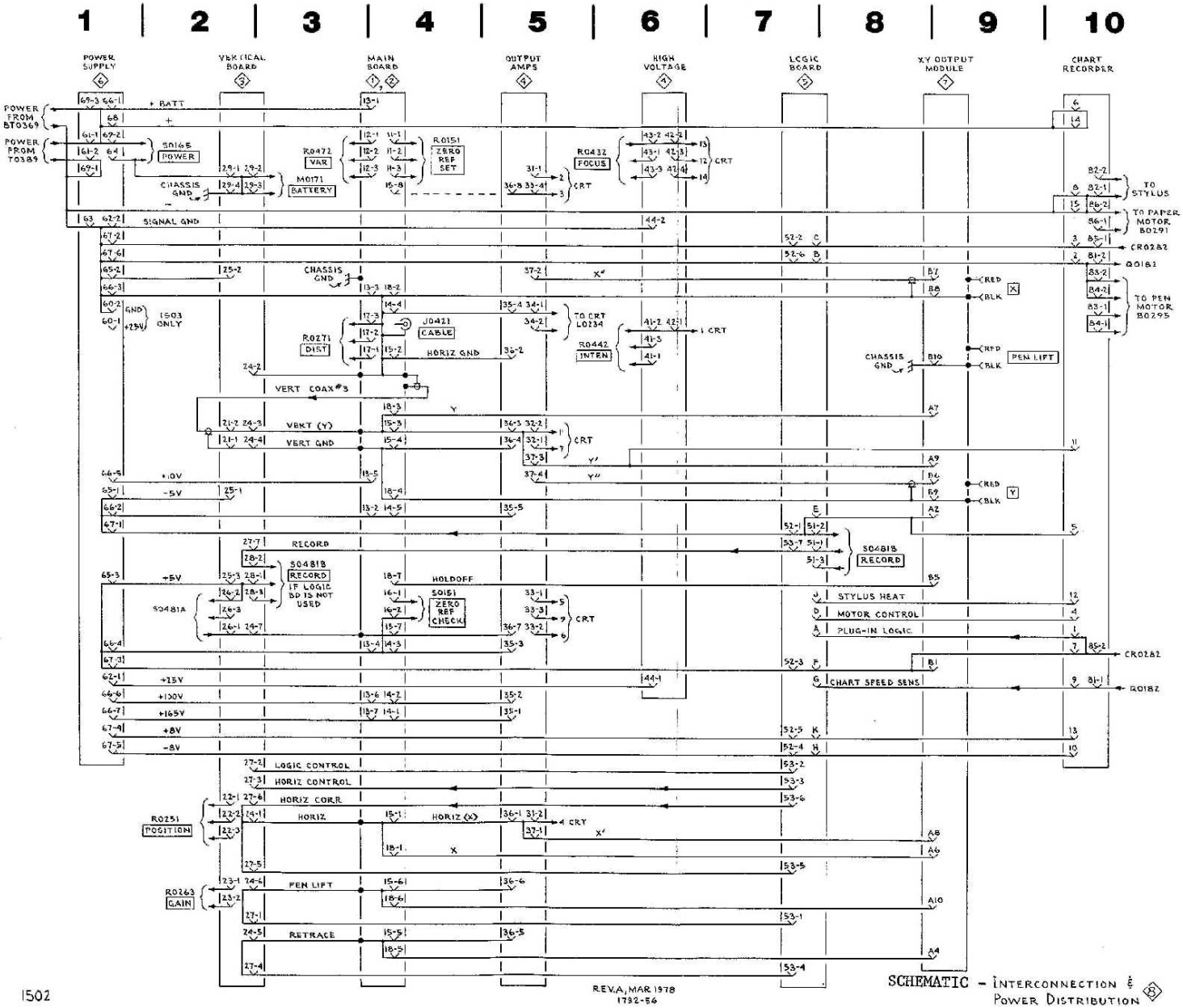
CKT NO	GRID LOC
C7132	F6
C7232	E6
CR7247	D6
Q7242	E7
R7122	F7
R7129	F7
R7138	F6
R7146	D6
R7224	E7
R7225	E7
R7234	E6
R7244	E6
R7245	E6



SCHEMATIC – X-Y OUTPUT MODULE & CHART RECORDER INTERCONNECT ◇7 NL1

REV. B, MAR 1978
1792-52

1502


1 2 3 4 5 6 7 8 9 10
A B C D E F G H
POWER SUPPLY
VERTICAL BOARD
MAIN BOARD
OUTPUT AMPS
HIGH VOLTAGE
LOGIC BOARD
X,Y OUTPUT MODULE
CHART RECORDER
POWER FROM BT0369
POWER FROM T0389
+ BATT
SIGNAL GND
CHASSIS GND
VERT COAX #3
VERT (Y)
VERT GND
HORIZ GND
HORIZ
HORIZ (X)
PEN LIFT
RETRACE
RECORD
HOLDOFF
LOGIC CONTROL
HORIZ CONTROL
HORIZ CORR
+10V
-5V
+5V
+15V
+100V
+165V
+8V
-8V
S0165 POWER
M0171 BATTERY
R0472 VAR
R0151 ZERO REF SET
R0432 FOCUS
J0421 CABLE
R0271 DIST
R0442 INTEN
S0481B RECORD
IF LOGIC BD IS NOT USED
S0481A
S0151 ZERO REF CHECK
R0251 POSITION
R0263 GAIN
1503 ONLY
TO CRT LO234
TO STYLUS
TO PAPER MOTOR B0291
TO PEN MOTOR B0295
CR0282
Q0182
R0182
STYLUS HEAT
MOTOR CONTROL
PLUG-IN LOGIC
CHART SPEED SENS
PEN LIFT
RED
BLK
REV.A, MAR 1978
1732-54
SCHEMATIC - INTERCONNECTION & POWER DISTRIBUTION

1502