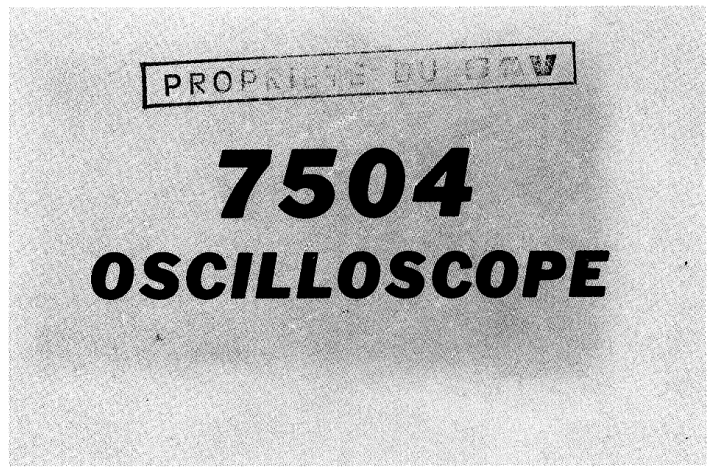
INSTRUCTION MANUAL

Serial Number _____



Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon 97005 ● Phone 644-0161 ● Cables: Tektronix
070-0932-00
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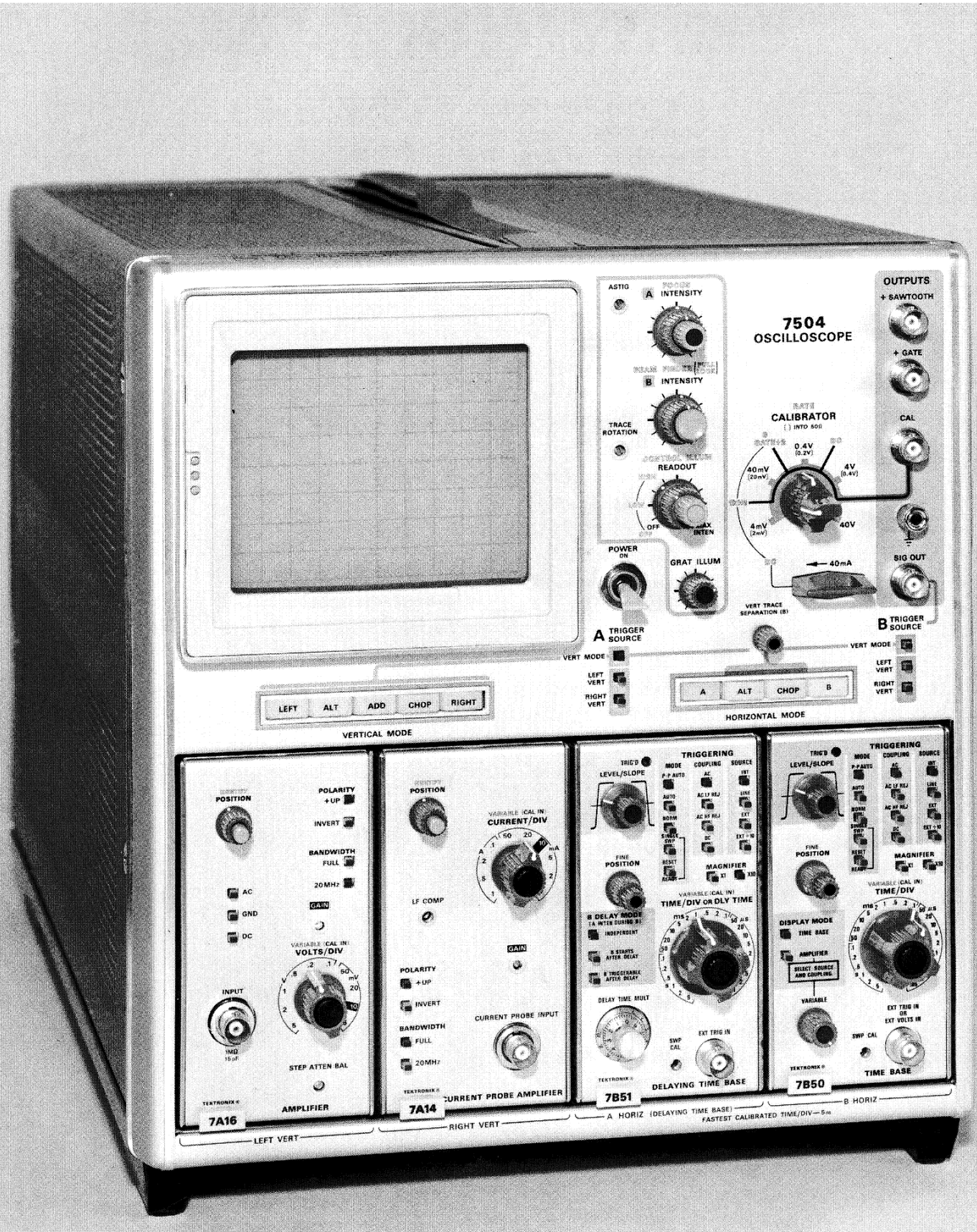

7504
OSCILLOSCOPE
OUTPUTS
+ SAWTOOTH
+ GATE
CAL
SIG OUT
ASTIG
A INTENSITY
B INTENSITY
TRACE ROTATION
READOUT
OFF
MAX INTEN
POWER ON
GRAT ILLUM
CALIBRATOR
0.4V (0.2V)
40mV (20mV)
4V (0.4V)
4mV (2mV)
40V
40mA
VERT TRACE SEPARATION (B)
A TRIGGER SOURCE
B TRIGGER SOURCE
VERT MODE
LEFT VERT
RIGHT VERT
LEFT
ALT
ADD
CHOP
RIGHT
VERTICAL MODE
A
ALT
CHOP
B
HORIZONTAL MODE
POSITION
POLARITY
+UP
INVERT
BANDWIDTH
FULL
20MHz
AC
GND
DC
GAIN
VARIABLE (CAL IN)
VOLTS/DIV
INPUT
1MΩ
15pF
STEP ATTEN BAL
TEKTRONIX
7A16
AMPLIFIER
LF COMP
CURRENT/DIV
CURRENT PROBE INPUT
7A14
CURRENT PROBE AMPLIFIER
TRIGGERING
TRIG'D
LEVEL/SLOPE
MODE
COUPLING
SOURCE
FINE POSITION
MAGNIFIER
B DELAY MODE
INDEPENDENT
B STARTS AFTER DELAY
B TRIGGERABLE AFTER DELAY
TIME/DIV OR DLY TIME
DELAY TIME MULT
SWP CAL
EXT TRIG IN
7B51
DELAYING TIME BASE
DISPLAY MODE
TIME BASE
AMPLIFIER
SELECT SOURCE AND COUPLING
VARIABLE
TIME/DIV
EXT TRIG IN OR EXT VOLTS IN
7B50
TIME BASE
LEFT VERT
RIGHT VERT
A HORIZ (DELAYING TIME BASE)
B HORIZ
FASTEST CALIBRATED TIME/DIV—5ns

SYSTEM SPECIFICATIONS

Your 7000-Series oscilloscope system will provide exceptional flexibility in operation with a wide variety of general and special purpose plug-in amplifiers and time bases. The Type number of a particular plug-in identifies it thus: the first digit (7) denotes the oscilloscope system (7000); the second character describes the use of the plug-in—A for amplifier, B for "real time" time base, J or K for spectrum analyzer, L for single-unit spectrum analyzer (a double-width plug-in). M for miscellaneous, S for sampling unit, and T for sampling time base. The third and fourth digits in the plug-in title are sequence numbers. The table following lists specifications that are dependent upon the system as a whole.

7000-SERIES OSCILLOSCOPE SYSTEM SPECIFICATION

	7500-Series			7700-Series		Vertical System Deflection Factor Accuracy*			SIG OUT		Horizontal System
Plug-In Unit	Probe	BW	T_r	BW	T_r	EXT CAL 0-50°C	INT CAL 15°-35°C	INT CAL 0-50°C	BW	T_r	
7A11	Integral	90 MHz	3.9 ns	150 MHz	2.4 ns	2%	3%	4%	60 MHz	5.9 ns	Horizontal System bandwidth with 2 units of the same type operated X-Y with phase correction is 2 MHz for the 7500-Series, 3 MHz for the 7700-Series unless otherwise stated. Without phase correction the 7700-Series horizontal bandwidth upper 10% down point is 3 MHz; that of the 7500-Series is 5 MHz, unless otherwise indicated. X-Y phase shift with correction is 2° at 2 MHz for both Series unless otherwise stated.
7A12	None	75 MHz	4.7 ns	105 MHz	3.4 ns	2%	3%	4%	55 MHz	6.4 ns	
	P6053	75 MHz	4.7 ns	105 MHz	3.4 ns	3%	4%	5%	55 MHz	6.4 ns	
7A13	None	75 MHz	4.7 ns	100 MHz	3.5 ns	1 1/2%	2 1/2%	3 1/2%	55 MHz	6.4 ns	
	P6053	75 MHz	4.7 ns	100 MHz	3.5 ns	1 1/2%	2 1/2%	3 1/2%	55 MHz	6.4 ns	
7A14	P6021	45 MHz	7.8 ns	50 MHz	7.0 ns	2%	3%	4%	40 MHz	8.8 ns	
	P6022	75 MHz	4.7 ns	105 MHz	3.4 ns	2%	3%	4%	50 MHz	7.0 ns	
7A16	None	90 MHz	3.9 ns	150 MHz	2.4 ns	2%	3%	4%	60 MHz	5.9 ns	
	P6053	90 MHz	3.9 ns	150 MHz	2.4 ns	3%	4%	5%	60 MHz	5.9 ns	
7A22	None or	1.0 MHz	350 ns	1 MHz	350 ns	2%	3%	4%	1.0 MHz	350 ns	Both the 7700- and 7500-Series are specified as follows: Bandwidth with phase correction is 800 kHz; without phase correction bandwidth is 1 MHz ±10%; X-Y phase shift with phase correction is 1° at 100 kHz.
	Any	±10%	±9%	±10%	±9%				±10%	±9%	

*Deflection Factor accuracy is checked as follows:

EXT CAL 0°C to 50°C, plug-in gain is set at a temperature within 10°C of operating temperature, using an external calibrator whose accuracy is within .25%.

INT CAL 15°C to 35°C, plug-in gain is set while operating within a temperature range of +15°C to +35°C, using the oscilloscope calibrator.

INT CAL 0°C to 50°C, plug-in gain is set using the oscilloscope calibrator (within 10°C of the operating temperature) in a temperature range between 0°C and +50°C.

SECTION 1
TYPE 7504 SPECIFICATION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

The Tektronix Type 7504 Oscilloscope is a solid-state, high performance instrument designed for general-purpose applications. This instrument accepts Tektronix 7-series plug-in units to form a complete measurement system. The flexibility of this plug-in feature and the variety of plug-in units available allow the system to be used for many measurement applications.

The Type 7504 has four plug-in compartments. The left pair of plug-ins is connected to the vertical deflection system. The right pair is connected to the horizontal deflection system. Electronic switching between the plug-ins connected to each deflection system allows a dual-trace vertical display and/or a dual-sweep horizontal display. This instrument features regulated DC power supplies to assure that performance is not affected by variations in line voltage and frequency, or by changes in load due to the varying power requirements of the plug-in units. Maximum power consumption of this instrument is about 280 watts (60 hertz, 115-volt line).

The Type 7504 features a CRT with an 8 X 10 centimeter graticule area with small spot size and high writing rate. Additionally, the instrument includes a readout system providing CRT display of alpha-numeric information from the plug-ins, including deflection factor, sweep rate and other encoded parameters.

This instrument will meet the electrical characteristics listed in Table 1-1 following complete calibration as given in Section 5. The performance check procedure given in Section 5 provides a convenient method of checking instrument performance without making internal checks or adjustments. The following electrical characteristics apply over a calibration interval of 1000 hours and an ambient temperature range of 0°C to +50°C, except as otherwise indicated. Warmup time for given accuracy is 20 minutes.

NOTE

Many of the measurement capabilities of this instrument are determined by the choice of plug-in units. The following characteristics apply to the Type 7504 only. See the system specification later in this section for characteristics of the complete system.

TABLE 1-1

ELECTRICAL

Characteristic	Performance
VERTICAL DEFLECTION SYSTEM	
Deflection Factor	Compatible with all 7-series plug-in units.
Deflection Accuracy	Less than 1% difference between compartments.
Low-Frequency Linearity	0.1 division or less compression or expansion of a center-screen two-division signal when positioned to the top and bottom of the graticule area.
Isolation Between Compartments	At least 100:1 from DC to 75 megahertz.
Chopped Mode Repetition Rate	One megahertz ±20%.
Time segment from each compartment	0.4 to 0.6 microsecond.
Delay Line	Permits viewing of leading edge of triggering signal.

Characteristic	Performance
Vertical Display Modes (selected by front-panel VERTICAL MODE switch)	Left: Left vertical only. ALT: Dual-trace, alternate between vertical units. ADD: Added algebraically. CHOP: Dual-trace, chopped between vertical units. RIGHT: Right vertical only.
Trace Separation Range	At least + and − four divisions from center horizontal line of graticule.

TRIGGERING

Trigger Source (selected by front-panel A TRIGGER SOURCE and B TRIGGER SOURCE switches)	VERT MODE: Determined by vertical mode. LEFT VERT: From left vertical unit only. RIGHT VERT: From right vertical unit only.

HORIZONTAL DEFLECTION SYSTEM

Deflection Factor	Compatible with all 7-series plug-in units.
Deflection Accuracy	Less than 1% difference between compartments.
Fastest Calibrated Sweep Rate	Five nanoseconds/division.
Phase Shift Between Vertical and Horizontal Deflection Systems	
Without phase correction	2° or less from DC to at least 35 kilohertz.
With phase correction	Adjustable to less than 2° from DC to two megahertz.
Chopped Mode	
Repetition rate	200 kilohertz ±20%.
Time segment from each compartment	2.0 to 3.0 microseconds.
Horizontal Display Modes (selected by front-panel HORIZONTAL MODE switch)	A: A horizontal only. ALT: Dual-sweep, alternate between horizontal units. CHOP: Dual-sweep, chopped between horizontal units. B: B horizontal only.

Characteristic	Performance

CALIBRATOR

Wave Shape	Square wave.	
Polarity	Positive going with baseline at zero volts.	
Output Voltage (selected by front-panel CALIBRATOR switch)		
Open circuit	Four millivolts to 40 volts in five decade steps.	
Into 50 ohms	Two millivolts to 0.4 volts in four steps.	
Output Current	40 milliamperes through current loop.	
Amplitude Accuracy (Voltage and Current)		
+15°C to +35°C	Within 1%.	
0°C to + 50°C	Within 2%.	
Repetition Rates (selected by front-panel RATE switch)	One kilohertz. One-half repetition rate of B sweep gate. DC.	
One-Kilohertz Accuracy	+15°C to +35°C Within 0.25%.	0°C to +50°C Within 0.5%
Duty Cycle	50% ±0.1%.	
Risetime and Falltime		
4 mV through 4 V and 40 mA	Less than 0.25 microsecond.	
40 V	Less than two microseconds with 10 pF load.	

EXTERNAL Z-AXIS INPUTS

High Sensitivity In-Put	
Sensitivity	Two volts peak-to-peak provides trace modulation over full intensity range.
Useful input voltage vs repetition frequency	Two volts peak-to-peak, DC to two megahertz; reducing to 0.4 volts peak-to-peak at 10 megahertz.
Polarity of operation	Positive-going signal decreases trace intensity; negative-going signal increases trace intensity.
Minimum pulse width that provides intensity modulation	40 nanoseconds at two volts.

Characteristic	Performance
Input resistance	500 ohms ±10%.
Maximum input voltage	15 volts (DC + peak AC).
High Speed Input	
Sensitivity	60 volts peak-to-peak provides trace modulation over full intensity range from DC to 75 megahertz.
Polarity of operation	Positive-going signal decreases trace intensity; negative-going signal increases trace intensity.
Minimum pulse width that provides intensity modulation	Five nanoseconds at 60 volts.
Input resistance at DC	7.5 kilohms ±10%.
Maximum input voltage	60 volts (DC + peak AC). 60 volts peak-to-peak AC.

SIGNAL OUTPUTS

+ Sawtooth	
Source (selected by internal Sweep switch)	A HORIZ time-base unit or B HORIZ time-base unit.
Polarity	Positive-going with baseline at zero volts ±one volt (into one megohm).
Output voltage	
Rate of rise	
Into 50 ohms	50 millivolts/unit of time ±15%.[1]
Into one megohm	One volt/unit of time ±10%.[1]
Peak voltage	
Into 50 ohms	Greater than 500 millivolts.
Into one megohm	Greater than 10 volts.
Output resistance	950 ohms ±2%.
+ Gate	
Source (selected by internal Gate switch)	From A HORIZ time-base unit, B HORIZ time-base unit, or the delaying time-base unit (in A HORIZ compartment).
Output voltage	
Into 50 ohms	0.5 volt ±10%.
Into one megohm	10 volts ±10%.
Risetime into 50 ohms	20 nanoseconds or less.
Output resistance	950 ohms ±2%.
Vertical Signal Output	
Source	Determined by B TRIGGER SOURCE switch.
Output voltage	
Into 50 ohms	25 millivolts/division of vertical deflection ±25%.
Into one megohm	0.5 volt/division of vertical deflection ±25%.
Output resistance	950 ohms ±2%

POWER SUPPLY

Line Voltage Range (AC, RMS)	*Line voltage and range selected by Line Voltage Selector assembly on rear panel.*
115-volts nominal	90 to 110 volts. 104 to 126 volts. 112 to 136 volts.
230-volts nominal	180 to 220 volts. 208 to 252 volts. 224 to 272 volts.
Line Frequency	48 to 440 hertz.
Maximum Power Consumption	280 watts, 3.2 amperes at 60 hertz, 115-volt line.

CATHODE-RAY TUBE (CRT)

Graticule	
Type	Internal with variable edge lighting.
Area	Eight divisions vertical by ten divisions horizontal. Each division equals one centimeter.
Resolution	
Horizontal	At least 15 lines/division.
Vertical	At least 15 lines/division.
Geometry	0.1 division or less total bowing of a displayed horizontal or vertical line.
Beam Finder	Limits display within graticule area.

[1] Unit of time selected by time-base time/division switch.

Characteristic	Performance
Photographic Writing Speed (without film fogging techniques)	
Tektronix C-51 Camera with f1.2 lens and 1:0.5 object-to-image ratio	At least 2250 centimeters/microsecond with Polaroid[2] Type 410 film (10,000 ASA) and P31 CRT phosphor.
Tektronix C-27 Camera with f1.3 lens and 1:0.5 object-to-image ratio	At least 1500 centimeters/microsecond with Polaroid Type 410 film (10,000 ASA) and P31 CRT phosphor.

TABLE 1-2

ENVIRONMENTAL

Characteristic	Performance
NOTE *This instrument will meet the electrical characteristics given in Table 1-1 over the following environmental limits. Complete details on environmental test procedures, including failure criteria, etc., can be obtained from Tektronix, Inc. Contact your local Tektronix Field Office or representative.*	
Temperature Range	
Operating	0°C to +50°C.
Non-operating	−55°C to +75°C.
Altitude	
Operating	15,000 feet.
Non-operating	Test limit 50,000 feet.
Electro-magnetic Interference (EMI) as tested in MIL-I 6181 D (when equipped with EMI modification only)	
Radiated interference	Interference radiated from the instrument under test within the given limits from 150 kilohertz to 1000 megahertz.
Conducted interference	Interference conducted out of the instrument under test through the power cord within the given limits from 150 kilohertz to 25 megahertz.
Transportation (packaged instruments, without plug-ins)	Qualifies under National Safe Transit Committee test procedure 1A.

[2] Registered trademark of the Polaroid Corporation.

TABLE 1-3

PHYSICAL

Characteristic	Performance
Ventilation	Safe operating temperature is maintained by convection cooling. Automatic resetting thermal cutout protects instrument from overheating.
Warm-up Time	20 minutes for rated accuracy.
Finish	Anodized front panel. Blue-vinyl painted aluminum cabinet.
Overall Dimensions (measured at maximum points)	
Height	13.5 inches (34.2 centimeters).
Width	12 inches (30.5 centimeters).
Length	24.6 inches (62.2 centimeters).
Net Weight (instrument only)	54 pounds (24.6 kilograms).

STANDARD ACCESSORIES

Standard accessories supplied with the Type 7504 are listed on the last pull-out page of the Mechanical Parts List illustrations. For optional accessories available for use with this instrument, see the Tektronix, Inc. catalog.

INSTRUMENT OPTIONS

General

The following options are available for the Type 7504 and can be installed as part of the instrument when ordered, or they can be installed at a later time. Complete information on all options for this instrument is given in this manual. For further information on instrument options, see your Tektronix, Inc. catalog, or contact your local Tektronix Field Office or representative.

Option 1

This option deletes the Readout System. Operation of the instrument is unchanged except that there is no alpha-numeric display on the CRT and the READOUT control is non-functional. The Readout System can be added at any time by ordering the readout conversion kit.

Option 2

The X-Y Delay Compensation Network can be added to the instrument to equilize the signal delay between the vertical and horizontal deflection systems. When this network is installed and activated, the phase shift between the vertical and horizontal channels is adjustable to less than 2° from DC to two megahertz.

Option 3

With option 3 installed, the instrument will meet the EMI interference specifications given in Table 1-2.

SECTION 3
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual contains a description of the circuitry used in the Type 7504 Oscilloscope. The description begins with a discussion of the instrument using the basic block diagram shown in Fig. 3-1. Then, each circuit is described in detail using detailed block diagrams to show the interconnections between the stages in each major circuit and the relationship of the front-panel controls to the individual stages.

A complete block diagram is located in the Diagrams section at the back of this manual. This block diagram shows the overall relationship between all of the circuits. Complete schematics of each circuit are also given in the Diagrams section. Refer to these diagrams throughout the following circuit description for electrical values and relationship.

BLOCK DIAGRAM

General

The following discussion is provided to aid in understanding the overall concept of the Type 7504 before the individual circuits are discussed in detail. A basic block diagram of the Type 7504 is shown in Fig. 3-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each block represents a major circuit within the instrument. The number on each block refers to the complete circuit diagram which is located at the rear of this manual.

Vertical signals to be displayed on the CRT are applied to the Vertical Interface circuit from both vertical plug-in compartments. The Vertical Interface circuit determines whether the signal from the left and/or right vertical unit is displayed. The vertical signal selected is then amplified by the Vertical Amplifier circuit to bring it to the level necessary to drive the vertical deflection plates of the CRT. This circuit also includes an input to produce the vertical portion of a readout display.

Horizontal signals for display on the CRT are connected to the X-Y Delay Compensation and Horizontal Interface circuit from both horizontal plug-in compartments. The X-Y Delay Compensation network (optional feature) provides a delay for the horizontal (X) portion of an X-Y display to match the delay of the vertical (Y) signal due to the delay line. The Horizontal Interface circuit determines whether the signal from the A and/or B horizontal unit is displayed. The horizontal signal selected by the Horizontal Interface circuit is connected to the Horizontal Amplifier circuit which amplifies it to provide the horizontal deflection for the CRT. This circuit also accepts the X-signal from the Readout System to produce the horizontal portion of a readout display. The Readout System provides alphanumeric display of information encoded by the plug-in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis with the analog waveform display.

The internal trigger signals from the vertical plug-in units are connected to the Trigger Selector circuit. This circuit selects the trigger signal which is connected to the horizontal plug-in units. It also provides the drive signal for the Output Signals circuit to provide an output which is a sample of the vertical signal. The Output Signals circuit also provides a sawtooth output signal and a gate output signal. The Calibrator circuit produces a square-wave output with accurate amplitude which can be used to check the calibration of this instrument and the compensation of probes. The repetition rate of the output signal is selectable; either DC, one kilohertz, or one-half the B gate. This signal is available as a voltage at the CAL connector and as a current through the 40 mA current loop.

The Logic Circuit develops control signals for use in other circuits within this instrument and the plug-in units. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and Type 7504 control settings. The Z-Axis Amplifier circuit provides the drive signal to control the CRT intensity level through the CRT Circuit. The CRT Circuit produces the voltages and contains the controls necessary for operation of the cathode-ray tube.

The Low-Voltage Power Supply circuit provides the power necessary for operation of this instrument. This voltage is connected to all circuits within the instrument. The Front-Panel Controls and Cabling circuit shows the switching logic of the front-panel controls. It also includes the input network for the Z-AXIS INPUTS and the output connectors to supply probe power to active probe systems.

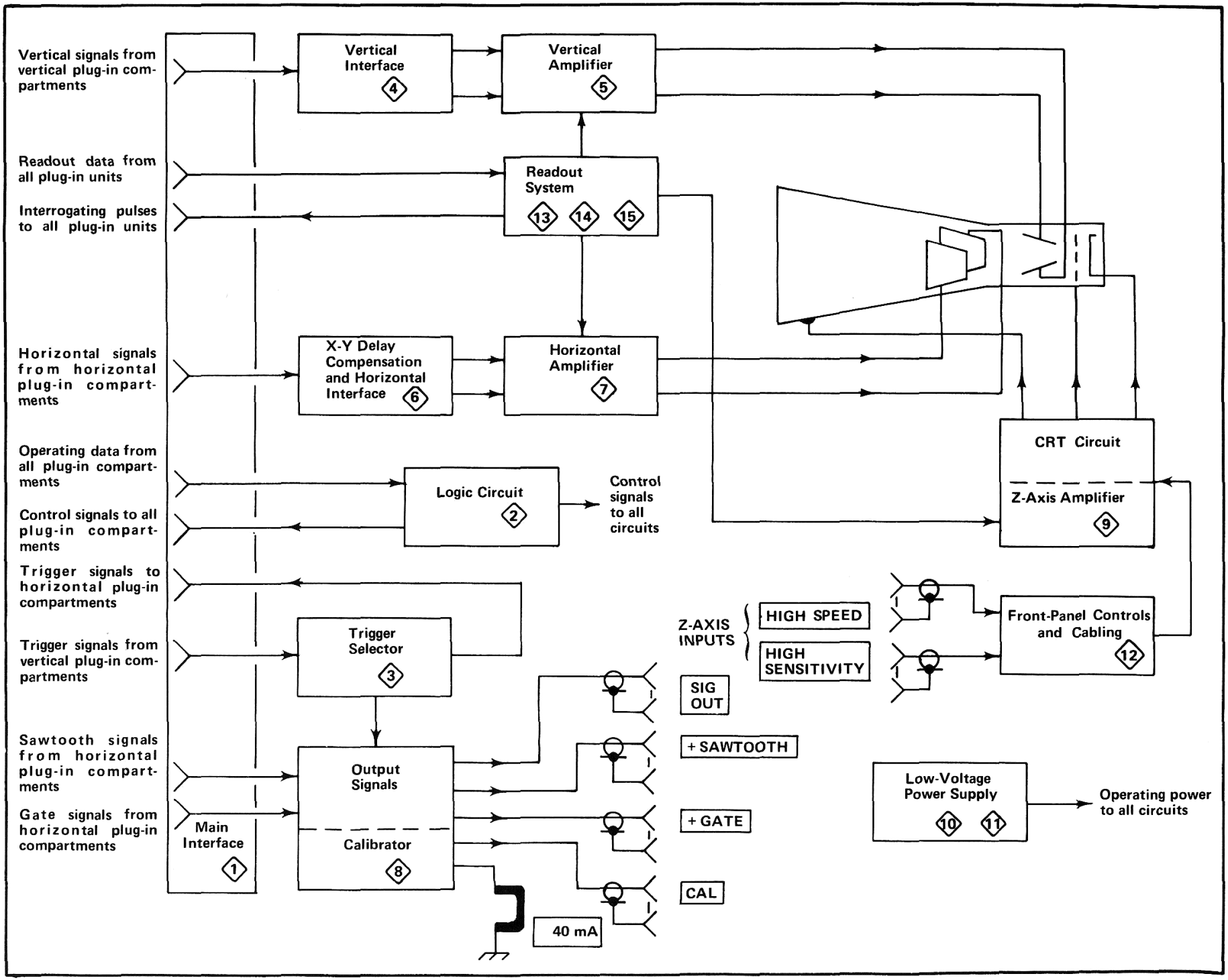


Fig. 3-1. Basic block diagram of the Type 7504 Oscilloscope.

CIRCUIT OPERATION

General

This section provides a detailed description of the electrical operation and relationship of the circuits in the Type 7504. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits which are commonly used in the electronics industry are not described in detail. If more information is desired on these commonly used circuits, refer to the following textbooks:

Tektronix Circuit Concepts Books (order from your local Tektronix Field Office or representative):

Cathode-Ray Tubes, Tektronix Part No. 062-0852-01.

Oscilloscope Trigger Circuits, Tektronix Part No, 062-1056-00.

Power Supply Circuits, Tektronix Part No. 062-0888-01.

Sweep Generator Circuits, Tektronix Part No. 062-1098-00.

Phillip Cutler, "Semiconductor Circuit Analysis", McGraw-Hill, New York, 1964.

Lloyd P. Hunter (Ed.), "Handbook of Semiconductor Electronics", second edition, McGraw-Hill, New York, 1962.

Jacob Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, 1965.

The following circuit analysis is written around the detailed block diagrams which are given for each major circuit. These detailed block diagrams give the names of the individual stages within the major circuits and show how they are connected together to form the major circuit. The block diagrams also show the inputs and outputs for each circuit and the relationship of the front-panel controls to the individual stages. The circuit diagrams from which the detailed block diagrams are derived are shown in the Diagrams section.

NOTE

All references to direction of current in this manual are in terms of conventional current; i.e., from plus to minus.

LOGIC FUNDAMENTALS

General

Digital logic techniques are used to perform many functions within this instrument. The function and operation of the logic circuits are described using logic symbology and terminology. This portion of the manual is provided to aid in the understanding of these symbols and terms. The following information is a basic introduction to logic concepts, not a comprehensive discussion of the subject. For further information on binary number systems and the associated Boolean Algebra concepts, the derivation of logic functions, a more detailed analysis of digital logic, etc., refer to the following textbooks:

Tektronix Circuit Concepts booklet, "Digital Concepts", Tektronix Part No. 062-1030-00.

Robert C. Baron and Albert T. Piccirilli, "Digital Logic and Computer Operations", McGraw-Hill, New York, 1967.

Thomas C. Bartee, "Digital Computer Fundamentals", McGraw Hill, New York, 1966.

Yaohan Chu, "Digital Computer Design Fundamentals", McGraw-Hill, New York, 1962.

Joseph Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, Chapters 9-11, 1965.

Symbols

The operation of circuits within the Type 7504 which use digital techniques is described using the graphic symbols set forth in military standard MIL-STD-806B. Table 3-1 provides a basic logic reference for the logic devices used within this instrument. Any deviations from the standard symbology, or devices not defined by the standard will be described in the circuit description for the applicable device.

Logic Polarity

All logic functions are described using the positive logic convention. Positive logic is a system of notation where the more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false or 0-state. The HI-LO method of notation is used in this logic description.

NOTE

The HI-LO logic notation can be conveniently converted to 1-0 notation by disregarding the first letter of each state. For example:

$$HI = H\,I$$
$$LO = L\,O$$

The specific voltages which constitute a HI or LO state vary between individual devices. Typical HI and LO logic levels are shown on the diagrams at the rear of this manual.

Wherever possible, the input and output lines are named to indicate the function that they perform when at the HI (true) state. For example, the line labeled, "Display B Command" means that the B Time-Base unit will be displayed when this line is HI or true. Likewise, the line labeled "X-Compensation Inhibit" means that the X-Compensation function is inhibited or disabled when this line is HI.

Input/Output Tables

Input/output (truth) tables are used in conjunction with the logic diagrams to show the input combinations which are of importance to a particular function, along with the resultant output conditions. This table may be given either for an individual device or for a complete logic stage. For examples of input/output tables for individual devices, see Table 3-1.

Non-Digital Devices

It should be noted that not all of the integrated circuit devices in this instrument are digital logic devices. The function of non-digital devices will be described individually using operating waveforms or other techniques to illustrate their function.

TABLE 3-1

Basic Logic Reference

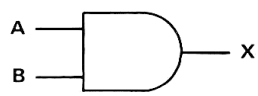
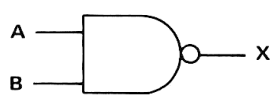
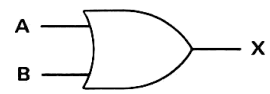
Device	Symbol	Description	Input/Output Table
AND gate		A device with two or more inputs and one output. The output of the AND gate is HI if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI LO HI LO LO HI HI HI
NAND gate		A device with two or more inputs and one output. The output of the NAND gate is LO if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI HI HI LO HI HI HI LO
OR gate		A device with two or more inputs and one output. The output of the OR gate is HI if one or more of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI HI HI LO HI HI HI HI

TABLE 3-1 (cont.)

Basic Logic Reference

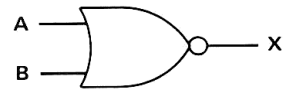
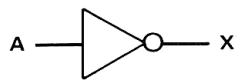
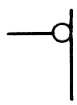
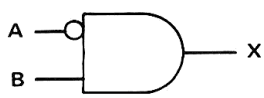
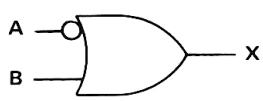
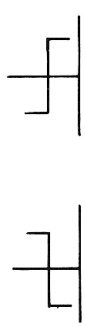
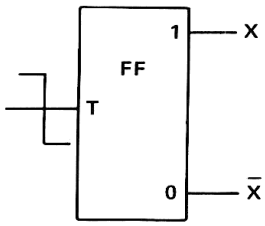
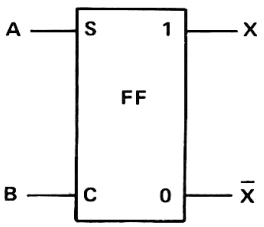
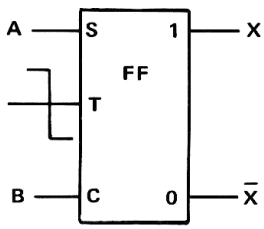
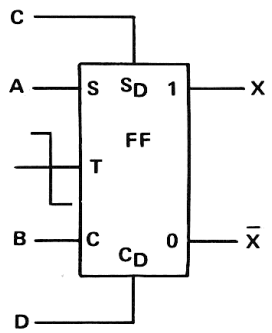
Device	Symbol	Description	Input/Output Table
NOR gate		A device with two or more inputs and one output. The output of the NOR gate is LO if one or more of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI LO HI LO LO HI HI LO
Inverter		A device with one input and one output. The output state is always opposite to the input state.	Input / Output A X LO HI HI LO
LO-state indicator		A small circle at the input or output of a symbol indicates that the LO state is the significant state. Absence of the circle indicates that the HI state is the significant state. Two examples follow:	
		AND gate with LO-state indicator at the A input. The output of this gate is HI if and only if the A input is LO and the B input is HI.	Input / Output A B X LO LO LO LO HI HI HI LO LO HI HI LO
		OR gate with LO-state indicator at the A input: The output of this gate is HI if either the A input is LO or the B input is HI.	Input / Output A B X LO LO HI LO HI HI HI LO LO HI HI HI
Edge symbol		Normally superimposed on an input line to a logic symbol. Indicates that this input (usually the trigger input of a flip-flop) responds to the indicated transition of the applied signal.	

TABLE 3-1 (cont.)

Basic Logic Reference

Device	Symbol	Description	Input/Output Table
Triggered (toggle) Flip-Flop		A bistable device with one input and two outputs which changes output states from one stable state to the other stable state with each trigger (either or both outputs may be used). The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	**Input / Output** **Condition before trigger pulse** / **Condition after trigger pulse** X | $\overline{X}$ | X | $\overline{X}$ LO | HI | HI | LO HI | LO | LO | HI
Set-Clear (J-K) Flip-Flop		A bistable device with two inputs and two outputs which changes output states in response to the states at the inputs (either or both outputs may be used). The outputs are complementary (i.e., when one output is HI the other is LO).	**Input / Output** A | B | X | $\overline{X}$ LO | LO | No change LO | HI | LO | HI HI | LO | HI | LO HI | HI | Changes state
Triggered Set-Clear (J-K) Flip-Flop	Without direct inputs  With direct inputs 	A bistable device with three or more inputs and two outputs (either or both inputs may be used). When triggered, the output changes states in response to the states at the inputs prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device. For devices with direct-set (S_D) or direct-clear (C_D) inputs, the indicated state at either of these inputs over-rides all other inputs (including trigger) to set the outputs to the states shown in the input/output table.	**Input / Output** A | B | C^1 | D^1 | X | $\overline{X}$ Conditions for triggered operation (output condition after trigger pulse) LO | LO | LO | LO | No change LO | HI | LO | LO | LO | HI HI | LO | LO | LO | HI | LO HI | HI | LO | LO | Changes state Conditions for direct-set, direct-clear operation Φ | Φ | LO | LO | No change Φ | Φ | LO | HI | LO | HI Φ | Φ | HI | LO | HI | LO Φ | Φ | HI | HI | Undefined Φ = Has no effect in this case [1] Applies only with direct inputs.

MAIN INTERFACE

General

Diagram 1 shows the plug-in interface and the interconnections between the plug-in compartments, circuit boards, etc. of this instrument. The circuitry shown on this diagram associated with Q24 and Q28 is described in connection with the Trigger Selector circuit.

LOGIC CIRCUIT

General

The Logic Circuit develops control signals for use in other circuits within this instrument. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and Type 7504 control settings. A block diagram of the Logic Circuit is shown in Fig. 3-2. This diagram shows the source of the input control signals, the output signals produced by this stage, and the basic interconnections between blocks. The interconnections shown are intended only to indicate inter-relation between blocks and do not indicate a direct connection or that only a single connection is made between the given blocks. Details of the inter-relation between stages in this circuit are given in the circuit description which follows. A schematic of this circuit is shown on diagram 2 at the rear of this manual.

This circuit description for the Logic Circuit is written with the approach that each of the integrated circuits and its associated discrete components comprises an individual stage as shown by the block diagram (Fig. 3-2). The operation of each of these stages is discussed relating the input signals and/or levels to the output, with consideration given to the various modes of operation that may affect the stage. A logic diagram is also provided for each stage. These diagrams are not discussed in detail but are provided to aid in relating the function performed by a given stage to standard logic techniques. It should be noted that these logic diagrams are not an exact representation of the internal structure of the integrated circuit but are only a logic diagram of the function performed by the stage. An input/output table is given, where applicable, for use along with the circuit description and logic diagram. These input/output tables document the combination of input conditions which are of importance to perform the prescribed function of an individual stage.

Horizontal Logic

General. The Horizontal Logic stage performs three separate logic functions. These functions are; A Sweep Inhibit, B Sweep Inhibit, and Alternate Pulse Generator. Fig. 3-3 identifies the three individual stages and the input and output terminals associated with each. Notice that some of the input levels are used in several or all of the individual stages.

A Sweep Inhibit. The A Sweep Inhibit stage produces an output level at pin 14 which determines if the A Time-Base unit can produce a sweep. If this level is HI, the A Time-Base unit is locked out (disabled) so it cannot produce a sweep. If the level is LO, the A Time-Base unit is enabled and can produce a sweep when triggered.

Only two combinations of input conditions produce an A Sweep Inhibit level (HI); if any one of the prescribed conditions is not met, the A Sweep Inhibit level is LO to enable the A Time-Base unit. These conditions are:

1. Pin 1 HI—HORIZONTAL MODE switch set to ALT.

   Pin 4 HI—A Horizontal unit operated in time-base mode.

   Pin 5 HI—B Horizontal unit operated in time-base mode.

   Pin 12 LO—A Time-Base unit in independent (non-delayed) mode.

   Pin 16 HI—B Sweep unit is being displayed in the horizontal-alternate mode.

2. Pin 2 LO—A Time-Base unit is not already producing a sweep.

   Pin 12 HI—A Time-Base unit in delayed mode.

   Pin 13 HI—B Time-Base unit has just completed a sweep and is in holdoff condition.

The first combination disables the A Sweep while the B Sweep is being displayed in the horizontal ALT mode (both units must be in time-base mode) if non-delayed operation is being used. The second combination disables the A Sweep during delayed-sweep operation so the B Sweep can complete its holdoff before the next A Sweep begins.

A logic diagram for the A Sweep Inhibit stage is shown in Fig. 3-4A. A table of input/output combinations for this stage is shown in Fig. 3-4B. This table shows the level at each input for the two combinations that produce a HI output level.

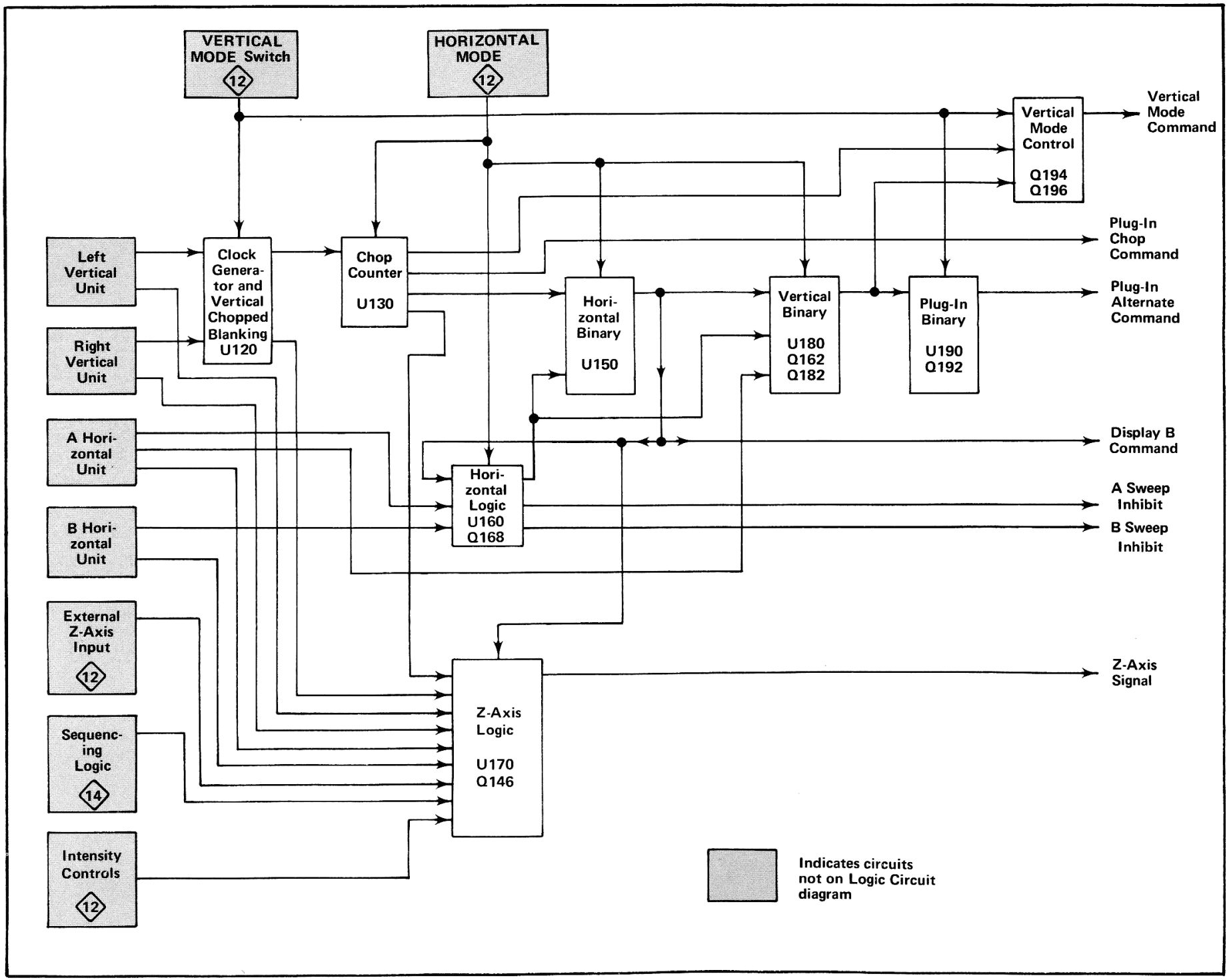


Fig. 3-2. Block diagram of Logic Circuit.

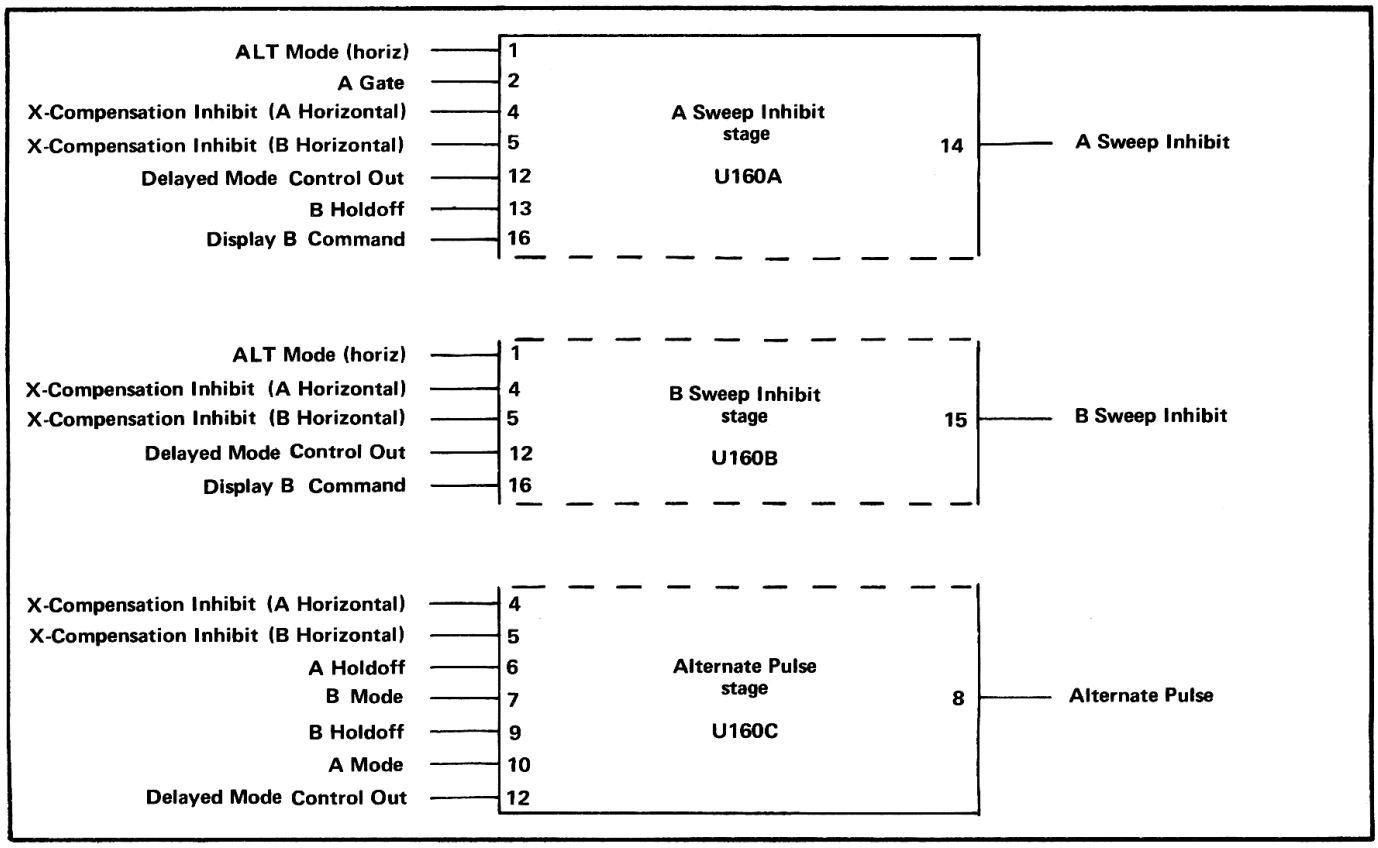


Fig. 3-3. Breakdown of separate stages within Horizontal Logic (U160) showing inputs and outputs for each stage.

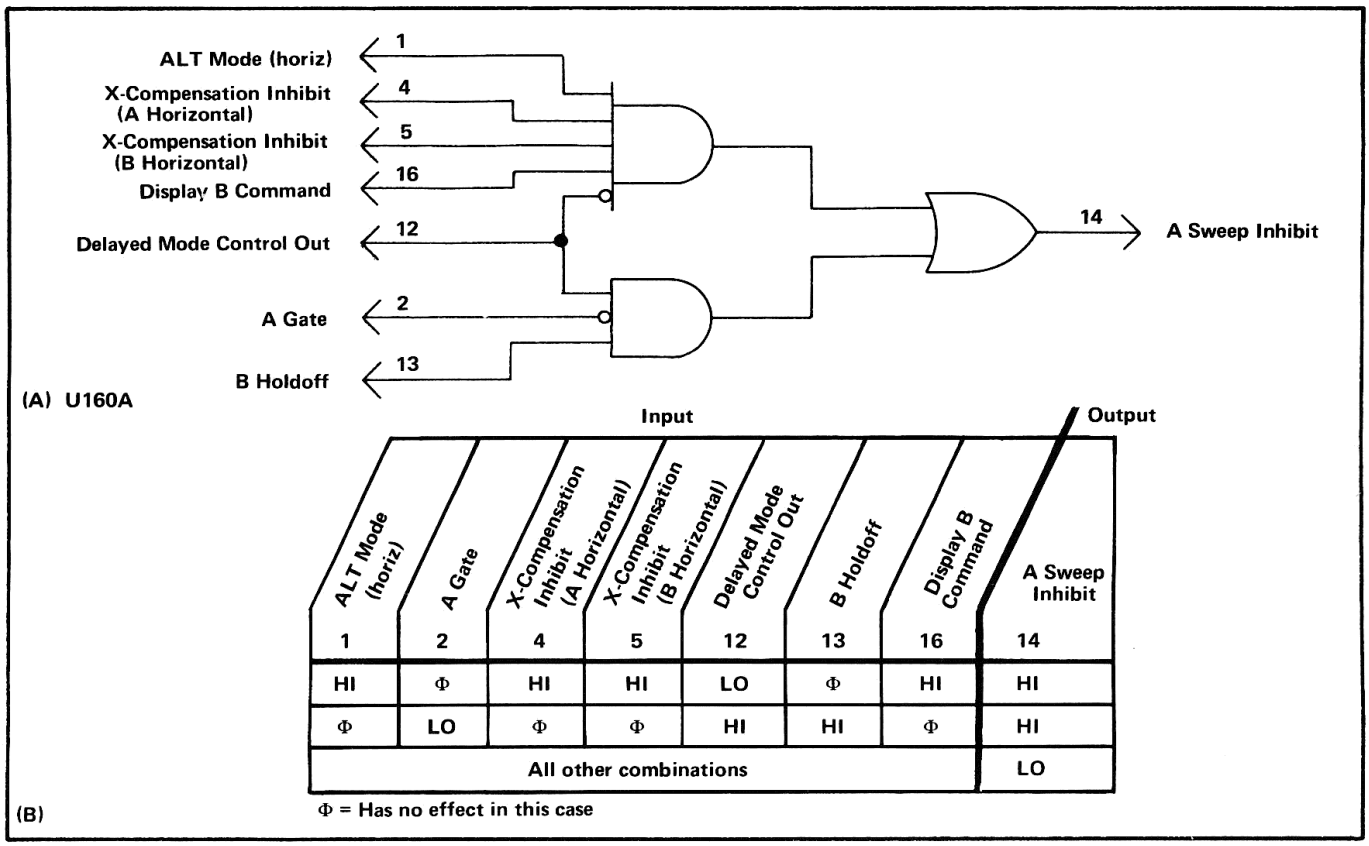


Fig. 3-4. (A) Logic diagram for A Sweep Inhibit stage, (B) Table of input/output combinations for A Sweep Inhibit stage.

B Sweep Inhibit. The B Sweep Inhibit stage produces an output level at pin 15 of U160B which determines if the B Time-Base unit can produce a sweep. A HI level at this pin disables the B Sweep and a LO level provides an enabling level to the B Time-Base unit. The output at pin 15 is HI only under one set of input conditions. These conditions are:

Pin 1 HI—HORIZONTAL MODE switch set to ALT.

Pin 4 HI—A Horizontal unit operated in time-base mode.

Pin 5 HI—B Horizontal unit operated in time-base mode.

Pin 12 LO—A Time-Base unit in independent (non-delayed) mode.

Pin 16 LO—A Sweep is being displayed in the horizontal-alternate mode.

These conditions disable the B Sweep while the A Sweep is being displayed in the horizontal ALT mode (both units must be in time-base mode) if non-delayed sweep is used. For any other combination of input conditions, the B Sweep Inhibit level at pin 15 is LO. However, the inhibit level to the B Time-Base unit is determined by both the Delay Gate from the A Time-Base unit and the B Sweep Inhibit level produced by this stage. The B Sweep is enabled only when both of these levels are LO.

Fig. 3-5A shows the logic diagram of the B Sweep Inhibit stage. The gate connected to the output of this stage is a phantom-OR gate located on the Main Interface diagram (a phantom-OR gate performs the OR-logic function merely by interconnection of the two signals). An input/output table for the B Sweep Inhibit stage is shown in Fig. 3-5B.

Alternate Pulse Generator. The third function performed by U160 is to produce alternate pulses for use by the horizontal and vertical alternate systems. The conditions that exist at the inputs to the Alternate Pulse Generator stage determine which time base provides the Alternate Pulse. The Alternate Pulse is a positive-going pulse (falling edge only used by following stages) which is coincident with the leading edge of the holdoff gate from the time-base units. The holdoff gate is produced at the end of the sweep by the respective time-base unit, and differentiated by either C165 or C166 to provide a positive-going pulse to pins 6 or 9. The Alternate Pulse is produced at the end of either the A Sweep or the B Sweep, or both, depending upon the operating conditions. The following discussions

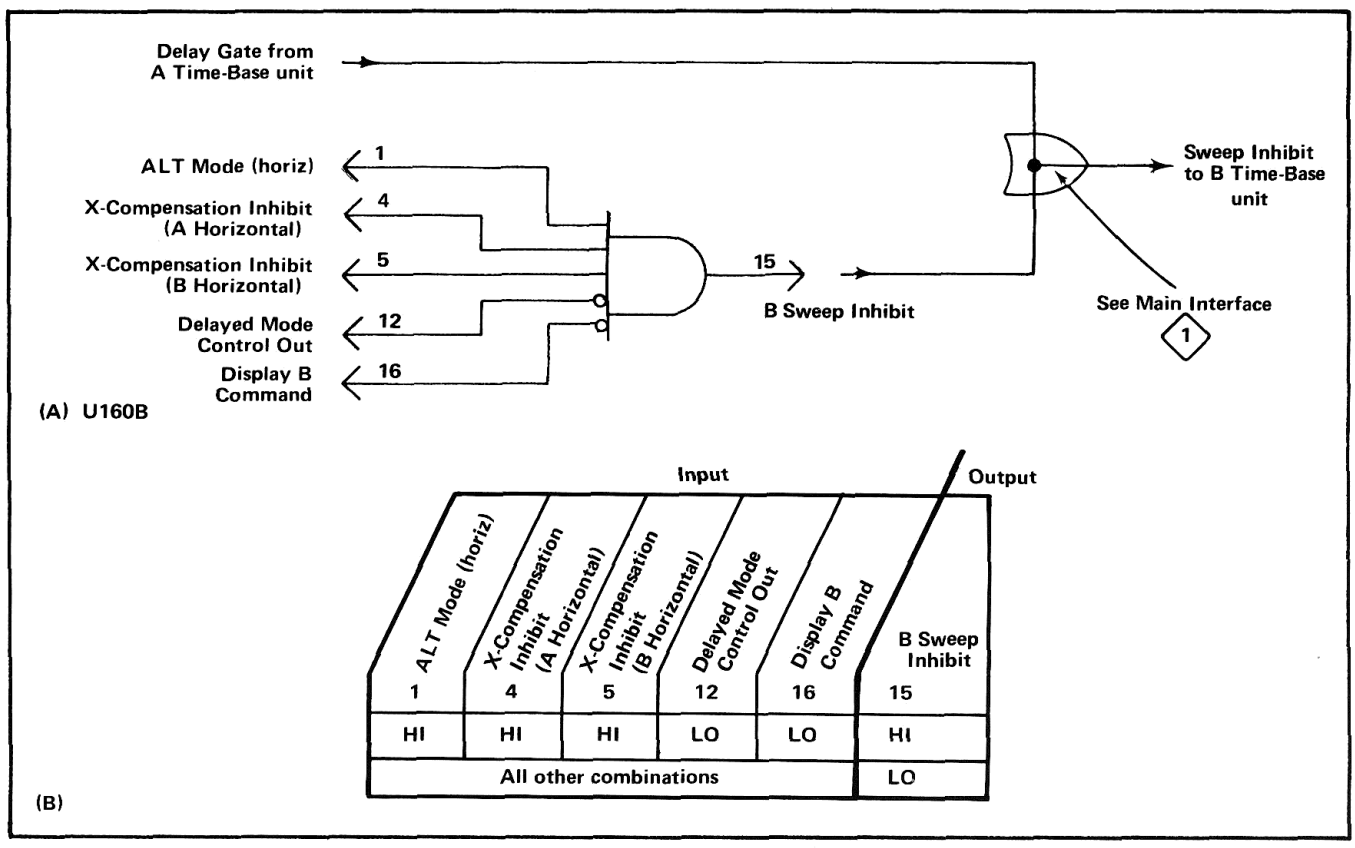


Fig. 3-5. (A) Logic diagram for B Sweep Inhibit stage, (B) Table of input/output combinations for B Sweep Inhibit stage.

describe the operation of the Alternate Pulse Generator stage in relation to various combinations of input conditions that can occur.

1. A (ONLY) MODE

The Alternate Pulse is produced only at the end of the A Sweep when the HORIZONTAL MODE switch is set to the A position. The input conditions are:

Pin 4 HI—A Horizontal unit operated in time-base mode.

Pin 6 HI—Holdoff pulse produced at end of A Sweep.

Pin 7 LO—HORIZONTAL MODE switch set to any position except B.

Pin 10 HI—HORIZONTAL MODE switch set to A.

2. B (ONLY) MODE—NON-DELAYED

In the B position of the HORIZONTAL MODE switch, the Alternate Pulse is produced only at the end of the B Sweep (A Time-Base must be in independent mode). The input conditions are:

Pin 5 HI—B Horizontal unit operated in time-base mode.

Pin 7 HI—HORIZONTAL MODE switch set to B.

Pin 9 HI—Holdoff pulse produced at end of B Sweep.

Pin 10 LO—HORIZONTAL MODE switch set to any position except A.

Pin 12 LO—A Time-Base unit in independent (non-delayed) mode.

3. ALTERNATE OR CHOPPED OPERATION—NON-DELAYED

When the HORIZONTAL MODE switch is set to ALT or CHOP (A Time-Base unit must be in independent mode), an Alternate Pulse is produced at the end of each sweep. For example, an Alternate Pulse is produced first at the end of the A Sweep, then at the end of the B Sweep, again at the end of the A Sweep, etc. Although Alternate Pulses are produced in the CHOP horizontal mode, they are not used in this instrument. The input conditions for this mode of operation are:

Pin 4 HI—A Horizontal unit operated in time-base mode.

Pin 5 HI—B Horizontal unit operated in time-base mode.

Pin 6 HI—Holdoff pulse produced at end of A Sweep[1].

Pin 7 LO—HORIZONTAL MODE switch set to any position except B.

Pin 9 HI—Holdoff pulse produced at end of B Sweep[1].

Pin 10 LO—HORIZONTAL MODE switch set to any position except A.

Pin 12 LO—A Time-Base unit in independent (non-delayed) mode.

4. DELAYED SWEEP

When the A Time-Base unit is set for delayed operation, the operation of the stage is changed so an Alternate Pulse is produced only at the end of the A Sweep even when the HORIZONTAL MODE switch is set to B. This is necessary since the A Time-Base establishes the amount of delay time for the B Time-Base whenever it is displayed. The input conditions for this mode of operation are:

Pin 4 HI—A Horizontal unit operated in time-base mode.

Pin 5 HI—B Horizontal unit operated in time-base mode.

Pin 6 HI—Holdoff pulse produced at end of A Sweep.

Pin 12 HI—A Time-Base unit in delayed mode.

5. VERTICAL UNIT IN HORIZONTAL COMPARTMENT

When a vertical unit is installed in either of the horizontal plug-in compartments, the Alternate Pulse can be produced only from the remaining time-base unit. If vertical units are installed in both horizontal plug-in compartments, an Alternate Pulse is not produced under normal operating conditions since there are no time-base units to produce a holdoff pulse.

NOTE

The conditions of the Alternate Pulse Generator with vertical units in both horizontal plug-in compartments are such that an Alternate Pulse could be produced if positive-going pulses are applied to pins 6 and 9. Although not used for normal operation, this mode may be used in special purpose plug-ins.

[1]**Simultaneous HI at pins 6 and 9 are not required; a HI at either input produces an Alternate Pulse if other conditions are met.**

6. ONE TIME-BASE UNIT REMOVED

If either of the time-base units is removed from its compartment, the Alternate Pulse is produced only from the remaining time-base unit.

A logic diagram for the Alternate Pulse Generator stage is shown in Fig. 3-6A. Note the resistors shown connected to pins 6 and 9 of U160C. These resistors, which are internal to the device, hold the level at pins 6 and 9 LO unless a HI level is applied to the corresponding input. Since the holdoff gate is capacitively coupled to pins 6 and 9, these inputs are at the LO level except when a differentiated A or B Holdoff Gate is received from the respective time base. Fig. 3-6B shows an input/output table for the Alternate Pulse Generator stage.

Z-Axis Logic

The Z-Axis Logic stage produces an output current which sets the intensity of the display on the CRT. The level of this output current is determined by the setting of the A or B INTENSITY controls, by a current added during B Sweep time to provide an intensified zone on the A Sweep for delayed-sweep operation, or by an external signal. The input current from the A and B INTENSITY controls is switched so the output current matches the horizontal display. The Vertical Chopped Blanking, Horizontal Chopped Blanking and Readout Blanking are applied to this stage to block the output current and blank the CRT display for vertical chopping, horizontal chopping, or during a readout display.

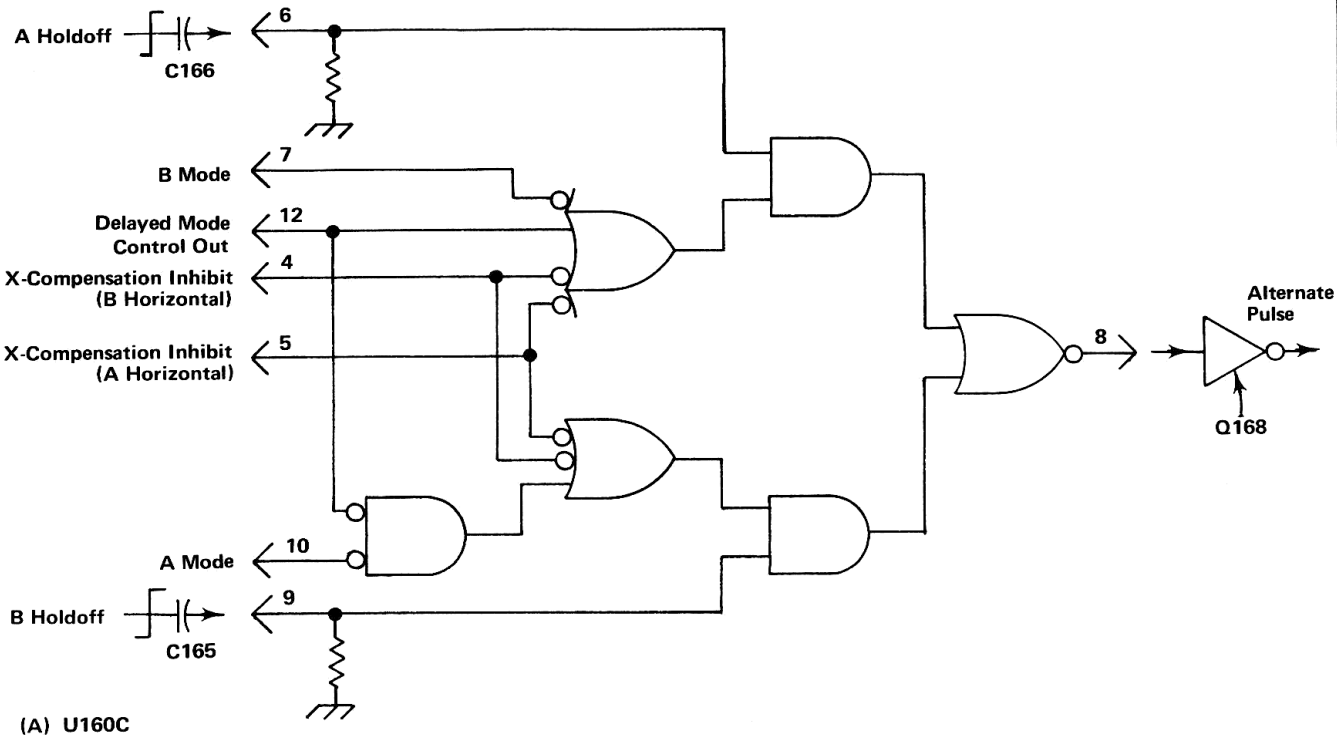
Fig. 3-7 identifies the inputs to the Z-Axis Logic circuit. This circuit is current-driven at all inputs except pins 5 and 15. The current at pins 1, 2, 9 and 16 is variable from 0 to 4 milliamperes and is determined by the applicable current source to control the output current at pin 8.

The Vertical Chopped Blanking connected to pin 6, and the Horizontal Chopped Blanking connected to both pins 6 and 7 through CR145-CR146, enables or disables this stage to control all output current. Quiescently, the level at pins 6 and 7 is HI so that the intensity current from pins 1, 2, 9 or 16 can pass to the output. However, pin 6 goes LO during Vertical Chopped Blanking and both pins 6 and 7 go LO for Horizontal Chopped Blanking or during a readout display. This blocks the output current and the CRT is blanked. The Vertical Chopped Blanking signal is connected to pin 6 of U170 directly from pin 4 of U120. The Horizontal Chopped Blanking signal is connected to U170 from pin 4 of U130 through LR134, Q146 and CR145-CR146 (see diagram 2). Notice that this signal is connected to the collector of Q146. This transistor is normally operating in the saturated condition and the HI Horizontal Chopped Blanking level from U130 is the collector source voltage. When the Horizontal Chopped Blanking level goes LO, the current through Q146 drops to produce a corresponding LO level at its emitter. This level is connected to both pins 6 and 7 of U170 through CR145 and CR146. Q146 also controls the levels at pins 6 and 7 for readout displays. The Z-Axis Logic OFF Command from the Readout Circuit is connected to the base of Q146 through VR148 and R147. This level is normally HI so Q146 operates as controlled by the Horizontal Chopped Blanking level at its collector. When a readout display is to be presented, the Z-Axis Logic OFF Command drops LO and this level is coupled to the base of Q146 through VR148 with very little voltage attenuation. Q146 is reverse-biased to produce a LO level at its emitter. This level is coupled to pins 6 and 7 of U170 through CR145 and CR146 to block the Z-Axis Logic output current during the readout display (intensity of readout display determined by a separate Readout Intensity level connected directly to the Z-Axis Amplifier; see CRT Circuit description). Diode CR147 clamps the emitter of Q146 at about −0.6 volts when this transistor is off.

The Intensity Limit input at pins 7 and 9 provides protection for the CRT phosphor at slow sweep rates. For conditions that do not require limiting, about 2.5 milliamperes is connected to pins 7 and 9. This current is established by resistors R141-R142-R143-R144-R145-R140-R175. When either of the time-base units is set to a sweep rate which requires intensity limiting, the junction of R143-R144-R145 is connected to ground in the time-base unit. This drops the current level at pins 7 and 9 to about 1.0 milliamperes to limit the output current from this stage. Limiting the output current of this stage in turn limits the maximum trace intensity for all CRT displays whenever either of the time-base units is set to a sweep rate that requires intensity limiting. The Max Intensity adjustment R140 is set to provide optimum writing rate on the CRT when the INTENSITY controls are set fully clockwise.

The A INTENSITY control sets the output current level when the A Gate at pin 14 is HI and the Display B Command at pin 15 is LO. Whenever the A Gate level goes LO indicating that the A Sweep is complete or the Display B level goes HI indicating that the B Sweep is being displayed, the A INTENSITY current is blocked. The current from the A INTENSITY control (see diagram 12) is connected to pin 16 through R176.

In the delayed mode, current is added to the A INTENSITY current during the A Sweep time to intensify a portion of the trace. This intensified portion is coincident with the B Sweep time to provide an indication of the portion of the display which will be displayed in the delayed mode. The A Intensified current is supplied to pin



(A) U160C

(B)

Input							Output	
X-Compensation Inhibit (A Horizontal) 4	X-Compensation Inhibit (B Horizontal) 5	A Holdoff 6	B Mode 7	B Holdoff 9	A Mode 10	Delayed Mode Control Out 12	Time-Base which is source of Alternate Pulse 8[2]	Horizontal Conditions
HI	Φ	HI[1]	LO	Φ	HI	Φ	A	A only
Φ	HI	Φ	HI	HI[1]	LO	LO	B	B only
HI	HI	HI[1]	LO	HI[1]	LO	LO	A and B	ALT or CHOP
HI	HI	HI[1]	Φ	Φ	Φ	HI	A	A delays B
HI	Φ[3]	HI[1]	Φ	LO	Φ	Φ	A	A with B Time-Base removed or vertical unit in B compartment
Φ[3]	HI	LO	Φ	HI[1]	Φ	LO	B	B with A Time-Base removed or vertical unit in A compartment
All other combinations							No output pulse (LO at output)	

Φ = Has no effect in this case

[1]Positive-going pulse. Where both A and B Holdoff are required to be HI, a HI at either input produces an Alternate Pulse.

[2]Negative-going pulse.

[3]LO if vertical unit installed in compartment.

Fig. 3-6. (A) Logic diagram for Alternate Pulse Generator stage, (B) Table of input/output combinations for the Alternate Pulse Generator stage.

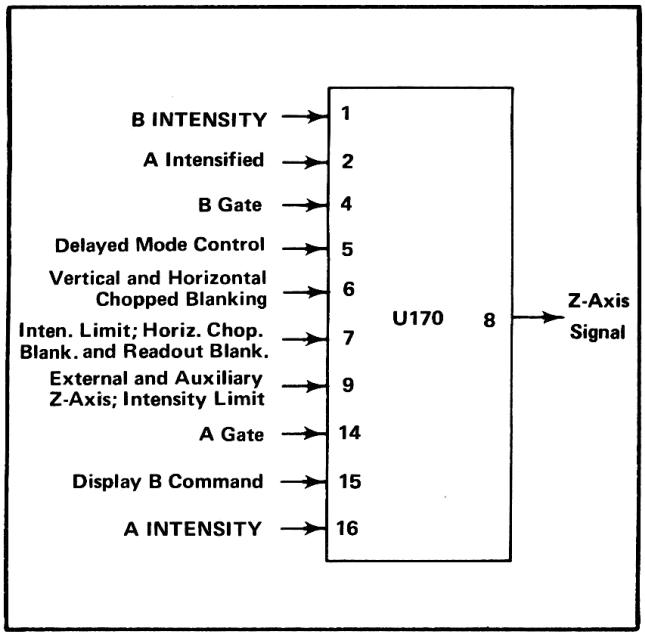


Fig. 3-7. Input and output pins for Z-Axis Logic stage.

2 of U170 from the A INTENSITY control through R178. With this configuration, the intensified current increases as the A INTENSITY control setting is advanced to provide a proportional intensity increase in the intensified zone as the overall A Sweep intensity increases. Therefore, the intensified zone is more readily visible at high intensity levels. The intensified current is added to the A INTENSITY current to produce an intensified zone on the A Sweep under the following conditions: HI A Gate level at pin 14, LO Display B Command at pin 15, HI B Gate level at pin 4, and HI Delayed Mode Control Out level at pin 5.

The B INTENSITY control determines the output current when the B Gate level at pin 4 and the Display B Command at pin 15 are both HI. The current from the B INTENSITY control (see diagram 12) is connected to the Z-Axis Logic stage through R179.

The current level established by the intensity controls can be altered by the External and Auxiliary Z-Axis current level at pin 9. The current at this pin can come from the Z AXIS INPUT connectors on the rear panel through R112 or from any of the plug-in compartments through R110, R111, R113, or R114. This current either increases or decreases, depending on polarity, the output current to modulate the intensity of the display. Input from the Z AXIS INPUT connectors allows the trace to be modulated by external signals. The auxiliary Z-Axis inputs from the plug-in compartments allow special purpose plug-in units to modulate the display intensity. Diodes CR175 and CR176 limit the maximum voltage change at pin 9 to about + and −0.6 volts to protect the Z-Axis Logic Stage if an excessive voltage is applied to the Z AXIS INPUT connectors.

Fig. 3-8A shows a logic diagram of the Z-Axis Logic stage. Notice the current-driven inputs as indicated by the current-generator symbols at the associated inputs. An input/output table for the Z-Axis Logic stage is given in Fig. 3-8B.

Horizontal Binary

The Horizontal Binary stage produces the Display B Command to determine which horizontal unit is to be displayed on the CRT. When this level is HI, the B Horizontal unit is displayed and when it is LO, the A Horizontal unit is displayed. The Display B Command is used in the following stages within the Logic Circuit: Horizontal Logic (A and B Lockout), Z-Axis Logic, and Vertical Binary. In addition, it is connected to the following circuits elsewhere in the instrument to indicate which horizontal unit is to be displayed: Main Interface circuit (A and B Horizontal plug-in compartments), Vertical Interface circuit (for trace separation) and Horizontal Interface circuit (for horizontal channel selection). Fig. 3-9 identifies the function of the input pins for this stage. The following discussions describe the operation of the Horizontal Binary stage in each position of the HORIZONTAL MODE switch.

1. A MODE

When the HORIZONTAL MODE switch is set to A, the Display B Command is LO to indicate to all circuits that the A Horizontal unit is to be displayed. The levels at pins 3, 4, 7 and 10 are determined by the HORIZONTAL MODE switch (see Front-Panel Controls and Cabling diagram). This switch indicates which horizontal mode has been selected by providing a HI output level on only one of four output lines; the remaining lines are LO. Therefore, for U150 either pin 3, pins 4 and 7 (notice that pins 4 and 7 are tied together at U150), or pin 10 can be HI and the two unselected lines from the HORIZONTAL MODE switch remain LO. The input conditions for A horizontal mode operation are:

Pin 3 HI—HORIZONTAL MODE switch set to A.

Pin 4 and 7 LO—HORIZONTAL MODE switch set to any position except B.

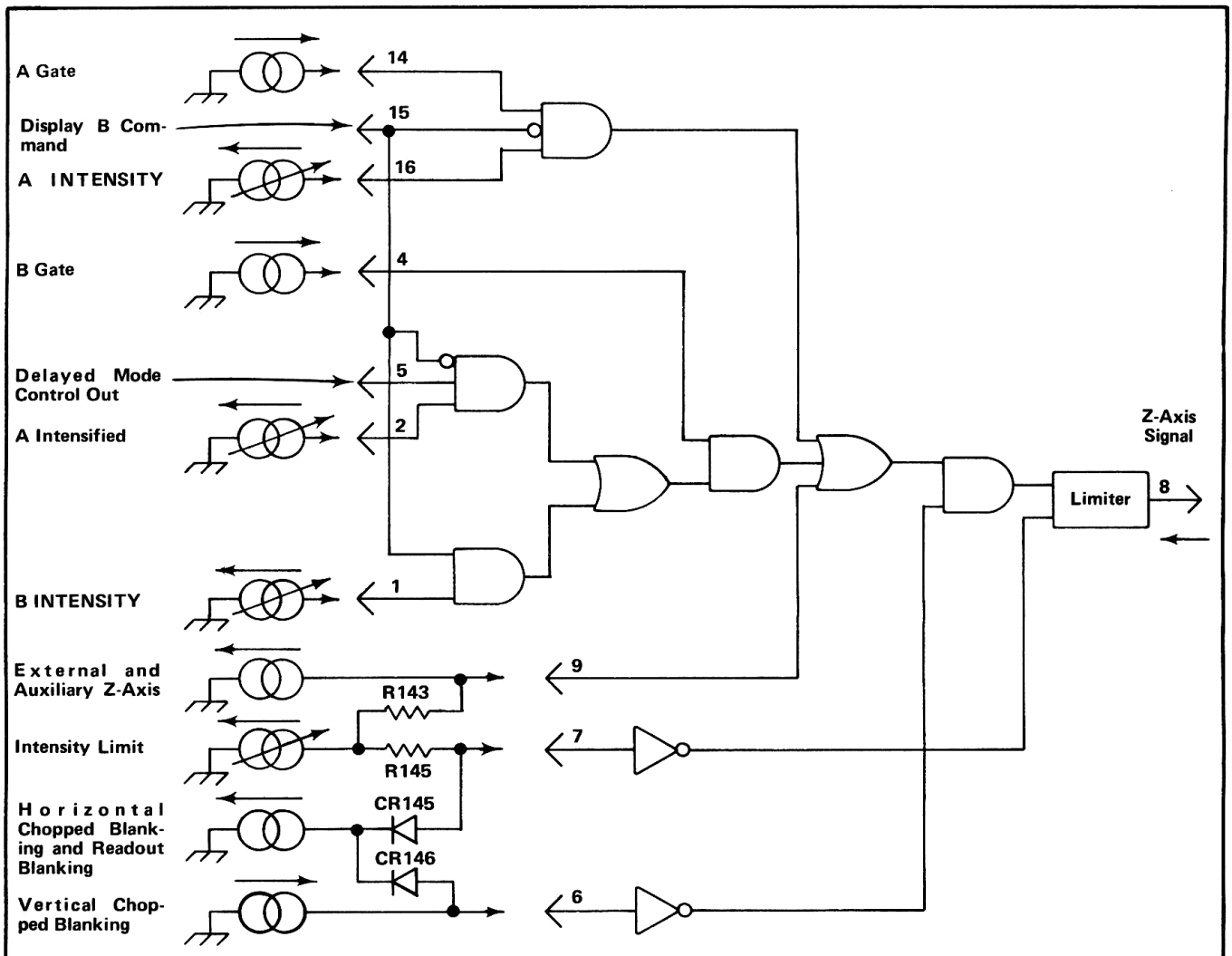
Pin 10 LO—HORIZONTAL MODE switch set to any position except CHOP.

2. B MODE

Selecting the B horizontal mode provides a HI Display B Command to all circuits. The input conditions are:

Pin 3 LO—HORIZONTAL MODE switch set to any position except A.

Pin 4 and 7 HI—HORIZONTAL MODE switch set to B.



(A)

Input									Output	
B INTENSITY	A Intensified	B Gate	Delayed Mode Control Out	Vertical and Horizontal Chopped Blanking	External and Auxiliary Z Axis	A Gate	Display B Command	A INTENSITY	Z-Axis Signal	Current source controlling Z-Axis Signal
1[1]	2[1]	4	5	6	9[1]	14	15	16[1]	8[1]	Z-Axis Signal
Φ	Φ	Φ	LO	HI	Φ[2]	HI	LO	HI	HI	A INTENSITY
HI	Φ	HI	Φ	HI	Φ[2]	Φ	HI	Φ	HI	B INTENSITY
Φ	HI	HI	HI	HI	Φ[2]	HI	LO	HI	HI	A INTENSITY and A Intensified
Φ	Φ	Φ	Φ	HI	HI	Φ	Φ	Φ	HI	External signal
All other combinations									LO	No output signal

(B)

LO = Minimum voltage or 0 mA current.

HI = Maximum voltage or maximum current.

Φ = Has no effect in this case

[1] Current level. LO = 0 mA
HI = Variable from 0 to 4 mA

[2] Current can be added or subtracted for intensity modulation.

Fig. 3-8. (A) Logic diagram for Z-Axis Logic circuit, (B) Table of input/output combinations for Z-Axis Logic circuit.

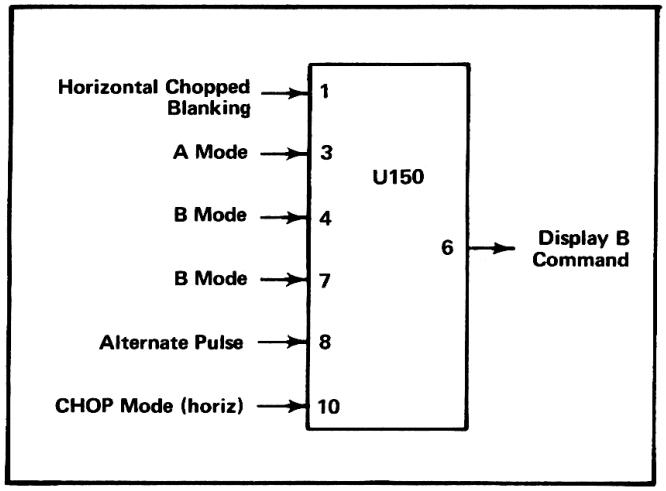


Fig. 3-9. Input and output pins for Horizontal Binary stage.

Pin 10 LO—HORIZONTAL MODE switch set to any position except CHOP.

3. CHOP MODE

In the CHOP position of the HORIZONTAL MODE switch, the Display B Command switches between the HI and LO levels to produce a display which switches between the A and B Horizontal units at a 0.2 megahertz rate. The repetition rate of the Display B Command in this mode is determined by the Horizontal Chopped Blanking pulse (see Chop Counter stage for further information on this pulse). Each time the Horizontal Chopped Blanking Pulse at pin 1 drops LO, the output at pin 6 switches to the opposite state. The input conditions which cause the output to change states are:

Pin 1 LO—Horizontal Chopped Blanking pulse generated by Chop Counter stage goes negative.

Pin 3 LO—HORIZONTAL MODE switch set to any position except A.

Pin 4 and 7 LO—HORIZONTAL MODE switch set to any position except B.

Pin 10 HI—HORIZONTAL MODE switch set to CHOP.

4. ALT MODE

For ALT horizontal operation, the Display B Command switches to the opposite state each time the negative-going portion of the Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Display B Command in this mode is one-half the repetition rate of the Alternate Pulse. The input conditions which cause the output to change states are:

Pin 3 LO—HORIZONTAL MODE switch set to any position except A.

Pin 4 and 7 LO—HORIZONTAL MODE switch set to any position except B.

Pin 8 LO—Alternate Pulse generated by Horizontal Logic stage goes negative.

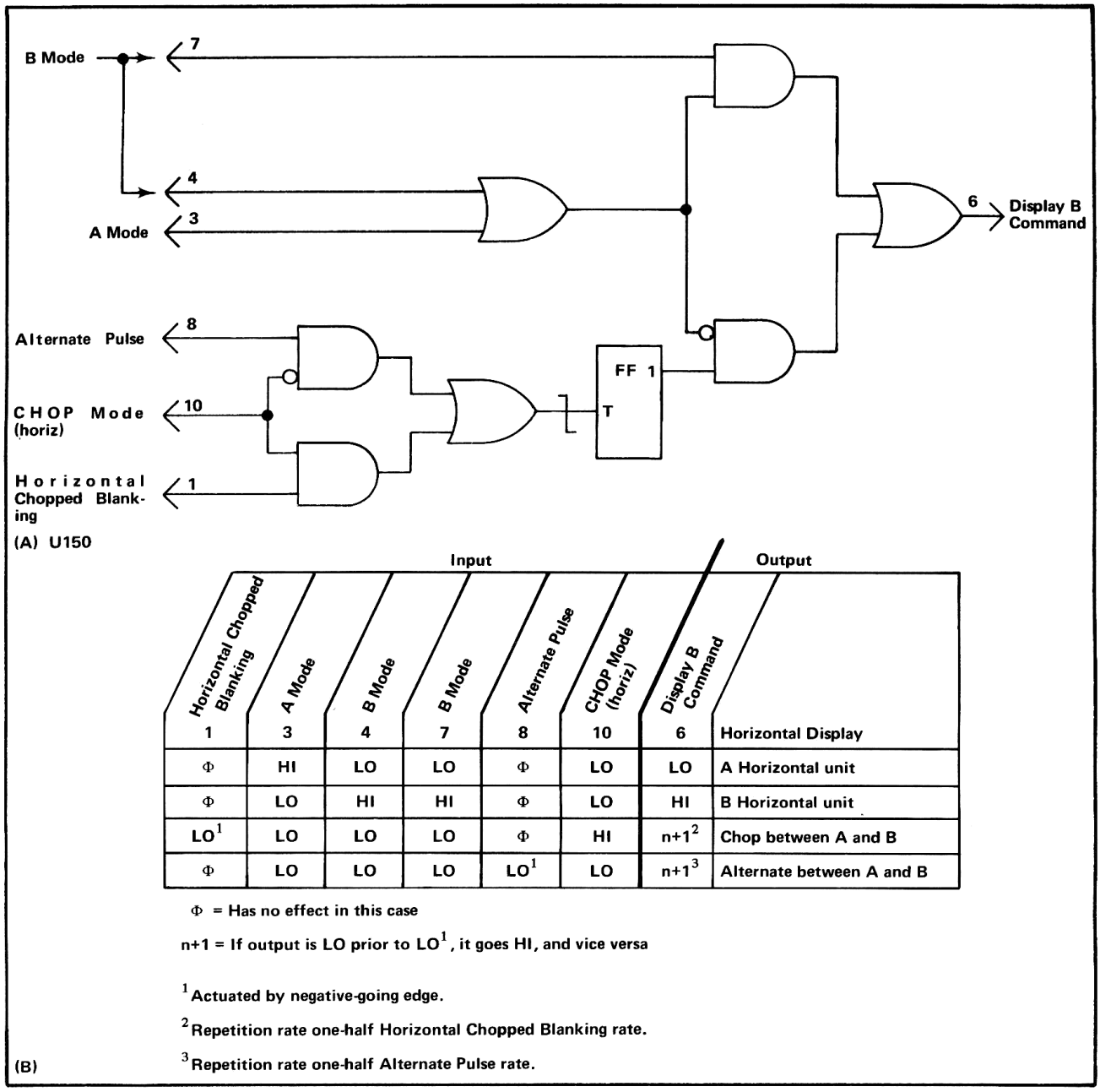
Pin 10 LO—HORIZONTAL MODE switch set to any position except CHOP.

Fig. 3-10A shows a logic diagram of the Horizontal Binary stage. An input/output table showing the conditions for each position of the HORIZONTAL MODE switch is shown in Fig. 3-10B.

Vertical Binary

The Vertical Binary stage produces the Display Right Command to determine which vertical unit is to be displayed on the CRT. When this output level is HI, the Right Vertical unit is displayed and when it is LO, the Left Vertical unit is displayed. In the ALT or CHOP positions of the HORIZONTAL MODE switch, (non-delayed operation only), the output of this stage is slaved to the output of the Horizontal Binary stage so that the Display Right Command is always HI when the Display B Command is HI, and vice versa. This action allows sweep-slaving operation in the ALT position of the VERTICAL MODE switch and the ALT or CHOP positions of the HORIZONTAL MODE switch whereby the Left Vertical unit is always displayed at the sweep rate of the B Time-Base unit and the Right Vertical unit at the sweep rate of the A Time-Base unit. When the A Time-Base unit is set to the delayed mode, the repetition rate of the Display Right Command is one-half the repetition rate of the Display B Command input. This results in each vertical unit being displayed first against the A Time-Base unit (delaying) and the B Time-Base unit (delayed) before the display is switched to the other vertical unit. The Display Right Command is used in the following stages within the Logic Circuit: Plug-In Binary, Vertical Chopped Blanking, and Vertical Mode Control. It is also connected to the following circuits elsewhere in the instrument to indicate which vertical unit is to be displayed (through Vertical Mode Control stage; ALT vertical mode only): Main Interface circuit (Left and Right Vertical plug-in compartments and trigger selection circuitry) and Vertical Interface circuit.

Fig. 3-11 identifies the function of the input pins for the Vertical Binary stage. This stage uses the same type of integrated circuit as the Horizontal Binary stage. Notice the Display A level at pin 7. This input is the inverse of the Display B level at pin 8. Therefore the Display A level is always HI when the Display B level is LO, and vice versa. The following discussions describe the operation of the Vertical Binary stage in relation to the modes of operation that can occur.



(A) U150

Input						Output	
Horizontal Chopped Blanking	A Mode	B Mode	B Mode	Alternate Pulse	CHOP Mode (horiz)	Display B Command	
1	3	4	7	8	10	6	Horizontal Display
Φ	HI	LO	LO	Φ	LO	LO	A Horizontal unit
Φ	LO	HI	HI	Φ	LO	HI	B Horizontal unit
LO[1]	LO	LO	LO	Φ	HI	n+1[2]	Chop between A and B
Φ	LO	LO	LO	LO[1]	LO	n+1[3]	Alternate between A and B

Φ = Has no effect in this case

n+1 = If output is LO prior to LO[1], it goes HI, and vice versa

[1] Actuated by negative-going edge.

[2] Repetition rate one-half Horizontal Chopped Blanking rate.

[3] Repetition rate one-half Alternate Pulse rate.

(B)

Fig. 3-10. (A) Logic diagram for Horizontal Binary stage, (B) Table of input/output combinations for the Horizontal Binary stage.

1. A OR B MODE

When the HORIZONTAL MODE switch is set to either A or B, the Display Right Command switches to the opposite state each time an Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Display Right Command in this mode is one-half the repetition rate of the Alternate Pulse. The input conditions for these modes are:

Pin 1 LO—Alternate Pulse generated by Horizontal Logic stage goes negative.

Pin 4 LO—HORIZONTAL MODE switch in any position except ALT or CHOP, or the A Time-Base unit is set for delayed sweep.

Pin 10 HI—HORIZONTAL MODE switch set to A or B.

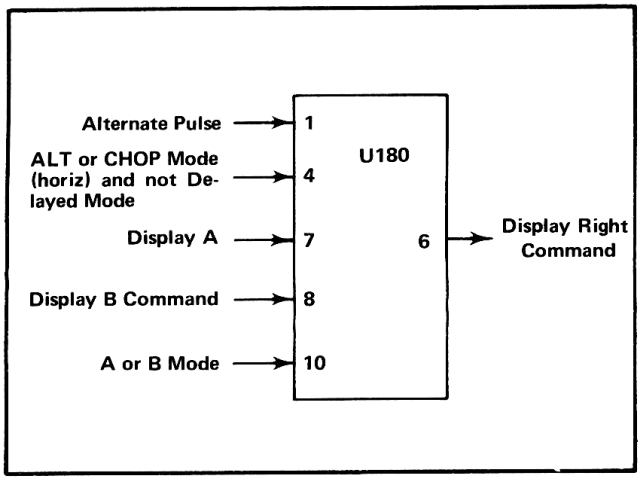


Fig. 3-11. Input and output pins for Vertical Binary stage.

2. ALT OR CHOP MODE (HORIZ.)—NON-DELAYED

In the ALT or CHOP positions of the HORIZONTAL MODE switch, the output level at Pin 6 is the same as the Display A level at pin 7. The Display A level is produced by inverting the Display B Command from the Horizontal Binary stage. Therefore, the repetition rate of the output signal is the same as the Display B Command. The result with the VERTICAL MODE switch set to ALT and the A Time-Base unit set for non-delayed operation is that the Right Vertical unit is always displayed at the sweep rate of the A Time-Base unit and the Left Vertical unit at the sweep rate of the B Time-Base unit (sweep slaving). The input conditions to provide a HI output level so that the Right Vertical unit can be displayed at the A Sweep rate are:

Pin 4 HI—HORIZONTAL MODE switch set to ALT or CHOP with non-delayed sweep.

Pin 7 HI—A Sweep is to be displayed (Display B Command LO).

Pin 10 LO—HORIZONTAL MODE switch set to any position except A or B.

The input conditions to provide a LO output level so the Left Vertical unit can be displayed at the B Sweep rate are:

Pin 4 HI—HORIZONTAL MODE switch set to ALT or CHOP with non-delayed sweep.

Pin 7 LO—B Sweep is to be displayed (Display B Command HI).

Pin 10 LO—HORIZONTAL MODE switch set to any position except A or B.

The Display Right Command switches from HI to LO along with the Display A level at pin 7 (inverse of Display B Command). However, notice that the Display Right Command changes from HI to LO as the Display B Command changes from LO to HI, and vice versa.

3. ALT OR CHOP MODE (HORIZ.)—DELAYED

If the A Time-Base unit is set to the delayed mode when the HORIZONTAL MODE switch is set to either ALT or CHOP, the operation of the stage is changed from that discussed above. Now, the Display Right Command switches between the HI and LO states at a rate which is one-half the repetition rate of the Display B Command. The resultant CRT display allows the Right Vertical unit to be displayed first against the A Sweep (delaying) and then against the B Sweep (delayed). Then the display switches to the Right Vertical unit and it is displayed consecutively against the A and B Sweeps in the same manner. The input conditions for this mode of operation are:

Pin 4 LO—A Time-Base unit set for delayed operation.

Pin 8 LO—Display B Command generated by Horizontal Binary stage goes negative.

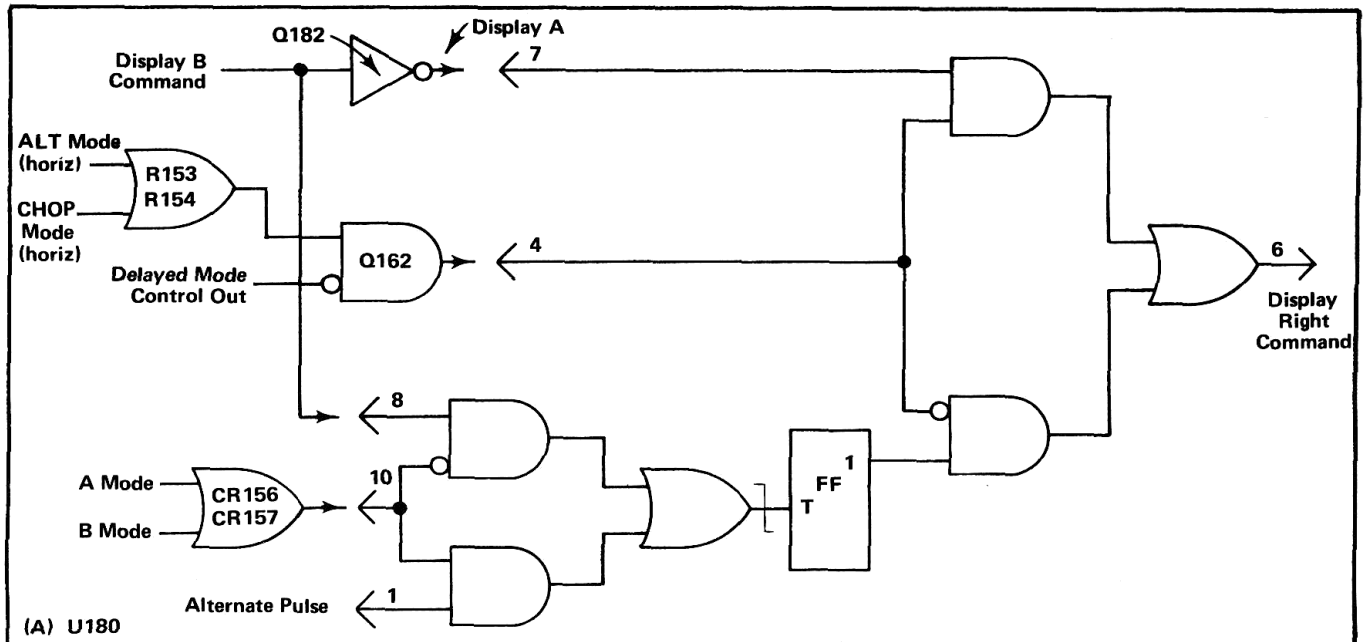
Pin 10 LO—HORIZONTAL MODE switch set to any position except A or B.

A logic diagram of the Vertical Binary stage is shown in Fig. 3-12A. Several Logic functions in this stage are performed by logic devices made up of discrete components. The components that make up these logic devices are identified on the logic diagram. An input/output table for the Vertical Binary stage is given in Fig. 3-12B.

Plug-In Binary

The Plug-In Binary stage produces the Display Channel 2 Command to provide a Plug-In Alternate Command to dual-trace vertical units. Fig. 3-13 identifies the function of the input pins for the Plug-In Binary stage. This stage uses the same type of integrated circuit as the Horizontal Binary and Vertical Binary stages.

When the Display Channel 2 Command level is HI and the vertical plug-ins are set for alternate operation, Channel 2 of the dual-trace unit is displayed. When it is LO, Channel 1 is displayed. The repetition rate of the Display Channel 2 Command is determined by the setting of the VERTICAL MODE switch. For all positions except ALT, the Display Channel 2 Command is the same as the Display Right Command from the Vertical Binary stage. Since the Display Right Command was derived directly from the Display B Command, this allows the two channels of a dual-trace vertical unit to be slaved to the time-base units (non-delayed, dual-sweep horizontal modes only) in the same manner



(B)

Input						Output
Alternate Pulse 1	ALT or CHOP Mode (horiz) and not Delayed Mode 4	Display A 7	Display B Command 8	A or B Mode 10	Display Right Command 6	Horizontal Mode
LO[1]	LO	Φ	Φ	HI	n+1[2]	A or B
Φ	HI	HI	LO	LO	HI	Display Right — ALT or CHOP, Non-delayed Mode (Sweep-slaving)
Φ	HI	LO	HI	LO	LO	Display Left — ALT or CHOP, Non-delayed Mode (Sweep-slaving)
Φ	LO	Φ	LO[1]	LO	n+1[3]	ALT or CHOP, Delayed Mode

Φ = Has no effect in this case.

n+1 = If output is LO prior to LO[1] it goes HI, and vice versa.

[1] Actuated by negative-going edge.

[2] Repetition rate one-half Alternate Pulse rate.

[3] Repetition rate one-half Display B rate.

Fig. 3-12. (A) Logic diagram for Vertical Binary stage, (B) Table of input/output combinations for the Vertical Binary stage.

as previously described for slaving between the vertical and time-base units. The resultant CRT presentation when the dual-trace unit is set for alternate operation displays the Channel 1 trace at the sweep rate of the B Time-Base unit and the Channel 2 trace at the sweep rate of the A Time-Base unit. Input conditions for a LO output level so that Channel 1 of the vertical plug-in can be displayed at the B Sweep rate are:

Pin 4 HI—VERTICAL MODE switch set to any position except ALT.

Pin 7 LO—B Sweep to be displayed (Display Right and Display B Command HI).

The input conditions to provide a HI output level so that Channel 2 of the plug-in can be displayed at the A Sweep rate are:

Pin 4 HI—VERTICAL MODE switch set to any position except ALT.

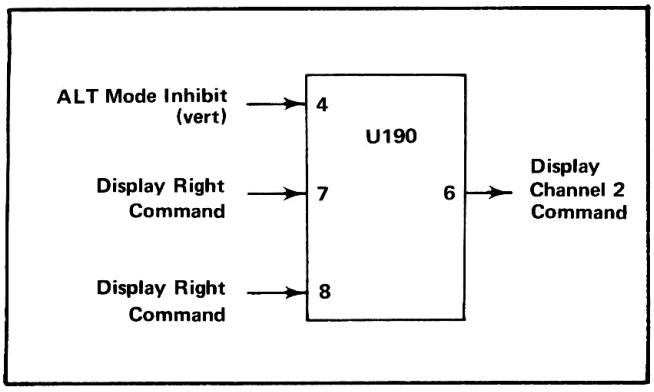
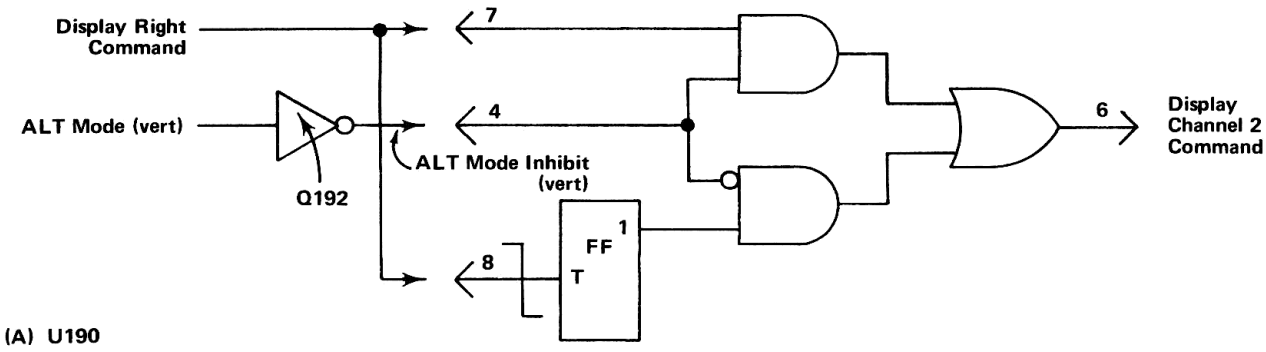


Fig. 3-13. Input and output pins for Plug-In Binary stage.

Pin 7 HI—A Sweep to be displayed (Display Right and Display B Command LO).

The Display Channel 2 Command switches from HI to LO as the Display B Command from the Horizontal Binary stage switches from LO to HI, and vice versa.

When the VERTICAL MODE switch is set to ALT, the Display Right Command from the Vertical Binary stage switches the vertical display between the two vertical units. However, if either or both of the vertical plug-in units are dual-trace units, they can be operated in the alternate mode also. To provide a switching command to these units, the Plug-In Binary stage produces an output signal with a repetition rate one-half the repetition rate of the Display Right Command. The sequence of operation when two dual-trace vertical units are installed in the vertical plug-in compartments and they are both set for alternate operation, is as follows (VERTICAL MODE and HORIZONTAL MODE switches set to ALT): 1. Channel 1 of Left Vertical unit at sweep rate of B Time-Base unit, 2. Channel 1 or



(A) U190

Input			Output	
ALT Mode Inhibit (vert) 4	Display Right Command 7	Display Right Command 8	Display Channel 2 Command 6	Comments
LO	Φ	LO[1]	n+1[2]	ALT Vertical Mode
HI	LO	Φ	LO	Channel 1 displayed — All vertical modes except ALT, provides sweep-slaving for non-delayed dual-sweep operation.
HI	HI	Φ	HI	Channel 2 displayed

Φ = Has no effect in this case.

n+1 = If output is LO prior to LO[1] it goes HI, and vice versa.

[1] Actuated by negative-going edge.

(B) [2] Repetition rate one-half Display Right Command rate.

Fig. 3-14. (A) Logic diagram for Plug-In Binary stage, (B) Table of input/output combinations for the Plug-In Binary stage.

Right Vertical unit at sweep rate of A Time-Base unit, 3. Channel 2 of Left Vertical unit at sweep rate of B Time-Base unit, 4. Channel 2 of Right Vertical unit at sweep rate of A Time-Base unit. Notice that under these conditions, both channels of the Left Vertical unit are displayed at the B Sweep rate and that both channels of the Right Vertical unit are displayed at the A Sweep rate. The repetition rate at the output of this stage is one-half the Display Right Command rate. Input conditions when the VERTICAL MODE switch is set to ALT are:

Pin 4 LO—VERTICAL MODE switch set to ALT.

Pin 8 LO—Display Right Command generated by Vertical Binary stage goes negative.

Fig. 3-14A shows a logic diagram of the Plug-In Binary stage. An input/output table for this stage is given in Fig. 3-14B.

Clock Generator

One half of integrated circuit U120 along with the external components shown in Fig. 3-15A make up the Clock Generator stage. R1, Q1, Q2 and Q3 represent an equivalent circuit which is contained within U120A. This circuit along with discrete components C117-R116-R117-R118 comprise a two-megahertz free-running oscillator to provide a timing signal (clock) for vertical, horizontal, and plug-in chopping.

The stage operates as follows: Assume that Q2 is conducting and Q1 is off. The collector current of Q2 produces a voltage drop across R1 which holds Q1 off. This negative level at the collector of Q2 is also connected to pin 14 through Q3 (see waveforms in Fig. 3-15B at time T_0). Since there is no current through Q1, C117 begins to charge towards −15 volts through R116-R117. The emitter of Q1 goes negative as C117 charges until it reaches a level about 0.6 volts more negative than the level at its base. Then, Q1 is forward biased and its emitter rapidly rises positive (see time T_1 on waveforms). Since C117 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q1 pulls the emitter of Q2 positive also, to reverse-bias it. With Q2 reverse biased, its collector rises positive to produce a positive output level at pin 14.

Now, conditions are reversed. Since Q2 is reverse biased, there is no current through it. Therefore, C117 can begin to discharge through R118. The emitter level of Q2 follows the discharge of C117 until it reaches a level about 0.6 volt

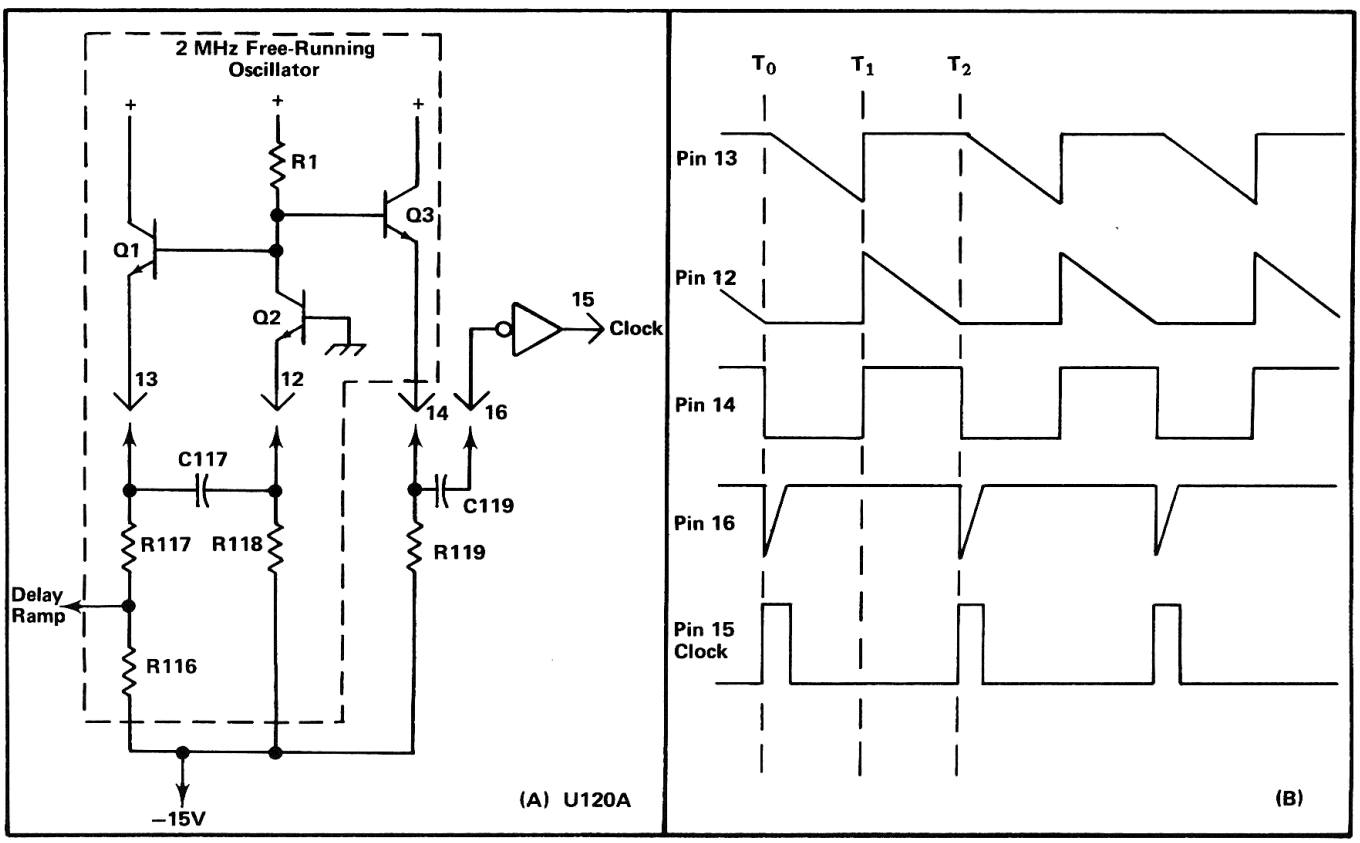


Fig. 3-15. (A) Diagram of Clock Generator stage, (B) Idealized waveforms for Clock Generator stage.

more negative than its base. Then, Q2 is forward biased and its collector drops negative to reverse-bias Q1. The level at pin 14 drops negative also, to complete the cycle. Once again, C117 begins to charge through R116-R117 to start the second cycle.

Two outputs are provided from this oscillator. The Delay Ramp signal from the junction of R116-R117 is connected to the Vertical Chopped Blanking stage. This signal has the same waveshape as shown by the waveform at pin 13 with its slope determined by the divider ratio between R116-R117. A square-wave output is provided at pin 14. The frequency of this square wave is determined by the overall RC relationship between C117-R116-R117-R118, and its duty cycle is determined by the ratio of R116-R117 to R118.

The square wave at pin 14 is connected to pin 16 through C119. C119, along with the internal resistance of U120A, differentiates the square wave at pin 14 to produce a negative-going pulse coincident with the falling edge of the square wave (positive-going pulse coincident with rising edge has no effect on circuit operation). This negative-going pulse is connected to pin 15 through an inverter-shaper which is also part of U120A. The output at pin 15 is a positive-going Clock pulse at a repetition rate of about two megahertz.

Vertical Chopped Blanking

The Vertical Chopped Blanking stage is made up of the remaining half of integrated circuit U120. This stage determines if Vertical Chopped Blanking pulses are required based upon the operating mode of the vertical system or the plug-in units (dual-trace units only). Vertical Chopped Blanking pulses are produced if: 1. VERTICAL MODE switch is set to CHOP; 2. Dual-trace vertical unit is operating in the chopped mode and that unit is being displayed; 3. Dual-trace vertical unit operating in the chopped mode with the VERTICAL MODE switch set to ADD. The repetition rate of the negative-going Vertical Chopped Blanking pulse output at pin 4 is always two megahertz as determined by the Clock Generator stage.

The Delay Ramp signal from the Clock Generator stage determines the repetition rate and pulse width of the Vertical Chopped Blanking pulses. The Delay Ramp applied to pin 10 starts to go negative from a level of about +1.1 volts coincident with the leading edge of the Clock pulse (see waveforms in Fig. 3-16B). This results in a HI quiescent condition for the Vertical Chopped Blanking pulse. The slope of the negative-going Delay Ramp is determined by the Clock Generator stage. As it reaches a level slightly negative from ground, the Vertical Chopped Blanking pulse output level changes to the LO state. This signal remains LO until the Delay Ramp goes HI again. Notice the delay between the leading edge of the Clock pulse generated by U120A and the leading edge of the Vertical Chopped Blanking pulses (see Fig. 3-16B). The amount of delay between the leading edges of these pulses is determined by the slope of the Delay Ramp applied to pin 10. This delay is necessary due to the delay line in the vertical deflection system. Otherwise, the trace blanking resulting from the Vertical Chopped Blanking pulse would not coincide with the switching between the displayed traces. The duty cycle of the square wave produced in the Clock Generator stage determines the pulse width of the Vertical Chopped Blanking pulses (see Clock Generator discussion for more information).

Whenever this instrument is turned on, Vertical Chopped Blanking pulses are being produced at a two-megahertz rate. However, these pulses are available as an output at pin 4 only when the remaining inputs to U120B are at the correct

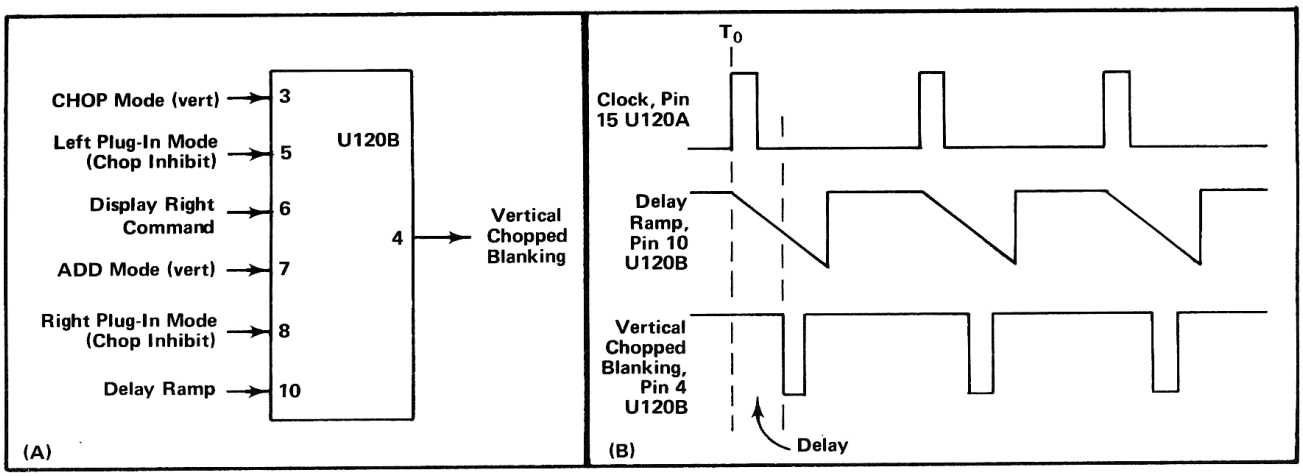


Fig. 3-16. (A) Input and output pins for Vertical Chopped Blanking stage, (B) Idealized waveforms for Vertical Chopped Blanking stage.

levels. The following discussions give the operating conditions which produce Vertical Chopped Blanking pulses to blank the CRT during vertical chopping. Fig. 3-16A identifies the function of the pins of U120B.

1. CHOP VERTICAL MODE

When the VERTICAL MODE switch is set to CHOP, Vertical Chopped Blanking pulses are available at pin 4 at all times. The input conditions necessary are:

Pin 3 HI—VERTICAL MODE switch set to CHOP.

Pin 7 LO—VERTICAL MODE switch set to any position except ADD.

Pin 10 LO—Delay Ramp more negative than about zero volts.

2. LEFT VERTICAL UNIT SET FOR CHOPPED MODE

If the Left Vertical unit is set for chopped operation, the setting of the VERTICAL MODE switch determines whether Vertical Chopped Blanking pulses are available. If the VERTICAL MODE switch is set to the CHOP position, conditions are as described in #1 above. Operation in the ADD position of the VERTICAL MODE switch is given later. For the LEFT position of the VERTICAL MODE switch or when the Left Vertical unit is to be displayed in the ALT mode, Vertical Chopped Blanking pulses are available at all times (two-megahertz rate). The input conditions are:

Pin 3 LO—VERTICAL MODE switch set to any position except CHOP.

Pin 5 LO—Left Vertical unit set to chopped mode.

Pin 6 LO—Left Vertical unit to be displayed (Display Right Command LO).

Pin 7 LO—VERTICAL MODE switch set to any position except ADD.

Pin 10 LO—Delay Ramp more negative than about zero volts.

Notice that the Display Right Command at pin 6 must be LO for output pulses to be available at pin 4. This means that when the VERTICAL MODE switch is set to ALT, Vertical Chopped Blanking pulses will be produced only during the time that the Left Vertical unit is to be displayed (unless Right Vertical unit is also set for chopped operation).

3. RIGHT VERTICAL UNIT SET FOR CHOPPED OPERATION

If the Right Vertical unit is set for the chopped mode, operation is the same as described above for the Left Vertical unit except that Vertical Chopped Blanking pulses are produced when the VERTICAL MODE switch is set to RIGHT or when the Display Right Command is HI in the ALT mode. The input conditions are:

Pin 3 LO—VERTICAL MODE switch set to any position except CHOP.

Pin 6 HI—Right Vertical unit to be displayed (Display Right Command HI).

Pin 7 LO—VERTICAL MODE switch set to any position except ADD.

Pin 8 LO—Right Vertical unit set to chopped mode.

Pin 10 LO—Delay Ramp more negative than about zero volts.

4. ADD VERTICAL MODE

When the VERTICAL MODE switch is in the ADD position and either or both of the vertical units are operating in the chopped mode, Vertical Chopped Blanking pulses must be available to block out the transition between the traces of the vertical units. The input conditions are:

Pin 3 LO—VERTICAL MODE switch set to any position except CHOP.

Pin 5 LO—Left Vertical unit set to chopped mode (can be HI if pin 8 is LO).

Pin 7 HI—VERTICAL MODE switch set to ADD.

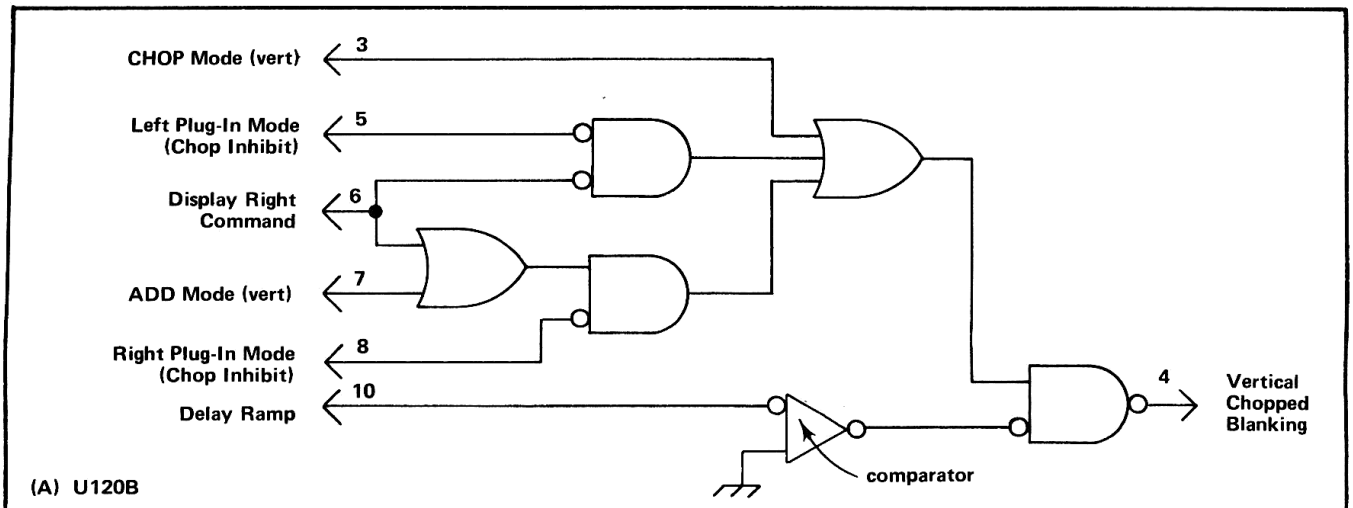
Pin 8 LO—Right Vertical unit set to chopped mode (can be HI if pin 5 is LO).

Pin 10 LO—Delay Ramp more negative than about zero volts.

Fig. 3-17A shows a logic diagram of the Vertical Chopped Blanking stage. Notice the comparator block on this diagram (one input connected to pin 10). The output of this comparator is determined by the relationship between the levels at its inputs. If pin 10 is more positive (HI) than the grounded input, the output is HI also; if it is more negative (LO), the output is LO. An input/output table for this stage is given in Fig. 3-17B.

Chop Counter

The Chop Counter stage produces the Vertical Chopping Signal, the Plug-In Chop Command and the Horizontal Chopped Blanking signal. The Clock pulse produced by the Clock Generator stage provides the timing signal for this stage. The function of the input and output pins for the Chop Counter stage are identified in Fig. 3-18A. Idealized waveforms showing the timing relationship between the input and output signals for this stage are shown in Fig. 3-18B.



(A) U120B

(B)

Input						Output	
CHOP Mode (vert) 3	Left Plug-In Mode (Chop Inhibit) 5	Display Right Command 6	Add Mode (vert) 7	Right Plug-In Mode (Chop Inhibit) 8	Delay Ramp 10[1]	Vertical Chopped Blanking 4[2]	Conditions
HI	Φ	Φ	LO	Φ	LO	LO	CHOP Mode (vert)
LO	LO	LO	LO	Φ	LO	LO	Left Plug-in Chopped
LO	Φ	HI	LO	LO	LO	LO	Right Plug-in Chopped
LO	LO[3]	Φ	HI	LO[3]	LO	LO	ADD Mode, Left or Right Plug-in Chopped
All other combinations						HI	No Vertical Chopped Blanking pulses at output.

Φ = Has no effect in this case.

[1] Ramp signal; considered LO when more negative than about zero volts.

[2] Negative-going pulse at two megahertz rate.

[3] Pin 5 can be HI and not affect operation if pin 8 is LO, and vice versa.

Fig. 3-17. (A) Logic diagram for Vertical Chopped Blanking stage, (B) Table of input/output combinations for Vertical Chopped Blanking stage.

The repetition rate of the output signals from this stage is determined by the setting of the HORIZONTAL MODE switch. When the HORIZONTAL MODE switch is set to any position except CHOP, the repetition rate of the Vertical Chopping Signal output at pin 1 is one megahertz (one-half Clock rate). This determines the switching between the Left and Right Vertical units when the VERTICAL MODE switch is set to CHOP. At the same time, the repetition rate of the Plug-In Chop Command at pin 8 is 0.5 megahertz (one-fourth Clock rate). This provides a chopping signal to dual-trace vertical units to provide switching between the two channels. The relationship between these output signals and the Clock input is shown by the waveforms in Fig. 3-18B in the area between T_0 and T_1. During this time, the level at pin 4 remains HI.

When the HORIZONTAL MODE switch is set to CHOP, the basic repetition rate of the Vertical Chopping Signal and the Plug-In Chop Command is altered. For example, if the HORIZONTAL MODE switch is changed to the CHOP position at time T_1 (see Fig. 3-18B), a HI level is applied to

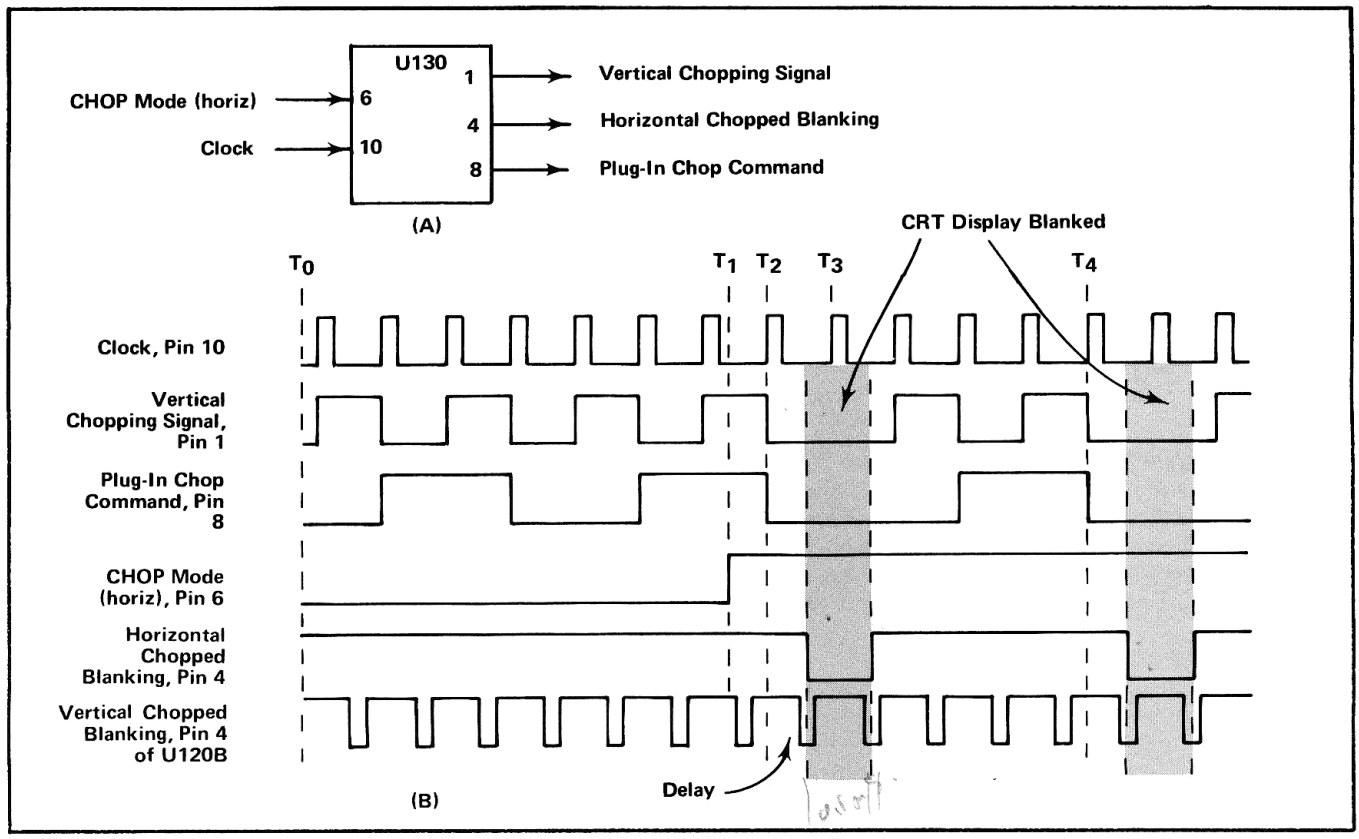


Fig. 3-18. (A) Input and output pins for Chop Counter stage, (B) Idealized waveforms for Chop Counter stage.

pin 6. This stage continues to produce outputs at pins 1 and 8 in the normal manner until both outputs are at their HI level (see time T_2; this condition only occurs once every fifth Clock pulse when the HORIZONTAL MODE switch is set to CHOP). When both of these outputs are at their HI level, the next Clock pulse switches both outputs LO and at the same time switches the Horizontal Chopped Blanking to the LO level. However, this change does not appear at pin 4 immediately due to a delay network in the circuit. The delay is necessary so the Horizontal Chopped Blanking coincides with the Vertical Chopped Blanking produced by U120A (compare bottom two waveforms of Fig. 3-18B; also see Vertical Chopped Blanking for further information). After the delay time, the output level at pin 4 goes LO where it remains for about 0.5 microsecond which is equal to the period of the Clock pulse (two megahertz repetition rate). The Horizontal Chopped Blanking time must be longer than the Vertical Chopped Blanking time since it takes more time for the display to switch between horizontal units than between vertical units. During the time that the level at pin 4 is LO, the CRT is blanked and the Vertical Chopped Signal and the Plug-in Chop Command cannot change levels. The Clock pulse at T_3 changes only the Horizontal Chopped Blanking output at pin 4. The level on this pin goes HI after the delay time to unblank the CRT.

For the next three trigger pulses, the Vertical Chopping Signal output and Plug-In Chop Command operate in the normal manner. However, just prior to the fourth clock pulse (time T_4) both outputs are again at their HI level. The fourth Clock pulse at T_4 switches the output at pin 1, pin 8, and pin 4 (after delay) to the LO level to start the next cycle. Notice that a Horizontal Chopped Blanking pulse is produced at pin 4 with every fifth Clock pulse. Also notice that with the HORIZONTAL MODE switch set to CHOP, two complete cycles of the Vertical Chopping Signal are produced with each five Clock pulses (repetition rate two-fifths Clock rate) and one complete cycle of the Plug-In Chop Command for every five Clock pulses (one-fifth Clock rate). Notice that the shaded area during the Horizontal Chopped Blanking pulse (see Fig. 3-18B) is not part of the display time (CRT display blanked). However, about the same time segment is displayed from the vertical signal source with or without Horizontal Chopped Blanking due to the change in repetition rate when in the CHOP horizontal mode.

The Vertical Chopping Signal at pin 1 of U130 is connected to the Vertical Mode Logic stage (see following description) through L138-R138. This signal is HI when the

Right Vertical unit is to be displayed and it is LO when the Left Vertical unit is to be displayed. The Plug-In Chop Command at pin 8 is connected to the plug-in units in the vertical compartments through L136-R136 via the Main Interface board. When this signal is HI, Channel 2 of the plug-in units can be displayed and when this level is LO, Channel 1 can be displayed. The Horizontal Chopped Blanking signal at pin 4 is connected through LR134 to the Horizontal Binary stage U150, and to the Z-Axis Logic stage U170 by way of Q146. When this signal is HI, the CRT is unblanked to display the selected signal. When it is LO, the CRT is blanked to allow switching between the time-base units.

A logic diagram of the Chop Counter stage is shown in Fig. 3-19. Details of operation for the flip flops (FF) are shown in Table 3-1 at the front of this section. Use the waveforms given in Fig. 3-18B along with this diagram.

Vertical Mode Logic

The Vertical Mode Logic stage made up of discrete components CR128-CR139, CR183-CR184, and Q194-Q196. These components develop the Vertical Mode Command which is connected to the Main Interface circuit (vertical plug-in compartments and trigger selection circuitry) and the Vertical Interface circuit to indicate which vertical unit is to be displayed. When this output level is HI, the Right Vertical unit is displayed and when it is LO, the Left Vertical unit is displayed.

The VERTICAL MODE switch located on diagram 12 provides control levels to this stage. This switch provides a HI level on only one of five output lines to indicate the selected vertical mode; the remaining lines are LO (notice that only four of the lines from the VERTICAL MODE switch are used on this schematic). Operation of this stage is as follows:

When the VERTICAL MODE switch is set to RIGHT, a HI level is connected to the base of Q194 through R127. This forward biases Q194 and the positive-going level at its emitter is connected to the emitter of Q196. The collector of Q196 goes HI to indicate that the Right Vertical unit is to be displayed. For the CHOP position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR128-CR139 through R128. Both diodes are forward biased so that the Vertical Chopping Signal from pin 1 of U130 can pass to the base of Q194. This signal switches between the HI and LO levels at a one-megahertz rate and it produces a corresponding Vertical Mode Command output at the collector of Q196. When the output is HI, the Right Vertical unit is displayed and when it switches to LO, the Left Vertical unit is displayed.

In the ALT position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR183-CR184 through R183. These diodes are forward biased so the Display Right Command from pin 6 of the Vertical Binary stage can pass to the base of Q194 to determine the Vertical Mode Command level. The Display Right Command switches between its HI and LO levels at a rate determined by the Vertical Binary stage.

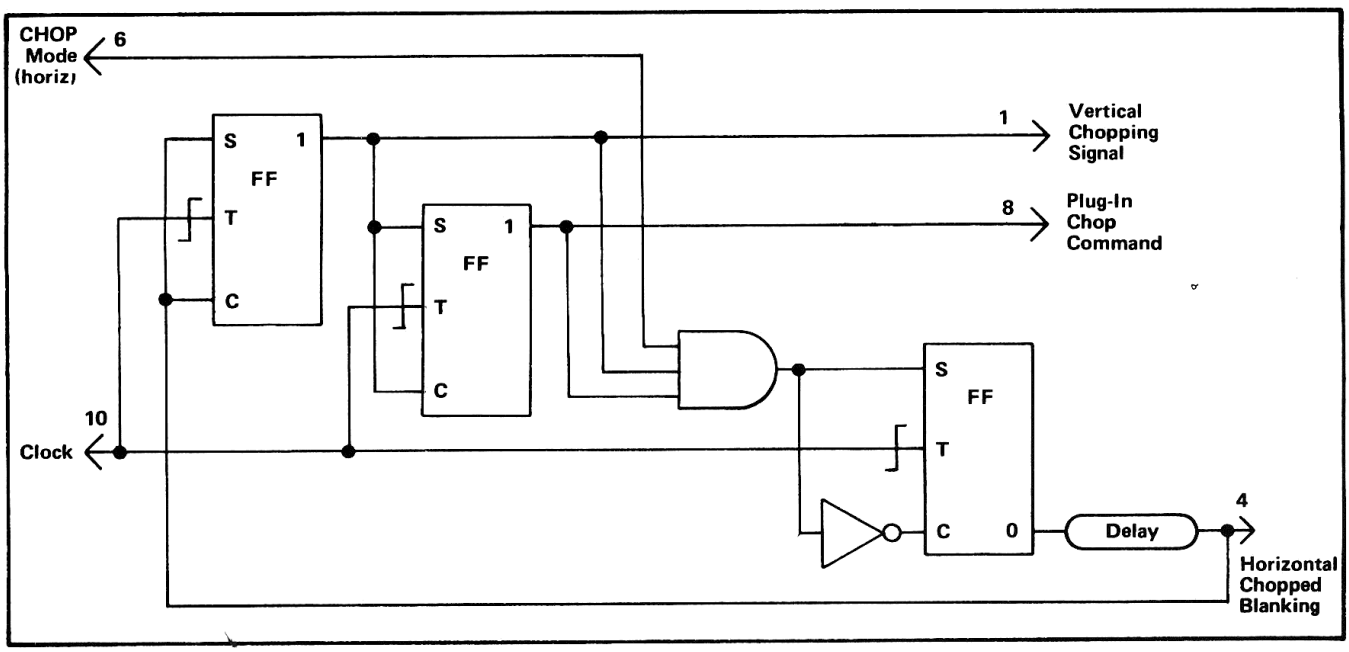


Fig. 3-19. Logic diagram of Chop Counter stage.

The control levels in the LEFT and ADD positions of the VERTICAL MODE switch are not connected to this stage. However, since only the selected line from the VERTICAL MODE switch can be HI, the RIGHT, CHOP and ALT lines must remain at their LO level when either LEFT or ADD are selected. Therefore, the base of Q194 remains LO to produce a LO Vertical Mode Control output level at the collector of Q196.

A logic diagram of the Vertical Mode Logic stage is shown in Fig. 3-20. The discrete components which make up each logic function are identified.

TRIGGER SELECTOR

General

The Trigger Selector circuit determines the trigger signal which is connected to the A and B Time-Base units as controlled by the A TRIGGER SOURCE and B TRIGGER SOURCE switches. This circuit also provides the drive signal for the Vertical Signal Amplifier circuit as controlled by the B TRIGGER SOURCE switch. Fig. 3-21 shows a detailed block diagram of the Trigger Selector circuit along with a simplified diagram of all the circuitry involved in selection of the trigger source. A schematic of the Trigger Selector circuit is shown on diagram 3 at the rear of this manual. Also see diagrams 1 and 12 for the trigger selection circuitry not shown on diagram 3.

Trigger Mode and ADD Signals

General. The circuitry shown on the left side of the simplified diagram in Fig. 3-21 determines the operation of the A and B Trigger Channel Switch stages. The A TRIGGER SOURCE switch S1011 controls the A Trigger Channel Switch U304 through Q24; the B TRIGGER SOURCE switch S1001 controls the B Trigger Channel Switch U324 through Q28. When the front-panel A or B TRIGGER SOURCE switches are set to the VERT MODE positions, the setting of the VERTICAL MODE switch determines the trigger selection. In the LEFT VERT or RIGHT VERT positions, the trigger signal is obtained from the indicated vertical unit. The following discussions give detailed operation in each position of the A and B TRIGGER SOURCE switches. It is written assuming that both of these switches are set to the same position. However, the A and B TRIGGER SOURCE switches operate independently to control the operation of the A and B Trigger Channel Switch stages respectively, to select the trigger output signal for the associated time-base unit.

VERT MODE. In the VERT MODE position of either the A or B TRIGGER SOURCE switch, the setting of the VERTICAL MODE switch determines the operation of the A and B Trigger Channel Switch stages (A TRIGGER SOURCE, B TRIGGER SOURCE and VERTICAL MODE switches shown on diagram 12). In the LEFT position of the VERTICAL MODE switch, the bases of Q24 or Q28 (see Main Interface schematic) are connected to ground through the ALT and RIGHT sections of S1021, CR1022 and CR1027, and S1001 or S1011. This holds Q24 or Q28 reverse biased to provide a LO level to pin 4 of U304 and U324 (see Fig. 3-22).

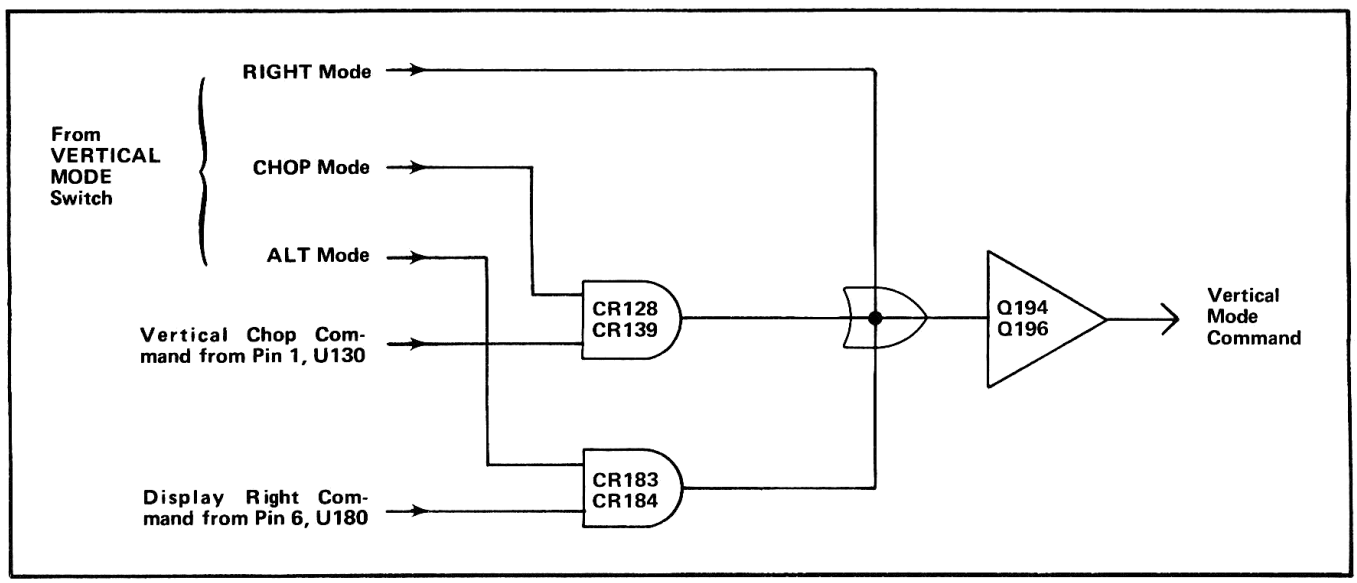


Fig. 3-20. Logic diagram of Vertical Mode Logic stage.

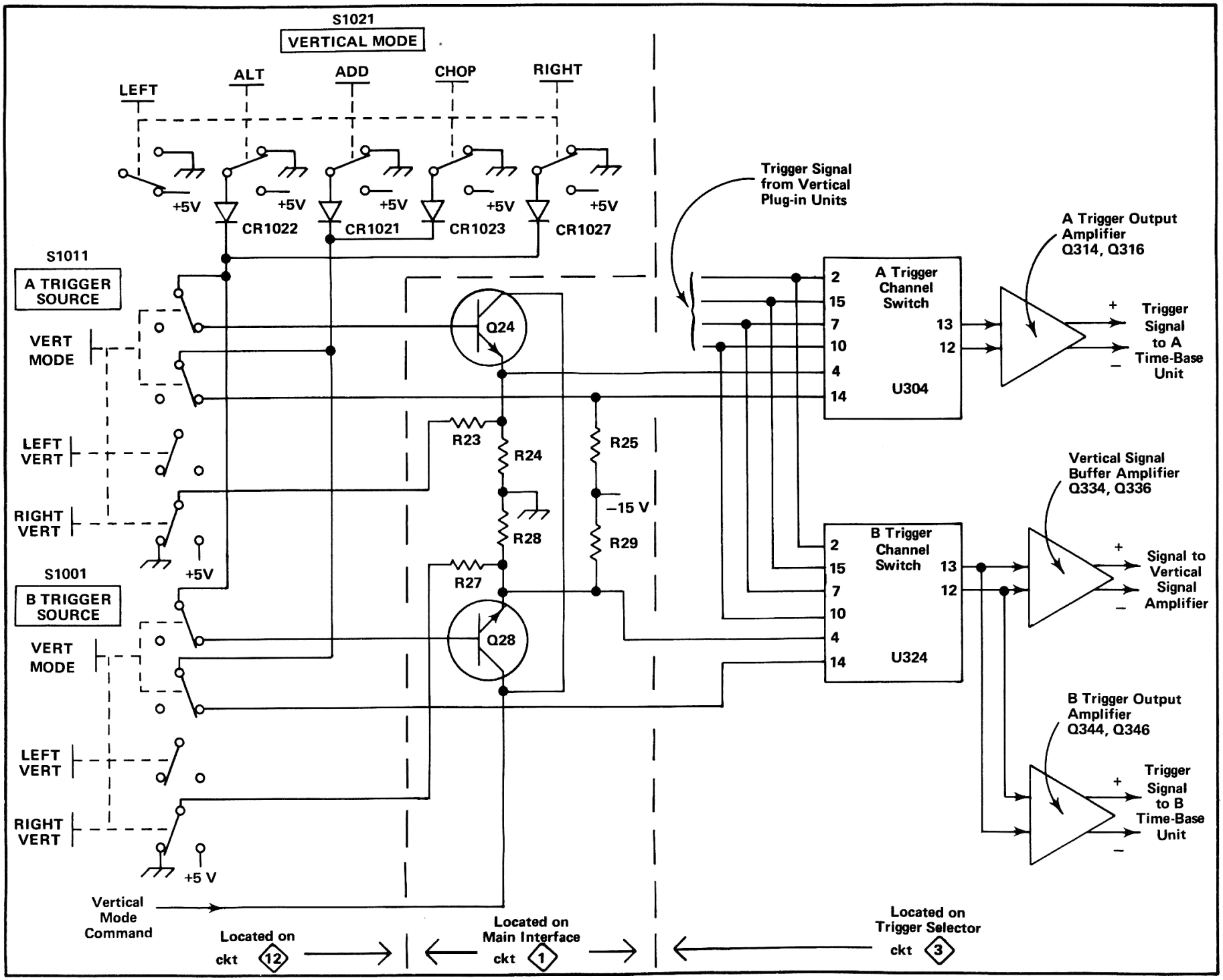
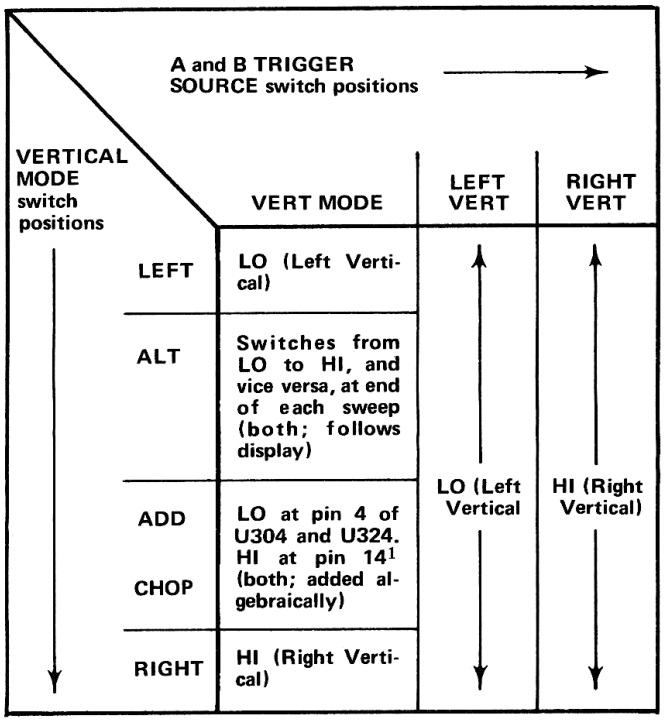


Fig. 3-21. Simplified schematic of trigger selector circuitry.



[1]Pin 14 LO for all other conditions.

Fig. 3-22. Input levels at pin 4 of U304 and U324 (source of triggering signal is shown in parenthesis).

When the VERTICAL MODE switch is set to ALT, +5 volts is applied to the bases of Q24 or Q28 through CR1022 and S1001 or S1011. Q24 and Q28 are forward biased and their emitter level is determined by the Vertical Mode Signal from the Logic Circuit applied to their collectors. This signal switches between the HI level (Right Vertical unit to be displayed) and the LO level (Left Vertical unit to be displayed) at the end of each sweep. When the Vertical Mode Signal is HI, it provides a positive collector voltage to Q24 and Q28. Q24 and Q28 are saturated due to CR1022, and their emitter levels are very near the collector level. This provides a HI output level to the Trigger Channel Switch stages. As the Vertical Mode Signal goes LO, the collector supply for Q24 and Q28 also goes negative. Q24 and Q28 remain saturated and the output again follows the collector level to supply a LO output level to U304 and U324.

For ADD and CHOP vertical mode operation, +5 volts is connected to pin 14 of U304 and U324 through CR1021 or CR1023 and S1001 or S1011. At the same time, the base of Q24 or Q28 is held LO by the ground connection through the ALT and RIGHT sections of S1021 so the level at pin 4 of the Trigger Channel Switches is LO also (produces an ADD mode in Trigger Channel Switches; see description of these circuits which follows). In the RIGHT position of the VERTICAL MODE switch, +5 volts is connected to the bases of Q24 or Q28 through CR1027 and S1001 or S1011 to forward bias these transistors. The Vertical Mode Signal connected to the collectors of Q24 and Q28 is also HI in this mode and a HI output level is produced at the emitters of Q24 or Q28.

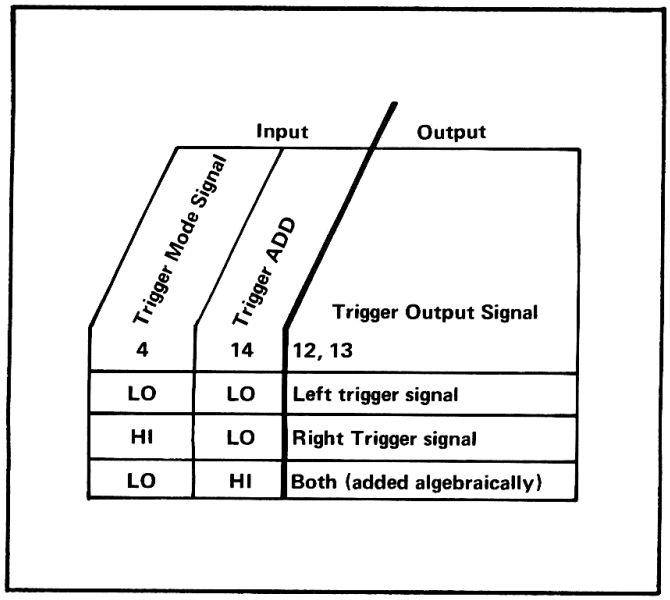
LEFT VERT. When the LEFT VERT trigger source is selected, the VERTICAL MODE switch is disconnected from the trigger selector circuitry. Now, the ground connection through the RIGHT VERT section of S1001 or S1011 establishes a LO output level at the emitters of Q24 and Q28.

RIGHT VERT. In the RIGHT VERT position of the A or B TRIGGER SOURCE switches, +5 volts is connected to the emitters of Q24 and Q28 through S1011-R23 or S1001-R27. This produces a HI output level to the A and B Trigger Channel Switch stages.

A and B Trigger Channel Switch

The A and B Trigger Channel Switch stages determine which input signal provides the trigger signal to the time-base units as controlled by the trigger mode and ADD signals from the trigger selection circuitry. Resistors R301-R321 and R302-R322 establish the input resistance of this stage and provide a load for the trigger output of the Left and Right Vertical plug-in units. Resistors R303-R304-R305 and R307-R308-R309 establish the operating levels for the A Trigger Channel Switch; R303-R305 and R307-R309 set the current gain for each channel. Resistors R323-R324-R325 and R327-R328-R329 establish the operating levels for the B Trigger Channel Switch; R323-R325 and R327-R329 set the current gain for each channel. These stages are made up primarily of integrated circuits U304 and U324. An input/output table for U304 and U324 is shown in Fig. 3-23. U304-U324 provide a high impedance differential input for the trigger signal from the Left Vertical unit at pins 2 and 15 and for the trigger signal from the Right Vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9 and 16 in all modes. This provides a constant DC bias to the stages which follow as the A or B TRIGGER SOURCE switches or the VERTICAL MODE switch are changed.

When the level at pin 4 is LO (see Trigger Mode and ADD Signals discussion and Fig. 3-23), the trigger signal from the Left Vertical unit passes to the output while the trigger signal from the Right Vertical unit is blocked. A HI level at pin 4 connects the trigger signal from the Right Vertical unit to the output and the trigger signal from the Left Vertical unit is blocked. For VERT MODE operation in the ALT position of the VERT MODE switch, the level at pin 4 switches between the LO and HI level at a rate



4	14	12, 13
LO	LO	Left trigger signal
HI	LO	Right Trigger signal
LO	HI	Both (added algebraically)

Fig. 3-23. Input/output table for A and B Trigger Channel Switch stages.

determined by the Vertical Binary stage (see Logic Circuit description). This action obtains the trigger signal from the Left Vertical unit when the Left Vertical unit is being displayed and from the Right Vertical unit when this unit is being displayed.

When the level at pin 4 is LO and the level at pin 14 is HI, the trigger signal from both the Left and Right Vertical unit passes to the output pins. This condition occurs only when the A or B TRIGGER SOURCE switches are set to VERT MODE and the VERTICAL MODE switch is set to either ADD or CHOP. Under this operating mode, the trigger output signal is the algebraic sum of the trigger input signals from the Left and Right Vertical units to prevent triggering on the vertical chopping transition or only on one signal of an added display.

A Trigger Output Amplifier

The trigger output signal at pins 12 and 13 of the A Trigger Channel Switch is connected to the emitters of common-base amplifier Q314-Q316 through R311-R312. These transistors provide a low-resistance load for the A Trigger Channel Switch while providing a high output impedance to the following circuits. The signal at the collectors of Q314 and Q316 is connected to the A Horizontal unit via the Main Interface circuit. The A Horizontal unit provides a 50-ohm differential load for this stage. If it is removed from its compartment, the voltage-swing at the collectors of Q314-Q316 will increase substantially.

Vertical Signal Buffer Amplifier

The trigger output signal at pins 12 and 13 of the B Trigger Channel Switch is connected to the emitters of common-base amplifier Q334-Q336. The output signal at the collectors of Q334 and Q336 is connected to the Vertical Signal Amplifier (see Output Signals and Calibrator description) through R337 and R338. R339 provides a differential output resistance of about 100 ohms.

B Trigger Output Amplifier

The signal at pins 12 and 13 of the B Trigger Channel Switch is also connected to the bases of Q344-Q346 to provide the internal trigger signal for the B Horizontal unit (via the Main Interface circuit). This stage provides isolation between the B Horizontal unit and the Vertical Signal Buffer Amplifier stage. The B Horizontal unit provides a 50-ohm differential load for this stage. If it is removed from its compartment, the collector load for Q344-Q346 changes and the voltage swing at their collectors increases. The action of this stage prevents this change from affecting the Vertical Signal Buffer Amplifier stage. CR342-CR346 clamp the collectors of Q344 and Q346 at about +0.6 volts to prevent these transistors from saturating under this no-load condition.

VERTICAL INTERFACE

General

The Vertical Interface circuit selects the vertical deflection signal from the output of the Left Vertical and/or the Right Vertical plug-in unit. This stage also includes an input from the Readout System to block the vertical signal while readout information is displayed on the CRT. Fig. 3-24 shows a detailed block diagram of the Vertical Interface circuit. A schematic of this circuit is shown on diagram 4 at the rear of this manual.

Vertical Channel Switch

The Vertical Channel Switch determines which input signal provides the vertical signal to the Delay-Line Driver stage as controlled by the Vertical Mode Command from the Logic Circuit. Resistors R201-R202 and R203-R204 establish the input resistance of this stage and provide a load for the Left and Right Vertical units. Resistors R209-R210-R211 and R217-R218-R219 establish the operating levels for this stage. R209-R211 and R217-R219 set the current gain for each channel. C207-R207 and C214-R214 provide frequency compensation.

This stage is made up primarily of integrated circuit U214, which is the same type as used for the Trigger Channel Switches. An input/output table for U214 is

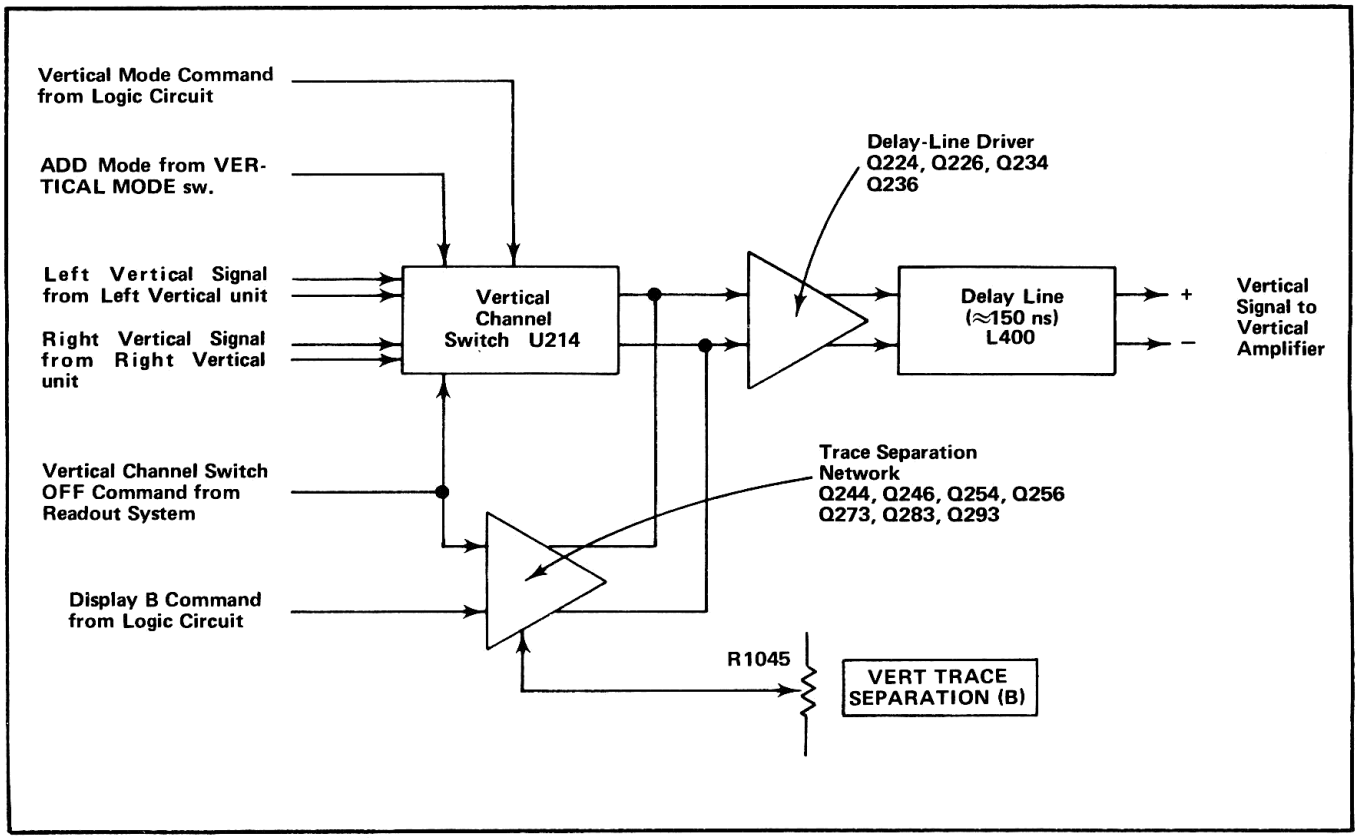


Fig. 3-24. Vertical Interface detailed block diagram.

shown in Fig. 3-25. U214 provides a high-impedance differential input for the signal from the Left Vertical unit at pins 2 and 15 and the signal from the Right Vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal which is connected to the Delay-Line Driver stage through R221-R222. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9 and 16 in all modes. This provides a constant DC bias to the following stage as the VERTICAL MODE switch is changed.

When the VERTICAL MODE switch is set to LEFT, the level at pin 4 is LO. This level allows the signal from the Left Vertical unit to pass to the output while the signal from the Right Vertical unit is blocked. In the RIGHT position of the VERTICAL MODE switch, the level at pin 4 is HI. Now, the signal from the Right Vertical unit is connected to the output while the signal from the Left Vertical unit is blocked.

When the VERTICAL MODE switch is set to either ALT or CHOP, the Vertical Mode Command at pin 4 switches between the LO and HI levels at a rate determined by either the Chop Counter or the Vertical Binary stages (see Logic Circuit description). This action allows the signal from the Left Vertical unit to be displayed when the Vertical Mode Signal is LO and the signal from the Right Vertical unit is displayed when the Vertical Mode Command is HI. When ADD vertical mode operation is selected, a HI level is applied to pin 14 and the level at pin 4 is LO as determined by the

Input			Output
Vertical Mode Command 4	ADD Mode (Vert) 14	Vertical Channel Switch OFF 6	Output signal 12, 13
LO	LO	LO	Left vertical signal
HI	LO	LO	Right vertical signal
LO	HI	LO	Both (added algebraically)
Φ	Φ	HI	Neither (blocked by Readout System)

Φ = Has no effect in this case

Fig. 3-25. Input/output table for Vertical Channel Switch.

Vertical Mode Control stage in the Logic Circuit. This allows both the Right and Left Vertical signals to pass to the output pins. Now, the signal from both vertical units is algebraically added and the resultant signal determines the vertical deflection.

The Vertical Channel Switch OFF signal from the Readout System which is applied to pin 6 has final control over the output signal from this stage. Quiescently, this signal is LO and the signal from the selected vertical unit can pass to output pins 12 and 13. However, when the Readout System is ready to display readout information, the level at pin 6 goes HI. This level blocks the signal from both vertical units so there is no signal output from this stage under this condition.

Trace Separation Network

The Trace Separation Network provides a variable positioning voltage to offset the B Sweep display when operated in either the ALT or CHOP dual-sweep modes (horizontal). The Display B Command from the Logic Circuit controls the conduction of Q244-Q246-Q254-Q256 through Q273 and Q283. When the B Sweep is being displayed (for ALT or CHOP horizontal operation), the Display B Command is HI to forward bias Q273. This provides a constant current, determined by R281, to Q254 and Q256. The amount of current through each of these transistors is determined by the VERT TRACE SEPARATION (B) control, R1045. This control varies the voltage at the base of Q254 through R14 and R257. The level set at the base of Q254 changes the current flow through Q244-Q254, and since Q273 is supplying a constant current, it changes the current through Q246-Q256 also. The output current at the collectors of Q244-Q246 is connected to the emitters of Q224-Q226 in the Delay-Line Driver stage to offset the B Sweep display up to about four divisions from the A Sweep display. This prevents a confusing display when using dual-sweep operation, as the A and B Sweeps would be displayed on top of each other without this feature.

When the Display B Command is LO (A Sweep displayed), Q273 is reverse biased and there is no current through Q254 and Q256. Instead, the current from R281 flows through Q283 to the base circuits of Q244 and Q246 to establish the vertical position of the A Sweep display. Q254 and Q256 are now by-passed so the VERT TRACE SEPARATION (B) control is effectively disconnected while the A Sweep is being displayed.

Two other signals also control the current through this stage. When the HORIZONTAL MODE switch is set to B (only), a HI level is connected to the base of Q283 through R291. This raises the emitter of Q273 positive enough so that it remains reverse biased even though the Display B Command at its base is HI for this mode. The current through R281 bypasses Q254 and Q256 so the VERT TRACE SEPARATION (B) control again has no effect. The Vertical Channel Switch OFF signal from the Readout System is applied to the base of Q293. Q293 is quiescently conducting through R293 and CR293 to hold CR292 reverse biased. When the Readout System is ready to display readout information, the Vertical Channel Switch OFF signal goes HI resulting in a HI level at the anode of CR293. This forward biases CR292 and allows current from R293 to forward bias Q283 and reverse biase Q273. The Trace Separation Network is disabled (as well as the Vertical Channel Switch) so the Readout System has full control of the trace position (see Readout System description for more information).

Delay-Line Driver

Output of the Vertical Channel Switch stage, along with any positioning current from the Trace Separation Network, is connected to the emitters of Q224-Q226. These transistors are connected as common-base amplifiers to provide a low-impedance current-summing point. The signal at the collectors of Q224-Q226 is connected to the bases of Q234-Q236 through R224 and R225. When the trace is at center screen, diodes CR233-CR234 in the emitter circuits of Q234-Q236 are slightly forward biased by the positive voltage applied to their anodes through R228. As the emitter of either Q234 or Q236 goes positive due to the applied signal at their bases, the corresponding diode is reverse biased and its internal resistance increases. This change in resistance produces a decrease in the gain of this stage for large signals, which compensates for the inherent expansion characteristic of the CRT. Output signal from the Delay-Line Driver stage is connected to the Delay Line through T236. This transformer prevents high-frequency common-mode oscillation of Q234-Q236. R236 provides the reverse termination for the Delay Line.

Delay Line

The Delay Line L400 provides approximately 150 nanoseconds delay for the vertical signal to allow the horizontal circuits time to initiate a sweep before the vertical signal reaches the vertical deflection plates of the CRT. This allows the instrument to display the leading edge of the signal originating the trigger pulse when using internal triggering. The delay line used in this instrument has a characteristic impedance of about 50 ohms per side or about 100 ohms differentially. It is of the coaxial type which does not produce preshoot or phase distortion in the CRT display.

VERTICAL AMPLIFIER

General

The Vertical Amplifier circuit provides the final amplification for the vertical signal before it is applied to the vertical deflection plates of the CRT. This circuit includes an input to produce the vertical portion of a readout display. The BEAM FINDER switch limits the dynamic range of this circuit to compress an over-scanned display within the viewing area of the CRT. Fig. 3-26 shows a detailed block diagram of the Vertical Amplifier circuit. A schematic of this circuit is shown on diagram 5 at the rear of this manual.

Buffer Amplifier

The Buffer Amplifier stage, Q404-Q406, provides a low input impedance for the Vertical Amplifier circuit to permit accurate Delay Line termination. C401-R401, C407-R407 and C400, along with the input resistance of this stage, provide the forward termination for the Delay Line. Collector current for the Delay-Line Driver stage in the Vertical Interface circuit is provided from this stage. The Centering adjustment R405 balances the quiescent DC levels in the Vertical Amplifier circuit so the trace is displayed at the center of the CRT when the inputs to this stage are at the same potential. R406 adjusts the thermal balance of the Vertical Amplifier circuit by varying the emitter current of Q404-Q406. The output signal from the Buffer Amplifier stage is connected to the First Push-Pull Amplifier stage through C411-R411 and C412-R412.

First Push-Pull Amplifier

Q424-Q444 and Q426-Q446 are connected as a push-pull cascode amplifier stage. The Vertical Gain adjustment R415 sets the resistance between the bases of Q424 and Q426 to control the current gain of Q424-Q444. This adjustment sets the overall gain of the vertical deflection system. Thermistors RT423-RT424 and varactors CR431-CR432 provide high-frequency temperature compensation for the Vertical Amplifier circuit. As the internal temperature of the instrument rises, the resistance of RT423-RT424 decreases to reduce the reverse bias on CR431-CR432. This increases the capacitance of varactors CR431-CR432 to change the emitter compensation of Q424-Q426 to maintain high-frequency response at high temperatures. The network C434-C435-C436-C437-C439-R434-R435-R436-R437-R439 provide high-frequency compensation. C435-R435 in this network are adjustable to provide high-frequency delay-line compensation. C434-R434 provide high-frequency response adjustment for this stage. The output signals at the collectors of Q424-Q426 are connected to the common-base transistors Q444-Q446 through C428-R428-R441 and C429-R429-R442. The low input re-

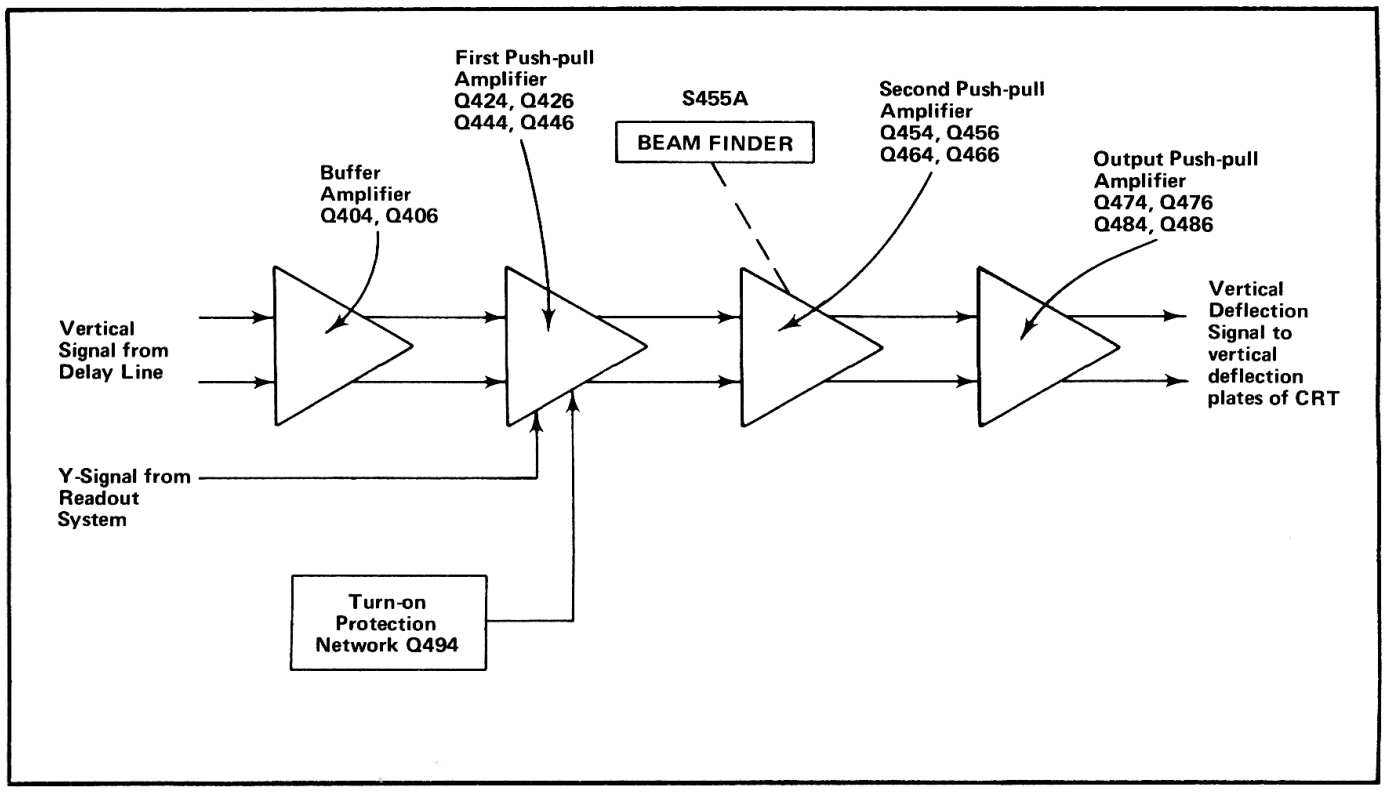


Fig. 3-26. Vertical Amplifier detailed block diagram.

sistance of the Q444-Q446 common-base transistors allows this stage to provide maximum high-frequency performance.

Q494 and its associated components provide a positioning voltage to deflect the CRT beam upward, off the display area when the instrument is turned on to protect the CRT phosphor from damage due to a high-intensity spot on the display area. When this instrument is turned off, C491 quickly discharges through CR491. Then, when the instrument is turned back on, C491 begins to charge toward −15 volts through R491 since CR491 is reverse biased. While C491 is charging, Q494 is forward biased, and it conducts current away from Q446 through CR493. This current-shunting deflects the display off the viewing area vertically until the high-voltage circuits reach their full operating capabilities. As C491 continues to charge, the collector level of Q494 rises positive until CR493 is reverse biased, which disconnects the Turn-on Protection Network from the Emitter circuit of Q446.

For readout displays, the Y-signal from the Readout System is connected to the emitter of Q446 through R494. Since the signal from the vertical units is blocked in the Vertical Channel Switch under this condition (see Vertical Interface discussion), the readout signal provides the only vertical deflection. Although this signal is connected to the emitter of Q446 as a single-ended signal, it is converted to a push-pull signal by the cross-coupling networks in the following stages.

Second Push-Pull Amplifier

The Second Push-Pull Amplifier, Q454-Q464 and Q456-Q466, operates in the same manner as the previous stage. The main difference between the stages is the compensation networks and the BEAM FINDER switch located in this circuit. L447-R446 in the base circuit and C450 in the emitter circuit of Q454-Q456 provide high-frequency compensation for the Vertical Amplifier circuit.

Normally, the emitter current for Q454-Q456 is supplied through parallel paths; S455A-L454-C454 and R454. When S455A is pressed in, the current source through L454 is interrupted and the only emitter-current source for Q454-Q456 is through R454. This limits the dynamic range of this stage by limiting its current, so the display is compressed vertically within the graticule area. At the same time, −15 volts is connected to the emitters of Q464-Q466 through R461-R462 to maintain the same DC currents in the following stages as when the Beam Finder switch is in the normal position. The BEAM FINDER switch can also be pulled out to lock it in the "find" position to aid in locating the traces of several plug-in units.

Output Push-pull Amplifier

The collector signals from Q464-Q466 are connected to the bases of Q474-Q476 in the Output Push-pull Amplifier through L474-L476. These inductors provide series peaking for the very high-frequency components of the vertical signal. Q474-Q484 and Q476-Q486 operate in the same manner as the previous stages. The output signals at the collectors of Q484-Q486 provide the vertical deflection signal for the CRT. RC networks C484-R484 and C486-R486 in the base circuits of Q484-Q486 and LR networks LR486-LR487 prevent oscillation of the output transistors. Diode CR485 provides protection for the output transistors by disconnecting the base circuit of Q484-Q486 from the +15-volt supply if it is shorted to ground or to a negative supply. R475-R477 also provide protection for these transistors by providing a small current source to the emitters of Q484-Q486 to prevent them from turning off completely if no current is supplied from the previous transistors. Additional high-frequency compensation for this stage is provided by variable inductor L485.

X-Y DELAY COMPENSATION and HORIZONTAL INTERFACE

General

The X-Y Delay Compensation network provides a delay for the horizontal (X) portion of an X-Y display to match the delay of the vertical (Y) signal due to the Delay Line. The Horizontal Interface portion of the circuit selects the horizontal deflection signal from the output of the A Horizontal and/or the B Horizontal plug-in unit. Fig. 3-27 shows a detailed block diagram of this circuit. A schematic of this circuit is shown on diagram 6 at the rear of this manual.

X-Y Delay Compensation

Time-Base Operation. When the plug-in unit installed in the A or B horizontal compartment is operated as a standard time-base unit to produce a horizontal sweep for deflection of the CRT beam, the A or B Delay Compensation Networks are effectively disabled. The X Compensation Inhibit command is HI and relays K50-K60 or K70-K80 are not actuated. Therefore, the relay contacts remain in the normally closed position so the horizontal signal passes directly through this network to the Horizontal Interface circuit without delay.

X-Y Operation. If the time-base unit installed in the A or B horizontal compartment is operated as an amplifier or if a vertical unit is installed in a horizontal compartment, the X Compensation Inhibit command to the applicable Delay Compensation Network drops to the LO level (zero volts). This provides an actuating level to relays K50-K60 or K70-K80 to connect the Delay Compensation Network into the circuit. Diodes CR50 and CR70 shunt the voltage

produced across the relays when the actuating level is removed. For example, if the X Compensation Inhibit command from the A Horizontal Unit goes LO, K50 and K60 close to route the A Horizontal Signal through the A Delay Compensation Network. LR networks L51-R51 and L61-R61 along with capacitors C53 and C55 provide a constant input impedance. The LC network comprised of C56-C58-C66-C68-L55-L56-L65-L66 provides a fixed delay from DC to about two megahertz to provide minimum phase shift between the X and Y portions of the CRT display. C55 is adjusted to match the horizontal delay to the vertical delay up to at least two megahertz.

The Delay Compensation Network normally produces negative preshoot distortion along with some corner rounding of fast step functions. The A Delay Disable switch S50 allows selection of a display with either minimum phase-shift characteristics or optimum step response. When this switch is set to Out (down), the X Compensation Inhibit command from the A Horizontal Unit is disconnected from relays K50-K60. Now, the signal from the A Horizontal Unit passes directly to the Horizontal Interface circuit without delay to provide a horizontal display with optimum step response.

The B Delay Compensation Network operates in the same manner as described above. The X-Y Delay Compensation Network is an optional feature. For instruments which are not equipped with this feature, the horizontal signals from the plug-in units are connected directly to the Horizontal Interface circuit.

Horizontal Channel Switch

The Horizontal Channel Switch determines which input signal provides the horizontal signal to the Horizontal Amplifier circuit as controlled by the Horizontal Mode Signal from the Logic Circuit. Resistors R371-R372 and R373-R374 establish the input resistance of this stage and provide a load for the A and B Horizontal units. Resistors R384-R385-R386 and R391-R392-R393 establish the operating levels for this stage. R384-R385 and R391-R392 set the current gain for each channel. C381-R381 and C391-R391 provide frequency compensation. Thermistors RT383 and RT390 provide a constant gain for this stage as the ambient temperature changes.

This stage is made up primarily of integrated circuit U384 which is the same type as used for the Trigger

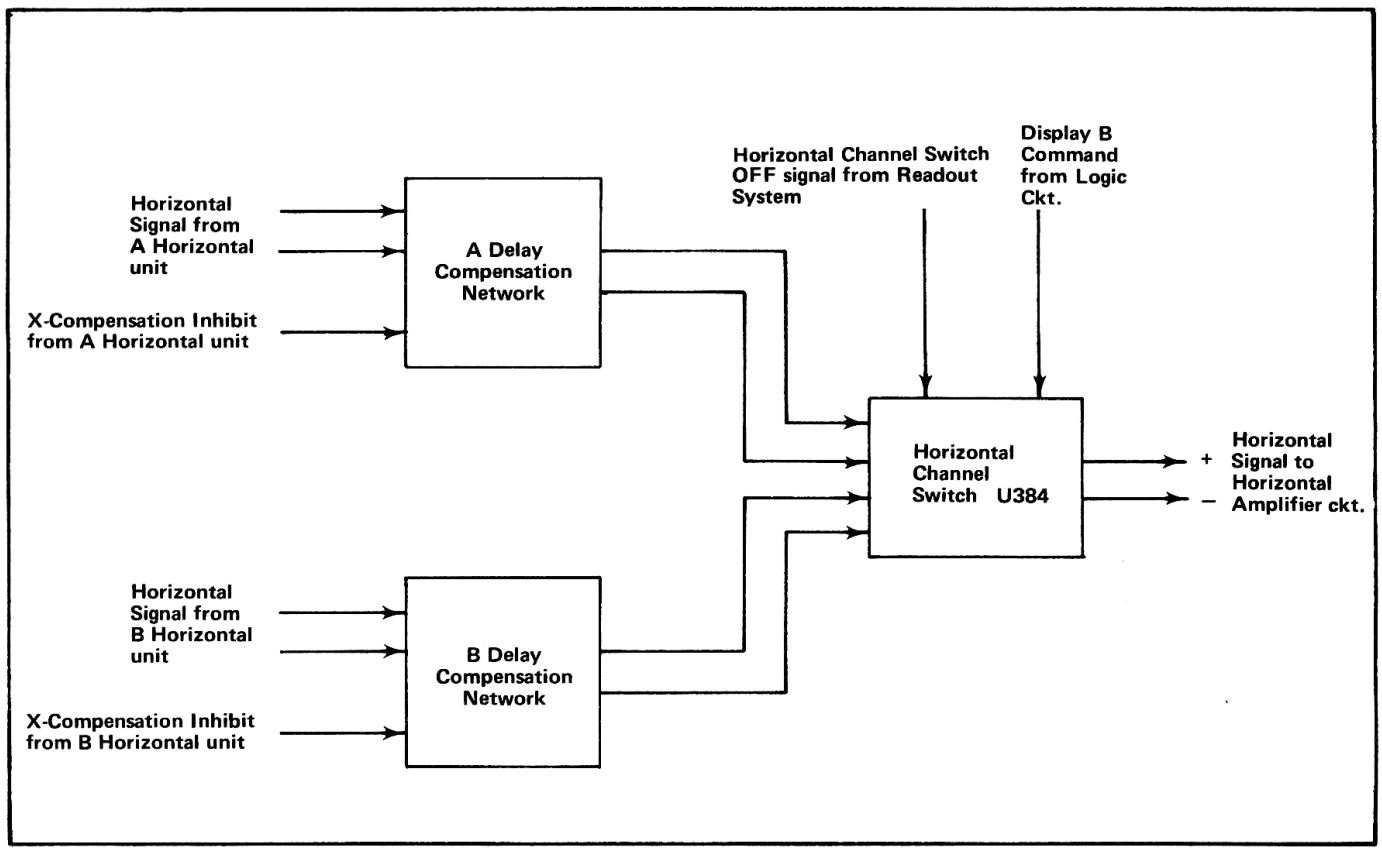


Fig. 3-27. Detailed block diagram of X-Y Delay Compensation network and Horizontal Interface.

Channel Switch and Vertical Channel Switch stages. An input/output table for U384 is shown in Fig. 3-28. U384 provides a high-impedance differential input for the signal from the A Horizontal unit at pins 2 and 15 and the signal from the B Horizontal unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal which is connected to the Horizontal Amplifier circuit. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9 and 16 in all modes. This provides a constant DC output current level to the following stage as the HORIZONTAL MODE switch is changed.

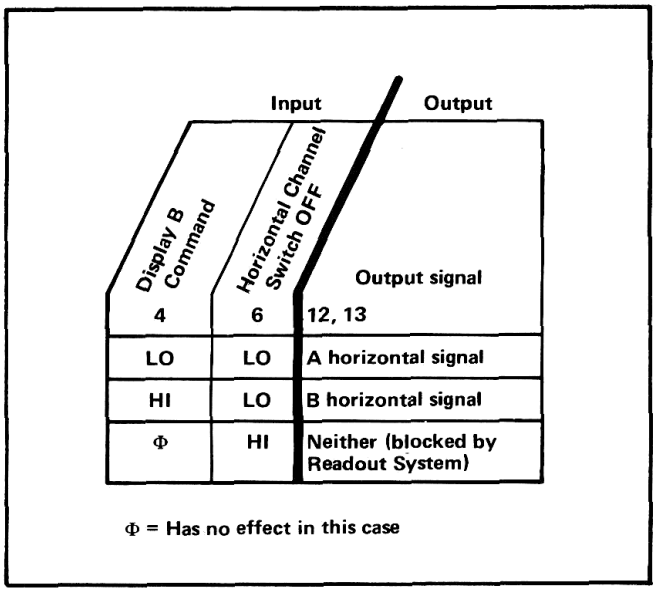


Fig. 3-28. Input/output table for Horizontal Channel Switch.

When the HORIZONTAL MODE switch is set to A, the level at pin 4 is LO. This level allows the signal from the A Horizontal unit to pass to the output while the signal from the B Horizontal unit is blocked. In the B position of the HORIZONTAL MODE switch, the level at pin 4 is HI. Now, the signal from the B Horizontal unit is connected to the output while the signal from the A Horizontal unit is blocked.

For ALT or CHOP positions of the HORIZONTAL MODE switch, the Horizontal Mode Signal at pin 4 switches between the LO and HI levels at a rate determined by the Horizontal Binary stage in the Logic Circuit. This action allows the signals from the A Horizontal unit to be displayed when the Horizontal Mode Signal is LO and the signal from the B Horizontal Unit is displayed when the Horizontal Mode Signal is HI.

The Horizontal Channel Switch OFF signal from the Readout System which is applied to pin 6 has final control over the output signal from this stage. Quiescently, this signal is LO and the signal from the selected horizontal unit can pass to output pins 12 and 13. However, when the Readout System is ready to display readout information, the level at pin 6 goes HI. This level blocks the signal from both horizontal units so there is no signal output from this stage under this condition.

The output signal at pins 12 and 13 is connected to the Horizontal Amplifier circuit via the Main Interface circuit. Resistors R395-R396 and R398-R399 establish the correct operating DC levels for U384 as well as to establish a load resistance of about 50 ohms for this stage. C397-R397 provide frequency compensation.

HORIZONTAL AMPLIFIER

General

The Horizontal Amplifier circuit amplifies the push-pull horizontal deflection signal from the Horizontal Interface circuit and connects it to the horizontal deflection plates of the CRT. This circuit also accepts the X-signal from the Readout System to produce the horizontal portion of a readout display. Fig. 3-29 shows a detailed block diagram of the Horizontal Amplifier circuit. A schematic of this circuit is shown on diagram 7 at the rear of this manual.

Input Amplifier

The horizontal signal from the Horizontal Interface circuit is connected to the bases of Q504 and Q514. The Input Amplifier is driven from an equivalent 50-ohm source. This stage provides adjustments to set the overall gain of the Horizontal Amplifier circuit and to balance the collector current of Q504 and Q514. Resistors R502-R503-R504-R514-R515 provide degeneration between the emitters of Q504 and Q514. Horizontal Gain adjustment R515 determines the amount of emitter degeneration to control the signal gain of this stage. DC Center adjustment R505 balances the quiescent current through Q504 and Q514 to produce a centered spot on the CRT with no horizontal deflection signal applied.

For readout displays, the X-signal from the Readout System is connected to the base of Q514 through R511. The signal from the horizontal units is blocked by the Horizontal Channel Switch (see Vertical and Horizontal Interface description). Q514 and Q504 operate as a paraphase amplifier to display the readout information. The signal connected to the base of Q514 produces an inverted output signal at the collector of Q514. At the same time, the emitter of Q514 moves in the same direction as the applied signal, and this change is connected to the emitter of Q504 through R502 and R515. As far as readout-signal change is concerned, Q504 operates as an emitter-driven

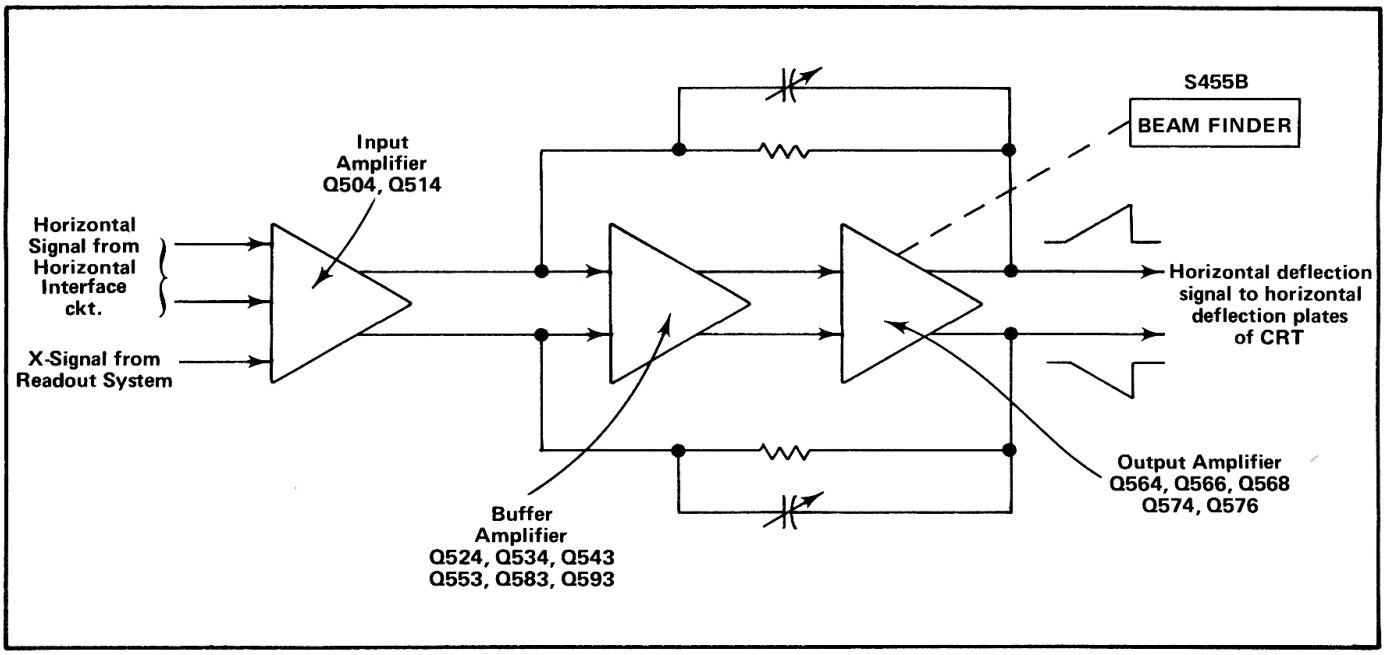


Fig. 3-29. Horizontal Amplifier detailed block diagram.

common-base stage. Therefore, the change at its emitter produces a similar change at its collector. Thus the single-ended input signal at the base of Q514 is available as a push-pull signal at the collectors of Q504 and Q514. For instruments which are not equipped with a Readout System, R511 is connected to ground at the chassis where the Readout System board is mounted.

Buffer Amplifier and Output Amplifier

The signal from the Input Amplifier stage is connected to the Buffer Amplifier through the limiting network CR508-CR518-CR523-CR533. These diodes protect the Buffer Amplifier stage from being overdriven by excessive current drive from the Input Amplifier stage. The output signal from the Input Amplifier stage is a current signal. With normal horizontal deflection signals which produce an on-screen display, CR523 and CR533 remain forward biased and CR508-CR518 are reverse biased. However, when high-amplitude horizontal deflection signals are applied to this circuit as a result of sweep magnification or high-amplitude external horizontal signals, either CR523 or CR533 is reverse biased, depending on the polarity of the overdrive signal. This results in a sufficient voltage change at the anode of either CR508 or CR518 to forward bias it. The shunt diodes provide a current path for the signal current to limit the voltage change during the overdrive condition. Limit Center adjustment R525 balances the quiescent current at the emitters of Q524 and Q534 so limiting does not occur during the displayed portion of the horizontal deflection signal.

The Buffer Amplifier Q524-Q534 provides a low-impedance input for the signal current from the Input Amplifier. The signal at the collectors of Q524-Q534 is connected to the Output Amplifier through emitter followers Q543-Q553. Q543 and Q553 provide a current gain for the horizontal deflection signal. Each half of the Output Amplifier is a current driven stage with a voltage output to drive the horizontal deflection plates of the CRT and feedback to the input of the Buffer Amplifier stage for linearity. The Output Amplifier has a low input impedance and requires very little voltage change at the input to produce the desired output change. Q568 provides a stable voltage source for the bases of Q566-Q576. Diodes CR564-CR574 limit the negative level at the bases of Q564 and Q574 to about 0.6 volts to protect these transistors in case of failure or removal of Q543 or Q553. Negative feedback is provided from the collectors of Q566 and Q576 to the input of the Buffer Amplifier through feedback networks C581-R580-R581-Q583-C588-R588-R589 and C591-R590-R591-Q593-C598-R598-R599. Emitter followers Q583-Q593 in the feedback networks provide isolation between the input of the Buffer Amplifier and the output of the Output Amplifier stage. With this configuration, the input impedance of the Buffer Amplifier appears low since the feedback network beyond the emitter followers is effectively disconnected as far as the input signal is concerned. However, the total feedback network is active for the feedback signal. Variable capacitors C581, C588, C591 and C598 adjust the transient response of the feedback networks to provide good linearity at fast sweep rates.

The BEAM FINDER switch S455B reduces horizontal scan by limiting the voltage swing of Q566 and Q576 when actuated. Normally the collectors of these transistors are returned to +150 volts and CR565 is reverse biased to disconnect the +75-volt level. However, when the BEAM FINDER switch is actuated, the power from the +150-volt supply is interrupted and the collector voltage for Q566-Q576 is supplied from the +75-volt supply through CR565. This reduced collector voltage limits the output voltage swing at the collectors of Q566-Q576 to limit the trace within the graticule area.

OUTPUT SIGNALS AND CALIBRATOR

General

The Output Signals and Calibrator circuit provides output signals to the connectors located in the OUTPUTS section of the front panel. These output signals are either generated within this instrument or are samples of signals from the associated plug-in units. Fig. 3-30 shows a detailed block diagram of the Output Signals and Calibrator circuit. A schematic of this circuit is shown on diagram 8 at the rear of this manual.

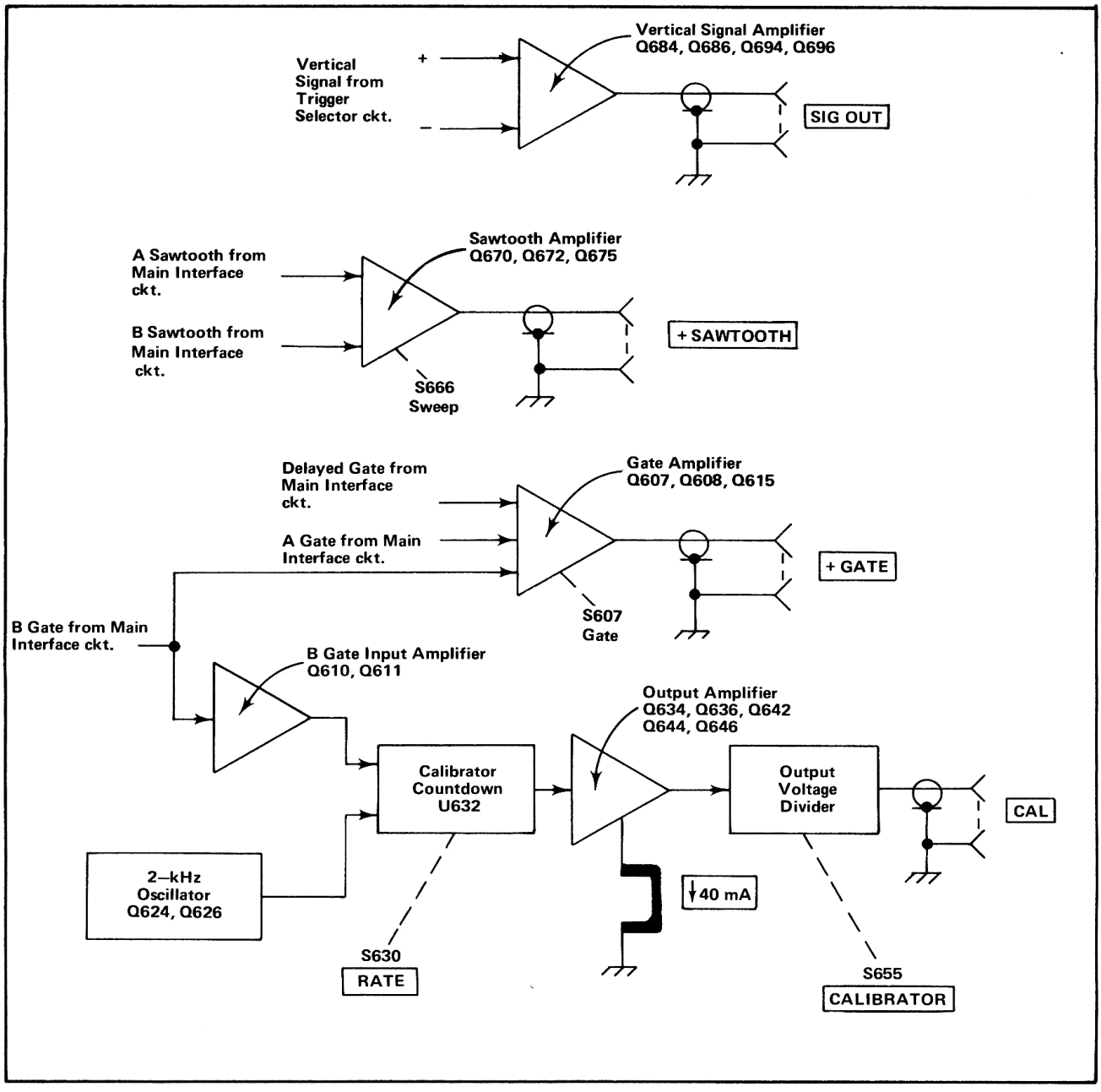


Fig. 3-30. Output Signals and Calibrator detailed block diagram.

Vertical Signal Amplifier

The vertical signal selected by the B Trigger Channel Switch (see Trigger Selector description for more information) is connected to the bases of differential amplifier Q684-Q694. Resistors R681-R692 establish an input resistance of about 50 ohms for this stage. The amplified signal at the collectors of Q684 and Q694 is connected to buffer amplifier Q686-Q696 through RC networks C686-R686 and C695-R695. These networks provide thermal balance for this stage. The single-ended signal at the collector of Q686 is connected to the front-panel SIG OUT connector J699. The signal at the collector of Q696 is connected to chassis ground. CR696 and CR699 protect this stage if high-level voltages are accidentally applied to the SIG OUT connector. CR696 provides protection from positive voltages and CR699 provides protection from negative voltages.

Sawtooth Amplifier

The sawtooth signals from the A Time-Base unit and the B Time-Base unit are both connected to the Sawtooth Amplifier stage through series resistors R32 and R34 respectively (on Main Interface board). The Sweep switch S666 (located on Output Signals board) determines which sawtooth signal provides the output signal. The other sawtooth signal is terminated by R667 to provide a similar load to the signal source. Transistors Q670, Q672 and Q675 comprise an inverting feedback amplifier. Gain of this stage is about two as determined by the ratio of feedback resistor R678 to the input resistance made up of R669 and either R32 or R34, depending on which sawtooth source is selected. The signal at the collector of Q675 is connected to the front-panel + SAWTOOTH connector J679 through R679. RC network C675-R675 provides frequency response stabilization for this stage. Diode CR674 provides protection from high-level positive voltages inadvertently connected to the output connector by providing a current path to the +15-volt supply through the collector-base junction of Q675. Then, CR674 is forward biased to clamp the base of Q675 at this level. CR676 provides protection from high-level negative voltages at the + SAWTOOTH connector by clamping the output if it attempts to go more negative than about −15.6 volts.

Gate Amplifier

The output signal at the front-panel + GATE connector J618 is selected from three input gate signals by Gate switch S607 (located on Output Signals board). In the A position, the A Gate signal from the A Time-Base unit is connected to the base of emitter-follower Q607 through R607. The base of Q608 is connected to ground by S607 in this position so it operates as a common-base stage. Q607 provides a high input impedance for the stage while the emitter coupling between Q607-Q608 provides temperature compensation. Operation is the same in the B position of S607 except that the B Gate signal from the B Time-Base unit provides the input signal. In the Dly'd position, S607 connects the base of Q607 to ground through R607 and disconnects both the A and B Gate signals. Now, the Delayed Gate signal from the delaying time base (in A HORIZ compartment) can pass to the base of Q608 through R602. Q608 inverts this negative-going input signal so the gate output signals at the + GATE connector are all positive going.

The input gate signal selected by S607 is connected to the emitter of Q615 through C612-R612. Diode CR614 provides temperature compensation for Q615. The signal at the collector of Q615 is connected to the + GATE connector through CR615 and R617. CR615 protects Q615 if a high-level positive voltage is applied to the + GATE connector and CR616 clamps the output at about −0.6 volts if a negative signal is applied to this connector.

B Gate Amplifier

The B Gate signal from the B Time-Base unit is connected to the base of Q610 through R610. Q610 amplifies and inverts the B Gate signal to provide a negative-going gate signal to the Calibrator circuit for B GATE operation of the Calibrator. Q611 provides temperature compensation for this stage.

Calibrator

General. The Calibrator circuit provides a 40 milliampere current output at the front-panel current loop and a voltage output in calibrated steps from four millivolts to 40 volts at the front-panel CAL connector. Mode and repetition rate of the output signal are selected by the calibrator RATE switch and the output voltage amplitude is selected by the CALIBRATOR switch.

2-kHz Oscillator. Q624 and Q626 are connected as a two-kilohertz, square-wave oscillator to provide the drive signal for the Calibrator Countdown stage (one-kilohertz output rate only). Oscillation occurs as follows: Assume that Q624 is conducting and Q626 is off. The collector current of Q624 through R624-R625 produces a voltage level which holds the base of Q626 low. This keeps Q626 turned off and since there is no current through it, its collector goes positive to produce the positive portion of the square wave. At the same time, C621 begins to charge toward −50 volts through R627. The emitter of Q626 goes negative also as C621 charges until it reaches a level about 0.6 volt more negative than the level at its base. Then, Q626 is forward biased and its emitter rapidly rises positive. Since C621 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q626 pulls the emitter of Q624 positive also to reverse bias it. The current through Q626 produces a voltage drop at its collector to produce the negative portion of the square wave.

Now, conditions are reversed. Since Q624 is reverse biased, there is no current through it. Therefore, C621 can begin to discharge through R621. The emitter level of Q624 follows the discharge of C621 until it reaches about −0.6 volt. Then, Q624 is forward biased and its collector drops negative to reverse bias Q626. This interrupts the current through Q626 and its collector goes positive again to complete the square wave. Once again, C621 begins to charge through R627 to start the second cycle. The signal produced at the collector of Q626 is a two-kilohertz square wave. C628 differentiates this signal to produce positive- and negative-going output pulses, coincident with the rise and fall of the square wave, which provides negative-going trigger pulses for the Calibrator Countdown stage (positive-going pulses have no effect on circuit operation). The 1 kHz adjustment, R625, sets this stage so an accurate one-kilohertz square-wave is produced at the output of the Calibrator circuit.

Calibrator Countdown. Integrated circuit U632 is a triggered set-clear flip-flop. An input/output table for this device is shown in Fig. 3-31. The calibrator RATE switch S630 determines the operating mode of U632 and also selects the source of its trigger signal. S630 is a cam-type switch; a contact-closure chart showing its operation is given on diagram 8. The dots on this chart indicate when the associated contact is closed. For the DC (current only) positions (contacts on diagram shown in this position), a LO level is applied to the Set input (pin 3) and a HI level is applied to the Clear input (pin 1). The next negative-going trigger from the 2-kHz Oscillator stage switches the output at pin 7 to its HI level (see input/output table). The output at pin 7 remains at the HI level as long as the RATE switch remains in this position.

For the 1 kHz position, all contacts except 5 are closed. This places a LO level at both the Set and Clear inputs so that pin 7 changes output levels with each negative-going trigger from the 2-kHz Oscillator stage. This results in a one-kilohertz square wave output signal at pin 7. The Set and Clear inputs are also held LO in the B GATE ÷2 position of S630 so that U632 changes output levels with each negative-going pulse at its trigger input. However, the signal from the 2-kHz Oscillator is disconnected and the B-Gate signal provides the trigger to pin 2 resulting in an output square wave with a repetition rate which is one-half the B Gate repetition rate. For DC (volts only) operation, the Clear input is held LO and the Set input is held HI. The negative-going trigger pulse, furnished by the 2-kHz Oscillator stage switches the level at pin 7 to LO where it remains until the RATE switch is changed.

Output Amplifier. Transistors Q642 and Q644 are connected as a comparator with the reference level at the base of Q644 determined by network R647-R648-R649-Q646. This network establishes a voltage level at the base of Q644 which results in 8.88 milliamperes collector current through Q644 when it is on. The 0.4 V adjustment R649 is set in the 0.4 V position of the

Input		Output
3	1	Condition at pin 7 after trigger pulse
LO	LO	Output changes state with each trigger pulse
LO	HI	HI
HI	LO	LO
HI	HI	No change

Fig. 3-31. Input/output table for U632.

CALIBRATOR switch to provide accurate calibrator output voltages at the CAL connector J650. Resistors R640-R641 and R642 form a current divider to determine the current through the front-panel 40 mA current loop when Q642 is conducting. The 40 mA adjustment R640 is set so eight milliamperes flows through R642 and the current loop. The current loop is a five-turn current transformer, so the effective current applied to a current probe is 40 milliamperes.

The output of the Calibrator Countdown stage is connected to the base of Q634 through R634. Q634 acts as a switch to control the current through Q636, and the output of Q636 controls the conduction of comparator Q642-Q644. When DC (current only) operation is selected by the calibrator RATE switch, a HI level is applied to the base of Q634 and it is forward biased. This allows current to flow through Q636 and the resultant voltage drop across R636 forward biases Q642. The collector current of Q642 produces an equivalent 40 milliampere DC current (eight milliamperes through five turns) in the probe loop. At the same time, Q644 is off and there is no current through the Output Voltage Divider so there is no output at the CAL connector. Conditions are reversed for DC (volts only) operation. A LO level is applied to Q634 to cut it off. Therefore, there is no current through Q636 and the base of Q642 rises positive to cut it off also. Now, the collector current of Q644 produces a voltage drop across the Output Voltage Divider to provide a DC voltage output at the CAL connector. Since Q642 is off, there is no current through the current loop under this condition.

For the 1 kHz and B GATE ÷2 positions, the base of Q634 varies between the LO and HI levels at the rate selected by the calibrator RATE switch. When the base of Q634 is LO, Q642 is off and Q644 is conducting. This produces an output voltage at the CAL connector but no current through the current loop as for DC (volts only)

operation. When the level at the base of Q634 is switched to HI, Q644 conducts and Q646 is reverse biased. Now, current flows through the current loop and the voltage level at the CAL connector drops to zero as for DC (current only) operation. Notice that the current and voltage output of the calibrator are out of phase; the current through the current loop is at maximum when the voltage output at the CAL connector is minimum, and vice versa.

Output Voltage Divider. The collector current of Q644 in the Output Amplifier stage is applied across the voltage divider made up of resistors R652 through R659. This divider is designed to provide a low output resistance in all positions except 40 V while allowing selection of output voltages between 4 mV and 40 V. The output resistance in the 40 V position is about 15 kilohms as determined by R651 and the equivalent resistance of divider network R652-R659. This means that a 1.5 megohm load will produce about 1% error in output voltage; error increases as the load resistance decreases. The CALIBRATOR switch S655 selects the output from the divider to provide the output voltages listed on the front panel (into high-impedance load). The values shown in brackets indicate the output resistance into a 50-ohm load (notice that 40 V position lists no output into 50 ohms and should not be used in this manner). S655 is a cam-type switch and the dots on the contact-closure chart (see diagram 8) indicate when the associated contact is closed.

CRT CIRCUIT

General

The CRT Circuit produces the high-voltage potentials and provides the control circuits necessary for the operation of the cathode-ray tube (CRT). This circuit also includes the Z-Axis Amplifier stage to set the intensity of the CRT display. Fig. 3-32 shows a detailed block diagram of the CRT Circuit. A schematic of this circuit is shown on diagram 9 at the rear of this manual.

High-Voltage Oscillator

Unregulated voltage for operation of the high-voltage supply is provided from the +15-Volts Rectifier (see Low-Voltage Power Supply). Diode CR759 disconnects the negative side of this unregulated voltage from the collector of Q756 at the time of turn-on. This allows the starting current for the High-Voltage Oscillator to be supplied from the +15-Volt Supply through R759 and Q756. As the output of the high-voltage supply increases to its required output level, the collector of Q756 goes negative until CR759 is forward biased. Now the collector supply level for Q756 is provided by the negative side of the unregulated voltage. This configuration provides a controlled starting current for the High-Voltage Oscillator at turn-on and at the same time allows the High-Voltage Regulator stage to

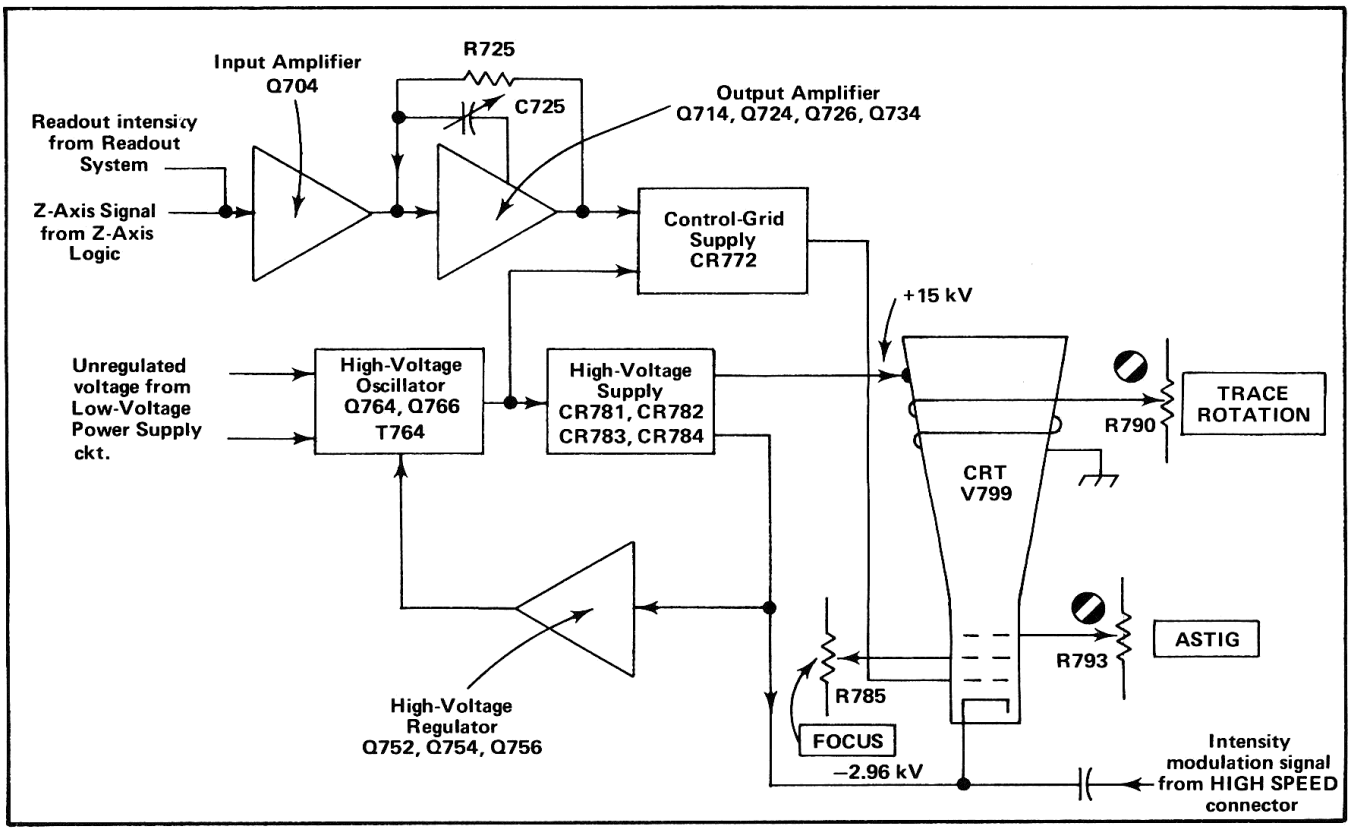


Fig. 3-32. CRT Circuit detailed block diagram.

control the current for the High-Voltage Oscillator after the stage reaches operating potentials to regulate the output level.

Q764-Q766 and the associated circuitry comprise the high-voltage oscillator to drive the high-voltage transformer T764. When the instrument is turned on, starting current is supplied to the bases of both Q764 and Q766. Both transistors are forward biased, and they both attempt to come into conduction. However, since the transistors will not have identical characteristics (even though they are of the same type), one transistor conducts more heavily than the other. For purposes of this explanation, assume that Q764 conducts more heavily. The collector current of Q764 produces a corresponding current increase in the base-feedback winding of T764 to further increase the bias on Q764. At the same time, the voltage developed across the base-feedback winding connected to Q766 reverse biases it. As long as the collector current of Q764 continues to increase, a voltage is induced into the base-feedback winding of T764 which holds Q764 forward biased. However, when the collector current of Q764 stabilizes, the magnetic field built up in T764 begins to collapse. This induces an opposite current into the base windings which reverse biases Q764, but forward biases Q766. When the induced voltage at the base of Q766 exceeds the bias set by Q756, Q766 is forward biased and the amplified current at its collector adds to the current flowing through T764 due to the collapsing field. Then as the current through T764 stabilizes again, the magnetic field around it once more begins to collapse. This induces a voltage into the base windings which forward biases Q764 and reverse biases Q766 to start another cycle.

The signal produced across the primary of T764 is a sine wave at a frequency of 35 to 45 kilohertz. C764-L764 shapes the signal in the primary of T764 so it maintains essentially a sine-wave characteristic. The amplitude of the oscillations in the primary of T764 is controlled by the High-Voltage Regulator stage to set the total accelerating potential for the CRT. Filter network C762-L762 decouples high peak operating currents from the +15-volt Supply.

High-Voltage Regulator

A sample of the secondary voltage from T764 is connected to the High-Voltage Regulator stage through divider R740-R741-R742. Q752 and Q754 are connected as an error amplifier to sense any change in the voltage level at the base of Q752. The −15-Volt Supply, connected to the emitter of Q752 through R753, provides the reference level for this stage. High-Voltage adjustment R745 sets the quiescent level at the base of Q752 to a level which establishes a −2.96 kV operating potential at the CRT cathode. CR741 protects Q752 from excessive reverse emitter-base voltage.

Regulation occurs as follows: If the output voltage at the −2.96 kV test point starts to go positive (less negative), a sample of this positive-going change is connected to the base of Q752. Both Q752 and Q754 are forward biased by this positive change, which in turn increases the conduction of Q756. This results in a more positive level at the emitter of Q756 and a more positive bias level at the bases of Q764 and Q766. Now, the bases of both Q764 and Q766 are biased closer to their conduction level so that the feedback voltage induced into their base-feedback windings produces a larger collector current. This results in a larger induced voltage in the secondary of T764 to produce a more negative level at the −2.96 kV test point to correct the original error. In a similar manner, the circuit compensates for output changes in a negative direction. Since the amplitude of the voltage induced into the secondary of T764 also determines the output level of the positive supply and the Control-Grid Supply, the total high-voltage output is regulated by sampling the output of the negative supply.

High-Voltage Supplies

The high-voltage transformer T764 has three output windings. One winding provides filament voltage for the cathode-ray tube. Two high-voltage windings provide the negative and positive accelerating potentials for the CRT and provide the bias voltage for the control grid. All of these outputs are regulated by the High-Voltage Regulator stage to maintain a constant output voltage as previously described.

Positive accelerating potential for the CRT anode is supplied by voltage tripler C782-C783-C784-CR782-CR783-CR784. This rectified voltage is filtered by C785-R780-R781 to provide a constant output of about +15 kilovolts. All of these components are included in an encapsulated assembly. The negative accelerating potential for the CRT cathode is also obtained from this same secondary winding. Half-wave rectifier CR781 provides an output voltage of about −2.96 kilovolts which is connected to the CRT filament and cathode through L781 and L788. The cathode and filament are connected together through L788 to prevent cathode-to-filament breakdown due to a large difference in potential between these CRT elements. A sample of the negative accelerating voltage is connected to the High-Voltage Regulator stage to maintain a regulated high-voltage output.

Half-wave rectifier CR772 provides a negative voltage for the control grid of the CRT. Output level of this supply is set by CRT Grid Bias adjustment R775. Neon bulbs DS786-DS787-DS788 protect the CRT by limiting the voltage difference between the cathode and control grid to a maximum of about 165 volts if either the Control-Grid Supply or negative High-Voltage Supply should fail. The Unblanking Gate from the Z-Axis Amplifier circuit is

connected to the positive side of this circuit. As the Unblanking Gate level changes, it shifts the overall supply level to change the bias on the CRT to control the intensity of the display.

Intensity modulating signals from the rear panel HIGH SPEED Z AXIS connector (see diagram 12), are applied to the CRT cathode through C789, R786 and C786. This signal changes the CRT bias, and thereby the intensity of the display, by changing the level on the cathode.

CRT Control Circuits

Focus of the CRT display is determined by the FOCUS control R785. This control is part of divider R782-R785-R744-VR786 between the negative high-voltage supply and ground. Therefore, the voltage applied to the focus grid is more positive (less negative) than the voltage on either the control grid or cathode. The ASTIG adjustment R793, which is used in conjunction with the FOCUS control to obtain a well-defined display, varies the positive level on the astigmatism grid. Geom adjustment R792 varies the positive level on the horizontal deflection plate shields to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field around the CRT. Y Axis adjustment R795 controls the current through L795 which affects the CRT beam after vertical deflection but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. The TRACE ROTATION adjustment R790 controls the current through L790 and affects both the vertical and horizontal rotation of the beam.

Z-Axis Amplifier

General. The Z-Axis Amplifier circuit is a current driven, shunt-feedback amplifier with a voltage output. This output voltage provides the drive signal to control the CRT intensity level through the Control-Grid Supply. Details of operation for the stages in this circuit follow.

Input Amplifier. Transistor Q704 is a common-base amplifier to establish a low input impedance for the Z-Axis Amplifier stage. Zener diode VR709 provides an operating level of about +5.1 volts at the base of Q704. The quiescent current to the emitter of Q704 is set by the DC level adjustment R705 so the Z-Axis Amplifier circuit operates within its linear range. The output level of this stage is determined by the input current from either of two circuits. For normal operation, the Z-Axis Signal from the Logic Circuit sets the input current as determined by the front-panel A and B INTENSITY controls, the chopped blanking logic or an external signal connected to either of the rear-panel Z-Axis inputs (see Logic Circuit description for details). For readout displays, the Z-Axis Signal is blocked in the Logic Circuit. Now, the input current is provided from the Readout System as determined by the READOUT intensity control on the front panel.

Output Amplifier. The output stage is a shunt-feedback operational amplifier with feedback connected from the output to the input through C725-R725. The output voltage is determined by the input current multiplied by the feedback resistor and is expressed by the formula: $E_{out} \cong I_{in} \times R_{FB}$ where R725 is R_{FB}. The signal current change at the base of Q714 for maximum intensity is about 4 milliamperes. Therefore, the output voltage change is about 63 volts (4 mA X 15.8 kΩ). AC feedback is provided from the base circuit of Q734 to the base of Q714 by C725 which is adjusted for optimum step response. This provides a fast-rise unblanking gate output signal with minimum overshoot or ringing. Otherwise, the CRT display would vary in intensity level following sudden changes in blanking level.

The signal from the Input Amplifier stage is connected to the bases of Q724 (through C723) and Q726 through emitter follower Q714. These transistors are connected as a collector-coupled complementary amplifier to provide a linear, fast output signal while consuming minimum quiescent power. Q726 maintains the low-frequency response of the input signal and provides a fast falling edge on the output signal. Only the fast-changing portions of the signal at the emitter of Q714 are coupled to the base of Q724 through C723. Since Q724 is a PNP-type transistor, it responds faster to negative-going changes at its base than to positive-going changes. This action provides a fast rising edge on the output signal (fast falling edge provided by Q726, an NPN-type transistor). Emitter follower Q734 and diode CR734 provide a low-impedance output with fast response for both positive- and negative-going changes in output level. CR734, connected across the base-emitter junction of Q734, improves the output response for the negative-going portion of the unblanking gate. When the base of Q734 is driven negative to cutoff, CR734 is forward biased to quickly pull the emitter of Q734 negative also to provide a fast falling edge on the output signal. The signal at the emitter of Q734 is connected to the Control-Grid Supply stage through R736.

Diodes CR714, CR726 and CR736 provide protection for the Z-Axis Amplifier circuit. CR714 and CR736 protect this stage from damage due to high-voltage surges connected back into this circuit from the high-voltage supplies. CR726 protects Q726 by clamping its base at −0.6 volts if Q714 fails or is removed from its socket while the instrument is on.

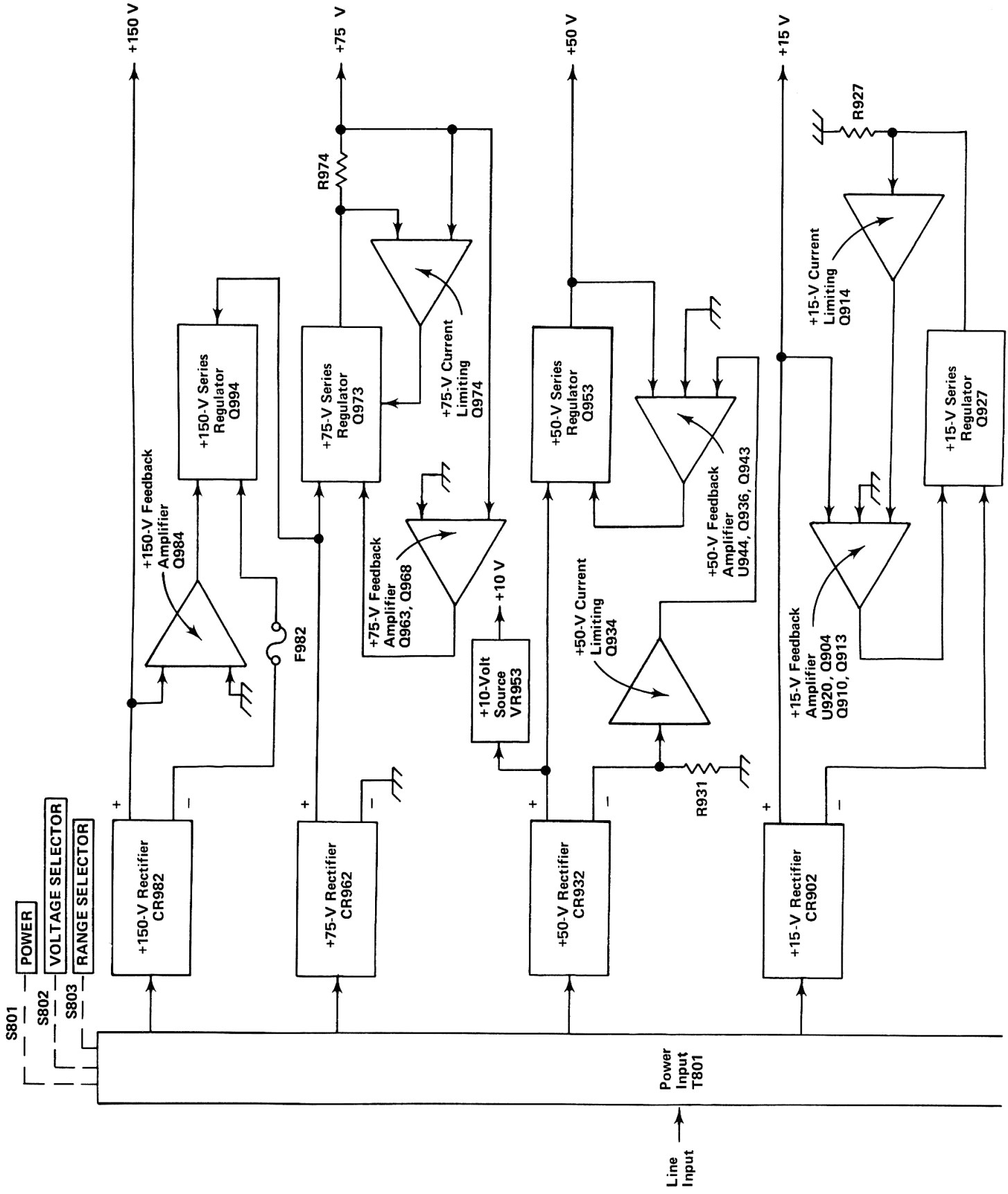


Fig. 3-33. Low-Voltage Power Supply detailed block diagram.

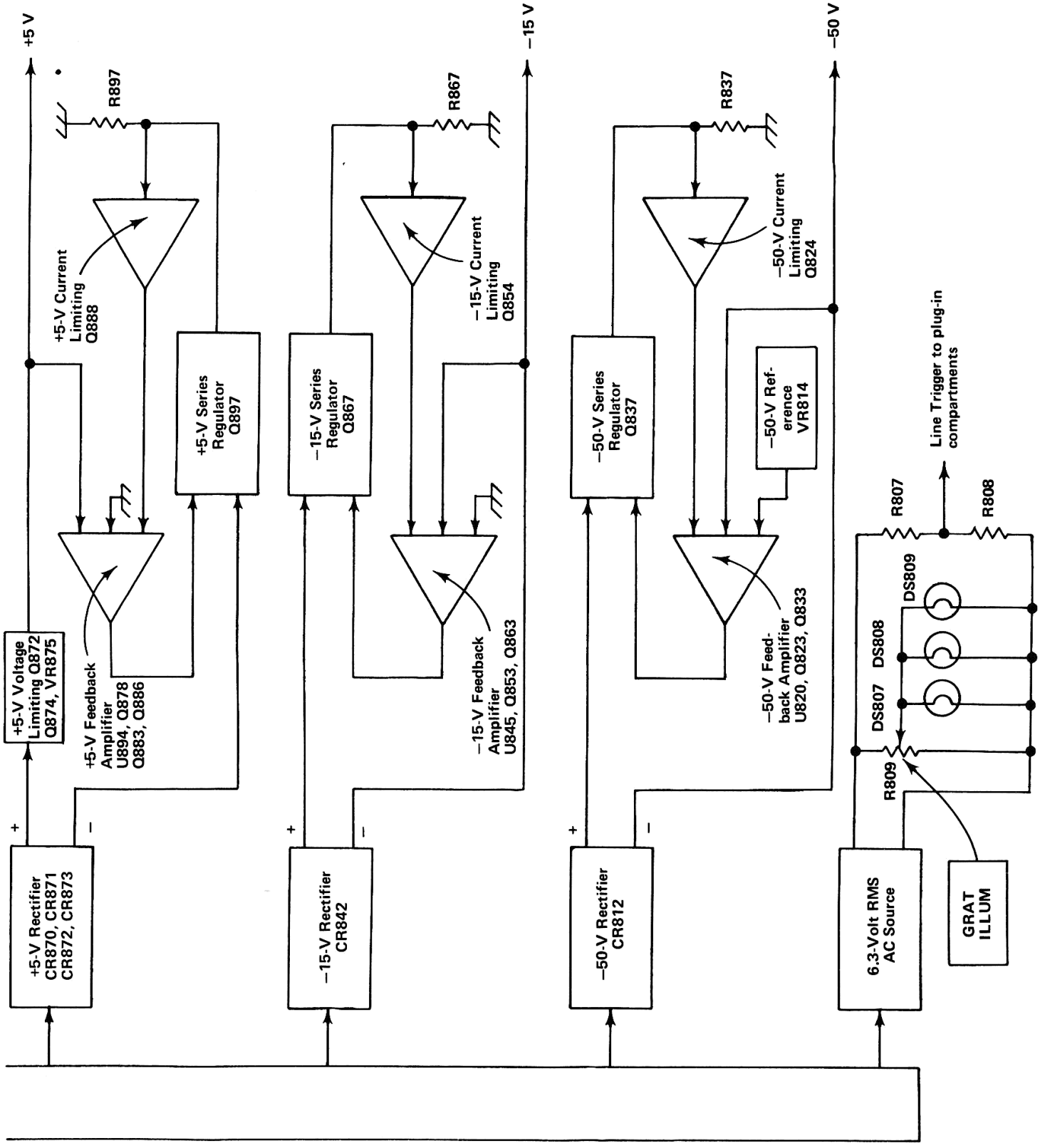


Fig. 3-33. Low-Voltage Power Supply detailed block diagram.

LOW-VOLTAGE POWER SUPPLY

General

The Low-Voltage Power Supply circuit provides the operating power for this instrument from seven regulated supplies. Electronic regulation is used to provide stable, low-ripple output voltages. Each regulated supply (except the +150-Volt Supply) contains a short-protection circuit to prevent instrument damage if a supply is inadvertently shorted to ground. The Power Input stage includes the Voltage Selector Assembly. This assembly allows selection of the nominal operating voltage and regulating range for the instrument. Fig. 3-33 shows a detailed block diagram of the Low-Voltage Power Supply circuit. A schematic of this circuit is shown on diagrams 10 and 11 at the rear of this manual.

Power Input

Power is applied to the primary of transformer T801 through the EMI (electro-magnetic interference) filter FL801, 115-volt line fuse F801, POWER switch S801, thermal cutout TK801, Voltage Selector switch S802 and Range Selector switch S803. The Voltage Selector switch S802 connects the two halves of the primary of T801 in parallel for 115-volt nominal operation, or in series for 230-volt nominal operation. A second line fuse, F802, is connected into the circuit when the Voltage Selector switch is set to 230 V position to provide the correct protection for 230-volt operation (F802 current rating less than rating of F801).

The Range Selector switch S803 allows the instrument to regulate correctly on higher or lower than normal line voltages. Each half of the primary of T801 has taps above and below the 115-volt (230) nominal point. As the Range Selector switch S803 is switched from LO to M to HI, more turns are effectively added to the primary winding and the turns ratio is decreased. This configuration compensates for higher or lower than normal line voltage to extend the regulating range of the Low-Voltage Power Supply.

Thermal cutout TK801 provides thermal protection for this instrument. If the internal temperature of the instrument exceeds a safe operating level, TK801 opens to interrupt the applied power. When the temperature returns to a safe level, TK801 automatically closes to re-apply the power.

–50-Volt Supply

The following discussion includes the description of the –50-V Rectifier, –50-V Series Regulator, –50-V Feedback Amplifier, –50-V Reference and –50-V Current Limiting stages. Since these stages are closely related in the production of the –50-volt regulated output voltage, their operation is most easily understood when discussed as a unit.

The –50-V Rectifier assembly CR812 rectifies the output at the secondary of T801 to provide the unregulated voltage source for this supply. CR812 is connected as a bridge rectifier and its output voltage is filtered by C812 before it is applied to the –50-V Series Regulator Q837. Integrated circuit U820 and transistors Q823, Q833 and Q837 operate as a feedback-stabilized regulator circuit to maintain a constant –50-volt output level. U820 is connected as a differential amplifier (see Fig. 3-34A) to compare the feedback signal at pin 1 against the reference signal at pin 5. The error output signal at pin 6 reflects the difference, if any, between the two inputs. The change in level at the error output is always in the same direction as the change at the feedback input (in phase). Q3 provides a constant current to Q1-Q2 as established by R1-R2 and the operating potentials connected to pins 3, 4 and 7. Pin 8 is connected to a V_{CC} supply voltage to provide the correct operating potential for Q1.

Zener diode VR814 sets a reference level of about –6.2 volts at pin 5 of U820. A sample of the output voltage from this supply is connected to the feedback input (pin 1) through divider R813-R815-R811. R815 in this divider is adjustable to set the output voltage level of this supply. Notice that the feedback voltage to this divider is obtained from a line labeled –50 V Sense. Fig. 3-35 illustrates the reason for this configuration. The inherent resistance of the interconnecting wire between the output of the –50-Volt Supply and the load produces a voltage drop which is equal to the output current multiplied by the resistance of the interconnecting wire. Even though the resistance of the wire is small, it results in a substantial voltage drop due to the high output current of this supply. Therefore, if the feedback voltage were obtained ahead of this drop, the voltage at the load might not maintain close regulation. However, the –50 V Sense configuration overcomes this problem since it obtains the feedback voltage from a point as close as practical to the load. Since the current in the –50 V Sense line is quite small, the feedback voltage is an accurate sample of the voltage applied to the load.

Regulation occurs as follows: If the output level of this supply decreases (less negative) due to ripple, changes in load, or changes in line voltage, the voltage across divider R813-R815-R811 decreases also. This results in a more positive level at the feedback input of U820 than at the reference input and the output current decreases. This decrease in output current from U820 allows more base current to flow through Q823 and Q833 to result in increased conduction of the –50-V Series Regulator Q837. This action increases the load current and the output voltage of this supply increases (more negative). The feedback voltage from the –50 V Sense line increases and the feedback input of U820 returns to the same level as the reference input. Similarly, if the output level of this supply increases (more negative), the output current of U820 increases. The feedback through Q823 and Q833 reduces the conduction of the –50-V Series Regulator to decrease the output voltage of this supply.

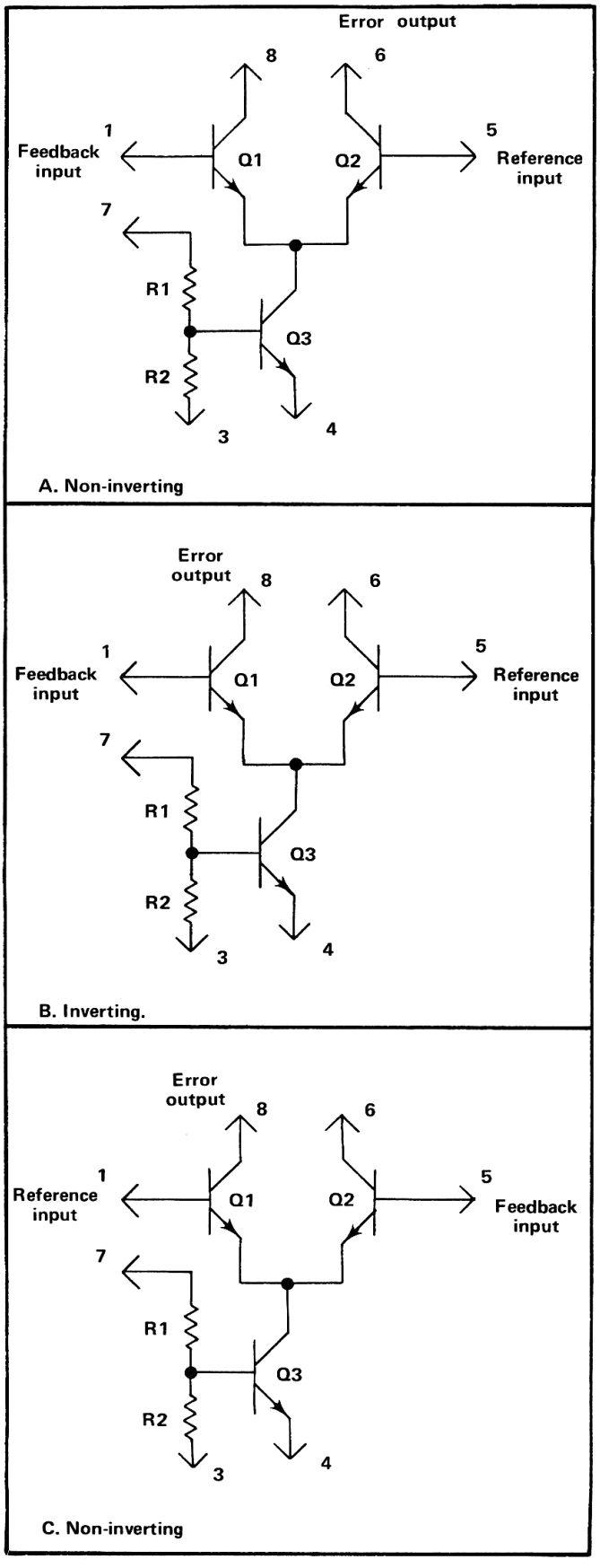


Fig. 3-34. Simplified schematics of RCA CA3028A in configurations used in the Type 7504.

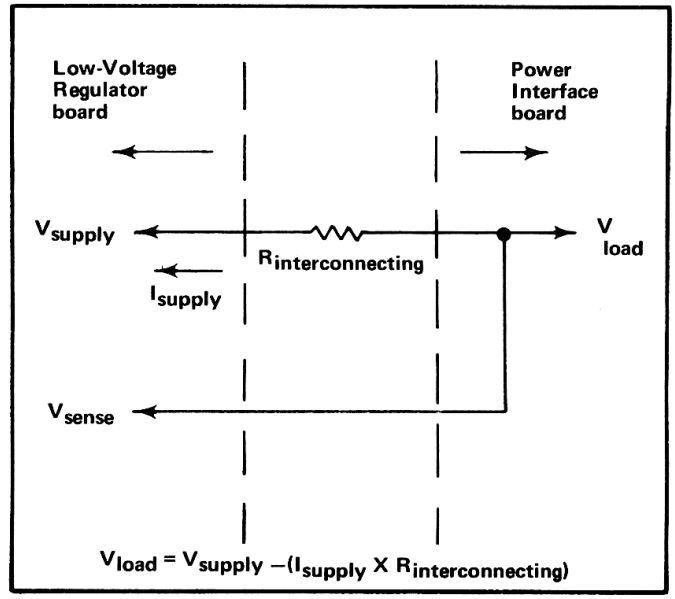


Fig. 3-35. Schematic illustrating voltage drop between power-supply output and load due to resistance of interconnecting wire.

The −50 Volts adjustment R815 determines the divider ratio to the error input of U820 and thereby determines the feedback voltage. This adjustment sets the output level of the supply in the following manner: if R815 is adjusted so the voltage at its variable arm goes less negative (closer to ground), this appears as an error signal at pin 1 of U820. In the same manner as described previously, this positive-going change at the feedback input of U820 increases the conduction of the −50-V Series Regulator to produce more current through the load and thereby increase the output voltage of this supply. This places more voltage across divider R813-R815-R811 and the divider action returns the feedback input of U820 to about −6.2 volts. Notice that the feedback action of this supply forces a change in the output level which always returns the feedback input of U820 to the same level as the reference input. In this manner, the output level of the −50-Volt Supply can be set to exactly −50 volts by correct adjustment of R815.

The −50-V Current Limiting stage Q824 protects the −50-Volt Supply if excess current is demanded from this supply. Since the ground return for the −50-Volt Supply is through R837, all current from the −50-Volt Supply must flow through R837. Transistor Q824 senses the voltage drop across R837. Under normal operation, there is about 0.25-volt drop across R837 which is not sufficient to forward bias Q824. However, when excess current is demanded from the −50-V Series Regulator due to a short circuit or similar malfunction at the output of this supply, the voltage drop across R847 increases until it is sufficient to forward bias Q824. The collector current of Q824 results in a reduction of current through Q823 and Q833 to limit the conduction of Q837. As the output voltage decreases due to the malfunction at the output, the bias established at the base of Q824 by divider R827-R829 increases. This

increases the conduction of Q824 to further limit the current through Q837. The current limiting protects Q837 from damage due to excess power dissipation. Several protection diodes are also included in this circuit. CR818 protects U820 by preventing pin 1 from going more than about 0.6 volt more positive than pin 5. CR832 prevents the base of Q833 from going more positive than about +0.85 volt. CR838 protects the −50-Volt Supply from damage if its output is shorted to one of the positive supplies. C824-R824 prevent oscillation in the feedback network.

−15-Volt Supply

Rectified voltage for operation of the −15-Volt Supply is provided by rectifier assembly CR842. This voltage is filtered by C842 to provide the unregulated voltage source for this supply. Basic operation of all stages in the −15-Volt Supply except the −15-V Feedback Amplifier is the same as for the −50-Volt Supply. Reference level for this supply is established by the ground connection at the reference input (pin 1) of U845. This is the same integrated circuit type as used in the −15-V Feedback Amplifier and the operation and function are the same. Feedback voltage to pin 5 of U845 is provided by divider R843-R844 between the −15-V Sense line and the +15-V Sense line. The divider ratio of R843-R844 is 1 to 1 and precision resistors are used so that the output level of this supply is −15 volts when the error input of U845 is near zero volts as controlled by the feedback. The level on the +15-V Sense line is held stable by the +15-Volt Supply. Any change at the output of the −15-Volt Supply appears at pin 1 of U845 as an error signal. The output voltage is regulated in the same manner as described for the −50-Volt Supply. Diode CR844 protects U845 by preventing pin 1 from going more than about 0.6 volt more positive than pin 5 (ground). CR848 prevents the base of Q854 from going more positive than about +5.6 volts.

+5-Volt Supply

Bridge rectifier CR870-CR871-CR872-CR873 provides the rectified voltage for the +5-Volt Supply. This unregulated voltage is also connected to the Control Illumination Network on the Front-Panel Controls and Cabling diagram to provide power to the front-panel indicator bulbs of this instrument as well as the associated plug-in units. The +5-V Series Regulator Q897 operates the same as the series regulators in the negative supplies except that it is connected in the negative side of the supply. The +5-V Feedback Amplifier U894 is connected in the inverting configuration (see Fig. 3-34B). In this configuration, the change at the error output (pin 8) is out of phase with the feedback signal at pin 1. A ground reference level is provided at pin 5 and the feedback voltage is connected to pin 1. Regulation occurs as follows: If the output of this supply goes more positive, the positve change at the feedback input of U894 results in an increase in output current at pin 8. This reduces the base current to Q883 and a resultant reduction of base current for Q886 and the +5-V Series Regulator Q897. The decreased base current for Q897 reduces the output current of this supply to decrease the voltage across the load. Zener diode VR882 provides voltage shifting between Q883 and Q886 without appreciable current loss, while CR886 provides reverse-bias protection for Q886.

The ground return for the +5-V Series Regulator is through current-sensing resistor R897. In the same manner as described for the previous supplies, the normal current through R897 is not sufficient to forward bias the +5-V Current Limiting stage Q888. However, when excess current is demanded from this supply, the voltage drop across R897 increases and Q888 is forward biased. The collector current of Q888 flows through R878 to decrease the voltage level at the anode of CR878. When this voltage drops to about +11 volts, CR878 and Q878 are reverse biased to reduce the conduction of Q883, Q886 and the +5-V Series Regulator Q897 which provides current limiting.

The +5-V Voltage Limiting stage provides protection for the light bulbs and integrated circuits which are powered from this supply if the output voltage rises above the normal five-volt level. The +5-volt output of this supply is connected across zener diode VR875 through R875. Under normal conditions, there is not enough voltage across VR875 to place it in the zener region. However, if the output of this supply rises positive due to a short to a more positive supply, or similar malfunction, the gate of Q874 (programmable unijunction transistor) is clamped at about +5.6 volts through R874 by zener diode VR875. As the output voltage increases to about +6 volts, Q874 is forward biased and its cathode current triggers silicon-controlled rectifier Q872 through R872. When Q872 conducts, it effectively shorts the output of the +5-V Supply to ground, demanding high output current. This high current is sensed by the +5-V Current Limiting stage and the output current is reduced as described previously. The output remains limited until the instrument is turned off and the problem is corrected. A momentary voltage surge may also trigger the +5-V Voltage Limiting stage and cause the +5-Volt Supply to shut down. Power can be restored in this case by momentarily turning off the POWER switch and returning it to ON.

Fuse F872 provides further current protection for this supply. If the +5-V Current Limiting stage malfunctions (for example, collector of +5-V Series Regulator shorted to ground) and a condition occurs which demands current limiting, F872 opens to interrupt the output of this supply before damage can occur. Diode CR893 provides protection for U894 by providing an alternate current path from the −15-Volt Supply if the −50-Volt Supply fails. CR898 protects this circuit if the output is shorted to one of the negative supplies. Due to the high current output of this supply, a separate ground return is used for this supply to

prevent its heavy return current from affecting other supplies in this instrument.

The elapsed-time meter M898 is connected to the +5-volt output through R898. This meter records the amount of time that this instrument has been operating; full-scale reading is 5000 hours.

+15-Volt Supply

Rectifier assembly CR902 provides the rectified voltage for the +15-Volt Supply. This unregulated voltage is also connected to the High-Voltage Oscillator stage in the CRT Circuit through F901. This fuse protects the +15-V Rectifier from damage due to failures in the High-Voltage Oscillator stage. Basic operation of the stages in this circuit are the same as described for the previous supplies. Diode CR904 prevents the junction of R904-R905 from going more positive than about −14.4 volts to protect Q910. CR906 normally clamps the emitter of Q904 at about +5.5 volts. However, when the +15-V Current Limiting stage comes into operation it disconnects the +5-Volt Supply at its cathode so the base of Q904 can be pulled negative to limit the output current of this supply. CR910 protects Q910-Q913 by limiting the reverse bias across them to about 0.6 volt. CR915 limits the positive level at the base of Q904 to about +5.6 volts if the output of this supply is shorted to one of the more positive supplies.

+50-Volt Supply

Bridge rectifier assembly CR932 provides the rectified voltage for the +50-Volt Supply. This unregulated voltage is applied across zener diode VR953 through R953 to provide a +10-volt source for operation of several circuits within the Low-Voltage Power Supply circuit. The unregulated voltage from CR932 is also the collector source for the +50-V Series Regulator. Regulation occurs much the same as described for the previous supplies. Notice that the reference level is connected to pin 1 and the feedback signal to pin 5 of U944. However, since the output is obtained from pin 8 (see Fig. 3-34C), the circuit is a non-inverting differential amplifier as described for the −50-Volt Supply. Feedback from U944 controls the conduction of the +50-V Series Regulator Q953 through Q936 and Q943. The +75-volt unregulated voltage provides the collector current for Q943 through R944. Diode CR944 forces the collector of Q943 to always be about 0.6 volts more positive than the collector of Q953. The +50-V Current Limiting stage Q934 senses the voltage drop across R931 to provide protection for this supply if excess current is demanded.

+75-Volt Supply

Unregulated +75-volts is provided by bridge rectifier assembly CR962 and filtered by C962-R962. Q973 is connected as a series regulator with R973 connected across Q973 to reduce its dissipation. Regulation is achieved as follows: Q963 and Q968 provide feedback from the +75-volt output to the +75-V Series Regulator. The ground connection at the emitter of Q968 provides a reference for this stage. The base level of Q963 is determined by divider R963-R965 between the −50-V Sense line and the output of this supply. Since the −50-V Sense line is held constant, any change that appears at the base of Q963 is due to changes in the +75-volt output level. To follow the regulation, assume that the output goes more positive. This appears as an error signal at the base of Q963 and in turn at the base of Q968. Q968 is forward biased, which results in a reduction of bias on the +75-V Series Regulator Q973. The current through Q973 is reduced, to supply less current through the load to correct the original error. Only a portion of the output current flows through Q973 and the degree of regulation this configuration can achieve is limited to the amount of current that Q973 controls. However, this stage provides adequate regulation for the circuits where the +75-volt level is used and allows a lower wattage-rating transistor to be used in the regulator circuit. The +75-V Current Limiting stage Q974 senses the voltage drop across R974 to protect Q973 from damage due to excess current. Normally, the current through R974 is insufficient to forward bias Q974. However, when excess current is demanded from this supply, Q974 is forward biased and the addition of the Q974 current in the base circuit of the +75-V Shunt Regulator limits the conduction of Q973 to a level which protects it from damage. Diode CR963 limits the base excursion of Q963 to about −0.6 volt if the output of this supply is interrupted. CR969 protects Q973 if Q968 fails.

+150-Volt Supply

Bridge rectifier assembly CR982 provides the rectified voltage for the +150-Volt Supply. However, this secondary winding of T801 does not supply the full potential necessary to obtain the +150-volt output level. To provide the required output level, the negative side of this supply is connected to the output of the +75-Volt Supply so that the two supplies are effectively connected in series between ground and the +150-volt output. +150-V Feedback Amplifier Q984 and +150-V Series Regulator Q994 provide basic regulation for the output level in a manner similar to that described for the +75-Volt Supply. Changes in the output level appear as an error signal at the base of Q984 (reference established by ground connection at emitter). These changes are reflected to the base of Q994 to provide regulation of the output level. Fuse F982 protects this supply if the output is shorted. However, since the response time of F982 is slow to a shorted condition, CR992 is provided to protect Q994 from breakdown until F982 opens. Diodes CR984 and CR994 limit the reverse bias on Q984 and Q994 respectively to about 0.6 volts if the output of this supply is shorted.

6.3-Volt RMS AC Source

The 6.3-volt RMS secondary winding of T801 provides power for the graticule illumination lights DS807, DS808

and DS809. The current through these lights is determined by the GRAT ILLUM control R809 to change the illumination of the graticule lines. Voltage divider R807-R808 provides a sample of the line voltage to the plug-in connectors in the Main Interface circuit for internal triggering at line frequency or for other applications.

FRONT-PANEL CONTROLS AND CABLING

General

Diagram 12 shows the front-panel controls of the Type 7504 and the interconnections between these controls and the circuit boards, as well as interconnections between the circuit boards within this instrument. To use the cabling diagram, note the number on the wire at the point where an individual wire joins the cable. Then follow the cable around until a break-out is found with the same number. This will be the source/location of the desired wire.

Switch Logic

The VERTICAL MODE and HORIZONTAL MODE switches determine the operating mode of the Vertical Interface and Horizontal Interface circuits respectively. Each of these switches is designed so that it is self-canceling; (i.e., only one button can be pressed at a time). Specific operation of these switches is described in connection with the circuits that they control.

The A TRIGGER SOURCE and B TRIGGER SOURCE switches control the operation of the Trigger Selector circuit. These switches are also self-canceling so that only one of the buttons can be pressed at a time. Operation of these switches is discussed in connection with the Trigger Selector circuit.

Indicator Lights

The indicator light shown in connection with the VERTICAL MODE and HORIZONTAL MODE switches indicate which mode has been selected. When one of the buttons of these switches is pressed, it completes the circuit between the associated bulb and the lamp-common line. Notice that a separate bulb is used for each mode switch position. Bulbs DS1035 and DS1037, located by the B INTENSITY and A INTENSITY controls respectively, are actuated by the HORIZONTAL MODE switch to indicate which of the intensity controls is active for the selected horizontal mode. The selected button of the A TRIGGER SOURCE and B TRIGGER SOURCE switches is also illuminated to indicate the trigger source. Notice that only one bulb is associated with each of the trigger source switches. The source switches are mechanically designed so that the button which is pressed receives light from the bulb, but the remaining buttons remain un-illuminated.

The CONTROL ILLUM switch S1040B determines the illumination level of the pushbutton switches on the Type 7504 and the associated plug-in units. In the HIGH position of this switch, the lamp power from the Low-Voltage Power Supply circuit is connected directly to the light bulbs. In the LOW position, the lamp power is connected to the bulbs through diodes CR1040 and CR1041. The forward drop across these diodes reduces the current available to the bulbs so that they operate at a lower intensity level. In the OFF position, the lamp power to all of the pushbutton switches is disconnected. However, lamp power is still provided to the bulbs associated with the A and B INTENSITY controls through CR1040 and CR1041 to provide an indication that the POWER switch is ON.

READOUT SYSTEM

Introduction to Readout System

General. The Readout System in the Type 7504 provides alpha-numeric display of information encoded by the plug-in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis with the analog waveform display. Schematics for the total Readout System are shown on diagrams 13, 14 and 15 at the rear of this manual.

The definitions of several terms must be clearly understood to follow this description of the Readout System. These are:

Character—A character is a single number, letter, or symbol which is displayed on the CRT, either alone or in combination with other characters.

Word—A word is made up of a related group of characters. In the Type 7504 Readout System, a word can consist of up to ten characters.

Frame—A frame is a display of all words for a given operating mode and plug-in combination. Up to eight words can be displayed in one frame. Fig. 3-36 shows one complete frame and the position at which each of the eight words is displayed.

Column—One of the vertical lines in the Character Selection Matrix (see Fig. 3-37). Columns C-0 (column zero) to C-10 (column 10) can be addressed in the Type 7504 system.

Row—One of the horizontal lines in the Character Selection Matrix (Fig. 3-37). Rows R-1 (row 1) to R-10 (row 10) can be addressed in the Type 7504 system.

Time-slot—A location in a pulse train. In the Type 7504 Readout System, the pulse train consists of 10 negative-going pulses. Each of these time-slots is assigned a number between one and ten. For example, the first time-slot is TS-1.

Time-multiplexing—Transmission of data from two or more sources over a common path by using different time intervals for different signals.

Display Format. Up to eight words of readout information can be displayed on the Type 7504 CRT. The position of each word is fixed and is directly related to the plug-in unit from which it originated. Fig. 3-36 shows the area of the graticule where the readout from each plug-in unit is displayed. Notice that channel 1 of each plug-in unit is displayed within the top division of the CRT and channel 2 is displayed directly below within the bottom division. Fig. 3-38 shows a typical display where only channel 1 of the Right Vertical unit and the B Horizontal unit are selected for display.

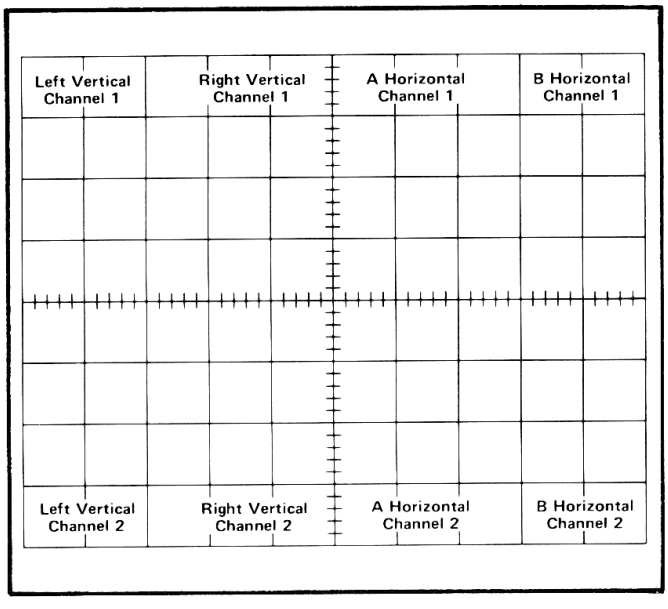


Fig. 3-36. Location of readout words on the CRT identifying the originating plug-in and channel (one complete frame shown).

Each word in the readout display can contain up to 10 characters, although the typical display will contain between two and seven characters per word. The characters are selected from the Character Selection Matrix shown in Fig. 3-37. Any one of the 50 separate characters can be addressed and displayed on the CRT. In addition, 12 operational addresses are provided for special instructions to the Readout System. The unused locations in the Matrix (shaded areas) are available for future expansion of the Readout System. The method of addressing the locations in the Character Selection Matrix is described in the following discussion.

Developing the Display. The following basic description of the Readout System uses the block diagram shown in Fig. 3-39. This description is intended to basically relate the function of each stage to the operation of the overall Readout System. Detailed information on circuit operation will be given later.

The key block in the Readout System is the Timer stage. This stage produces the basic signals which establish the timing sequences within the Readout System. Period of the timing signal is about 250 microseconds (drops to about 210 microseconds when Display-Skip is received; see detailed description of Timing stage for further information). This stage also produces control signals for other stages within this circuit and interrupt signals to the Vertical Interface and Horizontal Interface circuits, CRT Circuit and Z-Axis Logic stage which allow a readout display to be presented. The Time-Slot Counter stage receives a trapezoidal voltage signal from the Timer stage and directs it to one of ten output lines. These output lines are labeled TS-1 through TS-10 (time-slots one through ten) and are connected to the vertical and horizontal plug-in compartments as well as to various stages within the Readout System. The output lines are energized sequentially so that there is a pulse on only one of the 10 lines during any 250 microsecond timing period. When the Time-Slot Counter stage has completed time-slot 10, it produces an End-of-Word pulse which advances the system to the next channel.

Two output lines, row and column, are connected from each channel back to the Readout System. Data is typically encoded on these output lines by connecting resistors between them and the time-slot input lines. The resultant output is a sequence of ten analog current levels which range from zero to one milliampere (100 microamperes/step) on the row and column output lines. This row and column correspond to the row and column of the Character Selection Matrix in Fig. 3-37. The standard format in which information is encoded onto the output lines is given in Table 3-2 (special purpose plug-in units may have their own format for readout; these special formats will be defined in the manuals for these units);

Row Number \ Column Number →	Current (Milli-amperes)	C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	⩾1.0
R-1	0	SKIP*	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*
R-2	0.1		↯	<	*I*	/	+	–	+	*C*	Δ	>
R-3	0.2		Add* one zero	Add* two zeros	Reduce* prefix	Reduce* prefix and add one zero						*IDENTIFY**
R-4	0.3		*m*	*μ*	*n*	*p*	*X*	*K*	*M*	*G*	*T*	*R*
R-5	0.4		*S*	*V*	*A*	*W*	*H*	*d*	*B*	*c*	Ω	*E*
R-6	0.5		*U*	*N*	*L*	*Z*	*Y*	*P*	*F*	*J*	*Q*	*D*
R-7	0.6				Decimal* point location #3	Decimal* point location #4	Decimal* point location #5	Decimal* point location #6	Decimal* point location #7			
R-8	0.7											
R-9	0.8											
R-10	0.9	Add Space In Display*										

Unused locations. Available for future expansion of Readout System

Operational address.

Fig. 3-37. Character Selection Matrix for Type 7504 Readout System.

TABLE 3-2

Standard Readout Format

Time-Slot Number	Description
TS-1	Determines decimal magnitude (number of zeros displayed or prefix change information) or the IDENTIFY function (no display during this time-slot).
TS-2	Indicates normal or inverted input (no display for normal).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control (no display for calibrated condition).
TS-4	1-2-5 scaling.
TS-5 TS-6 TS-7	Not encoded by plug-in unit. Left blank to allow addition of zeros by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Define the units of measurement of the plug-in unit. May be standard units of measurement (V, A, S, etc.) or special units selected from the Character Selection Matrix.

The encoded column and row data from the plug-in units is selected by the Column Data Switch and Row Data Switch stages respectively. These stages take the analog currents from the eight data lines (two channels from each of the four plug-in compartments) and produce a single time-multiplexed analog voltage output which contains all of the column or row information from the plug-ins. The Column Data Switch and Row Data Switch are sequenced by a binary code from the Channel Counter.

The time multiplexed output of the Column Data Switch is monitored by the Display-Skip Generator to determine if it represents valid information which should be displayed. Whenever information is not encoded in a time-slot, the Display-Skip Generator produces an output level to prevent the Timer stage from producing the control signals which normally interrupt the CRT display and present a character.

The analog output of the Column Data Switch and Row Data Switch are connected to the Column Decoder and Row Decoder stages respectively. These stages sense the magnitude of the analog voltage input and produce an output current on one of ten lines. The outputs of the Column Decoder stage are identified as C-1 to C-10 (column 1 to 10) which correspond to the column information encoded by the plug-in unit. Likewise, the outputs of the Row Decoder stage are identified as R-1 to R-10 (row 1 to 10) which correspond to the row information encoded by the plug-in unit. The primary function of the row and column outputs is to select a character to be produced from the Character Selection Matrix by the Character Generator stage. However, these outputs are also used at other points within the system to indicate when certain information has been encoded. One such stage is in the Zeros Logic and Memory. During time-slot 1 (TS-1), this stage checks if zero-adding or prefix-shifting information has been encoded by the plug-in unit and stores it in memory until time-slots 5, 6, or 8. After storing this information, it triggers the Display-Skip Generator stage so there is no display during this time slot (as defined by Standard Readout Format; see Table 3-2). When time-slots 5, 6 and 8 occur, the memory is addressed and any information stored there during time-slot 1 is transferred out and connected to the input of the Column Decoder stage to modify the analog data during the applicable time-slot.

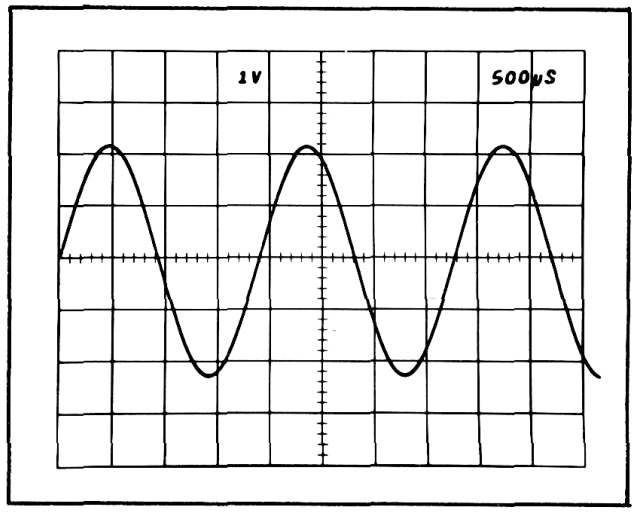


Fig. 3-38. Typical readout display where only channel 1 of the Right Vertical and B Horizontal units are displayed.

Another operation of the Zeros Logic and Memory stage is to produce the IDENTIFY function. When time-slot 1 is encoded for IDENTIFY (column 10, row 3), this stage produces an output level which connects the Column Data Switch and Row Data Switch to a coding network within the Readout System. Then, during time-slots 2 through 9, an analog current output is produced from the Column Data Switch and Row Data Switch which addresses the correct points in the Character Selection Matrix to display the word "IDENTIFY" on the CRT. The Zeros Logic and Memory stage is reset after each word by the Word Trigger pulse.

The Character Generator stage produces the characters which are displayed on the CRT. Any of the 50 characters shown on the Character Selection Matrix of Fig. 3-37 can be addressed by proper selection of the column and row

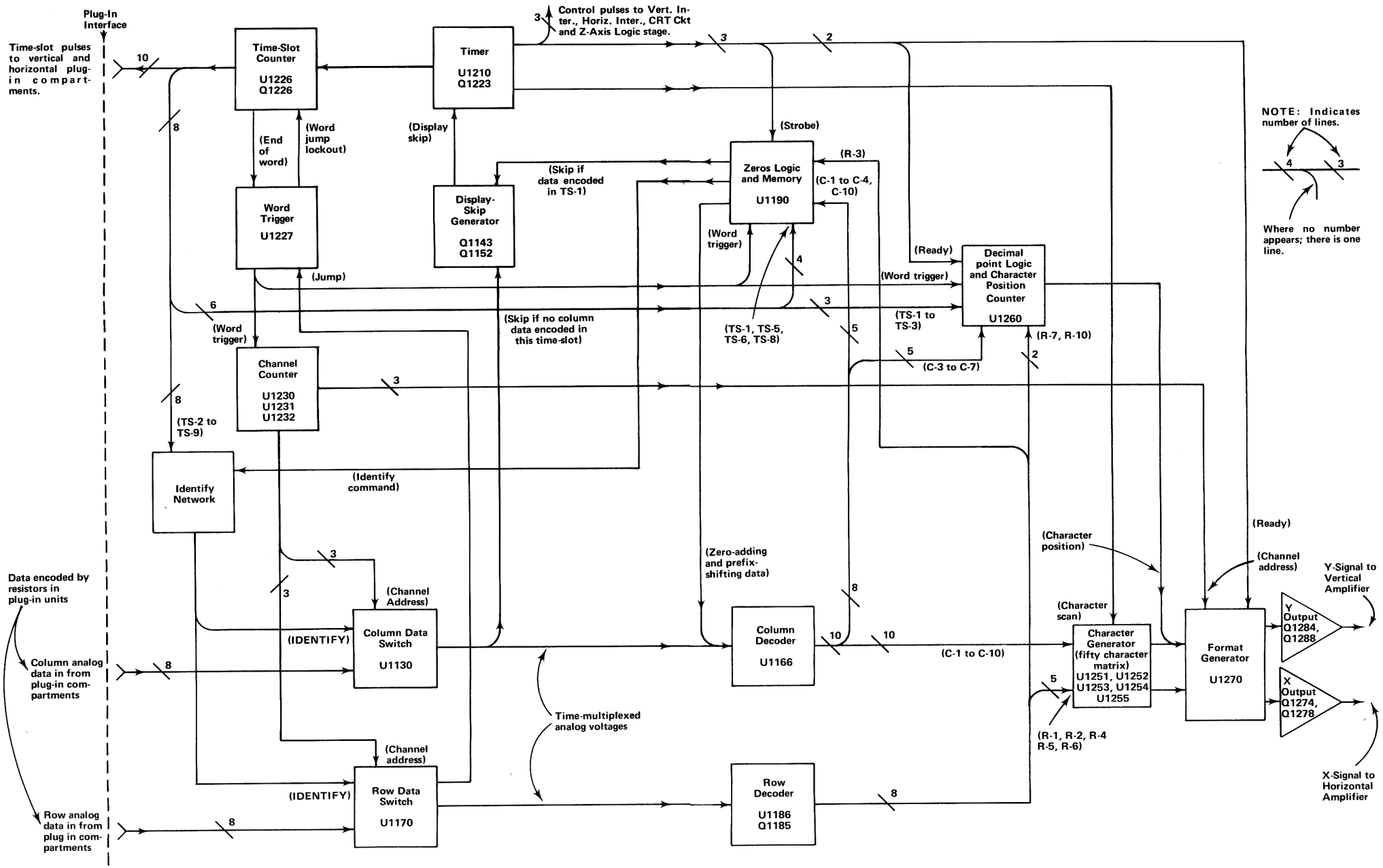


Fig. 3-39. Detailed block diagram of Readout System.

current. Only one character is addressable in any one time-slot; a space can be added into the displayed word by the Decimal Point Logic and Character Position Counter stage when encoded by the plug-in. The latter stage counts how many characters have been generated and produces an output current to step the display one character position to the right for each character. In addition, the character position is advanced once during each of time-slots 1, 2 and 3 whether a character is generated during these time-slots or not. This action fixes the starting point of the standard-format display such that the first digit of the scaling factor always starts at the same point within each word regardless of the encoded information in time-slot 2 (normal/invert) or time-slot 3 (cal/uncal) which precedes this digit. Also, by encoding row 10 and column 0 during any time-slot, a blank space can be added to the display. Decimal points can be added to the display at any time by addressing row 7 and columns 3 through 7 (see Character Selection Matrix for location of these decimal points). The Decimal Point Logic and Character Position Counter stage is reset after each word by the Word Trigger pulse.

The Format Generator stage provides the output signals to the vertical and horizontal deflection systems of the instrument to produce the character display. The binary channel address code from the Channel Counter stage is connected to this stage so that the display from each channel is positioned to the area of the CRT which is associated with the plug-in and channel originating the word (see Fig. 3-36). The positioning current or decimal point location current generated by the Decimal Point Logic and Character Position Counter stage is added to the horizontal (X) signal at the input to the Format Generator stage to provide horizontal positioning of the characters within each word. The X- and Y-output signals are connected to the Horizontal Amplifier and Vertical Amplifier through the Horizontal Output and Vertical Output stages respectively.

The Word Trigger stage produces a trigger from the End-of-Word pulse generated by the Time-Slot Counter stage after the tenth time-slot. This Word Trigger pulse advances the Channel Counter to display the information from the next channel or plug-in. It also provides a reset pulse to the Zeros Logic and Memory stage and the Decimal Point Logic and Character Position Counter stage. The Word Trigger stage can also be advanced to jump a complete word or a portion of a word when a Jump command is received from the Row Decoder stage.

Circuit Analysis of Readout System

The following analysis of the Readout System discusses the operation of each stage in detail. Complete schematics of the Readout System are shown on diagrams 13, 14 and 15 at the rear of this manual.

Timer

The Timer stage U1210 establishes the timing sequence for all circuits within the Readout System. This stage produces seven time-related output waveforms (see Fig. 3-40). The triangle waveform produced at pin 6 forms the basis for the remaining signals. The basic period of this triangle waveform is about 250 microseconds as controlled by RC network C1214-R1214. The triangle waveform is clipped and amplified by U1210 to form the trapezoidal output signal at pin 10. The amplitude of this output signal is exactly 15 volts as determined by U1210 (exact amplitude necessary to accurately encode data; see Encoding the Data). The Trigger output at pin 5 provides the switching signal for the Time-Slot Counter and Word Trigger stages.

The signals at pins 12, 13, 14 and 16 are produced only when the triangle waveform is on its negative slope and the trapezoidal waveform has reached the lower level. The timing sequence of these waveforms is very important to the correct operation of the Readout System (see expanded waveforms in Fig. 3-41). The Z-Axis Logic OFF Command at pin 14 is produced first. This negative-going signal provides a blanking pulse to the Z-Axis Logic stage (see diagram 2) to blank the CRT before the display is switched to the Readout System. It also produces the Strobe pulse through R1221, Q1223 and CR1224 to signal other stages within the Readout System to begin the sequence necessary to produce a character. The next signal to be produced is the Vertical/Horizontal Channel Switch OFF Command at pin 13. This positive-going signal disconnects the plug-in signals in the vertical and horizontal deflection systems so the plug-ins do not control the position of the CRT beam. The Ready signal derived from this output is connected to the Decimal Point Logic and Character Position Counter stage and the Format Generator stage (see diagram 15). The Readout Intensity output at pin 12 is produced next. This current is connected to the Z-Axis Intensity circuit to unblank the CRT to the level determined by the READOUT intensity control R1040 (see diagram 12). The Character Scan ramp at pin 16 started to go negative before this timing sequence began. However, character-generation does not start until the readout intensity level has been established. The triangular Character Scan ramp runs negatively from about −2 volts to about −8.5 volts and then returns back to the original level. This waveform provides the scanning signal for the Character Generator stages (see diagram 15).

The Timer stage operates in one of two modes as controlled by the Display-Skip level at pin 4. The basic mode just described is a condition which does not occur unless all ten characters of each word (80 characters total) are displayed on the CRT. Under typical conditions, only a few characters are displayed in each word. The Display-Skip level at pin 4 determines the period of the Timer output signal. When a character is to be generated, pin 4 is LO and the circuit operates as just described. However, when a character is not to be displayed, a HI level is applied to pin

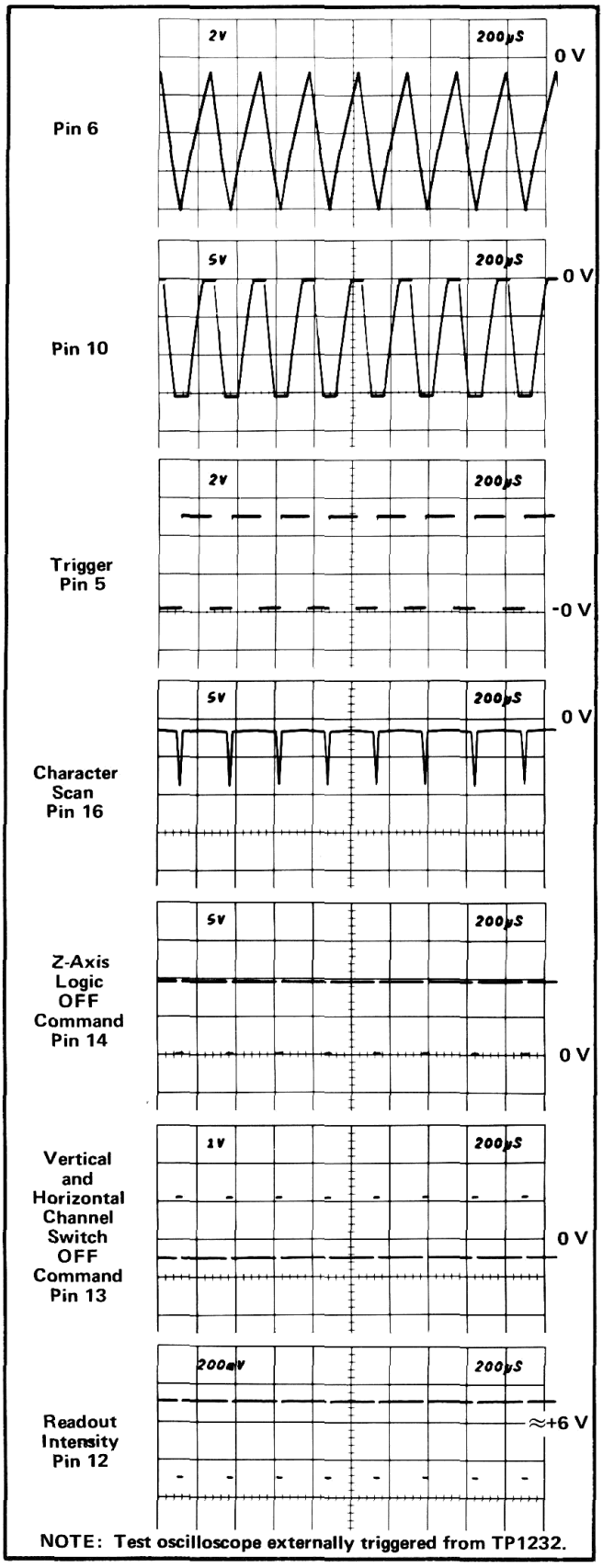


Fig. 3-40. Output waveforms of Timer stage.

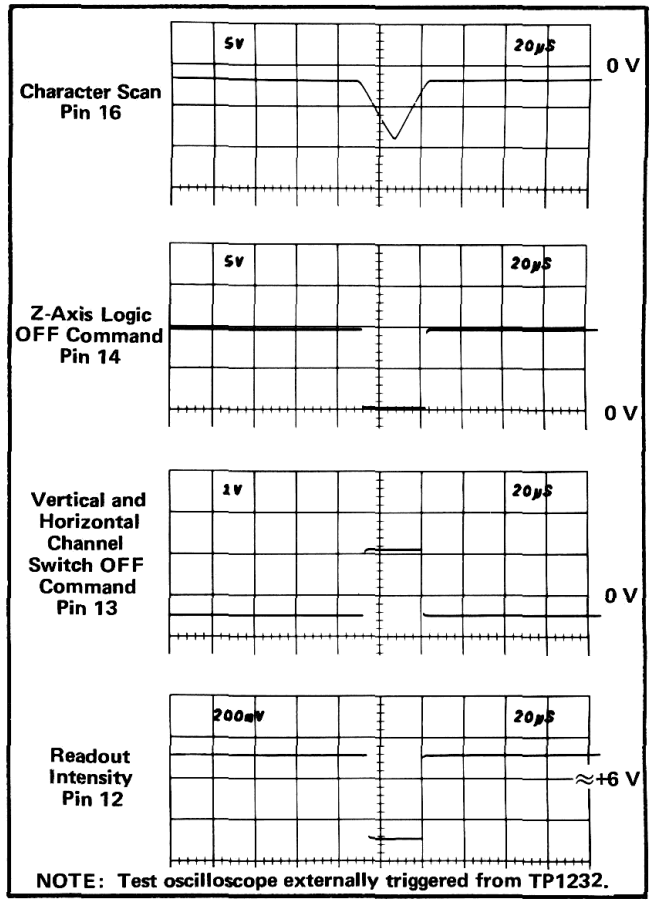


Fig. 3-41. Detail of outputs at pins 12, 13, 14 and 16 of U1210.

4 of U1210 through CR1207 from the Display-Skip Generator stage (diagram 14). This signal causes the Timer stage to shorten its period of operation to about 210 microseconds. The waveforms shown in Fig. 3-42 show the operation of the Timer stage when the Display-Skip condition occurs for all positions in a word. Notice that there is no output at pin 12, 13, 14 and 16 under this condition. This means that the CRT display is not interrupted to display characters. Also notice that the triangle waveform at pin 6 does not go as far negative and that the negative portion of the trapezoidal waveform at pin 10 is shorter. Complete details on operation of the Display-Skip Generator are given later.

The READOUT intensity control R1040 sets the intensity of the readout display independently of the A or B INTENSITY controls. The READOUT intensity control also provides a means of turning the Readout System off when a readout display is not desired. When R1040 is turned fully counterclockwise, switch S1040A opens. This interrupts the current to pin 11 and at the same time allows a positive voltage to be applied to pin 4 through R1206 and CR1206. This positive voltage switches the stage to the same conditions as were present under the Display-Skip

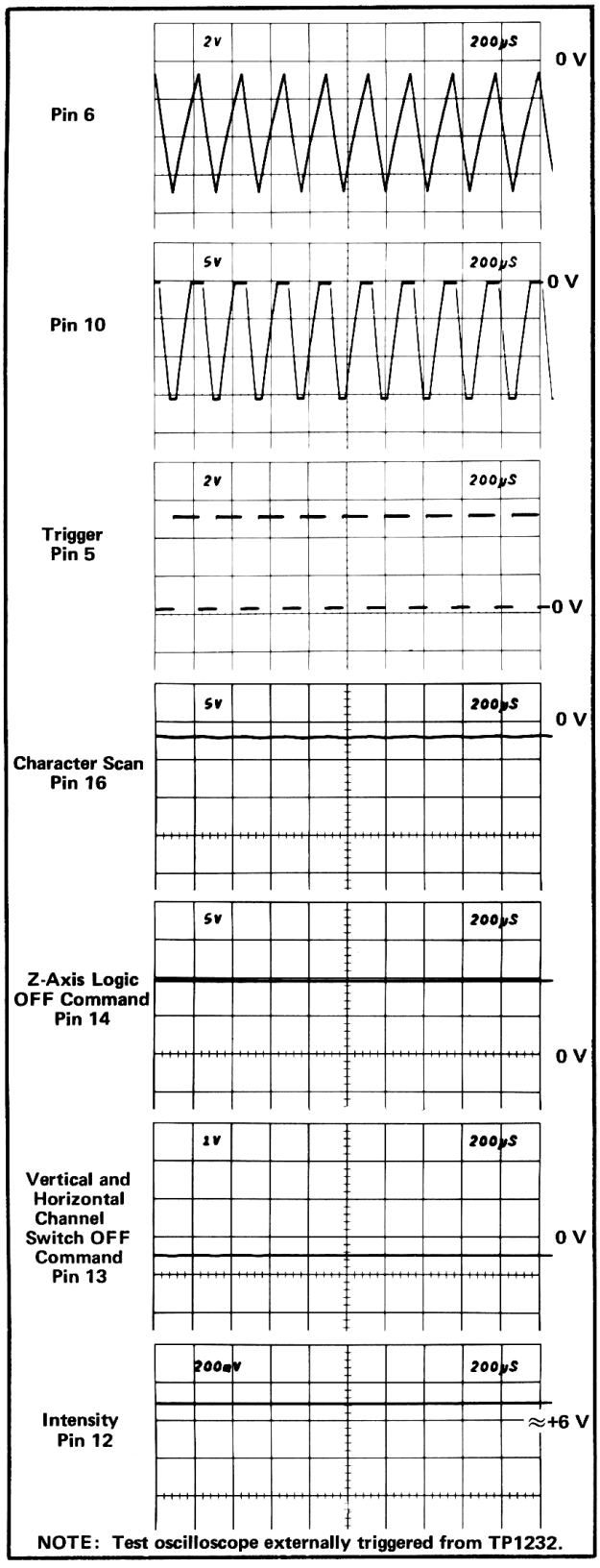


Fig. 3-42. Timer stage operation when Display-Skip condition occurs.

condition. Therefore, the CRT display is not interrupted to present characters. However, time-slot pulses continue to be generated.

Time-Slot Counter

The Time-Slot Counter stage U1226 is a sequential switch which directs the trapezoidal waveform input at pin 8 to one of its ten output lines. These time-slot pulses obtain the data for the Readout System from the plug-in units. The Trigger pulse at pin 15 switches the Time-Slot Counter to the next output line; the output signal is sequenced from time-slot 1 through time-slot 10. Fig. 3-43 shows the time-relationship of the time-slot pulses. Notice that only one of the lines carries a time-slot pulse at any given time. When time-slot 10 is completed, an End-of-Word pulse is produced at pin 2. The End-of-Word pulse provides a drive pulse for the Word Trigger stage and also provides an enabling level to the Display-Skip Generator during time-slot 1.

Pin 16 is a reset input for the Time-Slot Counter stage. When this pin is held LO, the Time-Slot Counter resets to time-slot 1. The Time-Slot Counter can be reset in this manner only when a Word Jump signal is received by U1227A (see following discussion).

Word Trigger

The Word Trigger stage is made up of 4 two-input NOR gates in U1227. The End-of-Word pulse produced by the Time-Slot Counter stage produces a HI level at pin 1 of U1227C. This level is inverted by U1227D to provide a negative-going advance pulse to the Channel Counter stage.

An output is also produced from U1227D when a Jump signal is received at pin 8 of U1227A. This condition can occur during any time-slot. U1227A and U1227B are connected as a bistable flip-flop. The positive-going Jump signal at pin 8 of U1227A produces a LO level at pin 10 (see Row Decoder for further information on origin of the Jump signal). This LO level is inverted by U1227B to produce a HI level at pin 13 which allows pin 9 of U1227A to be pulled HI through R1227. The flip-flop has now been set to its HI state where it remains until reset, even though the Jump signal at pin 8 returns to its LO level. The HI output level at pin 13 turns on Q1226 through R1226 to pull pin 16 of the Time-Slot Counter LO. This resets the Time-Slot Counter to time-slot 1 and holds it there until U1227 is reset. When the next Trigger pulse is received at pin 15, the Time-Slot Counter does not advance to the next output line (time-slot 2) but produces an output on the time-slot 1 line. A HI level is also applied to pin 4 of the Timer stage through CR1208 and CR1207. This HI level causes the Timer stage to operate in the display-skip mode so that a character is not generated.

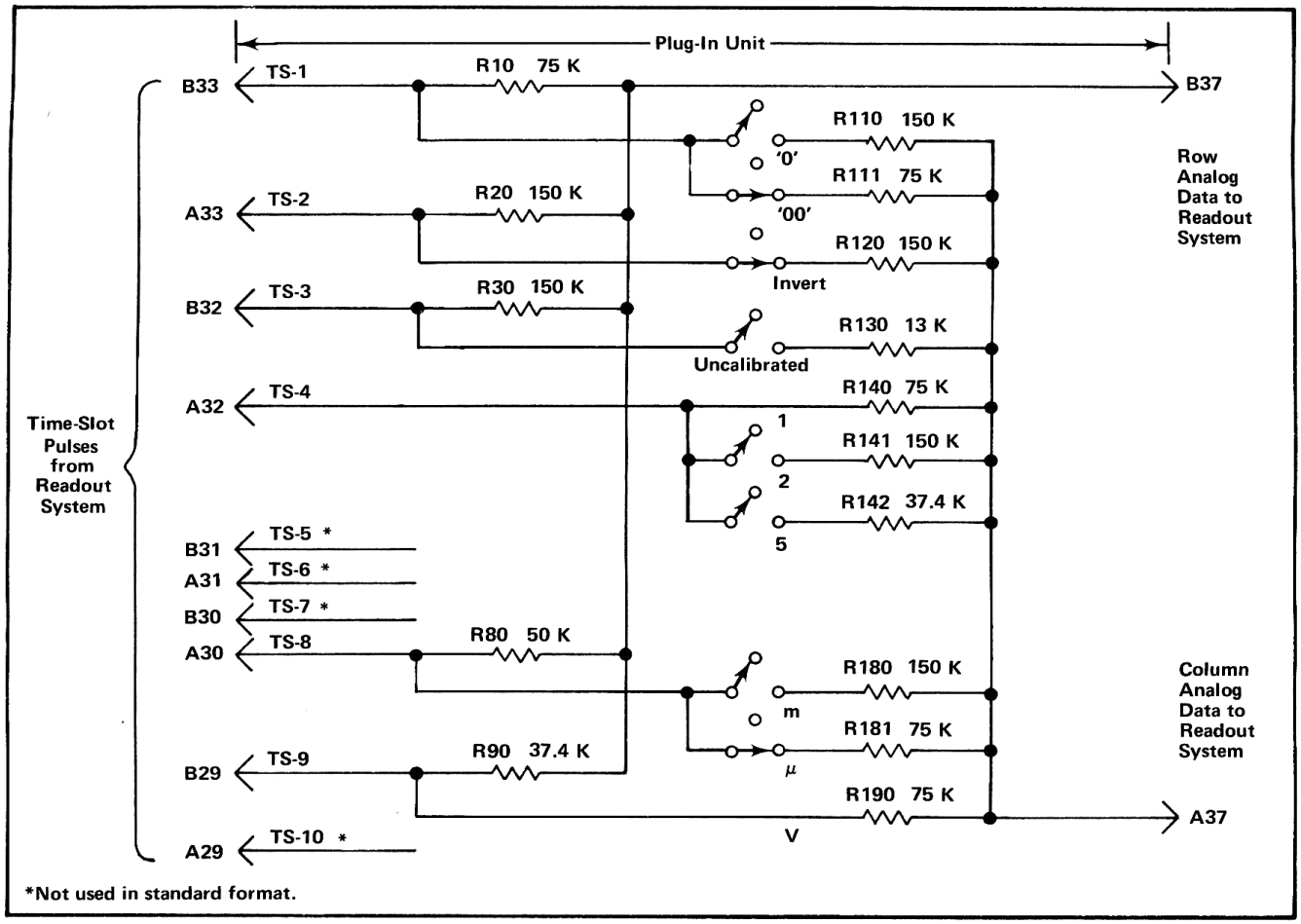


Fig. 3-44. Typical encoding scheme for voltage-sensing amplifier plug-in unit. Coding shown for deflection factor of 100 microvolts.

row analog data is connected back to the Readout System via terminal B37 of the plug-in interface.

The Column analog data is defined by resistors R110 through R190. The program resistors are connected to the time-slot lines by switch closures to encode the desired data. The data as encoded by the circuit shown in Fig. 3-44 indicates a 100 microvolt sensitivity with the display inverted and calibrated vertical deflection factors. This results in the idealized output current waveforms shown in Figure 3-45B at the column analog data output, terminal A37 of the plug-in interface. Resistor R111, connected between time-slot 1 and the column analog data output, encodes two units of current during time-slot 1. Referring to the Character Selection Matrix, two units of column current along with the two units of row current encoded by R10 (row 3) indicates that two zeros should be added to the display. Resistor R120 adds one unit of column current during time-slot 2 and along with the one unit of current from the row output, the Readout System is instructed to add an invert arrow to the display. R130 is not connected to the time-slot 3 line since the vertical deflection factors are calibrated. Therefore, there is no column current output during this time-slot and there is no display on the CRT (see Display-Skip Generator for further information). During time-slot 4, two units of column current are encoded by R140. There is no row current encoded during this time-slot and this results in the numeral 1 being displayed on the CRT. Neither row nor column analog data is encoded during time-slots 5, 6 and 7 as defined by the Standard Readout Format. During time-slot 8, two units of column current and three units of row current are encoded by resistors R181 and R80 respectively. This addresses the μ prefix in the Character Selection Matrix. The final data output is provided from time-slot 9 by R190 connected to the column output and R90 to the row output. These resistors encode three units of column current and four units of row current to cause a V (volts) to be displayed. Time-slot 10 is not encoded in accordance with the Standard Readout Format. The resultant CRT readout will be $\downarrow$ 100 μV.

In the above example, the row analog data was programmed to define which row of the Character Selection Matrix was addressed to obtain information in each time-slot. The

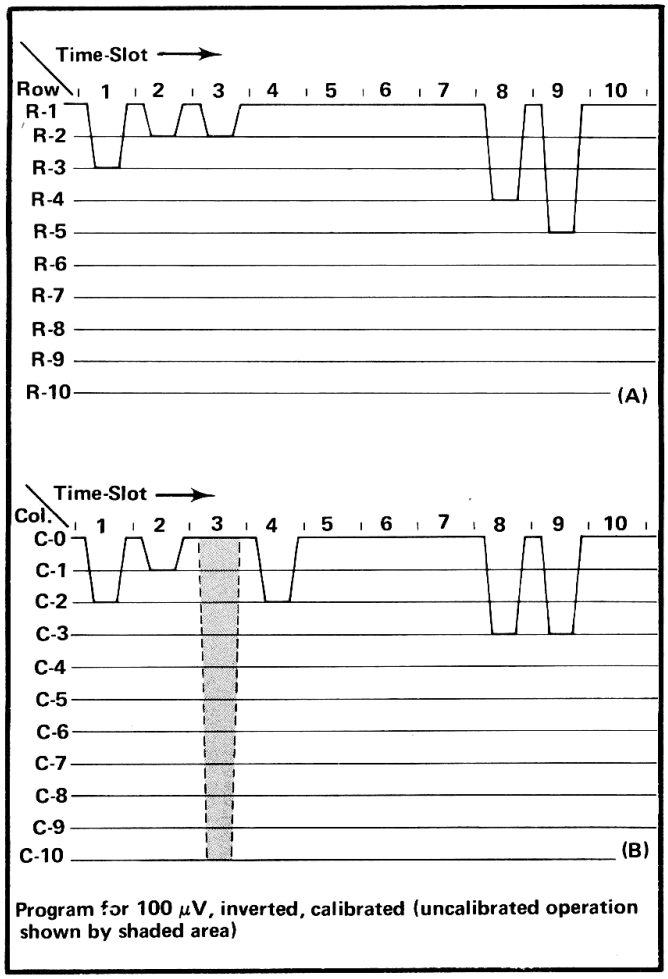


Fig. 3-45. Idealized current waveforms of: (A) Row analog data, (B) Column analog data.

column data changes to encode the applicable readout data as the operating conditions change. For example, if the variable control of the plug-in unit was activated, R130 would be connected between time-slot 3 and the column analog data output lines. This encodes 10 units of column current (see shaded area in time-slot 3 of the waveform shown in Fig. 3-45B). Since one unit of row current is also encoded during this time-slot by R30, a $>$ symbol is added to the display. The CRT readout will now say $\downarrow$ $>100\,\mu V$. In a similar manner, the other switches can change the encoded data for the column output and thereby change the readout display. For information on decoding this information, see the descriptions which follow.

The column analog data encoded by the plug-in can be modified by attenuator probes connected to the input connectors of vertical plug-in units. A special coding ring around the input connector of the plug-in unit senses the attenuation ratio of the probe (with readout-coded probes only). The probe contains a resistor which results in additional column current. For example, if a 10X attenuator probe is connected to a plug-in with the coding for 100 microvolts as shown in Fig. 3-44, an additional unit of current is added to the column analog data during time-slot 1. Since two units of current were encoded by R111 (see Fig. 3-44), this additional current results in a total of three units of column analog current during this time-slot. Referring to the Character Selection Matrix, three units of column current along with the two units of row current encoded by R10 indicates that the prefix should be reduced. Since this instruction occurs in the same time-slot which previously indicated that two zeros should be added to the display and only one instruction can be encoded during a time-slot, the zeros do not appear in the display. The CRT readout will now be reduced to 1 mV (readout program produced by plug-in same as for previous example).

Likewise, if a 100X readout-coded probe is connected to the input of the plug-in unit, the column current during time-slot 1 will be increased two units for a total of four units of column current. This addresses an instruction in the Character Selection Matrix which reduces the prefix and adds one zero to the display. The resultant CRT readout with the previous program is 10 mV.

Four other lines of information are connected from the plug-in compartments to the Readout System. The column and row analog data from channel 2 of a dual-channel plug-in are connected to the Readout System through terminals A38 and B38 of the plug-in interface, respectively. Force readout information is encoded on terminal A35 and plug-in mode information is provided on terminal B35. Function of these inputs is described under Column and Row Data Switches.

The preceding information gave a typical example of encoding data from an amplifier plug-in unit. Specific encoding data and circuitry is shown in the individual plug-in unit manuals.

Column and Row Data Switches

The readout data from the plug-in units is connected to the Column and Row Data Switch stages in the Readout System. A column-data line and a row-data line convey analog data from each of the eight data sources (two channels from each of the four plug-in compartments).

The Column Data Switch U1130 and the Row Data Switch U1170 receive the channel-address code from the Channel Counter stage. This binary code directs the Column Data Switch and the Row Data Switch as to which channel should be the source of the readout data. Table 3-3 gives the eight combinations of the channel-address code and the resultant channel which is selected with each combination. These stages have nine inputs and provide a single time-multiplexed output at pin 7 which includes the information from all of the input channels. Eight of the

nine inputs to each stage originate in the plug-in units and the ninth input comes from a special data-encoding network composed of resistors R1131 through R1138 and R1171 through R1178 (see Zeros Logic and Memory description for further information on ninth channel).

In addition to the data inputs from the plug-ins, channel-inhibit inputs are provided from each of the plug-in units. The channel inhibit lines are LO only when the associated channel has been selected for display. When a channel is not selected, the respective line is HI which forward biases the associated diode CR1112, CR1113, CR1117, CR1118, CR1122, CR1123, CR1127, or CR1128 to by-pass the encoded channel data from this plug-in. However, since it may be desired to display information from special-purpose plug-ins even though they do not produce a normal display on the CRT, a feature is provided to over-ride the channel inhibit. This is done by applying a LO input to the associated forcing over-ride input. The LO level diverts the HI channel inhibit current and allows the data from this channel to reach the Column Data switch, even though it has not been selected for display by the mode switches.

TABLE 3-3

Channel-Address Code to Column and Row Decoder Stages

Pin 1 U1190 "Identify" Command	Pin 5 U1232	Pin 5 U1231	Pin 5 U1230	Channel Selected
HI	HI	HI	HI	Channel 1 Left Vertical
HI	HI	HI	LO	Channel 2 Left Vertical
HI	HI	LO	HI	Channel 1 Right Vertical
HI	HI	LO	LO	Channel 2 Right Vertical
HI	LO	HI	HI	Channel 1 A Horizontal
HI	LO	HI	LO	Channel 2 A Horizontal
HI	LO	LO	HI	Channel 1 B Horizontal
HI	LO	LO	LO	Channel 2 B Horizontal
LO	Φ	Φ	Φ	IDENTIFY

Φ = Has no effect in this case.

Display-Skip Generator

The Display-Skip Generator stage, Q1143-Q1150-Q1152-Q1155, monitors the time-multiplexed column data at the output of the Column Data Switch during each time-slot to determine if the information at this point is valid data which should result in a CRT display. The base of Q1143B is fixed at about +14.25 volts by divider R1146-R1147-R1148. Quiescently, there is about 100 microamperes of current flowing through R1141 from Q1163 and the Zeros Logic and Memory stage (purpose of this quiescent current will be discussed in connection with the Zeros Logic and Memory stage). This current biases Q1143 so its base is about at +14.5 volts in the absence of column data. Therefore, since Q1143A and Q1143B are connected as a comparator, Q1143A will remain on unless its base is pulled more negative than about +14.25 volts. The analog data output from the Column Data Switch produces a 0.5-volt change for each unit of column current that has been encoded by the plug-in. Therefore, whenever any information appears at the output of the Column Data Switch, the base of Q1143A is pulled more negative than the base of Q1143B, resulting in a negative (LO) Display-Skip output to the Timer stage through Q1155. Recall that a LO was necessary at the skip input of the Timer stage so that the Timer stage could perform the complete sequence necessary to display a character.

Q1150-Q1152 also provide display-skip action. The End-of-Word level that is connected to their emitters through R1152 is LO only during time-slot 1. This means that these transistors are only enabled during this time-slot period. These transistors allow the Zeros Logic and Memory stage to generate a display-skip signal when information has been stored in memory which is not to be displayed on the CRT (further information given under Zeros Logic and Memory discussion).

Column and Row Decoder

The Column Decoder stage U1166 and Row Decoder stage U1186 sense the magnitude of the analog voltages at their inputs and produce a binary output on one of ten lines corresponding to the column or row data which was encoded by the plug-in. These outputs provide the Column Digital Data and Row Digital Data which is used by the Character Generator stages to select the desired character for display on the CRT. The column and row data is also used throughout the Readout System to perform other functions. The input current at pin 9 of the Column Decoder stage is steered to only one of the ten Column Digital Data outputs to determine the size of the character which will be displayed on the CRT. This size is fixed by the value of R1156. When a display-skip signal is present (collector of Q1155 HI), pin 9 is pulled HI through CR1155. This ensures that no current is connected to the Character Generator stage under this condition. Notice the corresponding input on the Row Decoder. This input is

connected to ground and causes only one of the ten row outputs to saturate to ground.

The network at the input of the Row Decoder stage made up of Q1185 and its associated components is a Row 13 detector which produces the Jump command. This row current is encoded by special-purpose plug-ins to cause all or part of a word to be jumped. Whenever row 13 (thirteen units of row current; 1.3 milliamperes) is encoded, the base of Q1185 is pulled negative enough so that this transistor saturates and produces a HI Jump output at its collector. This Jump command is connected to the Word Trigger stage (diagram 13) to advance the Channel Counter stage to the next word.

Zeros Logic and Memory

The Zeros Logic and Memory stage U1190 stores data encoded by the plug-ins to provide zeros-adding and prefix-shifting logic for the Readout System. The Strobe pulse at pin 15 goes positive when the data has stabilized and can be inspected. This activates the Zeros Logic and Memory stage so it can store the encoded data. A block representation of the memory sequence is shown in Fig. 3-46. Typical output waveforms for the five possible input conditions that can occur are shown in Fig. 3-47. When time-slot 1 occurs, a store command is given to all of the memories. If the plug-in unit encoded data for column 1, 2, 3, 4, or 10 during time-slot 1, the appropriate memory (or memories) is set. Notice that row 3 information from the Row Decoder stage must also be present at pin 16 for data to be stored in the memory of U1190. If data was encoded during time-slot 1, a negative-going output is produced at pin 7 as the memories are being set. This negative-going pulse is connected to the base of Q1152 in the Display-Skip Generator stage to produce a Display-Skip output. Since the information that was encoded during time-slot 1 was only provided to set the memories and was not intended to be displayed on the CRT at this time, the display-skip output prevents a readout display during this time-slot.

During time-slot 5, memory A is interrogated. If information was stored in this memory, a positive-going output is produced at pin 7. This pulse is connected to pin

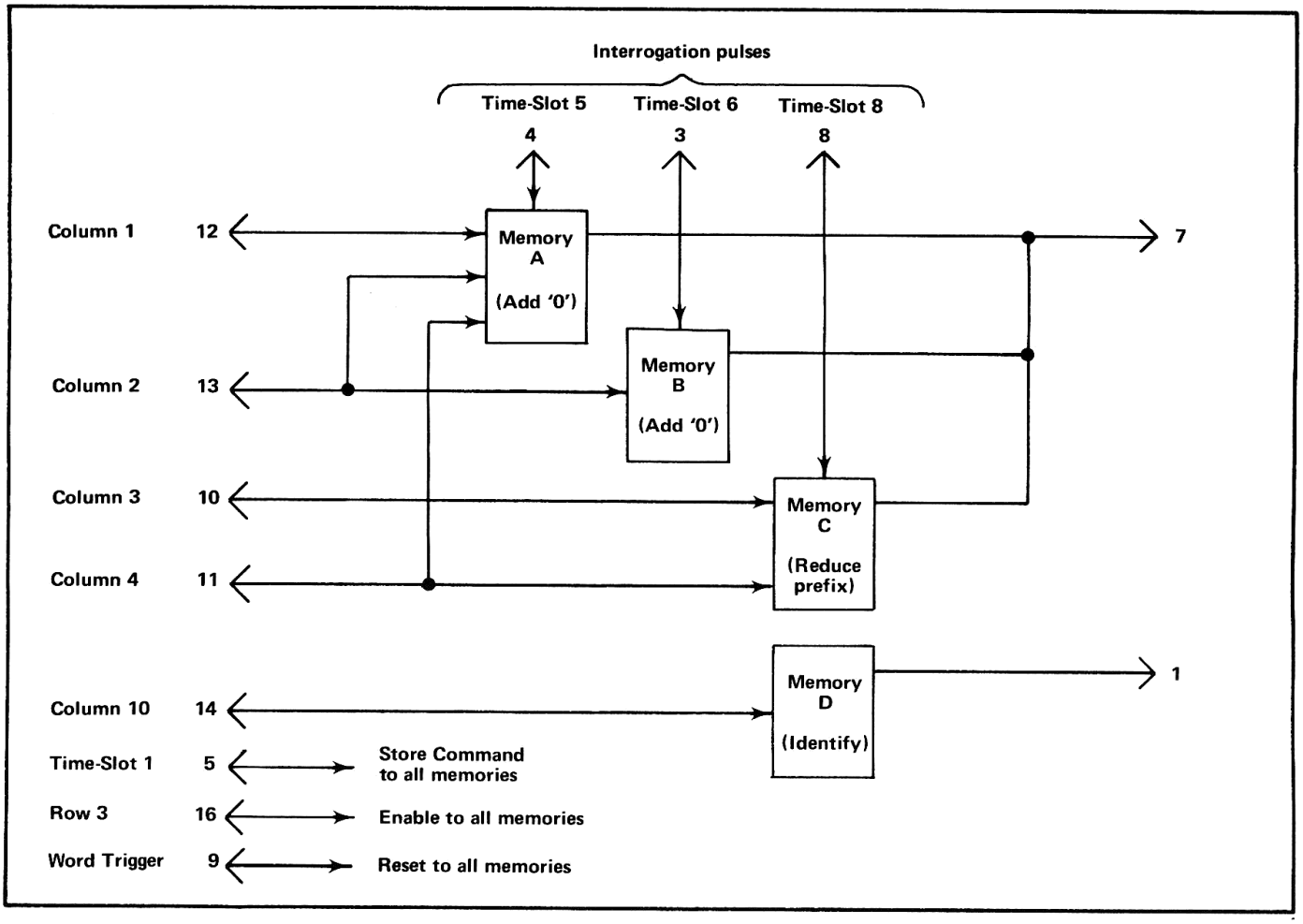


Fig. 3-46. Block representation of memory sequence in U1190.

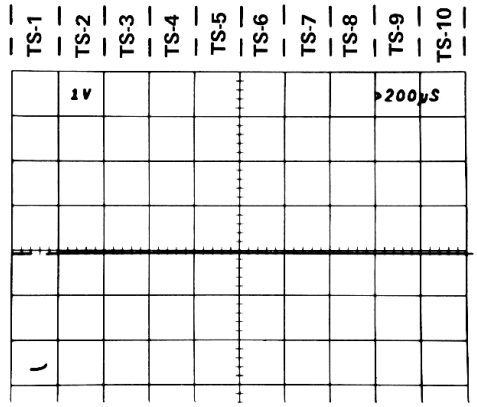
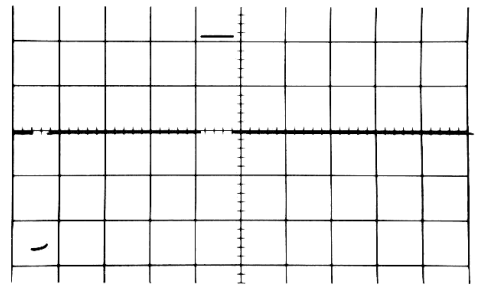
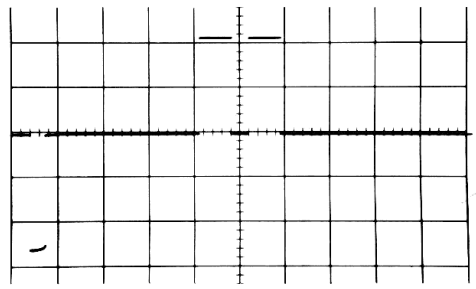
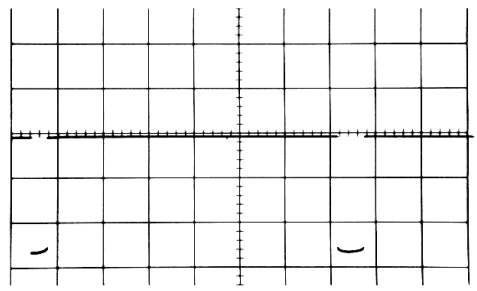
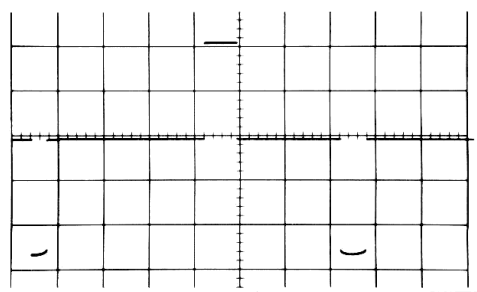
Input Pin of U1190 Activated	Command	Time-Slots
14	IDENTIFY	
12	Add one zero	
13	Add two zeros	
10	Decrease prefix	
11	Decrease prefix and add one zero	

Fig. 3-47. Typical output waveforms for Zeros Logic and Memory Stage operation (at pin 7 of U1190).

10 of the Column Decoder stage through Q1163 to add one unit of current at the input of the Column Decoder stage. This produces a zero after the character displayed on the CRT during time-slot 4. During time-slot 6, memory B is interrogated to see if another zero should be added. If another zero is necessary, a second positive output is produced at pin 7 which again results in a column 1 output from the Column Decoder stage and a second zero in the CRT display.

Finally, memory C is interrogated during time-slot 8 to obtain information on whether the prefix should be reduced or left at the value which was encoded. If data has been encoded which calls for a reduction in prefix, a negative-going output level is produced at pin 7. This negative level subtracts one unit of column current from the data at the input to the Column Decoder stage. Notice on the Character Selection Matrix of Fig. 3-37 that a reduction of one column when row 4 is programmed results in a one unit reduction of the prefix. For example, with the 100 μV program shown in Fig. 3-44, if the data received from the plug-in called for a reduction in prefix, the CRT readout would be changed to 1 mV (zeros deleted by program; see Encoding the Data).

The 100 microamperes of quiescent current through R1141 that was provided by Q1163 (see Display-Skip Generator) allows the prefix to be reduced from m (100 microamperes column current; column 1) to no prefix (zero column current; column zero) so only the unit of measurement encoded during time-slot 9 is displayed. Notice that reducing the prefix program from column 1 to column 0 programs the Readout System to not display a character at this readout location.

A further feature of the Zeros Logic and Memory stage is the Identify function. If 10 units of column current are encoded by the plug-in unit along with row 3 during time-slot 1, the Zeros Logic and Memory stage produces a negative-going output pulse at pin 1 which switches the Column Data Switch and Row Data Switch stages to the ninth channel. Then, time-slot pulses 2 through 9 encode an output current through resistors R1131-R1138 for column data and R1171-R1178 for row data. This provides the currents necessary to display the word IDENTIFY on the CRT in the word position allotted to the channel which originated the Identify command. After completion of this word, the Column Data Switch and Row Data Switch continue with the next word in the sequence.

The Word Trigger signal from the Word Trigger stage is connected to pin 9 of U1190 through C1190. At the end of each word of readout information, this pulse goes high. This erases the four memories in the Zeros Logic and Memory stage in preparation for the data to be received from the next channel.

Character Generators

The Character Generator stage consists of five similar integrated circuits U1251-U1255 which produce the X (horizontal) and Y (vertical) outputs at pins 16 and 1 respectively to produce the character displayed on the CRT. Each integrated circuit can produce 10 individual characters. For example, U1251 which is designated as the "Numerals" Character Generator can produce the numerals 0 through 9 shown in row 1 of the Character Selection Matrix (Fig. 3-37). U1252 can produce the symbols shown in row 2 of the Character Selection Matrix and U1253 produces the prefixes and some letters of the alphabet which are used as prefixes in row 4. U1254 and U1255 produce the remaining letters of the alphabet shown in rows 5 and 6 of the Character Selection Matrix. All of these stages receive the column digital data from the Column Decoder stage U1166. However, only one of the character generators receives row data at a particular time. Therefore, only the stage which receives both row and column data is enabled. For example, if column 2 is encoded by the plug-in, the five Character Generators are enabled so that either a 1, <, μ, V, or an N can be produced. However, if at the same time row 4 has also been encoded by the plug-in, only the Prefix Character Generator U1253 will produce an output to result in a μ displayed on the screen. This integrated circuit provides current outputs to the Format Generator stage which produce the selected character on the CRT. In a similar manner, any of the 50 characters shown in the Character Selection Matrix can be displayed by correct addressing of the row and column.

Decimal Point Logic and Character Position Counter

The Decimal Point Logic and Character Position Counter stage U1260 performs two functions. The first function is to produce a staircase current which is added to the X (horizontal) signal to space the characters horizontally on the CRT. After each character is generated, the negative-going edge of the Ready signal at pin 5 advances the Character Position Counter. This produces a current step output at pin 3 which, when added to the X signal, causes the next character to be produced one character space to the right. This stage can also be advanced when a Space instruction is encoded by the plug-in unit so that a space is left between the displayed characters on the CRT. Row 10 information from the Row Decoder stage is connected to pin 4 of U1260 through R1265. When row 10 and column 0 are encoded, the output of this stage advances one step to move the next character another space to the right. However, under this condition, no display is produced on the CRT during this time-slot.

Time-slot pulses 1, 2, and 3 are also connected to pin 4 of U1260 through R1260, R1261, and R1262 respectively. This configuration adds a space to the displayed word during time-slots 1, 2, and 3 even if information is not encoded for display during these time-slots. With this feature, the

information which is displayed during time-slot 4 (1-2-5 data) always starts in the fourth character position whether data has been displayed in the previous time-slots or not. Therefore, the resultant CRT display does not shift position as normal/invert or cal/uncal information is encoded by the plug-in. The Word Trigger pulse connected to pin 8 of U1260 through C1267 returns the Character Position Counter to the first character position at the end of each word.

The Decimal Point Logic portion of this stage allows decimal points to be added to the CRT display as encoded by the plug-in units. When row 7 is encoded in coincidence with columns 3 through 7 (usually encoded during time-slot 1), a decimal point is placed at one of the five locations on the CRT identified in row 7 of the Character Selection Matrix (Fig. 3-37). This instruction refers to the decimal point location in relation to the total number of characters that can be displayed on the CRT (see Fig. 3-48). For example, if column 3 and row 7 are encoded during time-slot 1, the system is instructed to place a decimal point in location #3. As shown in Fig. 3-48, this displays a decimal point before the third character that can be displayed on the CRT (first three time-slots produce a space whether data is encoded or not; see previous paragraph). The simultaneous Format Generator stage through R1269 raises the decimal point so it appears between the displayed characters.

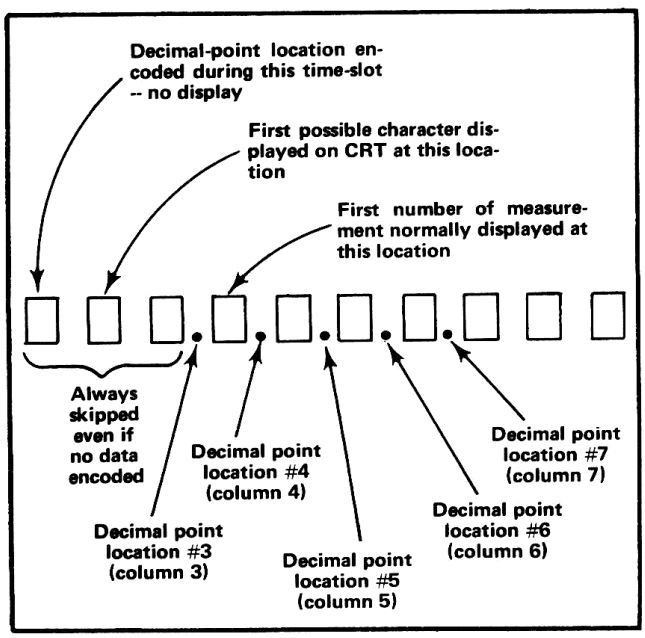


Fig. 3-48. Readout word relating 10 possible character locations to the decimal-point instructions that can be encoded, and the resultant CRT display.

When decimal-point data is encoded, the CRT is unblanked so a readout display is presented. However, since row 7 does not activate any of the five Character Generators, the CRT beam is not deflected but instead remains in a fixed position to display a decimal point between the characters along the bottom line of the readout word. After the decimal point is produced in the addressed location, the CRT beam returns to the location indicated by the Character Position Counter to produce the remainder of the display.

Format Generator

The X- and Y-deflection signals produced by the Character Generator stage, are connected to pins 2 and 7 respectively of the Format Generator stage U1270. The channel address code from the Channel Counter stage is also connected to pins 1, 8 and 15 of this stage. The channel-address code adds current to the X and Y signals to deflect the CRT beam to the area of the CRT which is associated with the plug-in channel that originated the information (see Fig. 3-36). The channel-address code and the resultant word positions are shown in Table 3-4. In addition, the character position current from the Decimal Point Logic and Character Position stage is added to the X (horizontal) input signal to space the characters horizontally on the CRT (see previous discussion). The Ready signal at pin 13 activates this stage so it can produce an output at the same time that the Timer stage produces the signal to disconnect the plug-in signals from the vertical and horizontal deflection systems.

TABLE 3-4

Channel-Address Code to Format Generator Stage

Pin 7 U1232	Pin 7 U1231	Pin 5 U1230	Channel Displayed
LO	LO	HI	Channel 1 Left Vertical
LO	LO	LO	Channel 2 Left Vertical
LO	HI	HI	Channel 1 Right Vertical
LO	HI	LO	Channel 2 Right Vertical
HI	LO	HI	Channel 1 A Horizontal
HI	LO	LO	Channel 2 A Horizontal
HI	HI	HI	Channel 1 B Horizontal
HI	HI	LO	Channel 2 B Horizontal

Y-Output Amplifier

The Y-output signal at pin 6 of U1270 is connected to the Y-Output Amplifier Q1284-Q1288. This stage provides a low impedance load for the Format Generator while providing isolation between the Readout System and the Vertical Amplifier. The Vertical Separation adjustment R1285 changes the gain of this stage to control the vertical separation between the words displayed at the top and bottom of the graticule area.

plifier

t Amplifier Q1274-Q1278 operates similar
t Amplifier to provide the horizontal de-

flection from the readout signal available at pin 4 of U1270. The gain of this stage is fixed by the values of the resistors in the circuit.

Display Sequence

Fig. 3-49 shows a flow chart for the Readout System. This chart illustrates the sequence of events which occurs in the Readout System each time a character is generated and displayed on the CRT.

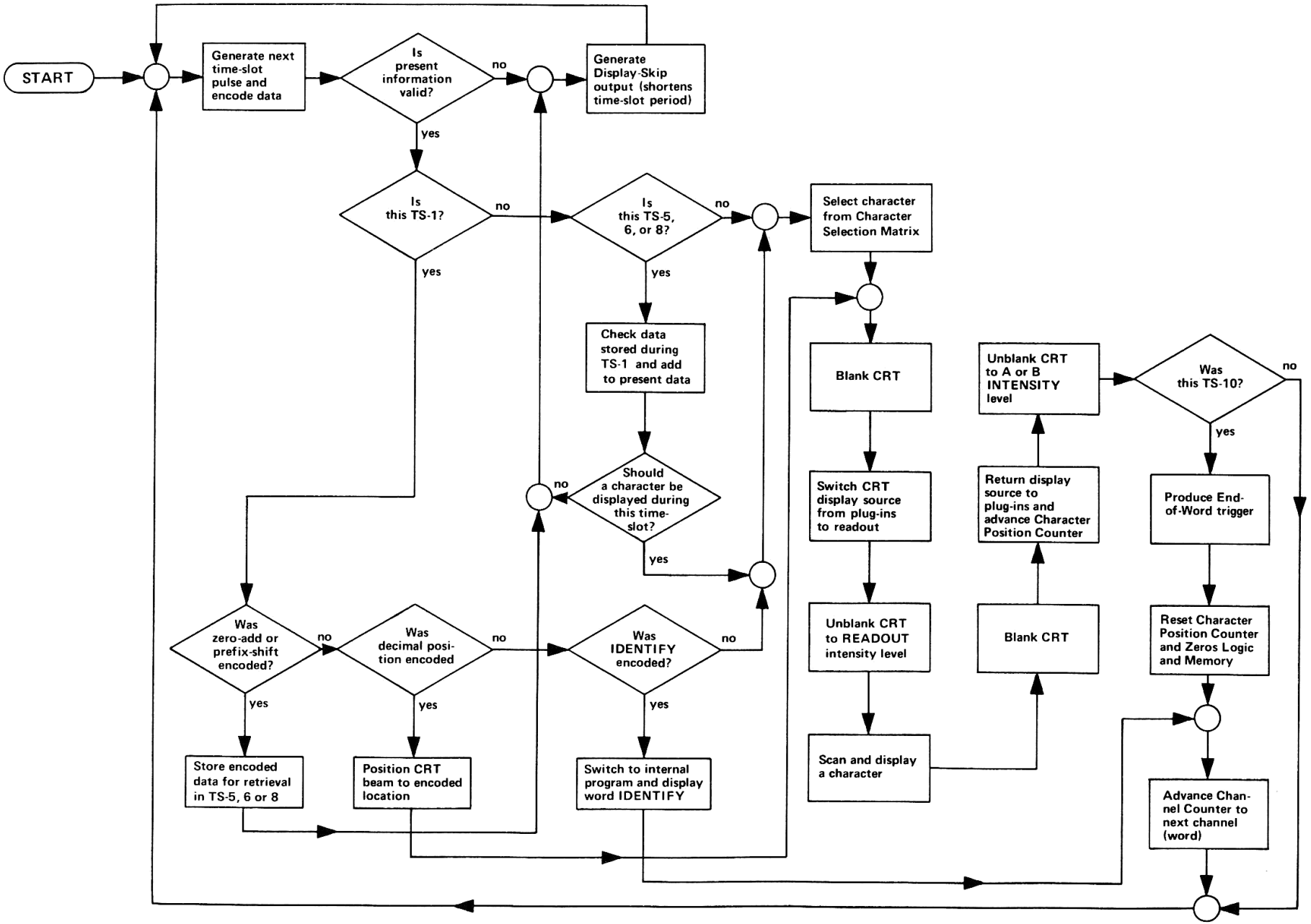


Fig. 3-49. Flow chart for character generation by the Readout System.