WAVETEK

INSTRUCTION MANUAL

Model 145

145-S-620, 145-S-872 & 145-S-1021

20 MHz Pulse/Function Generator

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Model 145-S-620 is a standard Wavetek Model 145 modified to provide a SYMMETRY control on the rear panel. This control allows the waveform time symmetry to be continuously adjusted over a 19:1 to 1:19 range. When this control is switched on, the generator operates at approximately 1/10 of the selected frequency. All procedures and descriptions in this manual assume that the SYMMETRY control is in the OFF position.

Model 145-S-872 is identical to the standard Model 145 except for the addition of an elapsed time meter installed on the rear panel.

Model 145-S-1021 is identical to the standard Model 145 except for the addition of both the SYMMETRY control and an elapsed time meter installed on the rear panel.

Option parts lists, assembly drawings and schematics as well as those for the Standard Model 145 are contained in Section 7 of this manual.

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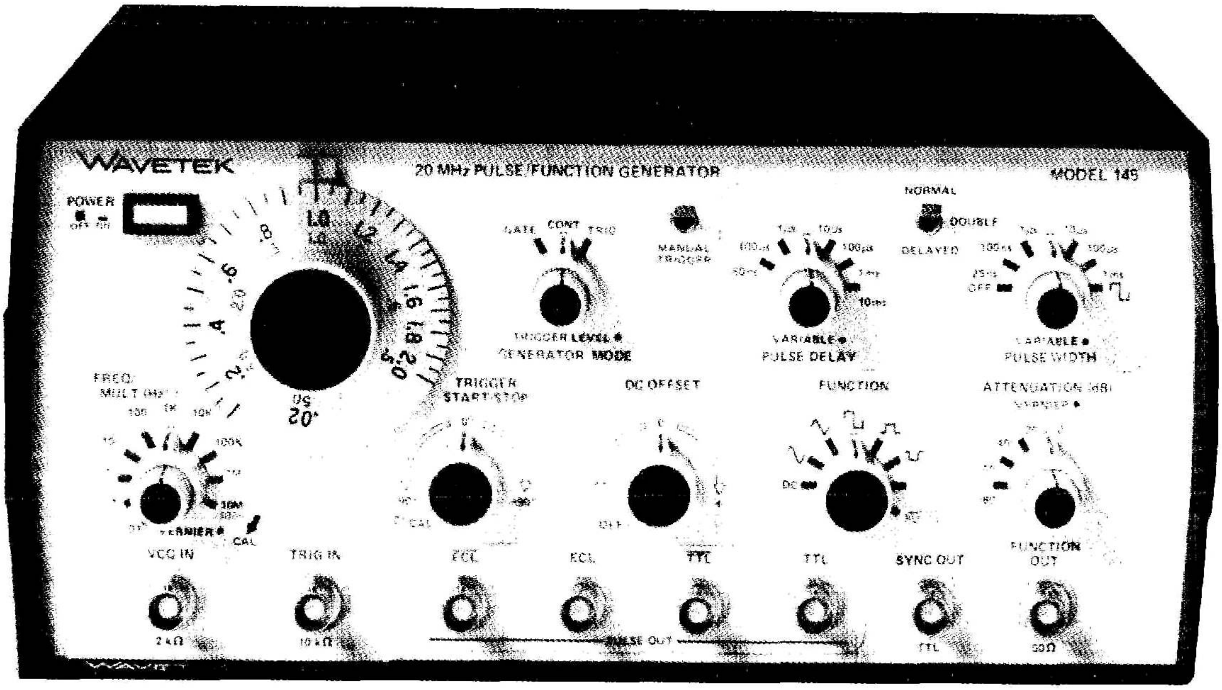

Model 145, 20 MHz Function/Pulse Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 145

The Model 145 20 MHz Pulse/Function Generator has the versatility of output found in a function generator, plus the pulse characteristics of a pulse generator. It is a precision source of sine, triangle, balanced square, positive square and negative square waveforms, a source of dc levels and a source of normal and inverted pulses. All are front panel and remote control variable from 0.0001 Hz to 20 MHz (periods from 50 ns to 10,000s). Pulse widths are variable from 25 ns to 1 ms and pulse delays variable from 50 ns to 10 ms. Double pulses (two pulses per period) are also available with variable time between pulses. The logical complement of the pulse is selectable and either pulse or complement are output simultaneously as ECL, $\overline{\text{ECL}}$, TTL, $\overline{\text{TTL}}$ and variable amplitude and offset pulses.

The amplitude controllable output of either waveform or pulse can be varied to 30 volts peak-to-peak (open circuit) and attenuated up to 80 dB. DC voltage or dc offset of signal is variable by front panel control and by external control between ±15 volts (open circuit). The outputs are also triggerable for one or multiple cycles by front panel switch or remote signal. A voltage representing generator frequency and a TTL level sync pulse at the frequency of the generator are auxiliary outputs.

1.2 SPECIFICATIONS

1.2.1 Versatility

Instrument operates as either a function generator or pulse generator.

1.2.2 Function Generator

Waveforms
Selectable sine ∿ , square ⊓⊔ , triangle ⋀⋁ , positive square ⊓ , negative square ⊔ and dc. TTL sync pulse and fixed amplitude pulses of TTL, $\overline{\text{TTL}}$, ECL and $\overline{\text{ECL}}$, all simulaneously available with function output.

Operational Modes
Continuous: Generator oscillates continuously at selected frequency.

Triggered: Generator is quiescent until triggered by an external signal or manual triger, then generates one cycle at selected frequency.

Gated: As triggered mode, except generator oscillates for the duration of the gate signal.

Frequency Range
0.0001 Hz to 20 MHz in 10 overlapping ranges with approximately 1% vernier control.

Function Output
∿ , ⊓⊔ , ⋀⋁ selectable and variable to 30 Vp-p (15 Vp-p into 50Ω). ⊓ , ⊔ , to 15 Vp (7.5 Vp into 50Ω). All waveforms and dc can supply 150 mA peak current and may be attenuated to 60 dB in 20 dB steps with an additional 20 dB vernier.

DC Output and DC Offset
Selectable thru FUNCTION OUT output. Controlled by front panel control or by applying an external voltage. Adjustable between a minumum of ±14.4 Vdc (±7.2 Vdc into 50Ω) with signal peak plus offset limited to ±14.4 Vdc (±7.2 Vdc into 50Ω). External offset sensitivity approximately −1 V/V with output into open circuit. DC offset and output waveform attenuated proportionately the 60 dB output attenuator.

Sync Output
A TTL level pulse. Will drive 50Ω termination.

GCV—Generator Controlled Voltage
At GCV OUT connector, a 0 to +2V signal proportional to generator frequency. 600Ω source impedance.

VCG—Voltage Controlled Generator
Up to 1000:1 frequency change with external 0 to 2 volt signal to VCG IN connector. Upper and lower frequencies limited to maximum and minimum of selected range.

Slew Rate: 2% of range per µs.

Linearity:
±0.2% for 10 Hz to 200 kHz.
±0.75% for 0.001 Hz to 2 MHz.

Impedance: 2 kΩ.

Trigger and Gate
Input Range: 1 Vp-p to ±10V.

Impedance: 10 kΩ, 33 pF.
Pulse Width: 25 ns minimum.
Repetition Rate: 10 MHz maximum.
Adjustable Triggered Signal Start/Stop Point (sine and triangle only): Approximately -90° to $+90^\circ$ to 2 MHz.

1.2.3 Frequency Precision

Dial Accuracy
±3% of full range from X .01 Hz to X 1 MHz.
±5% of full range on X 10 MHz.

Time Symmetry
Square wave variation less than:
±1% from 0.001 Hz to 200 kHz
±0.5% from 20 Hz to 20 kHz

1.2.4 Amplitude Precision

Amplitude Change With Frequency
Sine variation less than:
± 0.1 dB for 0.001 Hz to 200 kHz
± 0.5 dB for 200 kHz to 2 MHz
± 3.0 dB for 2 to 20 MHz

Step Attenuator Accuracy
0.3 dB per 20 dB step at 2 kHz.

1.2.5 Waveform Characteristics

Sine Distortion
<0.5% on X 100 Hz to X 10 kHz.
<1.0% on X .01 to X 10 Hz and X 100 kHz.
All harmonics 34 dB below fundamental on X 1 MHz.
All harmonics 26 dB below fundamental on X 10 MHz.

Square Wave Rise/Fall Times
At FUNCTION OUT <20 ns for 15V p-p output into 50Ω load.

1.2.6 Pulse Generator

Pulse Outputs
Variable amplitude pulse, and simultaneous fixed ECL, $\overline{\text{ECL}}$, TTL and $\overline{\text{TTL}}$ pulses and TTL sync pulse. All outputs can drive 50Ω terminations.

Operational Modes
Continuous, triggered and gated plus the following.
Normal Pulse: Adjustable width pulse in phase with sync signal.
Delayed Pulse: Pulse delayed with respect to normal pulse. Pulse delay and pulse width adjustable.
Double Pulse: Two pulses for every period. Time between pulses and pulse width adjustable. Minimum period 100 ns.

Pulse Period Range
50 ns to 10,000s in 10 overlapping ranges with approximately 1% vernier control.

Pulse Width
25 ns to 1 ms in 5 overlapping ranges with vernier control. Includes OFF and square wave.

Pulse Delay
50 ns to 10 ms in 6 overlapping ranges with vernier control.

Duty Cycle
Duty cycles to 70% for periods > 100 ns (< 10 MHz); for periods < 100 ns (> 10 MHz) duty cycles are approximately 50%.

Function Output
Variable to 30V p-p (15V p-p into 50Ω). DC offset and attenuation are same as for function generator.

Pulse Rise/Fall Times
At FUNCTION OUT, < 20 ns for 15V p-p output into 50Ω load.

1.2.7 General

Stability
Short Term: ±0.05% for 10 minutes.
Long Term: ±0.25% for 24 hours.
Percentages apply to amplitude, frequency and dc offset.

Environmental
Specifications apply at 23°C ± 5°C. Instrument will operate from 0°C to 50°C ambient temperatures.

Dimensions
28.6 cm (11 ¼ in.) wide; 13.3 cm (5 ¼ in.) high; 27.3 cm (10¾ in.) deep.

Weight
5 kg (11 lb) net; 6.6 kg (14½ lb) shipping.

Power
90 to 105V, 108 to 126V, 198 to 231V and 216 to 252V selectable; 48 to 400 Hz; less than 30 watts.

NOTE

All specifications apply from 0.1 to 2.0 on frequency dial when FUNCTION OUT output is at maximum and 50Ω terminated. Function generator specifications apply when PULSE WIDTH control is OFF.

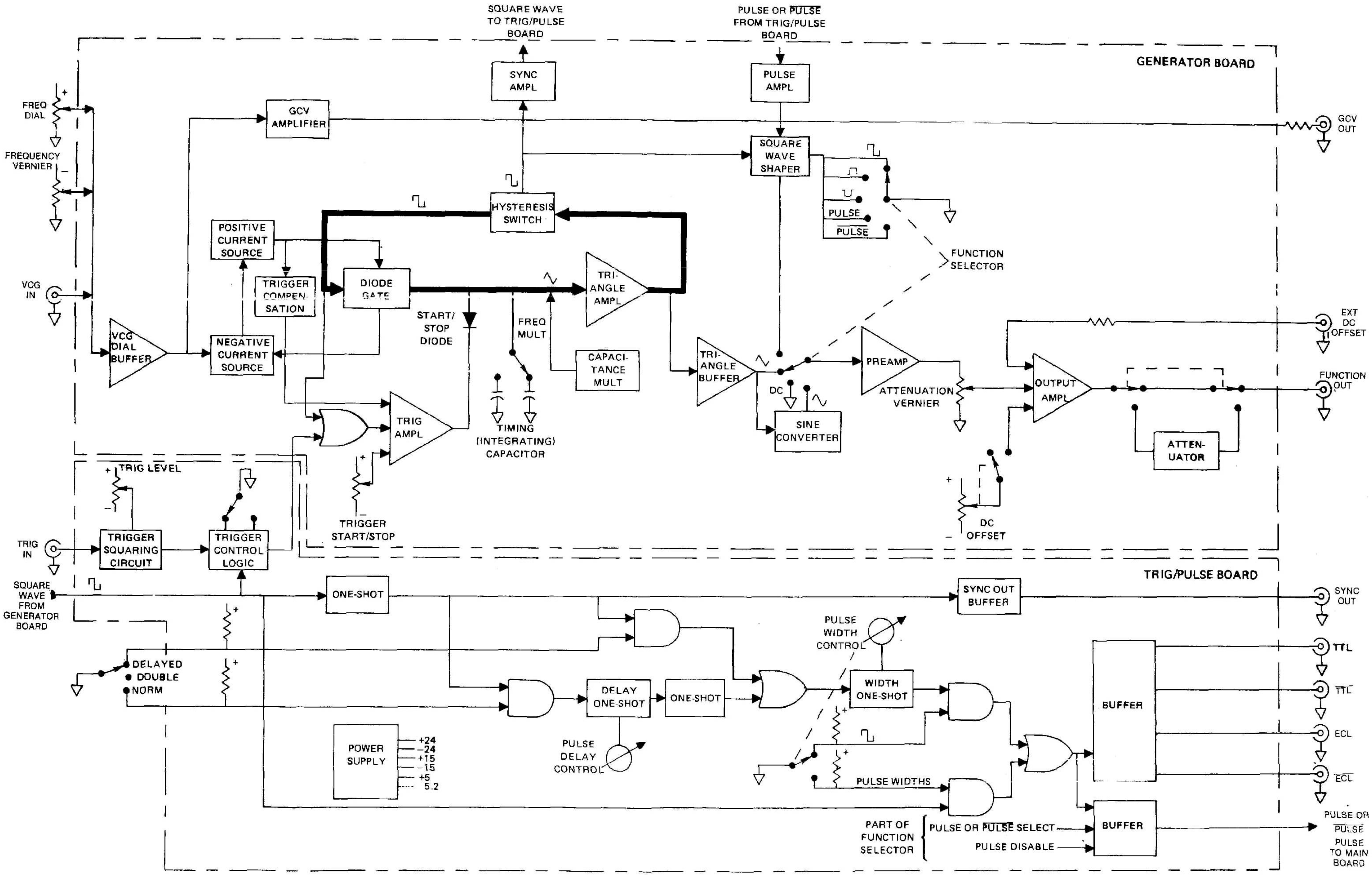

Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 BASIC WAVEFORM DEVELOPMENT

The heart of the generator (the bold path in figure 4-1) is a triangle and square wave generator. The triangle waves are developed by capacitor charging ramps that are alternately reversed in polarity. The polarity reversal is caused by a flip-flop circuit, or hysteresis switch, that in turn produces the square waves. The flip-flop changes states upon detecting amplitude limits of the charging ramps through the triangle amplifier.

As shown in figure 4-1, the VCG dial buffer sums the currents from the frequency dial, frequency vernier and VCG in connector. The VCG dial buffer is an inverting amplifier whose output voltage is used to control a positive current source and a negative current source. For symmetrical output waveforms, the currents from the two current sources are equal and directly proportional to the voltage of the VCG dial buffer output. The diode gate, which is controlled by the hysteresis switch, is used to switch the positive or the negative current to the integrating capacitor selected by the frequency multiplier. If the positive current is switched into the integrating capacitor, the voltage across the capacitor will rise linearly to generate the triangle rise transition. If the current is negative, the voltage across the integrating capacitor will fall linearly to produce the fall transition.

The triangle amplifier is a unity gain amplifier whose output is fed to the hysteresis switch. The hysteresis switch has two voltage limit points (+1.25 and −1.25V) at its input.

During the time the output voltage of the triangle amplifier is rising, the output voltage of the hysteresis switch is positive, but when the output voltage of the triangle reaches +1.25V, it triggers the hysteresis switch causing the output to switch negative. Once the control voltage into the diode gate becomes negative, it will switch the positive current out and switch the negative current in to the integrating capacitor, so that the voltage across the capacitor will reverse, starting a linear decrease of the waveform. When the decreasing voltage reaches −1.25V, the output of the hysteresis switch will switch back to positive, reversing the process. This action generates the triangle waveform as shown in figure 4-2. Since the output of the hysteresis switch is a square wave, the result is simultaneous generation of a square wave and a triangle wave at the same frequency.

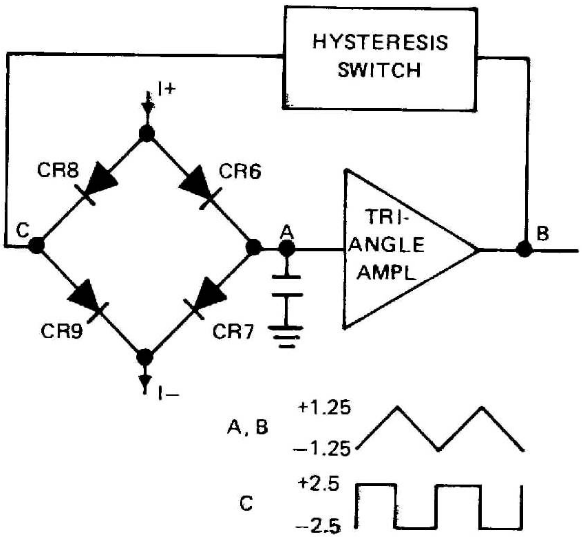

Figure 4-2. Basic Generator and Timing Diagram

The output frequency is determined by the magnitude of the capacitor selected by the frequency multiplier and the magnitude of the positive and negative current sources. Since the current sources are linearily proportional to the control voltage of the VCG circuit, the output frequency will also be linearily proportional to the control voltage.

The output of the hysteresis switch is fed to the sync amplifier and also the the square wave shaper. The square wave shaper consists of a shaping circuit which limits the square wave output swing to ±1.25V. For positive pulse outputs, it limits the output voltage swing from -1.25 to 0V; and for negative pulse outputs, it limits the output voltage swing from 0 to +1.25V. The PULSE or $\overline{\text{PULSE}}$ from the auxiliary board are bipolar and processed as the square wave.

The triangle wave from the triangle amplifier is coupled through a buffer amplifier and made available to the function selector switch. The buffer amplifier provides a low impedance to drive the sine converter circuit. The sine converter, using the nonlinear characteristics of its diodes, converts the triangle wave into a sine wave.

The square wave from the sync amplifier, processed through a one-shot and the sync out buffer, is externally available at the sync out connector. The sync pulse, then, is a TTL level pulse output of the generator frequency.

4.2 AMPLITUDE OFFSET AND ATTENUATION

The selected waveform is inverted and amplified in the preamplifier. The preamplified waveform is sent to the output amplifier.

The output amplifier is an inverting amplifier with a current limiting output stage for short circuit protection. The dc offset control provides the offset to the selected waveforms center reference. The dc offset can be set by voltage at the external dc offset connector. The output amplifier establishes the generator 0 dB attenuation reference. An output attenuator decreases this reference amplitude in operator selected 20 dB steps. The attenuator consists of three voltage dividers. Attenuation between the steps is provided by the attenuation vernier.

4.3 TRIGGER AND GATE CONTROL

Generator operation is controlled by allowing or preventing the timing capacitor to charge. Figure 4-3 shows in detail this portion of the circuit. For continuous operation, the trigger amplifier maintains a positive level above the positive peak developed by the charging capacitors. This reverse biases (turns off) the start/stop diode, and the trigger amplifier does not interfere with continuous operation.

When the trigger amplifier outputs some level below the positive peak charging level, the diode is forward biased (turned on) to sink the integrating current from the current source, preventing the capacitors from charging to the positive peak. This stops waveform generation and holds the triangle output at some dc level called the trigger baseline. The trigger baseline is the level where a triangle waveform cycle starts and where it stops. This baseline is directly applicable to the triangle waveform and thus affects the sine wave. The square wave levels, output via the hysteresis switch, are not affected by the triangle baseline levels.

The normal trigger baseline is zero volts, analogous to 0° phase of a sine or triangle waveform. The trigger start/stop control offsets the trigger amplifier output and can change the baseline for starting and stopping a sine or triangle waveform from its negative peak (−90°) to its positive peak (+90°) range. At the extreme positive peak level setting though, the diode is again reverse biased and generator operation goes continuous.

When charging level is being held, the positive current generator still varies its output with corresponding frequency control inputs. These varying currents must be sunk through the diode to keep the timing capacitors from varying their charge, and thus varying the trigger baseline. The baseline compensation circuit monitors the output from the positive current generator to control the trigger amplifier and thus control the necessary compensating current through the diode.

The trigger control logic determines that after a waveform starts, it always stops at a complete cycle and at the same phase at which it started. The trigger control logic latches the trigger amplifier for an enabling output from the time the cycle starts to when the negative peak of the last cycle is reached (just one cycle in the trigger mode). Upon reaching the negative peak, the timing capacitor continues charging positive again, but stops upon reaching the trigger baseline. A square wave from the hysteresis switch synchronizes the last negative peak time for unlatching the trigger amplifier for its trigger baseline output.

The generator mode control circuitry (not shown) determines whether the trigger control logic is to be fired for just one cycle, or is to be held on for the duration of the trigger input. When in gate mode, the trigger is directly coupled for controlling the trigger control logic. In the trigger mode, the squaring circuit output is converted by a one-shot to a narrow pulse which fires the trigger control logic.

The squaring circuit is a level detector that generates a square pulse for the duration of a trigger signal above the set trigger level. The pulse is also generated for the duration the manual trigger switch is held down in gate mode, and fires one cycle in triggered mode.

4.4 PULSE OUTPUTS

The pulse outputs are based on the square wave from the basic generator circuit (see figure 4-1); the pulse frequency is controlled by the frequency dial, frequency vernier and VCG voltage in the same manner as the waveforms. The square wave is first modified to the sync pulse by a one-shot circuit; then the normal/double/delayed pulse selector switch sets or inhibits AND gates to distribute the sync pulse to the delay one-shot and the width one-shot circuits. When the switch is in normal position, the sync pulse is gated to the width one-shot; the delay one-shot is bypassed. When the switch is in delayed position, the sync pulse is gated to the delay one-shot only. With the switch in the double position, the sync pulse is gated to both the delay and width one-shots.

Pulse width of the width and delay one-shot pulses can be varied by the front panel width and delay controls, respectively. The resulting pulse is gated by the selection of a pulse width value rather than the square wave (⊓⊔) detent on the pulse width switch. The pulse or the basic generator square wave, as selected by the pulse width control, is sent to a buffer circuit and output as TTL, $\overline{\text{TTL}}$, ECL and $\overline{\text{ECL}}$ pulses. The pulse or square wave is also routed to another buffer which is set by the selection of PULSE, $\overline{\text{PULSE}}$ or a waveform with the front panel function switch. This output, a normal pulse or a complemented pulse, is routed to the square wave shaper and output, if selected, through the output amplifier as a variable amplitude pulse. The pulse modes of normal, delayed and double are shown as timing diagrams in figures 4-4, 4-5 and 4-6.

4.5 WIDTH AND DELAY ONE-SHOTS

The pulse width and delay one-shots feature front panel adjustable current sources to regulate the capacitor charge time and as a result, the one-shot pulse width. The steady state condition of the one-shot circuit is as shown in figure 4-7: Upon triggering, $\overline{Q}$ goes low, the switch transistor switches off and the capacitor begins to charge. When the voltage across the capacitor is sufficient, the level detector senses the set level, the flip-flop is cleared and the circuit reverts to its steady state condition. The duty cycle of the one-shots is limited by the capacitor discharge time when returning to steady state conditions.

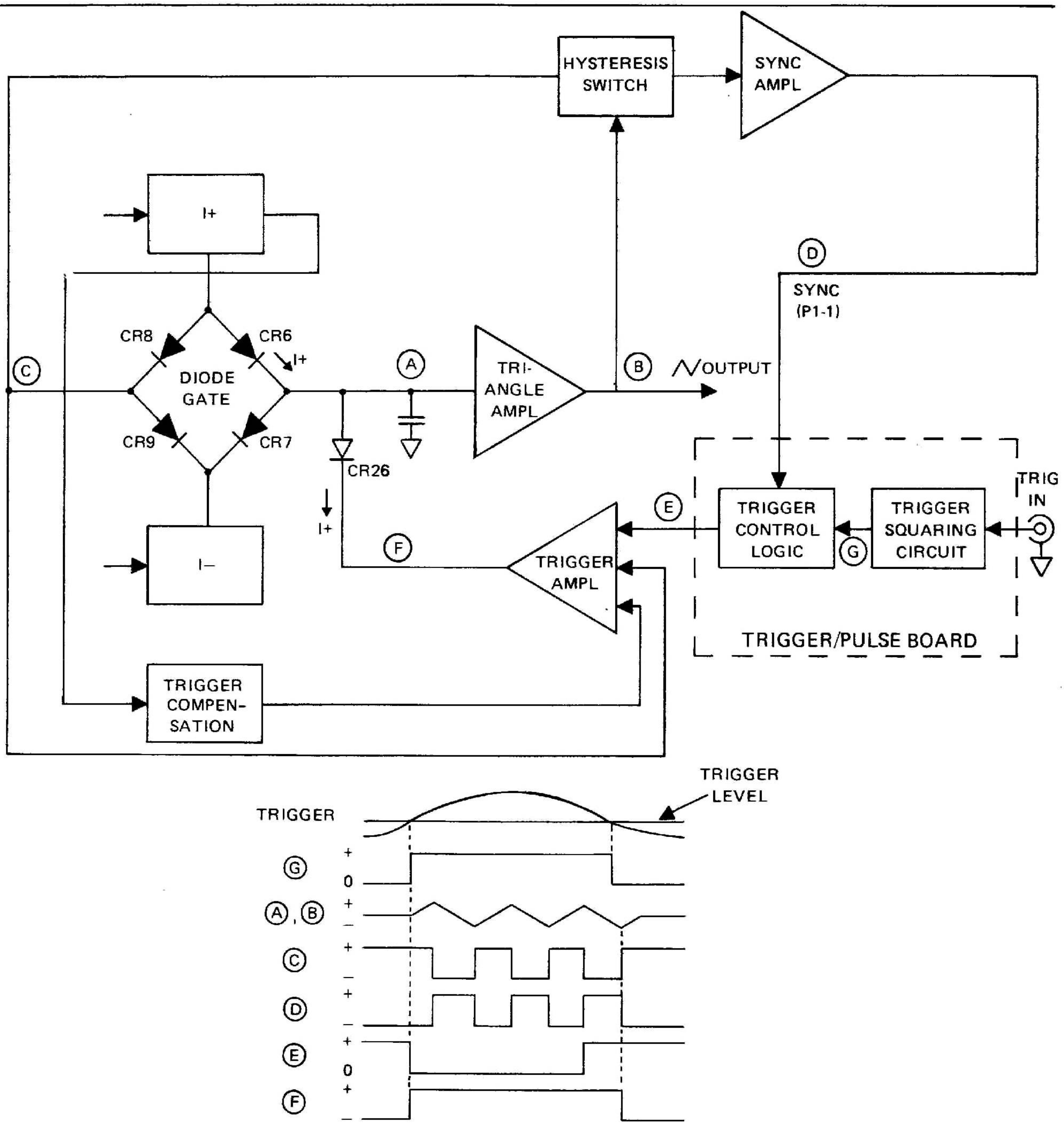

Figure 4-3. Trigger Circuit and Timing

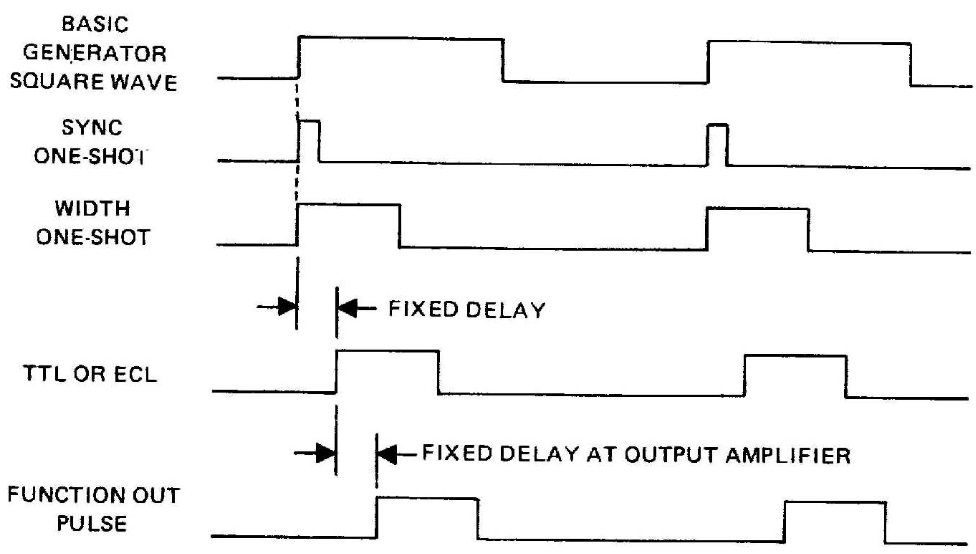

Figure 4-4. Normal Mode Timing

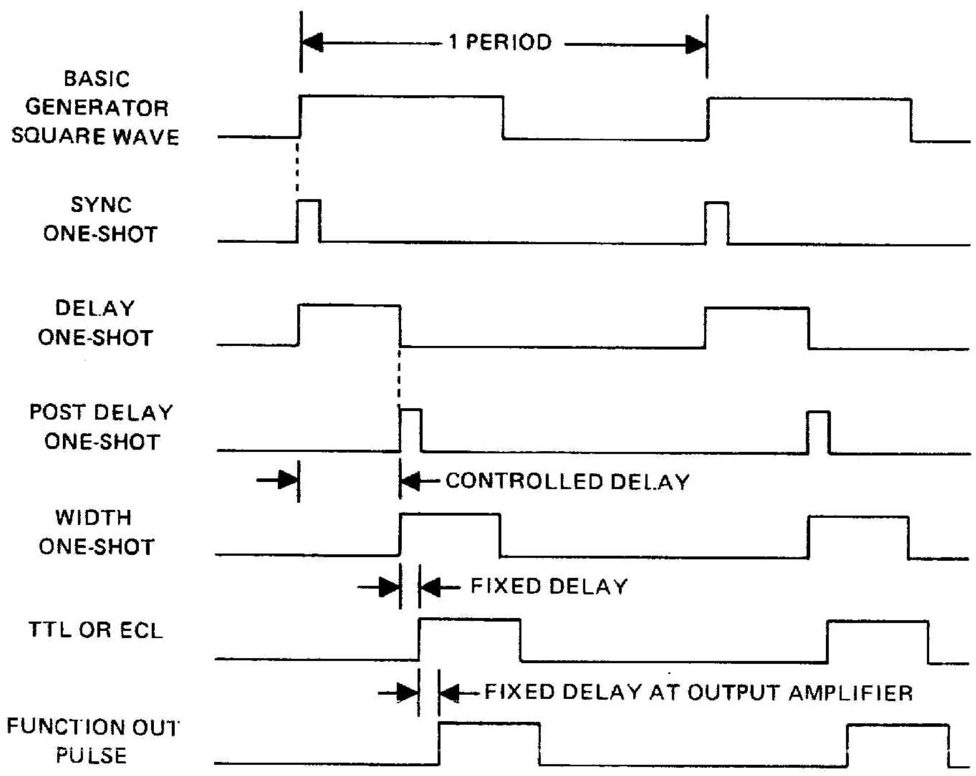

Figure 4-5. Delayed Mode Timing

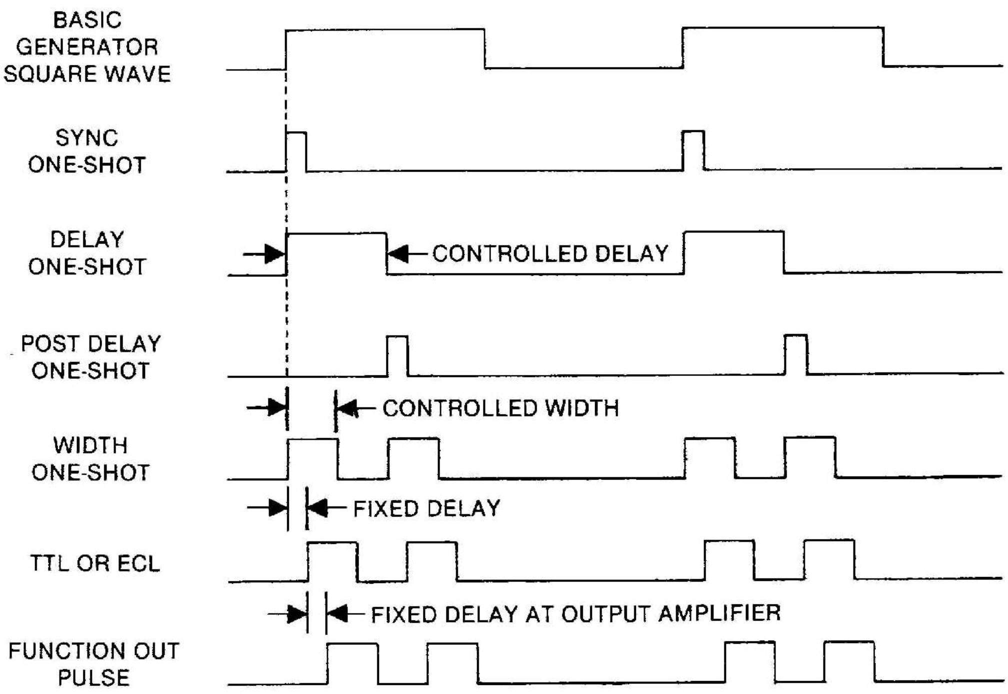

Figure 4-6. Double Mode Timing

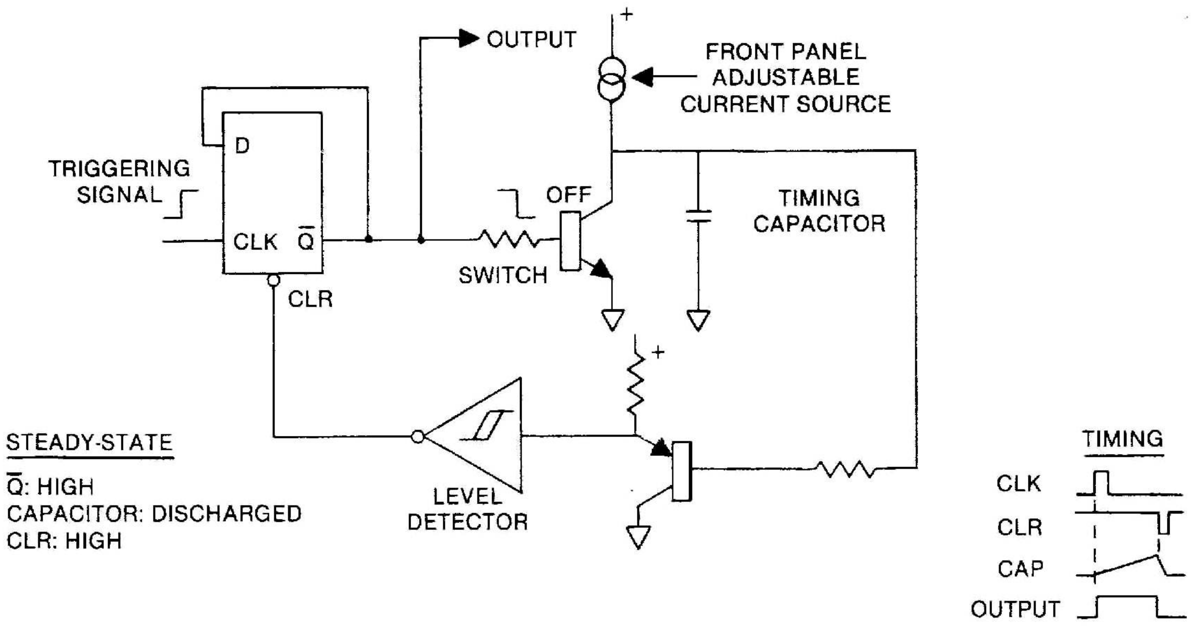

Figure 4-7. Width and Delay One-Shots

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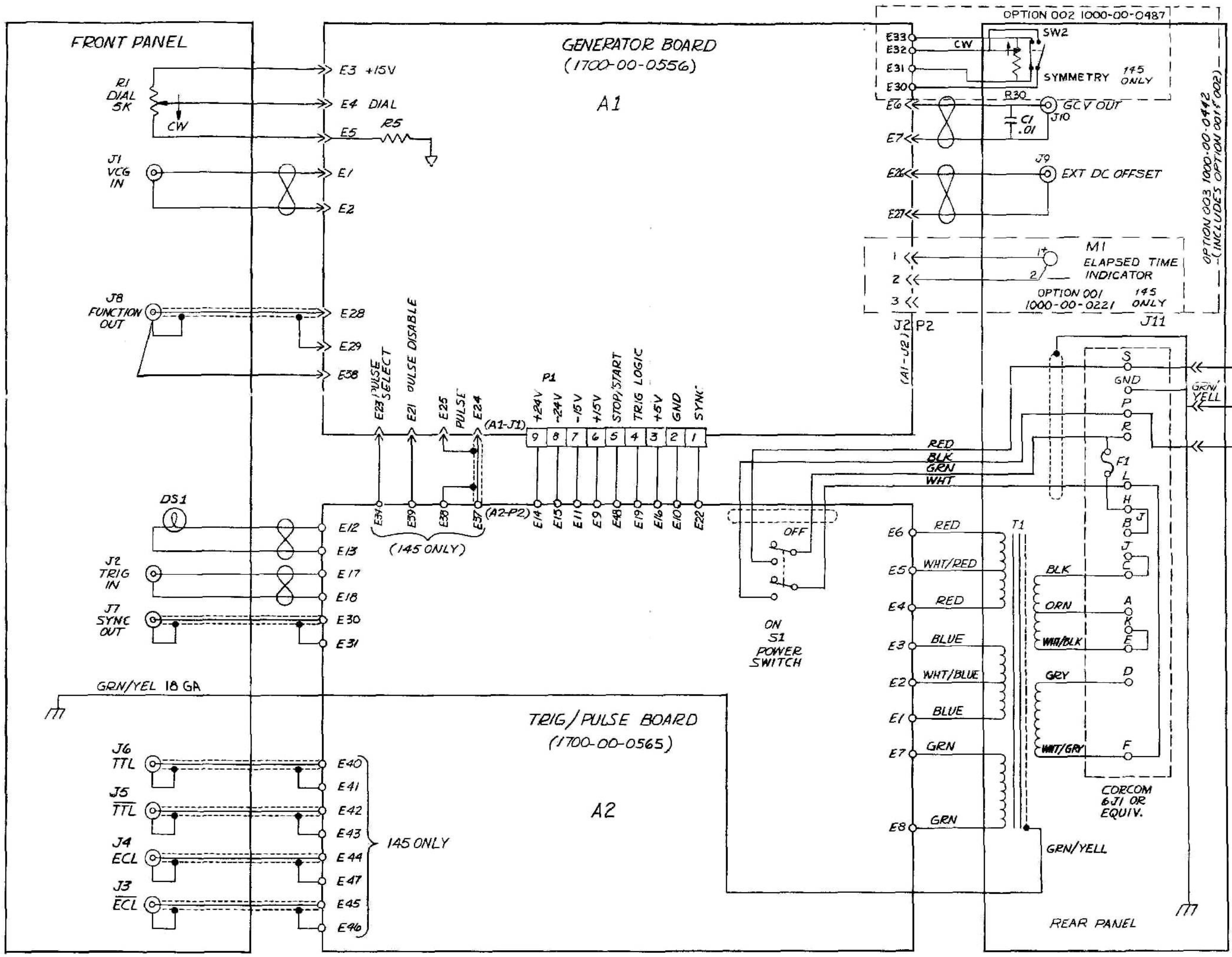
REV	ECN	BY	DATE	APP
B	ECN 1800	JRM	9-5-8	
C	ECN 1801	JRM	9-6-8	
D	ECN 2723 AUDIT	LOU	5-11-80	
E	ECN 3881	FN		
F	ECN6153		3-8-84	
G	9447			



1. F1 - 3/8 A 100-120 VAC
3/16A 220-240 VAC

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER, DATE 11-9-76
MATERIAL	PROJ ENGR
FINISH WAVETEK PROCESS	RELEASE APPROV
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030
	DO NOT SCALE DWG

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: INSTRUMENT SCHEMATIC

MODEL NO 143/145 | DWG NO 0004-00-0101 | REV G

CODE IDENT 23338 | SHEET 1 OF 1

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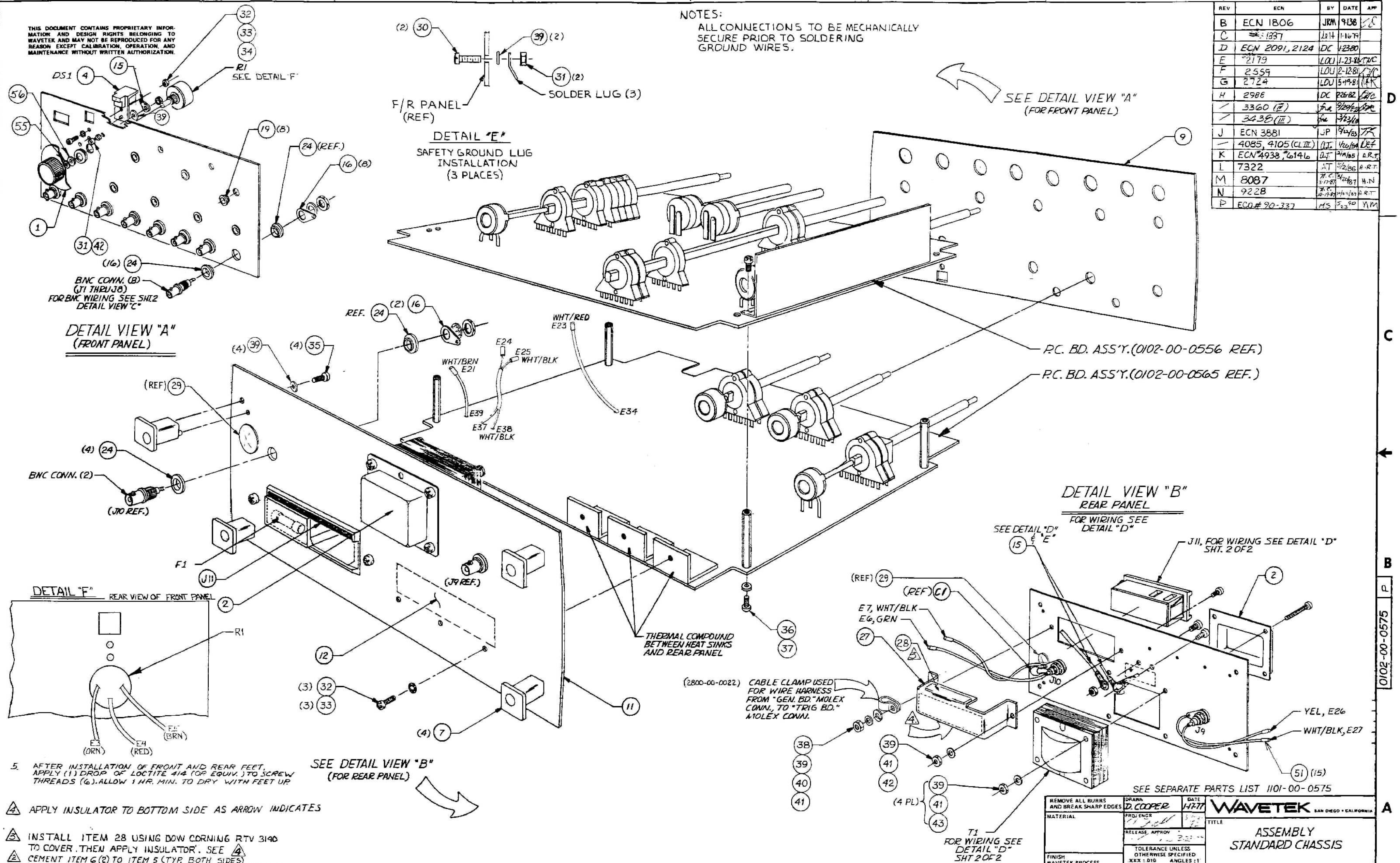
NOTES:
ALL CONNECTIONS TO BE MECHANICALLY SECURE PRIOR TO SOLDERING GROUND WIRES.

REV	ECN	BY	DATE	APP
B	ECN 1806	JRM	9-138	[illegible]
C	1337	[illegible]	1-16-79	
D	ECN 2091, 2124	DC	1-23-80	
E	2179	LOU	1-23-81	TWC
F	2559	LOU	2-12-81	[illegible]
G	2724	LOU	5-19-81	[illegible]
H	2986	DC	2-26-82	[illegible]
/	3360 (II)	fna	9/29/82	[illegible]
/	3438 (III)	fna	3/23/83	
J	ECN 3881	JP	8/22/83	TK
—	4085, 4105 (CL III)	A.J.	1/26/84	LEF
K	ECN #4938, #6146	A.J.	2/19/85	A.R.T.
L	7322	AT	5/2/86	A.R.T.
M	8087	M.C. 3-17-87	3/20/87	H.N
N	9228	M.C. 10-19-87	10/22/87	A.R.T.
P	ECO # 90-337	MS	5/23/90	YM



SEE SEPARATE PARTS LIST 1101-00-0575

5. AFTER INSTALLATION OF FRONT AND REAR FEET, APPLY (1) DROP OF LOCTITE 414 (OR EQUIV.) TO SCREW THREADS (6). ALLOW 1 HR. MIN. TO DRY WITH FEET UP

4 APPLY INSULATOR TO BOTTOM SIDE AS ARROW INDICATES

3 INSTALL ITEM 28 USING DOW CORNING RTV 3140 TO COVER, THEN APPLY INSULATOR. SEE 4

2 CEMENT ITEM 6 (2) TO ITEM 5 (TYP. BOTH SIDES)

1 MOUNT SWITCH TO P.C. BOARD PRIOR TO INSTALLING FRONT PANEL USE NO. 2-56 x 1/4 PAN HEAD SCREW WITH NUT (2)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 11-7-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ. ENGR [illegible]		TITLE ASSEMBLY STANDARD CHASSIS
	RELEASE APPROV [illegible]		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 145 · DWG NO 0102-00-0575 · REV P
	SCALE		CODE IDENT 23338 · SHEET 1 OF 2

0102-00-0575 P

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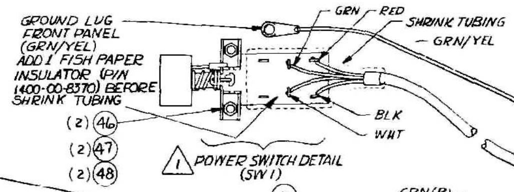

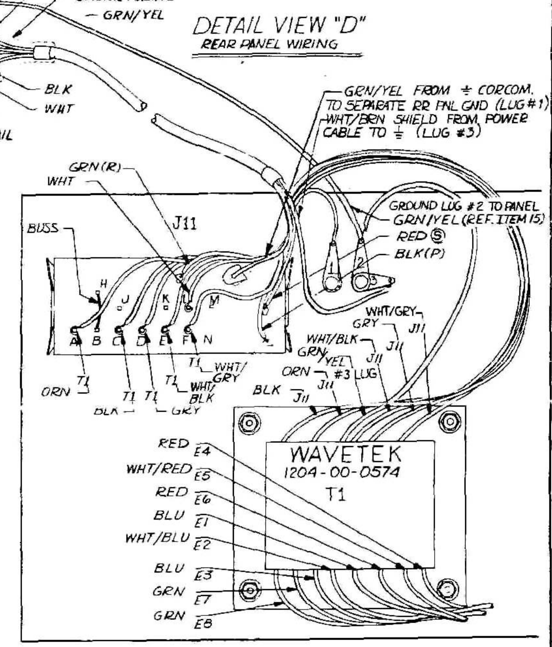

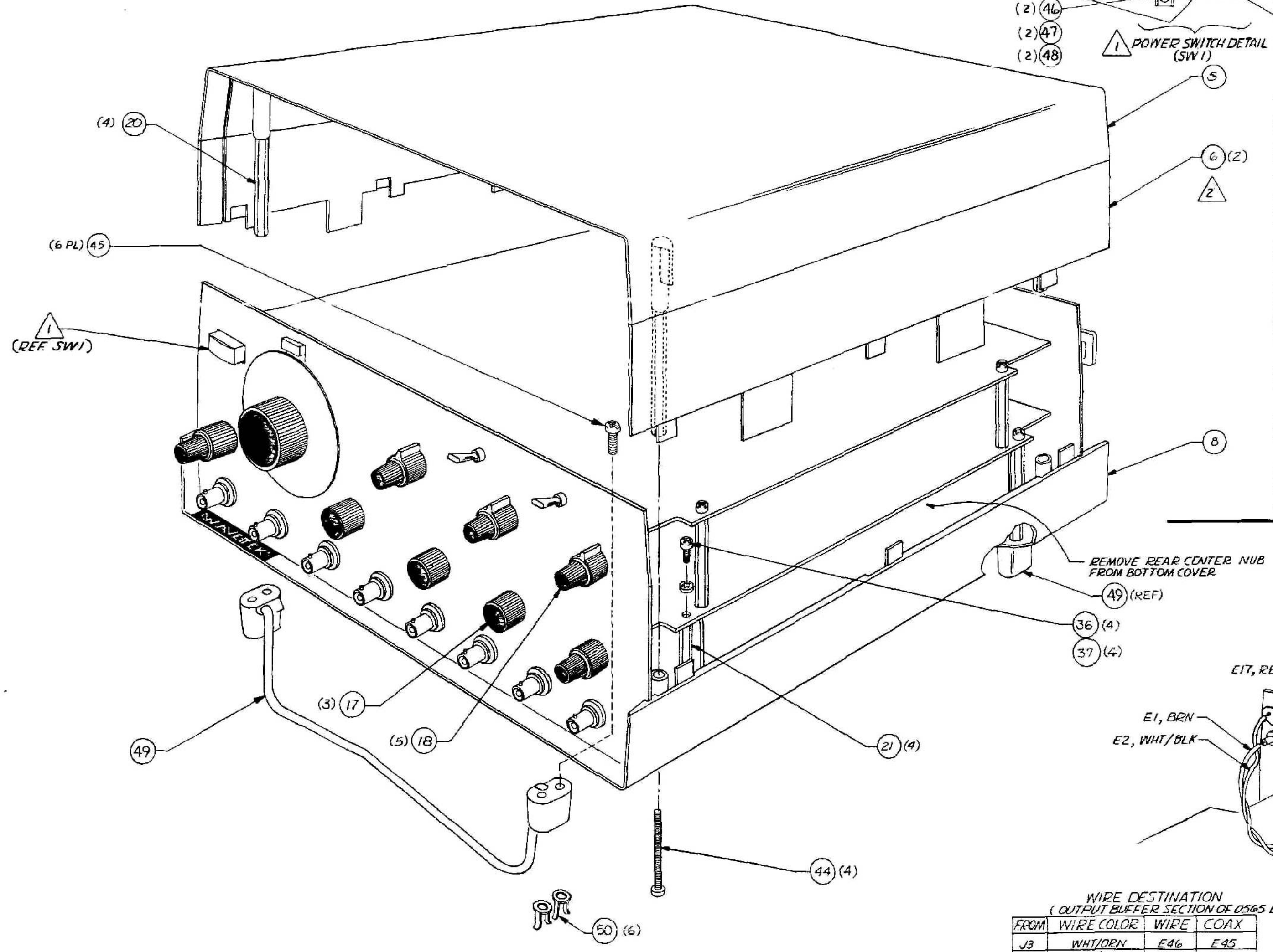

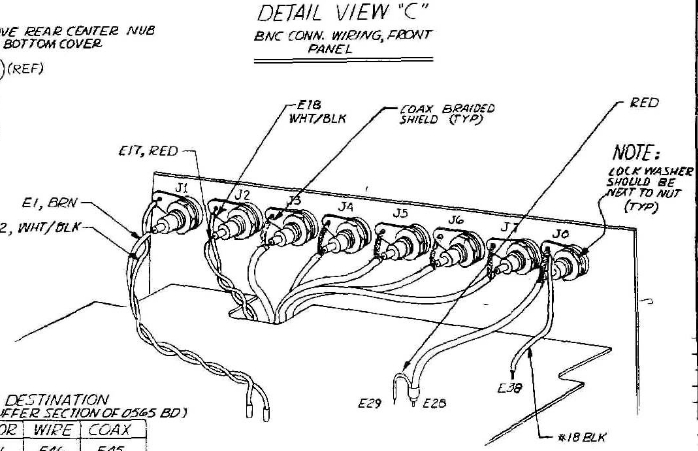

WIRE DESTINATION
(OUTPUT BUFFER SECTION OF 0565 BD)

FROM	WIRE COLOR	WIRE	COAX
J3	WHT/ORN	E46	E45
J4	WHT/YEL	E47	E44
J5	WHT/GRN	E43	E42
J6	WHT/BLU	E41	E40
J7	WHT/VIO	E31	E30

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D.COOPER	DATE HB-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	3/28/93	TITLE ASSEMBLY STANDARD CHASSIS
	RELEASE APPROV	3-23-77	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.020 ANGLES ±1		
	DO NOT SCALE DWG	MODEL NO 145	DWG NO 0102-00-0575 REV P
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

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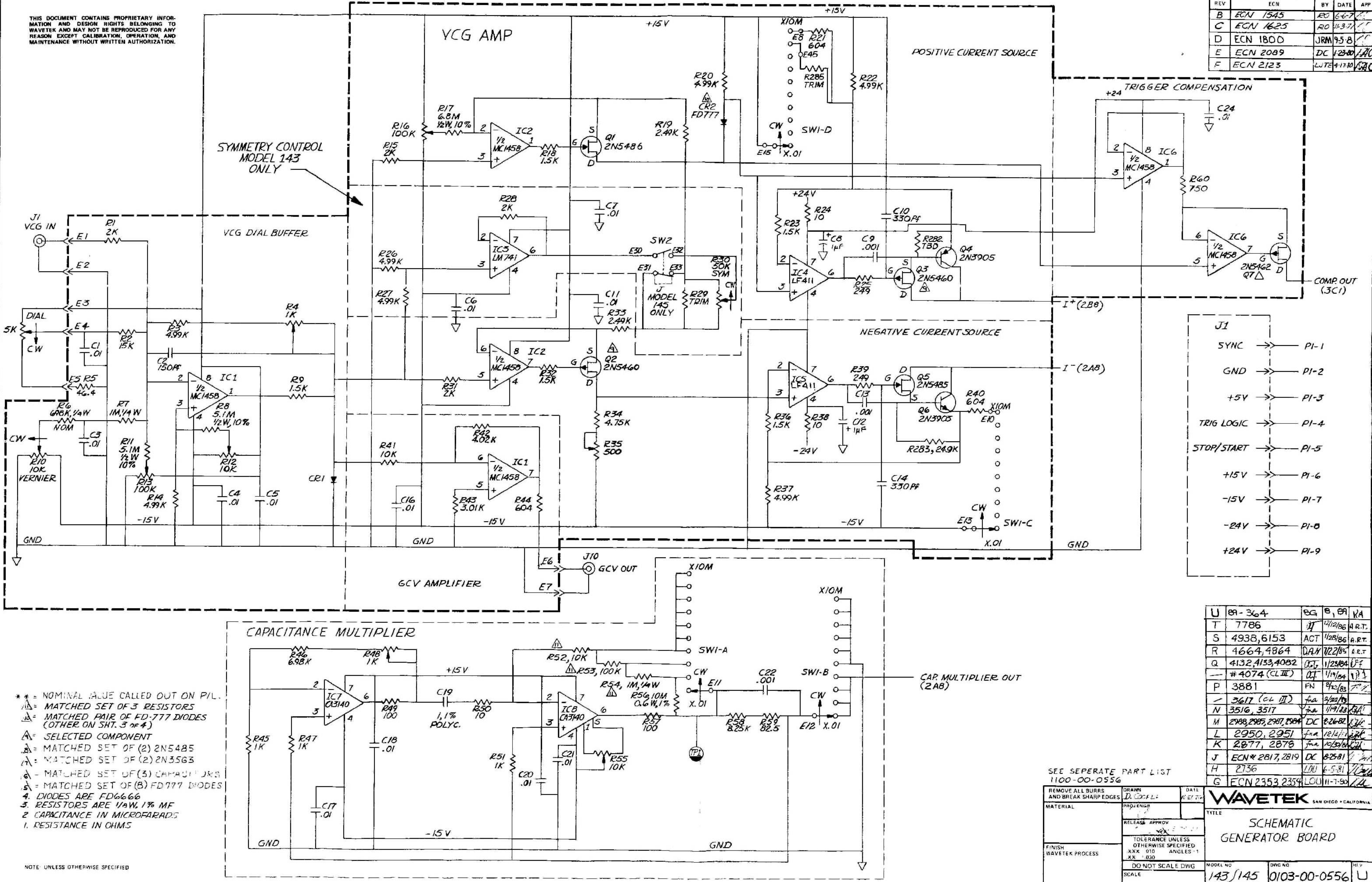
REV	ECN	BY	DATE	APP
B	ECN 1545	RO	6-6-7	
C	ECN 1625	RO	11-3-7	
D	ECN 1800	JRM	9-5-8	
E	ECN 2089	DC		
F	ECN 2123	LUTE		



∗∗ = NOMINAL VALUE CALLED OUT ON P/L.
⚠ = MATCHED SET OF 3 RESISTORS
⚠ = MATCHED PAIR OF FD-777 DIODES (OTHER ON SHT. 3 OF 4)
⚠ = SELECTED COMPONENT
⚠ = MATCHED SET OF (2) 2N5485
⚠ = MATCHED SET OF (2) 2N3563
⚠ = MATCHED SET OF (3) CAPACITORS
⚠ = MATCHED SET OF (8) FD777 DIODES
4. DIODES ARE FD6666
3. RESISTORS ARE 1/8W, 1% MF
2. CAPACITANCE IN MICROFARADS
1. RESISTANCE IN OHMS

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPERATE PART LIST 1100-00-0556

REV	ECN	BY	DATE	APP
U	89-364	BG	8, 89	KA
T	7786		12/12/86	A.R.T.
S	4938, 6153	ACT	1/28/86	A.R.T.
R	4664, 4864	DAH	1/22/85	A.R.T.
Q	4132, 4133, 4082		1/23/84	
—	#4074 (CL III)		1/19/84	
P	3881	FN	8/12/83	
—	3617 (CL III)		2/22/83	
N	3516, 3517		1/19/83	
M	2988, 2985, 2987, 2984	DC	8-26-82	
L	2950, 2951		12/4/81	
K	2877, 2878		10/30/81	
J	ECN # 2817, 2819	DC	8-25-81	
H	2736	LOU	6-5-81	
G	ECN 2353, 2354	LOU	11-7-80	

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN D. | DATE
MATERIAL | PROJ ENGR
RELEASE APPROV
FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030
DO NOT SCALE DWG
SCALE

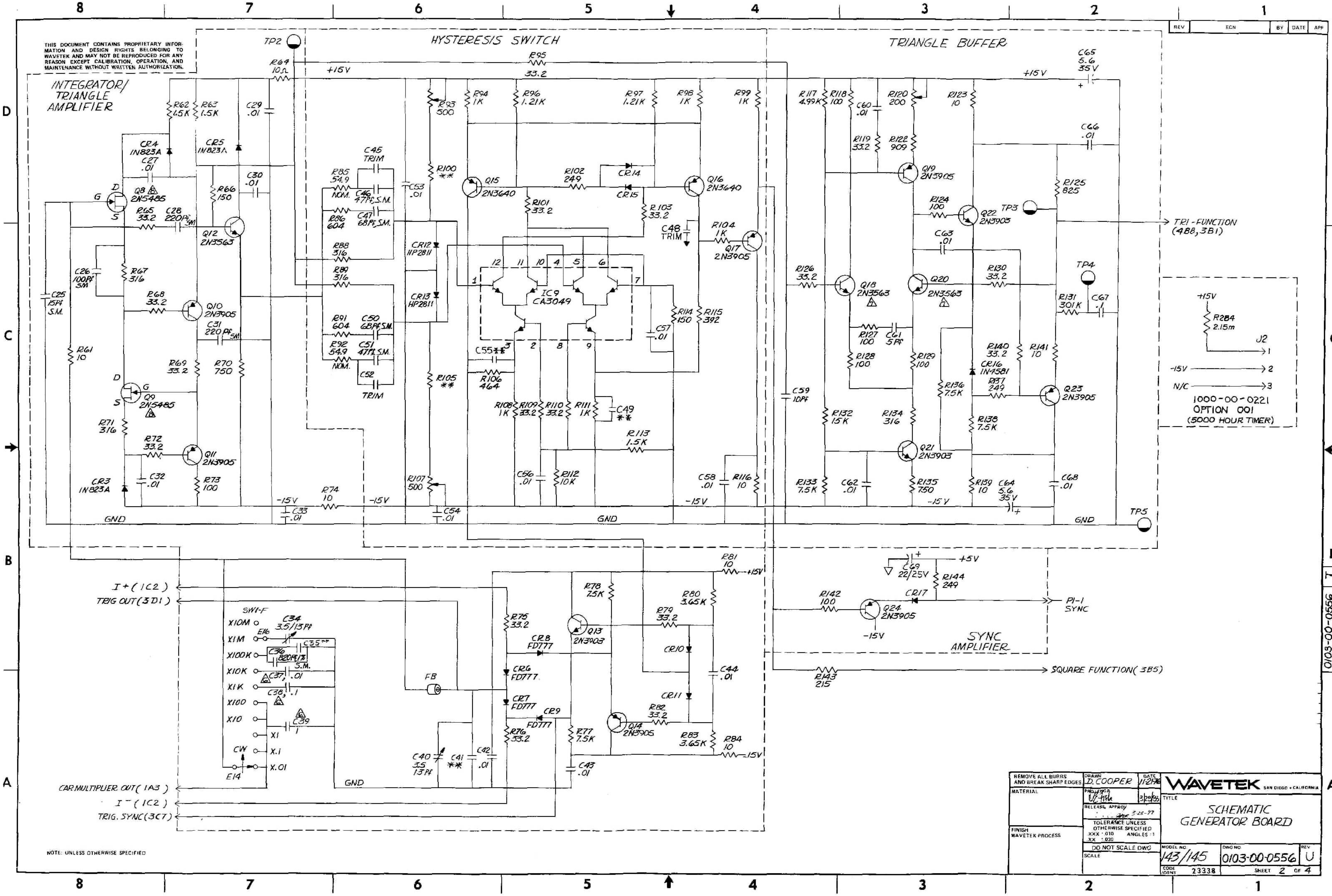
WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC GENERATOR BOARD

MODEL NO 143/145 | DWG NO 0103-00-0556 | REV U

CODE IDENT 23338 | SHEET 1 OF 4

0103-00-0556 U



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 11-2-76
MATERIAL		
FINISH WAVETEK PROCESS	RELEASE APPROV 3-25-77	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030	
	DO NOT SCALE DWG	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC GENERATOR BOARD

MODEL NO 143/145 — DWG NO 0103-00-0556 — REV U

CODE IDENT 23338 — SHEET 2 OF 4

NOTE: UNLESS OTHERWISE SPECIFIED

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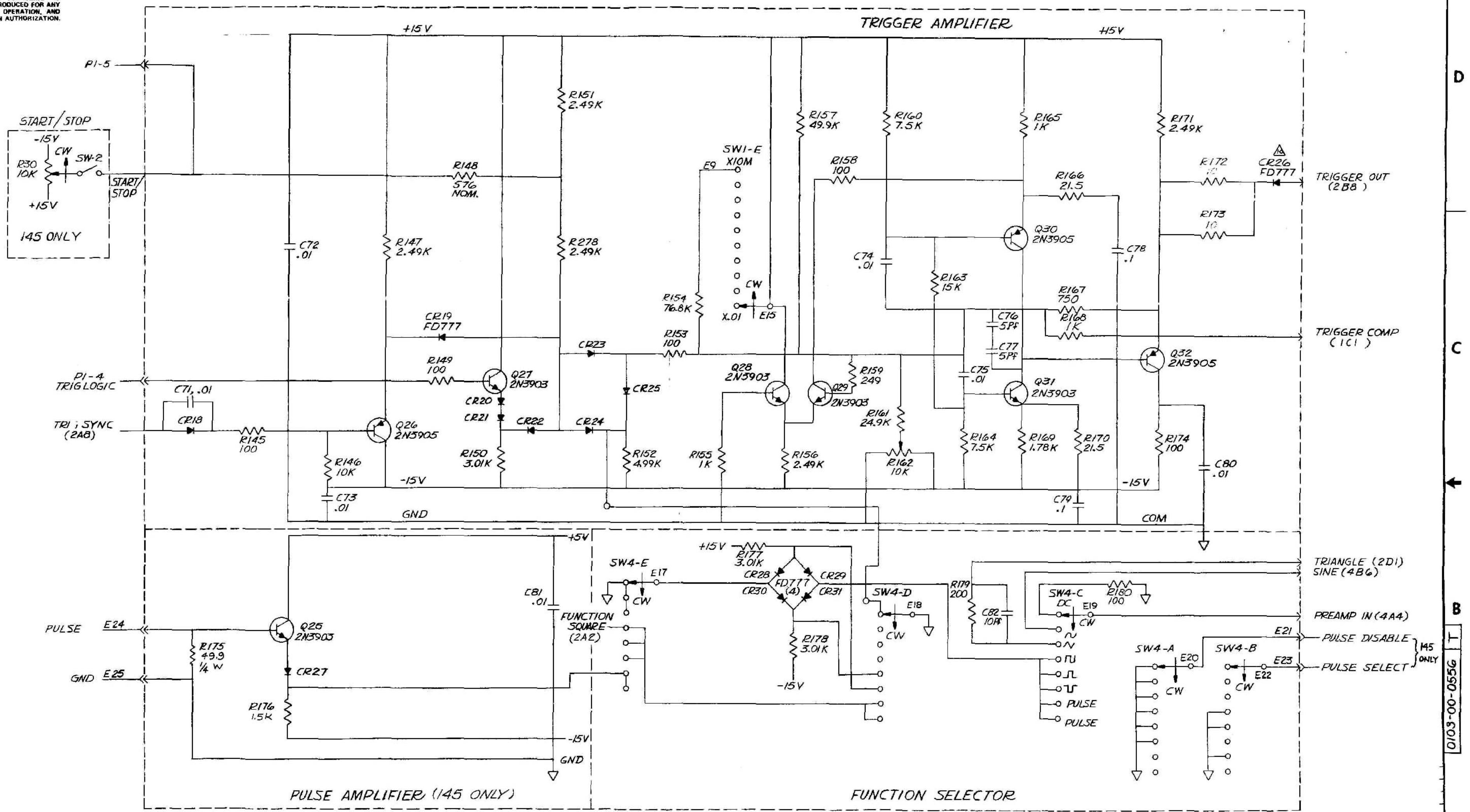


REV | ECN | BY | DATE | APP

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN D COOPER DATE 11-8-76

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030

DO NOT SCALE DWG

WAVETEK SAN DIEGO • CALIFORNIA

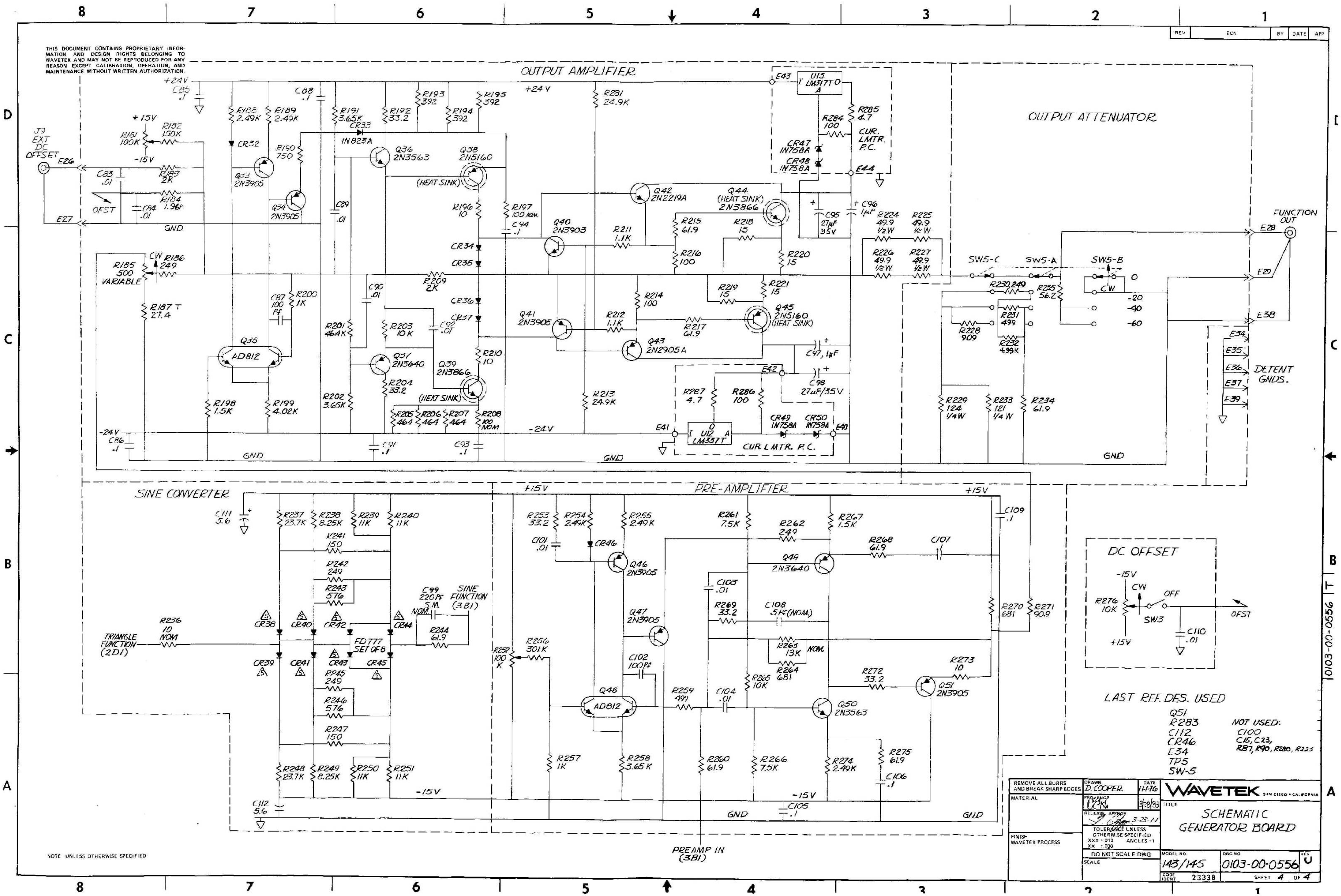
TITLE SCHEMATIC GENERATOR BOARD

MODEL NO 143/145 DWG NO 0103-00-0556 REV U

CODE IDENT 23338 SHEET 3 OF 4

NOTE: UNLESS OTHERWISE SPECIFIED

0103-00-0556 T



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OUTPUT AMPLIFIER
OUTPUT ATTENUATOR
SINE CONVERTER
PRE-AMPLIFIER
DC OFFSET
J9 EXT DC OFFSET
FUNCTION OUT
DETENT GNDS.
TRIANGLE FUNCTION (2D1)
SINE FUNCTION (3B1)
PREAMP IN (3B1)
CUR. LMTR. P.C.
CUR LMTR. P.C.
LAST REF. DES. USED
Q51
R283
C112
CR46
E34
TP5
SW-5
NOT USED:
C100
C15, C23,
R87, R90, R280, R223
NOTE UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER 11-1-76
TOLERANCE UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DWG
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC GENERATOR BOARD
MODEL NO 143/145
DWG NO 0103-00-0556
REV U
CODE IDENT 23338
SHEET 4 OF 4
0103-00-0556

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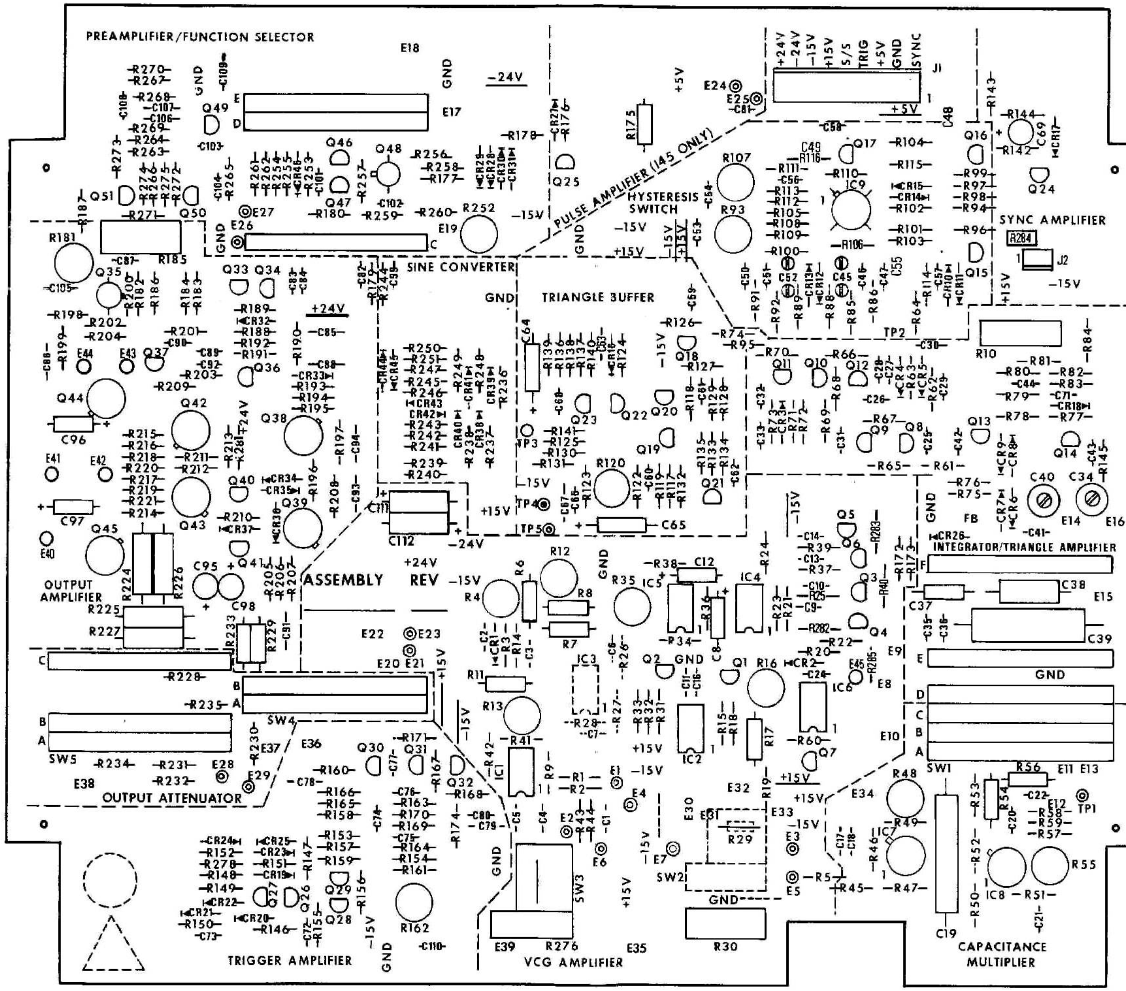

MADE FROM 0100-00-0556-3F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA, GENERATOR BD
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX .010, XX .030, ANGLES 1°		
	DO NOT SCALE DWG		MODEL NO: 145 — DWG NO: 1100-00-0556 — REV
	SCALE		CODE IDENT: 23338 — SHEET

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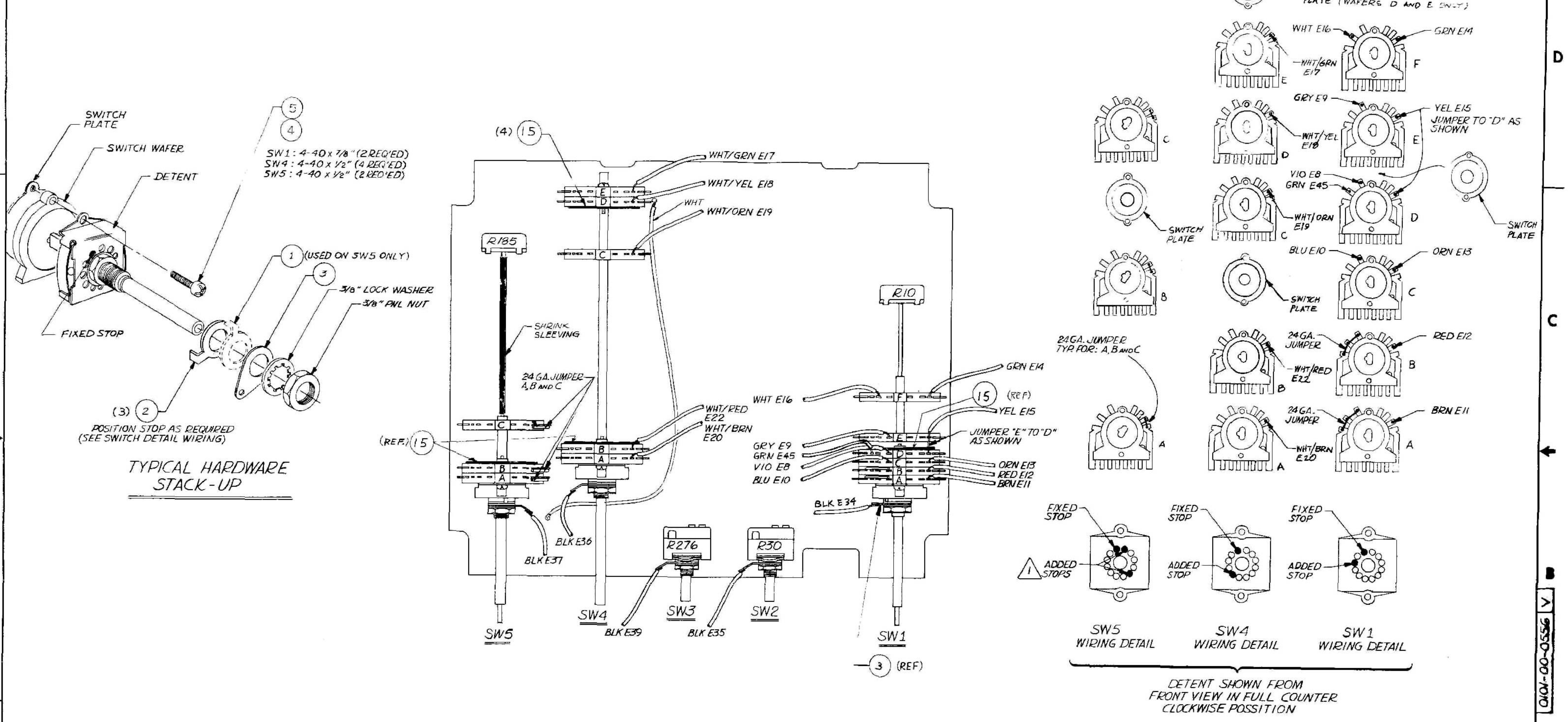
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR	TITLE ASSEMBLY GENERATOR BOARD	
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 145	DWG NO 0101-00-0556 REV V
	SCALE	CODE IDENT 23338	SHEET 2 OF 3

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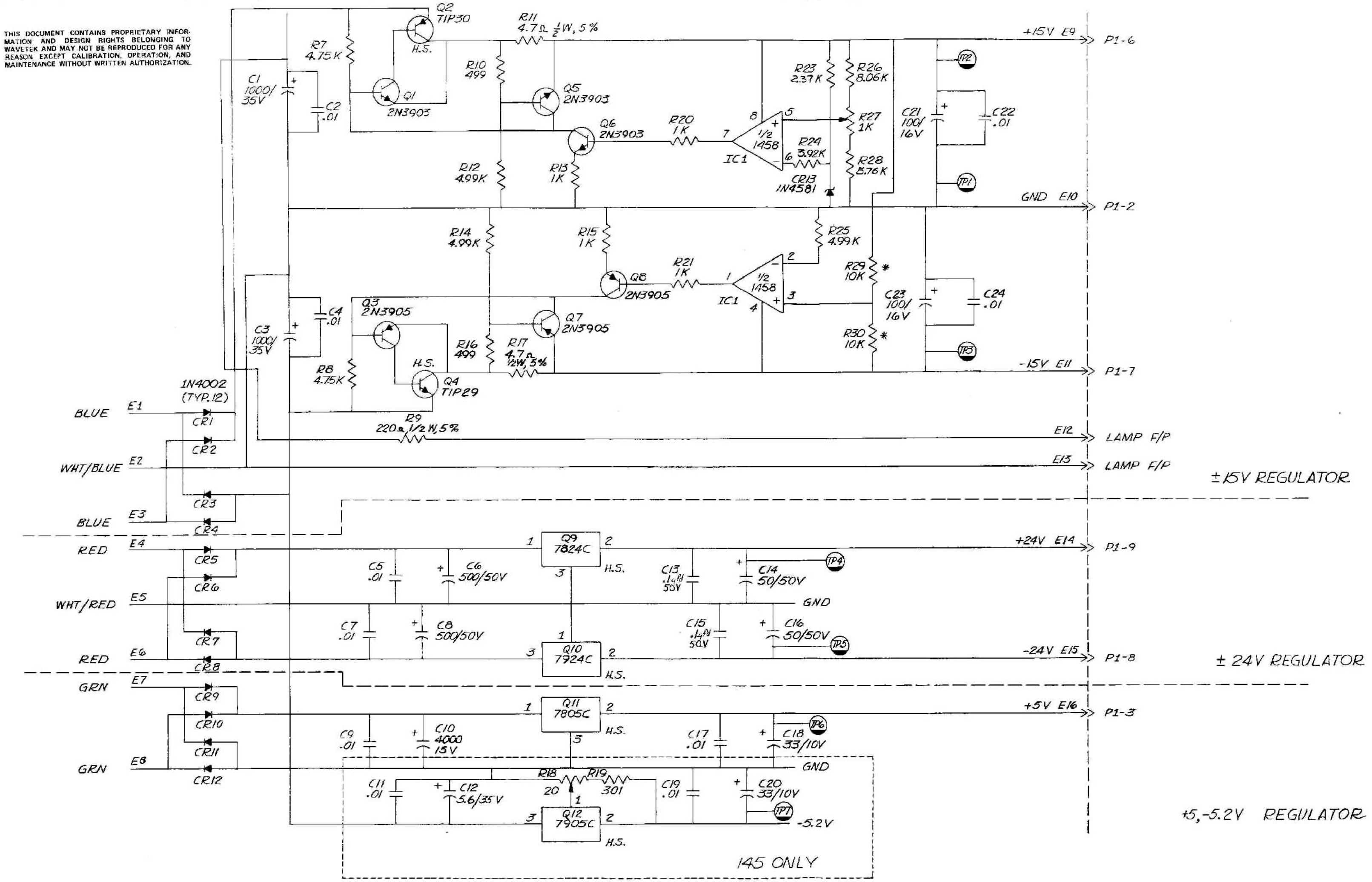


REV	ECN	BY	DATE	APP
B	ECN 1674	RO	[illegible]	
C	ECN 1800	JRM	9-5-8[illegible]	
D	ECN 2090	DC	[illegible]	
E	ECN # [illegible]	[illegible]	[illegible]	
F	ECN 2481	LOU	[illegible]	
G	ECN*2801	DC	[illegible]	
H	3195, 3196	[illegible]	[illegible]	
I	3618 (CL II)	[illegible]	[illegible]	
J	ECN 4417	KA	9/10/84	[illegible]
K	ECN 4674	HA	1/31/85	[illegible]
L	4664	DAM	[illegible]	[illegible]
M	7554	HT	7/7/88	[illegible]
N	89-410	BG	10/24/89	KA

0103-00-0565 N

LAST REF DES USED
C67
CR36
FB9
IC14
R72
SW4
Q21
F2

4. RESISTORS ARE 1/8W, 1% MF
3. RESISTANCE IN OHMS
2. CAPACITANCE IN MICROFARADS
1. * = M.P. 10K RESISTORS

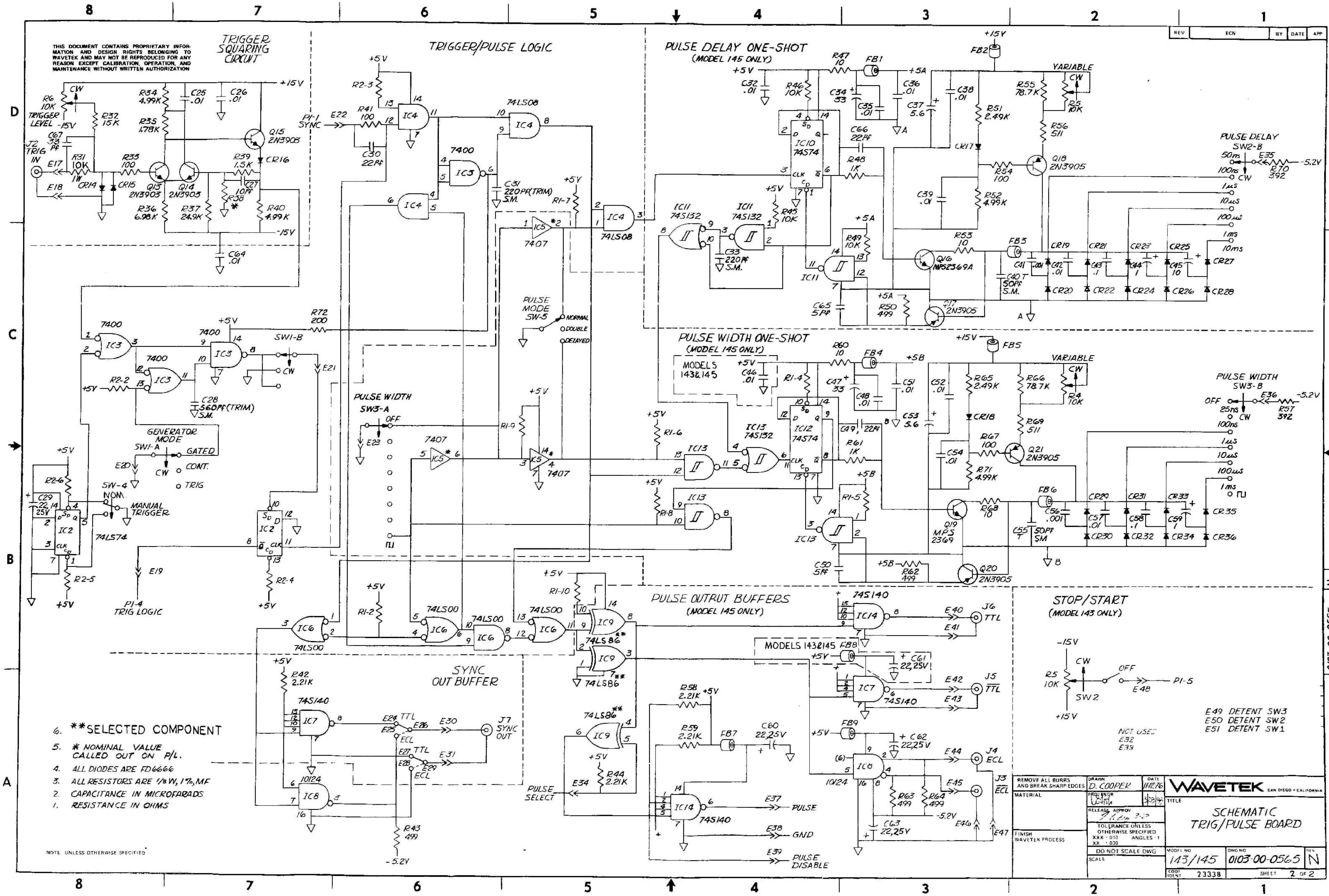
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER 11-10-76
ENGINEER [illegible]
RELEASE APPROV [illegible] 3-23-77
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC TRIG/PULSE BOARD

MODEL NO 143/145
DWG NO 0103-00-0565
REV N
CODE IDENT 23338
SHEET 1 OF 2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TRIGGER SQUARING CIRCUIT
TRIGGER/PULSE LOGIC
PULSE DELAY ONE-SHOT
(MODEL 145 ONLY)
PULSE WIDTH ONE-SHOT
(MODEL 145 ONLY)
MODELS 143&145
PULSE DELAY SW2-B
PULSE WIDTH SW3-B
PULSE WIDTH SW3-A
PULSE MODE SW-5
NORMAL
DOUBLE
DELAYED
GENERATOR MODE SW1-A
GATED
CONT.
TRIG
SW-4
NOM.
MANUAL TRIGGER
P1-4 TRIG LOGIC
P1-1 SYNC
J2 TRIG IN
TRIGGER LEVEL
PULSE OUTPUT BUFFERS
(MODEL 145 ONLY)
SYNC OUT BUFFER
J7 SYNC OUT
STOP/START
(MODEL 143 ONLY)
MODELS 143&145
J6 TTL
J5 TTL
J4 ECL
J3 ECL
PULSE SELECT
PULSE
GND
PULSE DISABLE
E49 DETENT SW3
E50 DETENT SW2
E51 DETENT SW1
NOT USED E32 E33
6. **SELECTED COMPONENT
5. * NOMINAL VALUE CALLED OUT ON P/L.
4. ALL DIODES ARE FD6666
3. ALL RESISTORS ARE 1/8 W, 1%, MF
2. CAPACITANCE IN MICROFARADS
1. RESISTANCE IN OHMS
NOTE: UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER
TOLERANCE UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DWG
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC TRIG/PULSE BOARD
MODEL NO 143/145
DWG NO 0103-00-0565
REV N
CODE IDENT 23338
SHEET 2 OF 2
0103-00-0565

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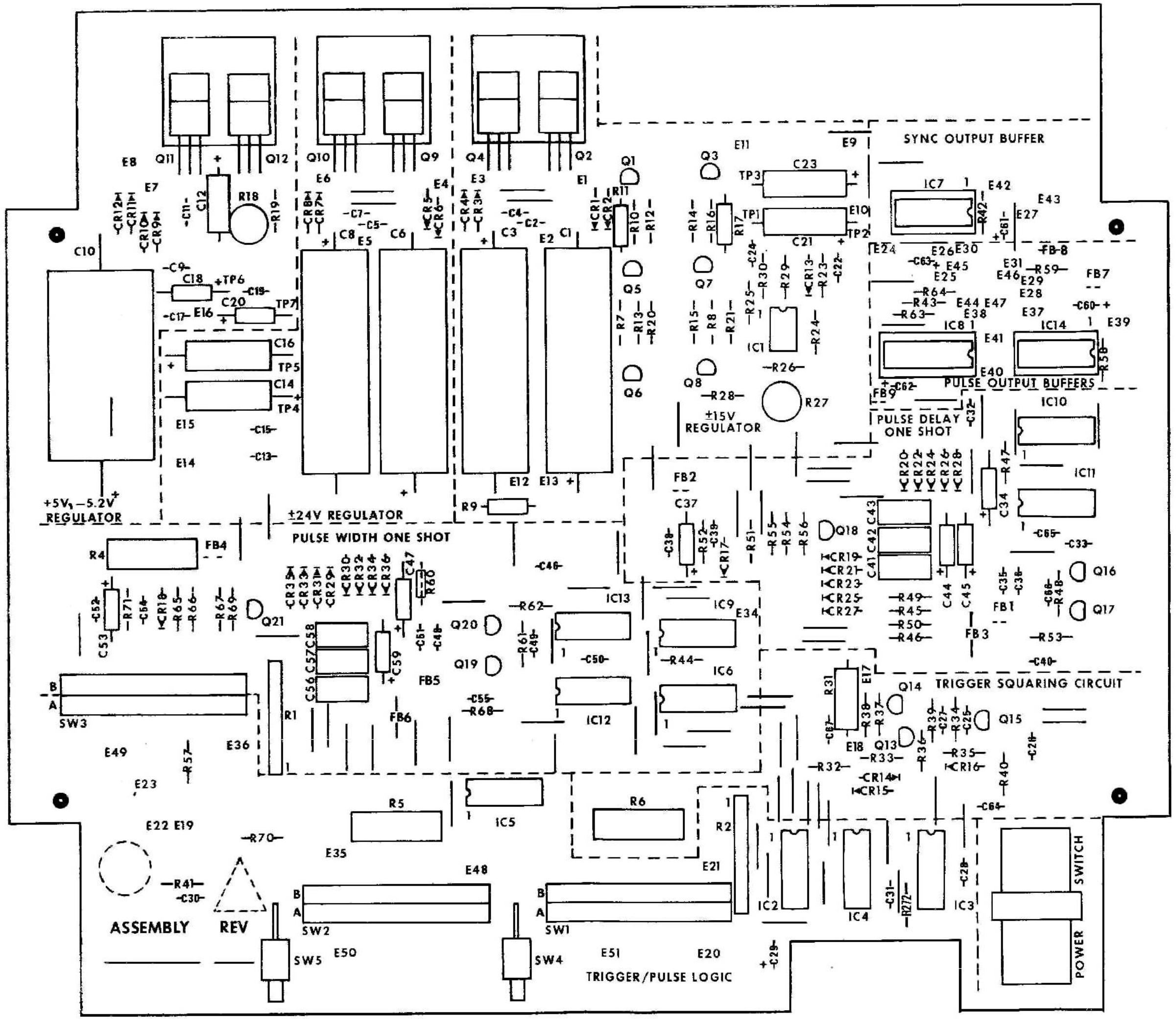
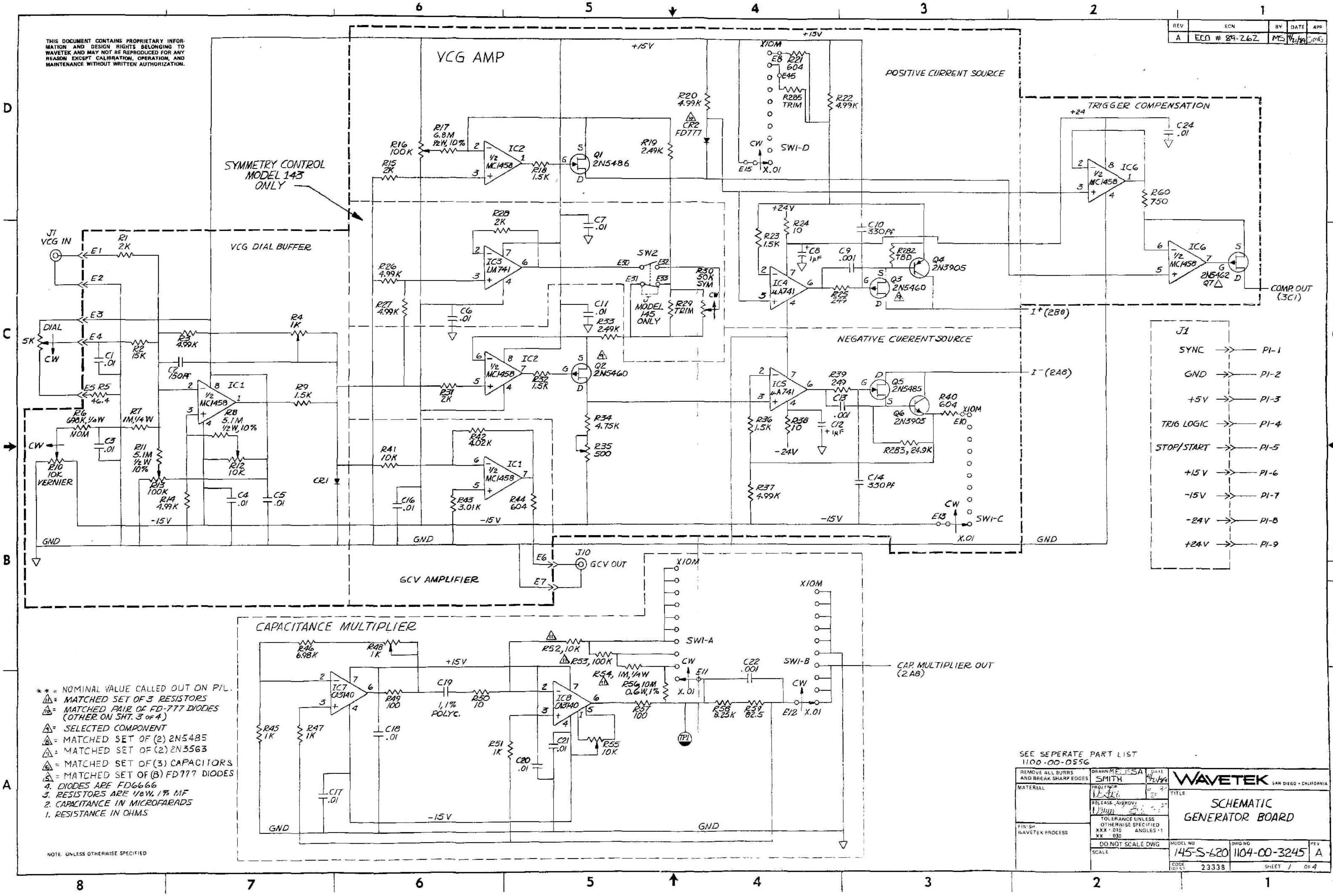


MADE FROM 0100-00-0565-3G

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	TITLE
	RELEASE APPROV	PCA, TRIG/PULSE BD
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	MODEL NO 145 / DWG NO 1100-00-0565 / REV
	SCALE	CODE IDENT 23338 / SHEET OF



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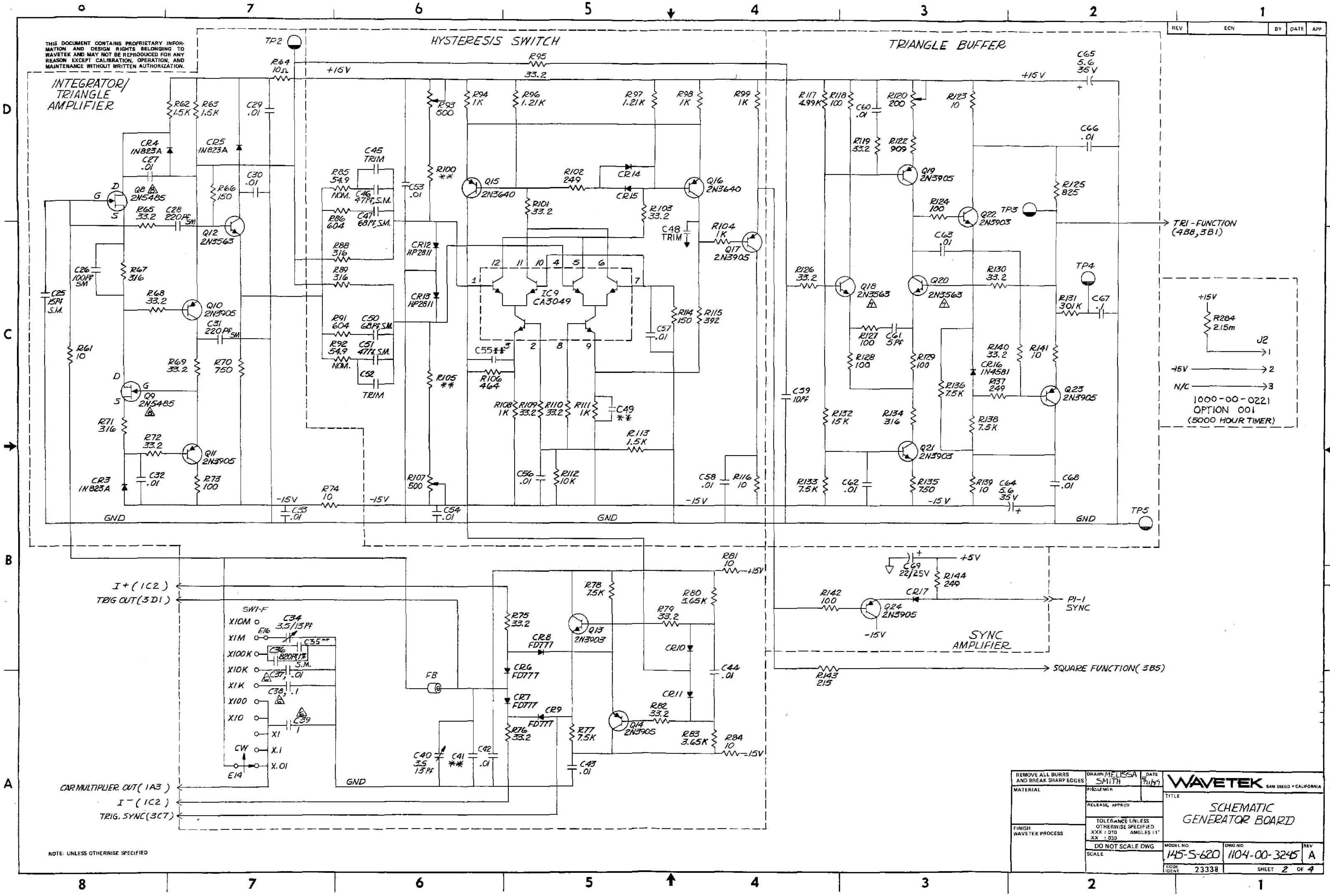
REV A ECO # 89-262 MS
VCG AMP
POSITIVE CURRENT SOURCE
TRIGGER COMPENSATION
SYMMETRY CONTROL MODEL 143 ONLY
VCG DIAL BUFFER
NEGATIVE CURRENT SOURCE
GCV AMPLIFIER
CAPACITANCE MULTIPLIER
J1 VCG IN
J10 GCV OUT
COMP. OUT (3C1)
I+ (2B8)
I− (2A8)
CAP. MULTIPLIER OUT (2A8)
MODEL 145 ONLY
J1
SYNC → P1-1
GND → P1-2
+5V → P1-3
TRIG LOGIC → P1-4
STOP/START → P1-5
+15V → P1-6
−15V → P1-7
−24V → P1-8
+24V → P1-9
** = NOMINAL VALUE CALLED OUT ON P/L.
1 = MATCHED SET OF 3 RESISTORS
2 = MATCHED PAIR OF FD-777 DIODES (OTHER ON SHT. 3 OF 4)
3 = SELECTED COMPONENT
4 = MATCHED SET OF (2) 2N5485
5 = MATCHED SET OF (2) 2N3563
6 = MATCHED SET OF (3) CAPACITORS
7 = MATCHED SET OF (8) FD777 DIODES
4. DIODES ARE FD6666
3. RESISTORS ARE 1/8W, 1% MF
2. CAPACITANCE IN MICROFARADS
1. RESISTANCE IN OHMS
NOTE: UNLESS OTHERWISE SPECIFIED
SEE SEPERATE PART LIST 1100-00-0556
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN MELISSA SMITH
TOLERANCE UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DWG
WAVETEK SAN DIEGO • CALIFORNIA
SCHEMATIC GENERATOR BOARD
MODEL NO 145-S-620
DWG NO 1104-00-3245
REV A
CODE IDENT 23338
SHEET 1 OF 4



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INTEGRATOR/ TRIANGLE AMPLIFIER
HYSTERESIS SWITCH
TRIANGLE BUFFER
SYNC AMPLIFIER
TRI-FUNCTION (4B8,3B1)
SQUARE FUNCTION (3B5)
P1-1 SYNC
I+ (1C2)
TRIG OUT (3D1)
CAR MULTIPLIER OUT (1A3)
I− (1C2)
TRIG. SYNC (3C7)
SW1-F
IC9 CA3049
+15V
R284 2.15m
J2
N/C
1000-00-0221
OPTION 001
(5000 HOUR TIMER)
GND
−15V
NOTE: UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN MELISSA SMITH
TOLERANCE UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DWG
WAVETEK SAN DIEGO • CALIFORNIA
SCHEMATIC GENERATOR BOARD
MODEL NO. 145-S-620
DWG NO. 1104-00-3245
REV A
CODE IDENT 23338
SHEET 2 OF 4

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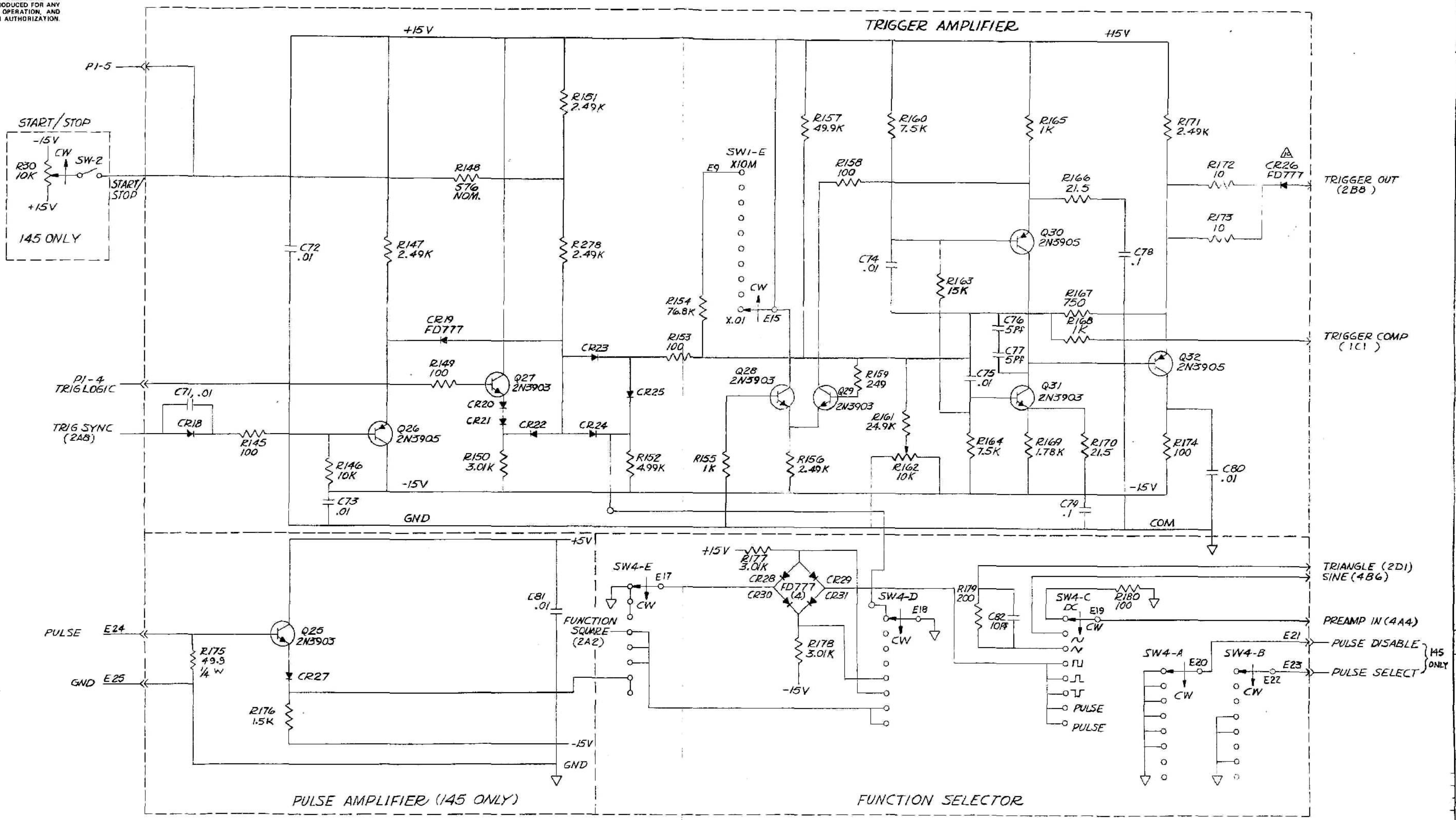

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN		WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL			TITLE: SCHEMATIC GENERATOR BOARD
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED		
	DO NOT SCALE DWG		145-S-620 / DWG NO 1104-00-3245 / REV A
			23338 / SHEET 3 OF 4

NOTE: UNLESS OTHERWISE SPECIFIED

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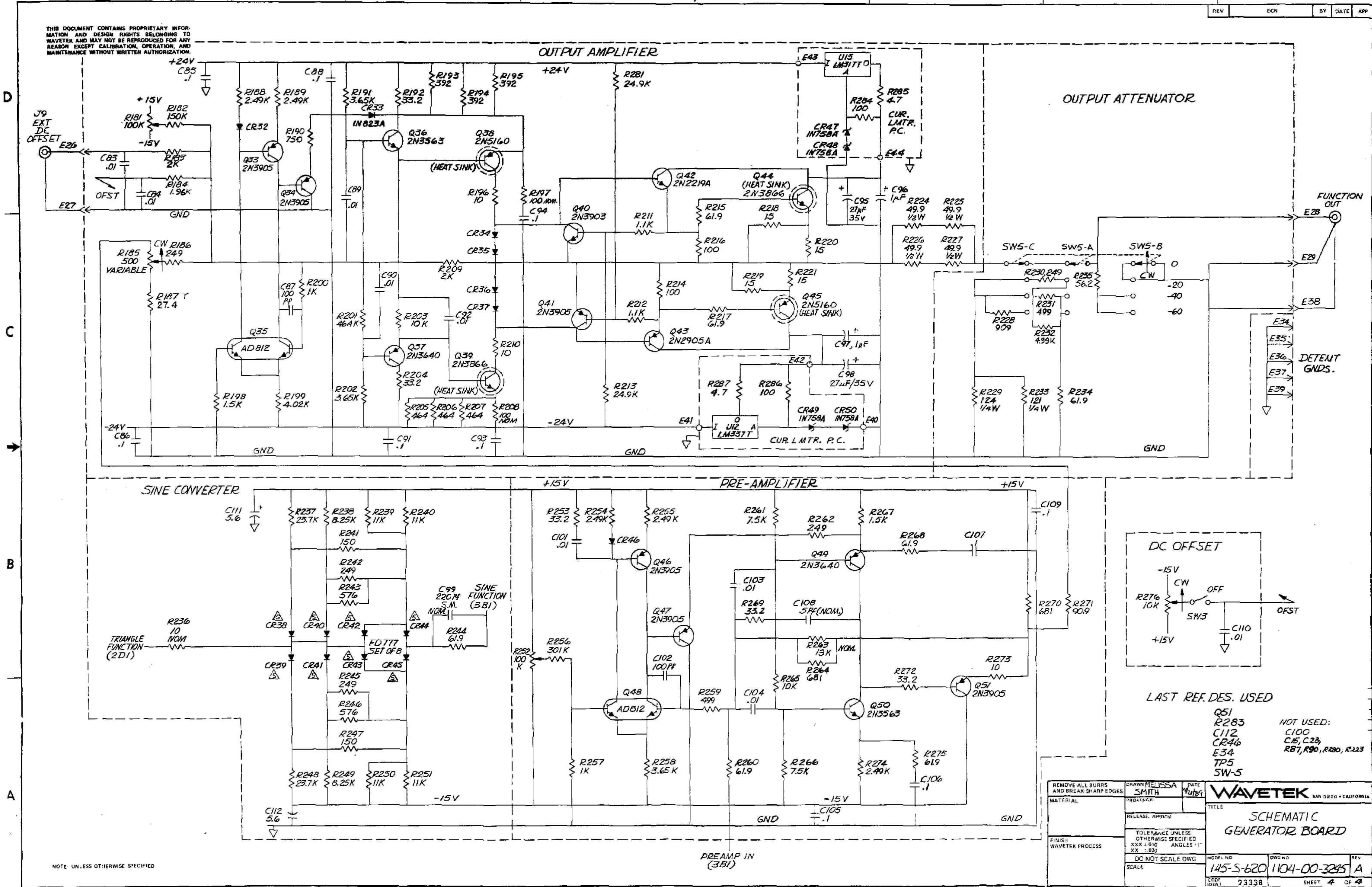

NOTE: UNLESS OTHERWISE SPECIFIED

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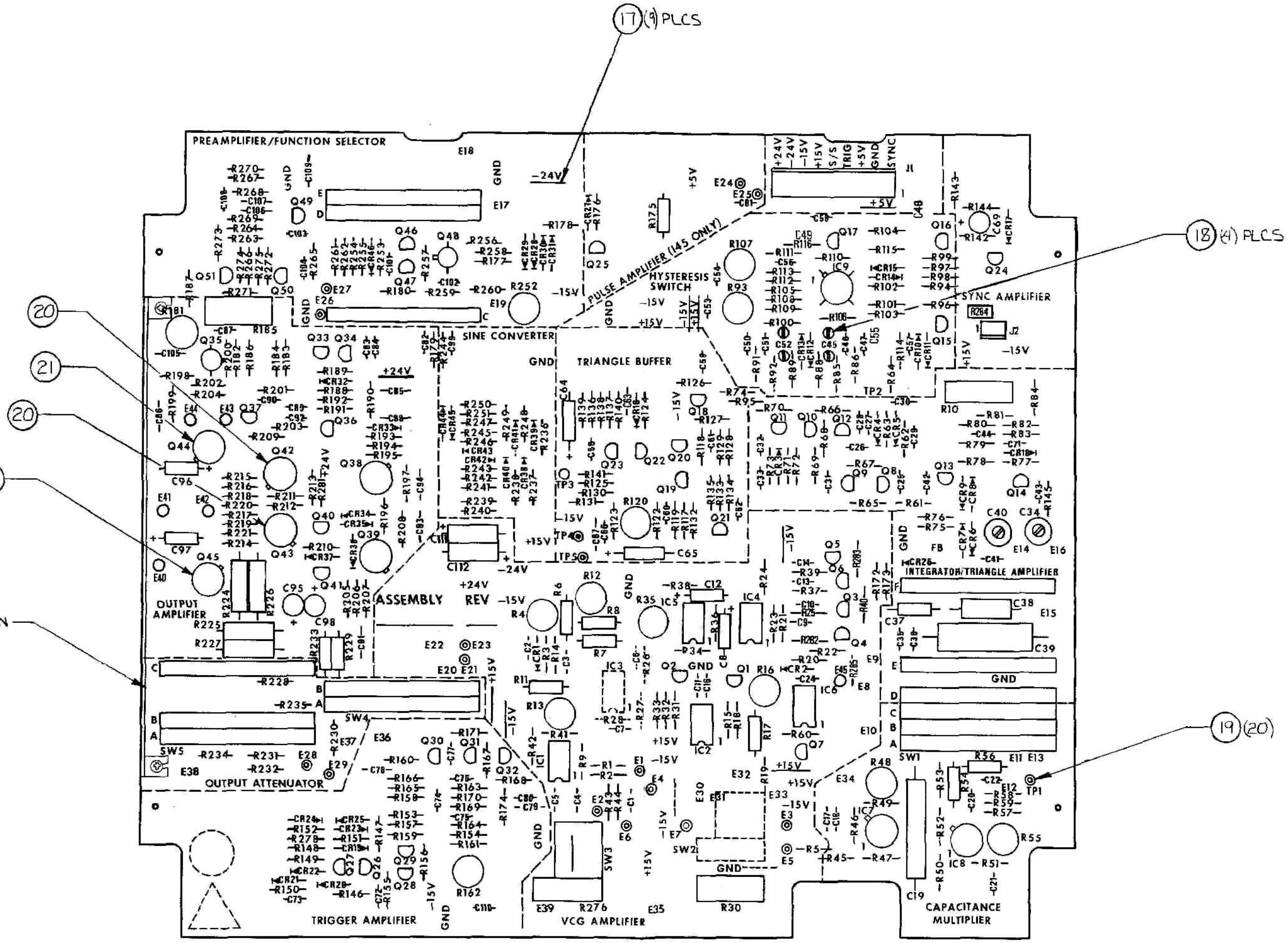
REV	ECO	BY	DATE	APP
A	ECO # 89-262	MS	[illegible]	DMB



FOR INSTALLATION SEE SHT 3 of 3 (REF: #12)

⚠ TURN TO FULL COUNTER CLOCKWISE POSITION THEN TURN BACK CLOCKWISE ONE POSITION TO INSTALL BOTH STOPS.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MELISSA SMITH	DATE [illegible]	WAVETEK SAN DIEGO CALIFORNIA
MATERIAL	CHECKED D. Buzzell	6/24/89	TITLE ASSEMBLY GENERATOR BOARD
	PROJ. ENGR [signature]	6/23/89	
FINISH WAVETEK PROCESS	RELEASE APPROV [signature]	6/23/89	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SIZE D · FSCM NO 23338 · DWG. NO. 1101-00-3245 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL 145 S 620 · SHEET 1 OF 3

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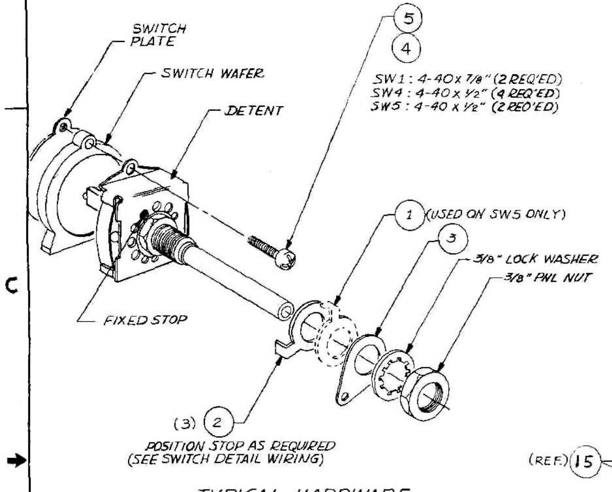
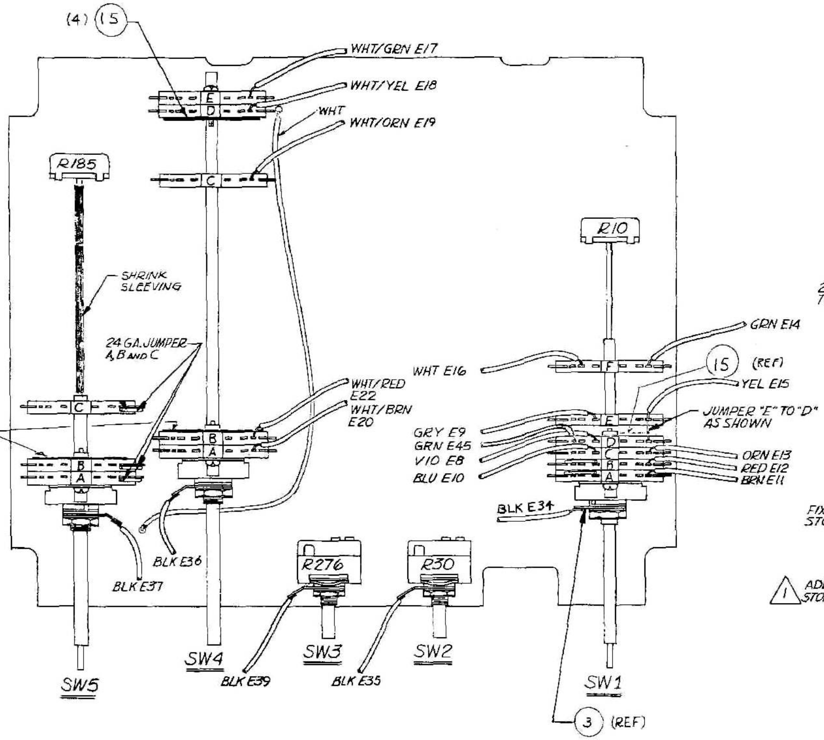
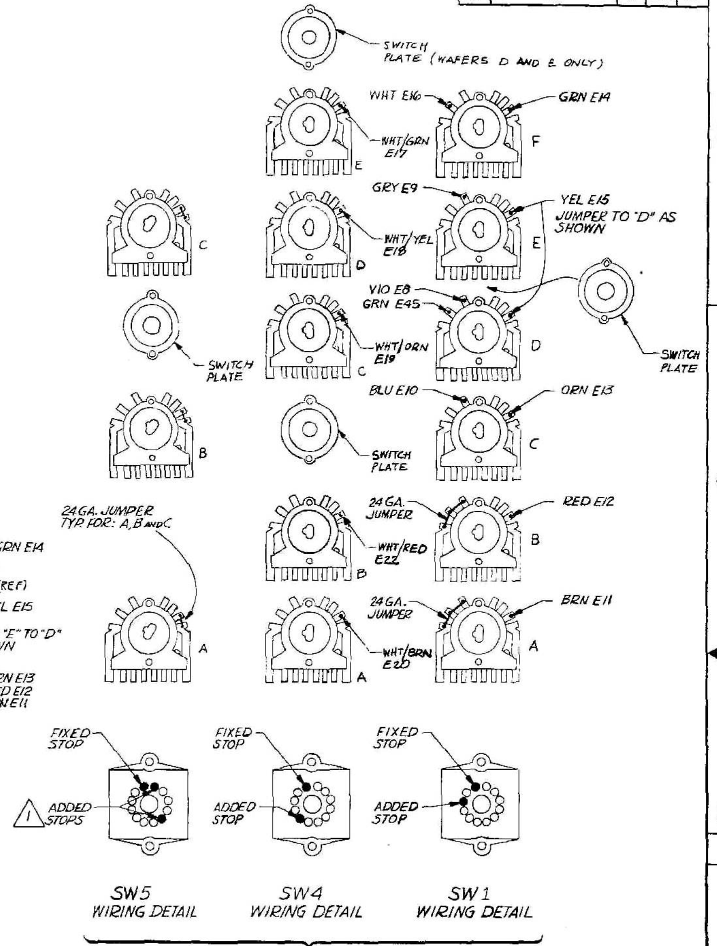
REV	ECN	BY	DATE	APP



TYPICAL HARDWARE STACK-UP





DETENT SHOWN FROM FRONT VIEW IN FULL COUNTER CLOCKWISE POSSITION

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MELISSA SMITH	DATE 4/21/89	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE ASSEMBLY GENERATOR BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		MODEL NO 145-S-620 · DWG NO 1101-00-3245 · REV A
	DO NOT SCALE DWG · SCALE		CODE IDENT 23338 · SHEET 2 OF 3