TELEQUIPMENT

OSCILLOSCOPE

TYPE D61

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CHAPTER 1
SPECIFICATION

1.1 VERTICAL SYSTEM

Operating Modes	Channel 1 Channel 2 Channels 1 & 2 Alternate (at time/div speeds between 1 ms and 0.5μs) Chop (100 kHz approx. at time/div between 500 ms and 2 ms and on EXT X) X–Y
3 dB bandwidth	
D.C. coupled	D.C. – 10 MHz
A.C. coupled	2 Hz – 10 MHz
Risetime	35 ns
Max. amplitude	5 div at 10 MHz
X–Y	Via CH1 with CH2 input selected via TIME/DIV switch as horizontal amplifier
Bandwidth (3 dB)	D.C. – 1 MHz
Deflection factors	
Calibrated (9 ranges 1, 2 & 5 sequence)	10 mV/div – 5 V/div ± 5%
Input impedance	1 MΩ and 35 pF in parallel
Maximum input	400 V peak

1.2 HORIZONTAL SYSTEM

Sweep generator rates	
(19 ranges 1, 2 & 5 sequence)	500 ms – 0.5 μs/div ± 5%
X5 magnification	$\geqslant$ 200 ns/div ± 7% 100 ns/div ± 10%
External horizontal amplifier	
3 dB bandwidth	2 Hz – 1 MHz
Deflection factor	100 mV/div approximately
Input impedance	1 MΩ and 10 pF in parallel

1.3 TRIGGER

Level	Variable Variable with auto free running in absence of trigger signal
Coupling	A.C. or TV field for sweep ranges up to 100 μs/div and TV line from 50 μs/div to 0.5 μs/div
Source	CH1, CH2 or external. All positive or negative

Sensitivity	
Internal	
40 Hz – 1 MHz	0.5 div, falling 1 div at 10 MHz
External	
40 Hz – 1 MHz	100 mV
1 MHz – 10 MHz	1 V

1.4 CATHODE RAY TUBE (CRT)

Display area	8 x 10 cm
Phosphor	
Standard	P31
Special order	P7
Overall accelerating potential	3.5 kV

1.5 OUTPUTS FRONT PANEL

Calibrator peak to peak	500 mV squarewave ± 2% at supply frequency
Probe test	2.5 V approx. rectangular pulse at sweep repetition rate and sweep width.

1.6 POWER SUPPLY

Voltage Model 1	100 – 120 in 10 V steps
Voltage Model 2	200 – 240 in 20 V steps
Frequency	48 – 400 Hz
Consumption	25 VA

1.7 SIZE

Height	280 mm
Width	160 mm
Depth	420 mm

1.8 WEIGHT

6.5 Kg

1.9 COOLING

Convection

1.10 TEMPERATURE LIMITS, ambient

Operating	–15 to +40°C
Non-operating	–25 to +70°C

CHAPTER 3

CIRCUIT DESCRIPTION

3.0 ATTENUATOR AND VERTICAL INPUT AMPLIFIER Figures 1A & 1B

CH1 and CH2 are identical and the following description covers both channels.

The input to the attenuator is connected via C901 to the input socket SK901 on AC, directly to the input socket on DC or to ground on GND. The capacity compensated attenuator is switched by S902 wafer 1 in steps of 100, 10 and 1 and the output is fed to the gate of TR601 via C601 and R602 which, together with D601, protect the input against overloads up to ± 400 V. TR601 is a F.E.T. source follower whose output DC level is adjusted to zero by R604 and R608. The output is then attenuated in steps of 5, 2 and 1 selected by S902 wafer 2 F and fed to the base of TR603 which together with TR604 forms a longtailed pair. The diodes D602 and D603 in the emitters increase the signal handling capacity without affecting the change in gain which remains directly proportional to current and, therefore, to supply voltage. This compensates for the CRT sensitivity which is inversely proportional to supply voltage and hence the overall vertical sensitivity remains independent of supply voltage. Vertical shift is fed to the base of TR604. The gain of the channel is set up by R613 which controls the total stage emitter current. The collector currents of TR603 and TR604 pass through thermal compensating networks R611, C602 and R614, C603 and also through grounded base stage TR602 to the output stages. TR602 isolates the channel switching waveforms from the input circuit.

3.1 VERTICAL OUTPUT AMPLIFIER Figure 2

The collector currents of the selected channel pass through diodes D637 and D638 for Channel 1, or D642 and D643 for Channel 2, to the bases of shunt feedback stages TR633 and TR636. The outputs of TR633 and TR636 are fed to the bases of TR634 and TR635, a longtailed pair whose collectors feed the Y plates of the CRT. C641 and R671 in the emitter circuit are adjusted for the best pulse response and TH631 compensates for the temperature coefficient of the input stages. The appropriate channel is selected either manually by S631 and S632 which are ganged to the vertical shift controls, or automatically by the Chop/Alternate circuit TR631 and TR632. On EXT X and Time/Div speeds of 2 ms/div and slower, TR631 and TR632 operate as a free-running multivibrator at a frequency of approx. 100 kHz. When TR632 conducts D635 and D636 conduct and turn off D637 and D638 thus disconnecting Channel 1. Conversely when TR631 conducts D639 and D641 conduct and turn off D642 and D643 thus disconnecting Channel 2. C632 and C634 feed pulses to the unblanking amplifier to blank out the trace during the transitions. On Time/Div speeds above 2 ms/div, TR631 and TR632 operate as a bistable whose state is changed at the end of each timebase sweep by an edge from the emitter of TR34. The network L631, C640, R640 in CH1 and L632, C649, R669 in CH2 delay the transitions until the trace is blanked. The vertical output amplifier current supplies the +13 V line which is decoupled by C645 and also the +7.5 V line which is stabilized by zener diode D644. The +7.5 V is used as a reference for the −7.5 V line which is a shunt stabilizer circuit consisting of TR637, R659, R666, R667 and R668. R658 compensates for variations in the −13 V line and reduces the effect of supply voltage variations on the −7.5 V line.

3.2 TRIGGER CIRCUIT Figures 3 & 4

This consists of a longtailed pair TR23 and TR25 similar to the Vertical Amplifier input stage but with temperature compensation in its emitter circuit. On the CH2 position the input is connected to CH2 and on EXT X position via C20, C21, C22 and R23 to the TRIG/EXT X socket. On all other positions of the Time/Div switch the input is connected to S20 which selects either the EXT TRIG Socket, CH1 or CH2 signal. The output from the appropriate collector, selected either by the Polarity switch S21 or the Time/Div switch S1, is connected via diode D27 or D31 to the emitter of common base stage TR26. The collector of TR26 is connected via D54, D33 and D34 to the input of the Horizontal Amplifier on CH2 and EXT X positions of the Time/Div switch S1. On other positions of the Time/Div switch the collector of TR26 is AC coupled via D32 to the base of TR21, a shunt feedback stage whose output swing is limited by diodes D21, D22 and D23. The output of TR21 is fed to the Schmitt trigger circuit, TR22 and TR24, which provides a constant amplitude trigger signal to the timebase and bright line auto circuit on the AC position of S22. On the TV position of S22, TR22 is converted to a sync separator and TR24 on TIME/DIV speeds slower than 100 µs has a long time constant in the emitter circuit which provides positive differentiated field pulses of much greater amplitude than the line pulses. The timebase therefore triggers on the field pulses. On TIME/DIV speeds faster than 100 µs, the emitter time constant is reduced by R50 so that the differentiated field and line pulses are of equal amplitude and the timebase therefore triggers at line frequency.

3.3 TIMEBASE, UNBLANKING AND BRIGHT LINE AUTO CIRCUIT Figure 4

3.3.1 The differentiated positive pulse from the trigger circuit is fed via D36 to the base of TR27 which together with TR29 forms a bistable. The positive pulse turns on TR27 which in turn cuts off the clamping transistor TR34. The timebase, a F.E.T. Miller circuit, then runs up linearly charging up the hold-off capacitor via D47 and resetting the bistable via R114. When TR27 cuts off, TR34 conducts and discharges the timing capacitor until D45 conducts and reduces the current in TR34 to the value required by the timing resistor. At this point the flyback stops. During the flyback the hold-off capacitor discharges through R114 until D48 conducts. At this point the action is complete and the timebase can be triggered by the next triggering pulse.

3.3.2 If the Trig level control is in the Auto position and no trigger pulses are present, TR35 and D49 conduct and reduce the potential at the anode of D48. This allows the hold-off capacitor to discharge further and re-trigger the bistable. The timebase then free-runs. If trigger pulses are present at the anode of D43 the positive pulses trigger the monostable TR32 and TR35. When triggered at frequencies above about 10 Hz the average collector current of TR35 is low and D49 is cut off returning the timebase to the normal triggered condition.

3.3.3 The collector current of TR29 which is cut off during the sweep is fed to the input of TR28. The collector of TR28 goes negative at the beginning of the sweep until diode D38 conducts and clamps the collector potential at about 3 V, thus unblanking the sweep. When TR29 conducts at the end of the sweep TR28 collector goes positive blanking the trace. On chop positions of the sweep negative edges from the chop circuit are fed to the base of TR28 to blank the trace during the transitions.

3.4 HORIZONTAL AMPLIFIER Figure 3

This consists of a shunt feedback stage TR31 with switched feedback resistors to give X5 expansion. The sweep and horizontal shift currents are mixed at the input of the shunt feedback stage and the output is fed to a longtailed pair, TR33 and TR37, which feeds the horizontal deflection plates of the CRT. D44 clamps the collector of TR33 and prevents it from bottoming.

On the EXT X and CH2 positions of the Time/Div switch the input of TR31 is switched to the collector of TR26 via D33, D34 and D54 and the X5 feedback resistor is shorted out by diodes D33, D34, D35 and D37. The trace is then deflected horizontally via the EXT X socket or from Channel 2. On these positions the gate of TR36 is connected to the cathode of D47 which clamps the output of the timebase at about +1 V and turns off TR29 thus unblanking the trace.

3.5 CRT CIRCUIT AND POWER SUPPLY Figure 5

The supply voltage is fed via the power ON/OFF switch S401, the fuse FS401 and the voltage selector SK401 to the appropriate primary tapping on T401.

3.5.1 The −13 V line is obtained from a full wave rectifier circuit consisting of D405, D406, C402 and R403.

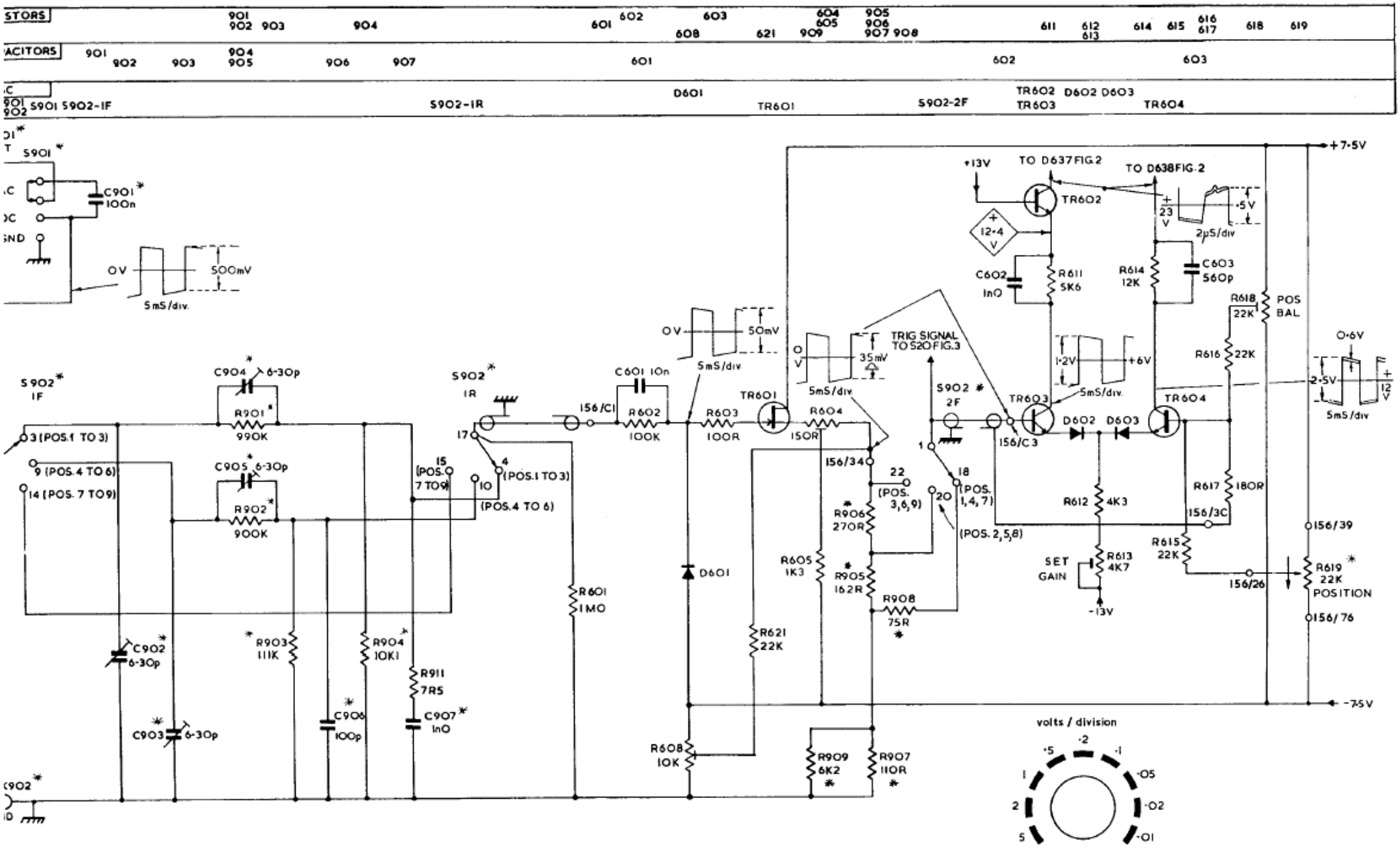
3.5.2 The +117 V line is obtained from a bridge rectifier D401, D402, D403 and D404 with reservoir capacitor C403 and smoothed by R406 and C408 to provide the +110 V line and by R407 and C406 to provide the +80V line.

3.5.3 The −1050 V line is obtained from a half wave rectifier circuit consisting of D407, C409, C411 and C412.

3.5.4 The +2500 V line is obtained from a voltage doubler circuit consisting of D408, D409, C401 and C404.

3.5.5 The calibrator circuit provides a 0.5 V squarewave at supply frequency. It is produced by a diode switching circuit in which a current derived from the stabilized −7.5 V line is passed through D413 and R408 during negative half cycles of the AC voltage from the 13 V transformer winding. On positive half cycles D413 is cut off and the current passes through D412 and R402. The output voltage is set by R405. The temperature coefficient of the diode D413 is compensated for by the negative temperature coefficient of the output resistor R408 giving an output voltage which is nominally independent of temperature.

3.5.6 The grid voltage of the CRT is derived from a zener diode connected between the CRT cathode and the −1050 V supply. The voltage is varied by the Intensity control R301. The Intensity of the trace may be varied by signals fed via the Z Mod socket SK301 and C301 to the grid of the CRT.

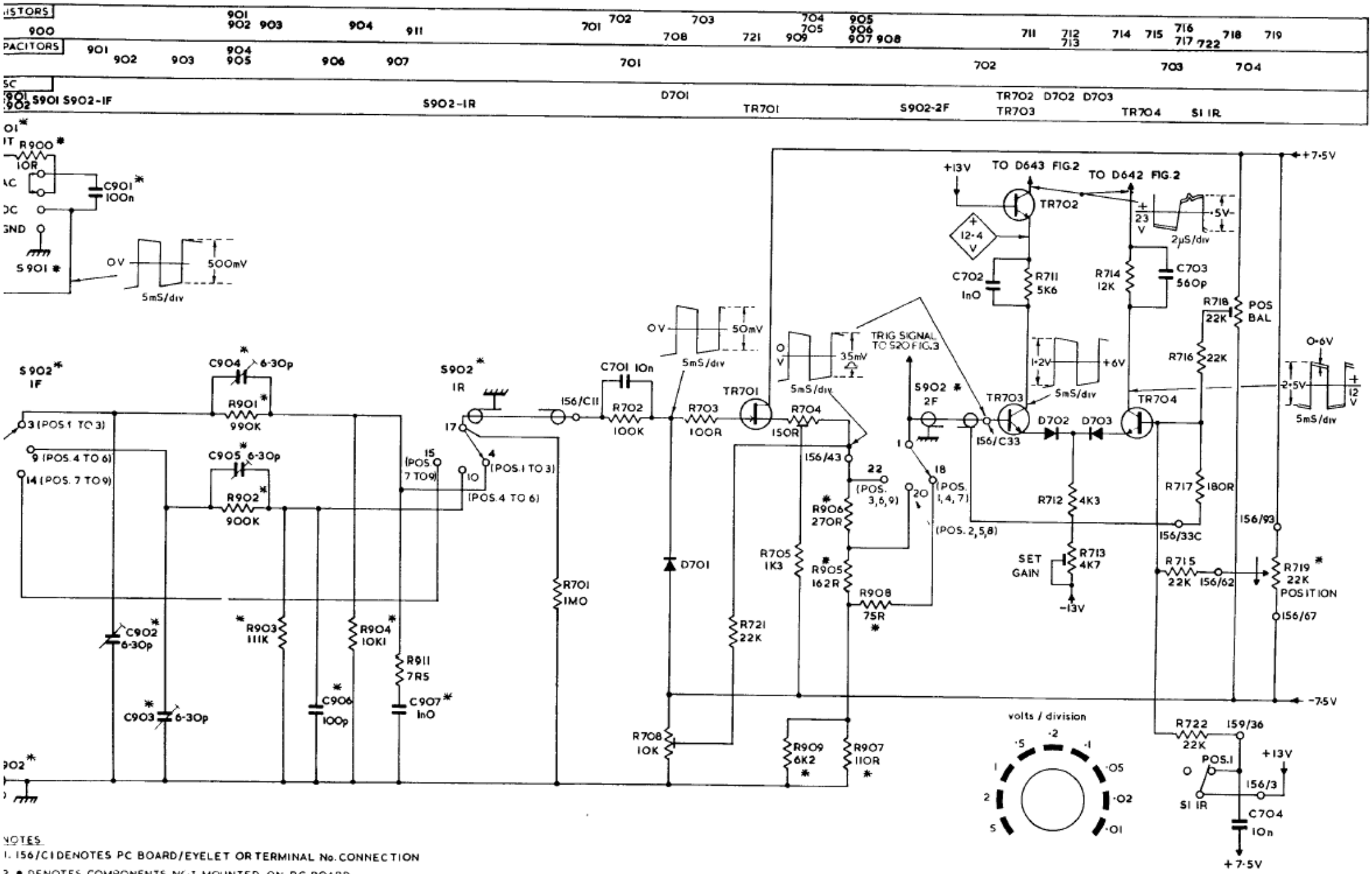


NOTES.

1. 156/C1 DENOTES PC BOARD/EYELET OR TERMINAL No. CONNECTION
2. * DENOTES COMPONENTS NOT MOUNTED ON PC BOARD.
3. SWITCH IS SHOWN IN FULLY ANTICLOCKWISE POSITION.
4. ALL WAVEFORMS MEASURED WITH CAL WAVEFORM FED TO BOTH CHANNELS VOLTS/DIV SET TO 0·1 TRIG SELECTOR TO CH.1 AND TIME/DIV. TO 2mS

VOLTS/DIV. SWITCH. & VERT. INPUT AMPLIFIER CH.1 D61

FIG. 1A



NOTES

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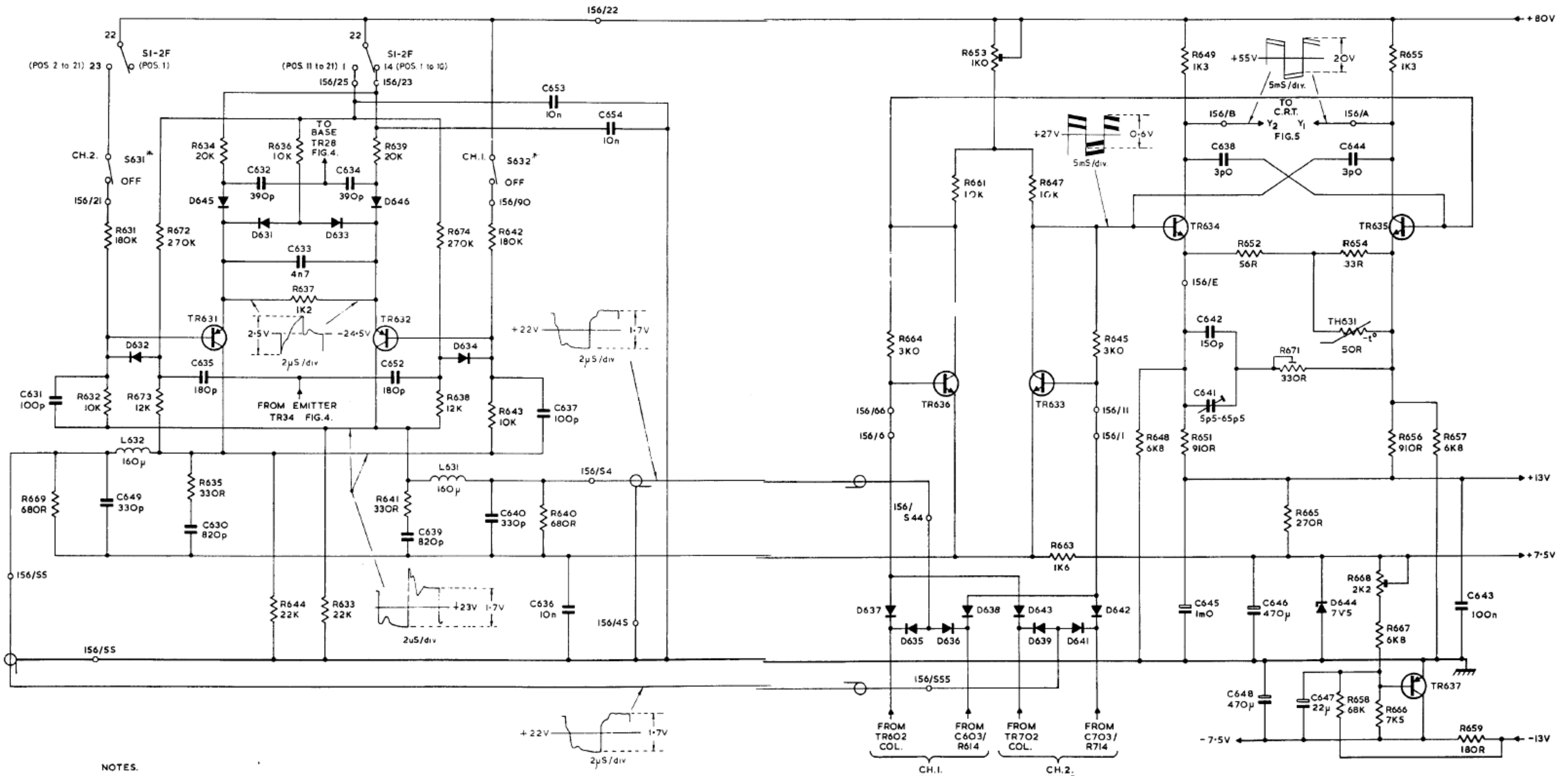
VOLTS/DIV. SWITCH. & VERT. INPUT AMPLIFIER CH.2 D61

FIG. 1B

RESISTORS	669 631 632 672 673 635 634 644 633 636 637 639 641 642 643 674 638 640 664 661 653 647 663 645 648 649 651 652 671 665 654 658 655 656 668 667 666 657 659
CAPACITORS	631 649 630 635 632 633 634 652 639 640 637 653 636 654 645 638 642 641 646 648 647 644 643
MISC.	L632 S1-2F S631 D632 TR631 D645 D631 D633 TR632 S1-2F D646 L631 D634 S632 TR636 D635 D637 D638 D636 TR633 D643 D641 D639 D642 TR634 TH631 TR635 TR637 D644

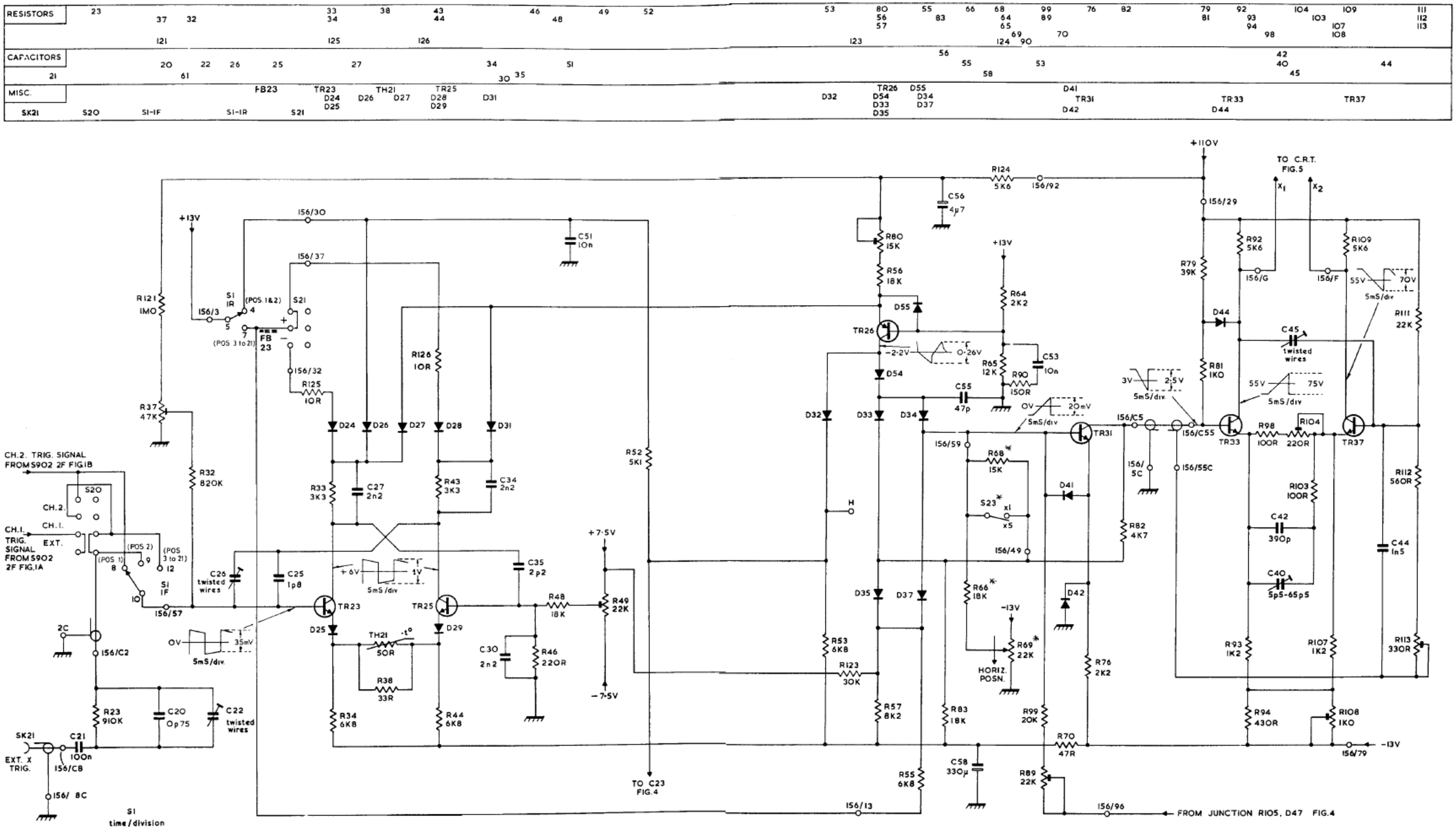


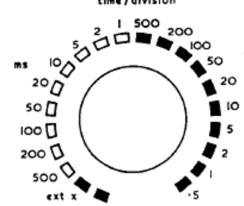
NOTES.

1. * DENOTES COMPONENTS NOT MOUNTED ON P.C. BOARD.
2. 156/SS DENOTES P.C. BOARD/EYELET OR TERMINAL No. CONNECTION.
3. ALL WAVEFORMS MEASURED WITH CAL WAVEFORM FED TO BOTH CHANNELS VOLTS/DIV SET TO 0·1 TRIG SELECTOR TO CH.1 AND TIME/DIV TO 2mS.

'Y' AMPLIFIER - D61

FIG. 2



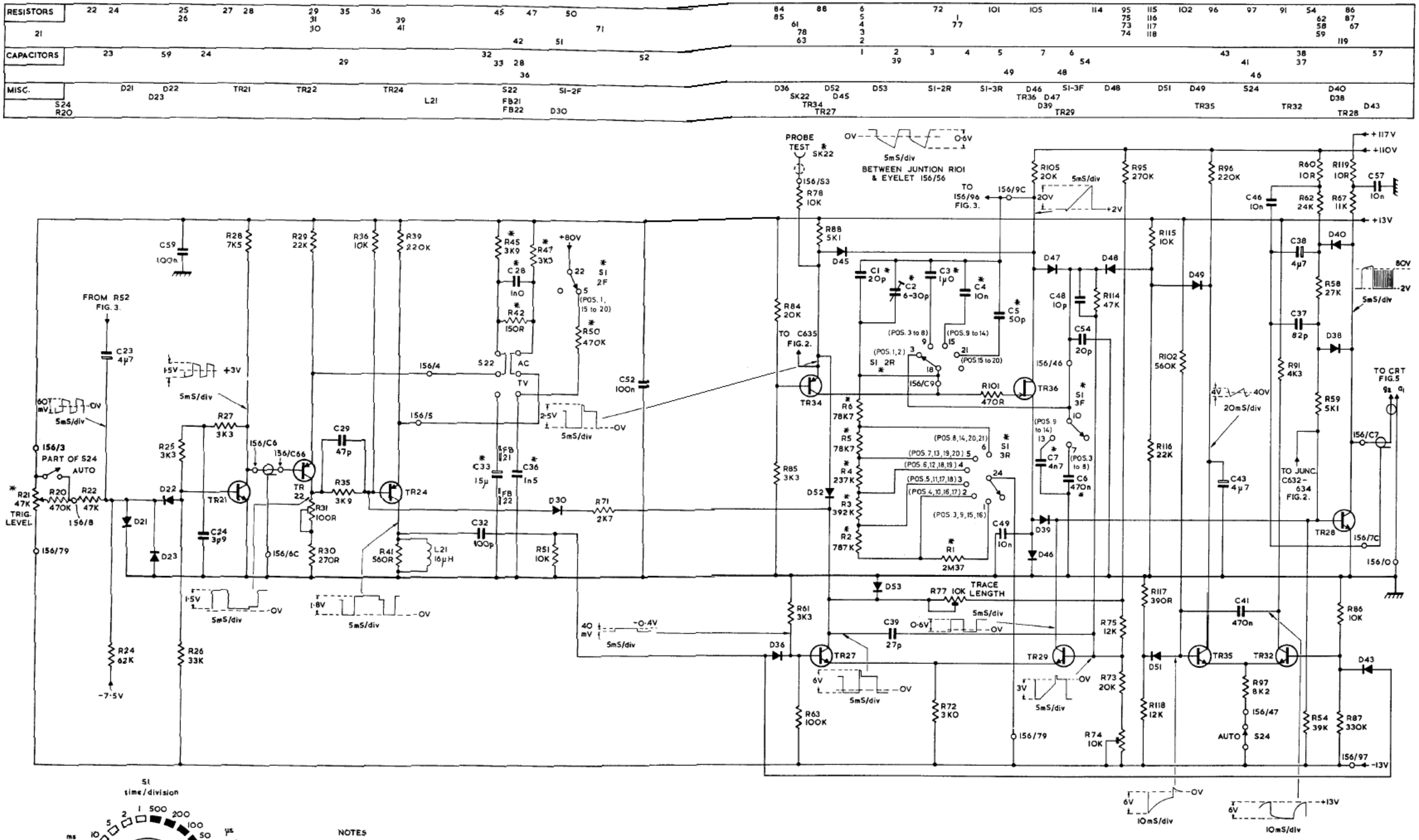


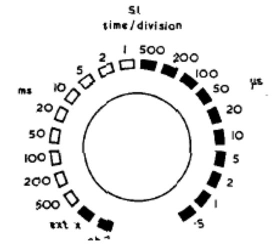
NOTES.

1. ✱ DENOTES COMPONENTS NOT MOUNTED ON P.C. BOARD.
2. 156/C8 DENOTES P.C. BOARD/EYELET OR TERMINAL No. CONNECTION
3. SWITCH SHOWN IN FULLY ANTI-CLOCKWISE POSITION.
4. FOR S1 SWITCH WAFERS SEE FIG.6.
5. ALL WAVEFORMS MEASURED WITH CAL WAVEFORM FED TO BOTH CHANNELS VOLTS/DIV. TO 0·1 TRIG SELECTOR TO CH.1 AND TIME/DIV TO 2mS.

TRIG INPUT & HORIZONTAL AMP D61

FIG. 3.





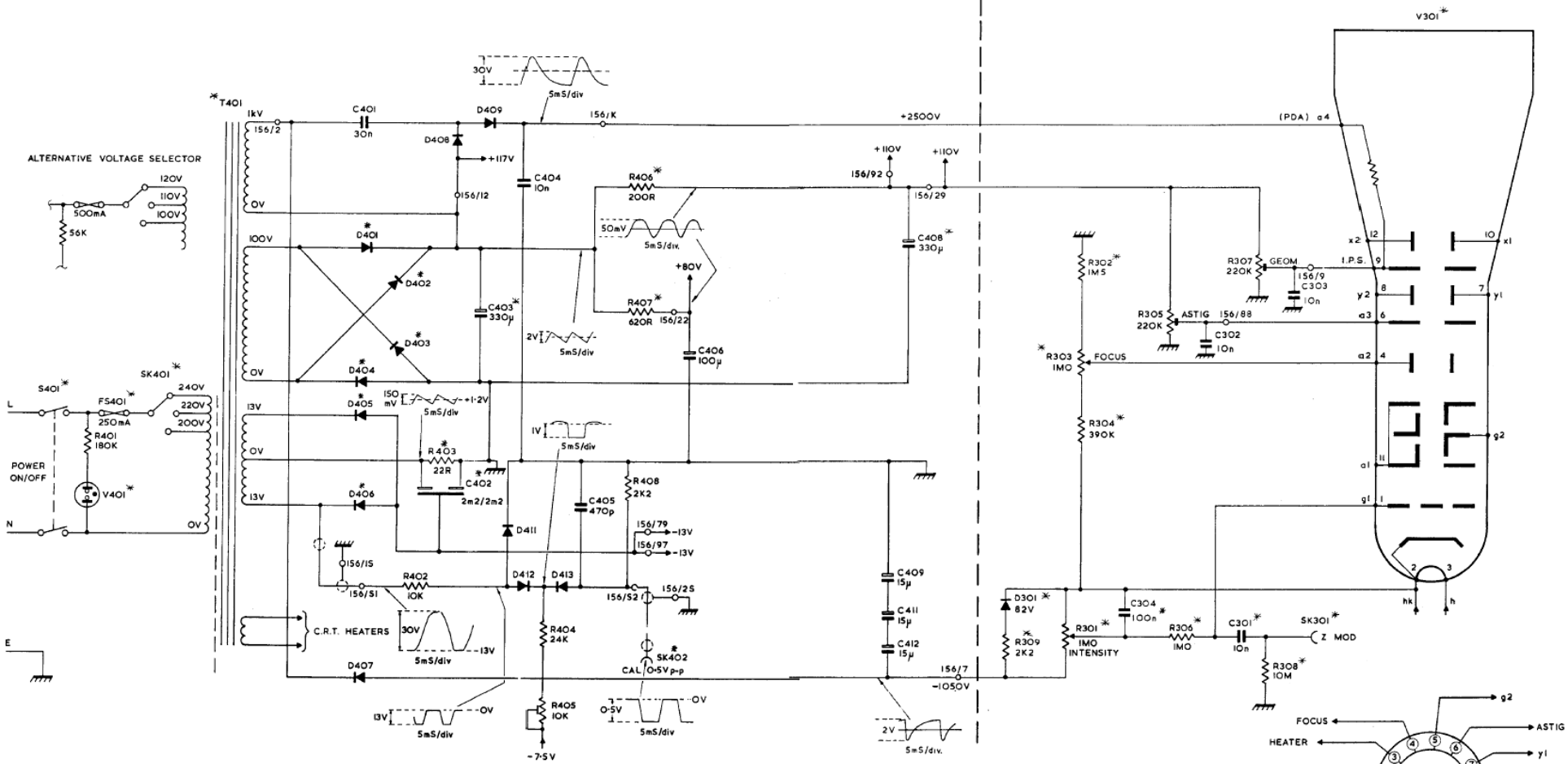
NOTES

1. * DENOTES COMPONENTS NOT MOUNTED ON P.C. BOARD.
2. 156/6C DENOTES P.C. BOARD/EYELET OR TERMINAL No. CONN.
3. SWITCH SHOWN IN FULLY ANTI-CLOCKWISE POSITION.
4. FOR S1 SWITCH WAFERS SEE FIG. 6.
5. ALL WAVEFORMS MEASURED WITH CAL. WAVEFORM FED TO BOTH CHANNELS, VOLTS/DIV. SET TO 0·1, AND TRIG. SELECTOR TO CH.1. AND TIME/DIV. TO 2mS.
6. PUSH PULL SWITCH S24 IS SHOWN IN THE OUT POSITION

SWEEP GENERATOR D61

FIG. 4.

RESISTORS	401 402 403 404 405 406 407 408	301 302 303 304 305 306 307 308 309
CAPACITORS	401 402 403 404 405 406 408 409 411 412	301 302 303 304
MISC.	V401 FS401 SK401 T401 D401 D402 D403 D404 D405 D406 D407 D408 D409 D411 D412 D413 SK402 S401	D301 SK301 V301



NOTES.

1. * DENOTES COMPONENTS NOT MOUNTED ON P.C. BOARD.
2. 156/2 DENOTES P.C. BOARD/EYELET OR TERMINAL No. CONNECTION
3. ALL WAVEFORMS MEASURED WITH CAL. WAVEFORM FED TO BOTH CHANNELS, VOLTS/DIV. SET TO 0·1, AND TRIG. SELECTOR TO CH.1. AND TIME/DIV. TO 2mS.

POWER SUPPLY & C.R.T. — D61