TEKTRONIX®

INSTRUCTION MANUAL

Tektronix, Inc.
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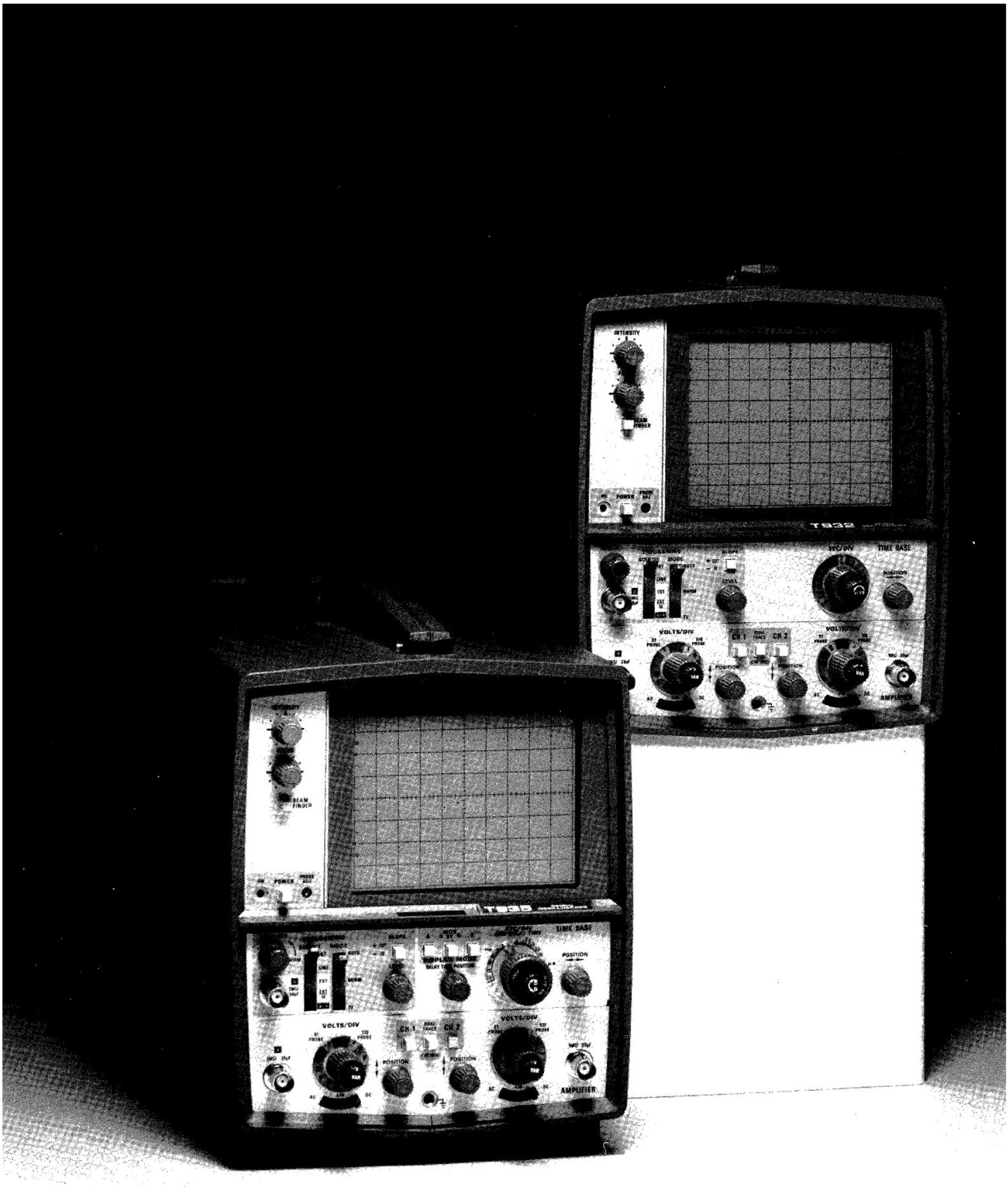

INTENSITY
BEAM FINDER
POWER
T932
TIME BASE
SEC/DIV
POSITION
LEVEL
VOLTS/DIV
CH 1
CH 2
AMPLIFIER
T935
TIME BASE
VOLTS/DIV
CH 1
CH 2
POSITION
AMPLIFIER

SPECIFICATIONS

This manual includes instructions for both the T932 and the T935 portable oscilloscopes. The T932 is a 35 MHz, dual trace oscilloscope and the T935 is a 35 MHz, dual trace oscilloscope capable of delayed sweep operation. The Vertical Amplifier provides calibrated deflection factors from 2 mV to 10 V/div. The Time Base provides stable triggering over the full bandwidth of the Vertical Amplifier and provides calibrated sweep rates from 0.5 s/div to 0.1 μs/div. A variable X1 to X10 magnifier extends the maximum sweep rate to 20 ns/div.

The following instrument specifications apply over an ambient temperature range of 0 to +45° C unless otherwise indicated. The adjustment procedures in Section 4, when performed completely, allow the T932 and the T935 to meet the electrical specifications listed in Table 1-1.

TABLE 1-1

Electrical

Characteristic	Performance Requirement
A. DISPLAY	
Probe Adjust Output	
Voltage (0° C to +40° C)	Approximately 0.5 V.
Repetition Rate	Approximately 1 kHz.
Z-Axis Input	
Sensitivity	5 volt signal causes a noticeable decrease in intensity.
Signal Polarity	Positive going from ground.
Usable Frequency Range	Dc to 5 MHz.
Maximum Input Voltage	30 V (dc + peak ac) 30 V p-p at 1 kHz or less.
Input Impedance	Approximately 10 kΩ.
Power Source	
Line Voltage Ranges (ac,rms)	
120 V Range	HI—108 to 132 V. LO—90 to 110 V.
240 V Range	HI—216 to 250 V. LO—198 to 242 V.
Line Frequency	50 to 60 Hz.
Maximum Power Consumption	36 W, 0.35 A at 60 Hz, 120 V line.
CRT Display	
Display Area	8 x 10 cm.
Trace Rotation Range	Adequate to align trace with horizontal center line.
Standard Phosophor	P31.
Nominal Accelerating Potential	12,400 V.

Characteristic	Performance Requirement
B. VERTICAL AMPLIFIER	
Deflection Factor	
Range	2 mV/div to 10 V/div; 12 steps in a 1-2-5 sequence.
Accuracy	
+20° C to +30° C	Within 3%.
0° C to +45° C	Within 4%.
Uncalibrated (VAR) Range	Continuously variable between settings. Extends deflection factor to at least 25 V/div (at least 2.5:1).
Frequency Response	
Bandwidth	Dc to at least 35 MHz (5 division reference signal centered vertically from a 25 Ω source with VOLTS/DIV VAR control in calibrated detent).
Chopped Mode Repetition Rate	Approximately 250 kHz.
Input Resistance	Approximately 1 MΩ.
Maximum Input Voltage	
DC Coupled	400 V (dc + peak ac). 800 V (p-p ac) at 1 kHz or less.
AC Coupled	400 V (dc + peak ac). 800 V (p-p ac) at 1 kHz or less.

TABLE 1-1 (cont)

Characteristic	Performance Requirement
C. TIME BASE	
Sweep Rate	
Calibrated Range (T932)	0.5 s/div to 0.1 μs/div; 21 steps in a 1-2-5 sequence. Variable X1 to X10 magnifier extends maximum sweep rate to 10 ns/div.
Calibrated Range (T935)	0.5 s to 0.1 μs/div; 21 steps in a 1-2-5 sequence. Variable X1 to X10 magnifier extends maximum sweep rate to 10 ns/div.
A Sweep	
B Sweep	50 ms to 0.1 μs/div; 18 steps in a 1-2-5 sequence. Variable X1 to X10 magnifier extends maximum sweep rate to 10 ns/div.
Accuracy	Accuracy specification applies over center 8 divisions. Exclude first 50 ns of sweep for both magnified and unmagnified sweep rates and anything beyond the 100th magnified division.
+20° C to +30° C	
Unmagnified	Within 3%.
Magnified	Within 5%.
0° C to +45° C	
Unmagnified	Within 4%.
Magnified	Within 6%.
Variable Magnifier	10:1 (In the X10 position, the sweep speed is one tenth of the SEC/DIV switch setting.).
Delay Time Position Range (T935)	0.5 to 10 div.
Delay Time Jitter (T935)	One part or less in 10,000 (0.01%) of one tenth of the SEC/DIV switch setting.

Characteristic	Performance Requirement
C. TIME BASE (cont)	
X-Y Operation	
Deflection Factor	
Variable Magnifier	
X10	Approximately 100 mV/div.
X1	Approximately 1 V/div.
X-Axis Bandwidth	Dc to at least 2 MHz with 10 div reference signal.
Input Resistance	Approximately 1 MΩ.
Input Capacitance	Approximately 30 pF.
Triggering	
Sensitivity	0.5 div internal or 100 mV external from 2 Hz to 2 MHz, increasing to 1.5 div internal or 150 mV external at 35 MHz.
TV Sync	Composite sync 1 div internal or 100 mV external (approximately 2.3 div or 230 mV of composite video).
External Trigger Input	
Maximum Input Voltage	400 V (dc + peak ac). 800 V (p-p ac) (1 kHz or less).
Input Resistance	Approximately 1 MΩ.
Input Capacitance	Approximately 30 pF.
Level Range	
EXT	+0.5 V to −0.5 V.
EXT 10	+5 V to −5V.

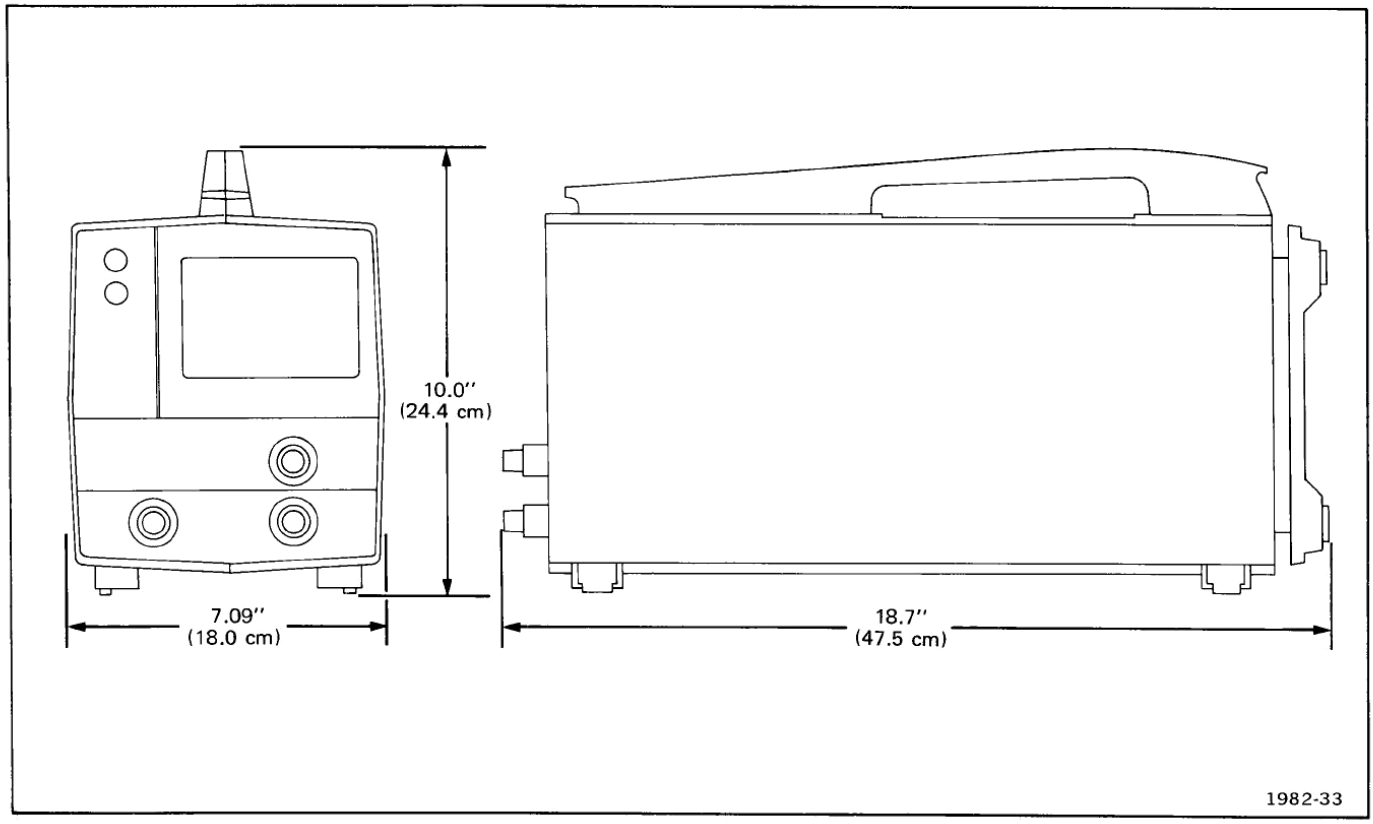


Fig. 1-2. T932/T935 dimensional drawing.

TABLE 1-2

Environmental

Characteristic	Performance Requirement
Temperature	
Storage	−55° C to +75° C.
Operating	0° C to +45° C.
Altitude	
Storage	To 50,000 ft.
Operating	To 15,000 ft. Maximum operating temperature decreases 1° C/1,000 ft. above 5,000 ft.

TABLE 1-3

Physical

Characteristic	Performance Requirement
Weight	
With Panel Cover, Accessories and Accessory Pouch	15.5 lbs. (7.0 kg).
Without Panel Cover, Accessories and Accessory Pouch	15.0 lbs. (6.8 kg).
Overall Dimensions	Refer to Fig. 1-2.

STANDARD ACCESSORIES

1	Instruction Manual	070-1983-01
2	Probes	010-6108-03

RECOMMENDED ACCESSORIES

NOTE

The following accessories have been selected from our catalog specifically for your instrument. They are listed as a convenience to help you meet your measurement needs. For detailed information and prices, refer to a Tektronix Products Catalog or contact your local Tektronix Field Representative.

COVERS

FRONT COVER: Protects the instrument front panel during transport or storage and provides storage for small accessories (probes, cables, etc.). Made of blue plastic to match the instrument case.

Order **016-0340-00**

PROTECTIVE WATERPROOF COVER: Blue vinyl cover provides protection for the entire oscilloscope during transport or storage.

Order **016-0361-00**

STAND

PORTABLE STAND: The Portable Stand sits on the floor and holds the instrument at an angle to provide easy viewing and access. Also provides storage for small accessories (probe, cables, etc.).

Order **209**

PROBES

P6101 GENERAL PURPOSE 1X VOLTAGE PROBE: Input capacitance is 54 picofarads (plus input capacitance of oscilloscope).

Order **010-6101-03**

P6062A SWITCHABLE 1X-10X VOLTAGE PROBE: Provides full bandwidth capabilities of T900-series instruments. Can be compensated to match the vertical input capacitance.

Order **010-6062-13**

P6009 GENERAL PURPOSE 100X VOLTAGE PROBE: Provides full bandwidth capabilities of T900-series instruments. Can be compensated to match the vertical input capacitance.

Order **010-0264-01**

P6015 GENERAL PURPOSE 1000X VOLTAGE PROBE: Provides full bandwidth capabilities of T900-series instruments. Can be compensated to match the vertical input capacitance.

Order **010-0172-00**

P6021 AC CURRENT PROBE: Provides a bandwidth from 120 Hz to the upper bandwidth of T900-series instruments. Spring-loaded slide opens (up to 0.150 inches) to allow measurement of current without breaking the circuit under test.

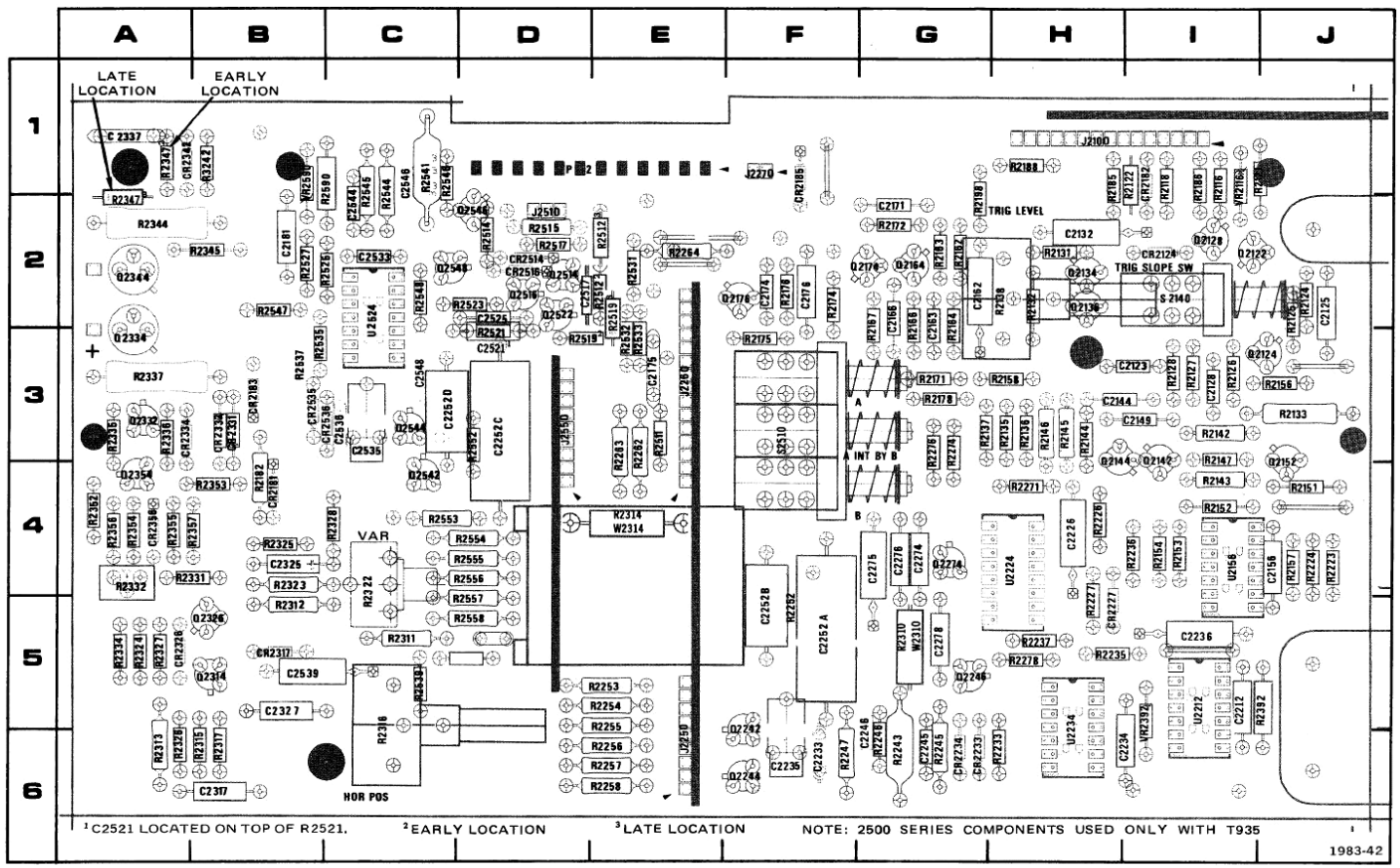
Order **015-0140-02**

CAMERAS

C-5A Option 3 Camera: Provides graticule illumination with xenon flash lamp powered by two AA penlight batteries. Recommended for, and molded to fit all bench version T900-series instruments. Fixed focus, fixed aperture *f*16 lens with 0.67 or 0.85 user adjustable magnification. Mechanical shutter with speeds of 1/5 to 1/25 s, plus bulb and time.

Order . . . . . **C-5A Option 3**

A12 HORIZ BAORD COMP LOC
& BLK DIAG CKT DESC



NOTE: ONLY A12 BOARD COMPONENTS ARE SHOWN SINCE OTHER BOARDS HAVE CIRCUIT NUMBERS MARKED ON BOARD.

Fig. 7-2. A12—Horizontal circuit board component locations.

*See Parts List for serial number ranges.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
C2123	3I	CR2535	3B	R2152	4I	R2332	4A
C2125	2J	CR2536	3B	R2153	4I	R2334	5A
C2128	3I			R2154	4I	R2335	3A
C2132	2H	J2100	1H	R2156	3I	R2336	3A
C2144	3H	J2250	6E	R2157	4J	R2337	3A
C2149	3F	J2260	3E	R2158	3H	R2342	1B
C2156	4J	J2270	1F	R2162	2G	R2344	2A
C2162	2G	J2510	2D	R2163	2G	R2345	2B
C2163	2G	J2550	3D	R2164	2G	R2347	1A[2,3]
C2166	2G			R2166	2G	R2352	4A
C2171	2G	P2	1D	R2167	2G	R2353	4B
C2174	2F			R2171	3G	R2354	4A
C2175	3E	Q2122	2I	R2172	2G	R2355	4A
C2176	2F	Q2124	3J	R2174	2F	R2356	4A
C2181	2B	Q2128	2I	R2175	3F	R2357	4B
C2212	5I	Q2134	2H	R2176	2F	R2392	5J
C2226	4H	Q2136	2H	R2178	3G	R2511	3E
C2233	6F	Q2142	3I	R2182	4B	R2512	2E
C2234	6I	Q2144	3H	R2185	1H	R2514	2D
C2235	6F	Q2152	3J	R2186	1I	R2515	2D
C2236	5I	Q2164	2G	R2188	1H	R2517	2D
C2245	6G	Q2174	2G	R2198	2G	R2519	3D[2]
C2246*	6G	Q2176	2F	R2223	4J	R2519	2E[3]
C2252A	5F	Q2242	6F	R2224	4J	R2521	3D
C2252B	5F	Q2244	6F	R2226	4H	R2523	2D
C2252C	3D	Q2246	5G	R2227	5H	R2525	2B
C2252D	3C	Q2274	4G	R2233	6H	R2527	2B
C2274	4G	Q2314	5B	R2235	5H	R2531	2E
C2275	4G	Q2326	5B	R2236	4I	R2532	3E
C2276	4G	Q2332	3A	R2237	5H	R2533	3E
C2278	5G	Q2334	3A	R2243	6G	R2535	3B
C2317	6B	Q2344	2A	R2245	6G	R2537	3B
C2325	4B	Q2354	4A	R2246	6G	R2539	5C
C2327	5B	Q2514	2D	R2247	6F	R2541	1C
C2337	1A	Q2516	2D	R2252	5F	R2544	1C
C2517*	2D	Q2522	2D	R2253	5E	R2545	1C
C2521[1]	3D	Q2542	4C	R2254	5E	R2546	1C
C2525	2D	Q2544	3C	R2255	5E	R2547	2B
C2533	2C	Q2546	2D	R2256	6E	R2548	2C
C2535	3C	Q2548	2C	R2257	6E	R2552	3D
C2536	3C			R2258	6E	R2553	4C
C2546*	1C	R2116	1I	R2262	3E	R2554	4D
C2539	5B	R2118	1I	R2263	3E	R2555	4D
C2544	2C	R2121	1J	R2264	2E	R2556	4D
C2546	1C	R2122*	1I	R2271	4H	R2557	5D
C2548	3C	R2124	2J	R2274	3G	R2558	5D
		R2125	2J	R2276	3G	R2590	1B
CR2124	2I	R2126	3I	R2278	5H		
CR2181	4B	R2127	3I	R2310*	5G	S2140	2I
CR2182	1I	R2128	3I	R2311	5C	S2510	3F
CR2183	3B	R2131	2H	R2312	5B		
CR2185	1F	R2132	2H	R2313	6A	U2212	5I
CR2227	5H	R2133	3J	R2314*	4E	U2224	4H
CR2233	6G	R2135	3H	R2315	6B	U2234	6H
CR2234	6G	R2136	3H	R2316	6C	U2156	4I
CR2317	5B	R2137	3G	R2317	6B	U2524	2C
CR2326	5A	R2138	2H	R2322	4C		
CR2331	3B	R2142	3I	R2323	4B	VR2116	1I
CR2332	3B	R2143	4I	R2324	5A	VR2392	5I
CR2334	3A	R2144	3H	R2325	4B	VR2590	1B
CR2342	1A	R2145	3H	R2326	6A	W2310	5G
CR2356	4A	R2146	3H	R2327	5A	W2314	4E
CR2514	2D	R2147	3I	R2328	4C		
CR2516	2D	R2151	4J	R2331	4B		

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I.1

BLOCK DIAGRAM DESCRIPTION

VERTICAL INPUT

Signals to be displayed on the crt are applied to either the channel 1 (Y) or channel 2 input connector. The input signals are amplified by the preamplifier circuits. Each preamplifier circuit includes separate input coupling, attenuators, gain switching, variable attenuators, balance, and gain adjustments.

A Trigger Pickoff circuit in each channel supplies a sample of the vertical input signal to the Trigger Input Amplifier via the Trigger Switching circuit and the SOURCE switch.

VERTICAL SWITCHING

The Vertical Mode switch selects which channel supplies the trigger signal. The vertical signal passes through the Input Buffer Amplifier circuit which isolates the preamplifier circuits from the Delay Line Driver. The output of each Input Buffer Amplifier is connected to the Delay Line Driver through a Diode Gate circuit. The Diode Gate circuits are controlled by the Vertical Switching circuit to select the channel(s) to be displayed. An output from the Vertical Switching circuit (through the Chop Blanking Pulse Generator) is connected to the Z Axis Amplifier to blank switching transients in the chop mode (SEC/DIV at 1 ms or slower). A sync pulse from the sweep (via the Alternate Sync Pulse Amplifier) switches the display between channels at the end of each sweep in the alternate mode (SEC/DIV at .5 ms or faster).

VERTICAL AMPLIFIER

The vertical input signal goes from the Delay Line Driver through the Delay Line to the Vertical Output Amplifier. The Delay Line provides approximately 120 ns delay in the vertical signal. This allows the sweep generator circuit time to initiate a sweep before the vertical signal reaches the crt vertical deflection plates. The Vertical Output Amplifier provides final amplification of the signal to drive the crt vertical deflection plates. One section of the BEAM FINDER switch, when pressed, causes the display to compress vertically to aid in locating off-screen displays. Another section affects the horizontal circuitry.

TRIGGER

The Trigger circuit produces a logic triggering signal to trigger the sweep. Trigger signals are selected by the SOURCE switch from three sources: external trigger (via the External Trigger Input Buffer circuit), vertical amplifier input signal (internal), or the line voltage at the secondary of T700. (No trigger signal is produced during X-Y operation.)

The selected trigger signal is amplified and inverted by the Trigger Input Amplifier. The trigger signal passes through coupling capacitor, C2132, to the Trigger Level Comparator, which determines the voltage level (on the trigger waveform) at which triggering occurs. The SLOPE switch determines whether the sweep triggers on the positive-going or negative-going portion of the trigger signal. For TV signals, the SLOPE switch determines whether the sweep triggers from positive or negative sync polarity. The Trigger Level comparator also supplies a signal to the TV Sync Separator circuit.

Two Schmitt Trigger circuits produce the logic trigger signal; one is for conventional trigger signals and the other is for TV signals. The MODE switch selects which Schmitt Trigger circuit is operating.

A SWEEP AND HORIZONTAL AMPLIFIER

The A Sweep circuit, when triggered by the Trigger circuit, produces a linear sawtooth output signal to the Horizontal Amplifier. The slope of the sawtooth is controlled by the SEC/DIV switch. When the sawtooth output reaches a predetermined level, the Hold-off Circuit resets the A Sweep circuit, blanks the crt (through the Z Axis Amplifier) and prevents subsequent triggers from initiating another sweep until the sweep reset is completed.

The sawtooth output from the Sweep circuit is amplified by the Horizontal Output Amplifier circuit to produce horizontal deflection on the crt. When the SOURCE switch is in the X-Y position, the X signal, from the External Trigger Input Buffer, is applied to the Horizontal Amplifier. One section of the BEAM FINDER switch, when pressed, causes the display to compress horizontally to aid in locating off-screen displays.

B SWEEP

The B Sweep circuit produces a linear sawtooth output signal to the Horizontal Amplifier after a delay. The length of the delay is determined by the DELAY TIME POSITION control. The output signal from the A sweep circuit triggers the B sweep circuit. The DISPLAY MODE switch selects A, A INTEN BY B, or B (delayed) modes. In the A INTEN BY B mode, the B sweep intensifies a portion of the A sweep.

CRT CIRCUIT

The Z Axis Amplifer determines the crt intensity and blanking. The Z Axis Amplifier sums the current inputs from several sources: INTENSITY control, X-Y intensity limit, unblanking signal from sweep circuit, chop blanking signal from the Vertical Switching circuit, and EXT Z AXIS INPUT connector, J419.

Output of the Z Axis circuit controls the trace intensity through the HV circuit. The HV circuit provides the voltages (greater than 100 V) necessary for operation of the crt.

The Probe Adjust Generator provides a square-wave voltage output for checking voltage probes.

POWER SUPPLY

The Power Supply circuits provide the low-voltage power necessary for operation of the instrument.

HIGH-VOLTAGE REGULATOR

Transistors Q446-Q454 and associated circuitry control the output voltage of the High Voltage supply. Components R443 and C443 provide a slow start up for the high-voltage oscillator. When the instrument is turned on, the +100 V supply charges C443 through R443. The voltage increases until it is sufficient to forward bias CR443, holding the voltage at slightly above +8 volts. This forms the reference for the high-voltage regulator.

The resulting current in R444A (100 μA) turns on Q446 and Q454, providing base current for Q458. This starts the high voltage oscillator, causing a negative voltage to develop at the crt cathode.

Resistors R444B, C, D, and R468 sample the cathode voltage. The high voltage increases until the cathode voltage is −2000 V, At this point the current in R444B is approximately the same as the current in R444A with Q446 barely conducting.

Any change in the level at the base of Q446 produces an error signal at the collector of Q446, which is amplified by Q454 and applied to the base of Q458 through the feedback winding of T460. Regulation occurs as follows:

If the cathode voltage at the −2000 V point starts to go positive (less negative), this positive-going change is applied to the base of Q446. Q446 conducts harder, which in turn causes Q454 to conduct harder. This results in greater bias current to the base of Q458 through the feedback winding of T460. Now Q458 is biased closer to its conduction level so that it comes into conduction sooner to produce a larger induced voltage in the secondary of T460. This increased voltage appears as a more negative voltage at the crt cathode to correct the original positive-going change. By sampling the output from the crt cathode supply in this manner, the total output of the high-voltage supply is held relatively constant.

Components, R445 and C445, damp the response of the regulator against fast changes in the load such as when the crt is unblanked at the beginning of the sweep.

Resistors, R446, R453, and R457, help prevent instabilities in the high-voltage oscillator.

HIGH-VOLTAGE RECTIFIERS AND OUTPUT

The high-voltage transformer, T460, has 3 output windings. One winding provides about 6.3 V for the crt filament. The crt filament is referenced to the cathode voltage (≈−2 kV), preventing cathode-to-filament breakdown. A second winding provides high ac voltage to the multiplier, U460, to produce a 10 kV crt anode accelerating voltage. The same winding is tapped and rectified by CR465 to produce the dc voltage for the crt cathode. Components C465, R465, and C466 filter the dc voltage.

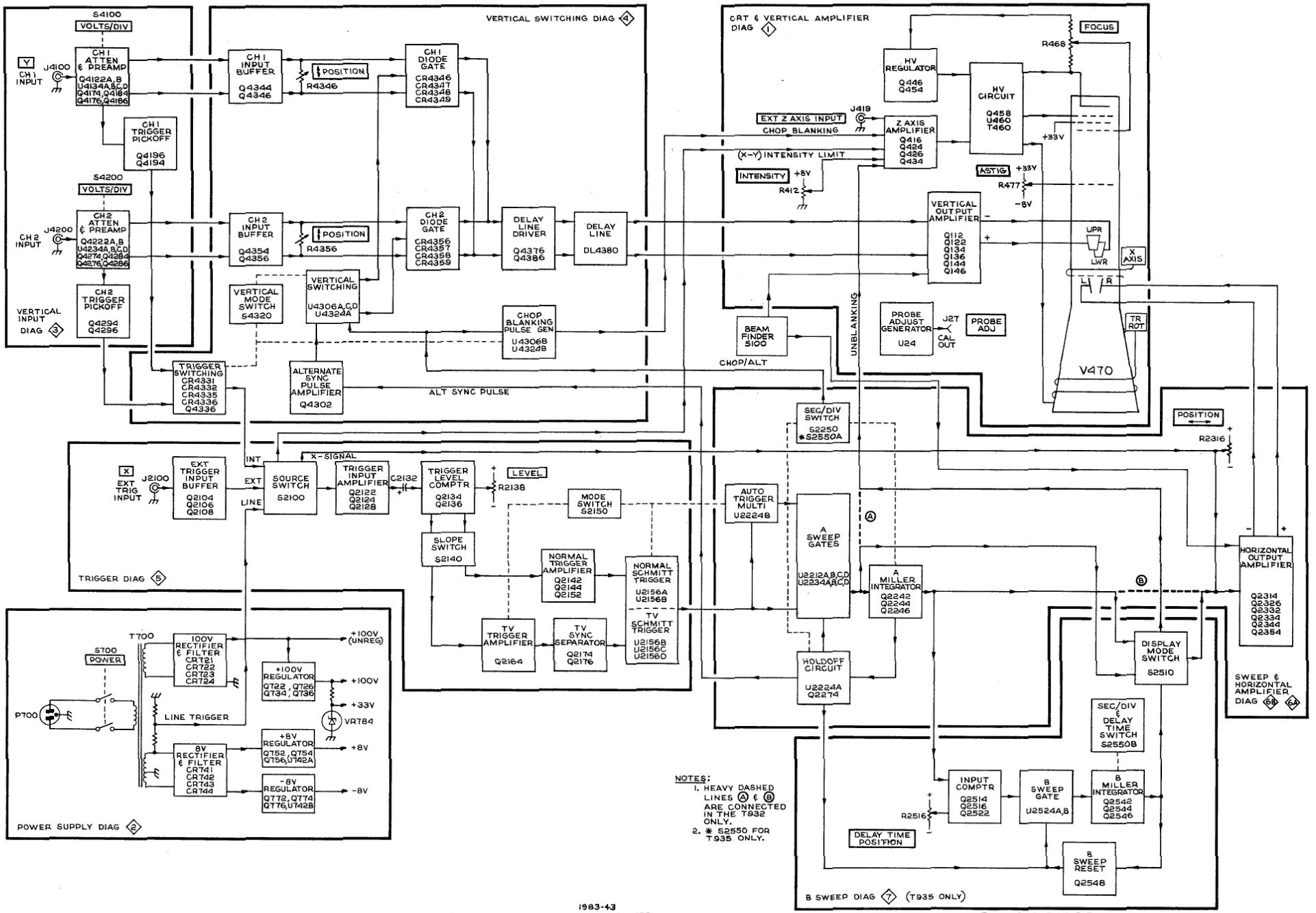
The third winding is used to control the crt intensity. Components CR463, C462, C463, C464, R462, and R463 rectify and filter the secondary voltage to provide approximately −2100 V which is applied to the crt grid. The entire winding is referenced to the output of the Z axis amplifier whose output voltage variations are used to control the crt intensity by varying the grid to cathode voltage. The dc path for the Z axis signal to the grid is through R462, CR463, R463 and the transformer winding. Resistor R462 isolates the transformer capacitance from the Z axis Amplifier. Capacitors C463 and C464 provide a path for fast changes in the Z axis output to the crt grid. Resistor R464 provides a discharge path for C462, C463, and C464. Glow lamps DS463 and DS465 prevent the grid-to-cathode voltage from rising high enough to cause breakdown within the crt during turn-on or when the cathode or grid is shorted to ground.

CRT CONTROL CIRCUITS

Crt display focus is controlled by FOCUS control R468. ASTIG adjustment R477, which is used in conjunction with the FOCUS control to provide a well-defined display, varies the voltage on the astigmatism grid. Geometry adjustment, R473, varies the voltage on the horizontal deflection plate shields to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field around the crt. Y axis adjustment, R474, controls the current through L470, which affects the crt beam after vertical deflection but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. Trace Rotation (TR ROT) adjustment, R472, controls the current through L472 and affects both vertical and horizontal rotation of the beam.

R475 and R476 provide the proper voltage for the vertical plate shield and R478 and C478 decouple the first accelerator electrode from the +33 V supply.



T932/T935

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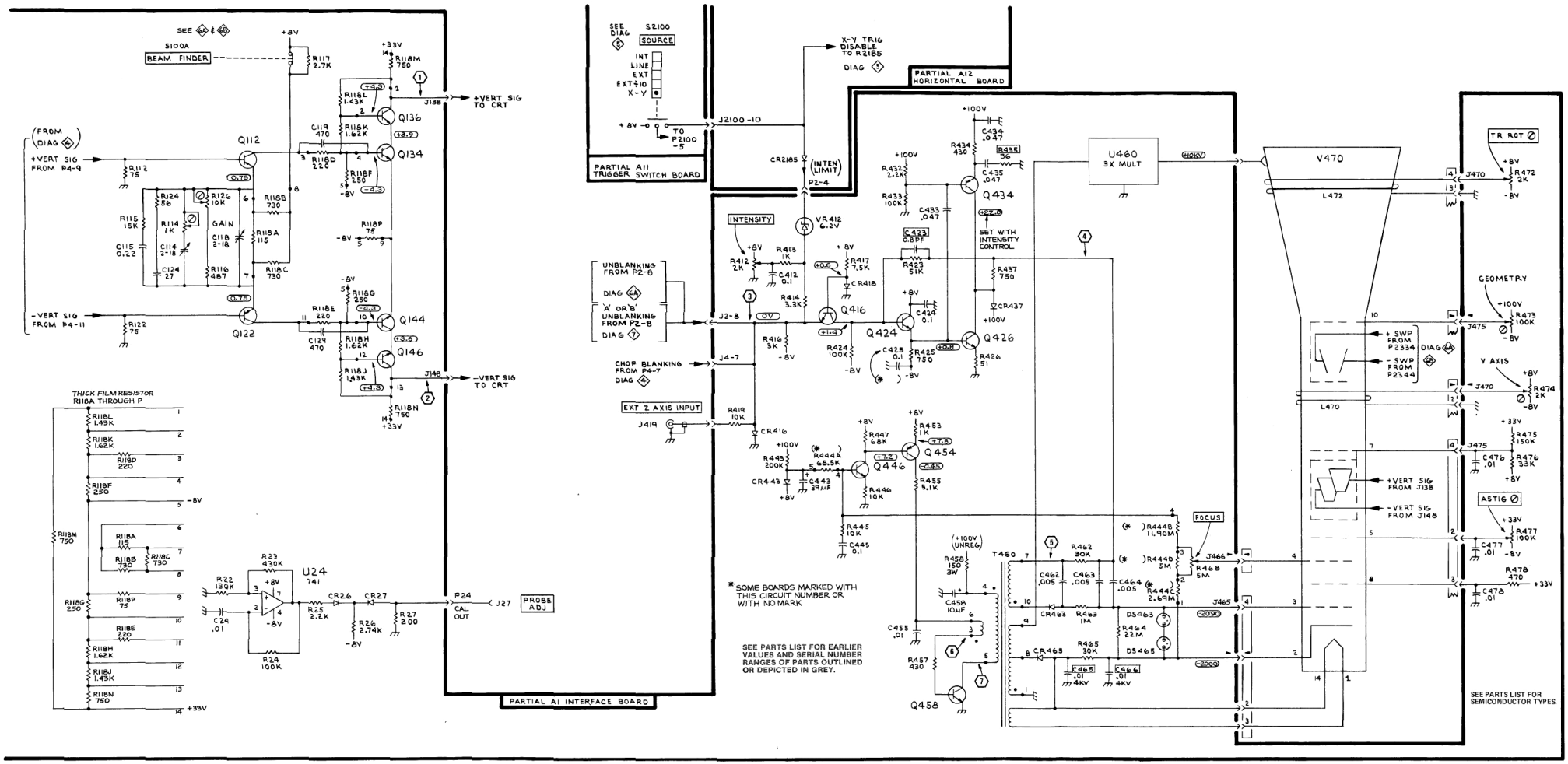
BLOCK DIAGRAM



CRT & VERTICAL AMPLIFIER 1

III.1

POWER SUPPLY CIRCUIT DESCRIPTION

POWER INPUT

AC power is applied to the primary of T700 though line fuse F700, POWER switch S700, Line Selector switch S701, and Range Selector switch S705.

The Line Selection switch, S701, connects the split primary windings of T700 in parallel for 120 V operation or in series for 240 V. When changing the nominal line voltage, also change the line fuse. See parts list for correct fuse values.

The Range Selector switch, S705, selects either LO (100 or 220 V) or HI (120 or 240 V) nominal line-voltage range.

SECONDARY CIRCUITS

The secondary circuit supplies four regulated voltages: −8 V, +8 V, +33 V, and +100 V.

Operational amplifiers U742A (+8 V supply) and U742B (−8 V supply) have differential inputs that monitor output voltage variations and provide correction signals to the series-regulating transistors. For example, suppose the +8 volt supply drops. This negative change is coupled to the inverting input of U742A through sense resistor R756, causing pin 7 to go positive. Since the voltage across VR746 remains essentially constant, Q754 and Q756 follow this change and raise the output voltage back to +8 volts. In the +100 volt supply, Q726 acts as the feedback amplifier with its base being the inverting input. The regulating action is the same as in the +8 and −8 volt supplies. Zener diode, VR762, provides a 5 volt reference for the −8 V supply, which in turn provides the reference for the +8 and +100 volt supplies. The series regulating elements in the +100 V and +8 V supplies are transistors Q734-Q736 and Q754-Q756. The series regulating element in the −8 V supply is a modified Darlington configuration consisting of Q774 and Q776. Current limiting circuits provide short-circuit protection for each regulated supply. The following describes the +8 V current-limiting circuit. The other current-limiting circuits operate similarly.

In the +8 V supply, Q752 is normally biased off. Under normal conditions, the base of Q752 is set at about +8 V. As the supply current increases, the voltage drop across R754 increases. Since the Q756 emitter-base diode voltage difference remains constant, the increasing voltage on Q756 emitter due to the R754 voltage drop causes a corresponding increase at the base of Q756. This voltage is applied to voltage divider R752 and R753, causing the base of Q752 to go more positive. When the supply current increases sufficiently beyond the normal operating current, Q752 turns on. The collector of Q752 moves in the negative direction, which begins turning off Q754-Q756 and creates a foldback condition, (see Fig. 7-3). Transistor, Q756, continues to conduct some current when the supply is limited, dropping enough voltage across R754 to keep Q752 biased on.

Regulated +33 V is provided by Zener diode VR784 from the +100 V supply. Current divider, R741, R742, R2102 (see diagram 5) provides a sample of the line voltage for line triggering.

POWER-ON LAMP CIRCUIT

The POWER (ON) lamp, DS796, remains on as long as the line voltage does not vary more than approximately 10% from the nominal selected line voltage (100, 120, 220, or 240 V). When the line voltage is not within the 10% limit, the ON lamp blinks.

As long as Q796 is conducting, DS796 remains on. If Q796 is biased off, DS796 goes out, allowing C796 to charge through R796 and R797. When C796 reaches about 80 V, it discharges through DS796 causing it to turn on momentarily. Capacitor, C796, again is charged through R796-R797 and discharged through DS796. This cycle repeats, causing the ON lamp to blink until the line voltage is within the 10% limit and Q796 conducts.

When the 100 V unregulated supply at voltage divider R791-R792 and R793 increases to more than about 10% above the nominal value, Q792 turns on and Q796 turns off, causing DS796 to blink. When the 100 V unregulated supply at voltage divider R794-R799 and R795 decreases to less than about 10% below the nominal value, Q796 turns off, causing DS796 to blink.

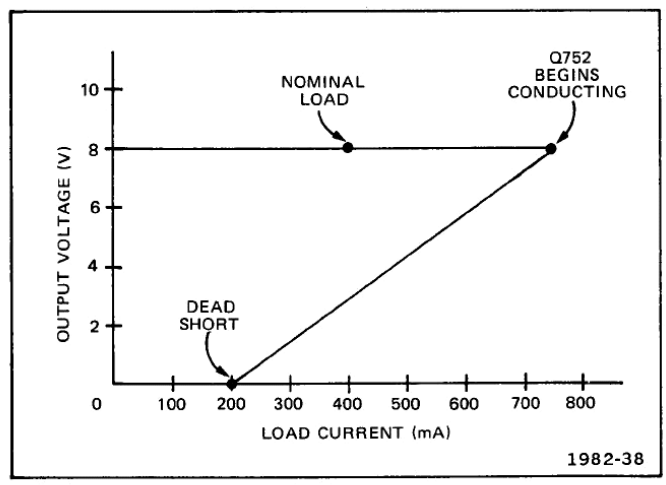
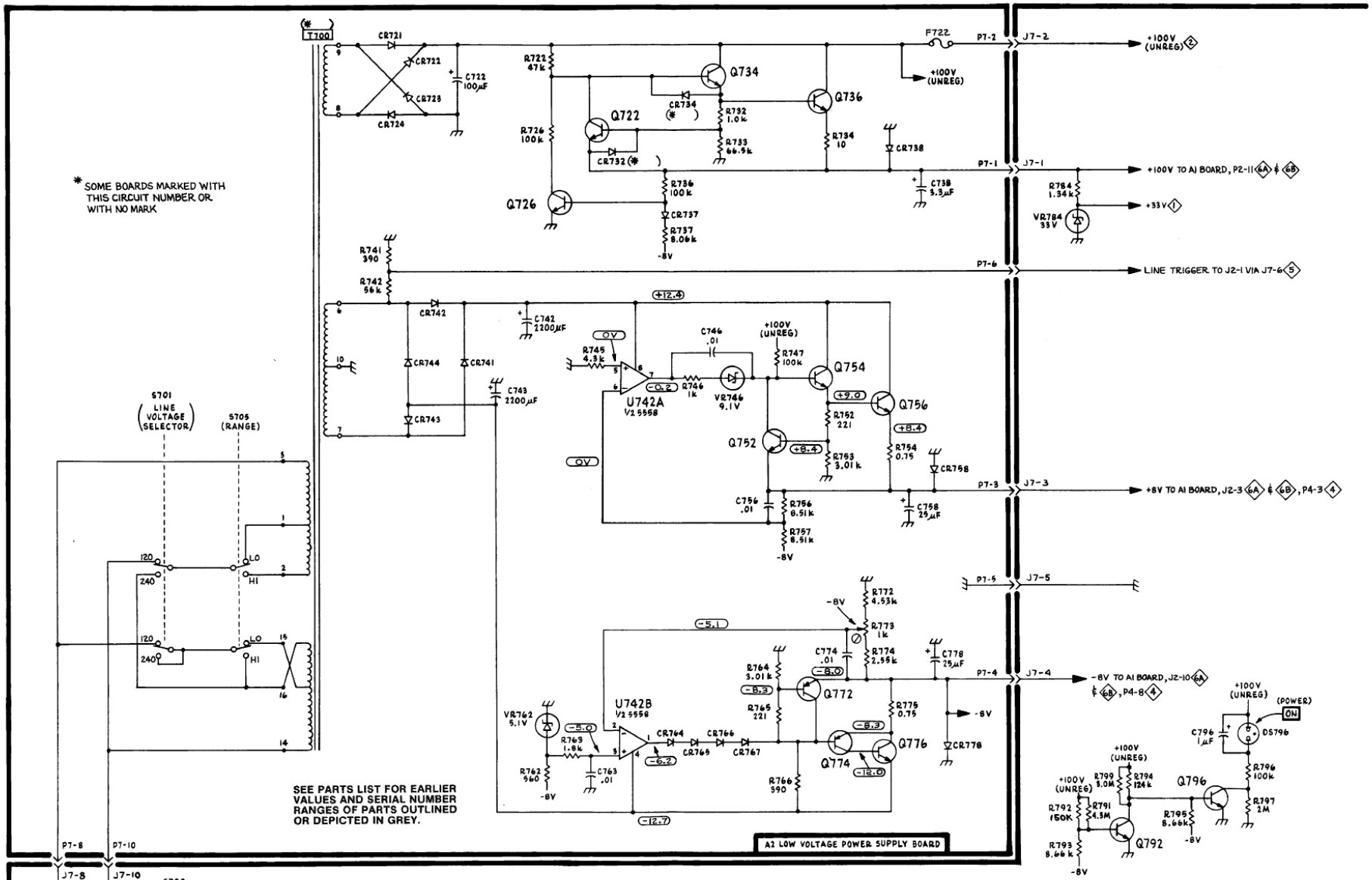


Fig. 7-3. Foldback circuit action.



VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a Tektronix DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or to the X (external trigger) input.

VERT INPUT CIRCUIT DESCRIPTION

Since Channel 1 and Channel 2 vertical input circuits are identical, only Channel 1 is discussed in detail. The 4100 series circuit numbers identify the Channel 1 components and 4200 series numbers identify the Channel 2 components.

INPUT COUPLING SWITCH

Vertical input signal is ac-coupled, dc-coupled, or grounded by S4100. In the DC position, the input signal is coupled directly to the VOLTS/DIV switch attenuator. In the AC position, the input signal passes through C4102 to the attenuator. In the GND position, the signal path from the input connector to the attenuator is grounded though C4102-R4102. This provides a ground reference without disconnecting the signal from the input connector. In the GND position, C4102 is charged to the average signal level through R4102 so that the trace remains on screen when S4100 is changed to the AC position.

VOLTS/DIV SWITCH

The VOLTS/DIV switch selects attenuator ratio and preamplifier gain to determine the deflection factor. The basic 1X deflection factor of the vertical deflection system is 2 mV/division. At this setting, no attenuators are switched in and the gain switching circuit sets the preamplifier gain to maximum. To provide the complete range of deflection factors indicated on the front panel, precision attenuators are switched in and out of the attenuator and gain switching circuit.

The attenuators are frequency compensated voltage dividers that provide constant attenuation at all frequencies within the bandwidth of the instrument. The input RC characteristics (approximately 1 MΩ times approximately 30 pF) are maintained for each setting of the VOLTS/DIV switch. The attenuator circuit consists of a 10X and a 100X attenuator. 1000X is obtained when the 10X and 100X attenuators are cascaded.

The gain switching circuit consists of R4143 through R4147 and three VOLTS/DIV switch contacts. Three preamplifier gains are selected: 1X (maximum), 2.5X reduction, and 5X reduction. Refer to Table 7-1 for the attenuator and gain switching sequence.

PREAMPLIFIER

The signal from the input attenuator is connected to source follower Q4122A via C4122 and R4122. Resistor R4121 determines the 1 MΩ input resistance, and R4122 limits current drive to the gate of Q4122A. Diode CR4122 protects the circuit from high negative-going input signals by limiting the voltage at the gate of Q4122A to about −8 volts. The Q4122A gate-drain junction provides protection from high positive-going signals by limiting the gate voltage to about +8 volts. FET Q4122B provides a constant-current source for Q4122A. For some serial numbers, Q4122 substrate (pin 8) is provided with a bias to compensate for possible substrate leakage. This bias is derived by the voltage divider action of R4128 and R4129 between +8 volts and ground.

Integrated circuits U4134B and U4134C are emitter followers. The signal at the emitter of U4134B follows the signal at the gate of Q4122A. Divider network R4143 through R4147 attenuates the signal from U4134B which drives the base of U4134D. DC BAL, R4130 adjusts for minimum trace shift when switching between adjacent positions of the VOLTS/DIV switch.

First Cascode Amplifier

Paraphase amplifier stage, U4134A, U4134D, and associated circuitry, converts the single-ended signal at the base of U4134D to a push-pull current signal. Capacitors C4158 and C4168 minimize the Miller effect through U4134D and U4134A. Components C4154, C4156, R4156, R4166 and C4166, connected between U4134A and U4134D emitters, compensate for high-frequency losses in the preamplifier. Gain adjustment R4151 determines the gain of the preamplifier. The VAR control, R4152, provides uncalibrated deflection factors between VOLTS/DIV switch settings by attenuating the signal to the base of U4134D. When R4152 is rotated clockwise, its full resistance is in series with R4162, and the deflection factors are calibrated.

Transistors Q4174 and Q4184 and associated circuitry make up a common base amplifier stage.

TABLE 7-1

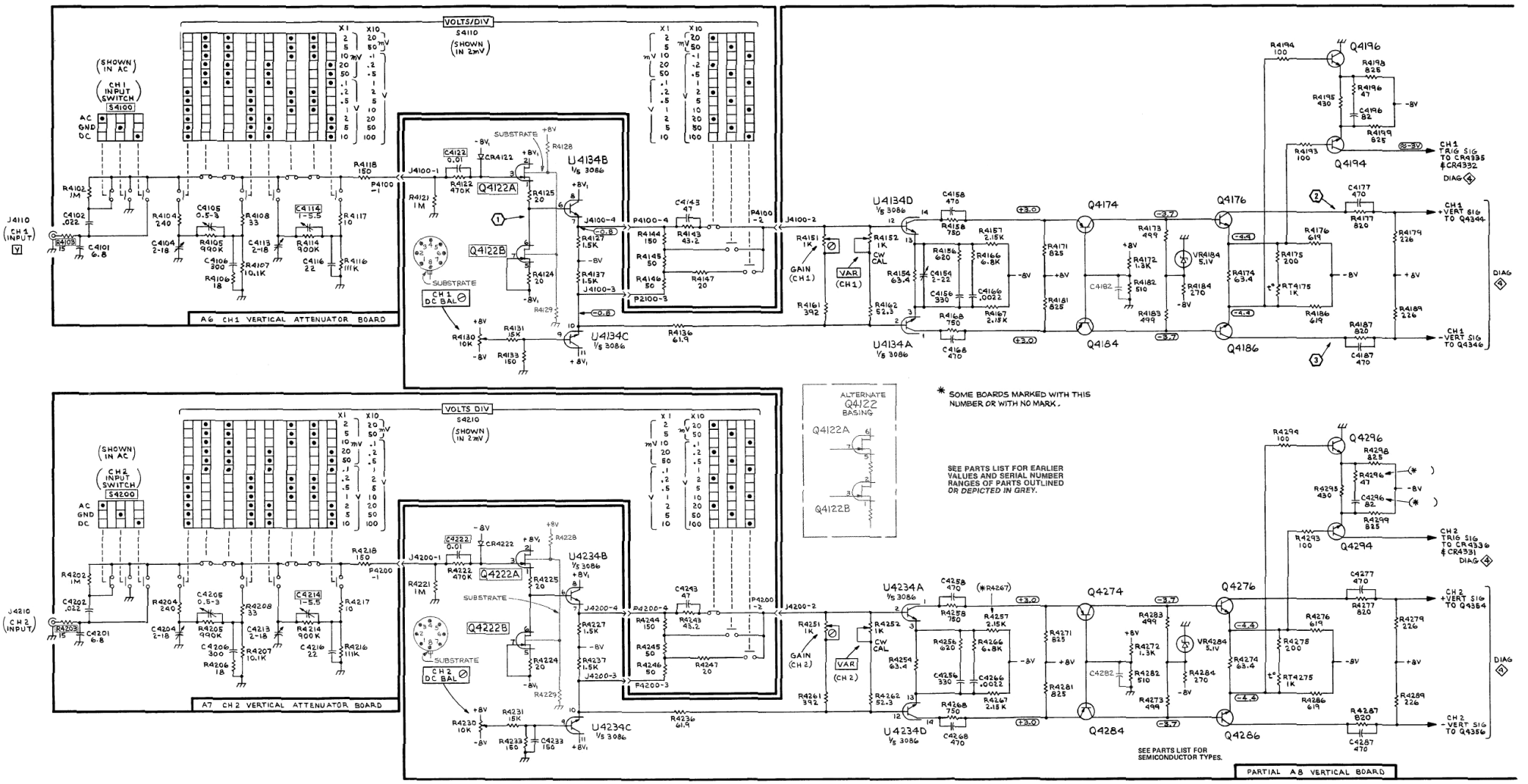
Attenuator and Gain Switching Sequence

VOLTS/DIV Setting	Attenuator (signal attenuation)	Gain Switch (preamp gain reduction)
2 mV	1X	1X
5 mV	1X	2.5X
10 mV	1X	5X
20 mV	10X	1X
50 mV	10X	2.5X
.1 V	10X	5X
.2 V	100X	1X
.5 V	100X	2.5X
1 V	100X	5X
2 V	1000X	1X
5 V	1000X	2.5X
10 V	1000X	5X

Second Cascode Amplifier

Transistors Q4176-Q4186 and Q4344-Q4346 (on diagram 4) comprise the second cascode amplifier. Capacitors C4177 and C4187 minimize the Miller effect through Q4176 and Q4186. The value of thermal resistor RT4175 (connected between emitters of Q4176 and Q4186) changes with temperature to counteract any gain change in the amplifier due to thermal variations. This holds the gain of the entire vertical amplifier constant over the operating temperature range of the instrument.

A sample of the vertical voltage signal from the emitters of Q4176 and Q4186 is applied to Q4194 and Q4196 where it is converted to a current signal. This current signal is applied to the trigger input amplifier (see diagram 5) via diode switching circuitry (see diagram 4). See circuit descriptions for diagrams 4 and 5 for further details.


VOLTS/DIV
S4110
(SHOWN IN 2mV)
(SHOWN IN AC)
CH 1 INPUT SWITCH
S4100
AC
GND
DC
A6 CH1 VERTICAL ATTENUATOR BOARD
CH 1 DC BAL
SUBSTRATE
U4134B
U4134C
U4134D
U4134A
Q4122A
Q4122B
GAIN (CH1)
VAR (CH1)
CW CAL
Q4174
Q4184
Q4176
Q4186
Q4196
Q4194
CH1 TRIG SIG TO CR4335 & CR4332
CH1 +VERT SIG TO Q4344
CH1 -VERT SIG TO Q4346
DIAG
VOLTS DIV
S4210
(SHOWN IN 2mV)
CH 2 INPUT SWITCH
S4200
A7 CH2 VERTICAL ATTENUATOR BOARD
CH 2 DC BAL
U4234B
U4234C
U4234D
U4234A
Q4222A
Q4222B
GAIN (CH 2)
VAR (CH 2)
Q4274
Q4284
Q4276
Q4286
Q4296
Q4294
CH2 TRIG SIG TO CR4336 & CR4331
CH2 +VERT SIG TO Q4354
CH2 -VERT SIG TO Q4356
ALTERNATE Q4122 BASING
SOME BOARDS MARKED WITH THIS NUMBER OR WITH NO MARK.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
PARTIAL A8 VERTICAL BOARD

VERT SWITCHING CIRCUIT DESCRIPTION

Since Channel 1 and Channel 2 vertical circuits are identical, only Channel 1 is discussed in detail.

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages that constitute a LO and HI logic state, may vary between individual devices.

POSITION CONTROL

POSITION control R4346 varies the dc voltage at the bases of Q4386 and Q4376 to vertically position the trace on the crt.

DELAY LINE DRIVER

The delay line driver is a push-pull feedback amplifier stage composed of Q4386, Q4376, and associated circuitry. A sample of the output of Q4386 and Q4376 is fed back through R4383 and R4373 to the bases of Q4386 and Q4376. Due to this feedback, this stage forms an inverting operational amplifier with a virtual ground at the bases of Q4386 and Q4376. Any current into these virtual ground null points causes an output voltage that is proportional to the feedback resistance.

Components C4396, R4396, C4397, C4395, R4397, C4398, R4398 provide compensation (peaking) to correct for delay line losses.

DELAY LINE

The delay line, DL4380 provides approximately 120 ns delay in the vertical signal. This allows the sweep *generator circuit time to initiate a sweep before the vertical* signal reaches the crt vertical deflection plates.

VERTICAL SWITCHING

The vertical switching circuit determines whether CH 1 or CH 2 is connected to the vertical output amplifier in the DUAL TRACE alternate or chopped modes. Both channels are alternately displayed on a time shared basis.

The diode gates, consisting of four diodes each, act as switches that allow either of the vertical preamplifier signals to be coupled to the delay line driver. Diodes CR4346, CR4347, CR4348, and CR4349 control the CH 1 output; CR4356, CR4357, CR4358, and CR4359 control the CH 2 output. These diodes are controlled by flip-flop U4324A, which in turn is controlled by Vertical Mode switch, S4320.

When the Vertical Mode switch is in the CH 1 position, pin 4 of U4324A is held LO, causing pin 5 to go HI. A HI at pin 5 (a voltage higher than at the bases of Q4386 and Q4376) reverse biases CR4347 and CR4348 and forward biases CR4346 and CR4349. This allows the CH 1 signal to pass to the delay line driver. When pin 5 is HI, pin 6 is LO, causing the cathodes of CR4357 and CR4358 to be connected to a voltage much lower than on the bases of Q4386 and Q4376. Diodes CR4357 and CR4358 are now forward biased and diodes CR4356 and CR4359 are reverse biased, preventing the CH 2 signal from passing to the delay line driver.

In the CH 2 mode, the above conditions are reversed. Diodes CR4357 and CR4358 are reverse biased, passing the CH 2 signal and blocking the CH 1 signal.

In the DUAL TRACE Vertical Mode, CH 1 and CH 2 are alternately connected to the delay line driver. There are two dual trace modes: chopped and alternate. These modes are determined by the SEC/DIV switch setting. Chopped mode is obtained for sweep speeds of 1 ms and slower; alternate is obtained for sweep speeds of 0.5 ms and faster.

In the chopped mode pin 2 of U4306A is ungrounded, allowing the multivibrator, U4306A and U4306D, to free run at about 250 kHz. The output at pin 8 of U4306C serves as a clock pulse for U4324A, which in turn switches the diode gates at the 250 kHz rate. The clock pulse is also fed to U4324B, which provides an output pulse to the Z Axis amplifier to blank out the transition between CH 1 and CH 2 traces. If pin 13 of U4324B goes LO, the output pin 9 is set LO, causing pin 6 of U4306B to go HI. This causes pin 13 of U4324A to go HI after being delayed by C4315 charging through R4315.

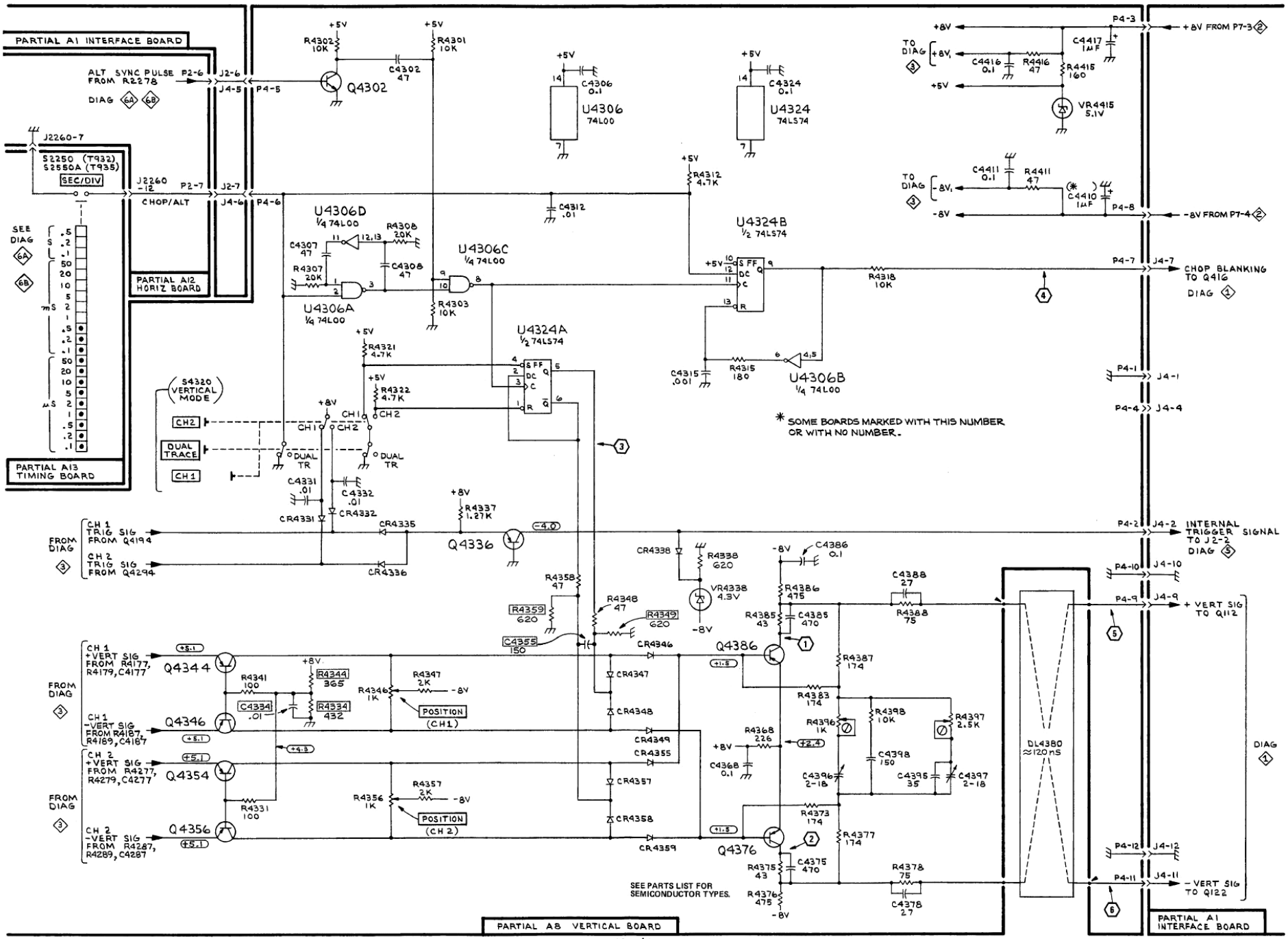
The clock pulse applied to pin 11 of U4324B causes pin 9 to go HI, which in turn, after passing through the inverter and after some delay, sets pin 13 LO again. This causes pin 9 to go LO again. The positive-going voltage pulse (whose width is determined by R4315 and C4315) is converted to current by R4318 and sent to the Z Axis Amplifier to blank switching transients.

In the alternate mode, pin 2 of U4306A is grounded (via SEC/DIV), preventing multivibrator operation, thus keeping pin 10 of U4306C HI. At the end of each sweep, the base of Q4302 receives a current pulse driving it into saturation. The resulting negative-going pulse at the collector is fed through C4302 to pin 9 of U4306C causing pin 8 to go HI. This in turn, switches U4324A to pass either CH 1 or CH 2 to the delay line driver at the end of each sweep. Pin 12 of U4324B is grounded through the SEC/DIV switch and prevents an output at pin 9.

The Vertical Mode switch also selects the appropriate internal triggering source for CH 1 and CH 2. With the Vertical Mode switch set to CH 1 and DUAL TRACE, CR4335 is forward biased and the signal from the CH 1 trigger pickoff goes to the sweep circuit. In these modes, CR4331 is connected to the +8 volts, thus reverse biasing CR4336, preventing the CH 2 trigger signal from entering the trigger input amplifier. With the Vertical Mode switch set to CH 2, CR4336 becomes forward biased while CR4335 is reverse biased because CR4332 is now connected to +8 volts.

TRIGGER PICKOFF

Transistors Q4196 and Q4194 (diagram 3) convert a sample of the vertical signal to a single-ended current signal to drive the trigger input amplifier. When the TRIGGERING SOURCE switch is set to INT, approximately −4 volts from the trigger input amplifier is applied to the collector of Q4336, reverse biasing CR4338 (diagram 4), and allowing the internal trigger signal (selected by diode switching circuit) to be applied to the trigger input amplifier. When the SOURCE switch is set to LINE, EXT, EXT÷10, or X-Y, the internal trigger signal is disconnected from the trigger input amplifier, forward biasing CR4338, and setting the collector of Q4336 at about −3 volts. The resultant Q4336 load maintains conduction of Q4196 and Q4194, thus presenting a constant load for Q4176 and Q4186 (see diagram 3) to prevent distortion of the main vertical signal.



T932/T935

1983-47
REV. A, JULY 1977

VERTICAL SWITCHING 4

VI.1

TRIGGER CIRCUIT DESCRIPTION

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit decription to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages that constitute a LO and HI logic state may vary between individual devices.

INPUT AND SWITCHING

SOURCE Switch

The SOURCE switch, S2100, selects trigger signals from INT, LINE, EXT, EXT ÷ 10, and X-Y sources.

INT. Signal from the trigger pickoff circuit in the vertical amplifier is connected to the trigger input amplifier Q2122. (See diagrams 3 and 4.)

LINE. A sample of the line voltage, obtained from the power transformer, is connected to the trigger input amplifier Q2122.

EXT. Externally applied signals pass through buffer amplifier Q2104-Q2106. FET Q2104 is a source follower and Q2106 is a current source. Transistor Q2108 and R2107 convert the voltage signal at the buffer output to a current for application to the trigger input amplifier. When EXT is selected, the collector of Q2108 is connected to the trigger input amplifier (Q2122) by SOURCE switch S2100.

EXT
÷10. The output of buffer amplifier Q2104-Q2106 is connected to R2111. Resistor R2111 converts the buffer output voltage to a current which is connected to the trigger input amplifier via S2100.

X-Y. Signals from the X (EXT) input are routed to the horizontal amplifier via CR2183. The SOURCE switch connects +8 volts to R2182, forward biasing CR2183 and providing current to the horizontal amplifier to center the crt display. Further, +8 volts is applied to CR2182 and R2185 to electrically place the sweep in the NORM mode and to disable the trigger circuit.

MODE Switch

The MODE switch (S2150) selects three triggering modes: AUTO, NORM, and TV.

AUTO. Allows the sweep to free run in the absence of a triggering signal. See sweep circuit description for details.

NORM. Connects +8 volts to R2223 in the sweep generator circuit. Allows the sweep to run only when a suitable triggering signal is present.

TV. The trigger signal is applied to the TV sync separator circuit (Q2164, Q2174, Q2176) and the normal trigger generator circuit is disabled. In this mode, the SLOPE switch is used to supply the sync separator with a signal of the proper polarity. For SEC/DIV settings of .1 ms/div or slower, the sweep is triggered by vertical sync pulses which occur at a field rate. For SEC/DIV settings of 50 μs and faster, the sweep is triggered by the TV horizontal line signals.

TRIGGER INPUT AMPLIFIER

The trigger input amplifier consists of Q2122, Q2124, Q2128, and associated circuitry. Resistors R2127 and R2128 set the amplifier input at −4 volts. The inverting configuration and feedback from the emitter of Q2128 form an inverting operational amplifier with a null point at the base of Q2122. Any current into the null point produces a voltage at the output proportional to the feedback resistor R2116. Diode CR2124 prevents the emitter of Q2128 from going below ground and reversing the voltage across C2132.

TRIGGER LEVEL COMPARATOR

Differential amplifier Q2134-Q2136 functions as a comparator. The LEVEL control R2138 selects the point on the waveform that starts a sweep. Capacitor C2132 ac couples the trigger signal to the comparator. As the trigger signal at the base of Q2134 passes through the same voltage level as the base of Q2136 (set by LEVEL control), the signal at the emitter of Q2152 passes through the threshold (about 1 volt) of Schmitt trigger U2156A-U2156B producing a logic trigger signal. The trigger signals at the collectors of Q2134 and Q2136 are of opposite polarity. This allows the SLOPE switch S2140 to invert the signals applied to the TV trigger input amplifier Q2164 and the normal trigger input amplifier Q2142, Q2144, and Q2152. When the SLOPE switch is in the +OUT position, the output at the collector of Q2142 is in phase with the trigger source signal. Transistors Q2142, Q2144 and Q2152 convert the current signal from the collectors of Q2134 or Q2136 to a voltage signal for triggering the Schmitt trigger.

TV TRIGGER CIRCUIT

Active devices Q2164, Q2174, Q2176, U2156B, C, D, and associated circuitry comprise the TV trigger circuit. When the MODE switch is in TV, R2186 is disconnected from +8 volts which allows trigger signals from the collectors of Q2134 and Q2136 to pass through the TV trigger circuit. (In AUTO and NORM, the +8 volts applied to R2186 biases Q2164 to saturation.)

Transistor Q2164 is a high gain feedback amplifier. To achieve stable triggering on TV signals, the LEVEL control must be set at a point that will allow the sync pulses to appear within the dynamic range of the amplifier.

The sync separator circuit consists of Q2174 and associated circuitry. It processes sync-positive pulses when the SLOPE switch is in the +OUT position and sync-negative pulses in the −IN position. Transistor Q2174 produces large positive-going pulses from negative-going sync signals at the collector of Q2164.

In the TV field mode (SEC/DIV switch set for .1 ms or slower), Q2176 is saturated (since base is grounded), and the integrator (composed of C2174, C2176, R2174, and R2176) is switched into the circuit (effectively connected to +8 volts through saturated Q2176). The integrator filters out the horizontal sync pulses, leaving only the integrated vertical sync pulses, which trigger the TV Schmitt trigger U2156B and U2156C.

In the TV line mode (SEC/DIV switch set for 50 μs or faster), Q2176 is turned off (base open), disconnecting C2174 and C2176 from +8 volts. Capacitors C2174 and C2176 no longer integrate the pulses, thus allowing both the horizontal and vertical sync pulses to pass through to the TV Schmitt trigger.

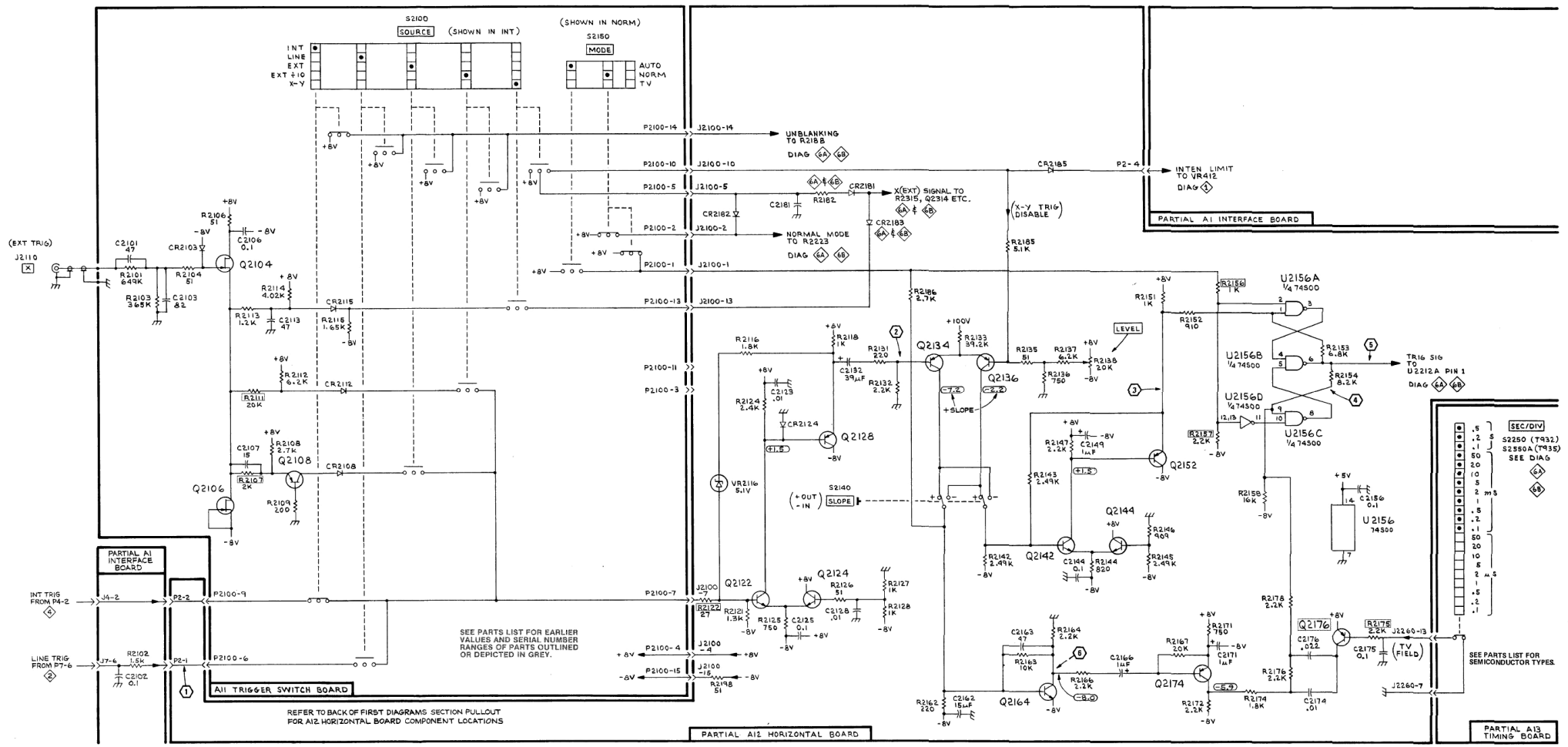
SCHMITT TRIGGERS

The Schmitt trigger for the NORM and AUTO triggering modes consists of U2156A, U2156B, and associated circuitry. Hysteresis of this trigger circuit is determined by R2152, R2153, and R2151.

The Schmitt trigger for the TV triggering mode is U2156B, U2156C, U2156D, and associated circuitry. Resistors R2154 and R2178 determine the sensitivity.

When the MODE switch S2150 is in AUTO or NORM, +8 volts is applied to R2156 which causes pin 1 of U2156A to go HI enabling Schmitt trigger U2156A-U2156B. At the same time, pins 12 and 13 of U2156D are also HI disabling Schmitt trigger U2156C-U2156B. A trigger signal from Q2152 triggers Schmitt trigger U2156A-U2156B to produce a logic trigger signal at pin 6 of U2156B.

When the MODE switch S2150 is in TV, +8 volts is removed from R2156 and pin 1 of U2156A is LO, disabling Schmitt trigger U2156A-U2156B. Pins 12 and 13 of U2156D are LO, enabling Schmitt trigger U2156B-U2156C. The trigger signal from the TV sync separator triggers Schmitt trigger U2156B-U2156C to produce a logic trigger signal at pin 6 of U2156B.


S2100
SOURCE
(SHOWN IN INT)
(SHOWN IN NORM)
S2150
MODE
INT
LINE
EXT
EXT ÷10
X-Y
AUTO
NORM
TV
UNBLANKING TO R218B
DIAG 6A 6B
X(EXT) SIGNAL TO R2315, Q2314 ETC.
NORMAL MODE TO R2223
INTEN. LIMIT TO VR412
DIAG 4
(X-Y TRIG) DISABLE
PARTIAL A1 INTERFACE BOARD
(EXT TRIG)
J2110
Q2104
Q2106
Q2108
Q2122
Q2124
Q2128
Q2134
Q2136
Q2142
Q2144
Q2152
Q2164
Q2174
Q2176
U2156A 1/4 74S00
U2156B 1/4 74S00
U2156C 1/4 74S00
U2156D 1/4 74S00
U2156 74S00
TR16 S16 TO U2212A PIN 1
DIAG 6A 6B
+SLOPE
LEVEL
SEC/DIV
S2250 (T932)
S2350A (T935)
SEE DIAG 6A 6B
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
INT TRIG FROM P4-2 4
LINE TRIG FROM P7-6 2
A11 TRIGGER SWITCH BOARD
PARTIAL A1 INTERFACE BOARD
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
REFER TO BACK OF FIRST DIAGRAMS SECTION PULLOUT FOR A12 HORIZONTAL BOARD COMPONENT LOCATIONS
PARTIAL A12 HORIZONTAL BOARD
PARTIAL A13 TIMING BOARD
(TV FIELD)

T932 SWEEP AND HORIZ AMPL CIRCUIT DESCRIPTION

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages which constitute a LO and HI logic state may vary between individual devices.

SWEEP

The sweep is produced by a Miller Integrator circuit consisting of Q2242, Q2244, and Q2246. A sweep ramp is initiated at the collector of Q2246 when pin 3 of U2234A goes LO, and is terminated when pin 3 goes HI (see Timing diagram, Fig. 7-4).

In the NORM triggering mode, pin 2 of U2212A is HI allowing a positive-going trigger signal at pin 1 of U2212A to cause pin 3 of U2234A to go LO (via U2212D and U2234C). This reverse biases CR2233 and CR2234, and allows the timing capacitor (selected by the SEC/DIV switch, S2250) to charge, producing a sweep ramp at the collector of Q2246. When the sweep ramp reaches about 12 volts, Q2274 turns on. This causes pin 7 of U2224A to go LO, pin 8 of U2234C to go LO, and pin 3 of U2234A to go HI. When pin 3 of U2234A goes HI, CR2233 and CR2234 are forward biased, terminating the sweep. Pin 7 of U2224A remains LO for a length of time (hold-off time) determined by C2275, C2274, R2271, R2274, and the HOLD-OFF control, R2272. Three hold-off times are selected by the SEC/DIV switch S2250 and varied by R2272. After the selected hold-off time, U2224A pin 7 goes HI. This allows the next trigger signal to switch pin 3 of U2234A LO and again start the sweep.

In the AUTO triggering mode, when no trigger signal occurs at pin 11 of U2224B for about 50 ms, pin 10 of U2224B goes LO, causing the sweep to start after the hold-off time ends. This allows the sweep to free run and provide a reference display. When a trigger signal is present, pin 11 of U2224B goes HI, then LO (when trigger signal ends), and the time constant of C2226 and R2226 prevents pin 10 from going LO as long as the repetition rate of the trigger signal is higher than about 20 Hz.

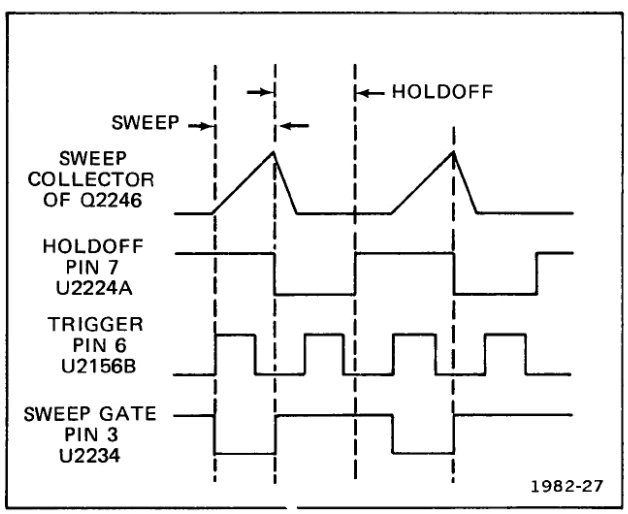


Fig. 7-4. Timing Diagram: sweep generator and sweep gate.

When pin 3 of U2234A goes HI, the current set by R2236, R2235, and R2237 is sent to the Z Axis Amplifier Q416 (see diagram 1) to blank the crt during hold-off.

HORIZONTAL AMPLIFIER

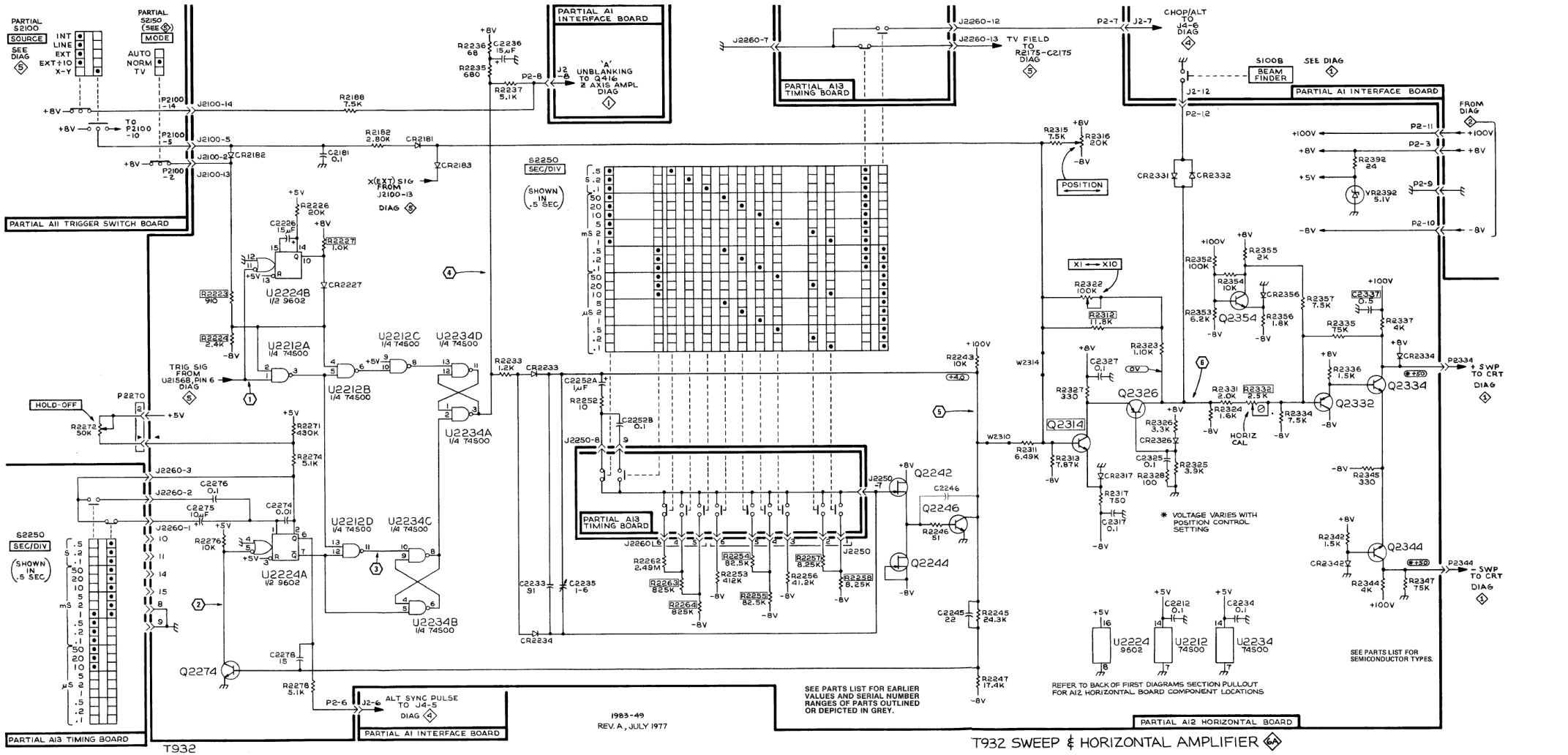
The horizontal amplifier converts the single-ended signal to a push-pull signal, which drives the crt horizontal deflection plates. The input of the horizontal amplifier comes from either the sweep generator or the X (external trigger) input connector. In the X-Y mode, the trace is shifted to the center of the screen by the current through R2182. In the AUTO and NORM modes, the input to the horizontal amplifier is a linear ramp from the sweep generator.

Transistors, Q2314, Q2326, and associated circuitry, form an operational amplifier with a variable gain range of over 10 to 1. The gain is set by feedback elements R2312, R2323, and X1-X10 control, R2322. The horizontal POSITION control, R2316, positions the crt display horizontally by varying the current into the base of Q2314. The cascode configuration of Q2314 and Q2326 improves the high frequency response.

When the BEAM FINDER switch, section S100B, is pressed, the dynamic range of Q2326 is decreased. This limits the horizontal deflection to the crt screen area. The BEAM FINDER switch (section S100A) also limits the vertical deflection to the crt screen area.

Transistors Q2332, Q2334. Q2344, and associated circuitry form a paraphase amplifier. Transistor Q2332 is a low-impedance input for Q2334. Horiz Cal adjustment R2332, sets the gain of the paraphase amplifier. When the current through the collector of Q2334 increases, the current through the collector of Q2344 decreases and is 180° out of phase with the current at the collector of Q2334. The resulting signal to the crt deflection plates is a push-pull signal. Diode CR2334 prevents Q2334 from saturating when R2322 is in the X10 position.

Since Q2334 is a shunt feedback amplifier and Q2344 is a common base amplifier, any noise in the 100 V power supply will appear as a part of the output. To prevent the noise from appearing on the crt screen, an operational amplifier, consisting of Q2354 and associated circuitry, supplies an inverted sample of the power supply noise to the output. Now, any noise in the 100 volt power supply appears common mode to the horizontal deflection plates, preventing horizontal deflection of the noise signal. Resistor R2354 provides feedback for the operational amplifier.


PARTIAL S2100 SOURCE
SEE DIAG 5
INT LINE EXT EXT÷10 X-Y
PARTIAL S2150 (SEE 5) MODE
AUTO NORM TV
PARTIAL A1 INTERFACE BOARD
'A' UNBLANKING TO Q416 2 AXIS AMPL DIAG 1
PARTIAL A13 TIMING BOARD
J2260-12
J2260-13 TV FIELD TO R2175-C2175 DIAG 5
J2260-7
P2-7
J2-7
CHOP/ALT TO J4-6 DIAG 4
S100B BEAM FINDER
SEE DIAG 4
J2-12
P2-12
FROM DIAG 2
P2-11 +100V
P2-3 +8V
P2-9 +5V
P2-10 -8V
R2392 24
VR2392 5.1V
R2315 7.5K
R2316 20K
POSITION
CR2331 CR2332
X1 ⟷ X10
R2322 100K
R2312 11.8K
R2352 100K
R2355 2K
R2354 10K
R2353 6.2K
Q2354
R2356 1.8K
R2357 7.5K
C2337 0.5
R2335 75K
R2337 4K
R2323 1.10K
C2327 0.1
R2327 330
Q2326
R2326 3.3K
CR2326
R2331 2.0K
R2332 2.5K
R2324 1.6K
HORIZ CAL
R2334 7.5K
Q2332
R2336 1.5K
Q2334
CR2334
P2334 + SWP TO CRT DIAG 4
Q2314
R2311 6.49K
R2313 7.87K
CR2317
R2317 750
C2317 0.1
C2325 0.1
R2328 100
R2325 3.9K
R2345 330
R2342 1.5K
Q2344
CR2342
R2344 4K
R2347 75K
P2344 + SWP TO CRT DIAG 4
* VOLTAGE VARIES WITH POSITION CONTROL SETTING
U2224 9602
U2212 74S00
U2234 74S00
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
REFER TO BACK OF FIRST DIAGRAMS SECTION PULLOUT FOR A12 HORIZONTAL BOARD COMPONENT LOCATIONS
PARTIAL A12 HORIZONTAL BOARD
PARTIAL A11 TRIGGER SWITCH BOARD
R2236 68
C2236 15µF
R2235 680
R2237 5.1K
P2-8
J2-8
R2188 7.5K
R2182 2.80K
CR2181
C2181 0.1
CR2183
CR2182
X(EXT) SIG FROM J2100-13 DIAG 6
J2100-14
J2100-5
J2100-2
J2100-13
P2100-14
P2100-10 TO P2100-10
P2100-5
P2100-2
S2250 SEC/DIV
(SHOWN IN .5 SEC)
R2226 20K
C2226 15µF
R2227 1.0K
CR2227
U2224B 1/2 9602
R2223 910
R2224 2.4K
U2212A 1/4 74S00
U2212C 1/4 74S00
U2234D 1/4 74S00
U2212B 1/4 74S00
U2234A 1/4 74S00
TRIG SIG FROM U2156B, PIN 6 DIAG 5
HOLD-OFF
P2270
R2272 50K
R2271 430K
R2274 5.1K
R2233 1.2K
CR2233
C2252A 1µF
R2252 10
C2252B 0.1
J2250-8
J2250-7
Q2242
C2246
Q2246
R2246 51
Q2244
J2250
J2260-3
J2260-2
J2260-1
C2276 0.1
C2275 10µF
C2274 0.01
R2276 10K
U2224A 1/2 9602
U2212D 1/4 74S00
U2234C 1/4 74S00
U2234B 1/4 74S00
R2262 2.49M
R2263 825K
R2254 82.5K
R2253 412K
R2255 82.5K
R2256 41.2K
R2257 8.25K
R2258 8.25K
R2264 825K
C2233 91
C2235 1-6
CR2234
C2245 22
R2245 24.3K
R2247 17.4K
Q2274
C2278 15
R2278 5.1K
P2-6
J2-6
ALT SYNC PULSE TO J4-5 DIAG 4
PARTIAL A1 INTERFACE BOARD
PARTIAL A13 TIMING BOARD
S2250 SEC/DIV
(SHOWN IN .5 SEC)
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
1983-49
REV. A, JULY 1977
T932
T932 SWEEP & HORIZONTAL AMPLIFIER 6A

VIII.1

T935 A SWEEP AND HORIZ AMPL CIRCUIT DESCRIPTION

A SWEEP GENERATOR

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages which constitute a LO and HI logic state may vary between individual devices.

The A sweep is produced by a Miller Integrator circuit consisting of Q2242, Q2244, and Q2246. A sweep ramp is initiated at the collector of Q2246 when pin 3 of U2234A goes LO, and is terminated when pin 3 goes HI (see Timing diagram, Fig. 7-5).

In the NORM triggering mode, pin 2 of U2212A is HI allowing a positive-going trigger signal at pin 1 of U2212A to cause pin 3 of U2234A to go LO (via U2212D and U2234C). This reverse biases CR2233 and CR2234, and allows the timing capacitor (selected by the A SEC/DIV switch, S2250A) to charge, producing a sweep ramp at the collector of Q2246. When the sweep ramp reaches about 12 volts, Q2274 turns on. This causes pin 7 of U2224A to go LO, pin 8 of U2234C to go LO, and pin 3 of U2234A to go HI. When pin 3 of U2234A goes HI, CR2233 and CR2234 are forward biased, terminating the sweep. Pin 7 of U2224A remains LO for a length of time (hold-off time) determined by C2275, C2274, R2271, R2274, and the HOLD-OFF control, R2272. Three hold-off times are selected by the SEC/DIV switch S2250A and varied by R2272. After the selected hold-off time, U2224A pin 7 goes HI. This allows the next trigger signal to switch pin 3 of U2234A LO and again start the sweep.

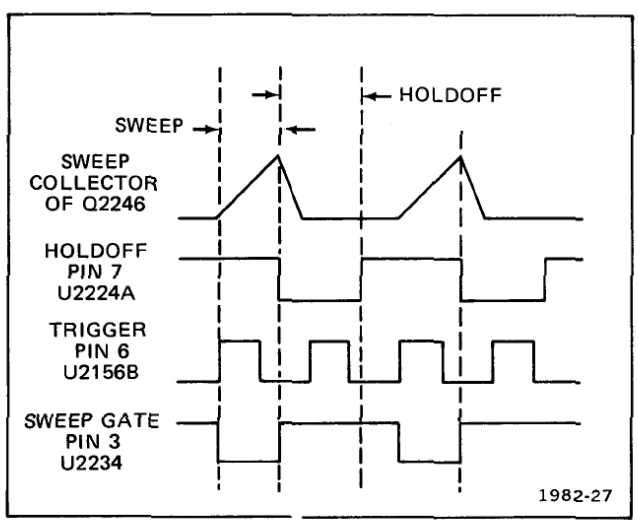


Fig. 7-5. Timing Diagram: sweep generator and sweep gate.

In the AUTO triggering mode, when no trigger signal occurs at pin 11 of U2224B for about 50 ms, pin 10 of U2224B goes LO, causing the sweep to start after the hold-off time ends. This allows the sweep to free run and provide a reference display. When a trigger signal is present, pin 11 of U2224B goes HI, then LO (when trigger signal ends), and the time constant of C2226 and R2226 prevents pin 10 from going LO as long as the repetition rate of the trigger signal is higher than about 20 Hz.

When the DISPLAY MODE switch S2510 (see diagram 7) is in the A or B modes, a signal is applied to Q416 in the Z Axis amplifier (see diagram 1) to blank the crt during hold-off time and unblank the crt during sweep time. In the A mode, when pin 3 of U2234A goes HI, R2236, R2235, and R2237 convert the voltage to a current for blanking and unblanking. Refer to T935 B Sweep circuit description for blanking and unblanking operation when S2510 is in B or A INTEN BY B modes.

HORIZONTAL AMPLIFIER

The horizontal amplifier converts the single-ended signal to a push-pull signal, which drives the crt horizontal deflection plates. The input of the horizontal amplifier comes from either the sweep generator or the X (external trigger) input connector. In the X-Y mode, the trace is shifted to the center of the screen by the current through R2182. In the AUTO and NORM modes, the input to the horizontal amplifier is a linear ramp from the sweep generator.

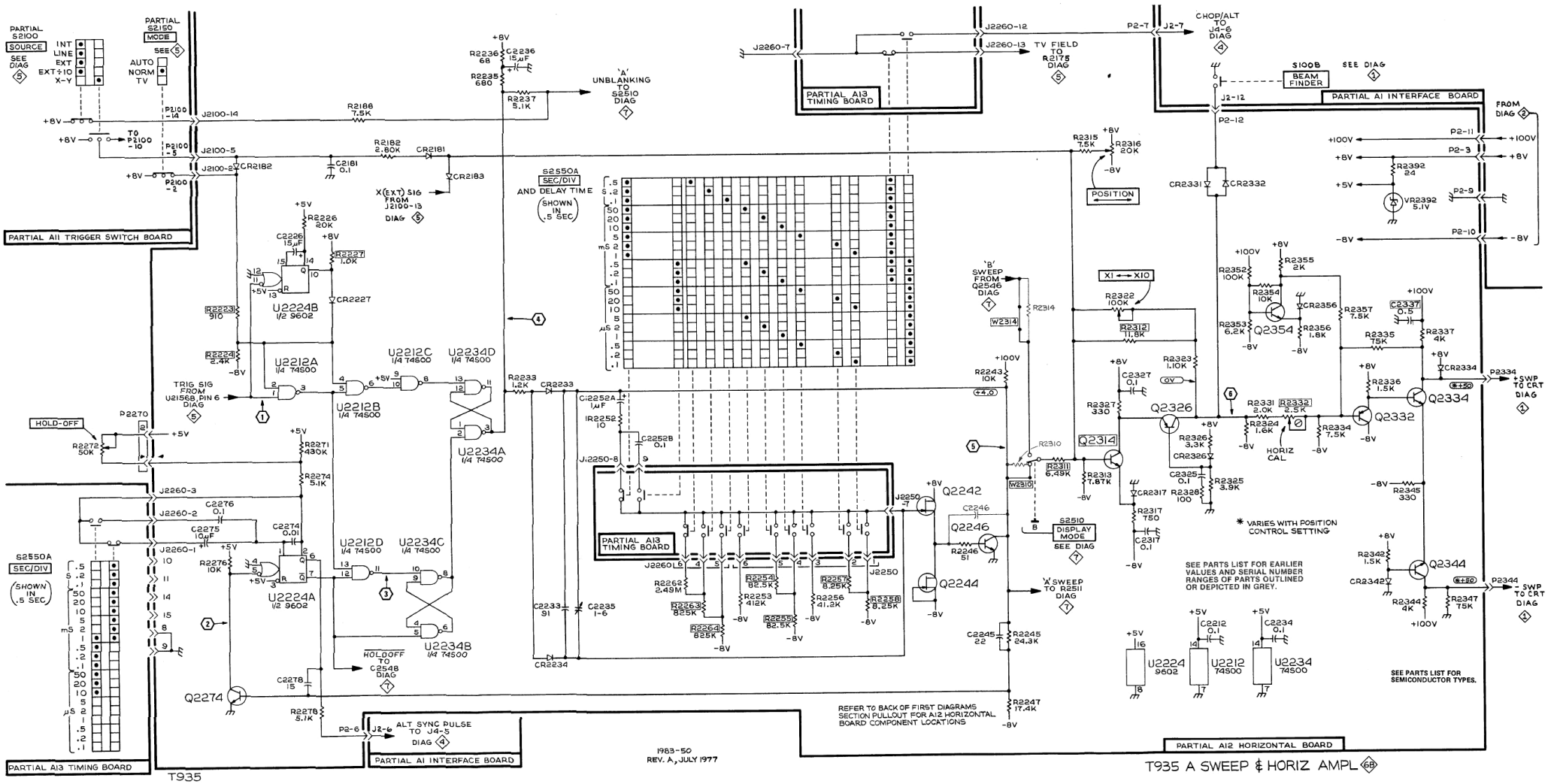
Transistors, Q2314, Q2326, and associated circuitry, form an operational amplifier with a variable gain range of over 10 to 1. The gain is set by feedback elements R2312, R2323, and X1-X10 control, R2322. The horizontal POSITION control, R2316, positions the crt display horizontally by varying the current into the base of Q2314. The cascode configuration of Q2314 and Q2326 improves the high frequency response.

When the BEAM FINDER switch, section S100B, is pressed, the dynamic range of Q2326 is decreased. This limits the horizontal deflection to the crt screen area. The BEAM FINDER switch (section S100A) also limits the vertical deflection to the crt screen area.

Transistors Q2332, Q2334. Q2344, and associated circuitry form a paraphase amplifier. Transistor Q2332 is a low-impedance input for Q2334. Horiz Cal adjustment R2332, sets the gain of the paraphase amplifier. When the current through the collector of Q2334 increases, the current through the collector of Q2344 decreases and is

180° out of phase with the current at the collector of Q2334. The resulting signal to the crt deflection plates is a push-pull signal. Diode CR2334 prevents Q2334 from saturating when R2322 is in the X10 position.

Since Q2334 is a shunt feedback amplifier and Q2344 is a common base amplifier, any noise in the 100 V power supply will appear as a part of the output. To prevent the noise from appearing on the crt screen, an operational amplifier, consisting of Q2354 and associated circuitry, supplies an inverted sample of the power supply noise to the output. Now, any noise in the 100 volt power supply appears common mode to the horizontal deflection plates, preventing horizontal deflection of the noise signal. Resistor R2354 provides feedback for the operational amplifier.


PARTIAL A13 TIMING BOARD
PARTIAL A11 TRIGGER SWITCH BOARD
PARTIAL A1 INTERFACE BOARD
PARTIAL A12 HORIZONTAL BOARD
T935
T935 A SWEEP & HORIZ AMPL
1983-50
REV. A, JULY 1977
REFER TO BACK OF FIRST DIAGRAMS SECTION PULLOUT FOR A12 HORIZONTAL BOARD COMPONENT LOCATIONS
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
* VARIES WITH POSITION CONTROL SETTING
U2224B 1/2 9602
U2212A 1/4 74S00
U2212B 1/4 74S00
U2212C 1/4 74S00
U2212D 1/4 74S00
U2234A 1/4 74S00
U2234B 1/4 74S00
U2234C 1/4 74S00
U2234D 1/4 74S00
U2224A 1/2 9602
Q2354
Q2326
Q2332
Q2334
Q2314
Q2242
Q2246
Q2244
Q2274
Q2344
U2224 9602
U2212 74S00
U2234 74S00

T935 B SWEEP CIRCUIT DESCRIPTION

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages which constitute a LO and HI logic state may vary between individual devices.

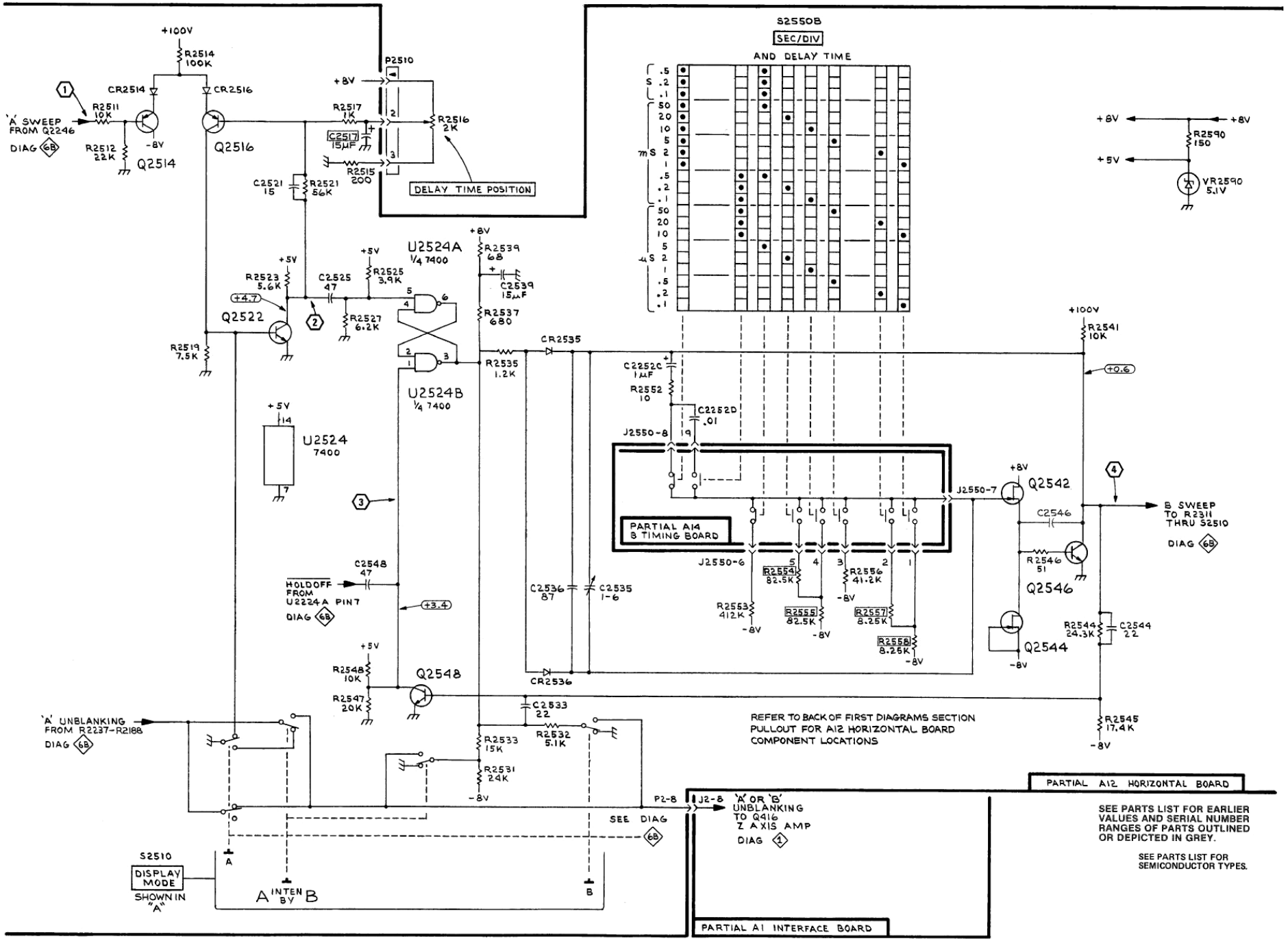
The DISPLAY MODE switch S2510 selects A, B, or A INTEN BY B. In the A position, the B sweep is disconnected from the Horizontal Output Amplifier. In the B position, the A sweep is disconnected from the Horizontal Output Amplifier and the B sweep starts after the delay. In the A INTEN BY B position, the A sweep is connected to the Horizontal Output Amplifier. In this mode, the A sweep starts and then after the delay, the B sweep runs and intensifies a portion of the A sweep.

With the B mode selected, when pin 3 of U2524B goes HI, R2539, R2537, and R2532 convert the voltage at pin 3 to a current signal. This signal is applied to Q416 in the Z-Axis amplifier (see diagram 1) to blank the crt during hold-off and unblank the crt during B sweep time. With S2510 in the A INTEN BY B mode, R2539, R2537, R2533 and R2531 provide the B sweep current source for Q416. This current signal is combined with the A sweep blanking and unblanking current signal from R2237 (see diagram 6B), allowing the A sweep to be intensified by the B sweep.

A Miller Integrator circuit consisting of Q2542, Q2544, Q2546, and associated circuitry, produces B sweep. The sweep ramp is initiated at the collector of Q2546 when pin 3 of U2524B goes LO, and is terminated when pin 3 of U2524B goes HI.

When pin 3 of U2524B goes LO, CR2535 and CR2536 are reverse biased. This allows the timing capacitor (selected by the B SEC/DIV switch S2550B) to charge, producing a sweep ramp at the collector of Q2546. When the sweep ramp reaches about 12 V, Q2548 turns on, causing pin 3 of U2524B to go HI. The HI at pin 3 of U2524B forward biases CR2535 and CR2536, ending the B sweep. If the A sweep ends before Q2548 turns on (before the B sweep ends), the Hold-off signal from pin 7 of U2224A causes pin 1 of U2524B to go LO. This in turn, causes pin 3 of U2524B to go HI, ending the B sweep. Pin 3 of U2524B will remain HI until pin 5 of U2524A goes LO again.

Transistors Q2514 and Q2516 make up a voltage comparator. The DELAY TIME POSITION control, R2516, sets the voltage at the base of Q2516. Initially, Q2514 is turned on, and Q2516 and Q2522 are turned off. The A sweep ramp from the collector of Q2246 increases the voltage at the base of Q2514. When the base of Q2514 is at the same voltage as the base of Q2516, Q2514 turns off, and Q2516 and Q2522 turn on. Components C2521 and R2521 provide feedback for a fast switch of Q2522, causing a sharp negative pulse through C2525. This pulse produces a LO at pin 5 of U2524A. The LO at pin 5 of U2524A produces a LO at pin 3 of U2524B which starts the B sweep. CR2514 and CR2516 are protection diodes. When S2510 is in the A position, the base of Q2522 is grounded, preventing the B sweep from starting.


+100V
R2514 100K
CR2514
CR2516
'A' SWEEP FROM Q2246
DIAG 6B
R2511 10K
R2512 22K
-8V
Q2514
Q2516
P2510
+8V
R2517 1K
C2517 15µF
R2516 2K
R2515 200
DELAY TIME POSITION
C2521 15
R2521 56K
S2550B
SEC/DIV
AND DELAY TIME
.5 S .2 .1
50 20 10 5 mS 2 1 .5 .2 .1
50 20 10 5 µS 2 1 .5 .2 .1
+8V
R2590 150
+5V
VR2590 5.1V
+5V
U2524A 1/4 7400
R2523 5.6K
C2525 47
R2525 3.9K
+4.7
Q2522
R2527 6.2K
R2519 7.5K
+8V
R2539 68
C2539 15µF
R2537 680
CR2535
R2535 1.2K
U2524B 1/4 7400
+100V
R2541 10K
+0.6
C2252C 1µF
R2552 10
C2252D .01
J2550-8
J2550-7
+8V
Q2542
C2546
R2546 51
Q2546
B SWEEP TO R2311 THRU S2510
DIAG 6B
PARTIAL A14 B TIMING BOARD
J2550-6
R2554 82.5K
R2556 41.2K
R2553 412K
R2555 82.5K
R2557 8.25K
R2558 8.25K
-8V
R2544 24.3K
C2544 22
Q2544
U2524 7400
+5V
HOLDOFF FROM U2224A PIN7
DIAG 6B
C2548 47
+3.4
C2536 87
C2535 1-6
CR2536
R2548 10K
R2547 20K
Q2548
C2533 22
R2533 15K
R2532 5.1K
R2531 24K
R2545 17.4K
'A' UNBLANKING FROM R2237-R2188
DIAG 6B
REFER TO BACK OF FIRST DIAGRAMS SECTION PULLOUT FOR A12 HORIZONTAL BOARD COMPONENT LOCATIONS
PARTIAL A12 HORIZONTAL BOARD
P2-8
J2-8
'A' OR 'B' UNBLANKING TO Q416 Z AXIS AMP
DIAG 4
SEE DIAG 6B
S2510
DISPLAY MODE
SHOWN IN "A"
A INTEN BY B
A
B
PARTIAL A1 INTERFACE BOARD
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.