FM MODULATOR CONTROLLER

GENERAL DESCRIPTION

The TDA2507 accepts FM signals that are sequentially modulated by two alternating subcarrier frequencies (SECAM signals) and provides sequential DC output levels to control the FM modulator.

The IC is intended for use with the SECAM encoder TDA2506 but can be adapted for other applications. Timing reference pulses from the modulator are required.

Two frequency reference phase-lock loops are contained within the IC; one for 4.40625 MHz, and one for 4.250 MHz. Other frequencies can be accomplished by using external reference sources.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)	$V_P = V_{3-6}$		4.75	5.0	7.0	V
Supply current	V_P = 5 V; both PLL circuits on	I_3	–	40	–	mA
Reference voltage		V_{2-6}	3.34	3.45	3.56	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Operating ambient temperature range		T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2507 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2507T: 16-lead mini-pack; plastic (SO16L; SOT162A).

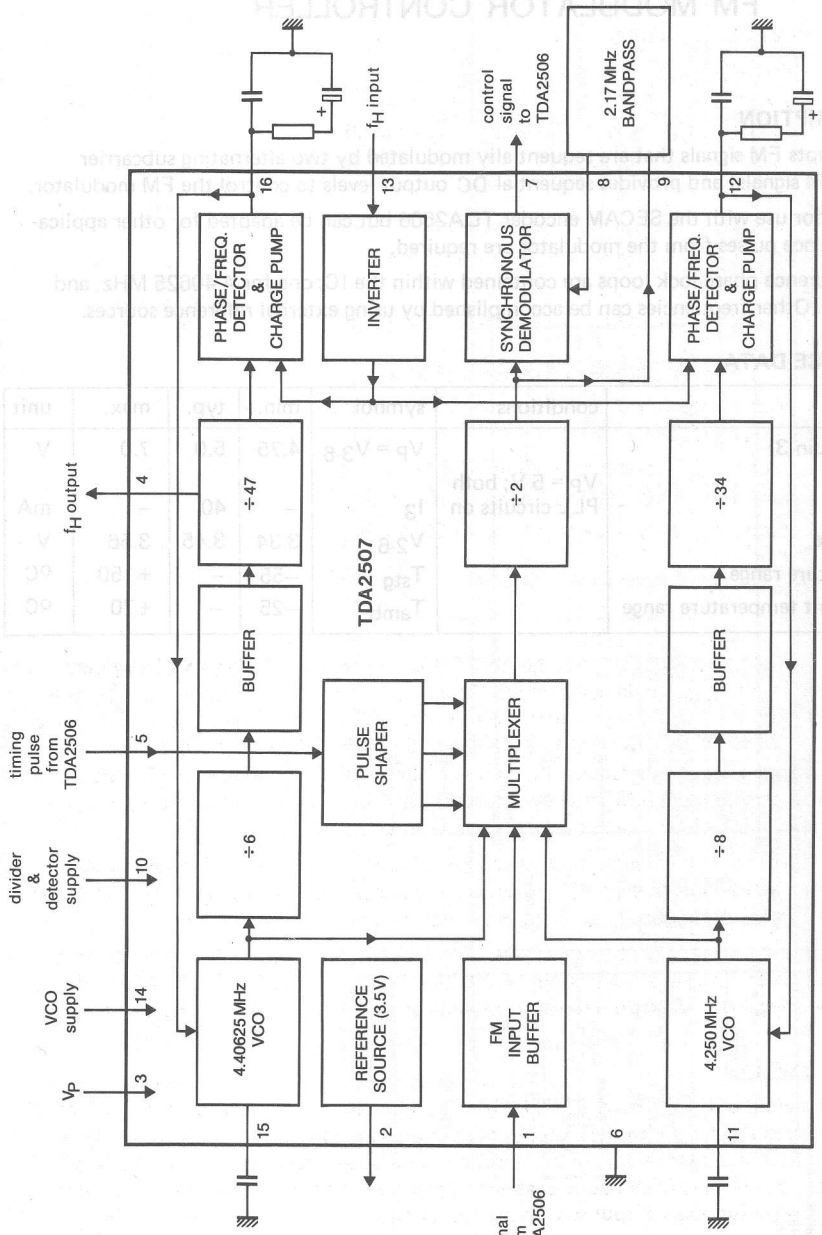

Fig.1 Block diagram.

PINNING

Pin functions

pin	description
1	FM signal input (from TDA2506)
2	Reference voltage output
3	Positive supply voltage
4	Horizontal sync output (f_H = 4 406.250/282 = 15.625 kHz)
5	Timing pulse input (from TDA2506)
6	Ground
7	Control signal output to TDA2506 via low-pass filter
8	Input to synchronous demodulator from band-pass filter
9	Output to band-pass filter
10	Supply voltage for the divider stages and phase/frequency detectors of the two phase-lock loops (PLL)
11	Tuning capacitor for the 4.250 MHz reference oscillator
12	Filter for the phase/frequency detector of the 4.250 MHz phase-lock loop
13	Horizontal sync input (f_H)
14	Supply voltage for the two reference oscillators
15	Tuning capacitor for the 4.40625 MHz reference oscillator
16	Filter for the phase/frequency detector of the 4.40625 MHz phase-lock loop.

FUNCTIONAL DESCRIPTION

Phase-lock loops

The two phase-lock loops each comprise a voltage-controlled reference oscillator, two frequency divider stages and a phase/frequency detector circuit. The loops are closed by charge pumping the reference oscillators from the phase/frequency detector outputs. The centre frequencies of the loops are set by external capacitors at pin 15 (4.40625 MHz) and pin 11 (4.250 MHz). The divider stages which follow the reference oscillators reduce the frequencies of both the loops to 15.625 kHz (f_H) at their respective inputs to the phase/frequency detectors. The reference signals to both phase/frequency detectors are obtained from the horizontal sync input at pin 13.

The divider and phase/frequency detector circuits can be switched off by connecting pin 10 to ground. This leaves only the VCO of each PLL in circuit and allows external signals to be injected at pins 15 and 11, or crystals to be used for tuning the oscillators.

The accuracy of crystal tuning using only one crystal can be obtained by connecting pins 10, 14 and 16 to the reference voltage at pin 2 and connecting a 4.40625 MHz crystal to pin 15. The 4.250 MHz PLL will follow the crystal-derived f_H reference from pin 4 via pin 13 and its phase/frequency detector.

Multiplexer and pulse shaper

The multiplexer receives the 4.40625 and 4.250 MHz reference frequencies from the two VCOs and the FM signals D'_R* and D'_B* from the TDA2506 modulator. The signals are gated one at a time to the multiplexer output in a sequence determined by the timing pulses from TDA2506. The levels of the timing pulses (pin 5) are used in the pulse shaper to generate enable pulses for the multiplexer (see Figs 2 and 3). The multiplexer output sequence is as follows:

4.40625 MHz (2 lines); D'_R* FM signal (1 line); 4.250 MHz (2 lines); D'_B* FM signal (1 line); repeating. The selection of D'_R* or D'_B* FM signal is a feature of the timing of the input at pin 5.

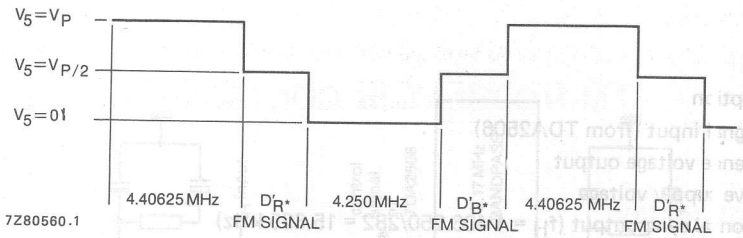

Fig.2 Timing pulse waveform for multiplexer output sequence.

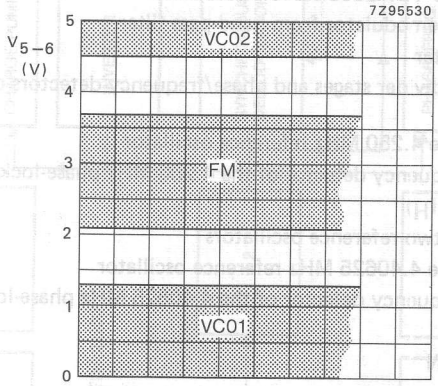

Fig.3 Switching levels of the timing pulse at pin 5.

Divide-by-two stage and synchronous demodulator

The divide-by-two stage halves the frequencies present in the multiplexer output and equalizes the amplitude and pulse shapes of the sequential signals.

Demodulation of the multiplexed signal is performed by filtering the signal via a 2.17 MHz band-pass filter (between pins 8 and 9) and using this filtered signal as a synchronous switch for the main signal. The DC level of the signal from pin 9 is referred externally to the reference voltage from pin 2. An external low-pass filter is required for the output signal from pin 7.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.4		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

CHARACTERISTICS

$V_P = V_{3-6} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3)		V_P	4.75	5.0	7.0	V
Supply current	$V_{14} = V_{10} = V_2$	I_P	–	35	–	mA
Supply current	$V_{14} = V_2$	I_P	–	20	–	mA
Reference voltage (pin 2)		V_{2-6}	3.34	3.45	3.56	V
Phase-lock loops						
DC voltage output level						
pin 11		V_{11-6}	2.4	2.6	2.8	V
pin 15		V_{15-6}	2.4	2.6	2.8	V
Amplitude of oscillation (peak-to-peak value)						
pin 11		$V_{11(p-p)}$	–	130	–	mV
pin 15		$V_{15(p-p)}$	–	130	–	mV
Input current	see Fig.5					
pin 11	$V_{12-6} = 1.5$ V	I_{11}	–	130	–	μA
pin 15	$V_{16-6} = 1.5$ V	I_{11}	–	130	–	μA
Limiting values for VCO control voltages						
pin 12		V_{12}	0.8	–	1.9	V
pin 16		V_{16}	0.8	–	1.9	V
Output resistance at pin 4	V_4 = HIGH	R_4	5.1	6.8	8.5	kΩ
Input resistance at pin 13		R_{13}	200	–	–	kΩ
Amplitude of f_H pulse required at pin 13	note 1	V_{13}	2	–	–	V
FM input buffer (pin 1)						
Input resistance		R_1	180	–	–	kΩ
Switching level of FM input		V_1	2.2	2.3	2.4	V
Required input amplitude		V_1	0.5	–	2.0	V
Pulse shaper input (pin 5)						
Input resistance		R_5	200	–	–	kΩ
Demodulator						
Sink current at pin 9 into divide-by-two circuit	V_9 = LOW	I_9	0.6	0.9	1.2	mA
Demodulator input bias voltage at pin 8		V_8	1.60	1.68	1.76	V
Demodulator output current from pin 7	see Fig.6					
output current at A		$-I_7$	0.6	0.9	1.2	mA
output current at B		I_7	1.2	0.9	0.6	mA

Note to the characteristics

1. Duty factor and timing not important.

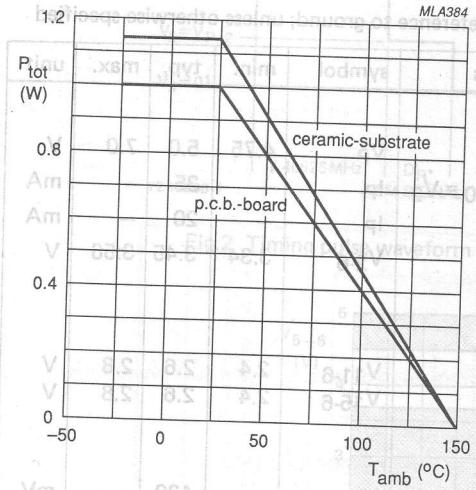

Fig.4a Power derating curve (TDA2507).

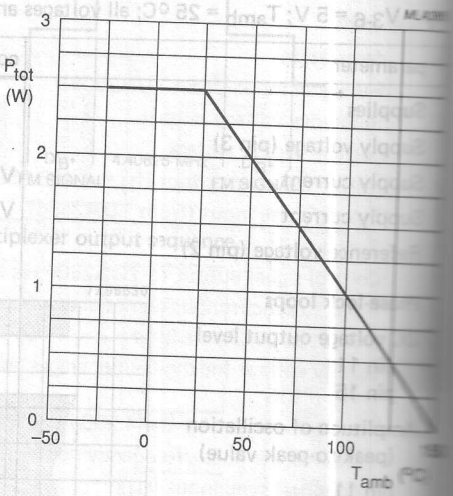

Fig.4b Power derating curve (TDA2507T).

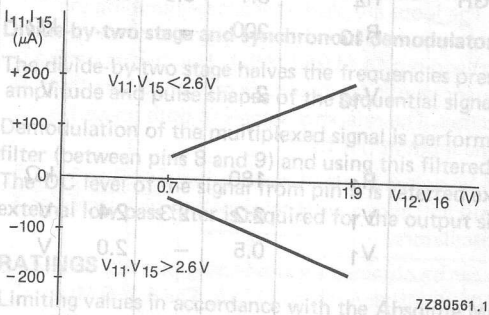

Fig.5 Current input to pins 11 and 15 as a function of voltage at pins 12 and 16 (typical values).

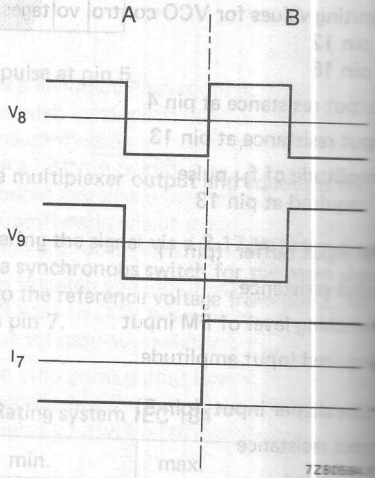

Fig.6 Demodulator output current from pin 7 (typical values).

APPLICATION INFORMATION (continued)

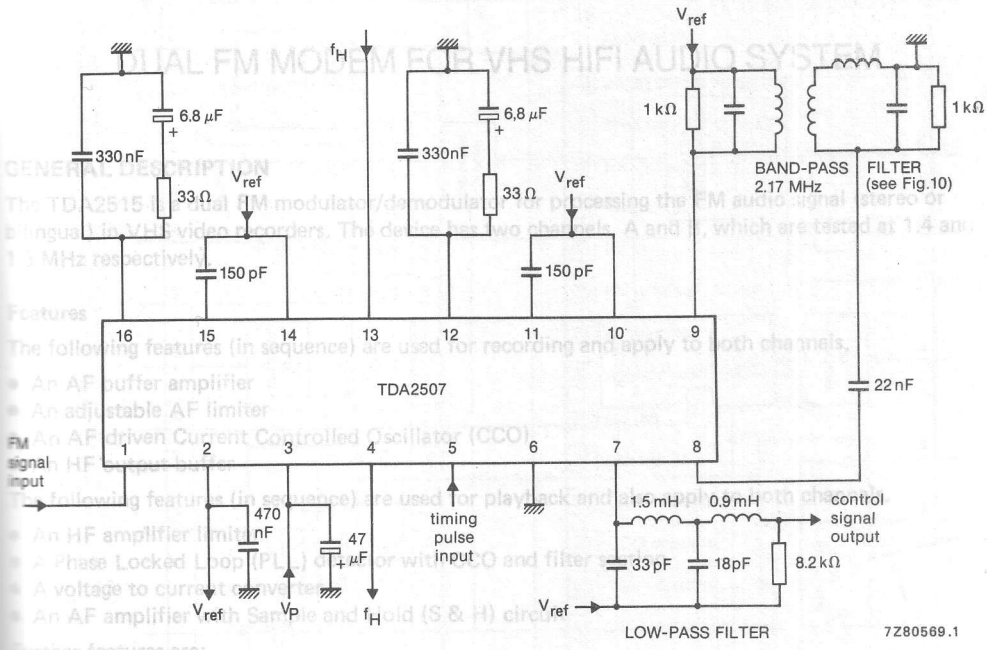

Fig.7 Application diagram using PLL tuning; V_P = 5 V.

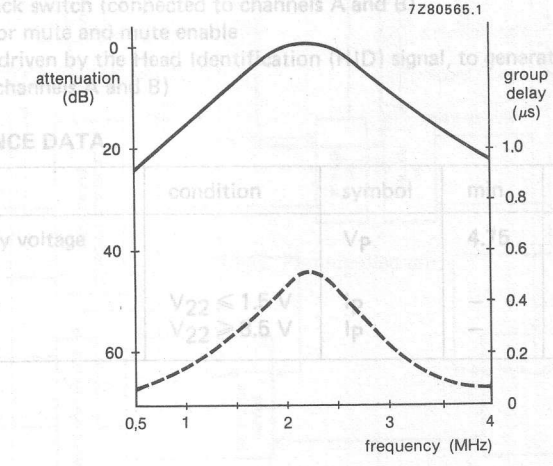

Fig.8 Typical response of 2.17 MHz band-pass filter.