NEW TECHNICAL THEORY FOR SERVICING

DTX-10

OPERATION MANUAL

1. BLOCK DIAGRAM & CIRCUIT DIAGRAMS

1-1. BLOCK DIAGRAM

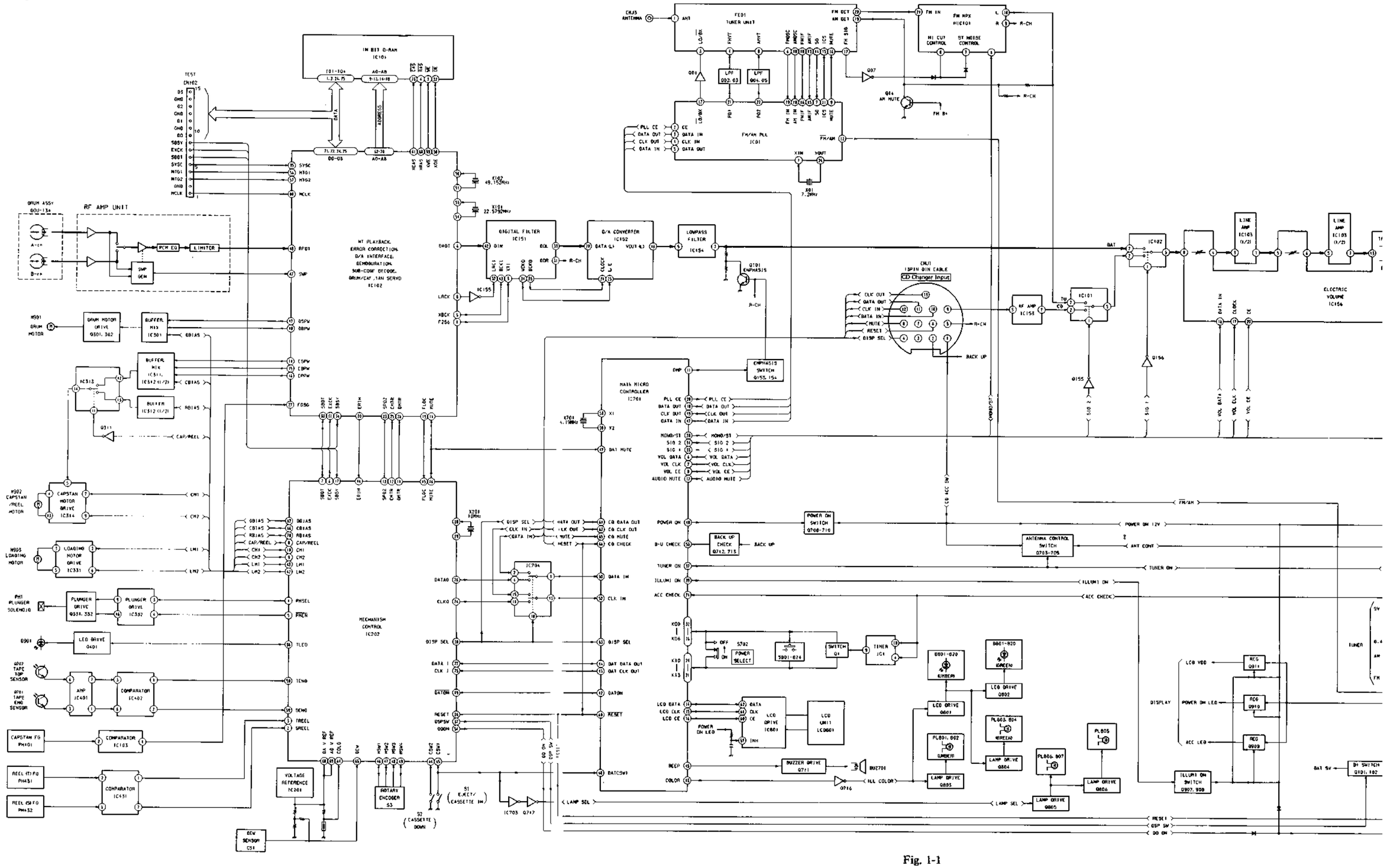
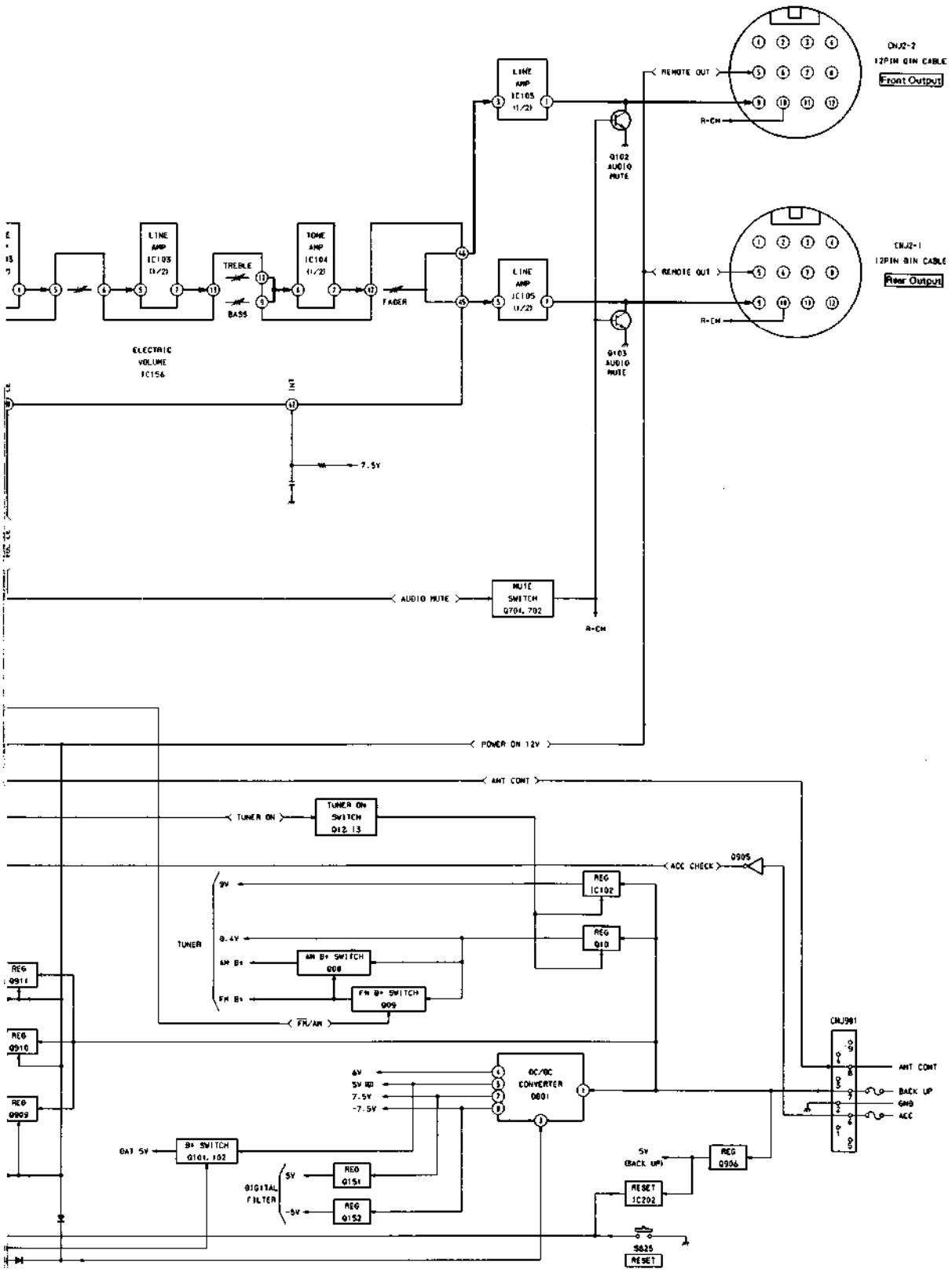


Fig. 1-1


CNJ2-2
12PIN BIN CABLE
Front Output
REMOTE OUT
R-CH
LINE AMP IC105 (1/2)
Q102 AUDIO MUTE
CNJ2-1
12PIN BIN CABLE
Rear Output
REMOTE OUT
R-CH
Q103 AUDIO MUTE
LINE AMP IC103 (1/2)
TREBLE
BASS
TONE AMP IC104 (1/2)
FADER
LINE AMP IC105 (1/2)
ELECTRIC VOLUME IC156
INT
7.5V
AUDIO MUTE
MUTE SWITCH Q704, 702
R-CH
POWER ON 12V
ANT CONT
TUNER ON
TUNER ON SWITCH Q12, 13
ACC CHECK
Q905
REG IC102
REG Q10
TUNER
9V
8.4V
AM B+
FM B+
AM B+ SWITCH Q08
FM B+ SWITCH Q09
FM/AM
REG Q911
REG Q910
REG Q909
CNJ901
ANT CONT
BACK UP
GND
ACC
DC/DC CONVERTER Q801
6V
5V SD
7.5V
-7.5V
DAT 5V
B+ SWITCH Q101, 102
DIGITAL FILTER
5V
-5V
REG Q151
REG Q152
5V (BACK UP)
REG Q906
RESET IC202
S825
RESET

1-2. SCHEMATIC DIAGRAMS

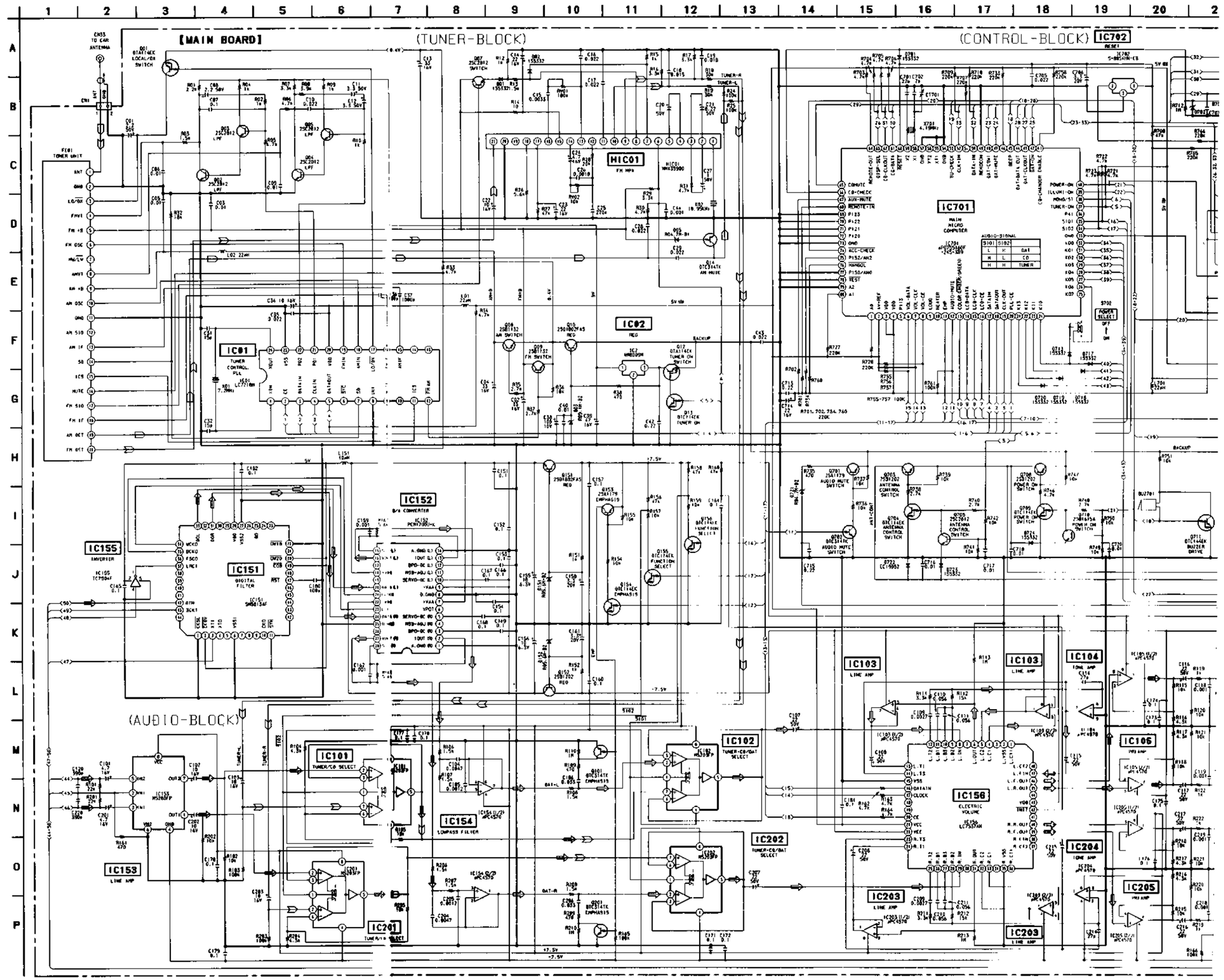
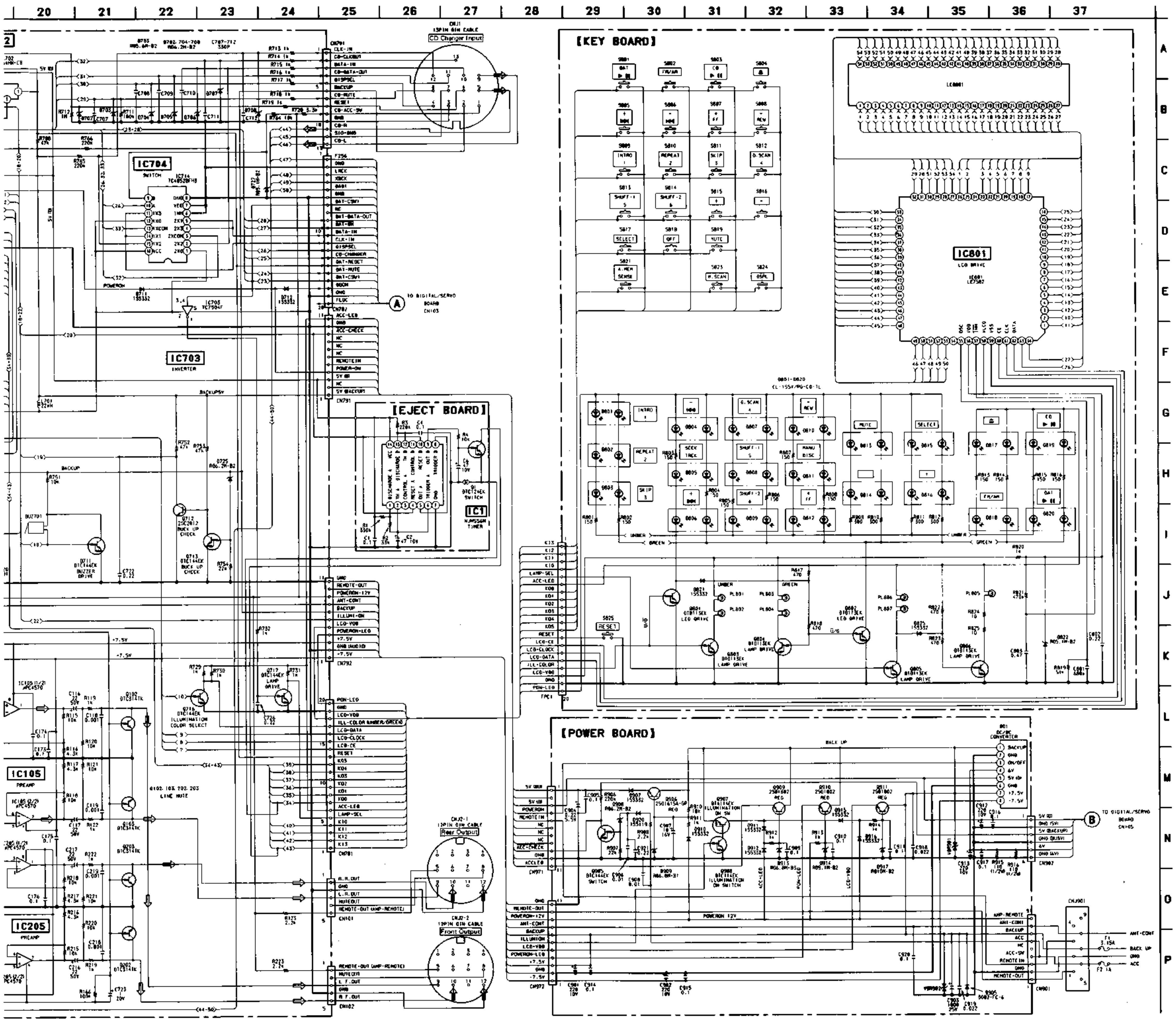


Fig. 1-2



KEY BOARD
EJECT BOARD
POWER BOARD
IC704
SWITCH
IC703
INVERTER
IC801
LCD DRIVE
IC1
NJM556M TIMER
IC105
PREAMP
IC205
PREAMP
CD Changer Input
Rear Output
Front Output
TO DIGITAL/SERVO BOARD CN103
TO DIGITAL/SERVO BOARD CN105
Q102, 103, 202, 203 LINE MUTE
DC/DC CONVERTER

SCHEMATIC DIAGRAM

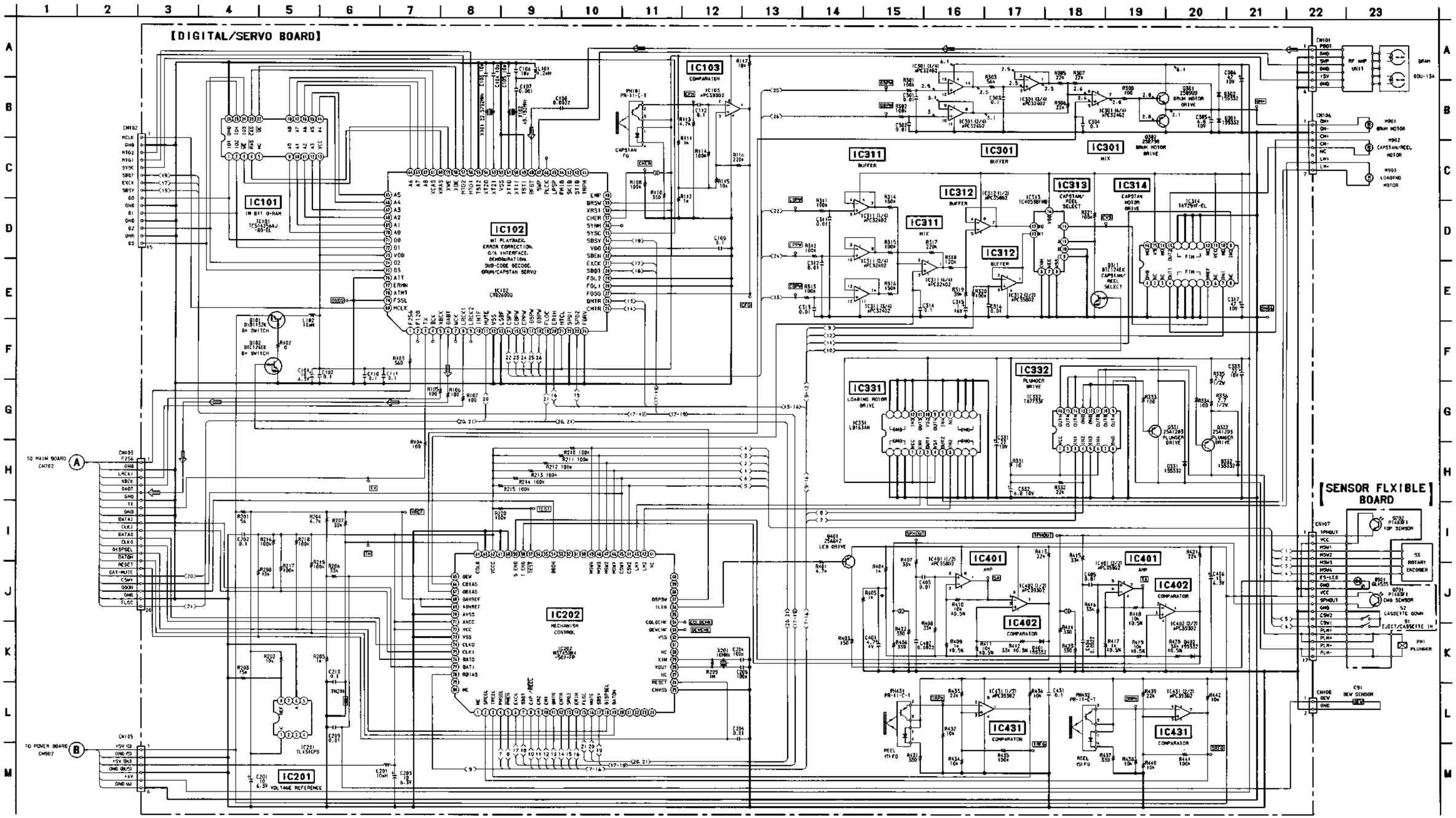


Fig. 1-3

2. BASIC DATA FORMAT

This unit uses a new mechanism featuring NT (non-tracking) system. Although it is used only for playback, prerecorded tapes to be used are the same as conventional ones. In this section, the DAT format is explained.

2-1. MAIN SPECIFICATIONS

Table 2-1

Mode / Item	DAT (REC/PB mode)				Pre-recorded tape (PB mode only)	
	Standard	Option 1	Option 2	Option 3	Normal track	Wide track
Number of channels (CH)	2	2	2	4	2	4
Sampling frequency (kHz)	48	32	32	32	44.1	
Quantization bits (bit)	16 (linear)	16 (linear)	12 (non-linear)	12 (non-linear)	16 (linear)	16 (linear)
Linear recording density (KBPI)	61.0	61.0			61.0	61.1
Surface recording density ($MBPI^2$)	114	114			114	76
Transmission rate (MBPS)	2.46	2.46	1.23	2.46	2.46	
Sub-code capacity (KBPS)	273.1	273.1	136.5	273.1	273.1	
Modulation method	8-10 conversion					
Correction method	Double Read-Solomon mode					
Tracking method	Area division ATF					
Cassette size (mm)	73 x 54 x 10.5					
Recording time (min)	120	120	240	120	120	80
Tape width (mm)	3.81					
Tape type	Metal powder					Oxide tape
Tape thickness (μm)	13 ± 1μ					
Tape speed (mm/s)	8.15	8.15	4.075	8.15	8.15	12.225
Track pitch (μm)	13.591				13.591	20.41
Track angle	6°22'59.5"					6°23'29.4"
Standard drum specification	φ30 90° wrap					
Drum speed (rpm)	2,000		1,000	2,000	2,000	
Relative speed (m/s)	3.133		1.567	3.133	3.133	3.129
Head azimuth angle	±20°					

2-2. TRACK FORMAT

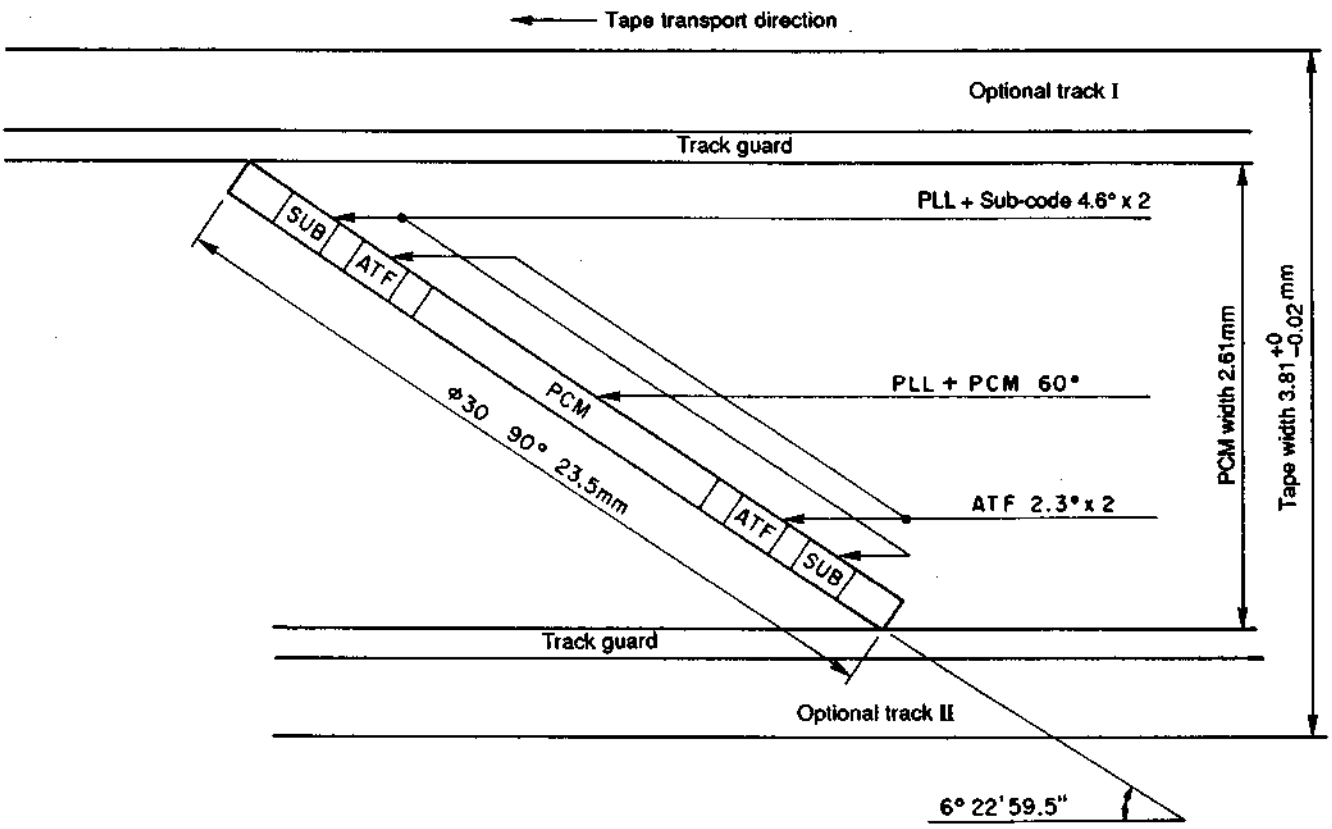


Fig. 2-1

Table 2-2

1	2	3 (SUB-1)	4	5	6 (ATF)	7	8	9 (PCM)	10	11 (ATF)	12	13	14 (SUB-2)	15	16

		Frequency	*Angle (deg)	Number of blocks	Time (μs)
1	MARGIN	1/2 fch	5.051	11	420.9
2	PLL (SUB)	1/2 fch	0.918	2	76.5
3	SUB-1		3.673	8	306.1
4	POST AMBLE	1/2 fch	0.459	1	38.3
5	IBG	1/6 fch	1.378	3	114.8
6	ATF		2.296	5	191.3
7	IBG	1/6 fch	1.378	3	114.8
8	PLL (PCM)	1/2 fch	0.918	2	76.5
9	PCM		58.776	128	4898.0
10	IBG	1/6 fch	1.378	3	114.8
11	ATF		2.296	5	191.3
12	IBG	1/6 fch	1.378	3	114.8
13	PLL (SUB)	1/2 fch	0.918	2	76.5
14	SUB-2		3.673	8	306.1
15	POST AMBLE	1/2 fch	0.459	1	38.3
16	MARGIN	1/2 fch	5.051	11	420.9
Total			90	196	7500

Recording density ..... 61.0 KBPI

fch 9.408MHz

* Value obtained by using ϕ30, 90° wrap angle, 2000 rpm cylinder.

2-3. MAIN DATA (PCM DATA)

2-3-1. Main data area format

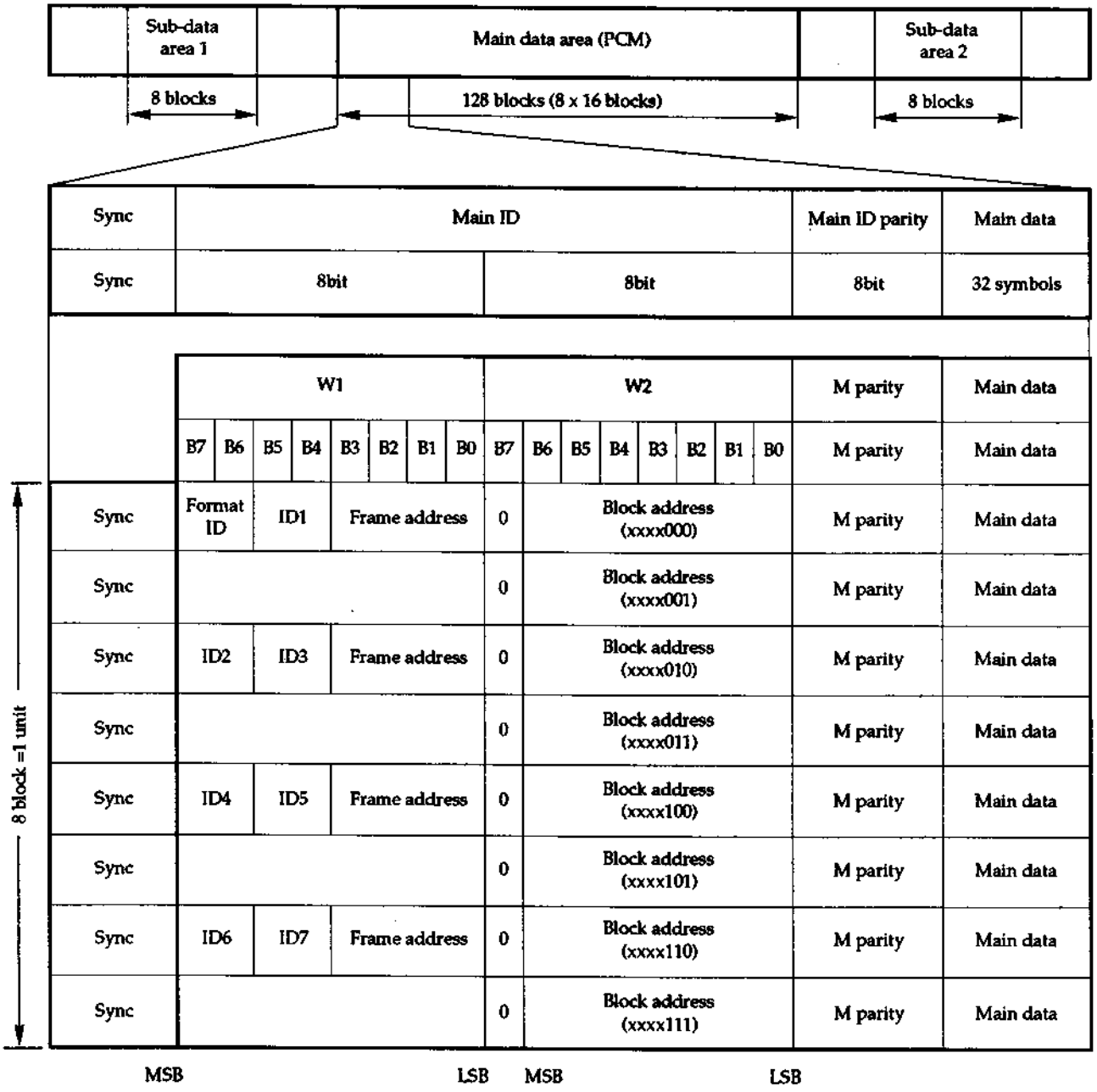


Fig. 2-2 Main data area format

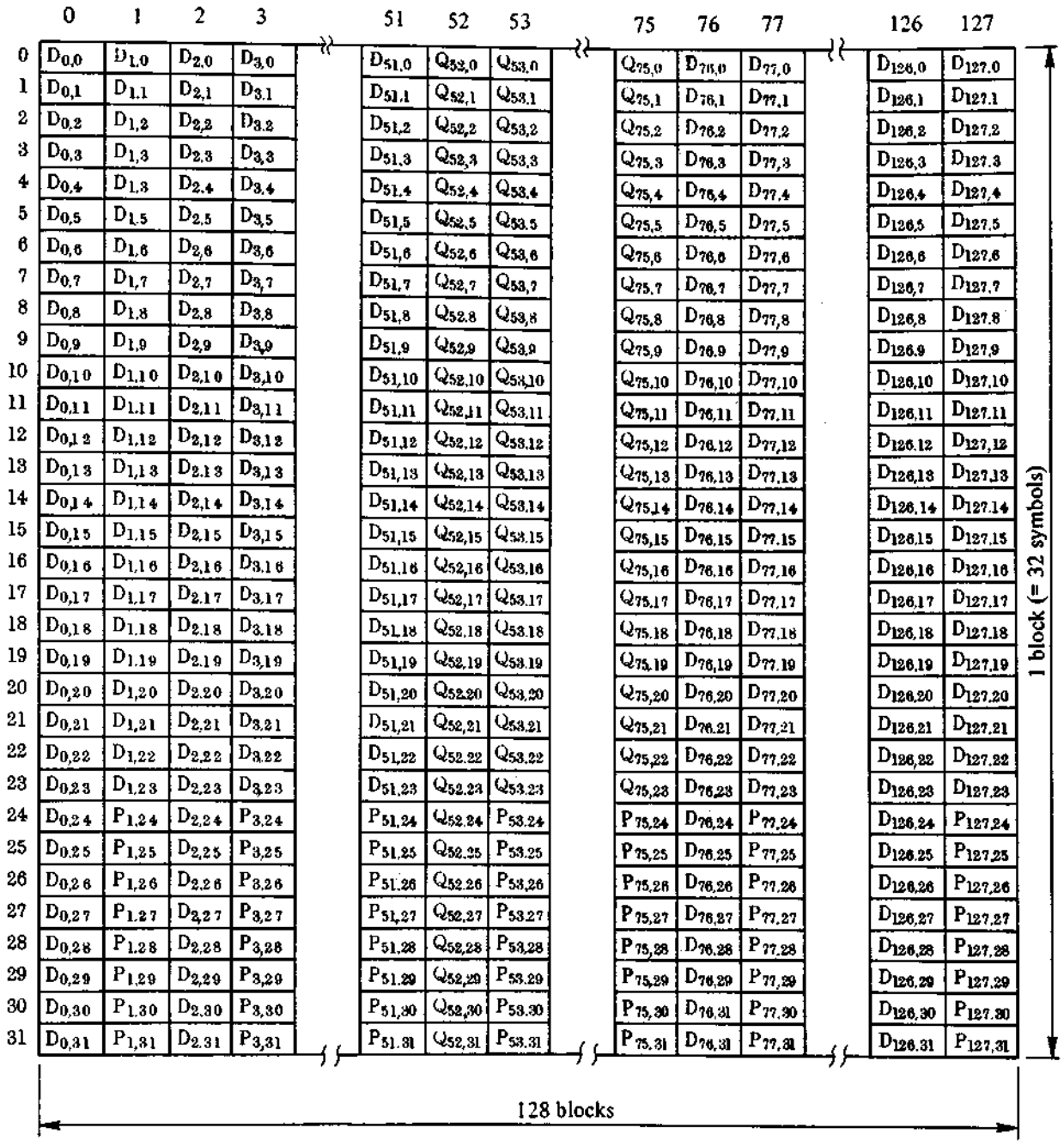
2-3-2. Contents of ID1 to ID7

Table 2-3

	Application	Bit allocation
ID1	Emphasis	B5, B4 0 0 : Not used, OFF 0 1 : 50/15 μs
ID2	Sampling frequency	B7, B6 0 0 : 48 kHz 0 1 : 44.1 kHz 1 0 : 32 kHz
ID3	Number of channels	B5, B6 0 0 : 2 channels 0 1 : 4 channels
ID4	Quantization	B7, B6 0 0 : 16 bits, linear 0 1 : 12 bits, non-linear
ID5	Track pitch	B5, B4 0 0 : Normal track mode 0 1 : Wide track mode
ID6	Digital copy	B7, B6 0 0 : Permit 1 0 : Inhibit 1 1 : Permit only for 1 generation
ID7	Pack	B5, B4 Contents of pack

2-3-3. Main data allocation

Table 2-4



D : Data P : C1 parity Q : C2 parity

2-4. SUB DATA

2-4-1. Sub data area format

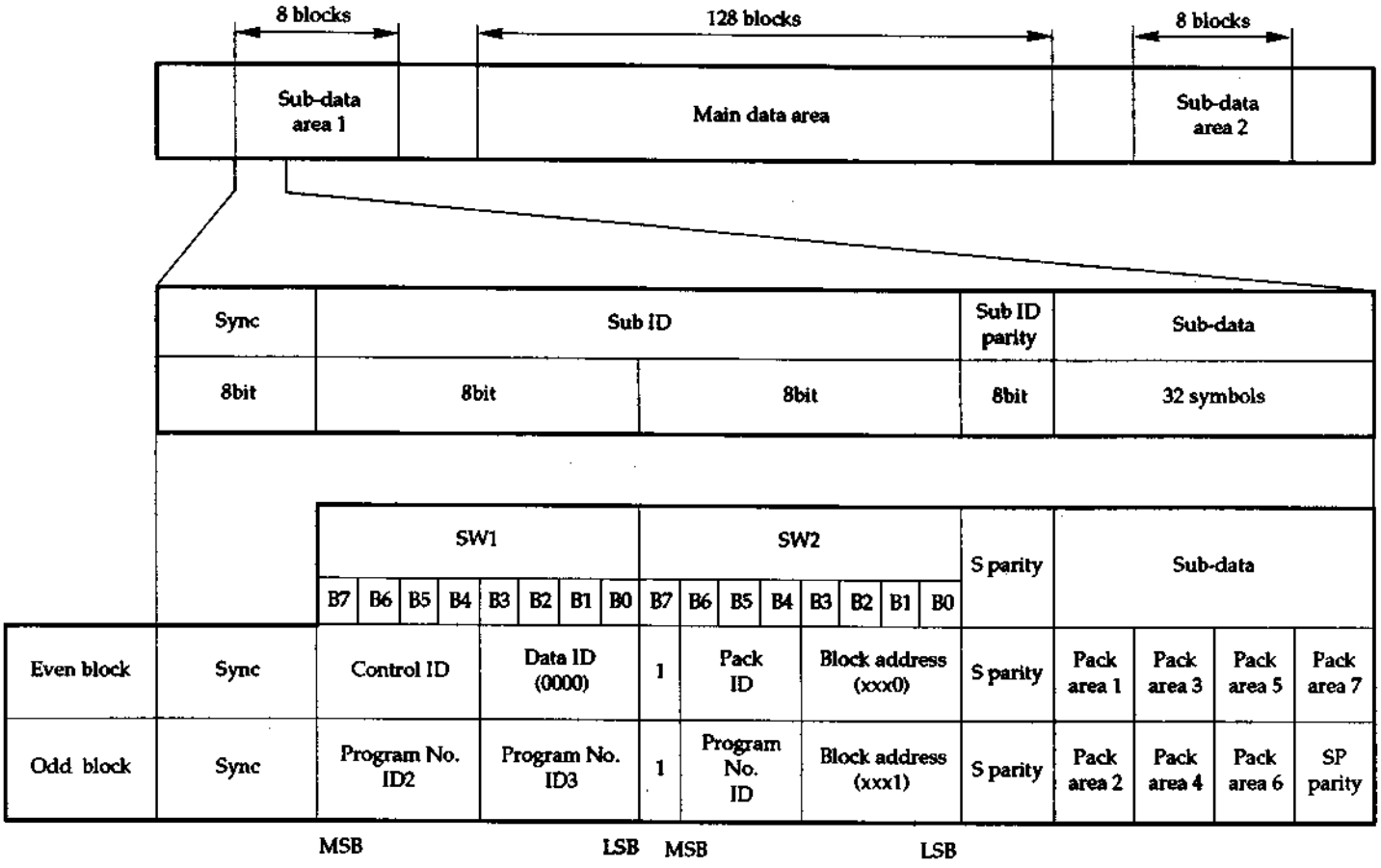


Fig. 2-3 Sub data area format

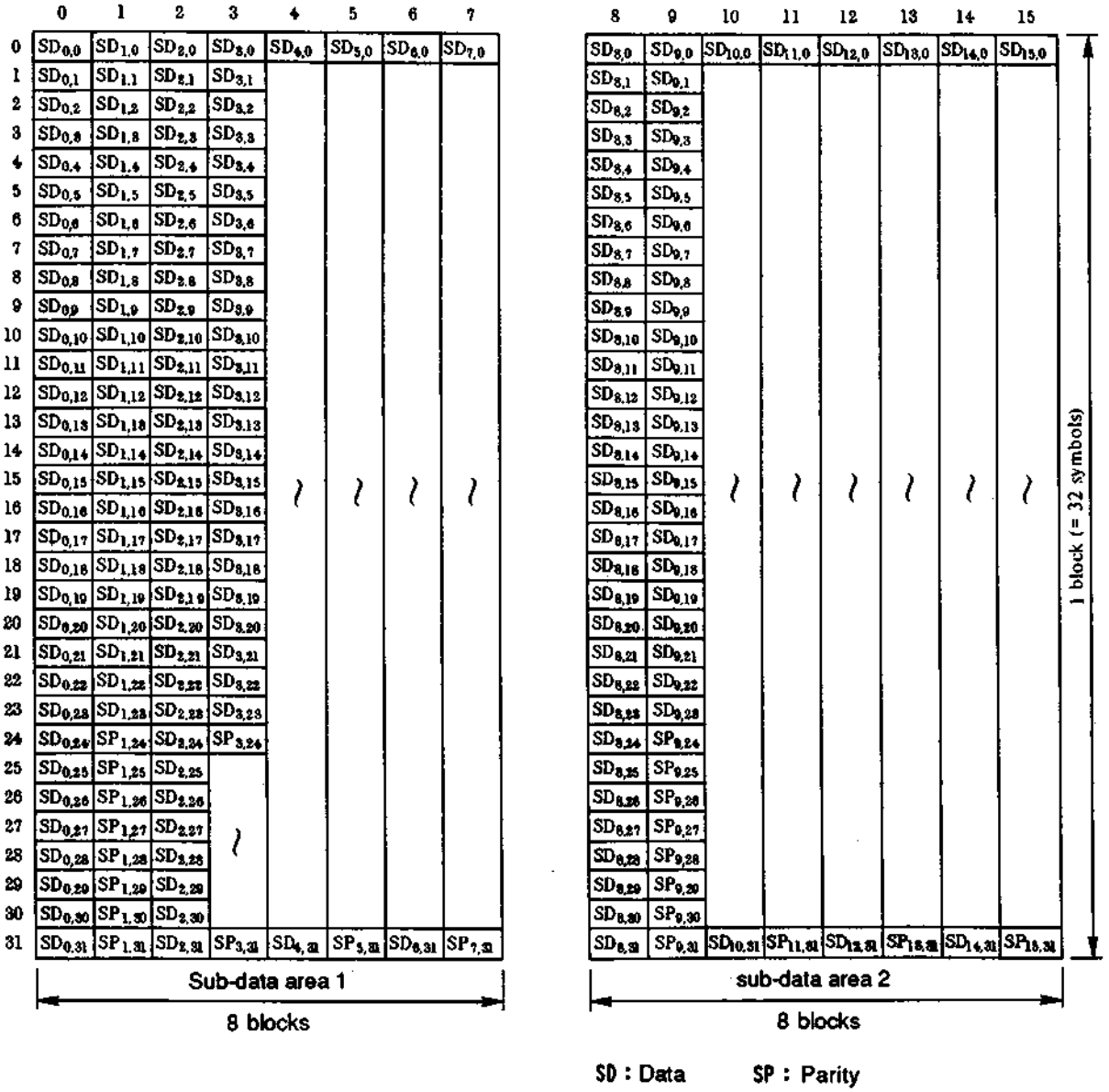
2-4-2. Contents of control ID

Table 2-5

Bit	Item	Contents
B4	TOC-ID	With/without TOC recording
B5	Skip ID	1: Fast-forward to the next S-ID
B6	Start ID (S-ID)	Start of music
B7	Priority ID	With/without after-recording of music No.

2-4-3. Sub data allocation

Table 2-6



3. NT (NON-TRACKING) PLAYBACK

3-1. DOUBLE DENSITY SCAN

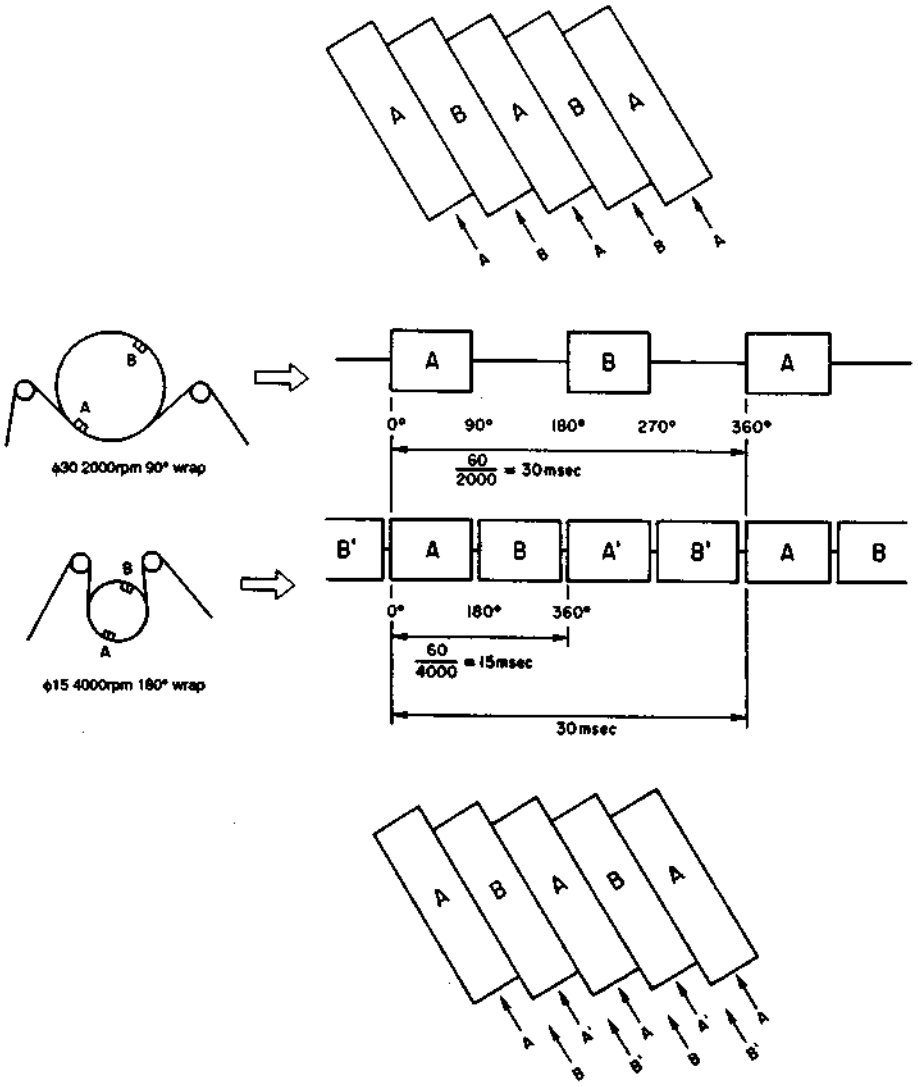


Fig. 3-1

The above shows the comparison of playback waveforms obtained by previous 30ϕ drum and the 15ϕ drum used in this unit. In either type of drum, the relative speed of the head and tape remains unchanged, as shown below.

$$Vr = 30 \times \pi \times \frac{2000}{60} = 15 \times \pi \times \frac{4000}{60} = 3.1\text{m/sec}$$

The RF waveform which is read by each head is the same. But the tape speed is the same so the head of this unit traces on the tape twice in 30 msec while changing its position by a half of tape width.

Each block on recorded track is subjected to C1 parity check, and a good one obtained by tracing twice is written in RAM which is combined as a playback data. This is called the double density scan.

In the following, the first trace is called the A, B scan and the second one is called the A', B' scan for convenience.

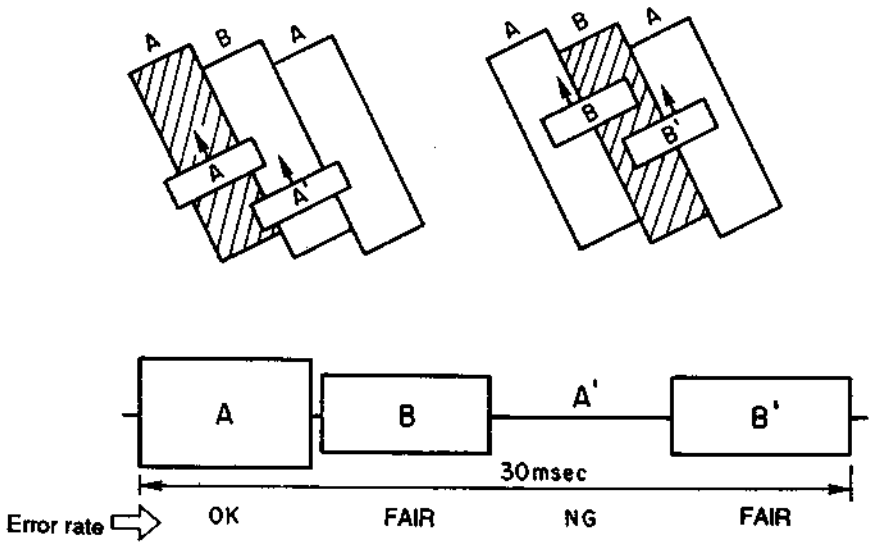


Fig. 3-2

The relation between the recording track on tape and the phase of the head is explained below.

Suppose that the A head is on-track at A track (The signal on B track is not read by the A head because of the azimuth effect). In this case, no signals are read by A' head which passes through the B track.

Also, B and B' heads are traced on the B track while off-tracking by a half, so the output from the head becomes smaller than that at on-track (the error rate becomes worse). But, it can be read twice and the good ones are combined together on the RAM, therefore, the combined error rate is improved as compared with that obtained by reading once as in the case of A and A' heads.

In this system, the playback head width is as large as 28.5μm for the recording track width of 13.6 μm while the previous type of head width is 20μm, so the head output is practically unchanged when the head is slightly off-tracking.

As explained above, the data can be read by the double density scan in any relation between the recording track and the phase of the head.

In the long-time playback mode, the drum speed is the same while the tape feed is reduced to 1/2 of that in normal mode. In this way, the data is read 4 times and hence the error rate is further improved.

3-2. NT PLAYBACK PROCESS

The main data recorded on tape contains 2-position data, a frame address showing the data on the designated track and a block address showing the data of the designated block in the track, in addition to music signals.

By using these address data, any data which are read abruptly in terms of time, which are arranged on tape independently of the actual recording order, can be arranged in a correct order.

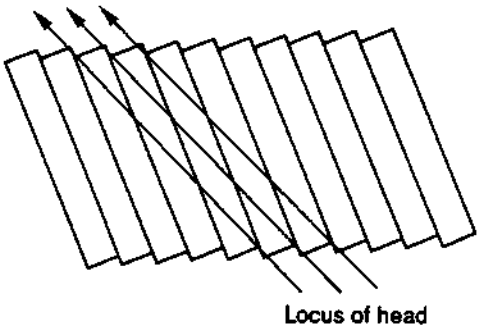


Fig. 3-3

As shown in the above diagram, when the tracing angle of the playback head is largely deviated from the recorded track, the order of recording the signal differs from the order of reproducing, which makes it impossible to reproduce the tape normally (in the case of VTR, a playback picture with noise bars like a picture search appears).

The NT playback process which has been developed this time is such that even a data which was read as shown in the above diagram can be stored in RAM so that the data is rearranged according to the address data when all the required data are stored in RAM. In this way normal playback is always enable.

The maximum inclination of the tracing locus of the head against the recording track depends on the capacity of RAM as a data buffer. This system uses a 1 Mbit RAM which has an allowable capacity of a maximum of 12 frames (1 frame is a pair of A and B tracks).

In other words, data on one track needs not be read throughout a scan. When it is read properly after it has been scanned several times, it is arranged correctly in RAM, whereby it is sent to the signal processing block for normal playback of audio signals.

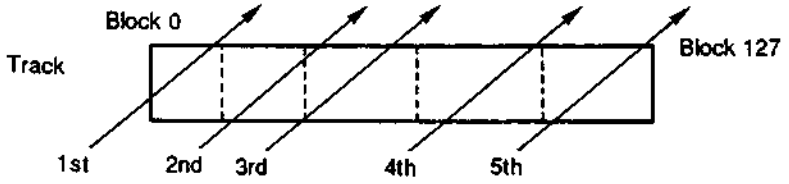


Fig. 3-4

At this time, when the data is scanned only once, a gap is produced between traces so some part of the data cannot be read (such data cannot be reproduced even by the NT system). Therefore, a ϕ15, 4000 rpm drum capable of double density scan is used to read all the data.

It should be noted that the ability of storing the data in a large capacity RAM eliminates the variations of time base in the tape drive direction, or wow-flutter. It is very useful against vibrations or thermal deformation of tape which easily occur during mobile operation.

4. CONFIGURATION

4-1. OUTLINE

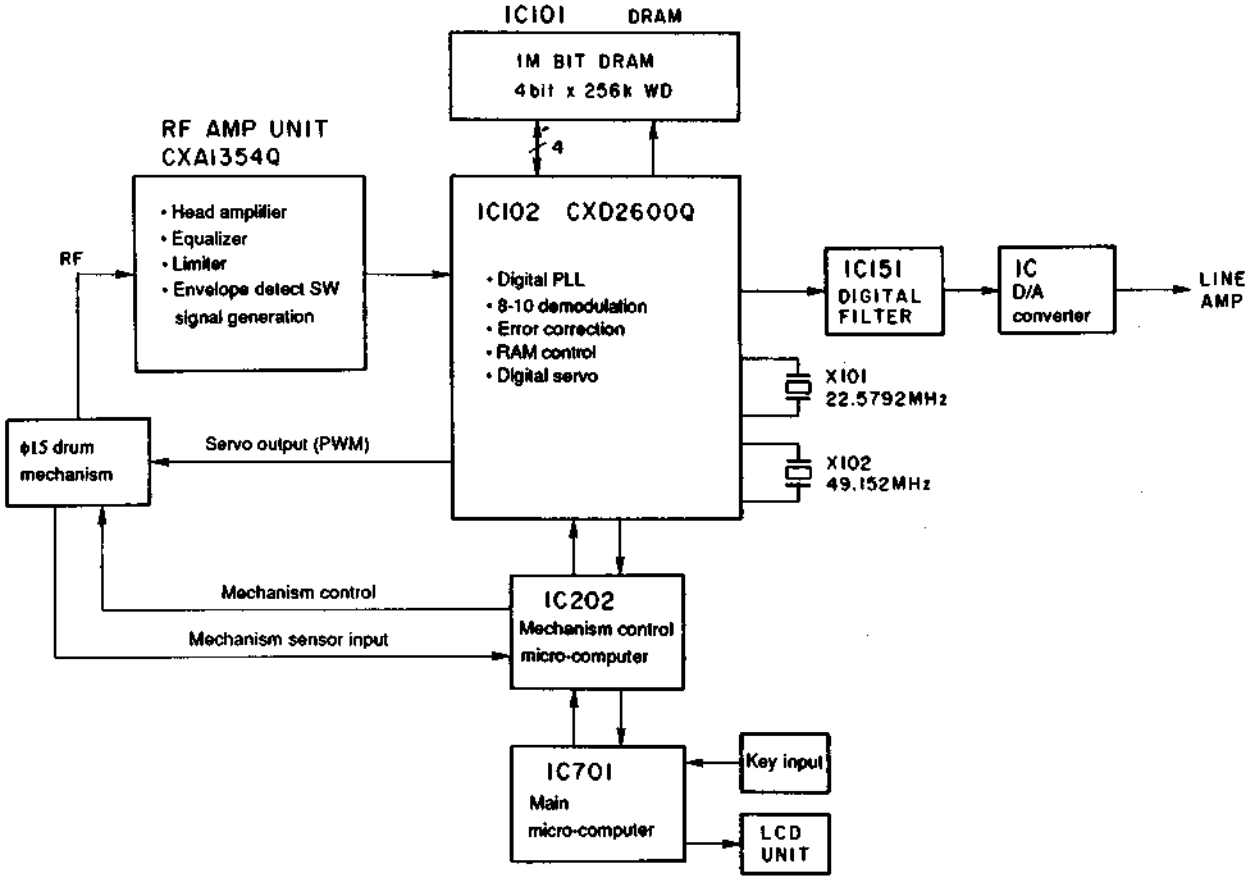


Fig. 4-1

The major parts used with this unit are as follows.

1. φ15 drum mechanism (with 3 motors) for mobile operation
2. Two micro-computers (main and mechanism control)
3. Playback equalizer amplifier IC CXA1354Q
4. Playback signal processing IC CXD2600Q (with 1M bit DRAM)

The NT (non-tracking) playback DAT is composed of these parts. Since this unit is used only for playback, drum PG and FG are not required.

4-2. IC701 MAIN MICRO-COMPUTER (μPD75516GF) PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function
1	AO	I	Destination setting input
2	AVREF	I	A/D converter reference voltage input
3, 4	VDD	—	Positive power supply input
5	NC	O	
6	VOL DATA	O	Serial data output(for electronic volume IC)
7	VOL CLK	O	Serial transfer clock(for electronic volume IC)
8	VOL CE	O	Electronic volume enable signal
9, 10	NC	O	
11	EMP	O	De-emphasis(H:De-emphasis ON)
12	AUDIO MUTE	O	Muting control
13	COLOR	O	Illumination color control
14	LCD DATA	O	Serial data output(for LCD driver)
15	LCD CLK	O	Serial data transfer clock(for LCD driver)
16	LCD CE	O	LCD drever enable signal
17	DATA IN	I	Information input from PLL-IC
18	DATA OUT	O	Serial data output(for PLL-IC)
19	CLK OUT	O	Serial data transfer clock(for PLL-IC)
20	PLL CE	O	PLL-IC enable signal
21~24	KI3~KI0	I	KEY information input
25~32	KO7~KO0	O	KEY-RETURN signal source
33	GND	—	Ground potential
34	SIG2	O	Audio source select signal
35	SIG1	O	

	SIG1	SIG2
AUX	L	L
DAT	L	H
CD	H	L
TUNER	H	H

Pin No.	Pin Name	I/O	Function
36	NC	O	
37	TUNER ON	O	Tuner power ON output
38	MONO/ST	I/O	AUTO STEREO/MONAURAL selection
39	ILLUMI ON	O	Illumination output
40	POWER ON	O	SYSTEM POWER ON output
41	CD CHANGER ENABLE	I	WITH/WITHOUT CD control function
42	DAT ON	O	DAT mechanical deck control(L:DAT ON)
43	DAT CLK OUT	O	DAT data transfer clock line
44	DAT DATA OUT	O	DAT data transfer data line
45	BEEP	O	Buzzer output signal(2kHz/1kHz)
46	————————	—	(Not used)
47	DAT MUTE	I	DAT mute request input
48	DAT CSW1	I	DAT mechanical deck cassette compartment SW No.1 (L →H:Tape loading start)
49	REMCOM	I	Remote control input(not used)
50	DATA IN	I	Auto changer information and DAT mechanical deck information input
51	————————	—	(Not used)
52	CLK IN	I	CD data and DAT data input clock
53	BU-CHECK	I	Back-up check
54～57	————————	—	(Not used)
58	X1	—	4.19MHz
59	X2	—	Main system clock
60	RESET	I	RESET input
61	CD DATA	O	CD data transfer data line
62	CD CLK OUT	O	CD data transfer clock line
63	DISP SEL	O	DISPLAY selection
64	REMOTE OUT	O	AUX-STOP(not used)
65	CD MUTE	I	CD mute request input

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>66</td><td>CD CHECK</td><td>I</td><td>CD presence check</td></tr>
<tr><td>67～72</td><td>————————</td><td>—</td><td>(Not used)</td></tr>
<tr><td>73</td><td>GND</td><td></td><td>Ground potential</td></tr>
<tr><td>74</td><td>ACC CHECK</td><td>I</td><td>Accessory input check</td></tr>
<tr><td>75～77</td><td>————————</td><td>—</td><td>(Not used)</td></tr>
<tr><td>78</td><td>TEST</td><td>I</td><td>Test mode switch
(L:Test mode,H:Normal mode)</td></tr>
<tr><td>79</td><td>A2</td><td>I</td><td rowspan="3">Destination setting input
<table>
<tr><th></th><th>A0</th><th>A1</th><th>A2</th></tr>
<tr><td>USA</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>JAPAN</td><td>H</td><td>H</td><td>L</td></tr>
<tr><td>E-9K</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>E-10K</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>AEP</td><td>L</td><td>Don't care</td><td>Don't care</td></tr>
</table></td></tr>
<tr><td>80</td><td>A1</td><td>I</td></tr>
<tr><td>1</td><td>A0</td><td>I</td></tr>
</table>

4-3. IC202 MECHANISM CONTROL MICRO-COMPUTER (M37450M4FP) PIN FUNCTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>NC</td><td>—</td><td>————————</td></tr>
<tr><td>2</td><td>S REEL</td><td>I</td><td>FGinput on supply side</td></tr>
<tr><td>3</td><td>T REEL</td><td>I</td><td>FG input on take-up side</td></tr>
<tr><td>4</td><td>PMSEL</td><td>0</td><td>Plunger PULL/RELEASE selection(H:PULL)</td></tr>
<tr><td>5</td><td>PMEN</td><td>0</td><td>Plunger ON/OFF selection(L:ON)</td></tr>
<tr><td>6</td><td>EXCK</td><td>0</td><td>Communication clock between mechanism controller and CXD2600Q</td></tr>
<tr><td>7</td><td>SBDT</td><td>I/0</td><td>Communication data between mechanism controller and CXD2600Q</td></tr>
<tr><td>8</td><td>CAP/REEL</td><td>0</td><td>Selection of capstan servo in CXD2600Q(H:Used, L:Not used)</td></tr>
<tr><td>9</td><td>CM2</td><td>0</td><td rowspan="2">Capstan motor control
<table>
<tr><th></th><th>CM1</th><th>CM2</th></tr>
<tr><td>Stop</td><td>0</td><td>0</td></tr>
<tr><td>Forward</td><td>1</td><td>0</td></tr>
<tr><td>Reverse</td><td>0</td><td>1</td></tr>
<tr><td>Brake</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>10</td><td>CM1</td><td>0</td></tr>
<tr><td>11</td><td>DMTR</td><td>0</td><td>CXD2600Q drum servo control(H:ON)</td></tr>
<tr><td>12</td><td>CMTR</td><td>0</td><td>CXD2600Q capstan servo control(H:ON)</td></tr>
<tr><td>13</td><td>SPD2</td><td>0</td><td>H:×10 speed, L:Others</td></tr>
<tr><td>14</td><td>ERIH</td><td>I</td><td>Capstan servo flag(H:Servo unlocked)</td></tr>
<tr><td>15</td><td>FLGC</td><td>I</td><td>Drum servo flag(L:Servo unlocked)</td></tr>
<tr><td>16</td><td>MUTE</td><td>0</td><td>DAT mute(H:ON)</td></tr>
<tr><td>17</td><td>SBSY</td><td>I</td><td>Communication start request between CXD2600Q and mechanism controller(H→L:Start)</td></tr>
<tr><td>18</td><td>DISPSEL</td><td>I</td><td>Communication selection between mechanism controller and main microcomputer
L:Main microcomputer→mechanism controller,
H:Mechanism controller→main microcomputer</td></tr>
<tr><td>19</td><td>DATON</td><td>I</td><td>Mechanism controller WAKE-UP/SLEEP selection(H:SLEEP mode)</td></tr>
<tr><td>20～24</td><td>NC</td><td>—</td><td>————————</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>25</td><td>CNVSS</td><td></td><td>Mechanism controller operation mode control(Fixed to L)</td></tr>
<tr><td>26</td><td>RESET</td><td>I</td><td>RESET(L:Active)</td></tr>
<tr><td>27</td><td>NC</td><td>—</td><td>————————</td></tr>
<tr><td>28</td><td>XOUT</td><td>O</td><td>System clock output</td></tr>
<tr><td>29</td><td>XIN</td><td>I</td><td>System clock input</td></tr>
<tr><td>30~31</td><td>NC</td><td>—</td><td>————————</td></tr>
<tr><td>32</td><td>VSS</td><td></td><td>GND</td></tr>
<tr><td>33</td><td>DEWCHK</td><td>O</td><td>H:DEW in TEST mode</td></tr>
<tr><td>34</td><td>COLDCHK</td><td>O</td><td>H:COLD in TEST mode</td></tr>
<tr><td>35</td><td>NC</td><td>—</td><td>————————</td></tr>
<tr><td>36</td><td>TLED</td><td>O</td><td>End sensor LED output</td></tr>
<tr><td>37</td><td>DSPSW</td><td>O</td><td>CXD2600Q power control(H:ON)</td></tr>
<tr><td>38~41</td><td>NC</td><td>—</td><td>————————</td></tr>
<tr><td>42</td><td>LM2</td><td>O</td><td rowspan="2">Loading motor control
<table><tr><th></th><th>LM1</th><th>LM2</th></tr><tr><td>Stop</td><td>0</td><td>0</td></tr><tr><td>Forward</td><td>1</td><td>0</td></tr><tr><td>Reverse</td><td>0</td><td>1</td></tr><tr><td>Brake</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>43</td><td>LM1</td><td>O</td></tr>
<tr><td>44</td><td>CSW2</td><td>I</td><td>Cassette compartment SW 1(detects cassette down)
(L:Cassette down)</td></tr>
<tr><td>45</td><td>CSW1</td><td>I</td><td>Cassette compartment SW 2(detects eject/cassette in)
(L:EJECT)</td></tr>
<tr><td>46</td><td>MSW1</td><td>I/O</td><td>Rotary encoder 1(COMMON 1)</td></tr>
<tr><td>47</td><td>MSW2</td><td>I</td><td>Rotary encoder 2</td></tr>
<tr><td>48</td><td>MSW3</td><td>I</td><td>Rotary encoder 3</td></tr>
<tr><td>49</td><td>MSW4</td><td>I/O</td><td>Rotary encoder 4(COMMON 2)</td></tr>
<tr><td>50~53</td><td>NC</td><td>—</td><td>————————</td></tr>
</table>

Pin No.	Pin Name	I/O	Function
54	DDON	O	DC/DC converter control(H:ON)
55~56	NC	—	————————
57	$\overline{\text{TEST}}$	I	L:DEW, COLD check mode
58	T END	I	End sensor input on take-up side
59	S END	I	End sensor input on supply side
60, 61		—	(Not used)
62	VCCC	I	VCC check
63		—	(Not used)
64	COLD	I	Thermistor input "COLD"=2.1V or more
65	DEW	I	DEW sensor input "DEW"=0.56V or more
66	CBIAS	O	Capstan servo bias output(analog)
67	DBIAS	O	Drum servo bias output(analog)
68	DAVREF		CBIAS, DBIAS reference voltage
69	ADVREF		DEW, COLD reference voltage
70	AVSS		Analog GND
71	AVCC		Power supply
72	VCC		Power supply
73	VSS		GND
74	CLKO	O	Mechanism controller→Main microcomputer communication clock
75	CLKI	I	Main microcomputer→Mechanism controller communication clock
76	DATO	O	Mechanism controller→Main microcomputer communication data
77	DATI	I	Main microcomputer→Mechanism controller communication data
78	RBIAS	O	Capstan bias(PWM)when capstan servo in CXD2600Q is not used
79, 80	NC	—	————————

4-4. PLAYBACK EQUALIZER AMPLIFIER (CXA1354Q) PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function
1	HA A Vcc	—	Power Supply for Ach Head Amp and 2nd Amp
2	MP HIGH2	—	For connection of resistor or current source to determine the high freq. range peak of PCM EQ (for metal-powder tape)
3	MP HIGH1	—	For connection of resistor or current source to determine the high freq. range response of PCM EQ (for MP)
4	MP PHASE	—	For connection of resistor of current source to determine the phase response of PCM EQ (for MP)
5	MP LOW	—	For connection of resistor or current source to determine the low freq. range response of PCM EQ (for MP)
6	PB GND	—	GND for other than Head Amp, 2nd AMP and limiter
7	EQ OUT	O	PCM EQ output
8	LIM IN	I	Limiter input
9	SWP OUT	O	Switching pulse output
10	LIM GND	—	GND for limiter
11	RFDT OUT	O	Limiter output
12	LIM Vcc	—	Limiter power supply
13	INT TC	—	For mounting integrating capacitor
14	PLCK IN	I	Integrator signal input
15	VREG OUT	—	Ragulator output with decoupling capacitor
16	TAPE SW	—	For selecting characteristics of 2 EQ response (for MP and Ba-Fe). EQ characteristic is obtained by resistor connected to pins ② and ⑤ at Lo and by pins ⑰ and ⑳ at Hi.
17	BF HIGH2	—	For connection of resistor or current source to determine the high freq. range peak of PCM EQ (for Ba-Fe)
18	BF HIGH1	—	For connection of resistor or current source to determine the high freq. range response of PCM EQ (for Ba-Fe)
19	BF PHASE	—	For connection of resistor or current source to determine the phase response of PCM EQ (for Ba-Fe)

Pin No.	Pin Name	I/O	Function
20	BF LOW	—	For connection of resistor or current source to determine the low freq. range response (for Ba-Fe)
21	PV Vcc	—	Power supply for other than Head Amp, 2nd Amp and limiter
22	EQ IN	I	EQ input
23	SW OUT	O	Switcher Amp output
24	HA B Vcc	—	Power supply for Bch Head Amp and 2nd Amp
25	HA B OUT	O	Output for Bch Head Amp
26	HA B GND	—	GND for Bch Head Amp and 2nd Amp
27	HA B PC	—	For connecting emitter pass capacitor of emitter-earthed Tr on the first stage of Bch Head Amp
28	HA B IN	I	Input for Bch Head Amp
29	HA A IN	I	Input for Ach Head Amp
30	HA A PC	—	For connecting emitter pass capacitor of emitter-earthed Tr on the first stage of Ach Head Amp
31	HA A GND	—	GND for Ach Head Amp and 2nd Amp
32	HA A OUT	O	Output for Ach Head Amp

4-5. IC102 PLAYBACK DAT SIGNAL PROCESSOR IC (CXD2600Q) PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function
1	F256	O	256×fs output
2	F128	O	128×fs output
3	TX	O	Digital out
4	BCK	O	BCK output (64×fs)
5	XBCK	O	BCK inverted output (64×fs)
6	DADT	O	DA data output
7	WCK	O	WCK output
8	LRCK1	O	LRCK output (1)
9	LRCK2	O	LRCK output (2)
10	INTF	O	DA data interpolate selection signal output(H:Interpolate)
11	MUTE	I	DA data mute signal input(H:Mute)
12	Vss	—	GND
13	LSBF	I	DA data LSB/MSB first select signal (H : LSB first, L : MSB first)
14	CSPW	O	Capstan speed control PWM output
15	CBPW	O	Capstan bias control PWM output
16	CPPW	O	Capstan phase control PWM output
17	DSPW	I/O	Drum speed control PWM output (when MTCL ㉑= H) (Note 1)
18	DBPW	I/O	Drum bias control PWM output (when MTCL ㉑= H) (Note 1)
19	FLGC	O	CRC monitor output
20	ERIH	O	Erasure condition monitor output (H : Erasure inhibit)
21	MTCL	I	System motor select signal input (H : Motor 2, L : Motor 1)
22	SPD1	I	Capstan speed select signal input (1)
23	SPD2	I	Capstan speed select signal input (2)
24	FDRV	I	Tape direction select signal input(H:REV, L:FWD)

Pin No.	Pin Name	I/O	Function
25	CMTR	I	Capstan motor ON/OFF signal input(H:ON, L:OFF)
26	DMTR	I	Drum motor ON/OFF signal input(H:ON, L:OFF)
27	FGSG	I	Capstan FG input
28	FGL1	I	Capstan FG frequency division ratio setting data input (1)
29	FGL2	I	Capstan FG frequency division ratio setting data input (2)
30	SBDT	I/O	Microcomputer interface data input/output
31	EXCK	I	Microcomputer interface CK input
32	$\overline{\text{SBEN}}$	I	Microcomputer interface enable signal input (L:Enable)
33	V_{DD}	—	Power supply (+5V)
34	SBSY	O	Microcomputer interface sync. signal output
35	SYSC	O	ECC start timing signal output(L:Ach, H:Bch)
36	SYNM	O	C1 syndrome monitor output
37	CHER	I	Error correction strategy setting input
38	XRST	I	RESET signal input(L:RESET)
39	DRSW	I	Drum FWD/REV recognition signal input(H: FWD, L: REV)
40	EMP	O	Emphasis ON/OFF output(H:Emphasis ON)
41	TRPH	O	Track pitch recognition signal output
42	STID	O	Start ID monitor output
43	SKID	O	Skip ID monitor output
44	FMID	O	Format ID monitor output
45	LPSP	O	Playback mode recognition signal output(L:SP, H:LP)
46	PLCK	O	PLL CK output
47	SWP	I	Switching pulse input(L:Ach, H:Bch)
48	RFDT	I	RF input
49	TST1	I	Test input (1)(Fixed to L)
50	XTI	I	Crystal input (49.152MHz)
51	XTO	O	Crystal output

Pin No.	Pin Name	I/O	Function
52	Vss	—	GND
53	XT2I	I	Crystal input (22.5792MHz)
54	XT2O	O	Crystal output
55	TST2	I	Test input (2)(Fixed to L)
56	MTG1	O	Error monitor data read signal output (1)
57	MTG2	O	Error monitor data read signal output (2)
58	XOE	O	External RAM XOE output
59	XWE	O	External RAM XWE output
60	XRAS	O	External RAM XRAS output
61	XCAS	O	External RAM XCAS output
62～70	A8～A0	O	Address bus
71	D0	I/O	Data bus 0
72	D1	I/O	Data bus 1
73	V_{DD}	—	Power supply (+5V)
74	D2	I/O	Data bus 2
75	D3	I/O	Data bus 3
76	ATT	I	Attenuator input
77	ERMN	I/O	CRC condition monitor output(when FSSL⑲=L) (Note 2)
78	ATMT	I/O	Auto mute monitor output(when FSSL⑲=L) (Note 2)
79	FSSL	I	Fs information setting input
80	MCLK	O	Internal system clock output

(Note 1) The DSPW and DBPW change over the PLL lock range when MTCL= "L"and DMTR= "H". They can be set as follows:

DSPW⑰	DBPW⑱	Lock range
0	0	±16%
0	1	−34～+ 4%
1	0	− 5～+39%
1	1	±22%

When DMTR = "L", "H" are output from both pins.

(Note 2) The ERMN and ATMT become input pins for the FS information when FSSL = "H". They are set as follows:

ERMN⑰	ATMT⑱	FS information
0	0	48kHz
1	0	44.1kHz
0	1	32kHz
1	1	———

5. DIGITAL SIGNAL PROCESSING SECTION

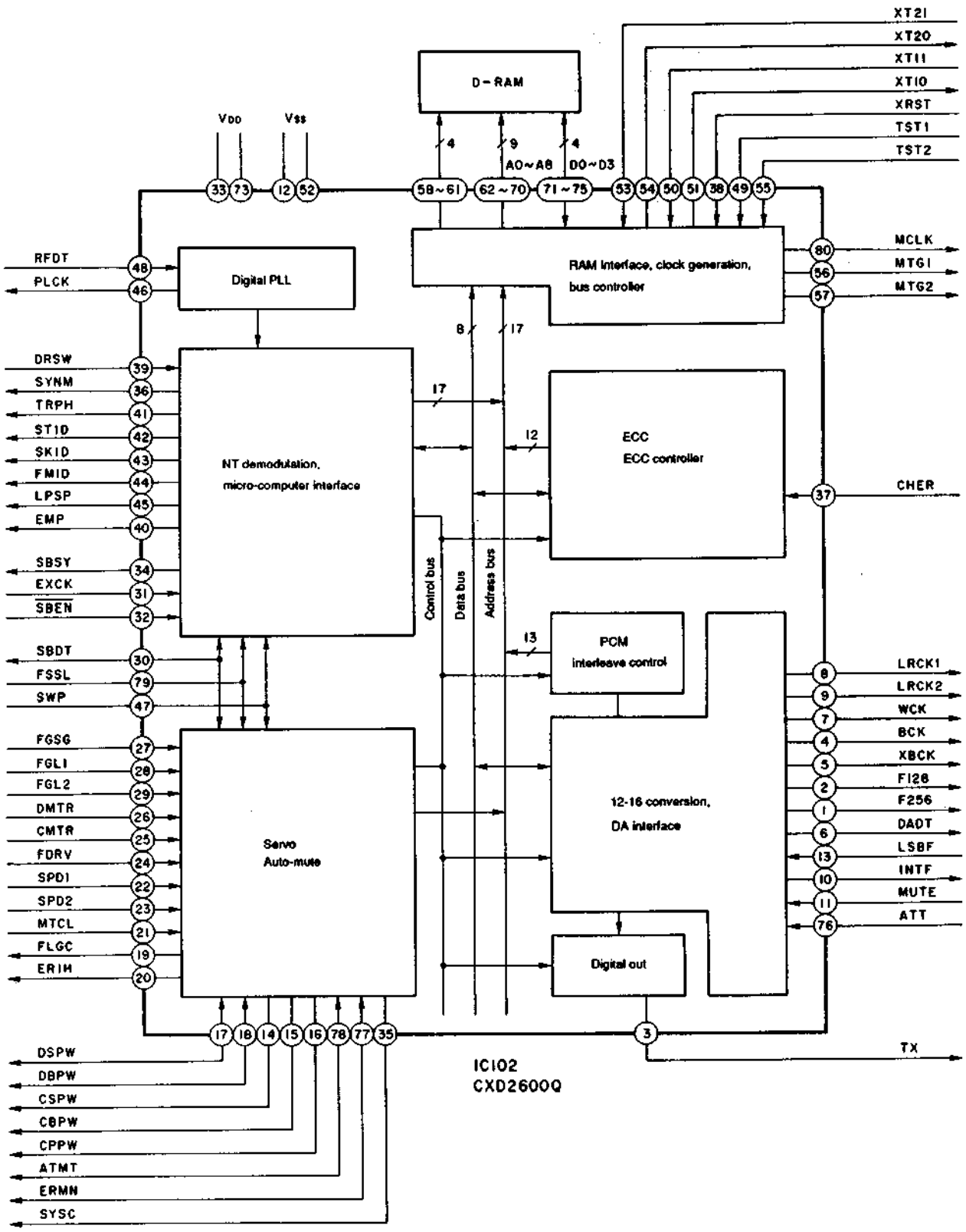


Fig. 5-1

5-1. DIGITAL PLL

For playback of RF signal with jitter read from tape, a clock signal (PLCK) synchronized with the jitter is generated by digital PLL. Although CXD2600Q is an IC which can be used for 1-motor mechanism, this unit uses a 2-motor mechanism so the MTCL (pin (21)) is pulled up to "H" and the PLL lock range is set ±15%.

5-2. DEMODULATION

CXD2600Q is not provided with ATF servo, yet NT (non-tracking) playback is possible. Therefore, special methods are used to process the data.

This unit features multiplex readout data processing to prevent the deterioration of error rate due to non-tracking system. Data are processed for each unit of 2 blocks having even and odd number block addresses.

5-2-1. Sync detection and block address

Block sync is detected by window check using previous sync and by the result of parity check. The output from the FLGC (pin (19)) is "H" when the number of parity check OK with odd number of block address in Ach or Bch is 8 or more. The output from ERMN (pin (77)) becomes "H" when parity N.G. are continuously present on 8 or more frames.

5-2-2. Frame address

In the NT system, data are sometimes read over several tracks and different frame address is detected. In this case, the playback frame address is the frame address near the center (block address of $30-$3F) on the track.

5-2-3. Main data

Main data is handled as a unit of C1 code series. In this case, no-error data picked up from the series which has been read several times, are written in the external buffer RAM. If errors are present on all the data, the data which is read last is picked up. The result of C1 check (error detection only) can be monitored from SYNM (pin (36)). Error is indicated at "H".

5-2-4. Pack data

When a pack with ITEM designated by micro-computer is read, ITEM data is sent to the micro-computer when no error is checked by C1 parity. When an error is checked, the transfer data are all "0".

5-2-5. Main ID and sub ID

Main ID and sub ID are each picked up by 4-fold and 3-fold coincidence respectively, and the contents are output to SBDT (pin (30)), digital out TX (pin (3)), and each ID data output terminal.

(ID data output terminals)

- EMP pin (40) ..... Emphasis data "H" : Emphasis ON
- TRPH pin (41) .... Track pitch data "L" : Normal track, "H" : Wide track
- STID pin (42) ..... Start ID "H" : Active
- SKID pin (43) ..... Skip ID "H" : Active
- FMID pin (44) ..... Format ID "00" : "L" output

These ID data are output from the digital out. Data of start ID and skip ID is output only in x1 playback mode. This limitation is released when SKPL of SBDT is set to "1" on the micro-computer interface. In this way, the data is output in any playback mode.

The data of Fs, channel number and quantitizing bit number in the main ID are used for setting the internal status. They are subjected to double coincidence to improve the reliability. Fs data can be selected by external setting. In this case, the FSSL (pin (79)) is set to "1", while the ERMN (pin (77)) and ATMT (pin (78)) are used as setting input terminals as shown in Table 5-1.

Table 5-1

	ATMT	ERMN
48 kHz	0	0
44.1 kHz	0	1
32 kHz	1	0
—	1	1

5-3. RAM INTERFACE

This unit uses a 1M bit (512 x 512 word x 4 bit) DRAM as an external buffer RAM. Refresh is automatically effected in a cycle within 7 msec. The RAM block diagram and the timing of each signal are as follows.

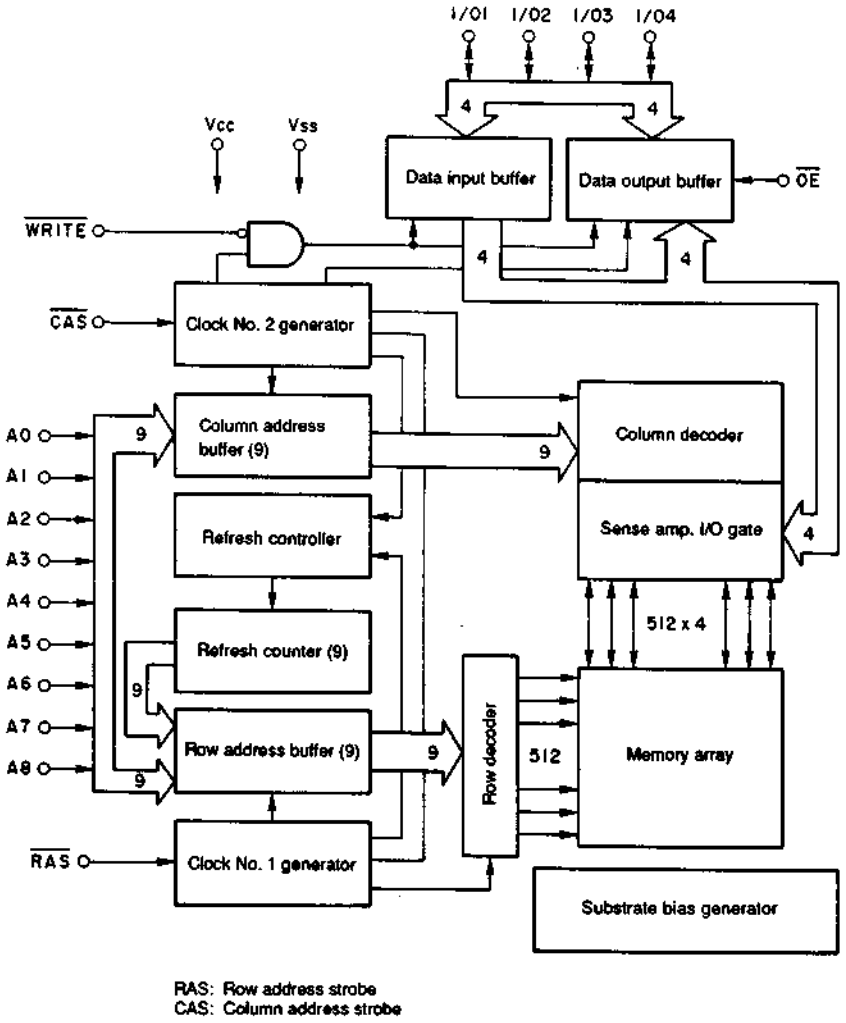


Fig. 5-2 Block diagram

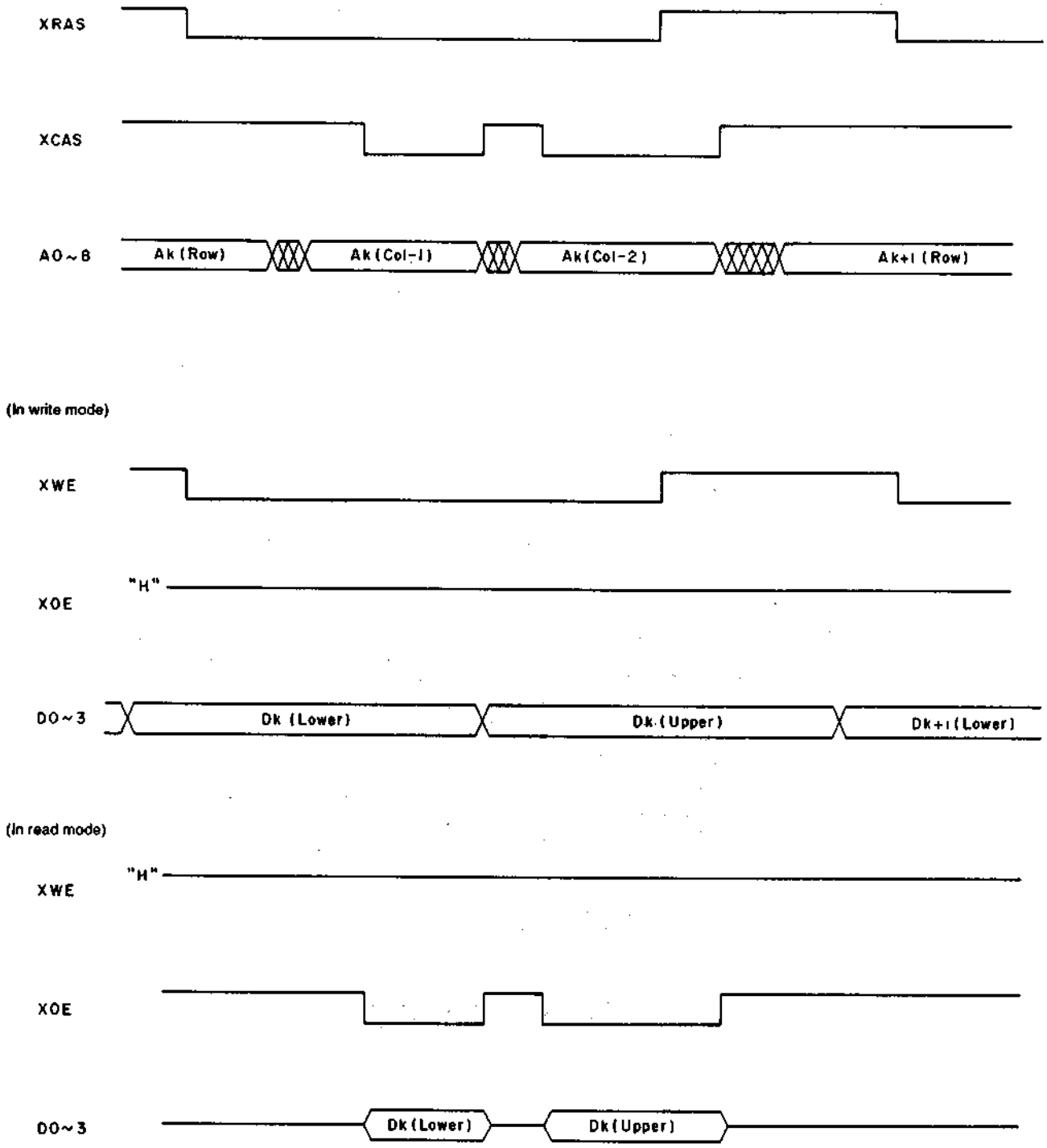


Fig. 5-3 DRAM interface timing

5-4. MICRO-COMPUTER INTERFACE

CXD2600Q and micro-computer are interfaced by the following 4 signals.

Table 5-2

Pin No.	Symbol	I/O viewed from CXD2600Q	Function
30	SBDT	I/O	Bidirectional serial data transfer line. Data from CXD2600Q is read at the rising edge of EXCK, and output data is changed at the falling edge of EXCK.
31	EXCK	I	Reference clock for data reading.
32	$\overline{\text{SBEN}}$	I	Input terminal for micro-computer interface enable signal. "L": Enable
34	SBSY	O	Reference timing signal in a cycle of about 15msec.

The 1 word data is composed of 4 bit, and 40 words are transferred at a time. The relation between the timing and each word is as shown below.

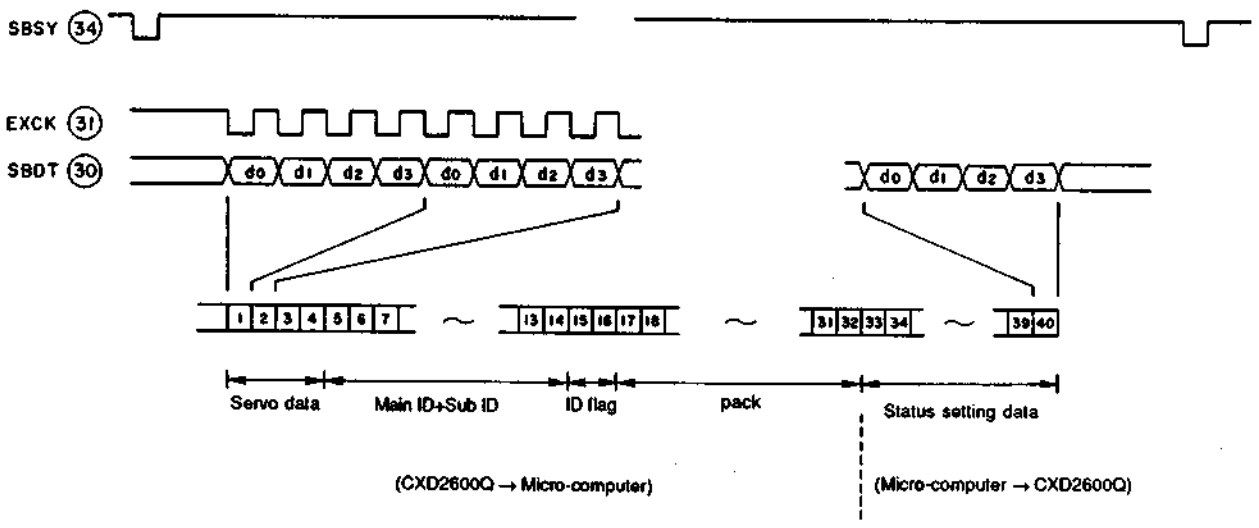


Fig. 5-4

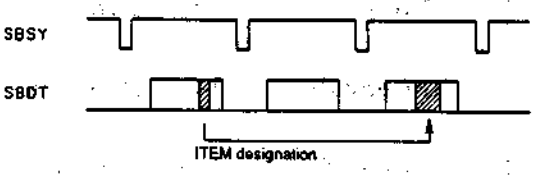
Table 5-3

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
d3	PH3	REF3	PB3		ID11	ID31	ID51	ID71	CTL ID	Data ID	PNO OD (3)	PNO ID (2)			F67		P3	P7	P3	P7
d2	2	2	2		10	30	50	70							F45		2	6	2	6
d1	1	1	1	PH flag	01	21	41	61		Pack ID			PNO ID (1)		F23	FPNO	1	5	1	5
d0	0	0	0		00	20	40	60							F01	PCTL	0	4	0	4
																	PC1		PC2	

	29	30	31	32	33	34	35	36	37	38	39	40
	P9	P7	P3	P7	B3	B7		SRT		D3	D7	D11
	2	6	2	6	2	6		ST1		2	6	10
	1	5	1	5	CTL	5	R1	ST0		1	5	9
	0	4	0	4		4	R0	SKPL		0	4	8
		PC7		PC8								

Table 5-4

Word No.	Contents	Description	Remark
1	PH data	Difference between reference frame address in CXD2600Q and playback frame address	Servo data (micro-computer input)
2	REF data	Reference frame address in CXD2600Q	
3	PB data	Playback frame address	
4	PH flag	PH generation method data	
5-8	Main ID	Format ID (ID0) and ID1-7 are output by 4-fold coincidence	ID data (micro-computer input)
9-13	Sub ID	Control ID, data ID, pack ID and program number ID are output by 3-fold coincidence. Data ID is output as a result of 4-bit OR.	
15, 16	ID flag	Multiple coincidence data of the above 6 ID data. Coincidence is indicated by "0". Non-coincidence is indicated by "1" and previous hold is applied. F01 ..... Flag for ID00, 01, 10 and 11 F23 ..... Flag for ID20, 21, 30 and 31 F45 ..... Flag for ID40, 41, 50 and 51 F67 ..... Flag for ID60, 61, 70 and 71 FCTL ..... Flag for Control ID, data ID and pack ID FPNO ..... Flag for Program number ID	

<table>
<tr><th>Word No.</th><th>Contents</th><th>Description</th><th>Remark</th></tr>
<tr><td>17-32</td><td>PACK data</td><td>Pack data with designated ITEM. When ITEM is not detected or when error is present in C1 series including the pack, the pack data is output as "All 0".</td><td>PACK data (micro-computer input)</td></tr>
<tr><td>33, 34</td><td>ITEM designation</td><td>When CTL bit is "0", the upper 4 bits of PC1 is designated (B7-B4). When it is "1" the upper 6 bits is designated (B7-B2). The designated data is output after 2 cycles of SBSY.
 
</td><td>ITEM designation PACK data (micro-computer output)</td></tr>
<tr><td>35</td><td>Area designation</td><td>Read area designation for sub ID and pack data.
<table>
<tr><th>R1</th><th>R0</th><th>Area designation</th></tr>
<tr><td>0</td><td>0</td><td>Read from sub-data area 1 and 2</td></tr>
<tr><td>0</td><td>1</td><td>Read from sub-data area 2</td></tr>
<tr><td>1</td><td>0</td><td>Read from sub-data area 1</td></tr>
<tr><td>1</td><td>1</td><td>Read from B-CH sub-data area 2</td></tr>
</table></td><td>Reed area designation for Sub ID and pack data. (micro-computer output)</td></tr>
<tr><td>36</td><td>SKPL</td><td>Setting of skip play mode. "1": ON</td><td rowspan="4">Setting data (micro-computer output)</td></tr>
<tr><td>36</td><td>ST0, 1</td><td>Setting of drum sweep time</td></tr>
<tr><td>36</td><td>SRT</td><td>Setting of search mode. "1": ON</td></tr>
<tr><td>38-40</td><td>D0-D11</td><td>Setting of capstan FG preset data</td></tr>
</table>

5-5. ERROR CORRECTION

CXD2600Q provides more powerful error correction ability with new strategy.

During normal playback, data are processed in the order of C1→C2→C1→C2. In the first C1 processing, error is detected, and then it is corrected in the next C2 and succeeding stages. The error correction ability in each stage is as shown below.

Table 5-5

C1 (first)	Error detection
C2 (first)	5-fold correction
C1 (second)	3-fold correction
C2 (second)	5-fold correction

When interleave error is present in the C1 series during RF demodulation, C2 is set for double correction (erasure correction inhibit). During double speed playback, only C1 error correction is set.

The CHER (pin ㊲) is used for input to change the strategy from the outside. C1→2 performs processing once at "H". The ERIH (pin ⑳) is used for "H" monitoring output in the erasure correction inhibit mode.

5-6 DA INTERFACE

DA data is output in series in the form of 2's compliment from the DADT (pin ⑥); bit clock, word clock and LR clock are output from BCK (pin ④), WCK (pin ⑦) and LRCK1 (pin ⑧), respectively.

The XBCK (pin ⑤) outputs inverted BCK signal and the LRCK2 (pin ⑨) outputs LR clock signal based on I^2S bus. The LSBF (pin ⑬) is input terminal for selecting LSB first or MSB first of DA data. LSB first is selected at "1".

The output from INTF (pin ⑩) indicates that DA data is interpolated (mean value interpolation or previous-hold) at "H".

[Attenuation]

When the ATT (pin ⑯) input is "1" or during double speed playback mode (LPSP (pin ㊾) output is "H"), the DA data is attenuated to -12dB.

[Muting]

DA data muting is classified into forced muting (mute at "1") by MUTE (pin ⑪) input and automatic muting by the internal circuit. The conditions of automatic muting is as follows.

1) For 16 frames after any of sampling frequency, channel number and quantization number is changed.
2) For 16 frames after there is a discontinuity of more than ±4 frames in playback frame address.
3) Capstan motor OFF (CMTR pin ㉕ = "0") or drum motor OFF (DMTR pin ㉖ = "0": 2-motor mechanism only)
4) x4 or x8 speed (SPD2 pin ㉓ = "1")
5) Search mode (micro-computer command SRT = "1")
6) FLGC (pin ⑲) signal "L" for 4 frames or more continuosly. Released 16 frames after FLGC (pin ⑲) signal becomes "H".

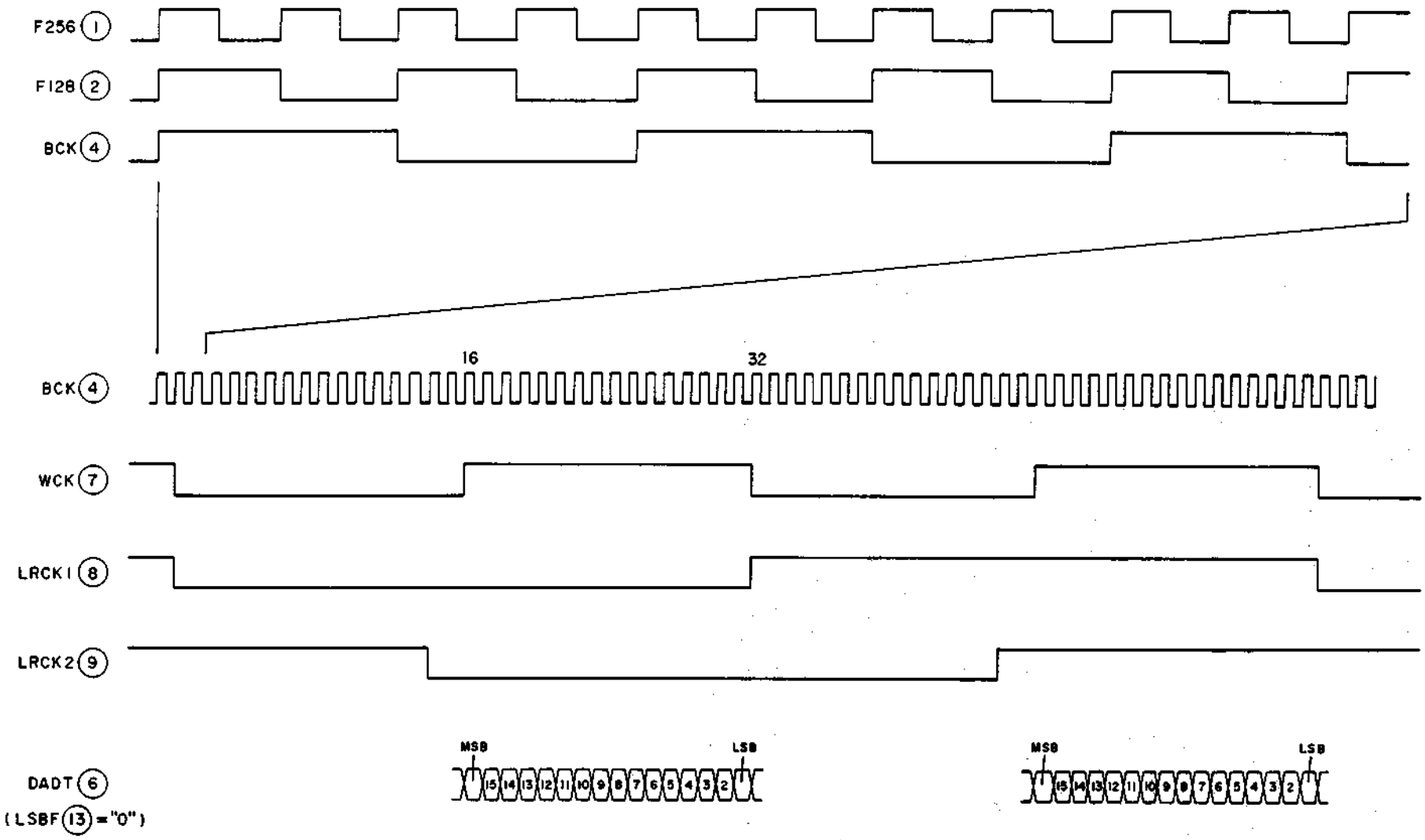


Fig. 5-5 DA data output timing

6. SERVO CIRCUIT

CXD2600Q is available not only for 1-motor mechanism with capstan servo but also for 2-motor mechanism with capstan servo and drum servo.

In the 1-motor mechanism, the drum speed control is lost so it is possible to select the lock range of the internal digital PLL.

Motor mechanism is set by the MTCL (pin (21)); 2-motor mechanism is selected at "H", while 1-motor mechanism is selected at "L". When using the 1-motor mechanism, the DSPW (pin (17)) and DBPW (pin (18)) are used as input terminals for selecting the digital PLL lock range.

6-1. DRUM SERVO

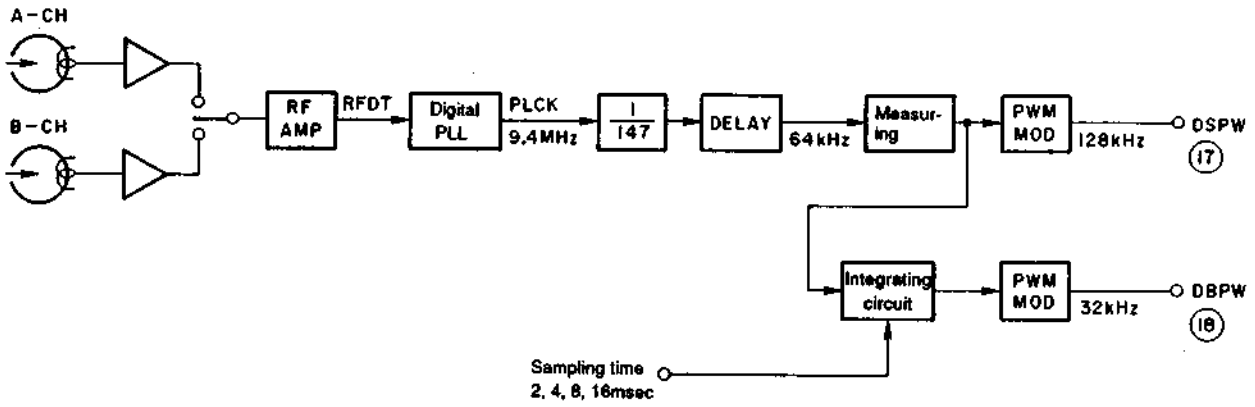


Fig. 6-1

CXD2600Q has no recording mode, so a precision drum servo is not required. Therefore, FG for motor and drum is eliminated to save the cost, but PLCK generated from the PLL circuit is used instead of FG. As lock as the PLL circuit is locked, PLCK is proportional to the relative speed obtained by the head and tape.

The drum servo is composed of 3 main sections; a speed servo section, a bias servo section and a search mode control section to obtain PLL lock.

6-1-1. Speed servo section

When the relative speed obtained by the head and tape is within the specified speed, the PLCK is 9.408 MHz which is divided by 147 and its one cycle is measured by the counter.

The change of the one cycle is converted into PWM and is output as DSPW, a relative speed error obtained by the head and tape. The carrier frequency is 128 kHz with a dynamic range of +33.3% to -20%.

6-1-2. Bias servo section

With the speed servo section alone, an offset may be caused by the motor characteristic variation or temperature characteristic. So the speed error is sampled at specified cycle to output the integrated value as DPPW. The carrier frequency is 32 kHz, while the sampling time is determined by combination of SRT, ST1 and ST0 bits of the interface command from the micro-computer.

Table 6-1. Drum servo setting by micro-computer interface

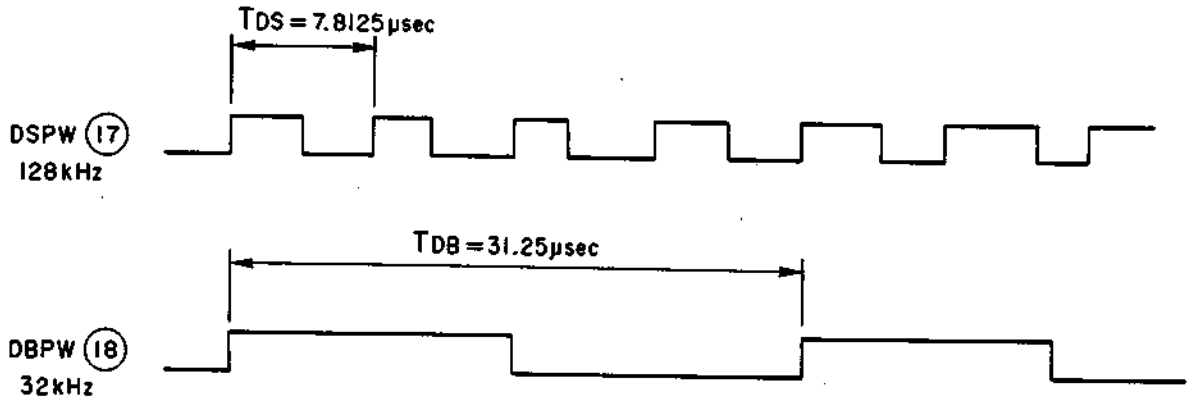
SBDT setting (micro-computer command)			Setting data			
SRT	ST1	ST0	Sweep range	Sweep cycle	Sampling cycle	
0	0	0	±50%	0.512 (sec)	2 (msec)	
	0	1		1.024 (sec)	4 (msec)	
	1	0		2.048 (sec)	8 (msec)	← Default value
	1	1		4.096 (sec)	16 (msec)	
1	0	0	±100%	0.512 (sec)	2 (msec)	
	0	1		1.024 (sec)	4 (msec)	
	1	0		2.048 (sec)	8 (msec)	
	1	1		4.096 (sec)	16 (msec)	

6-1-3. Search mode control section

As explained above, PLCK is used instead of FG so that it can be operated as FG only when PLL is locked. The FLGC (pin ⑲) is provided to check if the digital PLL is locked. When it is locked, "H" signal is obtained.

Also, as in the case of the disc servo of CD player, when the RF data cannot be read at the start up of drum rotation or due to external disturbance, the DBPW signal is swept within the range of –50% to +50%. The sweep cycle can be selected by the micro-computer as mentioned above. The sweep timing is shown in the following diagram.

(PLL lock)



(Search mode)

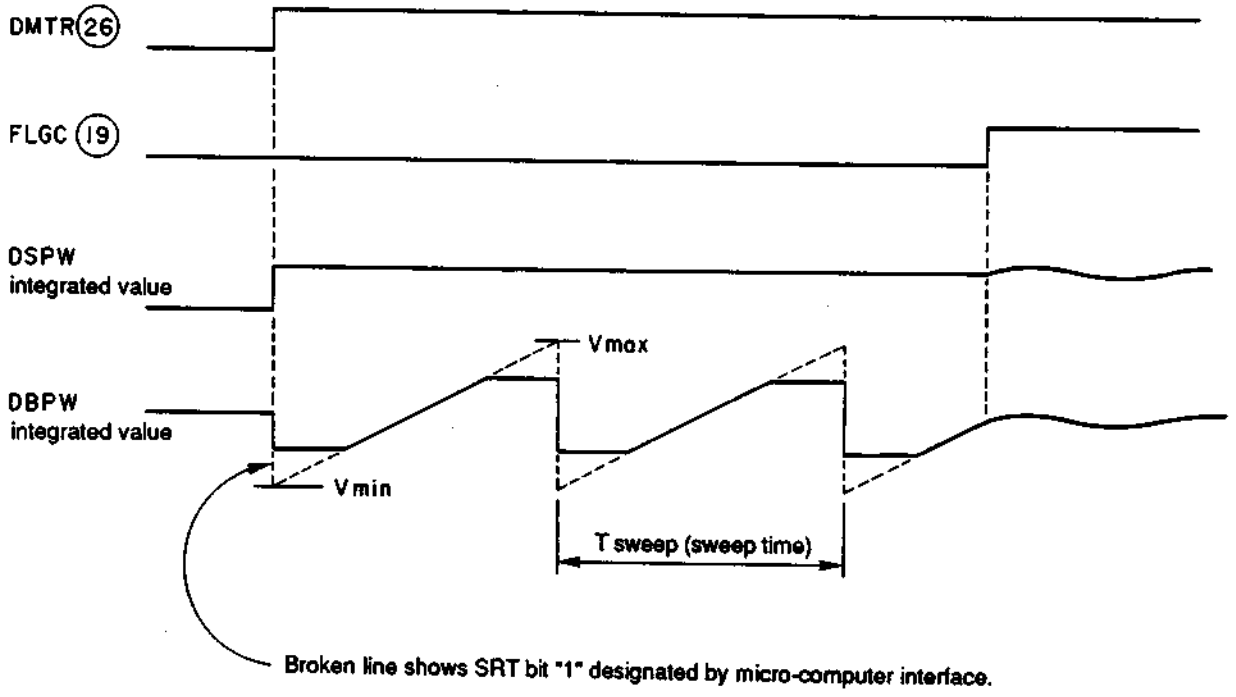


Fig. 6-2 Drum servo output waveform

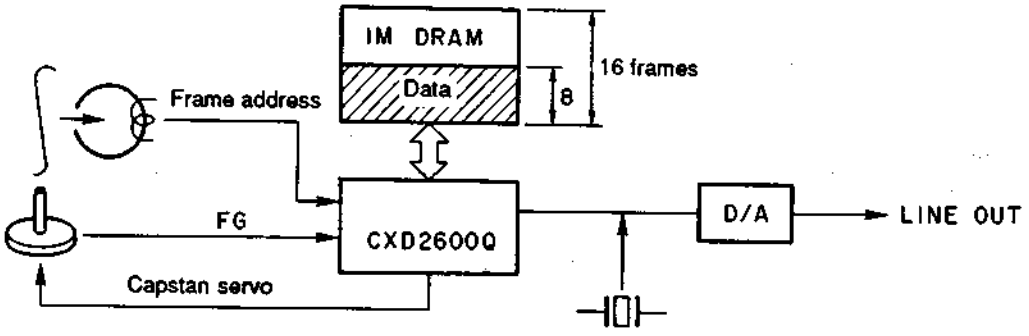


Fig. 6-3

In the 1st generation DAT, the capstan is controlled by using AFT signal recorded in tape. In CXD2600Q, NT system is used and hence a different control method is required. As shown in the diagram, the tape speed is controlled by checking the frame address recorded in an even number of blocks of the main data, in addition to FG, to obtain a certain quantity of data in the buffer RAM.

There are 3 signals to control the capstan; speed servo output CSPW (pin (14)), phase servo output CPPW (pin (16)) and phase bias servo output CBPW (pin (15)). The timing of these signals are shown in the following diagram.

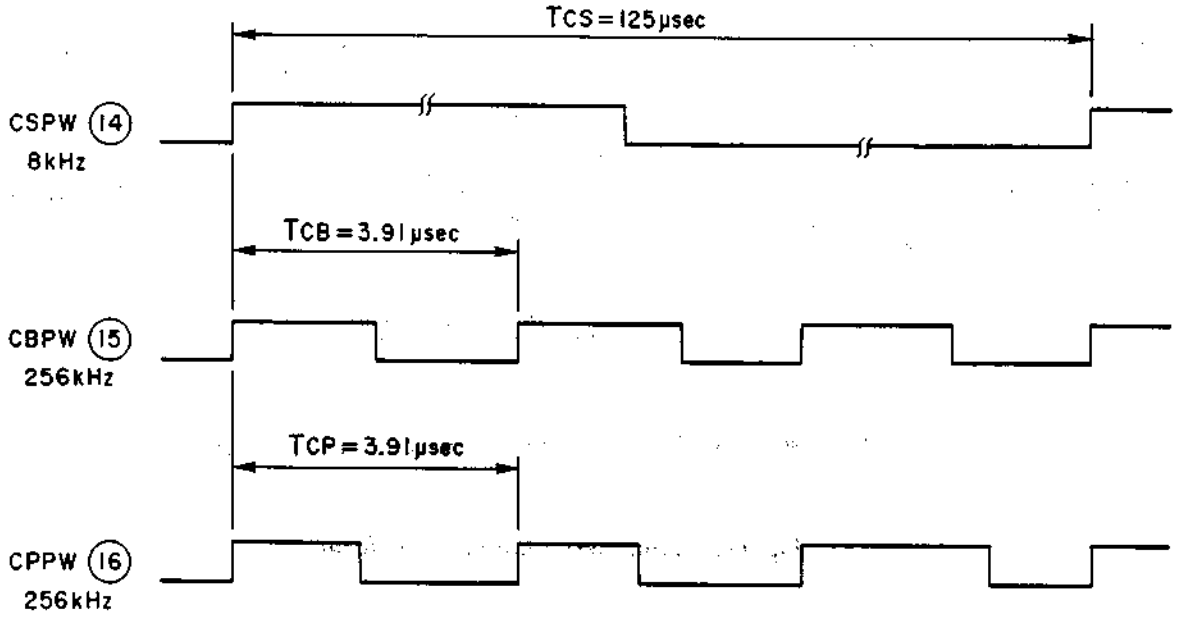


Fig. 6-4

6-2-1. Capstan speed servo section

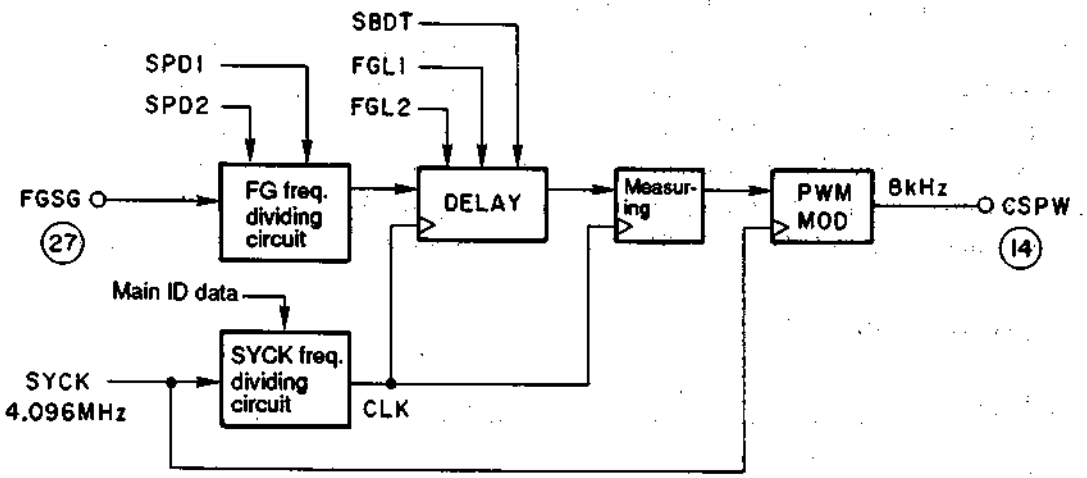


Fig. 6-5

Table 6-2 FG frequency setting by FGL2, 1

FGL2 (29)	FGL1 (28)	Reference FG frequency	Dynamic range
0	0	(Micro-computer setting)	—
0	1	400 Hz	–13% ~ +17%
1	0	600 Hz	–18% ~ +29%
1	1	800 Hz	–23% ~ +42%

Table 6-3 FG frequency division ratio setting

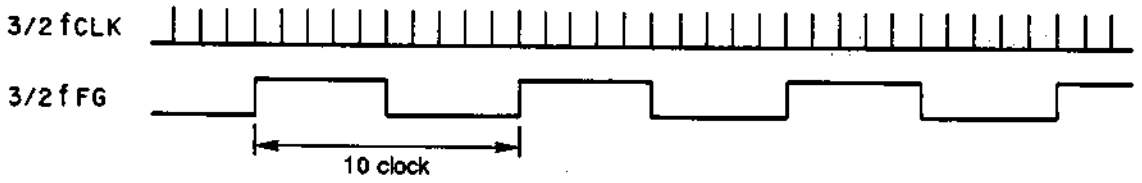
Speed	SPD2	SDP1	FG frequency division ratio
x8	1	1	1/8
x4	1	0	1/4
x2	0	1	1/2
x1	0	0	1/1

Speed control is effected by comparing the capstan FG frequency (input signal on FGSG pin (27)) with the internal reference FG frequency. The reference FG frequency can be set from the outside using FGL1 (pin (28)), FGL2 (pin (29)) or micro-computer interface (SBDT). In this unit, the speed control is effected by using the micro-computer interface. The control value can be set freely in 12 bits of D0-D11 in SBDT format.

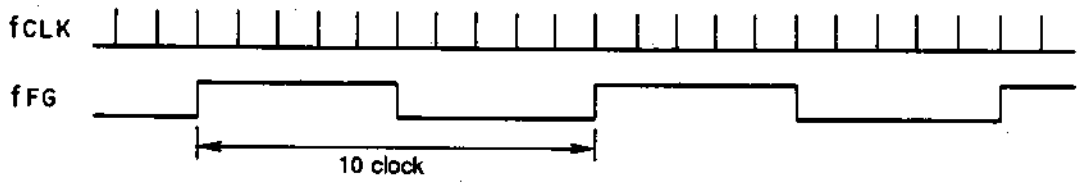
As shown in the above table, the FG frequency dividing circuit is controlled by SPD1 and SPD2. When the playback speed has been selected, it is set to FG x 1/2 for x2 playback or FG x 1/4 for x4 playback to obtain a constant dynamic range for measuring.

The frequency division ratio of SYCK frequency dividing circuit is selected according to the main ID data (CH number, track pitch, quantization bits, sampling frequency, etc.) in the main data. For example, a soft tape runs at x1.5 speed. Therefore, where the FG frequency of normal tape is expressed as (f_{FG}) and the clock frequency as (f_{CLK}), FG is set to (3/2 f_{FG}) and hence the dynamic range becomes constant by setting the clock frequency to (3/2 f_{CLK}). In the LP mode, FG is set to (1/2 f_{FG}) and clock to (1/2 f_{CLK}). The timing of it is shown in the following diagram.

[A] x1.5 playback (soft tape)



[B] x1.0 playback



[C] x1/2 playback (LP mode)

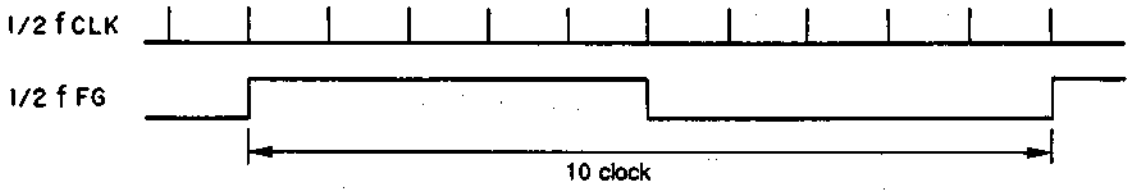


Fig. 6-6

6-2-2. Capstan phase servo section (track deviation control)

The buffer RAM of DAT using an ordinary ATF servo is a 128K bits DRAM capable of storing data for 2 frames. In the NT system, it uses DRAM with a capacity of 1M bits so it is able to store data 8 times 128K or data for 16 frames. The phase servo is used to control the phase so that the difference between the playback frame address and the reference frame address (frame address of DA output data) can always be set to 8 frames to obtain a constant amount of DRAM data. The diagram below shows the phase servo section and the phase bias servo section.

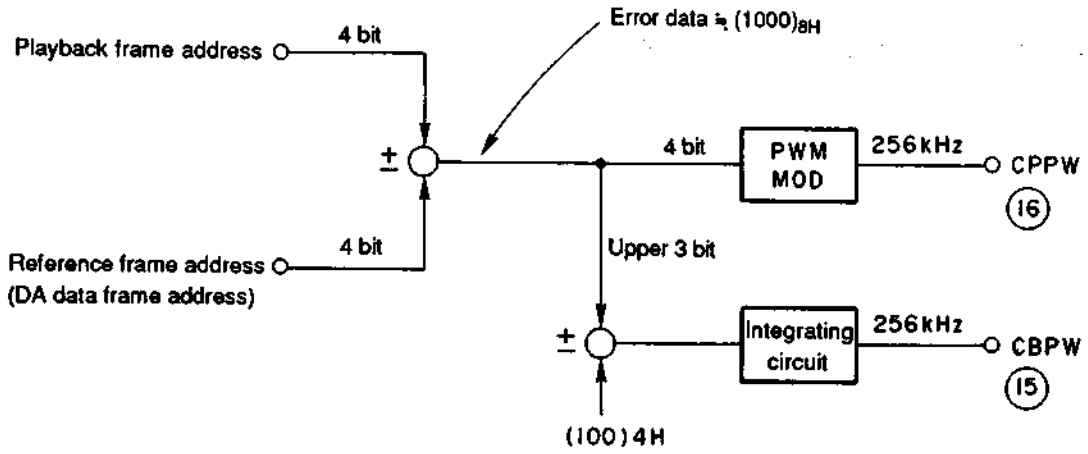


Fig. 6-7

6-2-3. Capstan phase bias servo section

Like the drum servo, the phase bias servo is used to cancel the offset caused by the motor or circuit characteristics variation. The upper 3 bits of the error data of phase servo is compared with 4H (100), and the error is integrated and output to the phase bias servo (see the above diagram). In the following condition, CBPW (pin (15)) is set to duty ratio 50% and then a constant voltage is applied to the motor.

1. FLGC (pin (19)) = "L" (many errors in RF signal from tape)
   In this case, CPPW (pin (16)) is also set to duty ratio 50% constant and then only the speed servo is operated.
2. Capstan speed servo is out of dynamic range.
3. SPD2 (pin (23)) = "H" (When tracking servo is not operated at x4 and x8 speed.)

7. MECHANISM

7-1. MAIN PARTS POSITIONS AND NAME

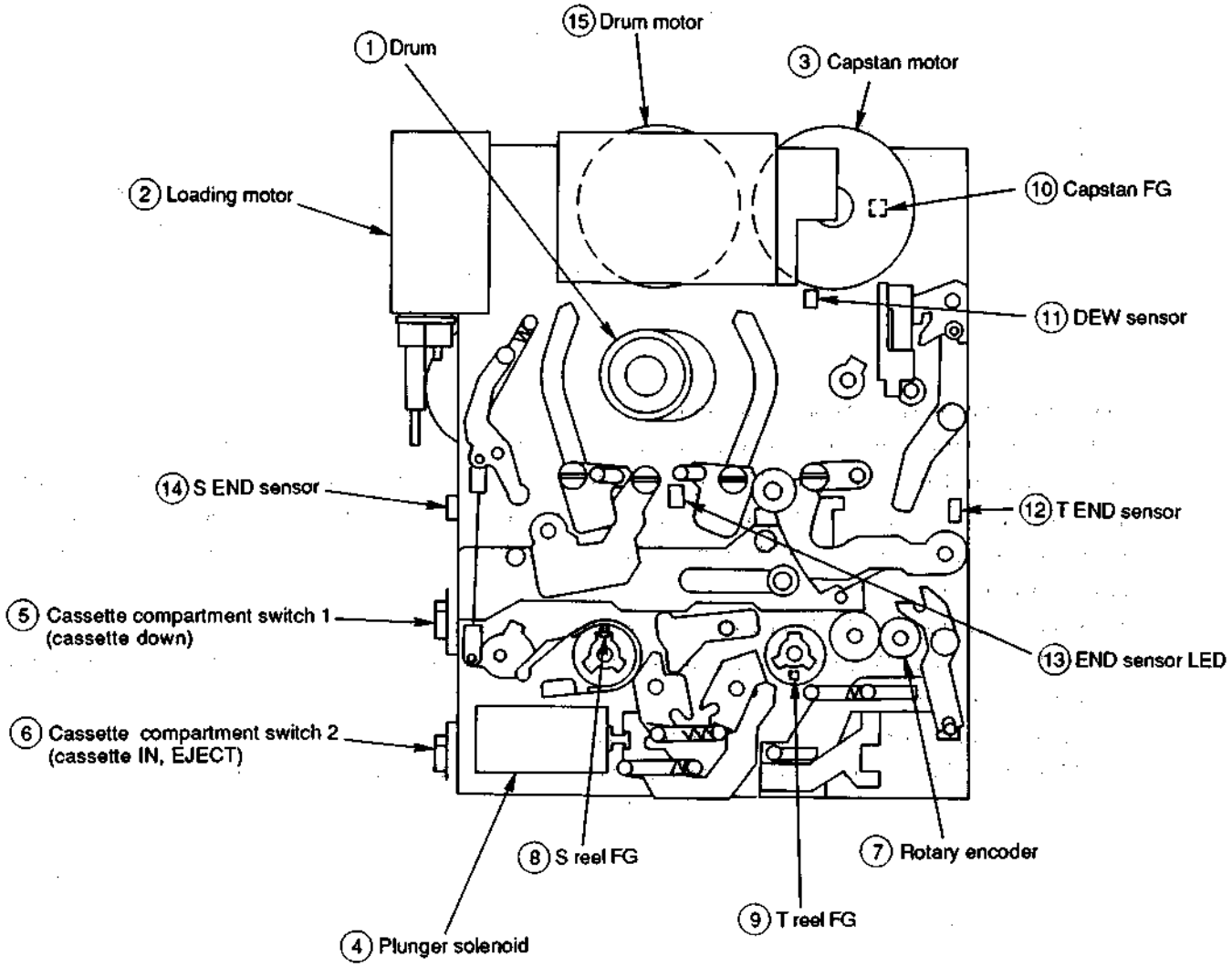


Fig. 7-1

7-2. OPERATION OF EACH PART

7-2-1. Operation of guide

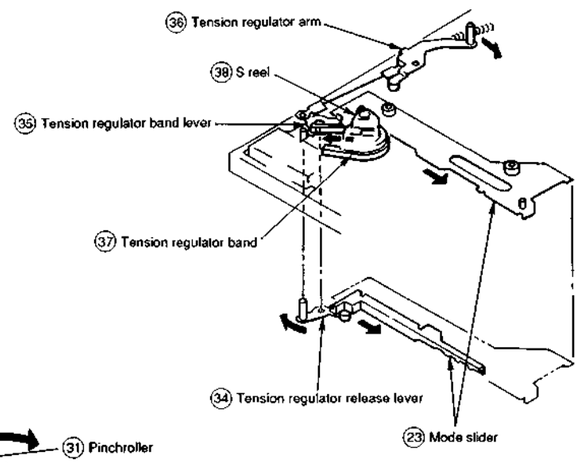
Loading motor (2) starts rotating.

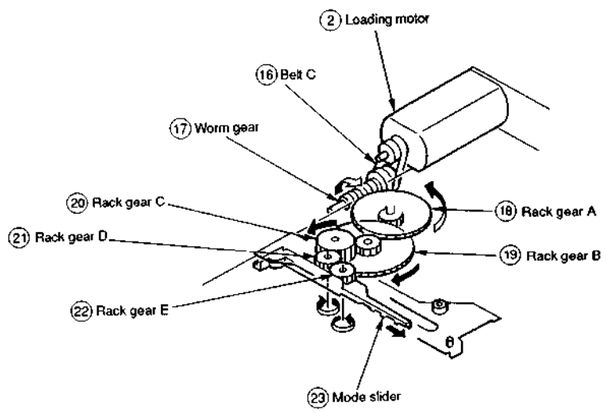
Rack gear E (22) starts rotating via belt C (16), worm gear (17), rack gear A (18), rack gear B (19), rack gear C (20) and rack gear D (21).

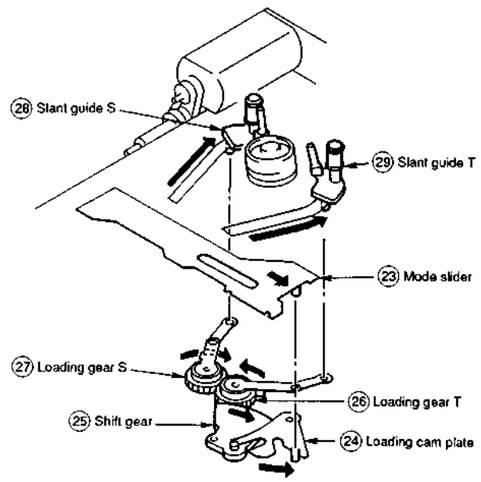
Mode slider (23) starts sliding.

- Shift gear (25) is operated via loading cam plate (24).
  - Loading gear T (26) starts rotating.
    - Loading gear S (27) starts rotating.
      - Slant guide S (28) operates for loading.
      - Slant guide T (29) operates for loading.
- Swing lever S (30) operates for loading in the direction of arrow mark.
- Pinchroller (31) operates for loading in the direction of arrow mark.
  - Swing lever T (32) operates for loading in the direction of arrow mark.
- Rotary encoder (7) starts rotating via mode switch gear (33). *1
- Tension regulator band (35) is operated via tension regulator release lever (34).
  - Tension regulator arm (36) is operated to apply tension to tape.
  - Tension regulator band (37) is pulled to brake S reel (38).
- S release lever (39) is operated (see 7-2-2).
- Speed reduction lever (40) is operated (see 7-2-3).
- Reel soft brake (47) is operated (see 7-2-4).
- Select lever (55) is operated (see 7-2-4).

*1: Mechanism operation is detected by rotary encoder (7) and controlled.







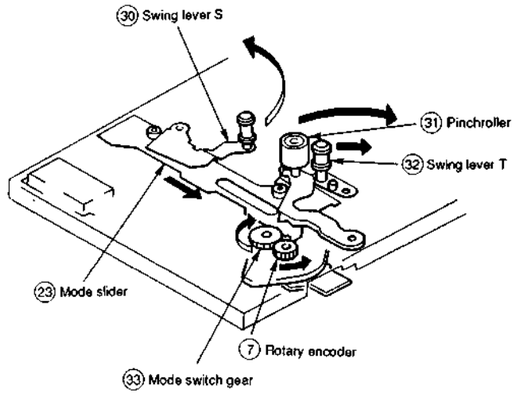
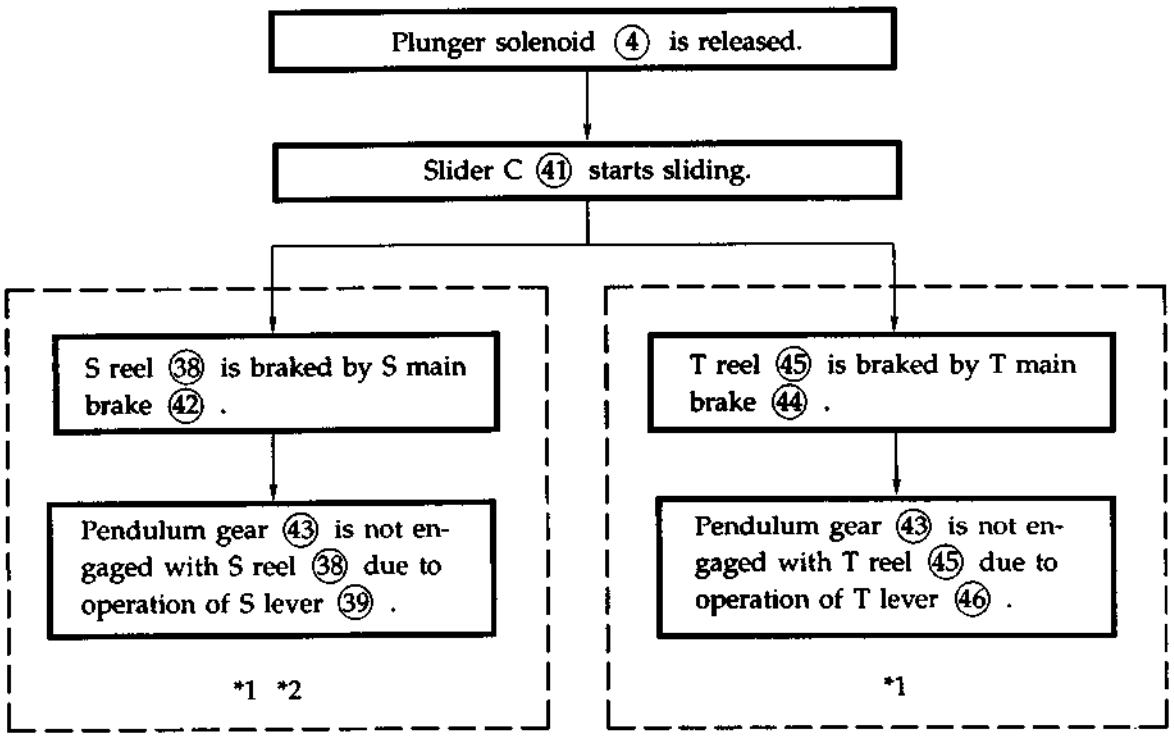


Fig. 7-2

7-2-2. Operation of main brake



*1: Reel is not rotated when it is braked by main brake.

*2: When mode slider (23) starts sliding, S release lever (39) is activated and the brake of S reel (38) is released by S main brake (42) . S main brake (42) is not activated even when plunger solenoid (4) operates under the condition of "loading, unloading or EJECT". (S main brake (42) is not operated during loading, unloading or EJECT).

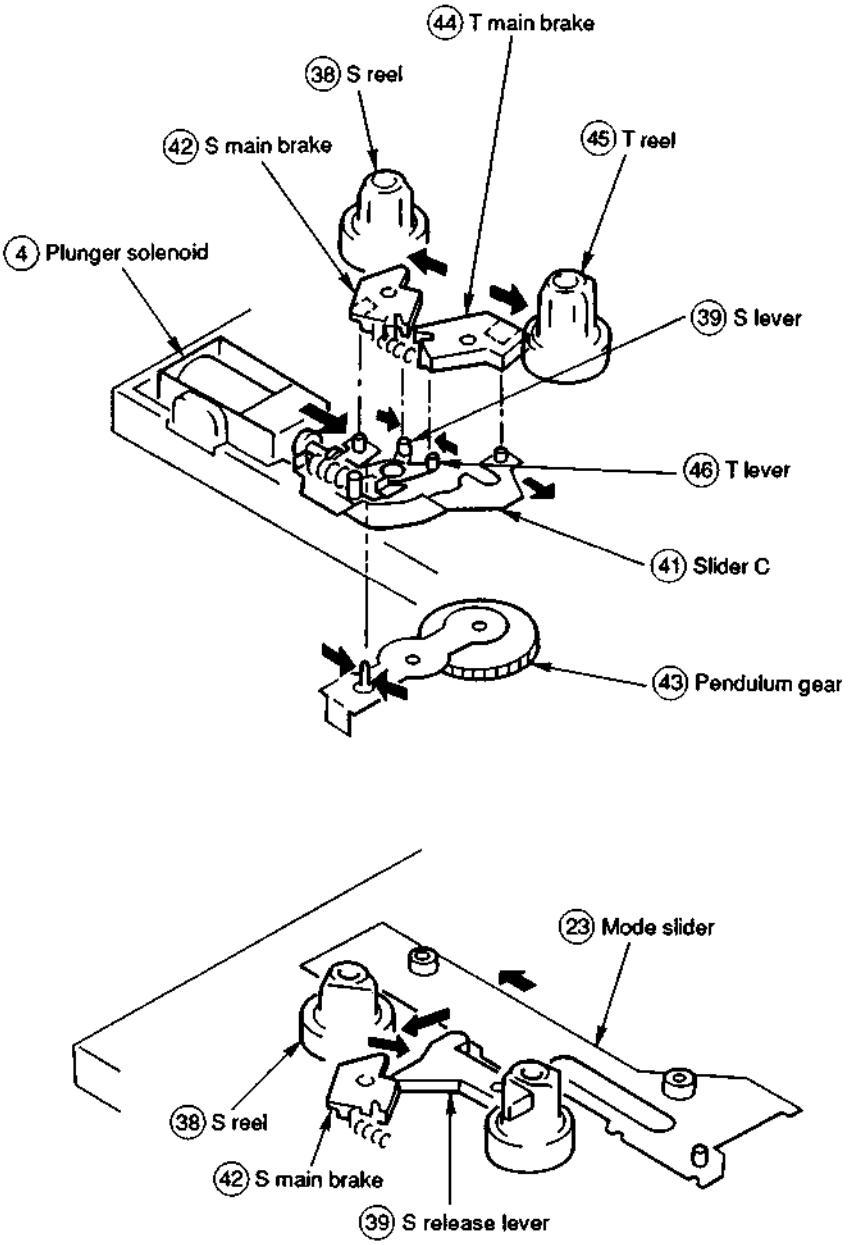
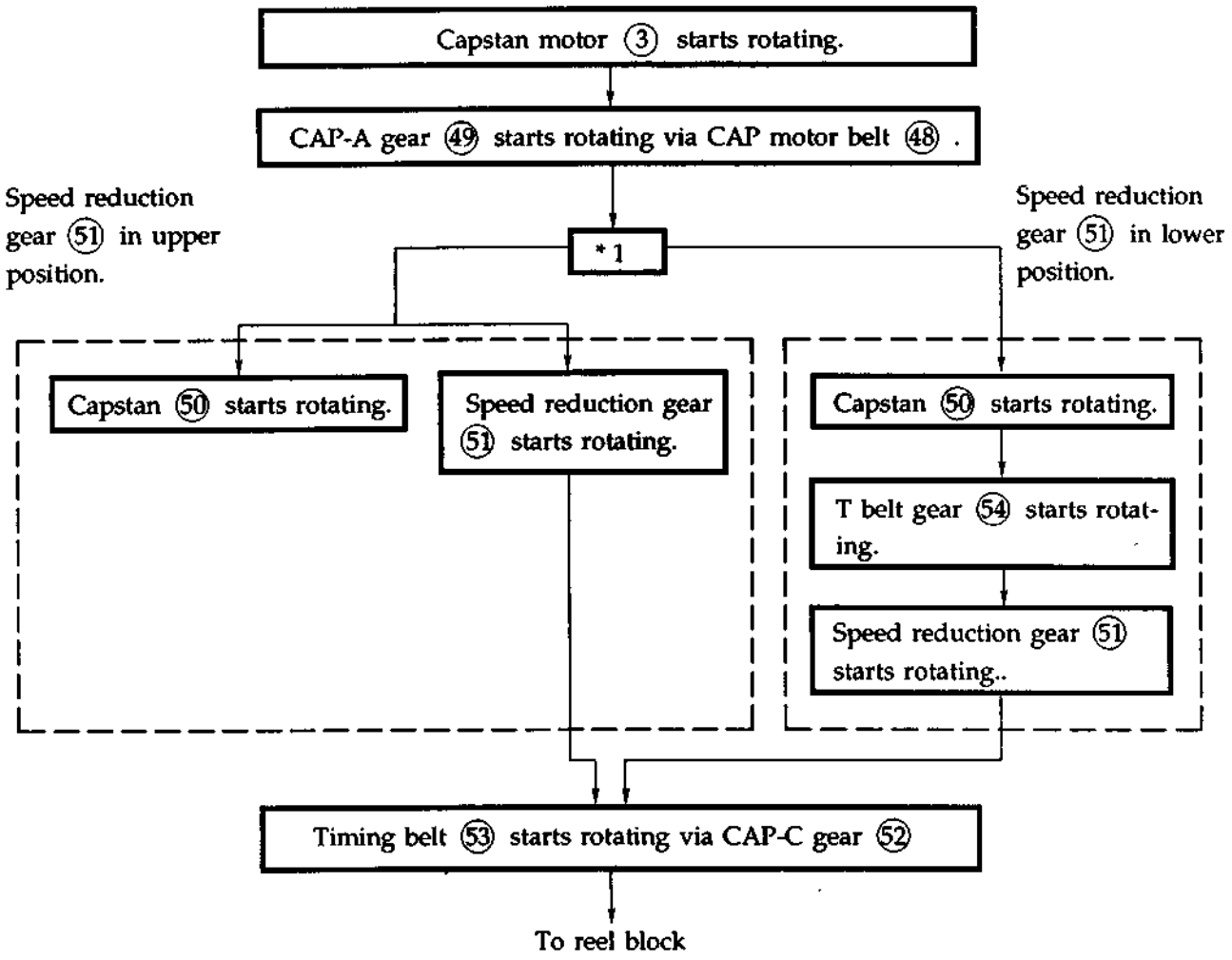

(44) T main brake
(38) S reel
(42) S main brake
(45) T reel
(4) Plunger solenoid
(39) S lever
(46) T lever
(41) Slider C
(43) Pendulum gear
(23) Mode slider
(38) S reel
(42) S main brake
(39) S release lever

Fig. 7-3

7-2-3. Operation of capstan



*1: Mode slider (23) starts sliding to move speed reduction gear (51) up and down via select lever (70) and speed reduction lever (40) .

- Speed reduction gear (51) in upper position:
  Capstan motor (3) speed is reduced to about 1/2 for operating reel block in loading, unloading, FF or REW mode.
- Speed reduction gear (51) in lower position:
  Capstan motor (3) speed is reduced to about 1/20 for operating reel block in PLAY mode.

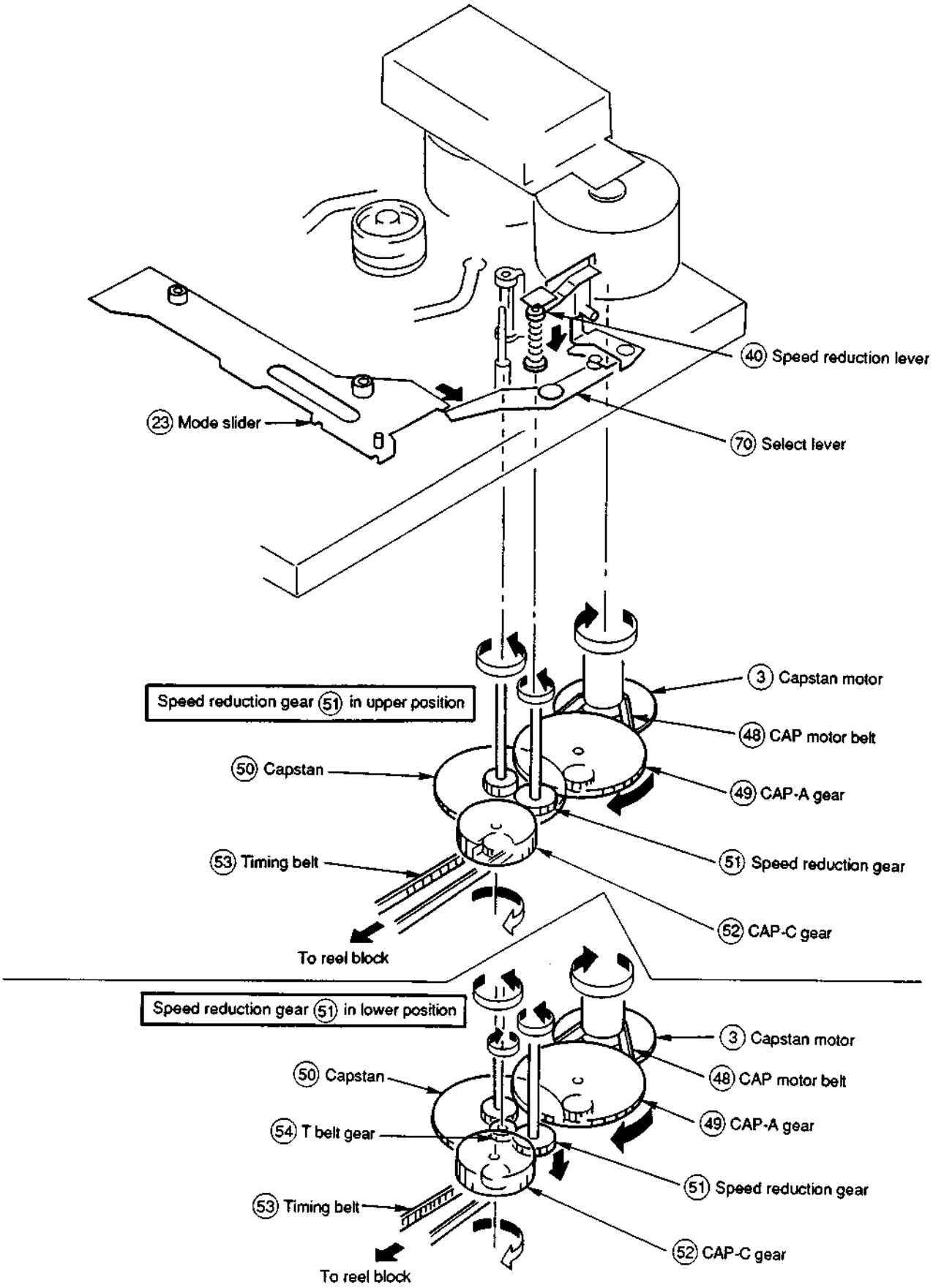
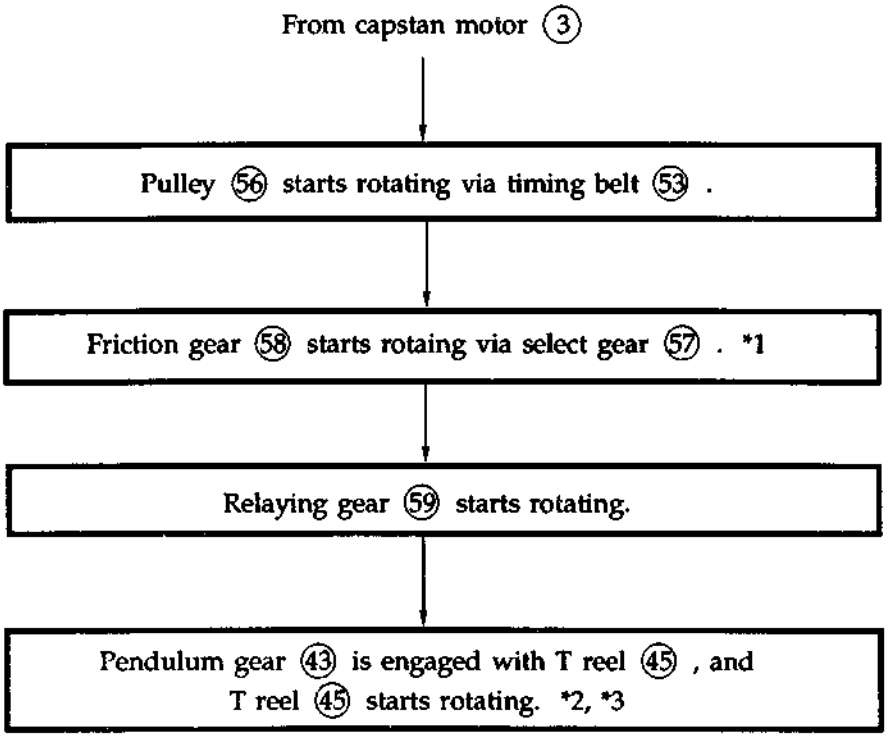

(40) Speed reduction lever
(23) Mode slider
(70) Select lever
Speed reduction gear (51) in upper position
(3) Capstan motor
(48) CAP motor belt
(50) Capstan
(49) CAP-A gear
(53) Timing belt
(51) Speed reduction gear
(52) CAP-C gear
To reel block
Speed reduction gear (51) in lower position
(3) Capstan motor
(50) Capstan
(48) CAP motor belt
(54) T belt gear
(49) CAP-A gear
(51) Speed reduction gear
(53) Timing belt
(52) CAP-C gear
To reel block

Fig. 7-4

7-2-4. Operation of reel



*1: Mode slider (23) starts sliding to move select gear (57) up and down via select lever (55) .
- Select gear (57) in upper position:
  Capstan motor (3) speed is controlled by friction gear (58) for rotating reel to stabilize tape speed in PLAY mode.
- Select gear (57) in lower position:
  Capstan motor (3) speed is directly transferred to reel in loading, unloading, FF or REW mode.

*2: When capstan motor (3) is in reverse rotation, pendulum gear (43) is engaged with S reel (38) . S reel (38) starts rotating.

*3: Mode slider (23) starts sliding, and reel is braked by reel soft brake (47) in STOP mode.

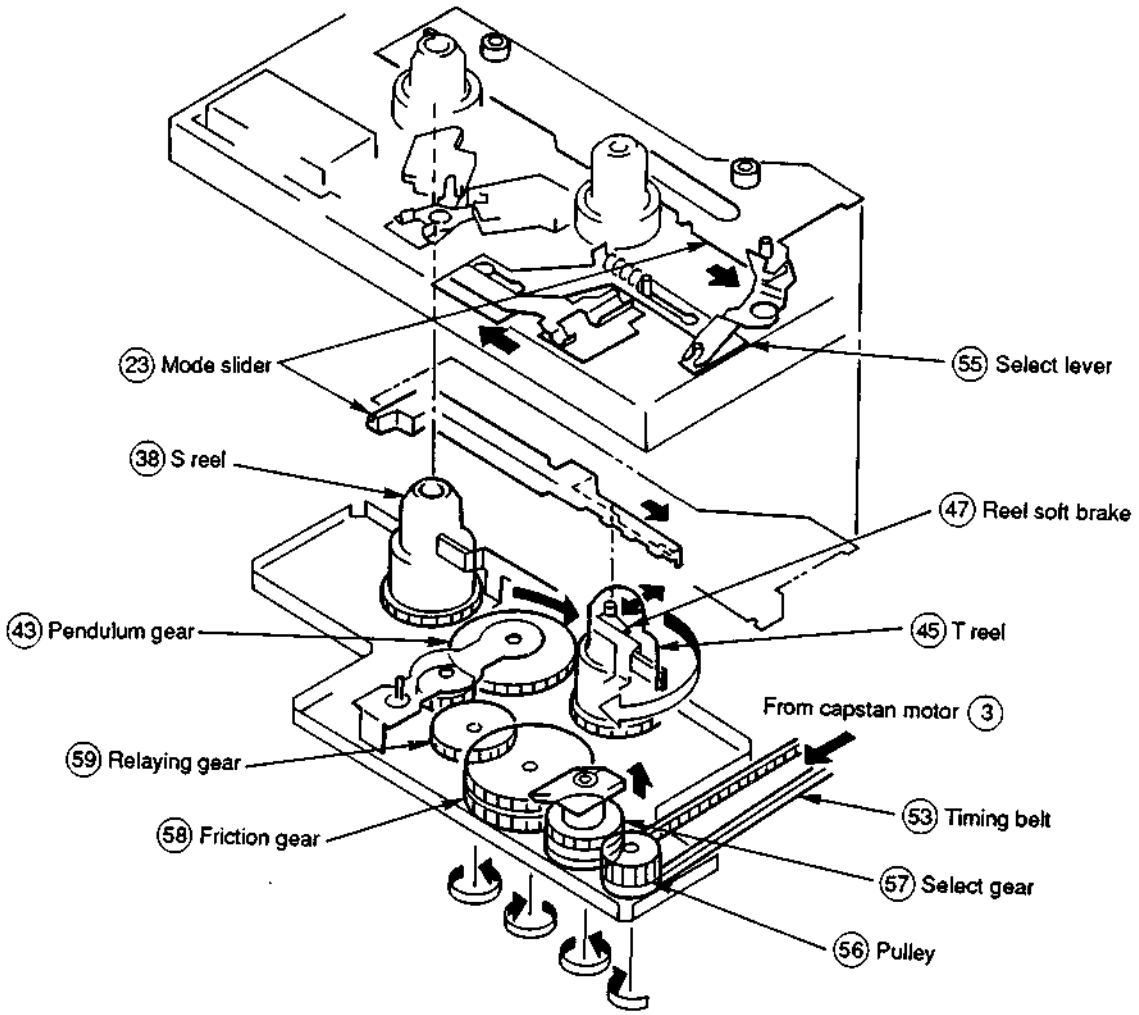

(23) Mode slider
(55) Select lever
(38) S reel
(47) Reel soft brake
(43) Pendulum gear
(45) T reel
From capstan motor (3)
(59) Relaying gear
(53) Timing belt
(58) Friction gear
(57) Select gear
(56) Pulley

Fig. 7-5

7-3. OPERATION OF EACH MODE

7-3-1. Cassette IN

Cassette is inserted.

↓

By pressing lever ⑥⓪ (left, right), lock arm ⑥① starts sliding to release the lock of cassette holder ⑥② .

↓

Cassette holder ⑥② slides a little.

↓

Cassette compartment switch 2 ⑥ (cassette IN, EJECT) turns OFF.

These parts are operated by inserting cassette.

↓

Loading motor ② starts rotating.

↓

Relaying gear C2 ⑥⑦ starts rotating via belt C ⑥③ , worm gear ⑥④ , worm wheel ⑥⑤ and gear C1 ⑥⑥ .

↓

Cassette holder ⑥② starts sliding in the direction of the arrow mark Ⓐ via gear C3 ⑥⑧ and gear C4 ⑥⑨ .

↓

Cassette lid is opened by lid lift lever ⑦① .

Cassette compartment switch 1 ⑤ (cassette down) turns ON.

- After the above operation, cassette is loaded automatically.

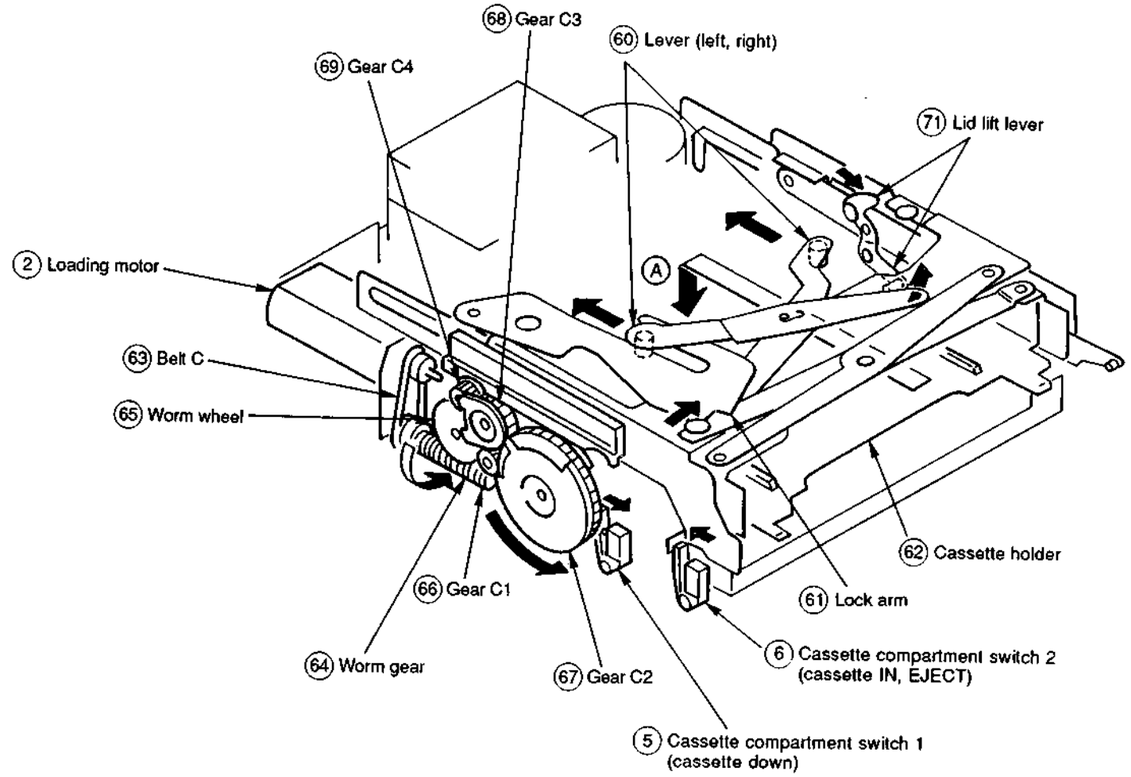
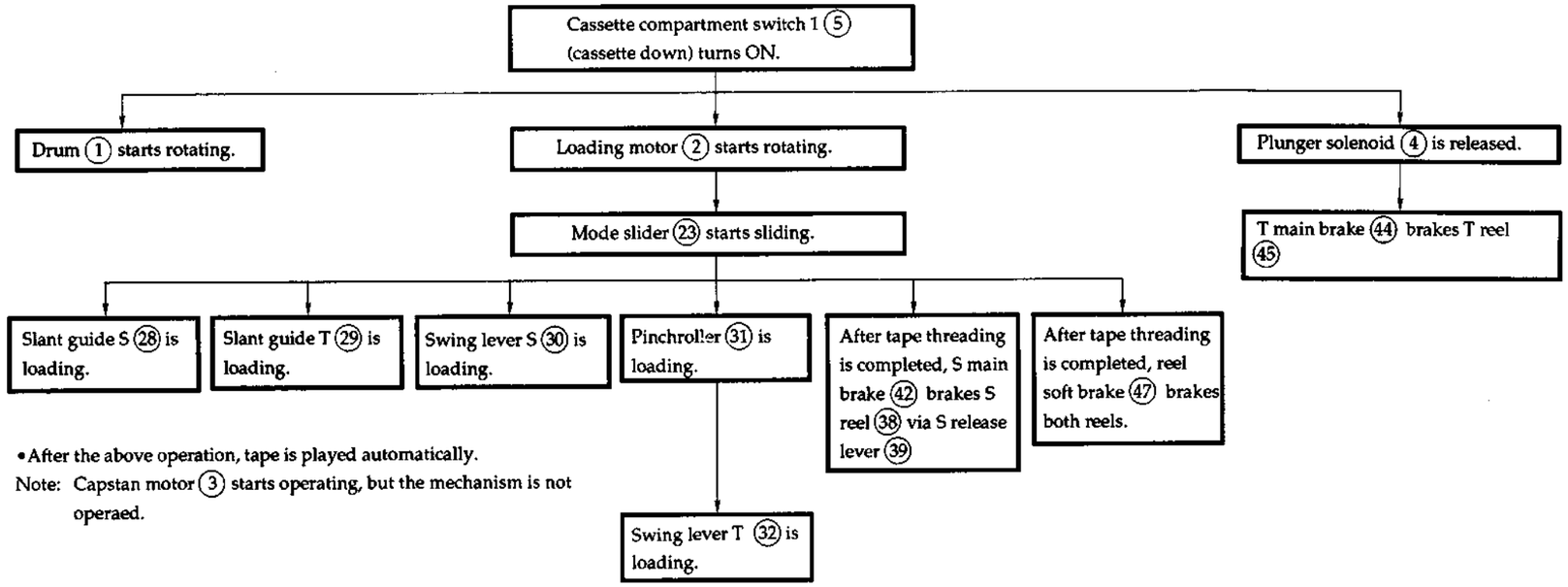


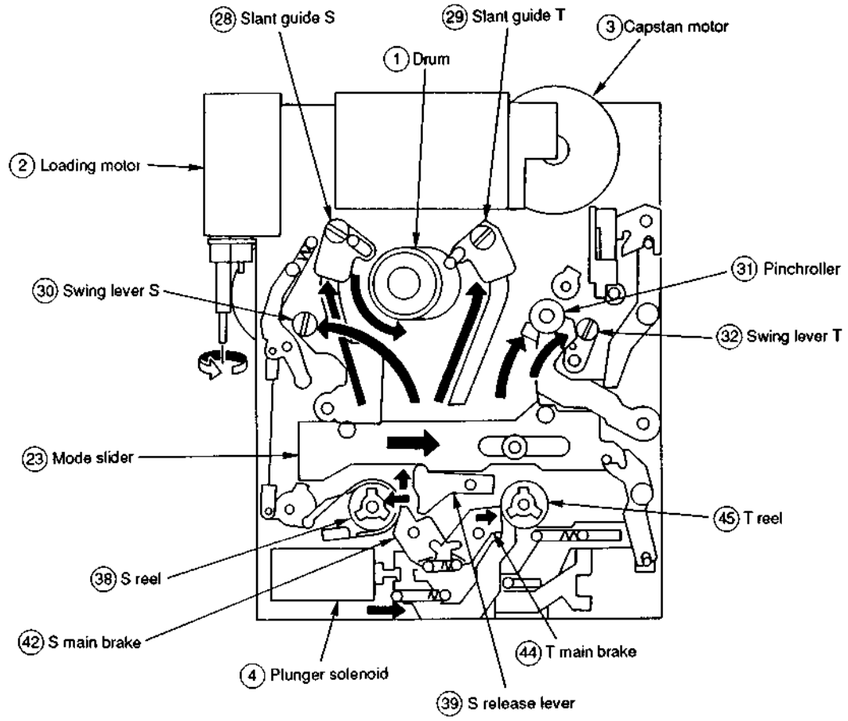
Fig. 7-6

7-3-2. Loading



- After the above operation, tape is played automatically.

Note: Capstan motor (3) starts operating, but the mechanism is not operaed.



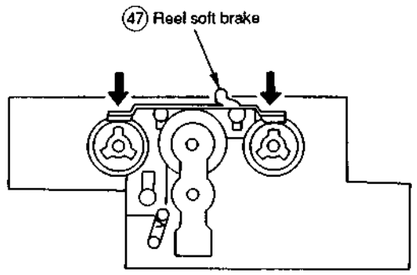
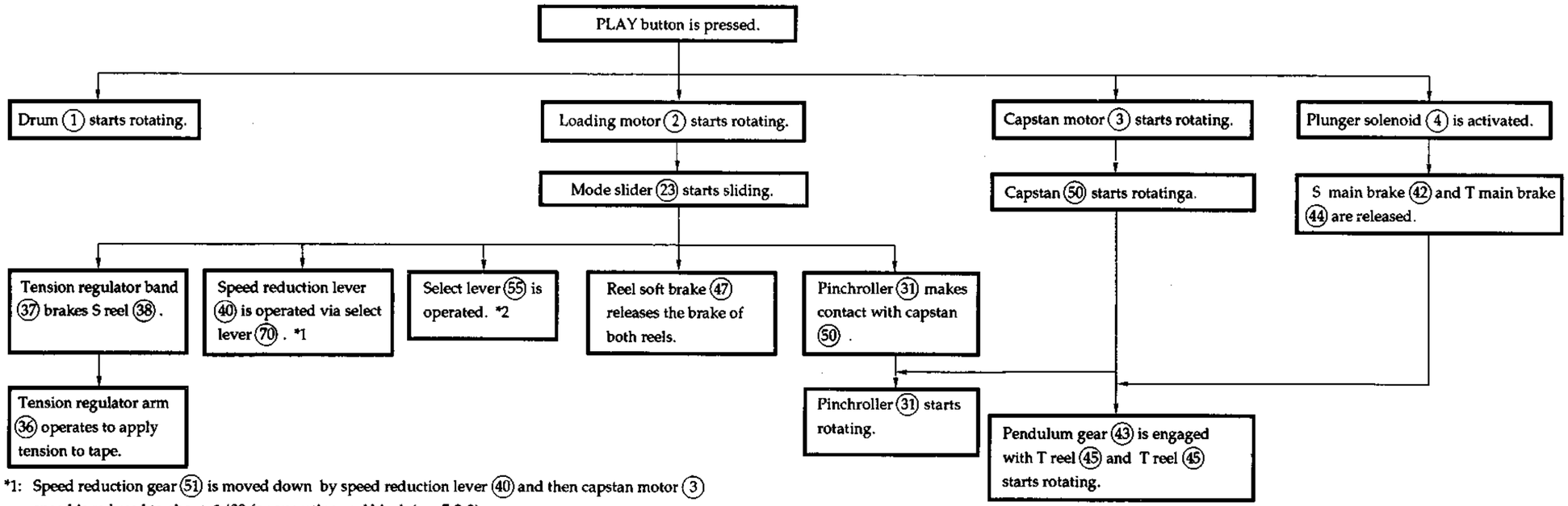


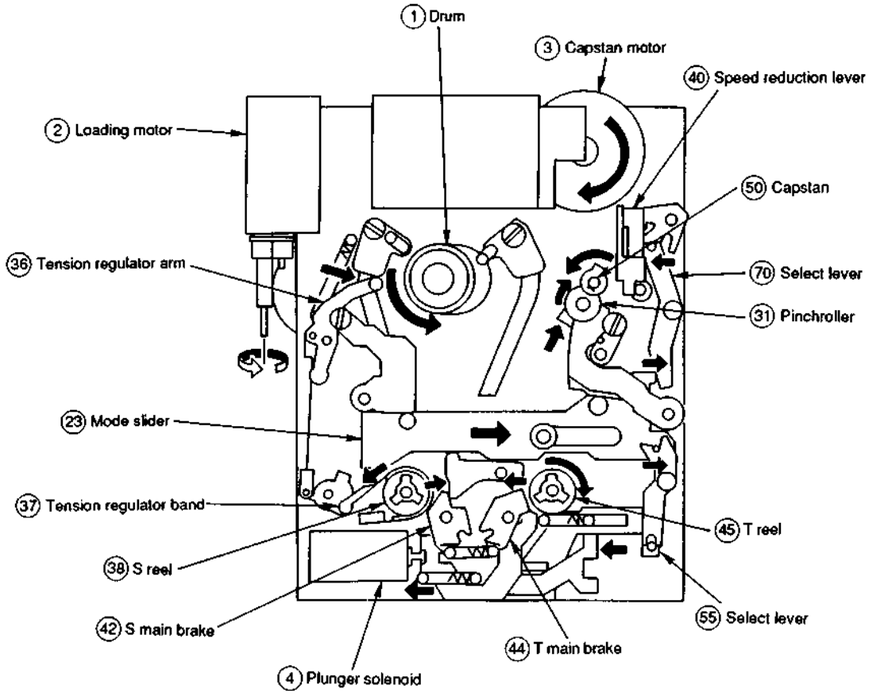
Fig. 7-7

7-3-3. PLAY



*1: Speed reduction gear (51) is moved down by speed reduction lever (40) and then capstan motor (3) speed is reduced to about 1/20 for operating reel block (see 7-2-3).

*2: Select gear (57) is moved up by select lever (55) and then capstan motor (3) speed is controlled for operating T reel (45) (see 7-2-4).



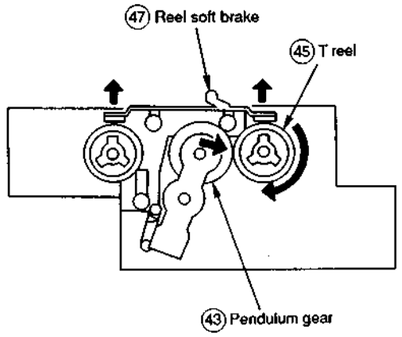
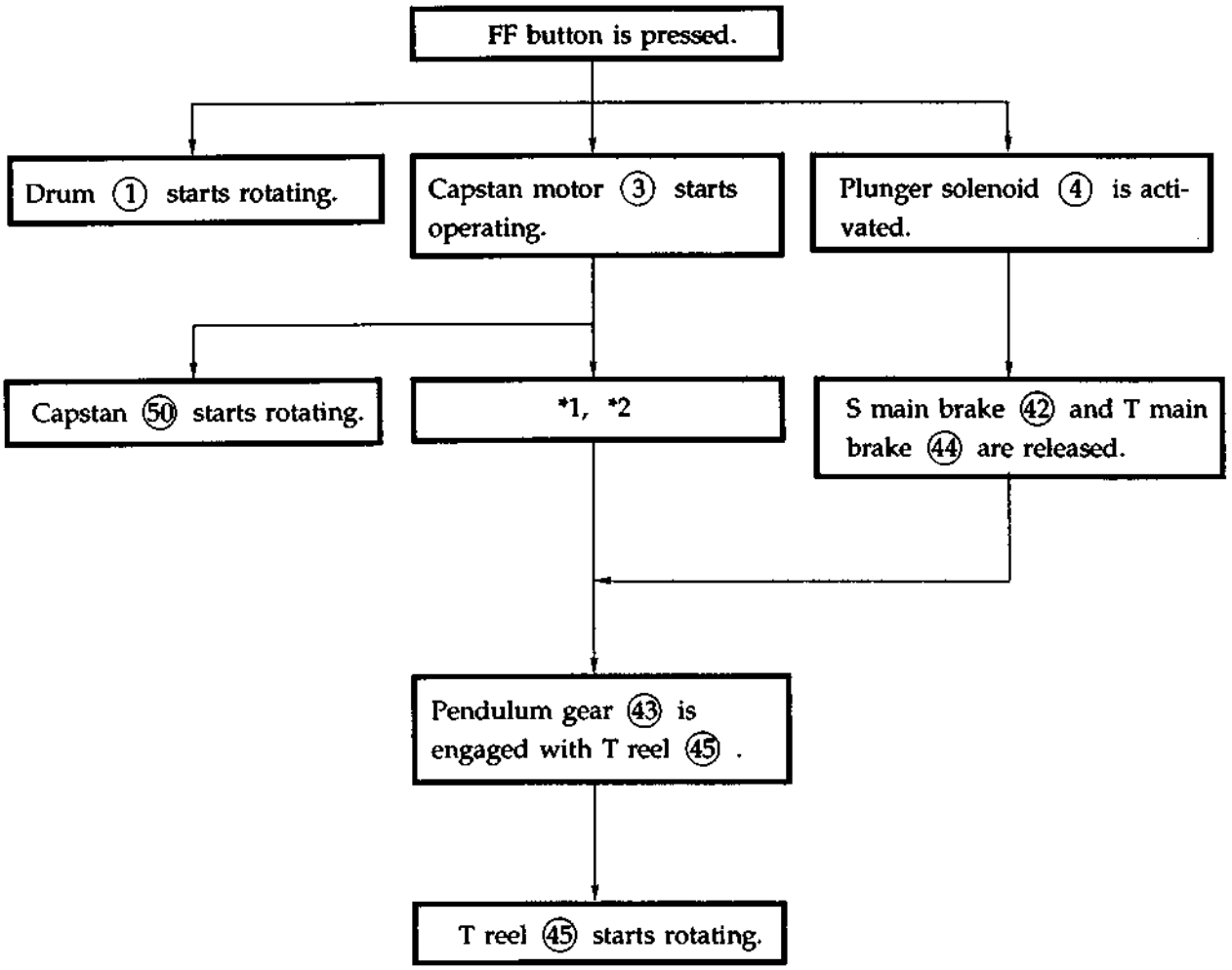


Fig. 7-8



*1: When speed reduction gear (51) is in upper position, capstan motor (3) speed is reduced to about 1/2 for operating reel block (see 7-2-3).

*2: When speed reduction gear (57) is in lower position, capstan motor (3) speed is directly transferred to T reel (see 7-2-4).

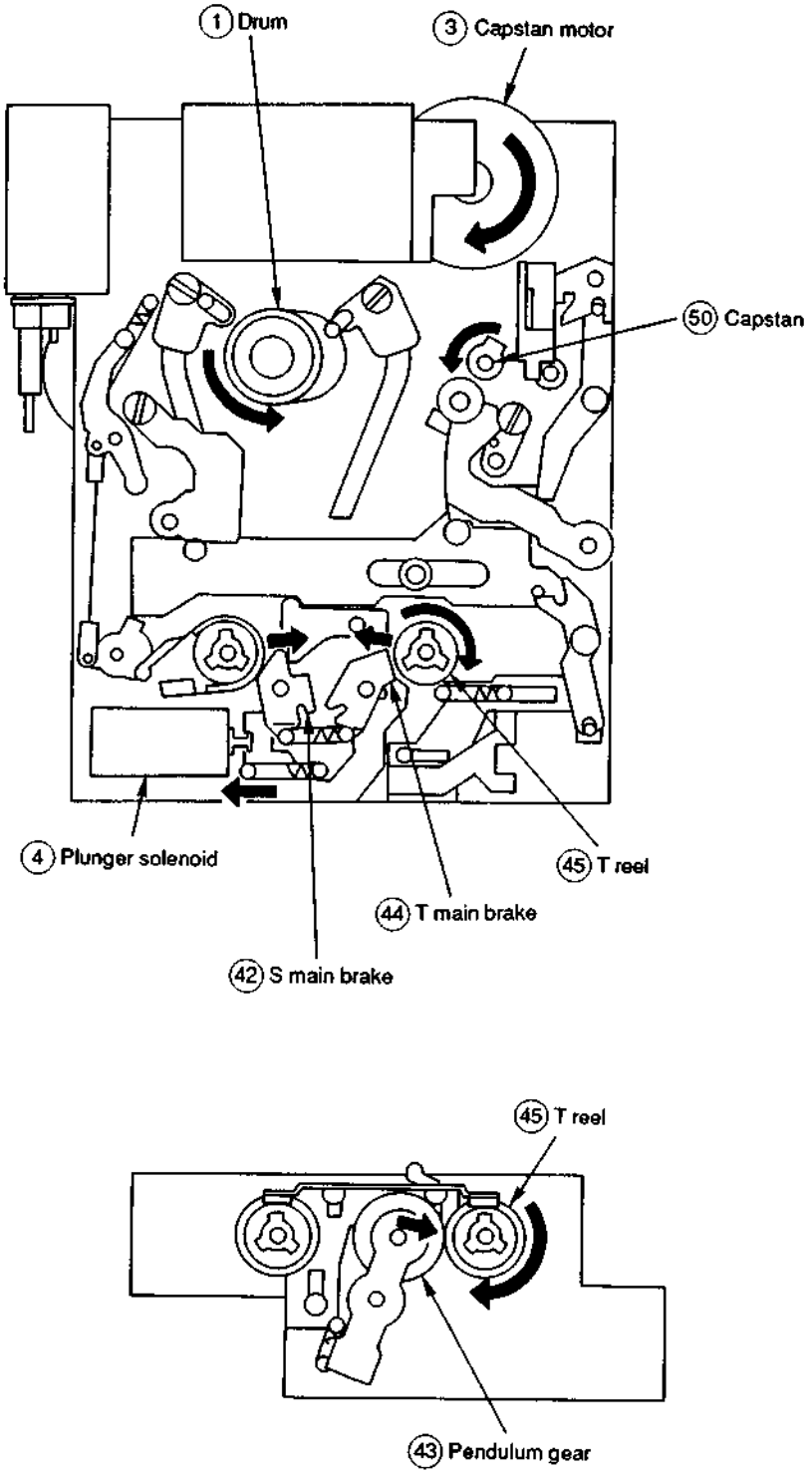
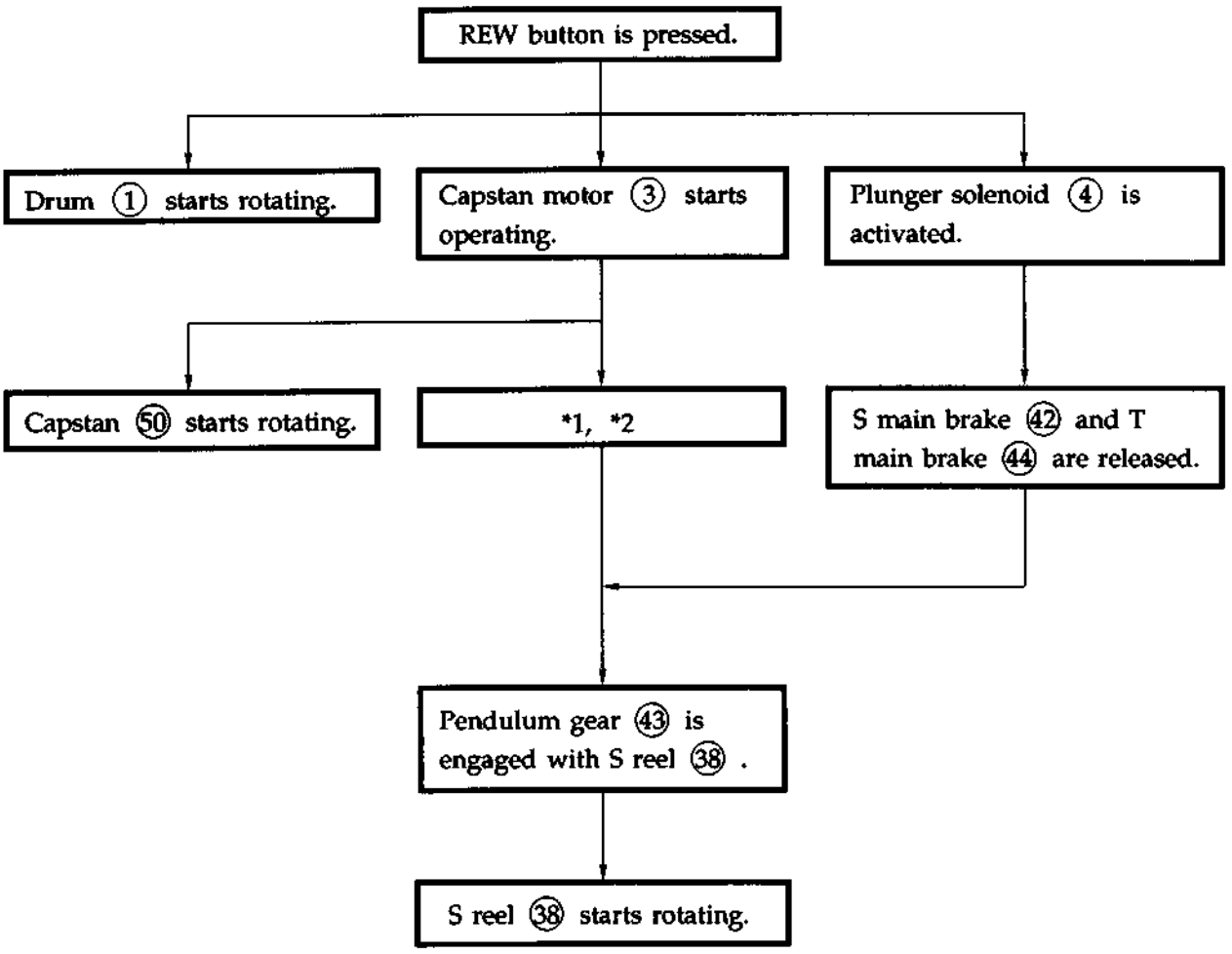

(1) Drum
(3) Capstan motor
(50) Capstan
(4) Plunger solenoid
(45) T reel
(44) T main brake
(42) S main brake
(45) T reel
(43) Pendulum gear

Fig. 7-9

7-3-5. REWIND



*1: When speed reduction gear ⑤① is in upper position, capstan motor ③ speed is reduced to about 1/2 for operating reel block (see 7-2-3).

*2: When speed reduction gear ⑤⑦ is in lower position, capstan motor ③ speed is directly transferred to S reel (see 7-2-4).

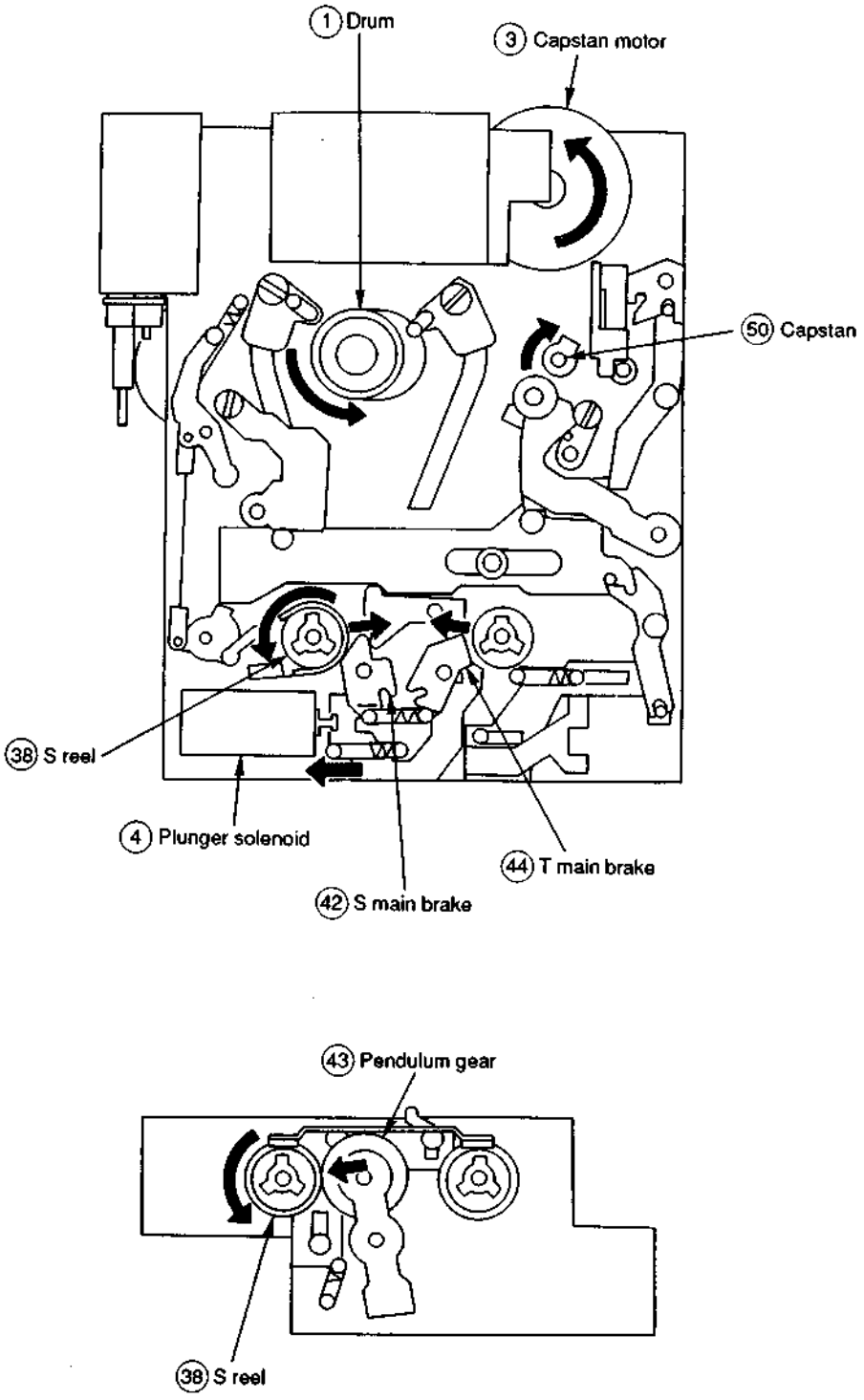
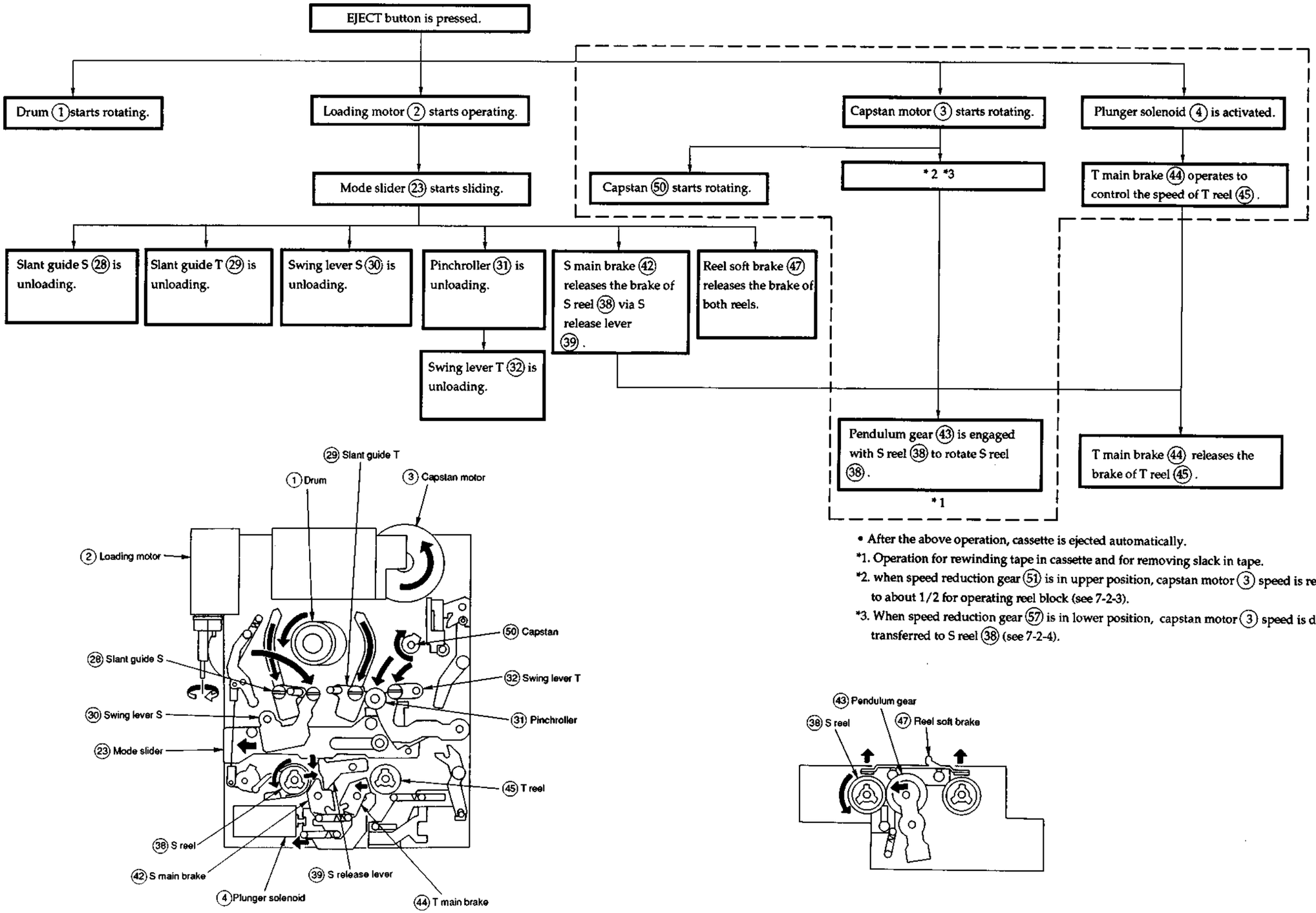

(1) Drum
(3) Capstan motor
(50) Capstan
(38) S reel
(4) Plunger solenoid
(44) T main brake
(42) S main brake
(43) Pendulum gear
(38) S reel

Fig. 7-10



- After the above operation, cassette is ejected automatically.

*1. Operation for rewinding tape in cassette and for removing slack in tape.

*2. when speed reduction gear (51) is in upper position, capstan motor (3) speed is reduced to about 1/2 for operating reel block (see 7-2-3).

*3. When speed reduction gear (57) is in lower position, capstan motor (3) speed is directly transferred to S reel (38) (see 7-2-4).

Fig. 7-11

7-3-7. EJECT (cassette OUT)

Loading motor (2) starts rotating.

↓

Gear C2 (67) starts rotating via belt C (63), worm gear (64), worm wheel (65) and gear C1 (66).

↓

Cassette holder (62) starts sliding in the direction of the arrow mark (A) via gear C3 (68) and gear C4 (69).

Cassette compartment switch 1 (5) (cassette down) turns OFF.

↓

Cassette compartment switch 2 (6) (cassette IN, EJECT) turns ON.

↓

Loading motor (2) stops.

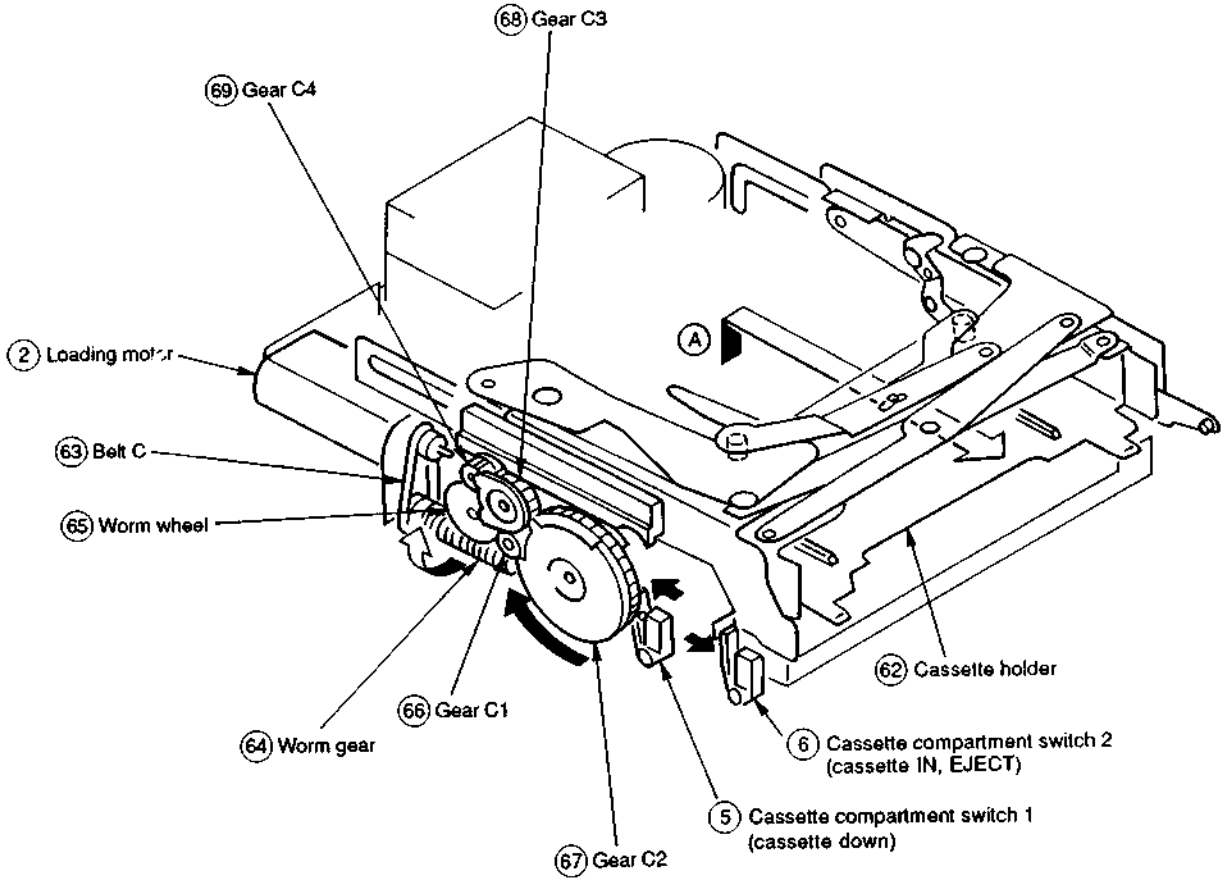


Fig. 7-12