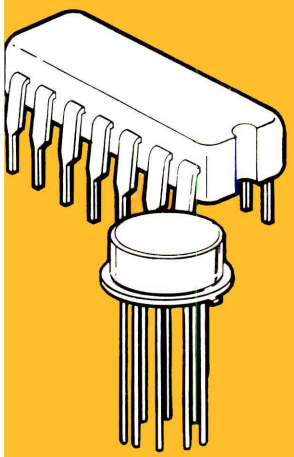
RCA Solid State
DATABOOK Series

SSD-202A

Linear
Integrated Circuits and MOS Devices
Application Notes



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1973 Edition

RCA Solid State
DATABOOK Series

Linear Integrated Circuits and MOS Devices

This DATABOOK contains application notes on linear integrated circuits and MOS field-effect (MOS/FET) devices presently available from RCA Solid State Division as standard products. Data sheets on both linear IC's and MOS/FET devices are contained in a separate DATABOOK, SSD-201A. For ease of reference, the application notes in this book are grouped in the same categories used in the SSD-201A: (a) IC receiver circuits; (b) IC arrays; (c) IC amplifier, control, and special-function circuits; (d) IC operational amplifiers; (e) MOS/FET devices.

A feature of this DATABOOK is the complete Guide to RCA Solid State Devices at the back of the book. This section includes a developmental-to-commercial-number cross-reference index, a comprehensive subject index, and a complete index to all standard devices in the solid-state product line: linear integrated circuits, MOS field-effect (MOS/FET) devices, COS/MOS integrated circuits, power transistors, power hybrid circuits, rf power devices thyristors, rectifiers, and diacs. All listings include references to volume number and page number in the 1973 DATABOOK series.

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G ☐ RF Power Semiconductors
H ☐ MOSFETS
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J ☐ Power Hybrid Circuits

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Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TRANSISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operations to provide some slack or an expansion elbow in each lead, to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. UNDER NO CIRCUMSTANCES, HOWEVER, SHOULD THE MOUNTING FLANGE BE SOLDERED DIRECTLY TO THE HEAT SINK OR CHASSIS BECAUSE THE HEAT OF THE SOLDERING OPERATION COULD PERMANENTLY DAMAGE THE DEVICE.

Such devices can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may

be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between transistor and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardware for the VERSAWATT transistors are given in the data bulletins for specific devices and in RCA Application Note AN-4124. When the transistor is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the transistor. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds

is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The transistor should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the transistor to become excessively high.

The TO-220AA plastic transistor can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. CD74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the transistor to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term transistor life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with respect to their component parts, as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol and unchlorinated freons are acceptable solvents. Examples of such solvents are:

1. Freon TE
2. Freon TE-35
3. Freon TP-35 (Freon PC)
4. Alcohol (isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44)

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing packages such as the JEDEC TO-5 and "modified TO-5" is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. These packages can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering. Soldering to the heat sink is preferable because it is the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. Such an arrangement is illustrated in RCA Publication MHI-300B, "Mounting Hardware Supplied with RCA Semiconductor Devices". If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trade Mark: Emerson and Cumming, Inc.

INTEGRATED CIRCUITS

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads,such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

COS/MOS (Complementary-Symmetry MOS) Integrated Circuits

Although protection against electrostatic effects is provided by built-in circuitry, the following precautions should be taken in handling these circuits:

1. Soldering-iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays. A conductive material such as "ECCOSORB LD26" or equivalent should be used.

Low-source-impedance pulse generators connected to the inputs of these devices must be disconnected before the dc power supply is turned off. All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit operation desired.

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to

moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

SOLID STATE LASERS AND EMITTING DIODES

Optoelectronic devices should employ the same mounting and heat-sink procedures utilized with other solid state devices. The temperature ratings established for storing, mounting, and operating these devices must not be exceeded to avoid damaging the emitters. Because the extremely small size and high driving-current requirements of some of these devices preclude the use of polarity marks on the housing and package configurations, care must be taken to insure that voltage is always applied in the proper direction. It is important, therefore, to refer to the data bulletin for the proper polarity before applying voltage to the device. Pulse driving circuitry should be designed to prevent transients (positive or negative) or momentary surges from exceeding drive conditions. The following suggestions are offered:

1. High-speed clipping diodes should be placed at terminals to bypass negative transients.
2. High-speed, sense-and-clamp circuitry should be used to prevent overdrive in peak or average current by clamping or disconnect techniques. For short pulses, ordinary thermal fuses should not be used because they do not provide adequate device protection.

The characteristics of solid state emitters vary substantially with changes in ambient temperature. Threshold, the point at which lasing starts, is highly dependent on temperature and requires compensation of drive current in applications where operation over a wide temperature range is a design requirement. A room-temperature laser can be damaged if a constant drive current is maintained while the ambient temperature is reduced to cryogenic levels. Published data bulletins for individual devices specify safe levels of operation.

In most cases, the voltage drop across a solid state emitter is of comparatively low amplitude; however, the required drive current may be many amperes. As in the case of other high-operating-current devices, therefore, clean and low-impedance contacts are required in all applications.

High voltage may be present in pulse-driven circuits utilizing these devices. Therefore, consideration should be given to the possibility of shock hazard which may result from contact with these high voltages. In general, where devices are operating at potentials which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Radiation Safety Considerations

Injection laser diodes emit electromagnetic radiation at wavelengths which may be invisible to the human eye. Suitable precautions must be taken to avoid possible damage to the eye from overexposure to this radiant energy. Precautionary measures include the following:

1. *In Systems with No External Lens* – Avoid viewing the laser source at close range. Since the emitted beam is not collimated, increasing the distance to the laser source greatly reduces the risk of overexposure.
2. *In Systems Utilizing External Optics* – Avoid viewing the emitter directly along the optical axis of the radiated beam.
3. *Reflections From Surfaces* – Minimize unwanted specular reflections in the system.

ADDITIONAL DATA

Additional information on handling, mounting, and operating RCA Solid State Devices is given in the following publications which are available on request from RCA/ Commercial Engineering, Harrison, N.J. 07029.

MHI-300B "RCA Mounting Hardware Supplied with RCA Semiconductor Devices"

1CE-338 "RCA Integrated Circuits Mounting and Connection Techniques"

AN-3822 "Thermal Considerations in Mounting of RCA Thyristors"

AN-4124 "Handling and Mounting of RCA Molded-Plastic Transistors and Thyristors"

Application Notes on IC Receiver Circuits

ICAN-5269	"Integrated Circuits for FM Broadcast Receivers"	14
ICAN-5380	"Integrated-Circuit Frequency-Modulation IF Amplifiers"	21
ICAN-5765	"Power-Supply Considerations for CA3041 and CA3042 Integrated Circuits"	28
ICAN-5831	"Application of the RCA-CA3044 and CA3044V1 Integrated Circuits in Automatic-Fine-Tuning Systems"	33
ICAN-5841	"Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits"	38
ICAN-6022	"An IC for AM Radio Applications"	42
ICAN-6544	"A Single IC for the Complete PIX-IF-System in TV Receivers"	46
ICAN-6724	"A Flexible Integrated-Circuit Color Demodulator for Color Television"	58

Integrated Circuits For FM Broadcast Receivers

by

R.L. Sanquini

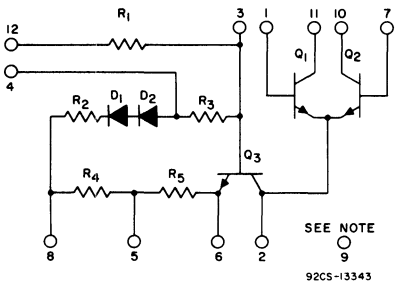
Silicon monolithic integrated circuits have certain design features which make them more attractive than discrete-component circuits for consumer electronic applications. These features include small size, light weight, high reliability, and more potential circuit functions per dollar of cost. Until recently, the major limitation to the extensive use of integrated circuits in commercial FM (88-to-108-MHz) broadcast receivers has been the relatively high cost of such circuits when they were designed to perform the same functions as their discrete-circuit counterparts. This limitation has now been removed by the introduction of high-reliability, low-cost, multifunction integrated circuits such as the RCA CA3005, CA3011, CA3012, CA3013, and CA3014. With these circuits, high-performance inexpensive FM receivers can be designed to meet the rigorous standards set by high-quality commercial FM receivers using vacuum tubes and transistors.

This note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits

CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

FM Tuner

The CA3005 is the basic building block for the three front-end approaches discussed below. A schematic diagram of the CA3005 is shown in Fig. 1. Fig. 2

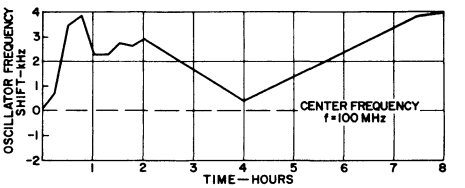


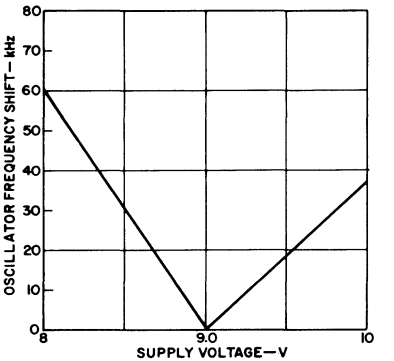
Note: Connect terminal 9 to most positive dc supply voltage.

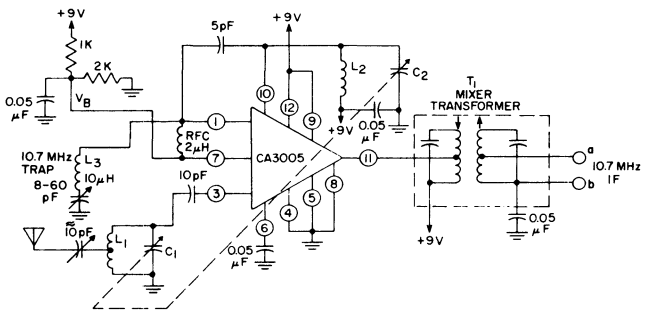
Fig. 1 - Schematic diagram of RCA CA3005 integrated-circuit rf amplifier.

shows a single-chip front end that uses one CA3005 and a two-gang capacitor tuning system. The CA3005 performs the functions of rf amplifier, oscillator, and mixer in a unique manner.

The circuit operation may best be explained by reference to Figs. 1 and 2. The first function of the current-sink transistor Q_3 in Fig. 1 is to supply the emitter currents for the differential-amplifier transistors Q_1 and Q_2. Positive feedback from the collector of Q_2 (terminal 10) to the base of Q_1 (terminal 1) through the 5-picofarad capacitor shown in Fig. 2 establishes the oscillator function; the frequency of oscillation is determined by the tuned circuit L_2 and C_2. Because the output impedance at the collector of Q_3 is high compared to the input impedance at the emitter of Q_1 and Q_2, Q_3 is isolated from Q_1 and Q_2 and receives very little oscillator signal. The rf input signal







L_1 – 4 turns of No. 22 wire, center-tapped; 1/4" O.D. coil form, "E" mat'l slug

L_2 – 6 turns No. 32 wire on toroid core; Radio Industries Inc., 1/4" O.D., No. 8 mat'l

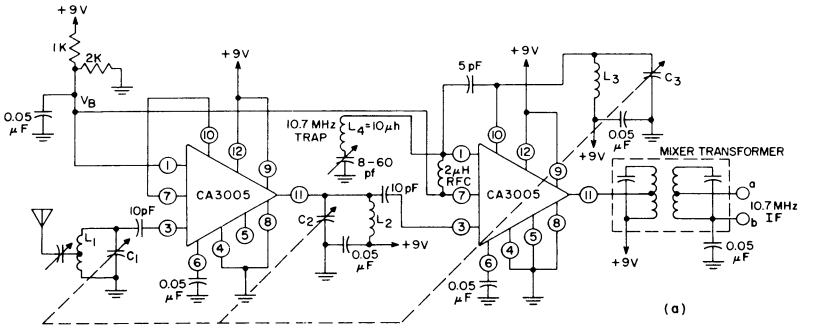
T_1 – TRW No. 21629, or equiv.

Fig. 2 - Single-chip front end using the CA3005. Curves show oscillator stability with time and supply voltage.

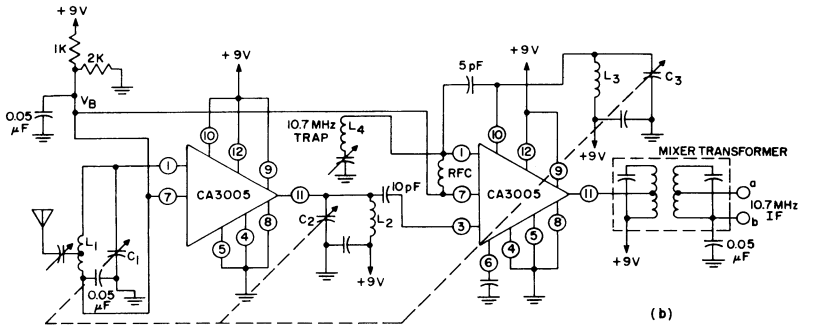
is applied to the base of Q_3 (terminal 3), amplified, and injected into the emitter of Q_1 and Q_2 to mix with the oscillator signal. The 10.7-MHz intermediate frequency is obtained from the collector of Q_1 (terminal 11).

The CA3005 draws a total current of 4.5 milliamperes from the +9-volt supply. The front end shown in Fig. 2 has a power gain of 15 dB and a sensitivity of 10 microvolts for 30 dB of quieting; it can handle a maximum input signal of 7 millivolts. Automatic frequency control can be applied to the oscillator in a conventional manner by connection of a voltage-dependent capacitor (diode) to the oscillator tuned circuit L_2 and C_2. Curves of oscillator stability as a function of time and supply voltage are also shown in Fig. 2.

The approach to the front end shown in Fig. 2, although economical, results in only adequate performance. Improved performance can be obtained by addition of an rf amplifier to the mixer-oscillator circuit, as shown in Fig. 3. In this figure, a CA3005 used as an rf amplifier and a three-gang capacitor tuning system are added to the basic single-chip circuit to provide higher power gain, lower noise figure, and improved selectivity. The CA3005 is connected as a cascode amplifier in Fig. 3(a) and in an emitter-coupled configuration in Fig. 3(b). Both configurations require no neutralization.



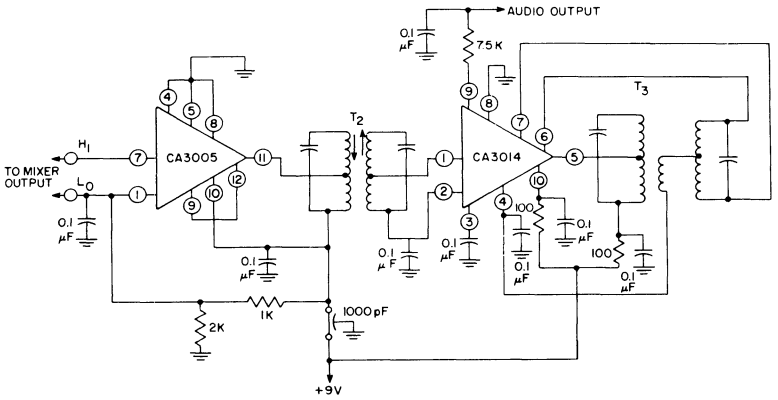
L_1 – 4 turns No. 22 wire; center-tapped; 1/4-inch outer-diameter coil form; "E" material slug
L_2 – Same as L_1 without center tap
L_3 – 6 turns No. 32 wire on toroid core; Radio Industries, Inc.; 1/4-inch outer diameter; No. 8 material
Mixer Transformer – TRW No. 21629, or equiv.



L_1 – 4 turns of No. 22 wire; center-tapped; 1/4-inch outer-diameter coil form: "E" material slug
L_2 – Same as L_1 without center tap
L_3 – 6 turns of No. 22 wire on toroid core; Radio Industries, Inc.; 1/4-inch outer diameter; No. 8 material
Mixer Transformer – TRW No. 21629, or equiv.

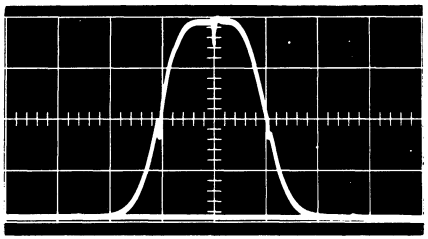
Fig. 3 - Two-chip front ends using CA3005 rf amplifier connected (a) in cascode, and (b) in emitter-coupled configuration.

The cascode front end has a higher power gain (28 dB, as compared to 24 dB for the emitter-coupled configuration), but the emitter-coupled front end has better cross-modulation characteristics. The emitter-coupled amplifier can handle interfering signals up to about 15 millivolts with 10 per cent cross-modulation at maximum gain, while the capability of the cascode amplifier is limited to that of a single transistor.[1] The cascode front end has a sensitivity of 2 microvolts for 30 dB of quieting, while the emitter-coupled front end has a sensitivity of 3 microvolts. Reverse agc can be applied to both configurations by variations of the voltage at terminal 12 from 9 volts (maximum gain) to 3 volts (full cutoff) from a 0.5-milliampere agc source. Both amplifiers have a dynamic agc range of 60 dB.

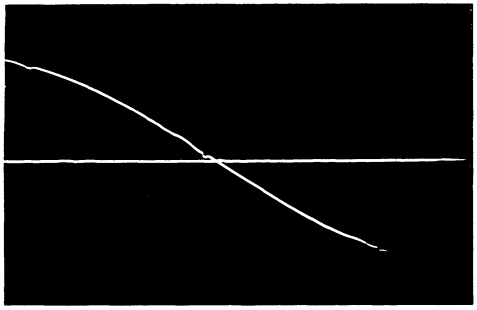


T_2 = TRW No. 22468 or equiv.

T_3 = TRW No. 21590 or equiv.



10.7-MHz IF SELECTIVITY CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)



DETECTOR "S" CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)

Fig.4 - Two-chip 10.7-MHz if amplifier, limiter, and discriminator using CA3005, CA3014, and Interstage transformer. Photographs show selectivity curve, detector "S" curve.

FM IF Amplifier, Limiter, and Detector

Fig. 4 shows a 10.7-MHz FM if strip and detector that uses a CA3005 and a CA3014 to provide 95 dB of gain. The schematic diagram of the CA3005 was shown in Fig. 1; the CA3014 schematic is shown in Fig. 5. The heart of both these integrated circuits is the differential amplifier, which is probably the best simple configuration on the market today for symmetrical limiting over a wide input-voltage range. The differential-amplifier configuration is also ideal for integration because the parameters that are most important in integrated-circuit design (matched V_{BE}, matched beta, and resistor ratios) are the easiest to control on a single silicon chip. In the FM if strip, therefore, three advantages are obtained: high performance, low cost, and fewer individual components.

The input limiting knee for the if strip shown in Fig. 4 is 30 microvolts. The recovered audio obtained from terminal 9 of the CA3014 is 220 millivolts rms. The if selectivity curve and the detector "S" curve are also shown in Fig. 4. The AM rejection referenced to a 30-percent modulated (FM and AM) signal with the AM signal at 30 millivolts is 50 dB.

The 10.7-MHz if-amplifier circuit of Fig. 4 operates as follows: The 10.7-MHz FM signal from the mixer is applied to terminal 7 of the CA3005. The gain from this point to the input of the CA3014 is 25 dB. The interstage transformer T_2 is designed so that the collector output of the CA3005 at terminal 1 does not saturate. As a result, bandpass spreading is kept to a minimum over large swings in input voltage. The 10.7-MHz FM signal receives additional gain of 70 dB and limiting from terminal 1 to terminal 5 in the CA3014. The FM output at terminal 5 is applied to the primary winding of the phase-shift (discriminator) transformer T_3. The secondary winding, which is connected to terminals 6 and 7, is in quadrature with the primary voltage at the center frequency, 10.7 MHz. As the FM signal varies, the phase shift of the secondary voltage follows the modulation. The detected output at the base of Q_{11} in the CA3014 (terminals 6 and 7) is thus amplified and buffered. The recovered audio is taken from the low-impedance terminal 9.

If more selectivity in the if strip is desired, an additional double-tuned transformer can be added to the circuit.

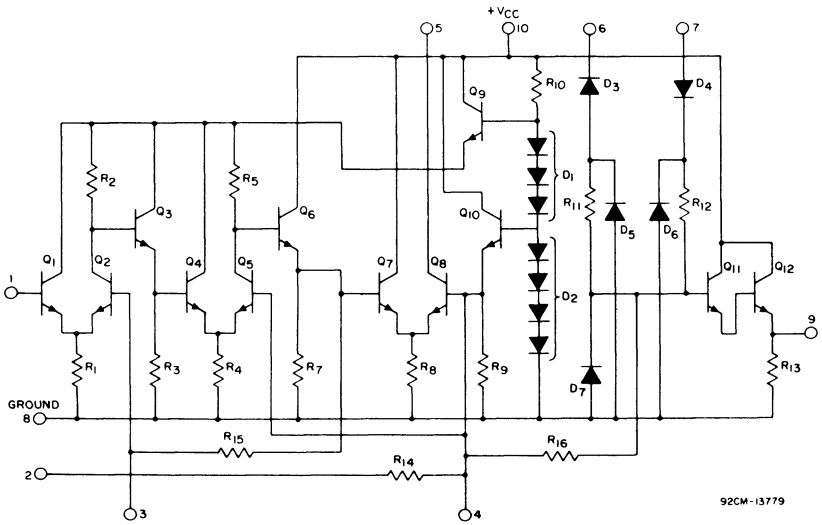


Fig. 5 - Schematic diagram of RCA CA3014 wide-band amplifier-discriminator.

Fig.6 shows an approach in which the two transformers areplaced immediately after the mixer stage. Fig.7 shows the details of the input filter and Fig.8 shows the schematic of the CA3012 used in the if stages of this circuit. When the transformers (10.7-MHz filter) are placed immediately after the mixer, better adjacent-channel rejection is obtained.

References

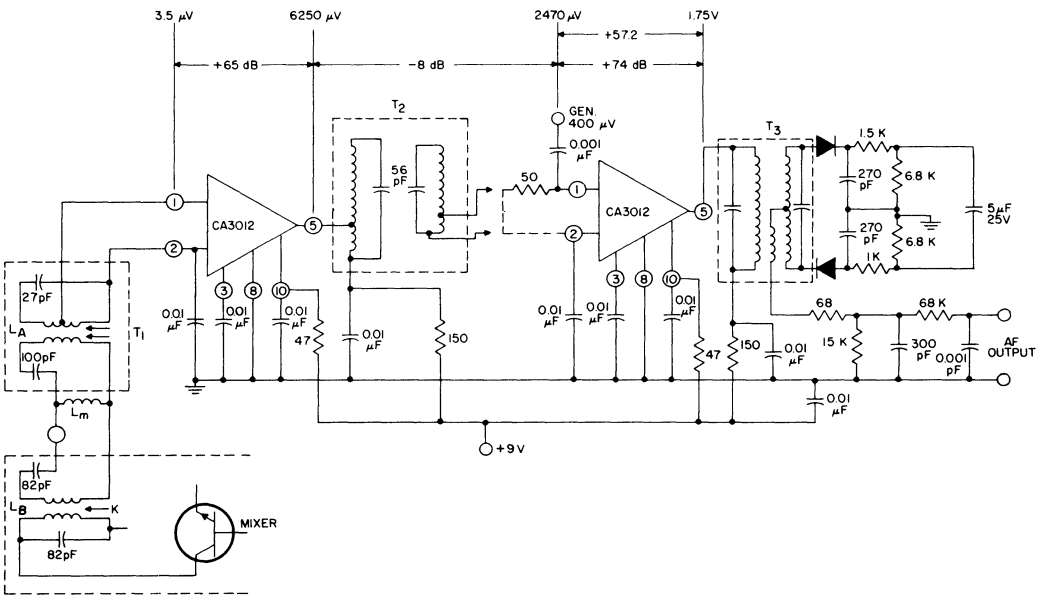
1. "Application of RF Amplifier-Mixer Integrated Circuits CA3004, CA3005, and CA3006," RCA APPLICATION NOTE ICAN-5022, November 1965

2. Mischa Schwartz, INFORMATION TRANSMISSION MODULATION AND NOISE, McGraw-Hill Book Company, 1959

3. J. Avins, "It's a television first. . . .receivers with integrated circuits," ELECTRONICS, March 21, 1966

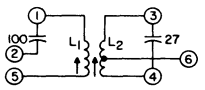
4. RCA Technical Bulletins: CA3005, CA3011-3012, CA3013-3014

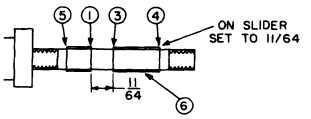
5. R. L. Sanquini, "Multipurpose Chips Cut Costs of FM Receiver," ELECTRONICS, May 16, 1966



T_1 - for details see Fig.7
T_2 - TRW No.22960-R2 or equiv.
T_3 - TRW 23148 or equiv.

Fig.6 - 10-MHz if amplifier and detector.





Winding 1-5 - 17 turns #36SE or equiv., $Q_\mu \approx 70$
Winding 3-4 - 40 turns #36SE or equiv., $Q_\mu \approx 75$
Winding 4-6 - 5 turns max; RX-Meter-900 ohms (no load)
Tuning slug: Winding 1-5 - Carbonyl TH or equiv., 1/4" long
Winding 3-4 - Carbonyl TH or equiv., 5/16" long
Front End: $KQ \leq 1$, $Lm = K\sqrt{LA\ LB} = 0.049\ \mu H$

TEST CIRCUIT:

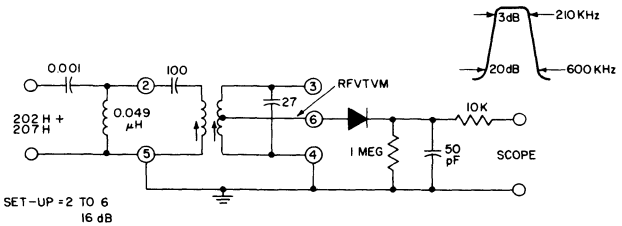
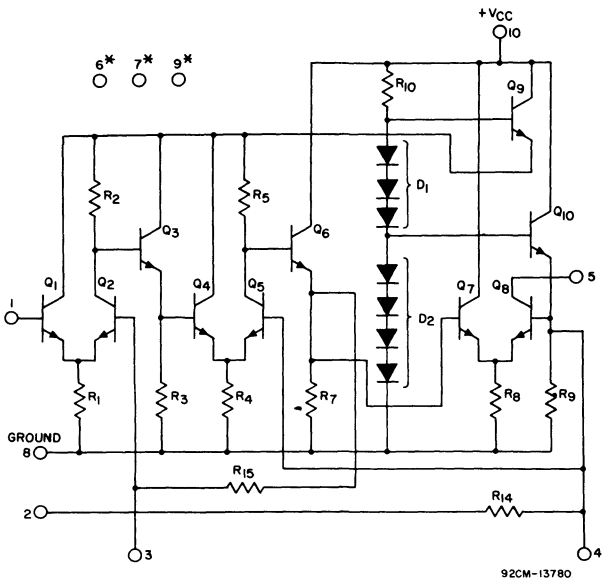


Fig.7 - Details of 10.7-MHz input filter, T_1.



* Internal Connection - Do Not Use
Note: R_6 Deleted

Fig.8 - Schematic diagram of RCA CA3012 wide-band amplifier.

Integrated-Circuit Frequency-Modulation IF Amplifiers

by

H.C. Kiehn and R.L. Sanquini

Silicon monolithic integrated circuits that use a differential-amplifier configuration have certain design features which make them more attractive than discrete-component circuits for FM if-amplifier applications. These features include better performance, small size, light weight, and more potential circuit functions per dollar of cost.

The Differential Amplifier

The heart of integrated-circuit FM if amplifiers is the differential amplifier, which is probably the best simple configuration available today for symmetrical limiting over a wide input-voltage range. Each half of the differential amplifier is alternately cut off on positive and negative half-cycles of the input signal.

As shown in Fig.1, the total current through the circuit I_T is relatively constant. A current equal to $I_T/2$ flows through each transistor at balance (quiescent condition). When the base voltage V_{B1} is made

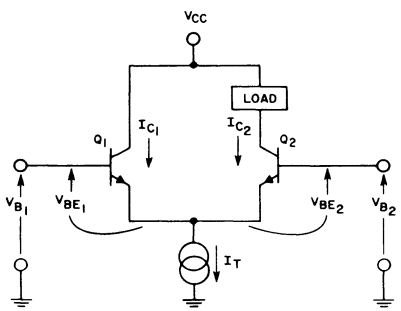


Fig.1 - Basic differential-amplifier configuration.

This material was presented at the IEEE Second Annual Semiconductor-Device Clinic on Linear Integrated Circuits in New York City, March 24, 1967.

more positive than V_{B2}, however, the collector current I_{C1} increases and I_{C2} decreases. The value of I_{C1} becomes equal to the total current I_T when the following condition exists:

$$V_{B1} - V_{B2} - V_{BE1} \geq V_{BE2} \text{ (threshold)}$$

The transistor Q_1 is then full on, and Q_2 is then cut off. Similarly, when V_{B1} is made more negative than V_{B2}, the value of I_{C2} becomes equal to I_T; Q_1 is then cut off and Q_2 is full on. When the worst-case value of I_T is known, the maximum load impedance for symmetrical limiting is selected so that collector saturation does not occur, as follows:

$$\text{Resistive Load: } R_L = V_{CC}/I_T$$

$$\text{Tuned Load: } R_L = 2\,V_{CC}/I_T$$

Under these conditions, symmetrical limiting is obtained without spurious phase modulation.

The transfer characteristics for a typical differential amplifier shown in Fig.2 illustrate the excellent

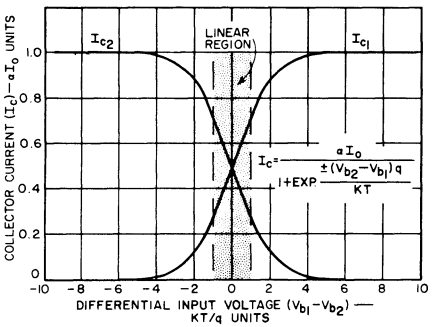


Fig.2 - Transfer characteristics of basic differential-amplifier circuit.

limiting characteristics. Further increases in input voltage (V_{B1} - V_{B2}) produce no change in collector current above 4KT/q units of input signal.

There are two basic approaches to the design of integrated-circuit FM if-amplifier stages using differential amplifiers: (1) lumped-filter FM if amplifiers using high-gain multi-stage integrated-circuit packages, or (2) individually tuned FM if amplifiers using single-stage integrated-circuit packages. This paper discusses the performance obtained with these approaches and outlines their merits and limitations.

Evolution of High-Gain Selective Building Blocks

The tuned rf amplifiers used in early broadcast receivers soon exhibited a point of diminishing returns with regard to gain and selectivity improvements. With the advent of the superheterodyne principle, the intermediate-frequency amplifier became the first building block that had fixed-frequency tuning, relatively high gain, and good selectivity as a result of its operation at a frequency lower than the signal frequency.

Because of its demands for high gain, phase linear amplification, and good symmetrical amplitude limiting, and because of the numerous FCC station allocations, FM broadcasting is now facing the dilemma of providing selectivity with good phase response. That is, receiver selectivity must be maintained for large signal inputs without deterioration of phase response. (A discussion of the practical solution of this problem is beyond the scope of this paper.) Successive limiting from the last stage back to the first stage can no longer be tolerated.

High-Gain-Per-Package Differential Integrated-Circuit IF Strips

Fig.3 shows the schematic diagram of a high-gain integrated circuit, the CA3012, which can be used in an if-amplifier strip to drive a ratio detector. The CA3012 wideband amplifier, designed for use in FM broadcast or communications receivers, is basically an if amplifier-limiter intended for use with external FM detectors. It consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the first two stages consists of an emitter-coupled amplifier and an emitter-follower. The operating conditions are selected so that the dc voltage at the

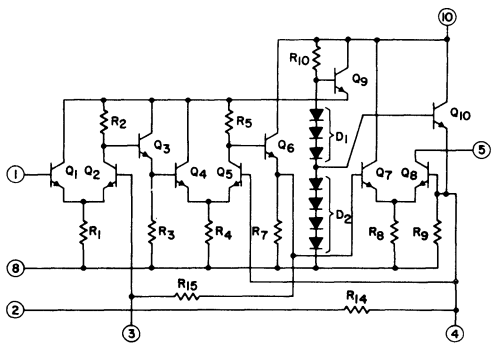


Fig.3 - Schematic diagram of CA3012 integrated-circuit wideband amplifier.

output of each stage is identical to that at the input of the stage. This condition is achieved by operation of the bases of the emitter-coupled differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the collector load resistor. As a result,

the voltage drops across the emitter and collector load resistors are equal, and the collector of the emitter-coupled stage operates at a voltage equal to the base-to-emitter voltage V_{BE} plus the common base potential. The potential at the output of the emitter-follower, therefore, is the same as the common base potential.

At an operating point 3 dB down from the knee of the transfer curve, therefore, the CA3012 requires an input between 400 and 600 microvolts, depending on the ratio-detector design. Fig.4 shows the use of two CA3012 units in a 10.7-MHz if-amplifier strip. A double-tuned filter that has a voltage insertion loss of 8 dB is located between the two CA3012 units to provide a filter input of approximately 1000 microvolts (at terminal 5 of the first CA3012). For an if-strip sensitivity of 4 microvolts, a gain of 48 dB is required. However, if the CA3012 used has a load impedance of 1200 ohms, the available gain is 65 dB, or approximately 17 dB more than required. The extra gain is not wasted, but drives the second CA3012 harder, causing it to limit so that its gain is reduced by approximately 17 dB.

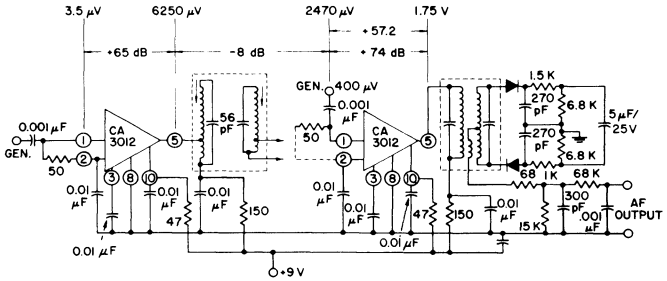


Fig.4 - 10.7-MHz if-amplifier strip using CA3012 integrated circuit.

Fig.5 shows the selectivity of the double-tuned interstage filter. The 3-dB bandwidth is 200 kHz at an input of 10 microvolts and 240 kHz at inputs from 500 microvolts to 0.5 volt. The coefficient of critical coupling is approximately 0.5 at 10 microvolts and increases to 1.0 but still maintains good phase response. The double-tuned filter should be coupled capacitance-aiding to avoid a nearly in-phase over-all relationship. Otherwise, bypassing of terminal 10 and the ratio-detector primary becomes critical and over-all stability is impaired.

The connection of the FM front end to the integrated-circuit if strip must provide good selectivity and good phase response. A double-tuned filter is not suitable from the standpoint of selectivity. An actual IHFM* receiver selectivity between 35 and 40 dB is practical and does not impose too much burden on alignment. Because IHFM selectivity includes other factors than passband, a combined filter design that provides second-channel attenuation between 52 and 60 dB becomes imperative.

Investigation of various types of inductance-capacitance filters indicates the use of a triple-tuned type to form the major lumped selectivity of the FM receiver. Fig.6 shows the response curve and two configurations for such a filter. Economy and ease of alignment are the major features in this approach.

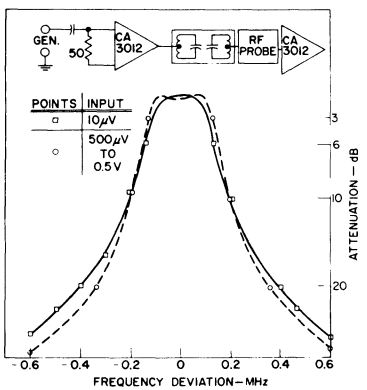


Fig.5 - Selectivity curve for double-tuned interstage filter.

The triple-tuned filter, which is located between the mixer and the first integrated circuit, may have a voltage insertion loss of 33 dB, depending on the desired gain distribution. The power insertion loss of the filter, which is between 12 and 17 dB, is the loss that contributes to if noise. If the primary impedance is reduced to provide a lower voltage insertion loss, the front-end gain is decreased by a corresponding amount. Stability criteria must be the deciding factor in impedance and gain distribution.

* Institute of High-Fidelity Manufacturers.

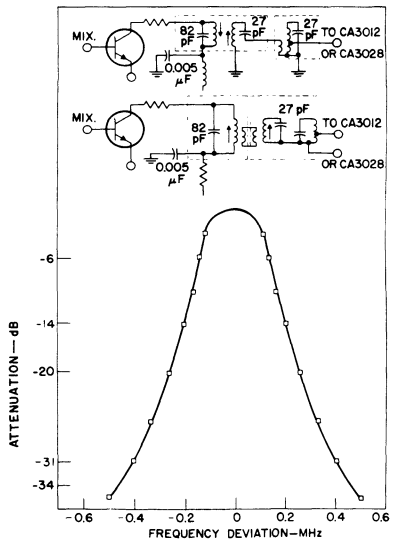


Fig.6 - Configurations and response curve for triple-tuned interstage filter.

Most FM front ends come equipped with a double-tuned 10.7-MHz if transformer in which a secondary high-impedance winding is brought out capacitively unterminated and non-polarized with respect to ground. This configuration does not lend itself readily to optimum skirt selectivity (form factor) when connected with an additional single-tuned transformer to form a triple-tuned filter. Most effective use of the existing front-end filter is accomplished by the addition of another double-tuned filter, such as those shown in Fig.7. Either

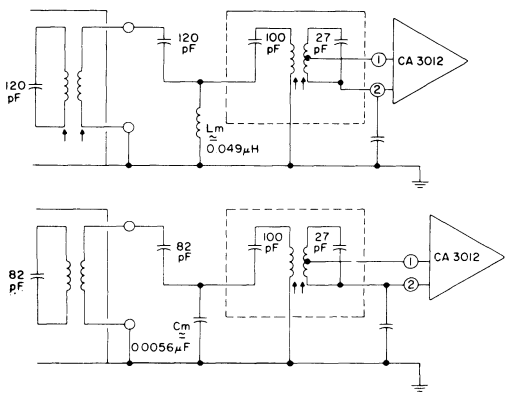


Fig.7 - Configurations of two quadruple-tuned interstage filters.

bottom inductance or capacitance coupling can be used. Voltage insertion losses from 18 dB to 26 dB can be expected. Fig.8 shows the response curve obtained

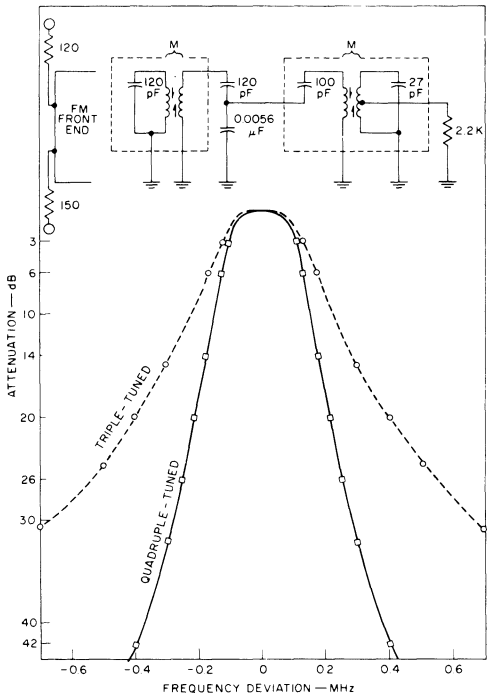


Fig.8 - Response curve obtained with quadruple-tuned filter.

with a quadruple-tuned interstage filter. The per-cent coupling between filters and the coupling mode must be determined on the basis of over-all stability and performance.

It may be appropriate to consider briefly the noise associated with high-insertion-loss filters. Over-all receiver noise F is calculated as follows:

$$F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2}$$

where F_1, F_2, and F_3 are the noise figures of the first (rf), second (mixer), and third (if) stages, respectively; and G_1 and G_2 are the power gains of the first and second stages. If a value of 27 dB is assumed for the if noise figure F_3 (filter plus integrated circuit), 10 dB for the mixer noise figure, and 30 dB for mixer power gain, the effect of if noise on mixer noise is determined as follows:

$$F_2' = F_2 + \frac{F_3-1}{G_2} = 10 + \frac{27-1}{1000} = 10.026 \text{ dB}$$

If the rf stage is assumed to have a power gain of 15 dB and a noise figure of 5 dB, total receiver noise is then determined as follows:

$$F = F_1 + \frac{F_2 - 1}{G_1} = 5 + \frac{10.87-1}{31.7} = 5.285 \text{ dB}$$

These calculations show that the power gain of the rf-amplifier stage overrides both if noise and mixer noise. A minimum power gain of 10 dB is advisable.

The use of a tuning capacitance of 82 picofarads in the collector circuit of the mixer stage provides a loaded primary impedance of approximately 10,000 ohms and eliminates the need for a tap. The 27-picofarad tuning capacitances that comprise the other poles of this filter could be reduced to obtain more favorable loaded-to-unloaded-Q ratios without use of additional resistor loading. The choice of 27 picofarads was based primarily on circuit stability considerations.

Fig.9 shows one type of complete integrated-circuit if strip, and Fig.10 shows the accompanying voltage gains and impedances. Values are given for two levels of mixer output impedance. All other impedance levels shown have exhibited good stability. Over-all performance of the circuit is illustrated in Fig.11.

Capture ratio, which was measured at various levels, varies from 5 dB at 2 microvolts to 1.2 dB above 500 microvolts. With careful adjustment, values as low as 0.8 dB can be obtained. The selectivity curve for the integrated circuit if strip is shown in Fig.12. Over-all selectivity for a given ratio detector and the if strip is shown in Fig.13. Some distributed-selectivity receivers have very little second-channel selectivity at an antenna input of 2000 microvolts. The points marked in Fig.13 show such selectivity for several antenna input levels.

Fig.14 shows an if strip that combines high gain per package and the single-stage-per-package approach. CA3012 and CA3028 integrated circuits are used in a differential-mode connection. An if sensitivity of 15 microvolts can be obtained with this if strip.

If discrete circuits are directly replaced by single differential integrated-circuit amplifiers, a minimum of if transformer and printed-circuit-board redesign is required. Values of voltage gain and impedance are indicated on the block diagram in Fig.15. All three double-tuned transformers are made symmetrical with respect to primary and secondary windings and taps.

Because the single- or double-tuned circuit used between the mixer and the if strip has inherently less

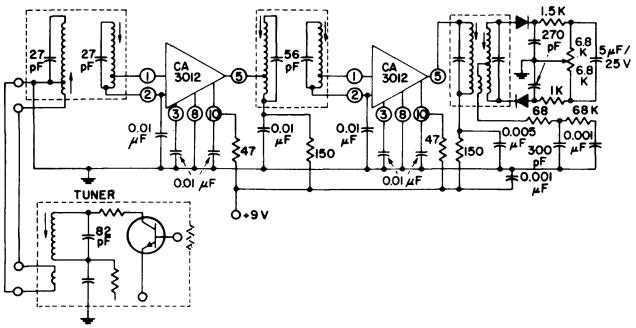


Fig.9 - Complete 10.7-MHz if-amplifier strip using two CA3012 integrated circuits.

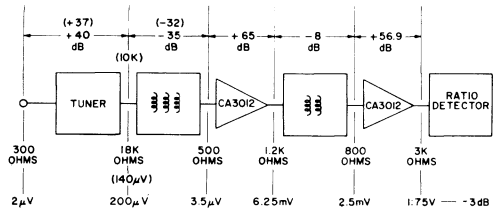


Fig.10 - Voltage gain and impedance values for if-amplifier strip of Fig.7.

insertion loss than a triple-tuned input filter, the input required is 20 instead of 3.5 microvolts. All three double-tuned if transformers have an insertion loss of 6 dB and a 3-dB bandwidth of 280 to 300 kHz. The ratio-detector primary impedance dictates the stage gain of 36 dB for the last integrated circuit. Each of the remaining three stages has a gain of 21.5 dB, for the total required gain of 100 dB. The impedance required for the desired stage gain was calculated to be 660 ohms for both the primary and secondary windings of the if transformers.

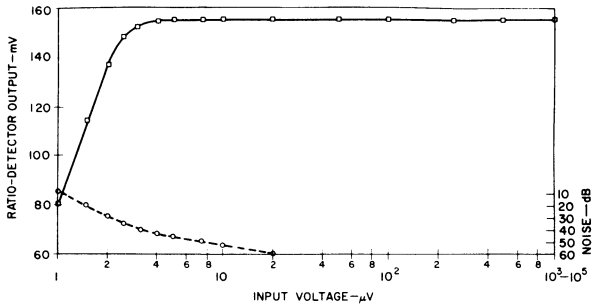


Fig.11 - Performance curves for if-amplifier strip of Fig.7.

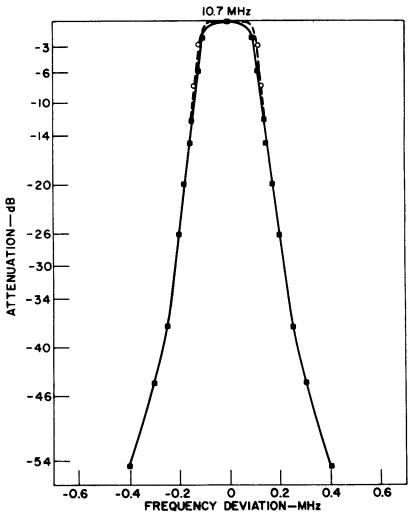


Fig.12 - Selectivity curve for if-amplifier strip of Fig.7.

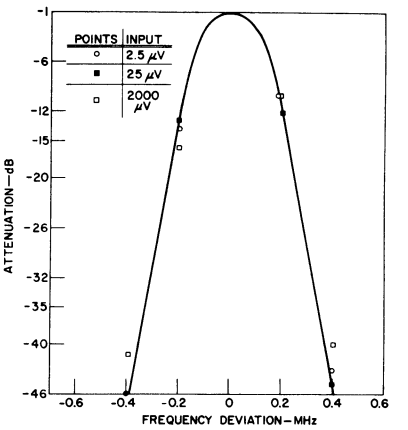


Fig.13 - Measured over-all selectivity curve for if-amplifier strip of Fig.7 and a given ratio detector.

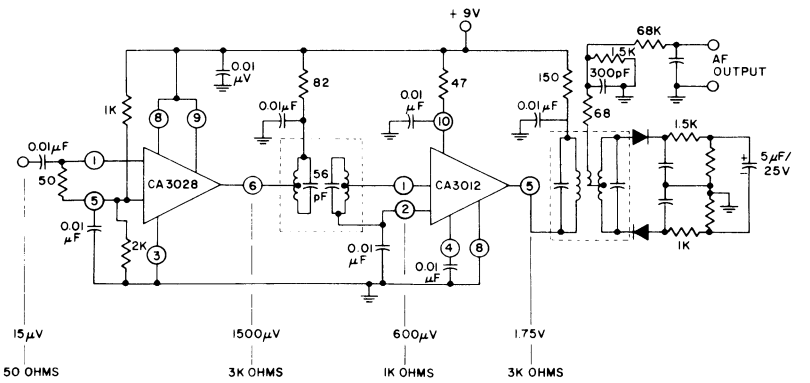


Fig.14 - IF-amplifier strip using CA3028 and CA3012 integrated circuits.

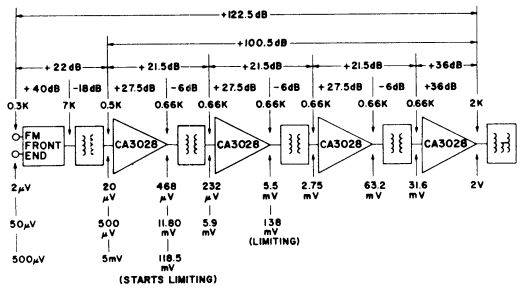


Fig.15 - Voltage gain and impedance values for if-amplifier strip of Fig.12.

With inputs from 20 to 200 microvolts, second-channel selectivity as high as 52 to 59 dB can be attained for three double-tuned and four double-tuned filters, respectively, for a 3-dB bandwidth of 196 kHz. For higher inputs, the same deterioration of selectivity occurs as that experienced with discrete circuits, as shown in Fig.16.

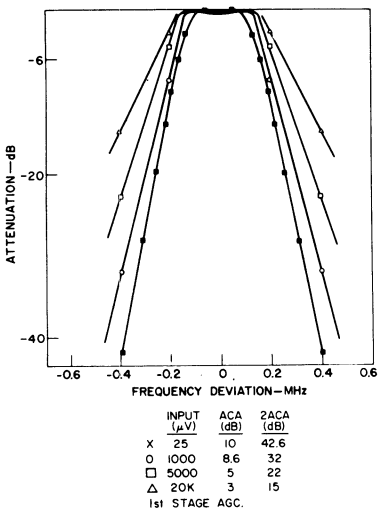


Fig.16 - Selectivity curves for discrete-component if strip using six double-tuned filters.

Several receivers incorporating the if strips shown have been field-tested in areas of 200-kHz station separation, where a weak station was sandwiched between two strong stations. The weak station was received without interference, as compared to the performance of other high-quality FM receivers fabricated with discrete-component if circuits, where lack of selectivity marred reception.

Conclusions

The preceding discussion has shown that the simplest approach to the use of integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

This approach, however, is not the best for cost performance in the long run. The single stage of gain is most difficult to justify economically when a single transistor stage is replaced with a single integrated-circuit package. The boundary condition for such an approach is that ultimately the cost of fabricating a package containing three transistors and three resistors (a typical complement for a differential-amplifier stage) must be the same as that of the one transistor the stage replaces.

Approaches to FM if stages which use the high-gain-per-package concept achieve the excellent AM rejection of differential amplifiers, as well as superior adjacent-channel attenuation, because more gain is inserted between the selectivity elements. From a performance point of view, this approach is superior to both discrete-stage and individually tuned integrated-circuit if strips.

From the point of view of cost, this approach has better possibilities because two packages are equivalent to four single stages of gain (four integrated-circuit packages). This approach results in maximum utilization of present-day monolithic integrated-circuit technology, and is closer to the optimum FM if amplifier shown in Fig.17.

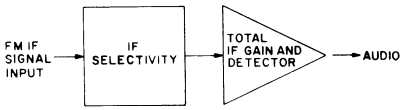


Fig.17 - Optimum FM if-amplifier configuration.

Power-Supply Considerations For CA3041 and CA3042 Integrated Circuits

by
J. H. Sundburg

The RCA CA3041 and CA3042 integrated circuits are designed for use as a major subsystem in FM receivers or the sound section of television receivers. In such applications, each circuit can provide if amplification and limiting, FM detection, and audio preamplification. These units, shown schematically in Fig. 1, offer exceptional versatility in circuit design because the wideband if amplifier/limiter section, the FM detector section, and the audio preamplifier/driver section can be used independent of each other. The dc operating voltage for the integrated circuits, applied at terminal 14, is usually provided from the external supply through a series dropping resistor. The CA3041 and CA3042 include Zener-diode-regulated power supplies that provide proper operating voltages to the various circuit stages independent of external power-supply considerations.

The shunt regulation provided by Zener diodes Z_2 and Z_3 stabilizes circuit voltages, but may also cause wide variations in the dissipation on the integrated-circuit chip, depending upon power-supply and device variations. The external power supply for CA3041 and CA3042 integrated circuits, therefore, must be carefully designed to insure both that the maximum dissipation rating of the integrated circuit is not exceeded, even under worst-case conditions, and that adequate voltage regulation is provided under all conditions.

This Note provides the data required to design an adequate power supply and describes a simple procedure that may be used to determine the value and tolerance of the required series dropping resistor when supply voltages differ from those specified in the published data for the CA3041 and CA3042 integrated circuits.

General Considerations

The main variables to be considered in determination of the external series dropping resistors are as follows: (1) power-supply voltage and tolerance, (2) maximum allowable integrated-circuit dissipation at the maximum ambient temperature, and (3) variations in integrated-circuit characteristics.

When the CA3041 or CA3042 is operated at high power-supply voltages, the integrated-circuit dissipation does not vary widely; operation of the circuit at higher temperatures is then permitted. Under such conditions, however, total system dissipation is increased and a higher power rating is required for the series dropping resistor.

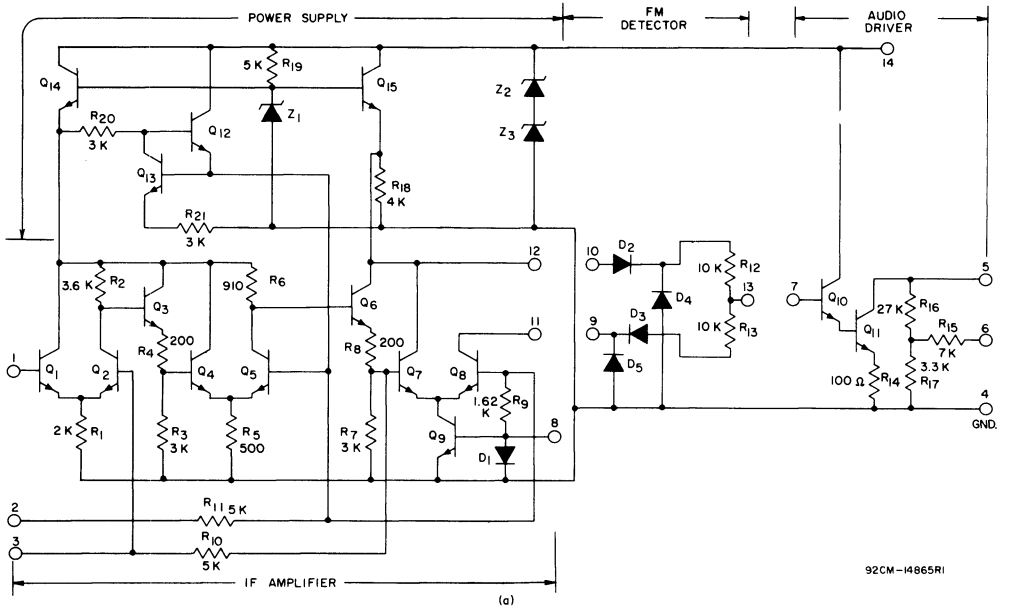


Fig. 1 — Schematic diagrams of (a) the CA3041 and (b) the CA3042 integrated circuits.

When low-voltage supplies are used, the power rating of the series resistor may be reduced, but a decrease in the temperature range of the integrated circuit also results.

The maximum value of the series dropping resistor R_S is the value for which a Zener current of 1 milliampere is allowed to flow under worst-case conditions, i.e., under conditions of low line voltage, high Zener voltage, and high integrated-circuit current drain. The minimum value of the resistor R_S is the value for which the worst-case dissipation is limited to that defined by the maximum ambient temperature and the circuit derating curve shown in Fig. 2.

The procedure used to define the resistor R_S differs slightly for the two types of integrated circuits. A few additional steps are required for the CA3041 because the dissipation of this circuit is a function of the load resistor of the audio-amplifier stage (this resistor is not used in CA3042). Tables I and II outline the procedure used to determine the resistor R_S for the CA3042 and CA3041, respectively. The voltage-current curves for the CA3041 and CA3042 also differ because of the difference in the audio-amplifier stage of these circuits.

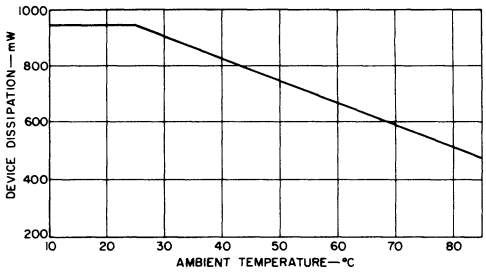


Fig. 2 — Maximum device dissipation derating curve for the CA3041 and CA3042 integrated circuits.

TABLE I — PROCEDURE FOR FINDING THE SERIES DROPPING RESISTOR R_S FOR THE CA3042
(Points referred to in the procedure are shown on Fig. 4.)

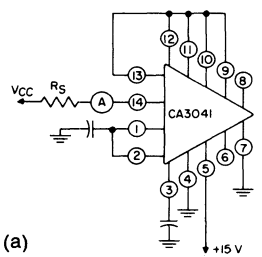
		EXAMPLE
1.	Define nominal supply voltage and tolerance, minimum and maximum supply voltage, and maximum ambient temperature	$V_S = 40\ V \pm 10\%$ $V_{S\ MIN} = 36\ V.$ $V_{S\ MAX} = 44\ V.$ $T_{A\ MAX} = 75°C$
2.	Compute maximum value of R_s using voltage and current at point X $R_{S\ MAX} = \frac{V_{s\ MIN} - V_x}{I_x}$	$R_{S\ MAX} = \frac{36 - 11.55}{21} = 1.16\ K\Omega$
3.	Assume resistor tolerance, and compute nominal value of R_s $R_{s\ NOM} = R_{s\ MAX}$ (1 − % Tolerance)	Tolerance = 10% $R_{s\ NOM} = 1.16 \times 0.9 = 1.05\ K\Omega$
	FIND NEXT LOWER STANDARD VALUE	1 KΩ
4.	Construct the worst-case load line using the minimum value of R_s and the maximum value of V_s. Two points are required. Because the voltage scale is incomplete, find the current at 10 volts and 13 volts. $I_{10} = \frac{V_{S\ MAX} - 10}{R_{S\ MIN}}$ $\quad I_{13} = \frac{V_{S\ MAX} - 13}{R_{S\ MIN}}$ Connect Points 10, I_{10} (F) and 13, I_{13} (G)	$I_{10} = \frac{44 - 10}{0.9\ K\Omega} = 36.8\ mA$ $I_{13} = \frac{44 - 13}{0.9\ K\Omega} = 34.5\ mA$
5.	Compute the worst-case dissipation. This condition occurs at the point at which the load line F-G intersects either curve A or curve D. Multiply the voltage and current at each intersection, and use the higher value.	$P_1 = 36 \times 11.1 = 400\ mW$ $P_2 = 34.8 \times 12.4 = 432\ mW$ $P_{MAX} = 432\ mW$
6.	Find the maximum allowable temperature permitted for P_{MAX} on Fig. 2.	From Fig. 2, $T_{A\ MAX} > 85°C$
7.	If $T_{A\ MAX}$ is greater than the maximum value required, the design is satisfactory.	
8.	If $T_{A\ MAX}$ is less than the maximum value required, go back to step (2) and recompute for a tighter tolerance on R_s, or go back and choose a higher supply voltage.	
9.	Compute the required dissipation rating for R_s. Use $V_{s\ MAX}$, R_{MIN} and the lower of the two values of power calculated in step (5). $P = \frac{V_{S\ MAX}^2}{R_{S\ MIN}} - P\ (\text{from 5})$	$P = \frac{44^2}{900} - 0.400 = 1.75\ \text{watts}$ R_s is a 1 KΩ resistor with a ±10% tolerance

TABLE II — PROCEDURE FOR FINDING THE SERIES DROPPING RESISTOR R_S FOR CA3041
(Points referred to in the procedure are shown on Fig. 5.)

		EXAMPLE
1. *to* 5.	Follow steps 1 through 5 from CA3042 procedure except note that the dissipation does not include the power dissipated in the audio amplifier.	
6.	Select power-supply voltage and nominal operating point for audio amplifier. Note from published data for CA3041 that the ac voltage swing is limited to the range of +1 to +29 volts by saturation effects and breakdown voltage.	Use same supply as before $V_{S\ NOM} = 40$ $V_{S\ MAX} = 44$ $V_{C\ NOM} = 15$ volts (Point N)
7.	Find the audio load resistor R_L $R_L = \frac{V_{S\ NOM} - V_{C\ NOM}}{I_{C\ NOM}}$	$R_L = \frac{40 - 15}{4\ mA} = 6.25\ K$ use nearest 10% resistor, 6.8 K
8.	Find worst-case load line using $V_{S\ MAX}$ and $R_{L\ Min}$ $R_{L\ Min} = R_L\ (1 - \%\ Tolerance)$ Load line intersects $V = 0$ at $I = \frac{V_{S\ MAX}}{R_{L\ MIN}}$ Load line intersects $V = 30$ V at $I = \frac{V_{S\ MAX} - 30}{R_{L\ MIN}}$	$R_{L\ MIN} = 6.8\ K \times .9 = 6.1\ K$ $I = \frac{44}{6.1} = 7.2\ mA$ (Point P) $I = \frac{14}{6.1} = 2.3$ (Point Q)
9.	Compute P_{audio} at point $P_{audio} = I_R \times V_R$	$P_{audio} = 4.7 \times 16 = 75\ mW$,
10. *to* 14.	Add P_{audio} to P_{Max} from Step 5, and proceed with steps 6 through 9 of the CA3042 procedure.	

Voltage-Current Curves

Figs. 3 and 4 show the limiting power-supply condition, together with the test circuit used to determine this condition, for the CA3041 and CA3042 circuits, respectively. For supply-voltage values (at terminal 14) below 10 volts, the Zener diodes Z_2 and Z_3 do not conduct, and the current drain is that of the connected portions of the integrated circuit. The vertical distances between the curves in Figs. 3 and 4 represent the limits of current drawn by the operating portions of the circuit. The current drawn



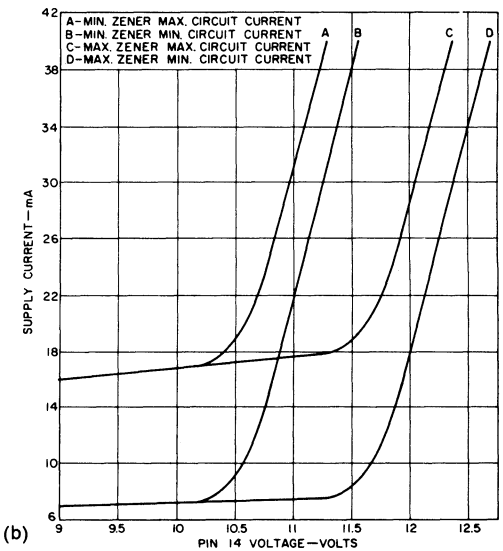


Fig. 3 — Supply current as a function of supply voltage for the CA3041 integrated circuit: (a) test circuit; (b) voltage-current curves.

by the Zener diodes adds to the circuit current at supply voltages (at terminal 14) above 10 volts. The voltage difference between curves A and C at a total drain of 25 milliamperes indicates a tolerance of less than ±5 per cent on the Zener voltage.

The voltage-current curves for the CA3041 and CA3042 differ because the current for the final amplifier stage is drawn from the main dropping resistor in the CA3042 and through an external resistor in the CA3041. Fig. 5 shows the dc voltage-current relationship for the audio-amplifier stage in the CA3041. The stage is self-biased by the 100-kilohm resistor between terminals 6 and 7 so that a unique curve is formed.

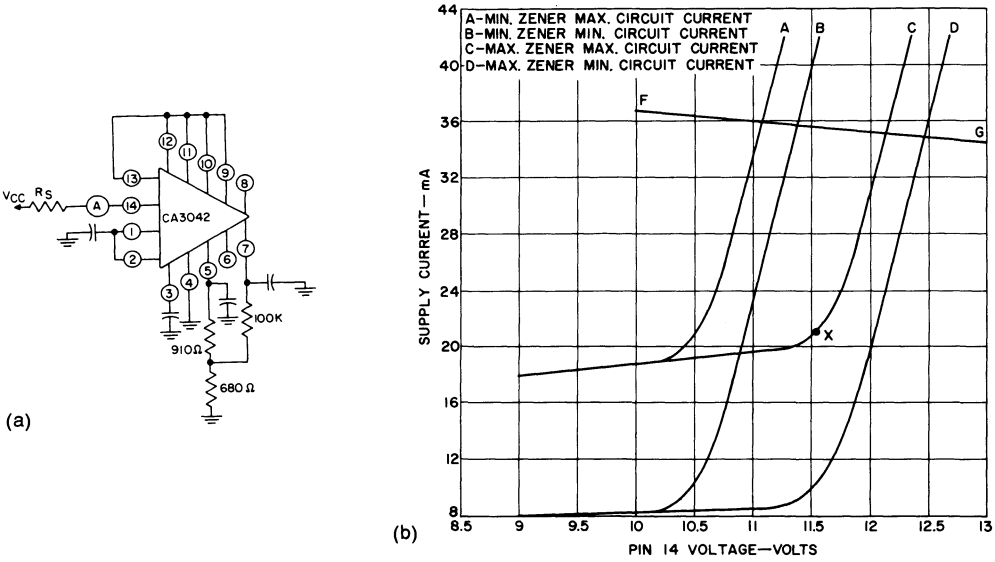


Fig. 4 — Supply current as a function of the supply voltage for the CA3042 integrated circuit: (a) test circuit; (b) voltage-current curves.

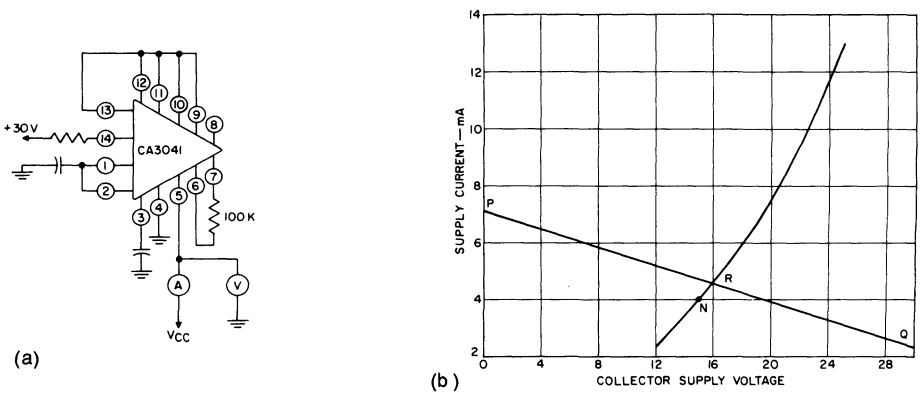


Fig. 5 — Collector characteristic of the audio-amplifier stage of the CA3041 integrated circuit: (a) test circuit; (b) voltage-current curves.

Application of the RCA-CA3044 and CA3044VI Integrated Circuits in Automatic-Fine-Tuning Systems

by

W. M. Austin, H. M. Kleinman, and J. Sundburg

This Note describes the use of the RCA-CA3044 and CA3044V1 integrated circuits as automatic-fine-tuning (AFT) system components and discusses the advantages of integrated circuits in this application. The CA3044V1 is electrically identical to the CA3044, but is supplied with formed leads for easier printed-circuit-board mounting; throughout this Note a reference to the CA3044 implies a similar reference to the CA3044V1.

The RCA-CA3044 is a special-function subsystem integrated circuit that represents a second generation of the AFT integrated circuit, the CA3034, that was designed specifically for frequency-control applications. The CA3044, unlike the CA3034, has an internal zener-regulated power supply that improves performance and reduces system cost. It is designed to replace the CA3034 in similar applications with only minor changes in the system circuit.

Circuit Description and Operation

The schematic diagram of the CA3044 is shown in Fig. 1; the use of the circuit in a typical automatic-fine-tuning (AFT) system for a color television receiver is shown in Fig. 2. In such a system, the CA3044 provides all of the signal-processing components needed (with the exception of the tuned phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The other components of the system provide signal coupling and power-supply decoupling as required for proper signal processing in the video intermediate-frequency range.

The CA3044 integrated circuit can be considered as the combination of four functional blocks: a limiter-amplifier, a balanced detector, a differential amplifier, and a regulator. The 45-MHz limiter-amplifier composed of Q_1 and Q_2 is a differential amplifier that supplies a

peak-to-peak output current of approximately 4 milliamperes for input levels above the limiting threshold. The use of a load impedance which does not exceed 2000 ohms guarantees an excellent limiting characteristic and eliminates detuning effects caused by saturation of the amplifier under worst-case conditions. In the system shown in Fig. 2, the load impedance at the center frequency is about 1800 ohms.

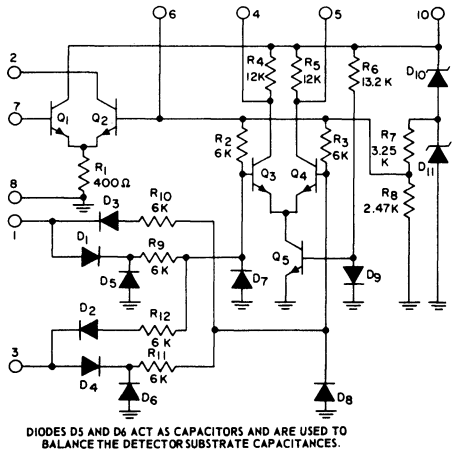


Fig. 1 - Schematic diagram of the CA3044 and CA3044VI.

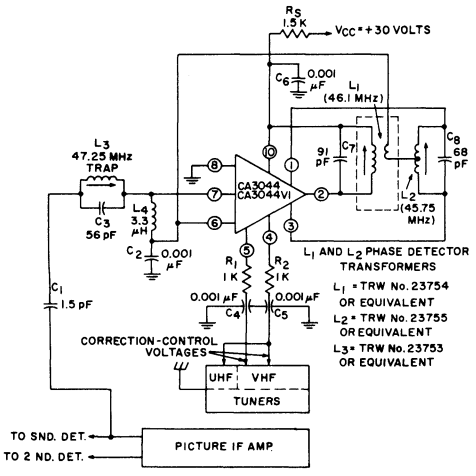


Fig. 2 - System diagram of a typical automatic-fine-tuning (AFT) application showing the CA3044 or CA3044VI in use in a color-TV receiver.

The diode matrix composed of D_1, D_2, D_3, and D_4 constitutes a balanced detector that converts the output of the phase transformer to a filtered dc signal. Diodes D_1 through D_4 perform the detection function. Diodes D_7 and D_8 are always reverse-biased and serve as capacitors; they filter the output of the detector in conjunction with R_9 through R_{12}. Diodes D_5 and D_6 are included to balance the parasitic diodes that exist between the cathodes of D_2 and D_3 and the substrate.

Transistors Q_3, Q_4, and Q_5 form a constant-current driven differential amplifier that is directly coupled to the output of the detector. The amplifier contributes greatly to the high sensitivity of the system and, in addition, provides sufficient power to allow the use of a low-cost tuning element. The output impedance at either output of the amplifier is approximately 12,000 ohms.

The zener-diode regulator comprising D_{10} and D_{11} provides the regulation necessary for a differential post-detection amplifier output that is both stable and independent of temperature and power-supply variations. The junction of D_{10} and D_{11} is connected to a bias divider network that assures correct base bias on both differential-amplifier pairs.

During normal operation, the proper dc bias for terminals 1, 3, and 7 of the CA3044 is supplied through terminal 6 and external rf coils, as shown in Fig. 2. RF bypassing is required both for terminal 6 and for terminal 10, which is connected through the primary winding of the detector transformer to terminal 2.

Operating Characteristics

The CA3044 is designed to operate from supply voltages greater than the zener regulating voltage; because the zener-diode voltage varies from 10.5 to 11.9 volts at the 14-milliampere current-drain level, the supply voltage should be greater than 15 volts for proper regulation and circuit operation. The effect of all component and power-supply tolerances on zener regulating current must be taken into account in calculation of the value of the series regulating resistor R_S shown at the top of Fig. 2. In the typical circuit shown in Fig. 2, power is supplied to terminal 10 of the CA3044 from a +30-volt supply through a 1500-ohm series dropping resistor. The recommended value of R_S can be determined for other supply conditions by use of the curves in Fig. 3, which show current at terminal 10 as a function of supply voltage.* An R_S load line may be drawn through the safe operating area to show extremes of voltage and current for normal variations in product. Safe operation with proper regulation is achieved on any load line that avoids the lower cross-hatched area and does not exceed the allowable maximum dissipation as determined for a given ambient temperature. The cross-hatched area represents voltage-regulation dropout resulting from an insufficient amount of zener-diode current.

* This type of curve is described in RCA Application Note ICAN-5765, "Power-Supply Considerations for CA-3041 and CA-3042 Integrated Circuits."

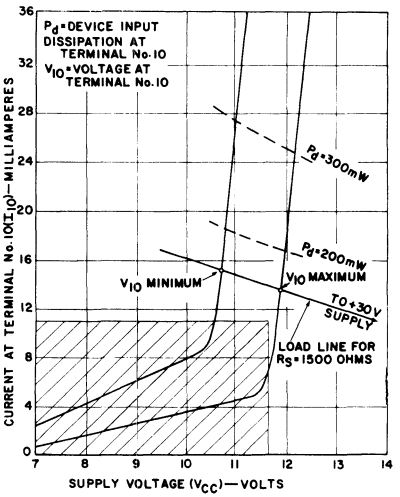


Fig.3 - Curves for determining the zener-diode regulating voltage at terminal 10.

The maximum value of R_S is determined by construction of a load line from the minimum supply voltage (V_{CC}) to the upper right corner of the cross-hatched area. The largest standard resistor having a maximum value (including tolerance) smaller than the slope of this line is selected. Dissipation under the worst-case conditions of minimum R_S and maximum V_{CC} must then be checked to assure compliance with the maximum device ratings.

The dissipation rating of the CA3044 is 830 milliwatts at an ambient temperature of 25°C. At ambient temperatures above 25°C, this maximum value must be derated by a factor of 5.6 milliwatts per degree. Fig.4 shows the permissible dissipation of the CA3044 as a function of ambient temperature. The worst-case dissipation may occur at either a voltage or a current maximum. The equation for total dissipation P_d in the CA3044 is

$$P_d = \frac{(V_{CC} - V_{10})}{R_S} \quad V_{10}$$

where V_{10} is the voltage at terminal 10 and V_{CC} is the power-supply voltage supplied through the series dropping resistor R_S to terminal 10. The permissible ambient-temperature operating range for the CA3044 is - 55°C to +125°C.

Dynamic Performance

The system diagram of Fig.2 shows the CA3044 in its function as rf amplifier, frequency discriminator, and post-detection differential dc amplifier. The circuit shown is a portion of a color television receiver in which critical tuning is essential because of the presence of the color subcarrier and its sidebands. The

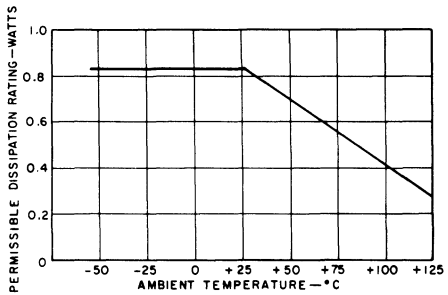


Fig.4 - Dissipation rating of the CA3044 and CA3044VI as a function of ambient temperature.

CA3044 AFT system provides a uniform and accurate tuning reference. When the correction voltage developed at terminals 4 and 5 of the CA3044 is sufficient, the system locks on the picture-carrier intermediate frequency and holds the tuner oscillator within ±25 kHz of the picture carrier so that a high-quality picture is produced at all times. Operation within such a narrow band of oscillator frequencies represents a color-reference deviation of less than 5 per cent from the ±500-kHz color-subcarrier sidebands; this deviation is in general far smaller than the amplitude and phase-change errors that are introduced by other receiver and transmitter functions.

The system shown in Fig.2 can be used in a typical color receiver. The sampling connection from the picture-if amplifier to the AFT circuit is made from the output of the last if stage directly to the input of the CA3044 rf amplifier. The loading effect of the AFT-system coupling circuit on the picture-if amplifier is negligible and does not distort the if response. Unless provision has been made to trap out the adjacent-channel sound carrier elsewhere in the circuit, such action must be taken at the input to the CA3044. Trapping of the adjacent-channel sound carrier is essential because it may have sufficient amplitude to cause limiting at the rf amplifier/limiter stage of the CA3044. The trapping circuit, composed of L_3 and C_3 in Fig.2, also helps to peak the picture carrier at 45.75 MHz while trapping the adjacent-channel sound carrier at 47.25 MHz. To compensate for an if response that places the picture carrier at the 50-per-cent point on the if slope, the input trap should be adjusted to peak the response above 45.75 MHz at the input to the CA3044.

Proper dc biasing of the amplifier/limiter stage composed of Q_1 and Q_2 requires that a small choke, L_4, be used to couple terminal 6 to terminal 7. The common bias connection at terminal 6 is bypassed with a 0.001-microfarad disc capacitor. No form of external dc connection should be made to either terminal 6 or terminal 7.

The output load on the differential amplifier consists of the impedance of the phase-shift transformer

comprising L_1 and L_2. The differential-amplifier stage assures symmetrical limiting above 100 millivolts at the input of terminal 7. The primary of the phase-shift transformer is typically tuned to 46.1 MHz as an additional error-correction device to help peak the picture carrier at 45.75 MHz. The secondary is tuned to 45.75 MHz and symmetrically drives the double-balanced detector comprising diodes D_1, D_2, D_3, and D_4. The detector diodes D_1 through D_4 minimize frequency shifting by symmetrically loading the discriminator transformer. Symmetrical loading is assured by diodes D_5 and D_6, which are used as capacitors to balance the inherent substrate capacitances associated with D_2 and D_3.

The error signal detected by the double-balanced detector is filtered by the 6000-ohm resistors R_9, R_{10}, R_{11}, and R_{12} and diodes D_7 and D_8 at the inputs to the differential output amplifier composed of Q_3 and Q_4. The differential output amplifier is compensated for all temperature-change effects including those of the zener-diode regulator. In the absence of an error signal, output terminals 4 and 5 are at a dc level of 6.5 volts; in mistuning or frequency correction, the output level varies from 33 to 85 per cent of the zener-regulated voltage over the ±25-kHz limits. Fig.5 shows the typical narrow-band response of the system shown in Fig.2; Fig.6 shows the wide-band response. The curves shown are characteristic of the Fig.2 circuit for an input rf signal level of 200 millivolts rms at terminal 7. Both narrow- and wide-band response characteristics are a function of the CA3044 limiting level. The narrow-band crossover slope decreases and the wide-band response becomes narrow as the signal level decreases.

The reference levels(A, B, C, and D) indicated on the curves of Fig.5 and 6 refer to the narrow- and wide-band control points expressed as a percentage of the zener reference voltage at terminal 10. References A and B are narrow-band (±25-kHz) control points at 85

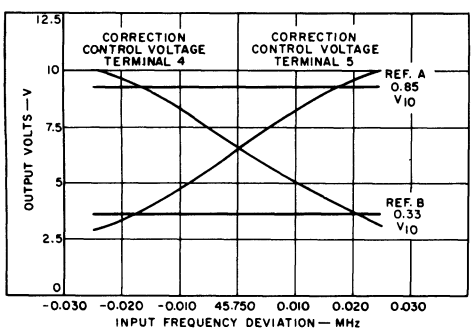


Fig.5 - Typical narrow-band dynamic control voltage characteristics.

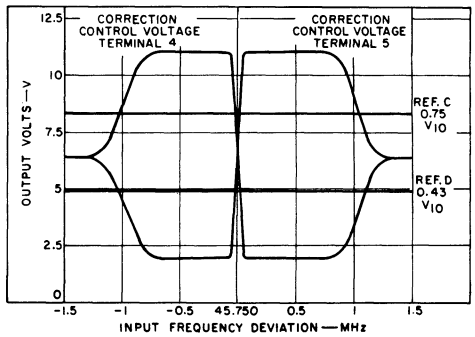


Fig.6 - Typical wide-band dynamic control voltage characteristics.

and 33 per cent of the terminal 10 reference voltage, while references C and D are the wide-band (±0.9-MHz) control points at 75 and 43 per cent of the same voltage. The dynamically controlled test circuit for measuring performance in the recommended application circuit is similar to that circuit and is shown in Fig.7. The correction voltages from terminals 4 and 5 are applied to

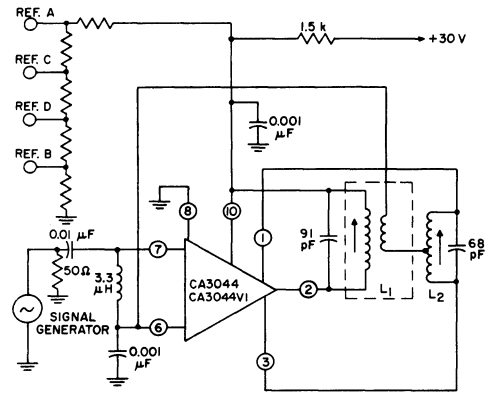


Fig.7 - Correction voltage test circuit for the CA3044 and CA3044VI.

the tuning elements of the voltage-controlled oscillator portion of the uhf and vhf tuners. These voltages may be used single-ended and of either phase-polarity for uhf oscillator control. The vhf oscillator may be controlled with a push-pull output to assure attainment of maximum tuning range. The channel-tuning defeat-switch function is normally accomplished by shorting the control-voltage terminals 4 and 5 together. For fil-

tering purposes and to protect the integrated circuit, it is best to include a shunt capacitor and series resistor between the tuning elements and terminals 4 and 5; in Fig. 2, 1000-ohm resistors and 0.001-microfarad feed-through capacitors are used.

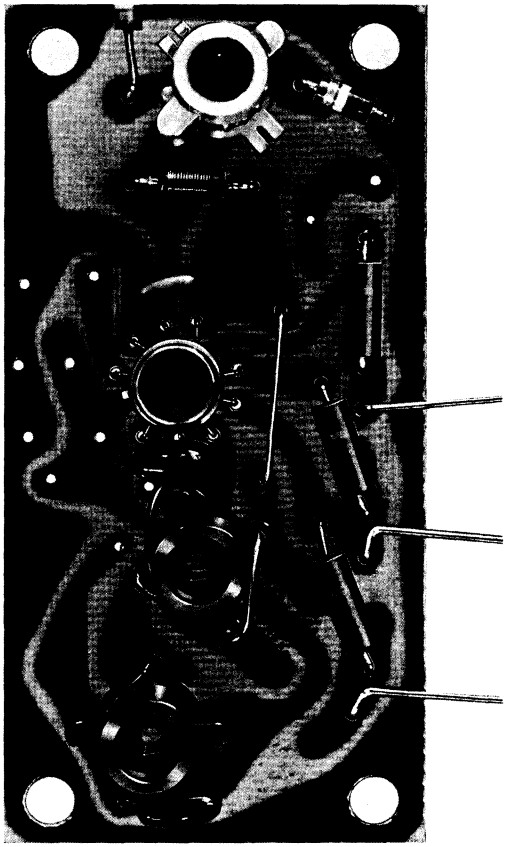


Fig. 8 - Printed circuit board containing the circuit of Fig. 2.

Construction

Fig. 8 shows a circuit board containing the circuit of Fig. 2; Fig. 9 is an unobstructed view of the printed-circuit board used. The location and orientation of the discriminator transformer coils affect the over-all response of the circuit; therefore, their placement should be given the greatest attention. Because the metal pattern must be taken into account in component placement, some experimentation may be necessary to achieve the best results. It is recommended that the circuit be shielded to prevent radiation of the 45.75-MHz signal.

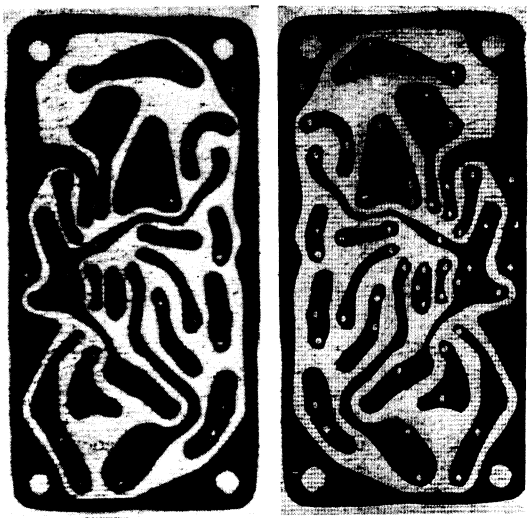


Fig. 9 - An unobstructed view of the top (a) and bottom (b) of the printed circuit board used in Fig. 8.

The circuit described in this Note has been duplicated many times with both hand-made and commercial coils. Alignment has always been rapid and positive and the performance extremely uniform.

Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits

by

L. Kaplan

This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

Types of Volume Controls

Fig.1 shows a conventional or "losser" type of volume control that is susceptible to hum and noise. When the input impedance of the amplifier is high, the input voltage E_i and the output voltage E_o depend on the voltage division between resistances R_1 and R_2. The gain of the amplifier is constant, but the input signal is increased or decreased according to the potentiometer rotation.

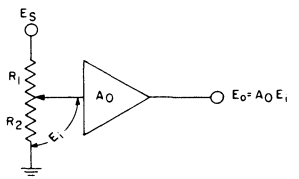


Fig.1 - Conventional volume-control circuit.

Fig.2 shows the basic variable-feedback volume control.* When the wiper arm of the potentiometer is close to the input terminal, which has a signal input E_S, the gain of the system is essentially the open-loop gain A_O. As the wiper arm approaches the output terminal, the gain is reduced to a closed-loop value A_C according to the following formula:

$$A_C = \frac{A_O}{1 + \beta A_O}$$

where β is the feedback factor.

* RCA Linear Integrated Circuits, Technical Series IC-41, "Integrated-Circuit Operational-Amplifier Configuration," pp.73-112, RCA Electronic Components, Harrison, N.J.

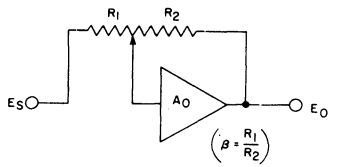


Fig.2 - A variable-feedback volume-control circuit.

Feedback Control

Fig.3 shows the equivalent circuit of a feedback control. Gain control in this circuit is provided by the potentiometer, which varies according to the resistance ratio of R_S and R_f. The system gain E_O/E_S for this circuit can be described by the following equation:

$$\frac{E_O}{E_S} = \frac{G_S\left(1-\frac{g_m}{G_f}\right)}{\left(G_S+G_i\right)\left(1+\frac{G_L}{G_f}\right)+g_m+G_L} \qquad (1)$$

where E_O and E_S are the output and input signal levels, respectively; g_m is the transconductance of the amplifier device; and G_S, G_f, G_i, and G_L are the conductances of the source, feedback, input, and load resistances, respectively.

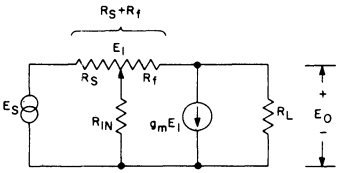


Fig.3 - Equivalent circuit of a feedback volume control.

When the control is set for maximum gain ($R_S = 0$; $G_S = \infty$), the system reduces to the following expression:

$$\frac{E_o}{E_s} = \frac{G_f - g_m}{G_f + G_L} = \frac{R_L - g_m R_f R_L}{R_L + R_f} \qquad (2)$$

At the minimum-gain setting, the gain of the system is given by

$$\frac{E_o}{E_s} = \frac{1}{1+\frac{1}{G_S}\left(G_i+G_L+g_m\right)} = \frac{1}{1+R_S\left(\frac{1}{R_i}+\frac{1}{R_L}+g_m\right)} \qquad (3)$$

The resistance R_f of Eq.(2) and the resistance R_S of Eq.(3) are the same because they represent the total resistance of the volume-control potentiometer. If the value of R_f in Eq.(2) is made large with respect to the load resistance R_L, the gain and maximum volume reduce to the familiar expression $g_m R_L$.

Eq.(3) shows that the gain of the system is not zero at the minimum volume setting. For both the RCA-CA3041 and CA3042 integrated circuits, typical values encountered indicate that the expression is dominated by the transconductance g_m. Substitution of typical values in Eq.(3) shows that the minimum-voltage gain of a 0.25-megohm volume control is of the order of 98 dB and 136 dB below the maximum gain for the RCA-CA3041 and CA3042 circuits, respectively, which is well below the normally acceptable residual levels.

Loudness Contouring

A desirable feature of audio systems in which low-frequency overload may be encountered is bass roll-off at high volume levels. The low-frequency overload may result because of limited amplifier power output or an inadequate loudspeaker. In either case, an unpleasant "honking" can be avoided by use of variable low-frequency cut-off. This cut-off is achieved by use of the characteristics of the circuit shown in Fig.3. The input impedance Z_i of the system, as shown in Fig.3, is as follows:

$$Z_i = R_S + \frac{1+G_L R_f}{G_i + G_L + g_m + G_i G_L R_f} \qquad (4)$$

If the total resistance of the volume-control potentiometer is denoted by R_V, the input impedance at minimum volume Z_i (min) is given by

$$Z_i(\text{min}) = R_V + \frac{1}{G_i + G_L + g_m} \approx R_v \qquad (5)$$

At maximum volume, the input impedance Z_i (max) changes to the following expression:

$$Z_i(\text{max}) = \frac{1+G_L R_V}{G_i + G_L + g_m + G_i G_L R_L} \qquad (6)$$

Thus, the input coupling capacitor can be selected to roll off at the desired frequency at maximum volume with assurance that at lower volumes the lower frequencies will be enhanced. With typical device parameter values of the CA3041 or CA3042, the input impedance reduces to approximately 10,000 ohms at maximum volume. When the CA3041 and CA3042 are used in the circuits shown in Figs.4 through 8, the input impedance at minimum volume is essentially the resistance of the volume control used.

Fig.4 shows a diagram of a feedback-type volume-control circuit for the CA3041. This circuit offers enhanced power output and gain as compared to a conventional "losser" type of volume-control-circuit such as that shown in Fig.5. At a carrier frequency of 4.5 MHz, the circuit provides one watt of power output at ±8.5-kHz deviation. In this circuit, the coupling capacitor and the resistor to the grid of the output tube are eliminated. This arrangement offers cost savings because it uses fewer parts and is easier to assemble.

Fig.6 shows a circuit in which the CA3042 is used in a feedback control. The circuit shown in Fig.6 can provide 2 watts of audio power output at ±7-kHz maximum

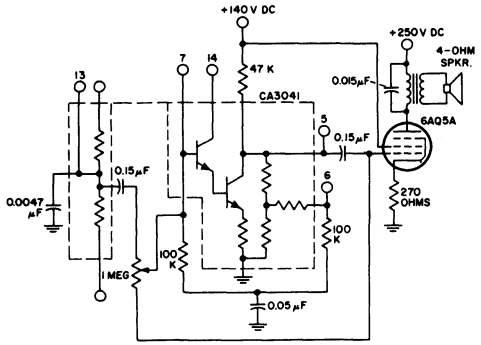


Fig.4 - A feedback volume-control circuit for the RCA-CA3041.

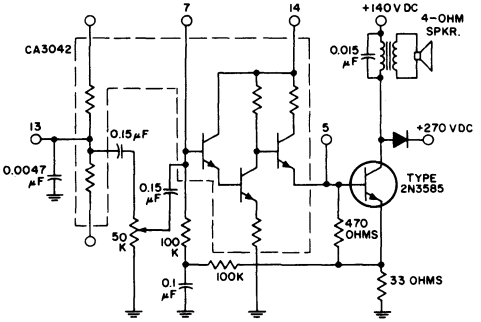


Fig.7 - A conventional volume-control circuit for the RCA-CA3042.

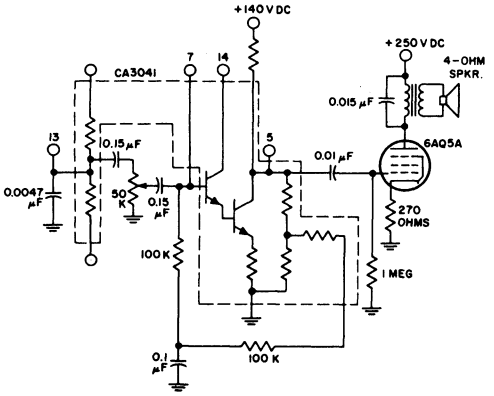


Fig.5 - A conventional volume-control circuit for the RCA-CA3041.

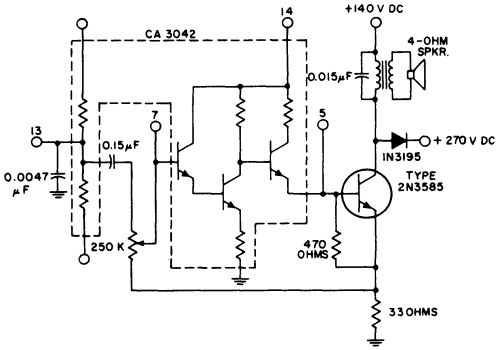


Fig.8 - A low-cost feedback volume-control circuit for the RCA-CA3042.

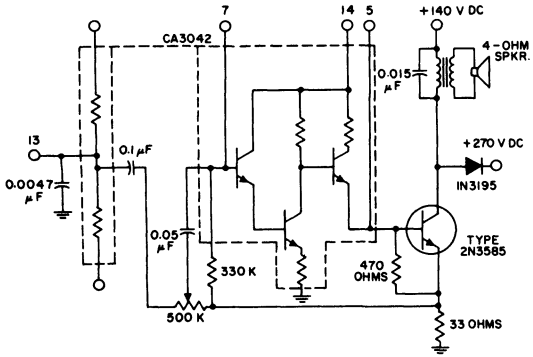


Fig.6 - A feedback volume-control circuit for the RCA-CA3042.

frequency deviation from the 4.5-MHz carrier. This circuit costs less than a conventional circuit such as that shown in Fig.7 because it uses smaller coupling capacitors.

Fig.8 shows a very-low-cost circuit that provides essentially the same performance as the circuit shown in Fig.6. An additional capacitor and resistor are eliminated in this circuit. Although a steady-state current flows through the volume control, it is limited to about 1.5 microamperes under worst-case conditions. Because of the small but finite current flowing through R1, the current shifts in the output transistor as the control is rotated from minimum to maximum. The current deviation is ±6 milliamperes maximum about the nominal value, and the flow is in a direction that reduces current at low volume and increases it at high volume.

Tapers

Because the gain of the system, rather than the input signal, is varied, the volume taper of a feedback

control is characteristically different from that of a conventional "losser" type of control. Therefore, Eq.(1) can be rewritten as follows:

$$\frac{E_o}{E_s} = \frac{1 - a g_m R_v}{1+(1-a)G_i R_v (1+a R_v G_L)+R_v G_L + g_m (1-a)} \quad (7)$$

where the term R_f of Eq.(1) is replaced by $(a R_v)$ and R_s is replaced by $(1-a)R_v$. The gain then becomes a function of the term a, which expresses the taper of the control. Curves of this equation for various tapers are shown in Fig.9.

The exponential functions of the taper factor, a, actually define the familiar logarithmic tapers; however, they are arranged counterclockwise so that, as the control is rotated clockwise, the resistance increases very rapidly at first and then more slowly toward maximum resistance. A linear taper (bottom curve of Fig.9) exhibits almost a step-function response, while the parabolic taper is slightly smoother. Clockwise log tapers fall below the linear-taper curve, and are thus totally unacceptable. The controls which are probably most satisfactory are those which correspond to very-low-percentage counterclockwise log tapers.*

* The percentage taper is calculated as follows:

$$\frac{R_{(\text{measured from start of control to wiper arm})}}{\text{Total resistance}} \times 100,$$

The measurement is taken at 50-per-cent rotation of the control.

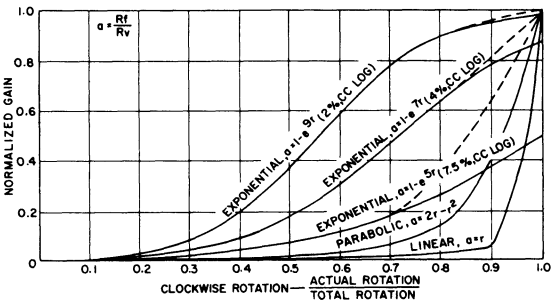


Fig.9 - Gain as a function of rotation for various types of potentiometers.

An IC for AM Radio Applications

by
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RCA Solid State Division
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An integrated circuit intended to be used in AM radio applications can assume many forms depending on the class of service in which it is to be used. The RCA-CA3088E is designed for use in high-quality AM superheterodyne receivers. It provides the basic functions of signal conversion, if amplification, detection, and audio preamplification sufficient to drive a separate power amplifier. Auxiliary functions supplied are: a supply-voltage regulator, internal agc for the first if amplifier, agc voltage for an optional external rf stage, and an amplified signal to drive a tuning-meter output. This device is housed in a 16-lead dual-in-line plastic package.

While the circuit design is intended for use in commercial AM broadcast receivers, it is equally suited for use in most AM receiver applications up to a frequency of 30 MHz. In addition, since most functions are externally accessible this device is also a general-purpose amplifier array. The possible number and variety of uses of the CA3088E are largely a function of the needs and imagination of the designer.

INTEGRATED CIRCUIT DESCRIPTION

The schematic diagram of the RCA-CA3088E is shown in Fig. 1. The correspondence of terminals to functional section within the device is shown in Table I. The various stages are designated in terms of AM-radio functions because the primary functions of the device are so intended; the AM-radio terminology is continued throughout the paper for the sake of continuity.

The heart of this integrated circuit is the second if amplifier-detector combination. The if amplifier consists of Q7, Q9 and Q10 with their associated components. Q7 and Q10 are emitter followers which isolate the gain stage, Q9. The supply voltage to the collectors is regulated by the zener diode, Z1. The quiescent operating point is stabilized by connecting the emitter of Q10 to the base of Q7 through R14. The connection is made by externally tying pin 7 to pin 8 through a suitable impedance. For dc stabilization, pin 7 should be at ac ground

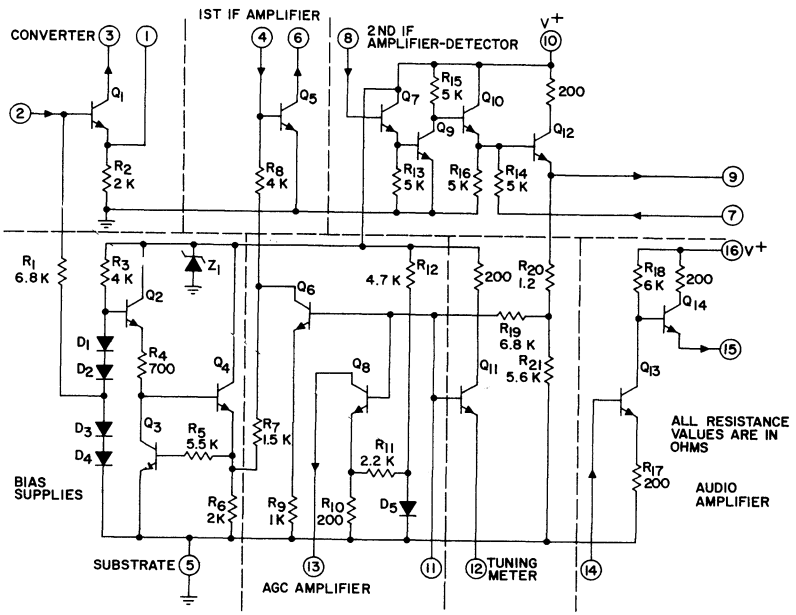


Fig. 1 — Schematic diagram of the RCA CA3088E.

TABLE I. CORRESPONDENCE OF TERMINALS TO FUNCTION

Function	Terminal
Converter	1, 2, 3
First IF Amplifier	4, 6
Second IF Amplifier-Detector	7, 8, 9, 10
AGC Amplifier	11, 13
Tuning-Meter Amplifier	12
Audio Preamplifier	14, 15, 16

potential, otherwise signal feedback will modify the basic characteristic of the stage. The output of Q10 is fed directly to Q12, an emitter follower operating at a quiescent current of approximately 100 microamperes. This stage becomes a detector by connecting the proper filter circuit to the emitter; the emitter is brought out on pin 9. The rectified emitter current develops a voltage at the junction of R20 and R21; the junction is connected to the bases of the agc and meter amplifiers.

Q11 is an emitter follower normally used to drive a tuning meter at pin 12. Q11 is biased off with no signal and will deliver approximately 150 microamperes with a maximum signal as indicated in the curve of Fig. 2.

Q8 is an agc amplifier intended to control an optional external rf amplifier. Collector voltage, applied through a load resistor to pin 13, provides a decreasing voltage at pin 13 with increasing signal. The voltage drop across diode D5 must be overcome by the drive voltage to the base of Q8, thus introducing a delay in the application of gain control to the rf stage. The agc curve of a typical circuit is shown in Fig. 2.

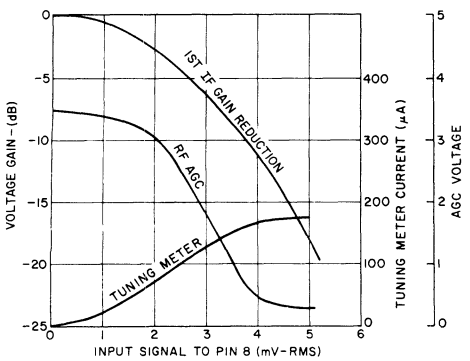


Fig. 2 — Typical performance curves for the CA3088E.

Q5 is the first if amplifier and is biased to draw one milliampere of current under zero signal conditions. This condition is set by the biasing circuit of Q2, Q3, Q4 and diodes D1 through D4. A nominal current of one milliampere is established in Q3, which is a mirror of Q5, thus determining the current in Q5. The supply voltage to the biasing circuit is also regulated by Z1. With no signal, Q6 is cut off and has no affect on the operating point of Q5. As signal strength increases and the base drive voltage increases, Q6 conducts some of the base current being applied to Q5 and reduces the collector current and, thus, the gain, as shown in Fig. 2.

Q1 is normally used as a converter stage. It is biased to a nominal current of 0.35 milliampere by diodes D3 and D4 in combination with the source resistor, R2. The emitter is brought out on pin 1; this terminal may be bypassed or may be used to apply a local-oscillator signal to the emitter.

Q13 and Q14 form the audio driver stage, a grounded emitter stage coupled directly to an emitter follower. The emitter follower provides a low-impedance drive for an external audio amplifier. This stage must be externally biased; a convenient method is to feed a portion of the dc potential on the emitter of Q14 to the base of Q13 with the proper network connected between pins 14 and 15. A nominal voltage gain from pin 14 to pin 15 of 30 times is determined by the ratio of resistor R18 to R17.

In addition to the voltage regulation provided by the zener diode, Z1, the circuit is temperature compensated by the bias circuit described previously. Transistors Q1, Q5, and Q13 are large-geometry devices which provide low-noise performance in the CA3088E. All emitter follower stages which have the emitters brought out to external terminals are protected against inadvertently shorted terminals. The size of the chip is 52 mils by 52 mils.

APPLICATIONS

AM Broadcast Receivers

When would a designer use the CA3088E as the basic subsystem of an AM radio? The typical low-cost table model or portable radio ordinarily has neither an rf amplifier stage nor a tuning meter; therefore, two features of the CA3088E have no use in simple AM radios. Furthermore, economic considerations make it difficult for integrated devices to compete with discrete devices in these minimal-performance receivers. On the other hand, the high-performance console receiver is an application in which all of the features of the CA3088E are useable. The CA3088E, in which the biasing of most stages is accomplished internally, provides savings in the number of components to be specified, purchased, handled, and connected.

Fig. 3 shows the circuit for a typical AM receiver using the CA3088E. Double-tuned transformer-coupled circuits are shown here, but any of the other forms of band-pass filters may be used that best suit the needs of the designer. The rf stage may take on any of several forms and so is shown only as a gain block. The intention here is not to present an optimum receiver design, but to show how a specific device, the CA3088E, may be used. Fig 4 shows performance curves obtained in a receiver using the CA3088E in conjunction with an external rf stage.

In addition to commercial broadcast-receiver, a multitude of receiver applications exist in communications equipment of all forms. The CA3088E will suit many of these applications with the extra features available in the circuit. The CA3088E may be used as a straight if amplifier for use with a separate tuner, or it could serve as a subsystem in a double-conversion receiver.

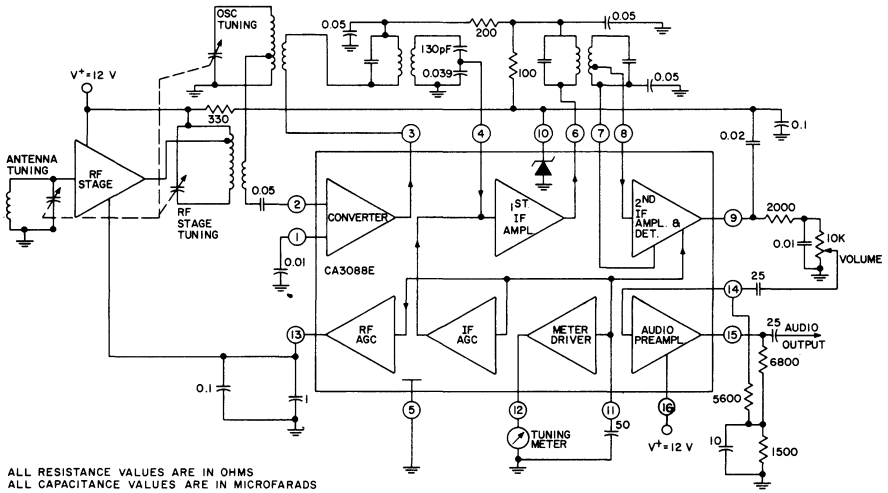


Fig. 3 — Typical AM broadcast receiver using the CA3088E.

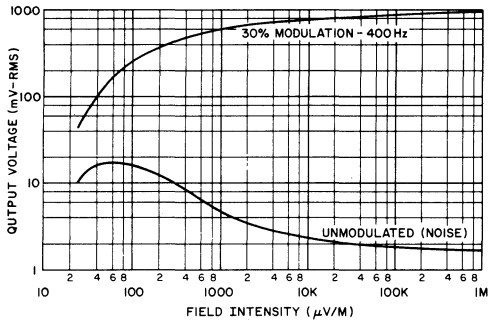


Fig. 4 — Performance curves for an AM receiver with an rf stage using the CA3088E.

Amateur radio receivers are a natural for the circuit. Narrow-band or fixed-tuned systems, such as remote control systems, and hand-carried receivers, systems in which the space saving features of an integrated circuit could be important, could make good use of the CA3088E.

High-Frequency Applications

Many receivers use if amplifiers at the higher frequencies; therefore, the high-frequency characteristics of the CA3088E are important. Table II shows some of the four pole characteristics of the individual signal stages of the CA3088E at 1 MHz and 30 MHz. The forward transconductance is not significantly affected in the frequency range considered.

The high-frequency performance of the second-if-amplifier/detector stage is determined within the chip. Fig. 5 is a plot of the voltage gain of the stage as a function of frequency. The gain is down about 6 decibels at 10 MHz and about 16 decibels

TABLE II. INPUT AND OUTPUT IMPEDANCE DATA

	C_{IN} Picofarads	C_{OUT} Picofarads	C_{fb} Picofarads	1 MHz R_i Ohms	30 MHz R_i Ohms	1 MHz R_o Ohms	30 MHz R_o Ohms
Q_1	12	5	1.5	3500	2000	100 K	9 K
Q_5	17	5	1.5	2000	1000	100 K	9 K
Q_7	3.5	–	–	75 K	45 K	-	–

at 30 MHz. The nominal gain of this stage is 40 decibels; therefore, this stage has considerable gain at these frequencies.

The converter and first-if stages will operate at higher frequencies, but stability considerations will control the practical gain. Calculations of maximum useable gain (MUG) and maximum available gain (MAG), using the data in Table I for the unneutralized single-stage amplifier, show that about 10 decibels of power gain must be sacrificed to maintain good stability at 30 MHz. More gain can be obtained by neutralizing, but at the expense of circuit simplicity.

The audio-preamplifier stage may also be used as another if stage provided that the low-output impedance of the emitter follower is not detrimental to performance. The stage may be used to drive a crystal or ceramic filter in which the typical matching impedances are quite low. The frequency response of this stage is very similar to that of the second-if stage with about 6 decibels drop in gain at 10 MHz. This stage may also be controlled by the output from pin 13 as is the case with the external rf stage.

Fig. 6 shows the circuit of a 10.7 MHz if amplifier using two ceramic filters. This circuit shows how the use of the CA3088E with low-impedance filters can simplify a design. Stability is maintained by the low-impedance terminations used with the filters. The first two stages are coupled together with a single-tuned circuit which provides impedance matching. A

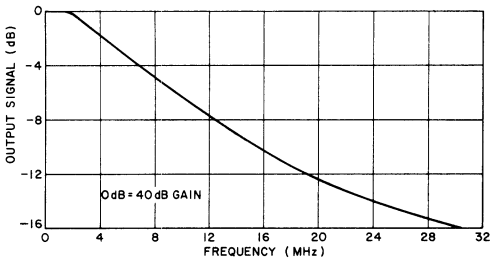


Fig. 5 – Plot of voltage gain as a function of frequency for the second-if-amplifier/detector stage of a CA3088E.

50-microvolt input signal with 30-percent modulation produces a detected audio signal of 22 millivolts at the detector output. The audio stage may be used as an audio driver or as an additional if stage to drive the input ceramic filter.

General-Purpose Amplifier Array

The CA3088E is versatile enough to be used as a general-purpose amplifier array. Q1 and Q5 are internally biased and require only a collector load to produce an amplifier. These devices may be operated to a maximum collector voltage of 16 volts. With the addition of external biasing, the operating points of these stages may be varied from the internally established quiescent point. The second-if-amplifier/ detector combination is biased externally as discussed previously. Q12, which is normally connected as an envelope detector may be connected as another emitter follower by loading resistors R20 and R21 with an external resistor.

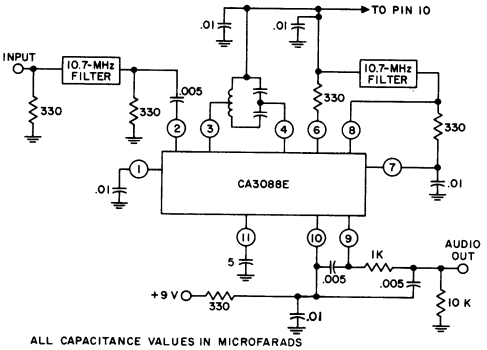
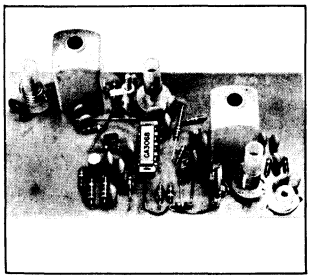


Fig. 6 – A 10.7-MHz if amplifier using the CA3088E and two ceramic filters.

The audio preamplifier is independent and biased externally. The gain-control circuits may be used as in the AM-radio applications. If Q12 is not used as a detector, the gain-control voltage can be applied on pin 11. Q11 provides a positive-going voltage with increasing signal and Q8 provides a negative-going voltage.

Acknowledgements

The author thanks Messrs. Leo Harwood and Max Malchow for their aid and suggestions in discussions concerning this project, and Mr. Frank Curley for his aid in circuit construction and collection of data.



A Single IC for the Complete PIX-IF-System in TV Receivers

by S. Reich and R. T. Peterson

The RCA CA3068 linear integrated circuit is a PIX-IF-subsystem in a shielded quad-formed dual-in-line plastic package of 20-lead configuration. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-IF-system for a TV receiver. This Note describes the receiver functions performed by the CA3068, and its application to color and black & white TV receivers.

Specifically, the receiver functions performed by the CA3068 are:

(1) Video IF Amplification
(2) Linear video detection
(3) Noise-limited amplification of detected video
(4) Keyed AGC, with noise-immunity circuits
(5) AGC delay for tuner RF stage
(6) Buffered output signal to drive Automatic-Fine-Tuning (AFT) circuits
(7) Amplification of intercarrier frequencies
(8) Sound-carrier detection
(9) Sound-carrier amplification
(10) Zener reference diode for voltage regulation.

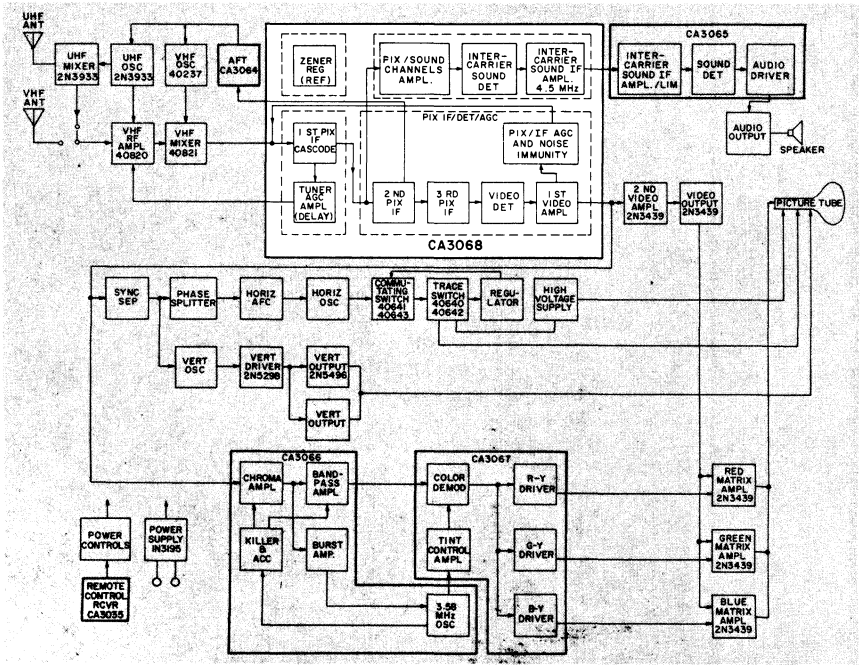


Fig. 1– Block diagram of a typical color TV receiver utilizing the CA3068.

The only external components required for the operation of this IF subsystem are bandwidth shaping networks, biasing networks and a power supply. A complete functional block diagram of a typical color TV receiver is shown in Fig. 1. A detailed block diagram of the CA3068, together with its peripheral tuned-circuits, is provided in Fig. 2. It should be noted that the circuit functions performed by the CA3068 represent a breakthrough in terms of IC design for PIX-IF systems, and that these circuit functions are accomplished without compromise in quality of performance.

This Note contains a detailed description of circuit functions within the integrated circuit, together with examples of the use of the CA3068 in actual PIX-IF amplifier PC-boards for color and black-and-white TV.

General Description of Circuit Functions in the CA3068

As shown in the block diagram of Fig. 2, the IF-signal from the tuner is applied to the input (terminal No. 6) of the cascode IF amplifier. Output from the cascode amplifier is then coupled to a wideband amplifier at terminal No. 13 through the interstage transformer (T_2). Under maximum-gain conditions the overall gain of the CA3068 is typically 75 dB at PIX-IF frequencies. This signal is then applied to a linear video detector, whose output signal is fed to a video amplifier having a gain of 12 dB.

Bandpass shaping is accomplished by means of tuned-circuits preceding the input stage (terminal No. 6) and at the interstage circuit comprising input and output terminations via terminals 9, 12 and 13 as shown in Fig. 2. Terminal No. 16 is tied in at this point to provide loop bias for the input stages of the amplifiers connected to terminals 12 and 13. The AGC-voltage developed within the CA3068 is applied to its input stage by an external path from terminal No. 4 to terminal No. 6 through the input circuitry, as shown in Fig. 2. The developed-AGC is gated by a keying pulse applied to terminal No. 3 from the horizontal sweep circuit of the TV receiver. Delayed AGC for the tuner's RF amplifier is obtained from terminal No. 7; the delay is variable by adjustment of a resistance (25kΩ) in series with the supply to terminal No. 8.

The zener reference voltage for the power-supply regulating pass-transistor is developed at terminal No. 18 when this terminal is connected to a voltage supply through a current limiting resistor. This resistor value should be selected to provide a quiescent current into the zener of 0.5 to 1.5mA (excluding the base current for the pass transistor).

Terminal No. 15 is the dc input terminal that provides power for most of the CA3068 and should be connected to a regulated supply of 11.3V. The CA3068 package has a 20-lead configuration with 18 active terminals. Terminal Nos. 11 and 20 have been omitted from the package; their

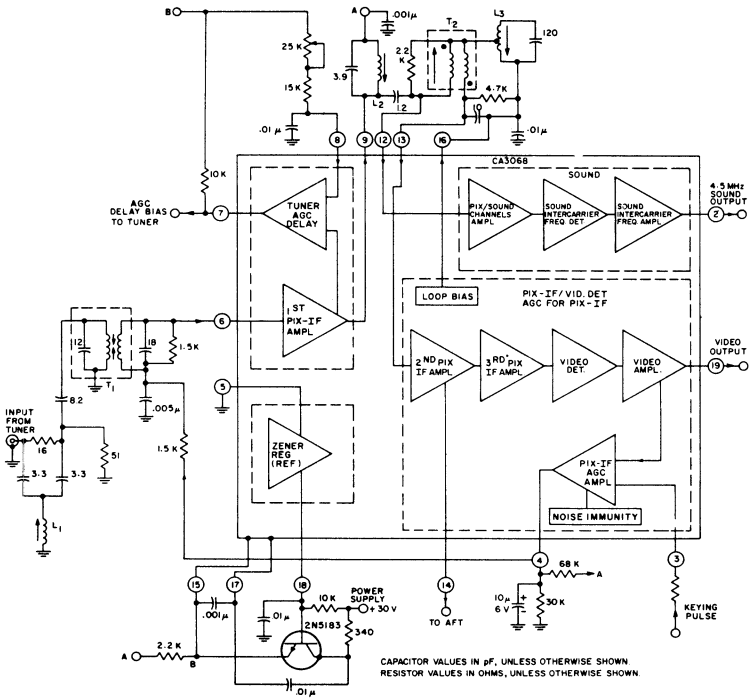


Fig. 2– Detailed block diagram of CA3068 showing interconnections with external components.

corresponding leads are internally connected to the shield. Terminals Nos. 1 & 5 are grounding pins. In addition, terminals Nos. 10 & 14 (not shown in Fig. 2) are at ground potential. Additional information relative to dc grounding is given in the section that discusses IF design.

Detailed Circuit Functions

A simplified schematic diagram of the CA3068 appears in Fig. 3. The diagram is partitioned to facilitate the explanation of the circuit configuration and its functions. Similar circuit function designations are used in the block diagram shown in Fig. 2.

The cascode input amplifier (1st IF) is a unique circuit designed for dual-mode operation. At low level input signals, the buffer stages formed by Q19 and Q20 drive the base of the cascode – IF amplifier comprised of Q3 and Q2. Negative-going AGC is applied to Q19 (through an external connection to terminal No. 6) which increases in proportion to the increase of the input signal level. After approximately 40dB of gain reduction is reached in this operational mode, Q3 is cut-off, and its function is assumed by Q4. Emitter degeneration in Q4 increases the dynamic input range of the cascode amplifier sufficiently to cope with the higher range of input signal level. The point at which Q4 assumes the input amplifier function is sensed by Q1. It should be understood that transistors Q1, Q20 and Q3 approach cut-off at essentially the same signal level. As Q1 approaches cut-off, it draws less shunting current from terminal No. 8 and base current drive to Q21 is increased. The point at which sufficient base current is available to drive Q21 into conduction is determined by an external delay-AGC potentiometer connected in series with the V+ supply-lead and terminal No. 8. As Q1 cuts-off, the current flowing into terminal No. 8 is diverted to the base of Q21. When Q21 starts to conduct it turns on Q5, thereby causing the open-circuit voltage at terminal No. 7 to drop and produce a negative-going AGC voltage for the tuner's RF stage. Q21 is also part of the IF-AGC feedback loop and provides an increase in AGC loop-gain. This increase compensates for the decrease in AGC loop-gain that occurs when the cascode-IF amplifier is transitioned to its modified cut-off characteristic. After tuner gain reduction has reached its maximum, an additional 10dB of gain reduction can be obtained in the cascode amplifier under this modified cut-off condition.

This reverse AGC system is used for the cascode input stages because the stability achieved under maximum-gain conditions is maintained throughout the range of AGC functioning.

The wideband-IF amplifier consists of transistors Q6, Q7 and Q8. Q6 serves as a buffer stage between the interstage tuned-circuits and the AFT output signal terminal. The actual IF signal amplification takes place in Q7 and Q8, effectively serving the function of 2nd & 3rd PIX-IF stages. Transistor Q8 is the driving source to Q22, the video detector. This driving source impedance is approximately 500 ohms as a result of the degenerative feedback loop through R13. The feedback network also extends the 3dB-down frequency response to beyond 70 MHz. It is this low detector driving point impedance and the absence of a tuned-circuit at this interstage point that contribute to the superior performance of the detector system. In most conventional detection systems, the detector is driven from a high-impedance source involving a double-tuned interstage

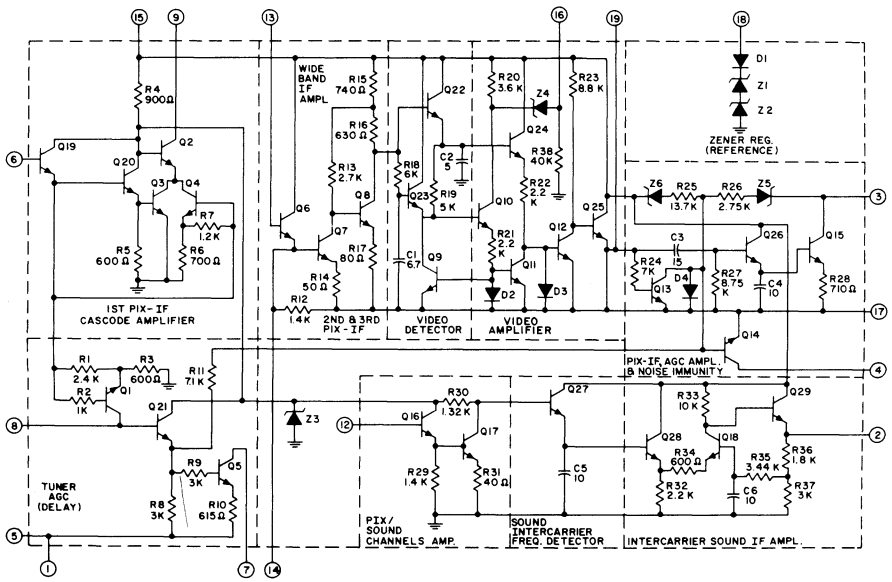


Fig. 3– CA3068 – Simplified schematic diagram.

transformer with unequal primary and secondary Q's. In such a system, variations in detector impedance (caused by normal video excursions) can produce significant phase shifts that adversely affect color fidelity. In the CA3068, the untuned, low-impedance detector drive circuit produces a nearly optimum condition for the detector circuit.

The detector circuit consists of transistor Q22 and its biasing network Q9, Q23 and R19. Q23 is biased to the same potential as Q22 because the bases are tied together through the resistance element of the low pass filter that consists of R18 and C1. R19 and C2 form a conventional peak detector in which the time constants are selected for optimum detector efficiency and desired video bandwidth. This system detects chroma subcarrier without introducing differential phase errors as a function of the video signal, and detects the video signals with a minimum of amplitude distortion. The low signal-level requirements for the detector, the absence of tuned-circuits in the detector drive circuit, and the low source impedance for the detector, all contribute to the superior detector performance.

The video detector is direct-coupled to the video amplifier. Consequently, a dc input voltage above the level of one V_{be} (0.7V) drop at the input to Q12 determines the condition for white level (dc) at the output (terminal No. 19). It is, therefore, necessary to prevent the conduction of Q12 in the absence of detected video. This function is accomplished by the differential amplifier circuit arrangement consisting of transistors Q10 and Q24. In the absence of signal. the dc potential at the emitters of Q10 and Q24 is identical. The current through Q10 must equal the current through Q24, because R21 is similar in value to R22. This current also flows through D2 (which has the same geometry as Q11). Consequently, Q11 carries all the current supplied by Q24 and no current is available for D3, so that Q12 is held on the edge of conduction. When an RF carrier is present, the current in Q24 increases in direct proportion to the carrier level. However, the current in Q10 remains fixed. When the current increases in Q24, this increase can only flow through D3. Since the current in Q12 is directly proportional to the current in D3, increased current flow in D3 causes a corresponding increase in current through Q12, and produces a video output at terminal No. 19.

As the video carrier signal increases, the dc level at the base of Q12 increases, and there is an accompanying decrease in the dc level at the base of Q25 and at terminal No. 19. With a sufficiently strong RF signal, the current through Q12 and R23 increases such that the base voltage of Q25 is driven toward dc ground. The "bottoming" level, at terminal No. 19, under nominal signal conditions is locked to about 0.8V as a result of the high loop gain of the AGC system. Any further increase in the signal, after "bottoming" is reached, will be clipped. This operational feature serves as a highly effective mechanism to limit impulse noise.

When a signal is present at the input, the composite video signal appears at the emitter of Q25. The sync tips in this composite waveform drive the keyed AGC amplifier Q13 which in turn drives Q14. Without a video RF signal there is no video signal output and Q13 conducts during the keying intervals, (horizontal pulse connected to terminal No. 3). As the detected signal level increases in amplitude and the output voltage at terminal No. 19 approaches its typical operational level of 7.0 volts peak-to-peak, the peak potential at the base of Q13 begins to fall below 0.8V. Under these conditions, the keying current formerly channeled through Q13 is diverted through the diode D4. As the signal level rises even higher, a greater portion of the Q13 collector current is diverted through D4 and the base current to Q14 is proportionately increased. A 10μF capacitor is normally connected between terminal No. 4 and ground and is, thereby, connected in shunt with Q13. The charge on this external capacitor is maintained through a bleeder resistor to V+. As the base current to Q14 increases, Q14 discharges the capacitor at a rate that is proportional to the base current of Q14. Integrating the total charge on the capacitor over the keying interval yields a dc level (AGC voltage) that is inversely proportional to the incoming signal level, i.e. AGC voltage approaches zero as the signal increases.

Any high performance AGC system must have noise immunity characteristics in order to avoid the establishment of false AGC levels. AGC voltage developed from random noise can produce "wash-out", "blank raster" and/or a momentary "loss of sync". The CA3068 is designed with an improved noise immunity circuit that essentially removes the keying current during periods of high noise input. The active devices responsible for providing protection against this deleterious effect of the impulse noise are the "noise detector", Q26, and the "noise clamp" Q15. Impulse noise is channeled through the high pass filter network consisting of C3 and R27 to the detector input Q26. Q26 and C4 comprise a conventional peak detector. The dc level across C4, which is proportional to the level of impulse noise, turns on Q15, thereby clamping the keying supply voltage (terminal No. 3) to ground. In actual operation, the terminal No. 3 supply has a series resistance that is large enough to limit the peak current into the zener diode (Z5) to approximately 0.8mA. When Q15 conducts it shunts this current to ground.

The sound-IF-channel and PIX-IF-channel signals whose "carrier" frequencies are 41.25 MHz and 45.75 MHz respectively, are applied to terminal No. 12. Q16 functions as a buffer between the interstage-tuned-circuits associated with terminal No. 12 and the PIX/sound-channels amplifier Q17. The intercarrier frequency (the difference frequency between the PIX and sound "carrier" frequencies) is detected by the peak detector Q27 and C5. The resultant 4.5 MHz FM sound-intercarrier signal is fed to transistor Q28. This transistor and Q18 form a differential pair that provides an amplified intercarrier sound-IF signal to the base of Q29. A feedback system through the RC networks in the emitter of Q29 provides bandpass shaping in the region of 4.5 MHz while maintaining a low dc gain. The low level of dc gain is desirable because the circuit receives its bias in an open-loop

manner from terminal No. 16. The bandpass of this amplifier system is fairly broad and even though it is optimized for 4.5 MHz operation, there is relatively high output at other intercarrier frequencies as shown in the curve in Fig. 4.

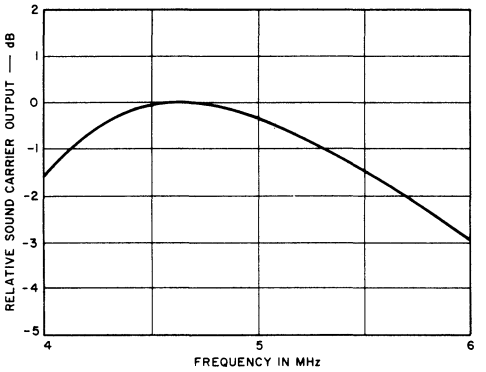
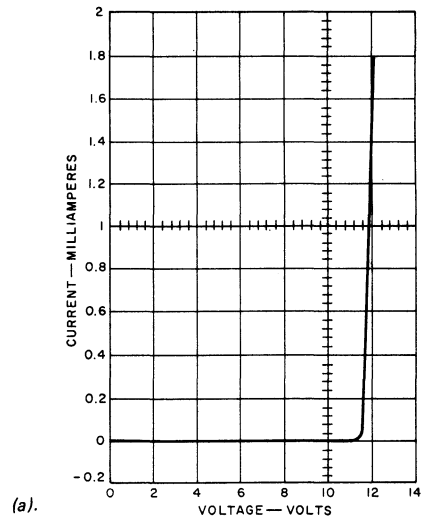


Fig. 4— Relative sound-carrier output-vs-frequency.

The internal zener reference-diode consists of the series diode arrangement shown connected between terminal No. 18 and the substrate. A regulator circuit configuration, showing the pass transistor interconnected with the reference diode, is given as part of the color and b&w IF amplifier circuits that are discussed in the following paragraphs. Similarly, the regulation curves shown in Figs. 5a and 5b will be discussed below in more detail. It should be noted that (with a proper heat sink for the 2N5183 and a lower value for the resistor in series with the collector) the regulated voltage from this supply may be used to provide power to other circuits in addition to the CA3068.

The distribution of tuned circuits around the CA3068 amplifier circuit is a matter of preference by the circuit designer. In general, a total of five tuned circuits will be required subsequent to the mixer for proper selectivity and band-pass shaping. In addition, at least one 47.25 MHz adjacent sound-channel and one 41.25 MHz sound-channel traps will be required. The systems to be discussed in this application Note are driven from a single tuned circuit connected to the mixer output.

In addition, both the color and b&w IF systems described subsequently utilize two double-tuned circuits; one at the input to the cascode amplifier and one at its output. The second transformer is used to couple output from the cascode-IF amplifier to the wide-band IF amplifier (i.e. the output from terminal No. 9 to input terminal No. 13 for the PIX-channel and input terminal No. 12 for the sound-channel). All the IF transformers are synchronously tuned.



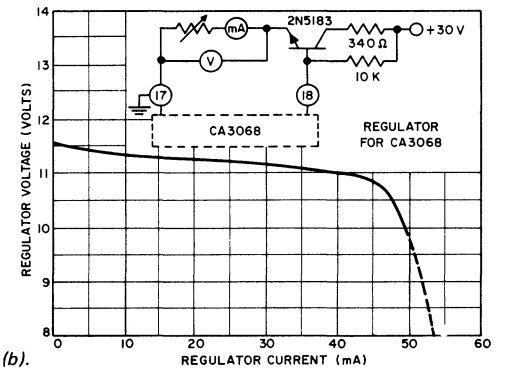


Fig. 5— Regulated supply of CA3068 (a) Voltage-vs-current for zener reference diode of CA3068 (b) Voltage-vs-current for regulated supply of CA3068.

The IF system for a color-tv receiver was designed to operate with a tuner containing an MOS field-effect transistor RF amplifier to illustrate the operation of the CA3068 with a "reverse" AGC arrangement. In contrast, the IF system for a b&w receiver was designed to operate with a tuner containing a bipolar transistor in the RF amplifier, to illustrate the operation of the CA3068 with a "forward" AGC arrangement.

IF Design for Color-TV Receiver

The circuit diagram of the IF system for a color receiver is shown in Fig. 6a. A schematic drawing of the PC board component layout and an actual size bottom view of the PC board are shown in Fig. 6b and 6c, respectively. The basic operation of the system may be explained by reference to the block and schematic diagram in Figs. 6a and 7. The input to the IF system is coupled through a 50 ohm cable from the TV mixer, that employs a single-tuned output coil having an impedance transformed down to 50 ohms. The input and interstage circuits include double-tuned over-coupled transformers. The IF input circuit drives a cascode-IF amplifier with a gain capability of 35 dB. The input impedance to the cascode IF-amplifier is greater than 4000-ohms at minimum signal levels and increases with AGC action. The source impedance as seen by the CA3068 is approximately 500 ohms, which completely dominates the input circuit conductance node. Similarly, the output impedance of the cascode amplifier is loaded by a tuned circuit with an impedance of approximately 3000 ohms. Again, the tuned-circuit conductance dominates the output node. For this reason, the IF amplifier stability is unaffected by the IC impedance variations and is a function of the feedback component. This feedback component consists of coupling within the IC packaging, PC-board stray capacitances, and PC-board common impedances. It can be shown that with the maximum device feedback capacitance the amplifier is stable. For example, with circuit bias conditions of $I_9 = 2mA$; $Y_{21} = 50mmhos$ and $C_{fb}\,(max) = 0.005pf$, the maximum usable gain (MUG) is 42 dB (which allows for a 20% skew factor). The fact that this value of MUG is greater than the actual circuit gain (35 dB) substantiates the stability.

Although these calculations show the device to be theoretically stable, it must be realized that it is possible for external feedback mechanisms to, in effect, raise the level of feedback in any high-gain physically small RF amplifier and produce instabilities. For this reason, the PC-board layout is extremely important, and any high-gain IF amplifier design would be incomplete without a board layout such as that shown in Fig. 6b.

As mentioned previously, the interstage transformer loads the cascade amplifier with approximately 3000 ohms. It provides a 500-ohm source impedance to the input terminal No. 13, (the wide-band IF amplifier section). The impedance at terminal No. 13 is approximately 5000 ohms. The driving-point impedance to the sound-IF terminal No. 12 is about 1000 ohms and it looks into a 5000-ohm input circuit.

The circuit design shown in Fig. 6a includes a 47.25 MHz bridged "T" adjacent-sound-channel trap at the input circuit. It may also be desirable to include a 39.75 MHz trap for adjacent video carrier when the receiver is intended for operation in CATV systems or in areas where adjacent channels are available. Such a trap may consist of a 39.75 MHz bridge "T" connected in parallel directly across the 47.25 MHz trap. The 41.25 MHz trap is a rejection filter for the video amplifier and allows the carrier to pass into the sound system. Both traps provide the additional selectivity necessary for attenuation of the undesired frequencies by more than 40 dB.

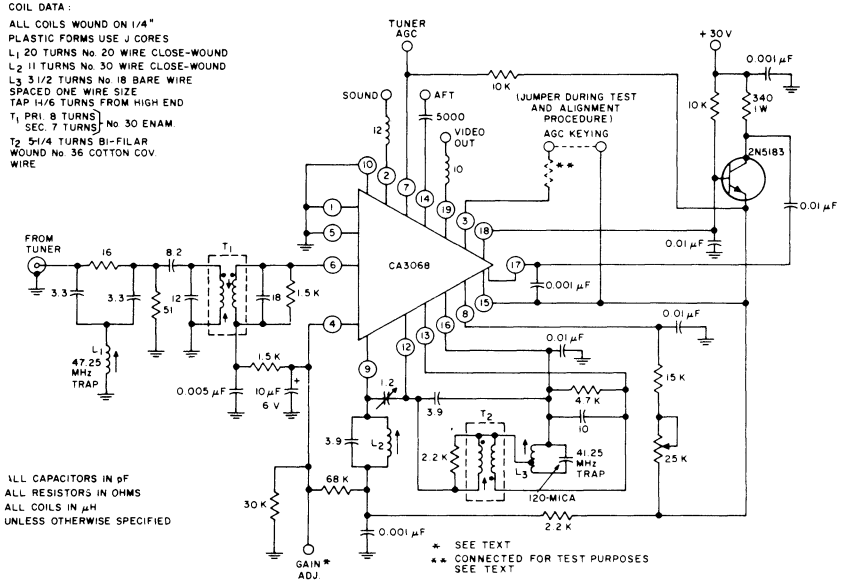
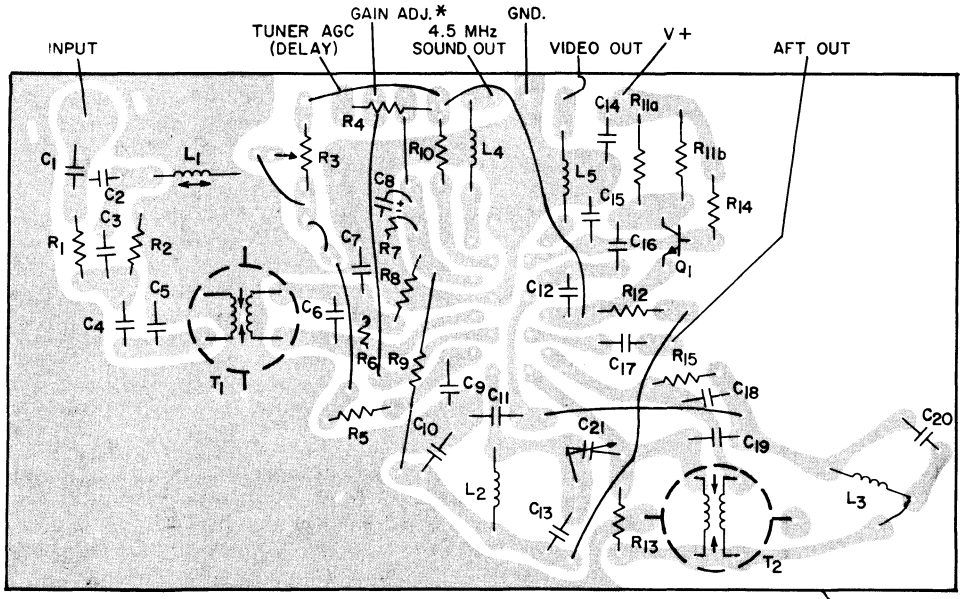


Fig. 6a— Schematic diagram and coil data.



R1	16	R11a }	340–1W	C4	8.2 pF	C14	0.001 μF	L1 }	SEE
R2	51	R11b }	(EQUIV.)	C5	12 pF	C15	0.01 μF	L2 }	FIG.
R3	25K	R12	2.2 K	C6	18 pF	C16	0.01 μF	L3 }	6A
R4	10K	R13	2.7K	C7	0.005 μF	C17	0.005 μF	L4	12 μH
R5	15K	R14	10K	C8	10μF – 6V	C18	8.2 pF	L5	10 μH
R6	1.5K	R15	4.7K	C9	0.01 μF	C19	3.9 pF		
R7	30K			C10	0.001 μF	C20	120 pF	Q1	2N5183
R8	1.5K	C1	0.001 μF	C11	0.01 μF	C21	1.2 pF		
R9	68K	C2	3.3 pF	C12	0.001 μF				
R10	2.2K	C3	3.3 pF	C13	3.3 pF				

* SEE FIG. 6A

Fig. 6b– Top view of circuit board layout.

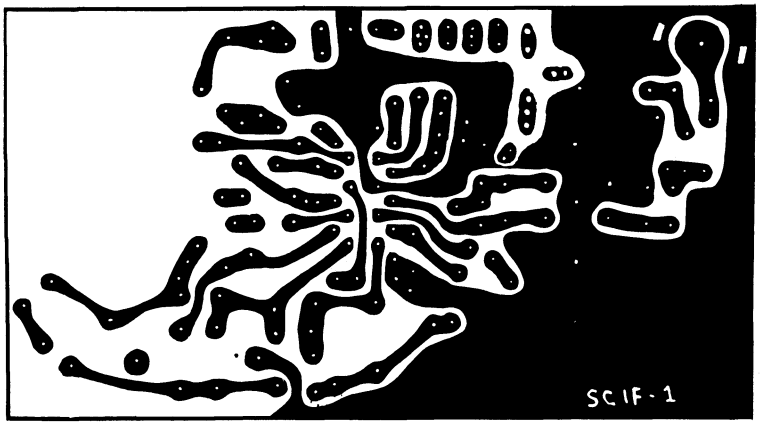


Fig. 6c– Bottom view of color P.C. board. (actual size).

The wide-band IF amplifier provides two extra stages of gain (approximately 40 dB). It presents a very low driving-point impedance to the linear detector, as described earlier. The detected signal then undergoes an additional 12 dB of video amplification. The video output at terminal No. 19 is nomimally 7 volts (peak-to-peak). AGC is developed when the input signal reaches and exceeds the magnitude necessary to produce this video output level. Fig. 8a shows the developed AGC bias (terminal No. 4 voltage) as a function of signal level at terminal No. 6. Fig. 8b shows the delayed AGC voltage at terminal No. 7 (for application to the tuner) with R1 adjusted so that this delay-bias is generated whenever the IF input signal at terminal No. 6 exceeds 8mV. The curve in Fig. 8c depicts the over-all AGC characteristic in terms of AGC bias voltage at terminal No. 4 when the AGC system is adjusted to yield the curves in Figs. 8a and 8b. Similarly Fig. 8d shows the AGC characteristics when delayed-voltage from terminal No. 7 is applied to the tuner.

Fig. 7 shows the CA3068 coupled to an RCA tuner that uses an RCA type 40820 MOSFET in the RF amplifier stage. AGC voltages are applied (shown in Fig. 7) to optimize over-all TV receiver performance; so that, when maximum receiver sensitivity is required, (such as during the reception of weak signals from the antenna), the tuner will operate at optimum noise factor and maximum gain. As the input signal level increases, it is still desirable to operate the RF stage at optimum signal-to-noise ratio until the signal level is of sufficient magnitude as to override any tuner noise degradation brought about by the application of AGC. Therefore, the gain reduction voltage should be delayed to the tuner until the signal level builds up. Fig. 8b shows that this AGC is delayed until the IF signal level reaches an 8mV level. Then the tuner-gain-reduction mode is initiated. After the tuner-gain reduction is expended, at least another 10 dB gain reduction is still available in the cascode portion of the IF amplifier.

An output signal is available at terminal No. 14 to drive an automatic-fine-tuning (AFT) subsystem-IC such as the RCA Type CA3064. This connection is a buffered output from an emitter follower as described earlier. The level of signal at 45.75 MHz to drive the AFT circuit is nominally 15mV.

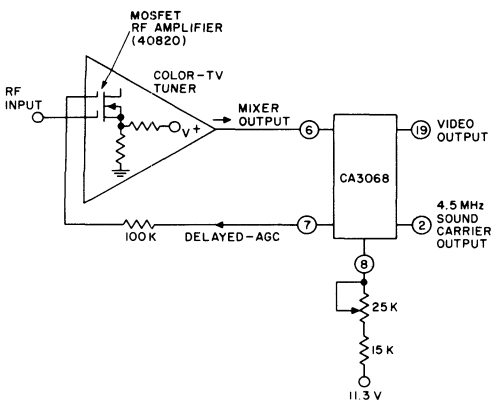


Fig. 7— Block diagram of a color IF system.

The AGC system is, for the most part, self-contained. An optimized AGC response characteristic can be achieved by use of a high quality tantalum 10μF capacitor connected between terminal No. 4 and ground. The 1500-ohm series resistor connected between terminal No. 4 and the 0.005μF capacitor to ground form a decoupling network which smooths the AGC ripple associated with the charge and discharge of the 10μF capacitor, at the horizontal oscillator frequency rate. The AGC system is normally keyed from the horizontal output circuit in the TV system. This keying pulse should be applied to terminal No. 3. The magnitude of the pulse should be sufficient to supply a nominal peak current value of 0.8mA into terminal No. 3. The value of the series resistor R_S, associated with terminal No. 3 may be computed as follows:

a. During the conduction period (with keying applied), the constant voltage components within the integrated circuit account for

$$V_K = 8.2V \text{ (it is assumed that } I_3 = 0.8mA)$$

b. If the keying pulse magnitude is $V_p = 15V$, then

$$I_3 = 0.8mA = \frac{15 - V_k}{R_s} = \frac{(15 - 8.2)V}{R_s}$$

$$R_S = 8.5\ k\Omega$$

The sound output is derived from terminal No. 2 at a level compatible with the input requirements of a TV sound IF-subsystem IC such as the RCA Type CA3065. There is also a dc component of approximately 6.7V present at terminal No. 2. Coupling networks to subsequent circuits must contain a suitable dc blocking capacitor.

Small chokes located in the sound and video outputs are self-resonating (terminals Nos. 2 and 19) at the intermediate frequencies to prevent IF leakage into subsequent stages.

The CA3068 IF subsystem has an internal zener reference-diode for operation with an external voltage-regulator pass transistor. A suggested circuit arrangement is shown as part of the over-all IF schematic in Fig. 5b. The voltage-regulator pass-transistor has a nominal output voltage of 11.3V. Bypassing of the V+ supply with reference to the IF subsystem is important and the suggested arrangement shown in the schematic should be used. Specifically, the base of the pass transistor should be bypassed to ground. The emitter is bypassed to terminal No. 17 on the CA3068. Even though terminal No. 17 is at dc ground *potential it* should not be tied to ground but rather should be bypassed in the manner shown, to avoid mutual impedance coupling within the CA3068.

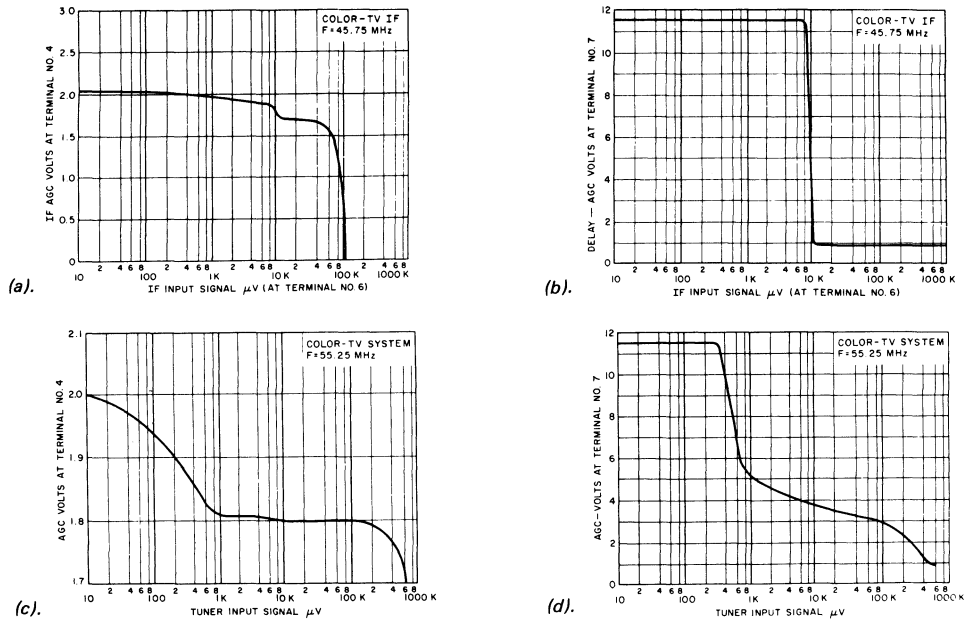


Fig. 8— Color TV IF AGC characteristics (a) AGC voltage-vs-IF input signal (b) Delayed AGC-vs-IF input signal (c) AGC-vs-tuner input signal (d) Delayed AGC-vs-tuner input signal.

The IF circuit shown in Fig. 6a was designed with two overcoupled IF transformers. The alignment procedure is straight forward and should follow the procedure given below:

1. Apply a negative bias supply through a 470kΩ series resistor to the terminal marked "gain adjust". This bias is intended to override the AGC loop-bias during the alignment procedure.
2. Apply a swept signal from a terminated 50-ohm signal generator directly to terminal No. 6. This signal will, in effect, "swamp" the response characteristic of the input circuit and enable alignment of the interstage transformer.
3. Adjust the level of the sweep generator so that approximately 2mV of IF signal (at carrier) is present at terminal No. 6.
4. Advance the negative bias from the external AGC override supply so that 5 to 6 volts peak-to-peak of video output is present at terminal No. 19.
5. Adjust the response characteristic so that the curve as shown in Fig. 9a is duplicated.
6. (This step may be omitted). If observation of the input IF response is desired, it can be accomplished by the swamping of the interstage transformer with a parallel 100-ohm resistor and .01μF bypass capacitor, and observing the response curve on an oscilloscope (shown in Fig. 9b) at terminal No. 19 while a swept IF signal is applied to the input terminal from a generator (50-ohm-source). The external bias must be adjusted to maintain the video output level at 5 to 6 volts peak-to-peak output 2mV carrier present at terminal No. 6.
7. Apply a 2mV IF signal to the system input from a 50-ohm-source generator, then tune the input transformer for an over-all response characteristic shown in Fig. 9c. The AGC override supply must be adjusted for 5 to 6 volts peak-to-peak output at terminal No. 19.
8. The overall response characteristic when the IF signal is applied to the mixer input is shown in Fig. 9d. The level of this IF signal is such as to keep the IF input at terminal No. 6 at 2mV, with AGC override adjusted for 5 to 6 volts peak-to-peak output at terminal No. 19.

IF Design for B&W Receivers

The schematic diagram, PC-board layout and PC-board bottom view (actual size) of the IF system for a b & w receiver are shown in Figs.10a, b, c. Coil information is shown on the schematic. Alignment procedures are similar to those described above in the section that discusses the IF system for a color receiver. The curves shown in Fig. 11 should be substituted for those cited for the color IF alignment procedure. These curves indicate a narrower bandwidth as reflected by the higher circuit Q's of the interstage transformers used in the b & w receivers.

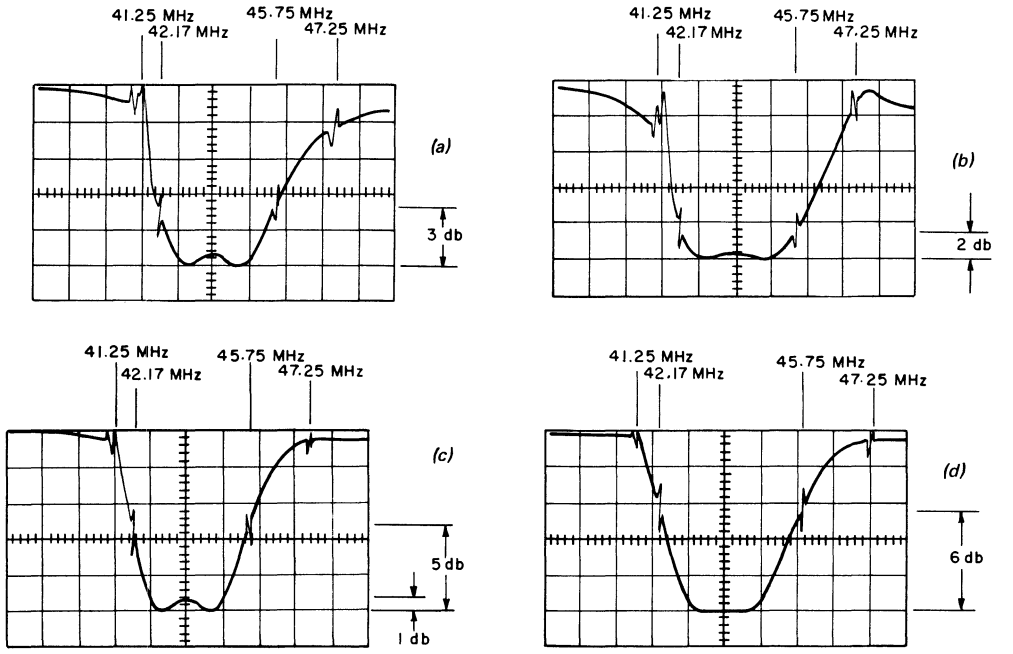


Fig. 9— CA3068-Color TV Waveforms (a) Video IF response of interstage transformer (b) Video IF response of mixer stage transformer (c) Video IF over-all system response (d) IF and mixer response.

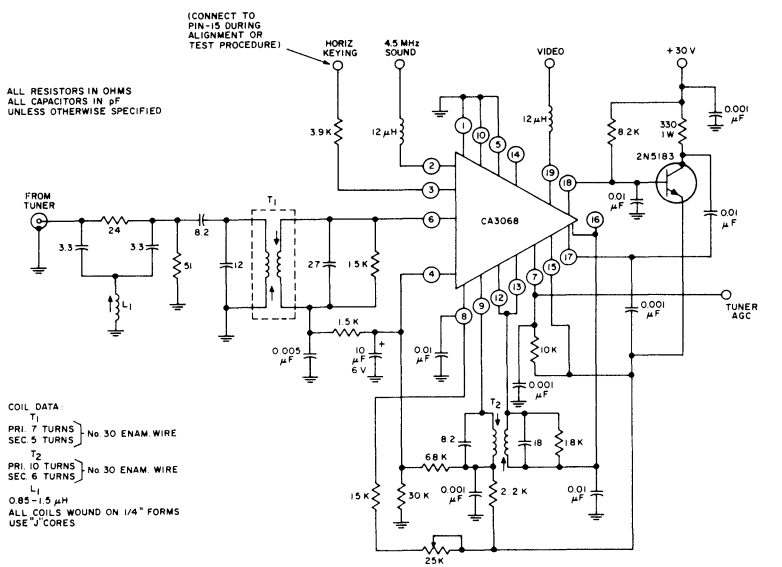
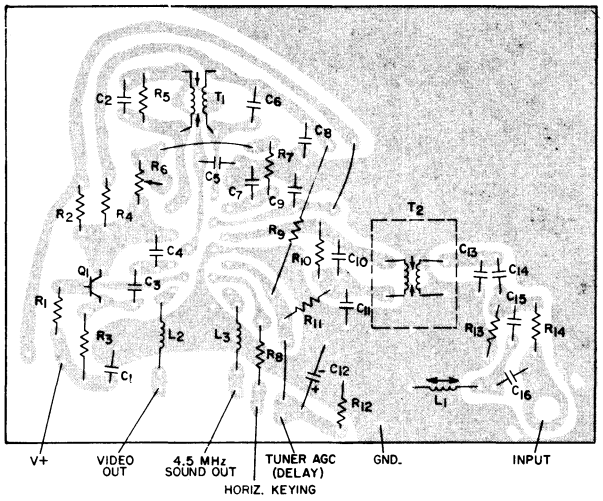


Fig. 10a—Schematic diagram and coil data.



R1	8.2 K	R11	1.5K	C5	0.01 μF	C14	8.2 pF
R2	10 K	R12	30 K	C6	8.2 pF	C15	3.3 pF
R3	330 Ω – 1W	R13	51 Ω	C7	0.01 μF	C16	3.3 pF
R4	2.2 K	R14	24 Ω	C8	0.001 μF	L1	SEE FIG. 10A
R5	1.8 K			C9	0.001 μF	L2	12 μH
R6	25 K	C1	0.001 μF	C10	27 pF	L3	12 μH
R7	15 K	C2	18 pF	C11	0.005 μF		
R8	3.9 K	C3	0.01 μF	C12	10 μF – 6V	Q1	2N5183
R9	68 K	C4	0.001 μF	C13	12 pF		
R10	1.5K						

Fig. 10b– Top view board layout.



Fig. 10c– Bottom view of circuit board (actual size).

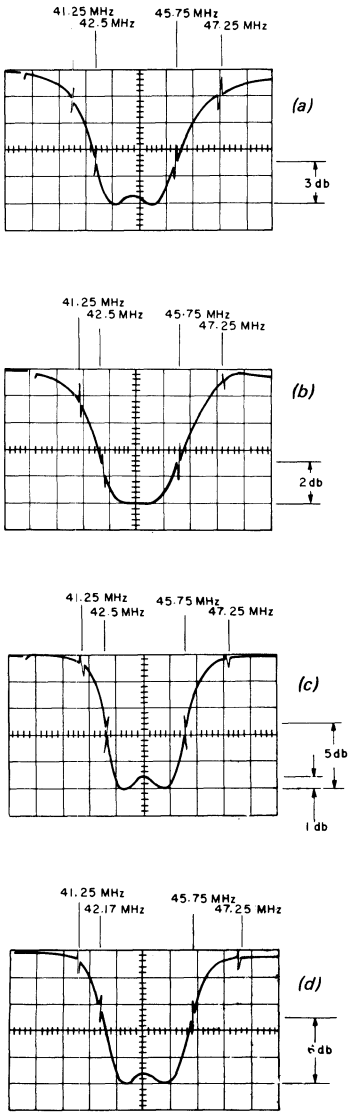


Fig. 11– CA3068 B&W TV waveforms, a) Video IF response of interstage transformer; b) Video IF response of input stage transformer; c) Video IF over-all system response; d) IF and mixer response.

In the color-IF system, the delay AGC was used to control a MOSFET in the RF stage of the tuner. This type arrangement permits direct application of the delayed AGC voltage from the CA3068 to the tuner. In the system for a b&w receiver the CA3068 AGC delay circuit is designed to control a bipolar transistor (which requires forward AGC) in the RF stage of the tuner. This function is accomplished by an inverter network utilizing a p-n-p transistor as shown in the circuit of Fig. 12. The forward-AGC delay is developed when the voltage at terminal No. 7 decreases, as the input signal level is increased. Under maximum gain conditions, the AGC voltage applied to the tuner (Fig. 12) is 1.6V measured at the collector of the p-n-p transistor. As the delay AGC voltage is generated, the base of the p-n-p inverter is driven into hard conduction, causing more current to flow through the collector circuit so as to generate a positive (or forward) AGC potential for the bipolar transistor in the tuner.

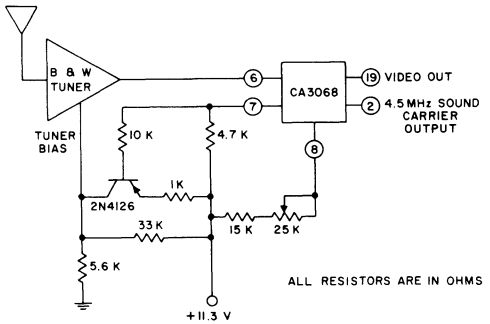


Fig. 12– Block diagram of B&W IF system showing required peripheral circuitry.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA, Commercial Engineering, Harrison, N. J. 07029.

CONCLUSIONS

A complete IF subsystem was described for both color and b&w TV Applications. The only signal inputs required by the CA3068 are IF signals from the tuner and a keying pulse from the horizontal circuitry. The CA3068 provides all outputs needed to drive the video output stage, delay line, sync separator circuitry, RCA type CA3065 sound-IF subsystem, RCA type CA3064 AFT subsystem, and delayed-AGC voltage for the RF stage in the tuner. Additionally, circuits for noise immunity and signal overload protection are designed into the CA3068. These subsystems have typical input sensitivities of 100μV for 4 volts peak-to-peak video output. A unique video detector arrangement provides extremely linear output throughout the 7 volts peak-to-peak video output range of the system.

Although this Application Note deals with subsystem designs in TV receivers, the CA3068 is suitable for performance in other AM systems requiring performance at frequencies within the range of 10-70MHz.

ACKNOWLEDGEMENT

The authors wish to express their gratitude to Mr. J.R. Harford, the designer of the CA3068 for his assistance during the evaluations required for this Note.

A Flexible Integrated-Circuit Color Demodulator for Color Television

By W. M. Austin

New color-TV receiver designs indicate a rapidly changing trend toward all solid-state circuitry with special emphasis on monolithic integrated circuits. The solid-state color-demodulator circuits in these receivers provide excellent demodulation gain, linearity, and uniformity. These advantages are easily achieved by the integrated-circuit design of the balanced demodulator. At present, the integrated circuit is economically adaptable to the current design requirements of the color-picture-tube drive circuits. The choice between a color- difference (CD) or a red-green-blue (RGB) receiver system has changed in favor of the RGB which has additional design advantages. Because of improved phosphors and improved color picture tubes in general, color shifting has caused the establishment of a new reference for the demodulation parameters. Consideration of these references and of many other recent requirements have set the design guidelines for the RCA CA3067 demodulator integrated circuit.

The CA3067, which is supplied in a quad-in-line 16-lead plastic package, provides the following color-demodulator circuit functions:

(1) Amplification

(2) Blanced chroma demodulation*

(3) DC-operated tint (phase) control

(4) Zener-diode voltage regulation

This Note describes the circuit operation and application of the CA3067 in a color television receiver. Fig. 1 shows the CA3067 interconnected with other units in a complete receiver.

The CA3067 has a phase-shift circuit for tint control and a limiting amplifier for the elimination of amplitude modulation on the reference subcarrier.** In addition, it has preamplifier circuits which amplify the subcarrier signal before it is injected into the balanced demodulators. Because integral rf filters remove the high-frequency products of demodulation, external filtering is unnecessary. The R-Y and B-Y color-difference signals are obtained by demodulation and the G-Y signal is derived from a matrix of the complementary R-Y and B-Y signals. The output amplifier for each of the color-difference signals has a very low output impedance for positive and negative signals and a sufficient drive capability for high-level voltage amplifiers for either a Red-Green-Blue (RGB) or a color-difference (CD) circuit. The operation of the CA3067 is described in the reverse signal-flow order to emphasize the output drive capability and requirements in direct-coupled circuit applications. Fig. 2(a) shows the CA3067 in a typical application.

The Output Amplifiers of the CA3067

An outstanding feature of the CA3067 output amplifier circuit is the feedback emitter-follower arrangement which keeps the output impedance low during both the positive and negative peak signal swings of the output stage. This arrangement assures sufficient drive capability for the high-voltage output transistors of present color systems without degradation of bandwidth characteristics, particularly when signal amplitudes are at peak values. The largest output drive capability from the B-Y color-difference stage is a voltage drive in excess of 3.0 V peak-to-peak. This range of output drive will satisfy the design requirements of most RGB or color-difference systems.

As shown in Fig. 2(b), the B-Y amplifier, which is similar to the R-Y and G-Y color-difference output circuits, has a feedback path from the collector of the emitter-follower Q_{30} to the base of Q_{29}. The zener diode, Z_1, has a voltage drop of

* "Chroma", defined here, means side bands of the modulated chrominance subcarrier.

** "Reference subcarrier", as used in this Note, means the same as "chrominance-carrier reference."

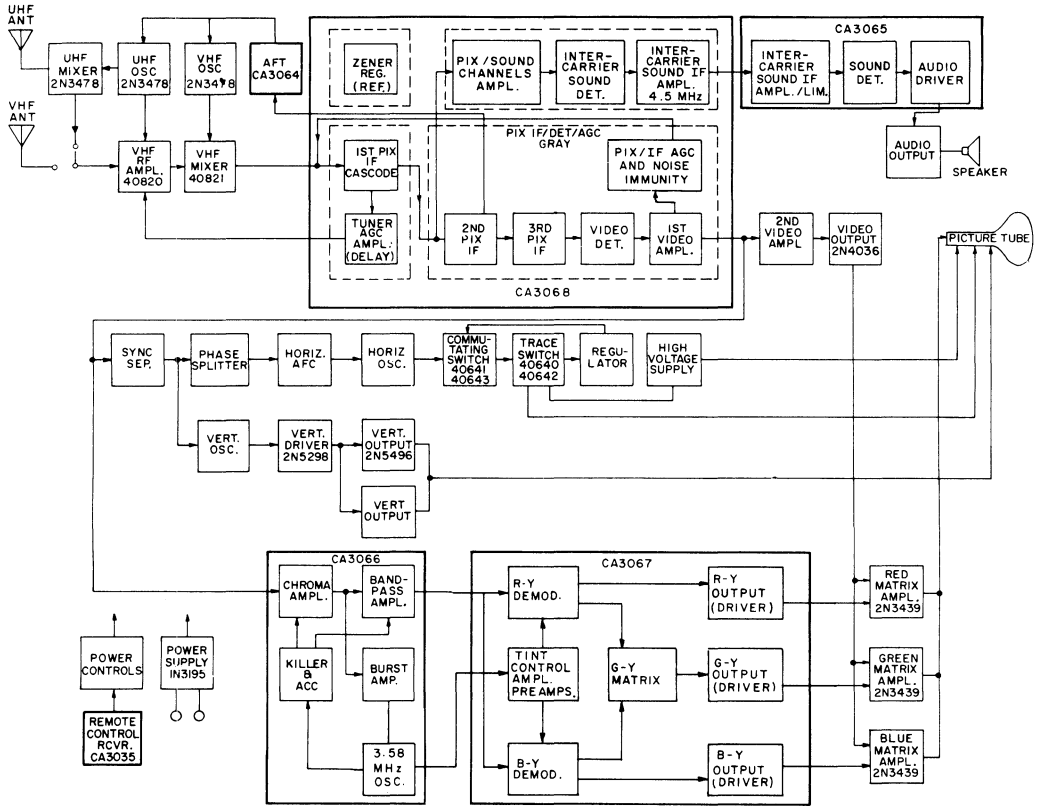


Fig.1—Block diagram of a typical color-TV receiver utilizing the RCA CA3067.

approximately 7 V (dc) and, with resistors R_{46} and R_{47}, establishes a bias voltage of 0.7 V (dc) at the base of Q_{29}. Because Z_1, R_{46}, and R_{47} are the feedback-loop components, they also establish the correction current that must flow in the collectors of Q_{29} and Q_{30} to provide the required voltage drop across R_{50}. The current in Q_{29} and Q_{30} is typically 1.5 mA; the current in the feedback loop is 0.5 mA. The loop gain is sufficient to keep the voltage errors small at the emitter-to-collector output junction (terminal No. 8). Within a normal range of circuit tolerances, Q_{29} and Q_{30} may have minimum values of collector-to-emitter current of approximately 1.1 mA. When external current loads are connected to terminal No. 8, no appreciable change in the voltage at this terminal occurs unless the maximum load current exceeds 1.1 mA.

When there is a high-current drain at terminal No. 8, the collector voltage of Q_{30} decreases and the reduced bias to Q_{29} may cut off Q_{29}. Consequently, excessive loading at terminal No. 8 can bias Q_{29} and Q_{30} out of their feedback range of operation. For this reason, loads that draw current in excess of 1.1 mA are not recommended.

Demodulation and Matrix

The demodulator is a balanced type that provides both positive and negative color-difference output signals. The chroma signal of terminal No. 14 is applied to the chroma amplifier transistors Q_{13}, Q_{14}, Q_{20}, and Q_{21} [Fig. 2(b)]. These chroma amplifiers provide the emitter drive to the demodulator-switching transistors Q_{15}, Q_{16}, Q_{17}, and Q_{18} in the B-Y demodulator and Q_{22}, Q_{23}, Q_{24}, and Q_{25} in the R-Y demodulator. Transistors Q_{22} and Q_{25} sum the positive output of the R-Y demodulator in resistors R_{38} and R_{39}. The transistors Q_{23} and Q_{24} provide the negative output voltage of the R-Y demodulator across the load resistors R_{37} and R_{32}.

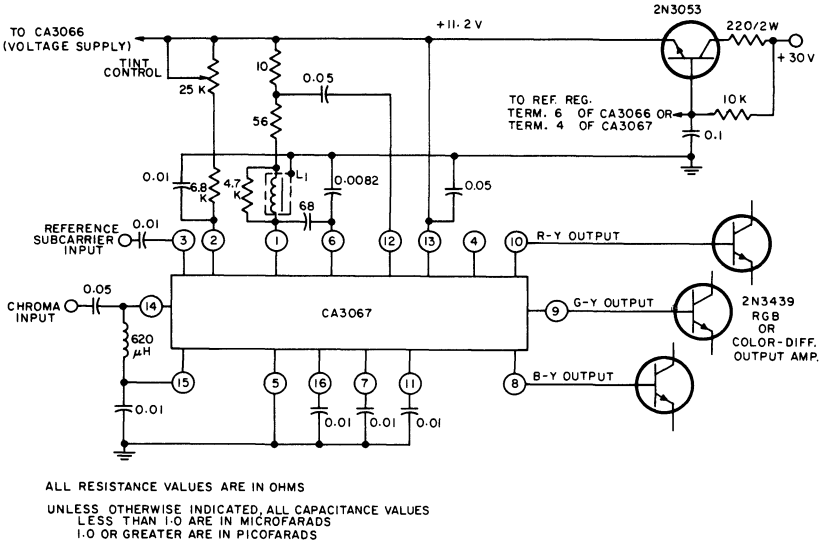


Fig. 2(a)—RCA-CA3067 in a typical application.

The positive output voltage of the B-Y demodulator provided by Q_{16} and Q_{17} is developed across the load resistor R_{33}, and the negative output voltage is the sum of the Q_{15} and Q_{18} outputs developed across resistor R_{32}. Thus, the addition of the negative outputs of the R-Y and B-Y demodulators provides the G-Y color difference signal. In this process, the negative outputs of the B-Y and R-Y demodulators are added in a ratio of 1.05:2.25, which are, respectively, the resistance values of R_{32} and $R_{32} + R_{37}$. Fig. 3 shows the vector additions of the complementary R-Y and B-Y color-difference signals that yield the G-Y color-difference signal. The matrix circuit at the CA3067 demodulator stages establishes the ratio of R-Y to B-Y color-difference signals as 1.0:1.2. This value is the ratio of $R_{38} + R_{39}$ to R_{33} resistance values, which are 6.7 and 8.2 kilohms, respectively.

An internal matrix circuit may, at first, appear to be disadvantageous. However, the ability to process uniform monolithic resistors on a single chip makes it desirable to matrix the R-Y and B-Y for the G-Y color-difference signal and to set a fixed ratio for all color-difference signals at the demodulator stages. The ratio of color-difference signal amplitudes at terminal Nos. 8, 9, 10 is easily modified by alteration of the gain- controlling circuit components that are either added to or used as a part of the high-level output stages.

The angle of demodulation is determined by the user's choice of reference-subcarrier phase applied to terminal Nos. 6 and 12. The signal input at terminal No. 6 relative to that of terminal No. 12 must be of opposite polarity to provide the same demodulation angle in each of the two demodulators. The CA3067 is presently being used in systems having demodulation angles separated by more than 90°. The reference-subcarrier signal at terminal No. 6 is displaced by 76° relative to the signal at terminal No. 12. This displacement produces a demodulation angle of 0° and (180° – 76°) or 104° in the B-Y and R-Y demodulator stages. This phase relationship relative to the color-difference signal amplitudes at terminal Nos. 8, 9, and 10 (which are respectively the B-Y, G-Y, and R-Y color-difference output terminals) is shown in the polar plot of Fig. 3.

Fig. 4 shows the typical demodulator voltage linearity and amplitudes at terminal Nos. 8, 9, and 10 for the circuit of Fig. 2(a). For a 76° phase difference of the voltage at terminal No. 6 relative to the voltage at terminal No. 12, (which is a 104° separation of the demodulation angles), the G-Y amplitude relative to the R-Y amplitude is 33 per cent. In a true quadrature demodulation, when the demodulation angles have 90° of phase separation, this ratio is 37/100.

Polarity

The polarity of the color-difference output signals may be reversed by the choice of chroma drive signal to terminal Nos. 14 or 15 [Fig. 2(b)]. Both terminal Nos. 14 and 15 are accessible to permit selection of the polarity for either the grid or cathode drive to the picture tube or to minimize the cost of the phase-shift components. Terminal No. 14 is the preferred chroma-signal input terminal for an RGB system which drives the cathodes of the picture tube when the CA3066 chroma processor system is used. An rf coil or

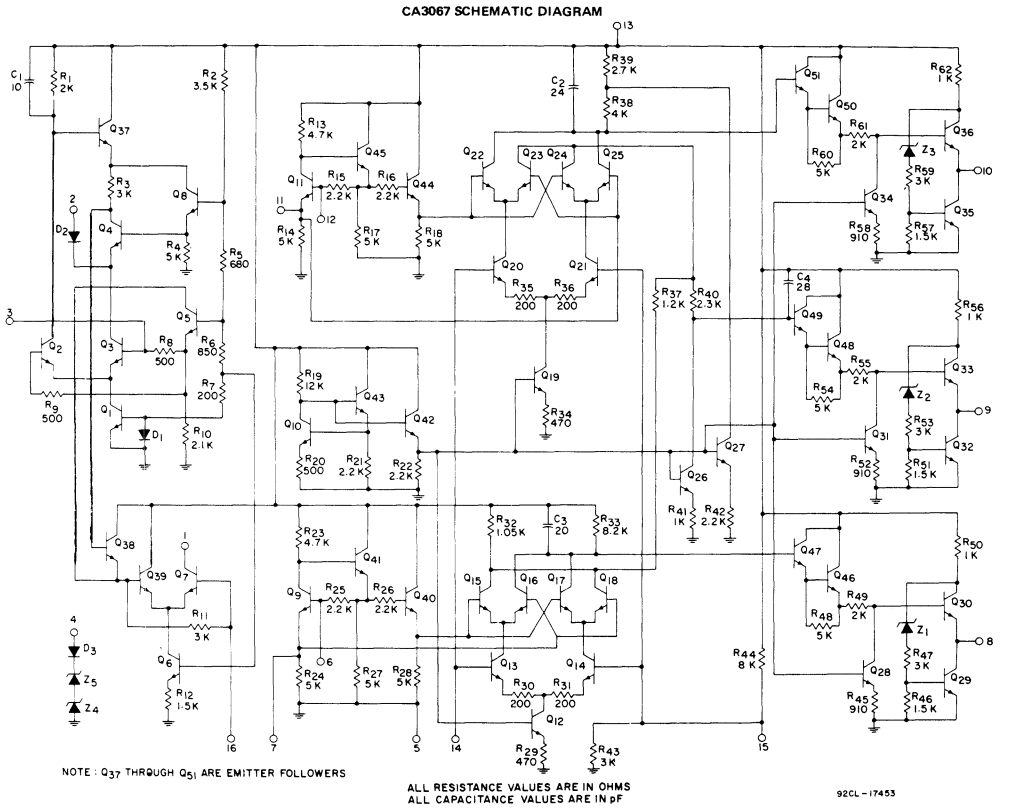


Fig.2(b)—RCA-CA3067, schematic diagram.

choke coupling is used between terminal Nos. 14 and 15. This coupling provides nearly equal bias to the chroma amplifiers Q_{13}, Q_{14}, Q_{20}, and Q_{21}. The balanced connections of the demodulators compensate for an unbalance in the external bias, if unbalance is not excessive. Resistors R_{43} and R_{44} may cause some signal loss when terminal No. 15 is the chroma-input terminal. The input impedance, however, is approximately 10 times greater than the output impedance of the chroma amplifier of the CA3066.

Filtering Capacitors

Capacitors C_2, C_3, and C_4 serve as ripple filters to reduce the 3.58-MHz and higher harmonic components of demodulation. The tolerance of the RC time constant is set for a minimum bandwidth of 450 kHz. Even without precise control over the RC time constant, there are three important advantages for the use of monolithic capacitor filtering at the output of the demodulator stages. First, ripple filtering before the output amplifiers extends the linear dynamic-voltage-swing capability of the output stages of the CA3067. Second, a savings in cost is realized because no added external ripple filter components are required. Third, the performance of the RGB high-level amplifier system is improved by the very low drive impedance from the output of the CA3067. This low output impedance is not degraded because no external filtering components are needed.

Demodulator Preamplifier

The R-Y and B-Y demodulators are driven by their respective subcarrier preamplifiers, which are transistors Q_{11}, Q_{44}, Q_{45}, and Q_9, Q_{40}, Q_{41} [Fig. 2(b)]. Although the preferred signal-drive voltage level is approximately 2.5 mV (rms), as little as 1.0 mV (rms) of signal at terminal Nos. 6 and 12 provides efficient demodulator conversion gain. Curves of the demodulation sensitivity as a function of signal levels at terminal No. 12 are shown in Fig. 5. These curves are determined from the circuit shown in Fig. 2(a). The drive voltage is applied to terminal No. 3 of the tint-control amplifier.

Each subcarrier preamplifier has a voltage gain of 100 when operated as a common-emitter amplifier having termi-

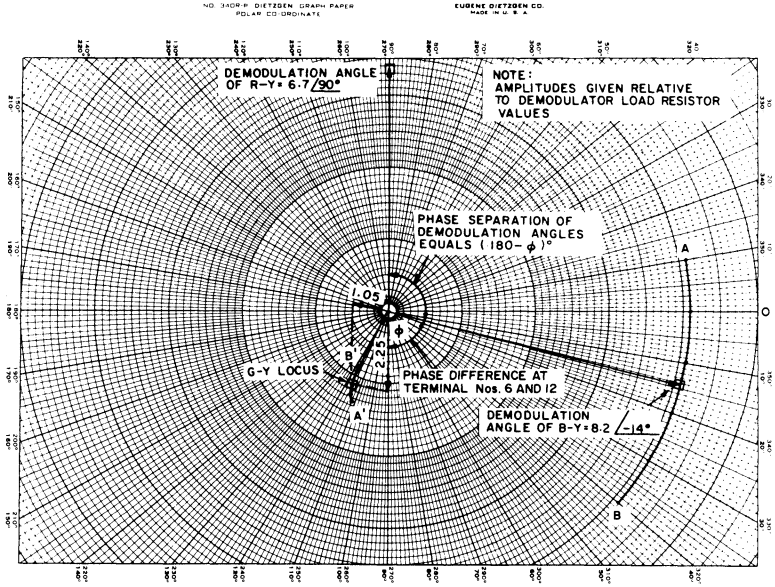


Fig.3—Vector plot of color-difference signals.

nal Nos. 7 and 11 bypassed for rf. Because of the collector-to-base feedback, each subcarrier preamplifier has a low input impedance which is a function of the amplifier gain. Terminal Nos. 6 and 12 have drive requirements of a few millivolts; there are no disadvantages associated with input attenuation caused by the low input impedance. Phase shift of the injected subcarrier caused by stray capacitance coupling is minimized.

Tint Control Amplifier

The tint-control section of the CA3067 contains the phase-shift and limiting-amplifier circuits that control the reference subcarrier signal (3.58-MHz). This signal is received from the CA3066 oscillator circuit and is adjusted to a nominally correct phase reference for the CA3067 tint-control system. The phase errors caused by transmission, circuit tolerance, and oscillator drift are corrected by the tint control. The tint control in the CA3067 circuit is a potentiometer which controls the direct current flowing into terminal No. 2. The 3.58-MHz signal is ac-coupled to the

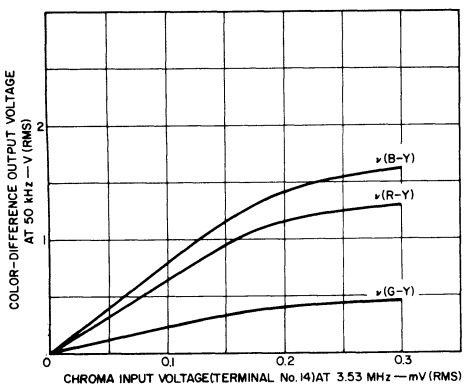


Fig.4—Demodulation linearity.

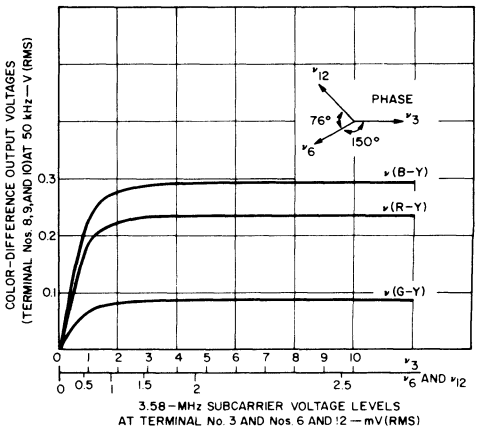


Fig.5—Demodulation sensitivity as a function of subcarrier signal level at terminal No. 3 and terminal Nos. 6 and 12.

tint-control amplifier input terminal No. 3. The amplitude-limited output signal is available at the collector of Q_7, terminal No. 1 [Fig. 2(b)].

The 3.58-MHz signal is differentially amplified following its injection into the base of Q_3, which is common to terminal No. 3. The differential amplifier consisting of Q_2 and Q_3 amplifies and divides the reference-subcarrier signal into two out-of-phase components. The current into the collector of Q_2 is in phase with the base current of Q_3; the current into the collector of Q_3 is out of phase with the base current of Q_3. Resistor R_1 in parallel with the cumulative circuit stray capacitance and the capacitance of C_1 form an RC time constant which causes a phase delay of approximately 45° at the collector of Q_2. Thus, the two components of the reference-subcarrier signal current are the "delayed phase" at the collector of Q_2 and the "reverse-phase" at the collector of Q_3. The "reverse-phase" signal current is divided between the diode D_2 and the emitter of Q_4 at the collector of Q_3; the amount of this division depends on the position of the tint-control adjustment. The divided current that passes through diode D_2 is bypassed to ground at terminal No. 2. The "delayed-phase" signal current at the collector of Q_2 is amplified in Q_{37} (an emitter-follower) and added to the "reverse-phase" signal which is present at the collector of Q_4. Because the current flow in the collector of Q_3 is typically 1.0 mA, the resistance range of the tint control shown in Fig. 2(a) is adequate for the full range of adjustment desired.

The vector addition of the "delayed-phase" and "reverse-phase" signals provides a controlled phase shift that is typically 105°. Fig. 6 shows the phase diagram for the minimum and maximum settings of the tint control. Vector B, in Fig. 6, is the maximum "reverse-phase" signal amplitude that may be obtained at the collector of Q_4 [Fig. 2(b)] and vector A is the "delayed-phase" signal amplitude. The relative voltage amplitude of each phase-separated signal is proportional to the load impedances at the collectors of Q_2 and Q_4. The "reverse-phase" signal amplitude is approximately two times greater than that of the "delayed phase". A minimum adjustment of the tint control will decrease the "reverse phase" signal at the collector of Q_4 to approximately zero amplitude. The resultant vector is determined from the addition of the "delayed–phase" and "reverse-phase" signals at the collector of Q_4 and may be any vector between vectors A and C shown in Fig. 6.

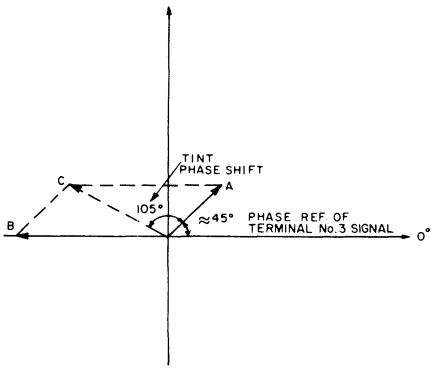


Fig.6—Vector addition of tint-control amplifier.

The resulting signal for any setting of the tint-control adjustment is amplified in the limiter-amplifier circuit consisting of Q_{37}, Q_{38}, and Q_{39} [Fig. 2(b)]. There is no further phase shift in the limiter-amplifier, which serves to limit any amplitude modulation of the reference-subcarrier signal, including the amplitude variations caused by the tint-control adjustment. The complete tint-control amplifier circuit limits the output signal at terminal No. 1 when the input signal amplitude at terminal No. 3 is greater than 7.0 mV (rms). Characteristic curves of the limiting of the CA3067 tint-control amplifier are shown in Fig. 7. In addition, curves of phase as a function of frequency are shown in Fig. 8.

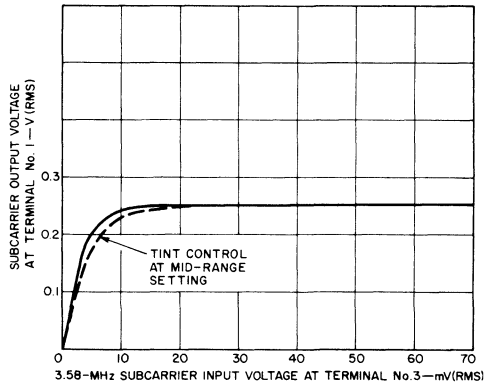


Fig.7—Limiting-characteristic curve for tint-control amplifier.

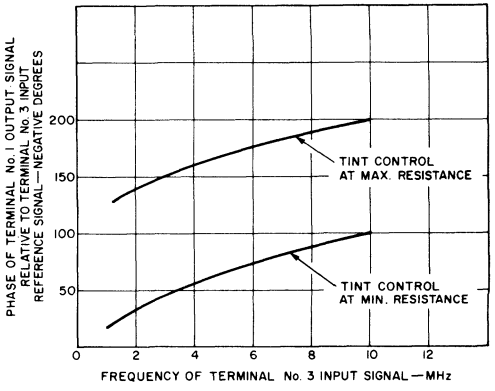


Fig.8—Typical phase characteristic of the tint-control amplifier as a function of frequency.

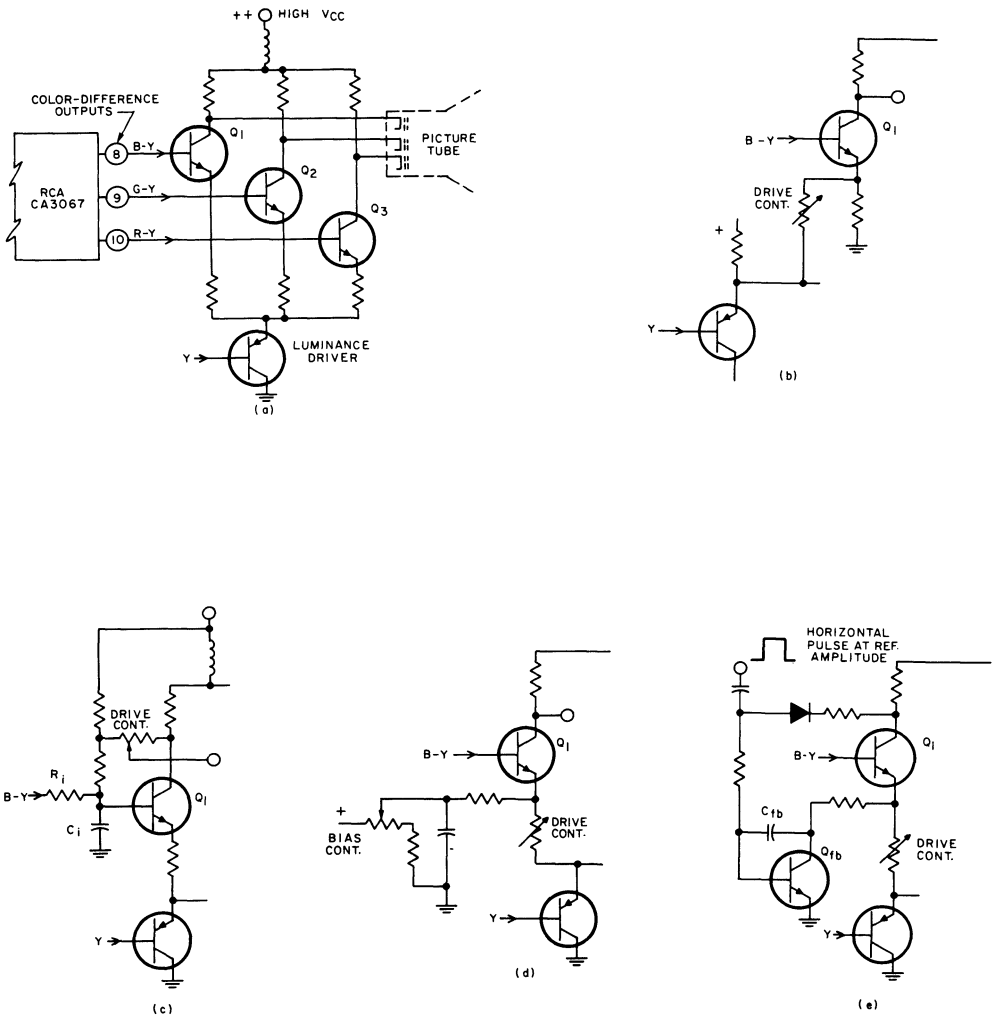


Fig.9—Use of RCA-CA3067 in RGB system of color drive to the picture tube: (a) basic systems; (b) emitter-drive control; (c) collector-feedback drive control; (d) emitter drive and bias controls; (e) automatic bias and drive control in the RCA CTC46 and CTC49 color-TV receivers.

The circuit of Fig. 2(a) shows one possible method of providing phase separation of signals to the R-Y and B-Y subcarrier amplifier. The tint-control amplifier output signal, which is the processed reference subcarrier, is separated in an RLC signal-tuned circuit that provides a phase separation of 76° at terminal Nos. 6 and 12. This circuit is considered a preferred matching network because it relates to the published data characterization. However, it is an arbitrary choice which yields the desired amplitude and phase separation to match the tint-control amplifier to the R-Y and B-Y subcarrier amplifiers. Fixed-tuned RC or delay-line circuits may also be considered as possible matching networks to meet the application needs in other systems which include monitoring equipment and test instruments.

CA3067 Application in RGB Color System

The basic connections for an RGB system are shown in Fig. 9(a). The CA3067 output amplifiers are direct-coupled to the RGB output amplifier circuits. Regardless of the direct-coupled bias considerations, it is always necessary to provide drive control to obtain proper gray-scale tracking. This control is accomplished by the adjustment of the relative gains of the RGB amplifiers. Usually the emitter or collector resistors are varied for gain-control adjustment. The emitter-resistor adjustment provides feedback gain control, and the collector-resistor adjustment is used for either attenuation or feedback control. Four different drive control methods are shown in Figs. 9(b) through 9(e).

When a design-center drive condition is established, the circuit of Fig. 9(b) is correct for center-value components. The dc shift at the limit adjustments of the drive control resulting from component tolerance require other supplementary adjustments such as a grid-to-cathode voltage adjustment at the picture tube. Fig. 9(c) shows a circuit that uses voltage feedback to stabilize the bias. Because an isolation resistance R_i must be added at the base of Q_1 to develop feedback voltage at that point, a capacitor C_i may be added to peak the luminance signal response. This capacitor is not needed to filter the 3.58-MHz signal and higher harmonics of demodulation; the CA3067 has internal filtering for this purpose.

The two circuits shown in Figs. 9(d) and 9(e) illustrate a more precise method of adjustment. The circuit of Fig. 9(d) has a dc-bias control which can be adjusted to compensate for any dc change caused by the drive control. The disadvantages of this circuit are the added bias control and the adjustment interaction of the drive and bias controls. The circuit of Fig. 9(e), which is presently used in the RCA CTC-46 and CTC-49 color-TV receivers, illustrates an emitter-type drive-control adjustment and an automatic bias-control circuit which compensates for both short-and long-term drift of the output circuit. The automatic bias-control circuit samples the voltage level at the output of the RGB amplifier during the horizontal retrace period. This voltage is compared with a fixed reference, and an error signal is fed back to the emitter of Q_1. The collector of transistor Q_{fb} acts as a voltage source with the correct line-by-line value of voltage to stablize the RGB output amplifier. The feedback error from the sampling circuit is returned to the base of Q_{fb}, and provides the correction for any temperature drift as well as for the voltage error caused by the drive-control adjustment.

The design of an RGB amplifier circuit to be driven from the CA3067 depends on the economics and the performance requirements of the application. Because the CA3067 output amplifiers have a very low source impedance, networks that add to the source impedance at the CA3067 output terminals detract from the inherent advantage of the use of the CA3067. An obvious performance advantage of the circuit of Fig. 9(e) is that the added cost of the feedback and the sampling components is offset by the performance gains of a self-adjusting system. Also, rigid specifications related to thermal tracking such as leakage currents and heat sinking may be relaxed. When modular construction and trouble-free interchangeability are primary design considerations, both cost and performance advantages are realized by the use of the CA3067.

Application Notes on IC Arrays

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Applications of the RCA CA3048 Integrated-Circuit Amplifier Array

by
L. Kaplan

The RCA CA3048 integrated circuit is an array of four identical amplifiers, each with independent inputs and outputs, all on a single monolithic silicon chip. The circuit is housed in a 16-lead dual-in-line plastic package. It has an operating and storage temperature range of -25°C to +85°C. Each amplifier in the array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The noise in the CA3048 is inherently very low and is tightly controlled in rigorous factory and quality-control testing.

The combination of low noise, high gain, and high input impedance make, the CA3048 a very versatile unit. and numerous applications suggest themselves for its use.

CIRCUIT DESCRIPTION

Fig. 1 shows the complete schematic of the CA3048 integrated-circuit amplifier array. Each amplifier (A_1 through A_4) provides two stages of voltage gain.

The input stage is basically a differential amplifier with a Darlington transistor added on the one side. The output stage consists of a combination of three transistors and associated resistors connected in an inverting configuration. For example, in amplifier A_3, Q_{19} is the Darlington input transistor, and Q_{20} and Q_{21} are the differential-pair transistors. The load resistor R_{29} for the differential input stage is located in the collector lead of transistor Q_{20}. Transistors Q_{13}, Q_{14}, and Q_{17} are used in the output stage. Transistor Q_{17} is the actual output transistor; transistors Q_{13} and Q_{14} raise the input impedance of the output stage so that the loading of the 30,000-ohm source resistance R_{29} (i.e., load resistor for the differential-amplifier input stage) is small. The ratio of total collector resistance to emitter resistance $[(R_{31} + R_{38})/R_{50}]$ in the output stage is 1000/200, or 5. In view of the small source loading, the stage gain, therefore, is essentially equal to 5.

A feedback network (R_{41}, R_{42}, R_{46}, and D_7) is connected between the output terminal and the base of transistor Q_{21}. The resistor values are chosen so that the output transistor is biased at approximately 5 milliamperes for maximum dynamic range. Diode D_7 compensates for variations in the base-to-emitter voltage of Q_{21} with changes in temperature. Because the other transistor (Q_{20}) of the differential amplifier has two emitter-base junctions in series, two diodes, D_3 and D_4, are required for temperature compensation. Diodes D_3 and D_4 also provide temperature compensation for the differential-pair transistor Q_1 in amplifier A_2 (similarly diodes D_5 and D_6 are shared by amplifiers A_1 and A_4).

Diodes D_3 and D_4 and diodes D_5 and D_6 are connected to their respective inputs through a relatively stiff voltage divider (for amplifier A_3, the divider consists of R_{27} and R_{28}). The input to amplifier A_3 is normally applied to the base of the Darlington transistor Q_{19}. The 100-kilohm resistor R_{37} supplies bias current to this transistor. The voltage drop across resistor R_{37} is small because of the very small base current of transistor Q_{19}.

Each amplifier of the CA3048 may be viewed as an ac operational amplifier in which a fixed resistance is permanently connected between the output and the inverting input. The built-in feedback resistor delimits the characteristics of the CA3048 amplifiers in the following ways:

1. The impedance as viewed from the noninverting input terminal consists mainly of the 100 kilohm input-bias resistance (R_{13}, R_{15}, R_{37}, or R_{39}). This resistance is shunted by the input capacitance of approximately 10 picofarads and the additional resistive loading presented by the input impedance of the Darlington input pairs. When the amplifier is operated under open-loop conditions (inverting input at ac ground), the total input impedance consists of 90 kilohms in shunt with the input capacitance. When the built-in feedback loop is allowed to function (by insertion of an unbypassed resistance in the noninverting input lead), then the loading caused by the Darlington input pairs is reduced, and the input resistance rises asymptotically towards 100 kilohms.
2. The impedance as viewed from the inverting input terminal is small (in the order of 40 to 50 ohms.)
3. When the CA3048 is used in its normal mode of operation, each amplifier in the array may be represented by the equivalent circuit shown in Fig. 2. (The capacitances shown are the sum of the device capacitances, socket capacitances, and stray capacitances.) The transconductance G_m, which is equal to the product of the voltage gain and the output conductance (10^{-3}mho), is typically 0.8 mho at midband.

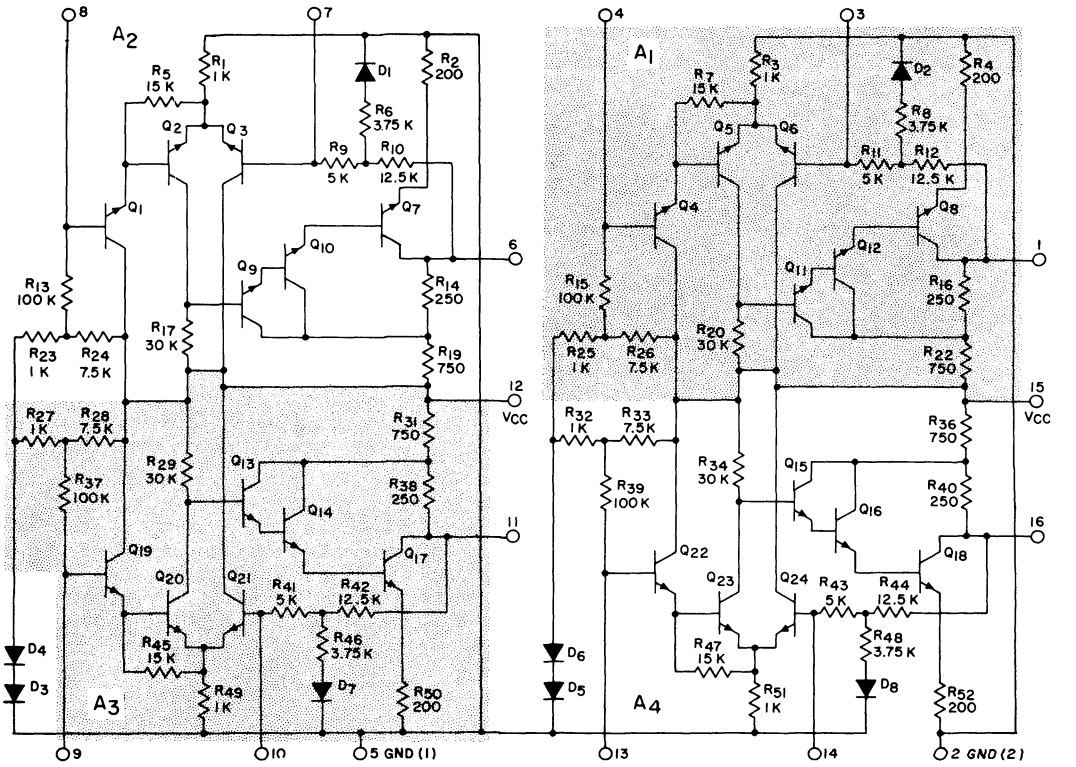


Fig. 1 - Schematic of the CA3048 integrated-circuit amplifier array.

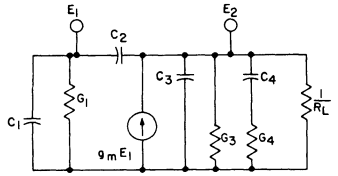


Fig. 2 - Equivalent circuit of a CA3048 amplifier.

GAIN-FREQUENCY RESPONSE

Curves of the transconductance of any amplifier in the CA3048 array as a function of frequency up to 30 MHz show two break points. At frequencies above the first break point, which occurs at 300 kHz, the transconductance rolls off at a rate of 6 dB per octave to 12 MHz. At frequencies above 12 MHz, the rate of roll-off increases to 12 dB per octave. At frequencies up to 12 MHz, therefore, the transconductance of any amplifier in the CA3048 array is expressed by the following equation:

$$g_m = \frac{\omega_o g_{mo}}{\omega_o + S} \qquad (1)$$

where S is the complex frequency, g_{mo} is the mid-band transconductance, and $\omega_o = 2\pi \times 300 \times 10^3$.

Fig. 3 shows the open-loop transconductance for an amplifier in the CA3048 array as a function of frequency. This response indicates potential uses of the CA3048 integrated circuit at frequencies that extend into the video range.

STABILITY

The equivalent circuit shown in Fig. 2 can be used to determine the stability of the amplifiers in the CA-3048 array under various conditions of loading when undesirable external capacitance is present in the wiring and socket. With no external generator connected to the circuit, the input conductance G_1 is equal to 1/100000 mho, and the output conductance G_3 is equal to 1/1000 mho (for amplifiers A_1, A_2, A_3, or A_4, respectively, G_1 is equal to $1/R_{15}$, $1/R_{13}$, $1/R_{37}$, or $1/R_{29}$, and G_3 is equal to $1/(R_{16} + R_{22})$, $1/(R_{14} + R_{19})$, $1/(R_{31} + R_{38})$, or $1/(R_{36} + R_{40})$. The capacitance C_4 and the conductance G_4 shown in Fig. 2 represent an external damping network which can be varied or deleted as demanded by stability or gain-bandwidth requirements.

A necessary and sufficient condition for a system to be stable is that the roots of the characteristic equation of the system have no positive real parts. The characteristic equation for the circuit of Fig. 2 is obtained by expansion of the circuit determinant and collection of the coefficients of the complex frequency S. The equation assumes the following form:

$$A_1 + A_2S + A_3S^2 + A_4S^3 + A_5S^4 = 0 \qquad (2)$$

After much tedious algebra, the coefficients are determined as follows:

$$A_1 = \omega_o G_1 G_3 G_4$$

$$A_2 = \omega_o G_4 [G_3(C_1 + C_2) + G_1(C_2 + C_3) - g_{m_o} G_2] + G_1 G_3 (C_3 \omega_o + G_4)$$

$$A_3 = \omega_o \{C_2 C_3 (G_1 + G_3 + G_4 - g_{m_o}) + C_1 [C_3(G_3 + G_4) + C_2 G_4]\} + G_4 [G_3(C_1 + C_2) + G_1(C_2 + C_3)] + G_1 G_3 C_3$$

$$A_4 = G_4 [C_1(C_2 + C_3) + C_2 C_3] + C_3 [C_1(\omega_o C_2 + G_3) + C_2(G_1 + G_3)]$$

$$A_5 = C_1 C_2 C_3 \qquad (3)$$

With the aid of a computer, it is possible to check very quickly many combinations of circuit values for stability by solving for the roots of Eq. (2) with different circuit values assigned to the various components.

Although there are many variables involved, it is possible to state in a general sense the results of several solutions of Eq. 2.

The system cannot oscillate without capacitor C_2 to introduce positive feedback. The analysis is reduced, therefore, to the determination of the maximum value of C_2 before oscillation occurs. With careful printed-circuit-board layout, the feedback capacitance C_2 is small, and the system is usually stable. If a socket is used the feedback capacitance is greatly increased, and

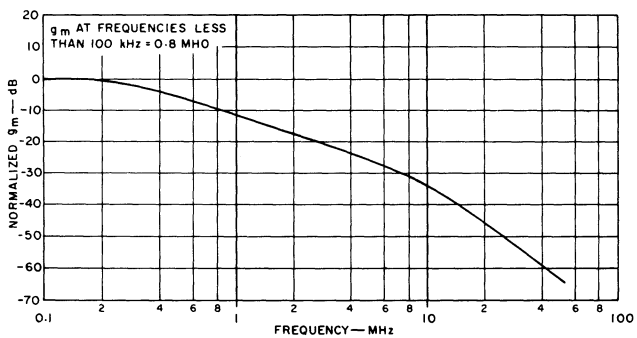


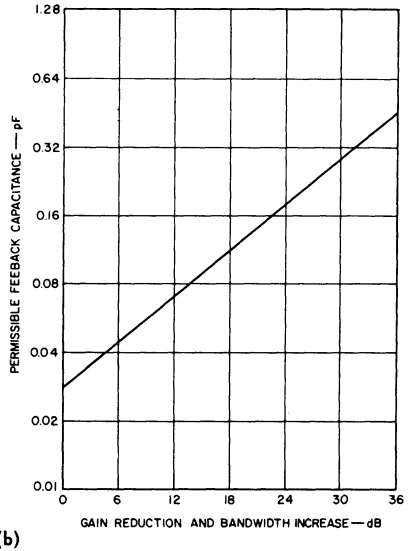
Fig. 3 - Typical gain-frequency response for a CA3048 amplifier.

stabilization of the circuit is generally required.

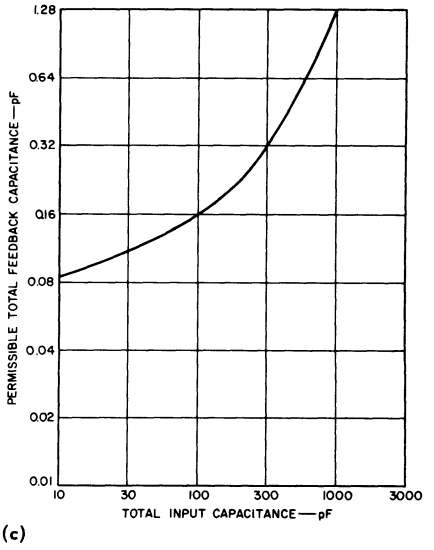
As with any two-port network, any increase in source or load conductance aids stability. In addition, analyses of Eq. (2) show that addition of shunt capacitance at the input is a very effective stability technique when the source impedance is high. Introduction of negative feedback into the circuit [which is simulated in Eq. (2) by a decrease in the value assigned to the transconductance g_m and an increase in the cutoff frequency] also improves circuit stability.

Another stability method, which is effective for any source impedance or gain value, is the addition of a damping network such as that formed by capacitance C_4 and conductance G_4 in Fig. 2. In this method, the value of C_4 is chosen so that its reactance is equal to the parallel combination of R_3 and R_L at the highest frequency of desired amplification. The value of R_4 is made small so that the gain is reduced at high frequencies and is typically 1/10 or 1/20 the value of the parallel combination of R_3 and R_L.

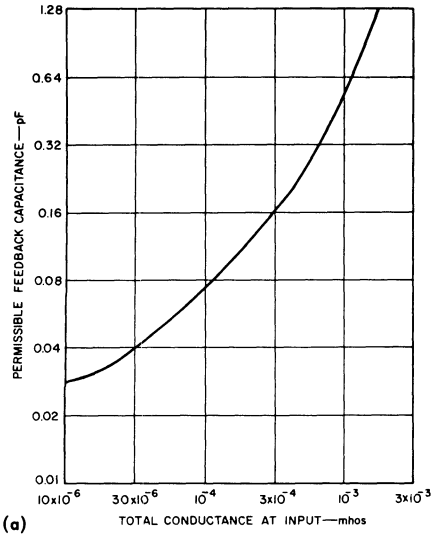
The series of curves in Fig. 4 show the results of the computation for the roots of E_q. (2). It should be noted that the maximum value shown for capacitance C_2 is that obtained just before oscillation occurs. Severe peaking of the response (or ringing) may result before the listed value of C_2 is reached. It is advisable, therefore, to maintain the capacitance of C_2 well below the indicated value.



(b)



(c)



(a)

Fig. 4 - Stability curves for a CA3048 amplifier: (a) permissible feedback capacitance as a function of the total conductance at the input; (b) permissible feedback capacitance as a function of gain reduction and of bandwidth increase; (c) permissible feedback capacitance as a function of the total input capacitance.

OUTPUT SWING VS. SUPPLY VOLTAGE

Fig. 5 shows the output voltage for any one of the CA3048 amplifiers as a function of supply voltage. The solid lines represent the performance obtained with the full open-loop gain. The dotted line shows the improvement obtained when 12 dB of negative feedback is added by inclusion of a 150-ohm unbypassed resistor in the inverting-input lead. The values obtained for this curve are those which prevail when the output is loaded only by the measuring equipment. It should be realized that any substantial loading will tend to reduce the magnitude of the available output voltage for equivalent distortion figures. For example, an additional 1000-ohm load exactly balances the internal load resistor, and would reduce the available output voltage by 50 per cent.

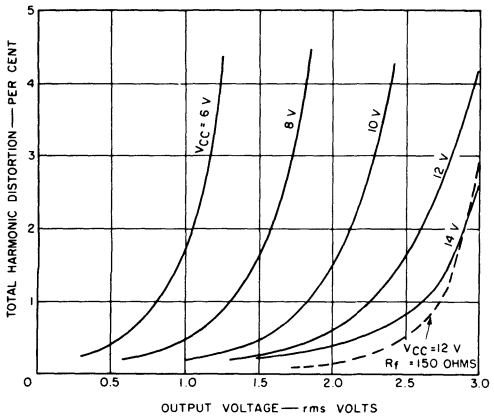


Fig. 5 - Total harmonic distortion of a CA3048 amplifier as a function of output voltage for different value of dc supply voltage.

NOISE

Fig. 6 shows output noise obtained when a single amplifier of the CA3048 is operated at 40 dB gain into a "C" filter. Table I shows typical values of noise voltage (E_{noise}) and current (I_{noise}) for the CA3048 at spot frequencies of 10, 100, 1000, 10000, and 100000 Hz. From these values, the equivalent input noise voltage for any value of source resistance may be computed by use of the following equation:

$$E_{equiv} = \sqrt{(E_{noise})^2 + (I_{noise}\, R_{source})^2} \qquad (4)$$

Laboratory measurements have shown that the noise performance of the CA3048 is not significantly affected by variation of the supply voltage. The values shown in Fig. 6, therefore, may be used with supply voltages down to about 2 volts if it is remembered that the open-loop gain decreases to about 35 dB at a supply voltage of 2.5 volts.

TABLE I

TYPICAL NOISE VOLTAGE AND CURRENT FOR AN AMPLIFIER IN THE CA3048 ARRAY

Frequency (Hz)	E_{noise} (volts)	I_{noise} (amperes)
10	30.5×10^{-9}	7.5×10^{-12}
100	17×10^{-9}	4.3×10^{-12}
1000	8×10^{-9}	1.2×10^{-12}
10000	6×10^{-9}	0.5×10^{-12}
100000	4×10^{-9}	0.3×10^{-12}

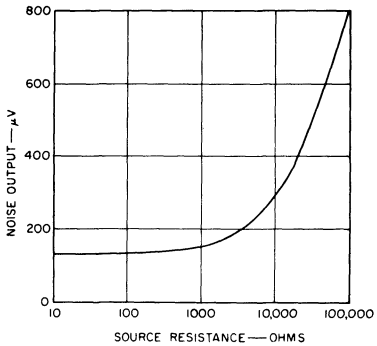


Fig. 6 - Noise output as a function of source resistance for a CA3048 amplifier.

CIRCUIT APPLICATIONS

In all the foregoing discussions, a single amplifier has been described as though it existed alone. The CA3048, however, consists of four separate amplifiers, which may be used independently or in combination. A glance at the complete schematic of the CA3048 reveals other aspects worthy of consideration.

Two supply-voltage terminals and two ground terminals are indicated. Terminal No. 12 supplies the V_{CC} voltage to amplifiers A_2 and A_3, and terminal No. 15 supplies the V_{CC} voltage to amplifiers A_1 and A_4. The ground return for amplifiers A_1 and A_4 is provided by terminal No. 2; all other ground returns are provided by terminal No. 5.

When two units are cascaded, it is preferred to let amplifiers A_2 and A_3 be the input units, and amplifiers A_1 and A_4 be the output units. This arrangement permits separation of both the V_{CC} and ground lines for low- and high-level signals.

If resistive decoupling is used, amplifiers A_2 and A_3 can be operated at lower V_{CC} voltages to effect a savings in current consumption.

Hartley Oscillator

The Hartley oscillator is easily designed and constructed using the CA3048 amplifier. No feedback capacitor is required, and it is possible to extract "square", sawtooth, or sinusoidal waveshapes.

In the circuit shown in Fig. 7, the tap on the coil is located at one-fourth the total turns, capacitors C_1 and C_2 provide dc blocking, and capacitor C_3 tunes with inductor L_1 ($\omega_o = 1/\sqrt{L_1C_3}$). When the circuit is operated from a 12-volt supply, the output voltage is a clipped sine wave that has a peak-to-peak value of about 7 volts. The voltage at the inverting input is a sawtooth that has a peak-to-peak value of about 0.300 volt. If an unclipped sine wave is desired, it is available across the coil L_1. A sine wave can be obtained in the single-ended connection if the value of C_2 is made large with respect to C_3 so that it effectively bypasses the sawtooth to ground; the voltage across L_1 is then sinusoidal with respect to ground.

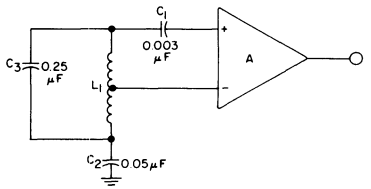


Fig. 7 - Hartley oscillator.

Colpitts Oscillator

A tunable Colpitts oscillator is readily designed using one of the amplifiers of the CA3048 array. Fig. 8 shows an example of the CA3048 used in this way. Capacitors C_1 and C_2 are dc blocking capacitors; the series combination of capacitors C_3 and C_4 resonates with coil L. The ratio of C_3 to C_4 determines the relative amounts of signal fed back to the two inputs, and may be chosen on the basis of stability or strength of oscillation.

For the component values shown in Fig. 8, the frequency of oscillation is 33.536 kHz with a 12-volt supply and decreases to 33.546 kHz when the supply voltage is reduced 25 per cent to 9 volts.

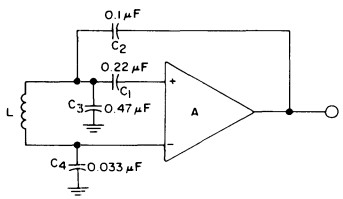


Fig. 8 - Colpitts oscillator.

Three waveshapes are available from the Colpitts oscillator. A sawtooth waveform is obtained at the output, a sinusoidal waveform is obtained at the inverting input, and a clipped sinusoidal waveform appears at the noninverting input.

Astable Multivibrator

The CA3048 may be connected as an astable multivibrator with the addition of only two external components. An example of this type of operation is shown in Fig. 9.

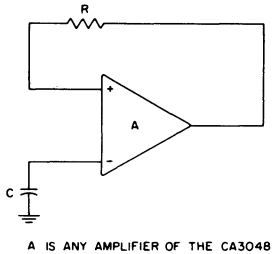


Fig. 9 - Astable multivibrator.

The resistor R introduces positive feedback into the circuit, and the capacitor C sets the period of the waveform. The operation of the circuit can be explained more easily if it is assumed that transistor Q_{17} (of amplifier A_3) has just turned OFF so that the voltage at terminal No. 11 becomes very positive. This positive voltage is fed through R to the base of Q_{19} to maintain the conduction of this transistor and to hold transistors Q_{21}, Q_{13}, Q_{14}, and Q_{17} cut off. Meanwhile, capacitor C charges through the internal bias resistors R_{41} and R_{42}. When the voltage on capacitor C reaches the level at which transistor Q_{21} begins to become forward-biased, some current is diverted from Q_{20} to Q_{21} and Q_{13}, Q_{14}, and Q_{17} begin to turn ON. The action is regenerative because the negative-going voltage from the collector of Q_{17} feeds a negative-going signal back to the base of Q_{19} to enhance the switching action. When C discharges to the point at which Q_{21} turns OFF, Q_{20} begins to turn ON and the process repeats itself.

Two waveforms are available from the astable multivibrator circuit, both at low impedance. A rectangular waveform that has a peak-to-peak amplitude of 7 volts or greater is obtained from the output terminal. The waveform available at the inverting input is an isosceles triange that has a peak-to-peak amplitude of approximately 0.220 volt.

With the circuit as shown, reliable oscillation is obtained for values of the resistor R in the order of 2.2 megohms, with supply voltages as low as six volts.

4-Channel Linear Mixer

Fig. 10 illustrates the use of the CA3048 as a linear mixer. Each input is connected to its own CA3048

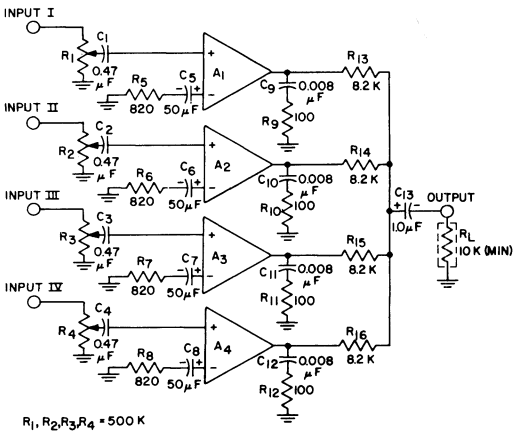


Fig. 10 - Linear mixer.

amplifier through the gain-control potentiometers R_1, R_2, R_3, and R_4. Capacitors C_1, C_2, C_3, and C_4 block the dc voltage at the inputs.

The gain of any input to the corresponding output is 20 dB for the circuit values shown and a load impedance of 10000 ohms or greater. Resistors R_5, R_6, R_7, and R_8 program the gain of the system, and may be varied to provide more or less gain, depending on the requirements of the application. The curve in Fig. 11 illustrates the effect of variation in the resistance in the feedback circuit of the CA3048. The difference in the 20 dB gain indicated for the mixer circuit and the approximately 34 dB shown in Fig. 12 results from the loss in the combining circuit that consists of R_{13}, R_{14}, R_{15}, R_6, and R_L.

A resistor-capacitor combination (R_9, C_9, R_{10}, C_{10}, R_{11}, C_{11}, R_{12}, C_{12}) connected to the output of each amplifier stabilizes the amplifiers when source and load conductances are too small to provide adequate damping.

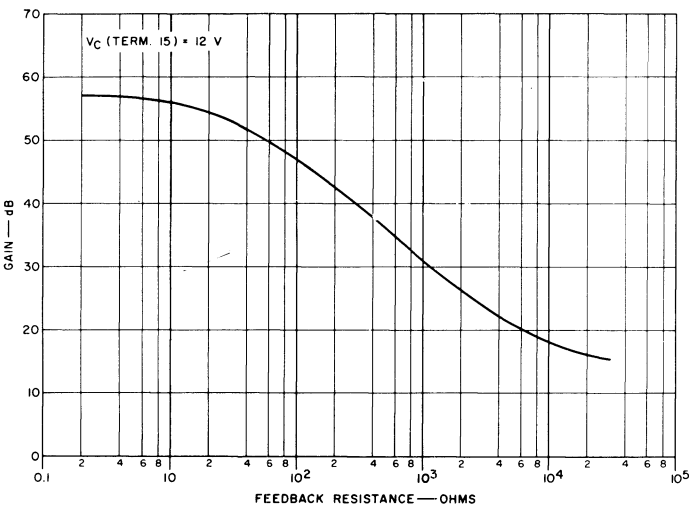


Fig. 11 - Gain of a CA3048 amplifier as a function of feedback resistance.

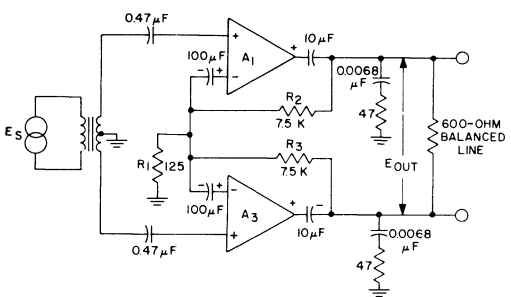


Fig. 12 - Balanced-line driver.

The input impedance of each amplifier of the CA-3048 is nominally 90 kilohms. In the linear mixer, however, the input potentiometers R_1 through R_4 are 500 kilohms. The effective impedance presented to the device, therefore, is quite high except when the circuit is adjusted for maximum gain. At this time, the impedance decreases to about 75 kilohms.

Driver for 600-ohm Balanced Line

Two amplifiers of the CA3048 may be connected to drive a 600-ohm balanced line at levels up to 1 volt rms with a gain of 40 dB. When the circuit is connected as shown in Fig. 12, the distortion is less than 1 per cent at an output level of 1 volt and a gain of 40 dB.

The output of the circuit is limited to a value slightly greater than 1 volt rms, primarily because of drive-current limitations to the output transistors. In this respect, it is self-protecting. Should a short circuit develop across the line, the circuit will not destroy itself.

Resistor R_1 in Fig. 12 is common to the output and input circuits of both amplifiers A_1 and A_3. Should a gain unbalance exist, or should the input signals be of unequal amplitude, then the outputs would tend to become unbalanced with respect to ground. For example, if amplifier A_1 had the larger output, a signal in phase with the output at A_1 would be developed across resistor R_1. In this event, the voltage developed at R_1 would tend to reduce the output of amplifier A_1 because this voltage is applied to the inverting input. At the same time, the voltage at R_1 is applied to the inverting input of amplifier A_3 and tends to increase the effective input voltage of that amplifier and, in this way, help to restore balance. The balancing effect takes place regardless of the cause of the initial unbalance.

Gain-Controlled Amplifier

Any amplifier of the CA3048 may be used as a gain-controlled amplifier in order to accommodate a wide range of input signal amplitude. Fig. 13 shows one amplifier of the CA3048 used in this type of configuration. By variation of the dc potential at the gate No. 1 of the MOS transistor Q_1, the gain of the amplifier may be varied from 14 dB to 49 dB. In this circuit, the MOS transistor Q_1 acts as a variable impedance in the feedback loop of the CA3048.

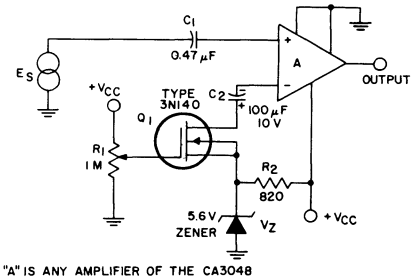


Fig. 13 - Gain-controlled amplifier.

In a circuit such as that shown in Fig. 13, the voltage gain may be expressed as follows:

$$\frac{E_o}{E_s} = \frac{A\,(R_a + R_f)}{R_f + R_a(A + 1)} \qquad (5)$$

where R_a is the equivalent resistance of the MOS transistor and R_f is the feedback resistance, which includes the internal feedback resistance of the integrated circuit together with any paralleled external feedback resistance.

As the value of resistor R_a approaches zero, the gain of the circuit approaches the open-loop gain of the amplifier (A). For very large values of resistor R_a the gain of the circuit approaches A/(A + 1), or approximately unity. The maximum theoretical agc range then is A.

The practical agc range of this circuit is limited on the high end by the "ON" resistance of the MOS transistor, and on the low end by the finite input impedance of the CA3048. In the circuit shown in Fig. 13, the range of control is 35 dB.

There is no necessity for direct current to flow in the MOS transistor, and if a low impedance source of about five volts is available, this voltage may be substituted for the Zener diode-resistor combination so that the power requirements of the circuit are further reduced.

Distortion, which is inherently low, ranges from 0.65 per cent at minimum gain (output of 2 volts rms) to 0.4 per cent at maximum gain.

APPLICATION OF THE RCA-CA3018 INTEGRATED-CIRCUIT TRANSISTOR ARRAY

BY

G.E. THERIAULT, A.J. LEIDICH, AND T.H. CAMPBELL

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers. Because the CA3018 has the feature of device balance, it is useful in special applications of the differential amplifier, and can be used to advantage in circuits which require temperature compensation of base-to-emitter voltage.

CIRCUIT DESCRIPTION AND OPERATING CHARACTERISTICS

The circuit configuration for the CA3018 is shown in Fig. 1. In a 12-lead TO-5 package, because it is necessary to provide a terminal for connection to the substrate, two transistor terminals must be connected to a common lead. The particular configuration chosen is useful in emitter-follower and Darlington circuit connections. In addition, the four transistors can be used almost independently if terminal 2 is grounded or ac grounded so that Q3 can be used as a common-emitter amplifier and Q4 as a common-base amplifier. In pulse video amplifiers and line-driver circuits, Q4 can be used as a forward-biased diode in series with the emitter of Q3. Q3 may be

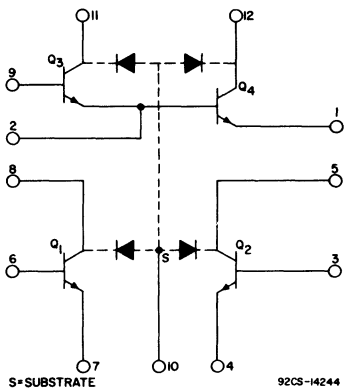


Fig. 1—Schematic diagram and TO-5 terminal connections for the CA3018 integrated-circuit transistor array.

used as a diode connected to the base of Q4; in a reverse-biased connection, Q3 can serve as a protective diode in rf circuits connected to operational antennas. The presence of Q3 does not inhibit the use of Q4 in a large number of circuits.

In transistors Q1, Q2, and Q4, the emitter lead is interposed between the base and collector leads to minimize package and lead capacitances. In Q3, the substrate lead serves as the shield between base and collector. This lead arrangement reduces feedback capacitance in common-emitter amplifiers, and thus extends video bandwidth and increases tuned-circuit amplifier gain stability.

Operating characteristics for the CA3018 are given in the technical bulletin.

CIRCUIT APPLICATIONS

The applications for the CA3018 are many and varied. The typical applications discussed in this Note have been selected to demonstrate the advantages of four matched devices available on a single chip. These few examples should stimulate the generation of a great many more applications.

Video Amplifiers

A common approach to video-amplifier design is to use two transistors in a configuration designed to reduce the feedback capacitance (appearing as a Miller capacitance) inherent in a single triode device. Three configurations which utilize two devices are (1) the cascode circuit, (2) the single-ended differential-amplifier, and (3) the common-collector, common-emitter circuit. In all three circuits, the output-to-input feedback capacitance is minimized by isolation inherent in the configuration. The availability of four identical transistors in a common package provides a convenient vehicle for these circuit configurations for video-amplifier design. Two of the many possible circuit variations are discussed below.

Broadband Video Amplifier. A broadband video-amplifier design using the CA3018 is shown in Fig. 2. This amplifier may be considered as two dc-coupled stages, each consisting of a common-emitter, common-collector configuration. The common-collector transistor provides a low-impedance source to the input of the common-emitter transistor and a high-impedance, low-capacitance load at the common-emitter output. Iterative operation of the video amplifier can be achieved by capacitive coupling of stages.

Two feedback loops provide dc stability of the broadband video amplifier and exchange gain for bandwidth. The feedback loop from the emitter of Q_3 to the base of Q_1 provides dc and low-frequency feedback; the loop from the collector of Q_4 to the collector of Q_1 provides both dc feedback and ac feedback at all frequencies.

The frequency response of the broadband video amplifier is shown in Fig. 3. The upper 3-dB break occurs at a frequency of 32 MHz. The low-frequency 3-dB characteristics are determined primarily by the values of capacitors C_1, C_2, and C_3. The low-frequency 3-dB break

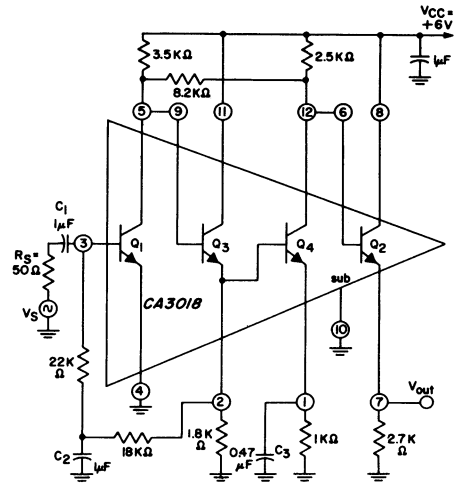


Fig. 2—Schematic diagram for a CA3018 broadband video amplifier.

occurs at 800 Hz. The mid-frequency gain of 49 dB is constant to within 1 dB over the temperature range from −55° to +125°C. The upper 3-dB break is constant at 32 MHz from −55°C to +25°C, and drops to 21 MHz at +125°C.

The total power dissipation over the entire temperature range is 22.8 milliwatts. The dc output voltage varies from 2.33 volts at −55°C to 3 volts at +125°C. The tangential sensitivity occurs at 20 microvolts peak-to-peak. The dynamic range is from 20 microvolts peak-to-peak to 4 millivolts rms at the input.

The circuit of Fig. 2 demonstrates a typical approach that can be altered, especially with regard to gain and bandwidth, to meet specific performance requirements.

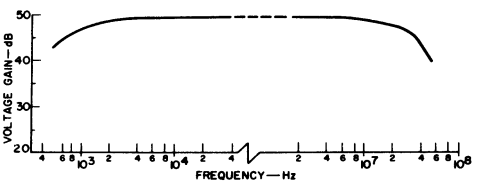


Fig. 3—Voltage gain as a function of frequency for the broadband video amplifier of Fig. 2.

Cascode Video Amplifier. The cascode configuration offers the advantages of common-emitter gain with reduced feedback capacitance and thus greater bandwidth. Fig. 4 shows a typical circuit diagram of a cascode video amplifier using the CA3018. Transistors Q_2 and Q_1 comprise the common-emitter and common-base portions of

the cascode, respectively. The common-base unit is followed by cascaded emitter followers (Q_3 and Q_4) which provide a low output impedance to maintain bandwidth for iterative operation.

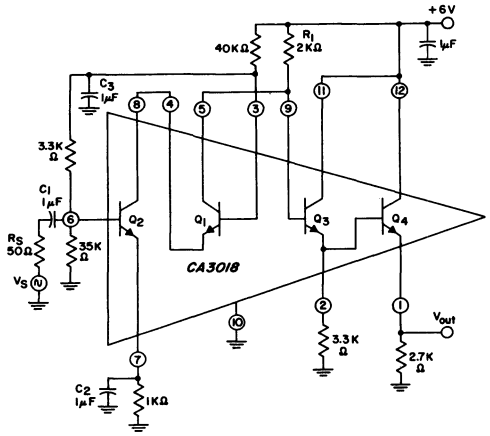


Fig. 4—Schematic diagram for a CA3018 cascode video amplifier.

The frequency response of the cascode video amplifier is shown in Fig. 5. The lower and upper 3-dB points occur at frequencies of 6 KHz and 11 MHz, respectively. The lower 3-dB point is primarily a function of capacitors C1, C2, and C3. The upper 3-dB point is a function of the devices and of the load resistor R_1, and is 10.5 MHz at −55°C and 5 MHz at +125°C.

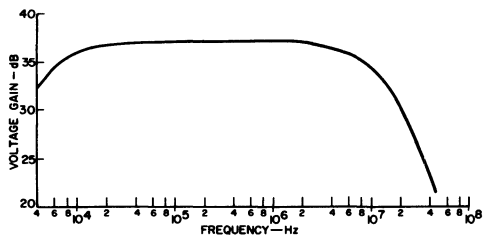
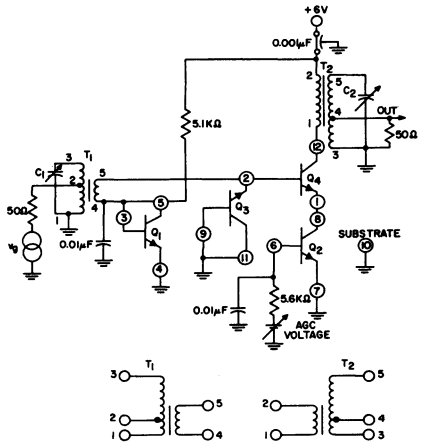


Fig. 5—Voltage gain as a function of frequency for the cascode amplifier of Fig. 4.

The mid-frequency voltage gain of the amplifier is 37 dB ± 1 dB over the temperature range from −55°C to +125°C. The power dissipation varies from 16.8 milliwatts at −55°C to 17.6 milliwatts at +125°C. The amplifier has a tangential sensitivity of 40 microvolts peak-to-peak and a useful dynamic input range from 40 microvolts to 16.6 millivolts peak-to-peak.

15-MHz RF Amplifier

Fig. 6 shows a typical design approach for a tuned amplifier for use in the frequency range of 2 to 30 MHz in military receivers. This circuit was designed for a mid-band frequency of 15 MHz to demonstrate its capability. Gain is obtained in a common-emitter stage (Q_4). Transistor Q_2 is used as a variable resistor in the emitter of Q_4 to provide improved signal-handling capability with agc. Transistor Q_1 is used as a bias diode to stabilize Q_4 with temperature, and the reverse breakdown of Q_3 as a diode is used to protect the common-emitter stage from signal overdrive of adjacent transmitters.



#22 wire on Q-2 material, CF107 Torroid from Indiana General.

C1, C2 = Arco 425 or equiv.

Fig. 6—Schematic diagram for a CA3018 15-MHz rf amplifier.

The tuned-circuit design of Fig. 6 utilizes mismatching to obtain stability. Although the usable stable gain for a common-emitter amplifier using this type of transistor is 26 dB at 15 mHz, the tuned rf amplifier was designed for a total gain of 20 dB to obtain greater stability and more uniform performance with device variations. The general performance characteristics of the circuit are as follows:

Power Gain	20 dB
Power-Gain Variation from −55 to +125°C	±1 dB

Bandwidth	315 kHz
Noise Figure at Full Gain	7.4 dB
AGC Range	45 dB
Power Dissipation	1.8 mW

Fig. 7 shows the cross-modulation characteristics of the circuit for in-band signals. For out-of-band undesired signals, the cross-modulation performance is improved by the amount of attenuation provided by the input tuned circuit. Cross-modulation performance also improves (i.e. more interfering signal voltage is required for cross-modulation distortion of 10 per cent) with increased agc as a result of the degeneration in the emitter of Q_4.

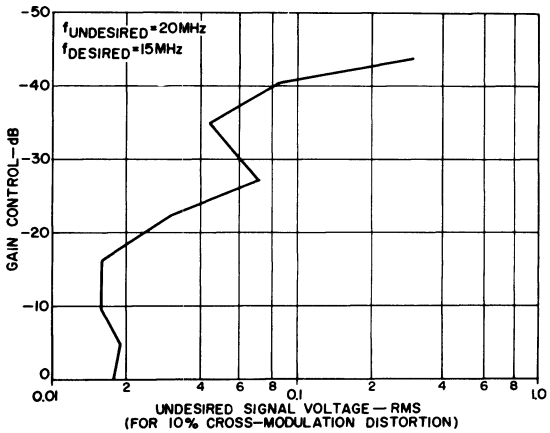


Fig. 7—In-band cross-modulation characteristic of 15-MHz amplifier of Fig. 6 (data taken with untuned input).

Final If Amplifier Stage and Second Detector

Fig. 8 illustrates the use of the CA3018 as a last if amplifier and second detector (0.1 volt emitter voltage on terminal 1). The bias on transistor Q_4 is maintained at approximately cutoff to permit the cascaded emitter-follower configuration (Q_3 and Q_4) to be used as a second detector. Because this stage is driven by a common collector configuration, the input impedance to the detector can be kept high. A low output load impedance can be used as a result of the output current capability of the cascaded emitter-follower configuration. The input impedance (terminal 9) of approximately 9000 ohms is largely determined by the bias network. A minimum if input power of 0.4 microwatt must be delivered to terminal 9 for linear operation. The audio output power for 60 per cent modulation for this drive condition is 0.8 microwatt. Linear detection is obtained through an input range of 20 dB for 60 per cent modulation. This detector arrangement requires less power-output capability from the last if amplifier than a conventional diode detector yet allows a low dc load resistor to achieve a good ac-to-dc ratio for the first audio amplifier.

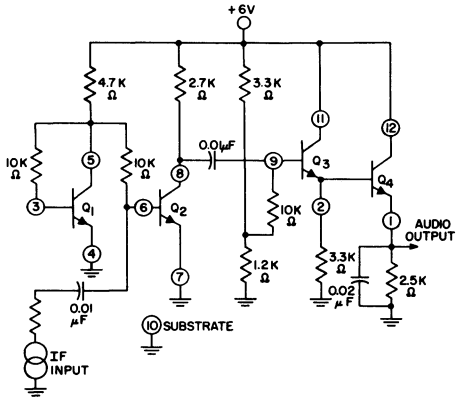


Fig. 8—Schematic diagram for a CA3018 final if amplifier and second detector.

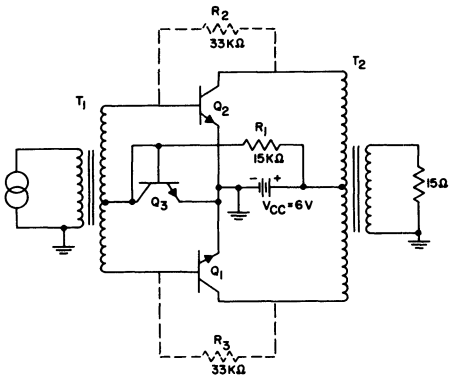
The if amplifier of Fig. 8 has a voltage gain of 30 dB at 1 MHz. Transistor Q_1 is used in the base-bias loop of the common-emitter amplifier Q_2 to stabilize the output operating point against temperature variations. This arrangement also eliminates the need for an emitter resistor and bypass capacitor, and thus provides a larger voltage-swing capability for Q_2. If Q_2 is biased conventionally with base-bias resistors, Q_1 can be made available for the first audio or agc amplifier.

Class B Amplifier

Characteristics were obtained on a low-level class B amplifier to establish the idling-current performance of nearly identical devices on a single chip with respect to temperature variations. The transistors in the CA3018 can be used only for low-power class B operation (maximum output of 40 milliwatts) because of the h_{FE} roll-off and moderately high saturation resistance at high currents. A typical circuit is shown in Fig. 9. Idling-current bias is provided to Q_1 and Q_2 by use of transistor Q_3 as a diode (with collector and base shorted) and connection of a series resistor to the supply. The idling current for each transistor in the class B output is equal to the current established in the resistance-diode loop. Because the resistor R_1 is the predominant factor in controlling the current in the bias loop, the bias current is relatively independent of temperature. In addition, because the devices have nearly equal characteristics and are at the same temperature, the idling current is nearly independent through the full military temperature range. The total idling current for transistors Q_1 and Q_2 in Fig. 9 varies from 0.5 to 0.6 milliampere from -55 to $+125$°C. Excellent balance between output devices is achieved throughout the range.

AC feedback as well as dc feedback can be obtained by substitution of two resistors R_2 and R_3 in place of R_1,

as shown by the dotted lines in Fig. 9. These two resistors, which have a parallel combination equal to R_1, are connected between collector and base of transistors Q_2 and Q_1. The added feedback reduces the power gain by approximately 6 dB (30 to 24 dB), but improves the linearity of the circuit. Although the output-power capability for the circuit shown in Fig. 9 is approximately 18 milliwatts, output levels up to 40 milliwatts can be obtained in similar configurations with optimized components.

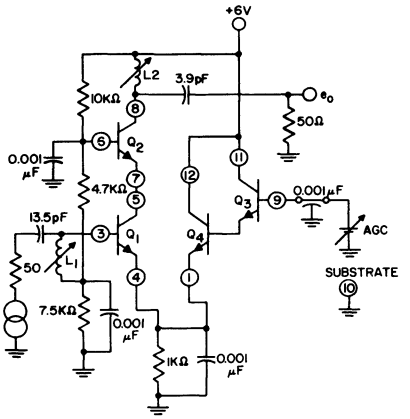


T_1 — ADC Products No. 5SX1322 or equiv.

T_2 — Chicago Standard Trans. Corp. No. TA-10 or equiv.

Note: R_1 is removed when R_2 and R_3 are added.

Fig. 9—Schematic diagram for a CA3018 class B amplifier.



L_1 = 0.11 to 0.17 μH

L_2 = 0.5 to 0.8 μH

Fig. 10—Schematic diagram for a CA3018 100-MHz cascode amplifier.

100-MHz Tuned RF Amplifier

Fig. 10 illustrates the use of the CA3018 in a 100-MHz cascode circuit with an agc amplifier. Transistors Q_1 and Q_2 are used in a cascode configuration, and transistors Q_3 and Q_4 are used to provide an agc capability and amplification. With a positive-going agc signal, current in the cascode amplifier is transferred to the Darlington configuration by differential-amplifier action. This agc amplifier has the advantage of low-power drive (high input impedance). In addition, the emitter of Q_1 can be back-biased with respect to the base to provide larger input-signal-handling capability under full agc conditions.

The operating characteristics of the amplifier shown in Fig. 10 are as follows:

Power Gain	— 26 dB
Agc Range	— 70 dB
3-dB Bandwidth	— 4.5 MHz
Noise Figure	— 6.8 dB
Power Dissipation	— 7.7 mW

The response characteristic is shown in Fig. 11

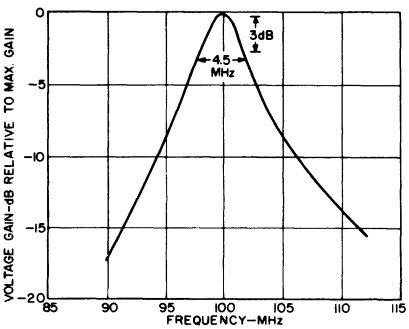


Fig. 11—Response characteristic of 100-MHz amplifier of Fig. 10.

APPLICATION OF THE RCA-CA3019 INTEGRATED-CIRCUIT DIODE ARRAY

BY
G. E. THERIAULT AND R. G. TIPPING

The RCA-CA3019 integrated circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits.

The CA3019 features all-monolithic-silicon epitaxial construction designed for operation at ambient temperatures from −55°C to 125°C. It is supplied in a 10-terminal TO-5 low silhouette package.

Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations as a result of their close proximity and the good thermal conductivity of silicon. Consequently, the CA3019 is particularly useful in circuit configurations which require either a balanced diode bridge or identical diodes.

CIRCUIT CONFIGURATION AND OPERATING CHARACTERISTICS

Fig. 1 shows the circuit diagram and terminal connections for the CA3019. Diodes D_1 through D_4 are internally interconnected to form a diode quad, while diodes D_5 and D_6 are available as independent diodes. Each diode is formed from a transistor by connection of the collector and the base to form the diode anode and use

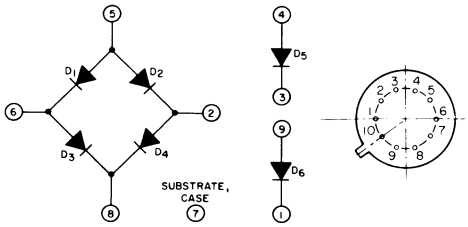
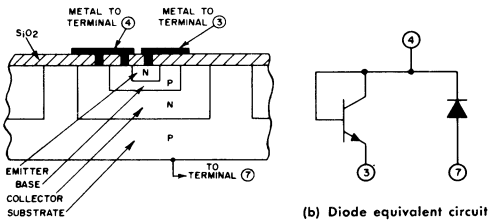


Fig. 1—Schematic diagram and terminal connections for the CA3019 integrated-circuit diode array.

of the emitter for the diode cathode (this technique is one of five methods by which the transistor structure can be utilized as a diode). This diode configuration, in which the collector-base junction is shorted, is the most useful connection for a high-speed diode because it has the lowest storage time. The only charge stored is that in the base. This configuration also exhibits the lowest forward voltage drop, and is the only one which has no p-n-p transistor action to the substrate. The diode has the emitter-to-base reverse breakdown voltage characteristic (typically 6 volts).

The monolithic process produces a substrate diode between the collector of a transistor and its supporting substrate, as shown in Fig. 2. Connected at each diode anode,

therefore, is the cathode of a substrate diode for which the anode is the substrate (terminal 7). In some applications, the substrate can be left floating because a forward bias on any substrate diode creates a self reverse-bias on the other substrate diodes. However, the uncertainty of this bias and the capacitive feedthrough paths provided by the substrate make it advisable to apply a reverse bias to all substrate diodes by returning the substrate through terminal 7 to a dc voltage which is more negative than the most negative voltage on a diode anode. Such reverse bias is most important when ac circuit balance is essential because the capacitance of the substrate diodes is a nonlinear function of the voltage across them. In such circuits, the changing capacitance of these parasitic elements can make good balance over a wide dynamic range impossible.



(a) Cross section of monolithic diode structure

(b) Diode equivalent circuit

Fig. 2—Diagram and equivalent circuit of the monolithic array.

Reverse bias of the substrate diodes is always indicated, therefore, and should be omitted only if the inclusion of such bias is not possible or practical. Terminal 7 may be returned to a negative power supply as long as the combined value of that supply voltage and the maximum positive voltage on any diode anode does not exceed the maximum rating of 25 volts. In systems that use single power supplies, the active circuit may be raised above ground potential and the signals coupled into the diodes by capacitive or inductive means.

The operating characteristics of the CA3019 integrated diode array are determined primarily by the individual diode characteristics, which are given in the technical bulletin.

APPLICATIONS

Although there are many possible applications for the CA3019, this note describes a few practical circuits to stimulate the thinking of the potential user. Besides the obvious uses as separate diodes and possible quad combinations, some of which are covered in the following discusssion, it should be noted that shorting of terminals 2 and 6 in the quad effectively provides two diodes in series. This diode connection can be used as the elements of special balanced mixers, as ring modulators, and as compensating networks that provide two diode drops. Fig. 3 shows an example of a typical synthesizer mixer circuit.

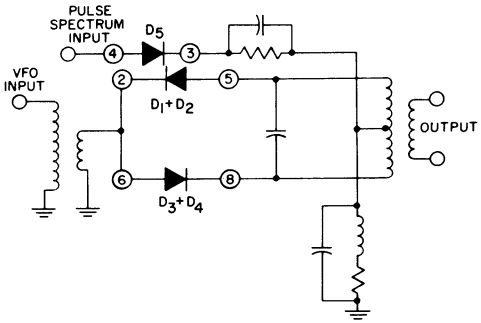


Fig. 3—Typical synthesizer mixer circuit.

Shorting of terminals 5 and 8 provides two independent sets of back-to-back diodes useful for limiting and clipping, as shown in Fig. 4.

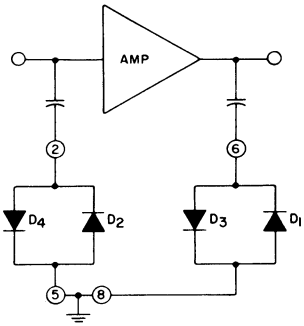


Fig. 4—Limiters using the CA3019.

Balanced Modulator

Fig. 5 shows the use of the CA3019 as a balanced modulator which minimizes the carrier frequency from the output by means of a symmetrical bridge network. A carrier of one polarity causes all the diodes to conduct, and thus effectively short-circuits the signal source. A carrier of the opposite polarity cuts off all the diodes and allows signal current to flow to the load. If the four diodes are identical, the bridge is perfectly balanced and no carrier current flows in the output load. Table I lists the characteristics of the balanced modulator.

High-Speed Gates

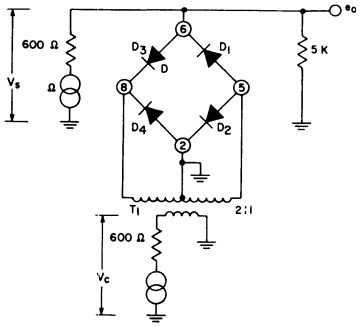
In high-speed gates, the gating signal often appears at the output and causes the output signal to ride a "pedestal." A diode-quad bridge circuit can be used to balance out the undesired gating signal at the output and reduce the pedestal to the extent that the bridge is balanced.

TABLE I. CHARACTERISTICS OF BALANCED MODULATOR OF FIG.5

Carrier Voltage VRMS at 30 KHz	0.75		0.75		0.75		0.50		1.0	
Signal Voltage mVRMS at 2 KHz	77		245		770		245		245	
Output Frequency KHz	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*
28 and 32*	34	6.5	115	7	440	5	51	14	170	3
30	0.7	41	0.82	49	2.6	50	0.1	68	3.6	37
26 and 34	0.02	72	0.05	72+	0.48	64	0.04	72+	0.07	71
24 and 36	0.03	69	0.49	54	60	22	0.58	52.5	0.6	53
22 and 38	0.001	72+	0.01	72+	1.4	55	.015	72+	0.02	72+

* Double-Sideband, Suppressed-Carrier Output.

All other outputs are spurious signals.

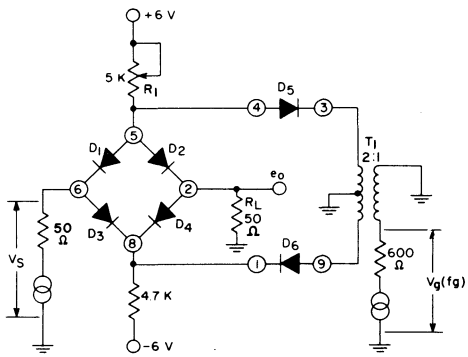


T1 — Technitrol No. 8511660 or equiv.

Fig. 5—Balanced modulator using the CA3019.

A diode-quad gate functions as a variable impedance between a source and a load, and can be connected either in series or in shunt with the load. The circuit configuration used depends on the input and output impedances of the circuits to be gated. A series gate is used if the source and load impedances are low compared to the diode back resistance, and a shunt gate is used if the source and load impedances are high compared to the diode forward resistance.

Series Gate. Fig. 6 shows the use of the CA3019 as a series gate in which the diode bridge, in series with the load resistance, balances out the gating signal to provide a pedestal-free output. With a proper gating voltage (1 to 3 volts rms, 1 to 500 kHz), diodes D_5 and D_6 conduct during one half of each gating cycle and do not conduct during the other half of the cycle. When diodes D_5 and D_6 are conducting, the diode bridge (D_1 through D_4) is not conducting and the high diode back resistance prevents the input signal V_s from appearing across the load resistance R_L; when diodes D_5 and D_6 are not conducting, the diode bridge conducts and the low diode forward resistance allows the input signal to appear across the load resistance. Resistor R_1 may be adjusted to minimize the



T1 — Technitrol No. 8511666 or equiv.

Fig. 6—Series gate using the CA3019.

gating voltage present at the output. The substrate (terminal 7) is connected to the −6-volt supply. Fig. 7 shows the on-to-off ratio of the series gate as a function of frequency.

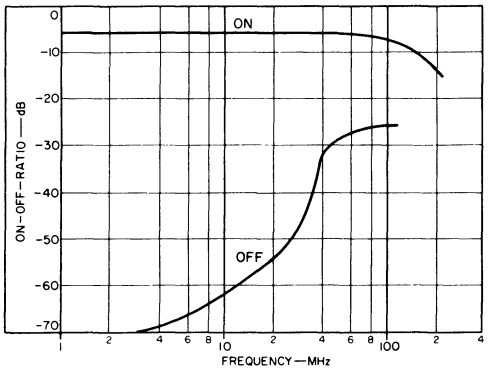
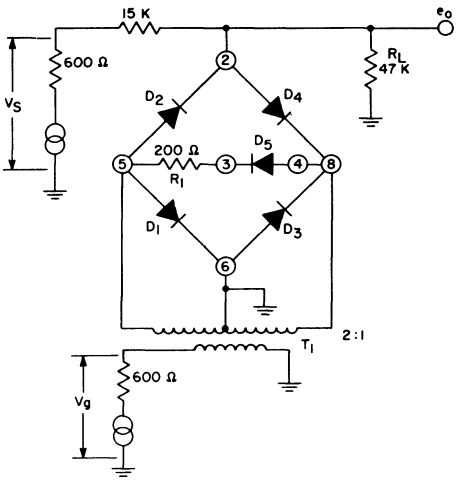


Fig.7—On-to-off ratio for the series gate of Fig.6 as a function of frequency.

Shunt Gate. Fig. 8 shows the use of the CA3019 as a shunt gate in which the diode bridge, in shunt with the load resistance, balances out the gating signal to provide a pedestal-free output. When the gating voltage V_g is of sufficient amplitude, the diode bridge (D_1 through D_4) conducts during one half of each gating cycle and does not conduct during the other half of the cycle. When the diode bridge is conducting, its low diode forward resistance shunts the load resistance R_L and prevents the input signal V_s from appearing at the output; when the diode bridge is not conducting, its high diode back resistance allows the input signal to appear at the output. Diode D_5 and resistor R_1 keep the transformer load nearly constant during both halves of the gating cycle. The substrate (terminal 7) can either be left floating or returned to a negative voltage, but it cannot be returned to ground. The characteristics of the shunt gate are as follows:

Gating frequency (f_g) — 1 to 100 kHz
Gating voltage (V_g) — 0.8 to 1.2 Vrms
Signal frequency (f_s) — dc to 500 kHz (2 dB down)
Signal voltage (V_g) — 0 to 1 Vrms

The frequency range of this circuit can be extended by application of a reverse bias to the substrate. The amount of gating voltage V_g present at the output as a function of the amplitude and frequency of V_g is shown in Table II.



T_1 — Technitrol No. 8511666 or equiv.

Fig.8 —Shunt gate using the CA3019.

TABLE II. GATING CHARACTERISTICS OF SHUNT GATE SHOWN IN FIG.8

Frequency of V_g kHz	*Amplitude of V_g volts*	*Present at the Amount of V_g* Output *mvs*
1	0.8	0.2
1	1.0	0.5
1	1.2	1.3
10	0.8	2.0
10	1.0	4.7
10	1.2	8.7
50	0.8	11.0
50	1.0	24.0
50	1.2	40.0

Series-Shunt Gate

A series-shunt gate which utilizes all six diodes of the CA3019 is shown in Fig. 9 This configuration combines the good on-to-off impedance ratio of the shunt gate with the low-output pedestal of the series gate.

On the gating half-cycle during which the voltage at A is positive with respect to the voltage at B, there is no output because the shunt diodes are forward-biased and

the series diodes are reverse-biased. Any signal passing through the input diodes (D_4 and D_2) encounters a low shunt impedance to ground (D_5 and D_6) and a high impedance in series with the signal path to the load (D_3 and D_1). This arrangement assures a good on-to-off impedance ratio. When the voltages at A and B reverse, the conduction states of the shunt and series diodes reverse, and the signal passes through the gate to the load resistor R_L. Any pedestal at the output is a function of the resistor, transformer, and diode balance.

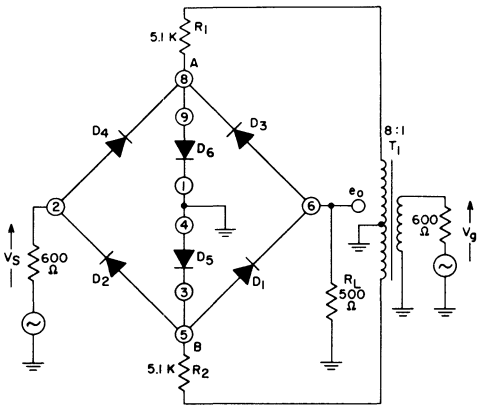


Fig.9 —Series-shunt gate using the CA3019.

The gate continues to operate successfully with resistors R_1 and R_2 shorted if the transformer center tap is removed from ground. In either case, no dc supply is required to bias the gate diodes.

Balanced Mixer

Fig. 10 illustrates the use of the CA3019 as a conventional balanced mixer. The load resistor across the output tuned circuit is selected to provide maximum power output. The conversion gain of the mixer for a 45-MHz input signal and a 55-MHz oscillator signal is shown in Fig. 11. The input impedance at point A is approximately 600-ohms for a 0.6-volt-rms oscillator drive.

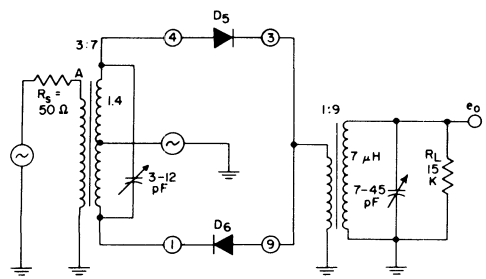


Fig.10 —Balanced mixer using the CA3019.

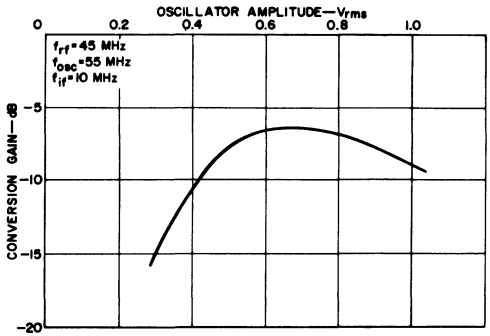


Fig.11 —Conversion gain as a function of oscillator amplitude for the balanced mixer of Fig.10.

The CA3019 mixer shown in Fig. 12 is essentially a balanced mixer with two additional diodes (D_3 and D_4) added to form a half-wave carrier switch. The additional diodes permit both legs of the circuit ($D_1 - D_2$ and $D_3 - D_4$) to function throughout the ac cycle. As compared with a conventional balanced mixer, shown in Fig.10, this circuit effectively doubles the desired output voltage

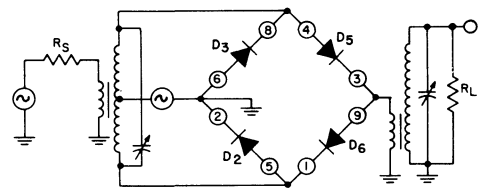


Fig.12 —Balanced mixer with half-wave carrier switch using the CA3019.

and reduces the output voltage at the oscillator frequency by half. However, the capacitances associated with the integrated diodes prevent this circuit configuration from realizing the improvement in conversion gain at frequencies above 20 MHz.

Ring Modulator

The use of the CA3019 as a ring modulator is shown in Fig. 13. If a perfectly balanced arrangement were used, carrier current of equal magnitude and opposite direction would flow in each half of the center-tapped transformer T_2. Thus, the effect of the carrier current in transformer T_2 would be cancelled, and the carrier frequency would not appear in the output. However, the ring modulator of Fig. 13 is not exactly balanced because diodes ($D_1 + D_2$) and ($D_3 + D_4$) are actually two diodes in

parallel, while diodes (D_5) and (D_6) are individual diodes. Nevertheless, this circuit attenuates the carrier in the output as well as an arrangement that uses both individual diodes in two CA3019 circuits.

As the carrier passes through half of its cycle, diodes ($D_1 + D_2$) and (D_6) conduct, and diodes ($D_3 + D_4$) and (D5) do not conduct. When the carrier passes through the other half of its cycle, the previously nonconducting diodes conduct, and vice versa. As a result, the output amplitude, is alternately switched from plus to minus at the carrier frequency. The signal-frequency component of the output waveform is thus symmetrical about the zero axis and is not present in the output. Therefore, the ring modulator suppresses both the carrier frequency and the signal frequency so that the output theoretically contains only the upper and lower sidebands. For single-sideband transmission, one of these sidebands can be eliminated by selective filtering. The performance of the CA3019 as a ring modulator is shown in Table III.

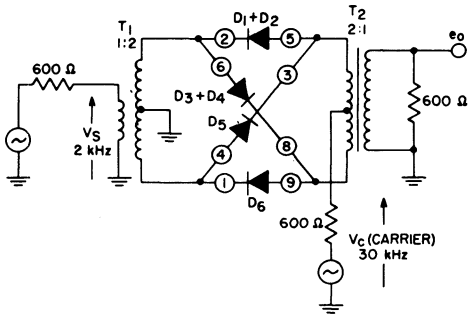


Fig.13 —Ring modulator using the CA3019.

TABLE III. PERFORMANCE CHARACTERISTICS OF RING MODULATION OF FIG.13

		For a given $V_S + V_g$, e_o in millivolts			
Output Freq. KHz	V_s mvs	300	350	450	500
	V_c mvs	600	500	350	300
28 or 32	Upper or Lower Sidebands	86	97	83	91
2	Sig. Freq.	0.042	0.02	0.015	0.020
30	Carrier Freq.	* 1.3 (−37db)	* 0.88 (−41db)	* 0.67 (−42db)	* 0.62 (−43db)
26 or 34	Higher Order Sidebands	0.018	0.016	0.036	0.043
24 or 36		0.021	0.054	0.047	5.0

* db below the desired upper and lower sidebands

Application Notes on IC Amplifier, Control, and Special-Function Circuits

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Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

BY

M.E. MALCHON AND G.E. THERIAULT

The RCA CA3004, CA3005, and CA3006 rf amplifiers are silicon-epitaxial monolithic integrated circuits, supplied in 12-terminal TO-5 packages. These circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from −55°C to +125°C, at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide the following types of functions:

1. Wide- or narrow-band amplification
2. Mixing
3. Limiting
4. Product detection
5. Frequency generation
6. Generation of pulse or digital waveforms

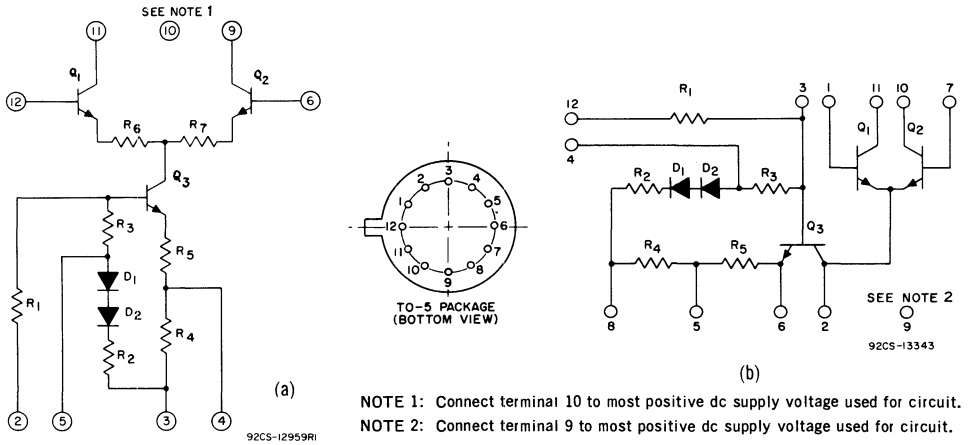
The CA3004 has linear transfer characteristics, excellent circuit stability, and a wide dynamic range. These features indicate that the CA3004 is particularly useful for applications in which the ability to handle large input signals is an important consideration.

The CA3005 and CA3006 feature high gain, sharp limiting characteristics, and exceptional versatility. The versatility in the operation of the CA3005 and CA3006 is made possible by the availability of internal circuit points to which external circuit elements may be connected to alter the basic circuit configuration. As a result of such external modifications, it is possible to operate these circuits as push-pull amplifiers, as cascode amplifiers, or as single amplifiers in cascade or parallel channels.

The CA3005 and CA3006 rf amplifiers are identical except for their input offset voltages. The offset voltage for the CA3006 is typically less than 1 millivolt, while the offset voltage for the CA3005 is normally in the order of 3 millivolts. The low level of input offset voltage makes the CA3006 well suited for balanced-modulator, mixer, or other push-pull applications that require a well-balanced circuit.

CIRCUIT DESCRIPTIONS AND OPERATING MODES

Fig. 1 shows the schematic diagrams, together with the terminal arrangement on the TO-5 packages, for the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. Each circuit consists of a balanced differential amplifier that is driven from a controlled, constant-current source.



NOTE 1: Connect terminal 10 to most positive dc supply voltage used for circuit.
NOTE 2: Connect terminal 9 to most positive dc supply voltage used for circuit.

Fig. 1—Schematic diagrams of the integrated-circuit rf amplifiers: (a) CA3004; (b) CA3005 or CA3006. The terminal arrangement on the TO-5 package, which is the same for each type, is also shown.

In the CA3004 circuit, resistors (R_6 and R_7) are included in the emitter leads of the differential pair of transistors, Q_1 and Q_2. The degeneration introduced by these unbypassed emitter resistors improves the linearity of the transfer characteristics and increases the signal-handling capabilities of the circuit. Fig. 2 shows the dynamic transfer and limiting characteristics of the CA3004. The characteristics show that linear operation is possible over a wide range of differential input voltage and, thus, indicate that relatively large input signals can be handled by the circuit without limiting.

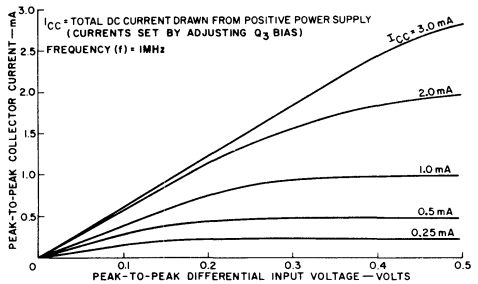


Fig. 2—Dynamic transfer and limiting characteristics of the CA3004 integrated-circuit rf amplifier.

In the CA3005 and CA3006 circuits, no emitter resistors are provided for the differential pair of transistors. As a result, these circuits have a smaller dynamic range and provide higher gain than the CA3004 circuit. The dynamic transfer and limiting characteristics of the CA3005 and CA3006, given in Fig. 3, show that these circuits are very good limiting amplifiers. A comparison of the curves in Fig. 3 with those given for the CA3004 in Fig. 2 emphasizes the excellent limiting characteristics of the CA3005 and CA3006.

SUPPLY-VOLTAGE CONNECTIONS

The CA3004, CA3005, and CA3006 circuits may be operated, at various levels of supply voltage, from single or dual dc power supplies. For dual-supply operation, either symmetrical or nonsymmetrical power supplies may be used.

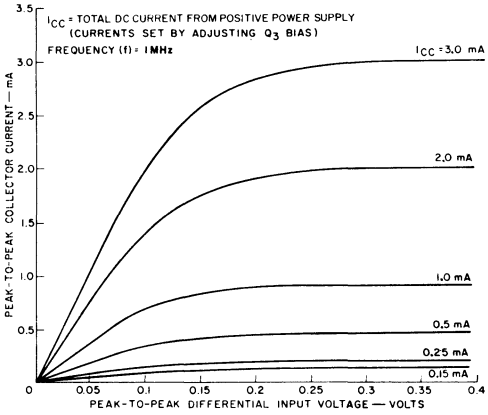


Fig. 3—Dynamic transfer and limiting characteristics of the CA3005 or CA3006 integrated-circuit rf amplifier operated in the differential-amplifier configuration.

Fig. 4 shows the supply-voltage connections for differential- and cascode-amplifier operation of the CA3005 or CA3006 from single and dual supplies. When two supplies, one for positive voltage and one for negative voltage, are used, as shown in Figs. 4(a) and 4(c), fewer external components are required. When only one supply is used, an external resistive voltage divider and bypass capacitor must

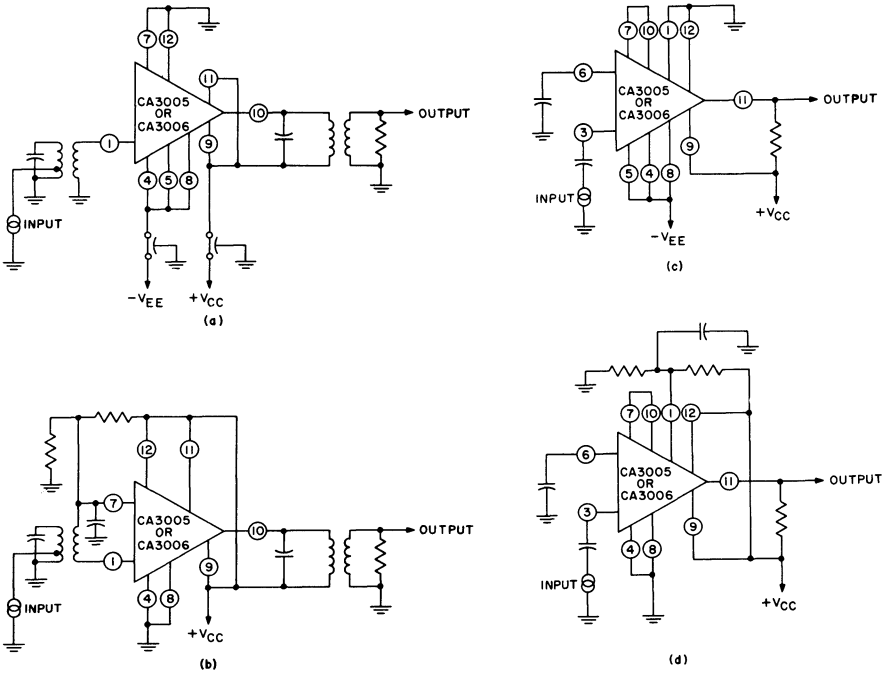


Fig. 4—Schematic diagrams showing supply-voltage connections to the CA3005 or CA3006 for operation from either single or dual power supplies: (a) Differential-amplifier configuration operated from dual supplies; (b) Differential-amplifier configuration operated from a single supply; (c) Cascode configuration operated from dual supplies; (d) Cascode configuration operated from a single supply.

be added to the circuit, as shown in Figs. 4(b) and 4(d). Tuned amplifiers that operate from dual supplies, such as that shown in Fig. 4(a), require the least number of external components.

For either single- or dual-supply operation, the operating current of transistor Q_3 is determined by the bias voltage, V_{EE}, applied between terminals 2 and 3 on the CA3004 or between terminals 8 and 12 on the CA3005 and CA3006 (refer to the circuit diagrams in Fig. 1). The more negative terminal of the bias-voltage source must be connected to terminal 3 on the CA3004 or to terminal 8 on the CA3005 and CA3006. In dual-supply systems, terminal 2 of the CA3004 and terminal 12 of the CA3005 and CA3006 are usually returned to dc ground.

OPERATING MODES

For any given bias voltage V_{EE}, there are four possible operating modes for the integrated-circuit rf amplifiers. In general, each mode is characterized by (1) a distinct level of operating current and corresponding transconductance, (2) the degree of dependence of the operating current on temperature, and (3) the way in which the transconductance is affected by temperature. The operating points for the various modes are established by:

1. The emitter resistance selected for the constant-current-source transistor, Q_3;
2. Whether the base-bias network includes the diodes shown in Fig. 1.
3. The magnitude of the bias voltage, V_{EE}, applied to the circuit.

Table I lists the required conditions for the four operating modes, designated A, B, C, and D. The following paragraphs describe the characteristics of the circuits in each operating mode. The data are given for operation of the circuits from symmetrical dual power supplies at three levels of dc supply voltage (± 3 volts, ± 4.5 volts, and ± 6 volts).

Fig. 5 shows the operating current for the various modes as a function of temperature. The current-temperature data show that, in addition to the obvious shift in the level of operating current, the dependence of the operating current on temperature varies significantly with a change in the operating mode.

When the diodes are included in the base-bias circuit

TABLE I

Required Conditions for Each Operating Mode of the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

*Operating Mode**	*CA3004 Terminals Shorted To Terminal 3*	*CA3005 or CA3006 Terminals Shorted To Terminal 8*	*Diodes In or Out of Bias Circuit*	*Q-3 Emitter Resistor(s)*
A	—	—	In	$R_4 + R_5$
B	5	4	Out	$R_4 + R_5$
C	4	5	In	R_5
D	4, 5	4, 5	Out	R_5

*For all modes, terminals 2, 6, and 12 of the CA3004 and terminals, 1, 7, and 12 of CA3005 and CA3006 are grounded.

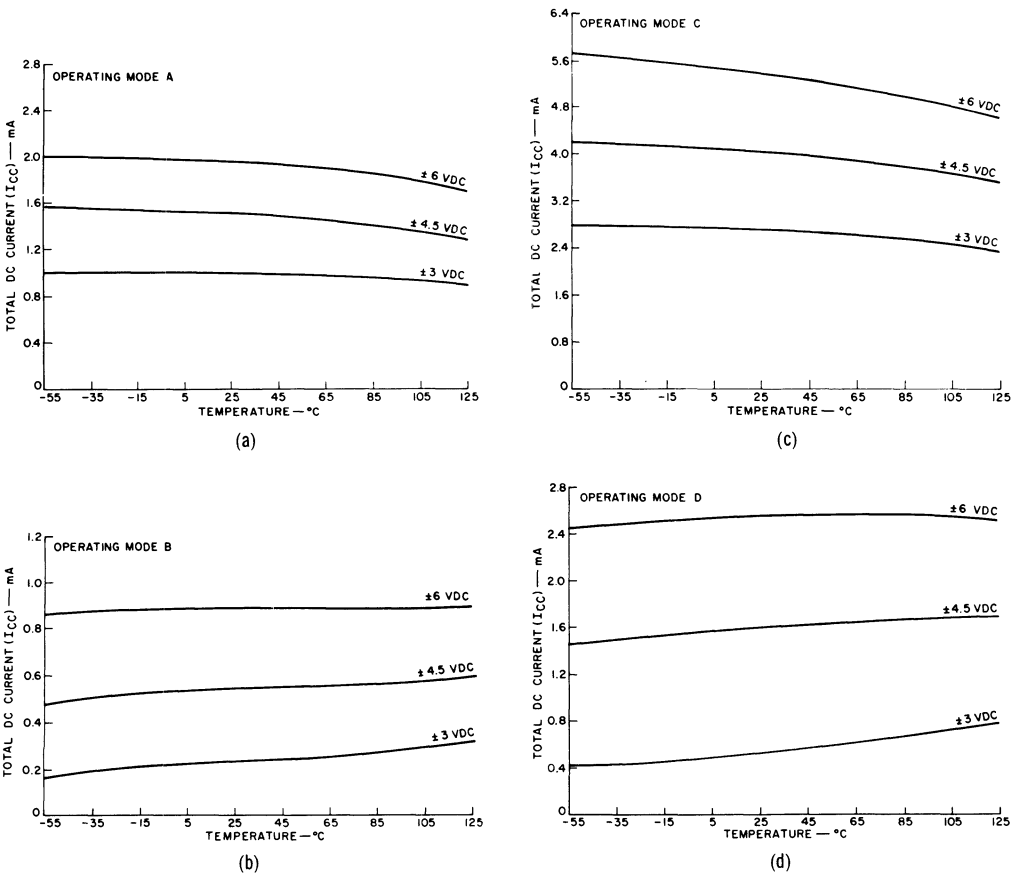


Fig. 5—Variation in the operating currents of the CA3004, CA3005, or CA3006 as a function of temperature for each mode of operation.

(modes A and C), the operating current, which is primarily dependent on the temperature coefficient of the diffused emitter resistor, tends to decrease with an increase in temperature at a rate that is relatively independent of the bias supply voltage V_{EE}. When the diodes are not used, however, the shape of the current-temperature curves is dependent on the magnitude of the supply voltage V_{EE}. The operating current then may remain constant or rise as the temperature is increased, depending upon the value of V_{EE}. The positive supply voltages, shown in Fig. 5, have no effect on the operating current, and the current-temperature curves are not changed by increases or decreases in this voltage. Some deviation in the current-temperature curves is to be expected because of normal variations in the absolute resistor values.

Fig. 6 shows the effects of different operating modes and variations in temperature on the single-ended transconductance* of the CA3004. In general, when diodes are used in the base-bias network, the transconductance decreases with increases in temperature. If the diodes are not used, the transconductance may decrease, increase, or remain constant as the temperature increases, depending on the value of the negative supply voltage V_{EE}. With the diodes out, however, the collector operating point tends to shift when resistive loads are used. In applications that require a stable collector dc operating point, therefore, operating mode A or C (diodes in) should be used.

Fig. 7 shows transconductance-temperature curves for each operating mode of the CA3005 or CA3006, operated in a differential-amplifier configuration. These transconductance curves differ from those for the CA3004 shown in Fig. 6 primarily because of the emitter resistors used in the CA3004. For each operating mode, the operating points for the differential-amplifier configuration of the CA3005 or CA3006, as well as for the CA3004, provide a current in each collector of the differential pair of transistors that is equal to one-half that shown in Fig. 5.

In a cascode configuration of the CA3005 or CA3006, the current through each part of the common emitter-common

*The single-ended transconductance is the incremental output current for one collector of the differential pair of transistors divided by the incremental input voltage. The curves shown of this parameter are obtained at an operating frequency of 1 MHz.

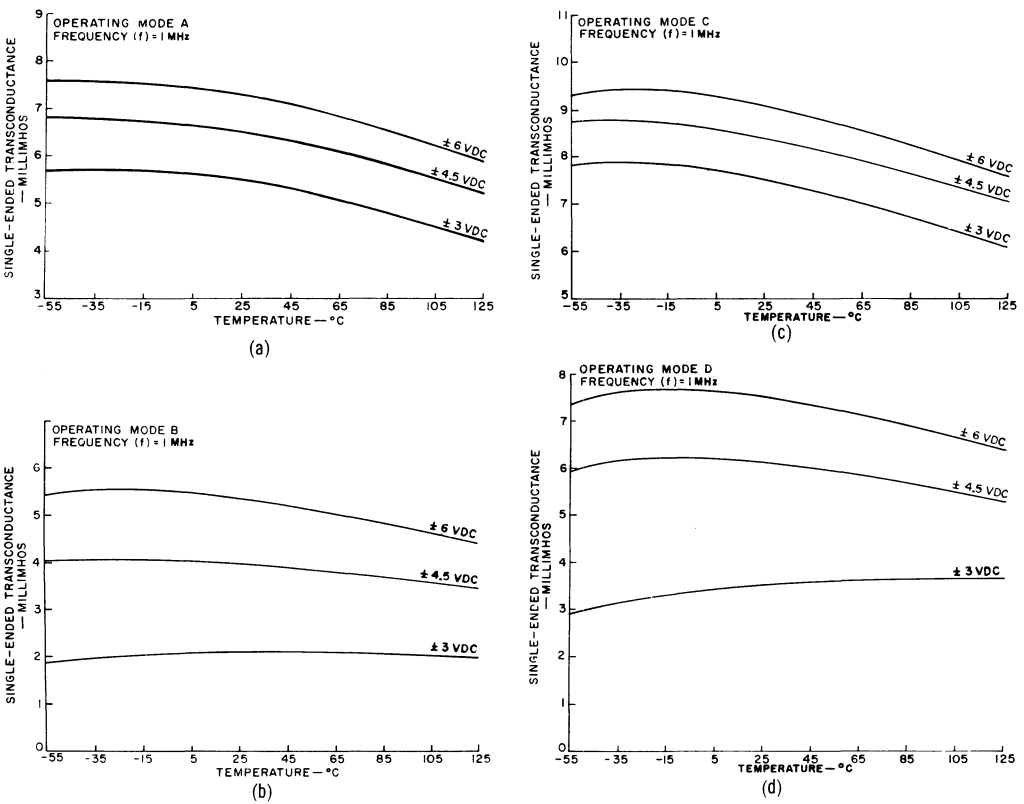


Fig. 6—Variation in the single-ended transconductance of the CA3004 as a function of temperature for each operating mode.

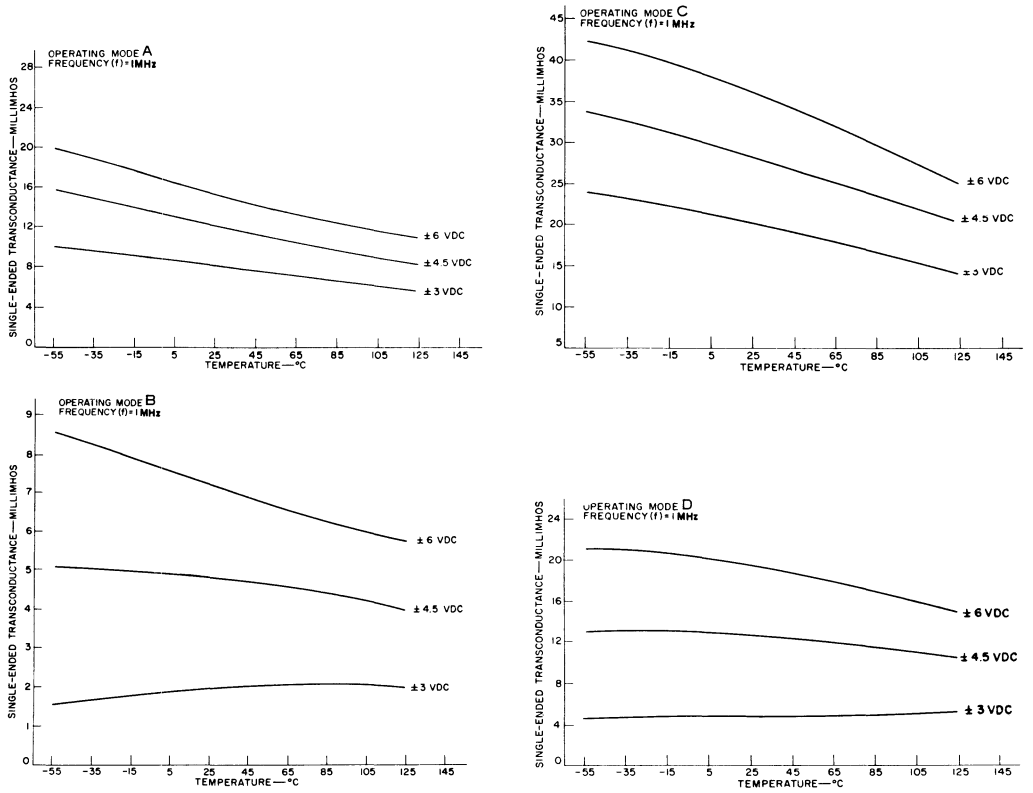


Fig. 7—Variation in the single-ended transconductance of the CA3005 or CA3006 in a differential-amplifier configuration as a function of temperature for each operating mode.

base cascode is equal to the total current shown in Fig. 5 in each mode. Fig. 8 shows the transconductance-temperature curves for each operating mode of the cascode circuit. These curves show that, in general, the transconductance is higher when the diodes are included in the base-bias network (modes A and C) than it is when the diodes are not used (modes B and D).

The power dissipation of the CA3004, CA3005, or CA3006 is highest when the circuit is operated in mode C. Table II shows power dissipation and the single-ended transconductance of the circuits for each operating mode. These data may be used to determine the operating point that provides the highest value of transconductance per milliwatt of circuit dissipation for given design conditions.

CHARACTERISTICS OF THE RF AMPLIFIER CIRCUITS

Y PARAMETERS

In the design of rf and if circuits, the four-terminal black-box short-circuit admittance parameters have become a valuable tool. The determination of stability criteria, input and output impedances as a function of load and source admittance, power gain, and voltage gain in iterative connections are all facilitated by a knowledge of the "y" parameters.

The "y" parameter curves presented in this section have been calculated from a model and verified at several points by measurements. These curves are a valuable aid in the design of systems that use integrated circuits. The admittance curves are all generated for a quiescent operating current of 1.25 milliamperes in each of the transistors Q_1 and Q_2 in the differential-amplifier configurations and for a current of 2.5 milliamperes in transistor Q_3 in the cascode configuration. This operating current is obtained in the operating mode D, as defined in the preceding section, with supply voltages of ±6 volts.

The "y" parameters and their symbols are listed below:

1. Input admittance with the output voltage constant
   $y_i = g_i + jb_i$

where y_i is the complex input admittance, g_i is the input conductance and b_i is the input susceptance.

TABLE II

Relationship Between the Transconductance and the Power Dissipation of the Integrated-Circuit RF Amplifiers in Each Operating Mode*

Operating Mode	*Type of Circuit*	*DC Supply Voltages (volts)*	*Single-Ended Transconductance (millimhos)*	*Power Dissipation (milliwatts)*
A	CA3004	±3	5.5	6.6
	CA3005 or CA3006		8.5	6.6
	CA3004	±4.5	6.7	15.0
	CA3005 or CA3006		12.8	15.0
	CA3004	±6	7.3	25.0
	CA3005 or CA3006		15.0	25.0
B	CA3004	±3	1.6	2.3
	CA3005 or CA3006		1.9	2.3
	CA3004	±4.5	4.0	7.2
	CA3005 or CA3006		4.9	7.2
	CA3004	±6	5.3	15.0
	CA3005 or CA3006		7.2	15.0
C	CA3004	±3	7.5	17.5
	CA3005 or CA3006		22.0	17.5
	CA3004	±4.5	8.5	40.0
	CA3005 or CA3006		29.0	40.0
	CA3004	±6	9.1	62.8
	CA3005 or CA3006		37.0	62.8
D	CA3004	±3	3.3	4.2
	CA3005 or CA3006		5.0	4.2
	CA3004	±4.5	6.0	17.4
	CA3005 or CA3006		13.0	17.4
	CA3004	±6	7.2	35.9
	CA3005 or CA3006		20.0	35.9

*Circuits are operated in differential-amplifier configurations. The transconductances and power dissipations shown are calculated values for nominal units.

2. Output admittance with the input voltage constant

$$y_o = g_o + jb_o$$

where y_o is the complex output admittance, g_o is the output conductance, and b_o is the output susceptance.

3. Forward-transfer admittance with the output voltage constant

$$y_f = g_f + jb_f$$

where y_f is the complex forward-transfer admittance, g_f is the forward-transfer conductance, and b_f is the forward-transfer susceptance.

4. Reverse-transfer admittance with the input voltage constant

$$y_r = g_r + jb_r$$

where y_r is the complex reverse-transfer admittance, g_r is the reverse-transfer conductance, and b_r is the reverse-transfer susceptance.

A comparison of the parameters of the various possible circuit configurations with those of the more familiar common-emitter parameters requires a second subscript to indicate the type of configuration being considered. Examples of the use of the second-subscript notation are given below:

The common-emitter reverse-transfer admittance is written as

$$y_{re} = g_{re} + jb_{re}$$

The differential-amplifier reverse-transfer admittance is expressed as

$$y_{rDA} = g_{rDA} + jb_{rDA}$$

The cascode-amplifier reverse-transfer admittance is given as

$$y_{rCAS} = g_{rCAS} + jb_{rCAS}$$

These cumbersome second subscripts will not be used when the type of circuit for which the parameter is given is clearly indicated by an illustration or a descriptive phrase in the text.

In general it is valuable to understand the essential differences between the "y" parameters of a regular common-emitter stage and those of the compound stages, such as differential and cascode amplifiers.

The differential amplifier, when used at radio frequencies, consists essentially of a common-collector stage that drives a common-base stage. In comparison to the regular, common-emitter "y" parameters, the input admittance y_i the output admittance y_o, and the forward transfer admittance y_f, are decreased, almost exactly, by a factor of two when the differential-amplifier configuration is used.

The reverse-transfer admittance y_r is also less for the differential amplifier than for the single transistor in the common-emitter configuration. The ratio of the imaginary term in the differential-amplifier admittance to that of the single transistor is 1/140 at low frequencies and 1/10 at 100 MHz. Fig. 9 shows the ratios of imaginary parts

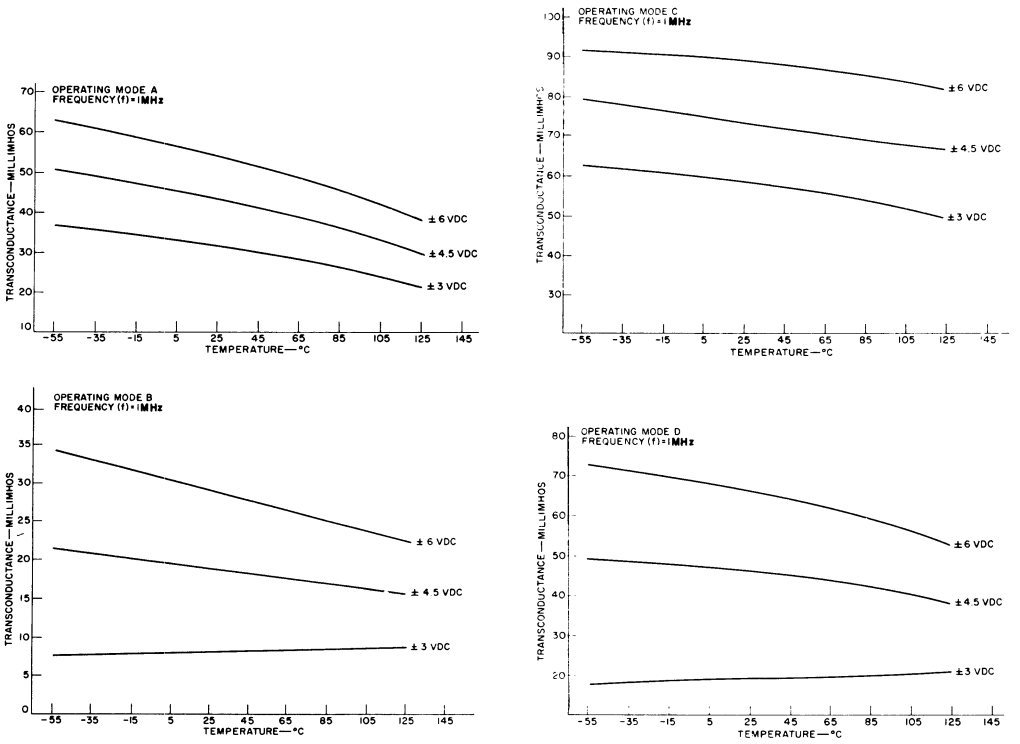


Fig. 8—Variation in the transconductance of the CA3005 or CA3006 in a cascode configuration as a function of temperature for each operating mode.

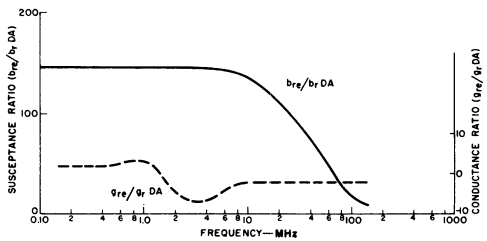


Fig. 9—Ratio of the real (conductance) and the imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a differential-amplifier stage as a function of frequency.

b_{re}/b_{rDA} and real parts g_{re}/g_{rDA} of the reverse-transfer admittances as a function of frequency.

In the cascode configuration of the rf amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance y_i is, therefore, that of a common-emitter stage. The forward-transfer admittance y_r is that of a common-emitter stage times alpha. Because of the high-impedance drive source on the common-base stage, the output admittance y_o is very low (0.06×10^{-5} mhos) at low frequencies and is both negative and low at high frequencies. Since the output admittance is low and may be negative, a conjugate match cannot be obtained at the output. Practical amplifiers are possible however, provided that the sum $Y_{out} + Y_{load}$ is positive.

The reverse-transfer admittance y_r for the cascode circuit is less than that for the single-stage common-emitter

circuit. The ratio of the imaginary terms of these admittances is 1/1200 at low frequencies and 1/35 at 100 MHz. The ratios of the real parts and of the imaginary parts as a function of frequency are shown in Fig. 10.

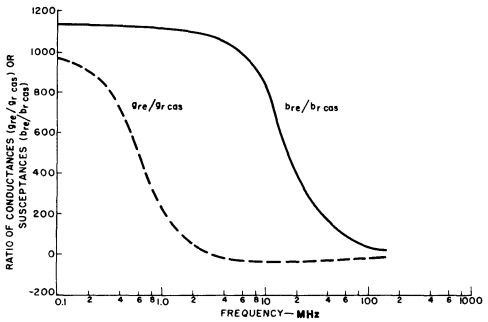


Fig. 10—Ratio of the real (conductance) and the imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a cascode stage as a function of frequency.

Although the y_r is low for both the differential and cascode configurations, instability can occur in high-gain amplifiers. A further consideration in high-gain circuits is that the layout can contribute more feedback than the integrated circuit. Shielding and layout therefore are of prime importance if proper advantage is to be taken of the low feedback of these circuits.

The computed y parameters for the CA3004 differential amplifier are shown in Fig. 11. The admittance parameters for differential-amplifier operation of the CA3005 or CA3006 are given in Fig. 12 and those for cascode-amplifier operation of either circuit are given in Fig. 13.

VIDEO-AMPLIFIER CAPABILITIES

The CA3004, CA3005, and CA3006 integrated circuits may be used as video amplifiers, as shown in Figs. 14(a) and 14(b). A relatively large number of external components is required, and the availability of internal-circuit connections for these external components provides a large degree of flexibility to the user with respect to such factors as bandwidth, gain, power dissipation and peaking. In the circuit shown in Fig. 14(a), R_1 should be equal to R_2 to preserve the circuit balance, and C_2 should be an adequate bypass so that the noise factor and gain are not degraded. For the cascode configuration shown in Fig. 14(b), C_2 is an emitter bypass, and its reactance should be less than 1.5 ohms at the lowest video frequency to be handled.

In either cascode or single-ended differential-amplifier configurations, the feedback is low. Each configuration provides good isolation from output to input; the high frequency performance therefore can be approximated from the input and output parallel R and C for a single stage or from the total shunt R and C between stages for an iterative connection. The mid-frequency voltage gain can be computed from the familiar $g_m R_L$ product. As an aid to such calculations, Table III gives the input and output parallel R and C and the absolute values of g_m for the various circuits and configurations for operation at 1, 10, and 40 MHz. For more precise, but more elaborate calculations, the y parameters may be used for video-amplifier design.

NOISE PERFORMANCE

The noise figure of the CA3004, CA3005 and CA3006 integrated-circuit rf amplifiers is a function of the dc operating current and frequency, for both differential and cascode-amplifier configurations. The noise figure increases both with an increase in current and with an increase in fre-

TABLE III

Input and Output Parallel RC Network, Transconductance, and Performance Data for the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

						VIDEO PERFORMANCE (Simulated Iterative Connection)			
Freq. (MHz)	*Input Parallel RC* R_{in} (ohms)	C_{in} (pF)	*Output Parallel RC* R_{out} (ohms)	C_{out} (pF)	*Transconductance,* g_m (millimhos)	*Interstage* R_L (ohms)	*High-Freq. 3-dB Point* (MHz)	*Mid-Band Voltage Gain* (dB)	
CASCODE OPERATION (CA3005 OR CA3006)									
1	500	42	—1.67 X 10^6	3.0	78		23	19.3	Measured
10	500	42	—1.67 X 10^6	3.0	77	150			
40	180	22	—6 X 10^5	3.0	58		20	20.6	Calculated
DIFFERENTIAL-AMPLIFIER OPERATION (CA3005 OR CA3006)									
1	2500	16	10^5	4.0	20		18	19.5	Measured
10	1800	13	4 X 10^4	4.0	20	500			
40	670	10.5	2800	7.6	18.6		16	20.0	Calculated
DIFFERENTIAL-AMPLIFIER OPERATION (CA3004)									
1	6650	8	1.7 X 10^5	6.5	7.8		18.4	17.2	Measured
10	6650	6.2	10^5	6.1	7.8	1000			
40	2000	5.0	2 X 10^4	6.8	7.6		15	18.0	Calculated

Data obtained for circuits operated from ±6-volt dc supplies in operating mode D.

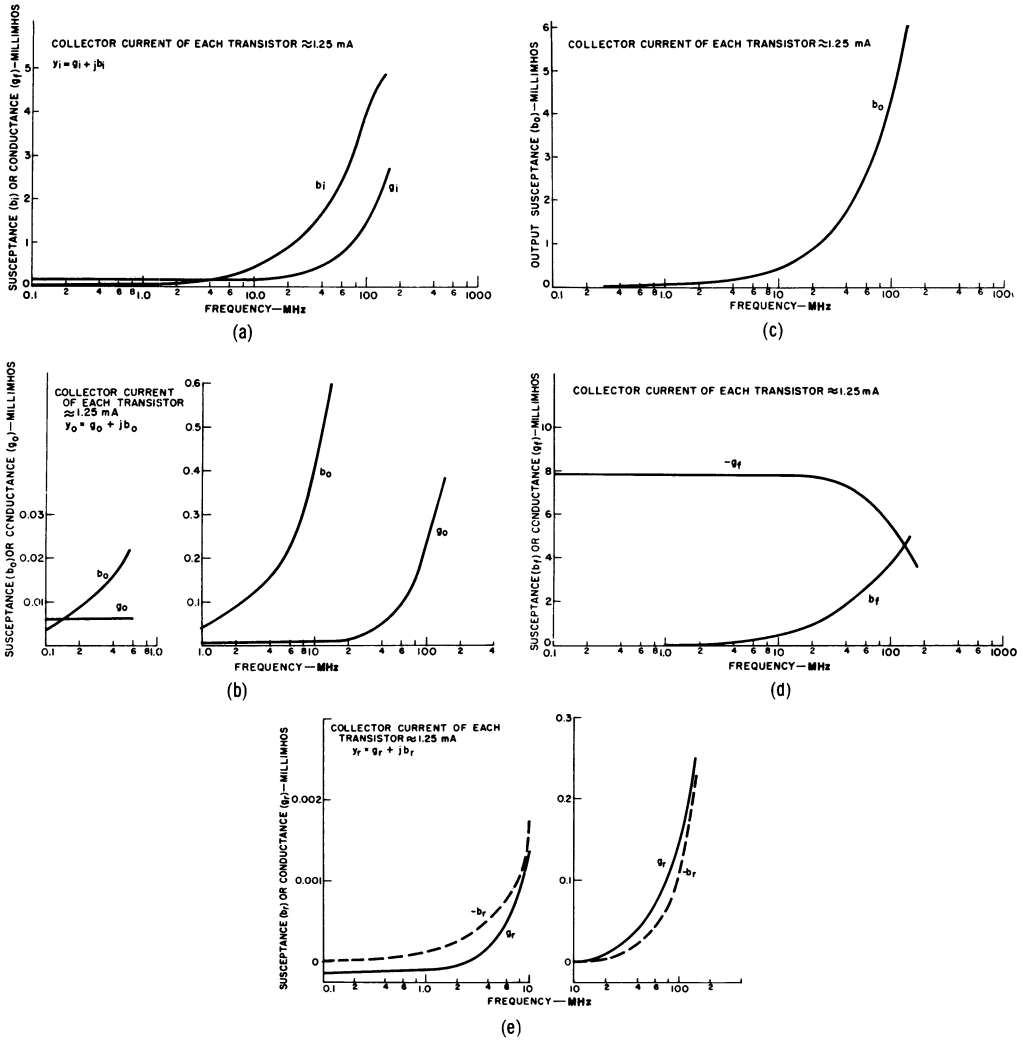


Fig. 11—Admittance characteristics of a CA3004 differential amplifier as a function of frequency: (a) Input admittance, y_i; (b) Output admittance, y_o; (c) Output susceptance, b_o, above 10 MHz; (d) Forward-transfer admittance, y_f; (e) Reverse transfer admittance, y_r.

quency. For convenience, noise data were taken in a fixed configuration as the negative supply voltage was varied. On the data plots, the operating currents that correspond to the various supply voltages are included as a separate abscissa to show that the noise figure is a direct function of operating current. Figs. 15 and 16 show representative noise-figure data for tuned amplifiers in the differential and cascode configuration, respectively. In each case, the input and output are tuned and the input is conjugately matched to a 50-ohm noise diode. Practically no change in noise figure occurs with variations of the positive supply voltage V_{CC}.

The curves in Figs. 15 and 16 show that, for optimum single-stage noise performance, the operating current should be low, which results in a low gain. Thus, in system applications of the tuned amplifiers, the operating current in each stage should be adjusted to obtain the optimum overall noise

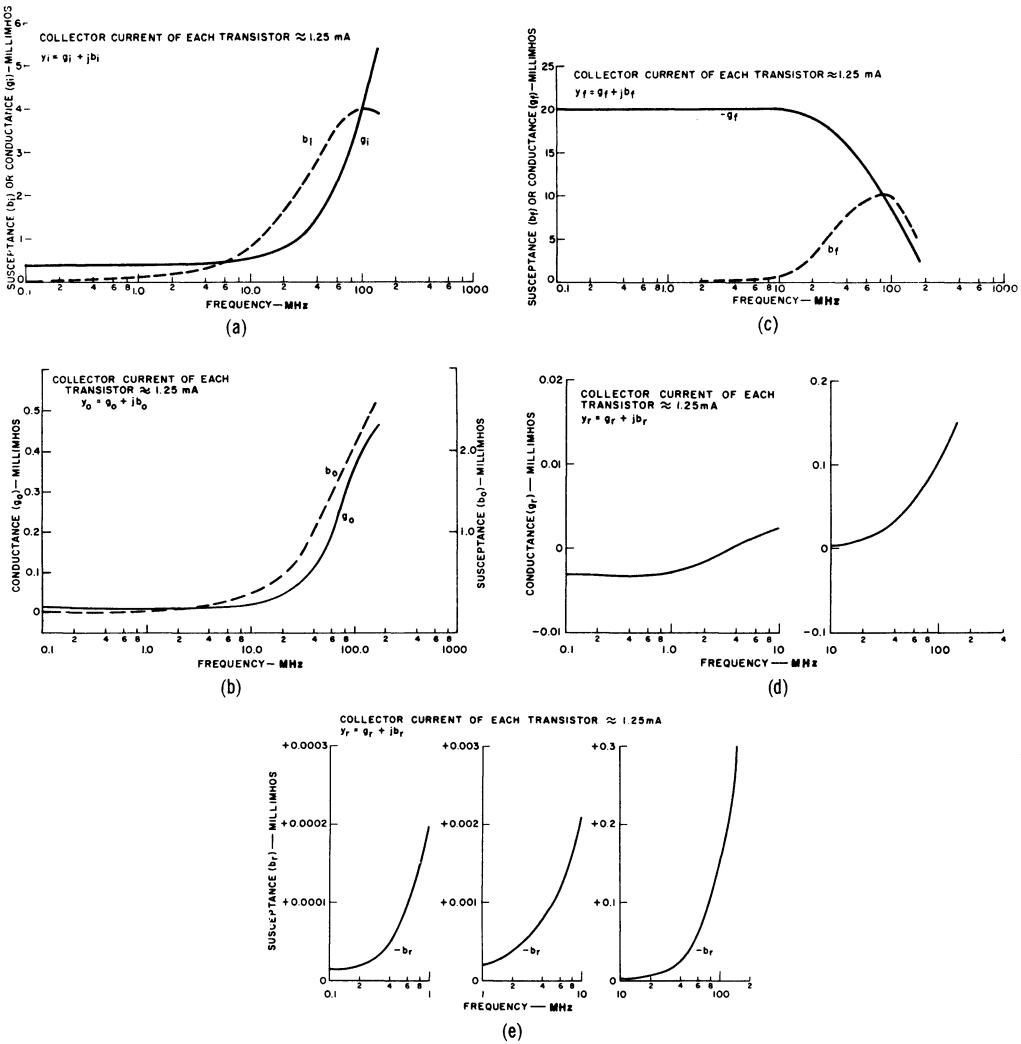


Fig. 12—Admittance characteristics of a CA3005 or CA3006 differential amplifier as a function of frequency: (a) Input admittance, y_i; (b) Output admittance, y_o; (c) Forward transfer admittance, y_f; (d) Reverse transfer conductance, g_r; (e) Reverse transfer susceptance, b_r.

figure by considering the gain and noise figure of the first stage and the noise figure of the second stage. The operating-current adjustment can be accomplished by a change in the negative-supply voltage (V_{EE}) or by means of the bias connections that are available.

Fig. 17 shows the noise figure as a function of the source resistance for a CA3005 or CA3006 used as a differential amplifier at an operating frequency of 12 MHz. The equation given in the figure can be used to predict noise performance as a function of source resistance for dc operating conditions. The load resistor R_L of the circuit is 2200 ohms and R_N = 800 ohms. (R_N is the equivalent noise resistance).

COMMON-MODE REJECTION RATIO

The common-mode rejection ratio of a differential amplifier, defined as the ratio between the full differential gain

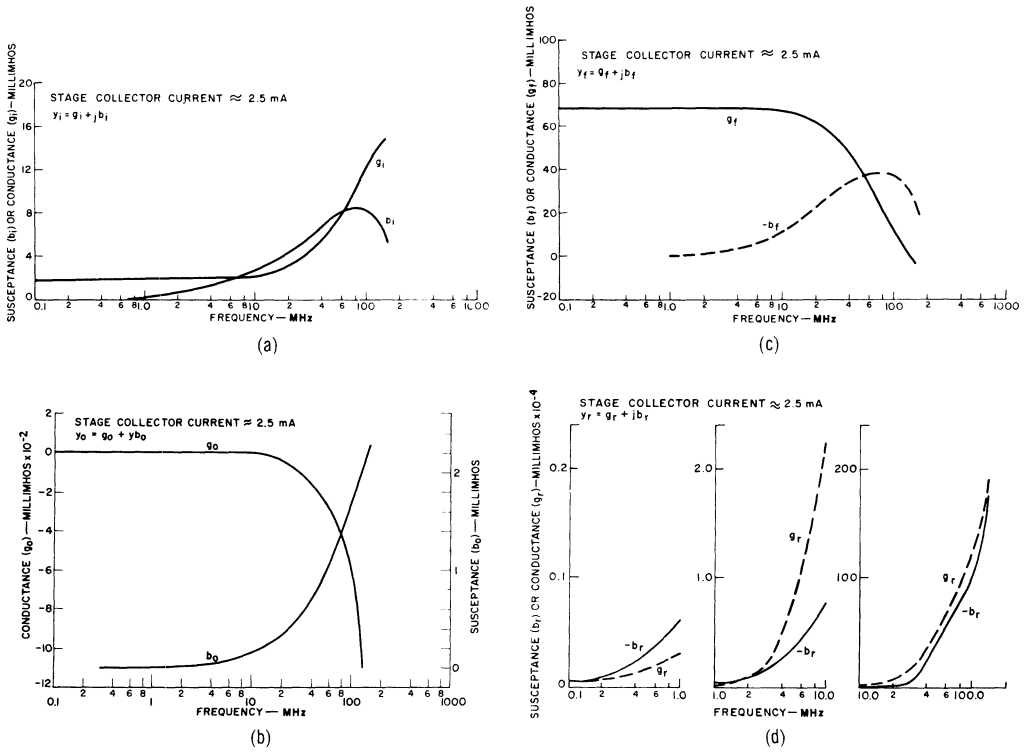


Fig. 13—Admittance characteristics of a CA3005 or CA3006 cascode amplifier as a function of frequency: (a) Input admittance, y_i; (b) Output admittance, y_o; (c) Forward transfer admittance, y_f (d) Reverse transfer admittance, y_r.

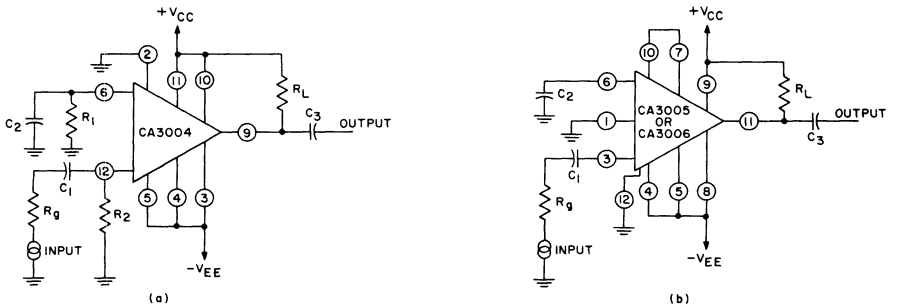


Fig. 14—Schematic diagrams showing the use of the integrated-circuit rf amplifiers as video amplifiers: (a) CA3004 in a differential-amplifier configuration; (b) CA3005 or CA3006 in a cascode-amplifier configuration.

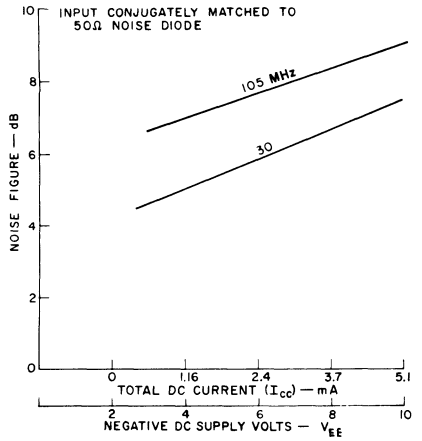


Fig. 15—Representative noise performance of the CA3004, CA3005, or CA3006 operated in a differential-amplifier configuration (operating mode D).

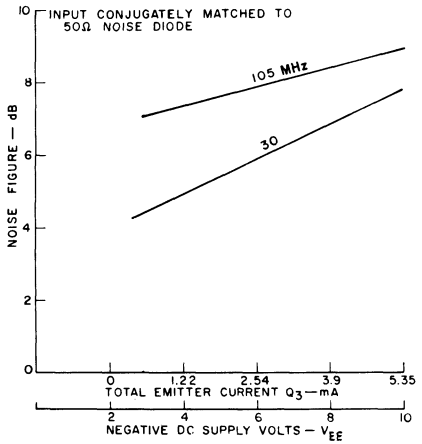


Fig. 16—Representative noise performance of the CA3005 or CA3006 operated in a cascode-amplifier configuration (operating mode D).

and the common-mode gain, is a useful performance characteristic. The common-mode rejection is a function of the ratio of the impedance of the constant-current transistor Q_3 to the load resistor. The common-mode rejection decreases if the signal applied is large enough to saturate the constant-current transistor. The maximum peak-to-peak input voltage, therefore, is a function of the supply voltages and the bias connections of the constant-current transistor. The common-mode rejection for a 1-kHz signal is shown in Table IV.

TABLE IV

Common-mode Rejection Ratio for the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

	At −55°C	*At 25°C*	*At 125°C*
CA3004	102 dB	98 dB	101 dB
CA3005 or CA3006	108 dB	101 dB	107 dB

Operating frequency = 1 kc/s.
Load resistance, R_L = 1000 ohms in each collector.

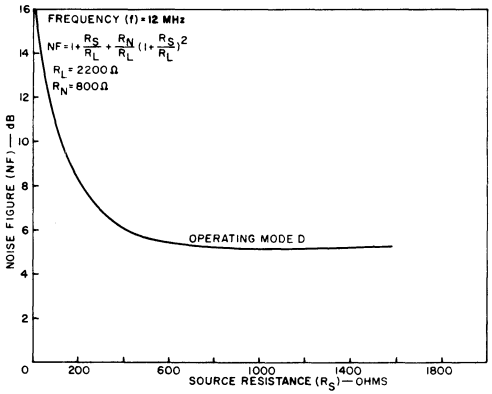


Fig. 17—Noise figure of the CA3005 or CA3006 in a differential-amplifier configuration as a function of the source resistance (operating mode D).

Fig. 18 shows the single-ended common-mode gain* for the CA3004, CA3005, and CA3006 as a function of frequency. (Fig. 19 shows the method used to determine the single-ended common-mode gain.) The common-mode rejection decreases with increasing frequency when the CA3004, CA3005, and CA3006 are operated with a single-ended output.

GAIN CONTROL

The gain of the CA3004, CA3005, and CA3006 circuits may be controlled in either of two ways: (1) The negative voltage applied to the base-bias resistor R_1 can be adjusted to vary the current in transistor Q_3 or (2) A differential offset voltage can be applied to transistors Q_1 and Q_2. In both techniques, the gain-control voltage has a ground reference in a two-supply system, and maximum gain is obtained at 0 volts. The first method provides greater gain-control range but also requires more control voltage than the second method. Figs. 20 and 21 show the typical gain control as a

*Single-ended common-mode gain: The ratio of the change in the single-ended output voltage, measured from either output terminal with respect to ground, to the change in the input voltage applied simultaneously to both inputs of the circuit, i.e., single-ended common-mode gain $= \Delta V_{in}/\Delta V_{out}$, as shown in Fig. 19.

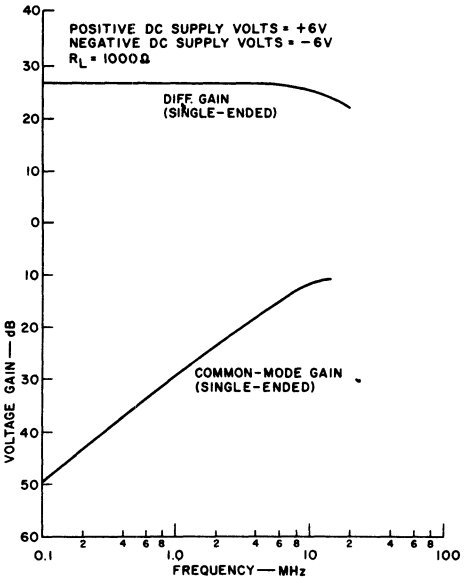


Fig. 18—Single-ended common-mode and differential-mode gains of the CA3004, CA3005, or CA3006 as a function of frequency.

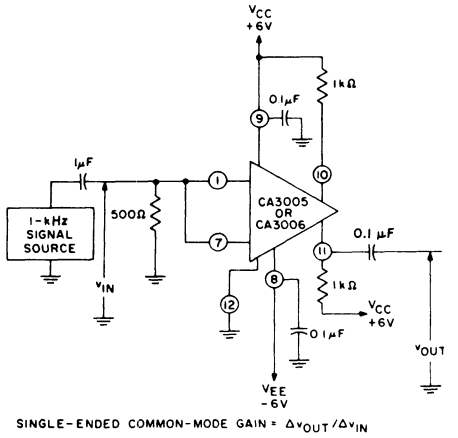


Fig. 19—Schematic of the circuit used to determine the single-ended common-mode gain.

function of voltage for the CA3005 or CA3006 for the two methods. Fig. 20 gives the gain-control characteristic for the CA3005 or CA3006 when the gain-control voltage is applied to the base-bias network of transistor Q_3. Since the

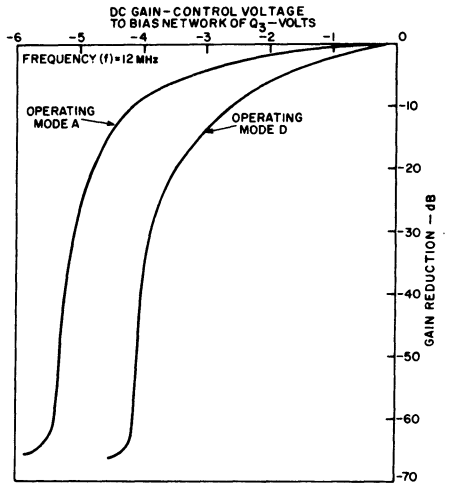


Fig. 20—Gain-control characteristics of the CA3005 or CA3006 as a function of the dc gain-control voltage applied to the bias network of transistor Q_3.

Q_3 bias networks are the same, the gain characteristics for the CA3004 are nearly the same as those for the CA3005 and CA3006. Fig. 21 shows that in the offset method of gain control the gain range is dependent on the polarity of drive. For maximum gain-control range on a single-ended amplifier, the common-collector transistor should be cut off (negative voltage applied to its base). Because of the emitter resistors, R_6 and R_7, the CA3004 circuit will require more dc voltage for the same gain reduction as the CA3005 or CA3006, and the dc voltage required will be a function of the initial operating current.

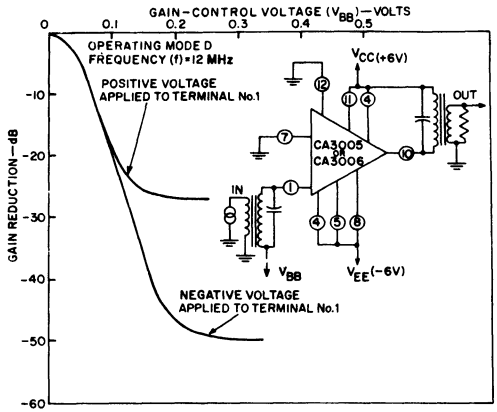


Fig. 21—Gain-control characteristics of the CA3005 or CA3006 as a function of the dc offset voltage, V_{BB}, applied to the differential pair of transistors Q_1 and Q_2.

The maximum gain-control range that can be provided by a reduction in the current of transistor Q_3 varies with frequency as shown in Fig. 22. The maximum gain-control range that can be obtained is dependent on the full gain used, the circuit loading, and the external-circuit layout.

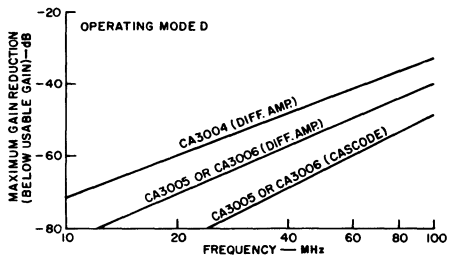


Fig. 22—Maximum gain control provided by variations in the current through Q_3 as a function of frequency.

A large part of the variation in the maximum gain control for the different circuits results from differences in the initial gain of the various circuits. Capacitive feed through appears less for the cascode than for the differential-amplifier configuration.

The following discussion of cross modulation describes variations of the two gain-control techniques.

CROSS-MODULATION AND MODULATION DISTORTION

Cross-modulation and modulation distortion are important considerations in the selection of an amplifier for use in AM systems. Cross-modulation distortion refers to the transfer of modulation from an undesired carrier to the desired carrier by nonlinearities in the amplifier. Modulation distortion is a change in the modulation on the desired carried caused by the same amplifier nonlinearities that produce cross modulation. The two forms of distortion are related by the following equation:

$$\frac{D_2}{V_1^2} : \frac{K}{V_2^2} = \frac{3}{8} m : 1$$

where D_2 is the per cent of distortion in the modulation on the desired carrier (i.e., the modulation distortion), K is the per cent of cross-modulation distortion, V_1 is the amplitude of the desired-carrier voltage at the input, V_2 is the amplitude of the undesired-carrier voltage at the input, and m is the per cent of modulation of the desired carrier.

When D_2 and K are equal and m is 100 per cent, the ratio of V_1 to V_2 is 1.64. In the following paragraphs, data are given for only the cross-modulation distortion. The modulation distortion can be predicted from these data, however, on the basis of the relationship of V_1 to V_2. For example, in Fig. 23, V_2 is given as 22 millivolts for a gain of 0 dB. The value of V_1, then, is 1.64 x 22, or 36 millivolts.

Figs. 23 through 27 show the cross-modulation distortion of the CA3004, CA3005, and CA3006 integrated circuits as a function of their gain-control characteristics in both differential-amplifier and cascode-amplifier configurations. The amount of cross-modulation distortion is determined by the two-generator method with the input of the circuit under test driven from a 50-ohm source and with its output tuned to the frequency of the desired carrier. The amplitude of the undesired-carrier input voltage is that necessary to produce 10 per cent cross-modulation distortion for each manually determined gain-control setting.

Differential-Amplifier Configurations — The availability of internal connection points make possible several methods of gain control in differential-amplifier configurations of the CA3004, CA3005, and CA3006 circuits. Only two of these methods need be considered, however, to obtain an adequate evaluation of the cross-modulation characteristics. These include (1) the variation of the current in the constant-current transistor, Q_3, and (2) the use of an offset voltage to produce an unbalance in the differential pair of transistors, Q_1 and Q_2.

Fig. 23 shows the cross-modulation distortion characteristics of the CA3004, CA3005, and CA3006 with the differential pair of transistors balanced and with agc applied to the constant-current transistor. Because of the increased linearity that results from the emitter resistors R_6 and R_7, the CA3004 has improved cross-modulation characteristics at high current. The interfering signal voltage required to produce 10 per cent of cross modulation distortion is practically a constant over the entire agc range for the CA3005 and CA3006. The value of the interfering signal voltage (approximately 15 mv) for the CA3005 and CA3006 is twice that calculated from the logarithmic transconductance characteristic of a single transistor.

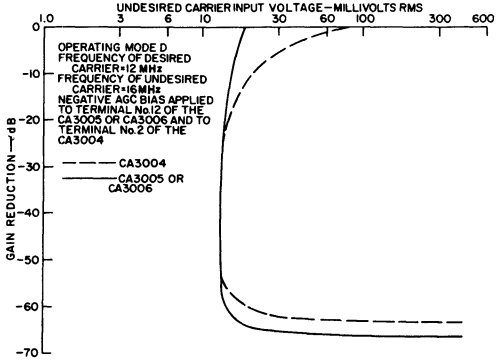


Fig. 23—Gain control as a function of the input voltage from an undesired carrier that will produce cross-modulation distortion of 10 per cent for balanced differential-amplifier operation of the CA3004, CA3005 and CA3006. The gain-control voltage is applied to bias network of the constant-current transistor.

Fig. 24 shows the cross-modulation distortion characteristic of the CA3005 and CA3006 when an offset voltage is applied to control the gain. The improved cross modulation performance at −5 dB gain is coincident with an inflection point on the curve of tranconductance as a function of input offset voltage. This point occurs at an offset voltage of approximately 50 millivolts.

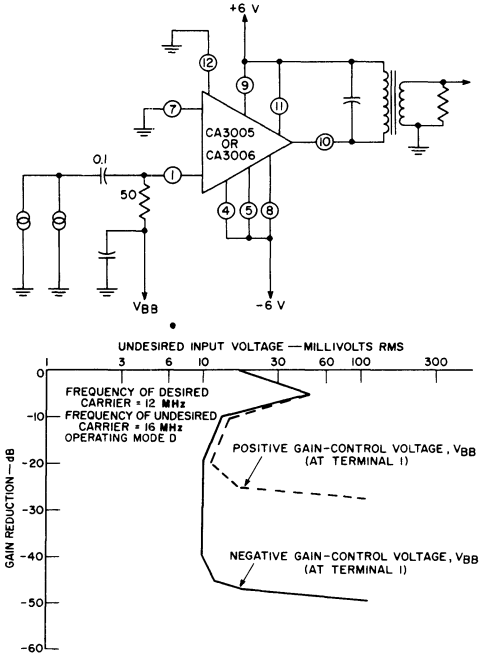


Fig. 24—Gain control as a function of the undesired-carrier voltage that will produce 10 percent cross-modulation distortion for differential-amplifier operation of the CA3005 or CA3006 when gain control is provided by the application of an offset voltage to the differential pair of transistors.

The cross-modulation performance is improved by the offset of the differential pair of transistors. Fig. 25 shows the cross-modulation data when an initial offset of 50 millivolts is employed and agc is applied to the constant-current transistor. The introduction of the unbalance reduces the cross-modulation distortion to approximately 10 dB less than that of the balanced circuit. This reduction in cross-modulation distortion, however, is accompanied by a decrease in gain of approximately 5 dB.

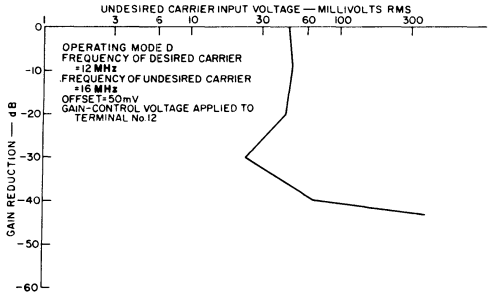


Fig. 25—Gain control as a function of the input voltage from an undesired carrier that will produce cross modulation distortion of 10 per cent, for a differential-amplifier configuration of the CA3005 or CA3006 having a 50-millivolt offset and with the gain control voltage applied to the bias network of the constant-current transistor.

Cascode Configurations — Cross-modulation data for cascode configurations of the integrated-circuit rf amplifiers are given for only the CA3005 and CA3006 circuits, because the CA3004 circuit is not designed for this type of operation. When the CA3005 or CA3006 is operated in the cascode configuration, gain control may be provided by either of two methods: (1) A negative voltage may be applied to the base of transistor Q_3 or (2) A negative voltage may be applied to the base of transistor Q_1.

In the first method, the gain is reduced by the application of a negative-going voltage at terminal 12. As the amplitude of this voltage is increased to the value required to cut off transistor Q_3, the gain of the circuit is decreased. The cross-modulation distortion characteristics for this type of gain control are shown in Fig. 26. The cross-modulation characteristics are comparable to those of a single transistor having a bypassed emitter resistor.

The cross-modulation distortion characteristics obtained for the second method of gain control are shown in Fig. 27. No improvement in cross-modulation characteristics over those obtained for the first gain-control method are observed, although the agc range is greater.

MIXER CAPABILITIES

The CA3004, CA3005, and CA3006 integrated circuits may be used as mixers, modulators, and product detectors. The schematic diagrams in Figs. 28(a) and 28(b) illustrate the use of these circuits in mixer applications. The oscillator input is injected at the base of transistor Q_3 (because there is no direct-base connection available on the CA3004, a higher oscillator drive voltage is required for this circuit); the rf input is injected single- or double-ended to the bases of transistors Q_1 and Q_2. The use of a center-tapped inductor for the output tuned circuit (double-ended) allows the common-mode signal of the oscillator to be balanced out so that the oscillator will not overload subsequent stages, and provides carrier suppression for modulators.

The gain performance and generation of harmonics in the CA3004, CA3005, and CA3006 mixer circuits are dependent on the amplitude of the oscillator drive signal and the dc bias. The expression for product detection or frequency multiplication in the CA3005 or CA3006 (consult Fig. 29) are determined as follows:

$$e_o = e_1 g_m Z_L \qquad (1)$$

where e_o is the output voltage, e_1 is the differential input voltage, g_m is the transconductance of the differential pair of transistors (Q_1 and Q_2), and Z_L is the load impedance (total between collectors). For a balanced circuit, the transconductance is given by

$$g_m = \frac{\alpha q}{2KT} I_o \qquad (2)$$

The term I_o, is used to represent the collector current of

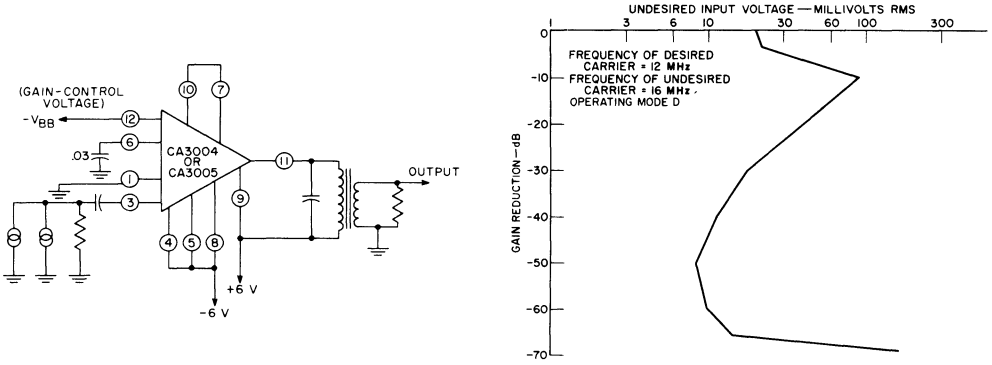


Fig. 26—Gain control of the CA3005 or CA3006, in a cascode configuration, as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion when the gain is controlled by a negative bias voltage applied to the base of transistor Q_3 The schematic diagram illustrates the circuit configuration.

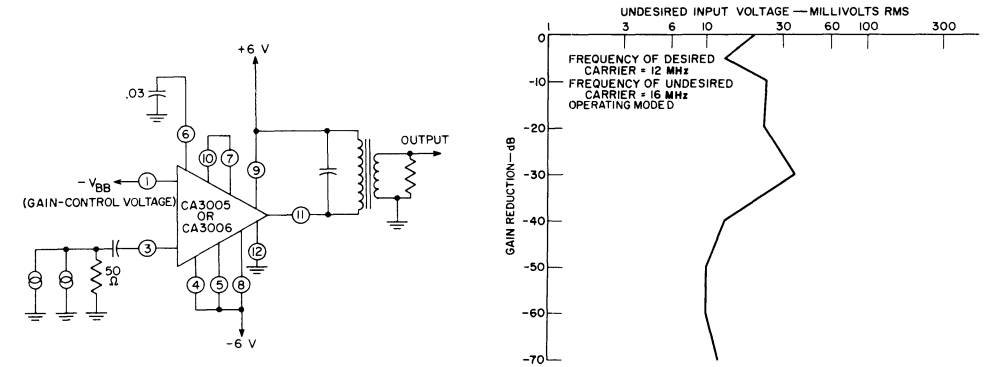


Fig. 27—Gain control of the CA3005 or CA3006, in a cascode configuration, as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion when the gain is controlled by a negative bias voltage applied to the base of transistor Q_1. The schematic diagram illustrates the circuit configuration.

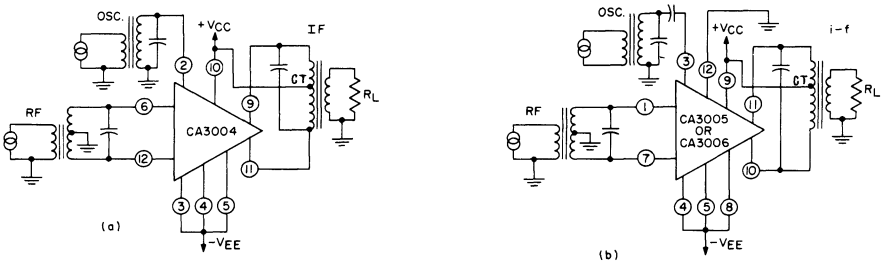


Fig. 28—Circuit diagrams for the use of the integrated-circuit rf amplifiers as mixers (operating mode D): (a) CA3004; (b) CA3005 or CA3006.

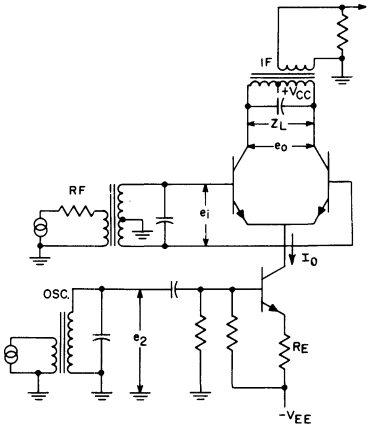


Fig 29—Circuit diagram of a CA3005 or CA3006 balanced mixer (operating mode D). The equation derived for product detection or multiplication are based on this circuit.

transistor Q_3 and may be expressed as

$$I_o = g_{m_2} e_2 \quad (3)$$

where g_{m_2} is the transconductance of transistor Q_3 and e_2 is input voltage applied to transistor Q_3. The output voltage, e_o, therefore is given by the following equation:

$$e_o = \frac{\alpha q}{2KT} e_1 e_2 g_{m_2} Z_L \quad (4)$$

Eq. (4) is a general expression for the output voltage of the mixer having input signals e_1 and e_2. With emitter degeneration in the constant-current transistor (Q_3), g_{m_2} is essentially constant for a sufficiently large emitter current (> 1 ma); the current I_o, therefore, follows the applied voltage e_2.

When e_1 and e_2 are sinusoidal and g_m is a constant, the input signal voltages are given as follows:

$$e_1 = E_1 e^{j\omega_1 t} + \overset{*}{E}_1 e^{-j\omega_1 t} \quad (5)$$

$$e_2 = E_2 e^{j\omega_2 t} + \overset{*}{E}_2 e^{-j\omega_2 t} \quad (6)$$

($\overset{*}{E}_1$ is the conjugate of E_1, and $\overset{*}{E}_2$ is the congugate of E_2)

With the substitution of these relationships, the equation for the output voltage the CA3005 or CA3006 now becomes

$$e_o = \frac{\alpha q}{2KT} g_{m_2} Z_L [E_1 E_2 e^{j(\omega_1+\omega_2)t} + \overset{*}{E}_1 \overset{*}{E}_2 e^{-j(\omega_1+\omega_2)t}]$$

$$+ \frac{\alpha q}{2KT} g_{m_2} Z_L [E_1 \overset{*}{E}_2 e^{j(\omega_1-\omega_2)t} + \overset{*}{E}_1 E_2 e^{-j(\omega_1-\omega_2)t}] \quad (7)$$

Eq. 7 gives the output voltage for a CA3005 or CA3006 used as a product detector or multiplier. (Note that only the two sideband frequencies are included in the output). The requirements for product detectors or multipliers are that the circuit should be biased in a linear region with a small signal voltage applied. Because $\alpha q\ g_{m_2}/2KT$ is essentially constant, the gain of the mixer is determined from Z_L and the $e_1 e_2$ product. The linearity of the CA3006 is illustrated by the curve of the conversion transconductance as a function of the oscillator voltage, shown in Fig. 30. (Although the curve is plotted on logarithmic paper because of the wide range, the relationship is linear.) The gain reaches a maximum value at approximately 2.5 volts rms. Because measurement inaccuracies prevent the use of this curve to determine harmonic generation, spurious-signal measurements were taken on CA3005 and CA3006 mixer circuits. For these measurements, the rf input was untuned and the oscillator and if frequencies were held constant. For a fixed amplitude of oscillator injection on terminal 3, the rf was varied in frequency, and the amplitude of the responses was recorded. The results are shown in Table V. The spurious signals generated are a function of oscillator drive. A low oscillator drive (0.1 volt rms) produced only three spurious signals for which the rejection was less than 70 dB down. These measurable spurious responses were third-order products that involved the second harmonic of either the oscillator or rf signal. The relative if gain increases with decreasing oscillator drive because of lower mixer gain.

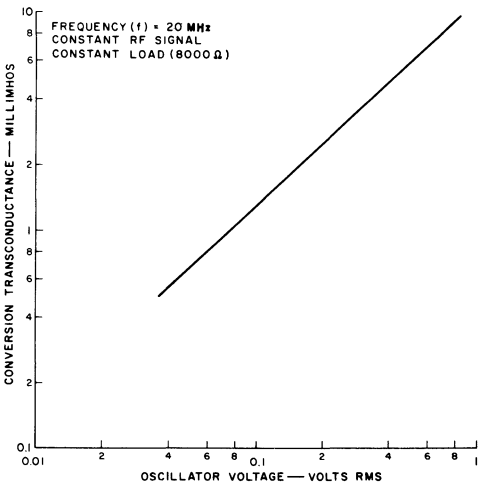


Fig. 30—Conversion gain of a CA3005 or CA3006 mixer circuit as a function of the oscillator voltage.

The common-mode cancellation of the oscillator signal at the collector outputs is indicative of the carrier suppression that can be provided in modulators. The carrier suppression is a function of output tuned-circuit balance and the transistor offset voltage. The contribution of the offset is illustrated in Figs. 31 and 32 which show the output signal as a function of the offset voltage for the CA3004 and for CA3005 and CA3006 respectively. These data were obtained on circuits operated with a balanced output tuned to the oscillator frequency.

TABLE V

Response of a CA3005 or CA3006 Mixer to Spurious Harmonics

Frequency	Signal Freq., f_x (MHz)	V_{osc} at term. 3 (rms volts)	Diff.-Freq. Output (dB relative to $f_o - f_x$)	V_{osc} at term. 3 (rms volts)	Diff.-Freq. Output (dB relative to $f_o - f_x$)	V_{osc} at term. 3 (rms volts)	Diff.-Freq. Output (dB relative to $f_o - f_x$)	V_{osc} at term. 3 (rms volts)	Diff.-Freq. Output (dB relative to $f_o - f_x$)
$f_o - f_x$	1.0	1	0	0.7	0	0.3	0	0.1	0
f_{if}	0.659	1	7.5	0.7	10	0.3	18	0.1	27
$2f_x - f_o$	1.159	1	−53.1	0.7	−53.1	0.3	−54.9	0.1	−52.3
$2f_o - 2f_x$	1.329	1	−76.1	0.7	—	0.3	—	0.1	—
$2f_x - 2f_o$	1.988	1	−75.5	0.7	—	0.3	—	0.1	—
$f_x - f_o$	2.318	1	0	0.7	0	0.3	0	0.1	0
$2f_o - f_x$	2.659	1	−31.7	0.7	−35	0.3	−39.7	0.1	−47.8
$2f_x - 3f_o$	2.813	1	−79.6	0.7	—	0.3	—	0.1	—
$f_x - 2f_o$	3.977	1	−31.7	0.7	− 35	0.3	−39.7	0.1	−47.8
$3f_o - f_x$	4.309	1	−35.8	0.7	−59.3	0.3	−74.7	0.1	—
$f_x - 3f_o$	5.627	1	−38.5	0.7	−57	0.3	−74	0.1	—
$4f_o - f_x$	5.977	1	−38.9	0.7	−63	0.3	—	0.1	—

f_o = 1.659 Mc/s; V_{osc} = oscillator injection voltage.

All blank spaces indicate difference-frequency output more than 70 dB below the $f_o - f_x$ output.

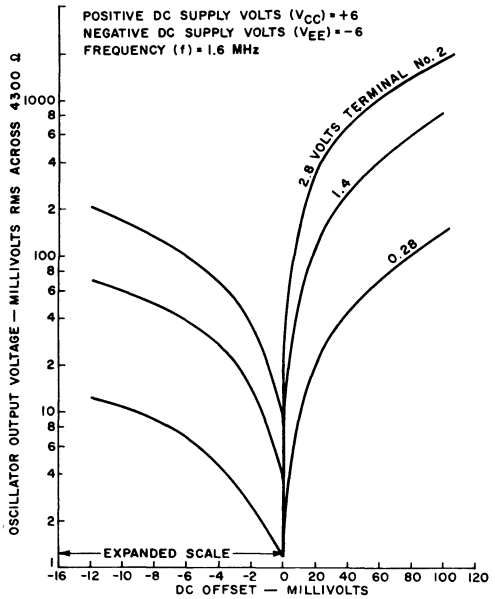


Fig. 31—Cancellation of the oscillator signal at the output of a CA3004 mixer as a function of the dc offset voltage.

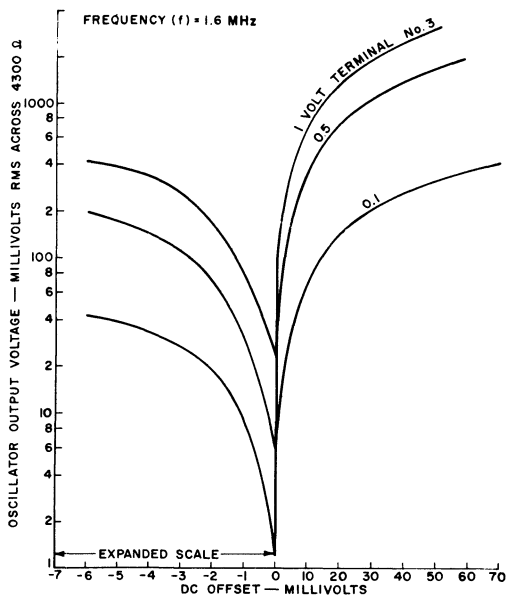


Fig. 32—Cancellation of the oscillator signal at the output of a CA3005 or CA3006 mixer as a function of the dc offset voltage.

LIMITER CHARACTERISTICS

Differential-Amplifier Configuration — The differential-amplifier, driven by a constant-current transistor, is probably the optimum circuit configuration for bipolar transistor limiters. The advantage of such circuits in limiter applications is that collector saturation of either transistor Q_1 or Q_2 can be avoided because of the action of the constant-current transistor Q_3. Figs. 2 and 3 show typical limiting characteristics for the CA3004 and for the CA3005 and CA3006 respectively. For the CA3005 and CA3006 (no emitter degeneration), "hard" limiting is achieved for a peak-to-peak input of 300 millivolts for all values of total dc current (I_{CC}). For the CA3004, the input voltage required for "hard" limiting is a function of I_{CC} because of the linearizing effect of the degenerative emitter resistors, R_6 and R_7. As saturation

TABLE VI
Limiter Performance of a Differential Amplifier

V Supply (volts)	$I_{C1} + I_{C2}$ *(mA)*	*Maximum Resistive Load (ohms)*	*Maximum Tuned Load (ohms)*	*Voltage Gain With Emitter Degeneration (dB)*		*Voltage Gain Without Emitter Degeneration (dB)*	
				Resistive Load	*Tuned Load*	*Resistive Load*	*Tuned Load*
6	0.5	12000	24000	31	37	35	41
6	1.0	6000	12000	28	34	35	41
6	2.0	3000	6000	25	31	35	41
6	3.0	2000	4000	22	28	35	41

$$R_L = \frac{V_{supply}}{I_{C1} + I_{C2}} \quad \text{Resistive Load}$$

$$R_L = \frac{2\,V_{supply}}{I_{C1} + I_{C2}} \quad \text{Tuned Load}$$

$g_m R_L$ = voltage gain

must be prevented for good limiting, a maximum load resistor and low-level voltage gain exists for a given I_{CC} and positive supply voltage. Table VI shows the maximum resistor values and voltage gains usable for $V_{CC} = 6$ volts, for the three circuit types. The low-level transconductance can be obtained from the slope near the origin for the curves shown in Figs. 2 and 3. The maximum voltage gain is independent of I_{CC} in the CA3005 and CA3006 and is dependent on I_{CC} in the CA3004. Figs 5 through 8 show the I_{CC} currents and transconductance for optional operating conditions.

When the differential amplifier is used for limiting, the emitter-to-base breakdown voltage for transistors Q_1 and Q_2 cannot be exceeded without degradation in performance. For the CA3004, CA3005, and CA3006, this voltage including a safety margin should not exceed 2.5 volts rms. Either of two methods may be used to prevent this value being exceeded: (1) Make sure the preceding stage limits before the input voltage reaches 2.5 volts (maximum voltage gain per stage approximately 20 dB), or (2) add one junction diode (D_1), as shown in Fig. 33 (this allows a maximum usable voltage gain consistent with good limiting and stability).

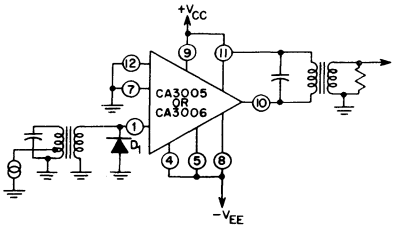


Fig. 33—Circuit diagram of a CA3005 or CA3006 differential-amplifier limiter that uses a diode to provide input overload protection.

Cascode Amplifier — The limiting characteristics of the CA3005 or CA3006, when used as a cascode amplifier are dependent on the current limiting in transistor Q_3 or the voltage limiting of transistor Q_1 (high-impedance output load). Limiting characteristics for both cases are shown in Figs. 34 and 35. The data in Fig. 34 are obtained with a collector load of 500 ohms. This limiting characteristic is "soft" and is acceptable over only a 20-dB range. The peak-to-peak voltage at the collector is never large enough to cause saturation. The limiting characteristic shown in Fig. 35 is obtained with a collector load of 5000 ohms, and saturation of transistor Q_1 occurs. The limiting is harder and covers a broader range, but severe tuned-circuit loading occurs.

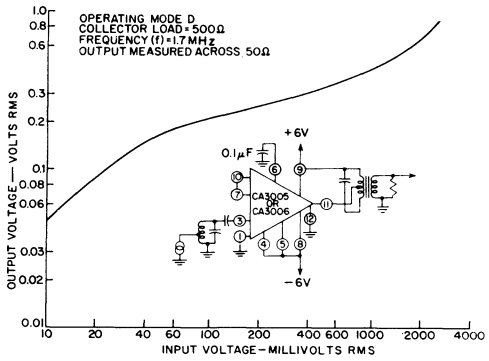


Fig. 34—Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 500-ohm collector load impedance.

APPLICATIONS OF THE RF AMPLIFIER CIRCUITS

RF AMPLIFIER

Figs. 36, 37, and 38 illustrate the use of the CA3004, the CA3005 or CA3006 differential-amplifier configurations, and the CA3005 or CA3006 cascode configurations, respectively, as single-ended rf amplifiers. Adjustable matching networks, derived from the y parameters, are included in each circuit. The values of the adjustable components as

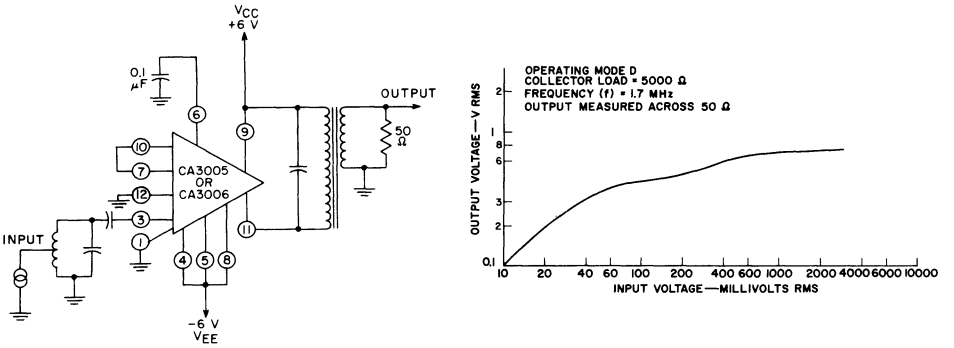
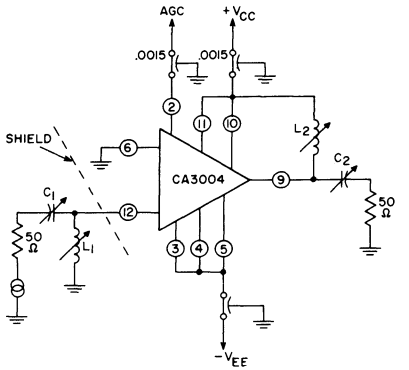


Fig. 35—Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 5000-ohm collector load impedance.



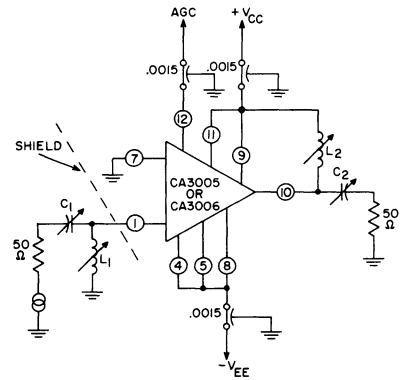
CIRCUIT ELEMENTS

FREQUENCY (MHz)	L_1 *(μH)*	C_1 *(pF)*	L_2 *(μH)*	C_2 *(pF)*
30	1.8-2.7	2-10	1.8-2.7	2-10
100	0.15-0.3	0.9-7	0.1-0.2	0.9-7

POWER GAIN PERFORMANCE

DC SUPPLIES (volts)	*POWER GAIN (dB) 30 MHz*	*100 MHz*
±6	24	12

Fig. 36—Circuit used to determine the rf performance capabilities of a CA3004 integrated-circuit rf amplifier.



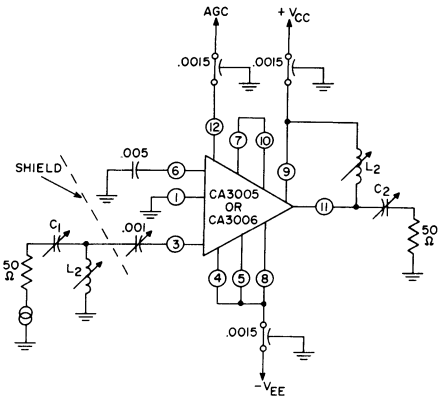
CIRCUIT ELEMENTS

FREQUENCY (MHz)	L_1 *(μH)*	C_1 *(pF)*	L_2 *(μH)*	C_1 *(pF)*
30	1.2-2	5-40	1.2-2	1.5-20
100	0.4-0.7	1-12	0.25-0.5	1-12

POWER GAIN PERFORMANCE

DC SUPPLIES (volts)	*POWER GAIN (dB) 30 MHz*	*100 MHz*
±6	29	18
±4.5	27.8	16
±3	23.0	11.5

Fig. 37—Circuit used to determine the rf performance capabilities of a CA3005 or CA3006 integrated-circuit rf amplifier in a differential-amplifier configuration.



CIRCUIT VALUES

FREQUENCY (*MHz*)	L_1 (*μH*)	C_1 (*pF*)	L_2 (*μH*)	C_2 (*pF*)
30	0.3-0.6	14-150	0.8-1.4	5-40
100	0.07-0.12	5-40	0.15-.3	5-40

POWER GAIN PERFORMANCE

DC SUPPLIES (*volts*)	*POWER GAIN* (*dB*) *30 MHz*	*100 MHz*
±6	36	20
±4.5	33	18.5
±3	21.5	15.0

Fig. 38—Circuit used to determine the rf performance capabilities of a CA3005 or CA3006 integrated-circuit rf amplifier in a cascode configuration.

well as typical power gains are also shown in the figures. A conjugate match at the input is provided for all configurations. A conjugate match at the output is impossible for the cascode configuration (as pointed out in the discussion of y parameters). At 30 MHz, the CA3005 differential amplifier output was mismatched. At high gains, the circuit feedback (y_r) is low, but the external-circuit layout adds feedback.

Tuned IF Amplifier — Two or more CA3004, CA3005 or CA3006 integrated circuits can be connected in cascade for use as a tuned if amplifier for either AM or FM applications. The schematic diagrams of two three-stage 12-MHz amplifiers are shown in Figs. 39 and 40, for FM and AM use, respectively. Both if amplifiers are housed in metal boxes, and adequate shielding and supply decoupling are provided.

The amplifier shown in Fig. 39 (limiting amplifier for FM use), is designed to provide a gain per stage of 26 dB. At this gain per stage, diodes are required at the input to prevent base-to-emitter breakdown. For operation as a low-level limiter, the circuit input is matched, and the required gain fixes the unloaded Q of the tuned circuit and the collector load. Good noise performance for the first stage is obtained by the use of a high Q (200) toroid inductor for input transformer T_1. The other transformers are slug-tuned and have relatively low unloaded Q's (70 to 100) which contribute the necessary insertion loss for the required gain. A lower unloaded Q was required for transformer T_2, so 10,000 ohms of resistance was added in parallel with this transformer. Little or no skew is detectable in the response characteristic for this circuit, shown in Fig. 41. The limiting characteristic of the circuit is shown in Fig. 42. Other typical over-all performance characteristics are:

Total power drain = 48 milliwatts
Overall power gain = 77 dB
3-dB bandwidth = 300 kHz
Input limiting level = 30 microvolts
Noise figure = 4 dB

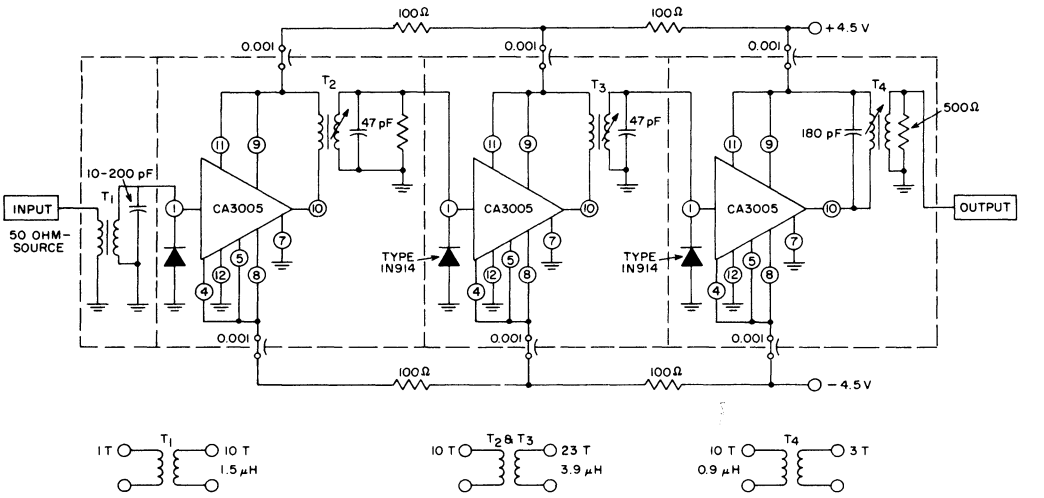
The AM circuit (Fig. 40) uses three CA3004 circuits and is designed to provide a stage gain of 25 dB. The source resistance to the input circuit was chosen as 800 ohms as a satisfactory compromise for gain, noise figure, and modulation-distortion performance. Input and output transformers, T_1 and T_4, have high unloaded Q's (200) to preserve good noise performance and to maximize the output power. The interstage transformers, T_2 and T_3, have low unloaded Q's (37) to achieve the required gain. The second detector has a 3-dB bandwidth of 5.0 kHz, the typical over-all performance characteristics are:

Power drain = 83 milliwatts
Power gain (to second-detector input) = 76 dB
AGC range (1st stage) = 60 dB
Noise figure = 4.5 dB
3-dB bandwidth = 160 kHz

The signal-to-noise ratio of the circuit as a function of the input is shown in Fig. 43, and the frequency-response characteristic is shown in Fig. 44.

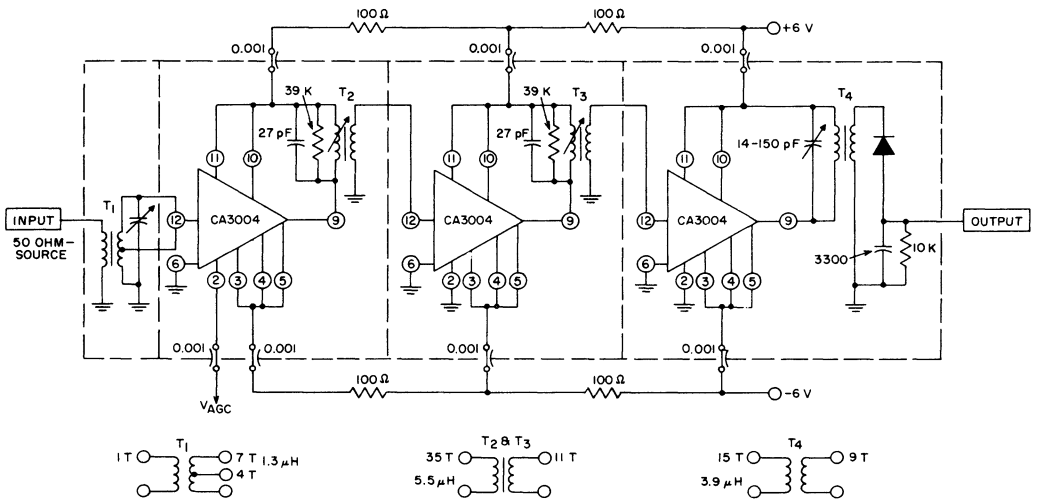
Mixers — The use of the CA3004 and the CA3005 or CA3006 as balanced mixers to convert 20 MHz to 1.75 MHz., is shown in Fig. 45. Because the input impedance of the two circuits differ by a factor of approximately 2:1, typically 4000 ohms for the CA3004 and 2200 ohms for the CA3005 or CA3006, different input transformers (T_1) are required; the other tuned circuits, however, are the same. The output load impedance between collectors is approximately 8000 ohms. The conversion power gain and noise figure as a function of the oscillator drive are shown in Fig. 46 and 47. Power gain increases and noise figure decreases with increases in the oscillator drive.

Suppressed-Carrier Modulator and Product Detector— The CA3005 and CA3006 were used in a suppressed-carrier double-sideband modulator and product detector. The double-sideband modulator is a convenient vehicle to evaluate carrier suppression and product detection. With the two circuits coupled together, the relation between modulation



NOTES: 1. Transformer T_1 is a Ferramic Q-2 Toroid Type (unloaded Q = 200).
2. Transformers T_2, T_3, and T_4 are slug-tuned with Carbonyl IT-75 material (unloaded Q = 75).

Fig. 39—Schematic diagram of a three-stage, 12-MHz limiting if amplifier that uses CA3005 circuits in operating mode D.



NOTES: 1. Transformers T_1 and T_4 are Ferramic Q-2 Toroid Types (unloaded Q =200).
2. Transformers T_2 and T_3 are slug-tuned with Carbonyl IT-71 material (unloaded Q = 70).

Fig. 40—Schematic diagram of a three-stage, 12-MHz gain-controlled AM amplifier that uses CA3004 circuits in operating mode D.

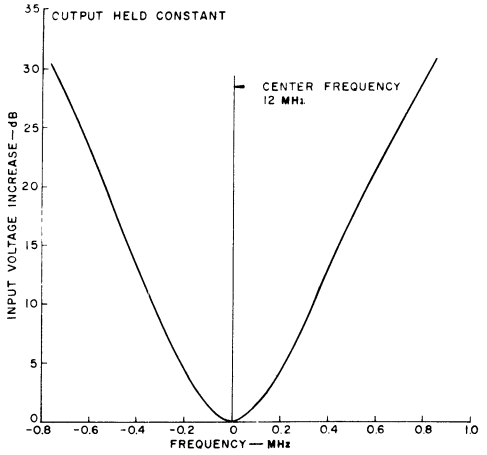


Fig. 41—Frequency-response characteristics of the 12-MHz limiting amplifier shown in Fig. 39.

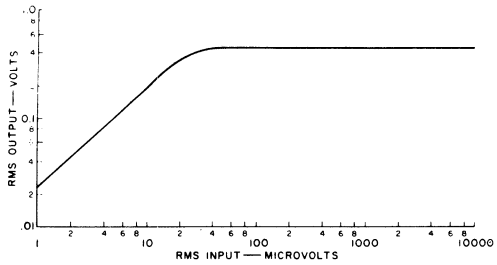


Fig. 42—Limiting characteristics of the 12-MHz limiting amplifier shown in Fig. 39.

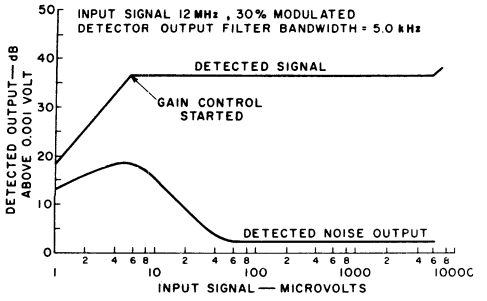


Fig. 43—Output signal-to-noise ratio as a function of the input signal for the 12-MHz gain-controlled amplifier shown in Fig.40 when gain control is used in only the first stage.

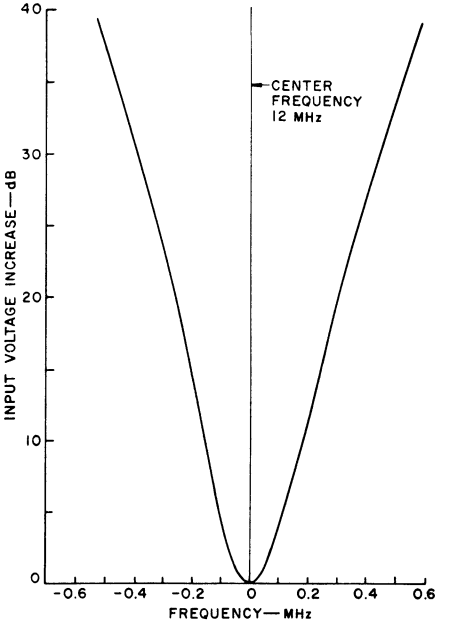


Fig. 44—Frequency-response characteristics of the 12-MHz gain-controlled amplifier shown in Fig. 40.

distortion and drive levels is readily established.

Feedback may cause oscillation or unbalance; care must, therefore, be taken in the external-circuit layout design. Shielding must also be provided for both the double-sideband modulator and product detector.

The circuit diagram of the double-sideband modulator is shown in Fig. 48. The modulating signal is applied single-ended to the differential pair of transistors, Q_1 and Q_2, and the oscillator signal is applied to the base of transistor Q_3. The output is taken double-ended from the balanced transformer, T_2. The carrier suppression is a function of bilateral symmetry (offset, output-transformer balance, and modulation drive circuits) and the modulation-to-carrier drive ratio. With the external-circuit bilateral symmetry carefully preserved, the carrier output is approximately 25 dB below the double-sideband output for CA3006 units (offset $\leqq$ 1 millivolt) operated with a drive v_1 = 10 millivolts rms and v_2 = 31.5 millivolts rms. Although the signal-to-carrier ratio of 25 dB represents an inadequate rejection for most systems (40 to 60 dB is usually required), this value relaxes the filter requirements from those necessary on more commonly used single-sideband modulators. An improvement over the 25-dB ratio is obtained if the modulation drive v_1 is increased and the carrier drive v_2 is decreased, because the output is a function of the product of v_1 and v_2.

The circuit diagram for a product detector is shown in Fig. 49. The product detector which provides the advantage

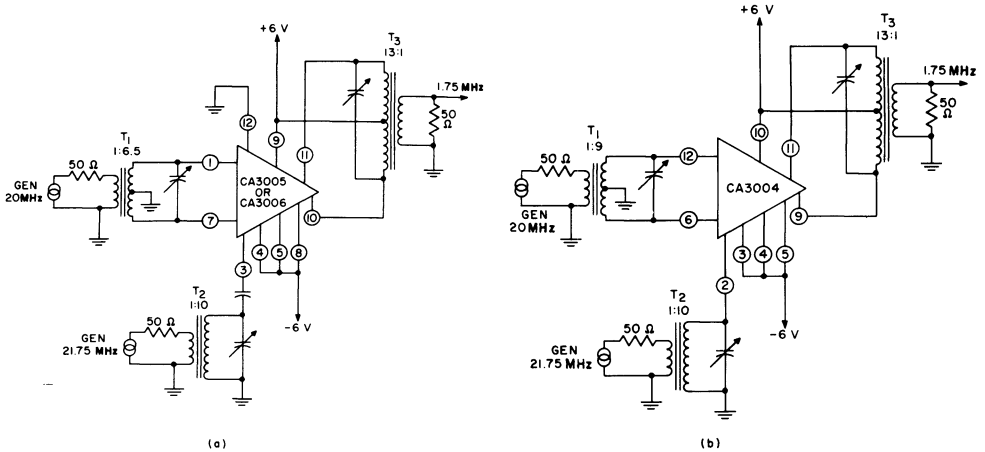


Fig. 45—Circuit diagrams for the use of CA3004, CA3005, and CA3006 integrated circuits as balanced mixers to convert an input frequency of 20 MHz to an output frequency of 1.75 MHz.

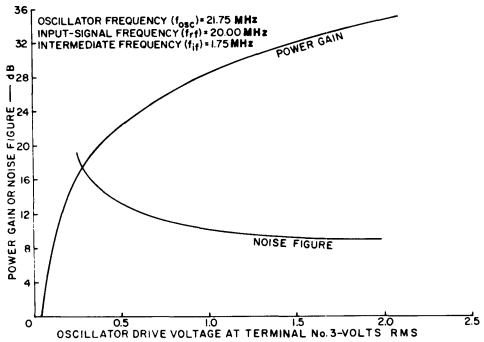


Fig. 46—Power gain and noise figure as a function of the oscillator drive voltage for the CA3005 or CA3006 balanced mixer.

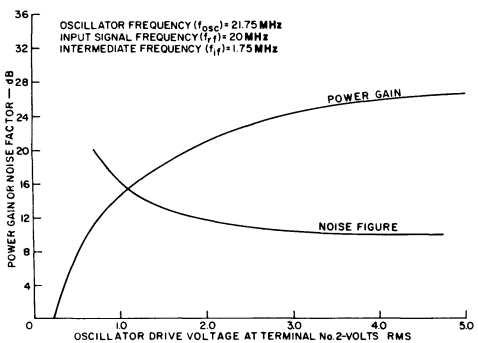


Fig. 47—Power gain and noise figure as a function of the oscillator drive voltage for the CA3004 balanced mixer.

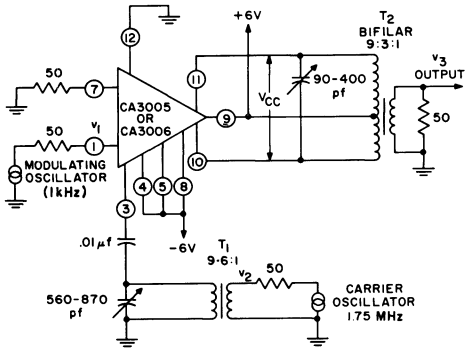


Fig. 48—Circuit diagram for the use of the CA3005 or CA3006 as a double-sideband, suppressed-carrier modulator.

of a double-ended out-of-phase output, is driven through a 50-ohm adjustable feed by the double-sideband signal from the modulator. The levels of v_1, v_2, v_4, and v_5 are altered to establish the relationship between the harmonic distortion and drive levels as well as gain values for typical operation.

The results are shown in Table VII. Overdrive by the modulation (v_1) or the modulated signal (v_4) results in third-harmonic distortion of the detected signal. Note that gain is a function of either the product of v_1 and v_2, or the product of v_4 and v_5.

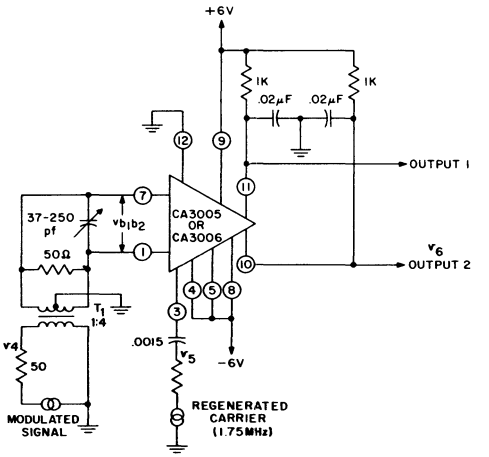


Fig. 49—Circuit diagram for the use of a CA3005 or CA3006 as a product detector.

TABLE VII

Gain and Distortion as a Function of Different Drive Levels for a Double-Sideband Modulator and Product Detector Using the CA3006

Condition	v_1 (mv rms)	v_2 (mv rms)	Terminal 3 Voltage (Volts rms)	v_{ce} (volts rms)	v_3 (mv rms)	v_4 (mv rms)	v_{b1b2} (mv rms)	v_5 (mv rms)	v_6 (mv rms)	Harmonic Distortion (dB below fundamental) 2nd	3rd	4th	5th
v_1 Varied	5	31.5	0.296	0.046	4.95	1	4	0.5	36		54		
	10	31.5	0.296	0.080	8.9	1	4	0.5	36		54		
	30	31.5	0.296	0.25	26.6	1	4	0.5	36		37.5		
v_2 Varied	10	31.5	0.296	0.083	8.9	1	4	0.5	36		54		
	10	100	0.96	0.262	28	1	4	0.5	36		51		
	10	315	2.96	0.83	89	1	4	0.5	36		50		
v_4 Varied	10	31.5	0.296	0.083	8.9	0.5	2	0.5	17.5		54		
	10	31.5	0.296	0.083	8.9	1	4	0.5	36		52		
	10	31.5	0.296	0.083	8.9	3	12	0.5	110		47.5		
	10	31.5	0.296	0.083	8.9	5	20	0.5	188	51	37		59
v_5 Varied	10	31.5	0.296	0.083	8.9	1	4	0.315	23	56	54		
	10	31.5	0.296	0.083	8.9	1	4	0.5	36		54		
	10	31.5	0.296	0.083	8.9	1	4	1.0	86		50		

Notes: 1. Consult Figs. 48 and 49 for explanation of voltage designations.
2. Blank spaces indicate harmonic distortion is more than 60 dB below the fundamental.

Application of RCA Integrated Circuits CD2150, CD2151, and CD2152 ECCSL Logic Gates

BY
M. V. D'AGOSTINO

This Note describes the features and typical applications of three new RCA ultra-high-speed ECCSL* monolithic integrated circuits: the CD2150 Dual Four-Input Gate, the CD2151 Dual Four-Input Gate with "Phantom-OR" Output Capability, and the CD2152 Eight-Input Gate with "Phantom-OR" Output Capability.

These circuits form a compatible group of high-speed logic building blocks that have an average delay per logic decision of approximately 4 nanoseconds. The "current-mode" configuration used in the circuits utilizes the most advanced RCA integrated-circuit fabrication techniques available. To a large extent, the parasitic effects normally encountered in diffused integrated circuits are minimized by use of the differential linear mode of operation. Each circuit is available in a 14-terminal flat-pack and offers the following advantages which contribute directly to over-all system speed and reliability:

(1) inherent high speed as a result of nonsaturated transistor operation;

(2) all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from 10 to 60°C;

(3) complementary OR/NOR emitter-follower output stages which provide a low output impedance and the capability to drive large fan-outs;

(4) constant power-supply current drain which results in low power-supply noise and low ground-lead noise;

(5) small logic swing and thus lower power requirements to charge and discharge circuit capacitances;

(6) capability of the ultra-high-speed ECCSL gates to drive 100-ohm terminated transmission lines;

(7) typical noise immunity of ±350 millivolts over the entire temperature range of 10 to 60°C;

(8) built-in, tracking, reference-threshold voltage to increase system packaging density and eliminate noise pickup on an external threshold voltage line.

* Emitter-coupled current-steered logic (pronounced EXCEL).

DESCRIPTION OF CIRCUITS

The **CD2150 dual four-input gate** shown in Fig. 1 is an ECL (emitter-coupled-logic) gate designed for highspeed OR/NOR (positive logic) or AND/NAND (negative logic)

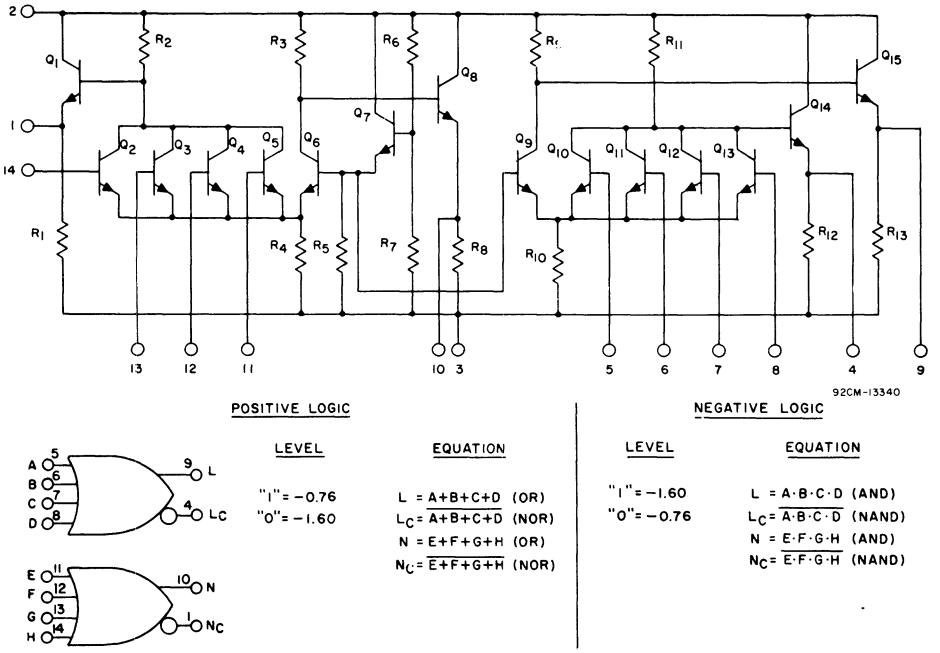


Fig. 1—Schematic diagram, logic diagrams, logic levels, and logic equations for the CD2150 dual four-input gate.

applications. Each gate has four inputs and provides both inverting and noninverting outputs. The switching-threshold reference supply is built in as part of the circuit. The stage delay for each gate is typically 4 nanoseconds, and the total power dissipation including the reference-threshold supply is typically 220 milliwatts. Each gate is capable of driving terminated 100-ohm transmission lines.

For normal operation of the CD2150, terminal 2 (V_{CC}) is grounded and terminal 3 (V_{EE}) is connected to a −5-volt supply. Nominal voltage signal swings for both inputs and outputs are −0.76 to −1.60 volts. The reference-threshold voltage (V_{ref}) is designed to be midway between the "1" and "0" levels, at approximately −1.2 volts, and tracks these voltage levels as they shift with temperature. Because the reference-threshold voltage is internally generated, higher system packaging density can be achieved by use of less interconnecting wiring and fewer circuit types. In addition, the possibility of noise pickup on the reference line is eliminated and system noise immunity is enhanced.

Each gate of the CD2150 operates as follows: With any one of the four inputs (5, 6, 7, 8 or 11, 12, 13, 14) in the high state, the NOR output (terminal 4 or 1) is in the low state and the OR output (terminal 9 or 10) is in the high state. The current in resistor R_4 or R_{10} flows through either of the two sides of the differential amplifier (Q_6 or Q_7, Q_3 Q_4, Q_5 in one gate; Q_6 or Q_{10}, Q_{11}, Q_{12}, Q_{13} in the other). The emitter-follower output stages (Q_1 and Q_8 or Q_{14} and Q_{15}) driven by the current switch provide a low output impedance which contributes to a large fan-out capability, provides the proper level shift to guarantee nonsaturating operation, and isolates the collectors of the switch from the load capacitance.

The **CD2151 dual four-input gate with Phantom-OR output capability** is similar to the CD2150 except that the NOR emitter-follower output resistors (R_1 and R_{12} in Fig. 1) are omitted to facilitate the "Virtual-OR" or "Phantom-OR" logic configuration, as shown in Fig. 2. As a result, the total dissipation of the circuit is approximately 175 milliwatts, and the logic levels are more negative than those

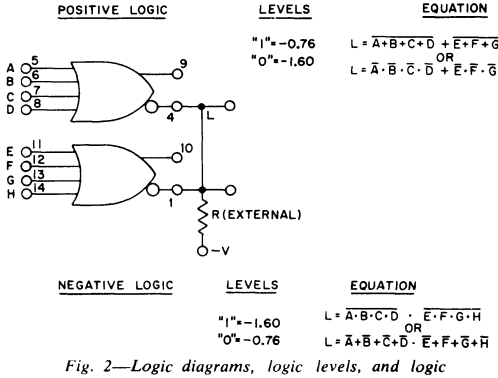


Fig. 2—Logic diagrams, logic levels, and logic equations for the CD2151 dual four-input gate connected in Phantom-OR configuration.

of the CD2150 by approximately 1 per cent. As many as ten CD2151 gates can be tied together with a common-emitter resistor to expand the "Virtual-OR" function.

The external emitter resistor required for use of the NOR outputs of the CD2151 may also be used as a terminating resistor for a transmission line that has a characteristic impedance Z_{oo}, as shown in Fig. 3. For example, an emitter

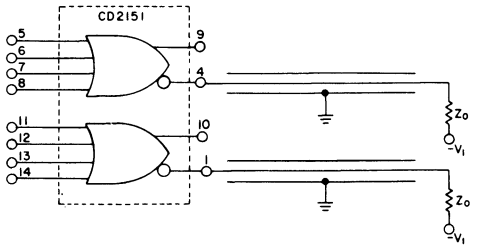


Fig. 3—Use of the CD2151 as a line driver.

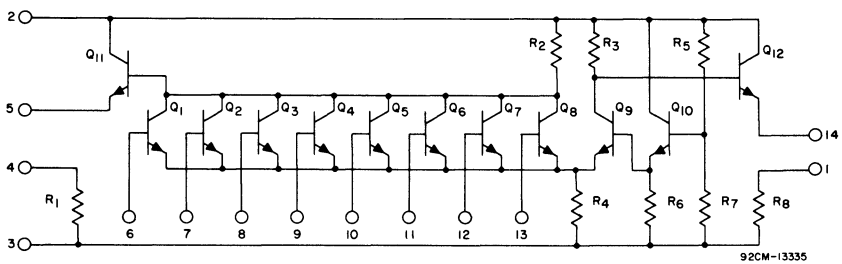
resistor of 100 ohms returned to a −1.6-volt supply can be used to terminate a length of printed strip line having a characteristic impedance of 100 ohms. (The −1.6-volt supply is used rather than the −5-volt supply to limit the current drain from the emitter-follower outputs.) In a system that uses large numbers of terminated lines, an appreciable power savings can be realized by use of the CD2151 circuit rather than the conventional CD2150. Because no appreciable speed advantage results from use of both a terminating resistor and a built-in emitter-follower resistor, the built-in resistor becomes redundant when low-resistance termination is required.

Another advantage of the CD2151 "Phantom-OR" gate is its flexibility. In system locations where very light load capacitance is encountered, a relatively large emitter resistor (in the order of 2000 ohms) can be used and compatible rise and fall times as well as compatible logic levels can still be obtained. As a result, appreciable savings in dissipation can be realized as compared to exclusive use of the conventional gate configuration. The disadvantage of the CD2151, of course, is the use of discrete components in such locations.

The OR outputs of the CD2151 gate have built-in emitter-follower output resistors, and thus are identical to the OR outputs of the CD2150.

The **CD2152 eight-input gate with "Phantom-OR" output capability** shown in Fig. 4 is also an ECL gate designed for high-speed OR/NOR (positive logic) or AND/NAND (negative logic) applications. This circuit provides both an inverting and a non-inverting output, together with eight inputs. A temperature-tracking reference-threshold supply is built in as part of the circuit. The stage delay of the gate is typically 4.5 nanoseconds, and the total power dissipation including the reference supply is 145 milliwatts with the emitter resistors connected. Each output is capable of driving a terminated transmission line.

This gate provides speed, driving capability, and system flexibility similar to those of the CD2150 and CD2151. Additional logic and system strength is provided by the eight inputs and by the Phantom-OR capability at the non-inverting output. It can be seen that a relatively low-power high-speed logic gate can be designed by judicious use of the emitter-follower hook-up options.



POSITIVE LOGIC	LEVEL	EQUATION
	"1" = −0.76	$L = A+B+C+D+E+F+G+H$ (OR)
	"0" = −1.60	$L_C = \overline{A+B+C+D+E+F+G+H}$ (NOR)

NEGATIVE LOGIC	LEVEL	EQUATION
	"1" = −1.60	$L = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$ (AND)
	"0" = −0.76	$L_C = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$ (NAND)

Fig. 4—Schematic diagram, logic diagrams, logic levels, and logic equations for the CD2152 eight-input gate.

NOISE IMMUNITY

From the system standpoint, evaluation of the noise tolerance of an integrated circuit is a very difficult problem. In any system, the noise susceptibility of the logic circuit itself is only part of the consideration; the other part depends on how well a particular configuration can suppress the generation of system noise. The constant power-supply drain, low drive current, and low-output-impedance characteristics of the ECCSL gate make it one of the most suitable logic circuits from the system noise aspect. However, crosstalk caused by stray capacitance, inductive coupling, power supply, and ground-plane impedances and noise caused by reflected waveforms also contribute to system noise. Therefore, the packaging method used in construction of a system using integrated circuits plays an important part in determining over-all system reliability. For a truly valid noise evaluation of a logic gate, it would be necessary to place the gate in the system environment in which it is expected to function and then to impose worst-case conditions peculiar to such a system. This approach, however, would require construction of a prototype system for circuit evaluation. For easier analysis, only the dc noise margin of the gates is discussed in this Note.

Fig. 5 shows typical noise immunity of the CD2150, CD2151, and CD2152 logic gates as a function of temperature. Noise immunity is arbitrarily defined as the voltage

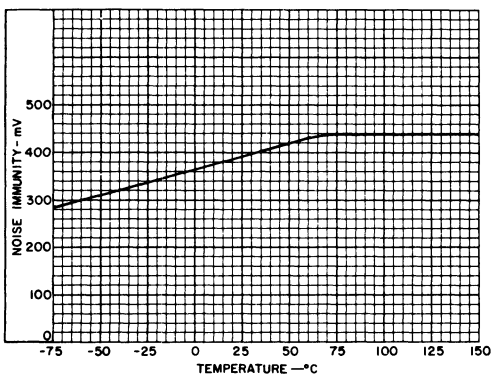


Fig. 5—Typical noise immunity of CD2150, CD2151, and CD2152 gates as a function of temperature.

excursion from the nominal logic level on the input that causes an output voltage level equal to the input level. Under ideal conditions, the threshold voltage of the gate is centered with respect to the upper and lower logic levels, as shown in Fig. 6, and the output is equal to the input when the input is equal to the threshold voltage. For the values shown, the noise immunity of the "1" state is then (−0.76)—(−1.18), or 0.42 volt, and that of the "0" state is (−1.18)—(−1.60), or 0.42 volt.

In practice, however, an accumulation of tolerance factors can cause the reference voltage to shift, as shown by the dashed portion of the transfer curve. (The 50-per-cent point of the transfer curve indicates the position of the threshold voltage. The curve shifts to the left if the threshold becomes more negative and to the right if the threshold becomes more positive.) When a noise level is then superimposed on the nominal "0" level, its positive excursion is not quite so great before the input and output levels are equal. For the example shown, a voltage of −1.242 volts on the input is required to produce a voltage of −1.242 volts on the output. Thus, the noise immunity for the "0" state is (−1.242)—(−1.60), or 0.358 volt, i.e., 62 millivolts less than that of the ideal condition. However, the noise immunity on the "1" side is (−0.76)—(−1.242), or 0.482 volt. The 62 millivolts lost on the "0" side are picked up on the "1" side. (If the reference voltage shifted in the positive direction, the noise immunity would increase for the "0" state and decrease for the "1" state.) The shift in noise immunity (62 millivolts) is smaller than the shift in reference voltage (75 millivolts) because of the gain in the transition region, as evidenced by the slope of the curve. In the curve of noise immunity as a function of temperature shown in Fig. 5, the smaller of the two noise immunity figures is used.

It can be seen that this technique of measuring noise immunity is a form of unity-gain concept applied to input-output dc levels. A noise pulse amplitude which is less than the minimum noise immunity of a gate is attenuated as it passes through successive stages of logic. This concept may be extended to incorporate any degree of safety margin desired. For example, if the worst-case logic "1" and "0" levels are known and the maximum noise amplitude is known, the specification can be established so that an input voltage equal to the sum of the worst-case logic level and the maximum noise amplitude produces an output that has a magnitude within 25 millivolts of the worst-case reference threshold. Effectively, this approach imposes a "tolerance box" around the transfer characteristic that limits the excursion of the nominal reference voltage to some desired percentage, as shown in Fig. 7.

Another advantage of this simple definition of noise immunity is that the effect of load, voltage, and temperature gradients can be determined, at least on an approximate basis, by use of the nomographs described later in this Note. For instance, if the power-supply voltage is reduced so that the logic swing is 0.7 volt rather than 0.84 volt, noise immunity on both the "1" and "0" levels is reduced by (0.84—0.70)/2, or 0.07 volt. The effect of loading and temperature gradient can then be determined by subtraction of the deviation of the logic levels as a result of temperature and loading from the calculated noise immunity. This approach makes the valid assumption that the reference threshold remains essentially centered under voltage variations.

This technique can be illustrated by consideration of a hypothetical situation. Under normal conditions at room temperature, the noise immunity of a gate is assumed to be 390 millivolts. The power-supply voltage is then reduced to −4.5 volts to reduce power dissipation. The nomographs show that the logic swing for the reduced voltage is (−0.75)—(−1.48), or 730 millivolts. The new noise immunity is then 390—(0.84—0.73)/2, or 335 millivolts.

If the "1" output of a gate is then loaded with a current of 2 milliamperes and cooled 20°C below the circuit it is driving, the "1" logic level shifts from −0.75 to −0.792 volt, and the noise immunity is reduced to 335—[(−0.75)

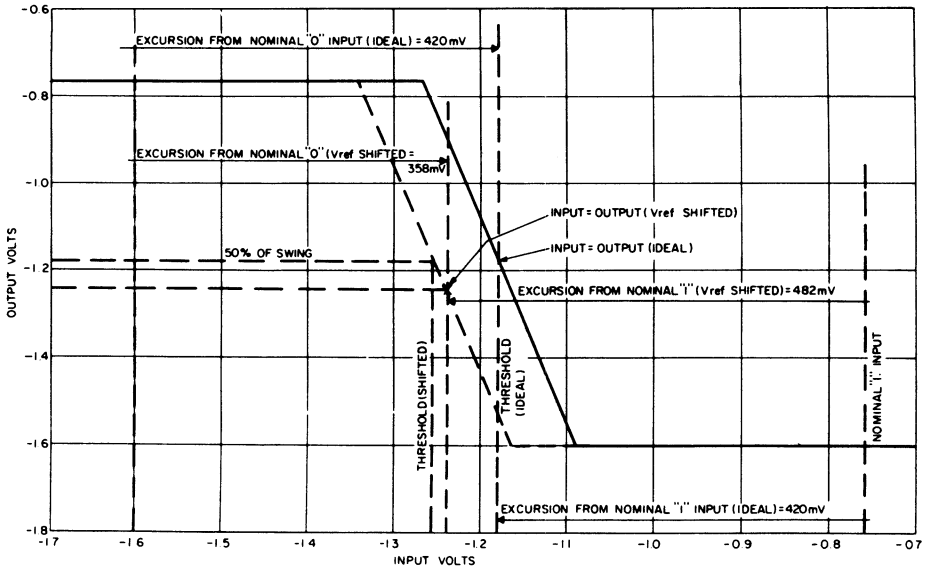


Fig. 6—Transfer characteristics of an ECCSL gate (NOR side).

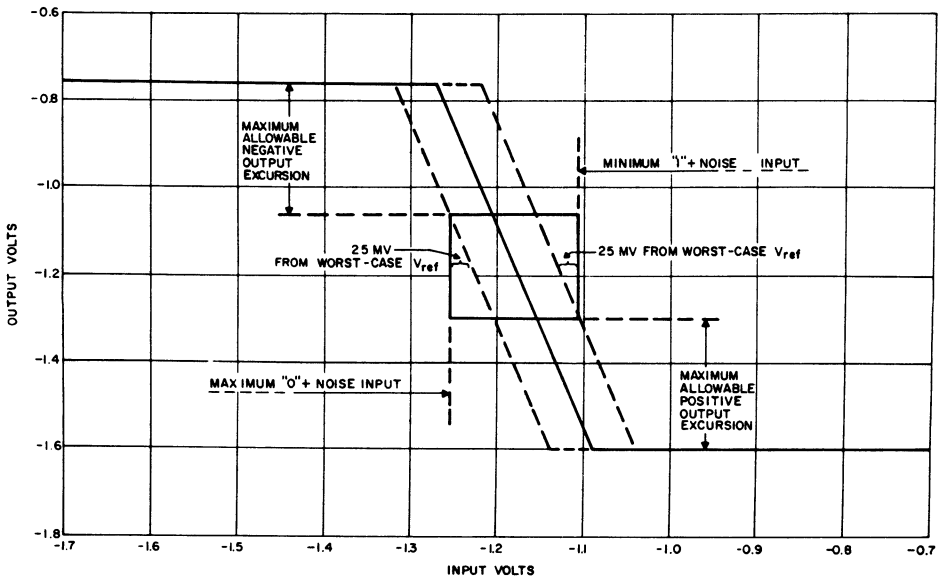


Fig. 7—Diagram illustrating "tolerance box" around transfer characteristic as imposed by noise-immunity specification.

—(−0.792)], or 295 millivolts. The same procedure may be used with different voltage, loading, and temperature-gradient information. This technique is not "worst-case", but shows the trends of dc logic levels and dc noise immunity under varied conditions.

To this point, no mention has been made of the ac noise immunity of the gate. Because of the relative magnitude of the common-emitter capacitance of the differential current switch as compared to the total collector capacitance of the switch, the ac noise immunity is equal to or greater than the dc noise immunity. Therefore, an input noise spike of amplitude "A" causes an output spike of amplitude "B" in the same manner that a noise level of magnitude "A" causes an output level of magnitude "B". Consequently, a dc test is used to evaluate the noise characteristics of the gates because test results can be reproduced more easily.

SYSTEM SPEED

In a synchronous system, the speed at which a given logic operation can be accomplished may be predicted with some degree of accuracy when the gate and flip-flop delay characteristics are known. The following expression relates system speed f_c in megacycles per second to these delays:

$$f_c = \frac{10^3}{t_{pd}(F) + n\,t_{pd}(G) + t}$$

where $t_{pd}(F)$ is the propagation delay of a flip-flop, $t_{pd}(G)$ is the propagation delay of a gate, n is the number of logic stages specified for the system, and t is the time interval, just prior to the trigger time, during which the ac trigger level must be static. All times are expressed in nanoseconds. For two levels of logic in the simple system shown in Fig. 8, $t_{pd}(F)$ is 11 nanoseconds (as shown later in Fig. 15),

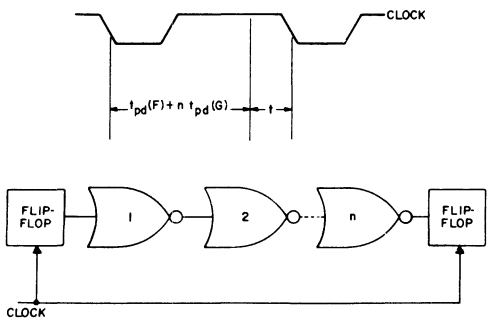


Fig. 8—Diagram of simple logic system.

$t_{pd}(G)$ is 4.0 nanoseconds (as stated previously for the CD2150), and t is 8 nanoseconds (two gate delays for a six-gate binary configuration, as shown later in Fig. 14). The system speed f_c is then given by

$$f_c = \frac{10^3}{[9 + (2)(4.0) + 8]\,[10^{-9}\ \text{s}]} = 40\ \text{Mc/s}$$

This expression can be extended to a worst-case equation as a function of maximum delay times which occur under various system conditions. In a system where long logic trains are used, the dominant speed limitation is presented by the worst-case gate delay, as shown in Fig. 9.

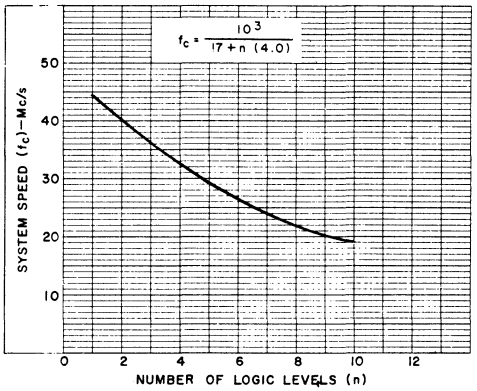


Fig. 9—System speed of a simple logic system as a function of the number of logic levels, n.

EFFECT OF POWER SUPPLY, TEMPERATURE, AND LOADING ON LOGIC LEVELS

The nomographs in Figs. 10 and 11 relate the logic "1" and "0" levels to various combinations of power supply, temperature, and loading. These graphs illustrate the flexibility of the CD2150, CD2151, and CD2152 circuits in meeting various conditions peculiar to given systems. For example, an obvious way to reduce system power dissipation is to reduce the power-supply voltage. However, reducing the voltage also reduces the logic swing. How small a logic swing can be tolerated is a function of how "clean" the system is. Another consideration is heavy dc loading. When heavy dc loads are applied to the outputs of these gates, the "1" level decreases to some extent because the emitter-follower outputs have some finite output impedance. This decrease in one of the levels also results in a reduced logic swing. The power supply may then have to be increased to counteract this loading effect, the amount of increased supply voltage being determined by the system noise-immunity requirement. The nomographs also permit determination of the logic levels of a circuit at a given temperature and load used to drive another circuit located elsewhere in the system at a different temperature. The detailed discussion of noise immunity of these circuits presented earlier more fully illustrates these concepts.

The nomographs shown in Figs. 10 and 11 cover the range of typical parameter variations with temperature and operating points. They indicate the trends that typical units follow, but are not an attempt to guarantee worst-case conditions. Basically, the graphs are generated as follows: First, the dc equation is written for the particular level to be investigated. Parameter variations are then inserted into the equation as a function of temperature, *current, and* other conditions. Finally, either linear or logarithmic scales are constructed for the parameter limits selected, and the scales are geometrically positioned with respect to one another as a function of the moduli used in construction.

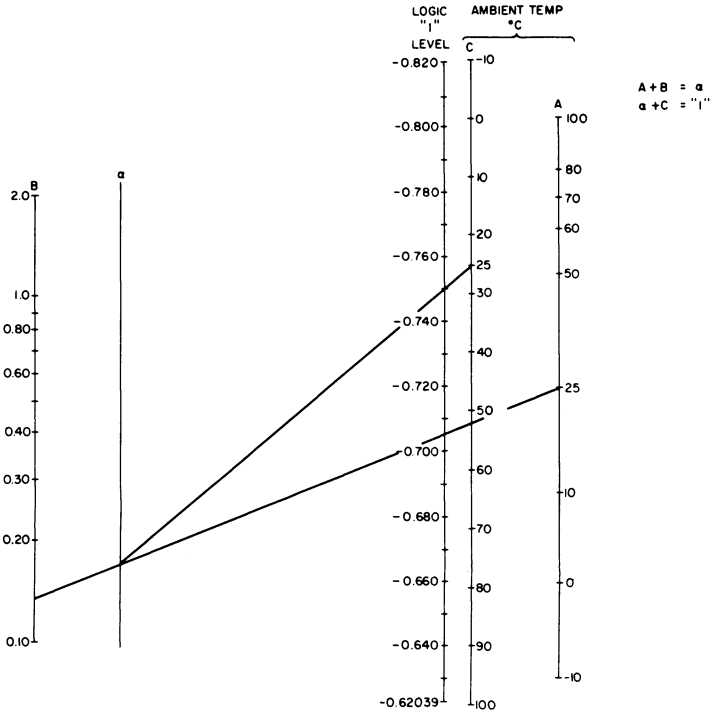


Fig. 10—Nomograph showing parameter relationships of an ECCSL gate for "1" level.

For example, the equation for the NOR output "1" level (e_1) is given by

$$e_1 = \frac{-I R_1 - \beta_3 V_{BE3} + V_{EE}(R_1/R_4)}{\beta_3 + (R_1/R_4)}$$

where I is the load current, R_1 is the collector resistor of the current switch, β_3 is the common-emitter current gain of the emitter-follower output transistor, V_{BE3} is the base-to-emitter voltage drop of the output transistor, V_{EE} is the power supply, and R_4 is the emitter-follower resistor.

This equation can be rewritten with R_1 as a function of temperature and β_3 and V_{BE3} as functions of temperature and current for the following assumptions: (1) the ratio R_1/R_4 is constant with temperature; (2) V_{EE} over the range from −4.5 to −5.5 volts has a negligible effect on the "1" level output of the gate. The load current I and the ambient temperature t then become the variables to be placed on the graphs to generate the corresponding logic "1" states. A similar procedure is used for the "0" state except that V_{EE} has a direct effect on the "0" level, and load current I is assumed to have a negligible effect.

The use of the nomographs is illustrated in Fig. 10. First, a desired temperature (25°C) is selected on scale "A" and a desired load-current condition (0.14 milliampere) on scale "B". A straight line is drawn connecting these two points. A second straight line is then drawn connecting the intersection of the first line on the "α" scale with the same temperature point (25°C) on the "C" scale. The intersection of this line with the "1" scale indicates the approximate NOR output "1" level (750 millivolts). A similar procedure is used for the nomograph shown in Fig. 11. However, the "0" level is determined simply by connection of the temperature and power-supply points with a straight line.

APPLICATIONS

The simplest binary element that can be constructed with the high-speed ECL logic gates described in this Note is a **dc set-reset flip-flop circuit.** Essentially, two inverting gates are cross-coupled, and the inputs to the gates are used as the set-reset inputs. Fig. 12 shows the hook-up and corresponding truth table when the CD2150 dual gate is used. If CD2151 gates were used, external resistors would be required on the outputs, but a power advantage could be realized. Two CD2152 could also be used. The complement of each output is available by use of the OR outputs of the gates. This feature might be utilized to relieve the loading of any one output. The propagation delay of the configuration shown in Fig. 12 is 8 nanoseconds; the rise and fall times are 4 and 3 nanoseconds, respectively.

Fig. 13 shows the CD2150 gate used in a **"one-shot"** configuration. The external RC network is used to generate the time constant which determines the output pulse duration.

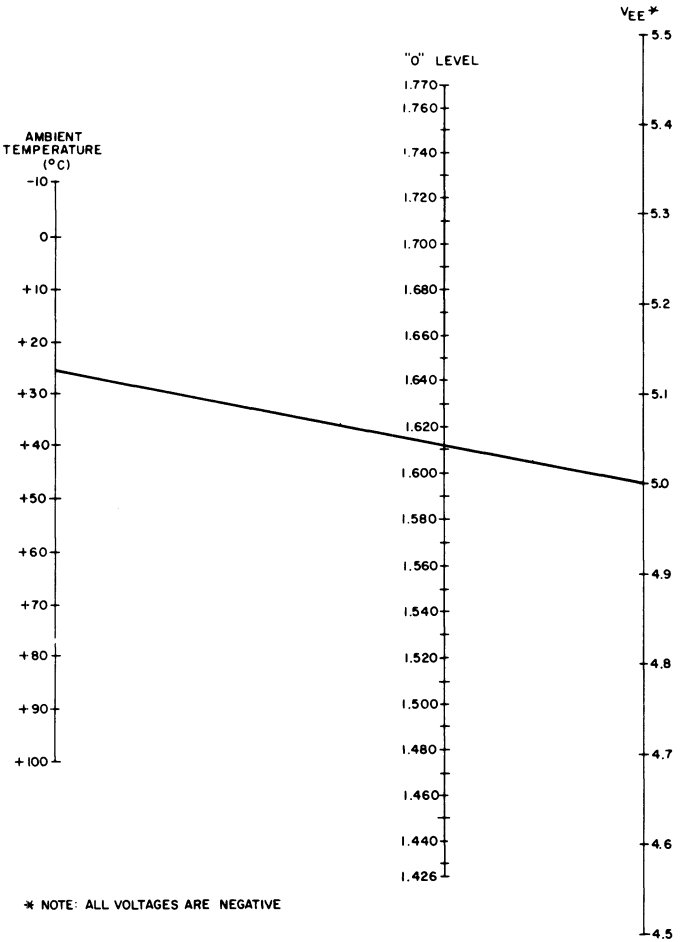


Fig. 11—Nomograph showing parameter relationships of an ECCSL gate for "0" level.

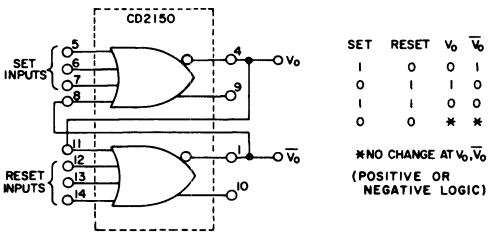


Fig. 12—Simple dc set-reset flip-flop circuit using CD2150 gate.

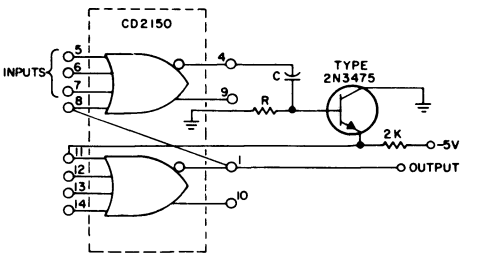


Fig. 13—One-shot circuit using CD2150 gate.

The delay through the circuit is 8 nanoseconds, and the output rise and fall times are typically 4 nanoseconds each. The tolerance of the output pulse is a function of the RC network tolerance, the input-impedance tolerance of the level shifter, and the logic-swing tolerance. The CD2151 and CD2152 gates could, of course, be used in similar fashion.

Fig. 14 shows a six-gate arrangement used to produce a **triggerable flip-flop** binary element. Although CD2150 logic circuits are shown, three CD2151 circuits with external resistors to limit power dissipation or six CD2152 circuits could be used equally well. Because this six-gate arrangement is essentially two flip-flops connected in a dual-rank combination, no capacitors or other circuit delay elements are required. The arrangement is direct-coupled throughout, and is not sensitive to the rise and fall times of logic signals. The B_1, B_2 flip-flop receives the input information when the clock voltage is high, and transfers it to the C_1, C_2 unit when the clock voltage is low. Two dc set and reset inputs are also available. As shown in Fig. 14, the information is applied to the inputs of the steering gates A_1 and A_2 and then, in turn, to the inputs of the B_1, B_2 flip-flop. However, a high-level clock input blocks the B_1, B_2 flip-flop. When the clock voltage decreases, the B_1, B_2 flip-flop switches and transfers the information to the C_1, C_2 flip-flop. The outputs of the B_1, B_2 flip-flop are also fed back to the input steering gates to make A_1 and A_2 insensitive to clock pulse duration. New information reaches the B_1, B_2 flip-flop when the clock returns to the high state.

Fig. 15 shows the effect of fan-out on the maximum clock frequency and stage delay of the circuit of Fig. 14. The rise time, fall time, and noise immunity of the triggerable flip-flop are, of course, compatible with those of the logic gate circuits.

A **shift register** can also be simply constructed by use of the basic binary element described above. Fig. 16 shows a block diagram of a five-stage shift register, and Fig. 17 shows the waveforms of successive stages operating at 67 megacycles per second with different register patterns. The waveforms shown were taken from a breadboard circuit that used conventional wiring techniques. No printed-circuit wiring or strip line was used. Printed-circuit wiring placed over a ground plane would present cleaner waveshapes. The information content of the register is shifted one stage to the right for each clock pulse applied. Setting and resetting of the individual stages is accomplished when the clock input is high.

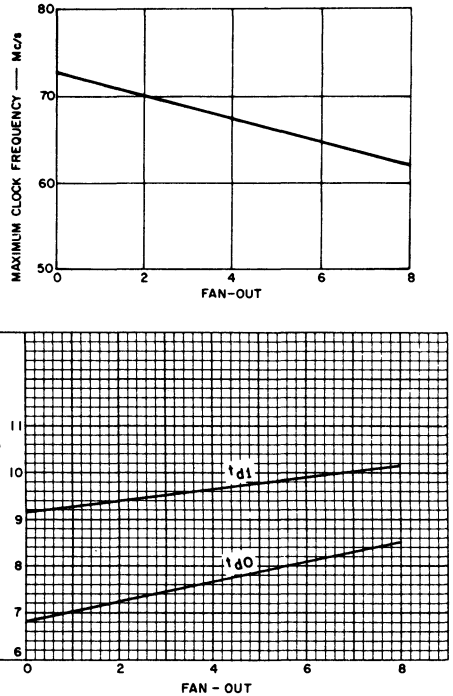


Fig. 15—Maximum clock frequency and stage delay of flip-flop circuit as a function of fan-out.

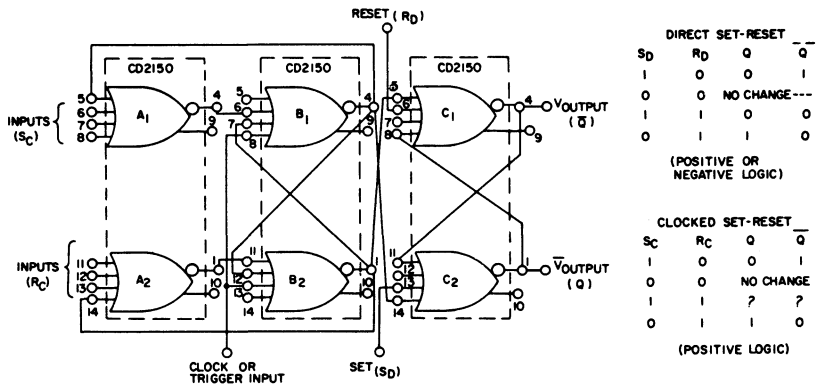


Fig. 14—Six-gate triggerable flip-flop circuit using three CD2150 gates.

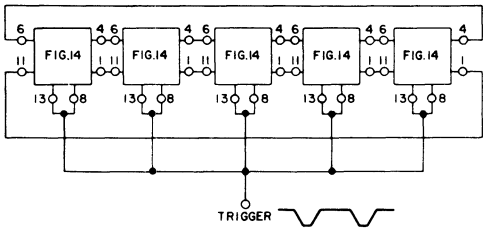


Fig. 16—Block diagram of five-stage shift-register circuit.

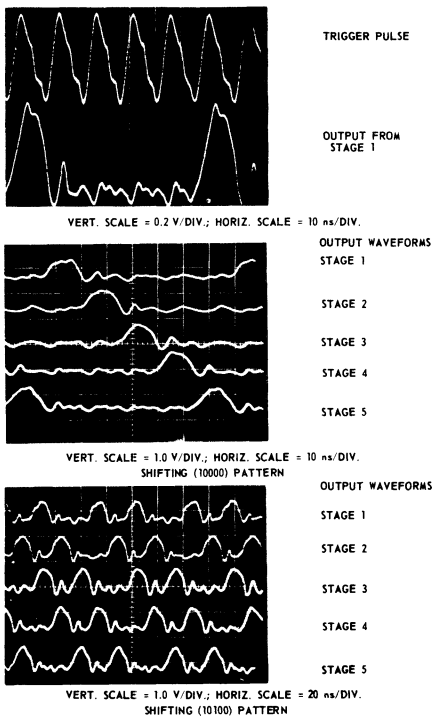


Fig. 17—Waveforms of successive stages of shift register with different register patterns; clock rate = 67 megacycles per second.

The block diagram of a five-stage **ripple counter** is shown in Fig. 18. This counter counts the input frequency down by 2^n, where n is the number of stages. The register can be set to any initial condition by use of the appropriate set-reset inputs. Again, the basic six-gate triggerable flip-flop configuration is utilized. Fig. 19 shows the waveforms of successive stages operating with a 70-megacycle-per-second clock input. The slightly higher repetition rate obtained results from the fact that the load on the clock source is considerably lighter because the clock is applied to only the first stage. Resetting of the counter is accomplished when the clock input is high. For setting or resetting of individual stages of a ripple counter, a slightly different arrangement of gate inputs and outputs is required, as shown in Fig. 20.

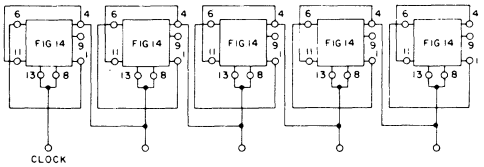


Fig. 18—Block diagram of five-stage ripple counter.

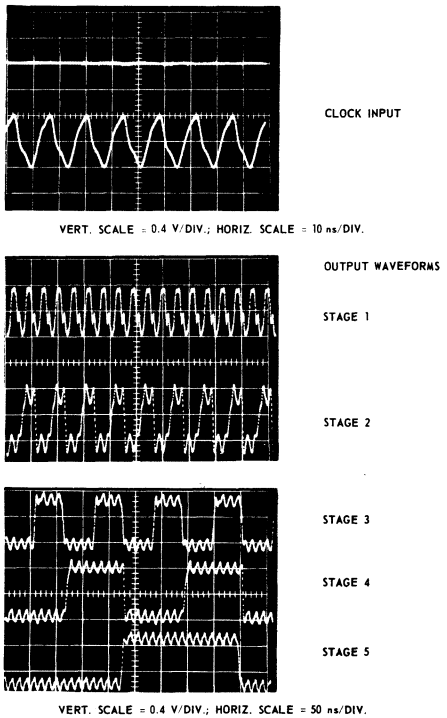


Fig. 19—Waveforms of successive stages of ripple counter with clock input of 70 megacycles per second.

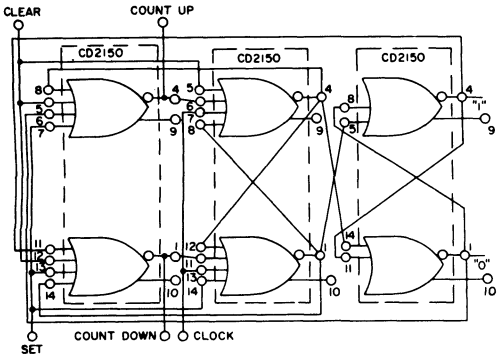


Fig. 20—Ripple counter with provision for setting and resetting of individual stages.

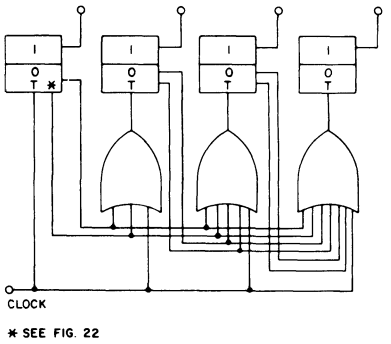


Fig. 21—Parallel-carry ripple counter.

Although the counting speed for the arrangement shown in Fig. 18 and described above is limited only by the speed of the lowest-order digit counter, the time required for the "carry" to progress through several stages may be objectionably long. As each pulse to be counted is received, the bit counters change successively, one at a time. As a result, a time lag is required for the counter to present the indication of a new total. Fig. 21 shows a **parallel-carry ripple counter** that substantially eliminates this time delay. The input pulse is sent on to the next higher order each time the corresponding counter is in the proper state. Thus, any stage that is going to change states will change when the clock pulse is present. Decoding of the register can then occur approximately one stage delay after the clock pulse is present.

The requirement for extra circuitry to accomplish the OR functions shown in Fig. 21 can be eliminated by use of the CD2152 eight-input gate for the B_1, B_2 flip-flop. This arrangement also provides higher speed because an extra gate delay between stages is eliminated. A triggerable flip-flop configuration using CD2152 eight-input gates is shown in Fig. 22. The counter hook-up for binary element is shown in Fig. 23. Use of the parallel-carry counter is demonstrated in the next two logic arrangements.

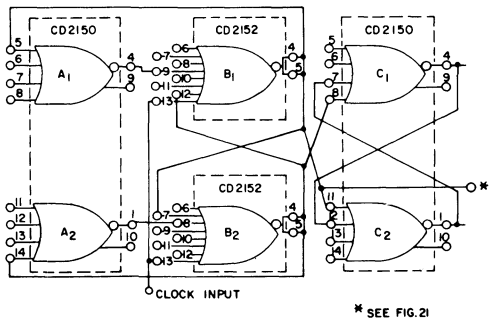


Fig. 22—Triggerable flip-flop using CD2152 eight-input gate.

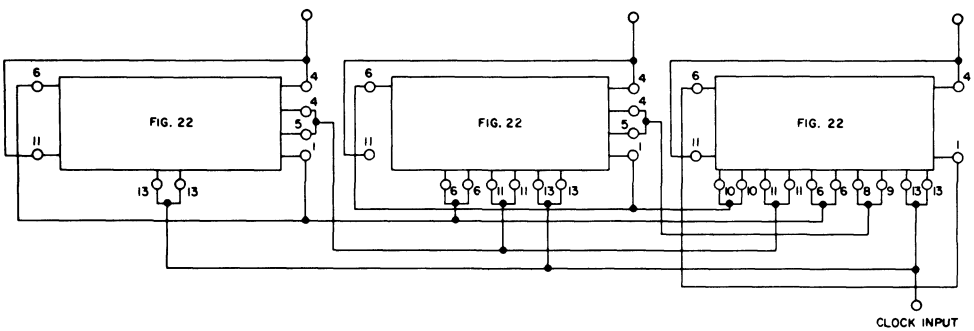


Fig. 23—Three-stage parallel-carry ripple counter using CD2150 and CD2152 logic gates.

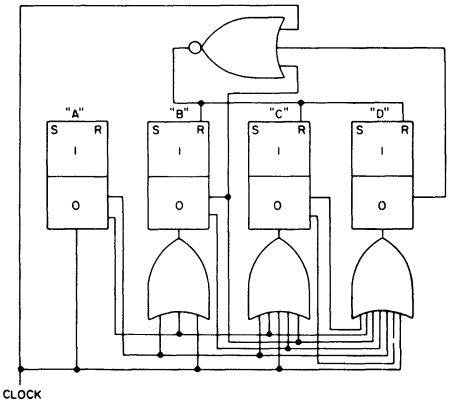
Fig. 24 shows a **four-stage binary decade counter** which incorporates the parallel-carry technique described above. The counter is capable of registering sixteen pulses, and an output may be obtained from the highest order upon the application of the sixteenth pulse. A four-order binary counter could therefore be used as a digit counter of radix sixteen. In the decimal digit counter with four binary elements shown in Fig. 24, six of the sixteen stable states are nullified by means of feedback techniques.

For the arrangement shown in Fig. 24, a feedback gate is required. Stages A through D use CD2150 or CD2151 logic gates and CD2152 gates to facilitate the parallel-carry technique. However, any combination of binary element configurations described thus far could be used. The photographs shown in Fig. 25 show the successive stages of the decade counter operated at clock rates of 5 and 25 megacycles per second. These photographs were taken from a counter which used all CD2150 dual logic gates. Therefore, an extra gate delay between stages is introduced.

A **Gray-code counter** is a counter that generates a binary pattern in which only one stage changes states at any one time. This type of counter is useful when decoding is accomplished without the use of a clock signal because no ambiguous condition exists while the counter is changing states. Therefore, no spiking appears at the decoded output. Fig. 26 shows the gate arrangement necessary to construct such a counter. Fig. 27 shows the waveforms at the outputs of the stages with clock-frequency inputs of 10, 25, and 45 megacycles per second. Although these waveforms were obtained from a counter using a CD2150 logic gate, any combination of the three gates described in this Note can be used.

A **half-adder** is a circuit capable of accepting two binary input signals and producing appropriate sum and carry output signals. The term half-adder is used because, except for the lowest order, two half-adders per order are required for the addition of two quantities. Fig. 28 shows the circuit arrangement for a half-adder function using two CD2150 circuits, and Fig. 29 shows how two half-adder functions can be realized with three of these integrated-circuit packages. The same type of logic functions can be generated by use of the CD2151 circuit with external components or the CD2152 eight-input gate.

A **full-adder** is capable of accepting three binary signals and producing both sum and carry outputs. Fig. 30 shows the logic arrangement for a full-adder using CD2150 circuits. A block diagram of a **serial full-adder** function is shown in Fig. 31. The one-bit delay needed in the "carry" feedback loop is provided by a shift-register stage comprised of six logic gates, as described previously.



COUNT SEQUENCE

A	B	C	D
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	0	0	0

ETC.

Fig. 24—Four-stage binary decade counter incorporating parallel-carry techniques.

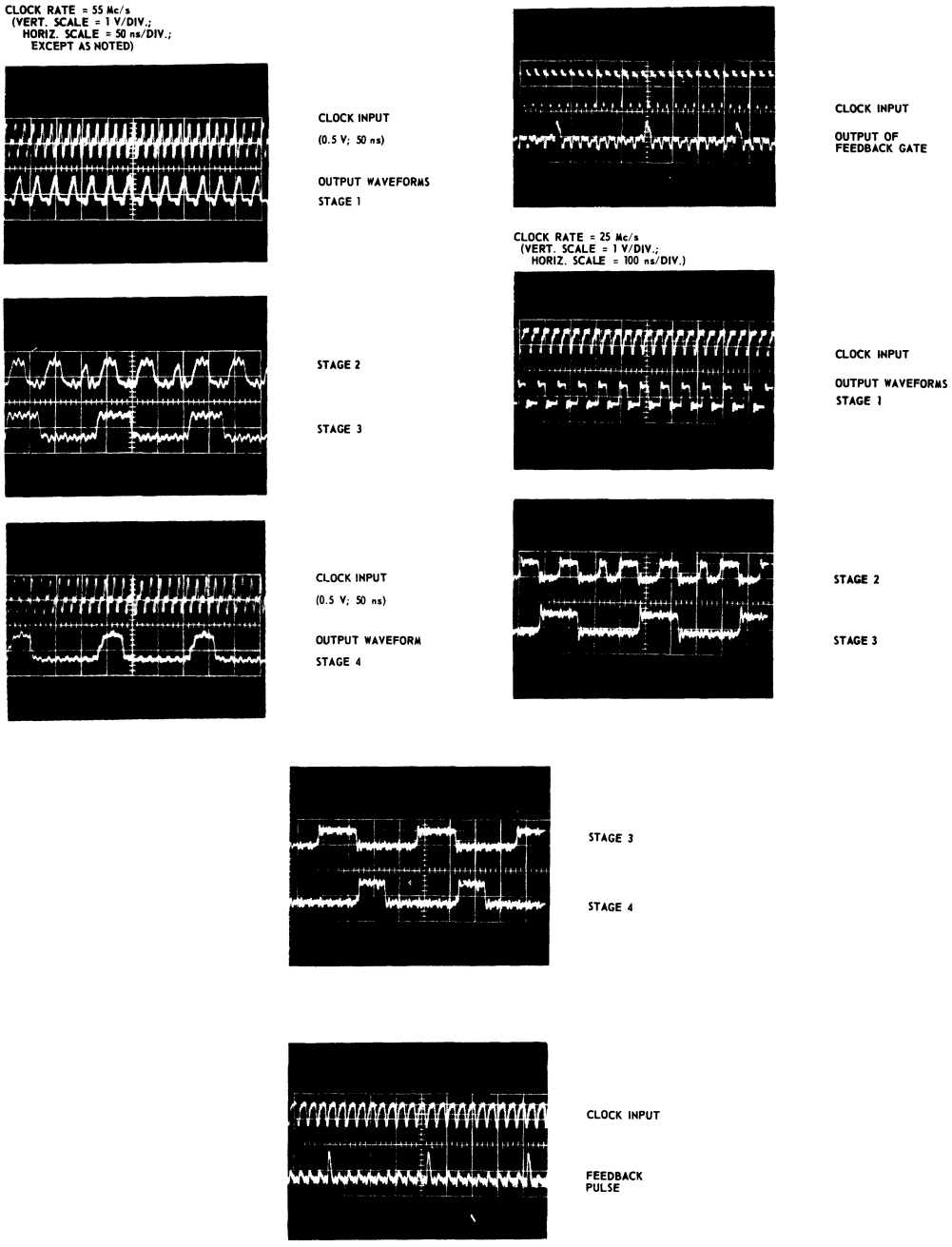


Fig. 25—Waveforms of successive stages of decade counter at clock rates of 55 and 25 megacycles per second.

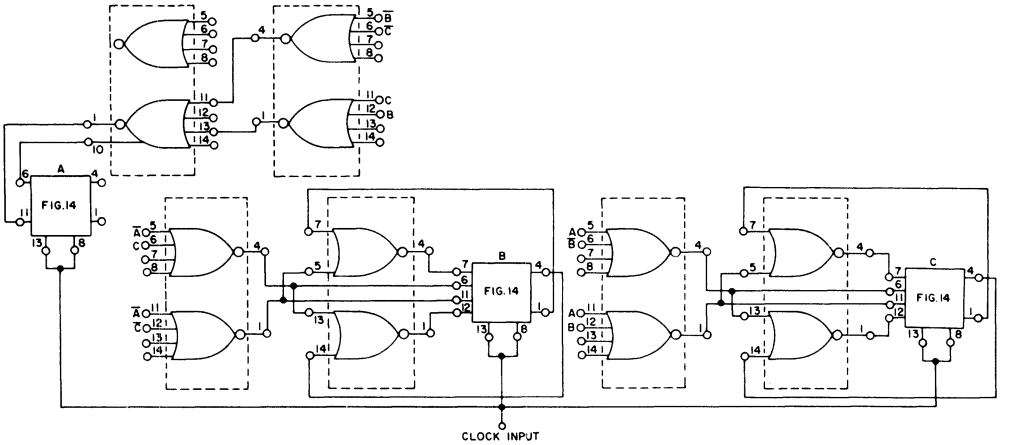
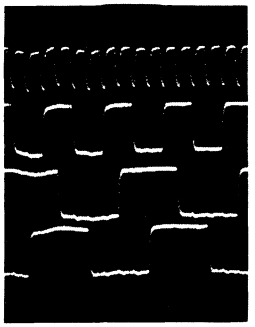
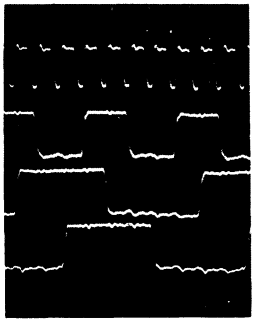


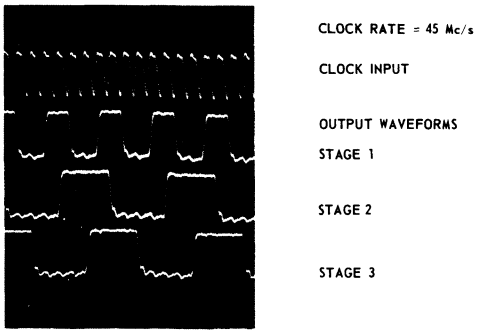
Fig. 26—Gray-code counter.



VERT. SCALE = 0.5 V/DIV.; HORIZ. SCALE = 0.2 μs/DIV.



VERT. SCALE = 0.5 V/DIV.; HORIZ. SCALE = 50 ns/DIV.



VERT. SCALE = 0.5 V/DIV.; HORIZ. SCALE = 50 ns/DIV.

Fig. 27—Waveforms at outputs of successive stages of Gray-code counter with clock input frequencies of 10, 25, and 45 megacycles per second.

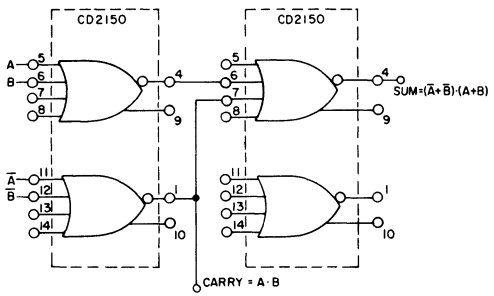


Fig. 28—Half-adder circuit using two CD2150 gates.

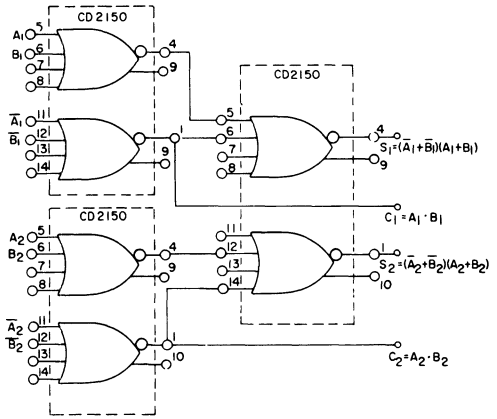


Fig. 29—Two half-adder functions using three CD2150 gates.

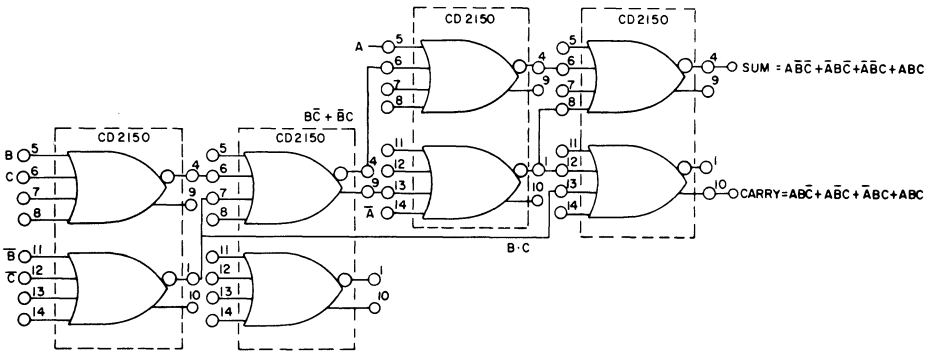


Fig. 30—Full-adder circuit using CD2150 gates.

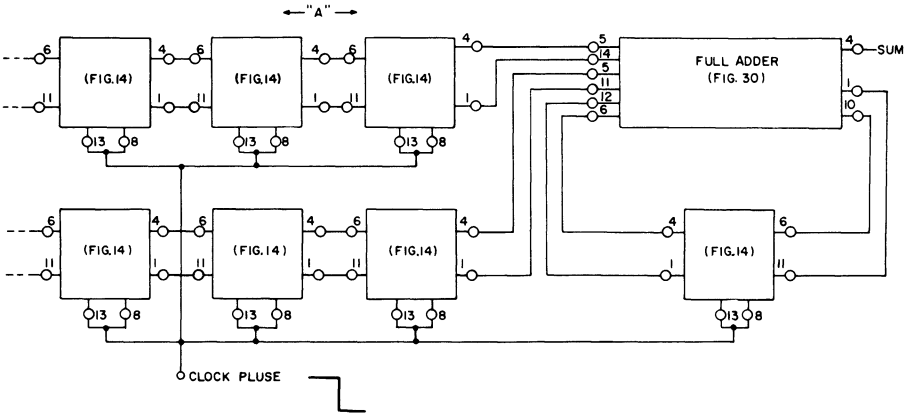
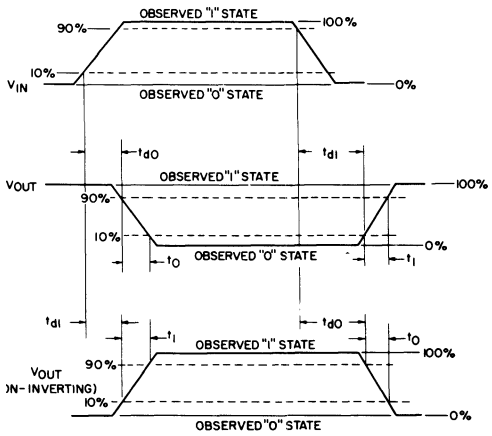


Fig. 31—Block diagram for serial full-adder circuit.

APPENDIX – Definitions

For an ECL gate that has an ideal transition region (i.e., infinite gain), the **reference threshold voltage** is defined as that voltage which causes the output voltage of the gate to change states whenever the input voltage passes through the reference value from either a positive or a negative direction.

The delay and transition times of the gate are defined by the waveforms shown below, where t_r is the **rise time,** t_f is the **fall time,** t_{dr} is the **rise delay,** and t_{df} is the **fall delay.**



Application of the RCA-CA3000 Integrated-Circuit DC Amplifier

BY
A. J. LEIDICH and M. E. MALCHOW

The RCA-CA3000 dc amplifier is a monolithic silicon integrated circuit supplied in a 10-terminal TO-5 package. This stabilized and compensated differential amplifier has push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to one MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils.

Because full gain-control capability is inherent in the CA3000, it can be used as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer, or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis. Within its specified frequency range, it is an excellent limiter, and can handle input signals up to about 80 millivolts rms before significant cross-modulation or intermodulation products are generated.

CIRCUIT DESCRIPTION

The circuit diagram and terminal connections for the CA3000 dc amplifier are shown in Fig. 1. The circuit is basically a single-stage differential amplifier (Q_2 and Q_4) with input emitter-followers (Q_1 and Q_5) and a constant-current sink (Q_3) in the emitter-coupled leg. Push-pull input and output capabilities are inherent in the differential configuration.

The use of degenerative resistors R_4 and R_5 in the emitter-coupled pair increases the linearity of the circuit and decreases its gain. The low-frequency output impedance between each output (terminals 8 and 10) and ground is essentially the value of the collector resistors R_1 and R_2 in the differential stage.

OPERATION OF THE CIRCUIT

The CA3000 is designed for operation from a wide range of supply voltages. Operation from either one or two power supplies is feasible, as illustrated by the typical biasing techniques shown in Fig. 2. However, operation from two supplies is recommended because fewer external bias networks are required and, therefore, less power is consumed.

The maximum voltage that can be applied across the circuit (positive supply voltage V_{CC} plus negative supply voltage V_{EE}) is 16 volts. The maximum voltage capability (V_{CE}) of the differential pair is limited to 8 volts. Extra care must be used to ensure that these values are not exceeded when the circuit is used to drive inductive loads.

The operating-current conditions of the differential pair are determined by the base-bias circuit and emitter resistance of the emitter-coupled constant-current sink (Q_3), as well as by the voltage between terminals 2 and 3. Each possible current condition is manifested by (1) a distinct set of dc operating characteristics with differing temperature characteristics, (2) a particular value of gain having its own temperature dependence, and (3) a particular dynamic

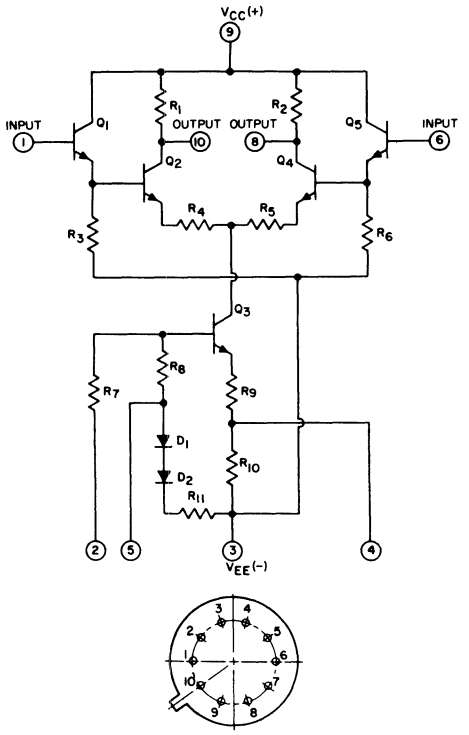


Fig. 1 - Schematic diagram and terminal connections for the CA3000 integrated-circuit dc amplifier.

output-voltage capability. For each value of voltage between terminals 2 and 3 (V_{EE} when terminal 2 is grounded), there are four possible operating modes, as described in Table I.

Table I—Operating Modes for CA3000 DC Amplifier

Mode	*Shorted Terminals*	*Condition of Diodes*	*Q_3 Emitter Resistor*
A	none	in	$R_9 + R_{10}$
B	5-3	out	$R_9 + R_{10}$
C	4-3	in	R_9
D	5-4-3	out	R_9

The operating characteristics for these modes of operation are summarized in Table II for various two-supply configurations with terminal 2 grounded and with V_{EE} values of −3 and −6 volts dc.

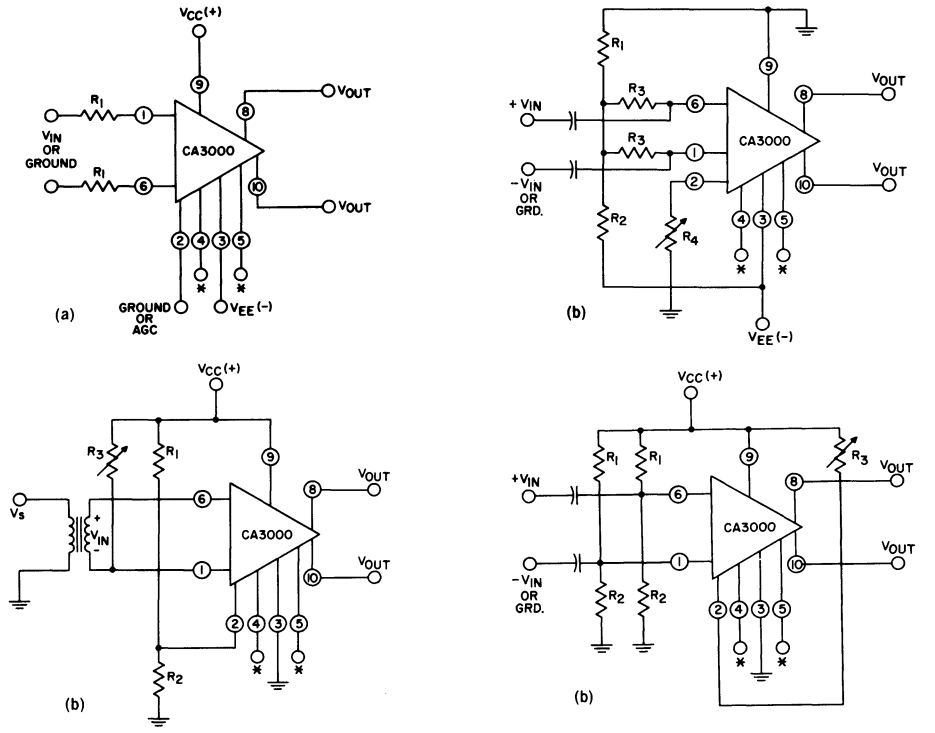
Table II shows that the positive supply voltage can be adjusted for each mode of operation and for each value of negative supply so that the nominal dc output voltage is zero. (Although the V_{CC} value required for mode C for a V_{EE} of −6 volts dc is in excess of the maximum rating, operation within ratings can be achieved with slightly negative values of output voltage.) The use of these adjusted values of positive supply provides two advantages: (1) direct interstage coupling can be effected in a single-ended configuration, and (2) negative feedback can be introduced from a single output back to the appropriate input. For low-level applications in mode D with a negative supply voltage V_{EE} of −3 volts dc and a positive supply voltage V_{CC} of 1.1 volts dc, the CA3000 has a gain of 24.4 dB, a dissipation of 6.2 milliwatts, an output capability of 2.2 volts peak-to-peak, and a dc output-voltage reference level of zero.

The information in Table II can be modified for single-supply designs by simple addition and/or subtraction of dc values. For example, the correct information for a single

Table II—Design Characteristics of CA3000 Operating Modes

DC Supply Volts Positive V_{cc}	*Negative* $-V_{EE}$	*Operating mode*	*Single-ended midband voltage gain — dB* G_{Vg}	*DC output volts (Terminal 8 or 10 to ground)* $V_{o_{dc}}$	*Positive voltage swing* $V_{o_{max}}$*	*Negative voltage swing* $V_{o_{min}}$*	*Total power dissipation — mW*
6	−6	A	31.2	+2.3	+3.7	−3.8	40
6	−6	B	27.3	+4.3	+1.7	−5.7	36
6	−6	C	34.6	−1.5 (saturated)	+7.5	0	61
6	−6	D	32.4	+1.0	+5.0	−2.4	47
3.7	−6	A	31.2	0	+3.7	−1.4	33
1.7	−6	B	27.3	0	+1.7	−1.4	25
10.6 (over rating)	−6	C	34.6	0	+10.6	−1.5	83
5.0	−6	D	32.4	0	+5.0	−1.5	43
3	−3	A	27.5	+1.2	+1.8	−2.6	8.8
3	−3	B	16.6	+2.6	+0.4	−4.1	7.4
3	−3	C	32.6	−1.5 (saturated)	+4.5	0	14
3	−3	D	24.4	+1.9	+1.1	−3.3	8.5
1.8	−3	A	27.5	0	+1.8	−1.5	7.2
0.4	−3	B	16.6	0	+0.4	−1.5	8.4
5.3	−3	C	32.6	0	+5.3	−1.5	19
1.1	−3	D	24.4	0	+1.1	−2.6	6.2

* $V_{o_{max}}$ and $V_{o_{min}}$ are the ac swing extremities above and below $V_{o_{dc}}$.



* Connection of terminals 4 and 5 depends on mode of operation.

Fig.2 - Typical biasing arrangements for the CA3000 for operation from (a) two separate voltage supplies, or (b) a single voltage supply.

supply of 12 volts dc for operating mode A can be obtained from the conditions shown in the table for mode A for $V_{CC} = 6$ Vdc and $V_{EE} = -6$ Vdc by the addition of 6 volts to the values shown for V_{CC}, V_{EE}, Vo_{dc}, Vo_{max}, and Vo_{min}. (It should be noted that the required voltage levels at the input terminals 1 and 6 and at terminal 2 are also 6 volts higher.

As mentioned previously, the four operating modes exhibit different temperature characteristics. Fig. 3 shows theoretical curves of dc output voltage as a function of

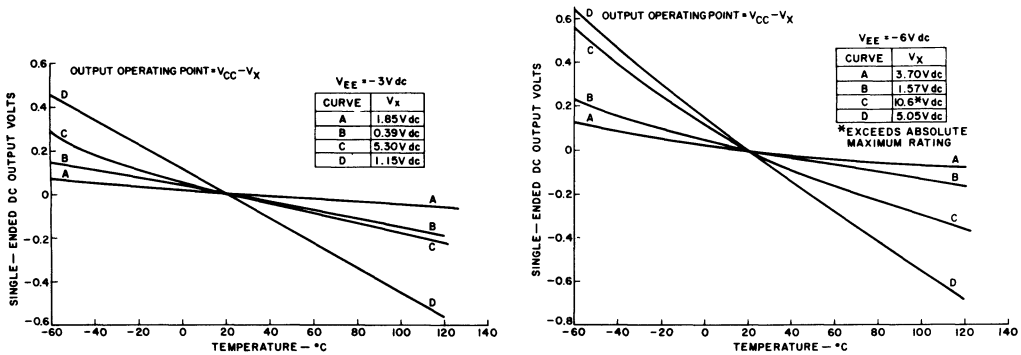


Fig.3 - Theoretical curves of dc output voltage as a function of temperature for negative-supply voltages of -3 and -6 volts dc (calculated for β = 35 at 20°C).

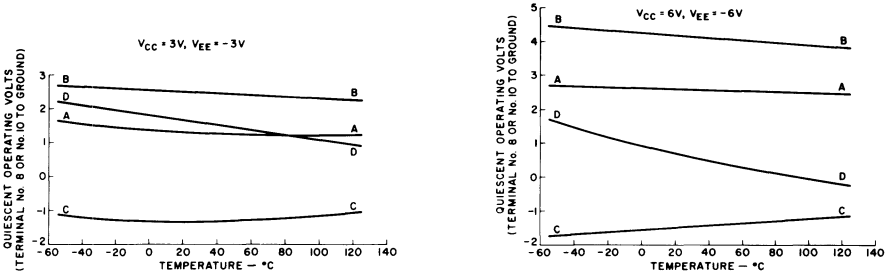


Fig.4 - Measured curves of dc output voltage as a function of temperature for negative-supply voltages of -3 and -6 volts dc.

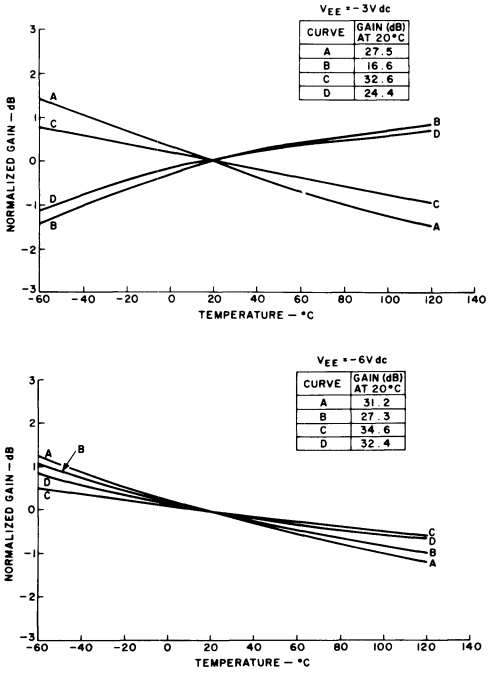


Fig.5 - Theoretical curves of gain as a function of temperature for negative-supply voltages of -3 and -6 volts dc (calculated for β = 35 at 20°C).

temperature for each operating mode for negative supply voltages V_{EE} of −3 and −6 volts dc. The experimental curves shown in Fig. 4 are in excellent agreement with the theoretical curves except in the case of mode C. In this mode, the differential-pair transistors Q_2 and Q_4 were driven into saturation as a result of the use of symmetrical supplies ($V_{CC} = V_{EE}$) for the experimental data. The discrepancy could be corrected by use of somewhat higher values of positive supply voltage.

Fig. 5 shows theoretical curves of gain as a function of temperature for the four operating modes with V_{EE} values of −3 and −6 volts dc. With the diodes in (modes A and C), the gain decreases for both values of V_{EE}. With the diodes out (modes B and D), on the other hand, the gain increases with temperature for a negative supply of −3 volts dc, but decreases with temperature for a negative supply of −6 volts dc. With the diodes out, there is a value of negative supply (approximately −4.5 volts dc) for which the gain is independent of temperature. Fig. 6 shows measured values of single-ended and push-pull gain for mode A with symmetrical power supplies of ±6 volts dc. (This configuration is used in the remaining discussion because it provides the maximum sinusoidal output capability, as shown in Table II, and because of the convenience of ±6-volt dc supplies.)

The typical single-ended voltage-gain/frequency-response curve of the CA3000 for dc supplies of ±6 volts in operating mode A is shown in Fig. 7, together with the test circuit used for voltage-gain measurements. The Bode responses of the CA3000 are virtually independent of source impedance up to 10,000 ohms because of the emitter-follower inputs. The curves in Fig. 8 show that gain and bandwidth are virtually independent of temperature for operation in mode A with ±6-volt dc supplies.

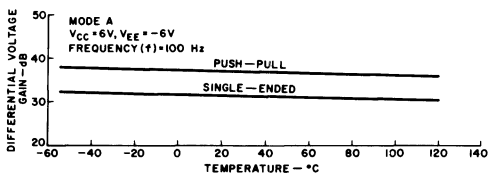


Fig.6 - Measured values of single-ended and push-pull gain for mode A operation with symmetrical power supplies of ±6 volts dc.

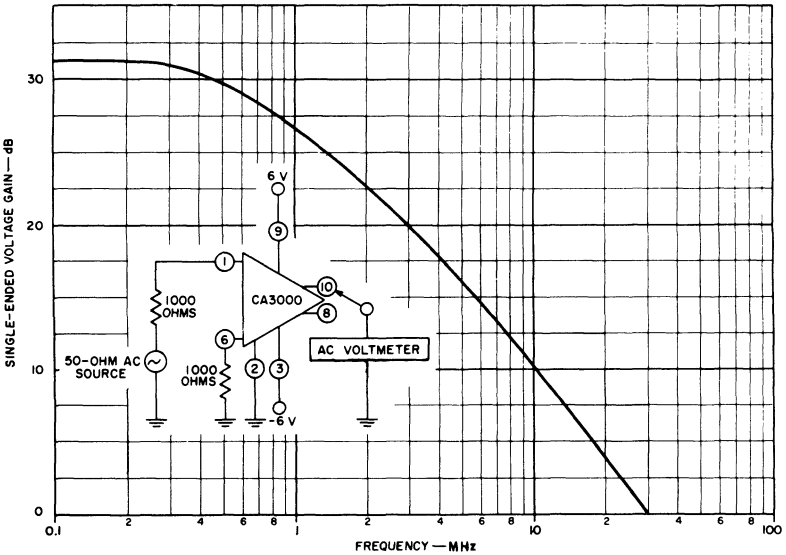


Fig.7 - Single-ended voltage gain of CA3000 as a function of frequency in test circuit shown.

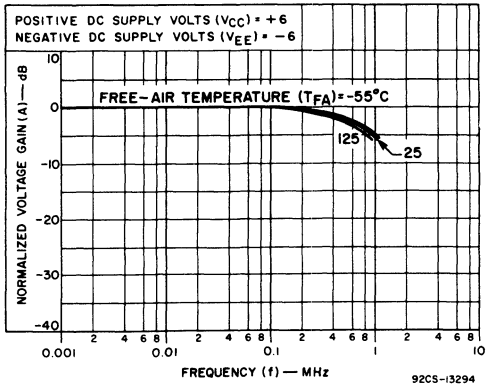
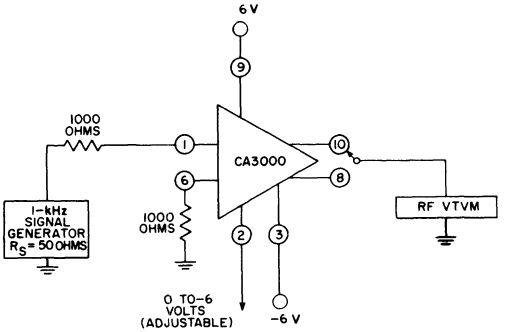


Fig.8 - Normalized gain-frequency curves for CA3000 at three different temperatures.

Fig. 9 shows agc characteristics for the CA3000 for an input frequency of 1 kHz, together with the agc voltage-gain test circuit. When the agc voltage at terminal 2 is varied from 0 to −6 volts, the amplifier gain can be varied over a range of 90 dB.

Fig. 10 shows the test circuit used to measure common-mode rejection, together with curves of common-mode rejection as a function of frequency and temperature. Typical rejection is 97 dB at a frequency of 1 kHz. Fig. 11 shows the test circuit used to measure the dc unbalance of the amplifier (referred to the input), together with a curve of the input offset voltage as a function of temperature. Typical input offset voltage (with an assumed push-pull differential gain of 37 dB) is 1.5 millivolts. Fig. 12 shows curves of input bias current, input impedance, and dynamic output voltage as functions of temperature.



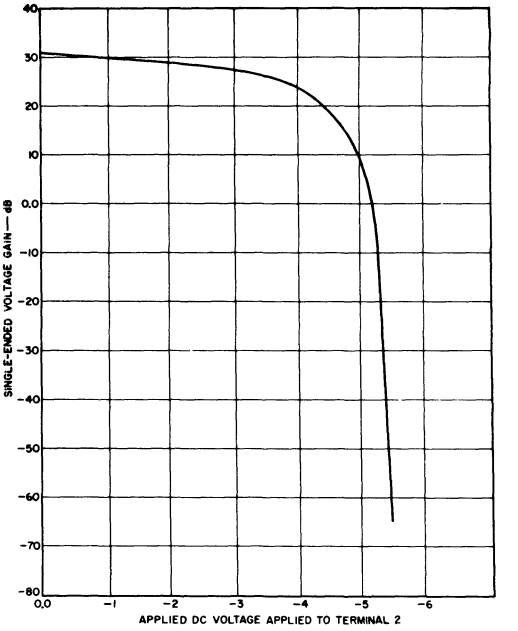
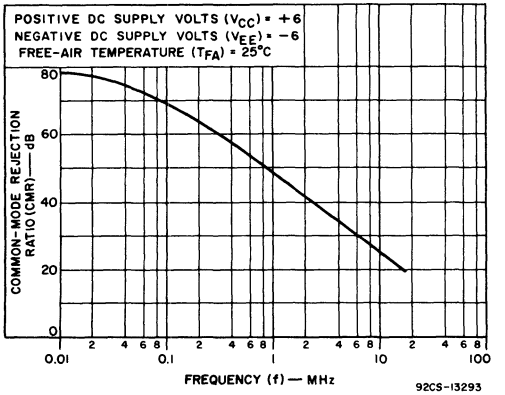
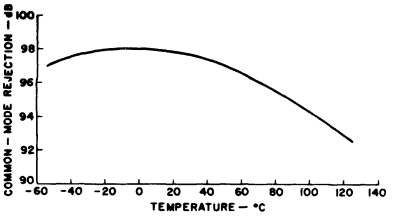


Fig.9 - AGC characteristics of CA3000 in test circuit shown at frequency of 1 kHz.





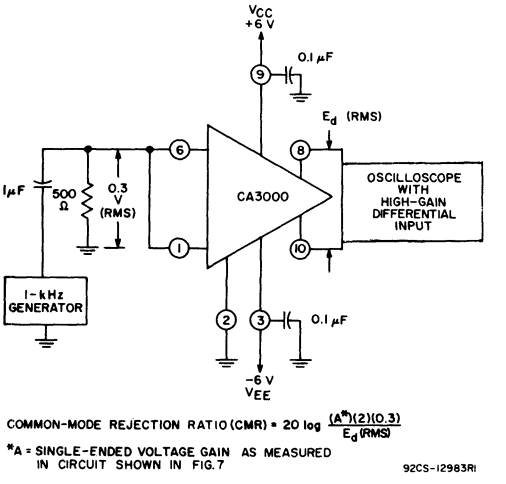


Fig.10 - Common-mode rejection of CA3000 as a function of frequency and of temperature in test circuit shown.

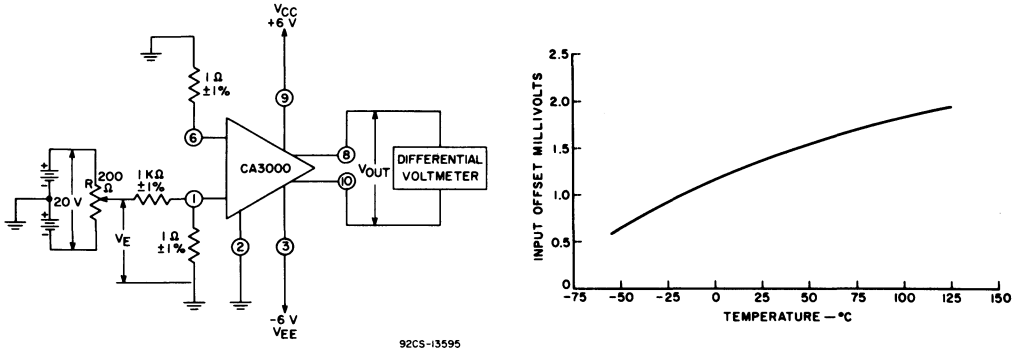


Fig. 11 - Input offset voltage of CA3000 as a function of temperature in test circuit shown.

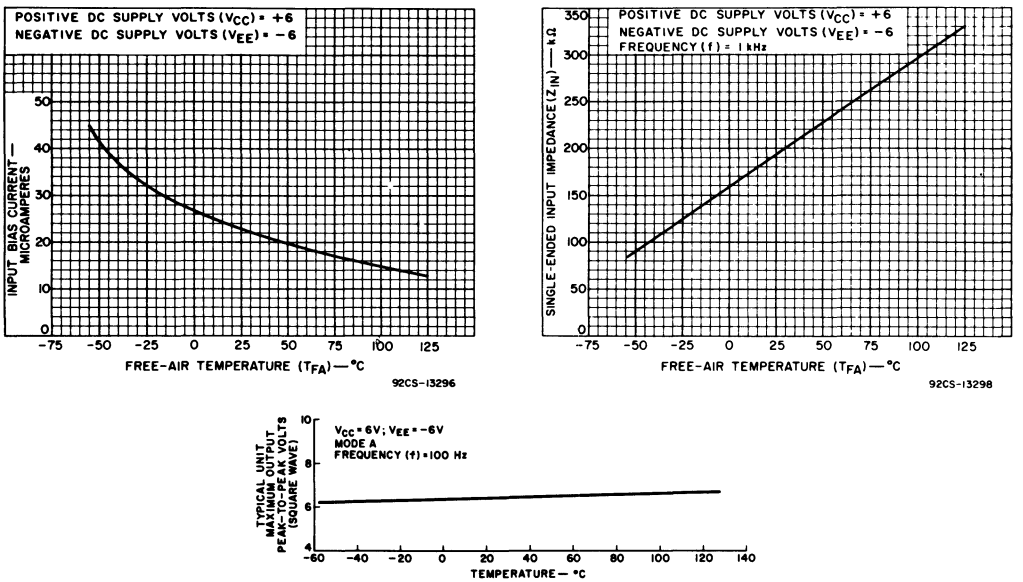


Fig. 12 - Input bias current, input impedance, and dynamic output voltage of CA3000 as functions of temperature.

APPLICATIONS

Crystal Oscillator—The CA3000 can be used as a crystal oscillator at frequencies up to 1 MHz by connection of a crystal between terminals 8 and 1 and use of two external resistors, as shown in Fig. 13(a). The output is taken from the collector that is not connected to the crystal (in this case, terminal 10). If a variable-feedback ratio network is used, as shown in Fig. 13(b), the feedback may be adjusted to provide a sinusoidal oscillation. Output waveforms for both circuits are also shown. The frequency in each circuit is 455 kHz, as determined by the crystal. The range of these crystal oscillators can be extended to frequencies of 10 MHz or more by use of collector tuning.

Modulated Oscillator—If a low-frequency signal is connected to terminal 2, as shown in Fig. 14, the CA3000 can function as an oscillator and produce an amplitude-modulating signal. The waveform in Fig. 14 shows the modulated signal output produced by the modulated oscillator circuit when a 1-kHz signal is introduced at terminal 2 and a high-pass filter is used as the output.

Low-Frequency Mixer—In a configuration similar to that used in modulated-oscillator applications, the CA3000 amplifier may be used as a mixer by connection of a carrier signal at the base input of either differential-pair transistor (terminal 1 or 6) and connection of a modulating signal to terminal 2 or 5.

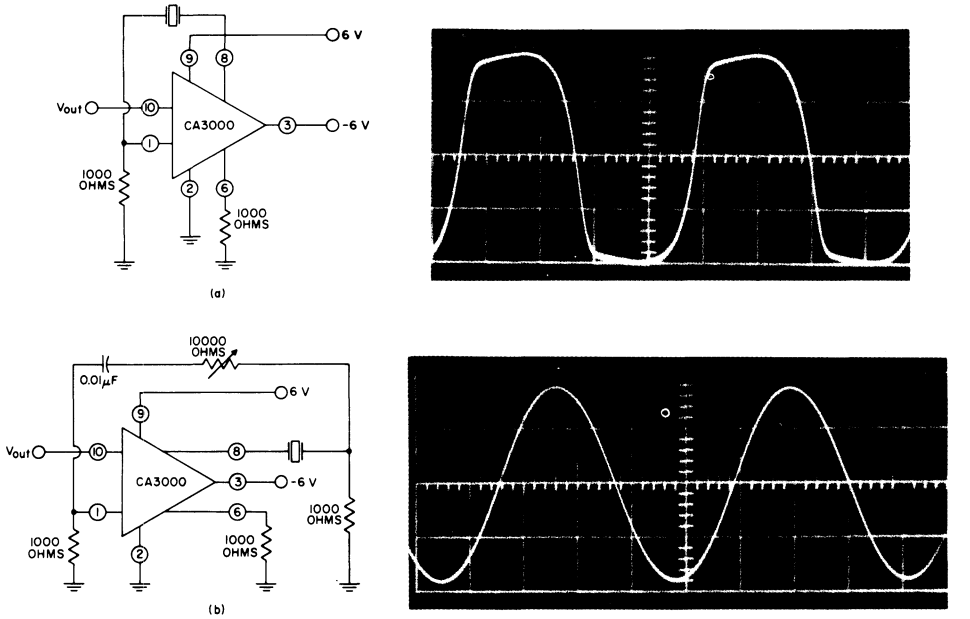


Fig. 13 - Schematic diagrams and output waveforms of (a) crystal oscillator and (b) crystal oscillator with variable feedback.

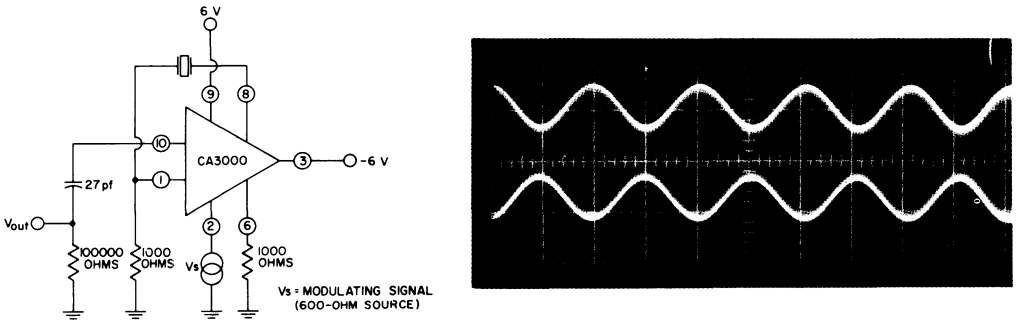


Fig. 14 - Schematic diagram and output waveform of CA3000 modulated oscillator.

Cascaded RC-Coupled Feedback Amplifier—The two-stage feedback cascade amplifier shown in Fig. 15 produces a *typical open-loop* midband gain of 63 dB. This circuit uses a 100-picofarad capacitor C_1 to shunt the differential outputs of the first stage. This capacitor staggers the high-frequency roll-offs of the amplifier and thus improves stability.

The gain-frequency characteristic of the feedback amplifier is shown in Fig. 16(a) for a feedback resistance R_f approaching infinity. The low-end roll-off of the amplifier is determined by the interstage coupling. Because agc may be applied to the first stage, the amplifier of Fig. 15 may be used in high-gain video-agc applications under open-loop conditions. If feedback is used to control the gain, agc may still be applied successfully.

Fig. 16(b) shows the agc characteristics for the two-stage amplifier under open-loop and two closed-loop conditions at a frequency of 1 kHz. As shown in Fig. 16(a), the open-loop bandpass is 18 Hz to 135 kHz; under closed-loop conditions, the bandpass is 1.3 Hz to 2 MHz for 40-dB gain and 0.13 Hz to 6.6 MHz for 20-dB gain. The negative feedback thus improves low-frequency performance suffi-

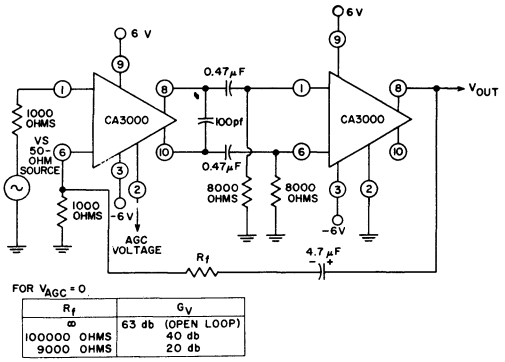
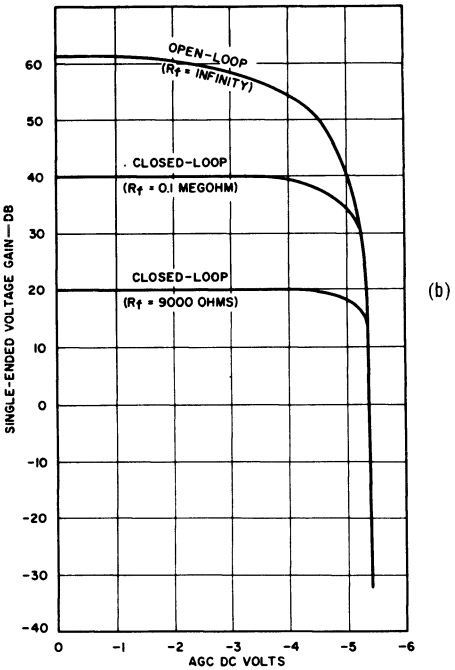


Fig.15 - Cascaded RC-coupled feedback amplifier using two CA3000 circuits.

ciently so that the use of small coupling capacitors C_2 and C_3 involves little sacrifice in low-frequency response. If three or more CA3000 amplifiers are cascaded, the low-frequency roll-offs must be staggered as well as those at the high end to prevent oscillation. A three-stage cascade has a midband gain of approximately 94 dB.

Narrow-Band Tuned Amplifier—Because of its high input and output impedances, the CA3000 is suitable for use in parallel tuned-input and tuned-output applications. There is comparative freedom in selection of circuit Q because the differential amplifier exhibits inherently low feedback qualities provided the following conditions are met: (1) the collector of the driven transistor is returned to ac ground and the output is taken from the non-driven side, and (2) the input is adequately shielded from the output by a ground plane.

The CA3000 has an output capacitance of approximately 9 picofarads at a frequency of 10 MHz. This capacitance



(b)

(a)

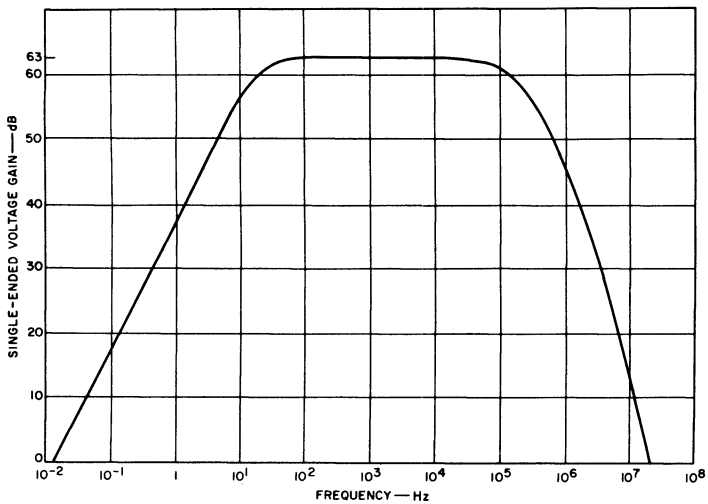
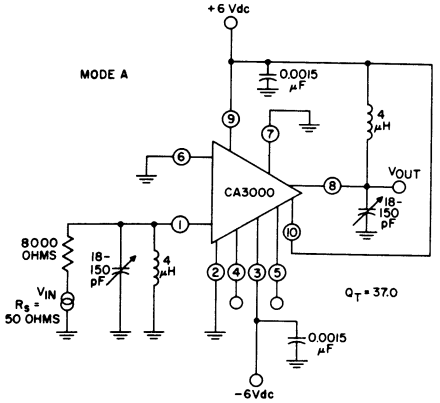


Fig.16 - (a) Gain-frequency and (b) agc characteristics of feedback amplifier shown in Fig.15.

will resonate a 28 microhenry coil at this frequency and give a minimum Q of 4.55 when the collector load resistor is the only significant load. With this low Q, stagger tuning may be unnecessary for many broad-band applications.

Fig. 17 shows the CA3000 in a narrow-band, tuned-input, tuned-output configuration for operation at 10 MHz with an input Q of 26 and an output Q of 25; the response curve of the amplifier is also shown. The 10-MHz voltage gain is 29.6 dB, and the total effective circuit Q is 37. There is very little feedback skew in the response curve. The CA3000 can be used in tuned-amplifier applications at frequencies up to the 30-MHz range.



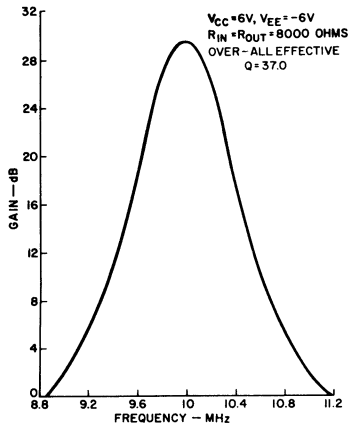


Fig. 17 - Schematic diagram and response curve for 10-MHz tuned-input, tuned-output, narrow-band amplifier using CA3000.

Schmitt Trigger—The CA3000 can be operated as an accurate, predictable Schmitt trigger provided saturation of either side of the differential amplifier is prevented (hysteresis is less predictable if saturation occurs). Non-saturating operation is accomplished by operation in mode B

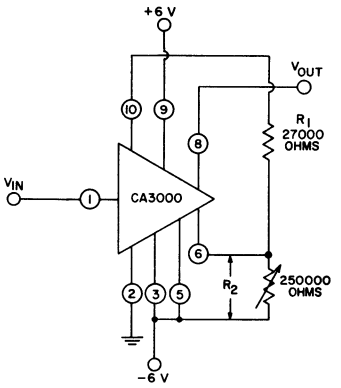


Fig. 18 - Schematic diagram for Schmitt trigger using CA3000.

(terminals 3 and 5 shorted together) in the configuration shown in Fig. 18. Large values are required for external resistors R_1 and R_2 because they receive the total collector current from terminal 10. Because of the high impedances, resistor R_2 is actually a parallel combination of the input impedance (approximately 0.1 megohm) of the CA3000 and the 0.25-megohm external resistor. The Schmitt-trigger design equations (for $\alpha = 1$) are summarized below. In these equations, Q_2 and Q_4 are the differential-pair transistors, Q_1 and Q_5 are the emitter-follower transistors, and Q_3 is the constant-current sink.

STATE I: Q_2 off, Q_4 conducting (not saturated)

$$V_{s_I} = \frac{V_{CC}(R_2) - V_{EE}(R_1 + 8000)}{R_1 + R_2 + 8000}$$

where 8000 ohms is the output impedance of Q_4 (obtained from the published data). For $R_1 =$ 27000 ohms and $V_{CC} = V_{EE} = 6$ Vdc,

$$V_{s_I} = \frac{6V(R_2) - 6V(35000)}{R_2 + 35000} \quad (A)$$

$$R_2 = (R_1 + 8000)\frac{V_{EE} + V_{s_I}}{V_{CC} - V_{s_I}}$$

$$R_2 = (35000)\frac{6V + V_{s_I}}{6V - V_{s_I}} \quad (B)$$

$$V_{s_I} = V_{CC} - I_E(8000)$$

where I_E = collector current of transistor Q_3 ≈0.48 milliampere in operating mode B with $V_{EE} = -6$ volts dc.

$$V_{s_I} = 2.14\ V \quad (C)$$

$V_{F_I} \equiv$ Firing voltage for transition from state I to state II

$$V_{F_I} = V_{s_I} - 0.053 - 100\,I_E \text{ at } 25°C$$

$$V_{F_I} = V_{s_I} - 0.101\ V \text{ at } 25°C \quad (D)$$

STATE II: Q_2 conducting (not saturated), Q_4 off

$$V_{s_{II}} = V_{CC}$$

$$V_{s_{II}} = 6\ V \quad (A)$$

$$V_{s_{II}} = \frac{(V_{CC} - I_E\,8000)\,R_2 - V_{EE}(R_1 + 8000)}{R_1 + R_2 + 8000}$$

$$V_{e_{II}} = \frac{2.14\ V\ (R_2) - 6\ V\ (35000)}{R_2 + 35000} \quad (B)$$

$V_{F_{II}} \equiv$ Firing voltage for transition from state II back to state I

$V_{F_{II}} = V_{e_{II}} + 0.053 + 100\ I_R$ at 25°C

$V_{F_{II}} = V_{e_{II}} + 0.101$ V at 25°C (C)

HYSTERESIS VOLTAGE

$V_{HYS} = V_{F_I} - V_{F_{II}}$

$$= \frac{3.86\ V\ (R_2)}{R_2 + 35000} - 0.202\ V \text{ at } 25°C$$

From the calculations for state I, it is evident that either V_{e_I} or R_2 must be a known design value. Because R_2 is a composite value, V_{e_I} is the more reasonable choice. The ability of these equations to predict the Schmitt-trigger performance is evidenced by the comparison of calculated and experimental data in Table III.

Table III — Comparison of Calculated and Experimental Data for Schmitt Trigger

Condition	*Parameter*	*Calculated*	*Experimental*
1) $V_{e_I} = -2V$	V_{F_I}	−2.1V	−2.2V
	$V_{F_{II}}$	−3.19V	−3.2V
	V_{HYS}	+1.09V	+1.0V
2) $V_{e_I} = -1V$	V_{F_I}	−1.10V	−1.0V
	$V_{F_{II}}$	−2.51V	−2.45V
	V_{HYS}	+1.41V	+1.4V
3) $V_{e_I} = 0$	V_{F_I}	−0.101V	0
	$V_{F_{II}}$	−1.83V	−1.8V
	V_{HYS}	+1.73V	+1.8V
4) $V_{e_I} = +1V$	V_{F_I}	+0.9V	+1.0V
	$V_{F_{II}}$	−1.15V	−1.0V
	V_{HYS}	+2.1V	+2.0V
5) $V_{e_I} = +2V$	V_{F_I}	+1.9V	+2.0V
	$V_{F_{II}}$	−0.472V	−0.5V
	V_{HYS}	+2.43V	+2.4V

Application of the RCA-CA3002 Integrated-Circuit IF Amplifier

BY
G. E. THERIAULT AND R. G. TIPPING

The RCA-CA3002 integrated-circuit if amplifier is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

The CA3002 features all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from −55 to 125°C, and contains a built-in temperature-compensating network for stabilization of gain and dc operating point over this operating-temperature range. It is supplied in a 10-terminal TO-5 low-silhouette package.

Because the CA3002 is a balanced differential amplifier fed from a constant-current source, it makes an excellent controlled-gain amplifier. The gain-control function may be extended to include video gating, squelching, and blanking applications. Envelope detection can be achieved by suitable biasing of the emitter-base diode of the output emitter-follower transistor. Product detection can be obtained by re-insertion of the carrier at the base of the constant-current-source transistor. Various trigger and waveform-generating circuits can also be achieved by the addition of suitable external components.

CIRCUIT DESCRIPTION AND OPERATING MODES

Fig. 1 shows the circuit diagram and terminal connections for the CA3002 integrated circuit. The circuit is basically a single-stage differential amplifier (Q_2 and Q_4) with input emitter-followers (Q_1 and Q_5), a constant-current sink (Q_3) in the emitter-coupled leg, and an output emitter-follower (Q_6). A single-ended input is connected to terminal 10 or a push-pull input to terminals 10 and 5. A single-ended output is direct-coupled at terminal 8 or capacitance-coupled at terminal 6. Terminals 5 and 10 must be provided with dc returns to ground through equal external base resistors. The emitters of the differential pair (Q_2 and Q_4) are connected through degenerative resistors (R_3 and R_4) to the transistor current source (Q_3). The use of these resistors improves the linearity of the transfer characteristic and increases the signal-handling capability.

Transistor Q_1 provides a high input impedance for the if amplifier. Transistor Q_5 preserves the circuit symmetry, and also partially bypasses the base of Q_4. Additional bypassing can be obtained by connection of an external capacitor between terminal 5 and ground. The emitter-follower transistor Q_6 provides a direct-coupled output impedance of less than 100 ohms.

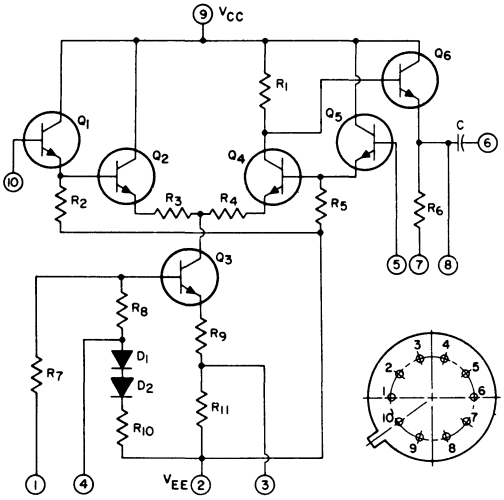


Fig. 1—Schematic diagram and terminal connections for the CA3002 integrated-circuit if amplifier.

When voltage supplies are connected to the CA3002, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 2 (internally connected to the substrate and case). The CA3002 may be operated from various supplies and at various levels. Operation from either single or dual power supplies is feasible. When two supplies are used, they may be either symmetrical or non-symmetrical. When both positive and negative voltage supplies are used, external components can be minimized, as shown in Fig. 2(a). For single-supply applications, a resistor divider and a bypass capacitor must be added externally, as shown in Fig. 2(b). The current through R_2 and R_3 should be greater than one milliampere. Except in applications that use inductive drive, equal external base resistors must be added at terminals 5 and 10 to provide base-current returns. Terminal 7 can be connected to ground, or to the negative supply if a larger negative-going voltage swing is desired at any operating point.

For either single or dual supplies, the operating current in transistor Q_3 is determined by the bias voltage between terminals 1 and 2. The more negative point of this bias voltage must be connected to terminal 2. For dual-supply systems, terminal 1 is usually referenced to ground.

For any given bias voltage (V_{EE} when terminal 1 is grounded), four operating modes are possible, as described in Table I. In general, each mode is characterized by (1) a distinct dc operating point with a characteristic temperature dependence, and (2) a particular value of gain that has a distinct temperature dependence.

When the diodes are utilized in the bias circuit (modes A and C), the current is essentially dependent on the temperature coefficient of the diffused emitter resistors R_9 and R_{11}, and has a tendency to decrease with increasing temperature at a rate independent of the negative supply voltage. The

Table I—Identification of CA3002 Operating Modes

Operating Mode	*Shorted Terminals*	*Condition of Diodes*	*Q_3 Emitter Resistor*
A	none	in	$R_9 + R_{11}$
B	4-2	out	$R_9 + R_{11}$
C	3-2	in	R_9
D	4-3-2	out	R_9

temperature coefficient of the diffused collector resistor R_1 is the same as that of the emitter resistor, and a constant collector-voltage operating point results at the collector of transistor Q_1. However, the operating point at output terminal 8 is modified by the base-emitter voltage drop of transistor Q_6 and its temperature dependence. Typical variation of the output operating point with temperature is shown in Fig. 3 for the four operating modes for V_{EE} supplies of -3 and -6 volts. The voltage between terminals 8 and 9 is denoted by V_X. In mode B (with the diodes out of the bias circuit), it should be noted that the output operating point is constant with temperature because the change in the collector operating point is cancelled by the change in the base-emitter voltage drop (V_{BE}).

When the diodes are out of the bias circuit, the current-temperature curves become dependent on the negative supply voltage. Therefore, the value of V_{EE} can be adjusted so that the transconductance decreases, increases, or remains constant with temperature. As shown in Fig. 4, the gain increases with temperature for a -3-volt V_{EE} supply, but decreases with increasing temperature for a -6-volt V_{EE} supply. At some intermediate value of V_{EE} (approximately -4.5 volts), the gain should be constant as a function of temperature. In any case, however, a constant ac gain with temperature is accompanied by a change in the collector operating point of transistor Q_4.

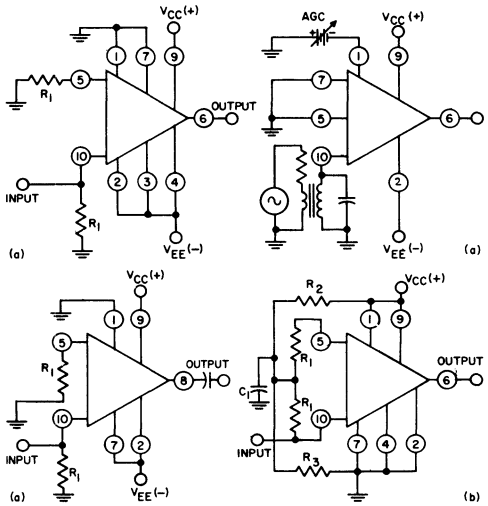


Fig. 2—Circuit configurations for the CA3002 with (a) dual voltage supplies, and (b) a single supply.

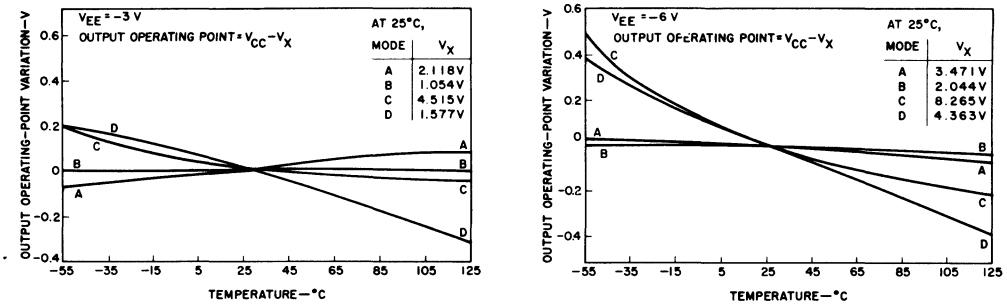


Fig. 3—Output operating-point variation of the CA3002 (normalized to the 25°C operating point) as a function of temperature with V_{EE} supply voltages of −3 and −6 volts.

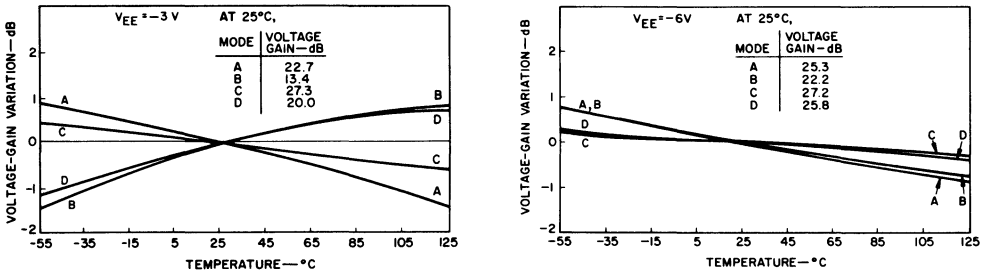


Fig. 4—Voltage-gain variation of the CA3002 (normalized to the 25°C voltage gain) as a function of temperature with V_{EE} supply voltages of −3 and −6 volts.

Table II lists typical design performance characteristics for the four operating modes of the CA3002. By use of the data in this table and in Figs. 3 and 4, it is possible to select the proper operating mode to provide the most transconductance per milliwatt of dissipation, the specified output-swing capability, and the desired temperature performance for a particular design requirement.

In operating mode C, a valid non-saturated operating point may be obtained by use of non-symmetrical voltage supplies. For example, when V_{EE} is −3 volts, the operating point will not be in saturation if a positive supply voltage of 4.5 volts or more is used (as indicated by Fig. 3). Resistor R_6 may then be returned to the negative supply instead of to ground to ensure the desired negative swings.

Table II—Typical Design Performance Characteristics for the Four Operating Modes of the CA3002 (Terminals 7 and 1 are grounded; temperature = 25°C)

Mode	*± Supply Volts*	*Output Operating Point (Volts) at Terminal 8 to Ground*	*Voltage Gain (dB) at 1 MHz*	*+ Supply Current (mA)*	*− Supply Current (mA)*	*Power Dissipation (mW)*
A	6	2.6	26.4	5.0	4.2	55.2
B	6	3.8	22.5	4.7	3.7	50.4
C	6	0		(transistor Q_4 saturated, transistor Q_6 cutoff)		
D	6	1.8	25.4	5.1	4.9	60
A	4.5	2.0	24.0	3.6	3.0	29.7
B	4.5	3.0	19.8	3.4	2.6	27.0
C	4.5	0		(Q_4 saturated, Q_6 cutoff)		
D	4.5	1.8	24.5	3.7	3.3	31.5
A	3	1.1	22	2.3	2.0	12.9
B	3	2.0	14.5	2.1	1.5	10.8
C	3	0		(Q_4 saturated, Q_6 cutoff)		
D	3	1.5	20	2.2	1.9	12.3

CHARACTERISTICS

Input Unbalance Current. The input unbalance current of the CA3002 is defined as the difference between the currents flowing into the base input terminals 10 and 5. Fig. 5 shows a curve of input unbalance current as a function of temperature. This unbalance current determines the maximum value of total effective external resistance that may be used in each base circuit (resistors R_1 in Fig. 2). A maximum value of 10,000 ohms is recommended for each base circuit. However, larger resistances may be accommodated if the resistors can be adjusted to maintain low input offset voltages, or if the operating points of Q_1 and Q_5 are not in the linear region (as in trigger circuits).

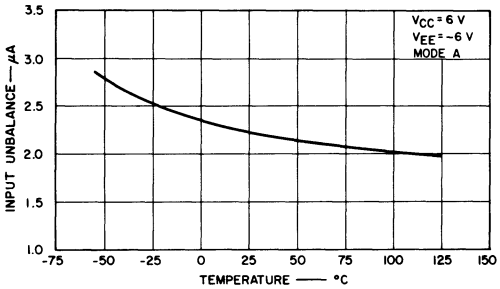


Fig. 5—Input unbalance current of the CA3002 as a function of temperature.

Input Impedance. The input impedance is essentially a characteristic of the input emitter-followers, Q_1 and Q_5. Because these transistors are lightly loaded, they have parallel input impedances that are approximately 0.1 megohm at low frequencies and rise to infinity and become negative at a few megahertz. In most cases, these impedances are negligible in comparison with the impedances of external base resistors or inductors. The input capacitance is 3 to 5 picofarads.

The input impedance decreases with decreasing operating temperature. A typical low-frequency value of parallel input resistance is 55,000 ohms at −55°C. If a resonant line or tuned circuit that has appreciable impedance in the vhf range is connected to either input terminal, a series parasitic resistor of 50 to 100 ohms should be placed in series with the input lead to prevent vhf oscillation.

Output Impedance. The output impedance is essentially that of the output emitter-follower Q_6, and is a function of the current in Q_6. The current, in turn, is determined by the operating mode, the supply voltages, and the connection of resistor R_6 to ground or to terminal 2. In operating mode D with R_6 returned to ground and ±6-volt supplies, the output resistance is approximately 80 ohms over most of the useful frequency range and rises to about 110 ohms (its highest value) at −55°C.

Frequency Response. The mid-frequency voltage gain of the CA3002 if amplifier is essentially independent of absolute resistor values, but depends on the resistor ratios. Fig. 6

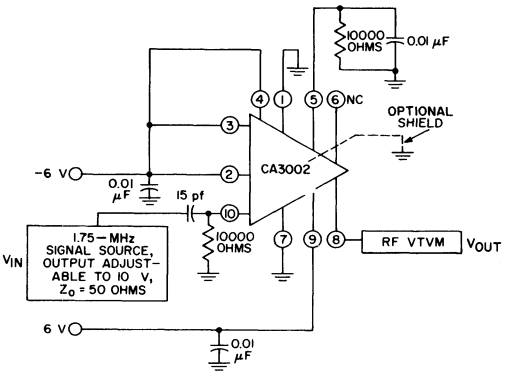
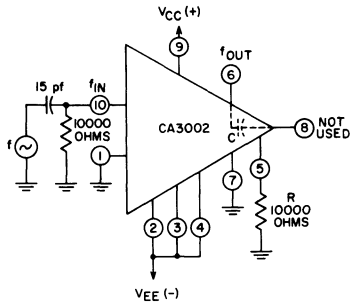


Fig. 6—Voltage-gain test circuit.

shows a test circuit used to measure the response characteristics of an iterative-coupled amplifier that uses an input-coupling capacitor of 15 picofarads.

The response curves for several values of positive and negative supply voltage are shown in Fig. 7. The gain of the



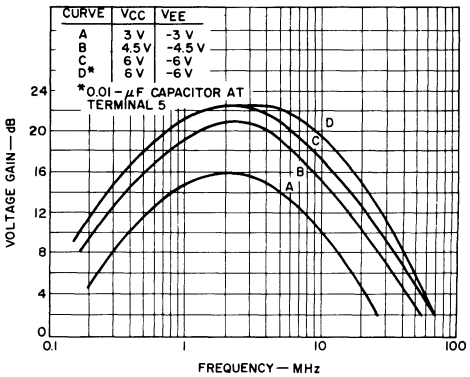
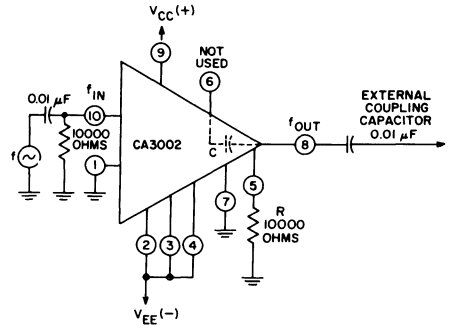


Fig. 7—Effective single-stage response characteristics of iterative-coupled if amplifier. Curve D represents operation with 0.01-microfarad capacitor connected at terminal 5 (not shown).

amplifier is reduced at low frequencies by the 15-picofarad input-coupling capacitor and at high frequencies by the RC roll-off within the circuit. The addition of a 0.01-microfarad bypass capacitor at terminal 5 improves both the high-frequency response and the mid-frequency gain by eliminating ac feedback from terminal 6 to terminal 5.

If a wideband video response is desired, the 15-picofarad internal silicon output-coupling capacitor of the CA3002 must be replaced with a larger external coupling capacitor connected to terminal 8. The response curves for an iterative-coupled amplifier that uses 0.01-microfarad input-coupling and output-coupling capacitors are shown in Fig. 8.



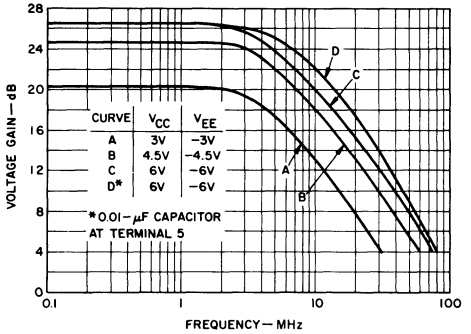


Fig. 8—Effective single-stage response characteristics for if amplifier using 0.01-microfarad coupling capacitors. Curve D represents operation with 0.01-microfarad capacitor connected at terminal 5 (not shown).

The response of the amplifier is substantially extended at the low frequencies. If 1-microfarad coupling capacitors are used, the low-frequency response can be extended below 100 Hz. Again, the addition of a 0.01-microfarad capacitor at terminal 5 improves the high-frequency performance. A shield separating the external leads at terminals 5 and 6 also reduces the feedback and extends the response.

AGC. The voltage gain of the CA3002 can be controlled over a wide range by adjustment of a negative dc voltage applied at terminal 1. Fig. 9 shows the voltage gain at 1.75 MHz (measured in the test circuit of Fig. 6) as a function

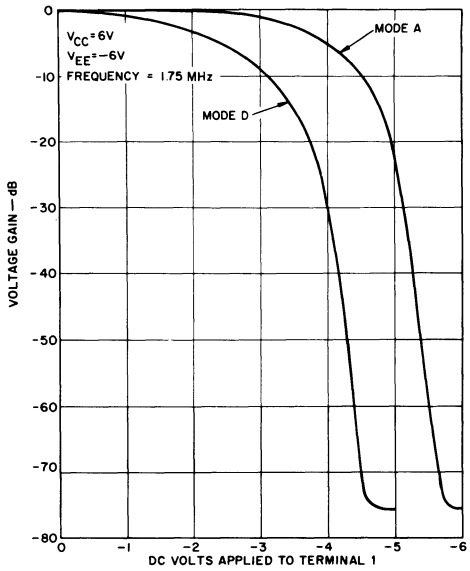


Fig. 9—Voltage gain of the CA3002 as a function of negative dc supply voltage applied at terminal 1 (normalized to a gain of 26 dB).

of the dc voltage. When the gain is controlled in this manner, the CA3002 can be used as an if amplifier with a 75-dB agc range, or as a video gating, squelching, or blanking circuit with a similar range. The circuit function depends only on the manner in which the dc voltage applied to terminal 1 is controlled. The agc range is dependent on frequency, and decreases from 75 dB at 1 MHz to 60 dB at 25 MHz.

Third-Order Intermodulation Distortion. Fig. 10 shows the peak-to-peak input signal required to produce third-order intermodulation distortion of 3 per cent as a function of gain control for the CA3002 integrated circuit. The maximum tolerable signal input for 3-per-cent intermodulation dis-

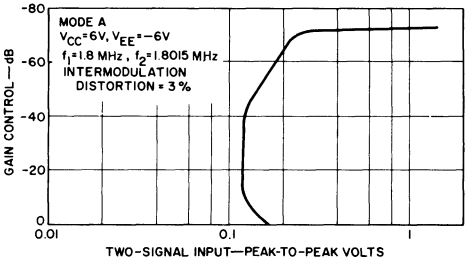


Fig. 10—Third-order intermodulation-distortion characteristic as a function of agc.

tortion is relatively constant over the entire agc range, but increases dramatically as cutoff is attained. When the CA3002 is operated in mode A with supplies of ±6 volts and an agc of −30 dB, a peak-to-peak input signal in excess of 100 millivolts is typically required for 3-per-cent distortion.

Noise Figure. Because noise figure is an important design parameter for both video and if-amplifier applications, it was evaluated for the CA3002 over the frequency range of 1 kHz to 10 MHz. Fig. 11 shows noise performance as a function of frequency when a 1000-ohm source is used. The noise figure is 4 dB over a large portion of the usable

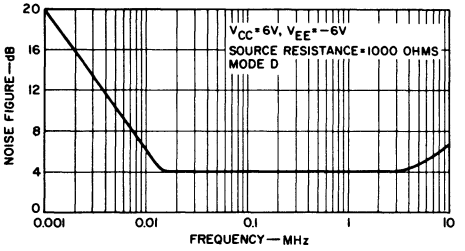


Fig. 11—Noise figure of the CA3002 as a function of frequency.

range. The 1/f noise corner occurs at approximately 15 kHz, and the high-frequency noise rise begins at approximately 4 MHz. Fig. 12 shows noise figure as a function of source resistance at 1.75 MHz. The typical noise figure is less than 4 dB. It is reasonably flat for source resistances from 500 to 2500 ohms, but rises rapidly at values below 500 ohms.

When external base-bias resistors are used, terminal 5 should be bypassed by an external capacitor for any stage which low noise figure is required. If the base-bias resistors are not bypassed, the noise figure increases. In a practical receiver, bypassing may be avoided if the input at terminal 10 is transformer driven (from a filter) and terminal 5 is grounded. In the later if stages, noise figure can usually be ignored.

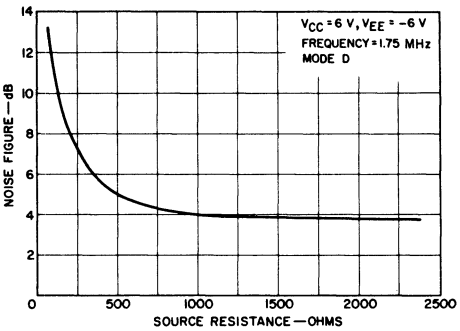


Fig. 12—Noise figure of the CA3002 as a function of source resistance.

APPLICATIONS

Four-Stage 1.75 MHz IF Amplifier. Effective if design for AM circuits requires consideration of both the signal level at the input stage (as a function of agc range) and the acceptable signal-to-noise ratio at the output. The agc action must be initiated at the first stage at the proper voltage level to prevent excessive modulation distortion throughout the entire agc range. This input-signal voltage level is calculated to be approximately 25 millivolts rms for 100-per-cent modulation at an allowable distortion of 10 per cent. Before the applied signal reaches 25 millivolts, the first stage must be gain controlled and completely cut off before gain control is applied to subsequent stages.

Fig. 13 shows a four-stage 1.75-MHz amplifier used to evaluate the performance of the CA3002 amplifier for AM

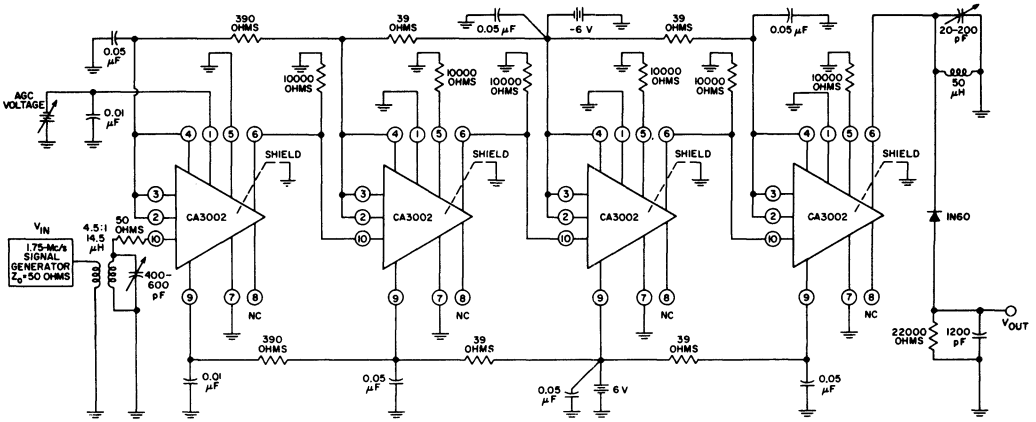


Fig.13—Four-stage 1.75-MHz if amplifier.

applications. A tuned circuit and a diode detector are connected to terminal 6 of the output stage to evaluate detected output and signal-to-noise ratio. The audio bandwidth of the detector output filter is 3 dB down at 4.2 kHz. The tuned circuit at the input is driven by a 50-ohm generator and provides a 1000-ohm source to the circuit. The first stage is operated at reduced supply voltages (about ±3 volts) to reduce the required agc control voltage. This lower supply-voltage level ensures that a sufficient control voltage can be developed by a separate CA3002 unit used as an agc amplifier without introducing a separate supply voltage. An additional advantage of lower-voltage operation in the first stage is a reduction in noise figure.

If desired, the first-stage tuned circuit in Fig. 13 can be replaced by a crystal filter and a transformer. Because the CA3002 input impedance is high and does not vary appreciably with agc, no impedance variations are presented to the crystal filter.

The voltage gain realized from terminal 10 of the first stage to terminal 6 of the fourth stage is 85 dB, or approximately 21 dB per stage. From the 50-ohm input, the typical voltage gain is 98 dB. Because the maximum signal-handling capability of the output stage is slightly greater than 0.7 volt rms, gain control should begin when this value is measured at terminal 6. The modulation distortion is acceptable over the entire 60-dB agc range. For input signals greater than 8 millivolts, modulation distortion begins to increase because of fourth-stage overload. Overloading can be prevented by application of a delayed gain control to the second stage. The signal-to-noise performance as a function of input signal is shown in Fig. 14.

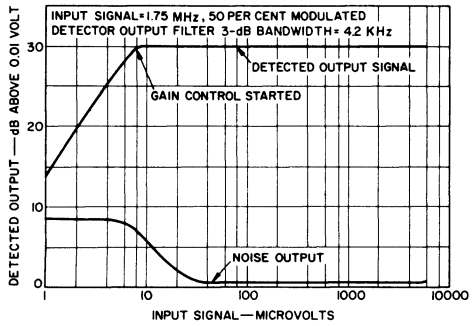


Fig. 14—Output signal and noise of the amplifier shown in Fig. 13.

Envelope Detector. The CA3002 integrated circuit can be operated as an envelope detector in either of two ways, as shown in Fig. 15: (1) the emitter of the output transistor Q_6 can be operated at zero voltage by connection of an external resistor in the bias loop of the constant-current transistor Q_3, or (2) the current in transistor Q_6 can be reduced by connection of a large resistor (12,000 to 18,000 ohms) in series with its emitter resistor.

In the circuit for method 1, the current in the differential pair (Q_2 and Q_4 in Fig. 1) is increased to the point at which the common-collector output transistor Q_6 is biased almost to cutoff. For this current increase, the constant-current transistor Q_3 is operated with terminal 4 open, and the emitter resistor R_3 is shunt loaded by the external resistor at terminal 3. Envelope detection can be accomplished only in mode A with method 1.

Although the output transistor is nearly cut off, all the other active devices are operating in their linear regions.

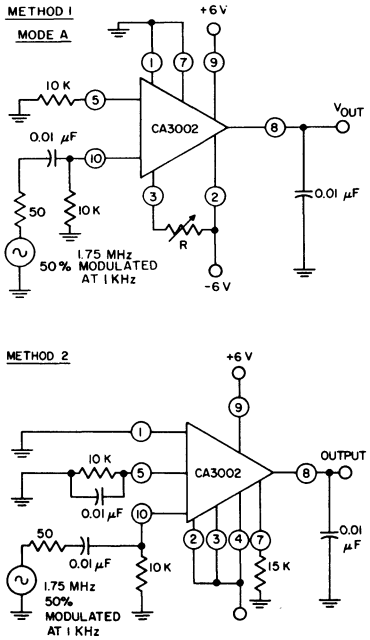


Fig. 15—Envelope detectors using CA3002 integrated circuits.

For small ac signals, therefore, the circuit provides linear operation except for Q_6, which is turned on only by a positive signal. The maximum acceptable input signal depends on the linear range of the differential amplifier. An external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

In the circuit diagram for method 2 shown in Fig. 15, a fixed value of resistance (15,000 ohms) is used to reduce the emitter current in the output transistor (Q_6) to approximately 100 microamperes. This operating point provides the nonlinearity for detection in transistor Q_6. Again, the remainder of the circuit produces gain because it is operating linearly. As in the case of method 1, an external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

Fig. 16 shows the input-output characteristics of the envelope-detector circuits shown in Fig. 15. The usable range of input signals for distortion below 3 per cent is 10 to 100 millivolts (20-dB range) for method 1 and 12 to 60 millivolts (14-dB range) for method 2. Automatic gain control of the if amplifier must maintain the input signals to the detector within this range.

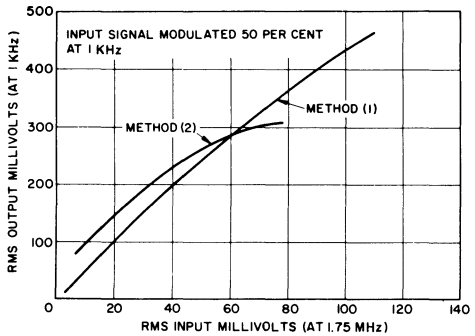


Fig. 16—Input-output characteristics of the envelope detectors shown in Fig. 15.

Product Detector. A differential pair driven by a constant-current transistor can be used as a product detector if a suppressed-carrier signal is applied to the differential pair and the regenerated carrier is applied to the constant-current transistor. There are two requirements for linearity: (1) the circuit must be operated in a linear region, and (2) the current from the constant-current transistor must be linear with respect to the reinserted carrier voltage.

The CA3002 satisfies these requirements and can be used as a product detector in the circuit shown in Fig. 17. A double-sideband suppressed-carrier signal is applied at terminal 10, and the 1.7-MHz carrier is applied to terminal 1.

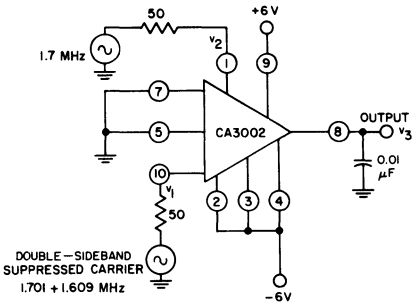


Fig. 17—Product detector circuit.

Because of the single-ended output, a high-frequency bypass capacitor (0.01 microfarad) is connected between terminal 8 and ground to provide filtering for the high-frequency components of the oscillator signal at the output.

When the amplitude of the suppressed-carrier signal and of the oscillator signal are varied, the gain and distortion characteristics shown in Table III are obtained. The conversion voltage gain is constant at input signals up to 16 millivolts and would be 6 dB less for a single-sideband signal than for the double-sideband signal. The distortion increases with increasing input signal; for distortion of less than 1 per cent, the input drive level does not exceed 8 millivolts. The gain maximizes for oscillator voltages of 1 to 2 volts, and the distortion characteristic is also best in this region. Distortion increases both at low oscillator drive levels (0.25 volt) and at high levels (3 volts).

Schmitt Trigger. Fig. 18 shows the use of the CA3002 as a Schmitt trigger. In this application, the input is applied to terminal 5 and both the output and the feedback are taken from the output emitter-follower at terminal 8. The emitter-follower output isolates the feedback loop from the differ-

Table III—Performance Data for CA3002 as Product Detector

v_1 Double-Sideband Voltage (mV)	v_2 Oscillator Voltage at Terminal 1 (V)	v_3 Output at Terminal 8 at 1 kc/s (mV)	Conversion Voltage Gain (dB)	dB down from Fundamental of Harmonics * Harmonic 2nd	3rd	4th	5th
1	1.7	12.5	21.9	60			
4	1.7	50	21.9	51	61		
8	1.7	100	21.9	46	56		
16	1.7	200	21.9	37	46		
32	1.7	310	19.8	32	30	51	64
4	0.25	22	15.6	15	42	44	
4	0.5	42	20.3	32	52		
4	1.0	60	23.5	45	60		
4	1.3	60	23.5	49	61		
4	1.7	50	21.9	51	61		
4	2.0	48	21.6	52	62		
4	2.5	31	17.8	49	60		
4	3.0	15	11.4	42	60		

*Harmonic Distortion Greater than 65 dB Down If Omitted

ential pair and makes it possible for the circuit to drive low-impedance loads. An additional advantage is that neither half of the differential pair saturates as the resistance of the feedback loop is varied. Fig. 18 also shows the output swing and associated hysteresis of the Schmitt trigger as a function of resistor R and the dc input voltage level at terminal 5.

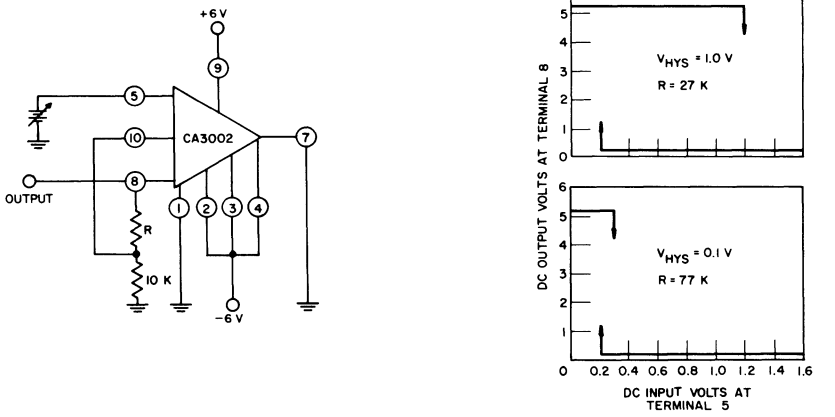


Fig. 18—Schmitt trigger circuit and output swing and associated hysteresis.

Application of the RCA-CA3007 Integrated-Circuit Audio Amplifier

by
R.G. TIPPING

The RCA-CA3007 audio driver is a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit features all-monolithic silicon epitaxial construction, and is intended for use as a direct-coupled driver in a class B audio amplifier which exhibits both gain and operating-point stability over the temperature range from -55 to 125°C. Because of its circuit configuration (a balanced differential pair fed by a constant-current transistor), the CA3007 is an excellent controlled-gain audio driver for systems requiring audio squelching. This circuit is also usable as a servo driver. The audio driver circuit is available in a 12-terminal TO-5 low-silhouette package.

CIRCUIT DESCRIPTION

Fig.1 shows the schematic diagram and terminal connections for the CA3007 circuit. The input stage consists of a differential pair (Q_1 and Q_2) operating as a phase splitter with gain. The two output signals from the phase splitter, which are 180 degrees out of phase, are direct-coupled through two emitter-followers (Q_4 and Q_5). The emitters of the differential pair are connected to the transistor constant-current sink Q_3.

The diodes in the bias circuit of the transistor constant-current sink make the emitter current of Q_3 essentially dependent on the temperature coefficient of the diffused emitter resistor R_3. Because the diffused collector resistors R_{15} and R_{16} should have identical temperature coefficients, constant collector-voltage operating points should result at the collectors of transistors Q_1 and Q_2. However, the quiescent operating voltages at the output terminals 8 and 10 increase as temperature increases because the base-emitter voltage drops of transistors Q_4 and Q_5 decrease as temperature increases. This small variation in the output quiescent operating voltage is sufficient to cause a large variation in the standby current of a class B push-pull output stage when the audio driver and the output stage are direct-coupled. Resistors R_{11}, R_{12}, R_{13}, and R_{17} and transistor Q_6 form a dc feedback loop which stabilizes the quiescent operating voltage at output terminals 8

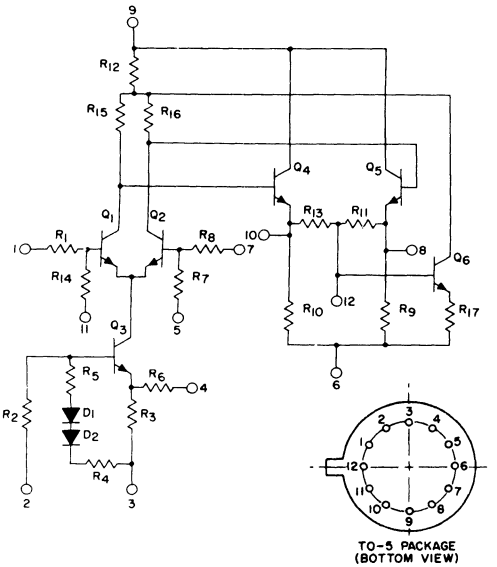


Fig.1 - Schematic diagram and terminal connections for the CA3007 audio driver.

and 10 for both temperature and power-supply variations so that variations in the output operating points are negligible.

Resistors R_1, R_7, R_8, and R_{14} form the input circuit; a double-ended input is applied to terminals 1 and 5, and a single-ended input is applied to either terminal 1 or terminal 5, with the other terminal returned to ground. The CA3007 must be ac-coupled to the input source. In addition, any dc resistance between terminal 1 and ground should be added between terminal 5 and ground. Output power-gain stabilization for a direct-coupled driver and output stage is accomplished by means of an ac feedback loop that connects terminals 7 and 11 to the proper emitters of the push-pull output stage, as shown in Fig.2.

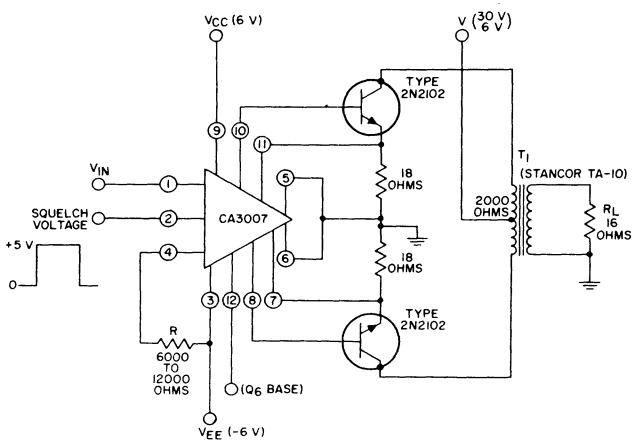


Fig.2 - CA3007 used as an audio driver for a direct-coupled 300-milliwatt audio amplifier.

Connection of voltage supplies to the CA3007 audio driver requires that the most positive voltage be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). The CA3007 may be operated from various supplies and at various levels. Operation from either a single supply (as shown in Fig.3) or from dual power supplies (as shown in Fig.2) is feasible. For dual-supply operation, symmetrical supplies must be used if the audio driver is to be direct-coupled to the audio output stage. For single-supply operation, the audio driver must be ac-coupled to the audio output stage, and the number of external components required increases.

The external resistor R connected between terminals 3 and 4 is used to set the class B output-stage standby current as required for a particular application. If the standby current is too low, crossover distortion will result; if it is too high, standby power drain will be excessive. Decreasing the value of resistor R reduces the standby current; for a standby current of 10 milliamperes, R is typically 10,000 ohms.

Terminal 2 must be grounded or, if an audio squelch is desired, must be connected to a positive voltage supply of 5 volts minimum. When terminal 2 is near ground, the audio amplifier functions normally. When

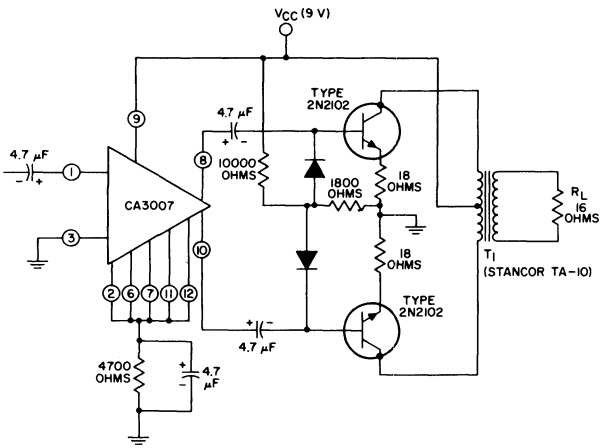


Fig.3 - CA3007 used as an audio driver for a 30-milliwatt audio amplifier.

For operation from either single or dual supplies, the operating current is transistor Q_3 is determined by the bias voltage between terminals 2 and 3. The more negative terminal of this bias voltage must be connected to terminal 3. For dual-supply systems, terminal 2 is either grounded or connected to a trigger circuit for audio-squelching purposes.

APPLICATIONS

Dual-Supply Audio Driver in a Direct-Coupled Audio Amplifier. Fig.2 shows the CA3007 used as a dual-supply audio driver in a direct-coupled audio amplifier. This amplifier provides a power output of 300 milliwatts for an audio input of 0.3 volt rms (V_{CC} = 6 volts, V_{EE} = -6 volts, V = 30 volts). For a voltage V of 6 volts, the output power is 10 milliwatts without transformer optimization; the use of a lower-impedance transformer would permit power outputs in the order of 100 milliwatts.

terminal 2 is at 5 volts, the differential pair of the audio driver saturates, and the push-pull output stage is cut off. The squelch source must be capable of supplying a current of 1.5 milliamperes in the 5-volt condition, and 0.75 milliampere in the near-ground condition.

For a symmetrical audio driver, there is no ac signal present at the base of transistor Q_6. However, unbalances between the two halves of the circuit may require that the base of Q_6 be bypassed for proper operation. The base of Q_6 may be bypassed by connection of an external capacitor (typically 50 microfarads, 6 volts) from terminal 12 to ground. Bypassing is usually not required unless high undistorted power outputs are required over the complete temperature range of -55 to 125°C.

Table I shows values of harmonic distortion and intermodulation distortion for the amplifier of Fig.2.

Table I - Distortion Measurements for Direct-Coupled Amplifier Shown in Fig.2

HARMONIC DISTORTION

Power Output (mW)	*Output-Signal Level (mVrms) with 2-kHz Input Signal*						*Harmonic Distortion (%)*
	2 kHz	*4 kHz*	*6 kHz*	*8 kHz*	*10 kHz*	*12 kHz*	
62.5	1000	9	3.0	—	—	—	0.95
140	1500	18	4.0	2.0	1.4	1.0	1.24
250	2000	25	4.2	5.0	1.0	1.5	1.30
330	2300	27	6.0	9.0	3.0	2.0	1.27

INTERMODULATION DISTORTION

Output-Signal Level:
at f_1 (2 kHz) ..... 1000 mV rms
at f_2 (3 kHz) ..... 1000 mV rms
at $2f_2$-f_1 (4 kHz) ..... 0.7 mV rms
3rd-Order IMD ..... 0.07 %

Single-Supply Audio Driver in a Capacitor-Coupled Audio Amplifier. Fig.3 shows the CA3007 used as a single-supply audio driver in a capacitor-coupled audio amplifier. This amplifier provides a power output of 30 milliwatts for an audio input of 6.5 millivolts rms (V_{CC} = 9 volts) with the transformer shown.

The connection shown in Fig.3 still represents a differential-pair phase splitter fed from a constant-current transistor. The two output signals from the phase splitter are direct-coupled through two emitter-followers which are capacitor-coupled to the push-pull output stage. Because of the ac coupling, there is no longer a dc dependence between the driver and the output stage, and any desired audio output design or drive source may be used. As a single stage, the CA3007 audio driver provides a voltage gain of 24 dB for a dc power dissipation of 20 milliwatts with the harmonic distortion reaching 3 per cent for outputs of 0.6 volt rms at terminals 8 and 10 (without feedback).

Both dc and ac feedback loops are eliminated in the circuit of Fig.3. Although the dc feedback loop is no longer required bacause of the ac coupling, removal of the ac feedback loop causes the output power gain to decrease about 1 dB for a 50°C rise in temperature.

Application of the RCA-CA3001 Integrated-Circuit Video Amplifier

BY
G. E. THERIAULT

The CA3001 silicon monolithic integrated circuit is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 incorporates the following primary features: (a) all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from —55 to 125°C; (b) balanced differential-amplifier configuration with low-impedance double-ended input; (c) built-in temperature-compensating network for gain or dc operating-point stability over the temperature range from —55 to 125°C. This integrated-circuit amplifier is available in a 12-pin TO-5 low-silhouette package.

CIRCUIT DESCRIPTION

Fig. 1 shows the schematic diagram and terminal connections for the CA3001 amplifier. The circuit consists of a differential pair Q_3 and Q_5, the current of which is controlled by a constant-current transistor Q_4. Transistors Q_1, Q_2, Q_6, and Q_7 are operated in the common-collector configuration to provide a high-impedance input and low-impedance output. Thus, the CA3001 provides double-ended input and output, and can be iteratively connected with low-value coupling capacitors. The high-frequency response of the circuit is determined primarily by the resistance and capacitance in the collectors of the differential pair Q_3 and Q_5.

BIASING

When voltage supplies are connected to the CA3001, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). For typical operation, terminals 2 and 10 are returned to ground. If desired, however, automatic gain control can be applied to terminal 2, and terminal 10 can be connected to the negative supply to permit larger negative-going output swings in the output transistors.

The CA3001 may be operated with various supplies and at various levels. Operation from either a single supply or dual supplies is feasible, as shown in Fig. 2. When dual supplies are used, they may be either symmetrical or nonsymmetrical. The use of separate positive and negative supplies minimizes the need for external components, as shown in Fig. 2(a). For single-supply applications, a resistor divider and a bypass capacitor must be added, as shown in Fig. 2(b).

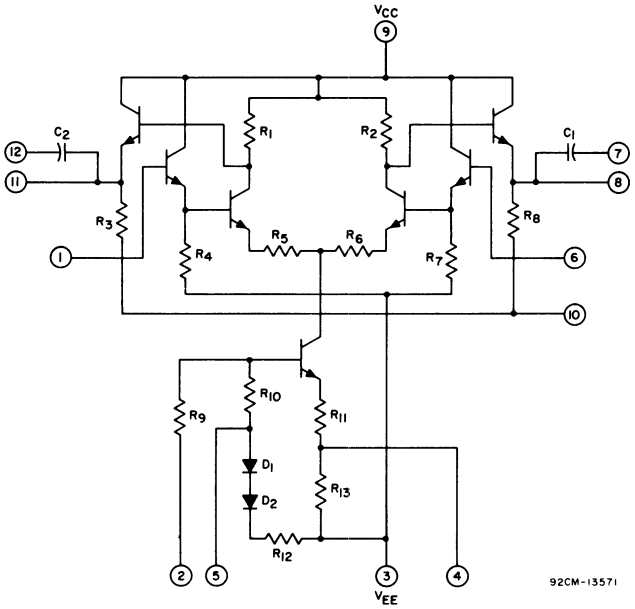


Fig.1 - Schematic diagram and terminal connections for the CA3001 video amplifier.

When dual supplies are used, the inputs (terminals 1 and 6) are referenced to ground through equal external resistors (the maximum recommended value of R is 3300 ohms for linear operation). The current through the resistor divider R_1 and R_2 should be greater than 1.5 milliamperes. For either single or dual supplies, the operating current in transistor Q_4 is determined by the operating mode. For any given bias voltage, four operating modes are possible, as described in Table I. Each mode is characterized by a distinct operating current and a corresponding voltage gain, both of which have a particular temperature dependence.

Table I—Four Possible Operating Modes for CA3001 Amplifier

Operating Mode	*Shorted Terminals*	*Condition of Diodes*	*Q_4 Emitter Resistor*
A	none	in	$R_{11} + R_{13}$
B	5-3	out	$R_{11} + R_{13}$
C	4-3	in	R_{11}
D	5-4-3	out	R_{11}

Table II shows typical design performance characteristics for the four operating modes of the CA3001 at room temperature. The output operating point and voltage gain of the circuit are reasonably independent of resistor value, but the

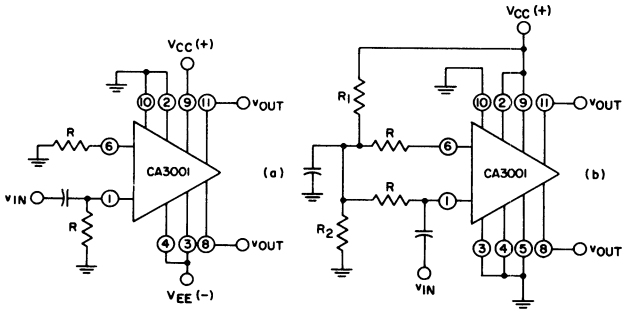


Fig.2 - Circuit connections for the CA3001 for (a) separate positive and negative voltage supplies, and (b) a single supply.

Table II—Typical Design Performance Characteristics for the CA3001 Amplifier (terminals 2, 10, 6, and 1 referenced to ground) at 25°C

Operating Mode	*Supplies (±V)*	*Output Operating Volts (Terminals 8 and 11 To Ground)*	*Positive Supply Current (mA)*	*Negative Supply Current (mA)*	*Power Dissipation (mW)*	*Single-Ended Voltage Gain at 1 MHz (dB)*
A	6	4.3	8.4	−4.7	79	15.5
B	6	4.8	7.8	−3.9	70	12.7
C	6	2.8	9.9	−7.9	106	17.8
D	6	4.1	8.7	−5.5	85	16.4
A	4.5	3.0	6.0	−3.4	43.6	14.6
B	4.5	3.4	5.6	−2.7	37.6	10.0
C	4.5	2.0	7.2	−5.8	58.4	17.7
D	4.5	2.9	6.0	−3.7	43.6	15.5
A	3	1.8	3.7	−3.9	22.6	13.0
B	3	2.1	3.3	−1.4	14.3	3.8
C	3	1.0	4.4	−3.7	25.5	16.4
D	3	2.0	2.4	−1.9	13.0	10.8

current and power dissipation may vary with resistor values. Figs. 3 and 4 show theoretical curves of output operating point and power gain, respectively, as functions of temperature for nominal resistor values with supply voltage V_{EE} of −3 and −6 volts dc. The voltage between terminals 8 and 9 or terminals 11 and 9 is denoted by V_X. Because the variation of voltage gain and operating point with temperature is small for all operating modes, the choice of mode depends on application requirements. With a supply voltage V_{EE} of −4.5 volts, voltage-gain variation is normally less than 0.5 dB for all operating modes over the temperature range of −55 to 125°C.

CHARACTERISTICS

Frequency Response. When the CA3001 video amplifier is used in cascade, its high-frequency response is determined primarily by the RC roll-off at the collectors of the differential pair Q_3 and Q_5. The generator source resistance may affect high-frequency bandwidth; for full bandwidth capability, the parallel combination of source resistance and base-bias resistance should not exceed 800 ohms. The low-frequency response is determined by the coupling capacitor and the base-bias resistance value.

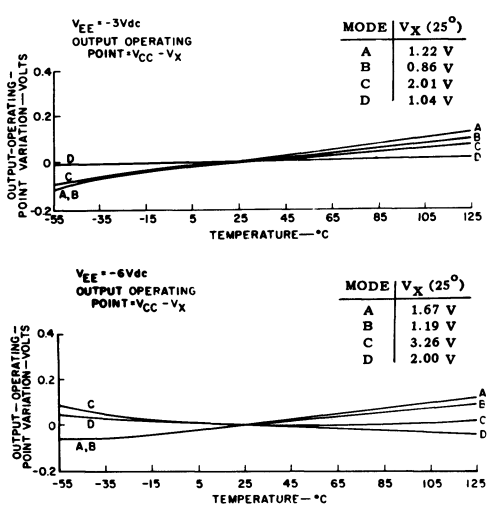


Fig.3 - Output operating point of the CA3001 (normalized to the 25°C operating point) as a function of temperature for V_{EE} supplies of -3 and -6 volts dc.

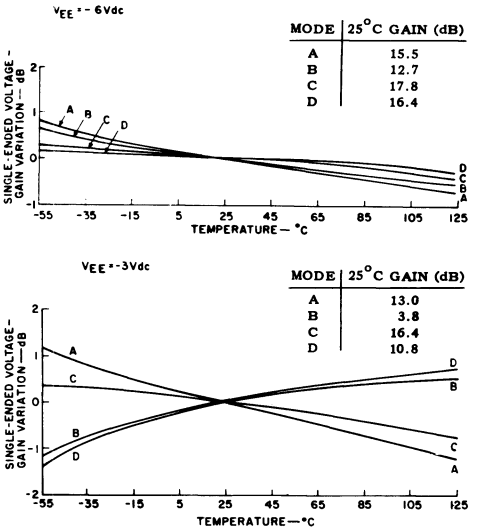


Fig.4 - Voltage gain of the CA3001 (normalized to the 25°C gain) as a function of temperature for V_{EE} supplies of -3 and -6 volts dc.

Fig. 5 shows the circuit used for evaluation of frequency response of the CA3001, together with the response characteristics obtained. The circuit is operated in mode C with supplies of ±6 volts. The 50-ohm generator simulates the frequency and gain behavior for iterative operation. The curves of Fig. 5 show the measured response characteristics with terminal 6 bypassed and unbypassed. When terminal 6 is bypassed, the voltage gain is down 3 dB at 16 MHz,

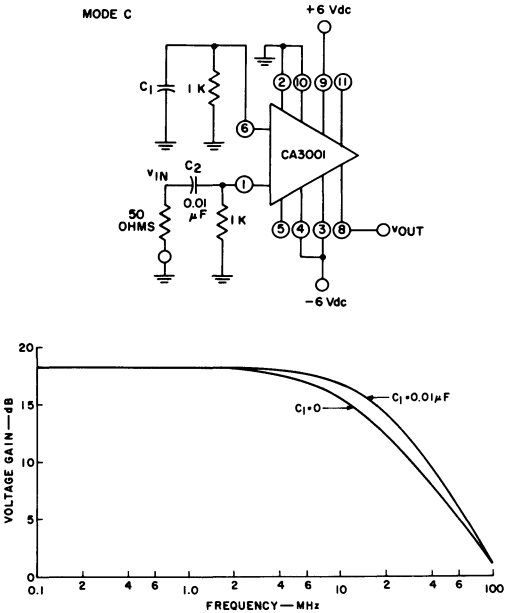


Fig.5 - Frequency response of the CA3001 as a function of capacitor C_1 in the test circuit shown with terminal 6 bypassed and unbypassed.

and is greater than 10 dB through 30 MHz. When the nondriven input (terminal 6 in the circuit shown) is not bypassed, the gain decreases more rapidly as a result of the feedback capacitance between terminals 7 and 6. This feedback can be minimized by use of short leads and inter-terminal shielding. A shielding method is to ground terminal 7.

The high-frequency roll-off of the CA3001 is a function of the values of resistors R_1 and R_2 in Fig. 1 and their variation with temperature. Fig. 6 shows the effect of temperature on high-frequency response. The variation in response can be accounted for by the resistance variation with temperature; capacitance variations with temperature are a secondary effect.

The internal capacitors provided at the outputs of the CA3001 (C_1 and C_2 in Fig. 1) can be used for coupling circuits in cascade for narrow-band applications. Because

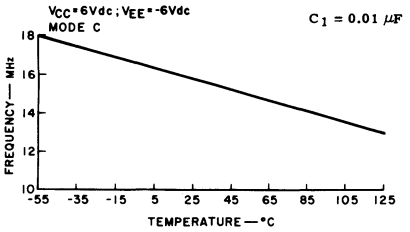


Fig.6 - High-frequency 3-dB bandwidth of the CA3001 as a function of temperature.

the value of these capacitors is small, the external base-bias resistors shown in Fig. 5 should be increased from 1000 to 3300 ohms to improve low-frequency response. Fig. 7 shows the response characteristics for a single stage in which the input is applied to terminal 1 from a 50-ohm generator through a capacitor (equal in value to C_2 in Fig. 1), and the voltage gain is measured from the generator to output terminal 8. Because this arrangement simulates single-ended operation, the results can be applied directly to iterative operation.

The voltage division between the input capacitance and the coupling capacitor causes a reduction in voltage gain at all frequencies. The feedback capacitance from output to input also affects the gain performance, as shown in Fig. 7.

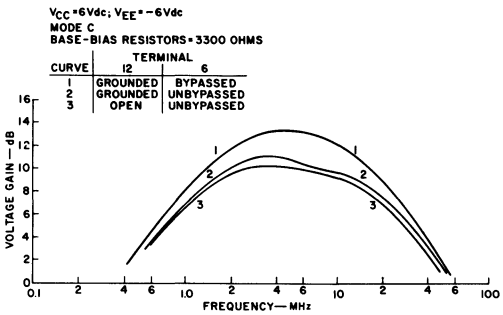


Fig.7 - Response characteristics of a CA3001 amplifier with capacitor-coupled input.

Input and Output Impedance. Fig. 8 shows the parallel input resistance and capacitance of the CA3001 as a function of frequency. The input capacitance is constant until it begins to decrease at high frequencies. The input resistance decreases through the frequency range from 0.1 to 10 MHz. Because the input resistance is high in comparison with the external base-bias resistors used (3300 ohms maximum), the high-frequency response characteristic of the input is determined by the driving-source resistance, the base-bias resistors, and the parallel input capacitance.

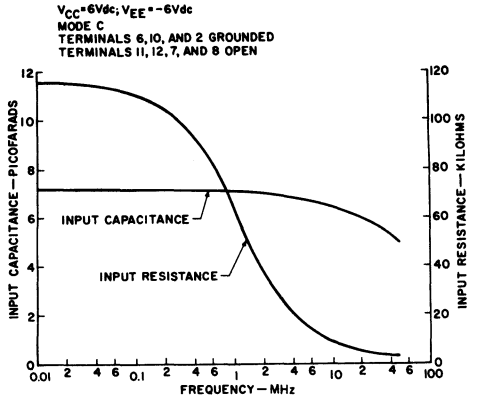


Fig.8 - Parallel input resistance and capacitance of the CA3001 as functions of frequency.

The parallel output resistance of the CA3001 is low (approximately 70 ohms), and the output reactance is sufficiently high to provide little or no degradation of frequency response through the usable frequency range.

Noise Figure. Fig. 9(a) shows noise figure as a function of frequency for a 1000-ohm source. The 1/f noise corner occurs at approximately 30 kHz; above this frequency, the noise figure remains flat at approximately 5 dB to 6 MHz, and then begins to rise.

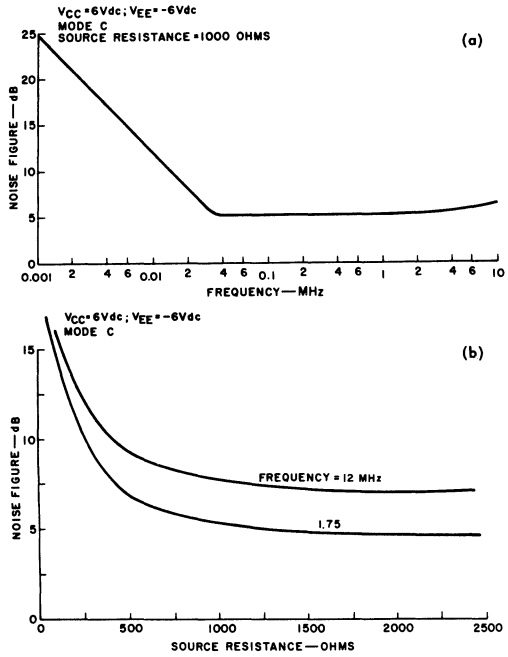


Fig.9 - Noise figure of the CA3001 as a function of frequency and source resistance.

Fig. 9(b) shows noise figure as a function of source resistance for frequencies of 1.75 and 12 MHz. For stages in which noise performance is important, the source resistance should not be less than 500 ohms because of the rapid rise in noise figure at lower values. The noise figure of the CA3001 increases when non-driven base-bias resistors are unbypassed. For stages in which noise performance is important, the external resistor on an input base that is not receiving a signal must be bypassed if minimum noise figure is to be achieved.

Gain Control. AGC can be applied to the CA3001 at terminal 2 for any of the four operating modes. Fig. 10 shows representative agc characteristics for modes C and D at a frequency of 1 MHz. The threshold voltage is higher in mode C than in mode D because of the difference in the base-bias circuit for the constant-current sink transistor (Q_4).

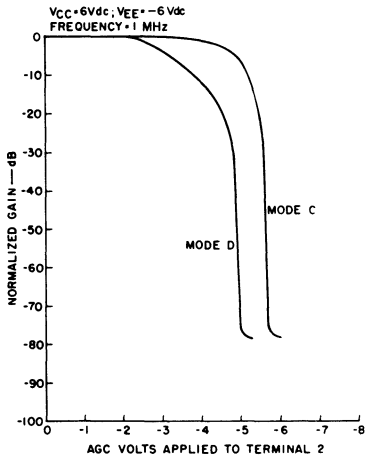


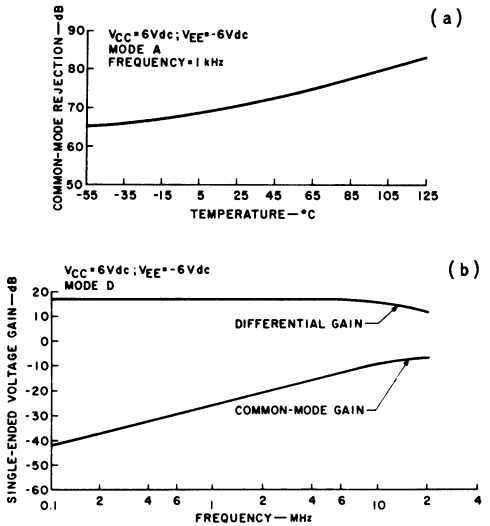
Fig.10 - AGC characteristics of the CA3001 in modes C and D at 1 megahertz.

The agc range is dependent on frequency. At high frequencies, because the feedthrough parameters are primarily capacitive, it should eventually decrease at a rate of approximately 20 dB per decade. The average measured agc range at 10 MHz is 62 dB, and is 15 dB less than that at 1 MHz.

Common-Mode Rejection. The common-mode rejection of a differential amplifier is defined as the ratio between the full differential gain and the common-mode gain. It is a useful performance characteristic, particularly at low

frequencies. Fig. 11(a) shows the common-mode rejection of the CA3001 as a function of temperature at a frequency of 1 kHz. The common-mode rejection increases with increasing temperature; a typical value at 25°C is 70 dB.

Because the CA3001 can be used in many applications with a single-ended output at high frequencies, both the single-ended differential gain and the single-ended common-mode gain are of considerable interest. Fig. 11(b) shows



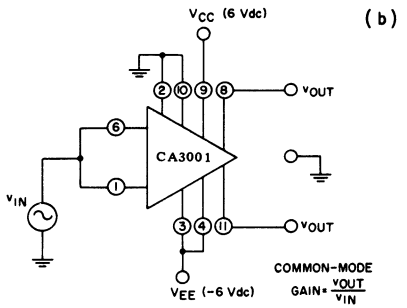


Fig. 11 - Common-mode rejection and voltage-gain characteristics of the CA3001 as a function of temperature and frequency.

both single-ended common-mode and differential-mode gain as functions of frequency. The common-mode gain is a function of the impedance ratio between the constant-current transistor (Q_4) and the load resistor in one side of the differential pair (Q_3 or Q_5). The common-mode gain increases with increasing frequency.

The common-mode rejection is degraded if sufficient signal is applied to saturate the constant-current transistor (Q_4). The maximum peak-to-peak input voltage without degradation of common-mode rejection is a function of the voltage supplies and the operating mode of the constant-current transistor.

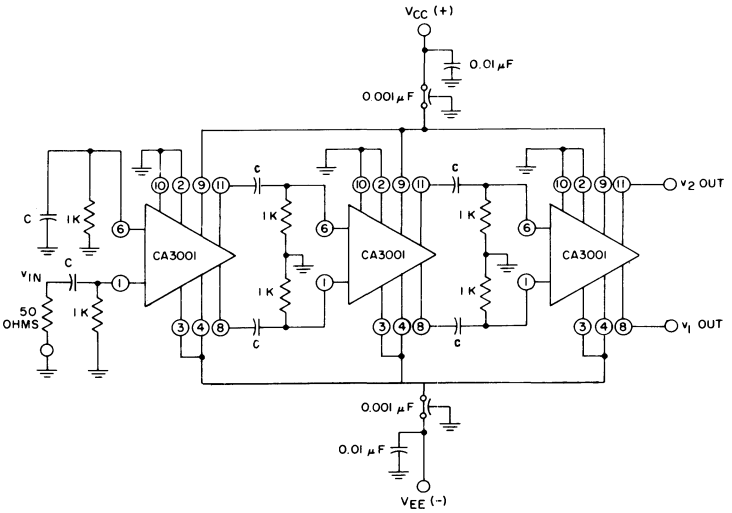
Harmonic Distortion and Swing Capability. When equal positive and negative supplies are used, operating mode C provides the largest swing capability because the output operating point is approximately centered. With voltage supplies of ±6 volts dc at a frequency of 1 MHz, the single-ended output is 1.3 volts rms for 3-per-cent distortion in mode C and 0.665 volt rms in mode D.

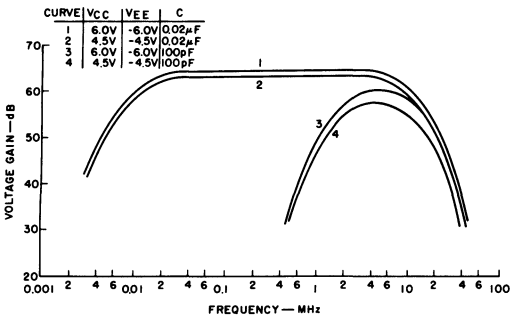
The signal-swing capability was also evaluated as a function of temperature in mode C with voltage supplies of ±6 volts dc. For 3-per-cent distortion, an output swing of 1.2 volts rms can be obtained over the complete temperature range from 25 to 125°C.

For pulse-type signals, the total possible swing capability is important. The voltage at the collectors of the differential pair may rise to the positive supply voltage, V_{CC}, and fall to the saturation level. If the bases of the input emitter-followers are maintained at zero potential, the emitters of the differential pair are negative by twice the base-to-emitter voltage drop, V_{BE}, or approximately −1.4 volts. If the saturation voltage is assumed to be 0.2 volt, the collectors drop to about −1.2 volts before saturation. Therefore, the total swing available at the collectors is approximately V_{CC} + 1.2 volts; for a V_{CC} of 6 volts, the swing is 7.2 volts. The output voltage swing is lower than this value by V_{BE}, or from 5.3 to −2.0 volts. This total swing capability can be realized only when the resistors R_3 and R_8 (terminal 10) are returned to the negative supply voltage (terminal 10 shorted to terminal 3). Selection of the operating point to obtain most of the available total swing in one direction involves proper choice of the operating mode and the negative supply voltage.

APPLICATIONS

Cascaded Stages. Over-all performance characteristics for three CA3001 stages operated in cascade are shown in Fig. 12. The need for supply decoupling is minimized by the symmetry of the circuit, which ensures equal and out-of-phase currents in the supply leads. Three circuits in close proximity can provide stable over-all gains of approximately 65 dB. A further advantage of the CA3001 in cascade is





$$\text{Voltage Gain} = 20 \log \frac{V_{1\,OUT}}{V_{IN}}$$

Fig. 12 - Three-stage CA3001 cascade amplifier and frequency-response characteristics.

that a gain increase of 6 dB accrues each time a double-ended output is used.

Table III and Fig. 12 show the performance of the CA3001 in the three-stage cascade circuit for various values of supplies and coupling capacitors. The only advantage of ±6-volt supplies as compared to ±4.5-volt supplies is a larger output-swing capability. The use of ±4.5-volt supplies entails no sacrifice in bandwidth and little gain loss, and provides a saving in power dissipation of almost 2 to 1. Better signal-to-noise performance can be achieved

Table III—Performance of CA3001 Cascade Amplifier shown in Fig. 12

Coupling Capacitor		*0.02 μF*		*100 pF*		
Voltage Supplies		*±6*	*±4.5*	*±6*	*±4.5*	*Vdc*
Power Dissipation		276	146	276	146	mW
Single-Ended-Output Midband Gain		64.5	63	60.5	57.5	dB
3-dB Response	Upper	9	9	10.5	10.5	MHz
	Lower	0.0125	0.0125	1.9	1.9	MHz
AGC Range		65	63	61	59	dB
Output Signal for 3-per-cent Distortion		1.3	1.15	1.15	0.7	Vrms
Input Signal for 3-dB Signal-to-Noise Ratio		26	14	20	18.5	μVrms

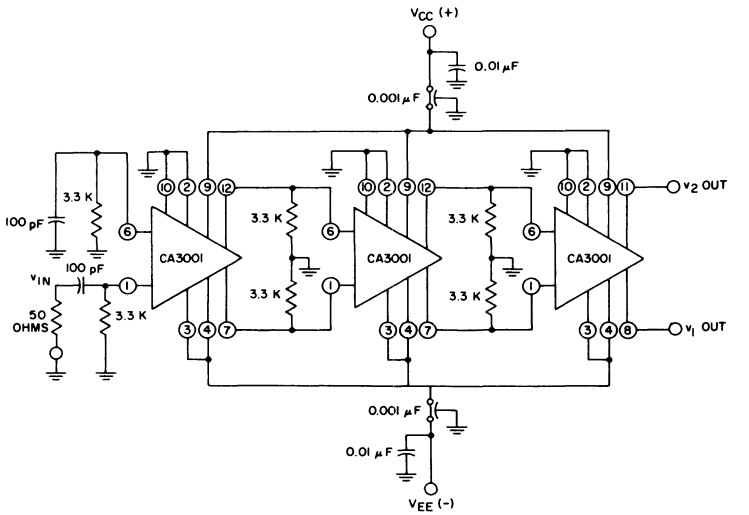
with no change in bandwidth if a higher value of source resistor is used (e.g., 800 ohms, rather than the value of 50 ohms shown in Fig. 12). The agc range of the cascaded circuits was 10 dB less than that for an individual circuit because no interstage shielding was provided and double-ended output was not used.

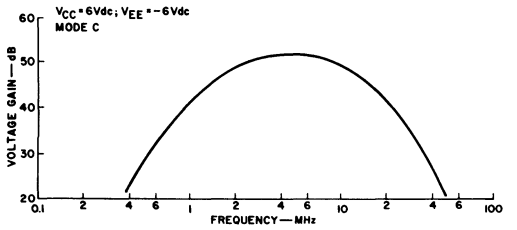
The CA3001 was also evaluated in a three-stage cascade arrangement in which the internal capacitors were used for coupling. The circuit diagram for this evaluation is shown in Fig. 13, and the measured characteristics are shown in Table IV and Fig. 13.

Schmitt Trigger. The CA3001 has an advantage in Schmitt-trigger applications because the emitter-follower outputs isolate the impedances of the feedback loop from the differential stage. These outputs are also capable of driving low-impedance loads. When symmetrical power supplies of up to ±6 volts are used, the CA3001 operates without saturation of the basic differential pair (Q_3 and Q_5). For each of the four operating modes, a complete offset at the input that causes all the sink-transistor current to pass through either Q_3 or Q_5 does not bring these transistors into saturation. As a result, uncertainties resulting in hysteresis prediction caused by storage time are eliminated.

Table IV—Performance of CA3001 Cascade Amplifier shown in Fig. 13

Operating Mode	*C*	
Voltage Supplies	±6	Vdc
Power Dissipation	276	mW
Single-Ended-Output Midband Gain	51.5	dB
3-dB Reponse Upper	11.3	MHz
Lower	1.8	MHz
Output Signal for 3-per-cent Distortion	0.85	Vrms
Input Signal for 3-dB Signal-to-Noise Ratio	19	μVrms





$$\text{Voltage Gain} = 20 \log \frac{V_{1\,OUT}}{V_{IN}}$$

Fig. 13 - Three-stage CA3001 cascade amplifier using internal capacitors for coupling and frequency-response characteristics.

When the CA3001 is connected as a Schmitt trigger, as shown in Fig. 14, the firing points can be changed by adjustment of the resistor R_2. This resistor value effectively sets the voltage at the input terminal 6 and requires that the input firing voltage at terminal 1 approach this value to obtain trigger action. The hysteresis voltages obtained for various trigger levels in the circuit of Fig. 14 are shown in Table V.

Table V—Performance Data for CA3001 Used as a Schmitt Trigger

Input Firing Volts			
Transition from State 1 to State 2	*Transition from State 2 to State 1*	*Hysteresis Volts*	R_2 *Approximate Setting*
3.0	1.5	1.5	max. resistance
1.1	0.1	1.0	
−1.4	−1.9	0.5	decreasing R_2
−3.2	−3.2	0	

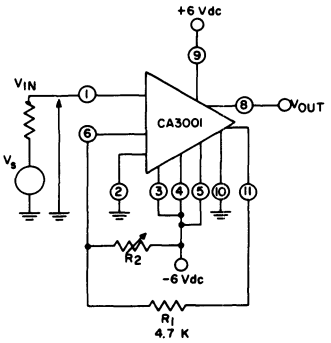


Fig. 14 - CA3001 Schmitt trigger.

Application of the RCA-CA3028A and CA3028B Integrated-Circuit RF Amplifiers in the HF and VHF Ranges

by

H. M. KLEINMAN

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers. Each circuit also contains a constant-current transistor and suitable biasing resistors. The circuits are primarily intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in the following applications:

- RF Amplifier
- Autodyne Converter
- IF Amplifier
- Limiter

In addition to the applications listed above, the CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers. The CA3028B, which features tight control of operating current, input offset voltage, and input bias and offset current, is recommended for those applications in which balance and operating conditions are important.

Useful information concerning operation of the CA3028A and CA3028B in mixers, oscillators, balanced modulators, and similar circuits may be found in ICAN-5022, "Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers." Biasing considerations for the CA3028A and CA3028B differ from the types discussed in ICAN-5022; however, dynamic performance is quite similar to that of the CA3005 and CA3006. ICAN-5022 contains circuits that illustrate operation from dual supplies which, when available, can simplify the biasing of the CA3028A or CA3028B.

Both the CA3028A and CA3028B are supplied in an 8-terminal TO-5 package which assures minimum interlead capacitance and consequently excellent stability in high-frequency circuits. The spacing of the leads on the hermetically sealed package permits installation of the integrated circuits on printed circuit boards by wave-soldering techniques.

Circuit Description

The circuit diagram and terminal connections for the CA3028A and CA3028B are shown in Fig.1. The circuit is basically a single-stage differential amplifier composed of transistors Q_1 and Q_2 driven from a constant-current source Q_3. A single-ended input may be connected to terminal 1 or terminal 5, or push-pull inputs to terminals 1 and 5. Each of these terminals must be provided with a biasing network. Care must be taken to insure that the bias voltages on terminals 1 and 5 are nearly equal when balanced operation is desired. This can only be achieved in practice by using a single voltage divider as shown in Fig.2(a). Bias is first established on the base of one transistor, in this case Q_1, through terminal 1. The base of the second transistor, Q_2 in Fig.2(a), is then connected to the first through a low-valued dc impedance. In Fig.2(a), the inductive winding of the input transformer provides the

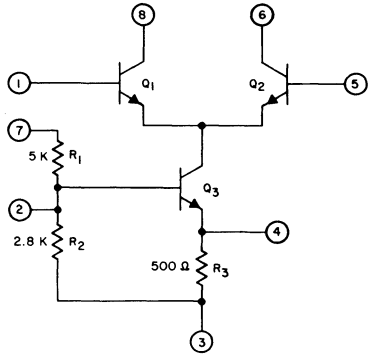


Fig.1 - Schematic diagram and terminal connections for the CA3028A and CA3028B integrated circuits.

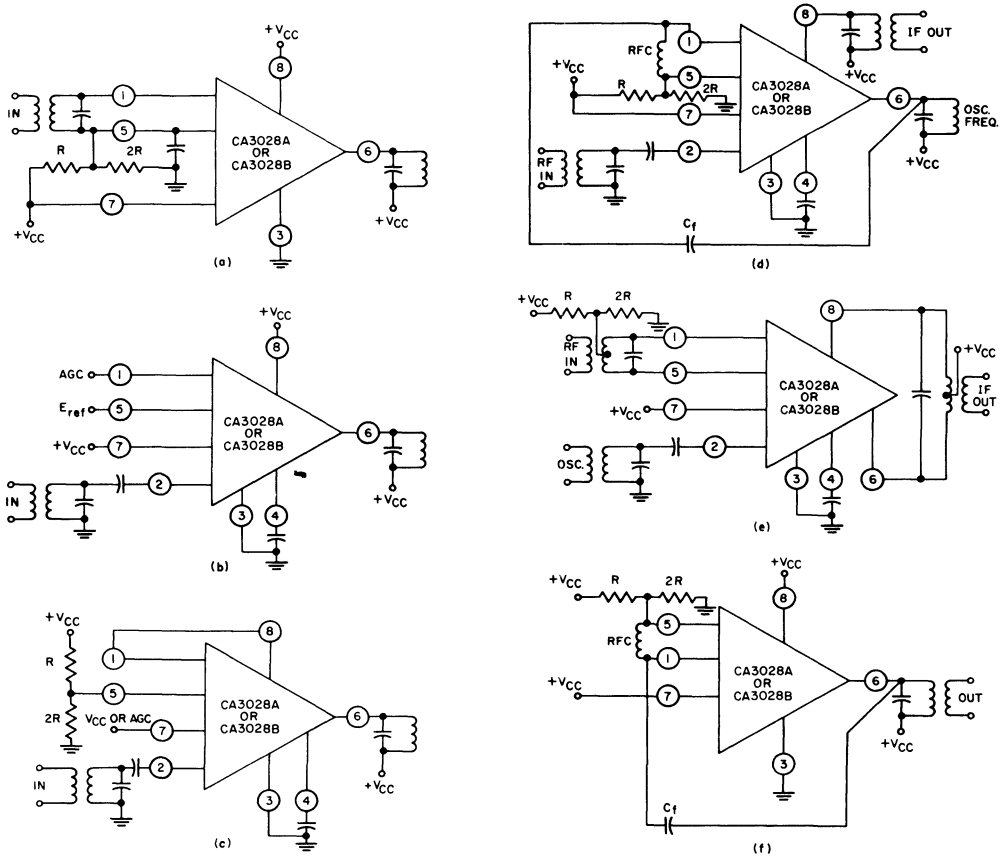


Fig.2 - Connections for the CA3028A and CA3028B for use as (a) a balanced differential amplifier with a controlled constant-current-source drive and agc capability; (b) a cascode amplifier with a constant-impedance agc capability; (c) a cascode amplifier with conventional agc capability; (d) a converter; (e) a mixer; (f) an oscillator.

low-resistance path. An rf choke or low-valued resistor may be used in place of transformer coupling, but caution must be exercised because even as little as 100 ohms may cause serious unbalance in some applications. A single-ended output may be taken from terminal 6 or terminal 8, or push-pull outputs from terminals 6 and 8. In systems with a single power supply of up to 12 volts, terminal 7 is connected to the highest positive potential for maximum gain. Other operating points can be selected by application of a varying bias voltage (agc) to Q_3.

The circuit diagrams in Fig.2 illustrate the flexibility of the CA3028A and CA3028B. Terminal connections are shown for a differential amplifier driven from a controlled constant-current source that has agc capability; a cascode amplifier with constant-impedance or conventional agc capability; a converter; a mixer; and an oscillator. The cascode mode of operation is recommended for applications that require higher gain. The differential mode is preferred when good limiting is required.

Operating Modes

The CA3028A and CA3028B integrated-circuit rf amplifiers can be operated in either the differential mode or the cascode mode. Applications using the differential mode are distinguished by high input impedance, good gain-control characteristics, large input-signal-handling capability, and good limiting.

For ease of design of systems using the CA3028A and CA3028B, admittance or "y" parameters are shown in Fig.3 for the differential mode and in Fig.4 for the cascode mode. It should be noted that the y parameters of the more complex differential and cascode amplifier stages differ from those of simple common-emitter transistor stages.

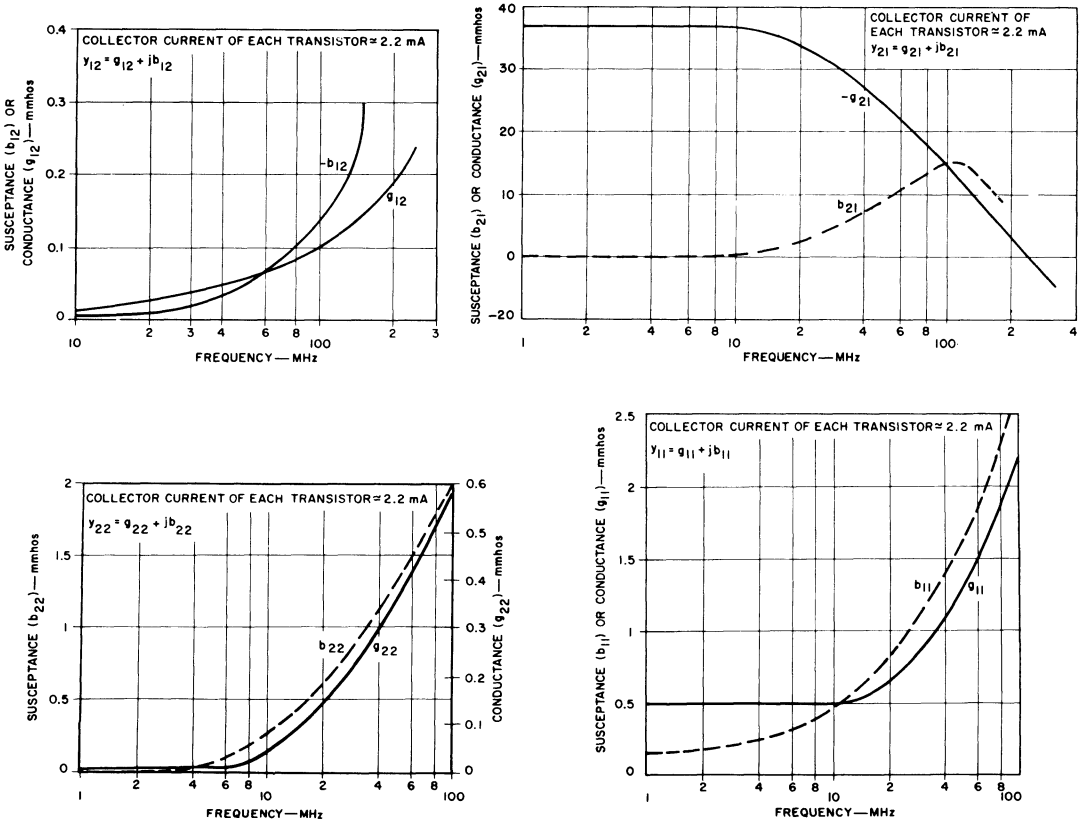


Fig.3 - Y parameters of the CA3028A and CA3028B in the differential-amplifier connection.

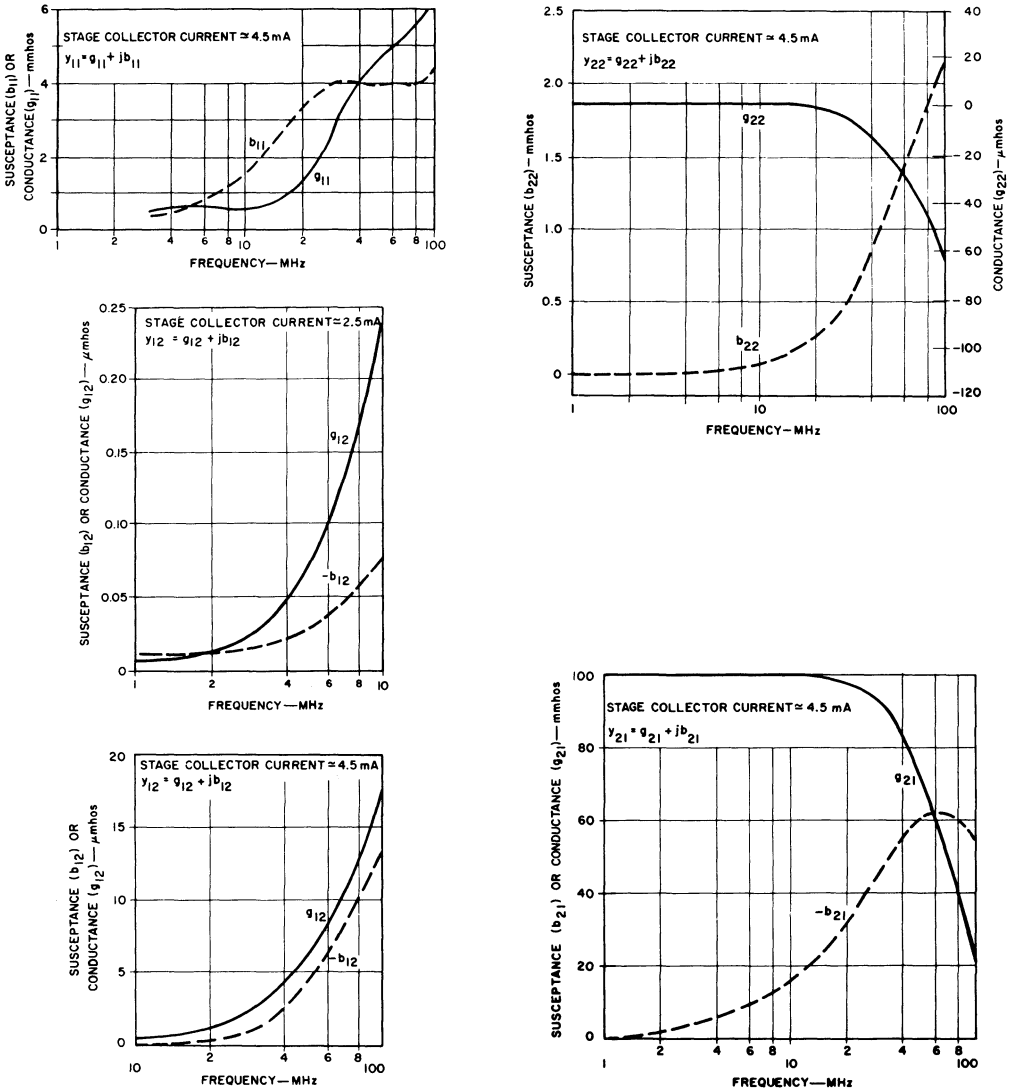


Fig.4 - Y parameters of the CA3028A and CA3028B in the cascode connection.

For quick reference, values for input and output parallel RC networks and transconductance values are listed in Table I for the differential amplifier and in Table II for the cascode amplifier.

Although the reverse transfer admittance y_{12} of the CA3028A or CA3028B is low for either cascode or differential operation, circuit-layout-induced instability can occur in high-gain amplifiers. Circuit layout is of paramount importance in both modes because undesirable coupling admittances can be much greater than the CA3028A or CA3028B admittances. Attention to layout and shielding is imperative if proper advantage is to be taken of the low feedback of the CA3028A and CA3028B.

Table I Input and Output Parallel RC Network Component Values, Transconductance Values, and Performance Data for the CA3028A and CA3028B Integrated Circuits in the Differential Amplifier.

Frequency	Input Parallel RC Network		Output Parallel RC Network		Transconductance
(MHz)	R_{in} (ohms)	C_{in} (pF)	R_{out} (ohms)	C_{out} (pF)	g_m (millimhos)
10.7	1800	8	2.2×10^4	4	35
100	500	4.5	1.8×10^3	4	15

Table II Input and Output Parallel RC Network Component Values, Transconductance Values, and Performance Data for the CA3028A and CA3028B Integrated Circuit Cascode Amplifier.

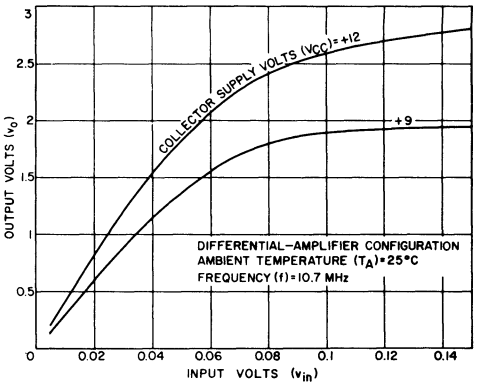
Frequency	Input Parallel RC Network		Output Parallel RC Network		Transconductance
(MHz)	R_{in} (ohms)	C_{in} (pF)	R_{out} (ohms)	C_{out} (pF)	g_m (millimhos)
10.7	900	22	-1.67×10^6	3.1	100
100	170	6.3	-5×10^5	3.5	14

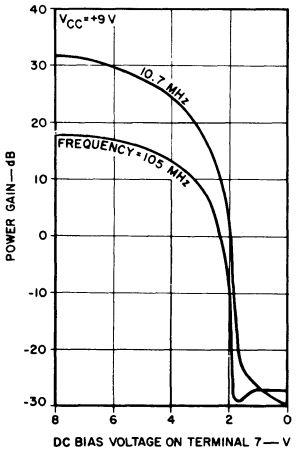
Differential Amplifier

The differential amplifier shown in Fig.2(a) is designed for operation at 10.7 MHz and 100 MHz. Because the amplifier consists essentially of a common-collector stage driving a common-base stage, the input admittance y_{11}, the output admittance y_{22}, and the forward transfer admittance y_{21} are decreased by a factor of two. The reverse transfer admittance y_{12} is typically 140 times lower than that of a single common-emitter transistor at 10.7 MHz, and 10 times lower at 100 MHz. As a result, the CA3028A and CA3028B can be aligned easily in if strips without need for neutralization.

The transfer characteristic in Fig.5(a) shows the excellent limiting capabilities of the CA3028A and CA3028B differential amplifiers. This limiting performance is achieved because the constant-current transistor Q_3 limits the circuit operating current so that the collectors of the differential-pair transistors Q_1 and Q_2 do not saturate. Table III shows the maximum permissible load resistances for non-saturating operation when single supply voltages of 9 and 12 volts are used.

When linear operation over a wide input-voltage range is imperative, agc voltage may be applied to the constant-current source Q_3 at terminal 7. Gain-control





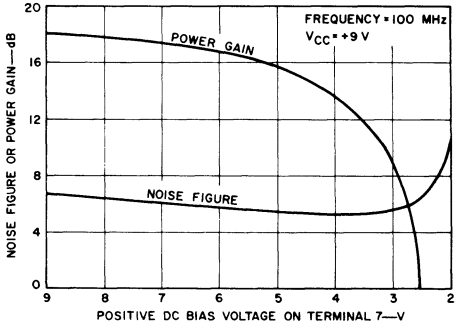


Fig.5 - Characteristics of the CA3028A and CA3028B in the differential-amplifier connection: (a) 10.7-MHz transfer characteristics; (b) agc capabilities; (c) power gain as a function of noise figure.

Table III Maximum Load Resistance Permissible for Non-Saturating Operation with +9 and +12 volt Single-Supply Voltages

V_{CC} (volts)	$I_{C1} + I_{C2}$ (milliamperes)	Maximum Tuned Load (ohms)	Maximum Resistive Load (ohms)
+9	5.0	3.6 K	1.8 K
+12	6.8	3.5 K	1.7 K

$R_L = V_{CC}/I_{C1} + I_{C2}$ Resistive Load

$R_L = 2\ V_{CC}/I_{C1} + I_{C2}$ Tuned Load

capabilities are -60 dB at 10.7 MHz and -46 dB at 100 MHz, as shown in Fig.5(b). Fig.5(c) shows curves of power gain and noise figure as a function of agc voltage. The combination of an optimum noise figure of 5.5 dB and a power gain of 15 dB at 100 MHz makes this circuit suitable for use as an rf amplifier in the commercial FM band.

Cascode Amplifier

When the CA3028A or CA3028B is used in the cascode configuration for rf-amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance y_{11} is essentially that of a common-emitter stage, and the forward transfer admittance y_{21} is that of a common-emitter stage times the common-base alpha. Because of the high-impedance drive source for the common-base stage, the output admittance y_{22} is quite low at low frequencies (0.6 μmho). The reverse transfer admittance y_{12} for the cascode circuit is 900 times less than that for a single-stage common-emitter at 10.7 MHz, and 35 times less at 100 MHz. As in the differential amplifier, ease in tuning is obtained without need for neutralization.

The transfer characteristic in Fig.6 shows the suitability of the cascode configuration for agc take-off for FM front-end controls.

Applications

The typical applications described below illustrate the use of the CA3028A and CA3028B integrated-circuit rf amplifiers in both the differential and the cascode modes.

10.7-MHz Cascode IF Amplifier. Fig.7 shows an FM if strip in which the CA3028A or CA3028B is used in a high-gain, high-performance cascode configuration in conjunction with a CA3012 integrated-circuit wide-band amplifier. The CA3012 is used in the last stage because of the high gain of 74 dB input to the 400-ohm-load ratio-detector transformer T_4. An input of approximately 400 microvolts is required at the base of the

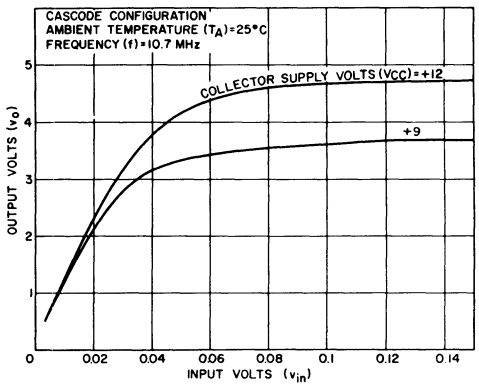


Fig.6 - 10.7-MHz transfer characteristics of the CA3028A and CA3028B in the cascode connection.

CA3012 for -3 dB below full limiting. An impedance-transfer device and filter must be connected between the CA3012 base (terminal 1) and the output of the CA3028A or CA3028B (terminal 6). The insertion loss of this filter should be kept near 6 dB (1:2 ratio of loaded to unloaded Q) so that all possible gain can be realized up to the CA3012 base. In addition to this insertion loss, a voltage step-down loss of 5.8 dB in the interstage filter is unavoidable. Therefore, the total voltage loss is approximately 9 to 14 dB, and an output of 1500 to 2000 microvolts must be available from the CA3028A or CA3028B to provide the required 400-microvolt input to the CA3012.

The voltage gain of the CA3028A or CA3028B into a 3000-ohm load is determined as follows:

$$VG = \frac{-y_{21}}{y_{22} + y_L} = \frac{100 \times 10^{-3}}{0.33 \times 10^{-3}} = 300 = 49\ dB$$

This calculation indicated a sensitivity of 6.6 microvolts at the CA3028A or CA3028B base (terminal 2). This value cannot be realized, however, because the CA3012 limits on noise peaks so that the gain figure is reduced.

A sensitivity of 7.5 microvolts was realized in the design shown in Fig.7. The filter approach with high-gain integrated-circuit chips differs from that for single, cascaded transistor stages in that lumped selectivity is required rather than distributed selectivity.

Special care must be exercised when second-channel attenuation in the order of 45 dB is required. Selectivity is then proportioned as follows:

Interstage filter: double-tuned 220 kHz at -3 dB; coefficient of critical coupling, 0.7; voltage loss, 8 dB

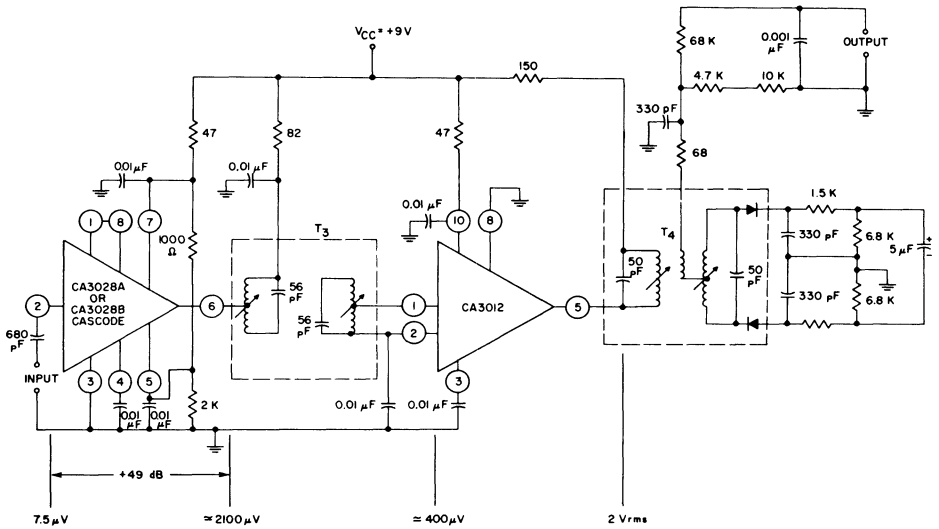
Converter filter: triple-tuned, 220 kHz at -3 dB; coefficient of critical coupling, 0.8; voltage loss, about 28 dB

Because of input limiting in the CA3012, the interstage filter exhibits a somewhat wider bandwidth than the 220 kHz indicated. Therefore, a coefficient of critical coupling near 0.8 is realized, which is optimum for minimum deviation from constant time delay. The triple-tuned converter filter alone provides second-channel attenuation of 30 to 33 dB, while the interstage filter contributes 8 to 10 dB. The filters described meet requirements of both performance and economy.

The large collector swing that can be obtained in cascode operation of the CA3028A or CA3028B makes it desirable to take the agc voltage from the collector or "hot" end of the iftransformer for front-end gain control. The cascode stage then operates primarily in its linear region, and excellent selectivity (40 dB) is maintained even for large signal inputs of approximately 0.4 volt. Front-end gain reduction is between 40 and 50 dB.

10.7-MHz IF Strip Using Two CA3028A or CA3028B Circuits. The 10.7-MHz if strip shown in Fig.8 uses two CA3028A or CA3028B integrated circuits to provide less over-all gain than the circuit of Fig.7. The first integrated circuit is connected as a cascode amplifier and yields voltage gain of 50 dB; the second integrated circuit is connected as a differential amplifier and yields voltage gain of 42 dB.

When a practical interstage transformer having a voltage insertion loss of 9 dB is used, over-all gain is 83 dB and the sensitivity at the base of the first integrated circuit is 140 microvolts. A less sophisticated converter filter (double-tuned) could be employed at the expense of about 26 dB of second-channel attenuation. If the voltage insertion loss of the converter filter is assumed to be 18 dB and the front-end voltage gain (antenna to mixer collector) is 50 dB, this receiver would have an IHFM* sensitivity of approximately 8 microvolts.



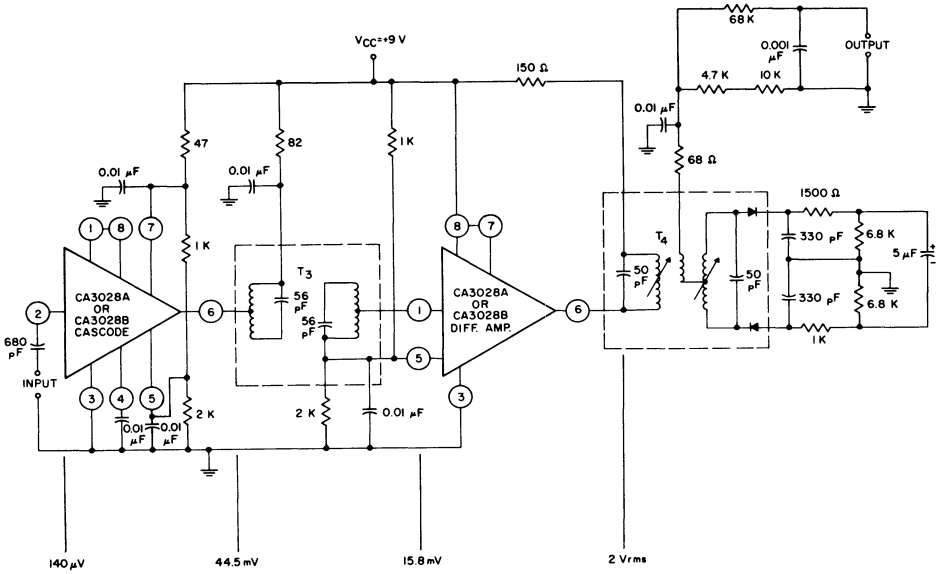
T_3: Interstage transformer TRW #22486 or equiv.

T_4: Ratio detector TRW #22516 or equiv.

Audio Output: 155 mV rms for 7.5 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig.7 - 10.7-MHz if amplifier using a CA3028A or CA3028B in the cascode mode.

* Institute of High-Fidelity Manufacturers.



T_3: Interstage transformer TRW #22486 or equiv.

T_4: Ratio detector TRW #22516 or equiv.

Audio Output: 155 mV rms for 140 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig.8 - 10.7-MHz if strip using two CA3028A or CA3028B integrated circuits.

10.7-MHz Differential-Amplifier IF Strip. Fig.9 shows a 10.7-MHz medium-gain if strip consisting of a CA3028A or CA3028B connected as a differential amplifier and a CA3012 wide-band amplifier. As in the circuit shown in Fig.7, an input of approximately 1500 microvolts is required to the interstage filter. The differential-mode voltage gain of the CA3028A or CA3028B into a 3000-ohm load is determined as follows:

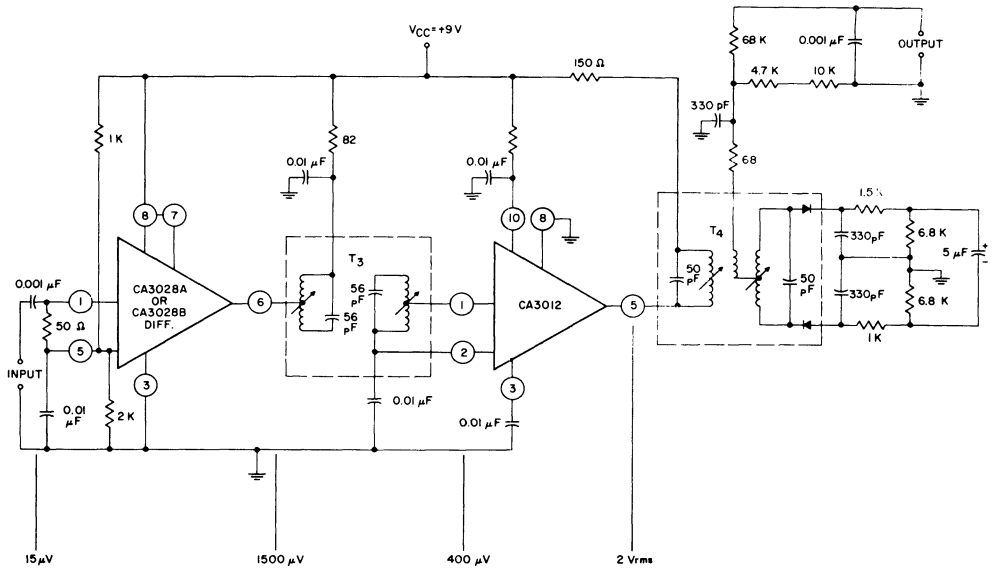
$$VG = \frac{-y_{21}}{y_{22} + y_L} = \frac{35 \times 10^{-3}}{0.38 \times 10^{-3}} = 92.5 = 39.3 \text{ dB}$$

This voltage gain requires that an input of approximately 15 microvolts be available at the base of the CA3028A or CA3028B differential amplifier.

Even if a triple-tuned filter having a voltage insertion loss of 28 dB is used in a low-gain front end, a receiver having an IHFM sensitivity of 5 microvolts results. If 26 dB second-channel attenuation is permissible, a 3-microvolt-sensitivity IHFM receiver can be realized.

88-MHz-to-108-MHz FM Front End. Fig.10 illustrates the use of the CA3028A or CA3028B as an rf amplifier and a converter in an 88-to-108-MHz FM front end. For best noise performance, the differential mode is used and the base of the constant-current source Q_3 is biased for a power gain of 15 dB. The rf amplifier input circuit is adjusted for an insertion loss of 2 dB to keep the noise figure of the front end low. Because the insertion loss of the input transformer adds directly to the integrated-circuit noise figure of 5.5 dB, the noise figure for the front end alone is 7.5 dB, as compared to noise figures of about 6 dB for commercial FM tuners.

Although a single-tuned circuit is shown between the collector of the rf-amplifier stage and the base of the converter stage, a double-tuned circuit is preferred to reduce spurious response of the converter. If the double-tuned circuit is critically coupled for the same 3-dB bandwidth as the single-tuned circuit, the insertion loss remains the same.



T_3: Interstage transformer TRW #22486 or equiv.

T_4: Ratio detector TRW #22516 or equiv.

Audio output: 155 mV rms for 15 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig.9 - 10.7-MHz if strip using a CA3028A or CA3028B in the differential mode.

The collector of the rf stage is tapped down on the interstage coil at approximately 1500 ohms, and the base of the converter stage at 150 ohms. RF voltage gain is computed as follows:

Antenna to base	0 dB
Base to collector	22 dB
Voltage insertion loss of interstage coil	-13 dB
Net rf voltage gain	9 dB

If an if converter transformer having an impedance of 10,000 ohms is used, the calculated voltage conversion gain is

$$VG_c = \frac{-y_{21}}{y_{22} + y_L} = 112 = 41.3 \text{ dB}$$

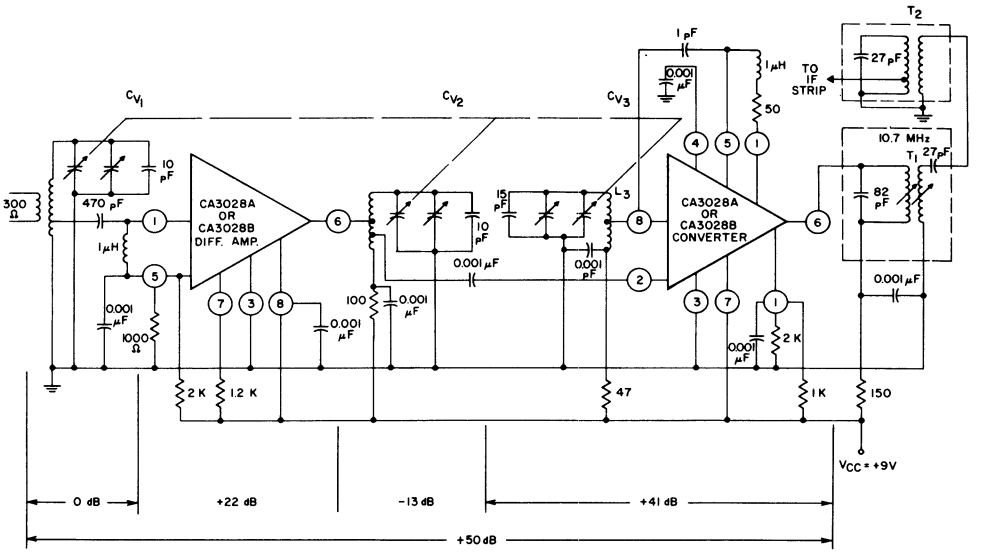
Measured gain into the collector of the converter is 42 dB. The measured voltage gain of the rf amplifier and converter into a 10,000-ohm load is 52 dB; calculated gain is 50 dB. When the converter is tuned for the commercial FM band (88 to 108 MHz), the following parameters apply:

Input resistance R_{in}	170	ohms
Input capacitance C_{in}	6.3	pF
Output resistance R_{out}	80K	ohms
Output capacitance C_{out}	3.5	pF
Conversion transconductance	13	mmhos

The rf amplifier and converter shown in Fig.10 were combined with the if amplifier shown in Fig.7, and the following performance data were measured at 100 MHz:

30-dB (S + N)/N IHFM Sensitivity	3 μV
Image Rejection	46 dB

Receiver noise figure is the limiting factor that permits a sensitivity of only 3 microvolts to be realized.



L_1: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 1-3/4 T; primary — 2 turns #30 SE.

L_2: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 6 2-1/4 T, A 3/4 T.

C_{V1-2}: variable $\Delta C \approx 15$ pF

T_1: Mixer transformer TRW #22484 or equiv.

T_2: Input transformer TRW #22485 or equiv.

L_3: 3-1/2 T #18 tinned copper wire; winding length 5/16" on 9/32" form.

C_{V1-3}: variable, $\Delta C \approx 15$ pF.

Fig. 10 - 88-MHz-to-108-MHz FM front end.

Application of the RCA CA3021, CA3022, and CA3023 Integrated-Circuit Wideband Amplifiers

BY

G.E. THERIAULT, T. H. CAMPBELL, AND A. J. LEIDICH

The RCA-CA3021, CA3022, and CA3023 integrated circuits are multi-purpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. These circuits feature monolithic-silicon construction, and are usable throughout the temperature range from -55°C to 125°C. They are supplied in a 12-terminal TO-5 package.

The CA3021, CA3022, and CA3023 have the same circuit configuration and the same mid-band open-loop gain. However, different resistor values are used in the three circuits to provide different values of power dissipation and open-loop bandwidth. Typical power dissipation with a 6-volt supply is 3 milliwatts for the CA3021, 12 milliwatts for the CA3022, and 36 milliwatts for the CA3023. Wider bandwidths can be achieved with the CA3023, intermediate bandwidths with the CA3022, and narrower bandwidths with the CA3021.

The major feature of these circuits is a flexibility that permits their use in the following applications: video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired. The areas of circuit flexibility are as follows:

- Operation with dc supplies of 4.5 to 12 volts.
- Automatic-gain-control capability (60-dB agc range with large input-signal-handling capability).
- Limiting capability (by connection of diodes provided on the chip).
- Gain adjustment (by addition of external feedback resistor or network to obtain desired operating gain and bandwidth).

Circuit Description

The circuit diagram for the CA3021, CA3022, and CA3023 is shown in Fig. 1. Amplifier gain is obtained by use of transistors Q_1, Q_3, Q_4, and Q_6, which are connected as two dc-coupled common-emitter/common-collector amplifiers having a voltage gain of approximately 60 dB. The

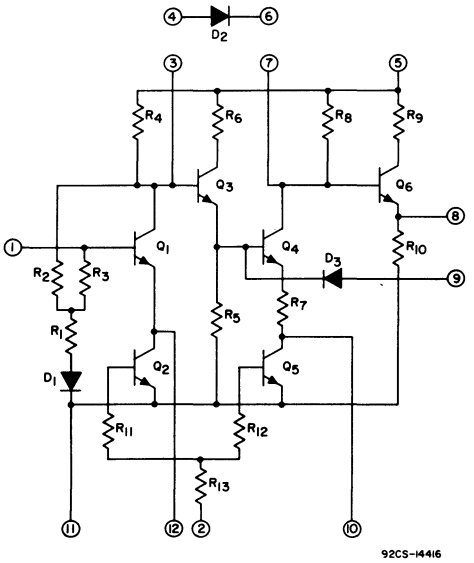


Fig. 1 - Circuit diagram and TO-5 terminal connections for the CA3021, CA3022, and CA3023 integrated circuits.

common-collector configuration provides the necessary impedance transformation (high-impedance input and low-impedance output) for wide bandwidth. The output transistor Q_6 provides the low output impedance desired for iterative operation. The circuit must be capacitively coupled, and should have a low-impedance source. A source resistance of 50 ohms was used for the circuit measurements given in this Note.

Fig. 2 shows typical connections for the CA3021, CA3022, and CA3023 for wideband and bandpass applications with and without agc, and for limiter applications. An external feedback resistor R_f or a tuned circuit can be added between terminals 3 and 7 for desired bandwidth and gain performance. Linear operating conditions are maintained by the bias applied between the collector and the base of Q_1 by the resistor-diode network R_2, R_3, R_1, D_1. Because the collector of Q_1 is held at a fixed potential that is relatively independent of supply, device characteristics, and temperature, dc coupling to the remainder of the circuit can be used.

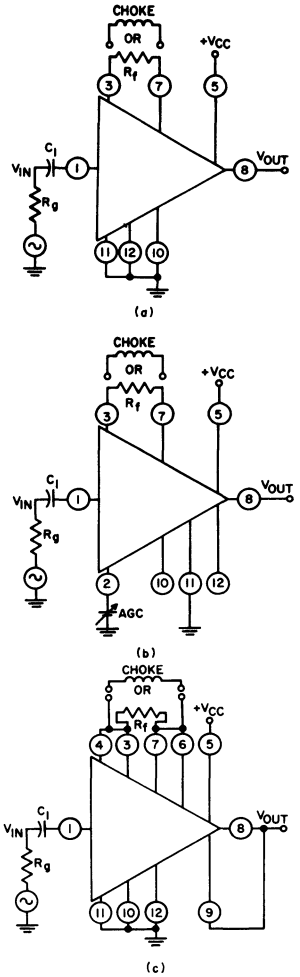


Fig. 2 - Typical connections for the CA3021, CA3022, and CA3023 for (a) wideband and bandpass applications, (b) wideband and bandpass applications requiring agc, and (c) limiter applications.

For applications in which gain control is desired, terminals 10 and 12 are left floating and agc is applied to terminal 2, as shown in Fig. 2b. For maximum gain, terminal 2 is operated at a positive voltage not larger than the supply voltage applied to terminal 5. In the positive voltage condition, transistors Q_2 and Q_5 are saturated and the impedance in the emitters of Q_1 and Q_4 is low. When the gain-control voltage becomes negative, Q_2 and Q_5 come out of saturation and provide high degenerative emitter resistance which reduces the gain. Because most of the increasing signals appear across the increasing degenerative resistance, the active gain transistors Q_1, Q_3, Q_4, and Q_6 handle only a small part of the large signal. As a result, signal-handling capability increases with increasing agc. Further increases of gain-control voltage reduce the current in Q_1 and Q_4 and thus provide the additional gain control needed to achieve maximum agc range.

In limiting applications, diodes D_2 and D_3 are connected in the feedback loops, as shown in Fig. 2c (terminals 4 to 3, 6 to 7, and 8 to 9). The diodes provide clamping for sufficient input-signal swing; limiting can be achieved with input-signal swings up to 2.5 volts rms.

Operating Characteristics

DC Supply Considerations. The most positive voltage to be applied to the CA3021, CA3022, and CA3023 integrated circuits is connected to terminal 5. The most negative voltage is connected to the substrate through terminal 11.

The circuits can be used with single power supplies of 4.5 to 12 volts. The bias technique used for transistor Q_1, and thus for the remainder of the circuit, makes the collector operating voltage of Q_1 and Q_4 relatively independent of the supply. Consequently, the current in the circuit increases almost linearly as a function of supply voltage. Fig. 3 shows typical power dissipation for the three circuits as a function of supply voltage. Because there is little change in the collector voltage of Q_4, there is little change in output operating point as a function of supply voltage.

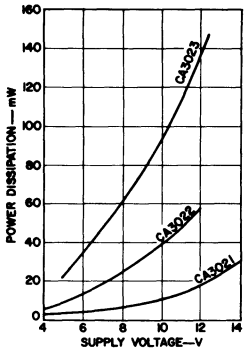


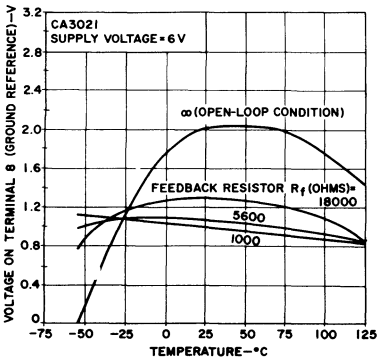
Fig. 3 - Power dissipation as a function of supply voltage.

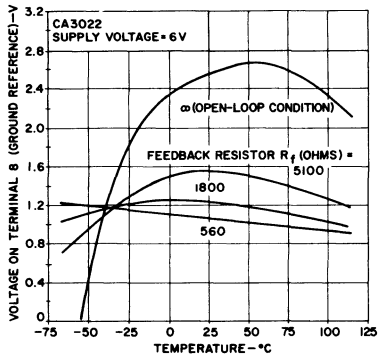
DC Stability with Temperature. The output operating points of the CA3021, CA3022, and CA3023 are shown in Fig. 4 as a function of temperature and feedback resistance. As a result of the resistor values used in each circuit, the output operating point is compensated in the temperature range between -20°C and 75°C when the circuit is operated under open-loop conditions (terminals 3 and 7 floating). Insertion of a feedback resistor between terminals 3 and 7 is recommended to minimize degradation in performance at temperatures outside this range. The maximum value of the feedback resistor R_f recommended for optimum performance of each circuit is shown in the following table:

Circuit	R_f - ohms
CA3021	18000
CA3022	5100
CA3023	2000

Use of a feedback resistor of the maximum value provides equal ac and dc feedback, but reduces the usable gain of the circuit to approximately 40 dB. When equal ac and dc feedback is not desired, as in the case of bandpass or tuned responses, a choke or tuned circuit can be included between the feedback terminals 3 and 7 to provide dc temperature stability and permit gains of 50 to 55 dB.

As a general rule, feedback should be included in all applications in which operation over an extended temperature range is required.





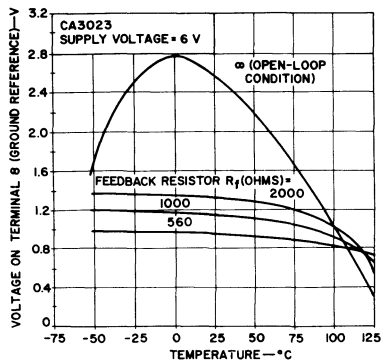


Fig. 4 - Output operating point as a function of temperature for various values of feedback resistance.

DC Considerations for Gain Control. When the agc transistors Q_2 and Q_5 are included in the circuit, the output operating point can be held constant only by addition of feedback. Variation of operating point is caused by the added collector-to-emitter voltage of Q_2 and Q_5 in saturation in the emitters of Q_1 and Q_4. The effect is more pronounced in the higher-current circuits, CA3022 and CA3023. As discussed previously, full dc feedback can be used to stabilize the operating point; ac feedback can be removed by the use of tuned circuits. The maximum recommended values of R_f provide satisfactory stability when the circuit is connected for agc.

DC Considerations for Limiting. In limiter applications, diodes D_2 and D_3 are included in the feedback loops in the circuit (external connections are made as shown in Fig. 2c). Under open-loop conditions, the dc operating point may be such that D_2 and D_3 (usually D_3) are turned on. The gain is then reduced and the amplifier will not operate linearly at low levels. The values of R_f recommended previously also assure correct operation for limiting amplifiers.

AC Frequency Response and Gain Performance. Open-loop frequency responses for the CA3021, CA3022, and CA3023 are given in Fig. 5. The curves also show the response characteristics to the 3-dB point for various values of feedback resistance. Values of feedback resistance larger than those recommended for operating-point temperature stability are included to indicate gain performance at resonance when tuned circuits or chokes are used in the feedback loop. For these measurements, the circuits were operated with a 50-ohm source and a high impedance load.

Fig. 6 shows the variation of gain with temperature for the three circuits. Each circuit was operated with sufficient feedback to provide a closed-loop gain of approximately 40 dB. The gain variation is practically independent of feedback, and is slightly greater for the CA3023 than for the other two circuits. Fig. 7 shows typical upper-3-dB frequency shifts with temperature for the three circuits for a gain of approximately 40 dB.

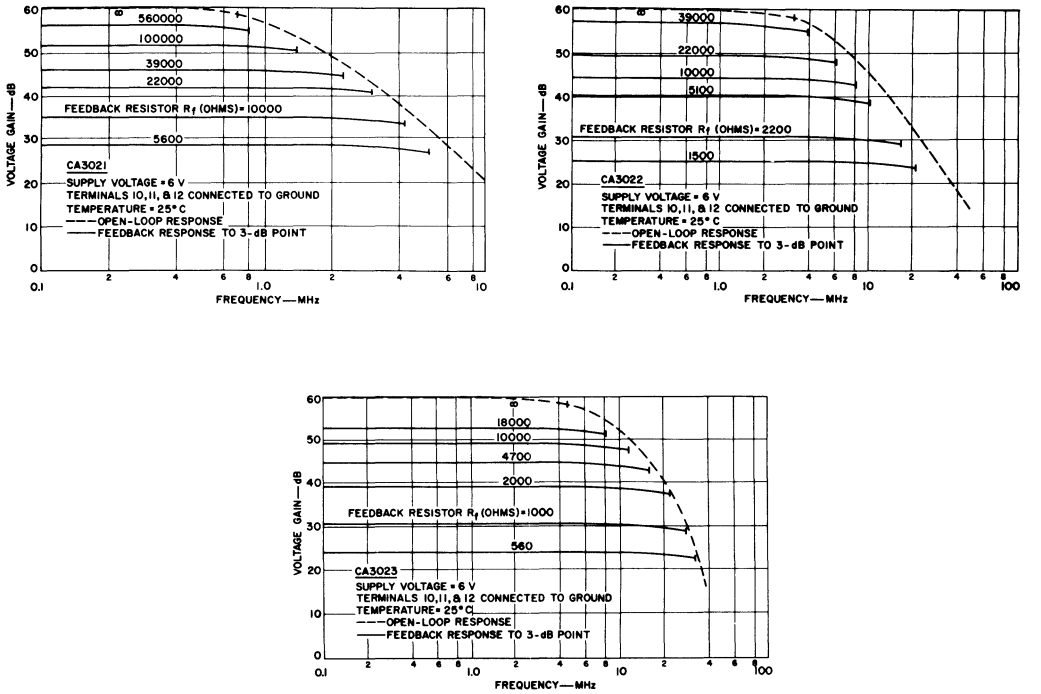


Fig. 5 - Frequency-response characteristics.

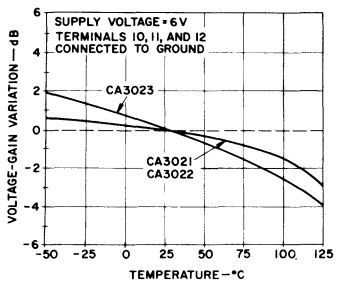


Fig. 6 - Voltage-gain variation with temperature (feedback adjusted to provide gain of approximately 40 dB at 25°C).

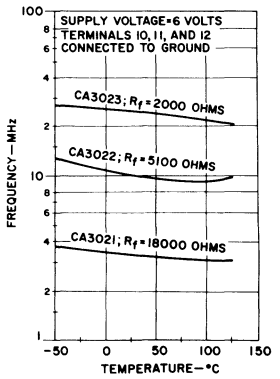


Fig. 7 - Upper-3-dB frequency shift with temperature.

In buffer-amplifier applications, reverse feedback or isolation capability is required. The following table shows the isolation performance of the CA3021, CA3022, and CA3023 at three frequency levels with the input terminated in 50 ohms.

Circuit	Feedback Resistor R_f (ohms)	Voltage Injected at Output (volts rms)	Resultant Feedthrough Input Voltage Below the Applied Output Voltage (dB)		
			f = 1 MHz	f = 10 MHz	f = 50 MHz
CA3021	18000	2	66	66	54
CA3022	5000	2	66	66	54
CA3023	2000	2	66	66	52

AC Signal Power Output. The maximum power-output capability of the common-collector output transistor Q_6 in Fig.1 occurs for a load-resistance value higher than the output impedance. For determination of optimum load-resistor values, each circuit was operated from a 6-volt supply at a gain of approximately 40 dB with a variable resistor capacitively coupled to terminal 8. The variation of maximum linear signal output as a function of load resistance is shown in Fig.8.

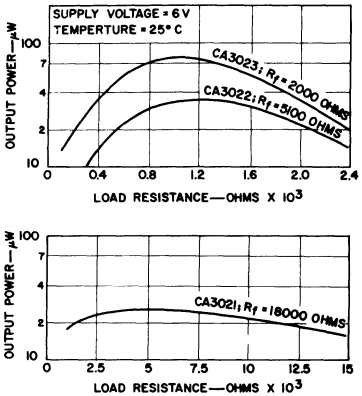


Fig.8 - Maximum linear signal output as a function of load resistance.

Maximum power output was measured at a level at which output distortion was just discernible on an oscilloscope.

Tuned Circuit in the Feedback Loop. When a parallel tuned circuit is included in the feedback path between terminals 3 and 7 of the CA3021, CA3022, or CA3023, the gain at resonance is a function of the equivalent resistance of the feedback loop. Gain characteristics of the three circuits as a function of feedback resistance are shown in Fig.9. For each circuit, there is a value of feedback

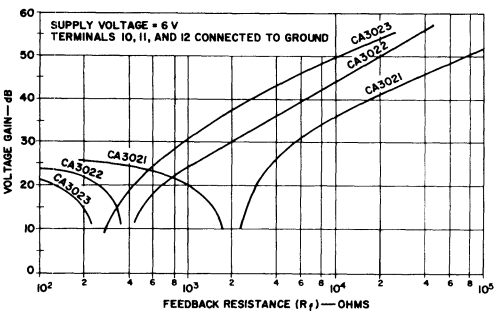


Fig.9 - Voltage gain as a function of feedback resistance.

resistance R_f for which the gain approaches zero. This condition occurs when the small-signal transconductance g_m of the transistor Q_4 is equal to the conductance of the parallel tuned circuit; signal cancellation then results at terminal 7. In a tuned circuit designed with the correct feedback resistance R_f, therefore, zero gain can be obtained at the resonant frequency. The resistance values required for signal cancellation are 2000 ohms for the CA3021, 400 ohms for the CA3022, and 230 ohms for the CA3023. When the tuned-circuit impedance is made equal to these cancellation resistance values at resonance, the gain increases

at frequencies off resonance and a trapping effect results. For zero feedback resistance, the gain of each circuit is approximately 24 dB. For values of feedback resistance in excess of the cancellation resistance, the gain increases. When the tuned circuit has a resonant impedance higher than the cancellation resistance, the response is added to the video response characteristic, as shown in Fig.10. Then, because no

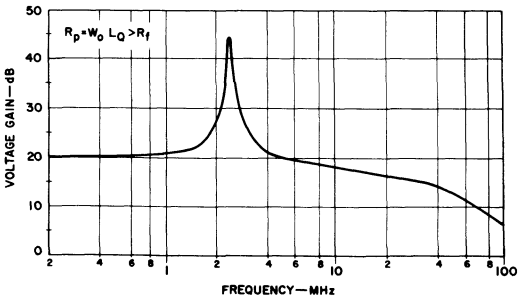


Fig. 10 - Voltage gain as a function of frequency in a bandpass amplifier when the tuned-circuit resonant impedance R_p is higher than the cancellation resistance R_{fc}.

purely resistive value occurs that is equal to the cancellation resistance, no cancellation occurs.

The bandwidth of the response can be approximated by determining the total loading of R_p on the parallel tuned circuit in the feedback path, as follows:

$$R_p = \frac{R_T R_X (R_4+R_8)}{(R_X+R_T)(R_4+R_8)+R_X R_T}$$

where R_T is the resistance at resonance of the unloaded Q, R_X is the resistance added to the tuned circuit for adjustment of gain, and $(R_4 + R_8)$ is the series combination of the two common-collector load resistors. The 3-dB bandwidth for the response is given by

$$\frac{f_o}{\Delta f} = \frac{R_P}{X_L} = \frac{R_P}{X_C} = Q_L$$

Typical values for $(R_4 + R_8)$ for the three circuits are 39000 ohms for the CA3021, 10900 ohms for the CA3022, and 4800 ohms for the CA3023.

Output Tuned Circuits. The curves of Fig.8 indicate that capacitive coupling of the common-collector output transistor Q_6 to a matched load severely limits the transistor output-voltage-swing capability. If the required mismatch is achieved by ac coupling of a tuned circuit directly across the output, the tuned circuit will be loaded by the low output impedance of the common-collector transistor. However, comparable output power can be obtained by use of a resistor in series with the circuit output and the tuned circuit. This arrangement provides a load for the common-collector transistor for frequencies off resonance of the tuned circuit, and prevents the possibility of reactive loads causing emitter-follower transistor instability.

Gain Control. The CA3021, CA3022, and CA3023 are connected as shown in Fig.2b when gain-control application is desired. Transistors Q_2 and Q_5 are then included in the emitter-signal path of transistors Q_1 and Q_4, respectively. For maximum gain, a positive voltage is applied to terminal 2 which saturates transistors Q_2 and Q_5. If a voltage of 6 volts is applied to terminal 2, the typical gain-control current is 0.8 milliampere. The gain-control action is provided by reduction of the voltage on terminal 2. The decreasing voltage causes transistors Q_2 and Q_5 to come out of saturation and present a high impedance in the emitter leads of transistors Q_1 and Q_4. It is important that good filtering and isolation be maintained at the agc terminal 2 because transistors Q_2 and Q_5 are in the linear active region for a portion of the agc range and can, therefore, provide gain for a signal on the agc terminal.

The minimum gain is determined by a combination of the gain of Q_1 and feedthrough to the collector of Q_1 along a resistance path made up of R_3 and R_2. Because the signals are out of phase, there is a point at which cancellation of signal results. This cancellation occurs in all three circuits when terminal 2 is 0.5 volt more negative than terminal 11.

It is accompanied by severe distortion of signal and AM modulation. Techniques for obtaining agc without reaching the cancellation point are discussed later.

When the maximum recommended feedback resistance for operating-point stability is used in the connection of Fig.2b, maximum gain is reduced because of the extra emitter resistance presented by the saturation resistance of transistors Q_2 and Q_5. Maximum voltage gain for each circuit is approximately 30 dB with the maximum recommended feedback resistance and a 6-volt supply. The typical agc range for each circuit is 55 dB with resistive feedback.

When a tuned circuit is used in the feedback loop, higher maximum gain can be obtained in the agc connection shown in Fig.2b. The maximum gain obtainable is approximately 50 dB when high feedback impedance is maintained. A self-resonant choke is a convenient element to add in the feedback loop to obtain high impedance because it provides wide bandwidth; resistance loading can be added to adjust the gain to the desired value. When a combination of self-resonant choke and added resistance is used, dc feedback is complete and the operating point is temperature-stable. Wide-bandwidth tuned circuits are suggested for all three circuits, but especially for the CA3022 and CA3023 because the bandwidth shifts with gain control, as shown in Fig.11. For a tuned frequency of 3 MHz at full gain,

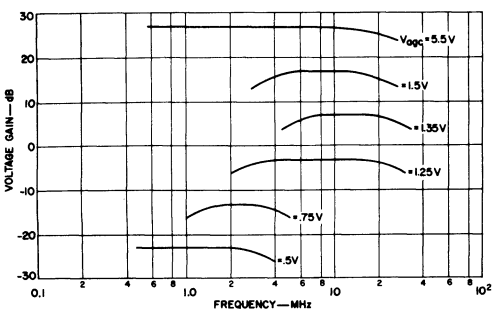


Fig.11 - Effect of gain control on response characteristics.

for example, the resonance point of the tuned response increases slightly (about 5 per cent) for gain control of -20 to -30 dB because of the combination of the low-frequency roll-off and the tuned response. In the region of gain control of -50 dB, the high-frequency roll-off affects the response and the resonant frequency decreases below 3 MHz (by about 10 per cent). At full agc the tuned circuit becomes a trap in the feedthrough path, minimum gain is achieved at the 3-MHz frequency, and the response is inverted, i.e., a notch occurs where a bandpass had existed. When tuned circuits are included in the feedback path of the gain-controlled amplifier, therefore, it is recommended that the bandwidth be chosen as wide as possible to minimize detuning effects. Desired bandwidth control should be obtained at the input, at the output, or in the feedback path of stages without gain control.

The use of emitter degeneration as a gain-control technique improves signal-handling capability. At full gain control, signals as high as 2 volts rms can be handled without the occurrence of serious overload distortion. Typical cross-modulation characteristics for the CA3021, CA3022, and CA3023 with only feedback resistance in the feedback loop are shown in Fig.12. Maximum gain for each circuit

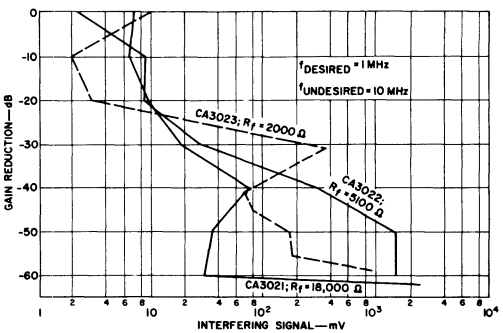


Fig.12 - Cross-modulation distortion characteristics.

was approximately 30 dB. When a tuned circuit is used in the feedback loop, more gain-control range is available as a result of the feedthrough reduction. Depending on the impedance of the tuned circuit, the gain-control range is between 60 and 80 dB. The cross-modulation characteristics when tuned circuits are

used are similar to those obtained with resistive feedback except for modifications caused by different feedback characteristics of interfering signals outside the tuned-circuit passband.

Limiting. For applications in which signal limiting is required, the diodes of the CA3021, CA3022, and CA3023 are connected as shown in Fig. 2c. At low signal levels, the diodes are cut off and the gain performance is similar to that described previously except for some bandwidth reduction caused by the inherent capacitance of the diodes. For large input-signal swings in the negative direction, the collector of transistor Q_1 becomes positive and the collector of transistor Q_4 becomes negative, and diode D_2 begins to conduct. This action clamps the collector of Q_1 to the collector of Q_4 and, because the diode is in the feedback path, reduces the gain. For positive swings at the input, the collector of transistor Q_1 becomes negative and the output at terminal 8 becomes positive. Two effects tend to limit input signals of positive polarity: transistor Q_4 going to cutoff, and diode D_3 going into conduction. When the circuits are connected as shown in Fig. 2c, limiting is symmetrical at the onset. With increased signal, however, the symmetry is not perfectly preserved because of dc shift in the circuit. Typical output-signal characteristics as a function of input level are shown in Fig. 13. The lack of symmetry at high input levels causes a decrease in power output, as shown in the waveforms.

Limiting characteristics for the CA3021, CA3022, and CA3023 were measured in the circuit configurations shown in Fig. 14. The output tuned circuit was designed to provide filtering for the desired output frequency so that rms values of output voltage could be obtained. Limiting characteristics were measured for two types of feedback, resistive and tuned circuit; results are shown in Fig. 15. When a resonant circuit is used in the feedback loop, the gain of the circuits is higher and limiting occurs at a lower input level. The effects of multistage limiting are described later.

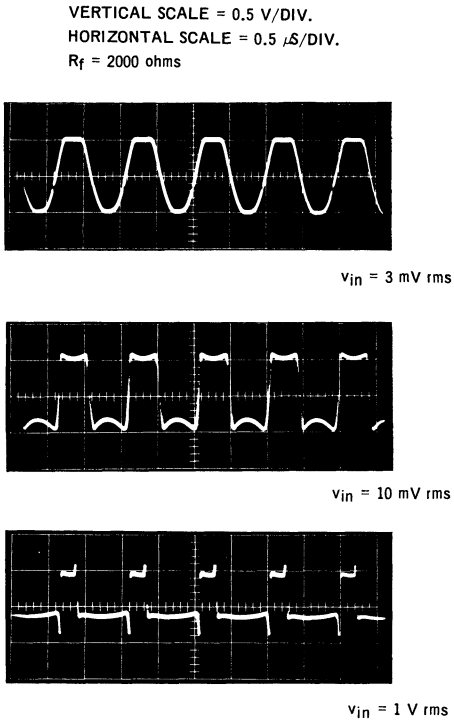
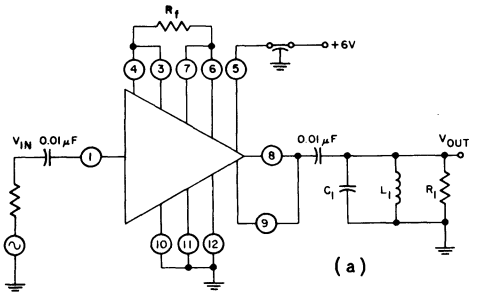
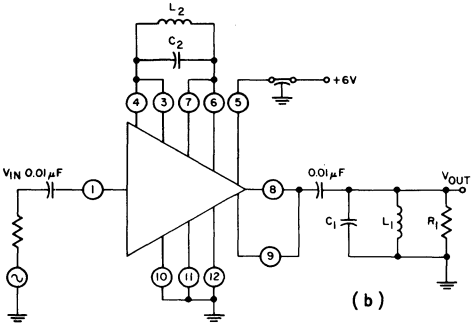


Fig. 13 - Output waveforms obtained in a limiter application.

Noise Performance. The table below shows typical noise figures for the CA3021, CA3022, and CA3023 circuits for a frequency of 1 MHz, a supply voltage of 6 volts, and a source resistance of 50 ohms. The data in the first column of noise figures were measured in the connection shown in Fig. 2a; the second column shows data measured in the connection shown in Fig. 2b.

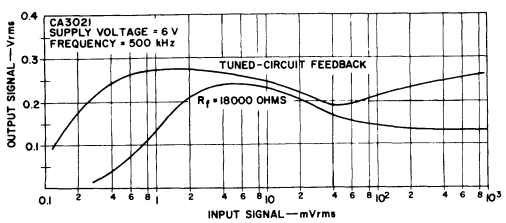
Circuit	Noise Figure — dB	
	Term. 10, 11, 12 connected to ground; gain = 40 dB	AGC operating, noise measured for maximum gain of 30 dB
CA3021	5.8	7.5
CA3022	7.1	8.7
CA3023	7.2	8.7

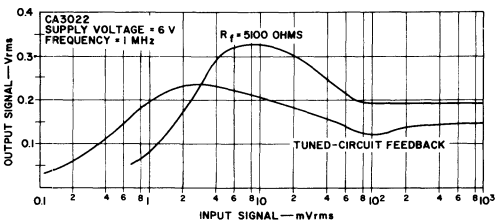




TYPE	FREQ. (MHz)	C_1 (pF)	L_1 (μH)	R_1 (kΩ)	CIRCUIT(a) R_F (kΩ)	CIRCUIT(b) L_2 (mH)	CIRCUIT(b) C_2 (pF)
CA3021	0.5	2000	36-64	8.2	18	10	-
CA3022	1	5000	3-5	1	5.1	1.2	4-45
CA3023	5	600	1.8	1	2	-	-

Fig. 14 - Circuits used for evaluation of limiting characteristics.





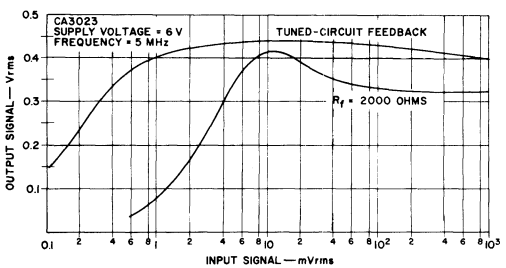


Fig. 15 - Limiting characteristics.

Applications

Video Amplifiers. The use of single CA3021, CA3022, or CA3023 integrated circuits in video applications was discussed previously. For an evaluation of iterative video performance, two CA3022 circuits were operated in cascade. Each circuit employed 0.01-microfarad coupling capacitors and feedback resistors of 2000 ohms. Performance data can be summarized as follows:

Supply voltage	6	volts
Supply current	4.5	mA
Power dissipation	27	mW
Voltage gain	61	dB
Maximum undistorted output with 510-ohm load	0.25	Vrms
Signal level for 3-dB signal-to noise ratio	11	μV
Dynamic range (input-output linearity)	27	dB
Bandwidth, 3-dB points:		
upper frequency	10.5	MHz
lower frequency	50	kHz

10-MHz IF Amplifier. Fig.16 shows a 10-MHz amplifier employing two CA3023 circuits. The first stage is operated in a broadband mode with a 2000-ohm feedback resistor between terminals 3 and 7, in accordance with the design rules described previously. The second stage is a tuned if amplifier. Because the sinusoidal output capability of the CA3023 at 10-MHz is in the 200-millivolt range, it is necessary to step up the voltage to drive the envelope detector; therefore, a tuned transformer that has a 1-to-4 turns ratio is used at the second-stage output. The total effective circuit Q for this if configuration is 200, and the full rf voltage gain is 86 dB from the input of the first stage to the output of the step-up transformer.

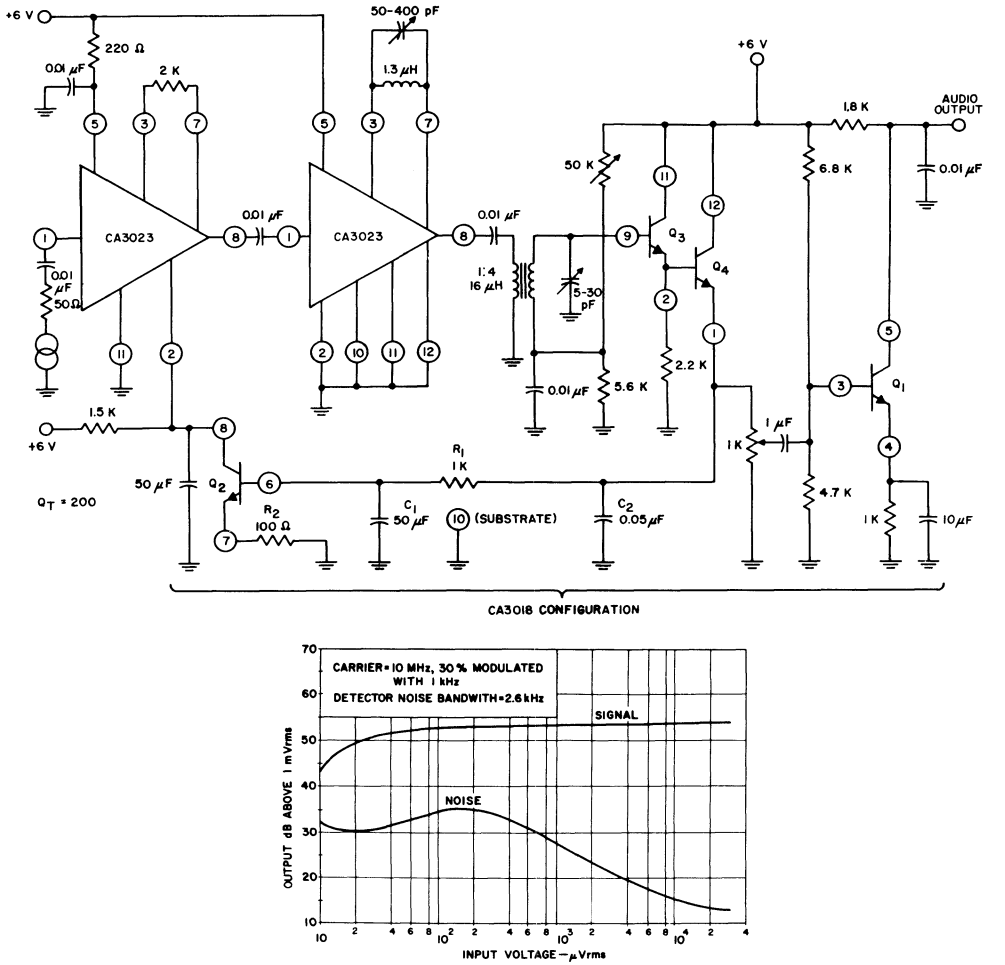


Fig. 16 - Schematic diagram and performance curves for 10-MHz if amplifier using two CA3023 circuits.

A CA3018 integrated-circuit transistor array is used to provide detection, audio amplification, and dc amplification. Detection is provided by transistors Q_3 and Q_4 of the CA3018; the detected output is passed through a low-pass filter (C_1, C_2, and R_1) and applied to the agc amplifier transistor Q_2. Transistor Q_2 goes from cutoff to saturation with increasing signal. The voltage drop across a 100-ohm degenerative resistor R_2 prevents the gain-control voltage in terminal 2 of the first CA3023 amplifier from decreasing below 0.5 volt and causing signal cancellation. Transistor Q_1 of the CA3018 provides audio gain and is biased in a conventional manner. Fig.16 also shows the output-signal and noise characteristics of the circuit as functions of rf input level for an input signal that is 30-percent modulated by a 1-kHz sine wave. The audio-output equivalent-noise bandwidth is 2.6 kHz.

455-kHz IF Amplifier. Fig.17 shows a 455-kHz two-stage if amplifier using

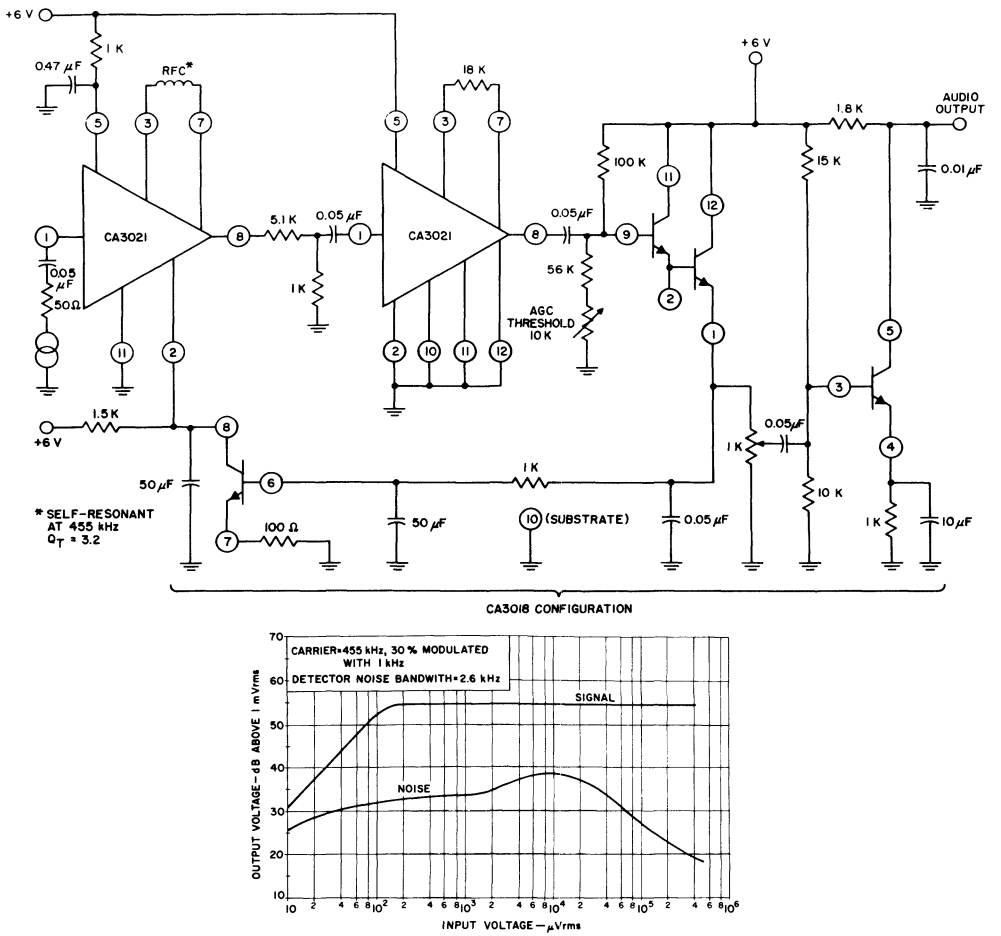


Fig. 17 - Schematic diagram and performance curves for 455-kHz if amplifier using two CA3021 circuits.

the CA3021. The tuned-circuit approach discussed previously is used in the first stage. The rf feedback choke is self-resonant at 455 kHz and has a Q of 3.2 in the circuit. The second stage is a video amplifier. Input filtering would normally be provided to obtain the desired if response. For the particular choice of stage gain and agc loop gain, an interstage pad network is used to maintain stability and achieve an acceptable signal-to-noise ratio with gain control. The CA3018 output configuration is essentially the same as that used in the circuit of Fig.16. The signal and noise characteristics of the 455-kHz amplifier are also shown in Fig.17 for the same conditions used for the 10-MHz amplifier.

28-MHz Two-Stage Limiter Amplifier. Fig.18 shows the circuit diagram of a 28-MHz two-stage limiter amplifier using two CA3023 integrated circuits. Terminals 3 and 7 are connected to terminals 4 and 6, respectively; terminal 8 is connected to terminal 9 to provide limiting action. A self-resonant coil in parallel with a 2000-ohm resistor is inserted in the feedback loop of each amplifier to provide gain and stability. The bandwidth of the system before limiting is 3.8 MHz, and the effective Q is 7.35. The total gain is 61 dB (30.5 dB per stage), and the power dissipation is 66 milliwatts. Fig.18 also shows the limiting performance of the system. Full limiting occurs at an input of 300 microvolts.

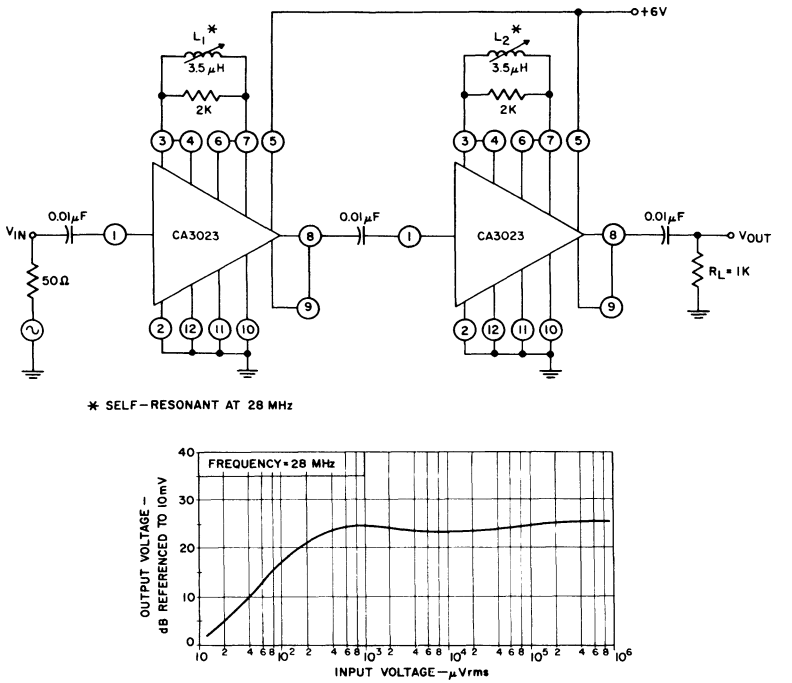


Fig.18 - Schematic diagram and limiting performance of two-stage 28-MHz limiter amplifier using the CA3023.

500-kHz Limiting Amplifier. Fig.19 shows the circuit diagram of a 500-kHz limiting amplifier using two CA3021 circuits. Two 500-kHz self-resonant chokes are used in the feedback path. A tuned circuit is included in the output to obtain a sine-wave output. The limiting characteristics of this amplifier are also shown. Although limiting occurs for noise, a limited signal is apparent above the noise at an input signal of 1 microvolt. Because of the noise and early limiting, voltage gain can only be estimated; however, it is at least 100 dB. Good limiting performance was obtained for input signals up to 3 volts rms. Total power drain for the circuit with a 6-volt supply was approximately 6 milliwatts.

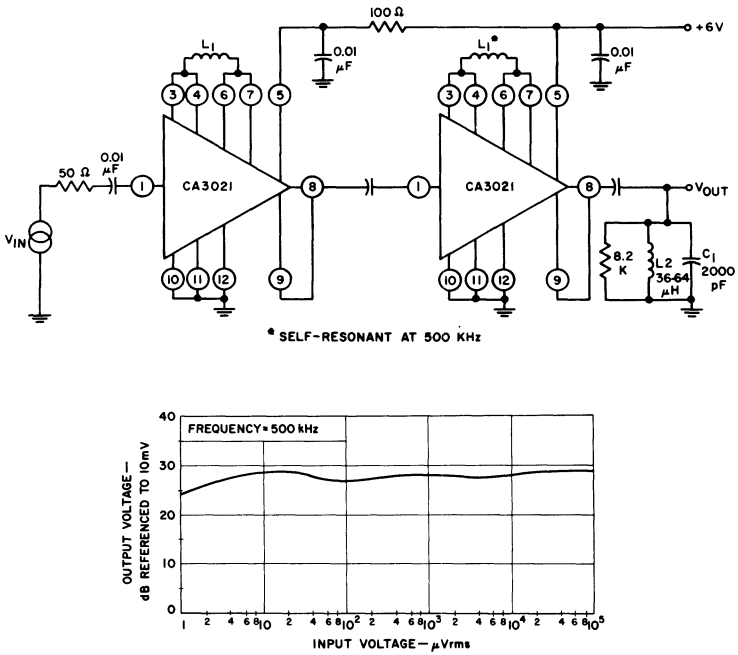


Fig. 19 - Schematic diagram and limiting performance of two-stage 500-kHz limiter amplifier using the CA3021.

APPLICATION OF THE RCA CA3020 AND CA3020A INTEGRATED-CIRCUIT MULTI-PURPOSE WIDE-BAND POWER AMPLIFIERS

by

W. M. AUSTIN AND H. M. KLEINMAN

The discussions in this Note are applicable to both integrated-circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has a lower voltage rating and must not be used in applications which require voltages on the output transistors greater than 18 volts. The integrated circuit protects the output transistor by limiting the drive to the output stages. The drive-limited current capability of the CA3020 is less than that of the CA3020A, but peak currents in excess of 150 milliamperes are an assured characteristic of the CA3020.

The RCA CA3020 and CA3020A integrated circuits are multi-purpose, multi-function power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz.

The discussions in this Note are applicable to both integrated-circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has more limited voltage- and current-handling capability and must not be used in applications which require voltage swings on the output transistors greater than 18 volts or peak currents in excess of 150 milliamperes.

The CA3020 and CA3020A are designed to operate from a single supply voltage which may be as low as +3 volts. The maximum supply voltage is dictated by the type of circuit operation. For transformer-loaded class B amplifier service, the maximum supply voltages are +9 and +12 volts for the CA3020 and the CA3020A, respectively. When operated as a class B amplifier, either circuit can deliver a typical output of 150 milliwatts from a +3-volt supply or 400 milliwatts from a +6-volt supply. At +9 volts, the idling dissipation can be as low as 190 milliwatts, and either circuit can deliver an output of 550 milliwatts. An output of slightly more than 1 watt is available from the CA3020A when a +12-volt supply is used.

CIRCUIT DESCRIPTION AND OPERATION

Fig. 1 shows the schematic diagram of the CA3020 and CA3020A, and indicates the five functional blocks into

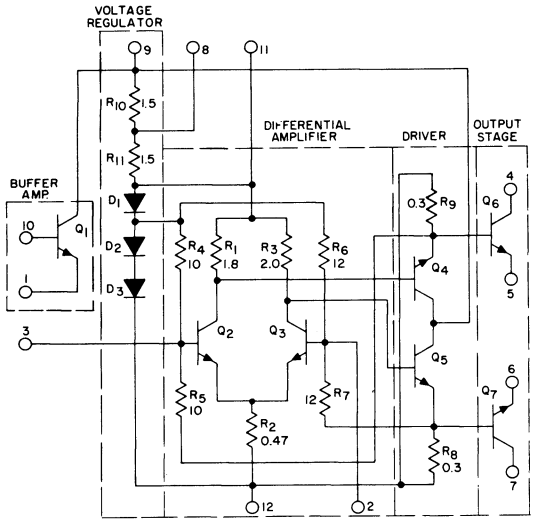


Fig. 1—Schematic diagram of CA3020 and CA3020A integrated-circuit amplifiers.

which the circuit can be divided for understanding of its operation. Fig. 2 shows the relationship of these blocks in block-diagram form.

A key to the operation of the circuit is the voltage regulator consisting of diodes D_1, D_2, and D_3 and resistors R_{10} and R_{11}. The three diodes are designed to provide accurately controlled voltages to the differential amplifier so that the proper idling current for class B operation is established in the output stage. The characteristics of these monolithic diodes closely match those of the driver and output stages so that proper bias voltages are applied over the entire military temperature range of −55 to +125°C. The close thermal coupling of the circuit assures against thermal runaway within the prescribed temperature and dissipation ratings of the devices.

The differential amplifier operates in a class A mode to supply the power gain and phase inversion required for the push-pull class B driver and output stages. In normal operation, an ac signal is capacitively coupled to terminal

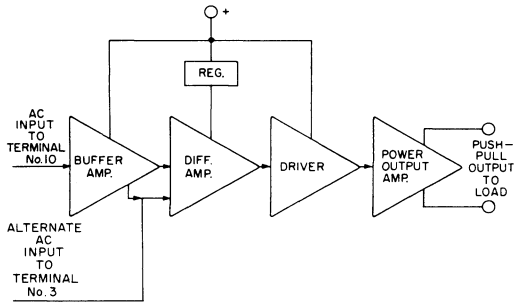


Fig. 2—Functional block diagram of the CA3020 and CA3020A.

3, and terminal 2 is grounded through a suitable capacitor. When the signal becomes positive, transistor Q_2 is turned on and its collector voltage changes in a negative direction. The same current flows out of the emitter of Q_2 and tends to flow to ground through resistor R_2. However, the impedance of R_2 is high compared to the input impedance of the emitter of Q_3, and an alternate path is available to ground through the emitter-to-base junction of transistor Q_3 and then through the bypass capacitor from terminal 2 to ground. Because this path has a much lower impedance than R_2, most of the current takes this alternate route. The signal current flowing into the emitter of Q_3 reduces the magnitude of that current and, because the collector current is nearly equal to the emitter current, the collector current in Q_3 drops and the collector voltage rises. Thus, a positive signal on terminal 3 causes a negative ac voltage on the collector of transistor Q_2 and a positive ac voltage on transistor Q_3, and provides the out-of-phase signals required to drive the succeeding stages. It should be noted that the differential amplifier is not balanced; resistor R_3 is ten per cent greater than R_1. This unbalance is deliberately introduced to compensate for the fact that all of the current in the emitter of Q_2 does not flow into Q_3. Use of a larger load resistor for transistor Q_3 compensates for the lower current so that the voltage swings on the two collectors have nearly the same magnitude.

The driver stages (transistors Q_4 and Q_5) are emitter-follower amplifiers which shift the voltage level between the collectors of the differential-amplifier transistors and the bases of the output transistors and provide the drive current required by the output transistors.

The power transistors (Q_6 and Q_7) are large, high-current devices capable of delivering peak currents greater than 0.25 ampere. The emitters are made available to facilitate various modes of operation or to permit the inclusion of emitter resistors for more complete stabilization of the idling current of the amplifier. Inclusion of such resistors also reduces distortion by introducing negative feedback, but reduces the power-output capability by limiting the available drive.

Inclusion of emitter resistors between terminals 5 and 6 and ground also enhances the effectiveness of the internal dc feedback supplied to the bases of transistors Q_2 and Q_3 through resistors R_5 and R_7. Any increase in the idling current in either output transistor is reflected as an increased voltage at its base. This change is coupled to the input through the appropriate resistor to correct for the increased current.

A later section of this Note describes how stable class A operation of the output stages may be obtained.

OPERATING CHARACTERISTICS

Supply Voltages and Derating. The CA3020 operates with any supply voltage between +3 and +9 volts. The CA3020A can also be operated with supply voltages up to +12 volts with inductive loads or +25 volts with resistive loads. Fig. 3 shows the permissible dissipation rating of the CA3020 and CA3020A as a function of case

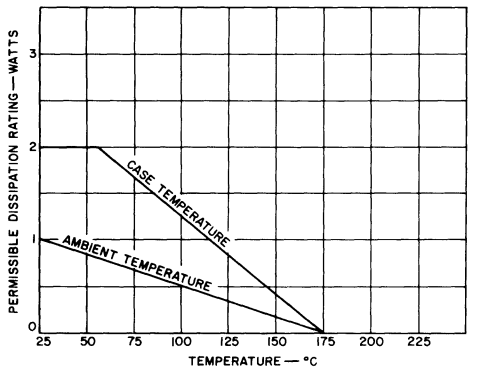


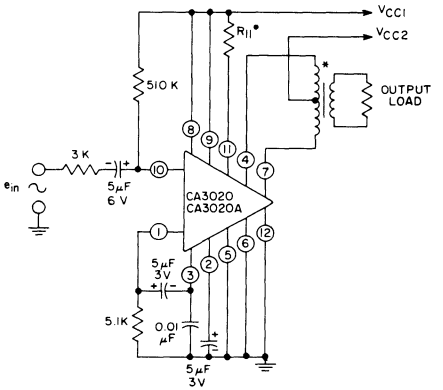
Fig. 3—Dissipation rating of the CA3020 and CA3020A as a function of case and ambient temperatures.

and ambient temperatures. At supply voltages from +6 to +12 volts, a heat sink may be required for maximum power-output capability. The worst-case dissipation $P_{d_{max}}$ as a function of power output can be calculated as follows:

$$P_{d_{max}} = (V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}) + (V_{CC_2}{}^2/(R_{CC})$$

where V_{CC_1} and V_{CC_2} are the supply voltages to the differential-amplifier and output-amplifier stages, respectively; I_{CC_1} and I_{CC_2} are the corresponding idling currents; and R_{CC} is the collector-to-collector load resistance of the output transformer. This equation is preferred to the conventional formula for the dissipation of a class B output transistor (i.e., 0.84 times the maximum power output) because the $P_{d_{max}}$ equation accounts for the device standby power and device variability.

Basic Class B Amplifier. Fig. 4 shows a typical audio-amplifier circuit in which the CA3020 or CA3020A can provide a power output of 0.5 or 1 watt, respectively. Table I shows performance data for both types in this amplifier. The circuit can be used at all voltage and power-output levels applicable to the CA3020 and CA3020A.



* Better Coil and Transformer DF108A, Thordarson TR-192, or equivalent. see text and tables.

Fig. 4—Basic class B audio amplifier circuit using the CA3020 or CA3020A.

The emitter-follower stage at the input of the amplifier in Fig. 4 is used as a buffer amplifier to provide a high input impedance. Although many variations of biasing may

Table 1 — Typical Performance of CA3020 and CA3020A in Circuit of Fig. 4*

Characteristic	CA3020	CA3020A	
Power Supply — V_{CC_1}	9	9	V
V_{CC_2}	9	12	V
Zero-Signal Idling Current — I_{CC_1}	15	15	mA
I_{CC_2}	24	24	mA
Maximum-Signal Current — I_{CC_1}	16	16.6	mA
I_{CC_2}	125	140	mA
Maximum Power Output at 10% THD	550	1000	mW
Sensitivity	35	45	mV
Power Gain	75	75	dB
Input Resistance	55	55	kΩ
Efficiency	45	55	%
Signal-to-Noise Ratio	70	66	dB
% Total Harmonic Distortion at 150 mW	3.1	3.3	%
Test Signal	1000 Hz/600Ω generator		
Equivalent Collector-to-Collector Load	130	200	Ω
Idling-Current Adjust Resistor (R_{11})	1000	1000	Ω

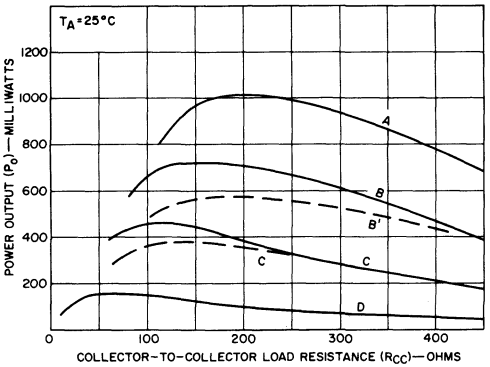
* Integrated circuit mounted on a heat sink, Wakefield 209 Alum. or equiv.

be applied to this stage, the method shown is efficient and economical. The output of the buffer stage is applied to terminal 3 of the differential amplifier for proper balance of the push-pull drive to the output stages. Terminals 2 and 3 must be bypassed for approximately 1000 ohms at the desired low-frequency roll-off point.

At low power levels, the cross-over distortion of the class B amplifier can be high if the idling current is low. For low cross-over distortion, the idling current should be approximately 12 to 24 milliamperes, depending on the efficiency, idling dissipation, and distortion requirements of the particular application. The idling current may be increased by connection of a jumper between terminals 8 and 9. If higher levels of operating idling current are desired, a resistor (R_{11}) may be used to increase the regulated voltage at terminal 11 by a slight amount with additional current injection from the power supply V_{CC_1}.

In some applications, it may be desirable to use the input transistor Q_1 of the CA3020 or CA3020A for other purposes than the basic buffer amplifier shown in Fig. 4. In such cases, the input ac signal can be applied directly to terminal 3.

The extended frequency range of the CA3020 and CA3020A requires that a high-frequency ac bypass capacitor be used at the input terminal 3. Otherwise, oscillation could occur at the stray resonant frequencies of the external components, particularly those of the transformers. Lead inductance may be sufficient to cause oscillation if long power-supply leads are not properly ac bypassed at the CA3020 or CA3020A common ground point. Even the bypassing shown may be insufficient unless good high-frequency construction practices are followed.

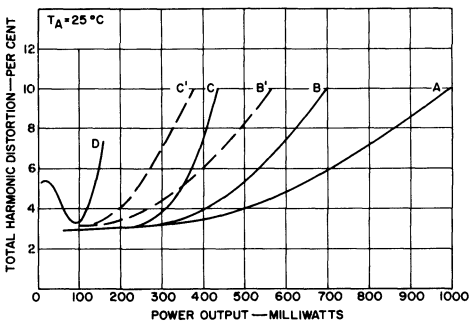


CURVE CA3020	CURVE CA3020A	IDLING CURRENT (mA) I_{CC1}	IDLING CURRENT (mA) I_{CC2}	POWER-SUPPLY VOLTAGE (V) V_{CC1}	POWER-SUPPLY VOLTAGE (V) V_{CC2}	R_{11} (OHMS)
	A	9	10	9	12	00
B	B	9	10	9	9	00
C	C	7	6	6	6	00
	D	8	8	3	3	220

Fig. 5—Power output of the CA3020 and CA3020A as a function of collector-to-collector load resistance R_{CC}.

Fig. 5 shows typical power output of the CA3020A at supply voltages of +3, +6, +9, and +12 volts, and of the CA3020 at +6 and +9 volts, as measured in the basic class B amplifier circuit of Fig. 4. The CA3020A has higher power output for all voltage-supply conditions because of its higher peak-output-current capability.

Fig. 6 shows total harmonic distortion (THD) as a function of power output for each of the voltage conditions shown in Fig. 5. The values of the collector-to-collector load resistance (R_{CC}) and the idling-current adjust resistor (R_{11}) shown in the figure are given merely as a fixed reference; they are not necessarily optimum values. Higher idling-current drain may be desired for low cross-over distortion, or a higher value of R_{CC} may be used for better sensitivity with less power-output capability. Because the maximum power output occurs at the same conditions of peak-current limitations, the sensitivities at maximum power output for the curves of Figs. 5 and 6 are approximately the same. Increasing the idling-current drain by reducing the value of the resistor R_{11} also improves the sensitivity.



CURVE CA3020	CURVE CA3020A	IDLING CURRENT (mA)		POWER-SUPPLY VOLTAGE (V)		R_{CC} (OHMS)	R_{11} (OHMS)
	A	15	24	9	12	200	1000
B	B	15	24	9	9	150	1000
C	C	12	14	6	6	100	1000
	D	9	9	3	3	50	220

Fig. 6—Total harmonic distortion of the CA3020 or CA3020A as a function of power output.

Fig. 7 illustrates the improvement in cross-over distortion at low power levels. Distortion at 100 milliwatts is shown as a function of idling current I_{CC_2} (output stages only). There is a small improvement in total harmonic distortion for a large increase in idling current as the current level exceeds 15 milliamperes.

APPLICATIONS

Audio Amplifiers. The circuit shown in Fig. 4 may be used as a highly efficient class B audio power-output circuit in such applications as communications systems, AM or FM radios, tape recorders, phonographs, intercom sets, and linear mixers. Fig. 8 shows a modification of this

circuit which may be used as a transformerless audio amplifier in any of these applications or in other portable instruments. The features of this circuit are a power-output capability of 310 milliwatts for an input of 45 millivolts, and a high input impedance of 50,000 ohms. The idling-current drain of the circuit is 24 milliamperes. The curves of Fig. 5 may be used to determine the value of the center-tapped resistive load required for a specified power-output level (the indicated load resistance is divided by two).

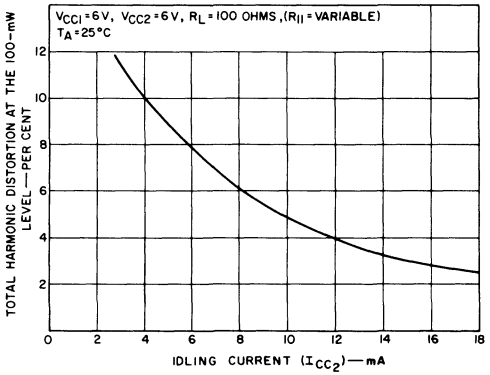


Fig. 7—Total harmonic distortion as a function of idling current for a supply voltage of 6 volts and an output of 100 milliwatts.

The CA3020 or CA3020A provides several advantages when used as a sound output stage or as a preamplifier-driver in communications equipment because each type is a compact and low-power-drain circuit. The squelching requirement in such applications is simple and economical.

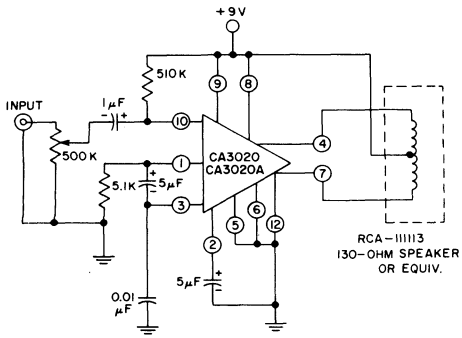


Fig. 8—310-milliwatt audio amplifier without transformers.

Fig. 9 shows a practical method of providing squelch to the CA3020 or CA3020A. When the squelch switching transistor Q_s is in the "on" state, the CA3020 or CA3020A

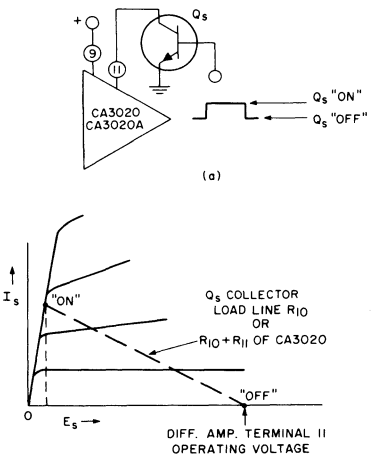


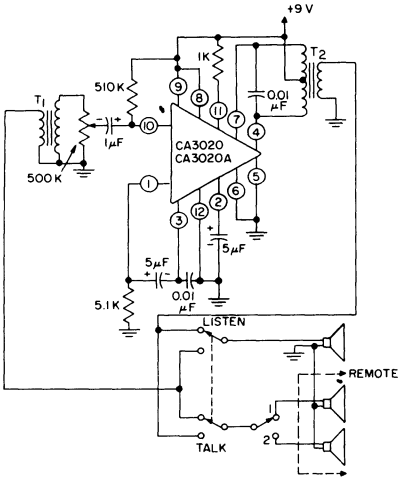
Fig. 9—Method of applying squelch to the CA3020 or CA3020A to save idling dissipation.

is "off" and draws only fractional idling dissipation. The only current that flows is that of the buffer-amplifier transistor Q_1 in the integrated circuit and the saturating current drain of Q_s. For a circuit similar to that of Fig. 8, the squelched condition requires an idling current of approximately 7 milliamperes, as compared to a normal idling-current drain of 24 milliamperes.

In applications requiring high gain and impedance matching, the CA3020 or CA3020A can be adapted for use without complex circuit modifications. Detectors having low signal outputs or high impedances can be easily matched to the input of the CA3020 or CA3020A buffer amplifier. The typical integrated-circuit input impedance of 55,000 ohms may be too low for crystal output devices such as phonograph pickups, but the sensitivity may be sacrificed to impedance-match at the input while still providing adequate drive to the CA3020 or CA3020A. Both types may be used in tape recorders as high-gain amplifiers, bias oscillators, or record and playback amplifiers. The availability of two input terminals permits the use of the CA3020 or CA3020A as a linear mixer, and thus adds to its flexibility in systems that require adaptation to multiple functions, such as communications equipment and tape recorders.

Fig. 10 illustrates the use of the audio amplifier shown in Fig. 4 in an intercom in which a listen-talk position switch controls two or more remote positions. Only the speakers, the switch, and the input transformer are added to the basic audio amplifier circuit. A suitable power supply for the intercom could be a 9-volt battery used intermittently rather than continuously.

Wide-Band Amplifiers. A major general-purpose application of the CA3020 and CA3020A is to provide high gain and wide-band amplification. The CA3020 and CA3020A



T_1: Primary 4 ohms, Secondary 25,000 ohms; Stancor A4744 or equiv.

T_2: Better Coil and Transformer DF1084, Thordarson TR-192, or equiv.

Speakers: 4 ohms

Fig. 10—Intercom using CA3020 or CA3020A.

have typically flat gain-bandwidth response to 8 MHz. Although the circuits are normally biased for class B operation, only the output stages operate in this mode. If proper dc bias conditions are applied, the output stages may be operated as linear class A amplifiers.

Fig. 11 shows the recommended method for achieving an economical and stable class A bias. The differential-amplifier portion of the CA3020A is placed at a potential

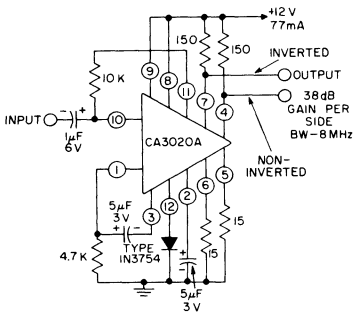


Fig. 11—Wide-band video amplifier illustrating economical and stable class A bias of CA3020A.

above ground equal to the base-to-emitter voltage V_{be} of the integrated-circuit transistors (0.5 to 0.7 volt). In this condition, the output stages have an emitter-current bias approximately equal to the base-to-emitter voltage divided by the emitter-to-ground resistance. The circuit in Fig. 11 is a wide-band video amplifier that provides a gain of 38 dB at each of the push-pull outputs, or 44 dB in a balanced-output connection. The 3-dB bandwidth of the circuit is 30 Hz to 8 MHz. Higher gain-bandwidth performance can be achieved if the diode-to-ground voltage drop at terminal 12 is reduced. The lower voltage drop permits the use of a higher ratio of output-stage collector-to-emitter resistors without departure from the desired portion of the class A load line. It is important to note that the temperature coefficient of the terminal-12-to-ground reference element should be sufficiently low to prevent a large change in the current of the output stages.

The same method for achieving class A bias is used in the large-signal-swing output amplifier shown in Fig. 12.

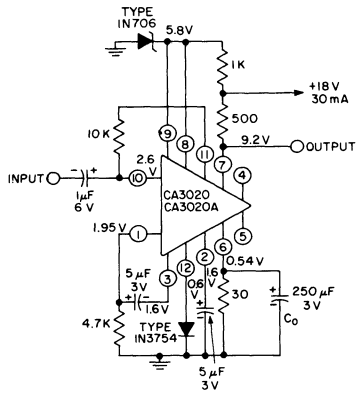


Fig. 12—Large-signal-swing output amplifier using CA3020 or CA3020A.

Either the CA3020 or the CA3020A may be used in this circuit with power supplies below +18 volts; the CA3020A can also be used with B+ voltages up to 25 volts with non-inductive loads. The circuit of Fig. 12 provides a gain of 60 dB and a bandwidth of 3.2 MHz if the output transistor Q_7 has a bypassed emitter resistor. With an unbypassed output emitter resistor, the gain is 40 dB and the bandwidth is 8 MHz. The output stage can deliver a 5-volt-rms signal when a supply of +18 volts is used. For better performance in this type of circuit, the input signal is coupled from the buffer amplifier Q_1 to the input terminal 3 of the differential amplifier. This arrangement provides higher gain because the collector resistor of the differential-amplifier transistor Q_3 is larger than that of Q_2. (This difference results from a requirement of differential drive balance that is not used in this circuit.) In addition, the terminals of the unused output transistor Q_6 help to form an isolating shield between the input at terminal 3 and the output at terminal 7. This cascade of amplifiers has a single phase inversion at the output for much better stability than could be achieved if terminal 4 were used as the output and terminal 3 as the input.

Fig. 13 illustrates the use of the CA3020 or CA3020A as a class A linear amplifier. This circuit features a very

low output impedance and may be used as a line-driver amplifier for wide-band applications up to 8 MHz. The circuit requires a 0.12-volt peak-to-peak input for a single-ended output of 1 volt or a balanced peak-to-peak output of 2 volts from a 3-ohm output impedance at each emitter. The input impedance is specified as 7800 ohms, but is primarily a function of the external 10,000-ohm resistor that provides bias to Q_1 from the regulating terminal 11.

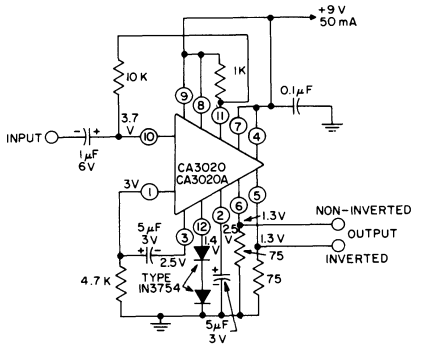


Fig. 13—Class A linear amplier using CA3020 or CA3020A.

Fig. 14 illustrates the practical use of the CA3020 or CA3020A as a tuned amplifier. This circuit uses dc biasing similar to that shown previously, and has a gain of 70 dB at a frequency of 160 kHz. The CA3020 or CA3020A can be used as a tuned rf amplifier or oscillator at frequencies well beyond the 8-MHz bandwidth of the basic circuit.

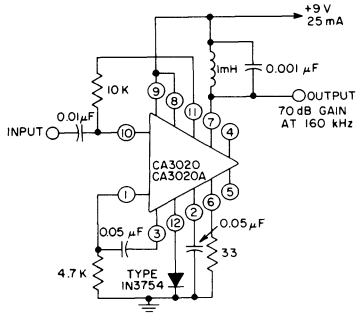
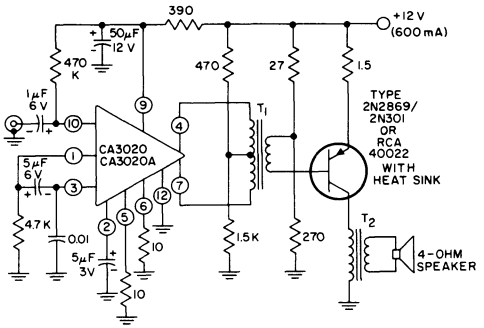


Fig. 14—160-kHz tuned amplifier using the CA3020 or CA3020A.

Driver Amplifiers. The high power-gain and power-output capabilities of the CA3020 and CA3020A make these integrated circuits highly suitable for use as drivers for higher-power stages. In most applications, the full power-output capability of the circuit is not required, and large emitter resistors may be used in the output stage to reduce distortion. The CA3020 and CA3020A can drive any transformer-coupled load within their respective ratings. Several examples of typical applications are given below.

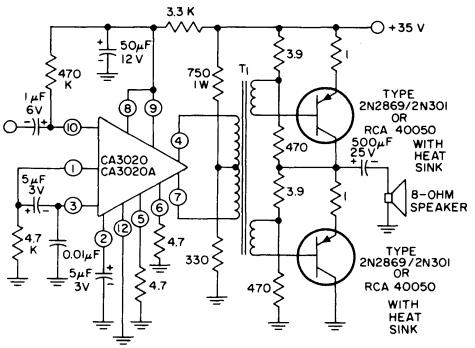
Fig. 15 illustrates the use of the CA3020 or CA3020A to drive a germanium power-output transistor to a 2.5-watt level. Because the integrated circuit is required to deliver a maximum power output of less than 50 milliwatts, an unbypassed emitter resistor can be used in the output stage to reduce distortion. Sensitivity for an output of 2.5 watts is 3 millivolts; this figure can be improved at a slight increase in distortion by reduction of the 4.7-ohm resistors between terminals 5 and 6 and ground.



T_1: primary impedance, 10,000 ohms; center-tapped at 160 ohms; primary direct current, 2 milliamperes; Thordarson TR-207 (entire secondary), or equiv.

T_2: primary impedance, 20 ohms; primary direct current, 0.6 ampere; secondary, 4 ohms; Thordarson TR-304, Stancor TP62, or equiv.

Fig. 15—2.5-watt class A audio amplifier using the CA3020 or CA3020A as a driver amplifier.



T_1: primary impedance, 4,000 ohms; center-tapped; secondary impedance, 600 ohms; center-tapped, split; Thordarson TR-454 or equivalent.

Fig. 16—10-watt single-ended class B audio amplifier using the CA3020 or CA3020A as a driver amplifier.

Because so little of the power-output capability of the CA3020 or CA3020A is used, higher-power class B stages can easily be accommodated by selection of suitable output transistors and appropriate transformers.

Fig. 16 shows a medium-power class B audio amplifier in which the CA3020 or CA3020A is used as a driver. The output stage uses a pair of TO-3-type germanium output transistors which must be mounted on a heat sink for reliable operation. Idling current for the entire system is 70 milliamperes from the 35-volt supply. Sensitivity is 10 millivolts for an output of 10 watts.

Motor Controller and Servo Amplifier. The CA3020 or CA3020A may be used as a 40-to-400-Hz motor controller and servo amplifier, as shown in Fig. 17.

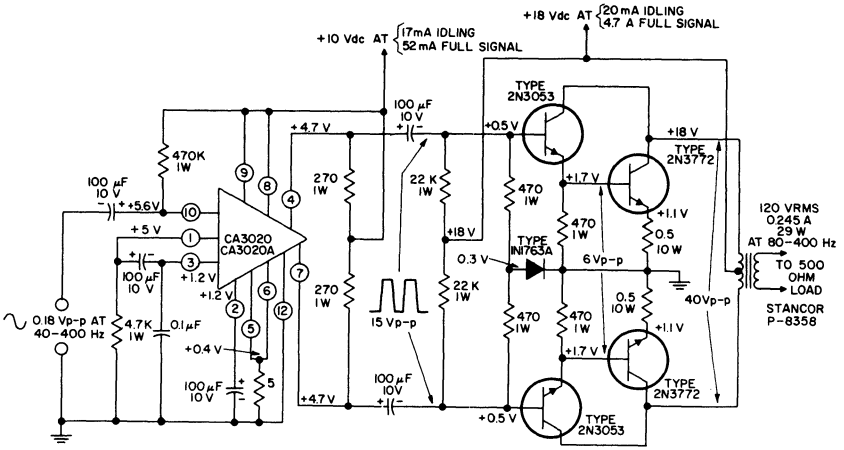


Fig. 17—Motor controller and servo amplifier using CA3020 or CA3020A.

Principal Features and Applications of the RCA-CA3040 Integrated-Circuit Wideband Amplifier

by
W. M. Austin

The RCA-CA3040 is a monolithic integrated circuit designed for use in wideband video and intermediate-frequency amplifier applications to frequencies as high as 100 MHz. The device, offered in a 12-pin TO-5 package, features a balanced differential voltage gain of 37 dB with less than 1 dB of imbalance and provides a typical 3-dB bandwidth of 55 MHz. Useful voltage gain is well beyond the 3-dB frequency roll-off point which, in some applications, extends to frequencies up to 200 MHz. Additional features of the CA3040 include temperature compensation for gain and voltage over the -55 to 125°C temperature range, a choice of zero or 180-degree phase shift from input to output terminals, and high input and low output impedance characteristics over a broad bandwidth. This Note describes the operation of the CA3040, its electrical characteristics and ratings, and its primary application as a wideband amplifier.

CIRCUIT DESCRIPTION

Fig. 1 shows the schematic diagram for the CA3040 circuit. The heart of this circuit consists of two differentially connected cascode amplifiers that form a so-called "differential cascode" amplifier. The transistors Q_3 and Q_4 are common-emitter amplifiers which are connected at the emitters to form the differential transfer junction. The common-base transistors Q_5 and Q_6 are emitter-driven from the common-emitter transistors Q_3 and Q_4, respectively, to form two differential-cascode amplifier pairs.

Each common-emitter amplifier is buffer-isolated from the input terminals by an emitter-follower stage for high input impedance and minimum co-channel phase pulling. Each common-base amplifier of the cascode is coupled to the output terminals by use of an emitter-follower stage for low impedance at the output terminals.

When the signal flow through the device is from terminal 4 to terminal 12 and from terminal 6 to terminal 10, there is a 180-degree internal phase shift; when signal flow is from terminal 4 to terminal 10 and from terminal 6 to terminal 12, the phase shift is zero. Fig. 2 shows a signal-flow diagram for the former case. The dc feedback loop shown is a bias-selection and temperature-tracking network. The bias network consists of reference diodes D_1 and D_2, transistor Q_9, and resistors R_3,

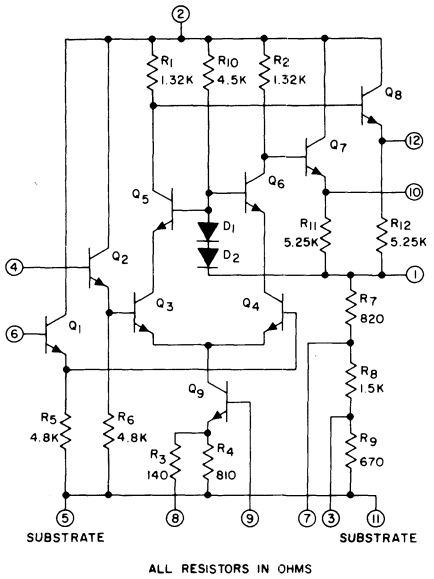


Fig. 1 – Schematic diagram of the CA3040 wideband amplifier.

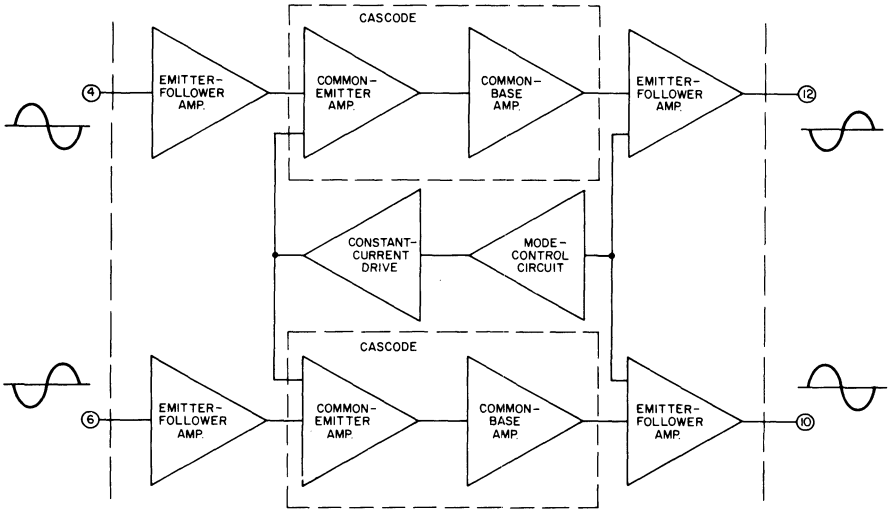


Fig. 2 – Signal-flow diagram of the CA3040.

R_4, R_7, R_8, R_9, and R_{10}. The bias network selected by proper connection of terminals 3, 7, 8, and 9 determines the "mode" of desired temperature tracking.

BIAS MODES

The dc bias-point stability or ac gain stability of the CA3040 is maintained over the temperature range of -55 to 125°C by the choice of two bias modes. These bias modes are selected by proper connection of the transistor Q_9 biasing network. Fig. 3 shows the bias modes for (a) constant voltage and (b) constant gain.

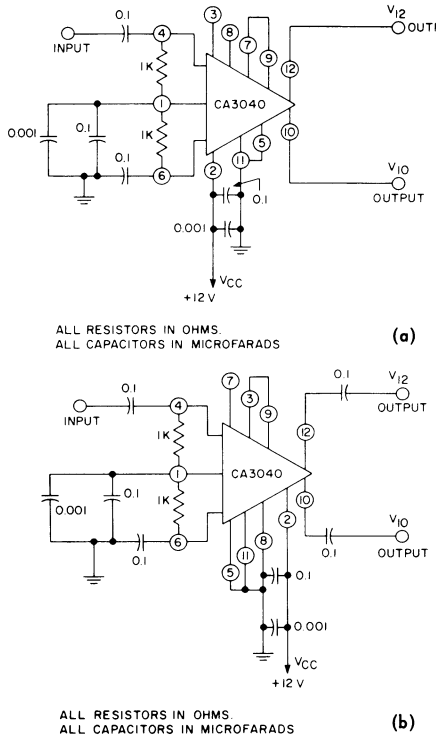


Fig. 3 – Bias configurations for the CA3040 using a single 12-volt power supply: (a) constant-voltage bias; (b) constant-gain bias.

In the constant-voltage bias arrangement, terminals 3 and 8 are open, and terminals 7 and 9 are externally connected. This circuit yields a constant-voltage output for applications that use dc coupling to succeeding stages or that require maximum dynamic range over the specified temperature. DC voltage variation in this mode is less than 0.1 volt over the entire temperature range; ac gain variation is ± 2.0 dB.

In the constant-gain bias arrangement, terminals 3 and 9 are externally connected, terminal 7 is open, and terminal 8 is externally connected to the substrate terminals 5 and 11. In this mode, the ac gain is extremely stable (typical variation is 0 dB); the dc variation at the output terminals is ± 0.8 volt.

For most applications, the constant-voltage bias mode is preferred. This mode provides typical ac-gain variation of less than 0.5 dB over the range from room temperature (25°C) to 85°C ambient. The dynamic range in this mode remains high, and the circuit exhibits less distortion and greater common-mode range for large-signal output swings. Finally, this mode requires one less terminal connection and provides a less complex layout design than that required for the constant-gain circuit.

Both modes have identical power-supply requirements, as illustrated in Figs. 3 and 4. Fig. 3 shows the use of a single 12-volt power supply, and Fig. 4

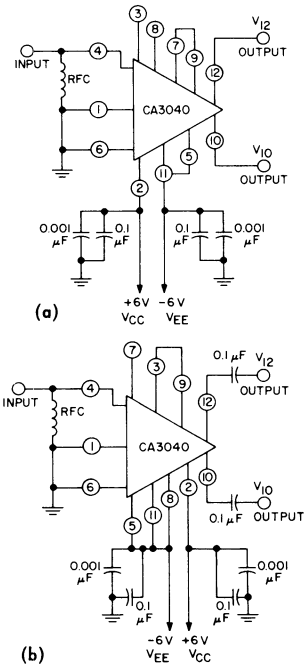


Fig. 4 – Bias configurations for the CA3040 using balanced dual (±6-volt) power supplies; (a) constant-voltage bias; (b) constant-gain bias.

shows balanced dual positive and negative 6-volt power supplies. In Fig. 3(a) and 3(b), the inputs are bias-coupled to terminal 1, which is a reference to the center point of the power supply. Although this connection is most commonly used to maintain the common-mode range, any dc supply or "stiff" bleeder (at one-half the power-supply voltage) may be used. It should be noted that terminal 1 should not be direct-coupled to any external

circuit except as a bias source; otherwise, the input transistors or the temperature-compensation characteristic will not remain within the limits.

CHARACTERISTICS AND RATINGS

The high-frequency capability of the CA3040 is a characteristic of the advanced design that has been developed in the second generation of monolithic integrated-circuit devices. The following are typical performance characteristics of the CA3040.

Fig. 5(a) shows gain as a function of frequency for the CA3040. The test circuit used to obtain this curve is shown in Fig. 5(b). The 3-dB bandwidth is typically 55 MHz and the minimum is 40 MHz at either differential output when terminal 4 is driven from a single-ended 50-ohm source. At 1 MHz, using a 63-millivolt output level, imbalance is not greater than ± 1 dB. In contrast

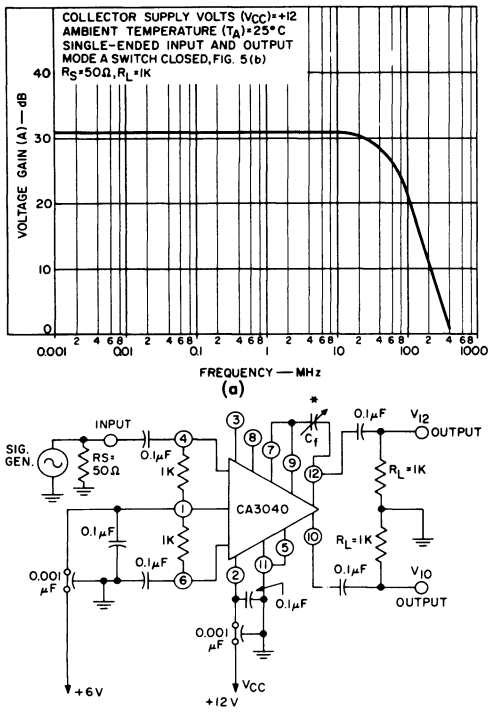


Fig. 5 – (a) Voltage gain as a function of frequency and (b) test circuit of CA3040.

to the more common specification of minimum gain at high frequency, the performance of the CA3040 is given in terms of flat bandwidth relative to the 1-MHz-gain test point.

Fig. 6(a) shows the input resistance and capacitance characteristics of the CA3040. (The input resistance R_{IN} is plotted as conductance G_{IN} because the resistance magnitude approaches infinity at approximately 22 MHz.) The test circuit used to obtain these data is shown in Fig. 6(b). These curves were obtained

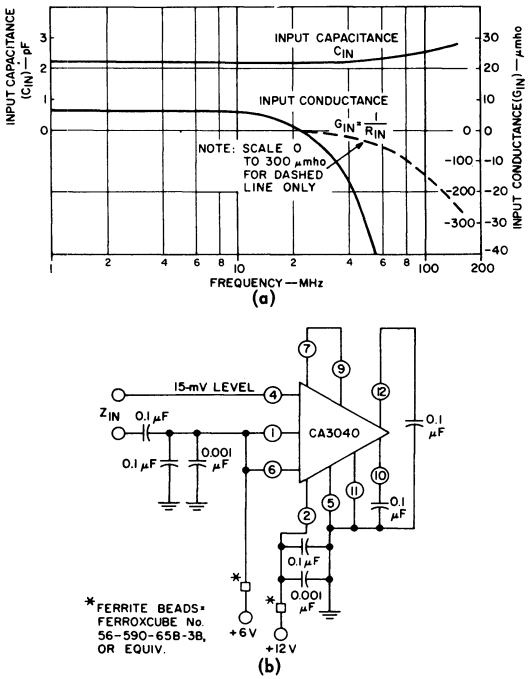


Fig. 6 – (a) Input impedance characteristics and (b) test circuit of CA3040.

with the output terminals shorted and by use of the constant-voltage bias configuration. Although this form of bias has a second-order effect on the input and output capacitance, the input and output capacitance and conductance values for the circuits of Figs. 3 and 4 do not change appreciably from those shown in Fig. 6(a). The negative value of input resistance remains high over the high-gain region and has sufficient magnitude (several thousand ohms) at 150 MHz so that the amplifier remains stable for practical values of the input matching impedance. From 1 to 10 MHz, this resistance remains approximately 150 kilohms. The input capacitance C_{IN} of the CA3040 is approximately 2.2 picofarads and remains relatively constant over the useful frequency range.

Fig. 7(a) shows the output resistance and output capacitance of the CA3040 amplifier as a function of frequency. The test circuit used for these measurements is shown in Fig. 7(b). The output resistance of the cir-

ciut is approximately 125 ohms at low frequencies and gradually rises to 215 ohms at 100 MHz, but decreases again to 200 ohms at 150 MHz. Although a lower output impedance (50 ohms or less) is more desirable, the higher output impedance results in greater temperature-stable gain. When necessary, however, the output impedance can be reduced by addition of another emitter-follower stage. Even when this stage is directly coupled to the output, it has little effect on the dc stability for bias-current drains less than 0.1 milliampere.

Fig. 8(a) shows the 30-MHz noise figure as a function of source resistance in the test circuit presented in Fig. 8(b). This amplifier is similar to the constant-voltage bias circuit shown in Fig. 4(a). The gain and frequency response of the amplifiers are equivalent. The 1-kilohm resistors at the input stage of the circuit of Fig. 5(a), however, produce a 2-dB increase in the noise figure when the CA3040 is matched for maximum power transfer. For low-noise applications, therefore, these shunt-biasing resistors should be replaced by low-loss input matching circuits which can include rf chokes, a transformer, or inductive-capacitive input circuits. It is important that the dc resistances of the two stages remain equal. An unequal dc voltage drop across the bias network produces a large dc offset at the output.

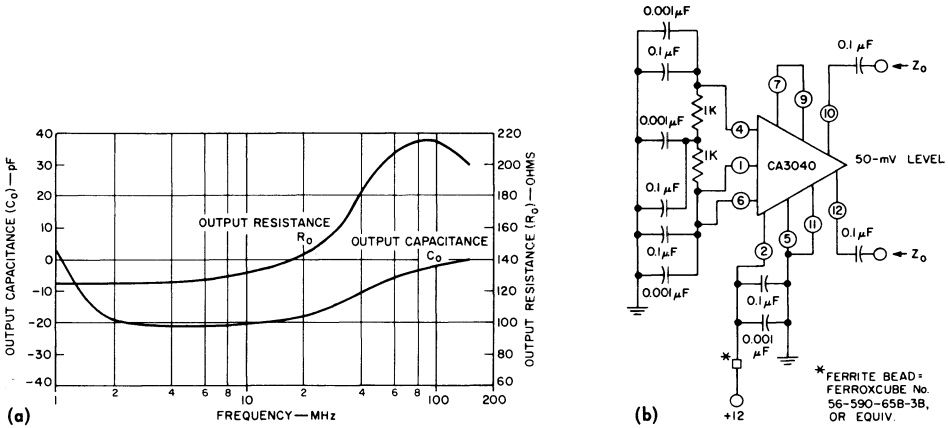


Fig. 7 – (a) Output impedance characteristics and (b) test circuit of CA3040.

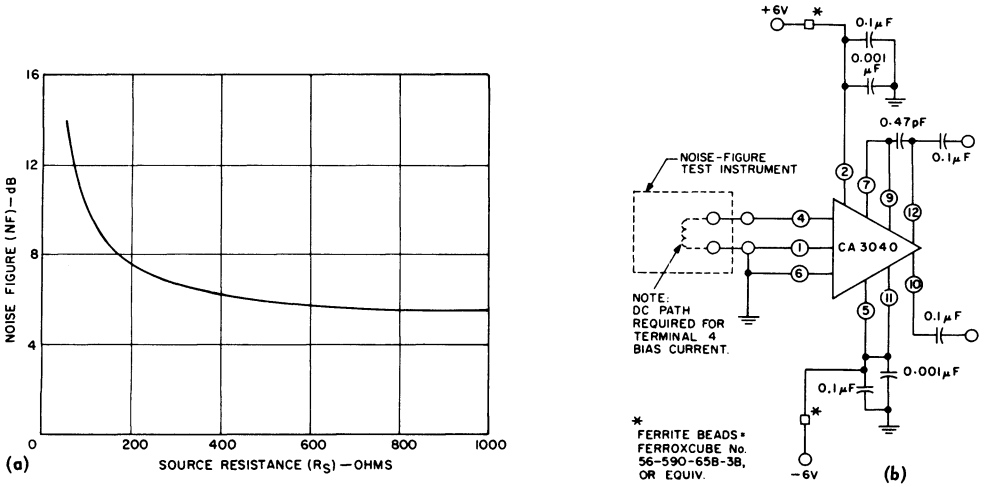


Fig. 8. – (a) Typical 30-MHz noise figure and (b) test circuit of CA3040.

Fig. 9(a) shows the 1/f noise characteristics of the CA3040 in the test-amplifier circuit of Fig. 9(b). The curves represent different values of source resistance. The bandwidth of the test amplifier circuit is restricted to adapt the circuit to a Quan-Tech noise analyzer. The equivalent input 1/f noise is expressed in nanovolts per

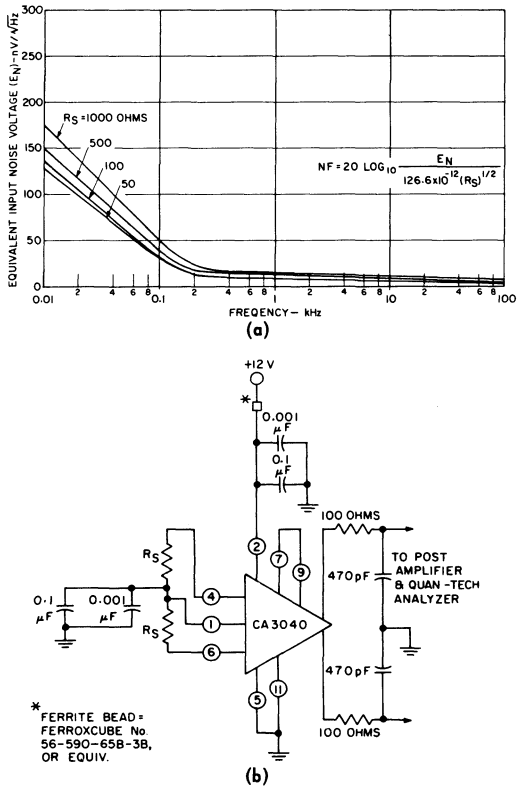


Fig. 9 – (a) Equivalent input noise voltage as a function of frequency and (b) test circuit of CA3040.

square root of the frequency. The limiting low-frequency 1/f noise approaches 125 nanovolts per $\sqrt{Hz}$ at 10 Hz and drops to approximately 25 nanovolts per $\sqrt{Hz}$ at 100 Hz. Above 200 Hz, the noise component is primarily shot noise.

The noise figure NF is related to the noise voltage E_N as follows:

$$NF = 20 \log_{10} \frac{E_N}{(4KTR_S)^{1/2}} = 20 \log_{10} \frac{E_N}{126.6 \times 10\text{-}12\ (R_S)^{1/2}},$$

where E_N is the noise voltage in volts per $\sqrt{Hz}$, K is Boltzmann's constant (1.38×10^{-23} joule/°K), T is the temperature in degrees Kelvin, and R_S is the external source resistance in ohms.

The CA3040 has a linear phase-shift characteristic. Fig. 10 shows the amplifier phase shift from input terminal 6 to output terminal 10 and the differential phase between outputs over the frequency range from 1 to 60 MHz. The test amplifier of Fig. 5(b) was used to obtain the data for these curves. The resistive portion of the output-impedance load in Fig. 5(b) consists primarily of the 1-kilohm resistors. The capacitive load consists of all essential circuitry as well as BNC connectors and phase-meter input probes that represent approximately 8.5 picofarads. Any imbalance from 180 degrees of differential phase at the output terminals remains small in comparison to the reference input-to-output phase shift and is typically less than 1 degree at frequencies up to 50 MHz. Fig. 10 shows the differential output phase

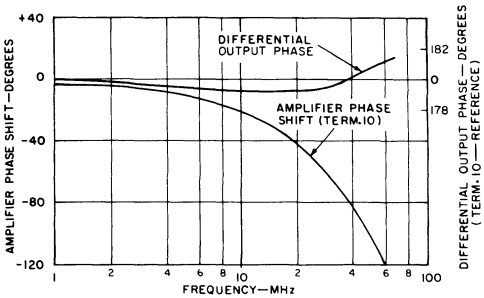


Fig. 10 – Amplifier phase shift and differential output phase as a function of frequency for the CA3040 test circuit of Fig. 5(b).

with terminal 10 given as the reference phase. The imbalance exists because the feedthrough capacitance from terminal 10 to terminal 9 is greater than that from terminal 12 to terminal 9. The constant-current transistor (Q_9 of Fig. 1) amplifies this unbalanced stray capacitance coupling. A fundamental correction for phase can be made by adjustment of the output-capacitance load. In Fig. 5(b), a variable capacitance C_f is used between terminals 9 and 12 for this purpose. The addition of C_f makes possible adjustment of the output signals for phase and gain balance at the high-frequency roll-off point.

Fig. 11(a) shows the frequency response of the CA3040 for various values of load resistance. The test circuit used for these measurements is shown in Fig. 11(b). This amplifier is biased from a balanced dual power supply, but is otherwise similar to the circuit of Fig. 5(b). The curves are valid for either method of biasing.

The low-frequency portion of the curves of Fig. 11(a) shows the decrease in gain with decreased load resistance which is characteristic of the 125-ohm output resistance. The higher-frequency range shows the reduction in bandwidth as the load resistance is decreased.

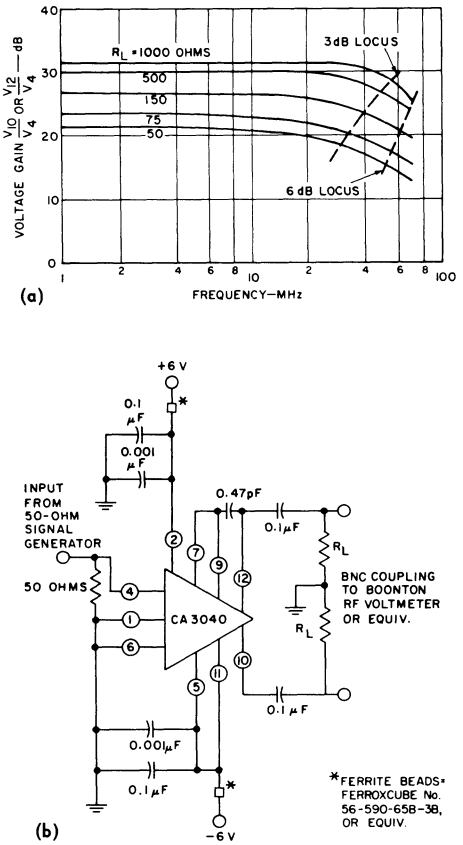


Fig. 11 – (a) Frequency response curves and (b) test circuit for CA3040.

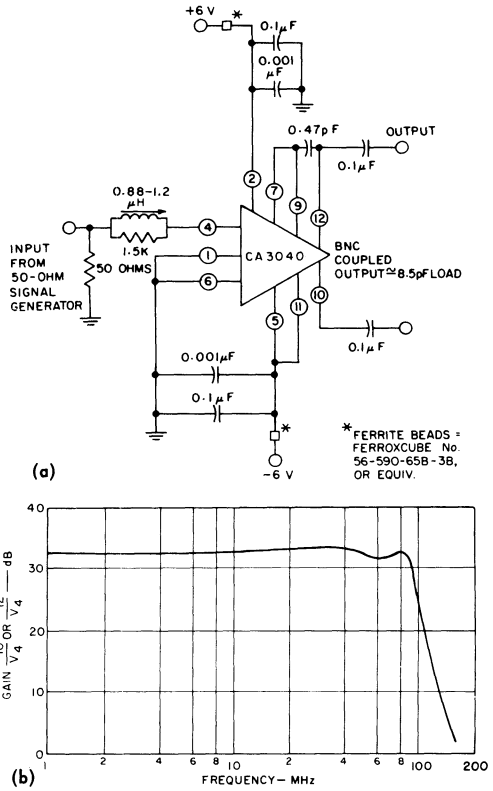


Fig. 12 – (a) Typical CA3040 wideband-amplifier circuit with series input peaking and (b) frequency response characteristic.

This output characteristic is typical of emitter-follower circuits and is caused by a reduction in transistor beta at higher frequencies.

WIDEBAND AMPLIFIERS

In the basic amplifier circuit of Figs. 5(b) and 11(b), the bandwidth of the CA3040 may be increased by use of conventional RL and RC peaking, as well as feedback correction, at the input and output stages. Fig. 12(a) shows a typical wideband amplifier configuration using the CA3040; Fig. 12(b) shows its frequency response. The circuit has a wide-band series-peaked bandwidth greater than 90 MHz at the 3-dB point and greater than 85 MHz to within ±1 dB of gain variation. In the circuit of Fig. 12(a), care is taken to avoid "over-peaking" of the input at higher signal levels so that limiting and distortion effects are minimized.

The frequency-response curves shown in Fig. 12(b), as well as in Figs. 5(a) and 11(a), were obtained with conventional output circuits that contain BNC connectors coupled to the rf voltmeters and produce a total capacitive load of approximately 8 to 9 picofarads. The curve of Fig. 5(a) shows a roll-off characteristic of approximately 12 dB per octave in the 100-to-200-MHz range which is the result of capacitive loading of the cascode and emitter-follower output stages. These output stages may be peaked for partial compensation of the bandwidth loss that results from emitter-follower output loading. The remaining loss in bandwidth, however, results from internal circuit effects and is less easily corrected.

Fig. 13 (a) shows a wideband-amplifier circuit that produces 50 dB ± 1 dB of gain up to 53MHz, as shown by the curve of Fig. 13 (b). The curve shown is for an input-drive signal of 1.0 millivolt rms although the post amplifier can provide an output of 1.0 volt rms before limiting. The post amplifier has a broadband

capability of approximately 85 MHz and uses adjustable rf coils, Miller Type 20A__RBI, or equivalent. The adjustable capacitor at the emitter or the cascode serves to "over peak" the post amplifier and compensate for the RC roll-off of the CA3040 amplifier. With this type of peaking compensation, a flat response that deviates less than 0.2 dB up to 50 MHz is obtained. Wideband capability of the post amplifier is also achieved through the use of high-performance silicon n-p-n transistors. The RCA-40235 has a high gain-bandwidth product f_T and a low collector-to-base feedback capacitance C_{cb} suitable for television rf applications. The 2N5187 is a high-speed switching transistor that has all the basic requirements for economical line-driver applications. The peaking circuit is of the series-shunt type at the collector of the RCA-40235 cascode. Because high idle current is needed in the amplifier output stage, the output level before limiting is set for the minimum requirement necessary for the desired level of peak-to-peak output signal. In this case, a peak-to-peak signal of 2 volts is easily obtained to drive a 50-ohm line that is matched at both ends.

The CA3040 amplifier in Fig. 13(a) is the same as the amplifier of Fig. 5(a), although the basic circuit can use any bias mode or power-supply configuration shown previously. In this particular case, the simple 12-volt power supply (at approximately 60 milliamperes of current drain) satisfies the requirement for a low-cost, wideband circuit. However, when several supply voltages are available, the circuit of Fig. 13(a) can be a direct-coupled combination of the balanced dual ±6-volt CA3040 circuit and the post amplifier. This post amplifier which uses RCA-40235 transistors in a cascode configuration, is designed for dc base voltages of 3 and 6 volts.

STABILITY

In the classical analysis, stability is evaluated as a function of the transfer impedance parameter. The number of possible operating modes and bias options, each of which is evaluated over the useful frequency range, limits the practicality of this type of analysis for the CA3040. Such an analysis would be further comp-

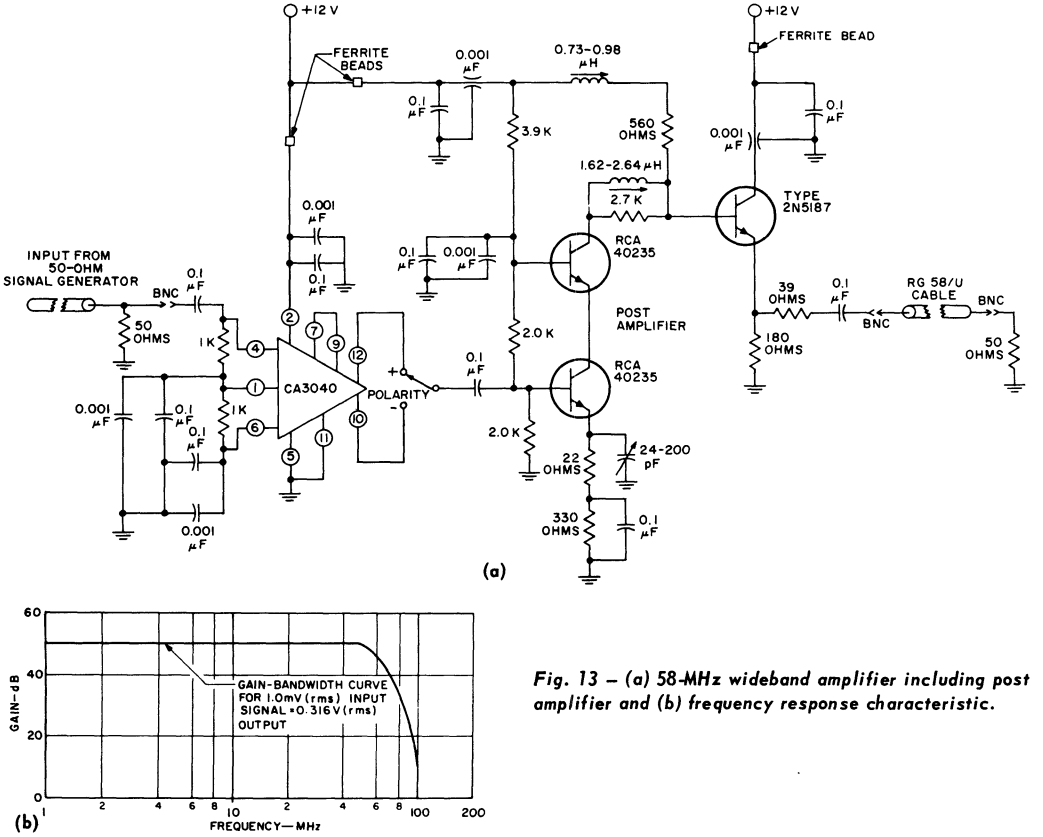


Fig. 13 – (a) 58-MHz wideband amplifier including post amplifier and (b) frequency response characteristic.

licated by the fact that y-parameter data are applicable only at the discrete frequency at which they are taken. In view of these factors, the characteristics of the CA-3040 are guaranteed to have a reasonable stability margin through evaluations in test circuits and by integrity of design. Poor circuit design or improper layout, however, can reduce the stability margin so that oscillations can possibly result.

The differential-amplifier configuration of the CA-3040 offers the advantage in wideband amplifier applications of neutralizing its own feedback. For this reason the circuit layout and printed-board pattern should be designed with a high degree of symmetry.

For stability purposes, terminal 9 of the CA3040 should not be bypassed because common-base oscillations may result in the constant-current transistor Q_9. This effect, however, may be used to advantage in oscillator and mixing applications.

For some applications, such as wideband if amplifiers, it is desirable to limit the high-frequency characteristics of the CA3040. In this case, series resistors in the base input leads of transistors Q_1 and Q_2 are recommended. Resistances of 10 to 100 ohms in series with terminals 4 and 6 not only limit the bandwidth but also act as parasitic suppressors.

CONSTRUCTION

The basic construction of the CA3040 generally follows the usual recommendations for high-frequency wideband amplifiers. Figs. 14 and 15 illustrate the

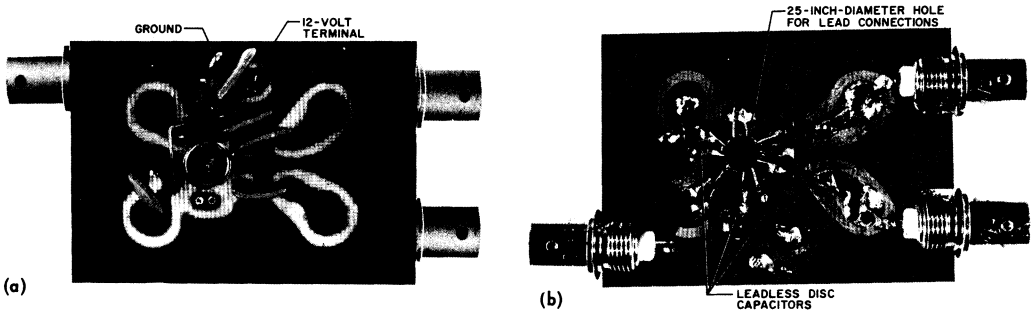


Fig. 14 – Printed-circuit board for the CA3040 wideband amplifier circuit of Fig. 5(b) using constant-voltage bias configuration and a single 12-volt power supply: (a) top view; (b) bottom view.

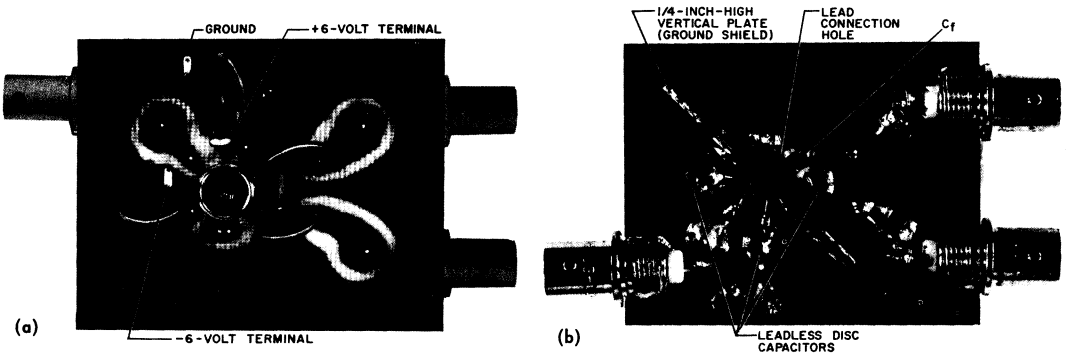
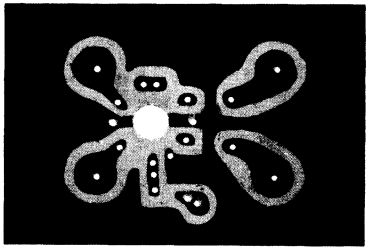
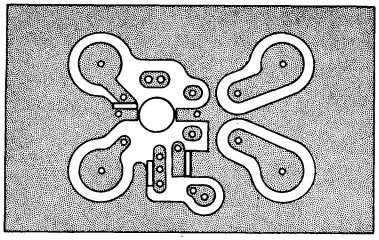


Fig. 15 – Printed-circuit board for the CA3040 wideband amplifier circuit of Fig. 8(b) using constant-gain bias configuration and balanced dual (±6-volt) power supplies; (a) top view; (b) bottom view.

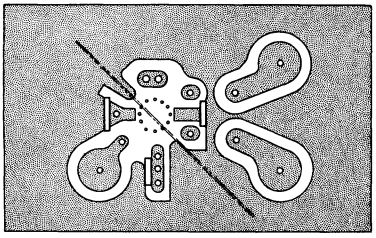
printed-board layout used for wideband applications of the CA3040. Fig. 16(a) is an exact-scale photograph of the printed board used in the circuits of Figs. 14 and 15. Figs. 16(b) and 16(c) show modifications in this board made to accommodate the different connections for the single 12-volt and balanced dual 6-volt power supplies. Fig. 16(c) shows an alternate mounting arrangement for the CA3040 in which lead connections are made through individual holes in the printed board. The printed board layout is intended for use with the constant-voltage bias connection in which terminal 7 is connected to terminal 9. Before the CA3040 is mounted, the pins for terminals 3 and 8 are cut off because they are not used in these circuits.



(a)



(b)



(c)

Fig. 16 – Printed-circuit board used for the construction of wideband amplifier circuits shown in this Note: (a) exact-scale photograph; (b) modifications required to accommodate connections for the single 12-volt dc supply; (c) modifications required to accommodate connections for balanced dual 6-volt supplies.

The balanced dual-power-supply circuit of Fig. 15 requires greater attention to layout because of the additional difficulty in bypassing the negative supply. The emitter circuits, as well as the substrate and case, of the CA3040 are common to the negative supply terminals 5 and 11. This arrangement permits the negative power-supply source impedance to become a common element for feedback. For wideband applications, however, this arrangement presents a problem for bypassing these circuit elements. The series lead inductance L in microhenries is given by

$$L = 0.005\ell\left[2.3 \log_{10}\left(\frac{4\ell}{d} - 0.75\right)\right]$$

where ℓ is the lead length and d is the lead diameter, both in inches.

Because this inductance is appreciable for some values of bypass capacitance, the circuit may resonate within the bandwidth of the amplifier. This resonance always exists and, therefore, requires extensive bypassing. As a result, the use of two and sometimes three capacitors at a bypass point is necessary for adequate bypassing of all frequencies in the pass band. In addition, the use of ferrite beads, chokes, and resistors may be necessary for suppression of "ripples" or "suck-out" in the pass band. Because of these problems a knowledge of the high-frequency self-resonant characteristics of passive circuit components up to frequencies near the unity-gain point of the amplifier device is essential. For the CA3040, this frequency may reach 800 MHz.

As an added precaution in minimizing inductance, the leads of the CA3040 should be trimmed to the minimum practical length. Lead trimming, forming, and soldering, however, should be performed at least 1/32 inch from the case to avoid damage to the package. Each lead of the CA3040 is inserted through a hole which has a sufficiently large diameter so that the lead just passes through without forcing. The leads are then folded out and soldered to their respective connections. Leadless disc capacitors are used with the circuit board slotted at the closest bypass point. The capacitors are soldered directly in vertical position to the printed board.

Fig. 17 shows the constructed wideband post amplifier in which most parts are easily identifiable. Because the case and collector lead of each 2N5187 transistor are connected together, direct bypassing to the case was used in this particular layout to reduce lead inductance in the collector circuit of the 2N5187. Leadless disc capacitors are used at critical bypass points. The terminal tie-points are teflon-insulated stand-offs. Input and output are shown as BNC connectors coupled by 0.1-microfarad disc capacitors. The output cable and 50-ohm load of Fig. 13(a) are not shown.

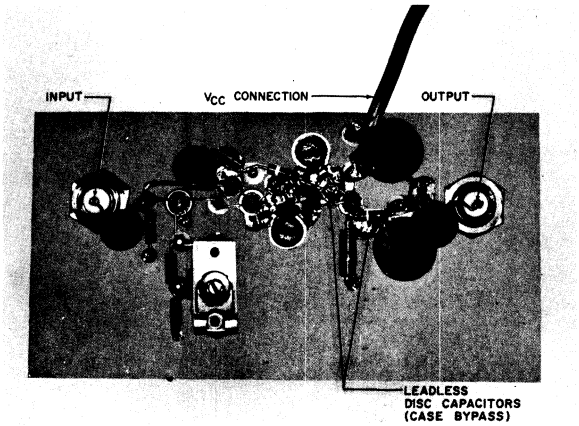


Fig. 17 – Photograph of constructed post amplifier of Fig. 13(a).

RCA Solid State Division

Linear Integrated Circuits

Application Note ICAN-6048

Some Applications of A Programmable Power Switch/Amplifier

by L. R. Campbell and H. A. Wittlinger

The RCA-CA3094 unique monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in the following circuit applications:

Class A instrumentations and power amplifiers

Class A driver-amplifier for complementary power transistors

Wide-frequency-range power multivibrators

Current- or voltage-controlled oscillators

Comparators (threshold detectors)

Voltage regulators

Analog timers (long time delays)

Alarm systems

Motor-speed controllers

Thyristor-firing circuits

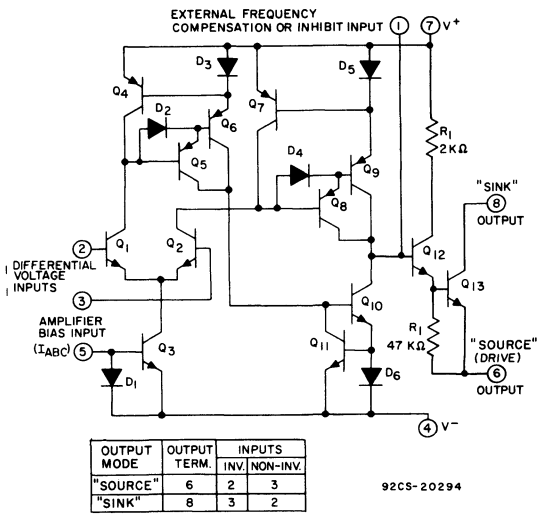
Battery-charger regulator circuits

Ground-fault-interrupter circuits

Circuit Description

The CA3094 series of devices offers a unique combination of circuit flexibility and power-handling capability. Although these monolithic IC's dissipate only a few microwatts when quiescent, they have a high current-output capability (100 milliamperes average, 300 milliamperes peak) in the active state, and the premium-grade devices can operate at supply voltages up to 44 volts.

Fig. 1 shows a schematic diagram of the CA3094. The portion of the circuit preceding transistors Q_{12} and Q_{13} is the preamplifier section and is generically similar to that of the RCA-CA3080 Operational Transconductance Amplifier (OTA).[1,2] The CA3094 circuits can be gain-programmed by either digital and/or analog signals applied to a separate Amplifier-Bias-Current (I_{ABC}) terminal (No. 5 in Fig. 1) to control circuit sensitivity. Response of the amplifier is essentially linear as a function of the current at terminal 5. This additional signal input "port" provides added flexibility in many applications. Thus, the output of the amplifier is a function of input signals applied differentially at terminals 2 and 3 and/or in a single-ended configuration at terminal 5. The output portion of the monolithic circuit in the CA3094 consists of a Darlington-connected transistor pair with access provided to both the collector and emitter terminals to provide capability to "sink" and/or "source" current.



OUTPUT MODE	OUTPUT TERM.	INPUTS INV.	INPUTS NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1—CA3094 circuit schematic diagram.

The CA3094 series of circuits consists of six types that differ only in voltage-handling capability and package options, as

shown below; other electrical characteristics are identical.

Package Options	Maximum Voltage Rating
CA3094S; CA3094T	24 V
CA3094AS; CA3094AT	36 V
CA3094BS; CA3094BT	44 V

The suffix "S" indicates circuits packaged in TO-5 enclosures with leads formed to an 8-lead dual-in-line configuration (0.1" pin spacing). The suffix "T" indicates circuits packaged in 8-lead TO-5 enclosures with straight leads. The generic CA3094 type designation is used throughout this Note.

Class A Instrumentation Amplifiers

One of the more difficult instrumentation problems frequently encountered is the conversion of a differential input signal to a single-ended output signal. Although this conversion can be accomplished in a straightforward design through the use of classical op-amps, the stringent matching requirements of resistor ratios in feedback networks make the conversion particularly difficult from a practical standpoint. Because the gain of the preamplifier section in the CA3094 can be defined as the product of the transconductance and the load resistance (g_m R_L), feedback is not needed to obtain predictable open-loop gain performance. Fig. 2 shows the CA3094 in this basic type of circuit.

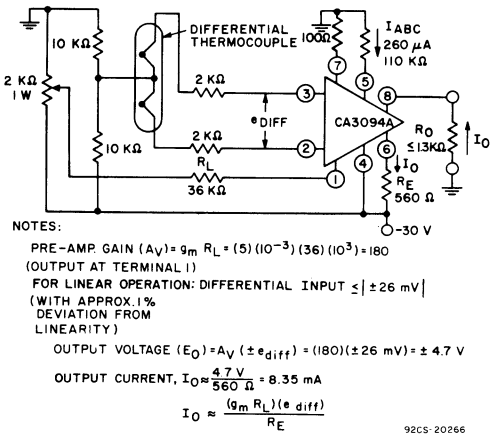


Fig.2—Open-loop instrumentation amplifier with differential input and single-ended output.

The gain of the preamplifier section (to terminal No. 1) is g_m R_L = (5 x 10^{-3}) (36 x 10^3) = 180. The transconductance g_m is a function of the current into terminal No. 5, I_{ABC}, the amplifier-bias-current. In this circuit an I_{ABC} of 260 microamperes results in a g_m of 5 millimhos. The operating point of the output stage is controlled by the 2-kilohm potentiometer. With no differential input signal (e_{diff} = 0), this potentiometer is adjusted to obtain a quiescent output current I_O of 12 milliamperes. This output current is established by the 560-ohm emitter resistor, R_E, as follows:

$$I_O \approx \frac{(g_m R_L)(e_{diff})}{R_E}$$

Under the conditions described, an input swing e_{diff} of ±26 millivolts produces a variation in the output current I_O of ±8.35 milliamperes. The nominal quiescent output voltage is 12 milliamperes times 560 ohms or 6.7 volts. This output level drifts approximately –4 millivolts, or –0.0595 per cent, for each °C change in temperature. Output drift is caused by temperature-induced variations in the base-emitter voltage of the two output transistors, Q_{12} and Q_{13}.

Fig. 3 shows the CA3094 used in conjunction with a resistive-bridge input network; and Fig. 4 shows a single-supply

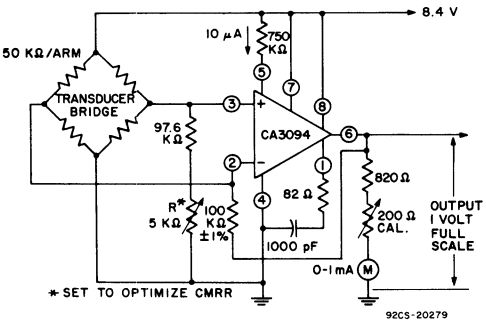


Fig.3—Single-supply differential-bridge amplifier.

amplifier for thermocouple signals. The RC networks* connected between terminals 1 and 4 in Figs. 3 and 4 provide compensation to assure stable operation.

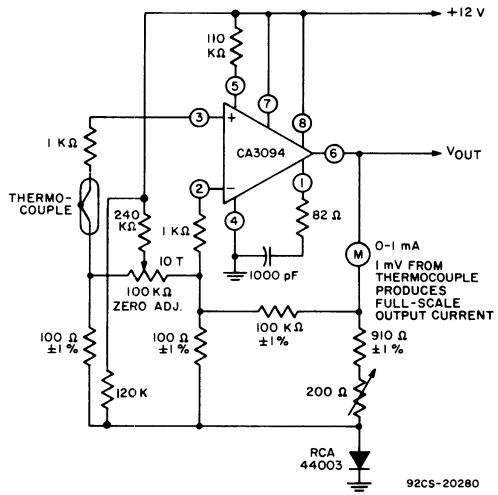


Fig.4—Single-supply amplifier for thermocouple signals.

Class A Power Amplifiers

The CA3094 is attractive for power-amplifier service because the output transistor can control current up to 100 milliamperes (300 milliamperes peak), the premium devices

*The components of the RC network are chosen so that

$$\frac{1}{2\pi RC} \approx 2 \text{ MHz}.$$

(CA3094B) can operate at supply voltages up to 44 volts, and the TO-5 package can dissipate power up to 1.6 watts when equipped with a suitable heat sink that limits the case temperature to 55°C.

Fig. 5 shows a Class A amplifier circuit using the CA3094A that is capable of delivering 280 milliwatts to a 350-ohm resistive load. This circuit has a voltage gain of 60 dB and a

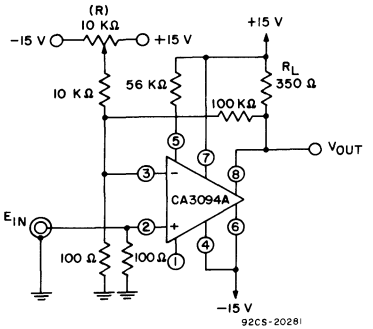


Fig.5—Class-A amplifier — 280-mW capability into a resistive load.

3-dB bandwidth of about 50 kHz. Operation is stable without the use of a phase-compensation network. Potentiometer R is used to establish the quiescent operating point for class A operation.

The circuit of Fig. 6 illustrates the use of the CA3094 in a class A power-amplifier circuit driving a transformer-coupled load. With dual power supplies of +7.5 volts and −7.5 volts, a

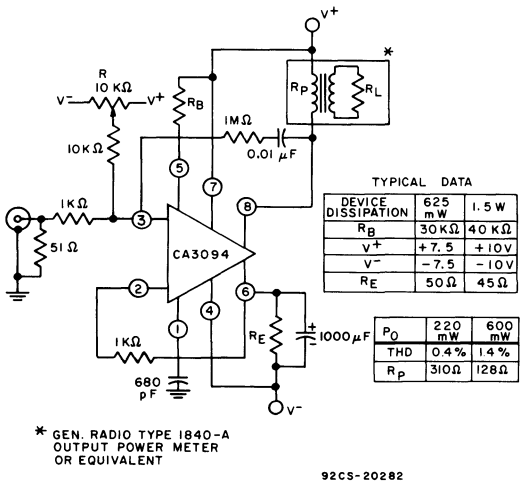


Fig.6—Class-A amplifier with transformer-coupled load.

base resistor R_B of 30 kilohms, and an emitter resistor R_E of 50 ohms, CA3094 dissipation is typically 625 milliwatts. With supplies of +10 volts and −10 volts, R_B of 40 kilohms, and R_E of 45 ohms, the dissipation is 1.5 watts. Total harmonic distortion is 0.4 per cent at a power-output level of 220 milliwatts with a reflected load resistance R_P of 310 ohms, and is 1.4 per cent for an output of 600 milliwatts with an R_P of 128 ohms. The setting of potentiometer R establishes the quiescent operating point for class A operation. The 1-kilohm resistor connected between terminals 6 and 2 provides dc feedback to stabilize the collector current of the output transistor. The ac gain is established by the ratio of the 1-megohm resistor connected between terminals 8 and 3 and the 1-kilohm resistor connected to terminal 3. Phase compensation is provided by the 680-picofarad capacitor connected to terminal 1.

Class A Driver-Amplifier for Complementary Power Transistors

The CA3094 configuration and characteristics are ideal for driving complementary power-output transistors;[3] a typical circuit is shown in Fig. 7. This circuit can provide 12 watts of audio power output into an 8-ohm load with intermodulation distortion (IMD) of 0.2 per cent when 60-Hz and 2-kHz signals are mixed in a 4:1 ratio. Intermodulation distortion is shown as a function of power output in Fig. 8.

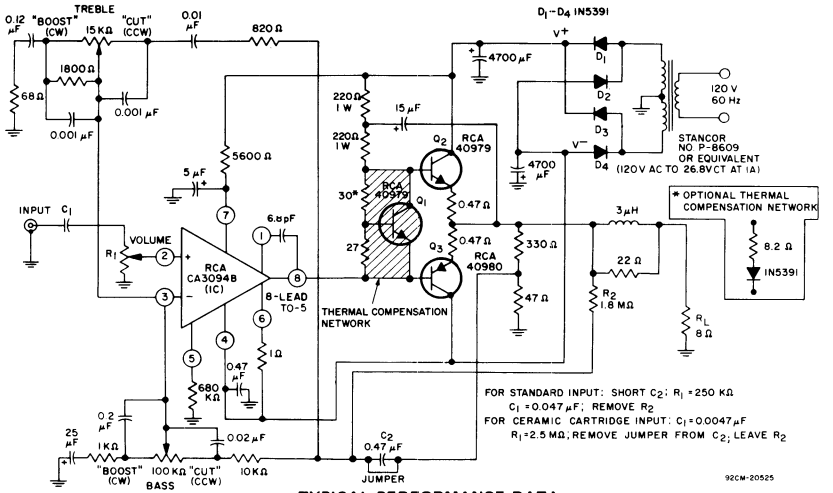
The large amount of loop gain and the flexibility of feedback arrangements with the CA3094 make it possible to incorporate the tone controls into a feedback network that is closed around the entire amplifier system. The tone controls in the circuit of Fig. 7 are part of the feedback network connected from the amplifier output (junction of the 330- and 47-ohm resistors driven by the emitters of Q_2 and Q_3) to terminal 3 of the CA3094. Fig. 9 shows voltage gain as a function of frequency with tone controls adjusted for "flat" response and for responses at the extremes of tone-control rotation. The use of tone controls incorporated in the feedback network results in excellent signal-to-noise ratio. Hum and noise are typically 700 microvolts (83 dB down) at the output.

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power-supply system. Typical values of power-supply rejection and common-mode rejection are 90 dB and 100 dB, respectively. An amplifier with 40-dB gain and 90-dB power-supply rejection would require a 31-millivolt power-supply ripple to produce one millivolt of hum at the output. Therefore, no filtering is required other than that provided by the energy-storage capacitors at the output of the rectifier system shown in Fig. 7.

For applications in which the operating temperature range is limited (e.g., consumer service) the thermal compensation network (shaded area) can be replaced by a more economical configuration consisting of a resistor-diode combination (8.2 ohms and 1N5391) as shown in Fig. 7.

Power Multivibrators (Astable and Monostable)

The CA3094 is suitable for use in power multivibrators because its high-current output transistor can drive low-impedance circuits while the input circuitry and the frequency-determining elements are operating at micropower levels. A typical example of an astable multivibrator using the CA3094 with a



TYPICAL PERFORMANCE DATA

For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9	

Fig.7—12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

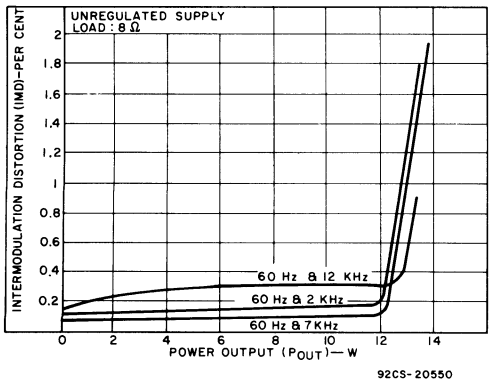


Fig.8—Intermodulation distortion vs. power output.

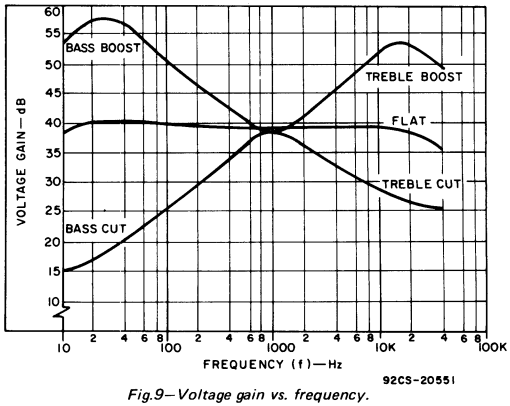


Fig.9—Voltage gain vs. frequency.

dual power supply is shown in Fig. 10. The output frequency f_{OUT} is determined as follows:

$$f_{OUT} = \frac{1}{2RC\ln[(2R1/R2) + 1]}$$

If R2 is equal to 3.08 R1, then f_{OUT} is simply the reciprocal of RC.

Fig. 11 is a single-supply astable multivibrator circuit which illustrates the use of the CA3094 for flashing an incandescent lamp. With the component values shown, this circuit produces one flash per second with a 25-per-cent "on"-time while delivering output current in excess of 100 milliamperes. During

the 75-per-cent "off"-time it idles with micropower consumption. The flashing rate can be maintained within ±2 per cent of the nominal value over a battery voltage range from 6 to 15 volts and a temperature excursion from 0 to 70°C. The CA3094 series of circuits can supply peak-power output in excess of 10 watts when used in this type of circuit. The frequency of oscillation f_{OSC} is determined by the resistor ratios, as follows:

$$f_{OSC} = \frac{1}{2RC\ln\left[(2R_1/R_2)+1\right]}$$

where

$$R1 = \frac{R_A R_B}{R_A + R_B}$$

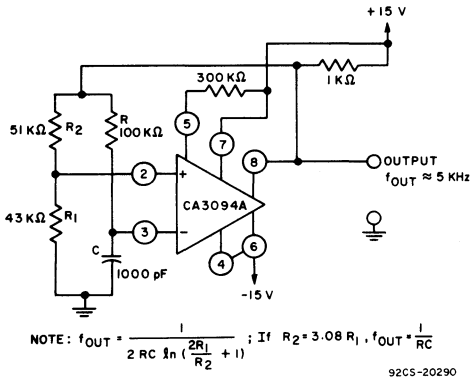


Fig. 10—Astable multivibrator using dual supply.

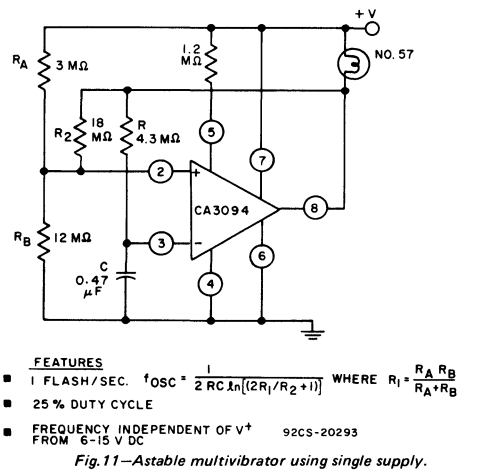


Fig. 11—Astable multivibrator using single supply.

Provisions can easily be made in the circuit of Fig. 11 to vary the multivibrator pulse length while maintaining an essentially constant pulse repetition rate. The circuit shown in Fig. 12 incorporates a potentiometer Rp for varying the width of pulses generated by the astable multivibrator to drive a light-emitting diode (LED).

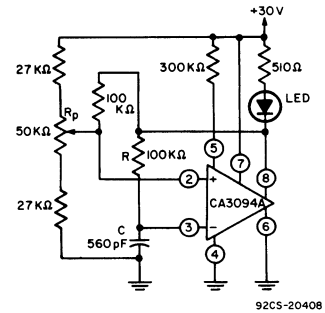


Fig. 12—Astable power multivibrator with provisions for varying duty cycle.

Fig. 13 shows a circuit incorporating independent controls (R_{ON} and R_{OFF}) to establish the "on" and "off" periods of the current supplied to the LED. The network between points "A" and "B" is analogous in function to that of the 100-kilohm resistor R in Fig. 12.

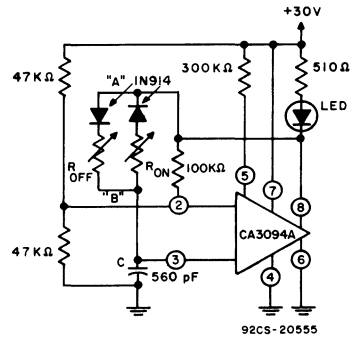


Fig. 13—Astable power multivibrator with provisions for independent control of LED "on-off" periods.

The CA3094 is also suitable for use in monostable multivibrators, as shown in Fig. 14. In essence, this circuit is a pulse counter in which the duration of the output pulses is independent of trigger-pulse duration. The meter reading is a function of the pulse repetition rate which can be monitored with the speaker.

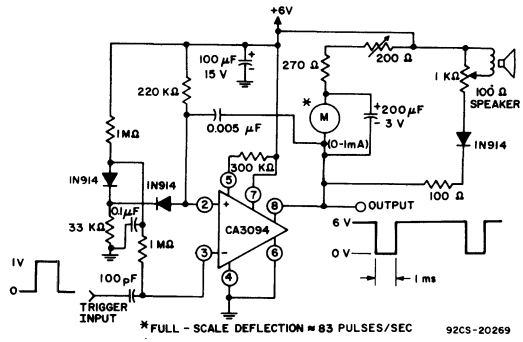


Fig. 14—Power monostable multivibrator.

Current- or Voltage-Controlled Oscillators

Because the transconductance of the CA3094 varies linearly as a function of the amplifier bias current (I_{ABC}) supplied to terminal 5, the design of a current- or voltage-controlled oscillator is straightforward, as shown in Fig. 15. Fig. 16 and 17 show oscillator frequency as a function of I_{ABC} for a current-controlled oscillator for two different values of capacitor C in Fig. 15. The addition of an appropriate resistor (R) in series with terminal 5 in Fig. 15 converts the circuit into a voltage-controlled oscillator. Linearity with respect to either current or voltage control is within 1 per cent over the middle half of the characteristics. However, variation in the symmetry of the output pulses as a function of frequency is an inherent characteristic of the circuit in Fig. 15, and leads to distortion when this circuit is used to drive the phase detector in phase-locked-loop applications. This type of distortion can be eliminated by interposing an appropriate flip-flop between the output of the oscillator and the phase-locked discriminator circuits.

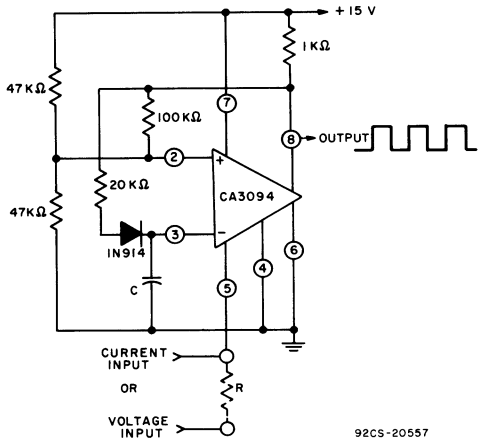


Fig. 15—Current- or voltage-controlled oscillator.

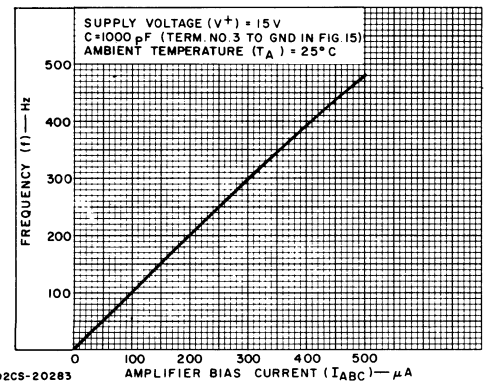


Fig. 16—Frequency as a function of I_{ABC} for C=1000 pF for circuit in Fig. 15.

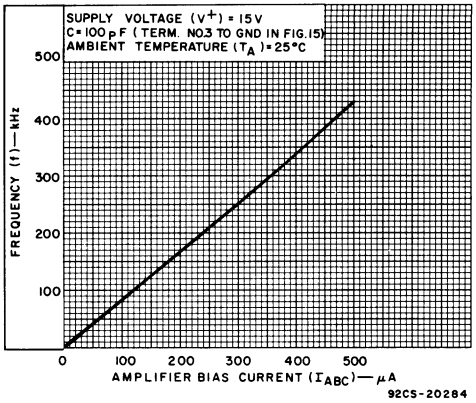


Fig. 17—Frequency as a function of I_{ABC} for C=100 pF for circuit in Fig. 15.

Comparators (Threshold Detectors)

Comparator circuits are easily implemented with the CA3094, as shown by the circuits in Fig. 18. The circuit of Fig. 18(a) is arranged for dual-supply operation; the input voltage exceeds the positive threshold, the output voltage swings essentially to the negative supply-voltage rail (it is assumed that there is negligible resistive loading on the output ter-

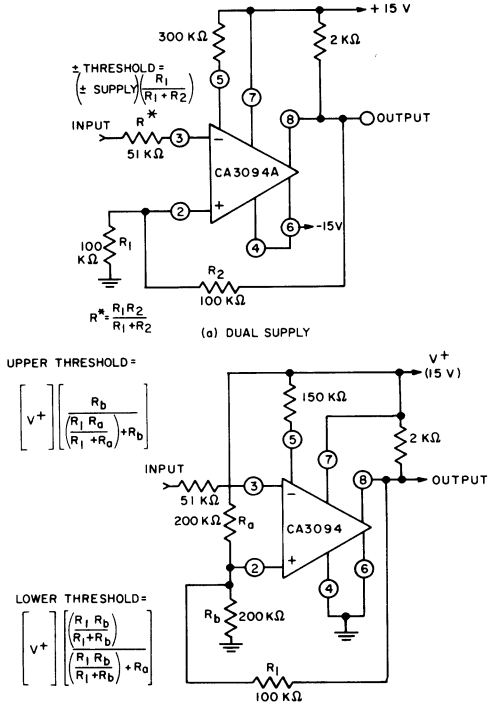


Fig. 18—Comparators (threshold detectors) — dual- and single-supply types.

minal). An input voltage that exceeds the negative threshold value results in a positive voltage output essentially equal to the positive supply voltage. The circuit in Fig. 18(b), connected for single-supply operation, functions similarly.

Fig. 19 shows a dual-limit threshold detector circuit in which the high-level limit is established by potentiometer R1

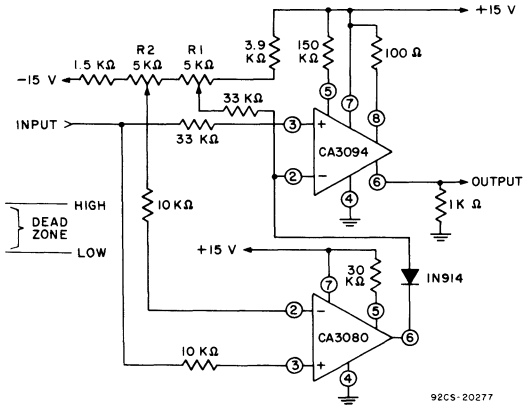


Fig. 19—Dual-limit threshold detector.

and the low-level limit is set by potentiometer R2 to actuate the CA3080 low-limit detector.[1,2] A positive output signal is delivered by the CA3094 whenever the input signal exceeds either the high-limit or the low-limit values established by the appropriate potentiometer settings. This output voltage is approximately 12 volts with the circuit shown.

The high current-handling capability of the CA3094 makes it useful in Schmitt power-trigger circuits such as that shown in Fig. 20. In this circuit, a relay coil is switched whenever the

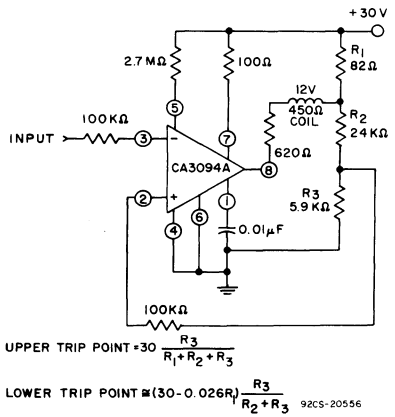


Fig. 20—Precision Schmitt power-trigger circuit.

input signal traverses a prescribed upper or lower trip point, as defined by the following expressions:

$$\text{Upper Trip Point} = 30\left(\frac{R3}{R1 + R2 + R3}\right)$$

$$\text{Lower Trip Point} \cong (30 - 0.026R1)\frac{R3}{R2 + R3}$$

The circuit is applicable, for example, to automatic ranging. With the values shown in Fig. 20, the relay coil is energized when the input exceeds approximately 5.9 volts and remains energized until the input signal drops below approximately 5.5 volts.

Power-Supply Regulators

The CA3094 is an ideal companion device to the CA3085 series regulator circuits[4] in dual-voltage tracking regulators that handle currents up to 100 milliamperes. In the circuit of Fig. 21, the magnitude of the regulated positive voltage provided by the CA3085A is adjusted by potentiometer R. A sample of this positive regulated voltage supplies the power for the CA3094A negative regulator and also supplies a refer-

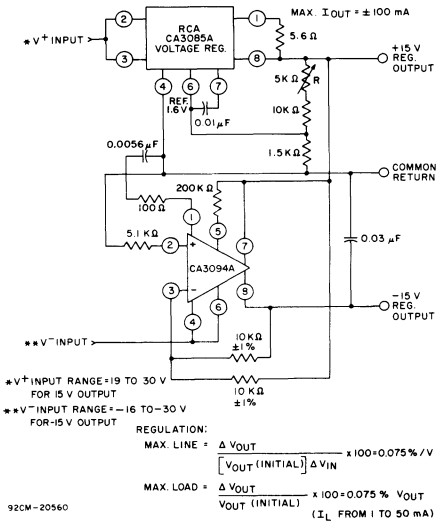


Fig. 21—Dual-voltage tracking regulator.

ence voltage to its terminal 3 to provide tracking. This circuit provides a maximum line regulation equal to 0.075 per cent per volt of input voltage change and a maximum load regula- of 0.075 per cent of the output voltage.

Fig. 22 shows a regulated high-voltage supply similar to the type used to supply power for Geiger-Mueller tubes. The CA3094, used as an oscillator, drives a step-up transformer which develops suitable high voltages for rectification in the RCA-44007 diode network. A sample of the regulated output voltage is fed to the CA3080A operational transconductance amplifier through the 198-megohm and 910-kilohm divider to control the pulse repetition rate of the CA3094. Adjustment of potentiometer R determines the magnitude of the regulated output voltage. Regulation of the desired output voltage is maintained within one per cent despite load-current variations of 5 to 26 microamperes. The dc-to-dc conversion efficiency is about 48 per cent.

Timers

The programmability feature inherent in the CA3094 (and operational transconductance amplifiers in general) simplifies the design of presettable timers such as the one shown in

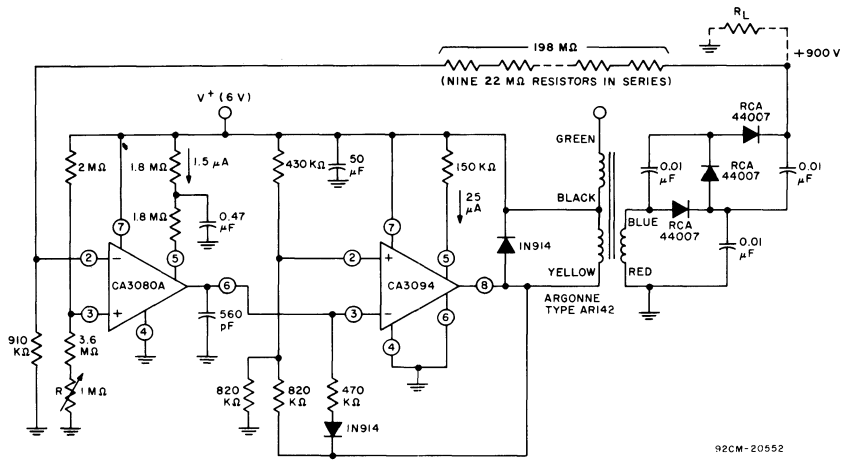


Fig.22—Regulated high-voltage supply.

Fig. 23. Long timing intervals (e.g., up to 4 hours) are achieved by discharging a timing capacitor C_1 into the signal-input terminal (e.g., No. 3) of the CA3094. This discharge current is controlled precisely by the magnitude of the amplifier bias current I_{ABC} programmed into terminal 5 through a resistor selected by switch S2. Operation of the circuit is initiated by charging capacitor C_1 through the momentary closing of switch S_1. Capacitor C_1 starts discharging and continues discharging until voltage E_1 is less than voltage E_2. The differential input transistors in the CA3094 then change state, and terminal 2 draws sufficient current to reverse the polarity of

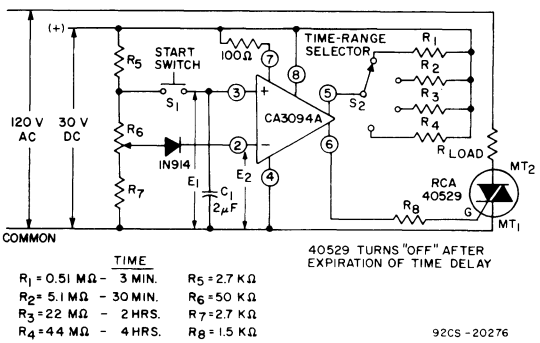


Fig.23—Presettable analog timer.

the output voltage (terminal 6). Thus, the CA3094 not only has provision for readily presetting the time delay, but also provides significant output current to drive control devices such as thyristors. Resistor R_5 limits the initial charging current for C_1. Resistor R_7 establishes a minimum voltage of at least 1 volt at terminal 2 to insure operation within the common-mode-input range of the device. The diode limits the maximum differential input voltage to 5 volts. Gross changes in time-range selection are made with switch S2, and vernier trimming adjustments are made with potentiometer R_6.

In some timer applications, such as that shown in Fig. 24, a meter readout of the elapsed time is desirable. This circuit uses the CA3094 and the CA3083 transistor array[5] to control the meter and a load-switching triac. The timing cycle starts with the momentary closing of the start switch to charge capacitor C_1 to an initial voltage determined by the 50-kilohm vernier timing adjustment. During the timing cycle, capacitor C_1 is discharged by the input bias current at terminal 3, which is a function of the resistor value R_1 chosen by the time-range selection switch. During the timing cycle the output of the CA3094, which is also the collector voltage of Q_1, is "high". The base drive for Q_1 is supplied from the positive supply through a 91-kilohm resistor. The emitter of Q_1, through the 75-ohm resistor, supplies gate-trigger current to the triac. Diode-connected transistors Q_4 and Q_5 are connected so that transistor Q_1 acts as a constant-current source to drive the triac. As capacitor C_1 discharges, the CA3094 output voltage at terminal 6 decreases until it becomes less than the V_{CEsat} of Q_1. At this point the flow of drive current to the triac ceases and the timing cycle is ended. The 20-kilohm resistor between terminals 2 and 6 of the CA3094 is a feedback resistor. Diode-connected transistors Q_2 and Q_3 and their associated networks serve to compensate for nonlinearities in the discharge-circuit network by bleeding corrective current into the 20-kilohm feedback resistor. Thus, current flow in the meter is essentially linear with respect to the timing period. The time periods as a function of R_1 are indicated on the Time-Range Selection Switch in Fig. 24.

Alarm Circuit

Fig. 25 shows an alarm circuit utilizing two "sensor" lines. In the "no-alarm" state, the potential at terminal 2 is lower than the potential at terminal 3, and terminal 5 (I_{ABC}) is driven with sufficient current through resistor R_5 to keep the output voltage "high". If either "sensor" line is opened, shorted to ground, or shorted to the other sensor line, the output goes "low" and activates some type of alarm system.

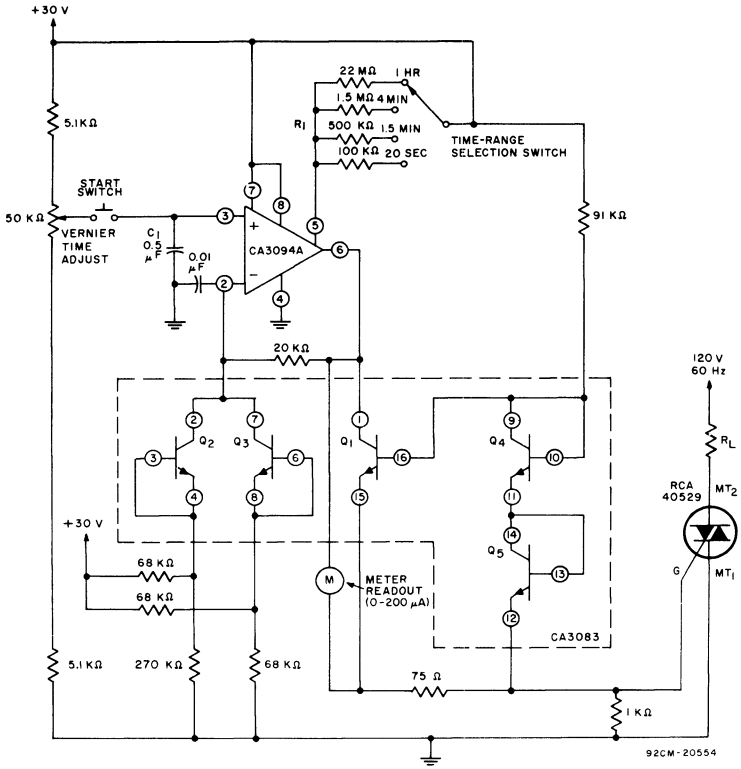


Fig.24—Presettable timer with linear readout.

The back-to-back diodes connected between terminals 2 and 3 protect the CA3094 input terminals against excessive differential voltages.

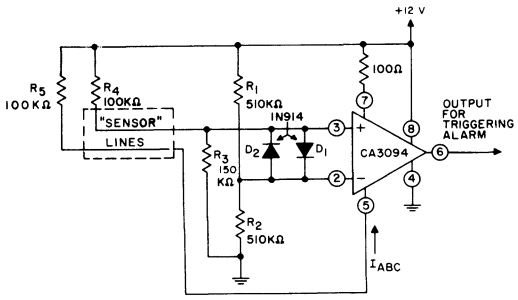


Fig.25—Alarm system.

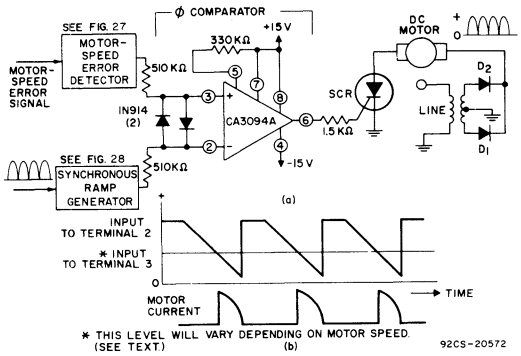


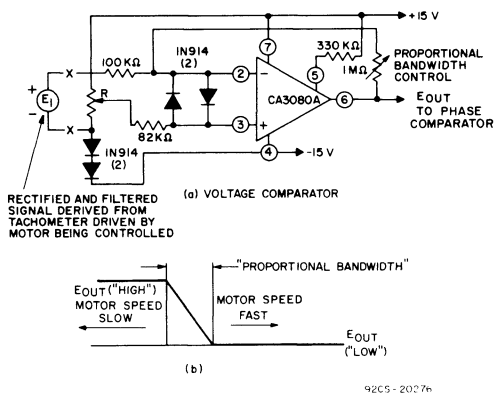
Fig.26—Motor-speed controller system.

Motor-Speed Controller System

Fig. 26 illustrates the use of the CA3094 in a motor-speed controller system. Circuitry associated with rectifiers D_1 and D_2 comprises a full-wave rectifier which develops a train of half-sinusoid voltage pulses to power the dc motor. The motor speed depends on the peak value of the half-sinusoids and the period of time (during each half-cycle) the SCR is conductive. The SCR conduction, in turn, is controlled by the time duration of the positive signal supplied to the SCR by the phase comparator. The magnitude of the positive dc voltage supplied to terminal 3 of the phase comparator depends on motor-speed error as detected by a circuit such as that shown in Fig. 27. This dc voltage is compared to that of a fixed-amplitude ramp wave generated synchronously with the ac-line-voltage frequency. The comparator output at terminal 6 is "high" (to trigger the SCR into conduction) during the period

when the ramp potential is less than that of the error voltage on terminal 3. The motor-current conduction period is increased as the error voltage at terminal 3 is increased in the positive direction. Motor-speed accuracy of ±1 per cent is easily obtained with this system.

Motor-Speed Error Detector. Fig. 27(a) shows a motor-speed error detector suitable for use with the circuit of Fig. 26. A CA3080 operational transconductance amplifier is used as a voltage comparator. The reference for the comparator is established by setting the potentiometer R so that the voltage at terminal 3 is more positive than that at terminal 2 when the motor speed is too low. An error voltage E_1 is derived from a tachometer driven by the motor. When the motor speed is too low, the voltage at terminal 2 of the voltage comparator is less positive than that at terminal 3, and the output voltage at terminal 6 goes "high". When the motor speed is too high, the opposite input conditions exist, and the output voltage at terminal 6 goes "low". Fig. 27(b) also shows these conditions graphically, with a linear transition region between the "high" and "low" output levels. This linear transition region is known as "proportional bandwidth". The slope of this region is determined by the proportional bandwidth control to establish the error-correction response time.



Synchronous Ramp Generator. Fig. 28 shows a schematic diagram and signal waveforms for a synchronous ramp generator suitable for use with the motor-controller circuit of Fig. 26. Terminal 3 is biased at approximately +2.7 volts (above the negative supply voltage). The input signal E_{IN} at terminal 2 is a sample of the half-sinusoids (at line frequency) used to power the motor in Fig. 26. A synchronous ramp signal is produced by using the CA3094 to charge and discharge capacitor C_1 in response to the synchronous toggling of E_{IN}. The charging current for C_1 is supplied by terminal 6. When terminal 2 swings more positive than terminal 3, transistors Q_{12} and Q_{13} in the CA3094 (Fig. 1) lose their base drive and become non-conductive. Under these conditions, C_1 discharges linearly through the external diode D_3 and the Q_{10}, D_6 path in the CA3094 to produce the ramp wave. The E_{out} signal is supplied to the phase comparator in Fig. 26.

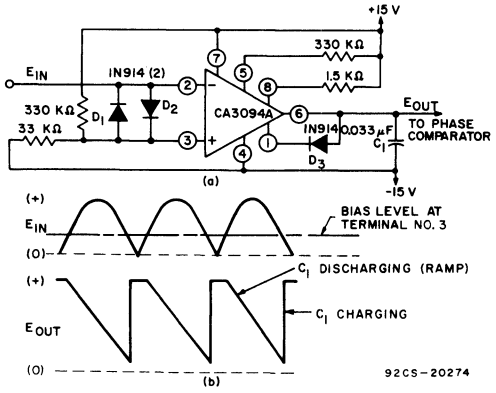


Fig.28—Synchronous ramp generator with input and output waveforms.

Thyristor Firing Circuits

Temperature Controller. In the temperature control system shown in Fig. 29, the differential input of the CA3094 is connected across a bridge circuit comprised of a PTC (positive-temperature-coefficient) temperature sensor, two 75-kilohm resistors, and an arm containing the temperature set control. When the temperature is "low", the resistance of the PTC-type sensor is also low; therefore, terminal 3 is more positive than terminal 2 and an output current from terminal 6 of the CA3094 drives the triac into conduction. When the temperature is "high", the input conditions are reversed and the triac is cut off. Feedback from terminal 8 provides hysteresis to the control point to prevent rapid cycling of the system. The 1.5-kilohm resistor between terminal 8 and the positive supply limits the triac gate current and develops the voltage for the hysteresis feedback. The excellent power-supply-rejection and common-mode-rejection ratios of the CA3094 permit accurate repeatability of control despite appreciable power-supply ripple. The circuit of Fig. 29 is equally suitable for use with NTC (negative-temperature-coefficient) sensors provided the positions of the sensor and the associated resistor R are interchanged in the circuit. The diodes connected back-to-back across the input terminals of the CA3094 protect the device against excessive differential input signals.

Thyristor Control from AC-Bridge Sensor. Fig. 30 shows a line-operated thyristor-firing circuit controlled by a CA3094 that operates from an ac-bridge sensor. This circuit is particularly suited to certain classes of sensors that cannot be operated from dc. The CA3094 is inoperative when the high side of the ac line is negative because there is no I_{ABC} supply to terminal 5. When the sensor bridge is unbalanced so that terminal 2 is more positive than terminal 3, the output stage of the CA3094 is cut off when the ac line swings positive, and the output level at terminal 8 of the CA3094 goes "high". Current from the line flows through the 1N3193 diode to charge the 100-microfarad reservoir capacitor, and also provides current to drive the triac into conduction. During the succeeding negative swing of the ac line, there is sufficient remanent energy in the reservoir capacitor to maintain conduction in the triac.

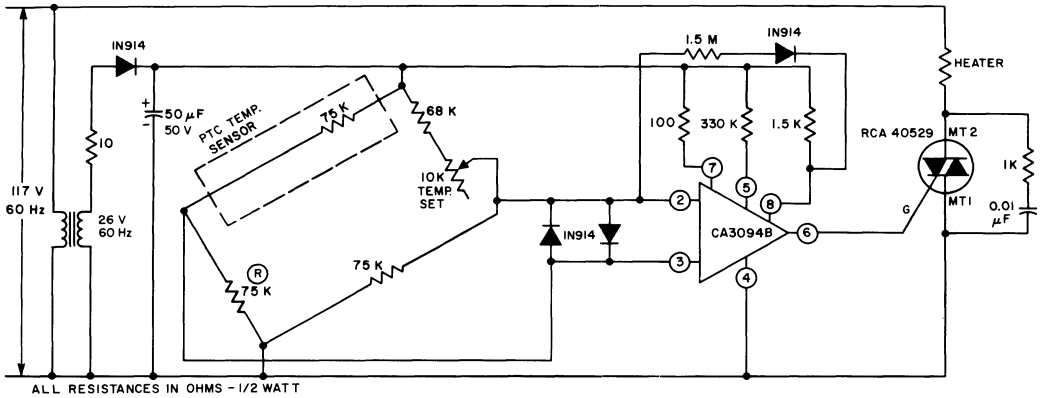
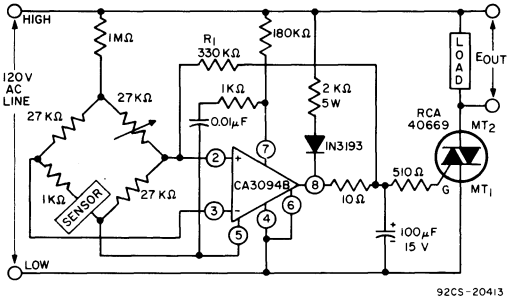


Fig.29—Temperature controller.

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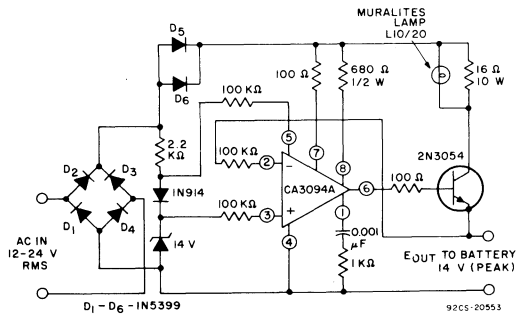
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Fig.30—Line-operated thyristor-firing circuit controlled by ac-bridge sensor.

When the bridge is unbalanced in the opposite direction so that terminal 3 is more positive than terminal 2, the output of the CA3094 at terminal 8 is driven sufficiently "low" to "sink" the current supplied through the 1N3193 diode so that the triac gate cannot be triggered. Resistor R_1 supplies the hysteresis feedback to prevent rapid cycling between turn-on and turn-off.

Battery-Charger Regulator Circuit

The circuit for a battery-charger regulator circuit using the CA3094 is shown in Fig. 31. This circuit accurately limits the peak output voltage to 14 volts, as established by the zener diode connected across terminals 3 and 4. When the output voltage rises slightly above 14 volts, signal feedback through a 100-kilohm resistor to terminal 2 reduces the current drive supplied to the 2N3054 pass transistor from terminal 6 of the CA3094. An incandescent lamp serves as the indicator of charging-current flow. Adequate limiting provisions protect the circuit against damage under load-short conditions. The advantage of this circuit over certain other types of regulator circuits is that the reference voltage supply doesn't drain the battery when the power supply is disconnected. This feature is important in portable service applications, such as in a trailer where a battery is kept "on-charge" when the trailer is parked and power is provided from an ac line.



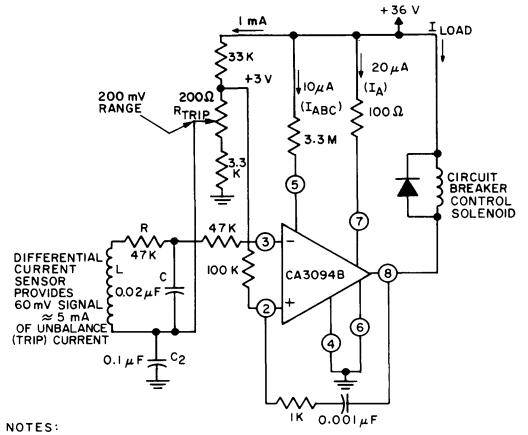
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Fig.31—Battery-charger regulator circuit.

Ground-Fault Interrupters (GFI)

Ground-fault-interrupter systems are used to continuously monitor the balance of current between the high and neutral lines of power-distribution networks. Power is interrupted whenever the unbalance exceeds a preset value (e.g., 5 milliamperes). An unbalance of current can occur when, for example, defective insulation in the high side of the line permits leakage of current to an earth ground. GFI systems can be used to reduce the danger of electrocution from accidental contact with a "high" line because the unbalance caused by the leakage of current from the "high" line through a human body to ground results in an interruption of current flow.

The CA3094 is ideally suited for GFI applications because it can be operated from a single supply, has adequate sensitivity, and can drive a relay or thyristor directly to effect power interruption. Fig. 32 shows a typical GFI circuit. Vernier adjustment of the trip point is made by the R_{TRIP} potentiometer. When the differential current sensor supplies a signal that exceeds the selected trip-point voltage level (e.g., 60 millivolts), the CA3094 is toggled "on" and terminal 8 goes "low" to energize the circuit-breaker trip coil. Under quiescent conditions, the entire circuit consumes approximately 1 milliampere. The resistor R, connected to one leg of the current sensor, provides current limiting to protect the CA3094 against voltage spikes as large as 100 volts. Fig. 32 also shows the pertinent waveform for the GFI circuit.



NOTES:

1. ALL RESISTORS IN OHMS, 1/2 WATT, ±10%
2. RC SELECTED FOR 3db POINT AT 200 Hz
3. C_2 = AC BY-PASS
4. OFFSET ADJ. INCLUDED IN R_{TRIP}
5. INPUT IMPEDANCE FROM 2 TO 3 EQUALS 800 K.
6. WITH NO INPUT SIGNAL TERMINAL 8 (OUTPUT) AT +36 VOLTS

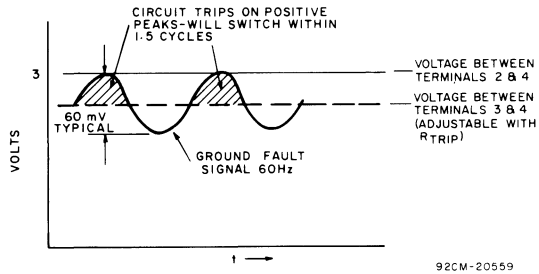


Fig.32—Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

Because hazards of severe electrical shock are a potential danger to the individual user in the event of malfunctions in GFI apparatus, it is mandatory that the highest standards of good engineering practice be employed in designing equipment for this service. Every consideration in design and application must be given to the potentially serious consequences of component malfunction in such equipment. Use of "reliability-through-redundancy" concepts and so-called "fail-safe" features is encouraged.

Acknowledgments

The authors thank A. Sheng and R. Baird for their assistance in designing some of the circuits described in this Note.

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3. L. Kaplan and H. A. Wittlinger, "An IC Operational-Transconductance-Amplifier (OTA) with Power Capability". Paper originally presented at the IEEE Chicago Spring Conference on Broadcast and TV Receivers, June 1972. Reprinted by the RCA Solid State Division as Publication No. ST-6077.
4. RCA Published Data for CA3085, File No. 491.
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Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC

By O. H. Schade, Jr.

RCA COS/MOS integrated circuits have demonstrated outstanding performance in a wide variety of DIGITAL applications. Simplified circuitry, design flexibility, low power consumption, moderate speed, and high noise immunity of these devices can complement the high transconductance of bipolar IC's in an extension to LINEAR signal processing applications. This Note demonstrates the use of the RCA-CD4007A COS/MOS Dual Complementary Pair Plus Inverter as the Digital-to-Analog (D/A) switch and op-amp output stage for a Digital-to-Analog Converter (DAC).

General Considerations

In combination with a p-channel input pair (two p-channels of the CD4007A), a buffer-follower COS/MOS-bipolar op-amp has been designed with the capability to attain essentially the negative supply voltage at both the input and output terminals. Therefore, to consider inexpensive single-supply operation becomes possible without the sacrifice of speed and bandwidth that results with many monolithic bipolar IC op-amps. An additional advantage is the use of an MOS input stage to provide exceptionally high input resistance and low input current.

A 9-bit DAC is described in this Note to illustrate this design approach. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide film resistors, a COS/MOS-bipolar op-amp follower, and an inexpensive monolithic regulator in a simple single-supply system. An additional feature which complements the ever-increasing use of COS/MOS IC's for digital signal processing is the readily interfaced COS/MOS-DAC input logic.

Although the accuracy of a DAC system depends on many factors, it is the ladder network which must initiate properly-proportioned current or voltage outputs. Recognition of various ladder types and an appreciation of the design flexibility and constraints are paramount to a well executed DAC development.

Resistance Networks for DAC's

Ladder networks for DAC's can take many forms, although three types are most generally encountered. Among the best-known variations is the current ladder shown in Fig. 1. This network is frequently used in combination with bipolar current switches which utilize a reference potential at the transistor base terminals to establish emitter currents having binary proportions. Because current summing is accomplished at the collectors of these transistors, the extent of V_{BE}- and beta-matching of these transistors depends on the degree of accuracy and temperature-range requirements. The use of a 10/20/40/80 –kΩ network in conjunction with a "quad" switch, a follower amplifier, and dual power supplies is common.

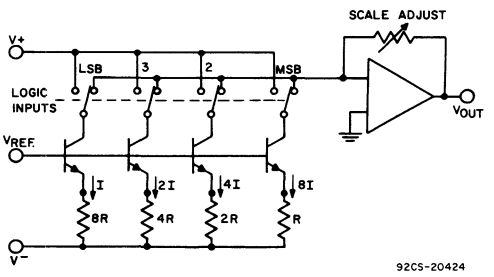


Fig. 1– Current ladder-network for bipolar DAC.

Fig. 2 shows an R/2R current ladder commonly employed in monolithic DAC's. Similar resistance values can simplify the problem of meeting ratio-match accuracy requirements. This ladder must be terminated in a single potential (or at least invariable values) to maintain proper current proportions. Although the *absolute* resistance values of the circuit in Fig. 1 must temperature track the summing resistor (or additional compensation must be employed), the R/2R current ladder must maintain only a resistance *ratio;* it is the current sink which must remain stable under external influences.

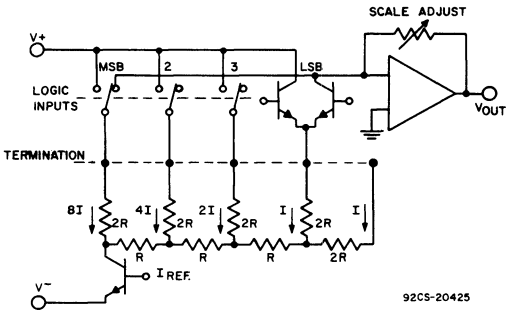


Fig. 2– R/2R current ladder-network for monolithic DAC.

Fig. 3 shows a less common *voltage* ladder suitable for DAC's using COS/MOS switches. Output potentials are obtained directly by terminating the ladder arms at either the positive or the negative power supply. Each COS/MOS inverter output pair functions as a double-throw switch. If the switch (channel) resistance is kept small compared to the ladder-arm resistance value, accuracy becomes a function of ladder supply voltage and resistance ratios alone. Operation of this ladder is *dynamic;* the current in an arm reverses as the logic state changes. Therefore, stray capacitances (or the inductance of a wirewound resistor) can limit speed as a result of typical settling times of several microseconds. However, the proper selection of parallel connection of switches for the most significant bit (MSB) to minimize channel resistance can result in COS/MOS-DAC speeds which approach those of the best bipolar systems, particularly when consideration is given to follower-amplifier speed limitations.

In the illustrative 9-bit application, a modified voltage-ladder design is employed. The use of 1%-tolerance metal-oxide film resistors can result in inexpensive networks suitable to about the 10-bit level. Such networks are readily constructed for system evaluations and may also prove to be suitable for production. Practical tolerance considerations call for variations from the "pure" R/2R configuration, as discussed later.

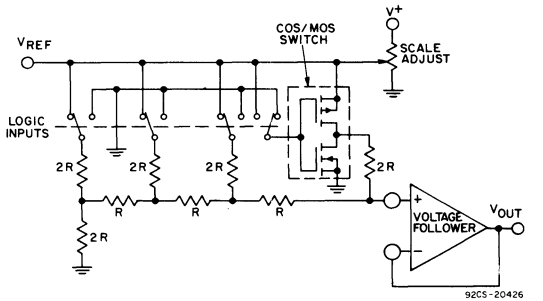


Fig. 3– R/2R voltage ladder-network for COS/MOS DAC.

TRIGGER

The COS/MOS Switch

A typical COS/MOS switch (CD4007A) is shown in Fig. 4. A change in input logic level causes the output to swing to either the positive or the negative supply voltage. Power consumption is low, typically a few microwatts to a few milliwatts, depending on the ladder resistance and voltage choice. Large DAC ladder resistance values can be used to minimize the effects of switch resistance. Fig. 5 shows the minimum ladder resistance value for a given saturation resistance to produce an accuracy of 1/2 LSB (Least Significant Bit), with bit number as a parameter. For example, the CD4007A which has a channel resistance of approximately 250-ohms (V_{DD} = 10 V), requires a minimum ladder resistance of 100 kΩ to maintain a 9-bit accuracy level. Reference to the dashed "settling time" line and the rightside ordinate shows that the approximate settling time of such a network having a 10-pF node capacitance is 6 μs. This settling time has been based on six time constants for settling to 1/2 LSB, an *average* value for the bit range illustrated. If a faster settling time is required, circuits employing the RCA-CD4041A can be used.

The CD4041A● can drive (in a theoretical example) a 4–kΩ, 6-bit ladder network which has a settling time of approximately 250 ns. This is as fast as the *best* presently available monolithic bipolar switches. High-slew-rate voltage-follower amplifiers are needed to maintain these speed levels; when the CD4007A is used the slew rate is approximately 30 V/μs and the settling time is several hundred nanoseconds for a 10-V full-scale signal. This performance approaches the state-of-the-art for monolithic op-amps, especially in low-cost systems. In fact, high-speed op-amps capable of swinging to the negative supply have not generally been available.

A Voltage-Follower Amplifier for Single-Supply Operation

It is practical to utilize commercially available COS/MOS and bipolar transistor-array IC's to provide a composite op-amp suitable for single-supply DAC systems. Fig. 6 shows a unity-gain follower amplifier having a COS/MOS p-channel input, an n-p-n second gain stage, and a COS/MOS inverter output. The IC building blocks are two CD4007A's and a CA3083 n-p-n transistor array. A zener-regulated leg provides bias for a 400-μA p-channel current source feeding the input stage, which is terminated in an n-p-n current mirror. Amplifier voltage-offset is nulled with the 10-kΩ balance potentiometer. The second-stage current level is established by the 20-kΩ load, and is selected to approximate the first-stage current level, to assure similar positive and negative slew rates. The COS/MOS inverter portion forms the final output stage and is terminated in a 2-kΩ load, a typical value used with monolithic op-amps. Voltage gain is affected by the choice of load resistance value. The output stage of this amplifier is easily driven to within 1 mV of the negative supply voltage.

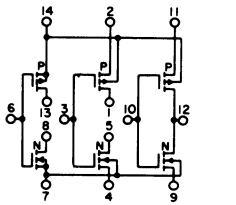


Fig. 4– CD4007A schematic diagram.

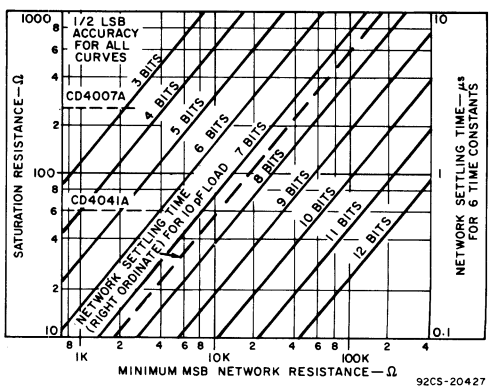


Fig. 5– COS/MOS-DAC voltage-network requirements.

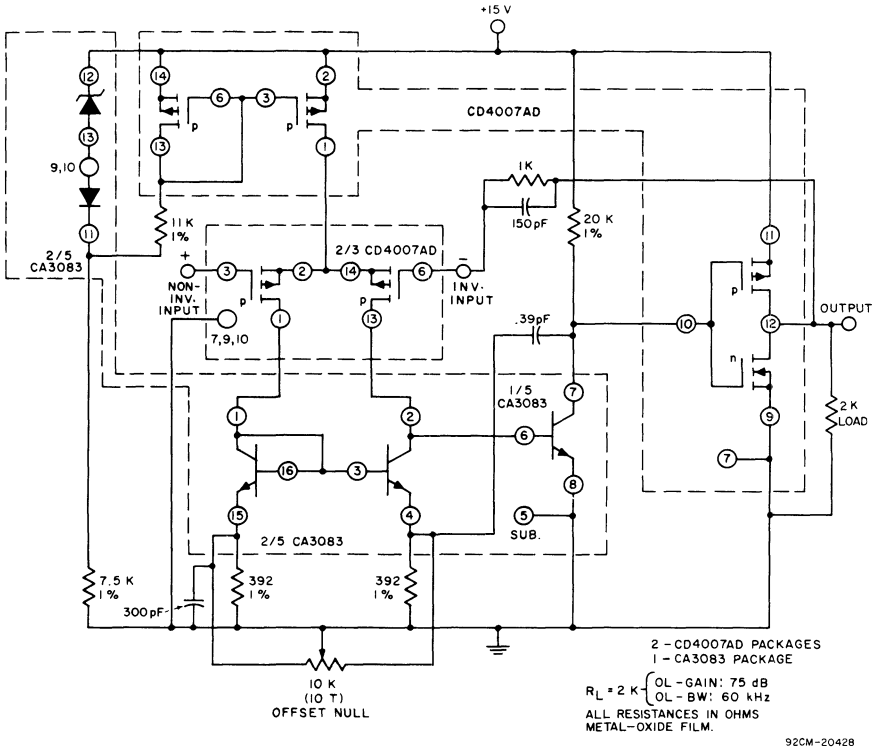


Fig. 6— Voltage-follower amplifier for single-supply operation.

Compensation for the unity-gain non-inverting mode is provided by Miller feedback of 39 pF and a 300-pF by-pass capacitor shunting one-half the driving current (1-2 MHz). Unity-gain bandwidth is just under 10 MHz and the open-loop gain is 75 dB. Fig. 7 shows the gain-bandwidth characteristics for this circuit. A potential latch situation at the bipolar mirror is avoided by use of resistor-capacitor network (R = 1 k Ω, C = 150 pF), which limits the dc feedback through the p-channel gate-protective diode.

The amplifier response to 4-V input pulses is shown in Fig. 8. Although the slew rate is approximately 30 V/μs, the settling time is significantly prolonged (approximately 2 μs) as a result of the method of second-stage biasing when the output swings near the negative supply. For many applications, this speed loss is not significant. If a faster amplifier is desired, the load resistor can be replaced with a p-channel CD4007A current source similar to that used for the first stage. In fact, it may be desirable to change the current and resistance values to optimize the gain/speed trade-off for a particular application. For example, if higher gain is desired for less follower offset, the 20-kΩ resistance value can be increased. The choice of output load resistance also affects the gain/speed compromise.

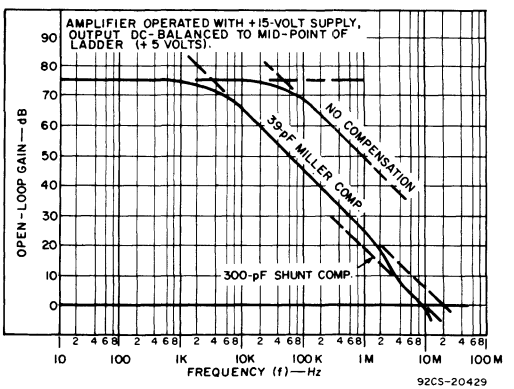


Fig. 7— Voltage-follower open-loop gain characteristics.

A 9-Bit COS/MOS DAC

An example of a 9-bit DAC is shown in Fig. 9. Three CD4007A IC packages perform the switch function using a 10-V logic level. A single 15-V supply provides a positive bus for the follower amplifier and feeds the CA3085 voltage regulator. The "scale-adjust" function is provided by the regulator output control which is set to a nominal 10 V in this system. The line-voltage regulation (approximately 0.2%) permits 9-bit accuracy to be maintained with a variation of several volts in the supply. System power consumption ranges between 70 and 200 mW; a major portion is dissipated in the load resistor and op-amp. The regulated supply provides a maximum current of 440 μA of which 370 μA flows through the scale-adjust leg.

The resistor ladder is composed of 1-per-cent tolerance metal-oxide film resistors available from several manufacturers at modest cost. The five arms requiring the highest accuracy are built of series and parallel combinations of 806-kΩ resistors from the same manufacturing lot. The *ratio match* between resistance values is in the order of 0.2%, usually without need for special selection. The construction of a "standard" with eight parallel resistors assures a high probability that ratio matching will be satisfactory. If the usual assumption that tolerances can be improved with the square-root of the sample number is adopted, the loss of tolerance is slower than the increase of resistance value toward the LSB. Once the most critical match has been attained, therefore, subsequent ratio matches should be more than adequate. An impedance-matching resistor is used between the fifth and sixth bits to permit ladder completion with individual resistors of the most desirable values where a 1% tolerance is adequate. This resistor value is chosen as R5-1/2R6, to terminate the first five bits in a fifth-bit value (the impedance is 1/2R6 looking left into that node).

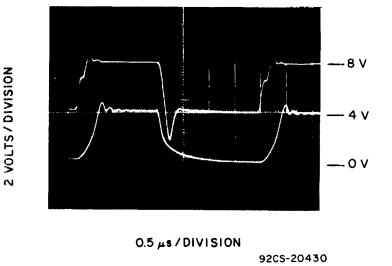
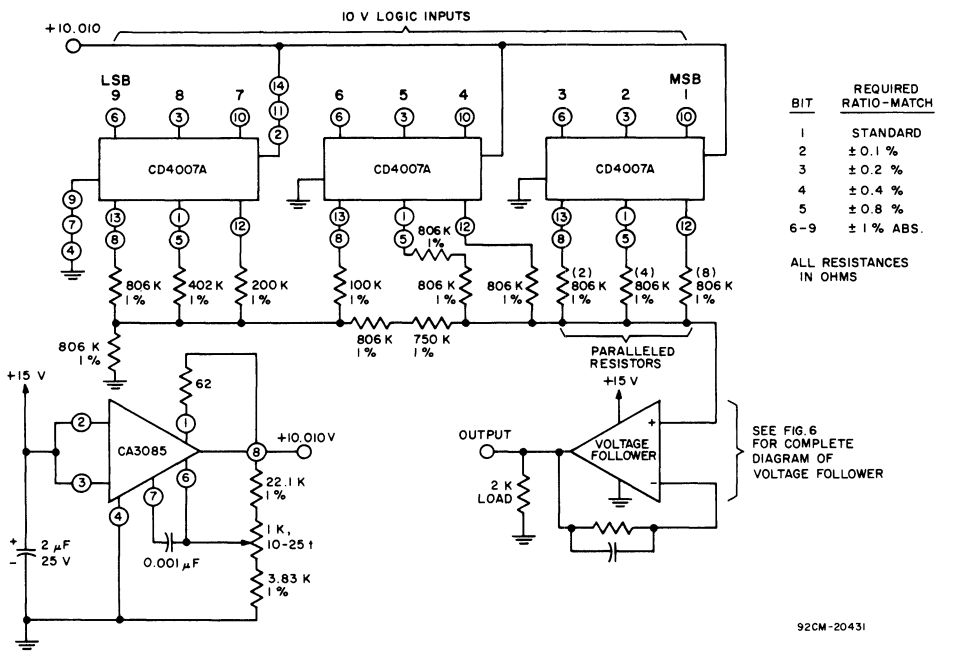


Fig. 8— Amplifier response to 4—V input pulses.



The follower amplifier has the offset adjustment nulled at approximately a 1-volt output level. System operating potentials are shown in Table I, where each bit is set "low" individually to observe the progression of output values. The positive ladder-supply voltage was adjusted to 10.010 V to provide a small compensation for the MSB switch resistance. A high-impedance 5-digit multimeter, such as the DANA 5330 or equivalent, is needed for direct measurement of the ladder output, and is invaluable during system development and evaluation. Table I shows ideal potential values, system output, and ladder output and illustrates the sources of system inaccuracy. The system output maintains proportional accuracy within ± 5.6 mV, or ± 1/4 LSB.

Fig. 10 shows the system output response to a 4-V logic pulse. The ringing is caused by the voltage follower, and the more gradual transients are caused by voltage-follower and ladder time constants. Settling time to 1/2 LSB is 5 μs.

This 9-bit COS/MOS-DAC demonstrates accuracy and simplicity with economical components and modest power-supply requirements. In addition, the design flexibility afforded by the COS/MOS building blocks simplifies the generation of DAC systems tailored to individual needs. COS/MOS switches used in conjunction with COS/MOS counters also find application in Analog-to-Digital Conversion Systems. The low-power and high noise-immunity features of these devices make them attractive A/D system components.

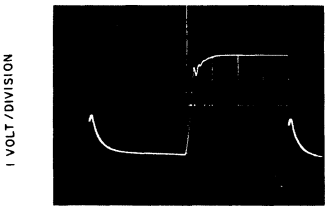


Fig. 10– System response to most-significant-bit logic pulse.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

Table I. Set Of Values For 10.010-V Regulated Supply Voltage

BINARY WORD	IDEAL POTENTIAL (V)	SYSTEM OUTPUT (V)	LADDER OUTPUT (V)	SYSTEM ERROR (mV)	VOLTAGE FOLLOWER OFFSET (mV)	LADDER & SWITCH ERROR (mV)	POSITIVE SWITCH DROP (mV)
000000000	9.9802	9.9856	9.9915	+ 5.4	- 5.9	+ 11.3	–
011111111	5.0000	4.9959	4.9997	- 4.1	- 3.8	- 0.3	14.8
101111111	2.5000	2.4996	2.5023	- 0.4	- 2.6	+ 2.3	11.0
110111111	1.2500	1.2554	1.2565	+ 5.4	- 1.0	+ 6.5	6.5
111011111	0.6250	0.6233	0.6226	- 2.7	+ 0.7	- 2.4	3.2
111101111	0.3125	0.3133	0.3113	+ 0.8	+ 2.1	- 1.2	1.7
111110111	0.1568	0.1603	0.1571	+ 3.5	+ 3.2	+ 0.3	14.0
111111011	0.0784	0.0826	0.0786	+ 4.2	+ 4.0	+ 0.2	11.8
111111101	0.0397	0.0439	0.0393	+ 4.2	+ 4.6	- 0.4	6.8
111111110	0.0198	0.0245	0.0195	+ 4.7	+ 5.0	- 0.3	3.6
111111111	0.0000	0.0056	0.0000	+ 5.6	+ 5.6	0.0	–

Application of the RCA-CA3058 and RCA-CA3059 Zero-Voltage Switches in Thyristor Circuits

by George J. Granieri

The RCA-CA3059 zero-voltage switch is a monolithic integrated circuit used primarily as a trigger circuit for the control of thyristors. This multistage circuit employs a diode limiter, a threshold detector, a differential amplifier, and a Darlington output driver to provide the basic switching action. The dc supply voltage for these stages is supplied by an internal zener-diode-regulated power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. This built-in power supply provides unique solutions to many application problems. An important feature of the CA3059 is that the trigger pulses developed by this circuit can be applied directly to the gate of a silicon controlled rectifier (SCR) or a triac. A built-in fail-safe circuit inhibits the application of these pulses to the thyristor gate circuit in the event that the external sensor for the integrated-circuit switch should be inadvertently opened or shorted.

The RCA CA3058 is similar to the CA3059 but utilizes a dual-in-line ceramic package. For additional information on this device, see RCA data bulletin File No. 490.

The CA3059 is particularly suited for use in thyristor temperature-control applications. The integrated circuit may be employed as either an on-off type of controller or a proportional controller, depending upon the degree of temperature regulation required. The availability of numerous terminal connections to internal circuit points greatly increases the flexibility of the CA3059 and permits the circuit designer to exercise his creativity to employ the integrated switch in unique ways. This Note describes the operation of the CA3059 integrated-circuit switch and discusses its operation in thyristor power-switching and control circuits.

CIRCUIT OPERATION

Fig. 1 shows a functional block diagram of the CA3059 integrated-circuit zero-voltage switch. Any triac that is driven directly from the output terminal of this circuit should be characterized for operation in the I(+) or III(+) triggering modes, i.e., with positive gate current (current flows into the gate for both polarities of the applied ac voltage).

*See chart

AC Input Voltage (Volts) 50/60 or 400 Hz	Series Resistor R_S (kΩ)	Power Rating of R_S (Watts)
24	2	0.5
120	10	2
208/230	20	4
277	25	5

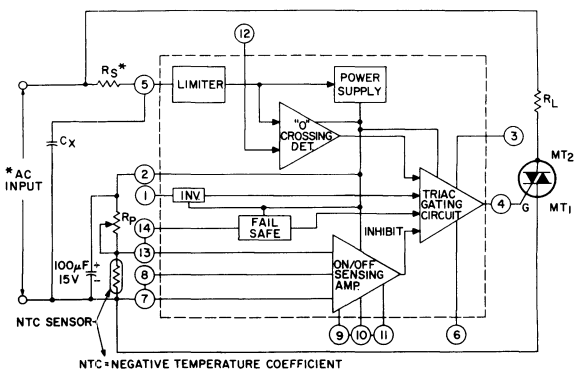


Fig.1 - Functional block diagram of the integrated-circuit zero-voltage switch.

The limiter stage of the CA3059 clips the incoming ac line voltage to approximately plus and minus 8 volts. This signal is then applied to the zero-voltage-crossing detector, which generates an output pulse during each passage of the line voltage through zero. The limiter output is also applied to a rectifying diode and an external capacitor that comprise the dc power supply. The power supply provides approximately 6 volts as the V_{CC} supply to the other stages of the CA3059. The on/off sensing amplifier is basically a differential comparator. The triac gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a high voltage, i.e., the line voltage must be approximately zero volts, the sensing-amplifier output must be "high," the external voltage to terminal 1 must be a logical "1," and the output of the fail-safe circuit must be "high."

Fig. 2 shows the circuit diagram of the CA3059. The zero-voltage threshold detector consists of diodes D_3, D_4, D_5, and D_6, and transistor Q_1. The differential amplifier consists of transistor pairs Q_2-Q_4 and Q_3-Q_5. Transistors Q_1, Q_6, Q_7, Q_8, and Q_9 comprise the triac gating circuit and driver stage. Diode D_{12}, zener diode D_{15}, and transistor Q_{10} constitute the fail-safe circuit. The power supply consists of diodes D_7 and D_{13}, and an external resistor and capacitor connected to terminals 5 and 2, respectively, and to ground through pin 7. If the transistor pair Q_2-Q_4 and transistor Q_1 are turned off, an output appears at terminal 4. Transistor Q_1 is in the OFF state if the incoming line voltage is less than approximately the voltage drops across three silicon diodes (2.1 volts) for either the positive or negative excursion of the line voltage. Transistor pair Q_2-Q_4 is OFF if the voltage across the sensor, connected from terminals 13 to 7, exceeds the reference voltage from 9 to 7. If either of these conditions is not satisfied, pulses are not supplied to terminal 4. Fail-safe operation requires that terminal 13 be connected to 14. The addition of hysteresis and elimination of half-cycling can be obtained by a resistive voltage divider connected from 13 to 8 and from 8 to 7.

Fig. 3 shows the position and width of the pulses supplied to the gate of a thyristor with respect to the incoming ac line voltage. The CA3059 can supply sufficient gate voltage and current to trigger most RCA thyristors at ambient temperatures of 25°C. *However, under worst-case conditions (i.e., at ambient-temperature extremes and maximum triggering requirements), selection of the higher-current thyristors may be necessary for particular applications.* RCA bulletin File No. 406 lists Triacs suitable for use with the CA3058 or CA3059. For example, the RCA-2N5444 40-ampere triac has a maximum gate trigger voltage V_{GT}(max) of 2.5 volts and a maximum gate trigger current I_{GT}(max) of 80 milliamperes in the III(+) quadrant

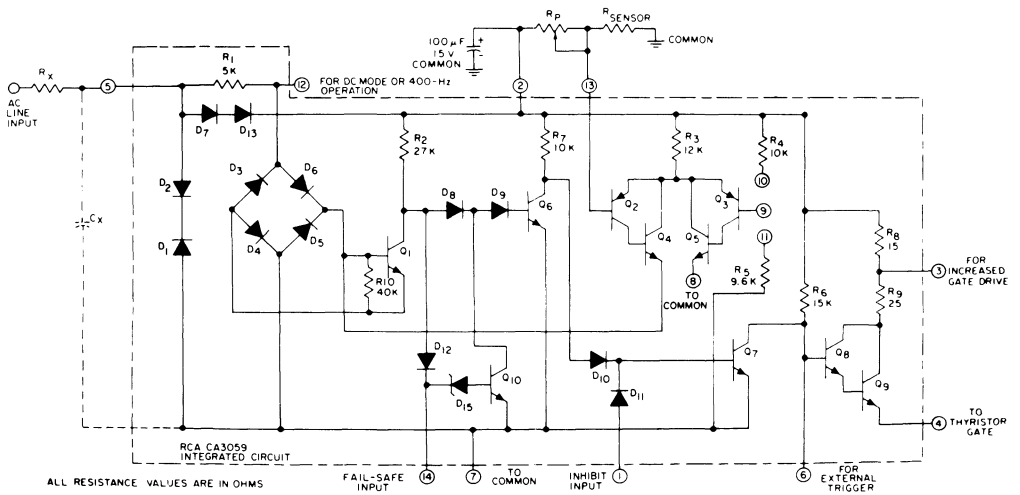


Fig.2 - Circuit diagram for the CA3059 zero-voltage switch.

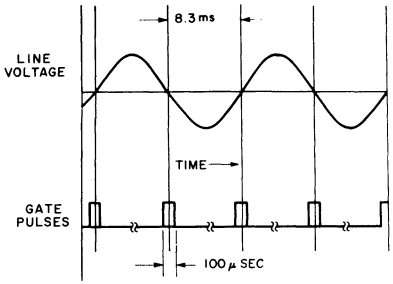


Fig.3 - Timing relationship between the output pulses of of the CA3059 and the ac line voltage.

at 25°C. Because the CA3059 cannot guarantee a drive of 80 milliamperes for a V_{GT} of 2.5 volts, triac selection will be required.

EFFECT OF CA3059 ON THYRISTOR LOAD CHARACTERISTICS

The CA3059 is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the CA3059 is of short duration, the latching current* of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching-current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the CA3059 to accommodate inductive loads and low-power loads. For example, for loads that are less than approximately 4 amperes rms or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by insertion of the capacitor C_x from terminal 5 to terminal 7 as shown in Fig. 1. The insertion of capacitor C_x permits switching of triac loads that have a slight inductive component and that are greater than approximately 200 watts (for operation from an ac line voltage of 120 volts rms). However, for loads less than 200 watts (for example, 70 watts), it is recommended that the user employ the RCA-40526 sensitive-gate triac with the CA3059 because of the low latching-current requirement of this triac.

For loads that have a low power factor, such as a solenoid valve, the user may operate the CA3059 in the dc mode. In this mode, terminal 12 is connected to terminal 7, and the zero-crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the CA3059 integrated circuit, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the CA3059 no longer operates as a zero-voltage switch. However, for many applications that involve the switching of low-current inductive loads, the amount of RFI generated can frequently be tolerated.

For switching of high-current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual-output over-under temperature controller and the transient-free switch controller described later in this Note is recommended.

* The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the OFF to the ON state and the gate signal is removed.

FAIL-SAFE FEATURE

As shown in Figs. 1 and 2, when terminal 13 is connected to terminal 14, the fail-safe circuit of the CA3059 is operable. If the sensor should then be accidentally opened or shorted, power is removed from the load (i.e., the triac is turned OFF). The internal fail-safe circuit functions properly, however, only when the ratio of the sensor impedance at 25°C, if a thermistor is the sensor, to the impedance of the potentiometer R_p is less than 4 to 1. It is readily apparent that, if the potentiometer is adjusted for 1000 ohms and the sensor is 100,000 ohms, the zener diode D_{15} (shown in Fig. 2) would conduct because virtually all the dc power-supply voltage (from terminal 2 to terminal 7) would appear across the sensor. The CA3059 would then detect this condition as an open sensor.

For ratios greater than 4 to 1, for example 100 to 1, the circuit shown in Fig. 4 may be employed to provide fail-safe operation. In this circuit, transistor Q_1 and diode D_1 are components external to the CA3059. Transistor Q_1 detects the sensor current which maintains this transistor in saturation so that terminal 1 is effectively shorted to terminal 7 through the collector-to-emitter junction of the transistor. Transistor Q_1 provides sufficient current gain to permit operation with a sensor impedance greater than 1 megohm. If the sensor becomes open-circuited, transistor Q_1 turns OFF, and current then flows into terminal 1, the inhibit terminal of the CA3059, and results in the removal of power to the load. For the shorted-sensor condition, the external diode D_1 conducts and causes triac Y_1 to turn OFF. Diode D_2 compensates for variations in the base-to-emitter voltage of transistor Q_1 with temperature. Terminals 13 and 14 on the CA3059 should not be connected when the external fail-safe circuit shown in this illustration is employed.

HALF-CYCLING AND HYSTERESIS CHARACTERISTICS

The method by which the CA3059 senses the zero crossing of the ac power results in a half-cycling phenomenon at the control

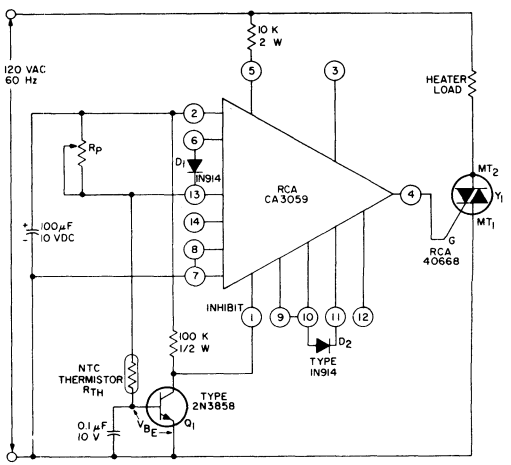


Fig.4 - CA3059 on-off controller that uses an external fail-safe circuit.

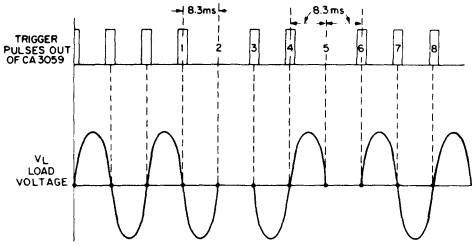


Fig.5 - Half-cycling phenomenon in the CA3059.

point. Fig. 5 illustrates this phenomenon. The CA3059 senses the zero-voltage crossing every half-cycle and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3 milliseconds, however, the differential amplifier in the CA3059 may change state and inhibit any further output pulses. The uncertainity region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the ac line voltage.

Several solutions exist for elimination of the half-cycling phenomenon. If the user can tolerate some hysteresis in the control, then positive feedback can be added around the differential amplifier. Fig. 6 illustrates this technique. The tabular data in the figure lists the recommended values of R_1 and R_2 for different sensor impedances at the control point.

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Fig. 7 may be employed. In this configuration, external transistor Q_1 provides a means for addition of positive feedback to the CA3059. It should be noted that the signal developed at the collector to Q_1 could perhaps be used to provide an auxiliary time-delay function.

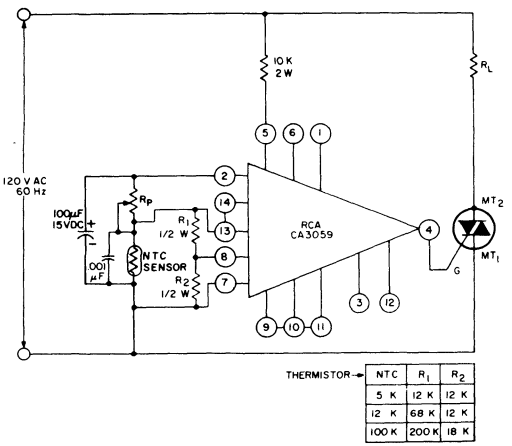


Fig.6 - CA3059 on-off controller with hysteresis.

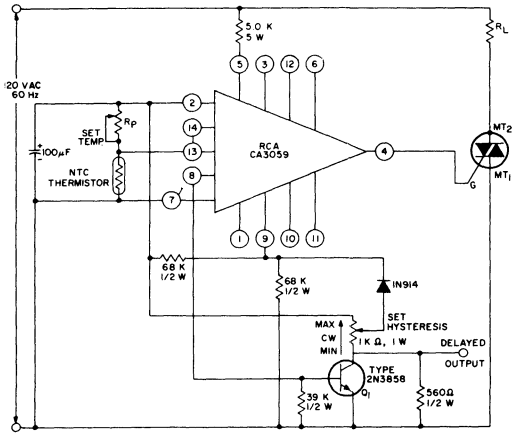


Fig.7 - CA3059 on-off controller with controlled hysteresis.

For applications which require complete elimination of half-cycling without the addition of hysteresis, the *integral-cycle* temperature controller described in a later section of this Note, which senses the zero-voltage crossing only once during the ac power cycle, can be used.

TEMPERATURE CONTROLLERS

Fig. 8 shows a triac used in an on-off temperature-controller configuration. The triac is turned on at zero voltage whenever the

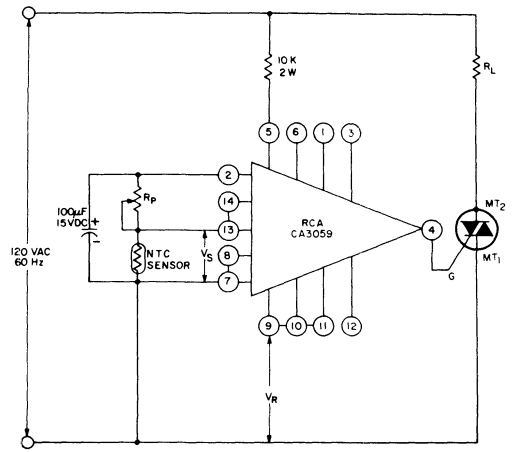


Fig.8 - CA3059 on-off temperature controller.

voltage V_s exceeds the reference voltage V_r. The transfer characteristic of this system, shown in Fig. 9(a), indicates significant thermal overshoots and undershoots, a well-known characteristic of such a system. The differential or hysteresis of this

system, however, can be further increased, if desired, by the addition of positive feedback.

For precise temperature-control applications, the proportional-control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Fig. 9(b). In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an "on-off" type of controller, full power (100 per cent duty cycle) is supplied to the system. This effect results in significant temperature excursions *because there is no anticipatory circuit* to reduce the power gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

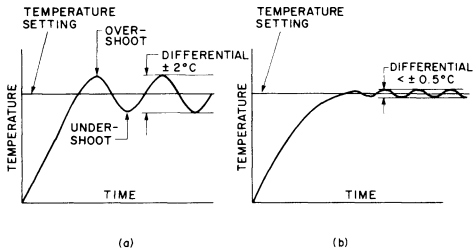


Fig.9 - Transfer characteristics of (a) on-off and (b) proportional control systems.

Before such a system is implemented, a time base is chosen so that the ON-time of the triac is varied within this time base. The ratio of the ON-to-OFF time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Fig. 10 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the dc control signal supplied to the opposite side of the differential amplifier. The triac then remains OFF for the remainder of the time-base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

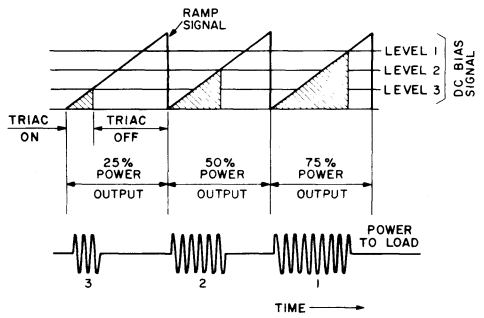


Fig.10 - Principles of proportional control.

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. It is noted that a ramp having good linearity is not required for proportional operation because of the nonlinearity of the thermal system and the closed-loop type of control. In the circuit shown in Fig. 11, ramp voltage is generated when the capacitor C_1 charges through resistors R_0 and R_1. The time base of the ramp is determined by resistors R_2 and R_3, capacitor C_2, and the breakover voltage of the A1N5411 diac. When the voltage across C_2 reaches approximately 32 volts, the diac switches and turns on the 2N3241A transistor. The capacitor C_1 then discharges through the collector-to-emitter junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through

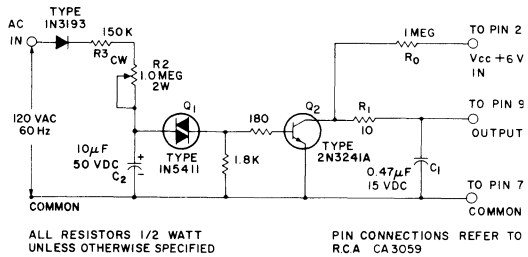


Fig.11 - Ramp generator.

adjustment of R_2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with the respect to the period of the 60-Hz line voltage. Fig. 12 shows a triac connected for the proportional mode.

Fig. 13 shows a dual-output temperature controller that drives two triacs. When the voltage V_s developed across the temperature-sensing network exceeds the reference voltage V_{R1}, motor M_1

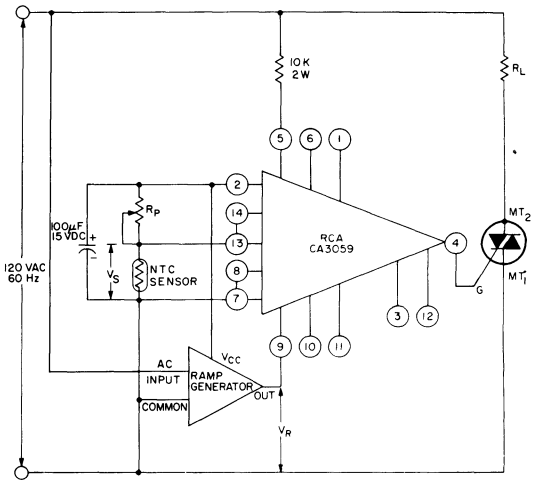


Fig.12 - CA3059 proportional temperature controller.

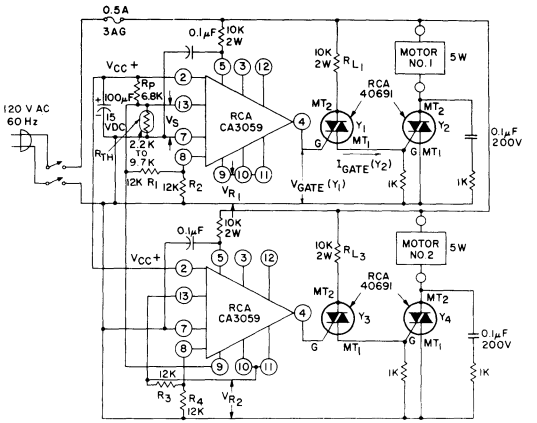


Fig.13 - Dual-output, over-under temperature controller using two CA3059 integrated circuits.

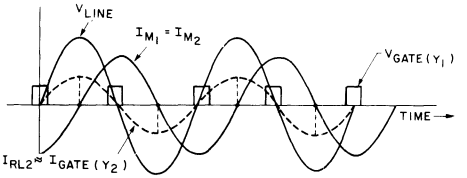


Fig.14 - Voltage and current waveforms for the dual-output temperature controller.

turns on. When the voltage across the network drops below the reference voltage V_{R2}, M_2 turns on. Because the motors are inductive, the currents I_{M1} and I_{M2} lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Fig. 14.

The problem of driving inductive loads such as these motors by the narrow pulses generated by the CA3059 circuit is solved by use of the sensitive-gate RCA-40526 triac. The high sensitivity of this device (3 milliamperes maximum) and low latching current (approximately 9 milliamperes) permit synchronous operation of the temperature-controller circuit. In Fig. 13, it is apparent that, though the gate pulse V_g of triac Y_1 has elapsed, triac Y_2 is switched on by the current through R_{L1}. The low latching current of the RCA-40526 triac results in dissipation of only 2 watts in R_{L1}, as opposed to 10 to 20 watts when devices that have high latching currents are used.

Electric-Heat Application

For electric-heating applications, the RCA-2N5444 40-ampere triac and the CA3059 circuit constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from the switching transients. The salient features of the 2N5444 40-ampere triac are as follows:

(1) 300-ampere single-surge capability (for operation at 60-Hz),

(2) a typical gate sensitivity of 20 milliamperes in the I(+) and III(-) modes,

(3) low ON-state voltage of 1.5 volts maximum at 40 amperes, and

(4) available V_{DROM} equal to 600 volts.

Fig. 15 shows the circuit diagram of a synchronous-switching heat-staging controller that is used for electric heating systems. Loads

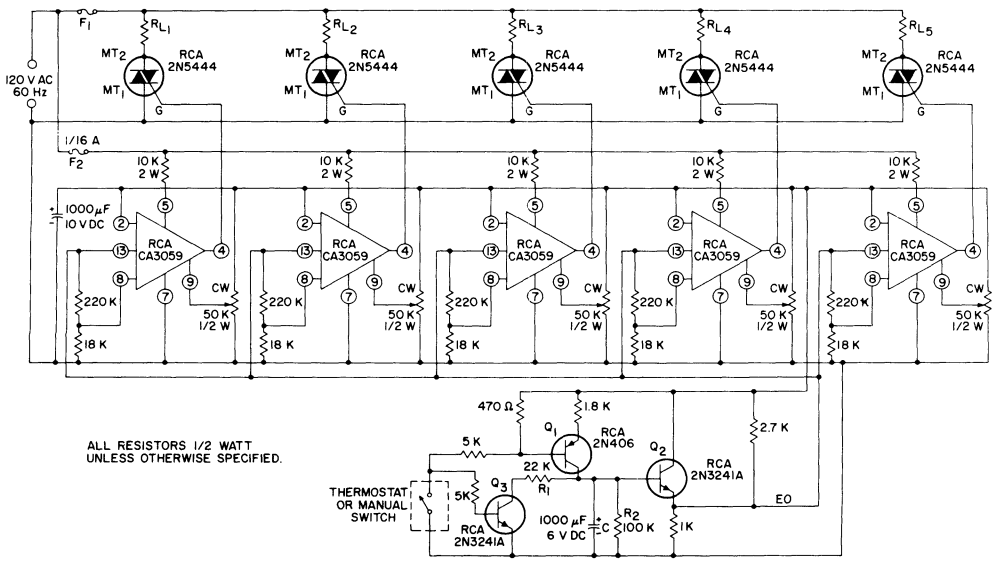


Fig.15 - Synchronous-switching heat-staging controller using a series of CA3059 integrated circuits.

as heavy as 5 kilowatts are switched sequentially at zero voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25 kilowatts were to be switched simultaneously.

Transistor Q_1 is used as a constant-current source to charge capacitor C in a linear manner. Transistor Q_2 acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output E_o. At approximately 3-second intervals, each 5-kilowatt heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through R_1 and R_2 to cause each triac to turn OFF in the reverse heating sequence. It should be noted that some half-cycling occurs before the heating element is switched fully ON. This condition can be attributed to the inherent dissymmetry of the CA3059 and is further aggravated by the slow-rising ramp voltage applied to one of the inputs. The timing diagram in Fig. 16 shows the turn-on and turn-off sequence of the heating system being controlled.

Seemingly, the basic method shown in Fig. 15 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitably results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.

Integral-Cycle Temperature Controller (No half-cycling)

If a temperature controller which is completely devoid of half-cycling and hysteresis is required, then the circuit shown in Fig. 17 may be used. This type of circuit is essential for applications in which half-cycling and the resultant dc component could cause overheating of a power transformer on the utility lines.

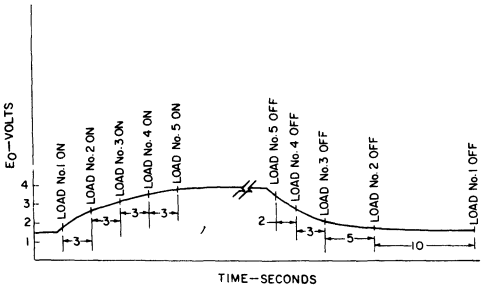
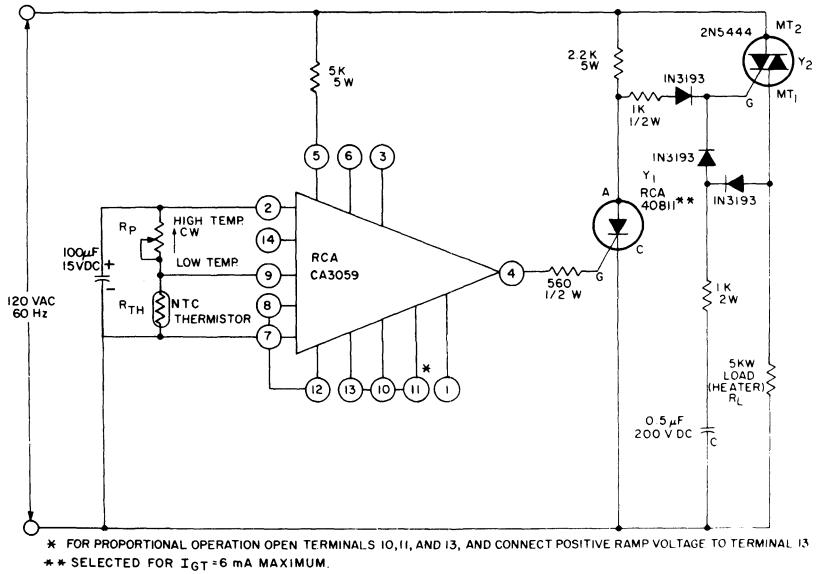


Fig.16 - Ramp-voltage waveform for the heat-staging controller.

In the circuit shown in Fig. 17, the sensor is connected between terminals 7 and 9 of the CA3059. This arrangement is required because of the phase reversal introduced by SCR Y_1. With this configuration, terminal 12 is connected to terminal 7 for operation of the CA3059 in the dc mode (however, the load is switched at zero voltage). Because the position of the sensor has been changed for this configuration, the internal fail-safe circuit cannot be used (terminals 13 and 14 are not connected).

In the integral-cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high and an



* FOR PROPORTIONAL OPERATION OPEN TERMINALS 10, 11, AND 13, AND CONNECT POSITIVE RAMP VOLTAGE TO TERMINAL 13

** SELECTED FOR I_{GT} = 6 mA MAXIMUM.

Fig.17 - CA3059 integral-cycle temperature controller in which half-cycling effect is eliminated.

output signal at terminal 4 of zero volts is obtained. The SCR (Y_1), therefore, is turned off. The triac (Y_2) is then triggered directly from the line on positive cycles of the ac voltage. When Y_2 is triggered and supplies power to the load R_L, capacitor C is charged to the peak of the input voltage. When the ac line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half-cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half-cycles of the ac input voltage after it is triggered on the positive half-cycle to provide only *integral cycles* of ac power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the CA3059. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned OFF. The cycle repeats when the SCR is again turned OFF by the CA3059.

The circuit shown in Fig. 18 is similar to the configuration in Fig. 17 except that the fail-safe circuit incorporated in the CA3059 can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor Q_o inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y_1). The internal power supply of the CA3059 supplies bias current to transistor Q_o.

Of course, the circuit shown in Fig. 18 can readily be converted to a *true proportional integral-cycle temperature controller* simply by connection of a positive-going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.

SENSOR ISOLATION

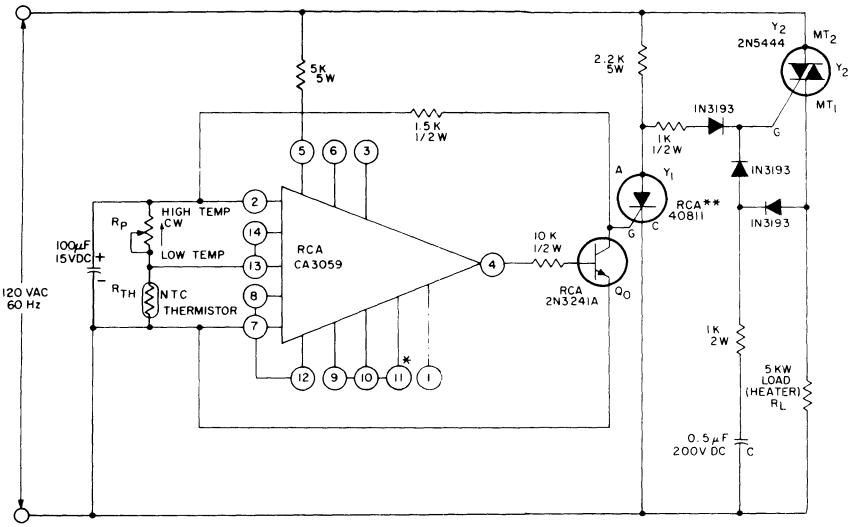
For some applications, electrical isolation of the sensor from the incoming ac power lines may be desired. Fig. 19 shows such a configuration. The pulse transformer T_1 isolates the sensor from main terminal No. 1 of the triac Y_1, and transformer T_2 isolates the CA3059 from the power lines. Capacitor C_1 shifts the phase of the output pulse at terminal 4 in order to retard the gate pulse delivered to triac Y_1 to compensate for the small phase shift introduced by transformer T_1.

DIFFERENTIAL COMPARATOR FOR INDUSTRIAL USE

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic "one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high-performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The CA3059 is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the CA3059, and the circuit becomes a differential comparator.

Fig. 20 shows the circuit arrangement for use of the CA3059 as a differential comparator. In this application, no external dc supply is required, as is the case with most commercially available integrated-circuit comparators; of course, the output-current capability of the CA3059 is reduced because the circuit is operating in the dc mode. The 1000-ohm resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3 milliamperes.

When the CA3059 is connected in the dc mode, the drive current for terminal 4 can be determined from a curve of the



* FOR PROPORTIONAL OPERATION OPEN TERMINALS 9,10 AND 11 AND CONNECT POSTIVE RAMP VOLTAGE TO TERMINAL 9
**SELECTED FOR I_{GT}=6 mA MAXIMUM

Fig.18 - CA3059 integral-cycle temperature controller that features fail-safe operation and no half-cycling effect.

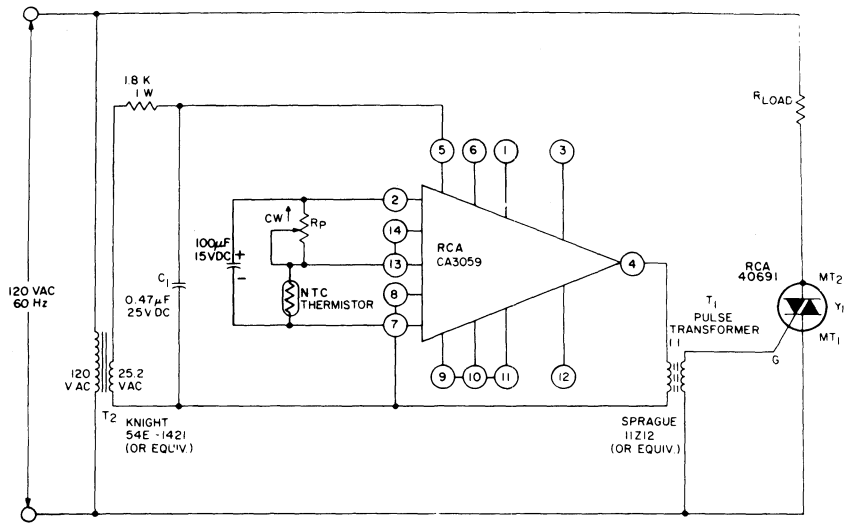


Fig.19 - CA3059 on-off controller with an isolated sensor.

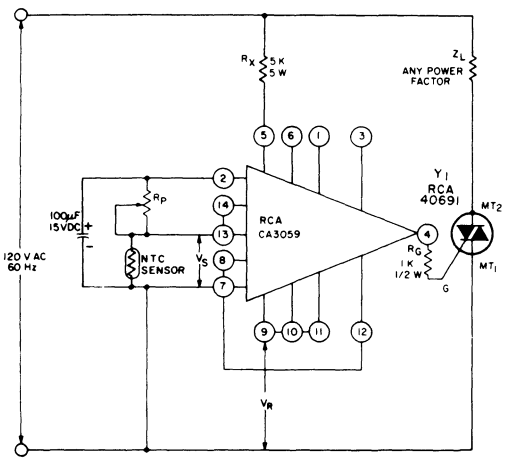


Fig.20 - Differential comparator using the CA3059 integrated circuit.

external load current as a function of dc voltage from terminals 2 and 7. This curve is shown in the technical bulletin for the CA3059 integrated circuit. Of course, if additional output current is required, an external dc supply may be connected between terminals 2 and 7, and resistor R_X (shown in Fig. 20)may be removed.

The chart below compares some of the operating characteristics of the CA3059, when used as a comparator, with a typical high-performance commercially available integrated-circuit differential comparator.

PARAMETERS	CA3059 (typical values)	Typical Integrated-Circuit Comparator (710)
1. Sensitivity	30 mV	2mV
2. Switching speed (rise time)	> 20 μs	90 ns
3. Output drive capability	*4.5V at ≤ 4mA	3.2V at ≤ 5.0mA

*Refer to Figure 20; R_X equals 5000 ohms.

POWER ONE-SHOT CONTROL

Fig. 21 shows a circuit which triggers a triac for one complete half-cycle of either the positive or negative alternation of the ac line

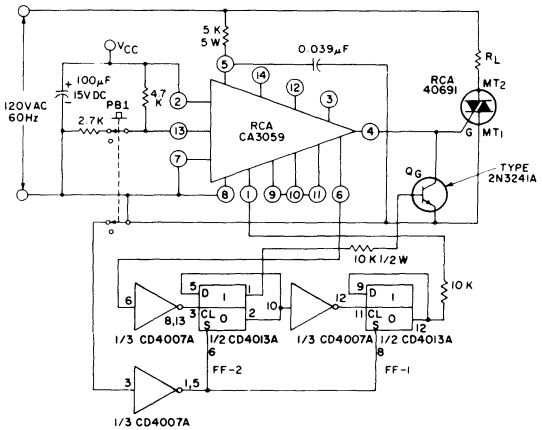


Fig.21 - Block diagram of a power one-shot control using the CA3059.

voltage. In this circuit, triggering is initiated by the push button PB-1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the ac cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling guns, impulse hammers, and the like, where load-current flow is required for only one complete half-cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

generated, but the state of Q_G determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF-1. Transistor Q_G is then turned off. The second pulse triggers the triac and FF-1 which, in turn, toggles the second flip-flop FF-2. The output of FF-2 turns on transistor Q_7, as shown in Fig. 22, which inhibits all further output pulses. When the pushbutton is released, the circuit resets itself until the process is repeated with the button. Fig. 23 shows the timing diagram for the described operating sequence.

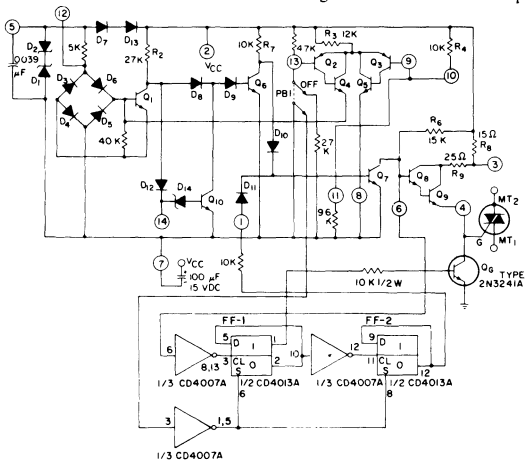


Fig.22 - Circuit diagram for the power one-shot control.

In the circuit of Fig. 21, before the button is depressed, both flip-flop outputs are in the "zero" state. Transistor Q_G is biased ON by the output of flip-flop FF-1. The differential comparator which is part of the CA3059 circuit is initially biased to inhibit output pulses. When the push button is depressed, pulses are

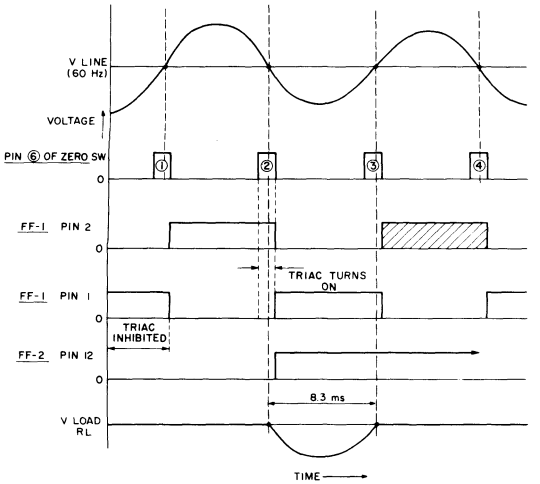


Fig.23 - Timing diagram for the power one-shot control.

SOLID-STATE TRAFFIC FLASHER

Another application which illustrates the versatility of the CA3059, when used with RCA thyristors, involves switching traffic-control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current-surge peak is approximately ten times the peak steady-state value or fifteen times the steady-state rms value. The second current-surge peak is approximately four times the steady-state rms value.

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn-on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the ac line.

Fig. 24 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces the initial di/dt,

decreases the required triac surge-current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF-1), the CA3059, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF-1 determines the triggering of triacs Y_1 or Y_2 by the output pulses at terminal 4 generated by the zero-crossing circuit. Transistors Q_1 and Q_2 inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" (V_{CC} high) state of the flip-flop.

The arrangement described can also be used for a synchronous, sequential traffic-controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

TRANSIENT-FREE SWITCH CONTROLLER

The CA3059 can be used as a simple solid-state switching device that permits ac currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Fig. 25 is connected so that, after the control terminals (14 and 7) are opened, electronic logic waits until the power-line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Fig. 26 is connected to provide the opposite control logic to that of the circuit shown in Fig. 25. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

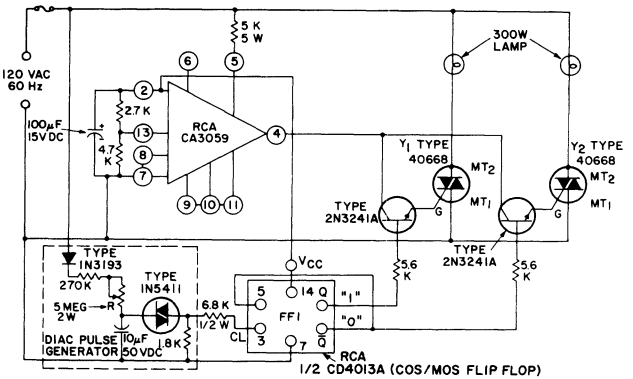
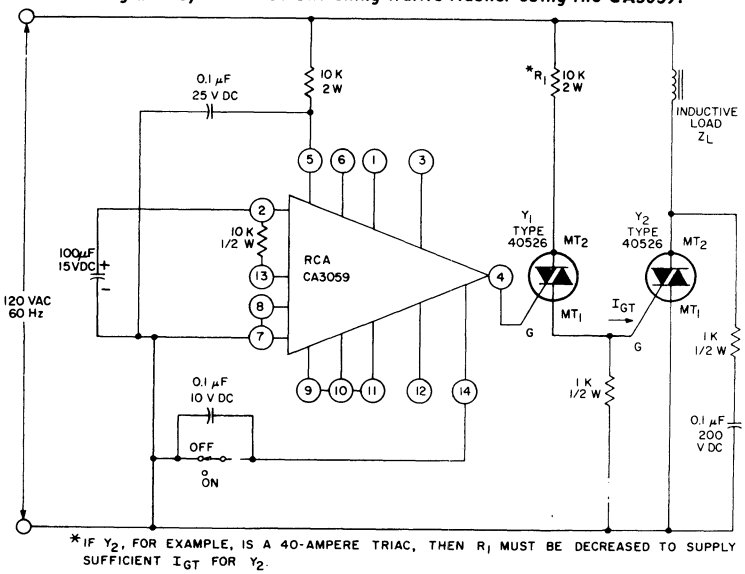


Fig.24 - Synchronous-switching traffic flasher using the CA3059.



*IF Y_2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, THEN R_1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y_2.

Fig.25 - CA3059 transient-free switch controller in which power is supplied to the load when the switch is open.

In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y_2. If Y_2 is an RCA-2N5444 triac, an rms current of 40 amperes can be switched.

ACKNOWLEDGMENTS

The author wishes to express his appreciation to P. Howard for his able assistance in development of many of the circuits described in this Note.

Ref. 1. RCA bulletin File No. 479, *"COS/MOS IC's* for Low-Voltage (3-15V) Applications.

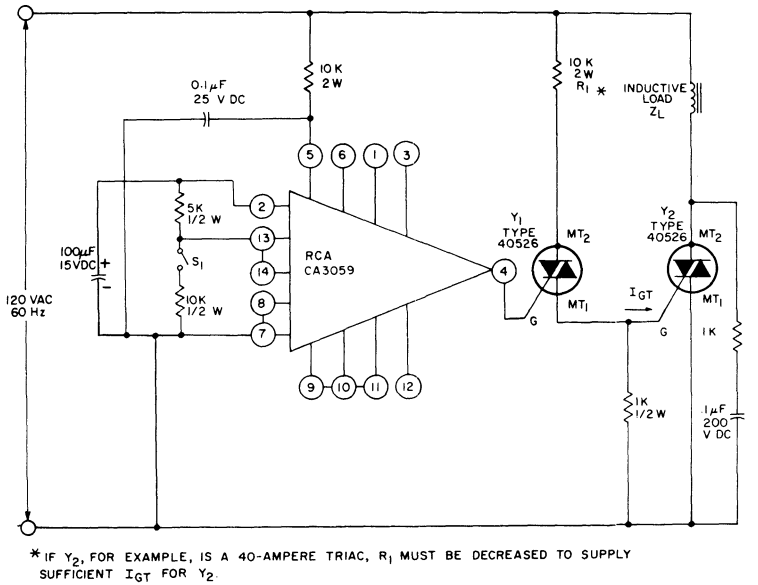


Fig.26 - CA3059 transient-free switch controller in which power is applied to the load when the switch is closed.

Applications and Extended Operating Characteristics for the RCA-CA3059 IC Zero-Voltage Switch

by H. M. Kleinman and A. Sheng

The RCA-CA3059 zero-voltage switch is a monolithic silicon integrated circuit designed to control a thyristor in a variety of ac power switching applications. A previous Application Note (ICAN-4158) described several useful control systems in which the CA3059 was used as a thyristor trigger. This Note briefly describes the CA3059 circuit, explains the circuit functions and basic system configurations, and gives supplemental data for extending operation to 220-volt, 50-to-60-Hz lines and temperatures from -40°C to +85°C. It also discusses additional applications including the switching of inductive loads, the provision of negative gate current, operation with low-impedance sensors, and synchronous light flashers.

CIRCUIT DESCRIPTION

Operation of the CA3059 can best be explained by reference to the functional block diagram shown in Fig. 1 and the schematic diagram shown in Fig. 2. In the following discussion, all voltages are referred to terminal 7.

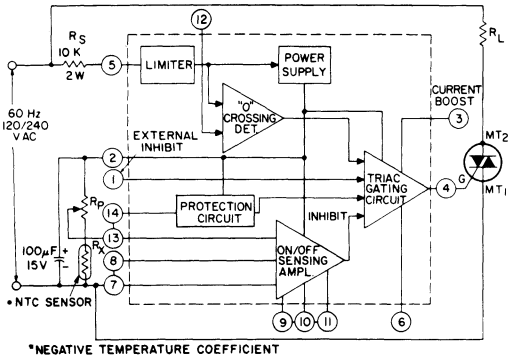


Fig. 1 - Functional block diagram of CA3059 integrated-circuit zero-voltage switch.

Power to the circuit may be derived directly from the ac line, as shown in Fig. 1, or from an external dc power supply connected between terminals 2 and 7, as shown in Fig. 3. In the normal mode of operation, a dropping resistor R_S of 5000 to 10,000 ohms is required to limit the current in the IC. The choice of resistor is a function of the average current drawn from the power supply, either by external circuits or by the thyristor trigger circuits, as shown in Fig. 4.

The diodes D_1 and D_2 in Fig. 2 form a symmetrical clamp that limits the voltages on the chip to ±8 volts; D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor. When an external power supply is used to increase the current capability of the IC, care must be used to avoid exceeding the 14-volt breakdown voltage rating between terminals 2 and 5. This requirement is not a problem if the supply voltage is 6 volts or less. If higher supply voltages are required, terminal 5 must be shorted to terminal 7 and the line synchronizing voltage applied to terminal 12 through a resistor of 10,000 ohms or more, as shown in Fig. 3.

The functions of the other blocks in Fig. 1 can best be understood by consideration of the normal state of a thyristor gating circuit as its ON state, in which current is being delivered to the triac gate through terminal 4. The other circuit blocks inhibit the gating circuit unless certain conditions are met. In the ON state, Q_8 and Q_9 are conducting, Q_7 is off, and Q_6 is on. Any action that turns Q_7 on removes the drive from Q_8 and allows the thyristor to turn off. Q_7 may be turned on directly by application of a minimum of +1.2 volts at 10 microamperes to the EXTERNAL INHIBIT terminal 1. (If a voltage of more than 2 volts is available, external resistance must be added to limit the current to 10 milliamperes.) Diode D_{10} isolates the base of Q_7 from other signals when an external inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher-priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Q_7 may

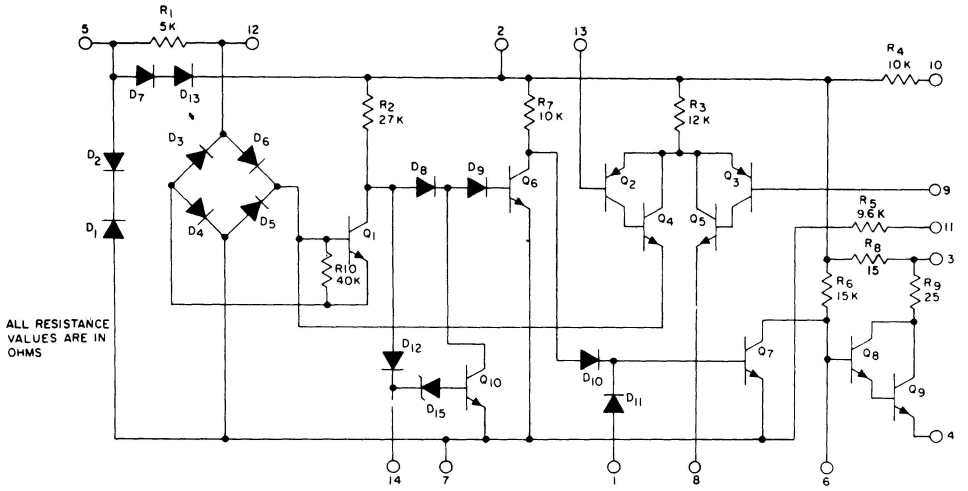


Fig. 2 - Schematic diagram of CA3059 zero-voltage switch.

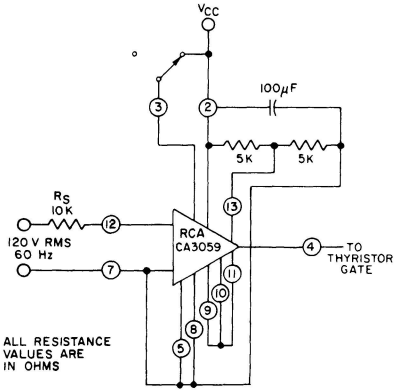


Fig. 3 - Operation of the CA3059 from an external dc power supply connected between terminals 2 and 7.

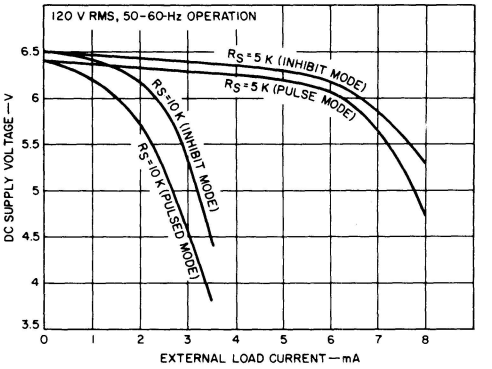


Fig. 4 - DC supply voltage as a function of external load current for several values of dropping resistance R_S.

also be activated by turning off Q_6 to allow current to flow from the power supply through R_7 and D_{10} into the base. Q_6 is normally held on by current flowing into its base through R_2,D_8, and D_9 when Q_1 is off.

Q_1 is a portion of the zero-crossing detector. When the voltage at terminal 5 is greater than +3 volts, current can flow through R_1, D_6, the base-to-emitter junction of Q_1, and D_4 to terminal 7 to turn on Q_1 and inhibit the pulse. For negative voltages with magnitudes greater than 3 volts, the current flows through D_5, the emitter-to-base junction of Q_1, D_3, and R_1, and again turns Q_1 on. Q_1 is off only when the voltage at terminal 5 is less than the threshold voltage of approximately 2 volts. When the CA3059 is connected as shown in Fig. 1, therefore, output occurs in a narrow pulse which is approximately centered about the zero-voltage time in the cycle, as shown in Fig, 5. In some applications, however, particularly those using either slightly inductive or low-power loads, the thyristor load current does not reach

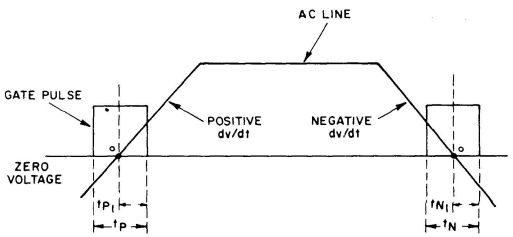


Fig. 5 - Waveform showing output-pulse duration of CA3059.

holding current by the end of this pulse. Fig. 6 shows how an external capacitor between terminal 5 and 7 can be used to delay the pulse to accommodate such loads. The amount of pulse stretching and delay is shown in Figs. 7(a) and 7(b).

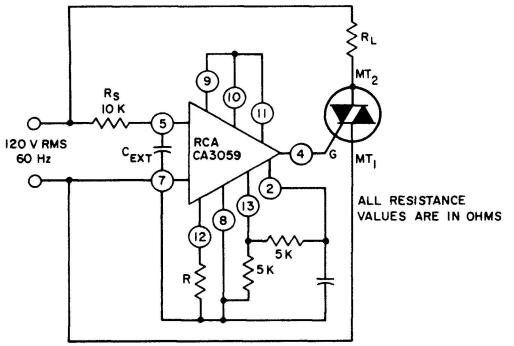


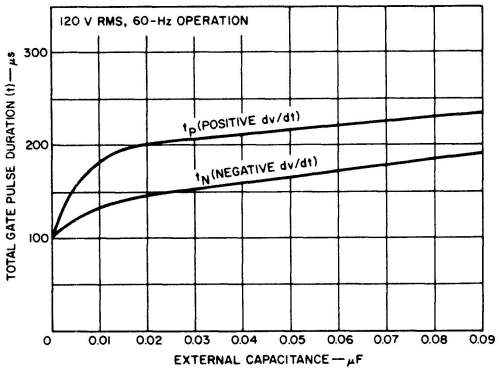
Fig. 6 - Use of a capacitor between terminals 5 and 7 to delay the output pulse of the CA3059.

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero-crossing detector. In this mode, Q_1 is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be used to avoid overloading of the internal power supply in this mode. A sensitive-gate thyristor should be used and a resistor placed between terminal 4 and the gate of the thyristor to limit the current.

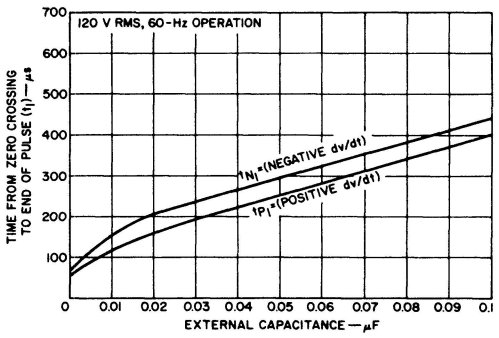
THE ON-OFF SENSING AMPLIFIER

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors Q_2, Q_3, Q_4, and Q_5 makes the CA3059 a flexible power-control circuit. The transistor pairs Q_2-Q_4 and Q_3-Q_5 form high-beta composite p-n-p transistors in which the emitters of Q_4 and Q_5 act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with R_3 acting as a constant-current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of Q_2 and Q_3. Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of Q_2-Q_4; when terminal 13 is negative with respect to terminal 9, most of the current flows through that path and none in terminal 8. When current flows in Q_2-Q_4, the path is from the supply through R_3, through Q_2-Q_4, through the base-emitter junction of Q_1, and finally through D_4 to terminal 7. Therefore, when V_{13} is equal to or more negative than V_9, Q_1 is on and output is inhibited.

In the circuit shown in Fig. 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, with R_p and the NTC sensor forming the other. At low temperatures, the large value of the sensor causes terminal 13 to be positive with respect to terminal 9 so that the thyristor fires on every half-cycle and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached and V_{13} approaches V_9. At this point, Q_2-Q_4 turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of R_p. For cooling service, either the positions of R_p and the sensor may be reversed or terminals 9 and 13 may be interchanged.



(a)



(b)

Fig. 7 - Curves showing effect of external capacitance on (a) the total output-pulse duration, and (b) the time from zero crossing to the end of the pulse.

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1 megohm at balance without introduction of substantial error (i.e., greater than 5 per cent). The error may be reduced if the internal bridge elements R_4 and R_5 are not used but are

replaced with resistors which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply; the curves shown in Fig. 4 should be consulted when low-impedance sensors are used. Operation with sensors as low as 300 ohms may be obtained with a 5000-ohm series resistor. Slightly better sensitivity can be realized if R_S is reduced to 4000 ohms.

ADDING HYSTERESIS

Because the logic circuitry of the CA3059 causes a decision concerning power delivery to be made on each half-cycle, it is possible that power may be required for an odd number of half-cycles once equilibrium is reached. In systems with relatively fast response times (less than 1 second), a substantial dc component might be placed on the power line and cause heating of any isolation or distribution transformers. This problem may be reduced by introducing hysteresis into the system, as shown in Fig. 8. A "dead zone" of 10 per cent of the sensor impedance may be achieved by

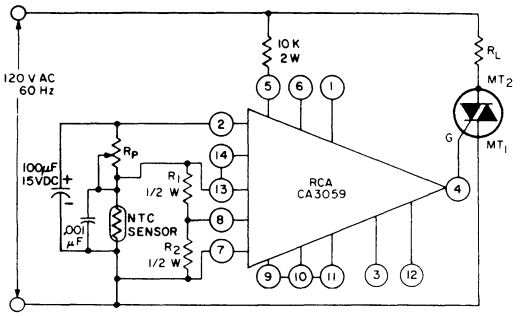


Fig. 8 - CA3059 on-off controller with hysteresis.

use of a sensor resistance R_a of 0.1 megohm, an R_1 value of 0.2 megohm, and an R_2 value of 18000 ohms. A decrease in the R_2 value reduces the effect. With a 5000-ohm sensor impedance, values of 12000 ohms for R_1 and R_2 yield a 5-per-cent dead zone. A more eleborate system (described in ICAN-4158) is required if the degree of hysteresis must be accurately controlled.

PROPORTIONAL CONTROL

The ON-OFF nature of the control shown in Fig. 1 causes some overshoot that leads to a definite steady-state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Fig. 9(a) can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free-running multivibrator. At balance, the voltage at terminal 13 is as shown in Fig. 9 (b). When this voltage is more positive than the threshold, power is applied to the load so that the duty cycle is approximately 50 per cent. With a 0.1-megohm sensor and

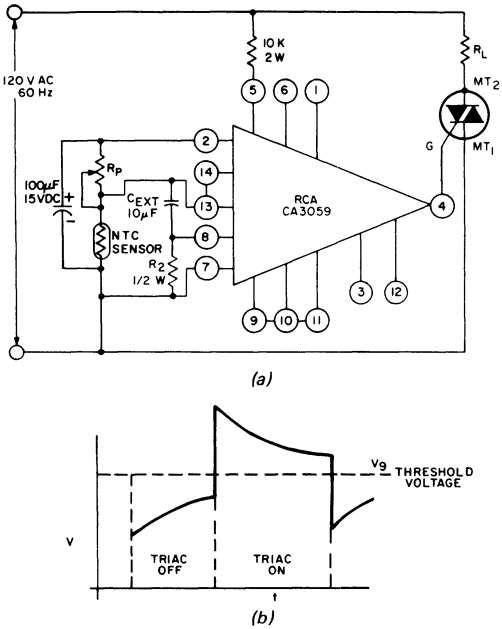


Fig. 9 - Typical heating control with proportional control: (a) schematic diagram, and (b) waveform of voltage at terminal 13.

values of R_P = 0.1 megohm, R_2 = 10,000 ohms, and $C_{ext.}$ = 10 microfarads, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. Changing the value of any of these elements changes the period, as shown in Fig. 10. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to V_9. A cooling sensor moves V_{13} in a positive direction. The triac is ON for a larger portion of the pulse cycle and increases the average power to the load.

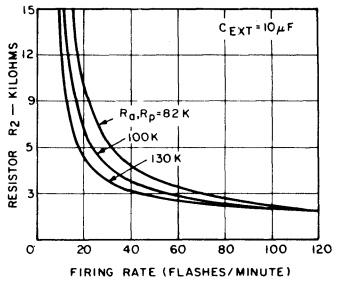


Fig. 10 - Effect of variations in time-constant elements on period.

As in the case of the hysteresis circuitry described, some special applications may require more sophisticated systems

to achieve either very precise regions of control or very long periods (see ICAN-4158).

FAIL-SAFE OPERATION

A special feature of the CA3059 is the inclusion of a fail-safe circuit which removes power from the load if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, fail-safe operation is guaranteed under the following conditions:

1. The circuit configuration of Fig. 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.

2. The value of R_p and of the sensor resistance must be between 2000 ohms and 0.1 megohm.

3. The ratio of sensor resistance and R_p must be greater than 0.25 and less than 4.0 for all normal conditions (if either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit).

Fail-safe operation may be applied to other systems when operation of the circuit is understood. The fail-safe circuit consists of D_{12}, D_{15}, and Q_{10}. D_{12} activates the fail-safe circuit if the sensor shown in Fig. 1 shorts or drops too low in value, as follows: Q_6 is on during an output pulse so that the junction of D_8 and D_{12} is 3 diode drops (approximately 2 volts) above terminal 7. As long as V_{14} is more positive or only 0.15 volt negative with respect to that point, D_{12} does not conduct and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of D_8 can have a potential of only 1.6 to 1.7 volts, and current does not flow through D_8, D_9, and Q_6; the thyristor then turns off. The actual threshold is approximately 1.2 volts at room temperature, but decreases 4 millivolts per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6 volts, the zener diode D_{15} breaks down and turns on Q_{10}, which then turns off Q_6 and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown of D_{15}, activation of the fail-safe circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may selection of the wrong external supply voltage. Fig. 11 shows a guide for the proper operation of the fail-safe circuit when an external supply is used.

SUPPLEMENTAL CHARACTERISTICS DATA

The characteristics curves shown in Fig. 12 are similar to curves shown in the published data for the CA3059 (RCA File No. 397, dated 10/69), but have been extended to cover the entire operating range from -40°C to +85°C. Fig. 13 presents data required for operation of the CA3059 from the 220-volt, 50-Hz lines which are common in Europe and from the 220-to-240-volt, 60-Hz lines which are commonly used for high-power applications in the United States. Although the CA3059 may be operated from any line voltage or frequency, the characteristics of the output pulse change for different line voltages and frequencies. Figs. 13(a) and (b) show relative pulse width and location of the zero-voltage crossing when a 10,000-ohm series dropping resistor is used. Figs. 13(c) and (d) show the same information for an increased resistor value of 20,000 ohms.

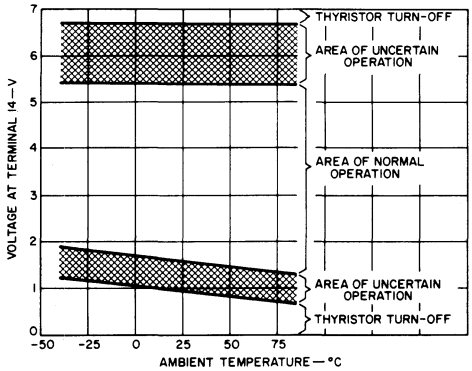


Fig. 11 - Operating regions for built-in protection circuits.

APPLICATIONS OF THE CA3059

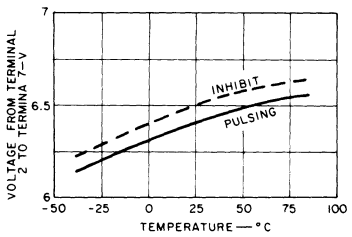
The early sections of this Note described the basic operation of the CA3059 in heating control systems. The circuit is adaptable to many other control functions by variation of the type of sensor used or by the use of the inputs of the differential amplifier to detect the difference between two externally developed voltages. A previous Application Note (ICAN-4158) describes the following useful CA3059 systems:

1) a controller with an external fail-safe circuit for use when the sensor does not meet the requirements for use of the internal circuit,
2) a controller with provisions for accurate setting of hysteresis,
3) a proportional control system with an external ramp generator,
4) a dual-output, over-under temperature controller,
5) a heat staging controller,
6) a circuit which eliminates half-cycling,
7) a circuit with an isolated sensor,
8) a power one-shot control,
9) a synchronously switched traffic flasher,
10) transient-free switch controllers.

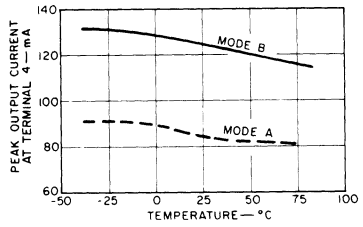
Although most of these circuits illustrate a heating control circuit, they are all adaptable to other control functions by change of the control logic or sensor.

SWITCHING INDUCTIVE LOADS

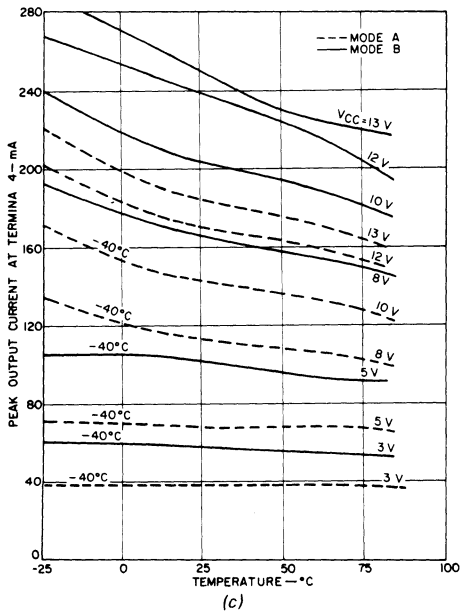
For proper driving of a thyristor in full-cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal



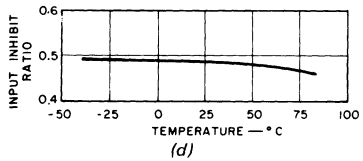
(a)



(b)



(c)



(d)

Fig. 12 - Characteristics curves of the CA3059 extended to cover the operating range from -40 to +85°C.

occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described in the published data for the CA3059. For highly inductive loads, however, this method is not suitable and different techniques must be used.

One technique is suggested in the circuit description section of this Note. If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero-crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI-eliminating function of the CA3059 is inhibited when the zero-crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

The limitation to this mode of operation is that the internal power supply cannot deliver a large average current; therefore, a sensitive-gate triac is required. Because these triacs have somewhat limited load-carrying capacity, this approach cannot be used universally.

The previous Note ICAN-4158 showed circuits which used a sensitive-gate triac to shift the firing point of the power triac by approximately 90 degrees. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Fig. 14 uses a CA3018 integrated-circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero-crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops or 1.3 volts. When A is positive, Q_3 and Q_4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, Q_1 and Q_2 conduct. When the voltage at point A is less than ± 1.3 volts, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in R_3 and output is inhibited.

The circuit of Fig. 14 forms a pulse of gate current in the manner described below, and can supply high peak drive to power triacs with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitably inductive because the zero-crossing detector is disabled and initial turn-on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3 volts; therefore, the

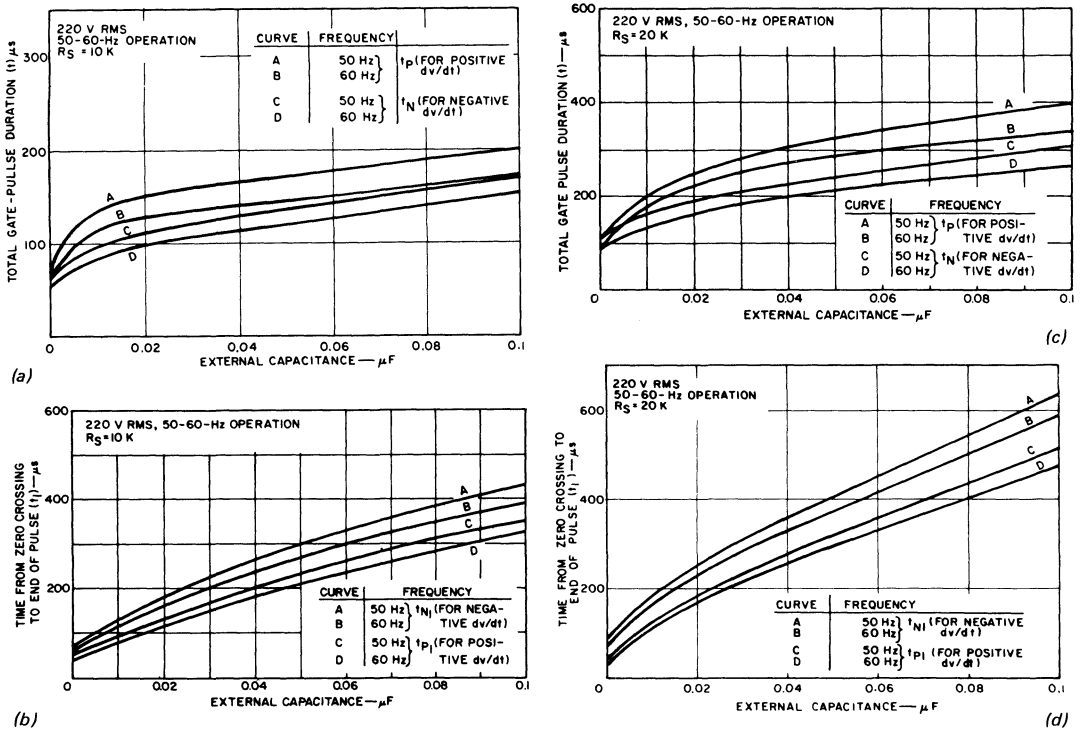


Fig. 13 - Relative pulse width and location of zero-voltage crossing for 220-volt operation.

output of the CA3059 is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one-third of the instantaneous on-state voltage (v_T) of the thyristor. For most RCA thyristors, v_T (max) is less than 2 volts and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4 volts, one portion of the CA3018 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the holding current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

PROVIDING NEGATIVE GATE CURRENT

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I^+ and III^- modes). Sensitivity is degraded when the polarities are opposite (I^- and III^+ modes). Although RCA triacs are designed and specified to have the same sensitivity in both I^- and III^+ modes, some other types have very poor sensitivity in the III^+ condition. Because the CA3059

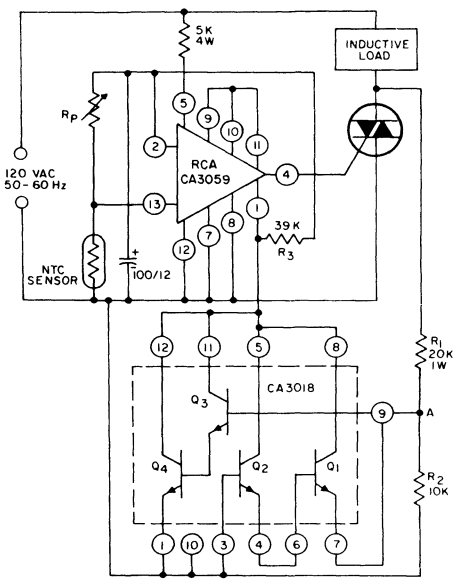
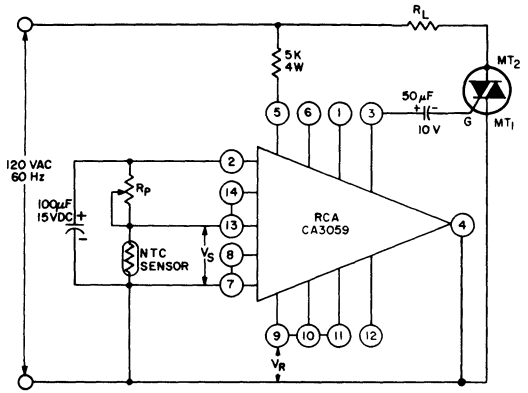


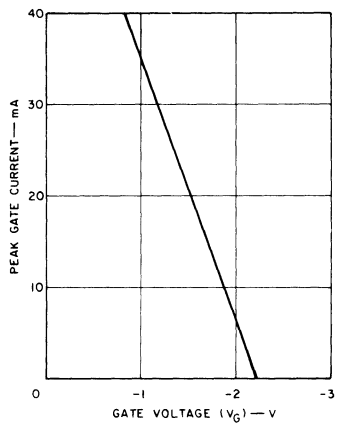
Fig. 14 - Circuit for switching inductive loads.

supplies positive gate pulses, it may not directly drive some higher-current triacs of these other types.

The circuit shown in Fig. 15 (a) uses the negative-going voltage at terminal 3 of the CA3059 to supply a negative gate pulse through a capacitor. The curve in Fig. 15 (b) shows the approximate peak gate current as a function of gate voltage V_G. Pulse width is approximately 80 microseconds.



(a)



(b)

Fig. 15 - Use of the CA3059 to provide negative gate pulses: (a) schematic diagram; (b) peak gate current (at terminal 3) as a function of gate voltage.

OPERATING WITH LOW-IMPEDANCE SENSORS

Although the CA3059 can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000 ohms are used. Typical sensitivity is one per cent for a 5000-ohm sensor and increases to three per cent for a 0.1-megohm sensor.

Low-impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000-ohm sensor with its associated 5000-ohm series resistor draws less than 1 milliampere. On the other hand, a 300-ohm sensor draws a current of 8 to 10 milliamperes from the power supply.

Fig. 16 shows the 600-ohm load line of a 300-ohm sensor on a redrawn power-supply regulation curve for the CA3059. When a 10,000-ohm series resistor is used, the voltage across the circuit is less than 3 volts and both sensitivity and output current are significantly reduced. When a 5000-ohm series resistor is used, the supply voltage is nearly 5 volts and operation is approximately normal. For more consistent operation, however, a 4000-ohm series resistor is recommended.

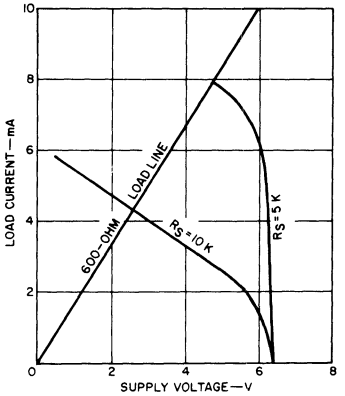


Fig. 16 - Power-supply regulation of the CA3059 with a 300-ohm sensor (600-ohm load) for two values of series resistor.

SYNCHRONOUS LIGHT FLASHER

The circuit shown in Fig. 17 is a simplified version of the system shown in the previous Note ICAN-4158. Flash rate is set by use of the curve shown in Fig. 10. If a more precise flash rate is required, the ramp generator described in the previous Note may be used. In this circuit, IC_1 is the master control unit and IC_2 is slaved to the output of IC_1 through

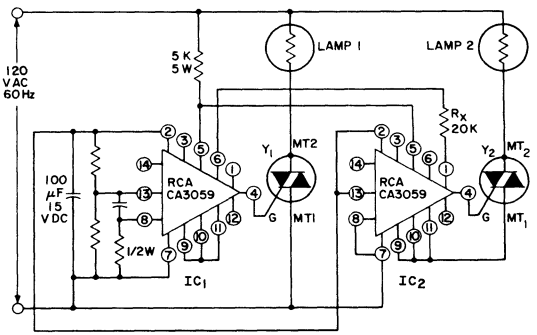


Fig. 17 - CA3059 synchronous light flasher.

its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on IC_1 is high and IC_2 is inhibited by the current in R_X. When lamp No. 1 is off, IC_2 is not inhibited and triac Y_2 can fire. The power supplies operate in parallel. The on-off sensing amplifier in IC_2 in not used.

Features and Applications of RCA-CD2500E-Series MSI BCD-to-7-Segment Decoder-Drivers

by J. Lee

The RCA BCD-to-7-segment decoder-drivers, types CD2500E, CD2501E, CD2502E, and CD2503E, are medium-scale-integration (MSI) monolithic circuits designed to accept four inputs in BCD 8-4-2-1 code and provide decoded outputs that represent a decimal number from 0 to 9 on a 7-segment incandescent display device. The decoder-drivers are supplied in 16-terminal dual-in-line plastic packages that can be used over the operating temperature range from 0°C to +75°C.

The CD2500E and CD2501E are 30-milliampere-per-line drivers intended for use with 7-segment incandescent display devices such as the RCA DR2000 and DR2010 Numitrons. The CD2502E and CD2503E are 80-milliampere-per-line drivers intended for use with high-current lamps and relays and may also be used for multiplex operation of RCA Numitrons. The CD2500E and CD2502E include a decimal-point driver, and the CD2501E and CD2503E have a special terminal that may be used for ripple blanking and/or intensity control. The basic features of the CD2500E-series 7-segment decoder-drivers are as follows:

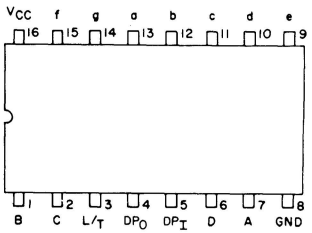
- High current-sink capability for direct display driving (no external discrete components are required)
- Provision for lamp test
- Operation from a 5-volt dc power supply
- Clamp diodes on all inputs
- Provision for ripple blanking and/or intensity control (CD2501E and CD2503E only)
- Decimal-point output (CD2500E and CD2502E only)
- BCD inputs that are compatible with commercially available diode-transistor-logic (DTL) and transistor-transistor-logic (TTL) devices
- Over-range detection (automatic blanking of display device when BCD inputs correspond to a number greater than 9)

LOGIC DESCRIPTION

Table I shows the logic levels ("0" or "1") required at each input terminal for selection of the appropriate segments on the display device to represent a specific decimal number from 0 to 9 and for the decimal-point output, the lamp test, or the ripple-blanking function. The lower-case letters over the OUTPUT columns in the table identify the segments on the display device to which each output is applied. The last column in the table indicates the type of displays obtained on the display devices for each specific combination of BCD inputs. Figs. 1 and 2 show the terminal numbers on the decoder drivers that correspond to these outputs, and Fig. 3 shows the segment arrangement and designations for two 7-segment incandescent display devices, the RCA DR2000 and DR2010 Numitrons.

Conversion of BCD Data Inputs to 7-Segment Display Outputs

The basic BCD-to-7-segment decoder-driver logic system consists of inverters, buffers, NAND gates (positive logic), TTL inputs, and open-collector transistor outputs, as shown in Fig. 4. Four information bits in BCD 8-4-2-1 code are applied to the BCD inputs. Eight input gates, Nos. 1 through



DP_O = DECIMAL POINT OUTPUT
DP_I = DECIMAL POINT INPUT

D,C,B, AND A REPRESENT THE FOUR INPUTS TO THE DECODER DRIVER (IN BCD 8-4-2-1 CODE) THAT ARE REQUIRED TO PRODUCE THE APPROPRIATE DECIMAL NUMBER ON THE DISPLAY DEVICE.

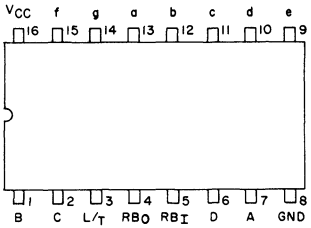
Fig. 1 - Terminal diagram for the CD2500E or CD2502E decoder-driver.

TABLE I – TRUTH TABLE FOR DECODER–DRIVER CIRCUITS

INPUT 0 = Low Level 1 = High Level							OUTPUT 0 = Filament Lit 1 = Filament OUT									DISPLAY
D	C	B	A	$L/\overline{T}$	DP_I	RB_I	a	b	c	d	e	f	g	DP_O	RB_O	
X	X	X	X	0	–	X	0	0	0	0	0	0	0	–	1	8
0	0	0	0	1	–	0	1	1	1	1	1	1	1	–	0	
0	0	0	0	1	–	1	0	0	0	0	0	0	1	–	1	0
0	0	0	1	1	–	X	1	0	0	1	1	1	1	–	1	1
0	0	1	0	1	–	X	0	0	1	0	0	1	0	–	1	2
0	0	1	1	1	–	X	0	0	0	0	1	1	0	–	1	3
0	1	0	0	1	–	X	1	0	0	1	1	0	0	–	1	4
0	1	0	1	1	–	X	0	1	0	0	1	0	0	–	1	5
0	1	1	0	1	–	X	0	1	0	0	0	0	0	–	1	6
0	1	1	1	1	–	X	0	0	0	1	1	1	1	–	1	7
1	0	0	0	1	–	X	0	0	0	0	0	0	0	–	1	8
1	0	0	1	1	–	X	0	0	0	0	1	0	0	–	1	9
1	0	1	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	0	1	1	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	0	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	0	1	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	1	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	1	1	1	–	X	1	1	1	1	1	1	1	–	1	
–	–	–	–	1	1	–	–	–	–	–	–	–	–	0	–	.
–	–	–	–	1	0	–	–	–	–	–	–	–	–	1	–	
–	–	–	–	0	X	–	–	–	–	–	–	–	–	0	–	.

X – 0 or 1 entry has no effect
$L/\overline{T}$ = Lamp Test
RB_I = Ripple Blanking Input
RB_O = Ripple Blanking Output

DP_I = Decimal Point Input
DP_O = Decimal Point Output



RBO = RIPPLE-BLANKING OUTPUT AND INTENSITY CONTROL INPUT

RBI = RIPPLE-BLANKING INPUT

D, C, B, AND A REPRESENT THE FOUR INPUTS TO THE DECODER DRIVER (IN BCD 8-4-2-1 CODE) THAT ARE REQUIRED TO PRODUCE THE APPROPRIATE DECIMAL NUMBER ON THE DISPLAY DEVICE.

Fig. 2 - Terminal diagram for the CD2501E or CD2503E decoder-driver.

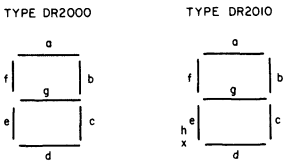


Fig. 3 - Segment arrangement and designations for two 7-segment incandescent display devices.

8, are connected in four pairs to provide the BCD data and the complements of these data to the input of ten NAND gates, Nos. 10 through 19. The ten NAND gates decode the data into their mutually exclusive outputs that represent the decimal numbers from 0 through 9 only; any BCD data that

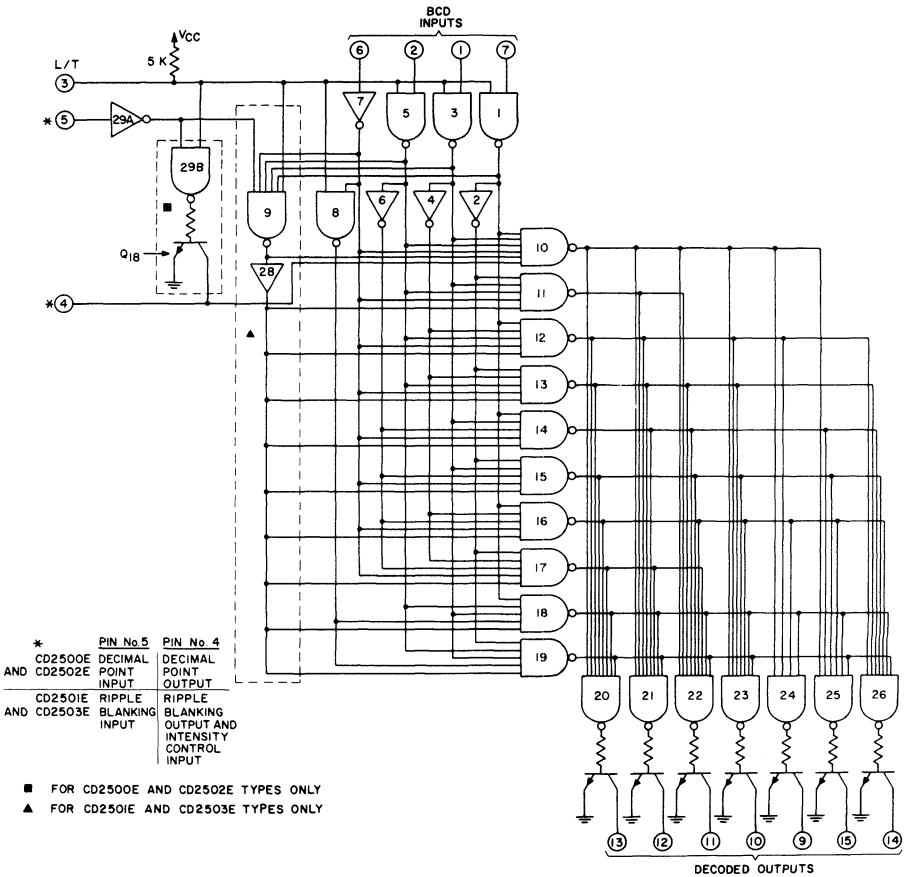


Fig. 4 - Logic diagram for the BCD-to-7-segment decoder drivers.

correspond to a number greater than 9 is inhibited. The outputs of these ten NAND gates are then encoded into seven outputs used to control the operation of a 7-segment incandescent display device by seven additional NAND gates, Nos. 20 through 26. The outputs of these seven NAND gates are applied through seven open-collector transistors that provide high current-sink capability and make possible direct-driving of the display device.

Decimal-Point Output

In the CD2500E and CD2502E decoder-drivers, gates Nos. 29A and 29B, shown in Fig. 4, develop a decimal-point output (DP_O) in response to a decimal-point-input (DP_I) control signal supplied from an external source. Transistor Q18 provides the inverter-driver function required to energize the decimal-point filament on the display device. This unique feature eliminates the necessity for separate external decimal-point driving circuitry.

Ripple-Blanking Function

The ripple-blanking feature of the CD2501E and CD2503E decoder-drivers allows suppression of leading- and/or trailing-edge zeroes in a multidigital display. This action does not affect the numerical value and provides easier reading of the decimal display.

The ripple-blanking function is performed by gates Nos. 9, 28, and 29A, shown in Fig. 4. The ripple-blanking input (RB_I) is inverted by gate No. 29A and applied to gate No. 9. Gate No. 28 is used as a buffer for gate No. 9. When the ripple-blanking input is at logical "0", gate No. 29A provides a logical "1" at the input of the ripple-blanking gate No. 9. Gate No. 9 also receives the complements of the BCD input data. This gate provides an inhibiting function for the decimal zero. When this inhibiting function occurs, i.e., when the ripple-blanking input (RB_I) and the BCD inputs are at logical "0", the ripple-blanking output (RB_O) goes to a logical "0", and all seven segment outputs to a logical "1". A logical "1" of the seven-segment output corresponds to the filament-off condition on the incandescent display device.

The ripple-blanking output terminal may also be used to provide an over-riding blanking input, regardless of other input conditions. When the ripple-blanking output is maintained at a logical "0", it inhibits all seven segment outputs, i.e., the segment outputs are maintained at a logical "1". For operation with a fixed lamp power supply, the ripple-blanking output may be used with external resistor-pull-up output gates to control lamp intensity by control of the pulse width of the gate input signal.

Lamp-Test Function

All four BCD-to-7-segment decoder-drivers include a lamp-test (L/T) input for use in testing the filaments of the display device. This input is normally maintained at a logical "1" by an internal resistor (no external circuit elements are required for the lamp-test function). For the lamp test, the L/T terminal is grounded. All segment outputs are then maintained at a logical "0", so that all lamp filaments on the display device are lighted. For the CD2500E and CD2502E, which include a decimal-point output, the L/T terminal can be grounded at any time to test all filaments in the display device including the filament for the decimal point. For the CD2501E and CD2503E, which include a ripple-blanking feature, care must be taken to assure that the ripple-blanking output is not grounded externally during the lamp test; otherwise, the test is performed in the same way as for the types CD2500E and CD2502E.

OPERATING CHARACTERISTICS

All inputs (terminals 1, 2, 5, 6, and 7) of the CD2500E-series decoder-drivers are TTL types and include clamp diodes to prevent the ringing that may result when long interconnecting leads are used. Fig. 5 shows an equivalent circuit for any one of these inputs.

Each output (terminals 9 through 15 and also terminal 4 of the CD2500E and the CD2502E) of the BCD-to-7-segment decoder-drivers consists of an open-collector transistor, together with its collector-to-substrate diode, as shown in Fig. 6. These outputs, in standard CD2500E-series devices, are specified to withstand up to 8 volts at a maximum collector-to-emitter leakage current of 200 microamperes over the operating temperature range. The transistor has a minimum collector-to-emitter breakdown voltage $V_{(BR)CEO}$ of 12 volts at a collector-to-emitter current I_{CEO} of 10 milliamperes. The output circuit, therefore, can safely withstand any load at supply voltages up to 8 volts without the occurrence of a dc-latched condition; damage to the output transistor because of excessive power dissipation is, therefore, avoided. The probability of an ac-latched condition depends upon the type

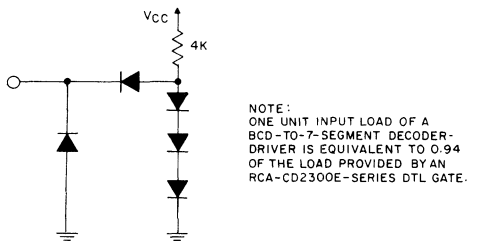


Fig. 5 - Equivalent input circuit at terminals 1, 2, 5, 6, and 7 of the decoder-drivers.

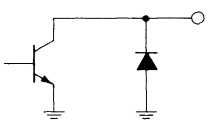


Fig. 6 - Equivalent output circuit at terminals 9 through 15 (and terminal 4 of the CD2500E and the CD2502E) of the decoder-drivers.

of load used. The circuit may become ac-latched during operation with a large inductive load. The "rule of thumb" for minimization of this probability is to ensure that the sum of the supply voltage and the counterelectromotive force developed across the lamp filament inductance does not exceed the collector-to-emitter breakdown voltage $V_{(BR)CEO}$ of the transistor.

For applications in which the output voltage may exceed the specified value of 8 volts, such as multiplex operation of RCA Numitrons, special selections of the CD2500E-series decoder-drivers are available.

The ac line voltage may also be used as the segment-voltage (lamp) supply provided that it is either half-wave or full-wave rectified so that only positive alternations remain. This type of rectification is necessary because the output transistors of the decoder-drivers cannot sustain negative voltages greater than 0.5 volt. Fig. 7 shows the relationship of the output voltage to the segment and decimal-point output currents of the CD2500E-series decoder-drivers.

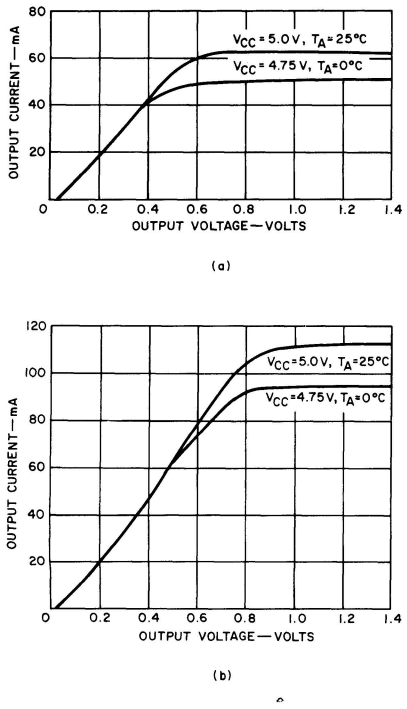


Fig. 7 - Relationship between segment and decimal-point output current (logical "0" state) and output voltage: (a) segment output currents for the CD2500E and CD2501E and decimal-point output current for the CD2500E; (b) segment output currents for the CD2502E and CD2503E and decimal-point output current for the CD2502E.

Fig. 8 shows an equivalent circuit of the ripple-blanking output (terminal 4). When the BCD code represents decimal zero and the ripple-blanking input (terminal 5) is at a logical "0", transistor Q then turns on and provides blanking of the decimal zero. When the BCD code represents a decimal number between 0 and 9, transistor Q is open-circuited. When the BCD code represents a number greater than 9, transistor Q and diode A are both open-circuited, and the ripple-blanking output circuit consists of only the 2-kilohm resistor between terminal 4 and the V_{CC} supply.

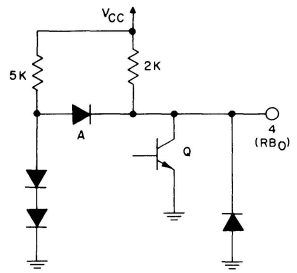


Fig. 8 - Equivalent circuit for the ripple-blanking output (terminal 4) of the CD2501E and CD2503E decoder drivers.

Supply- and ground-line noises can be effectively removed by addition of sufficient capacitance between the V_{CC} and ground lines, as near as possible to the integrated-circuit terminals. Use of separate integrated-circuit and display-device dc power supplies, although not an essential requirement, is recommended. The advantage of separate supplies is that the noise generated by high transient currents that result from lamp switching would be reduced.

DISPLAY-LAMP TURN-ON CHARACTERISTICS

The turn-on characteristics of the display lamps is an important factor in the operation of the decoder-drivers. The main consideration in these turn-on characteristics is the lamp in-rush current. For most incandescent lamps, the in-rush current may be several times greater than the normal operating current because the resistance of a cold filament is much less than that of the same filament after it has been heated to the normal operating temperature. Fig. 9 shows that the initial current of the RCA DR2000 Numitron is approximately five times greater than the normal operating current and that 2 milliseconds is required for the in-rush current to decrease to one-half the initial value. The output transistors of the decoder-drivers, therefore, must be able to handle large surge currents that are several times greater than the normal operating current of the incandescent display device. If desired, a resistor may be connected between each segment output terminal of the decoder-driver and ground so

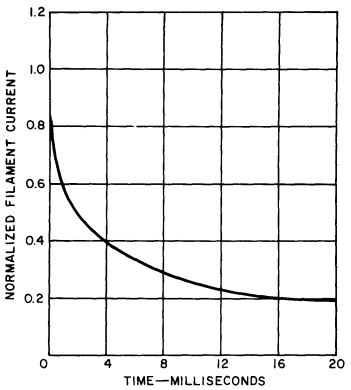
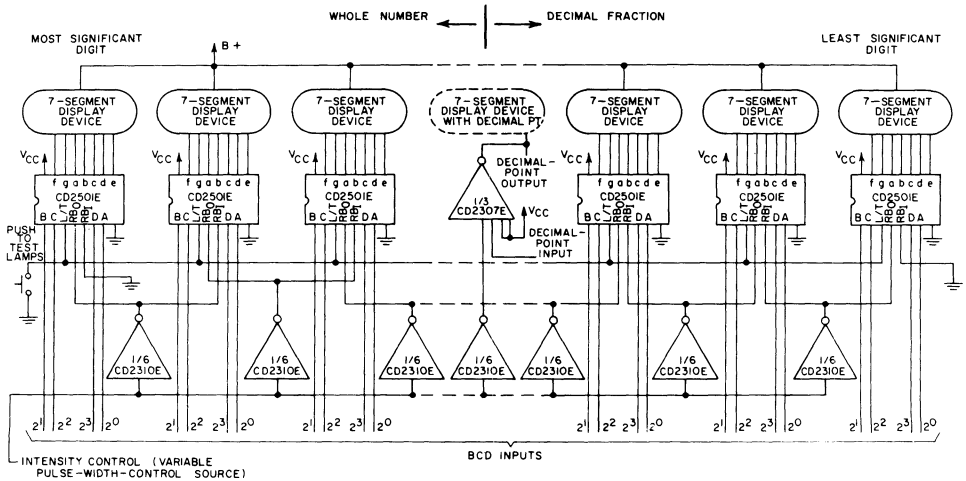


Fig. 9 - Turn-on characteristics for an RCA DR2000 Numitron.

that a small current is allowed to flow through the lamp filament during the lamp off period. This current should be sufficient to keep the filament warm, but not sufficient to illuminate the lamp. In this way, a high initial in-rush current can be avoided during the lamp turn-on period.

STATIC-DRIVE APPLICATIONS

The zeroes that have no value at both ends of a multidigital display can be suppressed by grounding the RB_I terminal of the most significant digit of the whole number and the least significant digit of the fraction, as shown in Fig. 10. The RB_O of the most significant digit is connected to the RB_I of the next lower digit, and the RB_O of this latter digit is, in turn, connected to the RB_I of the following digit. The RB_O of the least significant digit of the fraction side is connected to the RB_I of the next higher digit, and so on. Therefore, for the whole number, the ripple signal flow originates from the most significant digit, and for the fraction, the ripple signal flow starts from the least



CHARACTERISTICS OF THE DISPLAY DEVICES

DISPLAY DEVICE TYPE	TYPE OF DISPLAY	CHARACTERISTICS
DR2000		REQUIRED DRIVING CURRENT = 24 ±2 mA PER SEGMENT
DR2010		LETTER HEIGHT = 0.6 INCH

Fig. 10 - Typical ripple-blanking and intensity-control application using the CD2501E decoder driver with a 7-segment incandescent display device, such as the RCA DR2000 or DR2010.

significant digit. As soon as the BCD data inputs for a non-zero digit is encountered, the corresponding RB_O output assumes a logical "1" state, and any further signal rippling is inhibited. For example, the number 0102,0110 would be displayed as 102.011. The RB_I of the least significant digit of the whole number and the RB_I of the most significant digit of the fractional portion should be left open, because the suppression of zeroes in these two digits is not desirable in practice, e.g., 000.200 would be displayed as 0.2, and 000.000 would be 0.0.

The ripple-blanking arrangement described above is employed in the standard multiple-digit display. For other applications, however, ripple blanking may be used to blank out zeroes serially in time, as shown in Fig. 11. For this type of blanking, the ripple-blanking input RB_I and the ripple-blanking output RB_O are connected together. Fig. 11 shows that the zeroes that occur at time frames t_1 and t_2 are blanked out, and those that occur at time frames t_4 and t_6 are not. A ground-level strobe pulse must be injected at the

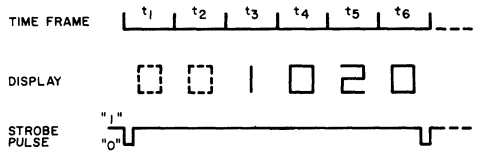


Fig. 11 - Timing diagram for ripple blanking that occurs serially in time.

connection of the RB_I and RB_O terminals to cause these terminals to be latched at the logical "0" level. This strobe pulse initiates the blanking operation. The RB_I and RB_O terminals are maintained at the "0" level until the BCD input data for a non-zero digit is applied. The RB_I and RB_O terminals are then shifted to a logical "1" level, and further zero blanking is inhibited.

The ripple-blanking output can also be used simultaneously as an intensity-control input when the lamp power-supply voltage is fixed. For this intensity-control effect, external gates are required, and an RCA CD2310E DTL type is chosen for this purpose, as shown in Fig. 10. The intensity control is achieved by variation of the pulse width of the signal at the intensity-control input (RB_O terminal). Pulse-width-controlled flip-flops can be used as the source for the intensity-control input. The logical "0" state of the external gates at the point of connection to the intensity control terminal should not be greater than 0.35 volt. For the CD2500E and CD2502E decoder-drivers, intensity control can be provided by variation of the segment power-supply voltage. Fig. 12 shows the relative light output of an RCA DR2000 Numitron at 50Hz as a function of pulse duty cycles for operation with a supply voltage of +5 volts.

The CD2500E decoder-driver is frequently used in counting applications, as shown in Fig. 13. A display-hold circuit is included to hold counts for the display device while

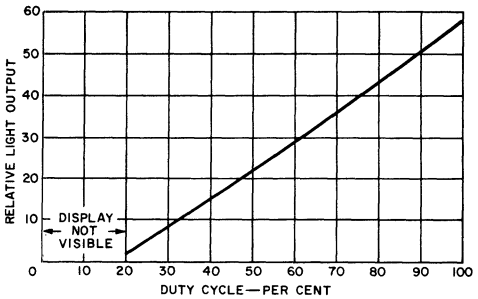


Fig. 12 - Relative light output of a DR2000 Numitron at 50 Hz as a function of pulse duty cycle for operation from a lamp-supply voltage of 5 volts.

the input count continues. The display-hold signal is usually synchronized with the count input signal. The hold circuit, which can be formed by use of latching flip-flops, is used because no data storage is provided in the decoder-driver. The decoder-driver simply operates as a slave circuit for the input data; the outputs of the decoder-driver, therefore, follow directly any change in the data applied to its inputs.

Fig. 14 illustrates the use of six CD2301E stages in a floating-decimal-point application. The selection of a decimal point requires that the corresponding decimal-point-select

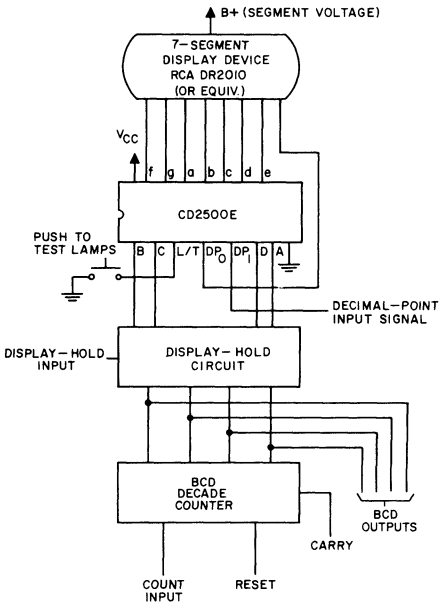


Fig. 13 - Counting circuit using the CD2500E decoder-driver.

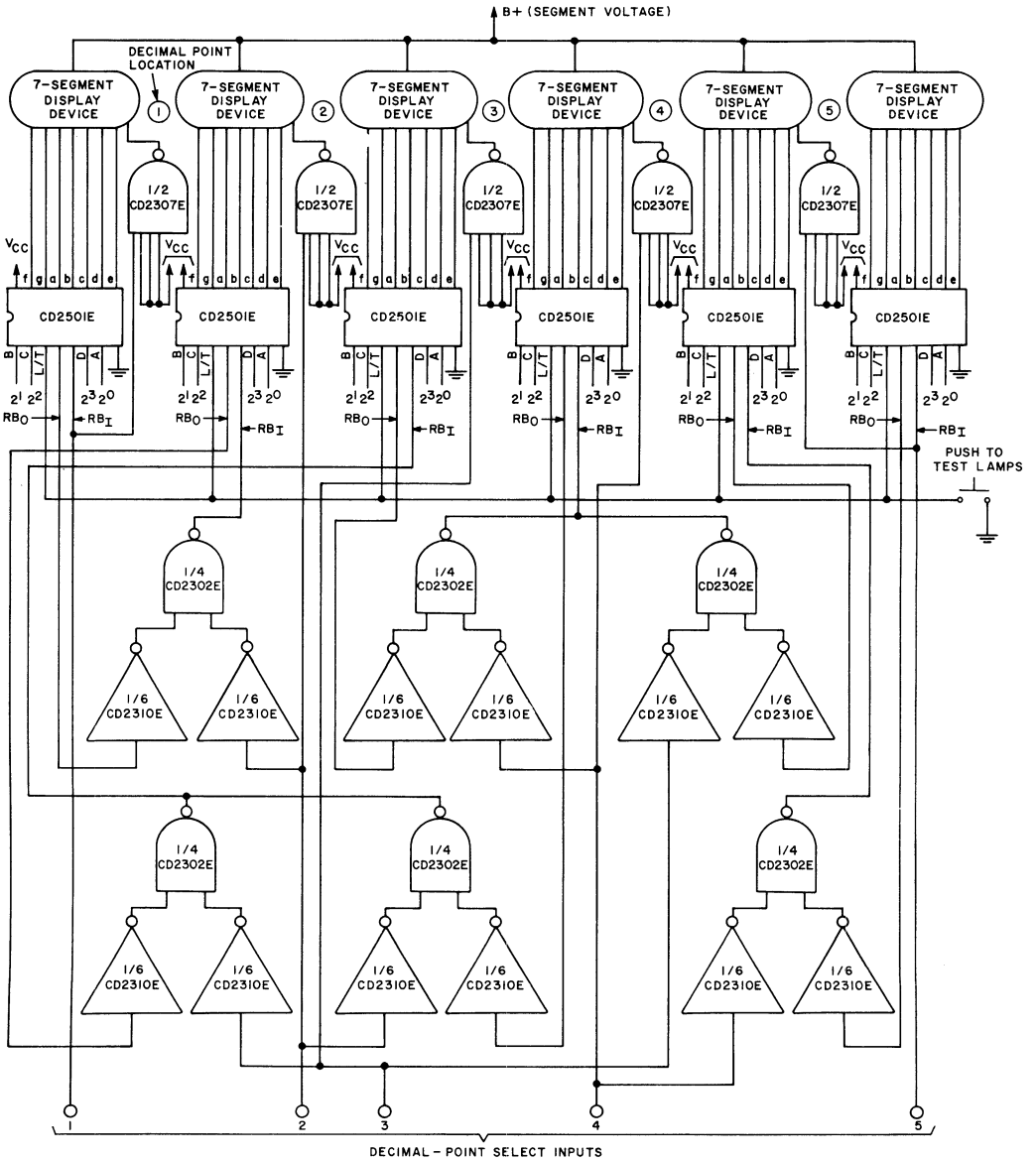


Fig. 14 - Floating-decimal-point application using six CD2501E decoder-drivers.

input be held at logical "1" with the other decimal-point-select inputs at logical "0". The operation is similar to the ripple-blanking application shown in Fig. 10, in which the flow of the ripple signals always starts from the extreme ends and move toward the chosen decimal point. The ripple input of the immediately adjacent stages on either side of the decimal point is made a logical "1" by the external gates, so that the ripple signal flow is terminated at these points and, therefore, cannot suppress zeroes in the two digits adjacent to the chosen decimal point.

The RCA CD2307E gate is used to energize the decimal-point filament in the display device, and CD2302E and CD2310E gates are used to enable the ripple-blanking circuits to blank out the no-value zeroes.

MULTIPLEX MODE OF OPERATION

In the standard static-drive application, a given number of display devices requires an equal number of decoder drivers for simultaneous display of the BCD data. In the time-multiplex system, however, one decoder-driver can be operated to drive a number of display devices sequentially with no noticeable flicker when the multiplexing repetition rate is greater than 50Hz. Fig. 15 shows a typical application of the CD2502E decoder-driver in the multiplexing mode of operation.

The complementary BCD data information is fed to the multiplexing NAND gate inputs and multiplexed in sequence by the trains of pulses, shown in Fig. 16, obtained from a ring counter. The complementary BCD data available at the input of a given set of multiplexing NAND gates during the pulse duration is inverted to BCD data and applied to the decoder driver. This decoder data, in turn, causes the proper decoder-driver output transistor to turn on. At the same time, the pulse complement is fed to the corresponding digit control gate, as shown in Fig. 15, so that the associated transistor Q_m is caused to conduct and provide segment current to the appropriate filaments of the display device.

Isolation diodes are required in series with each segment coil of the display devices, to prevent "sneak paths" which would simultaneously light segment coils of adjacent devices. In this circuit, one CD2502E 7-segment decoder-driver, which is specially selected for an output voltage rating V_{oh} of 12 volts, can be used to drive up to a maximum of six DR2010 Numitrons with a 16.7 per cent duty cycle. When the specially selected CD2503E is used, a blanking circuit may be incorporated at the ripple-blanking input terminal to blank out the no-value zeroes, if desired. Care must be taken to ascertain that, during multiplexing operation, the breakdown-voltage rating and the maximum output current rating of the decoder-driver are not exceeded, and transistor Q_m, shown in Fig. 15, must be carefully chosen to handle the maximum current required.

From the standpoint of packaging, troubleshooting, and system reliability, the static-drive mode of operation is generally preferable to the multiplexing mode. However, on the basis of the present costs of a decade that includes a decade counter and a readout device, an economic advantage can result for a display that employs more than six readout devices when the readout devices are multiplexed so that only one decoder driver is required. With the advances being made in integrated-circuit technology and as the demand for readout devices increases, it is anticipated that, during the next few years, the cost of decade devices will decrease to less than one-half the present cost. The multiplexing mode of operation then will no longer offer a significant economic advantage and will become even less desirable.

FAIL-SAFE CIRCUIT

Fig. 17 shows the diagram of a circuit designed to monitor the currents through filaments a, b, e, f, and g (refer to Fig. 3) of a display device. If any one of these five filaments should fail (open), the complete digit being displayed will be blanked out to avoid incorrect readings. Filaments c and d are not monitored, because failure of either of these filaments is readily indicated by incomplete or distorted digit displays.

With this circuit included in the display system, the standard lamp test can still be performed at any time. Moreover the over-range blanking provided by all four decoder-driver circuits and the ripple-blanking feature of the CD2501E and CD2503E circuits are not affected by the fail-safe circuit.

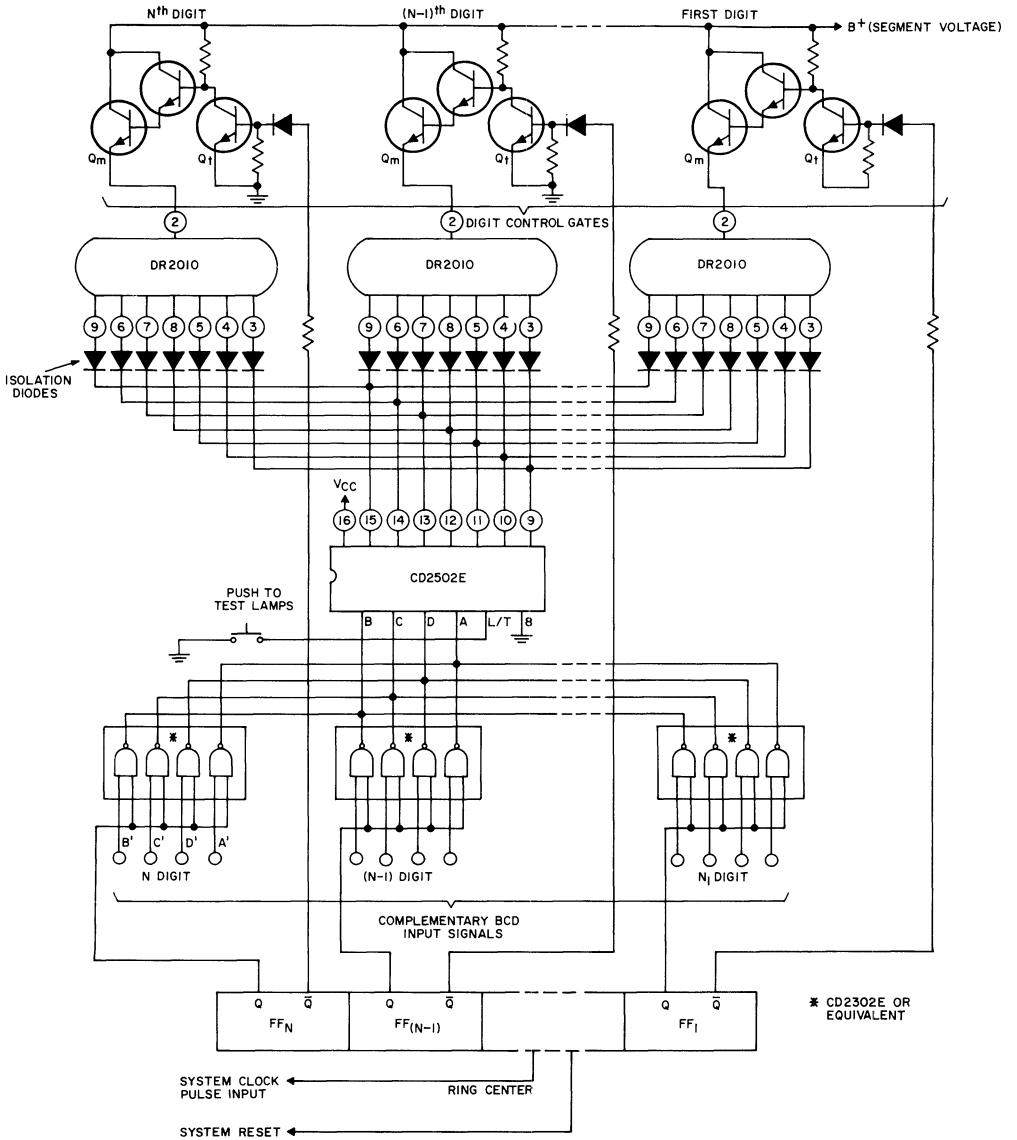


Fig. 15 - Typical multiplexing system using the CD2502E decoder-driver.

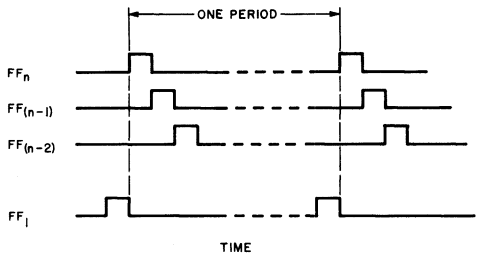


Fig. 16 - Timing relationship of the pulse trains supplied by the ring counter in the multiplexing system shown in Fig. 15.

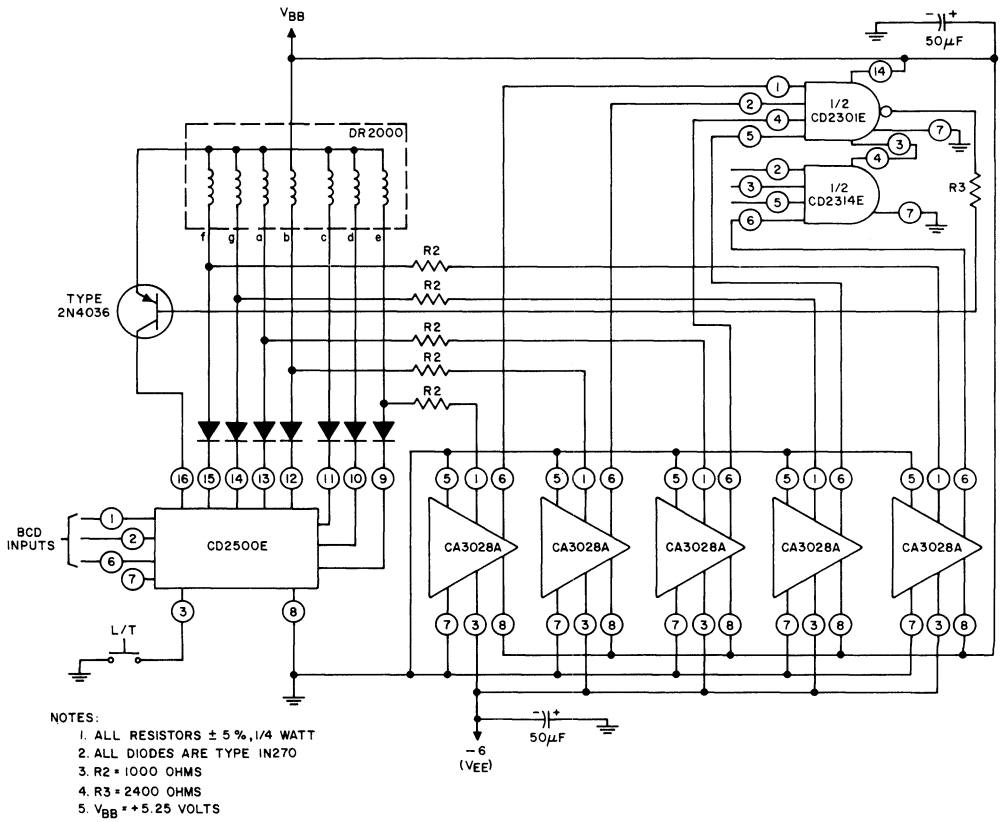


Fig. 17 - Fail-safe circuit designed to monitor filaments of the display devices.

Applications of the RCA-CA3062 IC Photo-Detector and Power Amplifier in Switching Circuits

by J. D. Mazgy

The RCA CA3062 is a monolithic silicon integrated circuit consisting of a photosensitive detector and a switching amplifier with a pair of high current output transistors. This note describes how the CA3062 with only 3 resistors can provide a light activated switch which will drive a variety of practical loads; such as solenoids, relays, triacs, SCR's, etc. "Normally ON" and "Normally OFF" outputs are available simultaneously.

Circuit Description

The circuit diagram and terminal connections for the CA3062 are shown in Fig. 1. The circuit consists of a photo-Darlington pair and a differential amplifier which is emitter-follower coupled to a pair of high-current output transistors, Q_6 and Q_7.

Circuit Operation

The CA3062 is designed for operation from power supply voltages of 5 to 15 volts between terminal Nos. 4 and 8, and voltages as high as 30 volts V+ on the output transistors.

The photo-detector system consists of four silicon transistors Q_1 and Q_9, with Q_{10} and Q_{11} in a parallel-connected Darlington circuit. The Darlington configuration is used to provide maximum photo current from the available detector area. The area of each photo-transistor is 1.3×10^{-4} cm^2. However, the effective photo-sensitive area is 2.6×10^{-4}cm^2 because transistors Q_1 and Q_{11} of each Darlington contribute a relatively small percentage of the total photo-current.

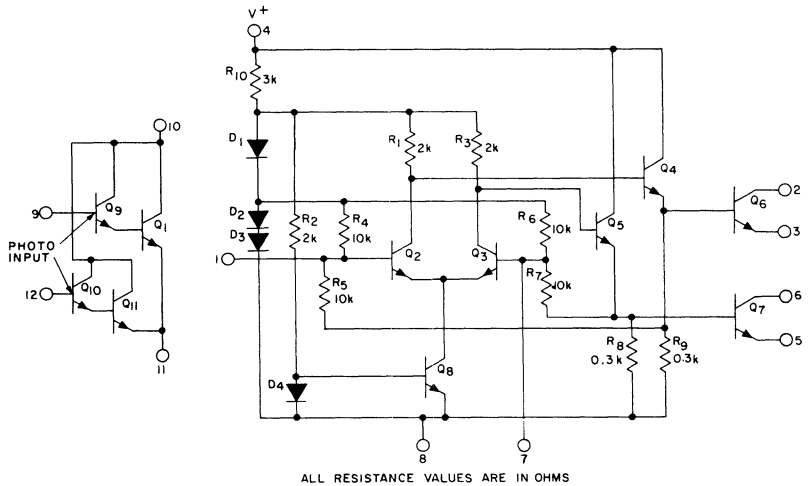


Fig. 1 – Schematic diagram of CA3062.

Fig. 2 shows a typical curve of photo-current in the collector and base as a function of light intensity. Fig. 3a & b shows the test set up used to obtain the data for Fig. 2. A typical spectral response curve of the photo sensitive Darlington is shown in Fig. 4. Fig. 5 shows typical rise and fall times for the photo detector output.

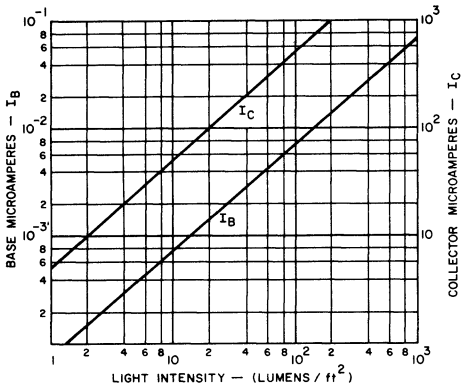


Fig. 2 — Typical I_C, I_B as a function of light intensity at 25°C.

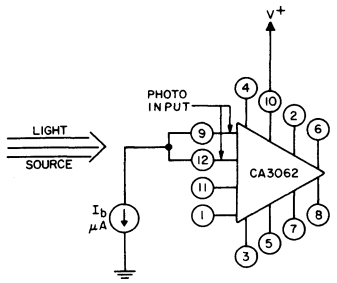


Fig. 3a — Base current test set-up.

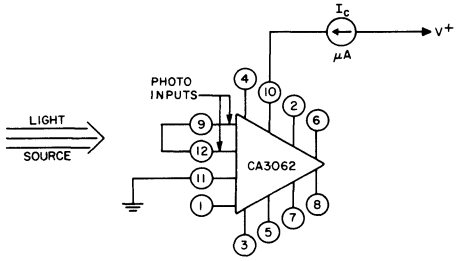


Fig. 3b — Collector current test set-up.

Fig. 3 — Test circuits.

The photo Darlington pair can be either emitter-coupled or collector-coupled to the differential amplifier consisting of Q_2 and Q_3 and constant current sink Q_8, operating with a total current of 0.7mA as shown in Figs. 6a and 6b,

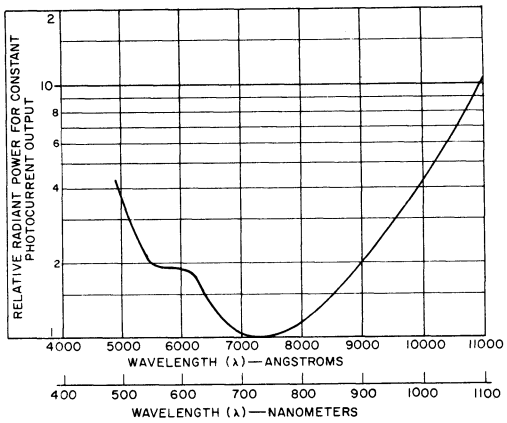


Fig. 4 — Typical spectral response of photosensitive Darlington unit.

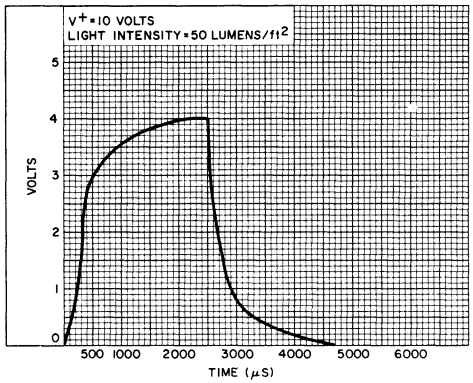


Fig. 5 — Typical photo-Darlington response.

respectively. The emitter-coupled mode is generally recommended. However, there are applications in which the collector-coupled mode is advantageous. Examples of the collector-coupled mode are shown in Figs. 8, 12 & 13.

In a balanced condition Q_2 and Q_3 are conducting 0.35mA each, which sets the dc voltage of each of the collectors of Q_2 and Q_3 at 0.7 volt below the three diode drops of D_1, D_2 and D_3.

With the dc potential on collectors Q_2 and Q_3 determined to be +1.4 volts above reference terminal No. 8, the voltage on the emitters of Q_4 and Q_5 then is 0.7 volt below the respective base, and, therefore, +0.7 volt above the reference point. Thus, the base potentials of Q_2 and Q_3 are set to +1.05 volts and +0.7 volt for Q_6 and Q_7, respectively. The emitter currents of Q_4 and Q_5 are set to approximately 2.33mA each under the balanced condition.

The input resistance at terminal No. 1 is approximately 1.4kΩ in the balanced mode with signals less than ±25mV.

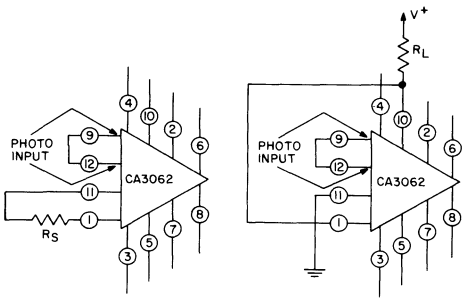


Fig. 6a – Emitter Coupled. *Fig. 6b – Collector Coupled.*

Fig. 6 – Methods of coupling photo-detector to amplifier portion of CA3062.

Recommended Operating Circuit:

To assure positive transistion between the "ON" and "OFF"states, Schmitt trigger operation is recommended.

Schmitt trigger operation can be achieved by connecting the CA3062 as shown in the circuit of Fig. 7. R_f provides the positive feedback which causes Q_3 to conduct and holds Q_7 in cut-off. A positive going voltage applied to terminal No. 1 will result in a change of output state. Resistor R_S limits the drive to the differential amplifier when high light levels are encountered. R_S is chosen to insure that the voltage at terminal No. 1 does not exceed 1.9 volts. If this voltage is exceeded, Q_6 will turn on. This overdrive condition causes both output transistors to be "ON". (Q_6 is supposed to be cutoff when the voltage at terminal No. 1 is more positive than the voltage at terminal No. 7). If the "Normally ON" output at terminal No. 2 is not being used, resistor R_S is not required, and terminal Nos. 2 and 3 should be left unconnected. (See Fig. 7.) The magnitude of the threshold voltage and the amount of hysteresis provided are determined by the value of the feedback resistor R_f. (See appendix for calculations.)

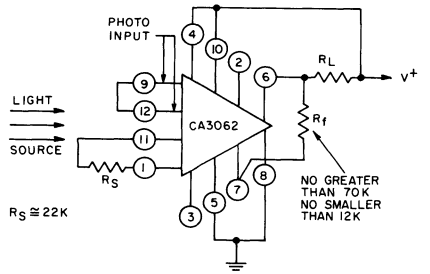


Fig. 7 – Schmitt-circuit.

Typical Applications

Latched Memory Circuit

A latched memory system can be used to stop clocks, record an intrusion, or activate light-actuated dark-room controls.

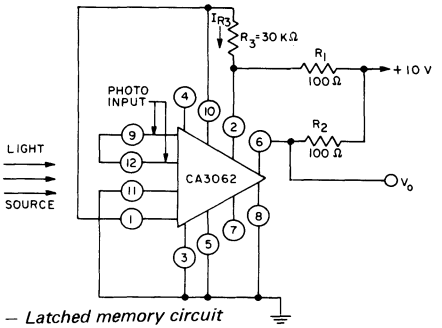


Fig. 8 – Latched memory circuit

Circuit Operation of Latched Memory

The initial conditions are: terminal No. 2 at "high"-output-voltage and terminal No. 6 at "low"-output-voltage. This condition is assured by the 30kΩ Resistor (R_3), which biases Q_2 on, Q_6 off and Q_7 on. When a light pulse is received, Q_1 turns on and takes base drive away from Q_2, turning on Q_6 thereby reversing the initial conditions. Q_6 remains on because terminal No. 1 is now more negative than terminal No. 7. Momentary interrupting of V+ will reset the circuit.

The photo current required to trigger a typical circuit is:

$$I_{R_3} \cong \frac{V^+ - V_{B21}}{R_3} = \frac{9}{(30)(10^{-3})} = (300)(10^{-6}) \text{ ampere}$$

More exactly:

$$I_{B3} = \frac{V \pm V_{B21}}{R_3} + \frac{60mV}{R_{B2}}$$

$$I_{R3} = \frac{9}{30 \times 10^{+3}} + \frac{60 \times 10^{-3}}{5 \times 10^{-3}} = \frac{300 \times 10^{-6}}{1} + \frac{60 \times 10^{-6}}{5} = 312 \times 10^{-6}$$

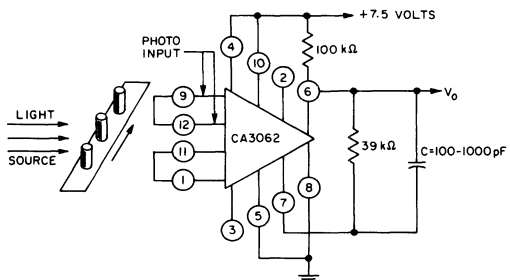


Fig. 9 – Circuit for slow speed counting level control, position sensor and end-of-tape control.

or an I_C produced by approximately 50 lumen/ft^2 at the photo-detector input. (See Fig. 3.)

Fig. 9 shows a circuit for a Photo-Detector Counting Control, Position Sensor or End-of-Tape Control.

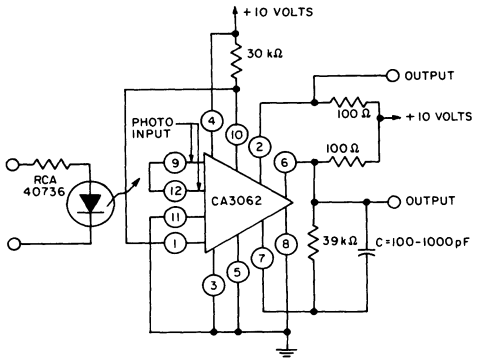


Fig. 10 – Isolator circuit.

TRIAC CONTROL SYSTEMS

A. Light Activated Triac Control

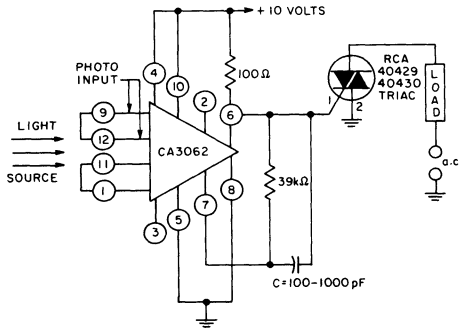


Fig. 11 – Light activated triac control.

An Optically Coupled Isolator Circuit, used to transfer signals that are at substantially different voltage levels, is shown in Fig. 10. Both polarity outputs are available. Current transfer ratios of as high as 10:1 can be achieved with this circuit. The design equations for this system are the same as those presented in the appendix.

B. Triac Control With Safety Feature Providing Automatic Shut Off And Alarm.

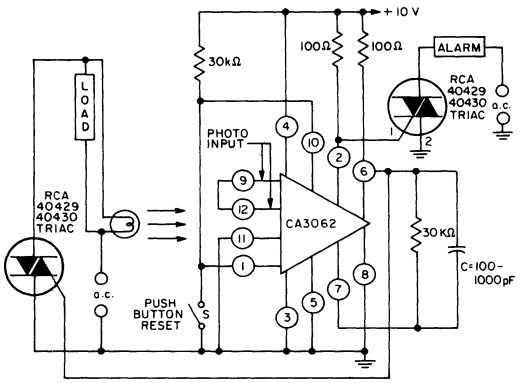


Fig. 12 – Triac automatic shut off and alarm.

In this system ac is supplied to the load as long as the light source is "on". If the light path to the CA3062 is broken, then the ac to the load and light source is opened, thereby activating the alarm circuit. The system can be reset with the push-button shown.

C. Triac Intrusion Alarm System.

If the light path is broken or the ac is interrupted, the alarm system will be activated, provided the battery is adequately charged.

The V+ acts as a charging circuit for the battery while the circuit is operating from the ac supply.

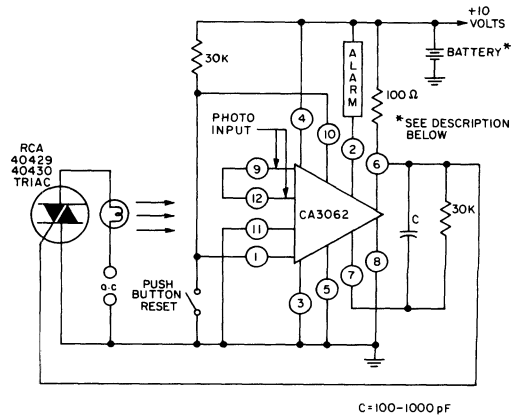


Fig. 13 – Triac intrusion alarm system.

APPENDIX

In general, Schmitt circuits have three voltages of interest.

V_I trigger: the voltage required to trigger the Schmitt from state I to state II.

V_{II} trigger: the voltage required to trigger the Schmitt from state II back to state I.

V hysteresis: the difference between the V_1 trigger and V_2 trigger. The hysteresis voltage for the configuration described is altered by the internal feedback of the CA3062 circuit which modifies the hysteresis expression.

Fig. a shows a typical configuration for operation as a Schmitt-Circuit.

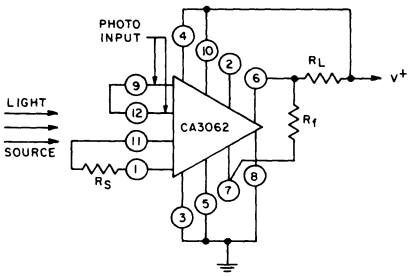


Fig. a – Schmitt-circuit

The trigger potential (V_I) to go from state I to state II is:

$$V_I \text{ trigger} = \frac{(V^+ - V_{B31})\,R_{B3}}{R_{B3} + R_f + R_L} + \frac{V_{B31}}{1}:$$

Where state I is defined as the case with pin 6 at a "high" output voltage, with no light into the Darlington photodetector. State II is defined as the case with pin 6 at a "low" output voltage, with no light into the Darlington photodetector.

and: $V_{B21} = 1.050\,V$ $\quad R_{B2} = R_4//R_5$ (Refer to Fig. 1)
$V_{B31} = 0.700\,V$ $\quad R_{B3} = R_6//R_7$
$V_{B22} = 0.700\,V$
$V_{B32} = 1.050\,V$

The trigger potential (V_{II}) to go from state II back to state I is--

$$V_{II} \text{ trigger} = \frac{V_{B32}}{1} - \frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}$$

The hysteresis voltage of the CA3062 Schmitt system is:

$$V \text{ hysteresis} = \left[\frac{(V^+ - V_{B31})\,R_{B3}}{R_{B3} + R_f + R_L} + \frac{V_{B31}}{1} + \frac{V_{B22}}{1} - \frac{V_{B21}}{1}\right] - \left[\frac{V_{B32}}{1} - \frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}\right]$$

The light intensity required to switch from state I to state II is determined from Fig. 2, which shows the number of lumens/ft^2 necessary to generate I_{CI}.

$$I_{CI} = \frac{V_{SIG\ I}}{R_{B2}} = \frac{V_{SIG\ I}}{5 \times 10^3}$$

where:

$$V_{SIG\ I} = \frac{(V^+ - V_{B31})\,R_{B3}}{R_{B3} + R_f + R_L} + \frac{V_{B31}}{1} - \frac{V_{B21}}{1}$$

To determine the lumens/ft^2 required to go from state II back to state I, it is necessary to calculate $V_{SIG\ II} + V_{B22}$, (the voltage required to cause the Schmitt circuit to switch).

$$V_{SIG\ II} + V_{B22} = \frac{V_{B32}}{1} - \frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}$$

Thus:

$$V_{SIG\ II} = V_{B32} - \left[\frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}\right] - \left[\frac{V_{B22}}{1}\right]$$

and:

$$I_{CII} = \frac{V_{SIG\ II}}{R_{B2}} = \frac{V_{SIG\ II}}{5k}$$

The rate at which V_{SIG} rises is governed by the response of the photo Darlington pair.

V_{SIG} during the rise time assumes a value:

$$V_{SIG} = V_m\,(1 - e^{\frac{-t}{RC}});$$

where V_m is the maximum signal voltage developed across terminal No. 1 and reference terminal No. 8 for any given light intensity. [See Fig. 4.].

The rise time of a typical photo Darlington of the CA3062 is:

$$t_r = \frac{RC \log \left[1 - \frac{1}{\frac{V_c}{V_m}}\right]}{\log e}$$

where $R = 40 \times 10^6$ and $C = 8 \times 10^{-12}$ and V_C any part of V_m.

APPENDIX (cont'd.)

By setting $V_C = V_{SIG\ I}$ the delay time, t_d, of the pulse output of the Schmitt circuit can be determined for any given light intensity.

The rate at which the photo Darlington output decreases is:

$$V_{SIG} = V_m e^{\frac{-t}{RC}}$$

Thus the fall time is

$$t_f = \frac{RC \log \frac{V_m}{V'_c}}{\log e}$$

Setting $V_C = V_{SIG\ II}$, then t_f becomes t_d which is turn off delay time, or the time the Schmitt circuit turns off with respect to the time the light input to the photo Darlington has been turned off. See Fig. b.

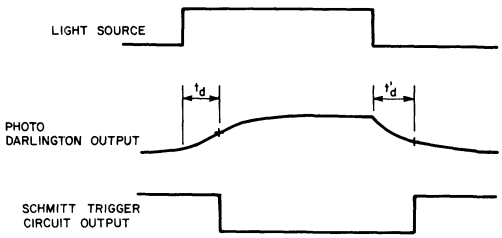


Fig. b – Waveforms for rise and fall response.

Application Notes on IC Operational Amplifiers

ICAN-5015	"Application of the RCA-CA3008 and CA3010 Integrated-Circuit Operational Amplifiers"	262
ICAN-5213	"Application of the RCA-CA3015 and CA3016 Integrated-Circuit Operational Amplifiers"	277
ICAN-5290	"Integrated-Circuit Operational Amplifiers"	283
ICAN-5641	"Application of RCA-CA3033 and CA3033A High-Performance Integrated-Circuit Operational Amplifiers"	303
ICAN-6668	"Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers"	311
ICAN-6732	"Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits"	327

Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers

BY
A. J. LEIDICH

The RCA CA3008 and CA3010 Operational Amplifiers are silicon monolithic integrated circuits designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from ±3 volts to ±6 volts). The power dissipation in the amplifiers ranges from 7.0 milliwatts to 92 milliwatts depending upon the supply-voltage level and the desired output-power level. The amplifiers are primarily intended to operate with externally applied negative feedback; however, they may also be operated successfully under open-loop conditions. The main features of the CA3008 and CA3010 Operational Amplifiers are listed below:

- All-monolithic construction designed to operate at ambient temperatures from −55°C to +125°C.
- Built-in temperature compensation which assures that the gain and dc operating point are stable over the temperature range of −55°C to +125°C.
- Capability of operating at extremely low dissipation and supply-voltage levels, as well as at medium levels.
- Balanced differential-amplifier input configuration and a single-ended output configuration.
- No shift in the dc level between the differential inputs and the output.
- Little effect on the input offset voltage from variations in the power-supply voltages.

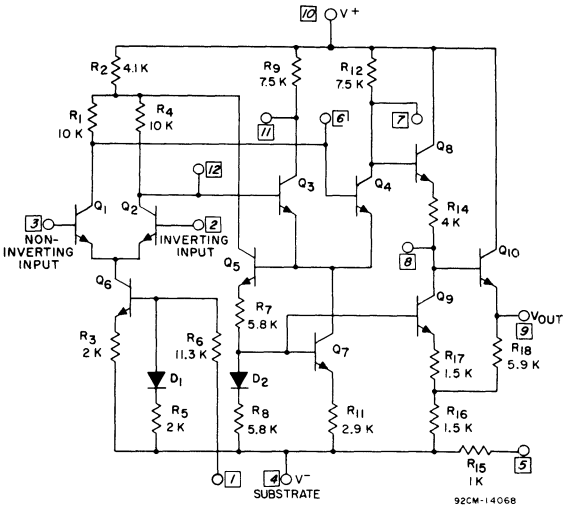
The CA3008 Operational Amplifier is supplied in a 14-terminal flat-pack; the CA3010 Operational Amplifier is supplied in a conventional 12-terminal TO-5 package. With the exception of the differences in their package construction, the two operational amplifiers are identical. This note describes the circuit arrangement, lists the performance characteristics, explains the major design considerations, and discusses typical applications of the operational amplifiers.

CIRCUIT DESCRIPTION

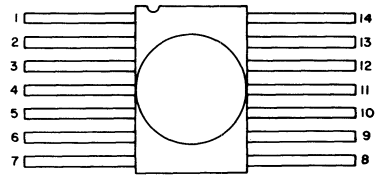
Fig. 1 shows the schematic diagram of the CA3008 or the CA3010 Operational Amplifier. The numerals shown alongside the circuit terminals indicate the terminal designations for the CA3008 14-terminal flat-pack and CA3010 12-terminal TO-5 package. The numerals enclosed in squares are the designations for the CA3010 package. The diagram in the upper right corner of the figure shows the orientation of the terminals on the CA3008 flat-pack; the diagram at the lower right corner shows the orientation on the CA3010 TO-5 package. (The number designations used to refer to specific terminals in the following discussion, or elsewhere in this note, are those for the CA3008 14-terminal flat-pack. The corresponding terminals on the

CA3010 12-terminal TO-5 package can be determined from the schematic in Fig. 1.)

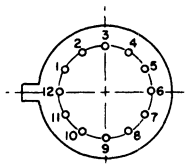
As shown in the schematic diagram, each operational amplifier consists basically of two differential amplifiers and a single-ended output circuit in cascade. Circuit elements are also included to provide thermal stabilization and to compensate for shifts in the dc operating point. In addition, negative feedback loops are employed to cancel common-mode signals (i.e., error signals developed when the two inputs to the operational amplifier are in phase and of equal amplitude).



Note: R_{10} and R_{13} not used.



CA3008
14-TERMINAL FLAT-PACK



CA3010
12-TERMINAL TO-5 PACKAGE

Fig. 1—Schematic diagram of the CA3008 or CA3010 Integrated-Circuit Operational Amplifier.

CASCADED GAIN STAGES

The pair of cascaded differential amplifiers are responsible for virtually all the gain provided by the operational-amplifier circuit. The inputs to the operational amplifier are applied to the bases of the pair of emitter-coupled transistors, Q_1 and Q_2, in the first differential amplifier. The inverting input (at terminal 3) is applied to the base of transistor Q_2, and the noninverting input (at terminal 4) is applied to the base of transistor Q_1. These transistors develop the driving signals for the second differential amplier. A dc constant-current-sink transistor, Q_6, is also included in the first stage to provide bias stabilization for transistors Q_1 and Q_2. Diode D_1 provides thermal compensation for the first differential stage.

The emitter-coupled transistors, Q_3 and Q_4, in the second differential amplifier are driven push-pull by the outputs from the first differential amplifier. Bias stabilization for the second differential amplifier is provided by current-sink transistor Q_7. Compensating diode D_2 provides the thermal stabilization for the second differential amplifier and also for the current-sink transistor, Q_7, in the output stage.

COMMON-MODE-REJECTION FEEDBACK LOOPS

Transistor Q_5 develops the negative feedback to reduce common-mode error signals that are developed when the same input is applied to both input terminals of the operational amplifier. Transistor Q_5 samples the signal that is developed at the emitters of transistors Q_3 and Q_4. Because the second differential stage is driven push-pull, the signal at this point will be zero when the first differential stage and the base-emitter circuits of the second stage are matched and there is no common-mode input. A portion of any common-mode, or error, signal that appears at the emitters of transistors Q_3 and Q_4 is developed by transistor Q_5 across resistor R_2 (the common collector resistor for transistors Q_1, Q_2, and Q_5) in the proper phase to reduce the error. The emitter circuit of transistor Q_5 also reflects a portion of the same error signal into current-sink transistor Q_7 in the second differential stage so that the activating error signal is further reduced.

Transistor Q_5 also develops feedback signals to compensate for dc common-mode effects produced by variations in the supply voltages. For example, a decrease in the dc voltage from the positive supply results in a decrease in the voltage at the emitters of transistors Q_3 and Q_4. This negative-going change in voltage is reflected by the emitter circuit of transistor Q_5 to the bases of current-sink transistors Q_7 and Q_6. Less current then flows through these transistors. The decrease in the collector current of transistor Q_7 results in a reduction of the current through transistors Q_3

and Q_4, and the collector voltages of these transistors tend to increase. This tendency to increase on the part of the collector voltages partially cancels the decrease that occurs with the reduction in the positive supply voltage. The partially cancelled decrease in the collector voltage of transistor Q_4 is coupled directly to the base of transistor Q_8 and is transmitted by the emitter circuit of this transistor to the base of output transistor Q_{10}. At this point, the decrease in voltage is further cancelled by the increase in the collector voltage of current-sink transistor Q_6 that results from the decrease in current mentioned above.

In a similar manner, transistor Q_5 develops the compensating feedback to cancel the effects of an increase in the positive supply voltage or of variations in the negative supply voltage. Because of the feedback stabilization provided by transistor Q_5, the CA3008 and CA3010 Operational Amplifiers provide high common-mode rejection, have excellent open-loop stability, and have a low sensitivity to power-supply variations.

OUTPUT STAGES

In addition to their function in the cancellation of supply-voltage variations, transistors Q_7, Q_9, and Q_{10} are used in an emitter-follower type of single-ended output circuit. The output of the second differential amplifier is directly coupled to the base of transistor Q_7, and the emitter circuit of transistor Q_7 supplies the base-drive input for output transistor Q_{10}. A small amount of signal gain in the output circuit is made possible by the bootstrap connection from the emitter of output transistor Q_{10} to the emitter circuit of transistor Q_9. If this bootstrap connection were neglected, transistor Q_9 could be considered as merely a dc constant-current sink for drive transistor Q_7. Because of the bootstrap arrangement, however, the output circuit can provide a signal gain of 1.5 from the collector of differential-amplifier transistor Q_4 to the output (terminal 12). Although this small amount of gain may seem insignificant, it does increase the output-swing capabilities of the operational amplifiers.

The output from the operational-amplifier circuit is taken from the emitter of output transistor Q_{10} so that the dc level of the output signal is substantially lower than that of the differential-amplifier output at the collector of transistor Q_4. In this way, the output circuit shifts the dc level at the output so that it is effectively the same as that at the input when no signal is applied.

Resistor R_{15} in series with terminal 8 (refer to Fig. 1) increases the ac short-circuit load capability of the operational amplifier when this terminal is shorted to terminal 12 so that the resistor is connected between the output and the negative supply.

OPERATING CHARACTERISTICS

The operating characteristics of the CA3008 and CA3010 Integrated-Circuit Operational Amplifiers are identical. The characteristics data given in the following paragraphs, therefore, apply equally to each type. A proper evaluation of the capabilities of the operational amplifiers requires a thorough understanding of the parameters in terms of which the operating characteristics are expressed. For this reason, the special parameters for which additional clarification may be necessary are defined in an appendix at the end of this note.

DC CHARACTERISTICS

The operational amplifiers are designed to operate from two symmetrical dc power supplies at supply voltages in the range from ±3 volts to ±6 volts. For operation with ±3-volt supplies, the power dissipation in the amplifiers is less than 7.0 milliwatts with terminal 8 open or 23 milliwatts with terminal 8 shorted to terminal 12. When ±6-volt supplies are used, the dissipation level increases to either 30 milliwatts or 92 milliwatts, depending upon whether terminal 8 is open or shorted to terminal 12.

The input offset voltage for the operational amplifiers is typically 1.1 millivolts for all symmetrical supply voltages. This parameter is relatively insensitive to variations in the supply voltages. When ±6-volt supplies are used, the variation in the input offset voltage with fluctuations in supply voltage is typically less than 300 microvolts per volt for either supply. For ±3-volt supplies, the variation is typically 700 microvolts per volt. The offset voltage varies slightly with temperature as shown in Fig. 2. (Fig. 3

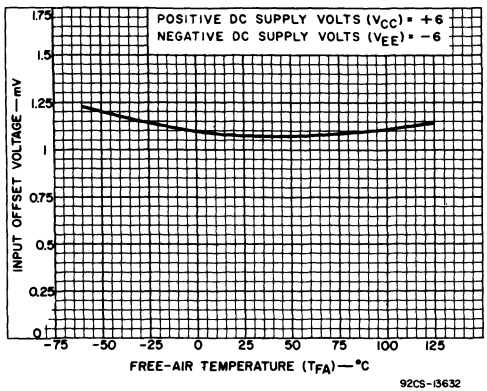
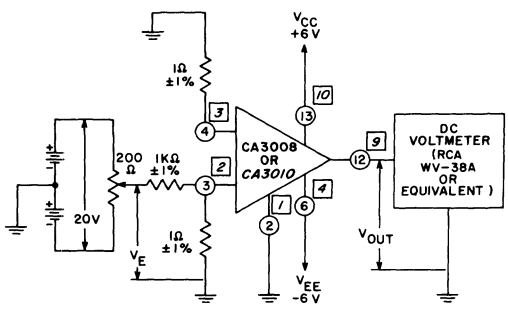


Fig. 2—Input offset voltage as a function of temperature.



NOTE: Pins 8 and 12 should be shorted for the pertinent power dissipation measurement ONLY!

Fig. 3—Test circuit used to measure the input offset voltage.

shows the schematic diagram of the special test circuit used for the offset-voltage measurements.)

The input bias current and the input offset current of the amplifiers are typically 5.3 microamperes and 0.54 microampere, respectively, when ±6-volt supplies are used. Figs. 4 and 5 show the variations in these parameters with temperature.

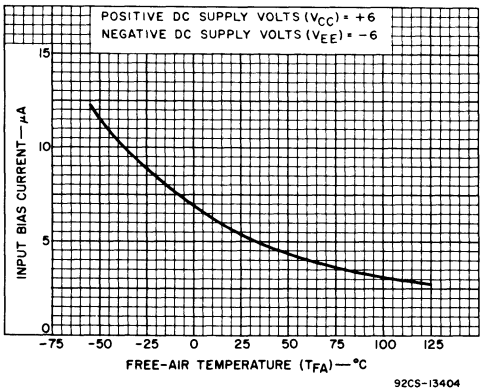


Fig. 4—Input bias current as a function of temperature.

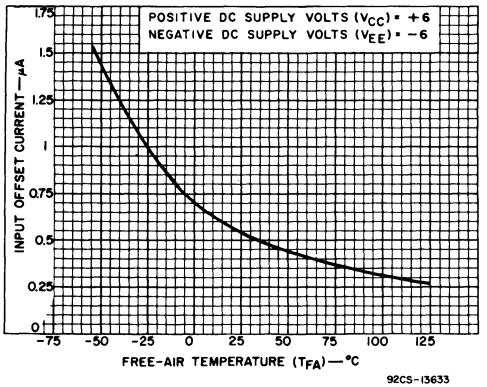


Fig. 5—Input offset current as a function of temperature.

AC CHARACTERISTICS

Gain-Frequency Response: The operational amplifiers provide a gain of 60 dB at low frequencies and have a unity-gain bandwidth of 18 MHz when operated from ±6-volt supplies. The typical gain-frequency response is shown in Fig. 6 for operation of the amplifier at −55°C, at +25°C, and at +125°C. The response of the amplifier exhibits little change over the temperature range. A typical gain-frequency characteristic for amplifiers operated from ±3-volt supplies at 25°C is shown in Fig. 7.

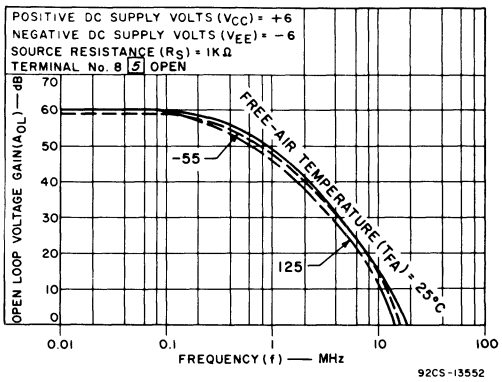


Fig. 6—Open-Loop gain as a function of frequency.

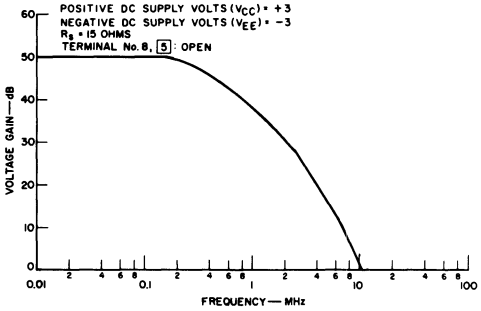


Fig. 7—Voltage gain as a function of frequency.

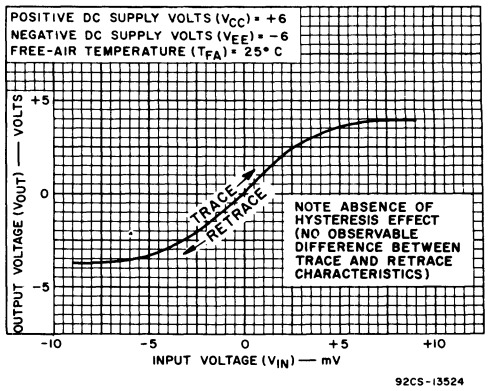


Fig. 8—Output voltage as a function of input voltage for an open-loop operational amplifier.

Transfer Characteristic: The transfer characteristic of the operational amplifiers is shown in Fig. 8. This characteristic shows that the amplifiers do not exhibit any hysteresis effect.

Common-Mode Rejection: The common-mode rejection provided by the operational amplifiers is typically 94 dB for operation with ±6-volt supplies. Fig. 9 shows the differential-gain and common-mode-gain frequency plots for the amplifiers. Fig. 10 shows the common-mode rejection as a function of frequency.

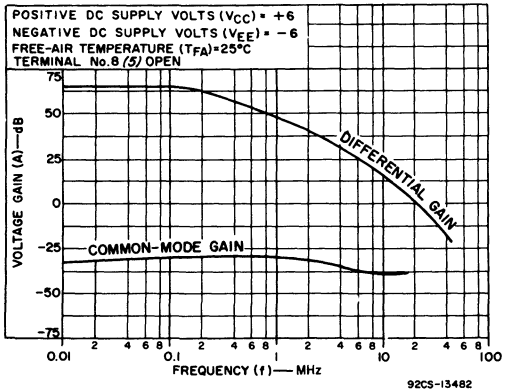


Fig. 9—Differential and common-mode gain as a function of frequency at different temperatures.

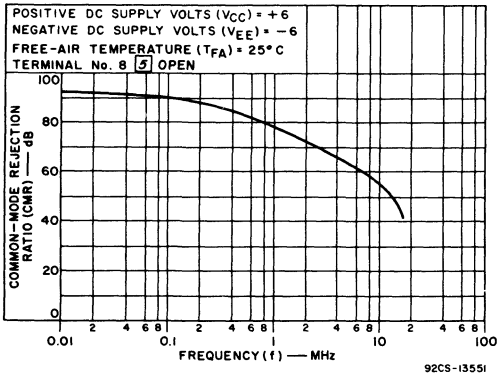


Fig. 10—Common-mode rejection as a function of frequency.

Output Swing: The operational amplifiers exhibit a maximum dynamic-swing capability of ±3.5 volts with terminal 8 open and of ±3.0 volts with terminal 8 shorted to terminal 12. The output-swing capability varies only slightly with temperature, as shown in Fig. 11. Fig. 12 shows the variation in the output-swing capability with frequency.

Input and Output Impedances: When the CA3008 or CA3010 Operational Amplifier is operated from ±6-volt supplies, it has an input impedance of 14,000 ohms at 1

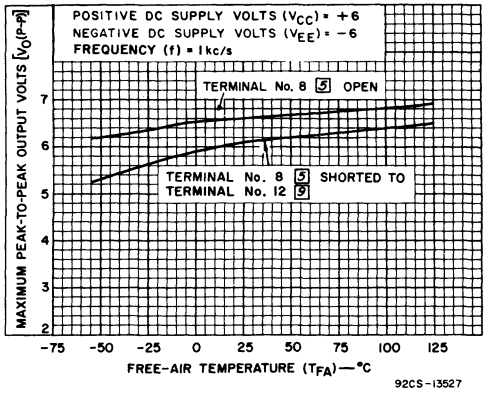


Fig. 11—Output-swing capabilities as a function of temperature.

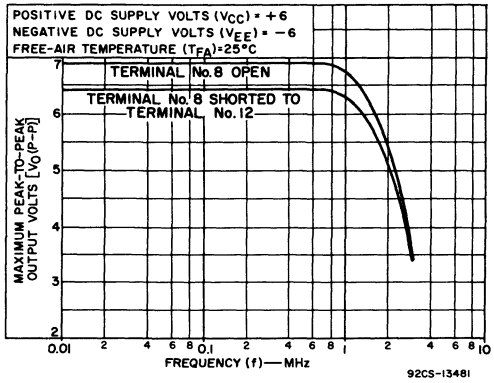


Fig. 12—Output-swing capabilities as a function of frequency.

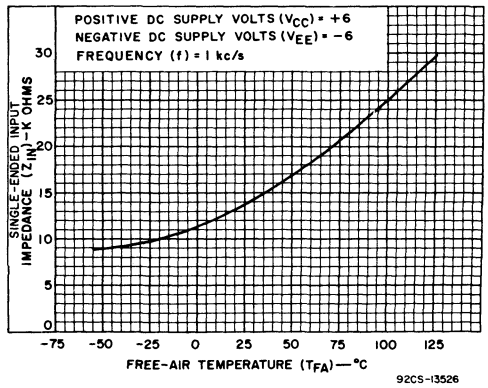


Fig. 13—Input impedance as a function of temperature.

kHz and an output impedance of 200 ohms (terminal 8 open) or 75 ohms (terminal 8 shorted to terminal 12). The input impedance and output impedance of the amplifier are affected by temperature as shown in Figs. 13 and 14, respectively.

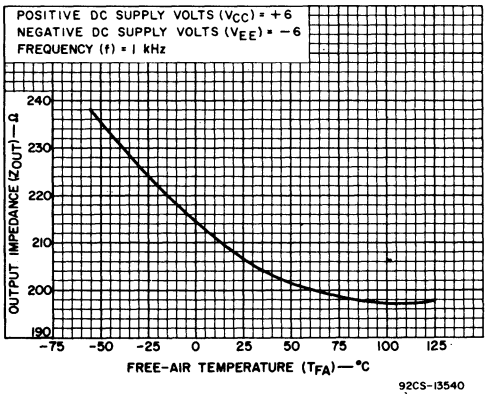
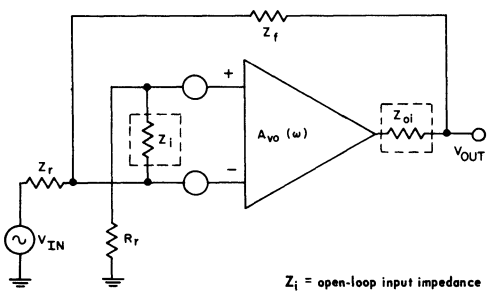


Fig. 14—Output impedance as a function of temperature.

CIRCUIT DESIGN CONSIDERATIONS

The basic design equations for the CA3008 or CA3010 Operational Amplifier in closed-loop circuits are summarized in Figs. 15 and 16. Fig. 15 shows the basic schematic diagram and gives the design equations for the generalized inverting feedback configuration, and Fig. 16 provides the diagram and the equations for the noninverting configuration. In both configurations, the inputs are returned to ground through dc paths that are effectively identical. This condition is necessary for minimum offset voltage (dc error).

Because the open-loop input capacitance of the operational amplifier is less than 10 picofarads, the frequency response is virtually independent of the drive source impedance. The input-impedance equations given in Figs. 15 and 16 indicate that this lack of dependence is even more pronounced when the amplifiers are operated with negative feedback.

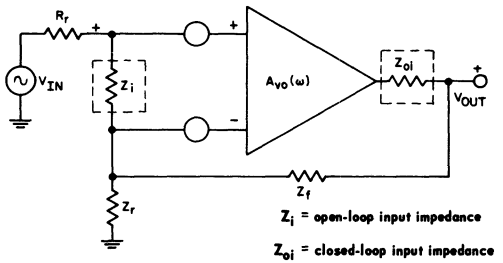


$$V_{out}/V_{in} = \frac{-Z_f}{Z_r + (Z_f + Z_r)/A_{Vo}(\omega)} \doteq -Z_f/Z_r$$

$$Z_{in} = Z_r + (Z_f/A_{Vo}(\omega)) // Z_i \doteq Z_r$$

$$Z_o = Z_{oi} \frac{(1 + V_{out}/V_{in})}{A_{Vo}(\omega)} \doteq 0$$

Fig. 15—Inverting-feedback configuration for an operational amplifier.



$$V_{out}/V_{in} = \frac{A_{Vo}(\omega)(Z_r + Z_f)}{Z_r + Z_f + Z_{vo} Z_r} \doteq 1 + Z_f/Z_r$$

$$Z_{in} = Z_i \left(1 + \frac{A_{Vo}(\omega)}{V_{out}/V_{in}}\right)$$

$$Z_o = Z_{oi} \left(\frac{V_{out}/V_{in}}{A_{Vo}(\omega)}\right)$$

Fig. 16—Noninverting-feedback configuration for an operational amplifier.

PHASE COMPENSATION

Basically, phase compensation is used to alter the response of an amplifier so that a phase shift of 180 degrees cannot occur at a frequency for which the loop gain is unity or greater. A rule of thumb that will guarantee an ac-stable amplifier is that at the intersection of the closed-loop response with the open-loop response, the respective slopes must have a difference less than 12 dB per octave.

With few exceptions (some of which will be covered in the section on applications), phase compensation must be accomplished by altering the open-loop response of the operational amplifier itself. One of the advantageous features of the CA3008 and CA3010 Operational Amplifiers is that small values of capacitance properly added to the amplifier circuit will provide the required phase compensation. When ±6-volt supplies are used, two phase-compensating networks, each of which consists of a 27-picofarad capacitor in series with a 2000-ohm resistor,

connected between terminals 1 and 14 and between terminals 9 and 10, cause the amplifier to roll-off at a slope of one (6 dB per octave) all the way to unity gain (where it then breaks into a slope of two). This value of compensation is sufficient to stabilize the amplifier for all resistive-feedback applications including unity gain. The response for this value of phase compensation is compared to the original open-loop response in Fig. 17. Although the two compensating networks are sufficient to ac stabilize the amplifier, they are not sufficient to produce a flat response (within ±1 dB) for closed-loop gains below 15 dB. Fig. 18 shows a plot of the capacitance required to produce

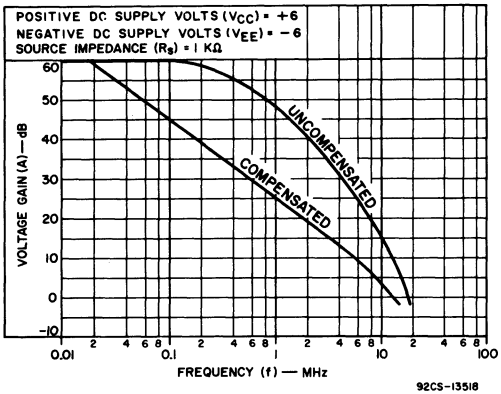


Fig. 17—Open-loop gain as a function of frequency for both phase-compensated and uncompensated operational amplifiers.

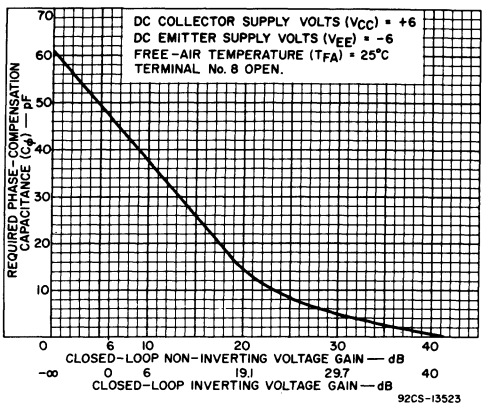


Fig. 18—Amount of phase-compensating capacitance required to obtain a flat (± 1-dB) gain response as a function of frequency.

a flat (±1-dB) gain response as a function of closed-loop gain. The capacitors must have a resistor in series with them so that $\frac{1}{2\pi RC} = 3$ MHz.

Phase compensation may also be effected conventionally by adding a capacitor in series with a resistor between terminal 11 and ground. A 0.02-microfarad capacitor in series with a 22-ohm resistor is sufficient to ac stabilize the CA3008 or CA3010 Operational Amplifier at resistive closed-loop gains down to unity.

The required phase compensation depends upon the feedback configuration and not upon the location of the drive source. Hence, phase-compensating networks that provide sufficient compensation for a 10-dB noninverting configuration also provide sufficient compensation for a 6-dB inverting configuration because the two feedback configurations are identical.

OUTPUT-POWER MODIFICATIONS

A choice of two output-power capabilities is provided in the CA3008 and CA3010 Operational Amplifiers. The output can be tailored to the specific load requirements by leaving terminal 8 open and placing an appropriate resistor between terminals 6 and 12. The minimum safe value of load resistance (including the aforementioned resistor) is 200 ohms when ±6-volt supplies are used. In determining the output capability, it should be kept in mind that the feedback network can contribute to the output loading especially in the lower-gain configurations.

APPLICATIONS OF THE OPERATIONAL AMPLIFIERS

The CA3008 and CA3010 Integrated-Circuit Operational Amplifiers can be adapted for use in a variety of diverse applications. For example, the amplifiers may be operated to provide the broad, flat gain-frequency response required for video amplifiers or the peaked responses required for various types of shaping amplifiers. Other applications of these amplifiers include comparators, integrators, differentiators, and summing amplifiers. The following paragraphs describe the circuit arrangements and the performance characteristics of the operational amplifiers in such applications:

VIDEO AMPLIFIERS

When the feedback is applied through a purely resistive network and suitable phase compensation is employed, flat gains are attainable from the operational amplifiers. Fig. 19 shows a 30-dB noninverting configuration of a video amplifier, together with the closed-loop response of the circuit. The phase compensation is provided by a 5-picofarad capacitor in series with a 10,000-ohm resistor. This arrangement provides the required amount of compensation, as predicted in Fig. 18. (For purposes of comparison, the uncompensated response of the 30-dB configuration is shown in Fig. 20. Observe the 13-dB peaking effect at 4.5 MHz.) An alternate method of phase compensation may be used when the intersection of the closed-loop characteristic and the open-loop response occurs in a two-slope region. The technique is to cause the feedback ratio

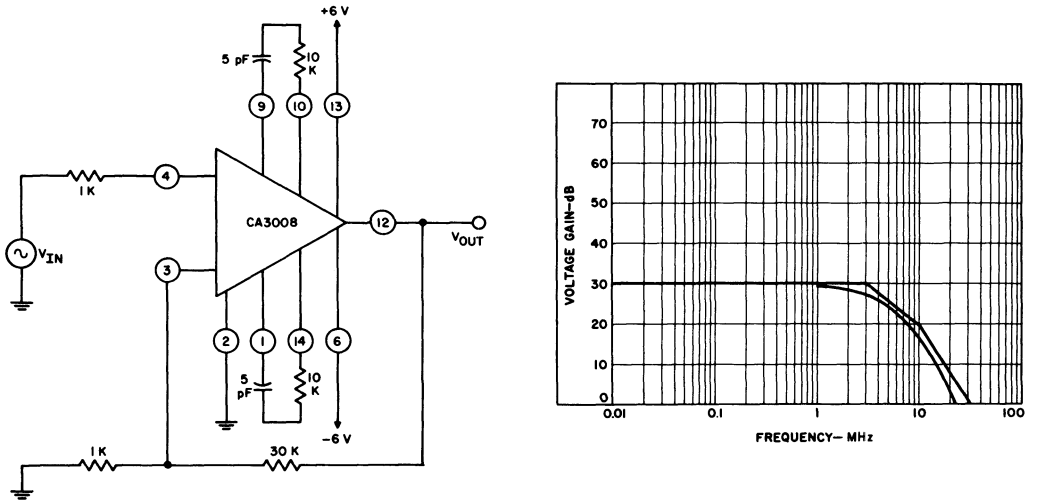


Fig. 19—Noninverting configuration and closed-loop response of an operational-amplifier type of video amplifier that provides a gain of 30-dB.

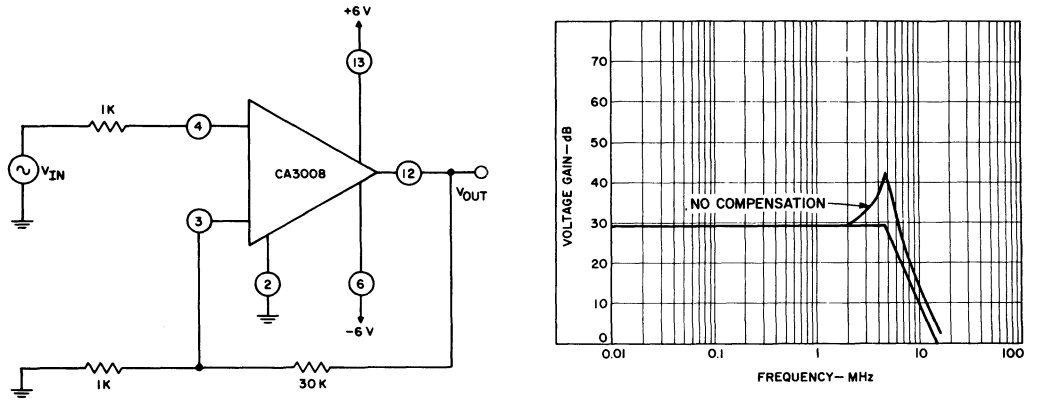


Fig. 20—Circuit diagram and gain-frequency response of the 30-dB noninverting video amplifier operated without phase compensation.

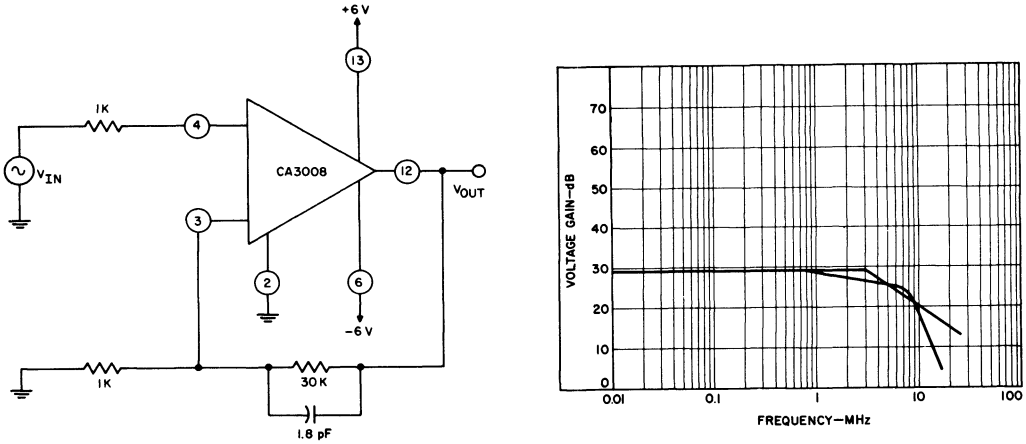


Fig. 21—Circuit diagram and gain-frequency response of the 30-dB video amplifier when the phase compensation is accomplished by the addition of a capacitor in parallel with the feedback resistor.

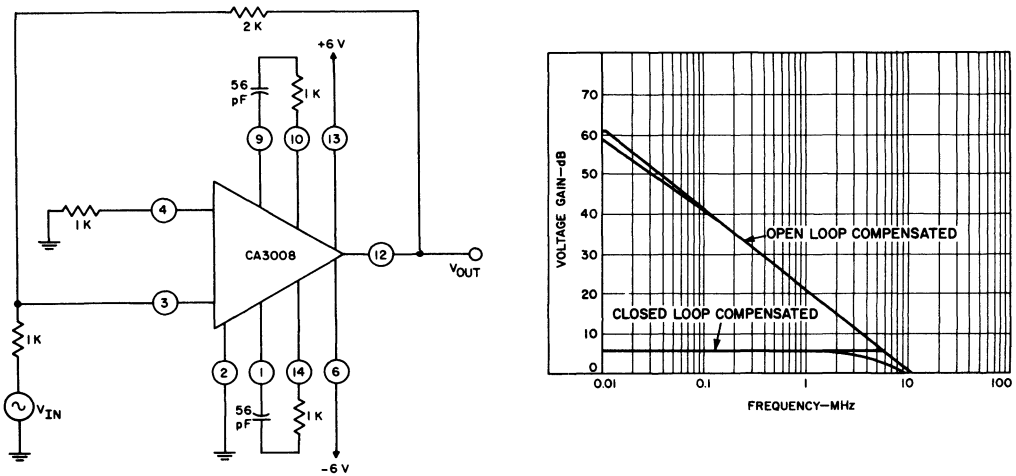
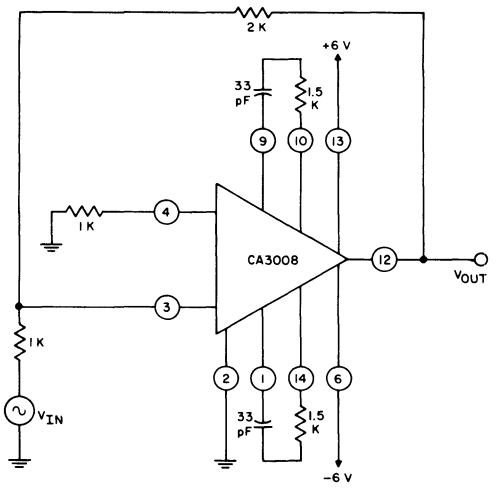


Fig. 22—Circuit diagram and response of an inverting type of operational amplifier used as a 6-dB video amplifier.



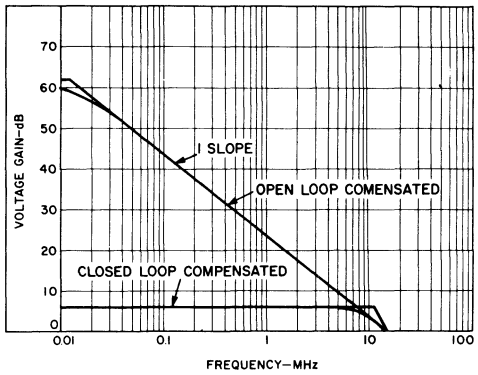


Fig. 23—Effect of a decrease in the phase-compensating capacitance from 56 picofarads to 33 picofarads on the response of the 6-dB video amplifier.

(Z_f/Z_r) to roll off at a one slope. Fig. 21 illustrates this alternate technique for the 30-dB gain circuit.

The low-frequency input impedance of the 30-dB noninverting configuration is 480,000 ohms, as calculated from the appropriate equation in Fig. 16 (Z_i = 14,000 ohms).

Fig. 22 shows the configuration and the response of a 6-dB inverting type of video amplifier. The intersection of the closed-loop characteristic with the compensated open-loop response predicts the 3-dB bandwidth of the video amplifier provided the transfer phase shift of the open-loop amplifier is approximately −90 degrees. This relationship suggests a way to extend the bandwidth without peaking. In the 6-dB video amplifier shown in Fig. 23, the 3-dB bandwidth has been increased from 5.6 MHz to 11 MHz by a decrease in the value of the phase-compensating capacitors from 56 picofarads to 33 picofarads.

Because a broadband amplifier should be capable of handling digital signals, data were taken to determine this capability. Figs. 24(a) and 24(b) illustrate the pulse-handling capabilities of the 30-dB noninverting circuit shown in Fig. 19. Fig. 24(a) shows the low-level (nonsaturating) pulse response. The input is a 38-millivolt, 960-nanosecond pulse; the output is a 1.1-volt pulse having a 40-nanosecond delay time, a zero storage time, and 125-nanosecond rise and fall times. Fig. 24(b) shows the response of the amplifier for a 960-nanosecond input pulse under 20-dB overdrive conditions. The output pulse has an amplitude of 3.2 volts, a delay time of 32 nanoseconds, a storage time of 160 nanoseconds, a rise time of 500 nanoseconds, and a fall time of 160 nanoseconds.

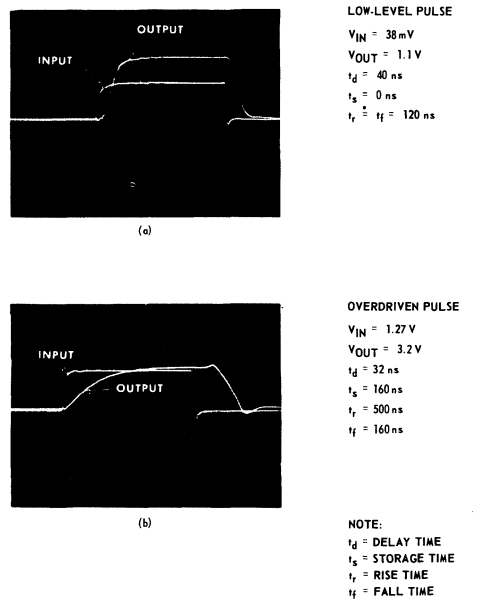


Fig. 24—Pulse-handling characteristics of the noninverting 30-dB video amplifier: (a) Low-level pulse response; (b) Pulse response under overdrive conditions.

FREQUENCY-SHAPING AMPLIFIERS

The operational amplifiers may be used to create simple frequency-shaped characteristics, such as those associated with band-pass, notched-response, and single-tuned narrow-band amplifiers.

Fig. 25 shows a noninverting amplifier that may be used to synthesize the following peaked-response transfer function:

$$\frac{V_{out}}{V_{in}} = +10\,\frac{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_4}\right)}{\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

where $f_1 = 10$ kc/s, $f_2 = 40$ kc/s, $f_3 = 200$ kc/s, and $f_4 = 800$ kc/s.

In terms of the notations employed in Fig. 25, the break-frequency equations for the amplifier may be expressed as follows:

$$\frac{10}{2\pi C_r(R_f + 10R_r)} = 10\text{ kHz}$$

$$\frac{1}{2\pi C_r R_r} = 40\text{ kHz}$$

$$\frac{1}{2\pi C_n(R_n + R_f)} = 200\text{ kHz}$$

$$\frac{40}{2\pi C_n(40R_n + R_f)} = 800\text{ kHz}$$

These break-frequency equations are the precise equations derived from the gain equation in Fig. 16. The amount of phase compensation required is that shown in Fig. 18 for a noninverting gain of 20 dB.

Fig. 26 shows the circuit configuration and the frequency response of a narrow-band, 100-kHz tuned amplifier. The circuit Q is 33.3. A true single-tuned response can be obtained from only an inverting circuit configuration, as shown by the gain equation for the two types of configurations given in Figs. 15 and 16 and repeated below:

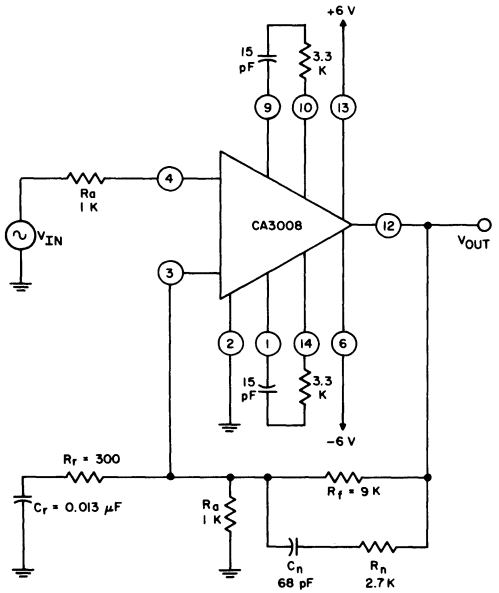
1. For the inverting configuration, the gain equation is given as:

$$\frac{V_{out}}{V_{in}} = -Z_f/Z_r$$

2. For the noninverting configuration, the following gain equation is used:

$$\frac{V_{out}}{V_{in}} = 1 + Z_f/Z_r$$

The "1+" term in the gain expression for the noninverting configuration indicates that the gain of this type of circuit will never decrease to zero as required for a true single-tuned response. The amount of phase compensation required for the narrow-band 100-kHz amplifier is the value given in Fig. 18 for an inverting gain of 0.0 (infinite attenuation).



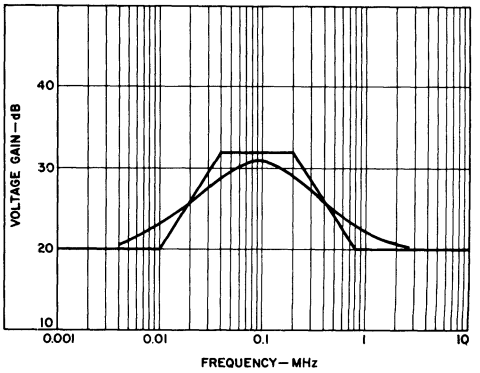
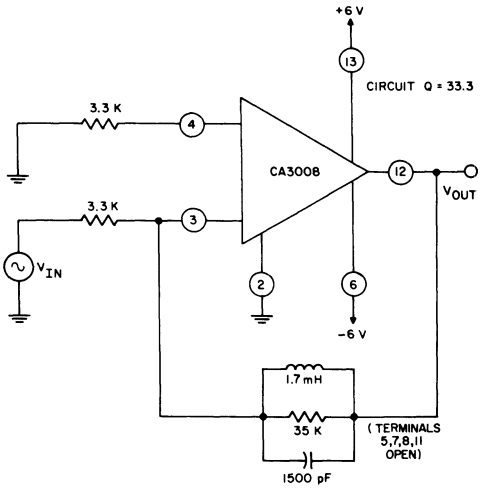
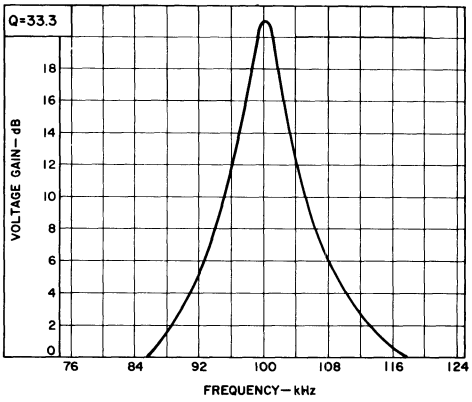


Fig. 25—Circuit diagram and response of a noninverting type of operational amplifier used to synthesize peaked-response transfer functions.





Phase Compensation not shown. It is 62 pF in series with 820 Ω between terminals 1 and 14 and between terminals 9 and 10.

Fig. 26—Circuit diagram and response of an inverting type operational amplifier used as a narrow-band 100-kc/s tuned amplifier.

COMPARATOR CIRCUITS

The CA3008 and CA3010 Operational Amplifiers have excellent transfer characteristics for comparator applications. As shown in Fig. 8, the amplifiers have no observable hysteresis effect; the trace (minus to plus) and retrace (plus to minus) excursions coincide.

INTEGRATORS

The important design consideration when an operational amplifier is to be used as an integrator is that dc feedback be provided. This feedback is necessary so that an offset (error) voltage cannot continuously charge the feedback capacitor until the amplifier limits. The required dc feedback is normally provided by shunting the integrating capacitor with a resistor so that the resulting time constant is considerably longer than the periods for the frequencies of interest. Fig. 27 shows the circuit configuration for the use of the CA3008 or CA3010 Operational Amplifier as an integrator and the responses of the circuit for 1-kHz square-wave inputs. The dc gain of the circuit is limited to 20 dB by the 39,000-ohm feedback resistor. The effect of this resistor on the gain, however, becomes negligible for ac signals at frequencies above 13 Hz because of the 0.03-microfarad capacitor in parallel with it. The weighting factor of integration for the circuit is about 1 millisecond (R = 39,000 ohms; C = 0.03 microfarad).

Phase compensation must also be provided in an integrating amplifier circuit to assure ac stability. In general, the amount of compensation required is the maximum value given by Fig. 18, because the closed-loop characteristic of the integrator has rolled off completely at the frequency where the intersection of the open-loop response and the closed-loop characteristic occurs.

DIFFERENTIATORS

The main problem in the design of differentiating amplifiers is that the gain of such amplifiers increases with frequency; hence, they are susceptible to high-frequency noise. The classical remedy for this effect is to connect a small resistor in series with the input capacitor so that the high-frequency gain is decreased. Actually, the addition of the resistor results in a more realistic model of a differentiator because a resistance is always added in series with the input capacitor by the source impedance. The schematic diagram of a CA3008 or CA3010 Operational Amplifier used as a differentiating circuit and the response of the circuit for 1-kHz square waves are shown in Fig. 28. A value of 51 ohms is selected for the gain-limiting resistor to illustrate that the effect of the source impedance is not necessarily negligible in differentiator applications. This 51-ohm resistor limits the high-frequency numerical gain factor of the amplifier to 433.

If the closed-loop gain of a differentiator rises to the open-loop value before the open-loop response has started to roll off, no phase compensation of the circuit is required. In order to assure that the intersection of the closed-loop characteristic with the open-loop response occurs at a slope less than two, the RC time constant of the phase-compensating network must be adjusted so that the open-loop response does not roll off in the region of the intersection.

SCALING ADDERS

The inverting feedback configuration of the CA3008 and CA3010 Operational Amplifiers lends itself not only to summing several different signals, but also to weighting

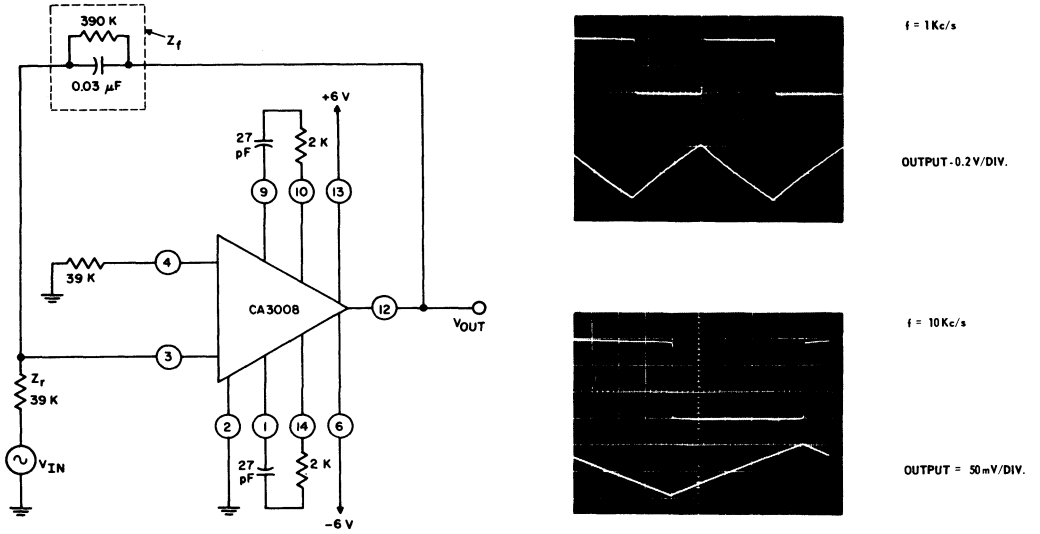


Fig. 27—Circuit diagram and the input and output waveforms for an operational amplifier used as an integrator.

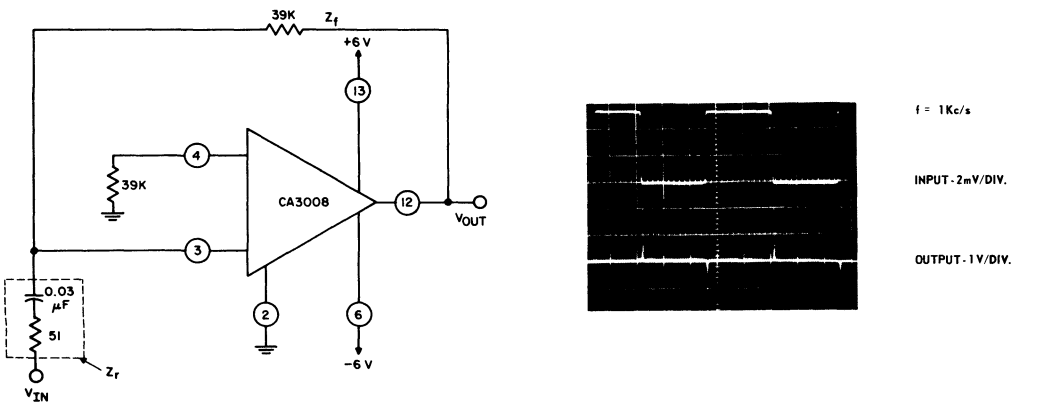
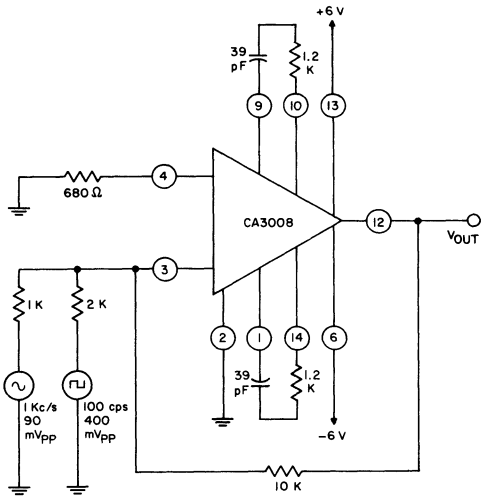


Fig. 28—Circuit diagram and the input and output waveforms for an operational amplifier used as a differentiator.

each signal to be summed. The weighting operation is possible because the virtual ground that exists at the junction of the feedback resistor and the inverting input (terminal 3) isolates each signal channel from the others. The weighting operation requires that each input signal enters the virtual-ground node through an impedance of such value that its ratio to the feedback impedance is equal to the desired weighting factor.

Fig. 29 illustrates the use of the CA3008 or CA3010 Operational Amplifier as a scaling adder (weighting amplifier). This figure also shows a photograph of the output waveform. The minimum phase compensation needed for this circuit is that required for the gain obtained when a single signal drives all the input channels in parallel.



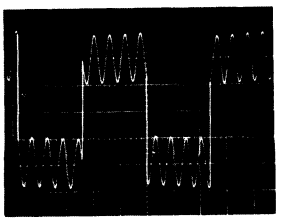


Fig. 29—Circuit diagram and output waveform obtained when an operational amplifier is used as a scaling adder.

EXTERNAL MODIFICATIONS OF THE OPERATIONAL AMPLIFIERS

Although the CA3008 and CA3010 units meet all the requirements of an operational amplifier, there are special applications for which certain modifications are desirable. The two most common examples are applications in which the operational amplifier is required to supply high levels of output power and those for which the amplifier is operated with low dc input bias current.

ADDITION OF A POWER-OUTPUT STAGE

The output-power capability of the operational amplifiers can be increased by the addition of an external emitter-follower output stage or a class B push-pull output stage. The emitter-follower approach is highly inefficient from a dissipation standpoint. A class B push-pull output stage, added as shown in Fig. 30, works well in a closed-loop circuit, but is subject to thermal runaway under open-loop conditions. The thermal-runaway effect may be controlled by the introduction of a small amount of emitter degeneration in each of the push-pull transistors. The load requirements, however, are sometimes severe enough to preclude the use of emitter degeneration. Moreover, depending on the choice of complementary transistors, the addition of the push-pull amplifier may limit the over-all bandwidth.

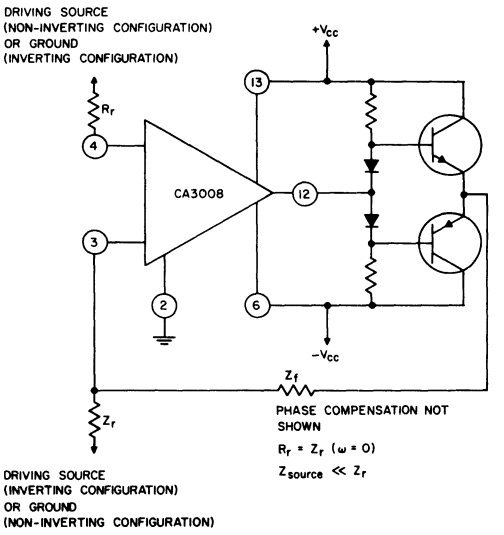


Fig. 30—Schematic diagram showing the addition of an external push-pull output stage to increase the output capability of an operational amplifier.

ADDITION OF INPUT EMITTER FOLLOWERS

The dc input bias current of the operational amplifiers is required to be low when the amplifiers are driven either from a high-impedance source, such as a vidicon tube, or from a drive source that cannot accommodate high levels of dc current. The input bias current required is substantially decreased when emitter followers are added to the input terminals of the operational amplifiers. An emitter-follower modification to the operational amplifiers is illustrated in Fig. 31. The use of the emitter followers reduces the input-bias-current requirements from 5 microamperes per input to 0.14 microampere per input. This modification, however, also results in a decrease in the bandwidth, as indicated by the response curve for the modified circuit (see Fig. 31). The bandwidth is decreased because the emitter followers operate at very low levels of collector current and are driven from a high-impedance source (1 megohm for the circuit shown in Fig. 31).

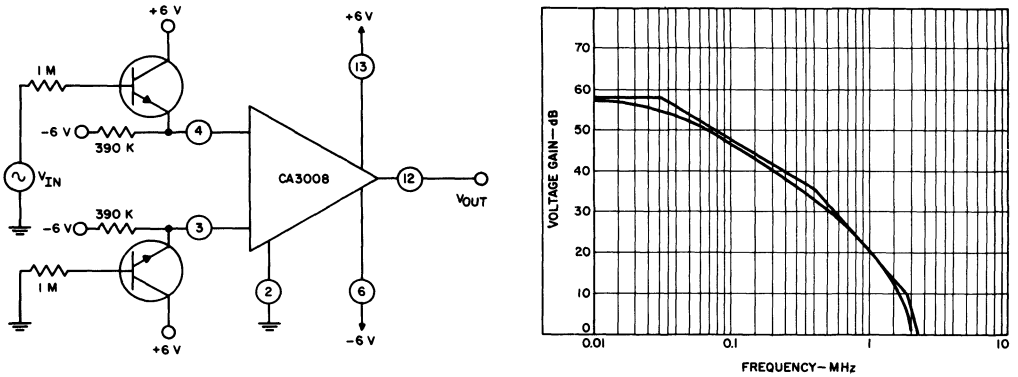


Fig. 31—Schematic diagram showing the addition of input emitter followers to reduce the input-bias-current requirements of an operational amplifier.

Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers

BY

T. C. CAMPBELL

The RCA integrated-circuit operational amplifiers CA3015 and CA3016 are identical in circuit configuration to the previously announced types CA3008 and CA3010, but have an improved device breakdown voltage that permits operation from ±12-volt supplies. Operation of the CA3015 and CA3016 from power supplies of ±6 volts or ±3 volts is the same as for the earlier types.[1] This Note describes the operating characteristics of the CA3015 and CA3016 at ±12 volts, and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages.

OPERATING CHARACTERISTICS

Fig. 1 shows the schematic diagrams and terminal numbers for the CA3015 and CA3016. As in the case of the CA3008 and CA3010, each operational amplifier consists basically of two differential amplifiers and a single-ended output circuit in cascade. The CA3015 is supplied in a 12-lead TO-5 package, and the CA3016 in a 14-lead flat package. Throughout this Note, terminal numbers for the CA3015 are shown in the illustrations; however, the discussion applies to both packages.

DC Characteristics

When operated from ±12-volt power supplies, these operational amplifiers have a typical dissipation of 175 milliwatts with terminal 5 of the CA3015 or terminal 8 of the CA3016 open. If terminals 5 and 9 of the CA3015 or terminals 8 and 12 of the CA3016 are shorted, higher output-current capability can be achieved, but the dissipation increases to a typical value of 500 milliwatts. The input offset voltage is typically 1.4 millivolts, and the variation in input offset voltage is typically less than 200 microvolts per volt for fluctuations of either supply voltage. At 25°C, the input bias current and input offset current are typically 9.6 and 1 microamperes, respectively. (Curves of input offset voltage, input bias current, and input offset current as functions of temperature are given in the technical bulletin for the CA3015 and CA3016.)

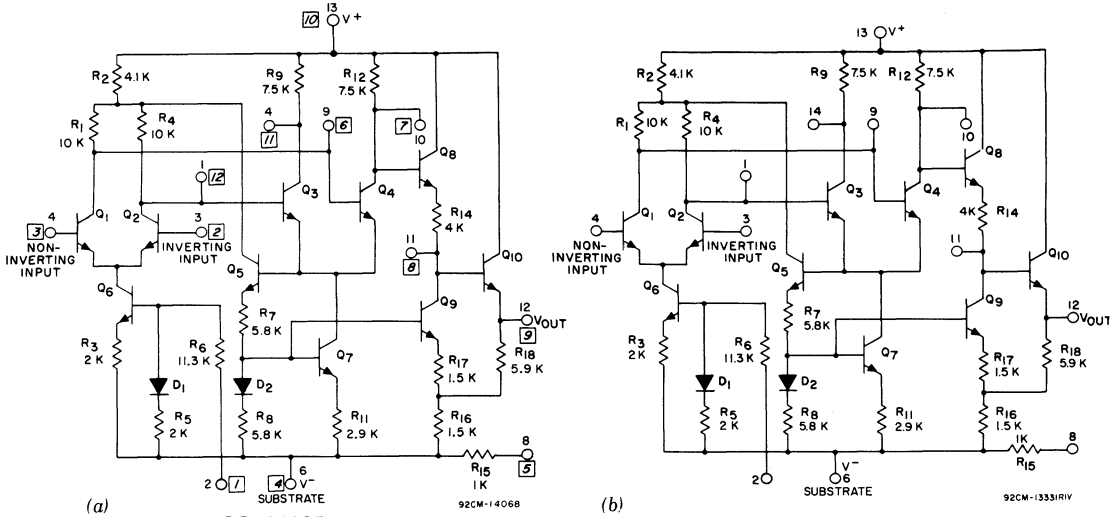


Fig.1 - Schematic diagrams and terminal connections for the (a) CA3015 and (b) CA3016 integrated-circuit operational amplifiers.

Derating. When these operational amplifiers are operated from ± 12-volt supplies with terminals 5 and 9 of the CA3015 or terminals 8 and 12 of the CA3016 shorted for greater output capability, the power dissipation is high enough so that temperature derating is necessary. The maximum junction-temperature rating is 150°C, and the thermal resistance is 100°C per watt. The maximum power-dissipation rating is 600 milliwatts at 25°C (with terminals shorted as described above). In this higher-output mode, the circuits can operate safely at ambient temperatures up to 90°C.

AC Characteristics

Transfer Characteristic. The open-loop transfer characteristic is shown in Fig.2. As in the case of the CA3008 and CA3010, there is no hysteresis effect. The CA3015 and CA3016 technical bulletin includes curves of maximum peak-to-peak voltages as functions of load resistance with terminal 5 of the CA3015 or terminal 8 of the CA3016 open and with terminals 5 and 9 of the CA3015 or terminals 8 and 12 of the CA3016 shorted. The CA3015 and CA3016 can drive a lower-resistance load when these terminals are shorted.

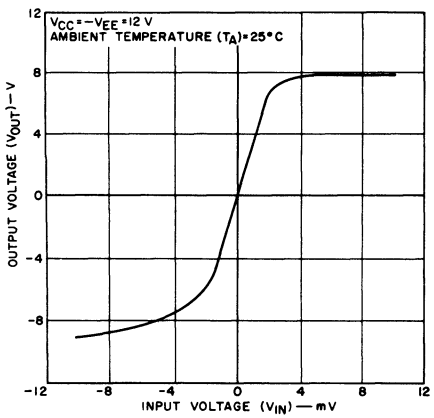


Fig.2 - Open-loop transfer characteristic.

Gain vs Frequency Response. The open-loop low-frequency gain of the CA3015 and CA3016 with ±12-volt supplies is typically 70 dB with a 3-dB bandwidth of 320 kHz. The unity-gain crossover occurs at a frequency of 58 MHz.

Common-Mode Rejection. The common-mode rejection ratio of the CA3015 and CA3016 is typically 104 dB for operation with ±12-volt supplies. A curve of common-mode rejection ratio as a function of frequency is included in the bulletin.

Input and Output Impedances. The technical bulletin for the CA3015 and CA3016 includes curves of input and output impedances as functions of temperature. At 25°C, the typical input impedance is 7800 ohms. The typical output impedance is 92 ohms with terminal 5 of the CA3015 or terminal 8 of the CA3016 open, and 76 ohms with these terminals connected to the output.

PHASE COMPENSATION

The following section describes phase-lag and phase-lead compensation techniques for these operational amplifiers. Fig.3 shows the various phase-compensation connections for the CA3015.

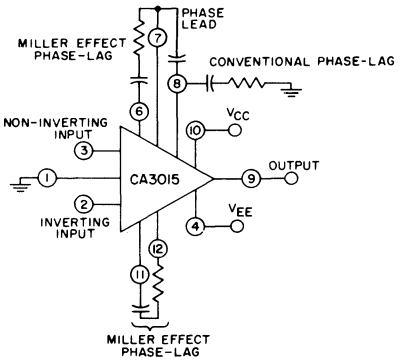


Fig.3 - Terminal connections for phase-lag and phase-lead compensation of the CA3015.

Phase-Lag Compensation

When the CA3015 and CA3016 are operated from ±6-volt supplies, the phase-compensation techniques described previously for the CA3008 and CA3010 are applicable.[1] When the CA3015 and CA3016 are operated from ±12-volt supplies, corrections must be made in the phase-lag compensation to allow for the shift in frequency at which the second break in the open-loop Bode plot occurs. At ±12 volts, this second break occurs at a frequency of 10 MHz. For Miller-effect and conventional phase-lag compensation, the series RC combinations must be adjusted so that $1/(2\pi RC) = 10$ MHz to correct for the shift in frequency. In addition, the Miller technique requires a larger value of phase-lag capacitance for a non-peaking (±1 dB) response to allow for the higher gain.

Fig.4 shows a curve of the required phase-lag capacitance as a function of gain, together with the corresponding response curves. (The required capacitance values shown in this figure are applicable not only for ±12-volt power supplies, but also for all lower-voltage symmetrical supplies; however, smaller capacitors could be used at lower voltages.)

Fig.5 shows curves of open-loop compensated and uncompensated frequency response with ±12-volt supplies. Although the phase-lag compensation capacitance of 18 picofarads shown in curve (B) of this figure is sufficient to provide stability in resistive-feedback amplifiers down to unity gain, it is not sufficient to provide flat closed-loop response (±1 dB) below 20 dB.

Phase-Lead Compensation

In addition to the standard phase-lag compensation discussed above, the CA3015 and CA3016 have a

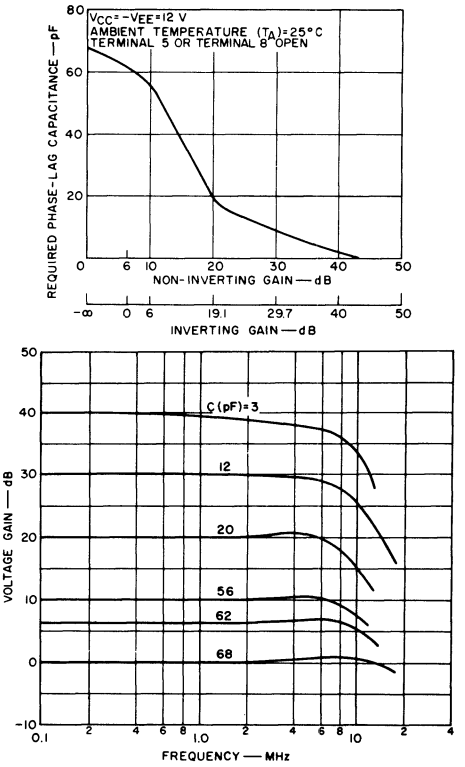


Fig.4 - Amount of phase-lag capacitance required to obtain a flat (±1 dB) response, and typical response characteristics.

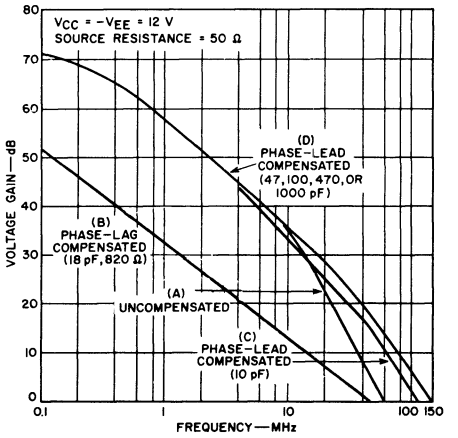


Fig.5 - Open-loop gain as a function of frequency for compensated and uncompensated amplifiers.

phase-lead compensation capability. For this phase-lead compensation, a capacitor is connected between terminals 7 and 8 of the CA3015, as shown in Fig.3, or between terminals 10 and 11 of the CA3016. The effect of this capacitor is to eliminate the break at 10 MHz in the Bode plot and thus extend the 6-dB-per-octave roll-off. The second break in the Bode plot then occurs at approximately 35 MHz, and the unity-gain crossover occurs at 150 MHz. The phase-lead compensated open-loop response is shown in curves (C) and (D) of Fig.5 for various values of capacitance. For optimum performance, a minimum phase-lead capacitance of 47 picofarads is recommended.

For flat (±1 dB) responses at closed-loop gains below 30 dB, a small amount of phase-lag compensation is required in addition to the phase-lead compensation. The required phase-lag capacitance for flat (±1 dB) responses and the corresponding response curves are shown in Fig.6. When phase-lead compensation is used, the series RC combinations should be adjusted so that $1/(2\pi RC) = 35$ MHz.

The phase-lead compensation is also applicable when ±6-volt power supplies are used, and provides a unity-gain crossover improvement of about one octave as compared to the uncompensated connection. As mentioned earlier, the phase-lag capacitance requirement for ±12-volt supplies shown in Fig.4 is satisfactory for ±6-volt supplies, although smaller capacitors could be used with the lower voltages.

APPLICATIONS

For all applications, ac and dc balance at the input must be preserved, i.e., the two inputs must be returned to ground through equal impedances.

50-dB Amplifier

Fig.7 shows the circuit configuration and frequency response for a non-inverting, 50-dB amplifier employing phase-lead compensation. This amplifier

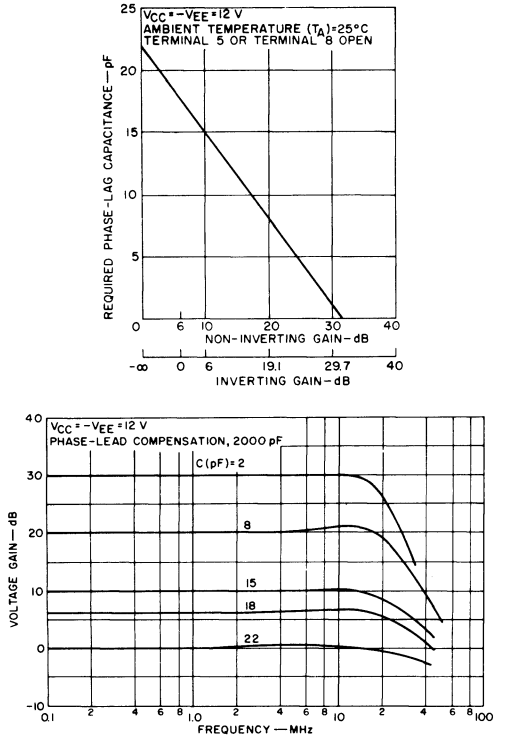


Fig.6 - Amount of phase-lag capacitance required to obtain a flat (±1 dB) response when phase-lead compensation is used, and typical response characteristics.

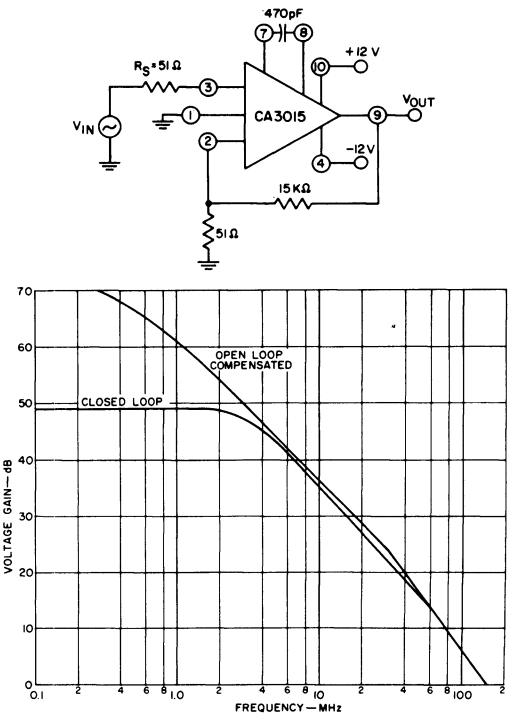
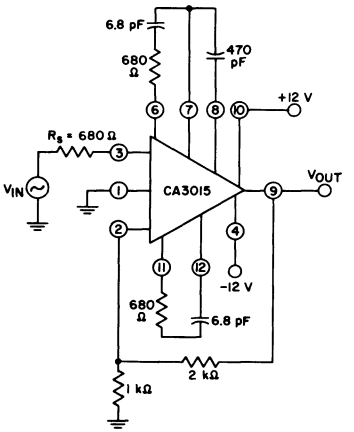


Fig.7 - Circuit diagram and response curve for a 50-dB, non-inverting amplifier with phase-lead compensation.

has a 3-dB bandwidth of 3.5 MHz, and a unity-gain crossover at 150 MHz.

10-dB, 42-MHz Amplifier

Fig.8 shows the circuit diagram and frequency response for a 10-dB, non-inverting amplifier employing both phase-lead and phase-lag compensation. Slight peaking (2 dB) occurs for the phase compensation shown. Flat response with bandwidth reduction to 25 MHz may be obtained by use of a phase-lag capacitance of 15 picofarads.



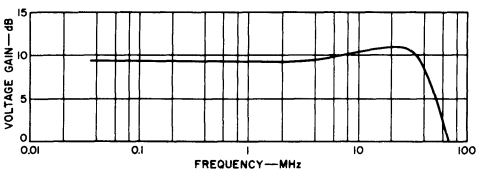
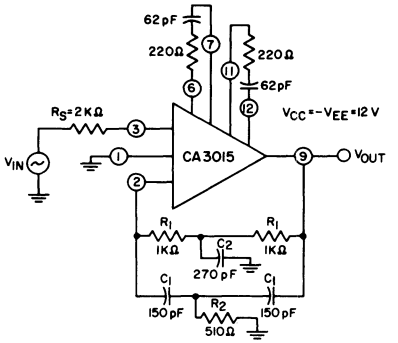


Fig.8 - Circuit diagram and response curve for a 10-dB, non-inverting amplifier with phase-lead and phase-lag compensation.

Twin-T Bandpass Amplifier

Fig.9 shows the circuit diagram and frequency response of a bandpass amplifier using a twin-T network in the feedback loop. The difference in resonant frequency between the bandpass-amplifier response and the twin-T network response is caused by device capacitances and loading effects. The unloaded Q (Q_O) of the twin-T network is 14.4; the Q_O of the bandpass amplifier is 12.8.



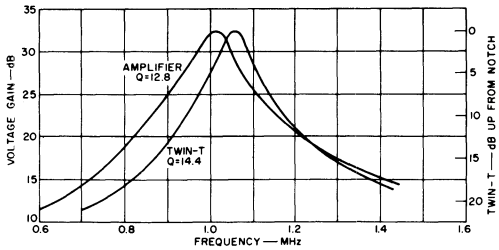


Fig.9 - Circuit diagram and response curves for a bandpass amplifier using a twin-T network.

The symmetrical twin-T network can be designed by use of the following equations:

$$R_1 = 2\,R_2$$

$$C_1 = \tfrac{1}{2}\,C_2$$

$$f_o = 1/(2\pi R_1 C_1)$$

It is important in the design of this type of bandpass amplifier that the two inputs be returned to ground through equal resistances; in this case a value of 2000 ohms is used.

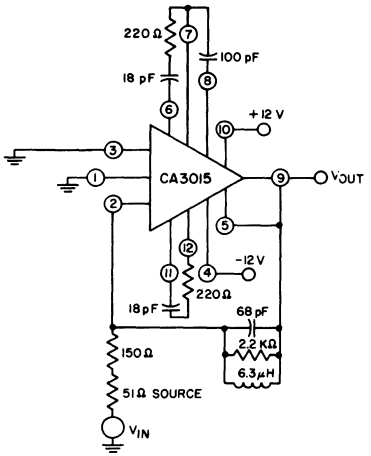
20-dB, 10-MHz Bandpass Amplifier

Fig.10 shows the circuit diagram and frequency response of an RLC bandpass amplifier. This amplifier is designed to have a Q_O of about 10 ($R_P = X_C Q_O$ = 2200 ohms) and a gain of about 20 dB at resonance (2200/200 = 11, or 20.9 dB). In this application, the inputs are effectively grounded.

Voltage Follower

A voltage follower is a non-inverting, unity-gain amplifier used primarily to transform from a high impedance to a low impedance. Because low voltages

are usually associated with high-impedance sources, the voltage follower need not have a great voltage capability.



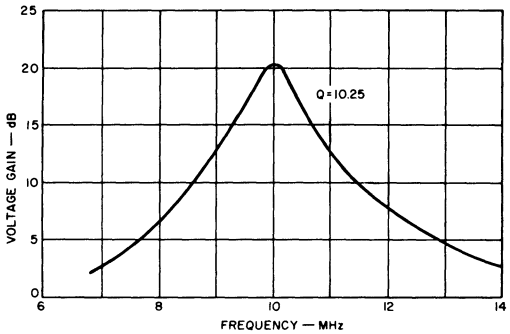


Fig.10 - Circuit diagram and response curve for a 10-MHz RLC bandpass amplifier.

Fig.11 shows the circuit diagram for a voltage follower using the CA3015, together with a curve of maximum undistorted output voltage as a function of load resistance. When terminals 5 and 9 are shorted (or terminals 8 and 12 of the CA3016), the voltage follower is capable of transforming a 3.4-volt peak-to-peak voltage from a 100,000-ohm source to a 470-ohm load.

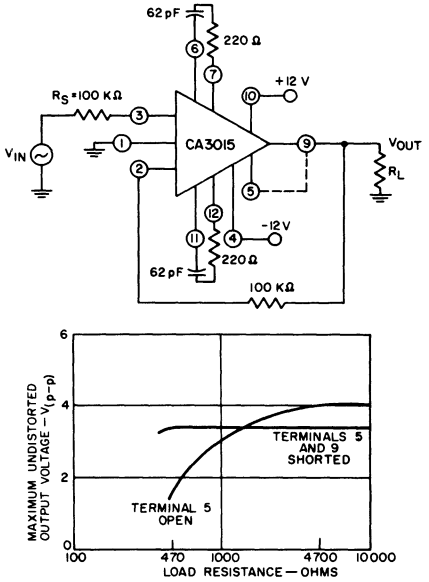


Fig.11 - Circuit diagram for a voltage follower driven from a 100,000-ohm source, and curve showing maximum undistorted output voltage as a function of load resistance.

If higher voltage-swing capability is desired, the positive supply voltage (V_{CC}) may be increased. Temperature derating may be necessary, depending on the magnitude of V_{CC} and whether the high- or low-current mode is used.

REFERENCE

1. "Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers", RCA Integrated Circuits Application Note ICAN-5015, November 1965.

Integrated-Circuit Operational Amplifiers

An operational amplifier is basically a very-high-gain direct-coupled amplifier which uses feedback for control of response characteristics. This circuit can be used to synthesize a broad variety of intricate transfer functions and thus can be adapted for use in many widely diverse applications. The operational amplifier is principally used to perform various mathematical functions, such as differentiation, integration, analog comparisons, and summation. This versatile circuit, however, may also be used for numerous other applications that have significantly different transfer and response requirements. For example, the same operational amplifier may be adapted to provide either the broad, flat frequency-gain response required of video amplifiers or the peaked responses required of various types of shaping amplifiers.

GENERAL CONSIDERATIONS

The configuration most commonly used for operational amplifiers is a cascade of two differential-amplifier circuits together with an appropriate output stage. The cascaded differential-amplifier stages not only fulfill the operational-amplifier requirement for a high-gain direct-coupled amplifier circuit, but also provide significant advantages with respect to application.

From an applications standpoint, an operational amplifier that has a differential input is much more versatile than a single-input type. This increased versatility results from greater flexibility in selection of the feedback configuration. With a single-input operational amplifier, only an inverting feedback configuration can be employed. When differential inputs are used, the feedback configuration may be either an inverting type or a noninverting type, which depends on the common-mode rejection for its negative feedback. The type of feedback affects the characteristics of an operational amplifier, and the two types tend to complement each other. Because the characteristics of each type are required equally often, the differential-input operational amplifier is twice as versatile as the single-input type.

The differential-input operational amplifier is readily adapted to integrated-circuit construction techniques because the stable dc-amplifier configuration lends itself well to the monolithic diffusion process used in the fabrication of silicon integrated circuits. In addition, symmetrical differential-amplifier stages can be dc-cascaded readily, provided that each stage is driven push-pull by the preceding stage. The common-mode effects that result from this arrangement make possible stable, direct-coupled cascaded.

The capabilities and limitations of operational amplifiers are firmly defined by a few very simple equations and rules, which are based on a certain set of criteria that an operational amplifier must meet. Effective use of these simple relationships, however, requires knowledge of the conditions under which each is applicable so that errors that may result from various approximations are held to a minimum. This Note explores the theory of the design and use of operational amplifiers, and develops each pertinent design equation in a general way. Evaluations are then made to determine the assumptions that must be made (or the criteria the operational amplifier must meet) to reduce these general equations to classical operational-amplifier design equations.

Frequency instabilities in the operational amplifier and the methods used to prevent them are also discussed. A thorough understanding of the principles of frequency stability is imperative to the successful application of operational amplifiers. The basic concepts and techniques involved in phase compensation (frequency stabilization) are explained in terms of (1) basic frequency-stability requirements, (2) the problems that may result from an uncontrolled frequency response, and (3) the techniques that may be used to correct these undesirable effects.

Finally, the basic criteria for an operational amplifier are given. This discussion is placed last because a basic insight to the theory of application is required before the effects of many of the operational-amplifier requirements can be fully appreciated.

BASIC THEORY OF OPERATIONAL AMPLIFIERS

In the development of the basic equations and concepts associated with the use of operational amplifiers, the precise formulations for the transfer functions, the input impedances, the output impedances, and the loop gains are presented for both the inverting and the noninverting feedback configurations, and classical design equations are then derived from these precise formulations. The effects of the load impedance and of common-mode gain (or common-mode rejection) on the inverting and noninverting feedback configurations are considered separately.

Inverting Feedback Configuration

An operational amplifier operated with an inverting feedback configuration is shown in Fig.1. The load resistor R_L is assumed to be large enough so that its effect on the transfer characteristic is negligible, i.e., $I_{OUT} = 0$. (The effects of a finite R_L are investigated and evaluated subsequently in the discussion of the equivalent-circuit model of an operational amplifier.)

Certain differential-input operational amplifiers require a significant flow of bias current at each input. For this condition, the dc paths to ground for each input must be equal so that a minimum dc offset voltage (error) is developed at the output. Thus, for the terminology employed in Fig.1, R_r must equal the parallel combination of $Z_r(\omega = 0)$ with the series combination of $Z_f(\omega = 0)$ and $Z_{oi}(\omega = 0)$.

In the circuit of Fig.1, the drive-source impedance affects the feedback in the inverting configuration and, therefore, must be considered part of the Z_r term. For

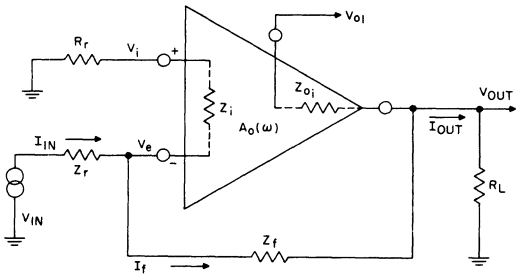


Fig.1 - Inverting-feedback operational-amplifier configuration.

brevity, the symbol Z_r is defined to include the source impedance as well as certain feedback design elements. The impedances Z_i and Z_{oi} are the open-loop *intrinsic* input and output impedances of the operational amplifier. Ordinarily, these impedances are assumed in the amplifier symbol. In Fig.1, however, they are identified to emphasize their importance in the ensuing equations. The term $A_o(\omega)$ is the open-loop differential voltage gain of the operational amplifier; this parameter is frequency-dependent. The terminals on the operational-amplifier symbol labled minus (−) and plus (+) refer to the inverting and noninverting input, respectively.

Inverting-Configuration Transfer Function – The transfer function or closed-loop gain of an operational amplifier is generally considered to express the relationship between the input and output voltages. (It is relatively simple to convert the voltage transfer function to another desired transfer relationship.) In the derivation of the transfer function for the schematic in Fig.1, the following differential-amplifier relationship is used as the starting point:

$$V_{o1} = -A_o(\omega)\,(V_e - V_i) \qquad (1)$$

where V_e and V_i are defined as follows:

$$V_e = \frac{V_{IN}\,(Z_f+Z_{oi})/\!/(Z_i+R_r)}{Z_r + (Z_f+Z_{oi})/\!/(Z_i+R_r)} + \frac{V_{o1}\,Z_r/\!/(Z_i+R_r)}{Z_f + Z_{oi} + Z_r/\!/(Z_i+R_r)} \qquad (2)$$

and

$$V_i = V_e\,R_r/(Z_i + R_r) \qquad (3)$$

(In these and subsequent equations, the load resistor R_L is assumed to approach infinity.)

If the expressions for V_e and V_i given by Eqs. (2) and (3) are substituted in Eq. (1), the resulting expression can be simplified as follows:

$$V_{o1} = \frac{-A_o(\omega)\, Z_i\, (Z_f+Z_{oi})\, V_{IN}}{(Z_f+Z_{oi})\,(Z_i+R_r)+Z_r\,(Z_f+Z_{oi}+Z_i+R_r)+A_o(\omega)Z_i\,Z_r} \quad (4)$$

The output voltage V_{OUT} is expressed in terms of V_{o1} and V_{IN} by the following equation:

$$V_{OUT} = \frac{V_{o1}\,[Z_f + Z_r /\!\!/ (Z_i + R_r)]}{Z_{oi} + Z_f + Z_r /\!\!/ (Z_i + R_r)} + \frac{V_{IN}\, Z_{oi}\, (Z_f + Z_{oi}) /\!\!/ (Z_i + R_r)}{(Z_f + Z_{oi})\,[Z_r + (Z_f + Z_{oi}) /\!\!/ (Z_i + R_r)]} \quad (5)$$

With V_{o1} defined as indicated by Eq. (4), the accurate equation for the transfer response (for $R_L \to \infty$) becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{oi}\,(Z_i+R_r) - A_o(\omega)\, Z_i\, Z_f}{(Z_f+Z_{oi})(Z_i+R_r)+Z_r(Z_f+Z_{oi}+Z_i+R_r)+A_o(\omega)Z_iZ_r} \quad (6)$$

If Z_i is assumed to be much greater than the combination of Z_r in parallel with $Z_f + Z_{oi}$, and if Z_{oi} is assumed to be much smaller than Z_f, then the closed-loop gain (or transfer function) may be expressed as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{-A_o(\omega)\, Z_f}{Z_f + Z_r + A_o(\omega)\, Z_r} \quad (7)$$

In addition, if the open-loop gain $A_o(\omega)$ is the dominant term in either Eq. (6) or (7), the transfer-function equation for the inverting configuration simplifies to the following familiar expression:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega) \to \infty} -\frac{Z_f}{Z_r} \quad (8)$$

Eq. (8) is considered to be the classical or ideal expression for the closed-loop gain (transfer function) for an operational amplifier that uses the inverting type of feedback configuration.

The difference between the open-loop gain and the closed-loop gain is in itself an important design parameter. This "gain throwaway", which is known as the loop gain L.G., is defined by the following equation:

$$\text{L. G.} = \frac{\text{open-loop gain, } A_o(\omega)}{\text{closed-loop gain, } \dfrac{V_{OUT}}{V_{IN}}} \quad (9)$$

When the transfer function is given by Eq. (7), the loop-gain equation may be written as follows:

$$\text{L. G.} = -\frac{Z_f + Z_r}{Z_f} - \frac{A_o(\omega)}{\dfrac{Z_f}{Z_r}} \quad (10)$$

Moreover, when the open-loop gain is very large, the inverting loop gain can be considered to be the open-loop gain divided by the *ideal* inverting closed-loop gain. The equation for L.G. then becomes

$$\text{L. G.} \doteq \frac{-A_o(\omega)}{\dfrac{Z_f}{Z_r}} \quad (11)$$

The loop-gain parameter can be used to predict the accuracy of the approximate operational-amplifier relationships. In general, the higher the loop gain, the more accurate the results provided by the approximate (or classical) relationships. This correlation is demonstrated in Table I, which compares values of V_{OUT}/V_{IN} obtained from the precise transfer expression, Eq. (6),

Table I – Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Inverting Configuration)

Conditions: $A_o(\omega) = 1000\ \angle 0°$, $Z_i = 15{,}000\ \angle 0°$, $Z_{o_i} = 200\ \angle 0°$, $Z_r = 1000\ \angle 0°$.

$Z_f\ \angle 0°$ (ohms)	V_{OUT}/V_{IN} (dB)	V_{OUT}/V_{IN} from Eq. (6) (dB)	Error (dB)	L.G. (dB)
200,000	46.0	44.3	1.70	14.0
100,000	40.0	39.1	0.90	20.0
30,000	29.6	29.3	0.30	30.4
10,000	20.0	19.9	0.10	40.0
2,000	6.03	6.0	0.03	54.0

with values obtained from the classical approximation, Eq.(8), for various gain settings. The tabular data show that the classical equation is accurate to within 1 dB provided the loop gain is at least 20 dB. Eq. (11) was used to calculate all of the loop-gain values given in the table.

Inverting-Configuration Input Impedance, Z_{IN} – The input impedance Z_{IN} for the inverting-feedback configuration of an operational amplifier, shown in Fig.1, can be expressed as follows:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}}. \quad (12)$$

where

$$I_{IN} = \frac{V_{IN} - V_e}{Z_r} \quad (13)$$

Therefore,

$$Z_{IN} = \frac{Z_r}{1 - \dfrac{V_e}{V_{IN}}} \quad (14)$$

The ratio V_e/V_{IN} may be determined by substituting the expression for V_{o1} given by Eq. (4) into Eq. (2) and dividing through by V_{IN} (with $R_L \rightarrow \infty$.) The resultant equation is then simplified to obtain the following relationship:

$$\frac{V_e}{V_{IN}} = \frac{(Z_f+Z_{oi})\,(Z_i+R_r)}{Z_r\,(Z_f+Z_{oi}+Z_i+R_r)+(Z_f+Z_{oi})\,(Z_i+R_r)+A_o(\omega)Z_i\,Z_r} \quad (15)$$

If this expression for V_e/V_{IN} is substituted into Eq.(14), the result can be simplified to obtain the following precise expression for the closed-loop input impedance:

$$Z_{IN} = Z_r + \frac{Z_r\,(Z_{oi}\,Z_i + Z_{oi}\,R_r + Z_f R_r + Z_f\,Z_i)}{Z_r\,(Z_f+Z_{oi}+Z_i) + R_r\,(Z_r+Z_{oi}) + A_o(\omega)Z_i\,Z_r} \quad (16)$$

If $A_o(\omega)$ is dominant and Z_{o_i} is small, Eq. (16) reduces to

$$Z_{IN} \doteq Z_r + \frac{Z_f\,(Z_i+R_r)}{A_o(\omega)\,Z_i} \quad (17)$$

A further simplification is possible when R_r is much smaller than Z_i, which is a common condition. In this case, the equation for the input impedance becomes

$$Z_{IN} \doteq Z_r + \frac{Z_f}{A_o(\omega)} \quad (18)$$

Eqs. (17) and (18), which are important in voltage-summing or scaling-adder* applications, can be used to predict the degree of interaction among multiple inputs.

When $A_o(\omega)$ is large enough, Eqs. (17) and (18) may be rewritten as follows:

$$Z_{IN} \xrightarrow{A_o(\omega)\rightarrow\infty} Z_r \quad (19)$$

Eq. (19) is the "classical" equation for the input impedance of an operational amplifier when an inverting-feedback configuration is used. This equation, together with Eq. (16), implies the existence of a condition known as a virtual ground at the node-assigned voltage V_e (shown in Fig.1). That is, the node is at ground potential even though there is no electrical connection between this point and ground. [This statement can be verified either intuitively by the use of Eq. (19) or directly if $A_o(\omega)$ is assumed to be infinite in Eq.(15).] Moreover, no current flows into the negative terminal of the amplifier when the open-loop gain is infinite because the voltage V_e is zero while the impedance at the negative terminal (i.e., $Z_i + R_r$) is not zero. The concept of a virtual ground leads to an extremely simple three-step analysis procedure for an inverting operational-amplifier configuration.

1. Because of the virtual ground ($V_e = 0$), the input current I_{IN} and feedback current I_f can be defined as follows:

$$I_{IN} = \frac{V_{IN}}{Z_r} \quad (20)$$

$$I_f = \frac{-V_{OUT}}{Z_f} \quad (21)$$

2. Zero current flow into the inverting terminal ($V_e = 0$) indicates the following relationships:

$$I_{IN} = I_f \quad (22)$$

$$\frac{V_{IN}}{Z_r} = \frac{-V_{OUT}}{Z_f} \quad (23)$$

3. Eq. (23) can then be rewritten to obtain the classical gain equation, as follows:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_f}{Z_r} \quad (24)$$

Although the foregoing analysis is certainly an idealized one, it is nevertheless practical because the required approximations are usually valid. Eq. (15) serves as a measure of the deviation from a true virtual ground.

Inverting-Configuration Output Impedance, Z_{OUT} – The closed-loop output impedance is the ratio of the unloaded output voltage V_{OUT} to the short-circuit output current I_{OUT} as follows:

$$Z_{OUT} = \frac{V_{OUT}\,(R_L \rightarrow \infty)}{I_{OUT}\,(R_L \rightarrow 0)} \quad (25)$$

It is apparent from Fig.1 then that the output current I_{OUT} is given by

$$I_{OUT}\,(R_L \rightarrow 0) = \frac{-A_o(\omega)\,(V_e - V_i)}{Z_{oi}} \quad (26)$$

If the expression given by Eq. (3) is substituted for V_i, Eq. (26) can be rewritten as follows:

$$I_{OUT}\,(R_L \rightarrow 0) = \frac{-A_o(\omega)\,Z_i\,V_e}{Z_{oi}\,(Z_i+R_r)} \quad (27)$$

Under short-circuit conditions ($R_L = 0$), the voltage V_e in terms of V_{IN} is given by

$$V_e = \frac{V_{IN}\,Z_f /\!\!/ (Z_i+R_r)}{Z_r + Z_f /\!\!/ (Z_i+R_r)} = \frac{V_{IN}\,Z_f\,(Z_i+R_r)}{Z_r\,(Z_f+Z_i+R_r) + Z_f\,(Z_i+R_r)} \quad (28)$$

*A scaling adder is an inverting operational-amplifier configuration which weights and sums multiple voltages.

Therefore, I_{OUT} (at $R_L = 0$) can be expressed in terms of V_{IN} as follows:

$$I_{OUT} = \frac{-A_o(\omega)\, Z_i\, Z_f\, V_{IN}}{Z_{o_i}\,[Z_r\,(Z_f+Z_i+R_r) + Z_f\,(Z_i+R_r)]} \quad (29)$$

If this expression for I_{OUT} is substituted in Eq. (25) and consideration is given to the intransience of V_{IN} in going from an unloaded to a fully loaded condition, the equation for Z_{OUT} becomes

$$Z_{OUT} = \frac{Z_{o_i}\,[Z_r\,(Z_f+Z_i+R_r) + Z_f\,(Z_i+R_r)]}{-A_o\,(\omega)\, Z_i\, Z_f} \left(\frac{V_{OUT}}{V_{IN}}\right) \quad (30)$$

Finally, the desired equation for the closed-loop output impedance is obtained if the expression for V_{OUT}/V_{IN} given by Eq. (6) is substituted into Eq. (30), as follows:

$$Z_{OUT} = \frac{Z_{o_i}[Z_r(Z_f+Z_i+R_r)+Z_f(Z_i+R_r)]}{A_o(\omega)Z_iZ_f[Z_r(Z_f+Z_{o_i}+Z_i+R_r)+(Z_f+Z_{o_i})(Z_i+R_r)+A_o(\omega)Z_iZ_r]} \cdot \frac{[A_o(\omega)Z_iZ_f-Z_{o_i}(Z_i+R_r)]}{} \quad (31)$$

If the open-loop gain term $A_o(\omega)$ is dominant, Eq. (31) simplifies to

$$Z_{OUT} \doteq \frac{Z_{o_i}\,[Z_r\,(Z_f + Z_i + R_r) + Z_f\,(Z_i + R_r)]}{A_o(\omega)\, Z_i\, Z_r} \quad (32)$$

This expression for Z_{OUT} does not simplify to its "classical" equation unless Z_i is dominant also; in this case, Eq. (32) becomes

$$Z_{OUT} \doteq Z_{o_i}\,\frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)} \quad (33)$$

The assumption that Z_i is a dominant term is not always valid, especially if bipolar transistor inputs are employed. Eq. (32), therefore, may be considered to take precedence over Eq. (33).

Noninverting Feedback Configuration

Fig.2 shows the general circuit for an operational amplifier operated with a noninverting feedback configuration. In this section, the equations for the transfer function and the closed-loop input impedance for this type of operational-amplifier circuit are derived. These derivations, as did those for the inverting circuit, assume that the load resistor R_L is large enough so that its effect is negligible, i.e., $R_L \to \infty$ and $I_{OUT} = 0$. (The effects of a finite load resistance on the noninverting operational amplifier are evaluated in the discussion of the equivalent-circuit model of an operational amplifier.)

A noninverting operational amplifier, unlike the inverting type, requires a differential-input arrangement because it uses the common-mode effect in its feedback

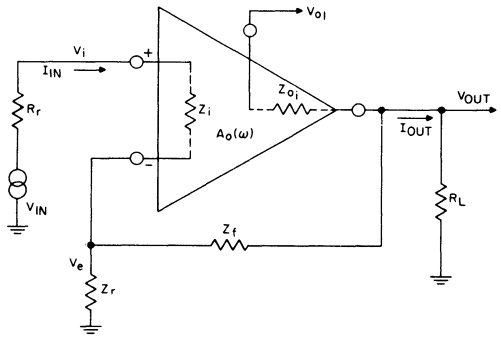


Fig.2 - Noninverting-feedback operational-amplifier configuration.

scheme. The following basic requirements and definitions that apply to the inverting circuit shown in Fig.1 are also valid for the general noninverting circuit of Fig.2:

1. The dc return paths to ground for the two inputs must be equal and finite for amplifiers that require a significant amount of input bias current.
2. The input and output impedances, Z_i and Z_{o_i}, are inherent in the basic amplifier unit and are shown on the diagram to emphasize their importance in the relationships to be derived.
3. The open-loop gain is frequency-dependent and is represented by the symbol $A_o(\omega)$.
4. The plus and minus labels on the input terminals designate the noninverting and inverting terminals, respectively.

In the noninverting circuit, however, the source impedance is included in the passive element R_r rather than the frequency-dependent parameter Z_r, as in the inverting circuit.

Noninverting-Configuration Transfer Function – As with the inverting circuit, the transfer function developed for the noninverting operational amplifier shows the relationship between the input and output voltages. It is relatively simple to convert this relationship to another type of transfer function.

When the load resistor R_L approaches infinity, the

output voltage V_{OUT} for the general circuit shown in Fig.2 can be expressed as follows:

$$V_{OUT} = \frac{V_{o1}\,[Z_f+Z_r/\!/(Z_i+R_r)]}{Z_{oi}+Z_f+Z_r/\!/(Z_i+R_r)} + \frac{V_{IN}\,Z_{oi}\,[Z_r/\!/(Z_f+Z_{oi})]}{(Z_f+Z_{oi})\,[Z_i+R_r+Z_r/\!/(Z_f+Z_{oi})]} \quad (34)$$

Eq. (34) may be rewritten in the following form:

$$V_{OUT} = \frac{V_{o1}\,[Z_f\,(Z_r+Z_i+R_r) + Z_r\,(Z_i+R_r)] + Z_r\,Z_{oi}\,V_{IN}}{(Z_i+R_r)\,(Z_r+Z_f+Z_{oi}) + Z_r\,(Z_f+Z_{oi})} \quad (35)$$

The voltage V_{o1} is defined by the differential-gain expression, as follows:

$$V_{o1} = A_o(\omega)\,(V_i - V_e) \quad (36)$$

where V_i is the source voltage V_{IN} less the voltage drop across R_r, as given by

$$V_i = V_{IN} - I_{IN}\,R_r \quad (37)$$

where

$$I_{IN} = \frac{V_i - V_e}{Z_i} \quad (38)$$

The voltage V_i, given by Eq. (37), can now be expressed in terms of the voltages V_{IN} and V_e, as follows:

$$V_i = \frac{Z_i\,V_{IN} + R_r\,V_e}{Z_i + R_r} \quad (39)$$

It can be determined from Fig.2 that, when R_L approaches infinity, the voltage V_e is given by the following equation:

$$V_e = \frac{V_{o1}\,Z_r/\!/(Z_i+R_r)}{Z_{oi}+Z_f+Z_r/\!/(Z_i+R_r)} + \frac{V_{IN}\,Z_r/\!/(Z_f+Z_{oi})}{Z_i+R_r+Z_r/\!/(Z_f+Z_{oi})} \quad (40)$$

If the relationships for V_{o1} and V_i given by Eqs. (36) and (39), respectively, are used, V_e can be expressed solely in terms of V_{IN}, as shown by the following equation:

$$V_e = \frac{(Z_r\,Z_f + Z_r\,Z_{oi} + A_o(\omega)\,Z_i\,Z_r)\,V_{IN}}{(Z_i+R_r)\,(Z_r+Z_f+Z_{oi}) + Z_r\,(Z_f+Z_{oi}) + A_o(\omega)\,Z_i\,Z_r} \quad (41)$$

Eqs. (36), (39), and (41) are now used to express V_{o1} in terms of V_{IN}, as follows:

$$V_{o1} = \frac{A_o(\omega)\,Z_i\,(Z_r+Z_f+Z_{oi})\,V_{IN}}{(Z_i+R_r)\,(Z_r+Z_f+Z_{oi}) + Z_r\,(Z_f+Z_{oi}) + A_o(\omega)\,Z_i\,Z_r} \quad (42)$$

If this expression for V_{o1} is substituted into Eq. (35), the new equation that results can be simplified and divided through by V_{IN} to obtain the desired transfer function, as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_r\,Z_{oi} + A_o(\omega)\,Z_i\,(Z_r+Z_f)}{(Z_i+R_r)\,(Z_r+Z_f+Z_{oi}) + Z_r\,(Z_f+Z_{oi}) + A_o(\omega)\,Z_i\,Z_r} \quad (43)$$

The transfer function that is usually associated with the noninverting feedback configuration of an operational amplifier can be derived from Eq. (43) if the impedance Z_{oi} is assumed to be zero and the impedance Z_i is assumed to be very high. When these assumptions are made, Eq. (43) becomes

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{(Z_r+Z_f)\,A_o(\omega)}{(Z_r+Z_f) + Z_r\,A_o(\omega)} \quad (44)$$

Eq. (44) may be rewritten as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + Z_f/Z_r}} \quad (45)$$

If the term $A_o(\omega)$ is dominant in Eq. (45), the following "classical" expression for the noninverting transfer response results:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega) \to \infty} 1 + \frac{Z_f}{Z_r} \quad (46)$$

The term $1 + Z_f/Z_r$ represents the closed-loop gain for the *ideal* noninverting configuration. This term, which is referred to as the *ideal feedback characteristic,* is basic to operational-amplifier frequency-stabilization theory.

As might be expected, the loop gain of an operational amplifier is defined in the same way [by Eq. (9)] regardless of the type of feedback configuration. Under the conditions for which Eq. (45) is a valid expression for the transfer response, the loop gain for the noninverting configuration is given by

$$\text{L. G.} = 1 + \frac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}} \quad (47)$$

If the second term of Eq. (47) is very large, this equation reduces to

$$\text{L. G.} \doteq \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \tag{48}$$

Table II compares the values calculated from the precise and the approximate expressions [Eqs. (43) and (46), respectively] for the closed-loop gain of the noninverting operational-amplifier configuration. The approximate formula is accurate to within 1 dB provided

Table II – Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Noninverting Configuration)

Conditions: $A_o(\omega) = 1000 \angle 0°$, $Z_i = 15{,}000 \angle 0°$, $Z_{o_i} = 200 \angle 0°$, $Z_r = 1000 \angle 0°$

$Z_f \angle 0°$ (ohms)	V_{OUT}/V_{IN} from Eq. (46) (dB)	V_{OUT}/V_{IN} from Eq. (43) (dB)	Error (dB)	L. G. from Eq. (48) (dB)
199,000	46.0	44.3	1.70	14.0
99,000	40.0	39.1	0.90	20.0
29,000	29.6	29.3	0.30	30.4
9,000	20.0	19.9	0.10	40.0
1,000	6.03	6.0	0.03	54.0

the loop gain is 20 dB or more. A comparison of Tables I and II shows that the error introduced by the use of the classical gain formula for the noninverting configuration [Eq. (46)] is identical to that introduced by the use of the classical gain formula for the inverting configuration [Eq. (8)].

Noninverting-Configuration Input Impedance, Z_{IN} – The following equation gives the basic definition of the input impedance Z_{IN}:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{49}$$

It can be readily determined from Fig.2 that the input current I_{IN} is given by

$$I_{IN} = \frac{V_{IN} - V_e}{Z_i + R_r} \tag{50}$$

When this relationship is applied in Eq. (49), the expression for the noninverting input impedance becomes

$$Z_{IN} = \frac{Z_i + R_r}{1 - \frac{V_e}{V_{IN}}} \tag{51}$$

If the expression for the ratio of V_e/V_{IN}, given previously by Eq. (41), is substituted into Eq. (51), the result can be simplified to obtain the following precise expression for the input impedance (for $R_L \to \infty$):

$$Z_{IN} = Z_i + R_r + Z_r \frac{Z_f + Z_{o_i} + A_o(\omega)\, Z_i}{Z_r + Z_f + Z_{o_i}} \tag{52}$$

For the case where Z_i is dominant and Z_{oi} is small, Eq. (52) reduces to

$$Z_{IN} \doteq Z_i + \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{53}$$

The following expression for the input impedance results if $A_o(\omega)$ is also considered dominant:

$$Z_{IN} \doteq \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{54}$$

Eq. (54) states that the noninverting input impedance is equal to the intrinsic input impedance Z_i multiplied by the loop gain.

Noninverting-Configuration Output Impedance, Z_{OUT}- As in the inverting configuration, the closed-loop output impedance for the noninverting configuration is defined as the ratio of the open-circuit output voltage, V_{OUT}, to the short-circuit output current, I_{OUT}, as follows:

$$Z_{OUT} = \frac{V_{OUT}\ (R_L \to \infty)}{I_{OUT}\ (R_L \to 0)} \tag{55}$$

where

$$I_{OUT}\ (R_L \to 0) = \frac{A_o(\omega)\ (V_i - V_e)}{Z_{o_i}} \tag{56}$$

For the general noninverting operational-amplifier configuration, the voltages V_i and V_e are given by the following equations for the conditions indicated:

$$V_i\ (R_L \to 0) = \frac{V_{IN}\ (Z_i + Z_r /\!\!/ Z_f)}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{57}$$

and

$$V_e\ (R_L \to 0) = \frac{V_{IN}\ Z_r /\!\!/ Z_f}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{58}$$

On the basis of the relationships expressed by Eqs. (57) and (58), Eq. (56) may be rewritten as follows:

$$I_{OUT}\ (R_L \to 0) = \frac{A_o(\omega)\ V_{IN}\ Z_i\ (Z_r + Z_f)}{Z_{o_i}\left[(Z_r + Z_f)\ (R_r + Z_i) + Z_r\, Z_f\right]} \tag{59}$$

The output impedance Z_{OUT} then becomes

$$Z_{OUT} = Z_{o_i}\left[\frac{Z_r\, Z_f + (Z_r + Z_f)\ (R_r + Z_i)}{A_o(\omega)\ Z_i\ (Z_r + Z_f)}\right]\left(\frac{V_{OUT}}{V_{IN}}\right) \tag{60}$$

Finally, the following precise equation for the output impedance Z_{OUT} is obtained when the ratio for V_{OUT}/V_{IN} is replaced by its impedance equivalent, as given by Eq. (43):

$$Z_{OUT} = \frac{Z_{o_i}[(Z_r+Z_f)(R_r+Z_i)+Z_rZ_f]}{A_o(\omega)Z_i(Z_r+Z_f)} \times \frac{Z_rZ_{o_i}+A_o(\omega)Z_i(Z_r+Z_f)}{(Z_i+R_r)(Z_r+Z_f+Z_{o_i})+Z_r(Z_f+Z_{o_i})+A_o(\omega)Z_iZ_r} \quad (61)$$

If $A_o(\omega)$ is dominant, then Eq. (61) becomes

$$Z_{OUT} \doteq Z_{o_i}\left[\frac{Z_rZ_f+(Z_r+Z_f)(R_r+Z_i)}{A_o(\omega)Z_iZ_r}\right] \quad (62)$$

The expression for the closed-loop output impedance does not revert to its classical form unless both the intrinsic input impedance Z_i and the open-loop gain $A_o(\omega)$ are very large. Under such conditions, the equation for the output impedance reduces to

$$Z_{OUT} \doteq Z_{o_i}\frac{1+\frac{Z_f}{Z_r}}{A_o(\omega)} \quad (63)$$

This classical expression indicates that the output impedance of the noninverting configuration is equal to the intrinsic output impedance Z_{o_i} divided by the loop gain. It should be noted that the classical expressions for the closed-loop output impedances for the inverting and noninverting configurations [Eq. (33) and (63), respectively] are identical.

Equivalent-Circuit Model of a Closed-Loop Operational Amplifier

Fig.3 shows the equivalent circuit of a closed-loop operational amplifier. This equivalent circuit is valid for either the inverting or the noninverting configuration. In the inverting configuration, Z_r is used to represent

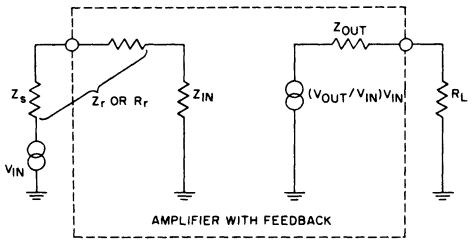


Fig.3 - Equivalent-circuit model of a closed-loop operational amplifier.

the impedance in series with the closed-loop input impedance Z_{IN}. In the noninverting configuration, term Z_r is replaced by R_r to show that the components thus represented are independent of frequency. The closed-loop input and output impedances (Z_{IN} and Z_{OUT}, respectively) and the transfer function V_{OUT}/V_{IN} were defined previously.

Effect of a Finite Load Impedance on Operational-Amplifier Characteristics – One of the important features of the equivalent-circuit model is that it accurately accounts for the effects of a finite load impedance, R_L. For example, if a 2000-ohm load impedance is used on the 46-dB (approximate) inverting amplifier for which data are given in Table I, the equation for the transfer response must be modified as follows:

$$V_{OUT} = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right)V_{IN}R_L}{R_L+Z_{OUT}} \quad (64)$$

If Eq. (6) is used to determine the value of V_{OUT}/V_{IN} and Eq. (30) is used to determine the value of Z_{OUT}, the transfer-function ratio for an R_L of 2000 ohms can be calculated from Eq. (64) as follows:

$$\frac{V_{OUT}}{V_{IN}} = 164\left(\frac{2000\text{ ohms}}{37.4\text{ ohms}+2000\text{ ohms}}\right) = 162 \quad (65)$$

Thus, a ratio of 44.15 dB is obtained, as compared to 44.3 dB for an open-circuit load. Similarly, if a 2000-ohm load is used for the 6-dB amplifier, the gain becomes 5.98 dB, as compared to 6 dB indicated in Table I for an open-circuit load. The error in neglecting a 2000-ohm load, therefore, is 0.15 dB for the 46-dB amplifier and only 0.02 dB for the 6-dB amplifier (for the conditions given in Table I).

Effect of the Common Mode Gain (CMG) on Operational-Amplifier Characteristics – In the developments of the basic equations for the inverting and noninverting feedback configurations of the operational amplifier, it was tacitly assumed that the common-mode gain was essentially zero (infinite attenuation). The common-mode gain is defined as the ratio of the output voltage, V_{OUT}, to the input voltages, V_i and V_e, when V_i and V_e are identical in amplitude and phase. The validity of this assumption is considered separately in this section because the basic feedback equations become burdensome when common-mode effects are included. As a result, the salient features of these equations become obscured.

An examination of Figs. 1 and 2 shows that, in either the inverting or noninverting configuration, the differential gain acts on the difference between the voltages V_i and V_e. On the other hand, the common-mode gain acts on those portions of V_i and V_e that are in phase and identical in magnitude. That is, the com-

mon-mode gain acts on the smaller of the two in-phase signals (V_i or V_e). In the inverting configuration V_i is less than V_e, but in the noninverting configuration V_i is greater than V_e. These conditions are reflected by the output-voltage equations when the effects of the common-mode gain (CMG) are considered, as follows:

1. For the inverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_i) \quad (66)$$

2. For the noninverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_e) \quad (67)$$

If these two equations are developed further, the following gain expressions are obtained for $Z_{o_i} = 0$ (i.e., $V_{o_i} = V_{OUT}$):

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega) Z_i Z_f - (CMG) R_r Z_f}{Z_r(Z_f+Z_i+R_r)+Z_f(Z_i+R_r)+Z_i Z_r A_o(\omega)+R_r Z_r (CMG)} \quad (68)$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega) Z_i (Z_r + Z_f) - (CMG) Z_r Z_f}{(Z_r+Z_f)(R_r+Z_i)+Z_r Z_f+A_o(\omega) Z_i Z_r+(CMG) Z_r (Z_i+R_r)} \quad (69)$$

In each case, the criteria for the common-mode gain, CMG, to be negligible compared to the open-loop gain, $A_o(\omega)$, are as follows:

1. For the inverting configuration,

$$CMG \ll \frac{A_o(\omega) Z_i}{R_r} \quad (70)$$

2. For the noninverting configuration,

$$CMG \ll \frac{A_o(\omega) Z_i}{Z_i + R_r} \quad (71)$$

Eq. (68) or inequality (70) shows that the gain of an inverting configuration is not affected by the common-mode gain when the input impedance V_i is assumed to be infinite. However, when this same assumption is made for a noninverting configuration, the gain is dependent upon the common-mode gain provided the open-loop gain is finite.

Inequalities (70) and (71) may be given in terms of the common-mode rejection, CMR, which is the open-loop gain, $A_o(\omega)$, divided by the common-mode gain, CMG. The following inequalities are then obtained:

1. For the inverting configuration,

$$CMR \gg \frac{R_r}{Z_i} \quad (72)$$

2. For the noninverting configuration,

$$CMR \gg \frac{Z_i + R_r}{Z_i} \quad (73)$$

Neither of these inequalities places a stringent restriction on common-mode rejection.

FEEDBACK PHASE SHIFTS IN OPERATIONAL AMPLIFIERS

In an operational amplifier, as in any other feedback amplifier, the phase of the feedback must be controlled to assure that the design is stable with frequency and that the desired gain-frequency response is obtained. Fig.4 shows the gain and phase characteristics as functions of frequency for a typical 60-dB operational amplifier in which no phase-compensation techniques are employed. Over the frequency range shown, the change in the phase of the feedback is substantially greater than 180 degrees. This phase response indicates that a low-frequency negative feedback can become positive and cause the amplifier to be unstable at high frequencies unless phase-compensation methods are employed to stabilize and control the response of the amplifier.

Effect of Excessive Phase Shift on Frequency Stability

The transfer equation for the inverting configuration, Eq. (7), can be rearranged so that it reflects the same classical feedback form as that for the noninverting configuration, given by Eq. (45). These equations, which are based on the assumptions that Z_i approaches infinity and Z_{o_i} is zero, are repeated below for convenience:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{Z_f}{Z_f + R_r}\right)\left[\frac{-A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}}\right]$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}}$$

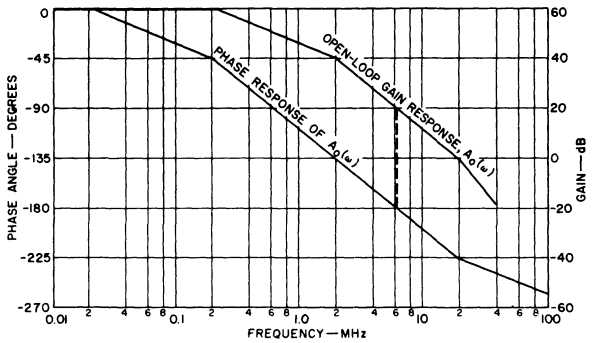


Fig.4 - Gain and phase response of an open-loop operational amplifier operated without phase compensation.

If the phase angle of the feedback term, $A_o(\omega)/(1 + Z_f/Z_r)$, reaches 180 degrees (not asymptotically) while the magnitude of the term is still unity or greater, oscillations will occur. [If the term is greater than unity, the oscillations will build until limiting occurs. This limiting decreases $A_o(\omega)$, and thus the entire feedback term, until unity magnitude at a phase angle of 180 degrees is achieved.] These unstable conditions can be predicted readily. Fig.5 shows a superposition of the gain-frequency curve shown in Fig.4 on several

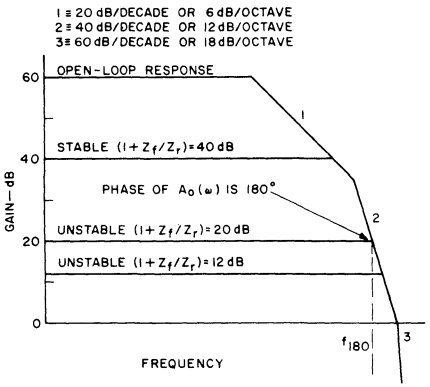


Fig.5 - Open-loop response and stability characteristics of an operational amplifier.

sample plots of the ideal feedback characteristic, as given by $1 + Z_f/Z_r$ when Z_f and Z_r are purely resistive. Because the crucial frequency for a purely resistive feedback network is that at which $A_o(\omega)$ has a phase angle of 180 degrees, the magnitude of $A_o(\omega)/(1 + Z_f/Z_r)$ at this frequency (f_{180}) determines whether the configuration is stable. If $A_o(f_{180})/(1 + Z_f/Z_r)$ is equal to or greater than unity, the configuration is *unstable*. On the other hand, if this term is less than unity, then the configuration is *stable*. This stability-determination technique is applied to the various values of $1 + Z_f/Z_r$ shown in Fig.5; in each case, the gain of the amplifier at the frequency for which the phase angle is 180 degrees is assumed to be 10 [i.e., $A_o(f_{180}) = 10$].

When $1 + Z_f/Z_r = 100/\underline{0^\circ}$, the stability ratio is calculated as follows:

$$\frac{A_o(f_{180})}{1 + \frac{Z_f}{Z_r}} = \frac{10/\underline{180^\circ}}{100/\underline{0^\circ}} = 0.10/\underline{180^\circ}$$

Because the value of 0.10 obtained for the stability ratio is less than unity, the configuration is stable.

When $1 + Z_f/Z_r = 10.0/\underline{0^\circ}$, the stability ratio becomes

$$\frac{A_o(f_{180})}{1 + \frac{Z_f}{Z_r}} = \frac{10/\underline{180^\circ}}{10/\underline{0^\circ}} = 1.0/\underline{180^\circ}$$

For this case, the stability ratio is unity, and the configuration therefore, is unstable. As a check, an examination of the transfer expressions for both the inverting and the noninverting configuration [Eqs. (7) and (45)] reveals that for the condition specified, each contains the following term:

$$\frac{1}{1 + 1/\underline{180^\circ}}$$

which is not finite and, therefore, indicates an oscillating condition.

When $1 + Z_f/Z_r = 4.0/\underline{0^\circ}$,

$$\frac{A_o(f_{180})}{1 + \frac{Z_f}{Z_r}} = \frac{10/\underline{180^\circ}}{4/\underline{0^\circ}} = 2.50/\underline{180^\circ}$$

The value obtained is greater than unity, and the circuit, therefore, is unstable.

When Z_f and Z_r are not restricted to purely resistive values, a more general situation exists because the phase of $A_o(\omega)/(1 + Z_f/Z_r)$ is no longer dependent solely upon $A_o(\omega)$. Two examples which essentially cover the field are given below.

Example No.1 – A characteristic of differentiating or peaking circuits is that the feedback term $1 + Z_f/Z_r$ is in the form $K(1 + jf/f_1)$, where K and f_1 are constants. Fig.6 shows a curve of this term as a function of frequency, for K = 10 and f_1 = 0.1 MHz, superimposed upon an operational-amplifier open-loop transfer curve. The equation for the open-loop characteristic can be derived from Fig.5, as follows:

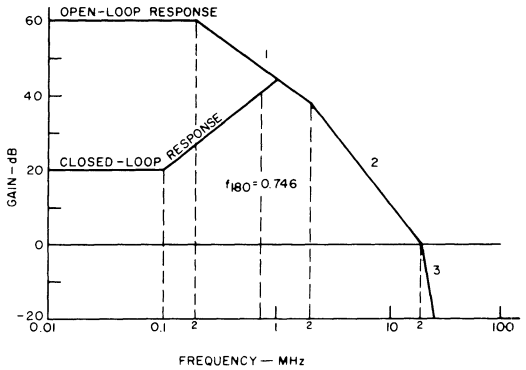


Fig.6 - Basic peaking response characteristics of an operational amplifier.

$$A_o(\omega) = \frac{1000}{\left(1 + j\frac{f}{0.2\ \text{MHz}}\right)\left(1 + j\frac{f}{2\ \text{MHz}}\right)\left(1 + j\frac{f}{20\ \text{MHz}}\right)}$$

$$1 + \frac{Z_f}{Z_r} = 10\left(1 + j\frac{f}{0.1\ \text{MHz}}\right)$$

$$A_o(\omega) = \frac{1000}{\left(1 + j\frac{f}{0.2\ \text{MHz}}\right)\left(1 + j\frac{f}{2\ \text{MHz}}\right)\left(1 + j\frac{f}{20\text{MHz}}\right)} \quad (74)$$

The frequency at which the stability ratio $A_o(\omega)/1 + Z_f/Z_r$ has a phase angle of 180 degrees and the magnitude of the ratio for this frequency can then be calculated. The computation reveals that the phase angle is 180 degrees at a frequency (f_{180}) of 0.746 MHz, and the magnitude of the ratio is 3.22 at that frequency. The stability ratio is greater than one; therefore, the configuration is *unstable*. The point of instability (f_{180}) is marked in Fig.6.

The stability of an operational amplifier may be determined more easily from an *estimate* of the phase angle of the ratio $A_o(\omega)/(1 + Z_f/Z_r)$ at the frequency of intersection (where the magnitude of the ratio is unity). If the estimate shows that the phase angle is less than 180 degrees, the configuration is stable. On the other hand, if the estimate indicates a phase angle in excess of 180 degrees, the circuit is unstable. When the estimate shows that the phase angle is near 180 degrees, an accurate calculation is required to determine whether the operational amplifier is stable. This border-line type of configuration, however, is generally undesirable from the standpoint of frequency response, as discussed later.

In the application of the estimation technique to the problem presented in Fig.6, the following conditions should be noted: The feedback characteristic $1 + Z_f/Z_r$ increases at the rate of 6 dB per octave (20 dB per decade) for a full decade before it intersects the open-loop response, $A_o(\omega)$. The intersection occurs near the second corner of the open-loop response, which decreases at the rate of 6 dB per octave for almost a full decade. The classical phase relationships associated with these observations are used to obtain the following phase estimates:

$$\text{Phase of } (1 + Z_f/Z_r) = +90°$$
$$-135° < \text{Phase of } A_o(\omega) < -90°$$

Therefore, the following phase estimate is obtained at the frequency of the intersection:

$$-225° < \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) < -180°$$

Thus, the configuration is *unstable*.

Example No.2 – An inherent characteristic of integrating or band-limiting configurations is that the feedback term $1 + Z_f/Z_r$ has the following form:

$$\frac{K}{1 + jf/f_1}$$

An example of this type of feedback characteristic is shown in Fig.7 for K = 10 and f_1 = 4 MHz. The application of the phase-estimation technique to this problem results in the following estimates:

$$-45° > \text{Phase of } 1 + Z_f/Z_r > -90°$$
$$-135° > \text{Phase of } A_o(\omega) > -225°$$

At the frequency of intersection, therefore, the phase estimate is given by

$$-45° > \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) > -180°$$

Thus, the configuration is *stable.*

If the three basic types of feedback characteristics shown in Figs.5, 6, and 7 are compared, it becomes evident that the differentiating or frequency-peaking

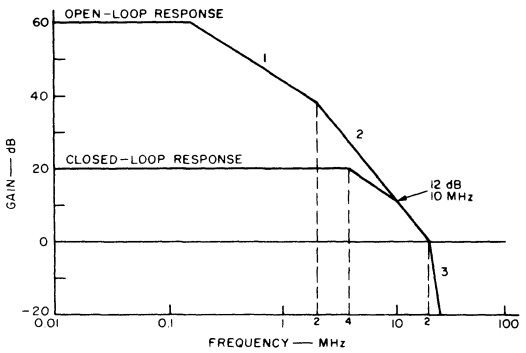


Fig.7 - Basic integrating response characteristics of an operational amplifier.

configuration is the most unstable and that the integrating or low-pass configuration is the most stable. In fact, the techniques used to devise this latter configuration may be considered a form of phase compensation for certain situations, as discussed later.

Effects of Excessive Phase-Shift on Frequency Response

The criterion evolved for frequency stability neither precludes uncontrolled frequency peaking nor provides for a 3-dB closed-loop bandwidth prediction. The conditions that are required to develop a stable, controlled-response feedback amplifier are evolved in this section.

Criteria for a Peaked Response – Frequently peaking results when the magnitude of the true closed-loop gain, as given by Eq. (7) for the inverting configuration and by Eq. (45) for the noninverting configuration, is greater than the magnitude of the ideal closed-loop gain (Z_f/Z_r for an inverting circuit and $1 + Z_f/Z_r$ for a noninverting circuit). The criteria for frequency peaking can be expressed for both configurations by the following expressions:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| > \left| 1 + \frac{Z_f}{Z_r} \right| \tag{75}$$

Inequality (75) may be used to develop a set of criteria that predict frequency peaking (or preclude the occurrence of frequency peaking).

The following substitution is first made in inequality (75):

$$\frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \equiv B\underline{/\theta} \tag{76}$$

If both sides of inequality (75) are then divided by the left-hand term, the following result is obtained:

$$1 > \left| 1 + \frac{1}{B}\,\underline{/-\theta} \right| \tag{77}$$

Inequality (77) may be rewritten in either of the following forms:

$$1 > \left[\left(1 + \frac{1}{B}\cos\theta \right)^2 + \left(-\frac{1}{B}\sin\theta \right)^2 \right]^{\frac{1}{2}} \tag{78}$$

or

$$1 > \left[1 + \frac{2}{B}\cos\theta + \left(\frac{1}{B} \right)^2 \right]^{\frac{1}{2}} \tag{79}$$

The real and imaginary parts of inequality (78) must also be less than unity, so that

$$1 > \left| 1 + \frac{1}{B}\cos\theta \right| \tag{80}$$

and

$$1 > \frac{1}{B} \left| -\sin\theta \right| \tag{81}$$

It is apparent from inequality (80) that

$$B > \frac{1}{2} \tag{82}$$

and from inequality (79) that

$$\cos\theta < -\frac{1}{2B} \tag{83}$$

The substitution indicated by the identity (76) is again made, and both sides of inequality (75) are then divided by the right-hand term to obtain the following expressions:

$$\left| \frac{B\underline{/\theta}}{1 + B\underline{/\theta}} \right| > 1 \tag{84}$$

or

$$\left| B\underline{/\theta} \right| > \left| 1 + B\underline{/\theta} \right| \tag{85}$$

For peaking to occur, the following relationships must be in effect:

$$0.5 < \left| B\underline{/\theta} \right| < 2.62$$

$$\cos\theta < -\frac{1}{2B}$$

3-dB Bandwidth Prediction – The 3-dB bandwidth of an operational amplifier is defined by the following condition:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| = \frac{\left| 1 + \frac{Z_f}{Z_r} \right|}{\sqrt{2}} \tag{86}$$

The terms of Eq. (86) are rearranged and the definition for $B\underline{/\theta}$ given by the identity (76) is used to obtain the following relationships:

$$\left| 1 + \frac{1}{B}\underline{/-\theta} \right| = \sqrt{2}$$

$$\left(1 + \frac{1}{B}\cos\theta\right)^2 + \left(-\frac{1}{B}\sin\theta\right)^2 = 2$$

$$1 + \frac{2}{B}\cos\theta + \left(\frac{1}{B}\right)^2 = 2 \tag{87}$$

Eq. (87) yields the following criteria for the 3-dB point:

$$1 \geq B > \frac{1}{1 + \sqrt{2}} = 0.414 \tag{88}$$

$$\cos\theta = \frac{B^2 - 1}{2B} \tag{89}$$

Inequality (88) predicts the possibility of a 3-dB bandwidth greater than that indicated by the intersection of $A_o(\omega)$ and $1 + Z_f/Z_r$ ($B = 1$ point). However, it should be realized that this "bandwidth extension" is actually caused by a slight peaking effect. Special care should be exercised in any attempt to use this effect to advantage.

Inequality (89) stipulates that the phase angle must be 90 degrees to obtain the 3-dB bandwidth where $B = 1$. This stipulation essentially coincides with a "rule of thumb" that has become a standard in the industry. This rule may be stated as follows: *For an unconditionally stable configuration, the ideal feedback characteristic, $1 + Z_f/Z_r$, must intersect the open-loop response, $A_o(\omega)$, at a slope less than 12 dB per octave.* An examination of this "rule of thumb" in terms of the phase relationship indicates that the phase angle asymptotically approaches 180 degrees when the change in amplifier response with frequency occurs at a rate of 12 dB per octave. Therefore, the amplifier is on the threshold of instability. Frequency dependence of less than 12 dB per octave indicates that the amplifier is stable; a dependence of greater than 12 dB per octave indicates that the amplifier is unstable.

PHASE-COMPENSATION TECHNIQUES FOR OPERATIONAL AMPLIFIERS

The design problems (i.e., ac instability and uncontrolled frequency response) created by excessive phase shift in the feedback can be solved by use of compensating techniques that alter the feedback response so that excessive phase shifts no longer occur. The frequency response can be controlled by limiting the slope of the intersection of the ideal feedback characteristic, $1 + Z_f/Z_r$, with the open-loop gain response, $A_o(\omega)$, to a safe value. Theoretically, this slope can have a maximum value of 12 dB per octave under certain conditions. In general, however, the maximum slope allowed for practical lumped-parameter systems is 6 dB per octave. In an operational amplifier, effective phase compensation can be accomplished only by a modification in one or more of the following parameters:

1. the ideal closed-loop gain (feedback characteristic), $1 + Z_f/Z_r$;
2. the open-loop input impedance, Z_i;
3. the open-loop gain, $A_o(\omega)$.

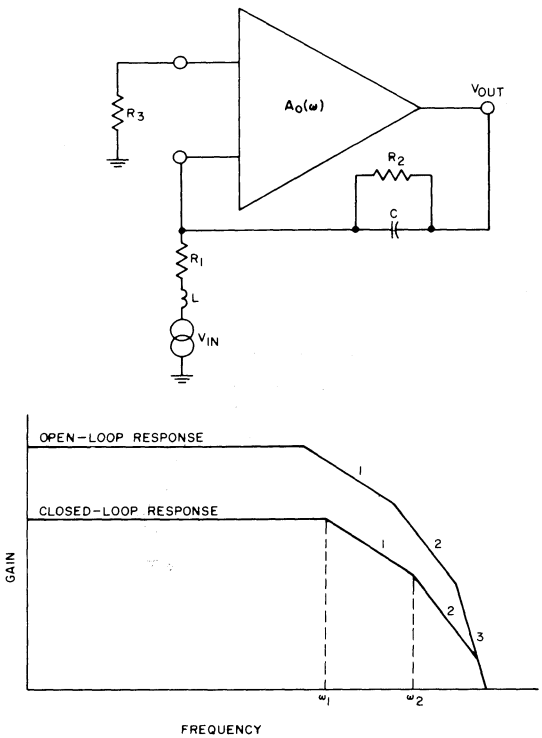
Closed-Loop Compensation Method

Phase compensation can be accomplished by modification of the closed-loop gain characteristic (i.e., the $1 + Z_f/Z_r$ term) for only those applications in which the intersection of the $1 + Z_f/Z_r$ characteristic with the open-loop response occurs in a region where the open-loop response rolls off at a slope of 12 dB per octave or 18 dB per octave. When the intersection occurs in a 12-dB-per-octave region of the $A_o(\omega)$ response, compensation techniques are used that cause the slope of the $1 + Z_f/Z_r$ response to roll off at 6 dB per octave near the intersection. As a result of these techniques, the slope of the intersection becomes 6 dB per octave. (An example of this method of phase compensation was discussed earlier, in the section on "Criteria for a Peaked Response", and the response curves for this example were shown in Fig.7.)

For applications in which the use of an inductor is permissible, phase compensation in the 18-dB-per-

octave region of the open-loop response can be accomplished by techniques that cause the $1 + Z_f/Z_r$ response to roll off at 12 dB per octave near the intersection. An example of this method of phase compensation, together with the appropriate response curves, is shown in Fig.8.

In this example, the Z_f term is altered by a shunt capacitor and the Z_r term is altered by a series inductor so that the $1 + Z_f/Z_r$ response has the required 12-dB-per-octave roll-off. The location of these frequency-dependent components in the feedback configuration is unique for this type of phase compensation.



$$R_3 = R_1 /\!/ R_2$$

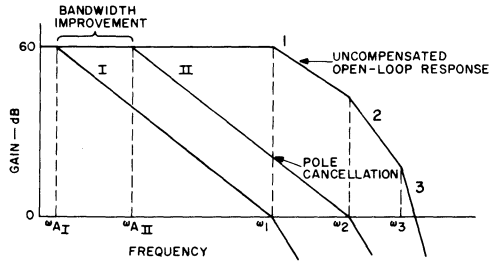
$$\frac{V_{OUT}}{V_{IN}} = \frac{-\dfrac{R_2}{1 + j\omega CR_2}}{R_1 + j\omega L}$$

$$= -\frac{R_2}{R_1}\left[\frac{1}{\left(1 + j\,\dfrac{\omega L}{R_1}\right)(1 + j\omega CR_2)}\right]$$

Fig.8 - Phase compensation of operational amplifier permissible in the "three-slope region".

Open-Loop Compensation Methods

Phase-compensation techniques that alter either the open-loop input impedance or the open-loop gain permit the introduction of a zero, in addition to the low-frequency pole, into the open-loop gain characteristic. This zero can be designed to cancel one of the poles in the open-loop gain characteristic and thus to increase substantially the bandwidth of the operational amplifier. Alternatively, the operational-amplifier bandwidth can be increased by the introduction of a pole at a frequency low enough so that all the other corner points will occur at frequencies below that at which the open-loop response, $A_o(\omega)$, intersects the closed-loop response, $1 + Z_f/Z_r$. The two methods are compared in Fig.9. It is apparent that the pole-cancellation method of phase compensation is superior to the method in



I—Compensated open-loop response using simple depression of higher corner frequencies.

II—Compensated open-loop response using pole cancellation.

Fig.9 - Phase compensation of operational amplifier by use of pole cancellation.

which the other corner frequencies are depressed. In the phase-compensation techniques discussed below, therefore, the pole-cancellation method is employed.

Modification of the Open-Loop Input Impedance — The following analysis shows the limitations imposed on alterations in the open-loop input impedance of an operational amplifier in order to provide phase compensation. In this phase-compensation technique, an appropriate network is connected between the input terminals so that it appears in parallel with the intrinsic input impedance, Z_i. Eqs. (7) and (45), which define the closed-loop inverting and noninverting responses, respectively, are used as the basis for establishing the conditions and the mechanisms involved in this kind of compensation.

If Z_i' is used to represent the modified open-loop input impedance and the open-loop output impedance,

Z_{oi}, is assumed to be zero, the following equations for the closed-loop response are obtained:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\, Z_i'\, Z_f}{Z_f\,(Z_i' + R_r) + Z_r\,(Z_f + Z_i' + R_r) + A_o(\omega)\, Z_i'\, Z_r} \quad (90)$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\, Z_i'\,(Z_r + Z_f)}{(Z_i' + R_r)\,(Z_r + Z_f) + Z_r\, Z_f + A_o(\omega)\, Z_i'\, Z_r} \quad (91)$$

A judicious rearrangement of terms in Eqs. (90) and (91) reveals the effect that the altered open-loop input impedance has on the open-loop response. With this rearrangement, the equation for the inverting configuration becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_f}{Z_f + \frac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \quad (92)$$

The equation for the noninverting configuration is then written as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] (Z_r + Z_f)}{Z_f + \frac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \quad (93)$$

For each configuration, the modified open-loop response is defined as follows:

$$A_o'(\omega) \equiv \frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'} \quad (94)$$

It is apparent from Eq. (94) that the alteration of the open-loop input impedance has no effect on the open-loop response unless Z_i', is at most, of the same order of magnitude as the $R_r + Z_r$ term. If Z_i' is made much less than $R_r + Z_r$, Eq. (94) becomes

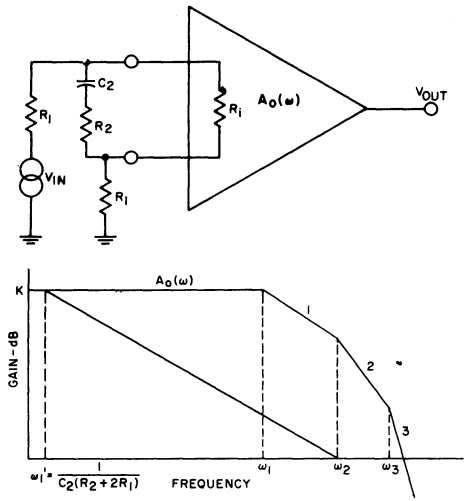
$$A_o'(\omega) \doteq \frac{A_o(\omega)\, Z_i'}{R_r + Z_r} \quad (95)$$

As predicted by Eqs. (94) and (95), three limitations are imposed in the use of the input-impedance modification technique to provide phase compensation: (1) the feedback impedance term Z_r is restricted in value and configuration by the phase-compensation requirements; (2) the effective open-loop input impedance must be smaller in magnitude than and different in configuration from the intrinsic input impedance, Z_i (thus the closed-loop input impedance, Z_{IN}, also is smaller and different); and (3) the dc open-loop gain is less for some input-impedance configurations.

Two examples of the input-impedance phase-compensation technique are shown in Figs. 10 and 11. In the method shown in Fig.10, the required modification of the open-loop response is achieved by proper choice of the frequency characteristics for the network connected in shunt with the input terminals of the operational amplifier. Fig.11 shows that the required modification of the response can be achieved by the appropriate choice of the frequency characteristics of R_r and Z_r. Both techniques employ pole-zero cancellation to extend the 6 dB-per-octave roll-off region depicted. The technique illustrated in Fig.10 causes an early roll-off, while the one shown in Fig.11 results in a reduction in the dc open-loop gain. Eqs. (94) and (95) indicate that phase-compensation can also be effected by an increase in the magnitude of $R_r + Z_r$, provided that the frequency characteristics of this parameter are controlled. However, this technique relies on the accuracy of the value of Z_i and therefore is unsatisfactory. (The intrinsic input impedance of an operational amplifier may vary significantly from unit to unit.)

Modification of Open-Loop Gain Characteristics – Phase compensation that is effected by internal modification of the open-loop gain response is the most widely accepted technique for integrated-circuit operational amplifiers. This method offers two distinct advantages over other types of phase compensation. First, the internal-modification technique affords complete isolation of the phase-compensation networks from the feedback parameters. This isolation is not possible with the compensation methods discussed previously. Second, the point at which the phase compensation is applied can be selected so that the open-loop response is altered in such a way that one of the existing 3-dB corner frequencies becomes the early roll-off corner in the compensated response. The advantage stems from the fact that no new corner frequencies are introduced, and an improved compensated response is thus obtained.

Internal phase compensation can be accomplished by either of two basic methods. In one method, referred to as the straight roll-off, an appropriate RC network is connected across a suitable internal resistor of the operational amplifier. With this method, the early roll-off starts at the corner frequency produced by the phase-compensating capacitor and the internal resistor. The other method is the Miller-effect roll-off. In this method, the phase-compensating network still appears electrically to be placed across an appropriate internal resistance of the amplifier, but is actually connected between the input and the output of an inverting-gain stage in the operational amplifier. The impedance of the compen-



$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain
R_i = low-frequency intrinsic input impedance

$$A_o'(\omega) = \frac{\pm A_o(\omega) R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}{\left(R_i + R_2 + \frac{1}{j\omega C_2}\right) 2R_1 + R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}$$

$$A_o'(\omega) = \left[\frac{\pm A_o(\omega) R_i}{2R_1 + R_i}\right]\left[\frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 \left(R_2 + \frac{2R_i R_1}{2R_1 + R_i}\right)}\right]$$

Because R_i is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \pm A_o(\omega) \frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 (R_2 + 2R_1)}$$

For $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

and if $$R_2 C_2 = \frac{1}{\omega_1}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) = \frac{K}{[1 + j\omega C_2 (R_2 + 2R_1)]\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + \frac{\omega}{\omega_3}\right)}$$

Fig.10 - Phase compensation of operational amplifier in which open-loop response is modified by connection of a compensating network that provides the required frequency characteristics in shunt with input terminals.

sating network then appears to be divided by the gain of that stage.

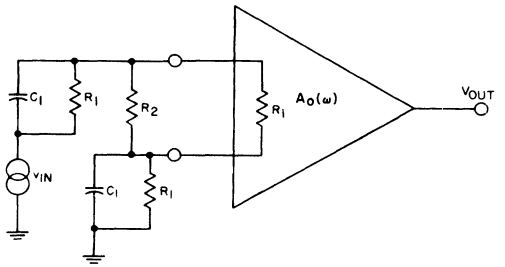
The Miller-effect roll-off technique requires a much smaller phase-compensating capacitor than that which must be used with the straight roll-off method. Moreover, the reduction in swing capability which is inherent in the straight roll-off is delayed significantly when the Miller-effect roll-off is used. Fig.12 illustrates the solution to the problem of phase compensation of an operational amplifier in which a straight roll-off is used to cause the second 3-dB corner frequency to occur at unity gain. Fig.13 illustrates the use of a Miller-effect roll-off to solve the same problem. For the same early corner frequency, the compensating capacitance required in the Miller-effect method is less than that required in the straight roll-off method by a factor of $1 + g_{mII}R_{c2}$ (g_{mII} and R_{c2} are defined in Fig.13).

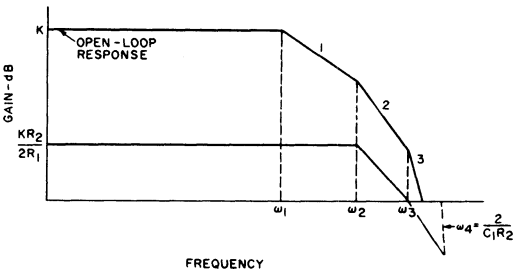
DESIGN CRITERIA FOR OPERATIONAL AMPLIFIERS

It is apparent from the previous discussions that a completely universal design of an operational amplifier would have to satisfy an impossible set of criteria. As a result, the design of operational amplifiers is a somewhat specialized process in that a particular amplifier is usually designed for specific applications. For example, certain operational amplifiers are designed to provide high-frequency gain at the expense of other performance characteristics, while other operational amplifiers provide very high gain or high input impedance in low-frequency applications. Integrated-circuit operational amplifiers, which are fabricated by the diffusion process, can be made suitable for comparator applications or can be processed to provide high gain at low dissipation levels. For these reasons, any discussion of the criteria for operational amplifiers must be of a general nature unless a specific application is being considered.

Input and Output DC Levels

In general, an operational amplifier should be designed so that the dc bias levels at the input and the output are equal. This condition is desirable to assure that the resistive feedback network can be connected between the input and the output without upsetting either the differential or the common-mode dc bias. Moreover, for applications in which two (positive and negative) power supplies are used, the operational amplifier should be designed so that it is possible to establish a set of standard supply values for which the equal input and output bias levels are at zero potential with respect to circuit ground. This latter condition is particularly important in direct-coupled cascade and comparator applications.





$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = \frac{\pm A_o(\omega)\, R_2\, R_i}{(R_2 + R_i)\left(\frac{2\,R_1}{1 + j\omega_1 R_1 C_1}\right) + R_2\, R_i}$$

$$= \left[\frac{\pm A_o(\omega)\, R_2\, R_i}{2R_1(R_2+R_i) + R_2 R_i}\right]$$

$$\left[\frac{1 + j\omega\, R_1 C_1}{1 + j\omega \dfrac{R_1 R_2\, R_1 C_1}{2R_1(R_2+R_i) + R_2 R_i}}\right]$$

Because R_i is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \left(\frac{\pm A_o(\omega)\, R_2}{2R_1 + R_2}\right)\left(\frac{1 + j\omega\, R_1 C_1}{1 + j\omega \dfrac{C_1 R_1 R_2}{2R_1 + R_2}}\right)$$

If $R_2 << R_1$, the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \left(\frac{\pm A_o(\omega)\, R_2}{2R_1}\right)\left(\frac{1 + j\omega R_1 C_1}{1 + j\omega C_1 \dfrac{R_2}{2}}\right)$$

For $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

and $$R_1 C_1 \equiv \frac{1}{\omega_1},$$

the compensated open-loop gain $A_o'(\omega)$ is given by

$$A_o'(\omega) = \frac{\pm K}{2\dfrac{R_1}{R_2}\left(1 + j\omega C_1 \dfrac{R_2}{2}\right)\left(1 + \dfrac{\omega}{\omega_2}\right)\left(1 + \dfrac{\omega}{\omega_3}\right)}$$

Fig.11 - Phase compensation of operational-amplifier in which open-loop response is modified by alteration of the $R_r + Z_r$ term to provide the required frequency characteristics.

Output-Power Capability

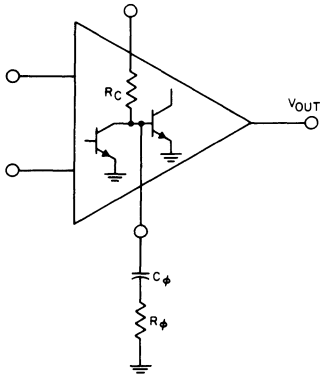
As with any amplifier circuit, the output-power requirements for an operational amplifier depend almost entirely on the application. A few general conclusions can be drawn concerning the design of the output stage. First, this stage should provide a voltage swing essentially equal to the sum of the power-supply voltages. It should have sufficient gain so that it is the first stage to limit when the amplifier is overdriven. Finally, because of the design trade-off that is always required between output-power capability and dissipation, the output stage should be sufficiently versatile so that the output capability and dissipation can be tailored to the power needs of the particular application in which the operational amplifier is used.

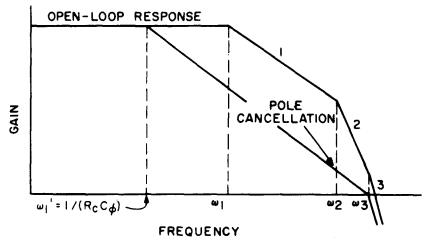
Gain and Frequency-Response Characteristics

The numerical values of the open-loop gain and the 3-dB bandwidth of an operational amplifier are of relatively little importance in themselves. The important requirement is that the open-loop gain must be much greater than the closed-loop gain of the transfer response over the frequency range of interest if an accurate transfer function is to be maintained. (This requirement is explained in detail in the discussions of transfer functions for both the inverting and noninverting configurations.) For example, if a 40-dB amplifier and a 60-dB amplifier are used in a 20-dB gain configuration and the open-loop gain is decreased 50 per cent in each case, the closed-loop gain of the 40-dB amplifier varies only 9 per cent and that of the 60-dB amplifier varies only 1 per cent.

The frequency roll-off characteristics are the prime determinants of the frequency response of an operational amplifier. The greater the rate of roll-off prior to the intersection of the feedback-ratio frequency characteristic with the open-loop response (in the active region), the more difficult phase compensation of the operational amplifier becomes. An 18-dB-per-octave roll-off is generally considered the maximum slope that can occur in the active region before proper phase compensation becomes extremely difficult or impossible to achieve

(as indicated in the discussion on the effects of feedback phase shifts). In addition, because operational amplifiers have useful applications down to and including unity gain, the active region of the amplifier may be considered as the entire portion of the frequency characteristic above its 0-dB bandwidth. Therefore, a well-designed amplifier should roll off at no greater than 18 dB per octave until well below unity gain.





$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the equation above accounts for the modification of the ω_1 3-dB corner.

For $$R_\phi C_\phi = \frac{1}{\omega_2}$$

and $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{K}{(1 + j\omega R_c C_\phi)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

A third corner-frequency term, which occurs because of the time constant of R_ϕ and the input capacitance of the succeeding stage, should also be included in the equation above; the effects of this corner frequency, however, is appreciable only at very high frequencies (and usually at a gain less than unity). Because the corner frequency normally occurs well out of the active region, it is omitted in the expression for $A_o'(\omega)$.

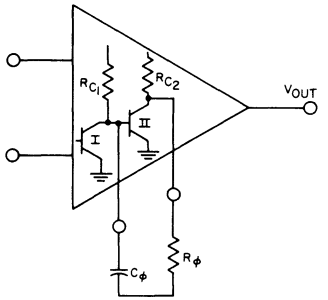
Fig.12 - Phase compensation of operational amplifier by use of straight-rolloff method to modify open-loop response.

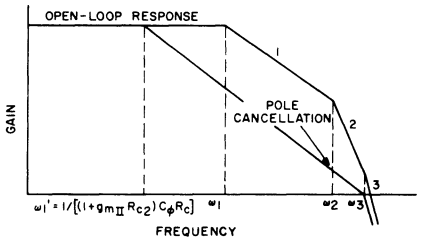
Intrinsic Input and Output Impedances

The ideal values for the input and output impedances of an operational amplifier are infinity and zero, respectively (as mentioned in the discussions on input and output impedances for both inverting and noninverting configurations). The degree to which a practical amplifier approximates these values depends, for the most part, upon the application. A 5000-ohm open-loop input impedance may be quite sufficient for one application, while a 0.1-megohm intrinsic input impedance may not be sufficient for another. In most applications, however, the restrictions on the intrinsic input impedance are not severe. The closed-loop input impedance, which is equal to the product of the intrinsic input impedance and the gain "throwaway" or loop gain, is a more critical parameter. This parameter effectively increases the input impedance (decreases input capacitance) and is the reason that many operational amplifiers that have an input roll-off in the active region have no input roll-off in this region after negative feedback is applied.

Because the closed-loop output impedance is also affected by the loop gain (the proportionality is inverse), the same conclusions might be drawn about the importance of the intrinsic output impedance. Another factor, however, affects the restrictions placed upon the open-loop output impedance. A limiting situation in an inverting-configuration application affords an alternate path to the signal when the intrinsic output impedance is sufficiently high. The loop gain decreases to zero as the open-loop gain decreases when overdrive occurs. Therefore, the closed-loop output impedance increases until it equals the intrinsic value at full limiting. Thus, the intrinsic output must be much less than the lowest

practical value of feedback impedance or an alternate signal path that effectively bypasses the limiting amplifier will exist through the feedback network.





$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c (1 + g_{m_{II}} R_{c_2}) C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the expression for $A_o'(\omega)$ accounts for the modification of the ω_1 3-dB corner.

For $$R_\phi C_\phi = \frac{1}{\omega_2}$$

and $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

The expression for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{K}{[1 + j\omega (1 + g_{m_{II}} R_{c_2}) C_\phi R_c]\left(1 + j\frac{\omega}{\omega_3}\right)}$$

A third corner frequency, which results from the time constant of R_ϕ and the feedback capacitance C_{bc}', is neglected in the expression for $A_o'(\omega)$, because this corner frequency occurs well out of the active region.

Fig. 13 - Phase compensation of operational amplifier by use of Miller effect to modify open-loop response.

Common-Mode Rejection

Under differential drive conditions, the common-mode rejection has no drastic effects on the performance of the operational amplifier unless the rejection ratio is extremely low (as discussed in respect to the effects of common-mode gain). However, in a common-mode drive situation, such as in a comparator type of application, high common-mode rejection is imperative. For example, if a 60-dB differential amplifier having a 50-dB common-mode rejection is used to compare a 1-volt signal against a 1-volt reference, the output will be 3.2 volts when it should be zero. Such results would be disastrous for almost any application of this type. In general, the common-mode rejection should be a minimum of 20 dB greater than the differential gain.

Input Bias Current

Although an amplifier may have a high intrinsic input ac impedance, it can still require a significant amount of dc input bias current. This condition is undesirable in applications in which the drive source cannot accommodate a significant dc current. Examples of such applications are those that require very high impedance sources or sources of a magnetic nature that can be severely unbalanced by a flow of dc current. Unfortunately, the bipolar transistor remedies for this effect add so much capacitance that the frequency response of the amplifier is impaired. Therefore, either field-effect devices should be used in the differential input stage or a scheme should be available to assure that a very low bias current is obtained when it is absolutely necessary. The latter technique requires that sufficient leads be provided so that two external transistors can be added to form a Darlington or a modified Darlington input configuration.

Offset Voltage and Current

The offset voltage of an operational amplifier is the deviation of the output dc level from the arbitrary input-output level usually taken as ground reference when both inputs are shorted together. The offset current is the deviation when the inputs are driven by two identical dc input bias-current constant-current sources. These two offset parameters are usually referred to the input because their output values are dependent on feedback. Under normal operating conditions, the offset in the amplifier results from a combination of the two factors. For example, if an operational amplifier has a 1-millivolt input offset voltage and a 1-microampere input offset current with the inputs returned to ground through 1000-ohm resistors, the total input offset is either zero or 2 millivolts depending upon the phase relationship between the two offset parameters. The offset of an operational amplifier is a dc error and should be minimized for numerous reasons, including the following:

(1) The use of an operational amplifier as a true dc amplifier is limited to signal levels much greater than the offset. (2) Comparator applications require that the output voltage be zero (within limits) when the two input signals are equal and in phase. (3) In a direct-coupled cascade, such as a video amplifier chain, the input offset of the first stage determines the offset characteristics of the entire system. Hence, the gain of the system must be limited to a value that is insufficient to cause limiting at rated output voltage. This value is reduced when the offset is significant.

Power-Supply Stability

The power-supply stability is a measure of the sensitivity that the offset has to power-supply variations. Because the value of the offset at the output is dependent on feedback, this sensitivity is normally referred to the input and expressed in microvolts per volt. In a fixed-installation application that employs heavily regulated power supplies, this parameter is of little importance. In battery-operated applications of the operational amplifier, however, the sensitivity of the offset to power-supply variations is of the utmost importance. In a single-supply system, this sensitivity should be an absolute minimum. In a two-supply system, the difference in the sensitivities to each supply can be minimized because the supplies in many dual systems tend to track. This tracking results in a cancellation, or at least a partial cancellation, of the two sensitivities.

Temperature-Stability Requirements

Temperature stability of an operational amplifier requires stable thermal characteristics for most of the parameters discussed in this Note. The stability demands imposed on the temperature characteristics of an operational amplifier are determined to a large extent by the application in which the circuit is used. In certain applications, stable temperature characteristics are of utmost importance; in other applications, the ability of the operational amplifier to perform the required functions is not appreciably affected by variations in circuit parameters with temperature.

In general, the dependence of the open-loop gain on temperature is of less importance than the thermal behavior of the amplifier frequency response. Variations in the intrinsic input and output impedances with temperature are of little consequence provided that the input impedance remains large enough and the output impedance remains small enough to satisfy the requirements of the application. If the value of the input bias current is important for the application in which the operational amplifier is used, stable temperature behavior is just as important. Variations in the offset voltage and current with temperature should always be small because they directly affect the internal biases, and thus the operation, of the operational amplifier.

Application of RCA CA3033 and CA3033A High-Performance Integrated-Circuit Operational Amplifiers

by

H. A. Wittlinger

The new RCA CA3033 and CA3033A high-performance operational amplifiers represent a significant step forward in monolithic integrated circuits in many respects. They are capable of delivering power outputs in excess of 250 milliwatts into a 500-ohm load resistance with harmonic distortion of less than 0.2 per cent, and have a typical input impedance of one megohm with voltage gain of at least 90 dB. Offset voltage is less than 5 millivolts, and offset current is typically 9 nanoamperes. Input bias current is typically 100 nanoamperes. These features make these amplifiers especially suitable for systems in which an operational amplifier and power amplifier or driver were formerly required.

Circuit Description

The RCA CA3033 and CA3033A consist of two differential-amplifier stages followed by a class B output stage, as shown in the schematic diagram of Fig.1. (The two circuits are designed to permit operation from dual 12- and 18-volt dc power supplies, respectively.) Emitter-follower inputs provide the exceptionally high input impedance and low bias current. An additional advantage of the emitter-follower inputs is that the Miller capacitance of the differential amplifier is substantially reduced and the input capacitance of the amplifier is lower than if a similar single-transistor configuration were used.

The output of the first differential-amplifier stage (Q_3 and Q_4) is buffered from the input of the next differential-amplifier stage (Q_6 and Q_7) by emitter followers Q_{19} and Q_{20}. This arrangement reduces the input-loading effects on the first stage and therefore maintains the first-stage gain.

A circuit is incorporated in this design to sense any change in the operating point of the first differential amplifier caused by variations in either the positive or the negative supply voltage. Any changes in the supply voltages are reflected to the base of transistor Q_5, which detects changes in the collector voltage of the first differential amplifier and compensates for them. For example, a rise in the voltage at the emitters of Q_6 and Q_7 increases the bias voltage to Q_5 and thus increases the collector current, countering the apparent rise in the collector voltage of either Q_3 or Q_4. At the same time, the emitter current of Q_5 also increases, and increases the voltage drop across the diode-connected

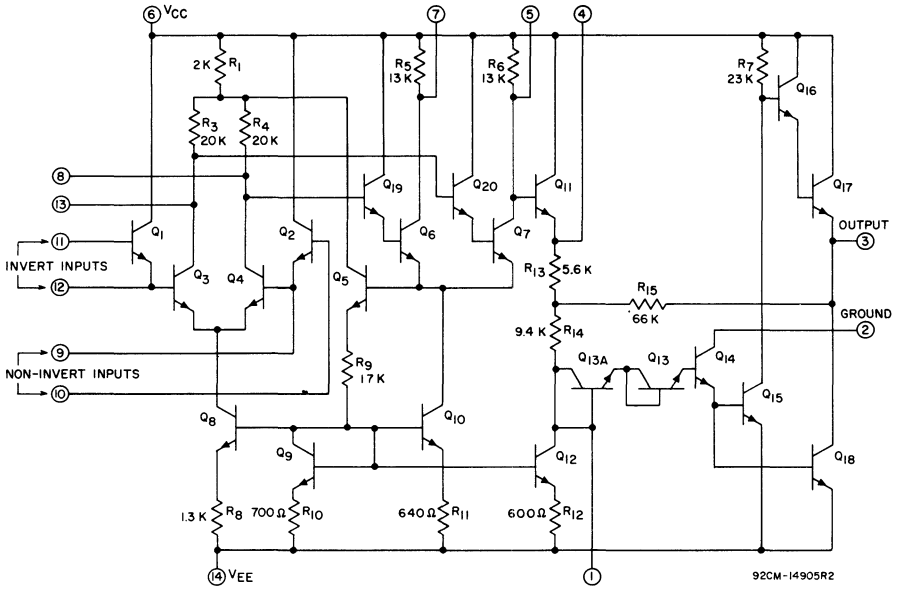


Fig.1 - Schematic diagram of a CA3033 or CA3033A operational amplifier.

transistor Q9 and resistor R10 to increase the collector current of Q8. Thus, any apparent increase in the collector voltage of the first differential stage causes a correction both at the constant-current source Q8 and at the collector supply voltage through R_1, the common load resistor for Q_3, Q_4, and Q_5.

An emitter-follower Q_{11} buffers the output of the second differential-amplifier stage and drives the divider and summing network to the output stage. Resistor R13 may be considered the input resistance of an amplifier to the summing point, the junction of R_{13}, R_{14}, and R15. Resistor R_{14} shifts to the operating point of the output stage with little attenuation of the signal as a result of the high collector impedance of the constant-current source Q_{12}.

Diode-connected transistors Q_{13A} and Q_{13} provide further dc shifting of the signal to the base of emitter-follower Q_{14}. This emitter-follower provides further level shifting and a low driving impedance to transistors Q_{15} and Q_{18}.

The excellent matching of the base-to-emitter voltage of the integrated-circuit transistors makes it possible to establish the idling current of the output stage accurately. Because the collector-current characteristics of Q_{15} and Q_{18} as a function of base-to-emitter voltage are matched, the collector current in Q_{15} determines the idling current in Q_{18}. For example, if the operating current of Q_{15} is set at 1 milliampere for a given base-to-emitter voltage, the operating current of Q_{18} is also 1 milliampere because the base-to-emitter voltages of both transistors are the same. This type of design results from the excellent transistor matching that is possible with monolithic processing.

Noise Figure

Fig.2 shows noise figure as a function of source resistance for the CA3033A. The curve shows that the optimum noise match occurs for input impedances between 100,000 ohms and 1 megohm. An improvement

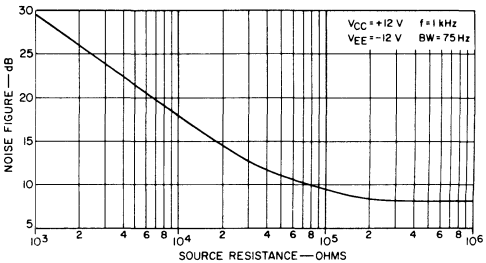


Fig.2 - Noise-figure curve for CA3033A.

in noise figure of approximately 14 dB at a frequency of 1 kHz and an input impedance of 1000 ohms may be obtained by addition of two 0.3-megohm resistors from the emitters to the V_{EE} supply to increase the operating current of the input transistors.

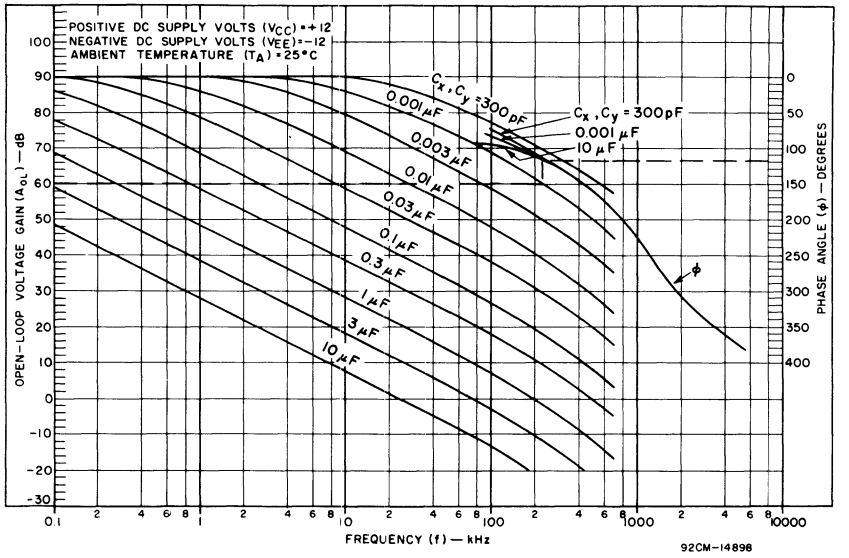


Fig.3 - Phase-compensation characteristics for CA3033 or CA3033A.

Compensation

Basic phase compensation of the CA3033 and CA3033A amplifiers is quite simple. Fig.3 shows typical phase-compensation characteristics for the CA3033; data for the CA3033A are similar. The two compensating capacitors C_x and C_y are connected from the collectors of the first differential amplifier (terminals 8 and 13) to ground. When capacitance values greater than 0.1 microfarad are used, however, a lower-voltage capacitor that has a value equal to half that given on the curves may be connected between terminals 8 and 13, and a 0.001-microfarad capacitor connected from either terminal 8 or 13 to ground. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of lower-voltage ceramic disc capacitors now available. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

The dashed lines in Fig.3 illustrate the use of the curves for design of a 60-dB amplifier. First, the intersection of the various gain-frequency curves is followed out to the curve for a capacitor value of 0.001 microfarad. At this point, the expected 3-dB amplifier response is approximately 230 kHz and the phase angle ϕ is 118 degrees; the phase margin ($180^o - \phi$) is thus 62 degrees. For a capacitance value of 300 picofarads, the expected 3-dB response is 580 kHz, but the phase angle is 175 degrees; the resulting phase margin of only 5 degrees is a most undesirable situation. In the other direction, the use of 0.003-microfarad compensating capacitors provides a 3-dB response of 90 kHz and a phase angle of approximately 90 degrees, with a phase margin of 90 degrees.

Slewing Rate

One of the most important considerations in using a high-power operational amplifier such as the CA3033 or CA3033A is the maximum full power output swing in terms of frequency that can be expected from the unit. This characteristic is important both in low-frequency applications and in pulse applications in which the rise times of a given design must be known. Fig.4 shows the maximum rate of change, or slewing rate, of a sine wave in volts per microsecond for various peak-to-peak output voltages.[1] For example, a 30-volt peak-to-peak sine wave at a frequency of 10 kHz has a maximum rate of change of 1 volt per microsecond. Besides being able to swing the value of 30 volts peak to peak at dc, therefore, an amplifier must also be able to swing this amplitude at a minimum rate of 1 volt per microsecond.

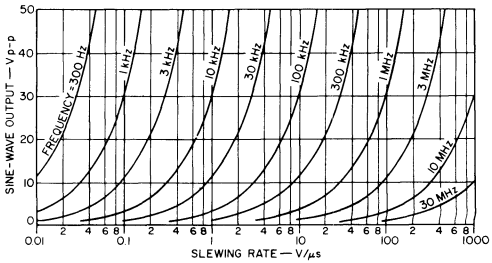


Fig.4 - Slewing-rate curve.

Slewing rate is a function of the phase-compensation circuit, the operational-amplifier design in terms of the gain after phase compensation, and the output-stage design. The phase-compensation circuit is usually placed around the input stages of an operational amplifier. This approach offers two advantages. First, it reduces the amplitude of any higher-frequency components that may overload the following stages. (For example, the residual rf carrier remaining on the output of a video detector with a single RC roll-off could cause serious overload and a distorted output if it were allowed to continue through the amplifier.) Second, because of the relatively high gain that follows the compensating circuit in the input stage, the compensating capacitors charge and discharge on a smaller and faster portion of the RC time constant associated with the collector load resistors and compensation capacitors.

Another consideration that influences the slewing rate is the signal-handling capability of the output stage. It is evident that, regardless of how fast the first portion of an amplifier responds to a step input, the output stage can limit the rate of rise and fall.

Fig.5 shows a curve of the maximum full-power-output frequency of the CA3033 and CA3033A as a function of the phase-compensation capacitance. This curve may be used with the curve of Fig.4 to determine the amplifier slewing rate. In the case of the 60-dB amplifier shown in Fig.6, for example, two 0.002-microfarad capacitors are used for phase compensation. The curves of Fig.3 indicate that the 3-dB bandwidth is 120 kHz.

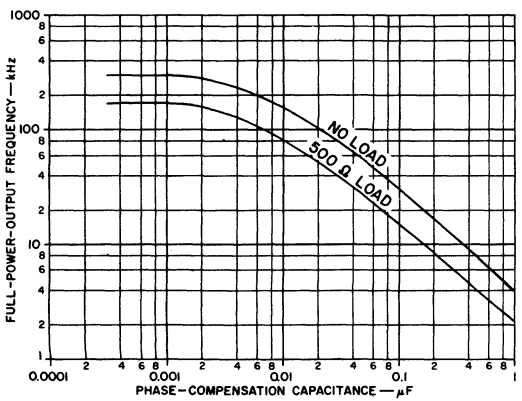


Fig.5 - Frequency for full power output as a function of phase-compensating capacitance.

Fig.5 shows that full output swing with no load may be expected up to a frequency of 280 kHz. Therefore, the design is capable of full power output up to the 3-dB point.

A similar approach may be used for a pulse amplifier. Two 0.01-microfarad phase-compensating capacitors are used to yield a 3-dB response of 30 kHz. The expected rise time in microseconds is equal to 0.35 divided by the 3-dB frequency in MHz, or 11.7 microseconds.[2] The power-output curve of Fig.5 shows that the maximum frequency for full power output is 155 kHz; thus the slewing rate is 10.6 volts per microsecond. For the 20-volt input-signal swing specified for the CA3033, the rise time based on this slewing rate would be (1 microsecond/10.6 volts) x 20 volts, or 1.9 microseconds. Because this value is greater than the rise time estimated from the 3-dB point, the design is not slewing-rate limited, and the 3-dB rise time will be met. Thus, for maximum high-frequency output, the lowest value of phase-compensation capacitors must be used; therefore, high closed-loop gains are implicit.

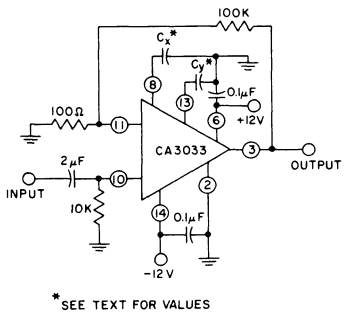


Fig.6 - 60-dB test amplifier for CA3033.

Waveforms for the 60-dB amplifier are shown in Fig.7.

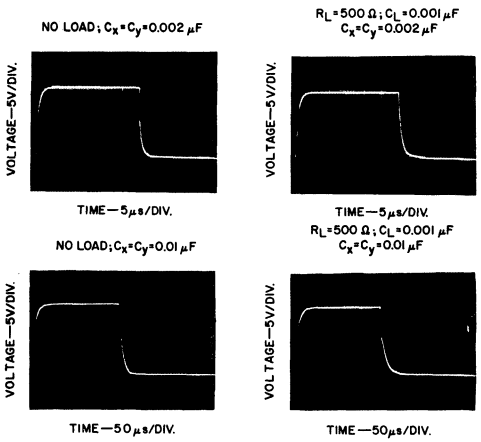


Fig.7 - Waveforms for the 60-dB amplifier shown in Fig.6.

Applications

Fig.8 illustrates the use of the CA3033A in a 20-dB, 255-milliwatt power amplifier operating from a single

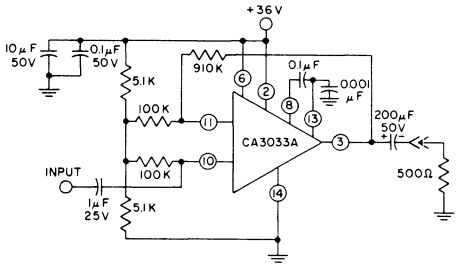


Fig.8 - 20-dB, 255-milliwatt power amplifier using a CA3033A operating from a 36-volt supply.

36-volt supply. Fig.9 shows the pulse response of this amplifier under no-load conditions and with a resistive load of 500 ohms; also shown are curves of distortion as a function of frequency. The waveforms show that the pulse response of the amplifier is limited by slewing rate rather than frequency response. Some crossover distortion is evident in the response for the 500-ohm load.

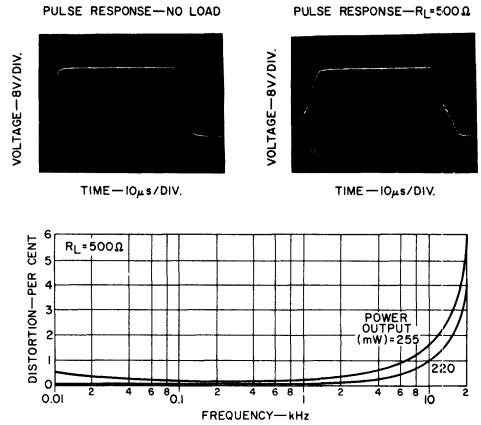


Fig.9 - Pulse-response waveforms and distortion curves for the amplifier shown in Fig.8.

The impedance of the feedback network can have a significant effect on the pulse response of a given amplifier design, particularly when higher-frequency performance is required. The response is influenced by the stray capacitance of the associated wiring, the shunt capacitance of the feedback resistors, and the input impedance of the operational amplifier. Because the CA3033 and CA3033A have higher input impedance as a result of the emitter-follower inputs, the input capacitive loading is reduced considerably and higher-impedance feedback networks can be used.

A simple system was fabricated to demonstrate the ease with which the CA3033 and CA3033A operational amplifiers may be applied. The basis of the system was the rudiments of a digital voltmeter, using the linear staircase approach, without the associated totalizing circuitry.

Fig.10 shows a block diagram of the system, together with the waveforms of all interfaces. A squelchable integrated-circuit multivibrator is used as the clock. As described later, the clock frequency is independent of supply voltage. Although this independence is not a necessary condition for circuit operation, it is inherent in this type of operational-amplifier multivibrator circuit and may be considered an integrated-circuit bonus.

The output from the clock drives a linear staircase generator. Input voltage to this circuit is applied directly from the multivibrator to minimize the effects of diode temperature coefficients. The output from the staircase generator is applied to a comparator that compares the staircase with the voltage to be measured.

The comparator output fires a monostable multivibrator that controls the display time, which is variable from about 100 milliseconds to one second. An inverter following the multivibrator supplies drive of the correct polarity to the integrator capacitor-discharge switch and the multivibrator squelch circuit.

Circuit operation begins with the staircase generator ramp running down until its voltage is equal to the unknown voltage on the input of the comparator. When the two voltages are equal, the monostable multivibrator is triggered by the output from the comparator. The output of the monostable multivibrator squelches the astable multivibrator and discharges the integrating capacitor through the bistable multivibrator. The wait, or display time, set by the monostable multivibrator allows sufficient time for full discharge of the integration capacitor and appears as a steady reading on the display device.

Astable Multivibrator - A schematic diagram of a squelchable multivibrator is shown in Fig.11. The only requirement that must be met by the squelch circuit is that the amplitude of the output pulse not change as a result of the squelch operation; otherwise, the amplitude of the final steps would be different from that of the initial steps and staircase linearity would suffer.

Freedom of the circuit from supply-voltage variations results from the excellent saturation characteristics of the integrated circuit at both positive and negative output swings. The positive and negative thresholds of the circuit are given by

$$\text{Positive threshold} = (V_{CC} - V_{CE+sat}) \frac{R_1}{R_1+R_2}$$

$$\text{Negative threshold} = (V_{EE} + V_{CE-sat}) \frac{R_1}{R_1+R_2}$$

where V_{CC} and V_{EE} are the positive and negative supply voltages and V_{CE+sat} and V_{CE-sat} are the positive and negative saturation voltages of the amplifier. Be-

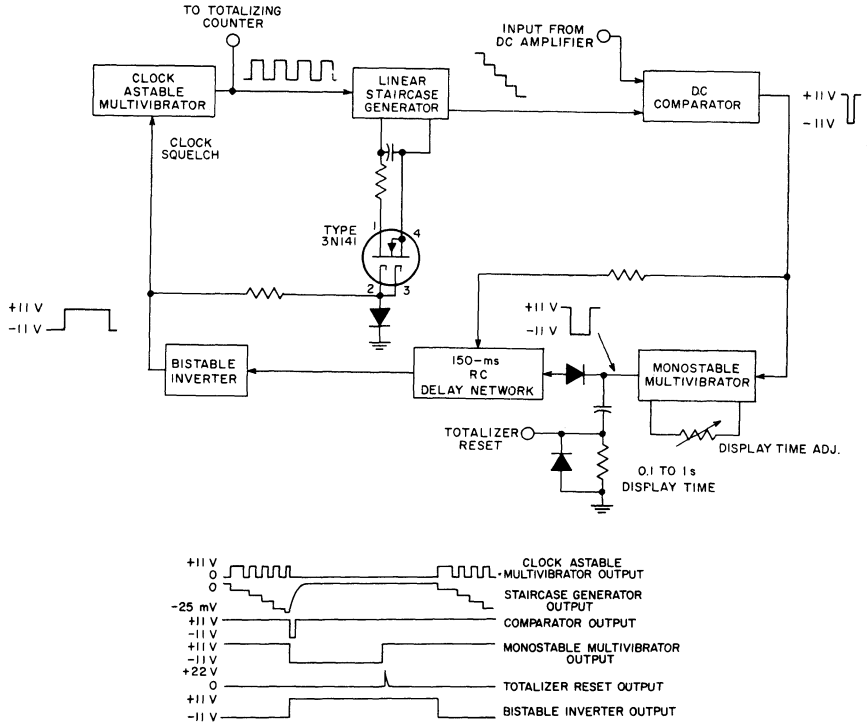


Fig.10 - Block diagram and waveforms of digital voltmeter system using five CA3033 integrated circuits.

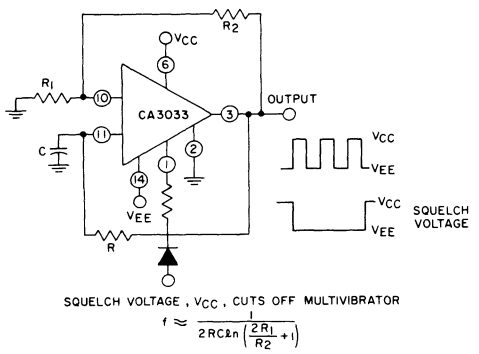


Fig.11 - CA3033 squelchable astable multivibrator.

cause these saturation voltages are low and have temperature coefficients less than 5 millivolts per degree C, they can be neglected for ease of computation. If the charging current is considerably greater than the base current, the frequency f may be expressed as follows:[3]

$$f \approx \frac{1}{2\,RC\,\ln\left(\frac{2R_1}{R_2}+1\right)}$$

Linear Staircase Generator - The design of a linear staircase generator is nearly identical to that of a linear ramp or sawtooth generator. Fig.12(a) shows a linear ramp generator in which the non-inverting input of an operational amplifier is grounded and a switch S_1 returns the output to the inverting input. When S_1 is closed, the amplifier is in the unity-gain configuration and the output is at ground less the input offset voltage. When S_1 is opened, the output moves in the positive direction when the reference voltage V_{ref} is negative, or in the negative direction when V_{ref} is positive. Because the output under closed-loop conditions tries to maintain the input terminal at zero voltage, the charging current to the capacitor is constant at a rate of $dV/dt = i/C$,

where $i = V_{ref}/R$. It is apparent that this analysis is valid as long as the input current to the first stage is considerably less than the charging current.

Fig. 12(b) shows the circuit for a linear staircase generator. In this circuit, a pulse of amplitude e couples a charge Q to the amplifier input. The charge Q is equal to $C_1 (e - 2V_{ak})$, where $2V_{ak}$ is the forward voltage drop across the two diodes. Again, if the amplifier input current is small compared to the effective charging current, capacitor C_2 is incrementally charged in steps of $(e - 2V_{ak}) C_1/C_2$. If the pulse height is made sufficiently large compared to the expected temperature variations of the diodes, a reasonable degree of temperature independence results.

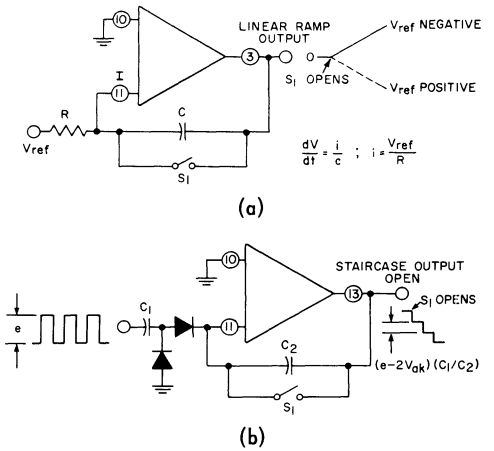


Fig. 12 - Diagrams of (a) linear ramp generator and (b) linear staircase generator.

Comparator - Regeneration is added around the comparator circuit in this system to accelerate the transition time when the two input voltages are equal. Fig. 13 shows a complete schematic diagram of the entire system. Waveforms at critical points are shown in Fig. 14. The 470-picofarad capacitor and 1000-ohm resistor between terminals 3 and 10 of the CA3033 in the comparator circuit provide the regeneration. Two 0.001-microfarad capacitors on each input filter any externally generated noise.

Monostable Multivibrator - The monostable multivibrator circuit shown in Fig. 13 makes use of the extremely low input bias currents of the CA3033 by using small timing capacitors and large timing resistors to obtain the long (one-second) display time. The small timing capacitor in conjunction with the diode D_3 permits the fast recycling time necessary for the one-step case. Triggering of the circuit is accomplished by the 470-picofarad capacitor to the non-inverting input (terminal 10).

An RC timing network is incorporated at the output of the monostable multivibrator to add an additional 150-millisecond delay tha. performs two functions. First, the added delay allows more time to complete the timing-capacitor recycling mentioned above. The second and more important function of this network is the generation of a reset pulse at the trailing edge of the monostable multivibrator. Diode D_4 couples the negative output of the multivibrator to the next stage and rapidly charges the 0.22-microfarad network timing capacitor through the 470-ohm resistor. After the monostable multivibrator completes the cycle, diode D_4 disconnects, and the 0.22-microfarad capacitor charges to the 1.1-volt switching threshold of the next stage through the two one-megohm resistors. This cycle is approximately 150 milliseconds.

Bistable Multivibrator - The output from the monostable multivibrator is coupled to the next stage, a bistable multivibrator or inverter. The switching thresholds are determined by the 100,000- and 10,000-ohm resistors in the positive feedback loop. The primary function of this stage is to invert the signals from both the comparator and the monostable multivibrator to drive the clock-astable-multivibrator squelch circuit and the staircase capacitor-discharge switch, an RCA-3N141 dual-gate MOS field-effect transistor. Diode D_6 protects the gates of the MOS transistor; the 47-picofarad capacitor reduces the rise time of the negative-going output of the bistable multivibrator and prevents it from coupling into the beginning of staircase and obscuring the first few steps by this negative transition.

Acknowledgment

The author thanks A. J. Leidich for his work on the design of the CA3033 and CA3033A and for supplying the noise-figure curve, and J. Klinger for breadboarding and evaluating the many circuits used in the paper.

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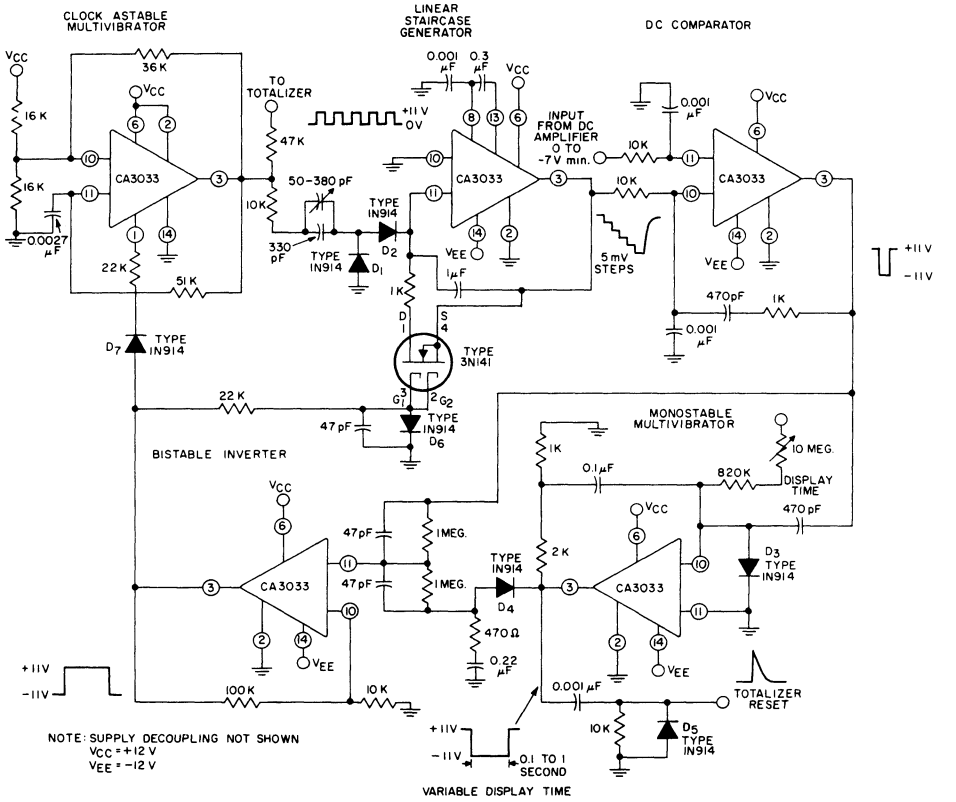


Fig.13 - Schematic diagram of a digital voltmeter using CA3033 integrated circuits.

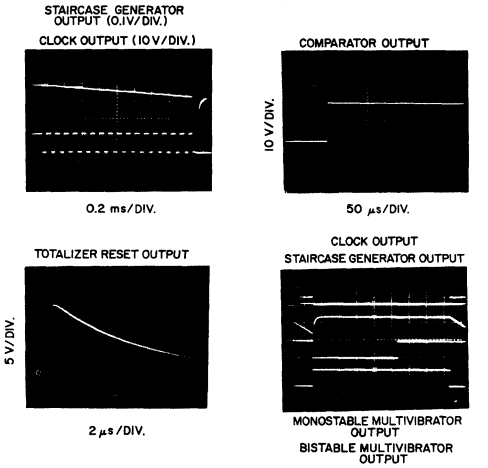


Fig.14 - Waveforms for the digital voltmeter shown in Fig.13.

Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

by H. A. Wittlinger

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply. (Transconductance $g_m = \frac{\triangle i_{out}}{\triangle e_{in}}$). The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with RCA COS/MOS devices as post-amplifiers.

Fig. 1 shows the equivalent circuit for the OTA. The output signal is a "current" which is proportional to the transconductance (gm) of the OTA established by the amplifier bias current (I_{ABC}) and the differential input voltage. The OTA can either source or sink current at the output terminals, depending on the polarity of the input signal.

The availability of the amplifier bias current (I_{ABC}) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

Circuit Description

A simplified block diagram of the OTA is shown in Fig. 2. Transistors Q1 and Q2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Fig. 3a shows the basic type of current-mirror which is comprised of two transistors, one of which is diode-connected. In a "current-mirror", with similar geometries for Q_A and Q_B, the current I' establishes a second current I whose value is essentially equal to that of I'.

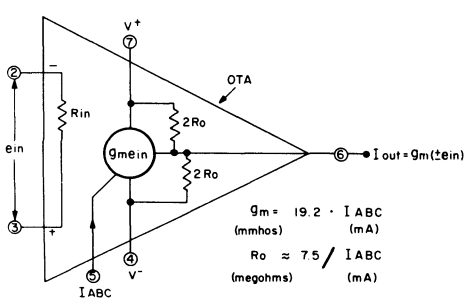


Fig. 1— Basic equivalent circuit of the OTA.

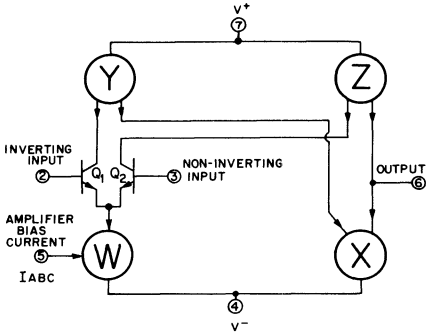


Fig. 2— Simplified diagram of OTA.

This basic current-mirror configuration is sensitive to the transistor beta (β). The addition of another active transistor, shown in Fig. 3b, greatly diminishes the circuit sensitivity to transistor beta (β) and increases the current-source output impedance in direct proportion to the transistor beta (β). Current-mirror W (Fig. 2) uses the configuration shown in Fig. 3a, while mirrors X, Y, and Z are basically the version shown in Fig. 3b. Mirrors Y and Z employ p-n-p transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes "current-mirrors" in more detail.

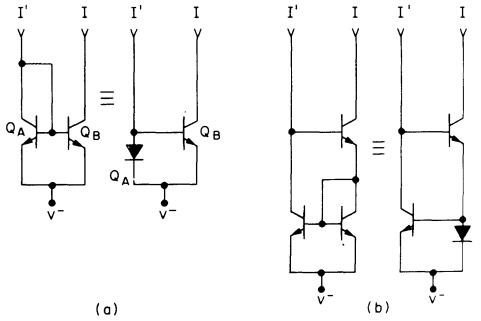


Fig. 3– Basic types of current mirrors; a) diode-connected transistor paired with transistor; b) improved version: employs an extra transistor.

Fig. 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, I_{ABC}, establishes the emitter current of the input differential amplifier Q1 and Q2. Hence, effective control of the differential transconductance (g_m) is achieved.

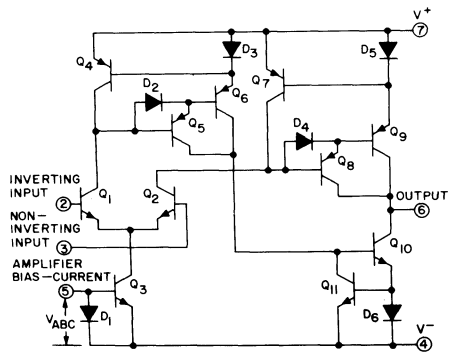


Fig. 4– Schematic diagram of OTA types CA3080 and CA3080A.

The g_m of a differential amplifier is equal to

$$\frac{qaI_C}{2KT}$$

(see Ref. 2 for derivation) where q is the charge on an electron, a is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), I_C is the collector current of the constant-current source (I_{ABC} in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_m = 19.2 \times I_{ABC}$, where gm is in mmho and I_{ABC} is in milliamperes. The temperature coefficient of g_m is approximately -0.33%/°C (at room temperature).

Transistor Q3 and diode D1 (shown in Fig. 4) comprise the current mirror "W" of Fig. 2. Similarly, transistors Q7, Q8 and Q9 and diode D5 of Fig. 4 comprise the generic current mirror "Z" of Fig. 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q10, Q11, and diode D6 of Fig. 2 comprise the current-mirror "X" of Fig. 2. Diodes D2 and D4 are connected across the base-emitter junctions of Q5 and Q8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the

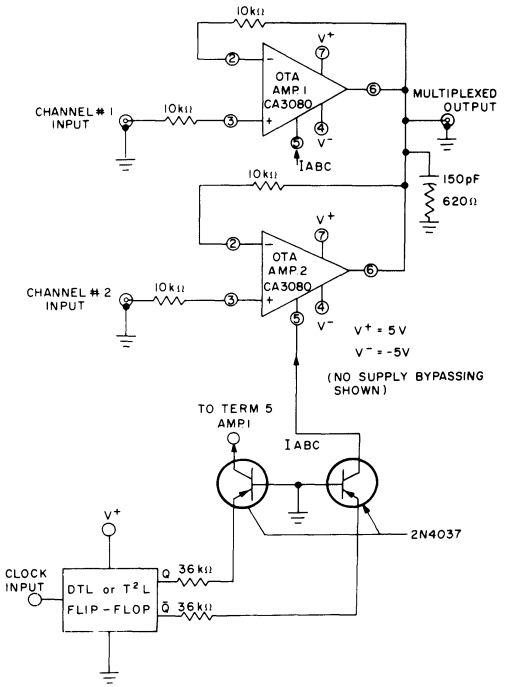


Fig. 5– Schematic diagram of OTAs in a two-channel linear time-shared multiplex circuit.

"Z" and "X" current-mirror of Fig. 2, providing a push-pull Class A output stage that produces full differential g_m. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of g_m and input offset voltage, less variation of input offset voltage with variation of I_{ABC} and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000 MΩ.

APPLICATIONS

Multiplexing

The availability of the bias current terminal, I_{ABC}, allows the device to be gated for multiplex applications. Fig. 5 shows a simple two-channel multiplex system using two CA3080 OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is low. To further increase the gain and reduce the effects of loading, an additional buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example positive and negative 5-V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15 V, with the positive-supply at 5 V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through p-n-p transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base configuration is used to minimize capacitive feed-through coupling via the base-collector junction of the p-n-p transistor.

Another multiplex system using the OTA's clocked by a COS/MOS flip-flop is shown in Fig. 6. The high output voltage capability of the COS/MOS flip-flop permits the circuit to be driven directly without the need for p-n-p level-shifting transistors.

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figs. 5 & 6. The values of the RC-network are chosen so that $\frac{1}{2\pi RC} \simeq 2\text{MHz}$. This RC-network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Fig. 7 shows an oscilloscope photograph of the multiplex circuit functioning with two input signals. Fig. 8 shows an oscilloscope photograph of the output of the multiplexer with a 6-V p-p, sine wave signal (22 kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80 dB between channels.

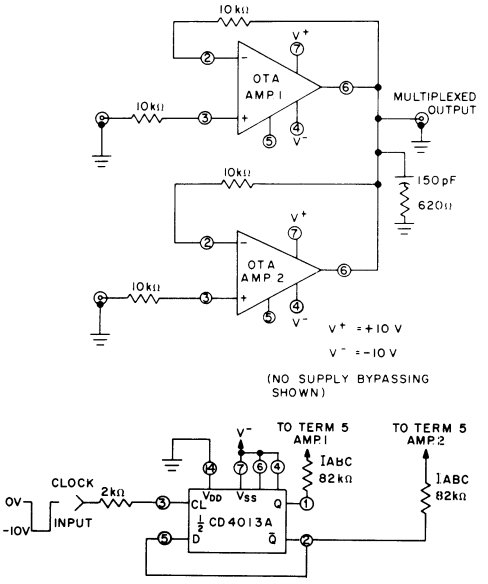
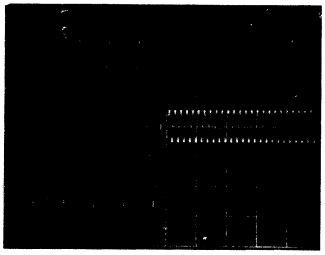
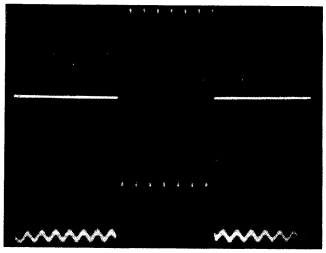


Fig. 6— Schematic diagram of a two-channel linear multiplex system using a COS/MOS flip-flop to gate two OTAs.



TOP TRACE: MULTIPLEXED OUTPUT 1 V/DIV & 100μsec/DIV
BOTTOM TRACE: TIME EXPANSION OF SWITCHING BETWEEN INPUTS 2 V/DIV & 5 μsec/DIV

Fig. 7— Voltage waveforms for circuit of Fig. 6; top trace: multiplexed output; lower trace: time expansion of switching between inputs.



TOP TRACE: 1 V/DIV & 100μsec/DIV —OUTPUT
BOTTOM TRACE: VOLTAGE EXPANSION OF OUTPUT 1mV/DIV & 100μsec/DIV ISOLATION IS IN EXCESS OF 80 db

Fig. 8— Voltage waveforms for circuit of Fig. 6; top trace: output; lower trace: voltage expansion of output; isolation in excess of 80 dB.

Sample-and-Hold Circuits

An extension of the multiplex system application is a sample-and-hold circuit (Fig. 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Fig. 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000 MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of an RCA 3N138 insulated-gate field-effect transistor (MOS/FET) in the feedback loop. This transistor has a maximum gate-leakage current of 10 picoamperes; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Fig. 9) is approximately 100 dB if the MOS/FET is used in the source-follower mode to the CA3080A as the input amplifier. The open-loop output impedance ($\frac{1}{g_m}$) of the 3N138 is approximately 220 Ω because its transconductance is about 4,600 μmho at an operating current of 5 mA. When the CA3080A drives the 3N138 (Fig. 9), the closed loop operational-amplifier output impedance characteristic

$$Z_{out} \cong \frac{Z_O \text{ (open-loop)}}{A \text{ (open-loop voltage-gain)}}$$

$$\cong \frac{220\ \Omega}{100\text{dB}} \cong \frac{220\ \Omega}{10^5} \cong 0.0022\ \Omega$$

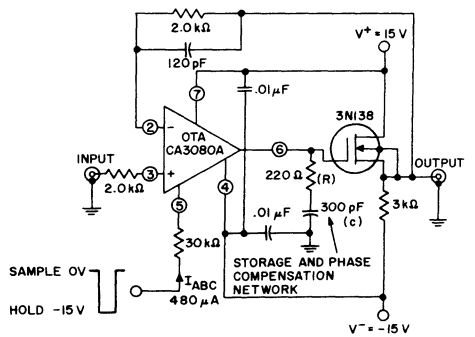
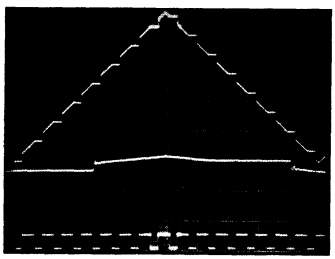


Fig. 9– Schematic diagram of OTA in a sample-and-hold circuit.

Fig. 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular wave-form. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2 μsec/div.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5 ηA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Fig. 11 shows the expected pulse "tilt" in microvolts as a function of time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50 ηA, 5 ηA, 500 pA.

Fig. 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14 ms with a 300 pF storage capacitor. The center trace (expanded to 20 mV/div) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170 pA ($I = C\frac{dv}{dt}$).



TOP TRACE:SAMPLED SIGNAL 1V/DIV & 20μsec/DIV
CENTER TRACE:TOP PORTION OF UPPER SIGNAL
1 V/DIV & 2μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 20μsec/DIV

Fig. 10– Waveforms for circuit of Fig. 9; top trace: sampled signal; center trace: top portion of upper signal; lower trace: sampling signal.

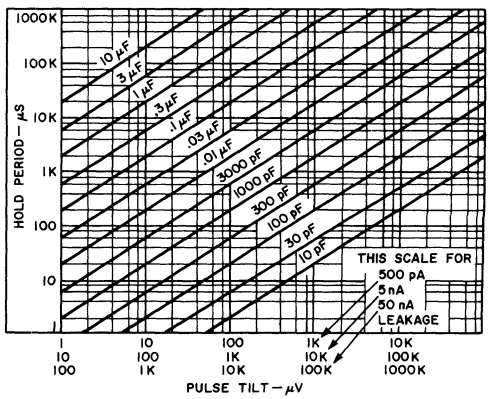
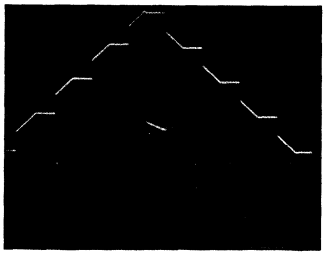


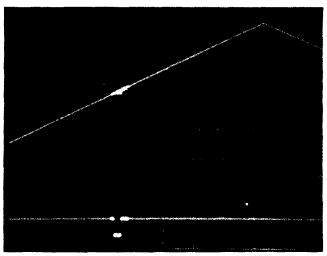
Fig. 11– Chart showing "tilt" in sample-and-hold potentials as a function of hold time with load capacitance as a parameter.

Fig. 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Fig. 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Fig. 13 were recorded with supply voltages of ±10 V and the series input resistor at terminal 5 was 22 kΩ.



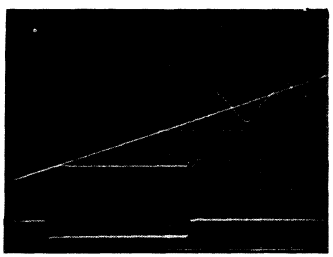
TOP TRACE:SAMPLED SIGNAL 1V/DIV & 20msec/DIV
CENTER TRACE:WORSE CASE TILT 20mV/DIV & 20msec/DIV

Fig. 12– Oscilloscope photo of "triangular-voltage" being sampled by circuit of Fig. 9.



TOP TRACE:INPUT AND OUTPUT SUPERIMPOSED 1V/DIV & 2μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 2μsec/DIV

Fig. 13– Oscilloscope photo of "ramp-voltage" being sampled by circuit of Fig. 9.



TOP TRACE:INPUT AND SAMPLED OUTPUT SUPER-IMPOSED 100mV/DIV & 100μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 100μsec/DIV

Fig. 14– Oscilloscope photo showing response of sample-and-hold circuit (Fig. 9).

In Fig. 14, the trace of Fig. 13 has been expanded (100 mV/div and 100 ηsec/div) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1 μs. The resistor in series with the 300 pF phase-compensation capacitor was adjusted to 68 ohms for minimum recovery time.

Fig. 15 shows the basic circuit of Fig. 9 implemented with an RCA 2N4037 p-n-p transistor to minimize capacitive feedthrough. Fig. 16 shows oscilloscope photographs taken with the circuit of Fig. 15 operating in the sampling mode at supply-voltage of ±15 V. The 9.1 kΩ resistor in series with the p-n-p transistor emitter establishes amplifier-bias-current (I_{ABC}) conditions similar to those used in the circuit of Fig. 9.

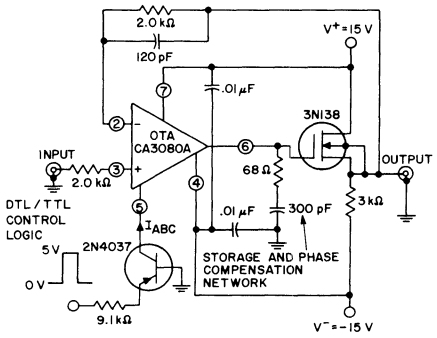
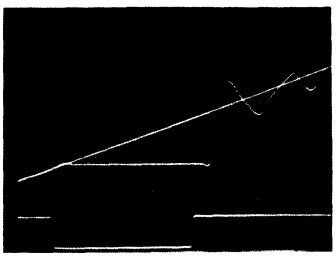


Fig. 15– Schematic diagram of the OTA in a sample-and-hold configuration (DTL/TTL control logic).

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $\frac{1}{2\pi RC} \simeq 2\text{MHz}$, corresponding to the first pole in the



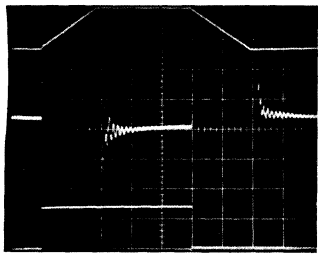
TOP TRACE:INPUT AND SAMPLED OUTPUT SUPER-IMPOSED 100mV/DIV & 100μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 5V/DIV & 100μsec/DIV

Fig. 16– Oscilloscope photo for circuit of Fig. 15 operating in sampling mode.

amplifier at an output current level of 500 μA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figs. 9 and 15. The 120 pF capacitor shunting the 2 kΩ resistor improves the amplifier transient response.

Fig. 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Fig. 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dV/dt) = 1.8V/μs.

The center trace in Fig. 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2 mV/div. The output of the amplifier system settles to within 2 mV (the offset voltage specification for the CA3080A) of the input level in 1 μs after slewing.



TOP TRACE: OUTPUT 5V/DIV @ 2μsec/DIV
CENTER TRACE: DIFFERENTIAL COMPARSION OF INPUT AND OUTPUT 2mV/DIV— 0 VOLTS THROUGH CENTER— 2 μsec/DIV
BOTTOM TRACE: INPUT 5V/DIV @ 2μsec/DIV

Fig. 17— Oscilloscope photo showing circuit of Fig. 9 operating in the linear sample-mode.

Fig. 18 is a curve of slew-rate as a function of amplifier-bias-current (I_{ABC}) with various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current (I_{ABC}) when the OTA is supplying its maximum output current.

Gain Control — Amplitude Modulation

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current (I_{ABC}) in the OTA because its g_m is directly proportional to the amplifier-bias-current (I_{ABC}). For a specified value of amplifier-bias-current, the output current (I_O) is equal to the product of g_m and the input signal magnitude. The output voltage swing is the product of output current (I_O) and the load resistance (R_L).

Fig. 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current (I_O) is equal to $-g_m V_x$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, I_{ABC}. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current (I_{ABC}) through resistor Rm. Amplitude modulation of the carrier frequency occurs because variation of the voltage Vm forces a change in the amplifier-bias-current (I_{ABC}) supplied via resistor Rm. When Vm goes positive the bias current increases which causes a corresponding increase in the g_m of the OTA. When the Vm goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the g_m of the OTA.

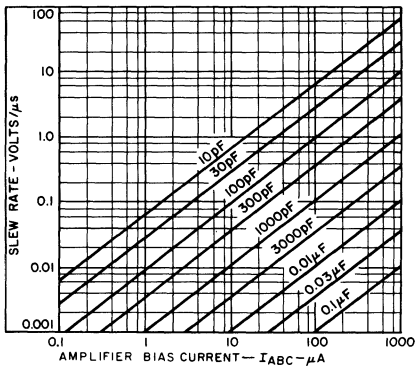


Fig. 18— Slew rate as a function of amplifier-bias-current (I_{ABC}) with phase-compensation capacitance as a parameter.

As discussed earlier, $g_m = 19.2 \times I_{ABC}$, where g_m is in millimhos when I_{ABC} is in milliamperes. In this case, I_{ABC} is approximately equal to:

$$\frac{Vm - (V^-)}{Rm} = I_{ABC}$$

$$(I_O) = -g_m Vx$$

$$g_m Vx = (19.2)(I_{ABC})(Vx)$$

$$I_O = \frac{-19.2\,[Vm - (V^-)]\,Vx}{Rm}$$

$$I_O = \frac{19.2\,(Vx)(V^-)}{Rm} - \frac{19.2\,(Vx)(Vm)}{Rm}$$ (Modulation Equation).

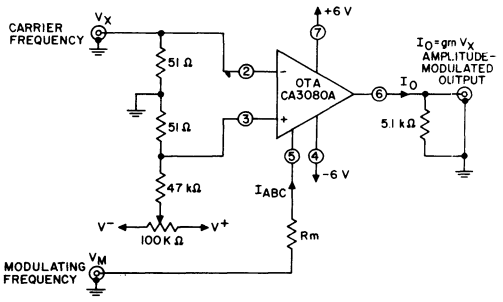


Fig. 19– Amplitude modulator circuit using the OTA.

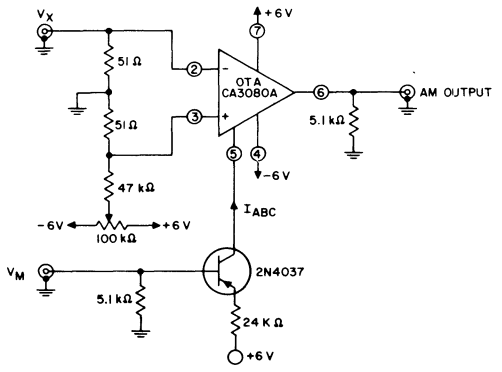


Fig. 20– Amplitude modulator using OTA controlled by p-n-p transistor.

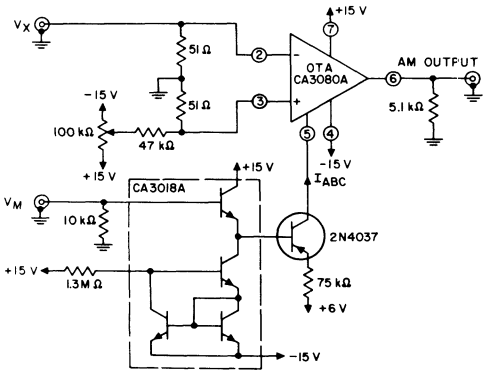


Fig. 21– Amplitude modulator using OTA controlled by p-n-p and n-p-n transistors.

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of Vm, and the second term represents the modulation, which either adds to or subtracts from the first term. When Vm is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term

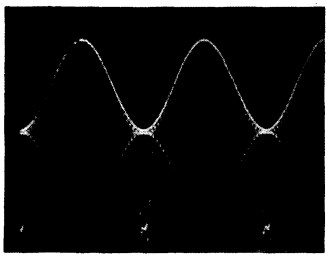
$$(19.2)\,(Vx)\ \frac{V_{ABC}}{Rm}$$

involving the amplifier-bias-current terminal voltage (V_{ABC}) (see Fig. 4 for V_{ABC}) was neglected. This term was assumed to be small because V_{ABC} is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a p-n-p transistor), the effect of V_{ABC} variation is eliminated and transferred to the involvement of the p-n-p transistor base-emitter junction characteristics. Fig. 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation. If an n-p-n transistor is added to the circuit of Fig. 20 as an emitter-follower to drive the p-n-p transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the n-p-n base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Fig. 21 shows a configuration using one transistor in the RCA type CA3018A n-p-n transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter – followers. The 100-kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figs. 22a and 22b show oscilloscope photographs of the output voltages obtained when the circuit of Fig. 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Fig. 22c shows the excellent isolation achieved in this modulator during the "gated-off" condition.

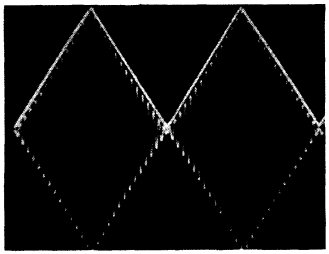
Four-Quadrant Multipliers

A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Fig. 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Fig. 19).

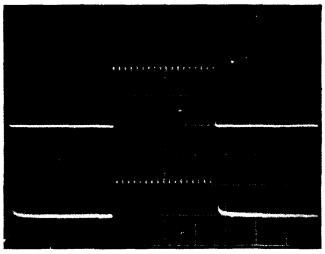
To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_m$. The output current is $I_O = g_m\,(-Vx)$ because the input is applied to the



TOP TRACE: MODULATION FREQUENCY INPUT
≈20 VOLTS P-P & 50μsec/DIV
CENTER TRACE: AMPLITUDE MODULATE OUTPUT
500mV/DIV & 50μsec/DIV
BOTTOM TRACE: EXPANDED OUTPUT TO SHOW
DEPTH OF MODULATION 20mV/DIV
& 50μsec/DIV



TOP TRACE: MODULATION FREQUENCY INPUT
20 VOLTS & 50μsec/DIV
BOTTOM TRACE: AMPLITUDE MODULATED OUTPUT
500mV/DIV & 50μsec/DIV



TOP TRACE: GATED OUTPUT 1V/DIV AND 50μsec/DIV
BOTTOM TRACE: VOLTAGE EXPANSION OF ABOVE
SIGNAL-SHOWING NO RESIDUAL
1mV/DIV AND 50μsec/DIV— AT
LEAST 80 db OF ISOLATION
fq = 100 kHz

Fig. 22— a) Oscilloscope photo of amplitude modulator circuit of Fig. 19 with R_m = 40 kΩ, V^+ = 10 v and V- = -10 V. Top trace: modulation frequency input ≃ 20-V p-p; center trace: amplitude modulated output 500-mV/div.; lower trace: expanded output to show depth of modulation, 20 mV/div.; b) triangular modulation; top trace: modulation frequency input ≃ 20 V; lower trace: amplitude modulated output 500 mV/div.; c) square wave modulation, top trace: gated output 1 V/div.; lower trace: expanded scale, showing no residual (1 mV/div) and at least 80 dB of isolation at fq = 100 kHz.

inverting terminal of the OTA. The output current due to the resistor (R) is $\frac{Vx}{R}$. Hence, the two signals cancel when R = $1/g_m$. The current for this configuration is:

$$I_O = \frac{-19.2\ Vx\ Vm,}{Rm} \text{ and } Vm = Vy$$

The output signal for these configurations is a "current" which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter shown in Fig. 24.

In Fig. 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10 mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).

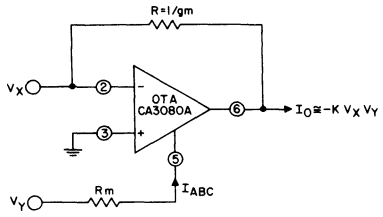


Fig. 23— Basic four quadrant analog multiplier using an OTA.

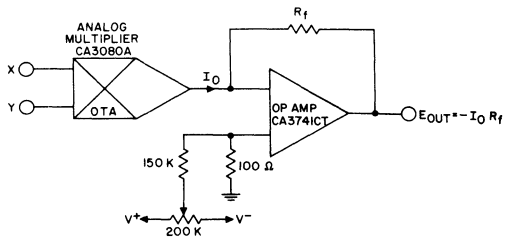


Fig. 24— OTA analog multiplier driving an op-amp that operates as a current-to-voltage converter.

Fig. 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent "full-scale". There are only three adjustments: 1) one is on the output, to

compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20-kΩ potentiometer establishes the g_m of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

Procedure for adjustment of the circuit:

1. a) Set the 1 MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100 kΩ potentiometer until a zero-V reading is obtained at the output.

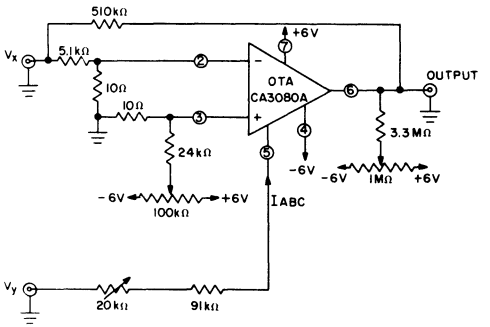


Fig. 25– Schematic diagram of analog multiplier using OTA.

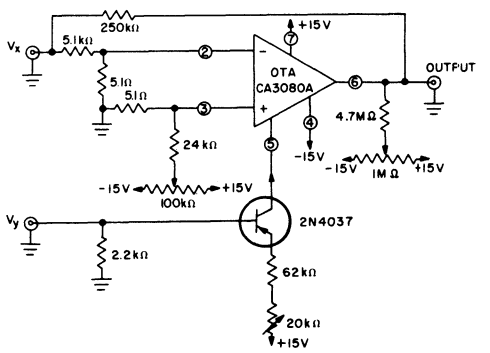
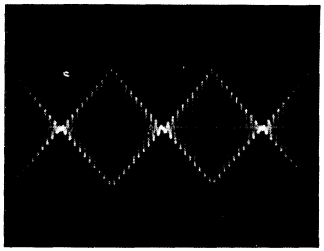
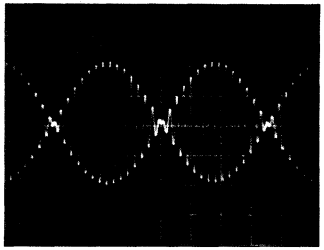


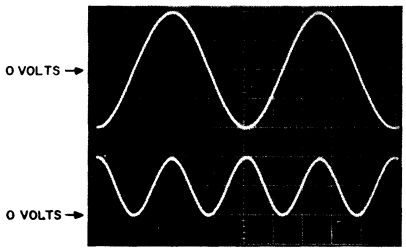
Fig. 26– Schematic diagram of analog multiplier using OTA controlled by a p-n-p transistor.



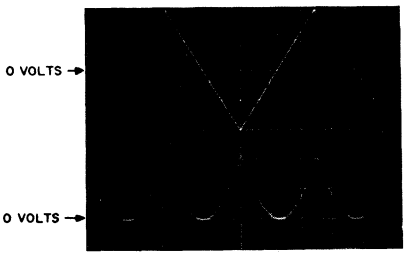
500 mV/DIV AND 200 μsec/DIV
TRIANGLAR INPUT 700 Hz TO V_Y INPUT 5 VPP
CARRIER INPUT 21 kHz TO V_X INPUT 13.5 VPP



500 mV/DIV AND 200μsec/DIV
MODULATING FREQUENCY 700 Hz TO V_Y INPUT 5 VPP
CARRIER INPUT 21 kHz TO V_X INPUT 13.5 VPP



TOP TRACE: INPUT TO X AND Y 2 V/DIV AND
1 msec/DIV – 200 Hz
BOTTOM TRACE: OUTPUT 500 mV/DIV AND
1 msec/DIV – 400 Hz



SAME SCALE AS 27C

Fig. 27– a) Waveforms observed with OTA analog multiplier used as a suppressed carrier generator; b) waveforms observed with OTA analog multiplier used in signal-squaring circuits.

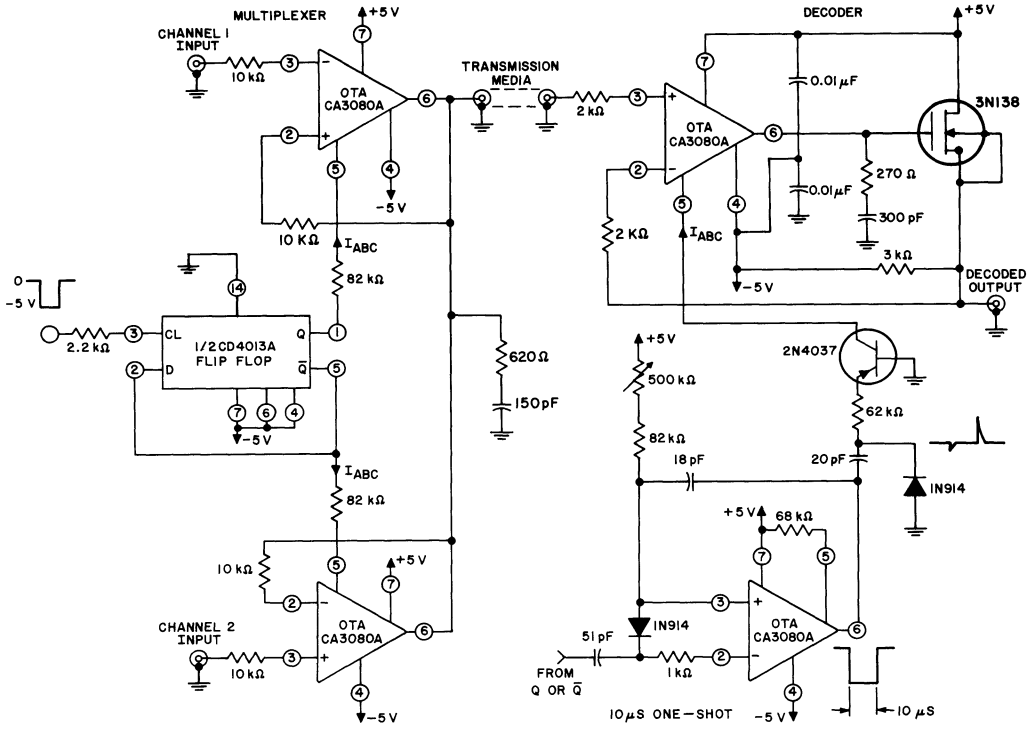


Fig. 28– Two-channel multiplexer and decoder using OTAs.

2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator. (It is essential that a low impedance source be used; this minimizes any change in the g_m balance or zero-point due to the 50-μA Y-input bias current).
   b) Adjust the 20-kΩ potentiometer in series with Y-input until a reading of zero-V is obtained at the output. This adjustment establishes the g_m of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510-kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1-MΩ resistor for an output voltage of zero-V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

Fig. 26 shows the schematic of an analog multiplier circuit with a 2N4037 p-n-p transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the p-n-p transistor. The addition of another emitter-follower preceding the p-n-p transistor (shown in Fig. 21) will further increase the current gain while markedly reducing the effect of the V_{be} temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

Figs. 27a and 27b show oscilloscope photographs of the output signals delivered by the circuit of Fig. 26 which is connected as a suppressed-carrier generator. Figs. 27c and 27d contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular-wave inputs.

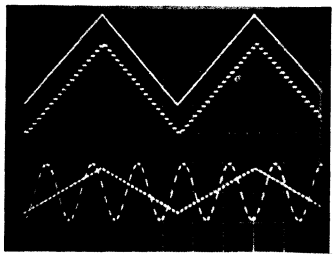
If ±15-V power supplies are used (shown in Fig. 26), both inputs can accept ±10-V input signals. Adjustment of this multiplier circuit is similar to that already described above.

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

Other forms of four-quadrant multipliers using operational transconductance amplifiers have been published. (See Ref. 2.) the circuit shown in Ref. 2 tends to reduce the effects of the previously discussed g_m temperature dependency.

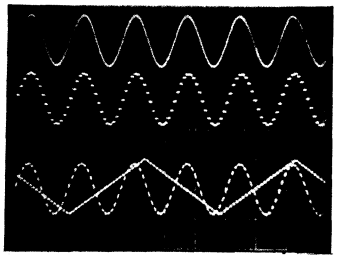
Linear Multiplexer – Decoder

A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Fig. 28. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Fig. 29 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10 μsec delay- "one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-



20 msec/DIV

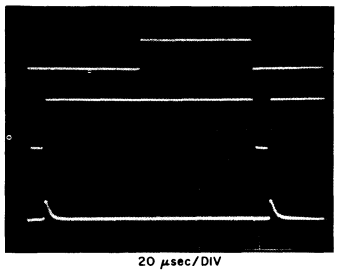
TOP TRACE: INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (2 VOLTS/DIV)



20 msec/DIV

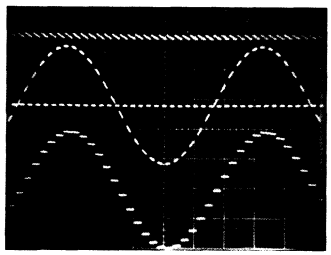
TOP TRACE: INPUT SIGNAL (1VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (1VOLT/DIV)

Fig. 29– Waveforms showing operation of linear multiplexer/sample-and-hold decode circuitry (Fig. 28).

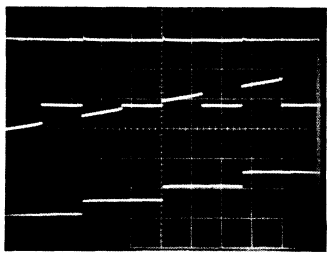


20 μsec/DIV

TOP TRACE: FLIP-FLOP OUTPUT (5 VOLTS/DIV)
CENTER TRACE: "ONE-SHOT" OUTPUT (5 VOLTS/DIV)
BOTTOM TRACE: PULSE AT THE COLLECTOR OF THE 2N4037 TRANSISTOR (0.1 VOLTS/DIV)



TOP TRACE: COLLECTOR OF PNP TRANSISTOR (0.5 V/DIV)
CENTER TRACE: MULTIPLEXED OUTPUT WITH ONE CHANNEL INPUT GROUND (0.5V/DIV)
LOWER TRACE: DECODED OUTPUT (0.5 V/DIV)
TIME ALL SCALES: 5 msec / DIV



TIME EXPANSION TO 500μsec/DIV

Fig. 30– (a) Waveforms showing timing of flip-flop, delay– "one-shot" and the strobing pulse to the sample-and-hold circuit (Fig. 28): top trace: flip-flop output (5 V/div); center trace: "one-shot" output (5 V/div); lower trace: pulse at collector of 2N4037 transistor (0.1 V/div); b) Waveforms showing the decoding operation from the decoder keying pulse (top traces) to the recovered "decoded" sampled output (lower traces). 1) top trace: collector of 2N4037; center trace: multiplexed output with one channel input grounded; lower trace: decoded output; 2) Expanded scale of (1).

hold circuit for approximately 1 μs. Fig. 30 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10 μsec "one-shot" to decode a signal.

High-Gain, High-Current Output Stages

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOS/FET) shown in Fig. 9. This configuration yields a voltage gain equal to the (g_m) (R_O) product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Fig. 9) are limited by the 3N138 MOS/FET performance and its source-terminal load. In the positive direction, the MOS/FET may be driven into saturation; the source-load resistance and the MOS/FET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOS/FET shown in Fig. 9.

Another variation of this generic form of amplifier utilizes the RCA CD4007A (COS/MOS) "inverter" as an amplifier driven by the CA3080. Each of the three "inverter"/amplifiers in the CD4007A has a typical voltage gain of 30 dB. The gain of a single COS/MOS "inverter"/amplifier coupled with the 100 dB gain of the CA3080 yields a total forward-gain of about 130 dB. Use of a two-stage COS/MOS amplifier configuration will increase the total open-loop gain of the system to about 160 dB (100,000,000). Figs. 31 through 34 show examples of these configurations. Each COS/MOS "inverter"/amplifier can sink or source a current of 6 mA (typ.). In Figs. 33 and 34, two COS/MOS "inverter"/amplifiers have been connected in parallel to provide additional output current.

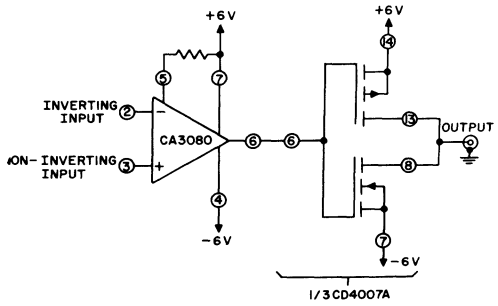


Fig. 31– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (open-loop mode). For greater current output the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown. Open-loop gain ≃ 130 dB.

The open-loop slew-rate of the circuit in Fig. 31 is approximately 65 V/μsec. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1 V/μsec (shown in Fig. 32). Even when the three "inverter"/amplifiers in the CD4007A are connected as shown in Fig. 33, the open-loop slew-rate remains at 65 V/μsec. A slew-rate of about 1 V/μsec is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 34. Fig. 35 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figs. 32 and 34. These photos illustrate the inherent stability of the OTA and COS/MOS circuits operating in concert.

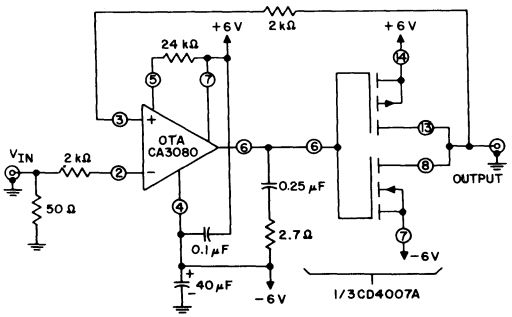


Fig. 32– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (unity-gain closed-loop mode). For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown.

Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A COS/MOS "inverter"/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figs. 31, 32, 33, and 34, for example, power-supply current drawn by the COS/MOS "inverter"/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

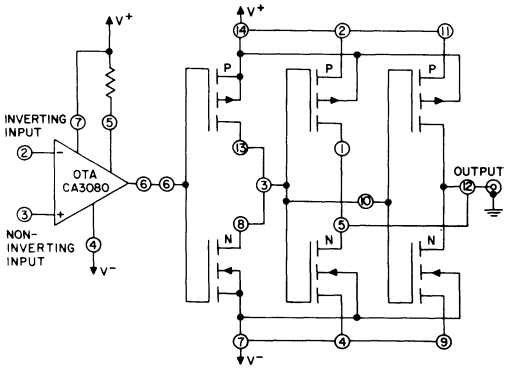


Fig. 33– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (open-loop mode). gain ≃ 160 dB.

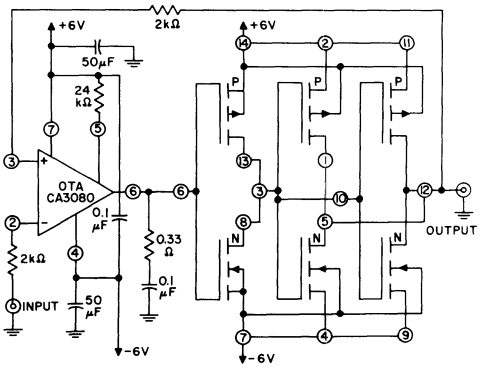
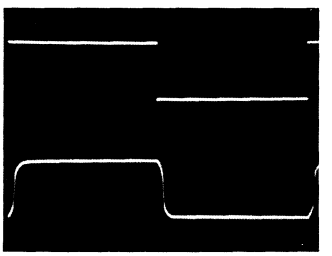


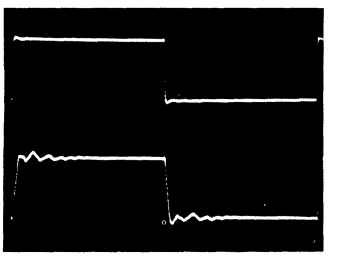
Fig. 34– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (unity gain closed-loop mode).

(a)



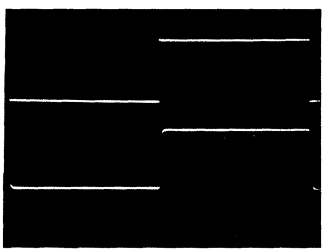
TOP TRACE: INPUT-5 V/DIV-100 μsec/DIV
BOTTOM TRACE: OUTPUT SAME SCALE

(b)



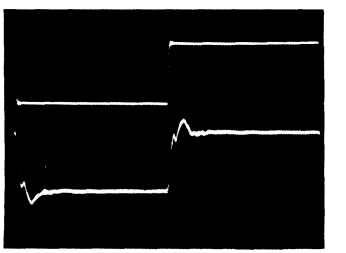
TOP TRACE: INPUT-50 mV/DIV-1 μsec/DIV
BOTTOM TRACE: OUTPUT-SAME SCALE

(c)



TOP TRACE: INPUT-5 V/DIV-100 μsec/DIV
BOTTOM TRACE: OUTPUT-SAME SCALE

(d)



TOP TRACE: INPUT-50 mV/DIV-1 μsec/DIV
BOTTOM TRACE: OUTPUT-SAME SCALE

Fig. 35– a) Waveforms for circuit of Fig. 32 with large signal input; b) Waveforms for circuit of Fig. 32 with small signal input; c) Waveforms for circuit of Fig. 34 with large signal input; d) Waveforms for circuit of Fig. 34 with small signal input.

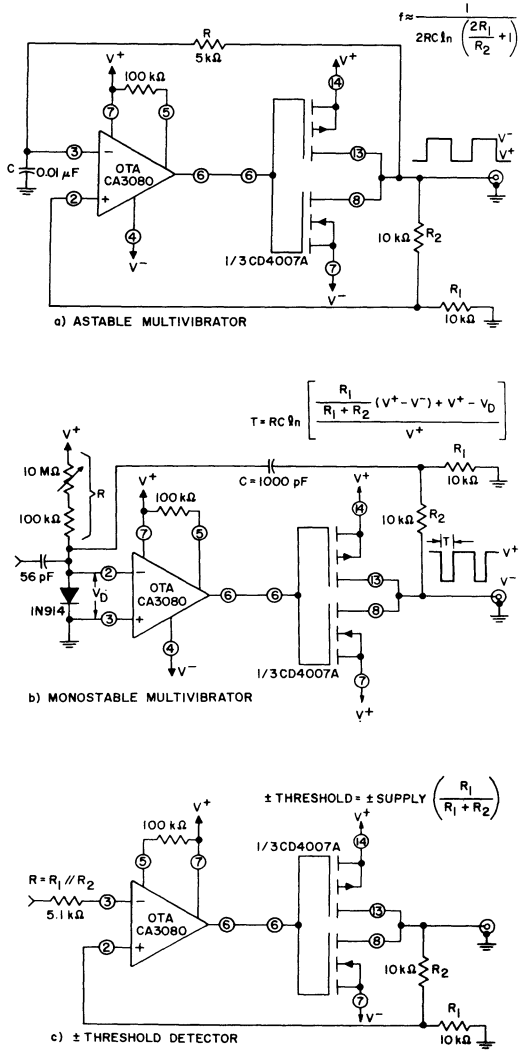


Fig. 36– Multistable circuits using the OTA and COS/MOS Inverter/Amplifiers: a) astable multivibrator; b) monostable multivibrator; c) threshold detector (plus or minus). For greater current output, the remaining amplifiers in the CD4007A may be connected in parallel with the single stage shown.

Fig. 36 shows a variety of circuits that can be assembled using the CA3080 to drive one "inverter"/amplifier in the CD4007A. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs. power consumption tradeoffs may be made by adjustment of the I_{ABC} current to the CA3080. The quiescent power consumption of the circuits shown in Fig. 36 is typically 6 mW, but can be made to operate in the micropower region by suitable circuit modifications.

Micropower Comparator

The schematic diagram of a micropower comparator is shown in Fig. 37. Quiescent power consumption of this circuit is about 10 μW (typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420 μW. Under these conditions, the circuit responds to a differential input signal in about 8 μsec. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 nsec., but the power consumption rises to 21 mW.

The differential amplifier input common-mode range for the circuit of Fig. 37 is -1V to +10.5 V. Voltage of the micropower comparator is typically 130 dB. For example, a 5 μV input signal will toggle the output.

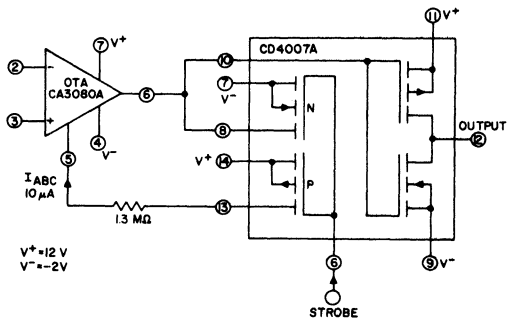


Fig. 37– Schematic diagram of micropower comparator using the CA3080A and COS/MOS CD4007A.

APPENDIX I
CURRENT MIRRORS

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Fig. A shows this basic configuration of the current-mirror. Q2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta I_b$. If a current I_1 is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q2 such that Q2 "sinks" the applied current I_1.

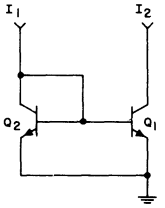


Fig. A— Diode – transistor current source.

If the base of a second transistor (Q1) is connected to the base-to-collector junction of Q2, shown in Fig. A, Q1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current (I_1) and the collector current (I_2) of transistor Q, is due to the fact that the base-current for both transistors is supplied from I_1. Fig. B shows this current division, using a unit of base current (1) to each transistor base. This base

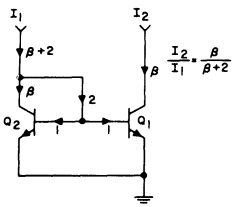


Fig. B— Diode – transistor current source. Analysis of current flow.

current causes a collector current to flow in direct proportion to the β of each transistor. The ratio of the "sinking" current I_2 to the input current I_1 is therefore equal to $\frac{I_2}{I_1} = \beta/(\beta+2)$. Thus, as β increases, the output "sinking" current (I_2) level approaches that of the input current (I_1). The curves in Fig. C show this ratio as a function of the transistor β. When the transistor β is equal to 100, for example, the difference between the two currents is only two percent.

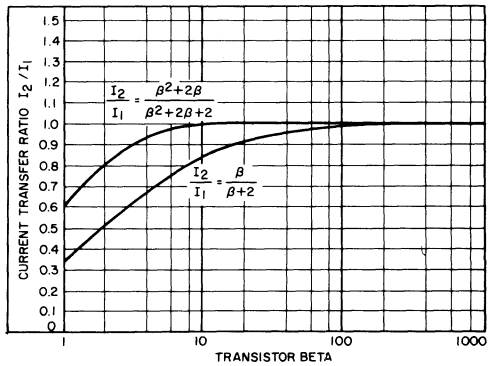


Fig. C— Current transfer ratio I_2/I_1 as a function of transistor beta.

Fig. D shows a curve-tracer photograph of characteristics for the circuit of Figs. A and B. No consideration in this discussion is given to the variation of the transistor (Q1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q1.

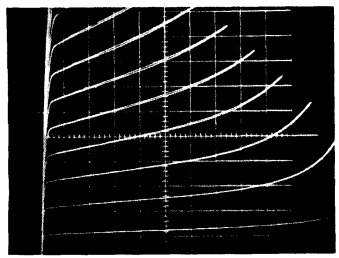


Fig. D— Photo showing results of Figs. A & B.

This diode-connected transistor (Q3 in Fig. E) may be considered as a current-sampling diode that senses the emitter-current of Q1 and adjusts the base current Q1 (via Q2) to maintain a constant-current in I_2. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Fig. F shows the improved output resistance characteristics of the circuit of Fig. E. (Compare Fig. D and F).

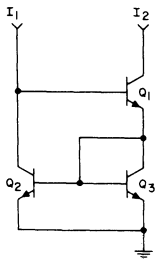


Fig. E— Diode – 2 transistor current source.

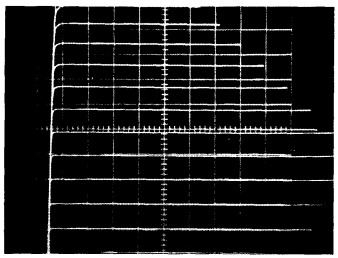


Fig. F— Photo showing results of Fig. E.

Fig. G shows the current-division within the "mirror" assuming a "unit" (1) of current in transistors (Q2 and Q3.

The resulting current-transfer ratio $I_2/I_1 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$. Fig. C shows this equation plotted as a function of beta. It is significant that the current transfer ratio (I_2/I_1) is improved by the β^2 term, and reduces the significance of the $2\beta + 2$ term in the denominator.

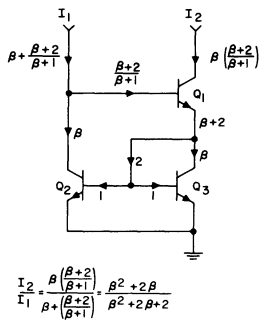


Fig. G— Current flow analysis of Fig. E.

Conclusions

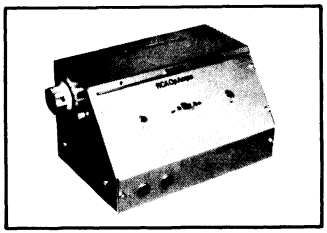
The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplications, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with COS/MOS (Complementary-Symmetry MOS) IC's being operated in the linear mode.

Acknowledgements

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.

References

1 RCA's Linear Integrated Circuits Manual, Basic Circuits Section.
2 RCA published data for CA3060 File No. 404



Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

by T. J. Robe

The advent in recent years of very high-gain operational amplifiers operating in the 1/f noise-frequency spectrum has placed emphasis on the need for very low-noise devices. This need is particularly true for operational amplifiers which have either low-offset characteristics and/or offset-null capability.

The traditional methods used to select such devices involve the measurement of either spot or wideband (≈ 10 kHz) noise figures in the 1/f frequency range (10 Hz to 10 kHz) at various source resistances. This type of measurement, however, only provides an indication of the average noise power at the measurement frequency and does not reveal the burst ("popcorn") noise characteristics of the Device Under Test (DUT). The metering circuits cannot respond fast enough to measure the effects of burst-noise. Fig. 1a shows a photograph of typical burst-noise as a function of time for an operational amplifier having poor burst-noise characteristics. This photo illustrates burst-noise which is characterized by random abrupt output voltage-level changes that persist for periods from approximately 1/2 millisecond to several seconds. Additionally, the random rate at which the bursts occur ranges from approximately several hundred per second to less than one per minute. Furthermore, these rates are not necessarily repetitive and predictable. Consequently, the nature of burst-noise prevents its measurement by means of the standard averaging techniques. Instead, a technique to detect individual bursts must be used and a DUT must be under observation for a period in the order of 10 seconds to one minute. Fig. 1b shows a photo of the output of a virtually burst noise-free operational amplifier, the RCA-CA6741T.

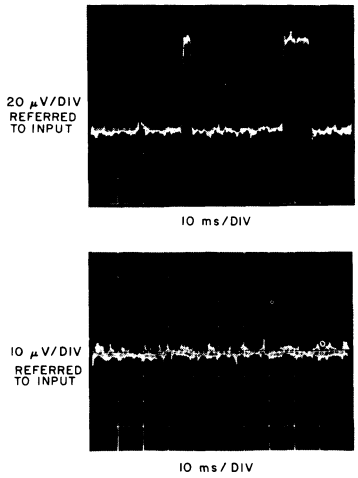


Fig. 1— (a) Photo of output waveforms for amplifier with poor burst-noise characteristics; (b) photo of output waveform for the RCA-CA6741T.

Test Configuration

Some of the major questions relevant to the type of test required are:

1. What characteristics of the burst-noise should be detected?
2. What test-circuit configuration is most suitable to detect these characteristics?
3. What are the "Pass-Fail" criteria?

There are three major characteristics of the noise burst which have an impact on the suitability of a device from the standpoint of applications: burst amplitude, duration, and rate of occurrence. Of these, burst-amplitude and rate of occurrence are of primary interest to potential users of a particular device. Long duration bursts (of sufficient amplitude) seriously degrade the performance of dc amplifiers; however, suitable devices could be selected by the rejection of any unit which produced even one burst during some prescribed test period. Therefore, an absolute measurement of burst duration is not a prime necessity.

The rate of occurrence, on the other hand, as measured by the burst-count in a given test period could conceivably

be considered as a variable of prime importance in the selection process. For instance, a burst-rate of 100 per second is clearly objectionable in almost any low-level low-frequency application, whereas the occurrence of only one low-amplitude burst in a one-minute period might be quite acceptable. Consequently, it is desirable to include flexibility in the testing system so that "Pass-Fail" criteria can be established on the basis of burst-noise count in some prescribed period of time. The test equipment described herein detects total noise (1/f noise plus burst noise) bursts with amplitudes above a preset threshold level during a given test period and allows acceptance or rejection on the basis of the number of noise voltage excursions beyond the threshold level, in the selected test period.

Another factor to be considered is the bandwidth of the test system. Excessive bandwidth allows the normal "white" noise of the terminating resistors and the DUT to obscure burst-noise occurrences and does not realistically simulate the low-frequency applications in which burst-noise is particularly objectionable. On the other hand, a test circuit having excessively narrow bandwidth prevents detection of the shorter-duration bursts ($\approx$ 1/2 ms) even if their amplitude is relatively high. A suitable compromise is chosen in which the system rise time permits a burst of "minimum" duration to reach essentially its full amplitude. Because the rise time and bandwidth of an amplifier are related by the equation:

$$BW \approx \frac{0.4}{t_r}$$

the minimum bandwidth to detect a 0.5 ms burst is approximately:

$$BW_{min} = \frac{0.4}{(0.5)(10^{-3})} = 0.8 \text{ kHz.}$$

Consequently, a 1 kHz bandwidth has been selected as a reasonable one for a burst-noise test system and, therefore, prescribes the need for a low-pass filter in the system.

The test requirements outlined above can be implemented with the following circuit elements shown in the block diagram of Fig. 2a. Fig. 2b shows the complete system schematic:

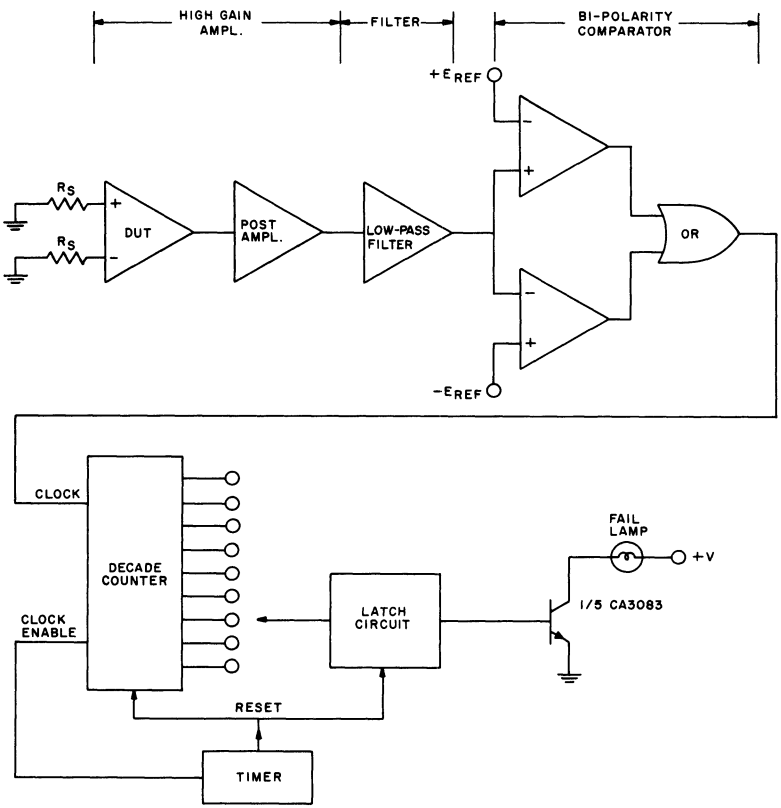


Fig. 2a— Block diagram of burst-noise test set-up.

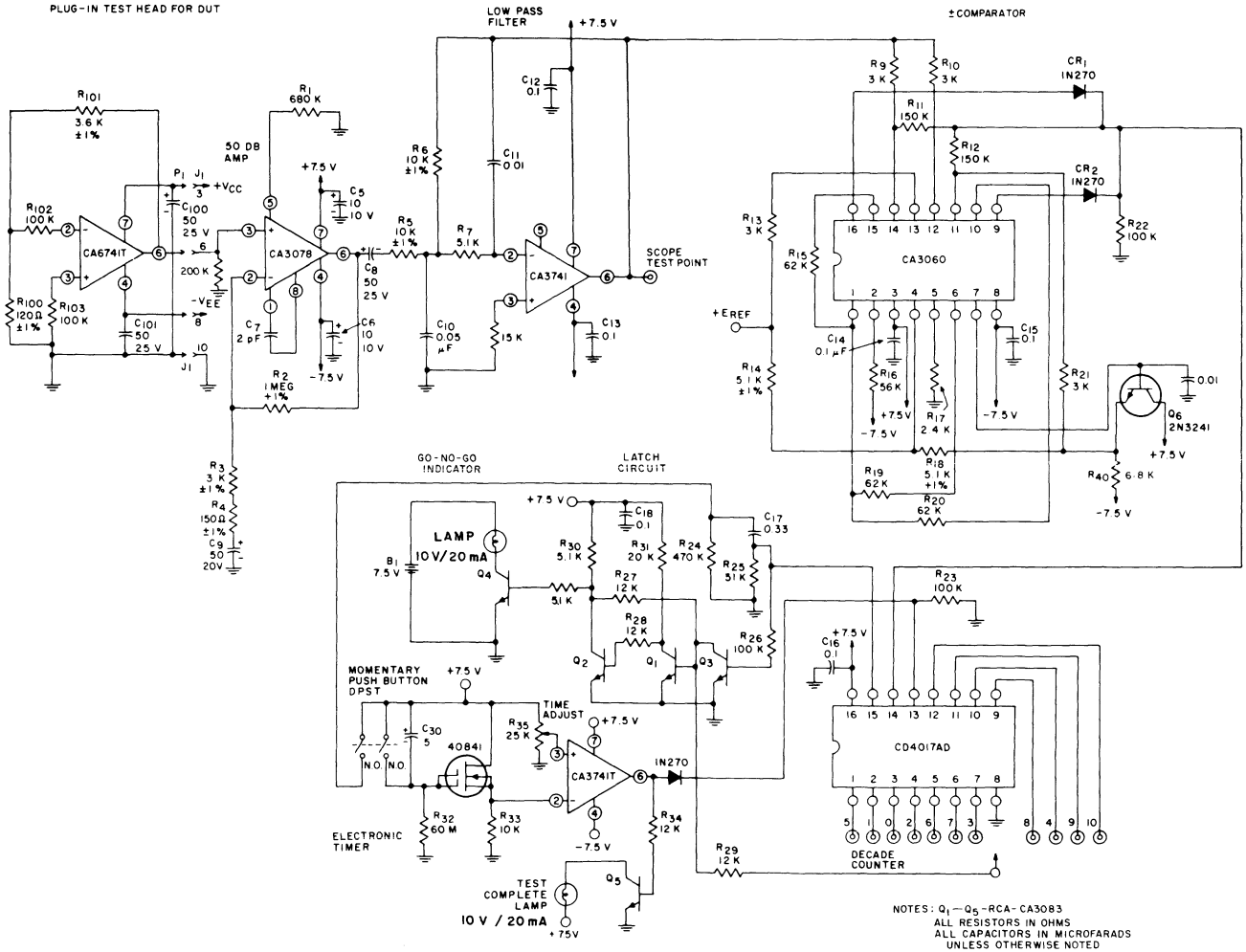


Fig. 2b– Complete schematic diagram for burst noise test-set.

1. A fixed high-gain amplifier incorporating the DUT as the first stage to amplify the microvolt-level burst to an easily detectable level (this should be a burst noise-free unit);
2. A low-pass filter to limit the test bandwidth to approximately 1 kHz,
3. A comparator to produce a fast-rise high-level single-polarity output pulse whenever an input burst-noise pulse (of either polarity) exceeds a preset (but adjustable) threshold level;
4. A counter to tally the number of pulses emanating from the comparator during the test period: a single decade counter is adequate.
5. A latch circuit which trips to the "latched" state when the count exceeds a preselected number (e.g. 1 to n). The latch circuit, if tripped, energizes an indicator lamp.
6. A timer to control the period over which the counter is enabled. It should incorporate the capability to reset both the counter and the latch circuit at the beginning of each test period.
7. Power supplies for the DUT and other auxiliary circuits.

Test Conditions

Some of the conditions which affect the burst-noise performance of the DUT include bias-level, source resistance (Rs), and ambient temperature (T_A).

The quiescent operating conditions in operational amplifiers are normally set by the magnitude of the positive and negative supplies. Many of the newer Op-Amp types, however, have bias-terminals into which fixed currents can be injected to set their performance characteristics. The RCA-CA3060, CA3080, and CA3080A Operational Transconductance Amplifiers (OTA's) and; the RCA-CA3078 and CA3078A Micropower Op-Amps are examples of such devices. For best low-frequency and burst-noise performance, these amplifiers should be operated at the lowest bias currents consistent with the gain-bandwidth requirements of the particular application.

In the test for burst noise, the source resistance (Rs) seen by the input terminals of the DUT, is a key test parameter. Burst noise causes effects which are equivalent to a spurious current-source at the device input and, therefore, burst-noise current generates an equivalent input noise-voltage in proportion to the magnitude of the source resistance through which it flows. Accordingly, to increase the sensitivity of the test system, it is desirable to use the highest source resistance consistent with the input offset-current of the DUT. For example, an Op-Amp which has 0.1 μA input offset current could realistically be tested with source-resistance in the order of 100KΩ (10 mV input offset), whereas a 1 MΩ source-resistance (100 mV input offset) could cause excessive offset in the output. For 741 type Op-Amps a 100kΩ resistance is recommended.

Burst-noise generation in amplifiers is usually more pronounced at lower temperatures (particularly below 0°C). Consequently, consideration must be given to the temperature of the DUT in relation to the temperature range under which the device is expected to perform in a particular operation.

A test parameter of importance is the time duration of observation. Because the frequency of burst-noise occurrence is frequently less than once every few seconds, the minimum test period should be in the range of from 15 to 30 seconds.

Pass-Fail Criteria

A test system built to accommodate the test philosophy outlined above has the ability to reject or pass a DUT on the basis of two variables: burst-amplitude and the frequency of burst occurrence. The burst-amplitude which will trip the counter can be no lower than the background 1/f noise peaks of burst-free units, otherwise normal background noise will fail the DUT.

The background noise peaks depend on the source termination Rs, the wide band 1/f noise figure of the DUT, and the test system bandwidth. A good estimate of the normal background noise-peak levels can be computed from the definition of noise factor and an empirically determined noise-crest factor of approximately 6:1. The crest-factor is the ratio of the maximum peak-noise voltage to the RMS noise voltage. The noise factor is defined as the ratio of the total noise power at the amplifier output to the output-noise power due to the source resistors alone. In terms of the RMS noise voltages at the input terminals of the amplifier this is equivalent to:

$$\text{Noise Factor (F)} = \frac{E^2\text{input noise total}}{E^2\text{noise source resist}} = \frac{(E_{NTi})^2}{(E_{NRS})^2} \quad (1)$$

E_{NTi} is the total input noise-voltage, i.e., the sum of noise generated in the source termination resistance and noise generated by the DUT.

E_{NRs} is that part of E_{NTi} due to Rs alone.

$$\text{Therefore,} \quad E_{NTi} = (\sqrt{F})\,(E_{NRs}). \quad (2)$$

E_{NRs} can be computed by using the well known expression for "white-noise" generated across the terminals of a resistor (R):

$$E_{NR}(\text{RMS}) = \sqrt{4kTBR} \quad (3)$$

where k = Boltzmans Constant = 1.372×10^{-23} j/°K

T = Absolute Temperature in °K
B = Noise Bandwidth in Hz
R = Value of the resistor in ohms.

Thus, at a room temperature of 290°K

$$E_{NR}(\text{RMS}) = 1.28 \times 10^{-10} \sqrt{BR}$$

For example, a 100 kΩ resistor preceding a system with a bandwidth of 1 kHz will generate a noise-voltage of

$$(1.28 \times 10^{-10}) \quad (\sqrt{10^3 \cdot 10^5}) \quad = 1.28\ \mu V_{RMS}$$

Both inputs of an Op-Amp are usually terminated in Rs, hence it is necessary to combine the effects of both resistors to determine the effective E_{NRs} at the input of the DUT. Because the noise voltages from these two resistors are uncorrelated their voltages must be added vectorally rather than algebraically.

$$E_{NRs}\ (\text{effective}) = \sqrt{(E_{NR_{s1}})^2 + (E_{NR_{s2}})^2} \qquad (4)$$

because $E_{NR_{s1}} = E_{NR_{s2}}$, when $R_{s1} = R_{s2}$

$$E_{NRs}\ (\text{effective} = (\sqrt{2})\ (E_{NRs})$$

and for 1 kHz bandwidth at 290°K

$$E_{NRs}\ (\text{effective}) = (\sqrt{2})\ (1.28\ \mu V) = 1.81\ \mu V_{RMS}.$$

If in this example, the DUT has a wideband 1/f noise figure of 4 dB (2.5:1 power ratio) the total RMS background noise-voltage at the input will be

$$E_{NTi} = (\sqrt{F})\ (E_{NRs})\ (\text{from eq.(2)})$$
$$= (\sqrt{2.5})\ (1.81) = 2.9\ \mu V_{RMS}$$

If a crest factor of 6:1 is assumed, the peaks of the background noise will be approximately (6) (2.9) = 17 μV peak. This voltage is the lower limit of the burst-amplitude rejection level. A reasonable threshold for burst detection and rejection might be 50-100% greater than this minimum value.

An alternate method used to set the burst-threshold limit involves a direct measurement (at the output of the high gain amplifier-filter combination) using a storage oscilloscope or a "true RMS" voltmeter. By this method the noise peak or RMS noise voltage of burst-free units is determined. This measurement provides a good practical check on the accuracy of the computation outlined above. Selection of the acceptable number of burst counts in the test period is arbitrary, but dependent on the type of application intended for the DUT. To be acceptable in some critical applications, the DUT may not generate even a single burst-pulse in a relatively long period of time.

Burst-Noise Test System Circuits

1. High gain Amplifier – Filter

Fig. 3 shows the schematic diagram of the high-gain amplifier-filter which provides a fixed gain of 80 dB with a 12 dB octave roll-off above 1 kHz. The gain-function is somewhat arbitrarily distributed between the DUT and

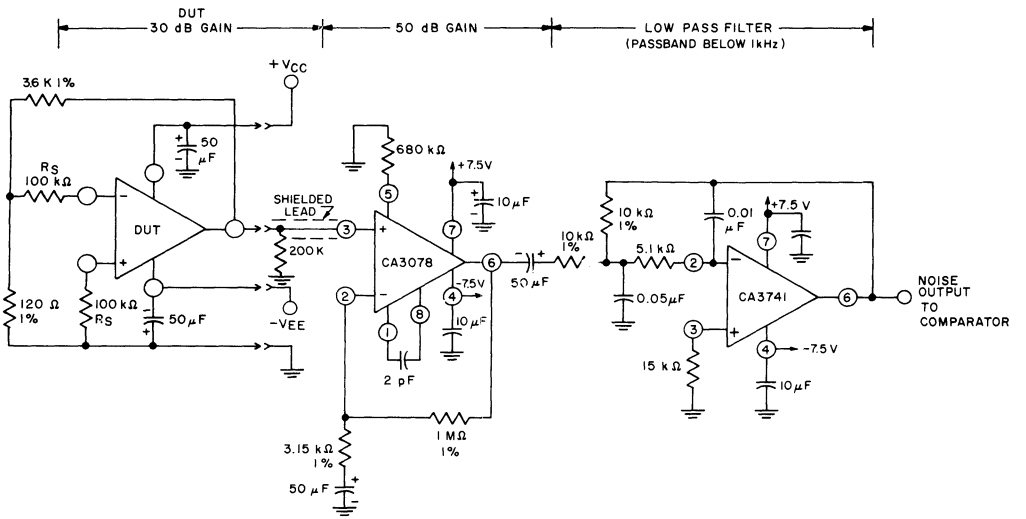


Fig. 3– Schematic diagram of high-gain amplifier/filter.

post-amplifier: 30 dB and 50 dB respectively. This distribution is based on the need for sufficient gain in the DUT portion to eliminate significant noise-signal contributions from the second stage while simultaneously allowing adequate loop-gain in each stage to provide accurate gain-setting with precise external resistors. The first stage is shown as a plug-in module so that any type of DUT configuration having 30 dB gain can be tested.

The capacitive coupling employed provides a low frequency cutoff of about 1 Hz and eliminates the need for dc-offset zero-adjustments. The dc offset-voltage at the filter output is less than 5 mV which corresponds to less than 0.5 μV error when referred to the noise input (an 80 dB gain is assumed.) Several seconds must be allowed, however, for the DC operating point to stabilize after the power is applied to the DUT.

2. Bi-Polarity Comparator

Fig. 4 shows the schematic diagram for the threshold-detecting comparator. Because bursts of either polarity must be detected and converted to positive output pulses, two comparators are required: one having a positive-threshold reference and the other having a negative-threshold reference of equal magnitude. The RCA CA3060 triple OTA is convenient to use because a single package provides circuits for both comparators plus a reference inverter for the negative threshold reference. The positive feedback provided by the R_f and R_i connections produces a hysteresis effect with reference to the input switching threshold, (i.e., the comparator does not return to its quiescent state until the input noise signal drops well below the initial threshold trip-level). This feature is necessary to prevent multiple triggering by the background noise signals superimposed on top of the burst-noise pulse. By this means, multiple counting of a single burst-noise pulse is avoided.

The magnitude of the threshold reference voltage E_R determines the burst-level which trips the comparator. If a voltage gain of 80 dB is provided by the amplifiers, a 200 mV reference voltage will enable the circuit to be triggered when a burst-noise pulse (whose amplitude is equivalent to the level of 20 μV referred to the DUT input) is present.

3. Counter-Latch-Timer Control Circuits

The remaining circuits of the go-no-go burst-noise tester are shown in Fig. 5. The decade-counter is incorporated in a single COS/MOS IC (RCA CD4017AE) which has clock, reset, and enable inputs, and an output terminal for each of ten count-positions (0 to 9). A carry-out signal is available if the use of more than a single decade is desired. The clock input-signal must be positive-going and have a magnitude of

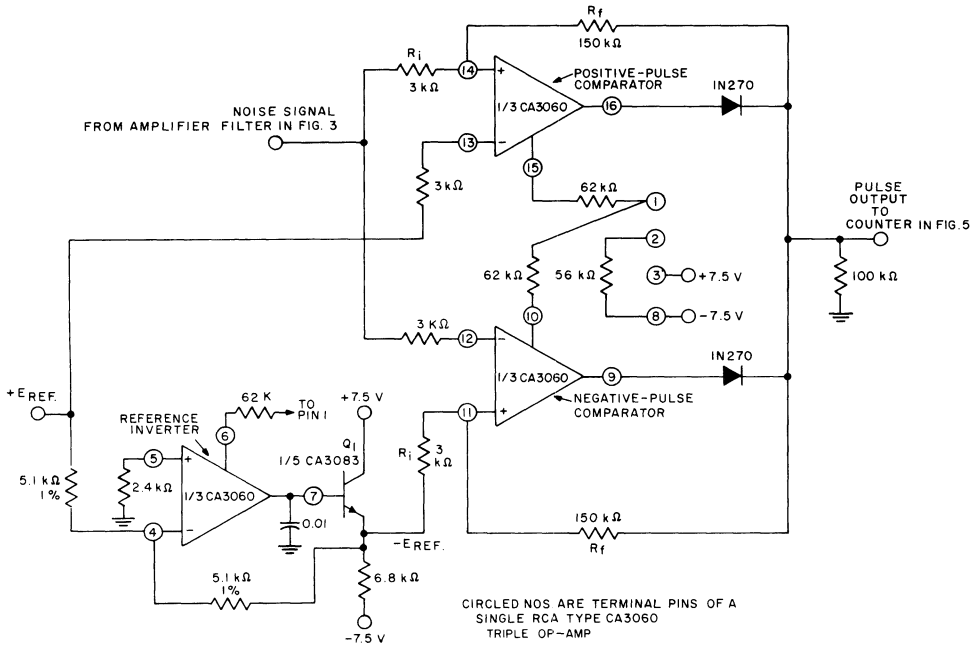


Fig. 4– Schematic diagram of threshold-detecting comparator.

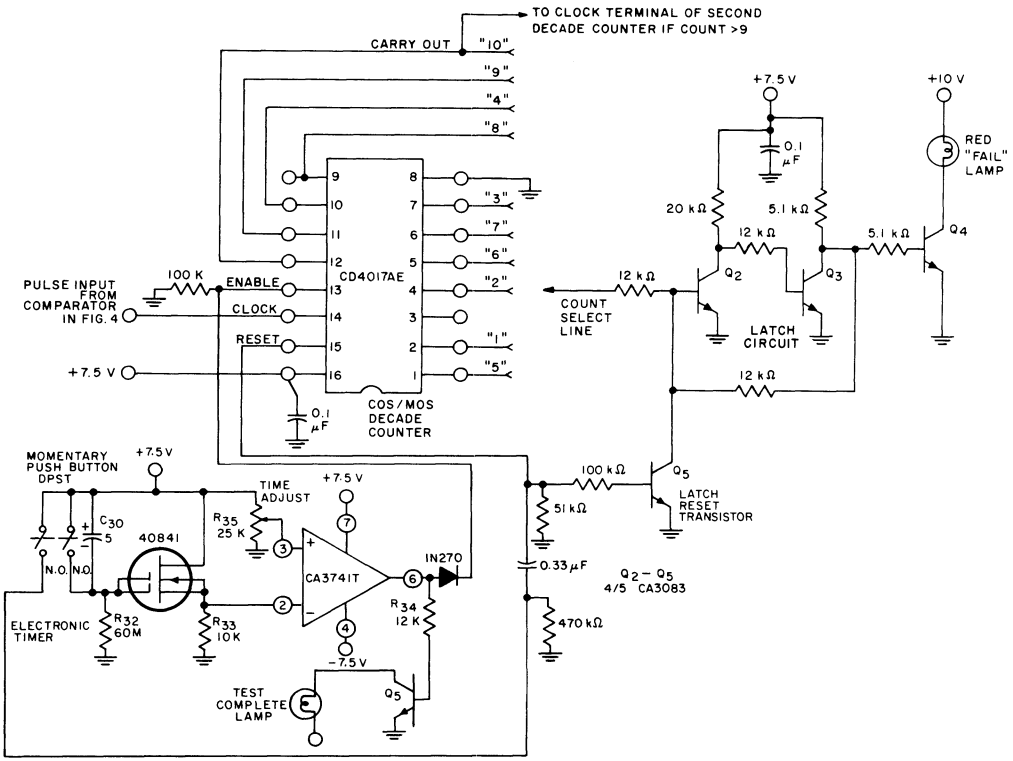


Fig. 5— Counter-latch-timer-control circuit schematic.

at least 70% of the supply-voltage and rise-time equal to or less than 15 μs. The comparator shown in Fig. 4 provides an output signal which meets these requirements.

Selection of the reject count is made by a pin-jack connection of the latch-circuit input-lead to the appropriate output terminal of the counter. Whenever the selected count-position voltage goes "high" the latch-circuit is switched to the latched-state, and the fail-indicator lamp "on". The latch and lamp will remain "on" until the reset button of the electronic timer is switched to the "Timer On" position. This action provides a momentary reset signal (≈ 20 ms) to both the latch and counter circuits and places a continuous enable voltage on the counter for the duration of the test period.

Spurious Noise Sources and Their Suppression

The very low voltage levels and the high source impedances normally used for burst testing render the system highly susceptable to external spurious noise sources. This problem is particularly serious if a test unit is going to be rejected for as little as one or two input burst-noise pulses exceeding 20-30 μV. The major sources of spurious noise encountered in the development of this test system were:

1. 60-Hz hum pickup,
2. power supply transients,
3. electromagnetic pick up of switching transients.

60-Hz hum is introduced by capacitive or inductive coupling or as power-supply ripple. Power-supply ripple is not normally a problem when testing operational amplifiers with regulated supplies, because the Op Amps generally have good power-supply rejection. This source of noise must be considered, however, when testing devices that do not have good inherent power-supply rejection. Capacitive or inductive coupling of hum can occur when 60-Hz line cord leads are within a few inches of the input terminals of the DUT. Precautions, such as proper lead dress and twisting of the 60-Hz leads, eliminate this problem.

Power-supply transients, as distinguished from power-supply ripple, can be of sufficient amplitude to introduce detectable noise pulses at the operational amplifier input. Such transients are produced when other equipment on the same ac line is switched on or off. A typical power-supply rejection ratio for an operational amplifier is 50 μV/V (i.e. a 1 volt transient on the power-supply is equivalent to a 50 μV noise pulse at the DUT input). This example demonstrates that the test system cannot tolerate power-supply transients greater than approximately 100 mV even when testing units with good power-supply rejection. Unless the power-supply is

known to be free of such transients, a battery-operated system is recommended. Even when this system is battery-operated, "On-Off" switching of nearby equipment introduces detectable transients into the system. These problems are eliminated by placing the test circuitry in a completely shielded enclosure with a hinged top for easy access to the test unit. The external noise problem is best solved by use of a shielded enclosure and by use of a battery-operated power-supply contained within the enclosure. Fig. 6 shows a photo of the circuit board layouts of the test unit.

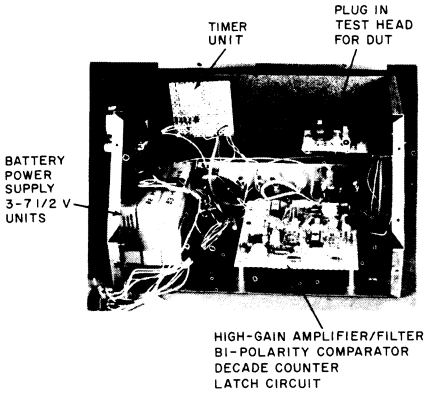


Fig. 6— Photo of circuit-board layout.

Application Notes on MOS/FET Devices

AN-3193	"Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor"	336
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Application Considerations for the RCA 3N128 VHF MOS Field-Effect Transistor

by

F. M. Carlson

Early MOS field-effect transistors were intended primarily for low-frequency applications in which their extremely high input impedance is advantageous,* and were not designed to be useful in the vhf range (30 to 300 MHz). Recently, however, RCA has developed high-frequency MOS transistors that exhibit high gain and low noise at vhf, together with very low feedback capacitance and cross-modulation distortion that approaches the low levels of electron tubes. The low level of cross-modulation distortion is a particularly important characteristic in view of the increasing congestion of the communications frequency bands.

This note describes applications and vhf circuit considerations for a new high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

Biasing Requirements and Circuit Configurations

The biasing requirements and operating characteristics of an n-channel MOS transistor such as the 3N128 are similar to those of an electron tube. For example, the 3N128 uses positive drain voltages and usually negative gate voltages which are analogous to the plate and grid voltages, respectively, of electron tubes. In addition, the current-voltage characteristics of the 3N128, shown in Fig.1, are similar to those of a pentode tube. An electron-tube analogy, therefore, can be useful in the analysis of the n-channel 3N128 MOS transistor.†

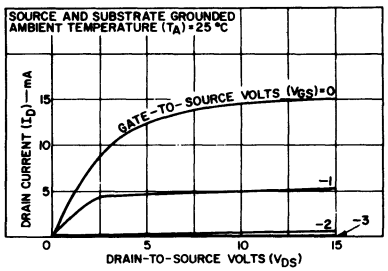


Fig.1 - Transfer characteristics for the RCA 3N128 vhf MOS transistor.

Although their characteristics are similar, MOS transistors have several important advantages over electron tubes. They can be operated at the low voltages typical of bipolar transistors. The dc gate current of MOS transistors is substantially less than the

* The basic theory of MOS transistors and equivalent circuits for these devices are discussed in RCA Application Note AN-201, "Application Considerations for RCA 3N98 and 3N99 Silicon MOS Transistors," by D. M. Griswold.

† The electron-tube analogy does not apply to p-channel MOS transistors or to enhancement types.

grid current of most electron tubes. In addition, the MOS transistor requires no heat-generating filament.

MOS transistors are most often used in the common-source type of circuit configuration. Fig.2 shows three basic methods of dc-biasing an MOS transistor in a common-source circuit. MOS transistors may also be used in common-gate or common-drain (source-follower) configurations.[2] These circuits are not widely used in vhf applications, however, because their gain is low at high frequencies.

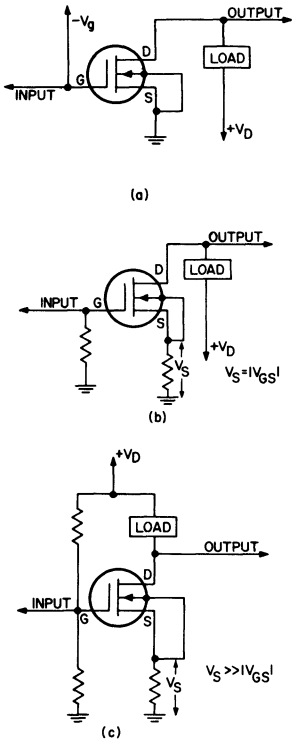
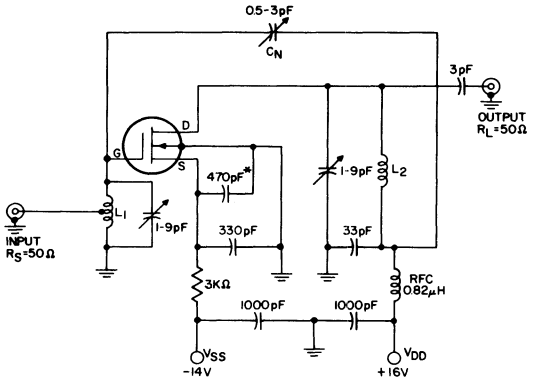


Fig.2 - Bias methods for common-source MOS transistor stages: (a) fixed bias; (b) source-resistor bias; (c) constant-current bias.

Fig.3 shows a 200-MHz common-source amplifier used to measure the rf power gain of the MOS transistor. This amplifier uses a modified form of the constant-current biasing arrangement shown in Fig.2(c). With this modified biasing arrangement, both the insulated gate and the case of the MOS transistor are operated at dc ground potential. The insulated gate should always have a dc path to ground even if the path is through a multimegohm resistor. If the gate is allowed to float, the resultant dc bias conditions may be unpredictable and possibly harmful.



L1 = 4-1/2 turns of No.20 wire, 3/16 inch in dia., 1/2 inch long, tapped at 1 turn

L2 = 3-1/2 turns of No.20 wire, 3/8 inch in dia., 1/2 inch long

* Leadless disc capacitor

Fig.3 - 200-MHz common-source amplifier.

Fig.4 illustrates the effect of the leakage resistances R_{L1} and R_{L2} when the insulated gate is floating. When these resistances ($\approx 10^{14}$ ohms) are approximately equal, they form a voltage divider which biases the insulated gate at $+V_{DD}/2$. This value of bias voltage may exceed the maximum rating for positive gate voltage and, in addition, may cause an excessive flow of drain current.

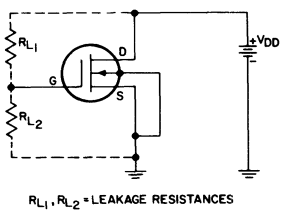


Fig.4 - Bias conditions for an MOS transistor when the insulated gate is floating.

The cascode configuration represents a useful variation of common-source circuit. In this configuration, a common-source-connected MOS transistor is used in the lower section of the cascode, and a common-gate-connected MOS transistor is used in the upper section. Fig.5 shows the use of MOS transistors in a 200-MHz cascode amplifier. This circuit normally requires a negative voltage on the gate of Q_1, a positive voltage on the gate of Q_2, and approximately equal drain-to-source voltages for each transistor. Although the gate of Q_2 may require a positive voltage of 5 to 10 volts, the net gate-to-source voltage for this transistor should be approximately 0 to -1 volt.

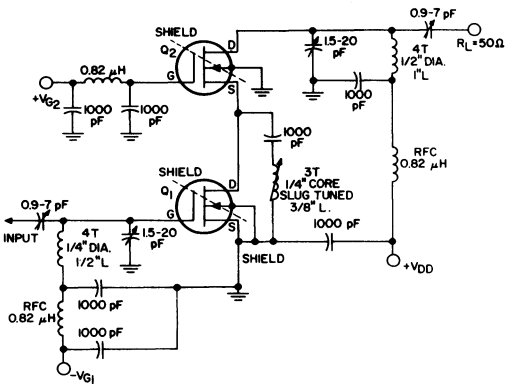


Fig.5 - 200-MHz cascode amplifier.

Selection of Operating Point

The operating point selected determines the power gain, noise figure, power dissipation, and, where applicable, battery life. In many applications, a compromise between gain and available supply voltages or battery lifetime is necessary. Knowledge of the variation in gain and noise figure as functions of voltage and current is essential, therefore, before an operating point can be selected.

The 3N128 provides maximum rf power gain at a drain-to-source voltage V_{DS} of approximately 20 volts and a drain current I_D of about 5 milliamperes. The transistor also exhibits a minimum noise figure at a V_{DS} of 20 volts for a drain current of about 2 milliamperes. The difference in the noise figures obtained at 2 milliamperes and at 5 milliamperes, however, is very small (usually between 0 and 0.2 dB) and generally is not a significant factor in the selection of the operating point. Although a V_{DS} of 20 volts represents the optimum value for the 3N128 in terms of both rf power gain and noise figure, this value is also the maximum V_{DS} rating for the transistor. Greater long-term reliability is achieved, therefore, by operation of the 3N128 at a V_{DS} of 12 to 15 volts rather than at 20 volts.

For a V_{DS} of 15 volts and an I_D of 5 milliamperes, the 3N128 typically provides a power gain of 18 dB and a noise figure of 4 dB at 200 MHz. Operation of the 3N128 at considerably lower drain currents, such as those normally employed in battery-powered equipment, does not seriously affect system performance. For example, when the transistor is operated at a V_{DS} of 15 volts and an I_D of only 1 milliampere, the power gain and noise figure at 200 MHz are typically 15.5 dB and 4.5 dB, respectively. Because the MOS transistor is a voltage-controlled device, its performance for a given power dissipation can often be improved by operation at high voltage and low current levels. At a power dissipation of 30 milliwatts, for example, the 3N128 typically provides a power gain of 17.3 dB and a noise figure of 3.9 dB when operated at 15 volts and 2 milliamperes. At the same dissipation level, however, the power gain is reduced to 14.6 dB and the noise figure is increased to 4.7 dB when the 3N128 is operated at 6 volts and 5 milliamperes. Fig.6 shows the variations in power gain and noise figure of the 3N128 as functions of the drain current and voltage.

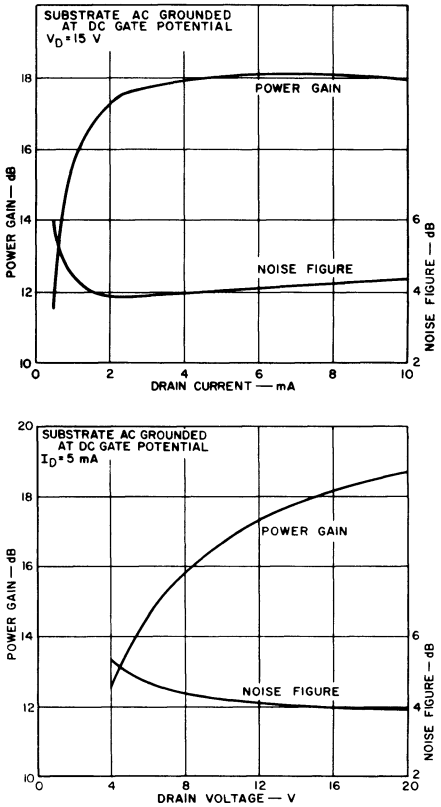


Fig.6 - Power gain and noise figure of the RCA 3N128 at 200 MHz as functions of drain current and voltage.

A gate voltage V_G of between -0.5 and -2 volts is normally required to bias a 3N128 for operation at a drain voltage V_D of 15 volts and a drain current I_D of 5 milliamperes. If a fixed-bias circuit, as shown in Fig.2(a), is used, the value of the gate voltage must be adjustable to compensate for variations among individual transistors. For the source-resistance bias circuit shown in Fig.2(b) the value of the biasing resistor should be 200 ohms (5 mA x 200 ohms = 1 volt). The source-resistance circuit will limit the variations in current among the different transistors to approximately

50 per cent. With the constant-current bias circuit shown in Fig.2(c), variations in current from one transistor to another can easily be limited to less than 10 per cent. Regardless of the bias circuit or the bias point selected, there is no danger of thermal runaway with the 3N128 because this transistor has a negative temperature coefficient at the zero-gate-bias point. In the selection of the bias circuit for an MOS transistor stage in which automatic gain control is employed, consideration should be given to the following principle: The more restrictive the tolerance imposed on quiescent operating-point current, the more difficult automatic gain control of the stage becomes because the self-compensating action of the constant-current bias circuit also resists current changes that result from the agc action.

AGC Methods

When it is necessary to employ agc in an MOS transistor stage, either of two methods may be used to reduce transistor gain. In one method, referred to as reverse agc, the reduction in gain is accomplished by an increase in negative gate bias. In the other method, the gain is decreased by reduction of the drain-to-source voltage.

In the reverse agc method, the application of higher negative voltage to the gate reduces the drain current and the transconductance of the transistor. The low feedthrough capacitance of the 3N128 (typically about 0.13 picofarad) usually permits more than 30 dB of gain reduction at frequencies up to 200 MHz. Substantially greater gain reduction can be achieved at lower frequencies or in neutralized amplifier circuits.

Gain reduction achieved by the decrease of drain-to-source voltage is usually controlled by a variable impedance in series, or in shunt, with the MOS transistor. The variable impedance may be another MOS transistor or a bipolar transistor. A major disadvantage of this method is that the MOS feedback capacitance rises by a factor of 4 or 6 times as V_D approaches zero. This increase in capacitance reduces the agc range obtainable and decreases the effectiveness of a fixed neutralization network. In addition, the output impedance of the 3N128 decreases with a reduction in the drain voltage.

In the cascode circuit, agc is accomplished most effectively by application of a negative voltage to the gate of the upper (common-gate) section. A wide agc range can be obtained in this circuit. Gain reductions greater than 45 dB at 200 MHz or 65 dB at 60 MHz are realizable in an unneutralized cascode circuit.

RF Considerations

One of the prime advantages of the 3N128 MOS transistor over bipolar transistors is its superior cross-modulation, intermodulation, and modulation distortion performance. The 3N128 has considerably lower feedback capacitance than junction-gate field-effect transistors. In addition, the 3N128 maintains a high input resistance at frequencies well into the vhf range (the real part of the input admittance, $Re(y_{11}) = 0.15$ mmho at 100 MHz).

At maximum gain, the cross-modulation distortion of the 3N128 is approximately one-tenth that of most bipolar transistors, or roughly comparable to the cross-modulation performance of vacuum tubes (at 200 MHz, an interfering signal of approximately 80 millivolts is required to produce cross-modulation distortion of 1 per cent). However, cross-modulation susceptibility changes as the gain of the stage is changed. For a single 3N128, the cross-modulation distortion increases when reverse agc is applied; the distortion is also increased, but to a lesser extent, if agc action is achieved by reduction of the drain-to-source voltage. A deterioration in cross-modulation performance at high attenuation results from the fact that the MOS triode is a sharp-cutoff device; as a result, large non-linearities occur near "pinch-off." Beyond "pinch-off," the transadmittance depends primarily upon the capacitive feedthrough, which does not have large third-order non-linearities. Cross-modulation performance at the extreme limits of attenuation, therefore, is very good.[1] In cascode stages, the effect of reverse agc on cross-modulation distortion is reduced when the agc is applied to the gate of the common-gate stage; application of reverse bias to the gate of the common-source stage results in cross-modulation performance similar to that of a single triode-connected stage. Figs.7 and 8 show the variation in cross-modulation susceptibility as a function of agc. The test circuits used to measure cross-modulation distortion of MOS transistors are shown in Fig.9.

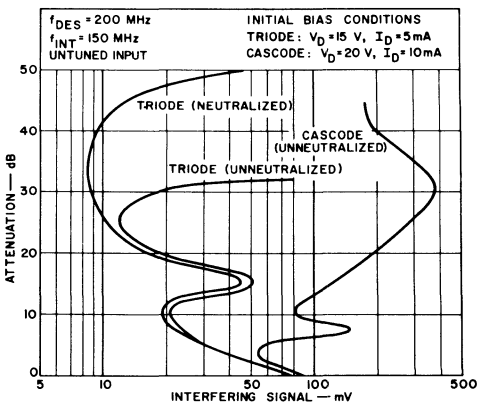


Fig.7 - Cross-modulation distortion as a function of the attenuation produced by reverse agc.

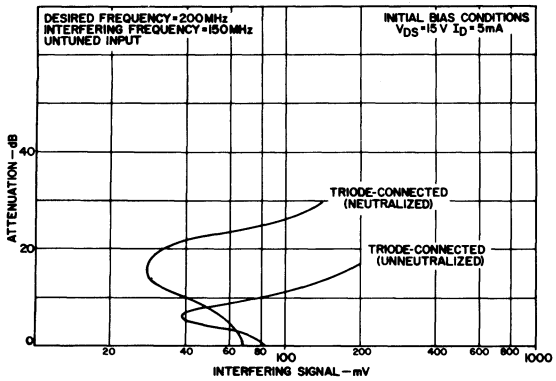


Fig.8 - Cross-modulation distortion as a function of the attenuation produced when agc is accomplished by a reduction of drain-to-source voltage.

The test circuit shown in Fig.10 is used to measure the intermodulation distortion of MOS transistors. In such measurements, the receiver is tuned to 150 MHz. The MOS is then inserted, and bias voltages are applied. When no signals are applied (i.e., the amplitudes of the signals f_1 and f_2 are both 0 volts), the rf indicator of the receiver indicates an equivalent input noise level of approximately 2.4 microvolts. The signals f_1 and f_2 are gradually increased in amplitude until the reading on the rf indicator is 1 microvolt above the noise level (3.4 microvolts total). This reading indicates that 2.4 microvolts of 150-MHz signal is being produced by the interaction of f_1 and f_2 (i.e., $2f_1 - f_2 = 150$ MHz). Table I lists the dc bias levels used for the 3N128 MOS transistor and the amplitude of the f_1 and f_2 signals required to produce an output, at 150 MHz, of 2.4 microvolts, which corresponds to 1 microvolt above the input noise level. The amplitudes of f_1 and f_2 were measured by an rf vacuum-tube voltmeter; the f_1 generator was turned down for measurement of f_2, and vice versa.

Table I

INTERMODULATION DISTORTION DATA FOR THE 3N128 MOS TRANSISTOR

		Interfering Voltages Required to Produce 2.4 microvolts at 150 MHz	
V_D volts	I_D mA	f_1 (175 MHz) mV	f_2 (200 MHz) mV
16.5	10	18	18
16.5	10	7	150
16.5	5	15	15
16.5	5	3.5	150
16.5	5	30	3.5
16.5	2.5	19	21

When the same test methods were used to measure the intermodulation distortion of bipolar transistors, distortion levels were found to be two to five times greater than those of the 3N128 MOS transistor.

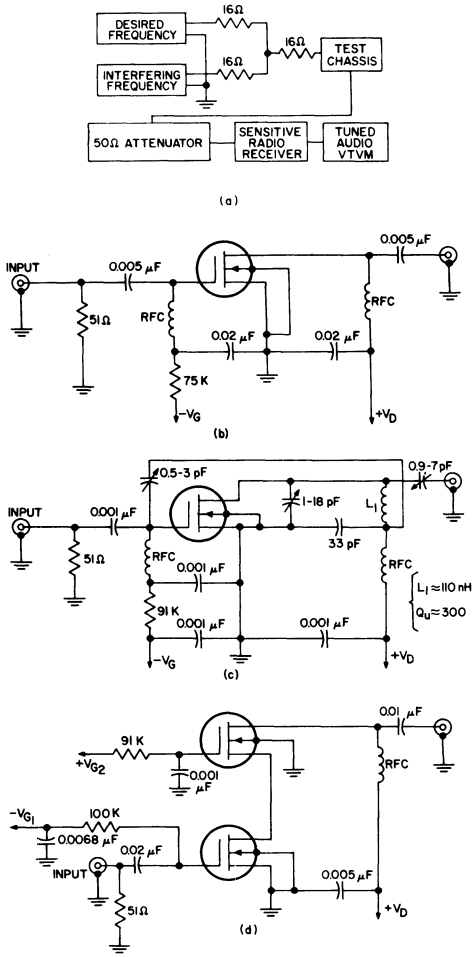


Fig.9 - Test circuits used to measure cross-modulation distortion in MOS transistors: (a) block diagram; (b) unneutralized-stage test circuit; (c) neutralized-stage test circuit; (d) cascode-stage test circuit.

Designing VHF MOS Amplifier Circuits

A complete set of graphs of typical y parameters, both as a function of frequency at constant bias and as as a function of bias at constant frequency, are given in the published data for the 3N128 MOS transistor. The application of these y parameters in the design of the 200-MHz amplifier shown in Fig.3 is discussed in following paragraphs.

For operation at a frequency of 200 MHz, an I_D of

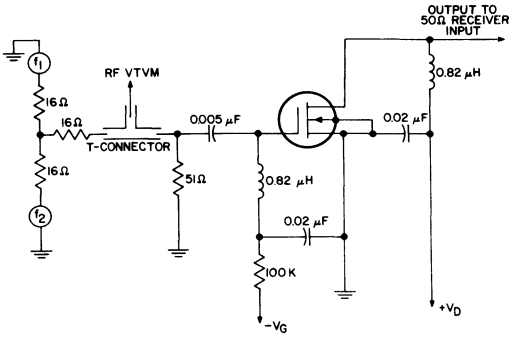


Fig.10 - Test circuit used to measure intermodulation distortion in MOS transistors.

5 milliamperes, and a V_D of 15 volts, the y parameters of the 3N128 are typically as follows:

y_{11} (input admittance with output short-circuited) = 0.45 + j7.2 mmhos

y_{22} (output admittance with input short-circuited) = 0.28 + j1.75 mmhos

y_{21} (forward transfer admittance with output short-circuited) = 7.0 - j1.9 mmhos

y_{12} (reverse transfer admittance with input short-circuited) = 0 - j0.16 mmhos

If y_{12} is assumed to be zero, the maximum available power gain (MAG) under conjugately matched conditions,* may be computed. MAG serves as a useful figure of merit for comparison of the vhf power gain of various MOS transistors. The MAG for the 3N128 is determined as follows:

$$MAG = \frac{|y_{21}|^2}{4Re(y_{11})Re(y_{22})} = \frac{|7.0-j1.9|^2}{4(0.45)(0.28)} = 104 = 20.2\,dB \quad (1)$$

where Re means "the real part of."

All MOS transistors have a small, but measurable, feedback component (y_{12}); it is possible, therefore, that some of them will oscillate under certain circuit conditions. This possibility may be checked by use of methods given by Linvill[2,4] and by Stern.[3,4] If the transistor is unconditionally stable for any combination of passive source and load admittances, then Linvill's critical stability factor C, as determined from the following equation, is less than |1|:

$$C = \frac{|y_{21}y_{12}|}{2Re(y_{11})Re(y_{22}) - Re(y_{21}y_{12})} \quad (2)$$

The critical stability factor for the 3N128 is calculated as follows:

$$C = \frac{|(7.0-j1.9)(0-j0.16)|}{2(0.45)(0.28) - Re(7.0-j1.9)(-j0.16)} = 2.08$$

Stern has derived a similar expression for stability C_S that includes the effect of the generator and load conductances, y_g and y_L, respectively, as follows:

$$C_S = \frac{|y_{21}y_{12}|}{2\,Re(y_{11}+y_g)Re(y_{22}+y_L) - Re(y_{21}y_{12})} < |1| \quad (3)$$

If a conjugate match is assumed at both the input and the output, then $Re(y_g) = Re(y_{11})$, and $Re(y_L) = Re(y_{22})$. For this condition, the stability factor is calculated as follows:

$$C_S = \frac{|(7.0-j1.9)(-j0.16)|}{2(0.45+0.45)(0.28+0.28) - Re(7.0-j1.9)(-j0.16)} = \frac{1.16}{1.31} = 0.885$$

These calculations show that the transistor itself is not unconditionally stable, but that it is stable when placed in a conjugately matched circuit. Therefore, neutralization is not required, although it may be used if a more symmetrical pass-band characteristic is desired. All unneutralized amplifiers have a certain amount of skew in the selectivity characteristic; if this skewness becomes objectionable for the required application, then neutralization (or mis-matching) is necessary.

When neutralization is desired, there are two common methods of obtaining the required feedback. The first, and more common method, is the capacitance-bridge technique shown in Fig.11(a). The capacitance bridge becomes more apparent when the circuit is redrawn as shown in Fig.11(b). The condition for neutral-

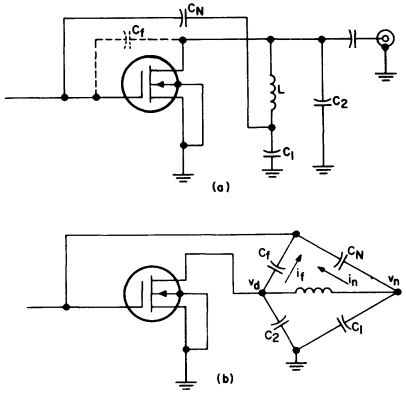


Fig.11 - Capacitance-bridge neutralization circuit: (a) actual circuit configuration; (b) circuit redrawn to emphasize capacitance-bridge network.

* Conjugate match means that the transistor input and the generator and the transistor output and load are matched resistively and that all reactance is tuned out.

ization is that $i_f = i_n$. This condition implies the following relationship:

$$\frac{v_d}{jX_f} = \frac{-v_n}{jX_n}, \text{ or } C_f v_d = -C_n v_n \quad (4)$$

The voltage v_n is defined by the following equation:

$$v_n = \left(\frac{v_d}{jX_L + jX_1}\right) jX_1 = \left(\frac{v_d}{\frac{-\omega^2 LC_1 + 1}{j\omega C_1}}\right) \frac{1}{j\omega C_1} = \frac{v_d}{-\omega^2 LC_1 + 1} \quad (5)$$

If this relationship for v_n is substituted in Eq.(4), the following result is obtained:

$$C_f v_d = -C_n \left(\frac{v_d}{-\omega^2 LC_1 + 1}\right), \text{ or } C_n = -C_f(-\omega^2 LC_1 + 1) \quad (6)$$

At resonance, the equation for the neutralization capacitance C_n may be rewritten as follows:

$$C_n = -C_f\left[\left(\frac{-1}{\omega C_2}\right)\omega C_1 + 1\right] = C_f\left(\frac{C_1}{C_2} - 1\right) \quad (7)$$

If $C_1 >> C_2$, Eq.(7) may be rewritten as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) \quad (8)$$

The other common method of neutralization is the transformer-coupled method shown in Fig.12. Again, the condition for neutralization is that $i_f = i_n$. The requirements for this condition are expressed by the following equation:

$$\frac{v_d}{X_f} = \frac{-v_n}{X_n}, \text{ or } C_f v_d = -C_n v_n \quad (9)$$

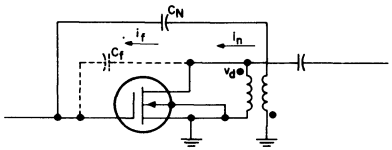


Fig.12 - Transformer-coupled neutralization circuit.

Eq.(9) may be rewritten in the following form:

$$\left|\frac{v_d}{v_n}\right| = \frac{C_n}{C_f} \quad (10)$$

The required turns ratio for the coupling transformer can be determined from Eq.(10).

The generator and load impedances must be matched to the transistor input and output impedances, respectively, to obtain maximum gain. For the 200-MHz amplifier shown in Fig.3, the generator resistance at the input is 50 ohms. For a conjugately matched input, the generator admittance y_g and the real part of the transistor input admittance must appear to be equal. Because the generator admittance y_g is 20 mmhos and the real part of the input admittance $Re(y_{11})$ is 0.45 mmho, the coupling transformer must provide a transformation ratio of 44 to obtain the desired impedance match. The turns ratio required is determined as follows:

$$\frac{N_2}{N_1} = \sqrt{44} = 6.6$$

Experimentally, a turns ratio of 4 was found to be approximately the optimum value. This difference results, in part, from the fact that the parallel resistance of the tank coil was not considered in the calculation. At the output of the 200-MHz amplifier, the load is also 50 ohms. Because the dc drain voltage must be blocked from the load, a series matching capacitor was selected which performs both dc blocking and resistive matching simultaneously.

In the actual load-circuit network shown in Fig.13(a), the value of capacitor C_S must be chosen so that the load admittance, $y_L = 20$ millimhos, is apparently equal to the real part of the transistor output admittance, $Re(y_{22}) = 0.28$ millimhos. Fig.13(b) shows the equivalent circuit of the load-circuit network for this condition.

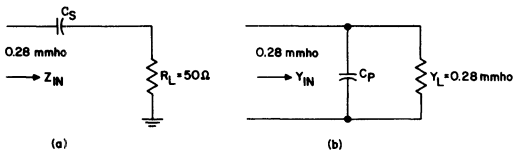


Fig.13 - Output network in which series coupling capacitance is used for dc-voltage blocking and resistive matching: (a) actual network; (b) electrical equivalent.

The following equation gives the input impedance Z_{IN} for the network shown in Fig.13:

$$Z_{IN} = R_S + \frac{1}{j\omega C_S} \quad (11)$$

The input admittance y_{IN}, therefore, may be expressed as follows:

$$y_{IN} = \frac{1}{R_p} + j\omega C_p = \frac{1}{Z_{IN}} = \frac{1}{R_S + \frac{1}{j\omega C_S}} \quad (12)$$

The terms in Eq.(12) are rearranged to obtain the following result:

$$\frac{R_S}{R_p} + j\omega C_p R_S + \frac{1}{j\omega C_S R_p} + \frac{j\omega C_p}{j\omega C_S} = 1 \quad (13)$$

The real and imaginary terms in Eq.(13) are equated to obtain the following relationships:

$$\frac{R_S}{R_p} + \frac{C_p}{C_S} = 1 \tag{14}$$

$$\omega C_p R_S - \frac{1}{\omega C_S R_p} = 0 \tag{15}$$

$$C_p = \frac{1}{(\omega C_S R_p)(\omega R_S)} \tag{16}$$

Eq.(16) is substituted into Eq.(14) to obtain the following equation for the matching capacitance C_S:

$$C_S = \frac{1}{\omega}\sqrt{\frac{1}{(R_p - R_S)R_S}} \tag{17}$$

Substitution of numerical values for the parameters in Eq.(17) yields the following value for C_S:

$$C_S = \frac{1}{2\pi(2 \times 10^8)}\sqrt{\frac{1}{(3600-50)50}} = 1.9 \text{ pF}$$

Experimentally, a 3-picofarad capacitor was found to perform very satisfactorily in the amplifier. If $R_p >> R_S$, then $C_p \approx C_S$. Therefore, a 3-picofarad capacitance appears in parallel with the 1.4-picofarad capacitance of the MOS transistor. A small 1-to-9-picofarad variable air capacitor was selected for the tank tuning capacitor to compensate for variations among transistors. For a nominal value of 2 picofarads for the air capacitor, the total output capacitance is 6.4 picofarads. The inductance required to resonate with 6.4 picofarads at 200 MHz is 0.1 microhenry. When the total output capacitance is known, the required neutralization capacitor can be calculated. If C_1 is arbitrarily selected as 33 picofarads, the neutralization is determined from Eq.(8), as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) = 0.2\left(\frac{33}{6.4}\right) = 1.0 \text{ pF}$$

The optimum value for the neutralization capacitor was determined experimentally by use of a small (0.5-to-3-picofarad) variable capacitor. This capacitor was adjusted to the optimum value for a typical unit (C_{rss} = 0.13 pF) and then fixed. The required input inductance was found to be 0.06 microhenry. The completed amplifier is shown schematically in Fig.3. The bandwidth of the amplifier is typically 8 MHz and shows negligible skew.

The y parameters may also be used to design a cascode vhf amplifier such as the one shown in Fig.5. This circuit had typical power gain and noise figure of 17 dB and 4.2 dB, respectively. The amplifier has a bandwidth of 10 MHz with negligible skew. The capacitance of the $source_2$-$drain_1$ interconnection must be tuned out to achieve a good vhf noise figure. The noise figure of the cascode amplifier is 2 to 3 dB higher if this capacitance is not tuned out.

References

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3 A. P. Stern, "Stability and Power Gain of Tuned Transistor Amplifiers," **Proceedings of the IRE**, March 1957.

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VHF Mixer Design Using the RCA-3N128 MOS Transistor

by

F. M. Carlson

The 3N128 is a vhf MOS field-effect transistor suitable for use throughout the vhf band (30 to 300 MHz) as an amplifier, mixer, or oscillator. This Note discusses some of the design criteria pertinent to the construction of MOS mixers, and presents an example of a complete vhf MOS converter.

Mixer Design Considerations

The conversion gain obtained from a mixer is the ratio of intermediate-frequency (if) power output divided by the radio-frequency (rf) power input. This conversion gain CG is usually expressed in dB, as follows:

$$CG = 10 \log \frac{\text{if } P_{out}}{\text{rf } P_{in}}$$

The value of CG approximates the gain of the active device operated as an amplifier (unneutralized) at the intermediate frequency, minus the rf losses at the input of the device. Practical mixers normally have a conversion gain of 3 to 5 dB less than their if-amplifier gain.

The 3N128 transistor has good gain and noise figure throughout the vhf band. Because it also has a nonlinear region of operation, it may be used as a vhf mixer to provide good conversion gain. The transfer function of the 3N128, shown in Fig.1, indicates that the maximum nonlinearities occur at a drain current of about 1.5 milliampere. At drain currents above approximately 5 milliamperes, the transfer function starts to become linear. No mixing action can occur if the transfer function is perfectly linear. Because the amplifier gain of the 3N128 is higher at 5 milliamperes than at 1.5 milliamperes, the best bias point for an MOS mixer is a compromise between the region where best mixing occurs and the region where optimum if power gain occurs. For the 3N128, this point is empirically determined to be between 3.5 and 4.5 milliamperes.

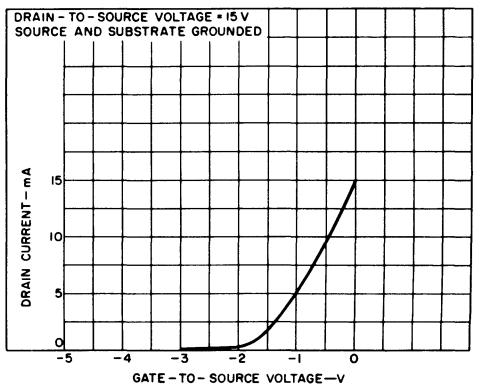


Fig.1 - Drain current as a function of gate-to-source voltage for the 3N128 vhf MOS transistor.

The local-oscillator signal may be introduced into a 3N128 mixer at the insulated gate, the source, or the junction gate (substrate). Application of the oscillator signal to the junction gate can be very effective, but is not recommended because the junction gate of the

3N128 is tied to the case; placing the transistor case at local-oscillator signal potential can pose possible radiation problems.

Injection of the oscillator signal at the source is not desirable because the source should always be at rf/if ground for optimum gain, but could not be at ground at the oscillator frequency. Designing a network to meet these criteria is difficult and adds to the cost of the mixer.

Injection of the oscillator signal at the insulated gate is the least troublesome of the three methods. The local oscillator may be coupled to the insulated gate by means of an inductive loop or a small coupling capacitor.

The input circuit is normally designed for a conjugate match with the input impedance of the MOS transistor at the radio frequency. The output circuit is normally designed for a conjugate match with the output impedance of the 3N128 at the intermediate frequency, unless electrical instabilities (oscillations) occur, in which case the output circuit must be mismatched. Oscillations are not normally a problem in a 3N128 mixer, provided the if and rf signals are relatively far apart in frequency. Under these conditions, the output circuit presents a low impedance to the rf signal, and the input circuit presents a low impedance to the if signal; consequently, oscillations at either frequency are unlikely to occur.

Neutralization is not generally used in mixers because of the different frequencies at the output and the input.

Design Example

A vhf receiver "front end" has been designed and built to demonstrate the preceding design considerations and to illustrate the use of the 3N128 vhf MOS transistor in all four stages: rf, mixer, if, and local oscillator. The complete converter, shown in Fig.2, uses an rf input frequency of 200 MHz and an if output frequency of 30 MHz.

The input stage is a straight-through 200-MHz amplifier* employing a source resistor for gate bias. This configuration permits the gate to be at dc ground, and greatly reduces the possibility of damage to the MOS gate from input transients. The 240-ohm resistor allows a current of approximately 5 milliamperes to flow through the device so that maximum vhf power gain is obtained. A variable inductor resonates with the output capacitance of the 3N128 to provide a bandwidth of approximately 12 MHz for the rf stage alone. (Narrower bandwidth could have been obtained by use of more capacitance in the tuned circuits and different loading on the output circuit; however, no particular effort was made to achieve very narrow bandwidth because a wide bandwidth is desirable in some applications.) Capacitive bridge neutralization is used to achieve the maximum allowable stage gain of 20 dB for the particular 3N128 used.

The input coil of the mixer stage is designed to permit a conjugate match with the transistor input admittance. The input admittance y_{11} of the 3N128 at 200 MHz is approximately 0.45 + j 7.2 millimhos. Therefore, an admittance of y_{11}* (=0.45 - j 7.2 milli-

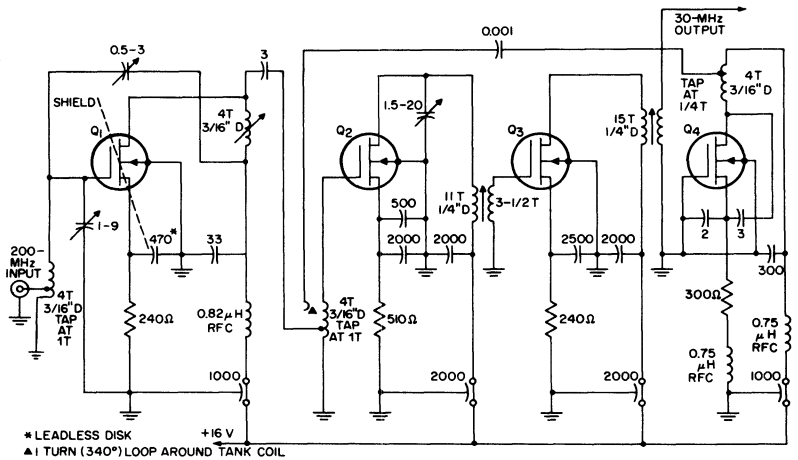


Fig.2 - VHF receiver "front end" using the 3N128 in all stages.

* Design information for vhf MOS amplifiers is given in RCA Application Note AN-3193: "Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor," by F.M. Carlson, August 1966.

mhos) should be presented to the mixer input. A conjugate match is not used at the output because it is desirable to load the input of the following (if) stage for stability. Therefore, a step-down transformer is used. (A conjugate match would require use of a step-up transformer because $g_{11} > g_{22}$ at 30 MHz.)

The local oscillator is coupled into the insulated gate of the mixer by means of an ungrounded 340-degree loop placed around the input tank coil at its high-impedance end. A small coupling capacitor could also be used for this purpose. Local-oscillator amplitude is approximately 1.4 volts rms into the coupling loop. Power gain of the mixer stage is 16 dB. Fig.3 shows the conversion gain of the mixer as a function of local-oscillator amplitude. A lower oscillator level than 1.1 volts would probably be desirable if spurious output frequencies were found to be troublesome.

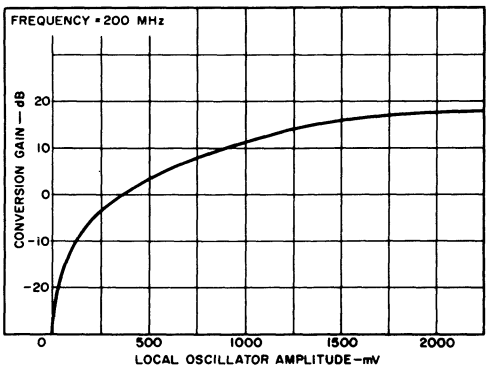


Fig.3 - Conversion gain of the mixer stage in Fig.2 as a function of local-oscillator amplitude.

A 510-ohm source resistor is used in the mixer stage to provide a drain current of 4 milliamperes. (This value is larger than would normally be expected for a drain current of this level because the gate is subjected to large signal excursions by the local oscillator.)

The maximum available gain (MAG) of the 3N128 at 30 MHz in a conjugately matched circuit (with y_{12} assumed to be approximately zero) may be computed from the y-parameters for the device, as follows:

$$MAG = \frac{|y21|^2}{4\, g_{11}\, g_{22}} = \frac{|7.2|^2}{4(0.03)(0.12)} = 3610 = 35.6 \text{ dB}$$

The maximum usable gain (MUG) of the 3N128 in an unneutralized 30-MHz amplifier is computed as follows:

$$MUG = \frac{0.4\, g_m}{\omega C_{rss}} = \frac{(0.4)(7.2)(10^{-3})}{(2\pi)(30)\,10^6\,(0.13)\,10^{-12}} = 118 = 20.7 \text{ dB}$$

If the 30-MHz stage is operated at a gain significantly above the MUG value, the possibility of circuit oscillation exists. Therefore, the input of the if stage is mismatched to reduce the stage gain from the MAG level to about 20 dB. (In some cases, it may be easier to mismatch at the output than at the input.) The output of the if stage is transformer-coupled to a 50-ohm load.

The local-oscillator stage is a Colpitts circuit in which frequency is adjusted by means of a slug-tuned inductor.

The complete converter has a power gain of 56 dB, a noise figure of 3 dB, and a bandwidth of 1.5 MHz. Spurious responses (referred to a level of 0 dB at the 200-MHz input frequency) are -51 dB at 100 MHz, -36 dB at 215 MHz, and -35 dB at 260 MHz. These spurious responses could be greatly improved by use of a narrower bandwidth in the rf stage; the present bandwidth is 12 MHz at the 3-dB points.

Table I shows measurements of cross-modulation of the converter as a function of frequency.

Interfering Frequency (MHz)	Interfering Signal Voltage Necessary for 1% Cross-Modulation (mV)
50	160
90	115
100	87
110	98
120	97
130	87
140	78
150	77
160	65
170	52
180	39
190	9

Table I - Cross-modulation of MOS mixer.

Chopper Circuits Using RCA MOS Field-Effect Transistors

by

F. M. Carlson

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but eliminate their inherent offset-voltage and leakage-current problems.

Basic Chopper Circuits

Chopper circuits are basically of either the shunt type or the series type, as shown in Fig. 1, or a combination of the two.

The shunt chopper circuit, shown in Fig. 1(a), operates as follows: When the switch S is opened, a voltage that is directly proportional to the input signal appears across the load. When the switch is closed, all of the input signal is shorted to ground. Therefore, if the switch is opened and closed periodically, the voltage across the load appears as a square wave that has an amplitude directly porportional to the input signal. This square wave may be highly amplified by a relatively drift-free, stable-gain ac amplifier. This procedure is generally used in low-level dc amplifiers, i.e., a small dc input is chopped, the resulting ac signal is amplified, and the output of the ac amplifier is rectified to produce a dc output directly proportional to the input.

The series chopper circuit, shown in Fig. 1(b), can also be used to chop dc signals. This type of circuit is particularly useful in telemetry or other systems in which a signal source such as a transducer is to be connected periodically to a load such as a transmitter.

An ideal chopper is simply an on-off switch that has certain desirable characteristics. Table I lists

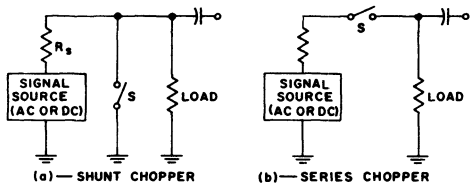


Fig. 1 - Basic chopper circuits.

Ideal Chopper Characteristics	Available Chopper Devices Compared to Ideal		
	MOS	Bipolar	Electromechanical Relay
Infinite Life	Good	Good	Poor
Infinite Frequency Response	Good	Good	Poor
Infinite OFF Resistance	Good	Fair	Good
Zero ON Resistance	Poor	Fair	Good
Zero Driving-Power Consumption	Good	Fair	Fair
Zero Offset Voltage	Good	Poor	Good
Zero Feedthrough between the driving signal and signal being chopped	Fair	Fair	Good
Small Size	Good	Good	Poor

Table I - Comparison of available chopper devices with an ideal.

some of these characteristics, and shows the relative merits of relays, bipolar transistors, and MOS transistors in each area.

Use of MOS Transistors as Choppers

Fig.2 shows voltage-current characteristics of an n-channel depletion-type MOS field-effect transistor such as the RCA-40460. Fig.3 shows an expanded view of the curves in Fig.2(a) in the region about the origin.

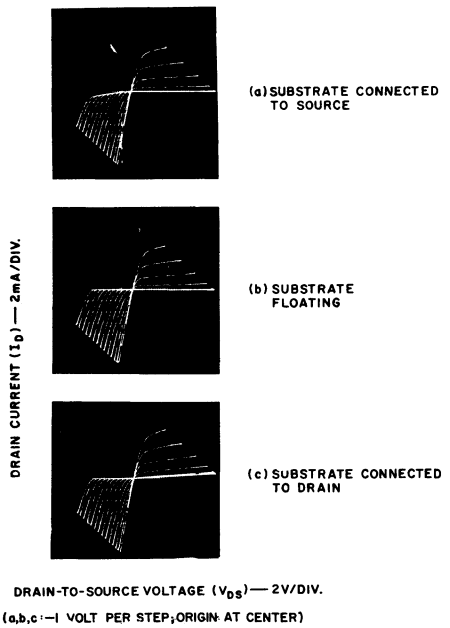


Fig.2 - Voltage-current characteristics of an n-channel depletion-type MOS transistor: (a) with substrate connected to source; (b) with substrate floating; (c) with substrate connected to drain.

Because each curve passes through the origin, the MOS transistor is said to have zero offset voltage. In an MOS shunt chopper circuit, therefore, the output is zero when the input voltage is zero. This result is not obtained with bipolar transistors. Even for zero input voltage, a bipolar transistor has an offset voltage equivalent to the collector-to-emitter saturation voltage $V_{CE}(sat)$ between its collector and emitter terminals. MOS transistors have no parameter comparable to $V_{CE}(sat)$.

When the gate-to-source voltage V_{GS} is zero, an MOS transistor such as the 40460 has an effective resistance of 200 to 300 ohms between its drain and source terminals. If the gate-to-source voltage is made positive, this resistance decreases to about 100 ohms (typically to 90 ohms for the 40460). No significant increase in gate current occurs when V_{GS} is made positive because the gate of an MOS transistor is insulated from the source-to-drain channel by an oxide layer. (In a junction-gate field-effect transistor, the gate and the channel form a p-n junction, and low gate current can be obtained only when this junction is reverse-biased.) When the resistance between the drain and source terminals is low (100 to 300 ohms), an MOS transistor is said to be ON; the drain-to-source channel resistance is then designated as $r_{ds}(ON)$. This ON condition corresponds to the closed-switch condition in the circuits of Fig.1.

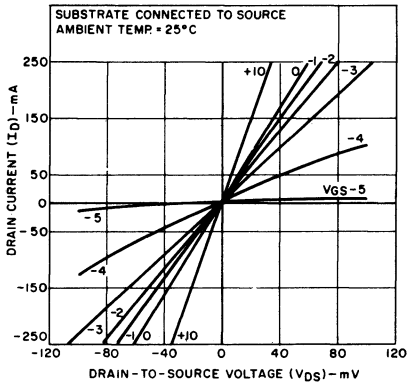


Fig.3 - Low-level drain current as a function of drain-to-source voltage in an n-channel depletion-type MOS transistor with substrate connected to source.

When a negative voltage of about -6 volts or more is applied between the gate and the source of the MOS transistor, the channel resistance between drain and source becomes extremely high (typically thousands of megohms). In this condition, which is known as "cutoff" or "pinchoff", it is impractical to measure the channel resistance directly; instead, the leakage current that flows from drain to source at cutoff is normally specified. This current $I_D(OFF)$, is typically 0.1 nanoampere for the 40460. Because $I_D(OFF)$ is measured at a drain-to-source voltage of 1 volt, the equivalent channel resistance is 10,000 megohms. This OFF condition corresponds to the open-switch condition in the circuits of Fig.1.

Fig.4 shows three basic chopper circuits using the MOS field-effect transistor. The gating signal for the 40460 should swing from zero to at least -6 volts, and may cover a range as large as ±10 volts. The substrate (and thus the case) of the 40460 transistor is usually connected to the source. However, if the incoming

signal to be chopped exceeds -0.3 volt, the substrate must be "floated", connected to the drain, or biased negatively so that the source-to-substrate and drain-to-substrate voltages never exceed -0.3 volt. If this value is exceeded, the substrate, which forms two p-n junctions with the drain and the source, becomes forward-biased and the resulting flow of diode current shunts the incoming signal to ground.

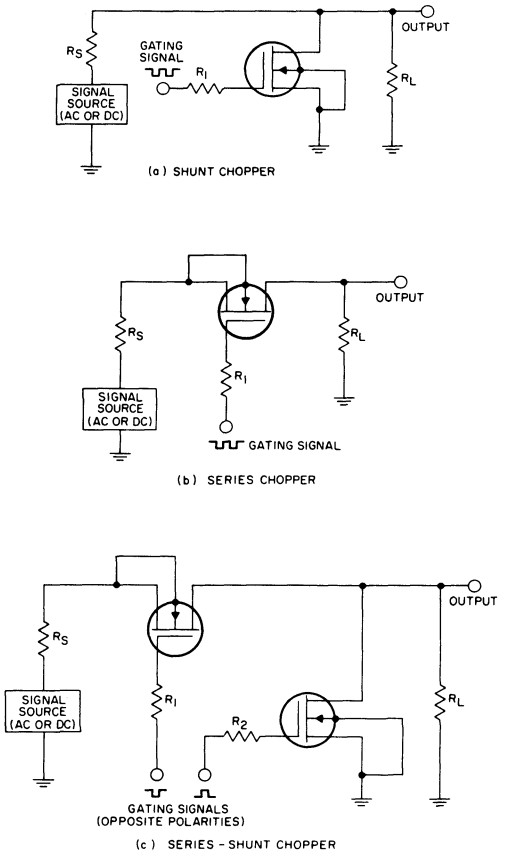


Fig.4 - Basic MOS chopper circuits.

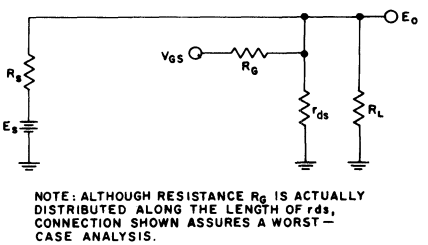
Steady-State Conditions

Ideally, when an MOS transistor in a shunt chopper circuit is ON, the output voltage of the circuit should be zero. Because the drain-to-source resistance r_{ds} is some finite value, however, the output cannot reach true zero. Fig.5 shows an equivalent circuit for steady-state conditions in an MOS shunt chopper. For the ON condition, the output voltage E_O is given by

$$E_O = E_S \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_S + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] \quad (1)$$

In Eq.(1), it is assumed that the gate leakage resistance R_G is much larger than the drain-to-source resistance r_{ds}. If the load resistance R_L is also much larger than r_{ds}; Eq.(1) can be simplified as follows:

$$E_O = E_S \left[\frac{r_{ds}}{R_S + r_{ds}} \right] \quad (2)$$



NOTE: ALTHOUGH RESISTANCE R_G IS ACTUALLY DISTRIBUTED ALONG THE LENGTH OF r_{ds}, CONNECTION SHOWN ASSURES A WORST-CASE ANALYSIS.

Fig.5 - Steady-state equivalent circuit of MOS shunt chopper.

For E_O to approach zero, it is necessary that the source resistance R_S be much greater than r_{ds}. The value of E_O is then given by

$$E_O = E_S (r_{ds}/R_S) \quad (3)$$

A typical value for R_S and R_L in an MOS shunt chopper is 0.1 megohm. A typical value of r_{ds}(ON) for the 40460 transistor is 90 ohms. If these values are substituted in Eq.(3) and the signal voltage E_S is assumed to be 1 millivolt, E_O is calculated as follows:

$$E_O = 10^{-3} (90/10^5) = 0.9 \text{ microvolt}$$

In the ON condition, therefore, the dc error voltage is less than 0.1 per cent for the values used, and is directly proportional to the input signal.

For the OFF condition, the steady-state output voltage E_O is given by

$$E_O = E_S \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_S + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] + V_{GS} \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_G + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] \quad (4)$$

In most MOS transistors, both $r_{ds}(OFF)$ and R_G are much greater than R_L. Therefore, Eq.(4) may be simplified as follows:

$$E_O = E_S \frac{R_L}{R_S + R_L} + V_{GS} \frac{R_L}{R_G} \qquad (5)$$

If R_S, R_L, and E_S are assumed to have the values used previously, the gate-to-source voltage V_{GS} is assumed to be -10 volts, and the gate resistance R_G is assumed to be 10^{12} ohms (minimum permissible gate resistance for the 40460), the value of E_O is calculated as follows:

$$E_O = 10^{-3}\left[\frac{10^5}{2 \times 10^5}\right] - 10 \left[\frac{10^5}{10^{12}}\right]$$

$$= \frac{10^{-3}}{2} - 10^{-6} \approx 0.5 \text{ millivolt}$$

The second term in Eq.(5) is the error term for the OFF condition; it is not proportional to the input signal E_S. For the numbers used, the output error in the OFF condition is only 0.2 per cent. If a typical value of 10^{14} ohms is used for the 40460 gate resistance instead of the minimum value of 10^{12} ohms, the error voltage is reduced to only 0.002 per cent. The output error remains small for any value of signal voltage E_S that does not approach the error voltage in magnitude.

Because the error voltage is inversely proportional to the gate leakage resistance R_G, most junction gate field-effect transistors produce larger error voltages than MOS transistors (the minimum R_G of most junction-gate devices is only 1 to 10 per cent that of MOS transistors).

A similar procedure may be used for analysis of series chopper and series-shunt chopper circuits.

The operation of all MOS chopper circuits is greatly affected by the magnitude of the source and load resistances. Table II lists the output voltages of the three basic chopper circuits for various combinations of source and load resistances. It is assumed that the input voltage E_S is 1 millivolt, and that the drain-to-source resistance r_{ds} is 100 ohms in the ON condition and 1000 megohms in the OFF position. The gate leakage resistance R_G (10^{12} ohms or more) is neglected. The following conclusions can be drawn from the data shown:

1. Only the series or the series-shunt circuit should be used when $R_S < r_{ds}(ON)$.
2. In general, R_L should be high. ($R_L >> r_{ds}(ON)$)
3. The load resistance should be higher than the source resistance. ($R_L \geq R_S$)
4. The performance of the series-shunt circuit is equal to or better than that of either the series or the shunt chopper alone for any combination of R_S and R_L.

Source Resistance R_S (ohms)	Load Resistance R_L (ohms)	Approximate Output Voltage E_o - μV (Max. Output = 1 mV) Shunt Chopper (ON)	Shunt Chopper (OFF)	Series Chopper (ON)	Series Chopper (OFF)	Series-Shunt Chopper (ON)	Series-Shunt Chopper (OFF)
1 M	1 M	0.1	500	500	1	500	0.0001
100 K	1 M	1	900	900	1	900	0.0001
100	1 M	500	1000	1000	1	1000	0.0001
0	1 M	1000	1000	1000	1	1000	0.0001
1 M	100 K	0.1	90	90	0.1	90	0.0001
1 M	100	0.05	0.1	0.1	0.0001	0.1	0.00005
100 K	100 K	1	500	500	0.1	500	0.0001
100	100	333	500	333	0.0001	333	0.00005

Table II - Steady-state chopper output voltage for various source and load resistances.

Transient Conditions

Fig.6 shows the ac equivalent circuit of an MOS shunt chopper. The interelectrode capacitances of the MOS transistor affect operation of the circuit at high frequencies. The input capacitance C_{gs} increases the rise time of the gate driving signal and thus increases the switching time of the chopper. This effect is not usually a serious limitation, however, because the switching time of the MOS transistor depends primarily on the input and output time constants. Switching times as short as 10 nanoseconds can be achieved when an MOS transistor is driven from a low-impedance generator and the load resistance is less than about 2000 ohms.

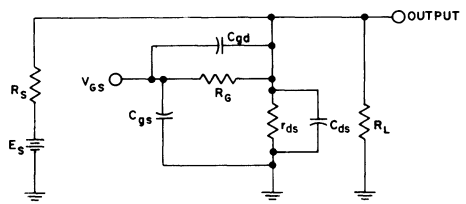


Fig.6 - AC equivalent circuit of MOS shunt chopper.

The output capacitance C_{ds} also tends to limit the maximum frequency that can be chopped. When the reactance of this capacitance becomes much lower than the load resistance R_L, the chopper becomes ineffective because $X_{C_{ds}}$ is essentially in parallel with R_L and $r_{ds}(OFF)$.

The feedthrough capacitance C_{gd} is the most important of the three interelectrode capacitances because it couples a portion of the gate drive signal into the load circuit and causes a voltage spike to appear across R_L each time the gate drive signal changes state. C_{gd} and R_L form a differentiating network which allows the leading edge of the gate drive signal to pass through. The output capacitance C_{ds} is beneficial to the extent that it helps reduce the amplitude of the feedthrough spike.

The effect of the feedthrough spikes can be reduced by several methods. Typical approaches include the following:

(a) use of a clipping network on the output when the input signal to be chopped is fixed in amplitude,

(b) use of a low chopping frequency,

(c) use of an MOS transistor that has a low feedthrough capacitance C_{gd} (some RCA MOS transistors have typical C_{gd} values as low as 0.13 picofarad),

(d) use of a gate drive signal that has poor rise and fall times,

(e) use of a source and load resistance as low as feasible,

(f) use of a shield between the gate and drain leads,

(g) use of a series-shunt chopper circuit.

Temperature Variations

The variation of MOS transistor parameters with temperature can affect the operation of a chopper circuit unless allowance is made for such variations in the circuit design. It is important, therefore, to determine the approximate degree to which each parameter can be expected to change with temperature. Fig.7 shows curves of channel resistance r_{ds}, gate leakage current

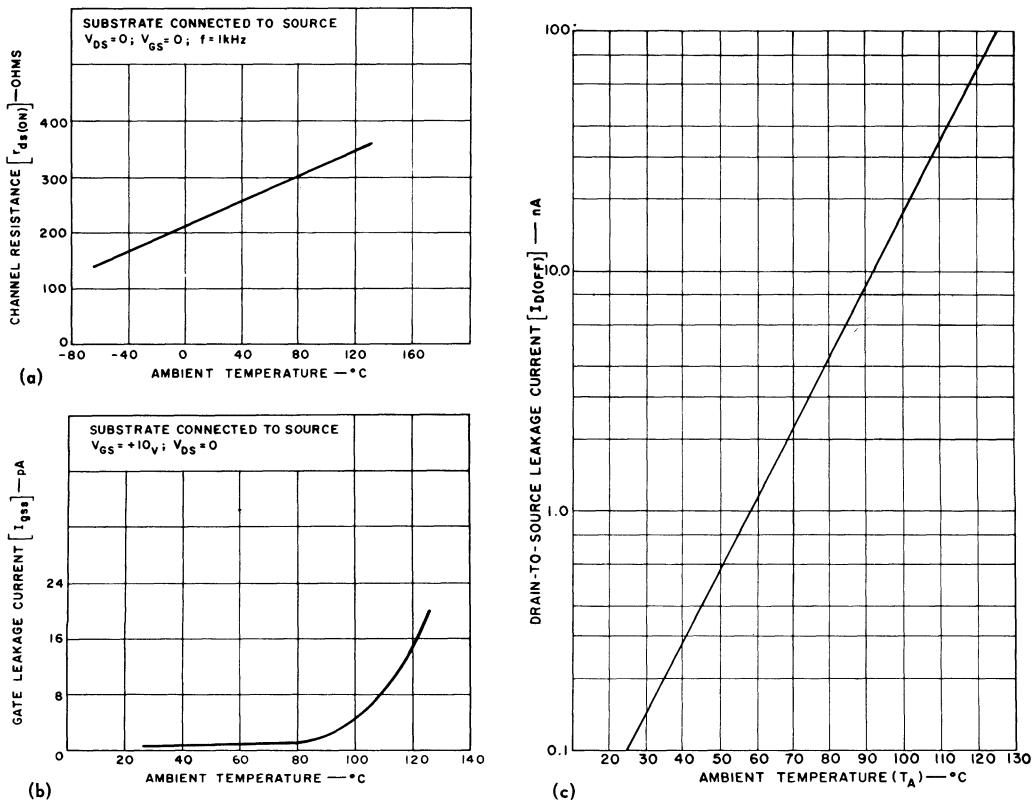


Fig.7 - Variation of 40460 parameters with ambient temperature: (a) channel resistance r_{ds}; (b) gate leakage current I_{gss}; (c) drain-to-source leakage current $I_{D(OFF)}$.

I_{GSS}, and drain-to-source leakage current $I_{D(OFF)}$ as a function of temperature for the 40460. I_{GSS} and $I_{D(OFF)}$ were not measured at temperatures below 25° C because condensation and frost that form on the test chassis result in erroneous and/or erratic readings of pico-ampere currents. Test circuits used to measure these parameters are shown in the Appendix.

Typical Circuits

Fig.8 shows three chopper circuits that were constructed for demonstration purposes: (a) a shunt chopper, (b) a series chopper, and (c) an ac chopper. The 0.005-microfarad capacitor across the gate drive generator in

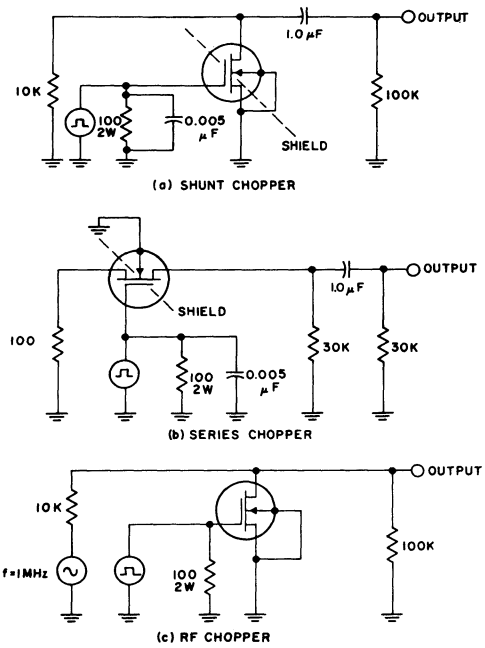


Fig.8 - Typical MOS chopper circuits: (a) shunt chopper; (b) series chopper; (c) rf chopper.

circuits (a) and (b) increases the rise time of the gate drive signal. A resistor is used in each circuit to simulate the impedance of the signal source. The actual input voltage was set at zero so that spike feedthrough and offset voltages could be measured. The dc offset voltage, which is caused primarily by the average value of the spikes over the whole cycle, was too small to be measured on the equipment available. Fig.9 shows the actual spike feedthrough for the 40460 and 3N128 MOS transistors in the shunt and series circuits of Figs.8(a) and 8(b); the rise time of the gate drive signal was 1 microsecond.

It is recommended that MOS choppers be driven from a square-wave source. Fig.10 shows the feedthrough that results when the circuits of Figs.8(a) and 8(b) are driven from a sine-wave generator instead of a square wave.

Fig.11 shows how the circuit of Fig.8(c) can be used to chop an rf signal at either a slow or a fast chopping frequency. The 40460 transistor can be used to chop rf signals extending up to the low vhf region. The frequency of the gate drive signal can be as high as several hundred kilohertz before excessive degradation of the square wave occurs. The rise time of the

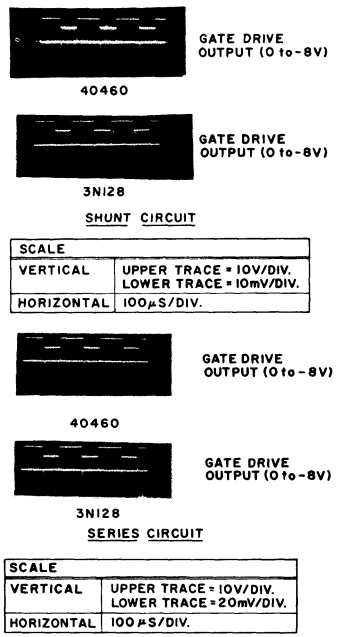


Fig.9 - Actual spike feedthrough in shunt and series chopper circuits employing the 40460 and 3N128 MOS transistors.

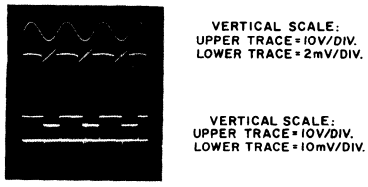


Fig.10 - Comparison of sine- and square-wave gate drive for an MOS shunt chopper employing the 40460.

gate drive signal for the circuit of Fig. 8(c) was 15 nanoseconds.

In field-effect-transistor choppers using a version of the series-shunt circuit shown in Fig.8(c), noise and offset voltages as low as 10 microvolts or less have been obtained.[1] Balanced MOS chopper circuits using special compensating networks have also been developed to chop 0.1-microvolt signals at impedance levels up to 40,000 ohms and chopping frequencies up to 250 Hz.[2]



Fig.11 - Results of using MOS rf chopper at a fast and a slow chopping frequency.

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1. "Airpax Electronics", ELECTRONICS, March 20, 1967, page 61.
2. J.J. Hitt and G. Mosley, "FET Chopper Circuits for Low-Level Signals", 1967 IEEE CONVENTION DIGEST, page 488.

APPENDIX

Test Circuits

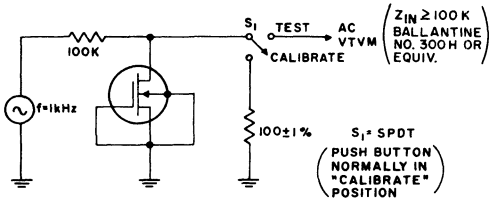


Fig.A-1 - Channel resistance ($r_{ds}(ON)$) measurement circuit.

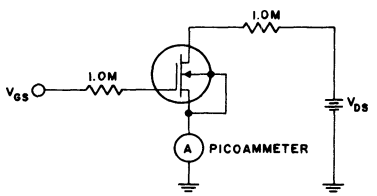


Fig.A-2 - Cutoff current ($I_D(OFF)$) measurement circuit.

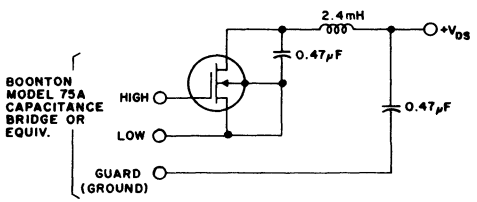


Fig.A-3 - Input capacitance (C_{iss}) measurement circuit.

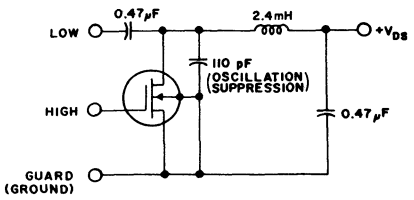


Fig.A-4 - Reverse transfer (Feedback) capacitance (C_{rss}) measurement circuit.

An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier

by

H. M. Kleinman and C. H. Lee

Previous work with field-effect transistors in general, and MOS field-effect transistors in particular, has demonstrated the superior signal-handling capability of this type of device.[1-3] This Note describes an FM tuner that incorporates an MOS field-effect transistor as the rf amplifier, and shows how the MOS transistor is instrumental in minimizing the spurious responses normally found in FM receivers.

Spurious responses result when harmonics of an unwanted incoming signal mix with harmonics of the local-oscillator signal to produce a difference frequency which falls within the if passband of the receiver.* When these harmonics of unwanted signals are created in the rf amplifier, they may be removed by improved filtering between the rf amplifier and the mixer. When used as an rf amplifier, the MOS transistor produces an output signal that contains low levels of the harmonics of unwanted signals. As a result, the need for a double-tuned rf interstage transformer is reduced and acceptable performance can generally be achieved with single-tuned circuits in both the antenna and rf interstage sections.

The FM tuner described in this Note utilizes an RCA-40468 MOS rf amplifier, an RCA-40478 bipolar mixer, and an RCA-40244 bipolar oscillator. The rf-stage gain of 12.7 dB and mixer gain of 21.8 dB yield a total tuner gain of 34.5 dB. A three-stage if-amplifier strip that uses RCA-40482 bipolar transistors and exhibits 94 dB of gain completes the FM tuner.

Table I summarizes the performance of the system. The figure shown for if rejection was achieved when the tuner section was tested with a fully shielded, remotely located if-amplifier strip. When the final tuner was assembled, only partial shielding was used around the if amplifier. This partial shielding, coupled with the close proximity of tuner and if amplifier, reduced the if rejection to 77 dB.

Carrier Frequency	100	MHz
Modulation	400 Hz, 22.5 kHz deviation	
Sensitivity:*		
For 20-dB signal-to-noise ratio	1.4	μV
For 30-dB signal-to-noise ratio	2.2	μV
For -3-dB limiting point (with 94-dB if strip)	1.6	μV
Image Rejection◆	72	dB
IF Rejection◆	91	dB
Half-IF Rejection◆	96	dB
Rejection of Other Spurious Responses◆ (with 0.2 volt at antenna terminals)	>100	dB

* Measured at antenna terminals (300-ohm nominal impedance).

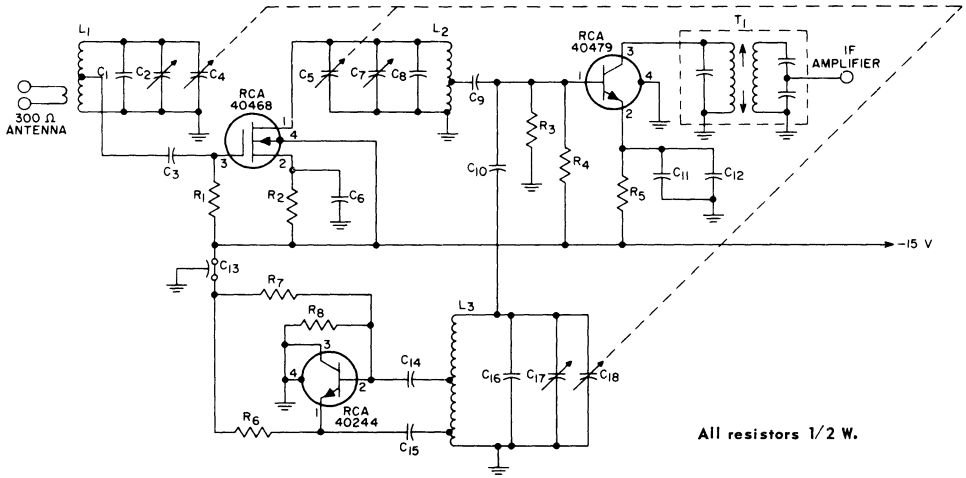
◆ Relative to 2 μV.

Table I - Over-all Tuner Performance

Circuit Considerations

The rf section of the tuner is shown in Fig.1, and the if strip in Fig.2. The if strip, which is described more fully elsewhere,[4] utilizes three 40482 bipolar transistors that operate at collector currents of 3.5

* In a receiver tuned to 100 MHz, the local oscillator is tuned to 110.7 MHz. The second harmonic of the local oscillator occurs at 221.4 MHz. A signal at a frequency of 210.7 MHz can beat with the 221.4-MHz signal to form the 10.7-MHz intermediate frequency. This 210.7-MHz frequency is the second harmonic of 105.35 MHz, which is above the desired channel by half the intermediate frequency.



R_1	= 100 KΩ	C_1, C_8, C_{16}	= 16 pF
R_2	= 220 KΩ	C_2, C_7	= 2-12 pF, Trimmer
R_3, R_4	= 47 KΩ	C_3, C_6	= 0.002 μF
R_5	= 4.7 KΩ	C_4, C_5, C_{18}	= 5.5-22.5 pF, ganged tuning capacitor
R_6	= 8.2 KΩ	C_9	= 5000 pF
R_7	= 120 KΩ	C_{10}	= 2.7 pF
R_8	= 22 KΩ	C_{11}	= 0.01 μF
		C_{12}, C_{14}, C_{15}	= 1000 pF
		C_{13}	= 1000 pF feedthrough type
		C_{17}	= 2-10 pF, Trimmer

L_1 = #18 bare copper wire, 4 turns, 1/4" I.D., 7/16" winding length, Q_o at 100 MHz = 130.
Tunes with 34 pF capacitance at 100 MHz.
Antenna Link approximately 1 turn from ground end.
Gate Tap approximately 1-1/2 turns from ground end.

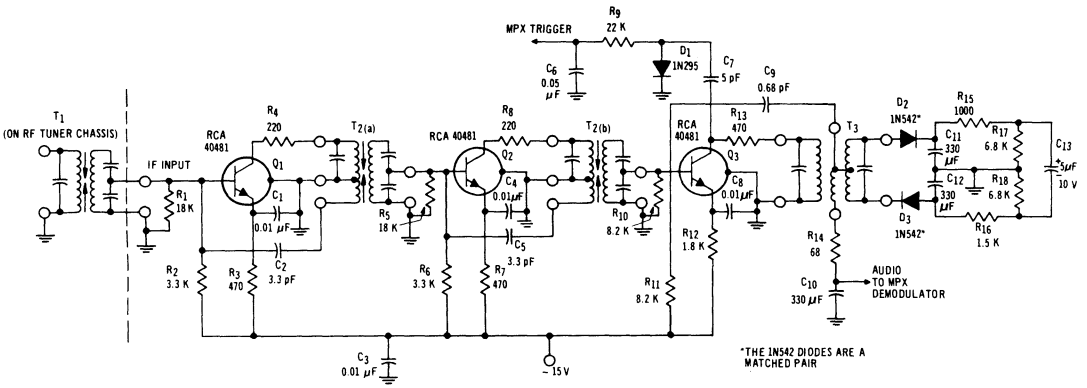
L_2 = #18 bare copper wire, 4 turns, 1/4" I.D., 7/16" winding length, Q_o at 100 MHz = 120.
Tunes with 34 pF capacitance at 100 MHz.
Base Tap approximately 3/4-turn.

L_3 = #18 bare copper wire, 4 turns, 7/32" I.D., 7/16" winding length, Q_o at 100 MHz =120.
Tunes with 34 pF capacitance at 100 MHz.
Emitter Tap approximately 1-1/2 turns from ground end.
Base Tap approximately 2 turns from ground end.

Fig.1 - Typical FM receiver front end using RCA-40468 MOS field-effect transistor.

milliamperes in neutralized configurations and provide an over-all if gain of 94 dB.

The rf section provides a total gain of 34.5 dB, which includes 12.7 dB in the rf stage and 21.8 dB in the mixer. The mixer and oscillator were designed according to principles established previously,[5,6] and details of their design are not discussed. The common-collector oscillator provides an extremely clean oscillator waveform. In addition, the low injection level at the mixer base, 25 to 30 millivolts, coupled with the design of the preceding circuits, limits the maximum possible signal at the mixer base and minimizes the generation of spurious responses in that stage.



T_1	TRW-EO-21124-RA
$T_{2(a)}$, $T_{2(b)}$	TRW-EO-21125-R1
T_3	TRW-EO-23023

All resistors 1/4 watt
0.01- and 0.05-μF capacitors, 50-V ceramic disks
330-pF capacitors, 1-kV disks

Fig.2 - Typical if-amplifier strip.

RF-Stage Design

The 40468 rf stage is designed to achieve the published maximum usable stable gain of 14 dB at a nominal operating point of 5 milliamperes. Additional losses of 1.3 dB reduce the actual gain in the tuner to 12.7 dB. Details of the rf-stage design are given in the Appendix.

Selection of the appropriate source and load impedances for the rf stage is based on the fact that a low spurious response requires the gate of the 40468 to be tapped as far down on the antenna coil as gain and noise considerations permit. This arrangement applies the smallest possible voltage swing to the gate and makes optimum use of the available dynamic range. (In a bipolar tuner designed to optimize the rejection of spurious responses, the tap point on the antenna coil was approximately 25 ohms.)

For low spurious response, therefore, the entire rf coil is used as the load for the 40468. The interstage coil presents a load impedance to the rf stage of 3800 ohms, which nearly matches the 4200-ohm output impedance of the 40468. Although this arrangement loads the interstage coil and causes a degradation of selectivity of the front end, it is an acceptable compromise in this case because the antenna coil is not loaded by the gate of the MOS transistor.

As indicated by the calculations in the Appendix, this approach yields a source impedance of approximately 200 ohms for the 4500-ohm input impedance of the gate of the 40468.

Tuner Performance

Performance of the tuner with respect to sensitivity limiting, if rejection, and image rejection compares favorably with that of tuners using high-performance bipolar transistors. Figs.3, 4, and 5 show typical performance characteristics of the receiver. Receiver performance, particularly as regards spurious-response-rejection figures, is highly dependent on such factors as physical layout, power-supply decoupling, and care in construction. The use of a negative supply voltage facilitates the grounding of tuned circuits and the decoupling of the supply.

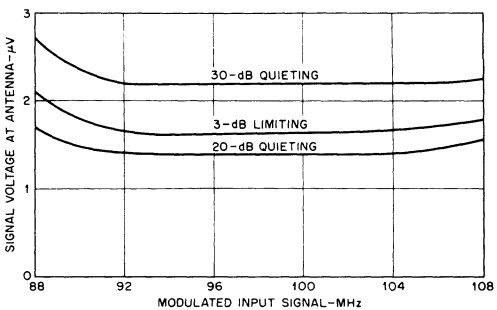


Fig.3 - Sensitivity curves for FM receiver using circuits of Figs.1 and 2.

The elimination of spurious response was the primary goal in this design. Generally, a circuit that has a low spurious response is difficult to reproduce. In some systems, the performance of such a circuit depends on the exact operating points of the transistors used; when the rf-amplifier transistor in Fig.1 was repeatedly changed, performance of the tuner remained essentially the same. The best correlation was found with the operating current of the transistor in the circuit. Fig.6 shows the change in the rejection of the "half-if" spurious response as a function of drain current for a

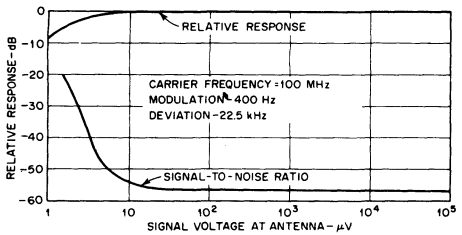


Fig.4 - Relative response as a function of signal voltage measured at antenna terminals.

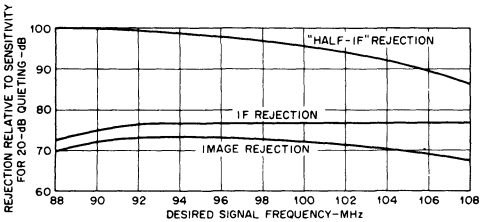


Fig.5 - Spurious-response rejection as a function of frequency.

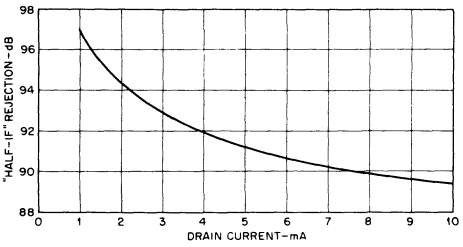


Fig.6 - Half-if rejection as a function of operating point.

typical 40468. For the normal spread of operating current in this circuit of 3.5 to 7 milliamperes, the variation in rejection is shown to be about ± 1 dB.

Fig.7 shows the variation of 20-dB quieting sensitivity as a function of drain current, and indicates why the 5-milliampere nominal operating point was chosen. Below 3 milliamperes, the sensitivity of the receiver degrades very rapidly. However, at 5 milliamperes the actual spread of 3.5 to 7 milliamperes causes a negligible change in performance.

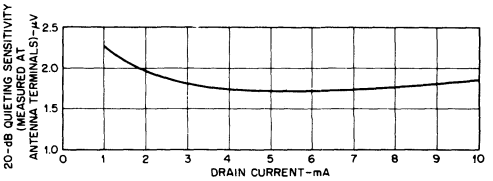


Fig.7 - 20-dB quieting sensitivity as a function of operating point.

Conclusions

The 40468 MOS field-effect transistor has been incorporated into an FM tuner in which all other stages are high-performance, low-capacitance bipolar types. The wider dynamic range of the MOS transistor provides significant improvements in the rejection of spurious responses over results previously achieved with bipolar rf amplifiers.

Most significantly, the performance with respect to spurious-response rejection has been repeated when devices with wide parameter variations have been used. Furthermore, the system has been duplicated with comparable results. These two factors strongly indicate that the performance advantages are real and are attributable to the characteristics of the MOS rf amplifier used rather than the result of cancellation or peculiar trapping in a single tuner.

Appendix - Design of 40468 RF-Amplifier Stage

The following parameters are important in the design of the rf-amplifier stage:

40468 parameters (at V_{DD} = 15 V, I_D = 5 mA):

input resistance R_{in}	4500	ohms
output resistance R_{out}	4200	ohms
forward transmittance y_{fs}	7500	μmhos
feedback capacitance C_{rss} (max).	0.2	pF

mixer-stage parameters:

input resistance R_{in}(mix)	550	ohms
input stability IS(mix) (from previous design)	4	

coil data:

mounted unloaded Q	120	
tuning capacitance C_T at 100 MHz	34	pF
antenna impedance	300	ohms

Fig.8 shows the ac equivalent circuit for the rf stage. At resonance, this circuit reduces to the form

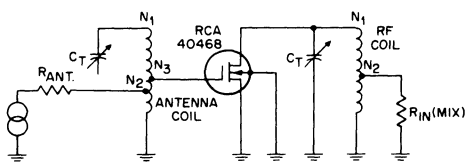


Fig.8 - AC equivalent circuit of the 40468 rf stage.

shown in Fig.9, where all impedances are referred to the gate and drain terminals of the 40468. The maximum available gain (MAG) is the gain in a conjugately matched, unilateralized circuit and is defined as follows:

$$MAG = \frac{|y_{fs}|^2 R_{in} R_{out}}{4} \quad (1)$$

For the values given above, MAG = 266 = 24.2 dB.

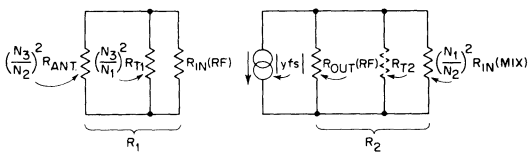


Fig.9 - Equivalent input (R_1) and output (R_2) circuit of the rf stage during resonance.

The maximum usable gain MUG is the stable gain which may be realized in a practical neutralized or unneutralized circuit. It is defined by the relationship for the unneutralized case as follows:

$$MUG = \frac{2|y_{fs}|}{\omega C_{rss}} \times \frac{a}{b} \quad (2)$$

where a is a skew factor smaller than unity which is used to maintain bandwidth, and b is a number equal to or greater than unity related to the number of stages (inserted to maintain bandwidth in multistage amplifiers). A skew factor of 0.2 is generally used. Because only one stage of 100-MHz gain is used in the amplifier shown in Fig.1, b = 1. For the values given, therefore, MUG is given by

$$MUG = \frac{0.4\, y_{fs}}{\omega C_{rss}} = 23.5 = 13.7 \text{ dB} \quad (3)$$

The total mismatch loss is called the stability factor S, and is equal to the difference (in dB) between MAG and MUG, as follows:

$$S = MAG - MUG = 10.5 \text{ dB, or } 11.3 \text{ times} \quad (4)$$

This value is arbitrarily divided between the input and output circuits by use of an input stability IS and an output stability OS, as follows:

$$IS = R_{in}/2R_1 \quad (5)$$

$$OS = R_{out}/2R_2 \quad (6)$$

where R_1 and R_2 are the total parallel impedances at the input terminal (gate) and the output terminal (drain), respectively. These stability terms are related to the stability factor S as follows:

$$S = IS \times OS \quad (7)$$

The division between IS and OS is made by means of some arbitrary choices. As mentioned previously, it was decided to maximize IS so that the signal level at the gate would be minimized. This choice necessitates matching or nearly matching R_{out} to its load. Therefore, the entire rf coil is used as the output load.

As indicated in Eq.(6), the value of R_2 must be determined to define OS; the value of IS can then be determined and the input circuit defined. R_2 consists of the parallel combination of R_{out}, R_{T2}, and $(N1/N2)^2 \times R_{in}$(mix), where R_{T2} is the tuned impedance of the rf coil and is given by

$$R_{T2} = Q_o/\omega_o C_t \quad (8)$$

The value of R_{out} is given above as 4200 ohms. The value of R_{T2} as calculated from Eq.(8) is 5600 ohms. The value of the input impedance of the mixer R_{in}(mix), obtained from the published data for the 40479, is 550 ohms. The only remaining component of R_2 to be determined is the turns ratio N_1/N_2.

In Fig.8, the rf coil L_2 represents both the input circuit of the mixer and the output circuit of the rf stage. Therefore, the stability of the mixer stage must also be considered. Because stability factors are equal to resistance ratios, the input stability of the

mixer can be considered at the top of the rf coil, as follows:

$$IS(mix) = \frac{(N_1/N_2)^2 R_{in(mix)}}{2R_2} \quad (9)$$

The value of IS(mix) was specified above as 4 (from a previous design). Because R_2 is a linear function of $(N_1/N_2)^2 R_{in(mix)}$, manipulation of the data through several steps provides a value of 5.5 for (N_1/N_2) and a reflected value of 16,800 ohms for $R_{in(mix)}$.

The output stability of the rf stage can then be determined. R_2 is computed as the parallel combination of R_{out}, R_{T2}, and $(N_1/N_2)^2 R_{in(mix)}$, and is found to be 2100 ohms. The output stability OS is determined from Eq.(6), as follows:

$$OS = R_{out}/2R_2 = 4200/(2 \times 2100) = 1$$

The value of unity indicates an impedance match between R_{out} and the load.

The input stability of the rf amplifier can then be determined from Eq.(7), as follows:

$$IS = S/OS = 11.3$$

By use of this stability term, the input-circuit constants can be calculated. R_1 is determined from Eq.(5), as follows:

$$R_1 = R_{in}/2IS = 191 \text{ ohms}$$

This value is so much lower than R_{in} that it is apparent the MOS transistor does not load the antenna coil at all.

Because it is desired to match the antenna with the input circuit, the value of R_1 should be one-half the reflected antenna impedance. Therefore, the value of $(N_3/N_2)^2 R_{ANT}$ is 382 ohms, which is a very slight step up. Because two of the three component terms of R_1 are then known, the remaining term $(N_3/N_1)^2 R_{T1}$ can be determined as 456 ohms. The turns ratios are then given by

$$N_1/N_2 = 4.3$$
$$N_1/N_3 = 3.7$$

The values of circuit components obtained by means of this design method are given in the parts list for Fig.1.

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An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

by

C.H. Lee and S. Reich

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response[1], dynamic range, noise immunity, gain, and feedthrough capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer. A conversion gain of 17.5 dB was obtained, to provide an over-all tuner gain of approximately 30 dB. RF and mixer circuit considerations pertinent to the design are discussed.

Performance Features of MOS Transistors

Spurious response in an FM tuner is caused by the mixture of unwanted signals with the desired carrier in either the rf stage or the mixer. This effect can be expressed mathematically by use of the Taylor series expansion of the simple transfer function of output current as a function of input voltage at the operating point, as follows:

$$i_o = I_o + \alpha e_s + \beta e_s^2 + \theta e_s^3 + \ldots \qquad (1)$$

where i_o is the instantaneous value of output current of the device; I_o is the dc component of output current; e_s is the rf signal voltage present at the input terminal of the transistor; and α, β, and θ are the coefficients of a Taylor series expansion. These coefficients are related to the first-, second-, and third-order derivatives of the transfer characteristic as determined by the bias point. It can be shown[2,3] that mixing action within the device is attributable to the second-order term (βe_s^2), and that cross-modulation and intermodulation result from third- and higher-order terms. Therefore, when a device has an inherent square-law transfer characteristic, i.e., the drain current varies as the square of the applied gate-to source voltage, third- and higher-order terms are zero and spurious response is eliminated. The transfer characteristic of MOS field-effect transistors more nearly approaches this ideal square-law relationship than the very steep exponential transfer characteristic of bipolar transistors.

The dynamic-range capability of MOS field-effect transistors is about 25 times greater than that of bipolar transistors. In an actual tuner circuit, this large intrinsic dynamic range is reduced by a factor proportional to the square of the circuit source impedances.[4] The net result is a practical dynamic range for MOS tuner circuits about five times that for bipolar types.

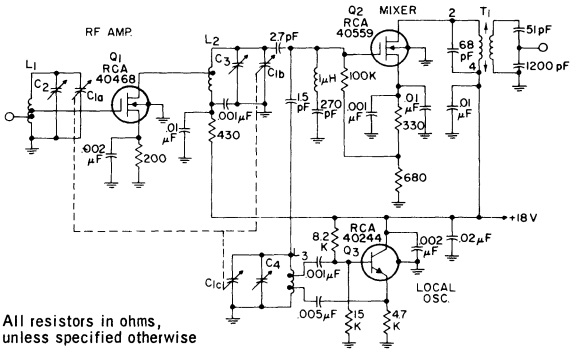
With MOS field-effect transistors, as contrasted with either bipolar transistors or junction-gate field-effect transistors, there is no loading of the input signal, nor drastic change of input capacitance even under extreme overdrive conditions.

In junction-gate field-effect transistors, a large incoming signal can have sufficiently high positive swing to drive the gate into conduction by a momentary forward bias; power is then drawn from the input signal in the same way as if a resistance were placed across the input circuit. In bipolar transistors, there is a gradual change of both input impedance and input capacitance as a function of large signal excursions. These changes are undesirable because they can result in detuning of tuned circuits and widening of the input selectivity curve.

FM Tuner Design

The FM tuner shown in Fig.1 uses single-gate MOS field-effect transistors in the rf-amplifier and mixer stages and a bipolar transistor as the local oscillator. The rf-amplifier transistor RCA-40468 operates in the common-source configuration with a stage gain of 12.7 dB. The mixer transistor RCA-40559 also operates in the common-source configuration, with both the rf and local-oscillator signals applied to the gate terminal. The bipolar oscillator transistor RCA-40244 operates in the common-collector mode. The conversion power gain from the mixer stage is 17.5 dB; the total gain of the tuner is 30.2 dB.

Performance of the FM tuner was evaluated by use of the bipolar-transistor if amplifier shown in Fig.2. The 10.7-MHz if output from the tuner is coupled to the first if-amplifier stage by means of a double-tuned transformer T_1. The if amplifier employs two 40245 and one 40246 bipolar transistors, each operating in a neutralized common-emitter configuration at a collector current of 3.5 milliamperes. The over-all gain of the if amplifier is 88 dB. A detailed analysis of a similar if amplifier is covered in an earlier publication.[5]



All resistors in ohms, unless specified otherwise

C_{1a}, C_{1b}, C_{1c} - 3-gang tuning capacitor, TRW 5-plate Model V2133 with trimmers stripped off.

C_2, C_3, C_4 - Arco 402 trimmer, maximum value 10 pF

L_1 - No.18 bare copper wire, 5 turns on 19/64" form, coil length 1/2", with IRN .250" x .250" Arnold slug. Q_0 = 164. Antenna tap at 0.8 of a turn, output tap at 1.4 turns.

L_2 - No.18 bare copper wire, 5 turns on 15/64" form, coil length 3/8", with 0.181" x 0.375" Arnold slug. Q_0 = 104.

L_3 - No.18 bare copper wire, 5 turns, air core with 3/8" O.D., coil length 1/2". Emitter tap on 1-1/2 turns. Feedback tap on 2 turns. Q = 164.

T_1 - Double tuned, 90 per cent of critical coupling. Primary unloaded uncoupled Q = 137 with 68-pF tuning capacitance, secondary unloaded uncoupled Q = 76 with 47-pF tuning capacitance. Secondary has a turns ratio of 26.2 to 1.0. Primary, No.32 enamel wire, 15 turns, space wound at 60 TPI, 0.250" x 0.500" TH slug. Secondary, No.36 enamel wire, 18 turns, close wound, 0.250" x 0.250" TH slug. Both coils on 9/32" form without shield.

Fig.1 - Circuit diagram of FM tuner using MOS transistors for the rf amplifier and mixer stages.

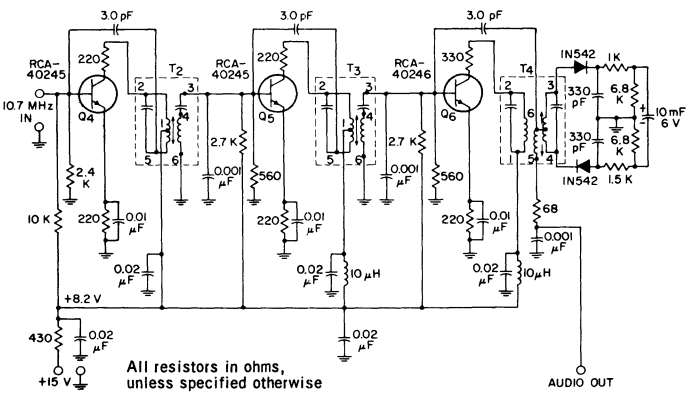


Fig.2 - Three-stage if amplifier using bipolar transistors.

Table I summarizes the performance of the MOS tuner. Spurious response was evaluated with a generator output of 350 millivolts.

OVER-ALL TUNER PERFORMANCE

Carrier Frequency	100	MHz
Modulation Frequency	400	Hz
Deviation (except IHFM)	22.5	kHz
Sensitivity:		
IHFM	1.75	μV
20-dB Quieting	1.5	μV
30-dB Quieting	1.75	μV
3-dB Limiting	2.5	μV
Image Rejection	62	dB
IF Rejection	96	dB
Half-IF Rejection	92	dB
Spurious Response across VHF band with $e_{gen.}$ = 0.35 volt	NONE	

Table I - Over-all performance characteristics of FM tuner.

RF-Circuit Considerations

The RCA-40468 MOS transistor used in the rf amplifier stage has a maximum available gain of 24 dB. Because the design criteria required a total mismatch plus insertion loss of 11.3 dB, the net gain for the stage is 12.7 dB. Although the design procedure used for these calculations has been discussed previously,[1,6] some of the considerations for optimizing performance warrant additional comment.

In the design of an rf stage for FM performance, the stage gain should be a compromise between optimum receiver sensitivity and spurious response rejection. In other words, the rf gain capability should be large to minimize the effects of noise from the mixer, and yet be limited to prevent a very large undesired incoming signal located on the skirt of the selectivity curve from driving the mixer beyond its dynamic range. Good FM tuner performance is achieved by selection of the proper rf-stage gain and step-down to the mixer input.

The rf input coil L_1 is tapped down to provide the smallest practical input swing to the gate of the rf-amplifier transistor for increased dynamic range. This tap-down is a compromise between optimizing for dynamic range and noise. When the degree of mismatch has been established, the drain-circuit load L_2 is determined from stage-gain and bandwidth requirements. Table II shows the device parameters used for the design of the rf stage.

The 40468 MOS transistor has a typical feedback capacitance of 0.12 picofarad, with a maximum value of 0.2 picofarad. This small value of C_{rss} minimizes oscillator radiation feedback through the device, and also makes it unnecessary to add neutralization components to the rf stage to achieve adequate gain.

Mixer-Circuit Considerations

The mixer circuit shown in Fig.1 is designed for operation into an 8000-ohm load. A load up to 12,000 ohms is permissible and provides a gain increase of about 1 dB from the mixer. The input circuit is tapped down by a 2.7-picofarad capacitor in series with the device input capacitance to improve dynamic range. These mismatch losses result in a stage gain of 17.5 dB, as compared to the maximum available gain of 21.5 dB shown in the published data for the 40559 transistor.

The trap consisting of a 1-microhenry inductor and 270-picofarad capacitor is designed to bypass any 10.7-MHz component that may appear at the input to the mixer. A 1.5-picofarad capacitor couples the oscillator signal to the mixer gate. Because the capacitor is small, interaction with the oscillator tuned circuit is minimized and good oscillator stability is maintained. The injection level at the gate of the mixer is 700 millivolts rms.

The biasing arrangement for the mixer stage is particularly important: substrate bias is used to provide the optimum combination of mixing and spurious-response rejection. Fig.3 shows the shift of the transfer characteristic as a function of negative substrate bias E_{bs} for the RCA-40559 mixer transistor.

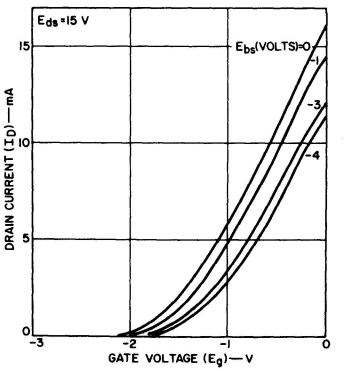


Fig.3 - Transfer characteristics of the RCA-40559 MOS field-effect transistor for several values of substrate bias.

The transconductance, which is the first derivative of the transfer characteristic, also varies as a function of substrate bias, as shown in Fig.4. As stated previously, mixing is accomplished by means of the quadratic term of Eq.(1); higher-order terms contribute only to undesired responses. For ideal mixing, therefore, the

transconductance curve should approach a straight line. As the transconductance curve becomes linear, higher-order derivatives (i.e., above the second) reduce to zero and the conversion transconductance increases. Fig.4 shows that the transconductance curve is most linear at

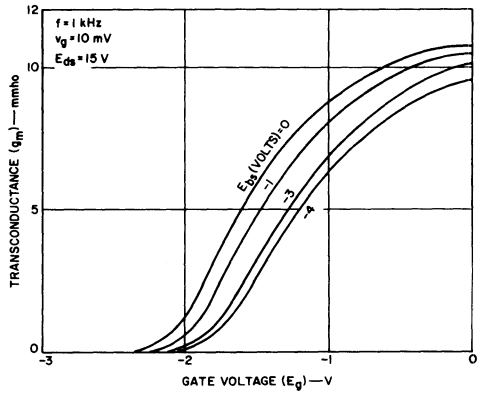


Fig.4 - Transconductance of the RCA-40559 as a function of gate bias with the substrate voltage as the parameter.

a substrate bias of -3 volts. Fig.5 shows the relative conversion gain of the RCA-40559 mixer stage as a function of the oscillator injection level at substrate bias of zero and -3 volts. It can be seen that the conversion transconductance also increases with the oscillator injection level.

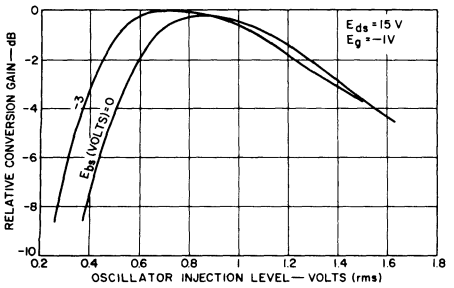


Fig.5 - Conversion transconductance as a function of oscillator injection level.

Table II shows the MOS device characteristics measured under circuit conditions. Reasonable verification of the measured conversion transconductance was obtained by calculation of the conversion transconductance for gate voltages ranging from zero to -2.1 volts. Details of these measurements are given in the Appendix.

Parameter	Units	RF Amplifier RCA-40468	Mixer RCA-40559
C_{rss}	pF	0.12	0.12
R_{in}	KΩ	4.5	6 (100 MHz)
C_{in}	pF	5.5	5.0
R_o	KΩ	4.2	12 (10.7 MHz)
C_o	pF	1.4	1.5
y_{21}	mmho	7.5	2.8
MAG	dB	24.2	21.5
MUG (unneutralized)	dB	14	-
G_p (in tuner)	dB	12.7	17.5

Table II - Device parameters for RCA-40468 and 40559 MOS field-effect transistors.

On the basis of these results, the optimum operating conditions for the mixer circuit were empirically established at an effective gate bias of -1 volt and an effective substrate bias of -3 volts to provide a typical drain current of 3 milliamperes.

Oscillator-Circuit Considerations

The common-collector oscillator circuit shown in Fig.1 generates an extremely clean output waveform. The absence of harmonics in the oscillator signal is an important factor in good tuner design. The oscillator signal is coupled to the mixer gate by means of a 1.5-picofarad capacitor which isolates the tuned circuit of the oscillator from the input circuit of the mixer and thus minimizes the possibility of oscillator instabilities as a result of "pulling".

Over-all Tuner Performance

The performance of the single-gate MOS tuner with respect to sensitivity, limiting, and particularly spurious response exceeds that obtained with the best bipolar transistors. In general, spurious-response performance can be degraded by inadequate circuit layout and wiring practices. For this reason, care should be exercised in arranging the physical layout of the tuner, and power-supply decoupling should be used.

Figs.6 and 7 show the measured sensitivity of the tuner of Fig.1. The quieting sensitivity, shown in Fig.6, is practically flat across the entire FM band. IHFM sensitivity and 3-dB limiting, shown in Fig.7, show the same excellent performance. The IHFM sensitivity test input voltage, as defined by the Institute of High Fidelity Manufacturers, is the minimum 100-per-cent-modulated signal input which, when applied to a receiver through the standard 300-ohm dummy antenna and an audio voltmeter connected through a 400-Hz filter, re-

duces a total internal receiver noise and distortion to the point where the output rises 30 dB when the 400-Hz null filter is removed from the audio voltmeter circuit. This value is expressed in microvolts.

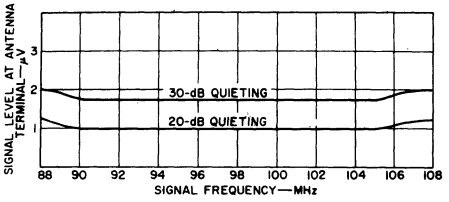


Fig.6 - Signal level for 20- and 30-dB quieting as a function of signal frequency.

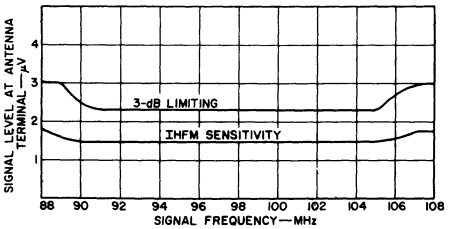


Fig.7 - Signal level for 3-dB limiting and IHFM sensitivity as a function of signal frequency.

Figs.8 and 9 provide additional performance characteristics. Fig.8 shows the gain and noise characteristics; Fig.9 shows the image and half-if rejection of the tuner. The spurious responses shown in Fig.9 were measured with a generator drive capability of 350-millivolts from 10.7 to 216 MHz.

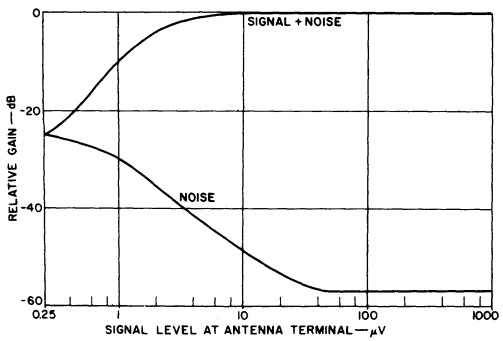


Fig.8 - Relative gain of signal and noise as a function of the signal voltage level.

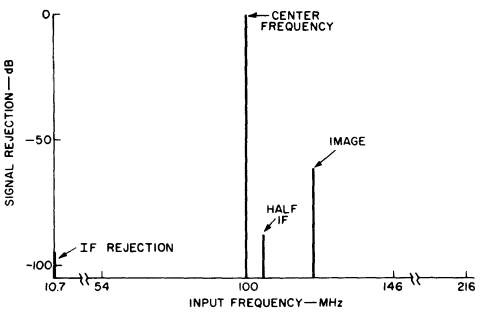


Fig.9 - Signal rejection as a function of input frequency, measured with a generator voltage of 350 millivolts.

MOS transistors covering a wide range of drain current were tested in the rf-amplifier and mixer sockets. Performance variations for image rejection and half-if rejection were within ± 1 dB of the values shown in Table I. Variations in sensitivity were less than 0.25 microvolt.

Conclusions

The RCA-40468 and 40559 MOS field-effect transistors were designed into an FM tuner. Evaluation of this tuner was made in conjunction with an FM-if amplifier that used 40245 and 40246 bipolar transistors. Over-all performance of the combination showed that the capability of MOS devices for dynamic range, sensitivity, and spurious response rejection exceeds that obtained with similar FM tuners that used bipolar transistors. Experimental work indicated that performance variations as a function of product distribution were insignificant.

APPENDIX

Calculation of Conversion Transconductance from the Operating Characteristic

The following procedure is used to calculate the conversion transconductance of the mixer stage based on the degree of linearity of the transconductance curves of Fig.4 and the magnitude of the oscillator injection voltage. The results show that the conversion transconductance is greatest for the curve that is most linear. For the mixer circuit described in this Note, this condition occurs at a substrate bias of -3 volts.

For the curves of Fig.4, the transconductance g_m is given by the following general relation:

$$g_m = f(E_g) \qquad (2)$$

where E_g is the gate bias. For a substrate bias of -3 volts, and a gate bias between zero and -2.1 volts,

the corresponding curve of transconductance is expressed as follows:

$$g_m = 12.5 - 2.14\epsilon^{-0.937E_g} \quad (3)$$

For optimum mixer performance with a minimum of spurious responses, a gate voltage of -1 volt was selected as the quiescent operating point. The Taylor series expansion for Eq.(3) for a center-point operating bias E_g of -1 volt is given by

$$g_m = 10.3 + 2.584\ e_g - 0.148\ e_g^2 + 0.75\ e_g^3 + \ldots \quad (4)$$

where e_g is the instantaneous voltage on the gate. This instantaneous gate voltage e_g can be expressed in terms of the peak oscillator signal voltage e_o, as follows:

$$e_g = -1 + e_o \sin \omega_o t \quad (5)$$

Substitution of Eq.(5) into Eq.(4) yields the following expression for transconductance:

$$g_m = 6.82 + 5.13\ e_o \sin \omega_o t - 2.39\ e_o^2 \sin^2 \omega_o t + 0.75\ e_o^3 \sin^3 \omega_o t \quad (6)$$

An expression for instantaneous drain current i_d in terms of Eq.(6) and the incoming signal e_s can then be written, as follows:

$$i_d = g_m e_s \sin \omega_s t \quad (7)$$

Expansion of Eq.(7) in terms of $e_o \sin \omega_o t$ and $e_s \sin \omega_s t$ and selection of those components which are effective at 10.7 MHz [i.e., sin $(\omega_o - \omega_s)t$ components] provides the following expression for drain current at the intermediate frequency:

$$i_{IF} = (2.57\ e_o + 0.28\ e_o)e_s \quad (8)$$

By definition, the conversion transconductance g_c is equal to the if current divided by the signal voltage, as follows:

$$g_c = i_{IF}/e_s \quad (9)$$

Therefore, g_c can be expressed in terms of the oscillator injection voltage e_o as follows:

$$g_c = (2.57 + 0.28)e_o \quad (10)$$

Because the magnitude of oscillator injection voltage e_o for the MOS FM tuner was selected to be 1 volt peak, the conversion transconductance is calculated to be

$$g_c = (2.57) + (0.28) = 2.85 \text{ mmhos}$$

By use of the same procedure, the conversion transconductance at a substrate bias of zero volts is calculated to be 2.29 millimhos. It is apparent that the application of a substrate bias provides an increase in conversion transconductance of more than 25 per cent.

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Design of Gate-Protected MOS Field-Effect Transistors

by L.A. Jacobus and S. Reich

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. [1,2] Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential build-up across the gate insulation.

Breakdown Mechanism

Before the techniques of gate protection can be applied, the breakdown mechanism associated with gate destruction must be understood. For the sake of simplicity in exploring the breakdown mechanism, a single-gate structure is used. Fig. 1 shows this single-gate structure (a), its electrical symbol (b), and a much simplified equivalent circuit (c) that explains the possible static discharge paths within the device. The substrate diode is formed by the p-n junction integrated over the entire junction area, i.e., the source and drain diffusions connected by the inversion layer or n-type channel. Fig. 1 (c) lumps the diffuse diode into one equivalent diode terminating at the center of the channel.

C_{IN} in Fig. 1(c) represents the gate-to-channel capacitance, and R_1 and R_2 represent the channel resistance. R_3 is the leakage resistance associated with the substrate-to-channel equivalent diode D_1. Leakage resistance across C_{IN} was intentionally deleted because it is more than a thousand orders of magnitude higher than R_3. In a typical RCA MOS field-effect transistor (e.g., 3N128), C_{IN} is less than 5 picofarads. The channel resistance $R_1 + R_2$, which is a function of the applied bias, can range from 10^2 to 10^{10} ohms. R_3 is also subject to variations determined by operating conditions, but can be assumed to be in the order of 10^9 ohms. Thus, the application of a dc potential between the gate and any other element results in practically all of this potential being applied across C_{IN}.

In a dual-gate MOS field-effect transistor, the oxide thickness of the C_{IN} dielectric is about 600 angstroms. The dielectric material is SiO_2, which has a breakdown constant of 5×10^6 volts per centimeter. The gate voltage-handling capability is therefore 30 volts. A cross-

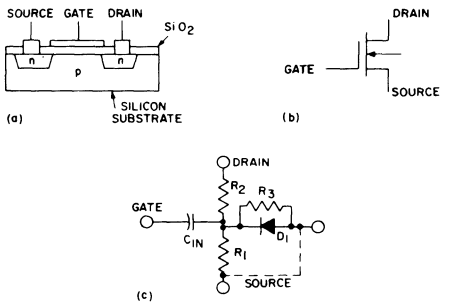


Fig. 1 - Single-gate MOS field-effect transistor: (a) structure; (b) electrical symbol; (c) simplified equivalent circuit.

section of a typical RCA dual-gate device is shown in Fig. 2 (a), and its schematic symbol in Fig. 2(b). The substrate in this structure is internally tied to the source; this connection is also shown schematically by the dotted line in Fig. 1(c).

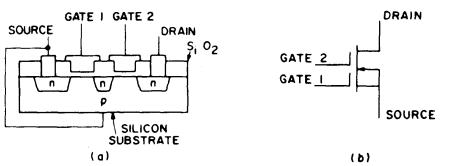


Fig. 2 - Dual-gate MOS field-effect transistor: (a) structure; (b) electrical symbol.

Static Discharge

If the potential applied to an MOS transistor were entirely within the control of the circuit designer, there would be no need for gate protection. Unfortunately, designers do not have complete control of the MOS field-effect transistor environment and static potentials do accumulate. These high potentials can inadvertently be discharged through the device when it is handled

during the equipment manufacturing cycle or by a receiving antenna associated with the end product in which the transistor is used. The more severe of these conditions, in terms of percentage of units that suffer damage, is probably the initial handling phase.

Fig. 3 shows a simple equivalent circuit of a static discharge generator as it appears at the input of an MOS transistor. E_S represents the static potential stored in the static generator capacitor C_D. This voltage must be discharged through internal generator resistance R_S. Laboratory experiments have determined that a human body acts as a static (storage) generator with a capacitance C_D ranging from 100 to 200 picofarads and a resistance R_S greater than 1000 ohms. Although there is

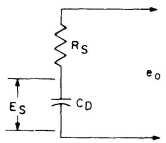


Fig. 3 - Equivalent circuit of a static discharge generator.

virtually no upper limit to the amount of static voltage that can be accumulated, repeated measurements suggest that the amount of potential stored is usually less than 1000 volts. Experience has also indicated that the potential from a static discharge is more severe during transistor handling than when the device is installed in a typical application. In an rf application, for example, a static potential picked up by the antenna would traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the input of the rf amplifier. For this reason, the development of gate-protected MOS transistors concentrated on the requirement that the devices be capable of withstanding the static discharges likely to occur during handling operations.

Gate-Protection Methods

It has been established above that in terms of a static discharge potential it is reasonable to represent the MOS transistor as a capacitor, such as C_{IN} in Fig. 4. The ideal situation in gate protection is to provide a signal-limiting configuration that allows for a signal such as that shown in Fig. 4(a) to be handled without clipping or distortion. The signal-limiting devices should limit all transient responses that exceed the gate breakdown voltage, as shown in Fig. 4(b). One possible means of securing proper limiting is to place a diode in parallel with C_{IN}, as shown in Fig. 4(c). *Unfortunately*, this arrangement causes several undesirable consequences. In terms of signal handling, the single diode clips the positive peaks of a sine wave such as that in Fig. 3(a) when the transistor is operated in the vicinity of zero bias. The 3N140 dual-gate MOS transistor, for example, is frequently operated with the rf signal superimposed on a slightly positive "bias" potential on gate No. 1. Furthermore, gate No. 2 of the 3N140 is designed to handle large positive and negative dc voltage swings from the agc loop. A single-diode arrangement would render this device useless for this type of circuit. It is important, therefore, that the limiting device be an effective open circuit to any incoming signals through the amplitude range of such signals. The best available method for accomplishing this effective open circuit is the back-to-back diode arrangement pioneered by RCA and shown in Fig. 3(d).

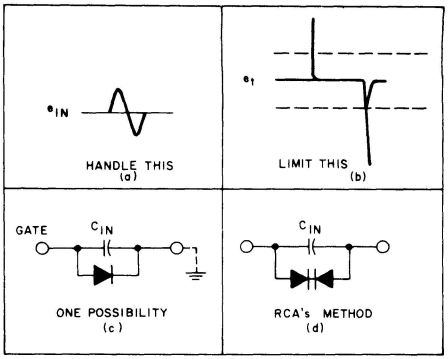


Fig. 4 - Gate-protection requirements and two solutions.

Ideally, the transfer characteristic of the protective signal-limiting diodes has an infinite slope at limiting, as shown in Fig. 5(a). Under these conditions, the static potential generator in Fig. 5(b) discharges through its internal impedance R_S into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, with an infinite transfer slope ($R_S = 0$), would then limit the voltage presented to the gates to its knee value, e_d. The difference voltage $E - e_d = e_S$ (where E is the static potential in the static generator, e_d is the diode voltage drop, and e_S is the voltage drop across the generator internal resistance) appears as an IR drop across R_S, the internal impedance of the generator. The instantaneous value of the diode current is then equal to e_S/R_S. During handling, the practical range of this discharge varies from several milliamperes to several hundred milliamperes.

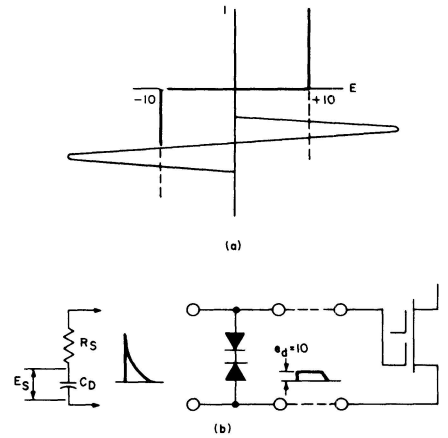


Fig. 5 - Transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).

Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the diode ideally adds no capacitance or loading to the rf input circuit.

The first phase in the development of gate-protected MOS field-effect transistors was, quite naturally, their construction in hybrid form. This form was used for initial measurements because it effectively enabled the physical separation of the diodes from the MOS pellet. This separation made it possible to measure the performance of the active device apart from the combined structure and thus obtain a more precise assessment of the loading effect of the diodes. The hybrid phase has now been followed by the development of monolithic gate-protected MOS field-effect transistors such as the RCA-40673. In this transistor, the diodes are an integral part of the MOS device and are internally connected as shown in Fig. 6.

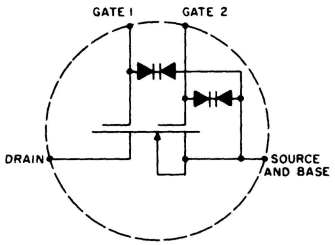


Fig. 6 - Connection of integral protective diodes in dual-gate MOS transistor.

Monolithic Gate-Protected MOS Transistors

In the design of a monolithic diode-protected MOS transistor, several factors must be taken into account. (1) The high-frequency performance of the device must be comparable to that of available unprotected units. (2) The device must be designed so that no additional assembly cost is incurred. (3) The silicon area must be used efficiently to provide the maximum number of devices per semiconductor wafer. (4) The diodes must provide adequate protection against the transients experienced primarily in handling but also when the transistor is finally installed in some piece of equipment.

One approach to integrating protective diodes into an MOS transistor structure on one chip is shown in Fig. 7. In this approach, the silicon substrate required for an n-channel depletion-type MOS device is the starting material. The n-type wells are diffused into the silicon to provide pockets for the protective devices. The surface concentration and depth of these wells are carefully controlled because both of these factors are important in determining diode characteristics.

The p^+-type regions are diffused into the n-type wells to form the diodes and around the periphery to isolate the diode structure from the surface of the MOS device and to provide a region into which the channels may be terminated. The size of the diodes is determined by the desired current-handling capability and the amount of capacitance that can be tolerated across the gate of the MOS transistor. The spacing of the diodes is determined by the area available and the desired amount of control of transistor action from diode to diode. After the diode structures are formed, they are covered by a protective oxide. The MOS device is then fabricated by conventional means.

Fig. 8 shows a photograph of a completed monolithic diode-protected dual-gate MOS transistor. In this structure,

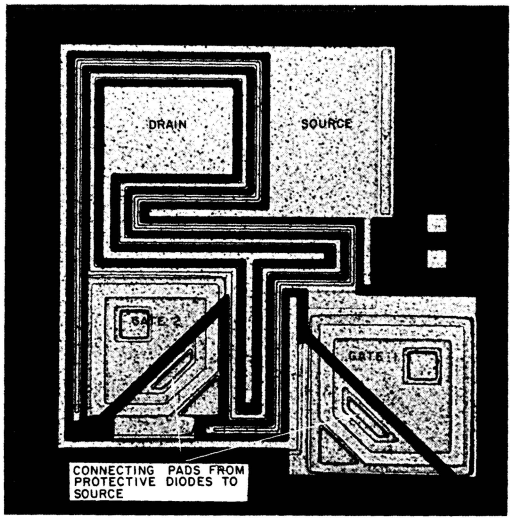


Fig. 8 - Completed monolithic diode-protected dual-gate MOS transistor.

one of the diodes of each pair has been located under the gate bonding pads. The small triangular metal pads

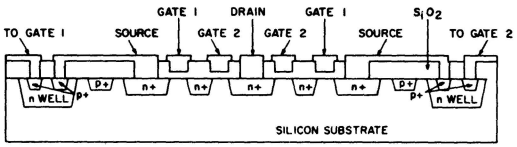


Fig. 7 - Structure of MOS transistor chip including protective diodes.

make contact with the second diode of each pair and connect it to the source metalization. In assembly, the source is shorted to the substrate so that a low-resistance path to ground is provided for the diodes. To ground the diodes under the second gate properly, it is necessary to break the metal of the first gate and terminate the first channel on the p^+-type guard band surrounding the diode structure of the second gate. This technique prevents spurious source-to-drain current which could result from the open nature of the structure.

Current-Handling Capability

Fig. 9 shows a typical diode transfer characteristic measured with a one-microsecond pulse width at a 4 x 10^{-3} duty cycle. The purpose of the protective diode is to limit the amplitude of the transient to a value that is below the gate breakdown voltage. Typically, a dual-gate transistor has a gate-to-source breakdown voltage rating of 20 volts. The curves in Fig. 9 show that the transfer characteristic of the signal-limiting diodes will constrain a transient impulse to potential values well below this 20-volt limit even when the input surge is capable of delivering hundreds of milliamperes.

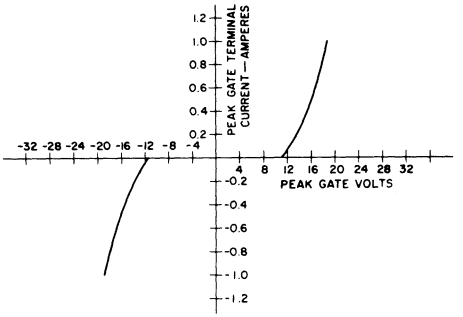


Fig. 9 - Typical diode transfer characteristic measured with 1-microsecond pulse width at 4 x 10^{-3} duty cycle.

The protection offered by the MOS signal-limiting diodes is more dramatically demonstrated when a gate-protected MOS transistor is compared to a high-frequency bipolar device. A laboratory experiment in which a static charge was accumulated in a capacitor and discharged through a circuit configuration like the one shown in Fig. 3 demonstrated that the special signal-limiting diodes made the protected-gate MOS field-effect transistor less vulnerable to static discharge damage than the bipolar transistor by a factor greater than two.

Input Capacitance and Resistance

The curves of input capacitance and input resistance as a function of drain current in Fig. 10 represent average readings taken from ten hybrid devices with diodes first connected and then disconnected (the readings for all ten devices were remarkably close to the averages). The curves indicate that the diodes increase input capacitance by about 2.5 picofarads and decrease input resistance by about 200 ohms.

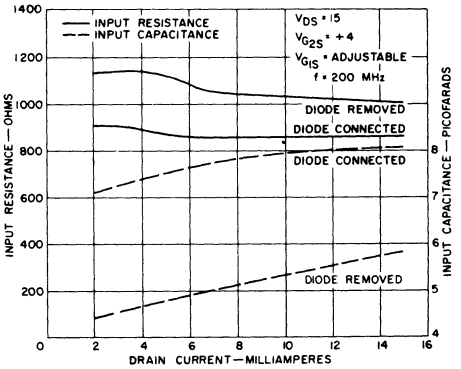


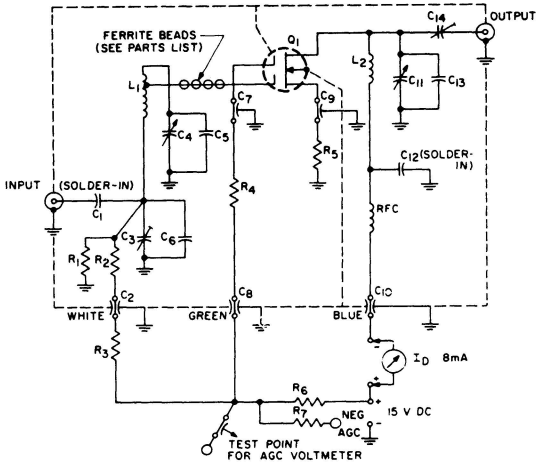
Fig. 10 - Input resistance and capacitances as a function of drain current for hybrid structures with and without diodes.

Power Gain and Noise Factor

In the final analysis, the question that must be answered is how the addition of the protective signal-limiting diodes affects circuit power gain and noise factor. Performance data taken on the ten units described above in the typical rf test circuit shown in Fig. 11 are given in Table 1. Noise-factor values show an average degradation of 0.25 dB when the diodes are connected. The power-gain values show that the change in this characteristic is insignificant.

Table 1 - Power Gain and Noise Factor at 200 MHz.

HYBRID UNIT	POWER GAIN (dB)		NOISE FACTOR (dB)	
	DIODES IN	DIODES REMOVED	DIODES IN	DIODES REMOVED
1	16.3	16.4	3.7	3.4
2	18.8	18.5	2.4	2.2
3	16.5	16.2	3.3	3.0
4	16.3	15.7	3.9	3.4
5	17.7	17.8	2.6	2.4
6	17.2	17.5	2.8	2.5
7	17.1	17.0	3.3	3.2
8	17.9	18.0	2.9	2.6
9	18.5	18.5	2.4	2.3
10	17.3	17.3	3.2	3.0



C_1: 100 picofarads, ceramic disc
C_2 C_7 C_8 C_9 C_{10}: 1000 picofarads, feed-through type
C_3: 1 to 10 picofarads, variable air (piston); JFD VAM-010, Johnson Co. No. 4335, or equivalent
C_4: 1.8 to 8.7 picofarads, variable air; Johnson Co. No. 160-104 or equivalent
C_5: 3 picofarads, tubular ceramic
C_6: 22 picofarads, ceramic disc
C_{11}: 1.5 to 5 picofarads, variable air; Johnson Co. No. 160-102 or equivalent
C_{12}: 100 picofarads, ceramic disc
C_{13}: 1.5 picofarads, tubular ceramic
C_{14}: 0.8 to 4.5 picofarads, variable air (piston); Erie 560-013 or equivalent
Ferrite beads: 4 beads on No. 24 wire between L_1 and socket; beads are Pyroferrio Co. "Carbonyl J" or equivalent: 0.093-inch OD, 0.03-inch ID, 0.063 inch thick
L_1: 4 turns 0.020-inch copper ribbon, silver-plated, 0.075 to 0.085 inch wide, 0.25-inch inside diameter, coil approximately 0.80 inch long
L_2: 4.5 turns 0.020-inch copper ribbon, silver-plated, 0.085 to 0.095 inch wide, 0.3125-inch inside diameter, coil approximately 0.90 inch long
Q_1: MOS transistor under test
RFC: Ohmite part No. Z235 or equivalent
R_1: 27,000 ohms
R_2: 47,000 ohms
R_3: 36,000 ohms
R_4: 1800 ohms
R_5: 275 ohms, ½ watt, 1
R_6: 120,000 ohms
R_7: 1000 ohms

Fig. 11 - RF test circuit for dual-gate MOS transistors.

Conclusions

Gate-protected dual-gate MOS field-effect transistors such as the RCA-40673 make available to the circuit designer a device capable of good rf performance without the hazards previously associated with the handling and installation of MOS devices. Moreover, the gate protection is provided by signal-limiting diodes that do not significantly compromise dynamic range, noise factor, or power gain.

Acknowledgment

The authors thank L. Baar for collecting data and providing general support for the work described, and C. Tollin for fabricating the devices tested.

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2. E.F. McKeon, "Cross-Modulation Effects in Singl Gate and Dual-Gate MOS Field-Effect Transistors" RCA Application Note AN-3435, August 1967.

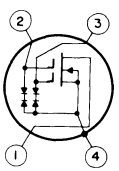
RF Applications of the Dual-Gate MOS FET up to 500 MHz

by L. S. Baar

The RCA dual-gate protected, metal-oxide silicon, field-effect transistor (MOS FET) is especially useful for high-frequency applications in RF amplifier circuits. The dual-gate feature permits the design of simple AGC circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS FET in RF applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

Gate-Protection Diodes

Fig. 1 shows the terminal diagram for the 3N200. Gate No. 1 is the input signal electrode and Gate No. 2 is normally used to obtain gain control. The back-to-back diodes are connected from each of the gates to the source terminal, lead No. 4. If short duration pulses greater than ±10 volts, generated for example by static discharge, are inadvertently applied to either gate, the protective diodes limit these voltages and shunt the current to the source terminal. Thus the gates, under normal operating conditions, are protected against the effects of overload voltages.[1]



LEAD 1 - DRAIN
LEAD 2 - GATE NO. 2
LEAD 3 - GATE NO. 1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE

Fig. 1 – Terminal diagram for the 3N200.

Operating Conditions

Typical two-port characteristics at 400 MHz including both "y" and "s" parameters, are given for the 3N200 in the RCA technical bulletin, File No. 437. This note makes use of the "y" parameters; however, designers who prefer the alternate method can, by parallel analysis, make use of the "s" parameters.

A recommended operating drain current (I_D) for the 3N200 is approximately 10 milliamperes with Gate No. 2 sufficiently forward biased such that a change in the bias voltage does not greatly affect the drain current. An adequate Gate No. 2-to-source voltage (V_{G2S}) is approximately +4 volts. The forward transadmittance (y_{fs}) increases with drain current, but saturates at higher current levels. The increase in RF performance at drain currents above 10 milliamperes is achieved only with less efficient use of input power.

To establish the optimum operating conditions for a type, consideration must be given to the range of variations in characteristics values encountered in production quantities of the type.[2] One important measure of type variation is the range of zero bias drain current (I_{DS}). The current range given in the 3N200 technical bulletin for I_{DS} is from 0.5 mA to 12 mA. A fixed bias condition intended to center the range of drain current at the desired level, still will produce an operating drain current range of 11.5 milliamperes with a resultant wide range of forward transconductance (g_{fs}). The drain current can be regulated by applying dc feedback with a bypassed source resistor (R_S). A good approximation of R_S (where $I_{DQ} \geq I_{DS}/2$) can be calculated by the use of the following formula*, assuming that V_{G1S} vs. I_{DS} is linear over the current range under consideration:

$$R_S \approx \left(\frac{1}{g_{fs}(\text{min.})}\right)\left(\frac{\Delta I_{DS}}{\Delta I_{DQ}} - 1\right) \qquad \text{Eq. 1}$$

*See Appendix

where:

ΔI_{DS} is the current range given in the 3N200 technical bulletin

ΔI_{DQ} is the desired range of operating current

g_{fs}(min.) is the minimum forward transconductance at 1000 Hz

With the value of R_S established, then the Gate-No. 1 Voltage (V_{G1}) can be calculated from the equation

$$V_{G1} = V_{G1S} + I_{DQ} R_S \qquad \text{Eq. 2}$$

where V_{G1S} is estimated by:

$$V_{G1S} \approx \frac{I_{DQ} - I_{DS}}{g_{fs}(avg.)} \qquad \text{Eq. 3}$$

where:

g_{fs}(avg.) is the average forward transconductance

To establish the Gate-No. 2 Voltage (V_{G2}), follow the same procedure described for calculating the Gate-No. 1 Voltage, except that a fixed V_{G2S} of approximately 4 volts is adequate.

If gain control is desired, apply a negative-going voltage to Gate No. 2. Because Gate No. 2 has little control in the voltage range of +2 to +5 volts, this characteristic may be used to effect AGC delay of the device in order to maintain the low noise figure until the RF signal is out of the noise-level range.

Stability Considerations

Typical "y" parameter data as a function of frequency are given in Table 1. Maximum available gain (MAG) calculated from these data are also included to indicate ideal gain performance (i.e., $y_{rs} = 0$). The ability of the MOS FET to approach these gain levels depends on the device maintaining stable performance at the required operating frequency.

There are several methods which may be used to test for gain vs. stability. One of these methods, the Linvill Criteria (C), is defined by the equation:

$$C = \frac{y_{rs}\, y_{fs}}{2g_{is}\, g_{os} - R_e\, (y_{rs}\, y_{fs})} \qquad \text{Eq. 4}$$

A value for C which is less than 1 indicates unconditional stability. Applying the 400-MHz values taken from Table 1 to the Linvill Criteria yields a value of C = 0.615; substantially less than the value indicating unconditional stability.

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 100	200	300	400	500	UNITS
y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-15.0	-25.0	-35.0	-47.0	-60.0	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.4	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	-60.0	-25.0	0	14.0	20.0	degrees
Maximum Available Gain	MAG	32.0	24.0	17.5	13	10.0	dB

Table 1 – "y" Parameters from 100 to 500 MHz

The following equation for Maximum Usable Gain $(MUG)^3$ is:

$$MUG = \frac{2K \left| y_{fs} \right|}{\left| y_{rs} \right| (1 + \cos \theta)} \qquad \text{Eq. 5}$$

where:

$\theta = \angle y_{fs} + \angle y_{rs}$

K = skew factor

$\angle y_{rs}$ = angle of reverse transadmittance

$\angle y_{fs}$ = angle of forward transadmittance

The skew factor, introduced in this equation, is a safety measure that establishes an arbitrary degree of skewing in the frequency response which may be introduced by regeneration. A value of 0.2 for K has been established on the basis of past experience. The value of MUG calculated at 400 MHz is 13.8 dB. This value of MUG is greater than the value of MAG, again indicating unconditional stability, since MAG, ignoring inherent feedback, is the conjugately matched gain. Therefore, neutralization or circuit loading is not required to insure stable performance, and the gain can approach MAG, limited only by circuit losses.

Reverse transadmittance (y_{rs}) is composed of several components, but the major ones are feedback capacitance (C_{rss}) and source-lead inductance (L_S). Therefore, care must be exercised in the application of the y_{rs} values, shown in Table 1, at the upper end of the usable frequency range. The 3N200 utilizes a JEDEC TO-72 package that has 4 leads. The data in Table 1 was compiled with the use of a socket which contacts the leads of the 3N200 as close as possible to the bottom of the package as specified by the JEDEC Standard Proposal SP-1028 "Measurement of VHF-UHF "y" Parameters". The leads are shielded from each other to eliminate stray capacitance between the leads, but some lead inductance is inevitable. If the device is soldered directly to the circuit components using commercial production techniques rather than by precise laboratory methods, then additional source lead inductance can be expected. Also, some additional capacitive coupling may result if the input and output circuits are not completely isolated from each other.

Because the published y_{rs} value for the 3N200 is very small, the circuit y_{rs} values may differ significantly from the y_{rs} values shown in Table 1 and hence, may result in an unstable operating condition. It is impossible to provide data for all possible mounting combinations, therefore, a recommended mounting arrangement is shown in Fig. 2. The source and substrate in the T0-72 package of the 3N200 are internally connected to lead No. 4 and the case. The source-lead inductance can be reduced, if the case is used as the source connection. Fig. 2 illustrates a partial component layout in which the case is held by a clamp or other fingered device. The clamp is soldered to a feedthrough capacitor to provide an effective, very-low inductance bypass to RF signals. This mounting arrangement still permits the use of a source resistor for DC stability, and enables the case to provide isolation between the input and output circuit in addition to the isolation afforded by the shield.

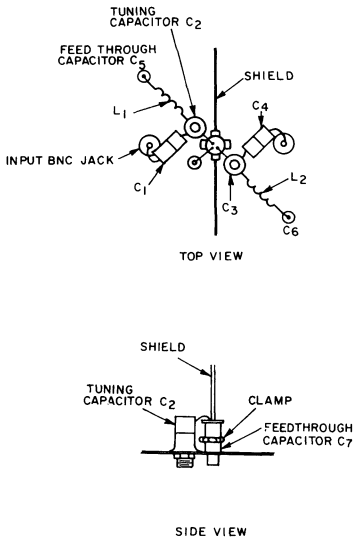


Fig. 2 – Partial component layout of 400-MHz amplifier circuit

The reduction of source-lead inductance provides in addition to greater stability, a lower input and output conductance. Table 2 shows the differences in "y" parameter values at 400 MHz when measured with the source connection made to lead No. 4 (in accordance with the published data for the 3N200) and when measured with the case connected directly to the ground plane of the test jig. The magnitude of reverse transadmittance is halved with a significant change in its phase angle. The input conductance is reduced by 30%, and the output conductance is reduced by 13%. A recalculation of the expressions for MAG, MUG, and Linvill Criteria (C) shows a significant improvement in gain and circuit stability.

While it is difficult to provide accurate information on the effects of shielding between the input and output circuits, its effect can be demonstrated when all other feedback components have been reduced to negligible values. The circuit, shown in Fig. 3 (for component layout see Fig. 2), was measured both with and without a shield. The maximum gain, without the shield, averaged 0.8 dB lower than with the use of the shield.

When receiver sensitivity is an important consideration in the design of an RF amplifier, a compromise must be made in the circuit power gain to achieve a lower noise

CHARACTERISTICS	SYMBOL	FREQUENCY (f) = 400 MHz		UNITS
		Normal Connection	Case Grounded	
Maximum Available Power Gain	MAG	13.0	15.7	dB
Maximum Usable Power Gain (unneutralized)	MUG	13.8	19.4	dB
Linvill Stability Factor, C	C	0.615	0.335	mmho
"y" Parameters				
Input Conductance	g_{is}	3.6	2.5	mmho
Input Susceptance	b_{is}	11.2	11.7	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.5	15.5	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-47.0	-40.0	degrees
Output Conductance	g_{os}	0.8	0.65	mmho
Output Susceptance	b_{os}	4.25	4.25	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.14	0.07	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	14.0	49.0	degrees

Table 2 – "y" Parameters at 400 MHz with source connection to lead No. 4 and with case connected to ground plane of test jig

factor. A contour plot of noise figure as a function of generator source admittance is shown in Fig. 4. Each contour is a plot of noise figure as a function of the generator source conductance and susceptance. Data for the noise figure were obtained from a test amplifier designed with very low feedback. Even though the area of very low-noise figure in the curves in Fig. 4 cover a broad range of source admittance, impedance-matching for maximum power gain could result in a relatively poor noise figure. As shown in Table 2, the input conductance (g_{is}) with the case grounded is 2.5 mmho. With the reactive portion tuned out, the noise factor at power matched conditions is almost 1 dB higher than the optimum noise figure. However, matching to 5.0 mmho results in a near optimum noise factor with a loss of only 0.5 dB in gain. In addition, impedance matching to high conductance

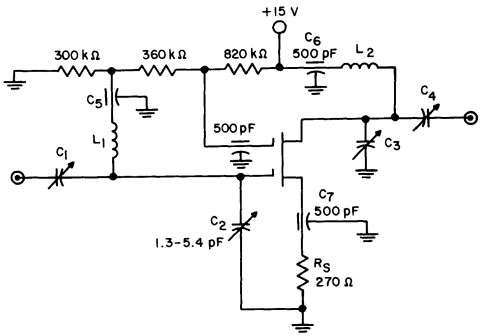


Fig. 3 – 400-MHz amplifier circuit

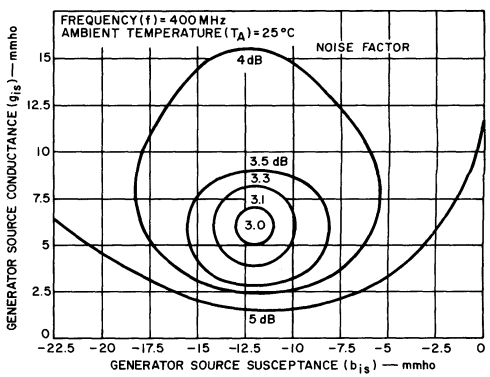


Fig. 4 – Noise factor vs. generator source (input) admittance (Yis)

also benefits crossmodulation performance, as will be discussed in a later section.

Gate Protection Diodes

The diodes incorporated into RCA dual-gate MOS FETs, for gate protection, have been designed to minimize RF loading on the input circuits. The small amount of RF loading results in only a fraction of a dB loss in power gain and a negligible increase in the noise figure. The advantages of diode protection, greatly outweigh the slight loss in power gain, especially in an RF amplifier intended for the input stage of a receiver.

In addition to the protection afforded in normal handling, the diodes also provide in-circuit protection against events such as: static discharge due to contact with the antenna, delay in transmit-receive switching, or connection of an antenna with an accumulated charge to the receiver.

Crossmodulation

Crossmodulation is an important consideration because it is an inherent device characteristic where circuit considerations are secondary. Crossmodulation is the transfer of modulation from an undesired signal on a desired signal caused by the non-linear characteristics of a device.

Crossmodulation is proportional to the third-order term of the expansion of the I_D - V_{GS} curve. It is normally specified as the undesired signal voltage required to produce a crossmodulation factor of 0.01. The crossmodulation factor is defined as the percent modulation on a desired carrier by the modulated undesired signal divided by the percent modulation of the undesired signal.[4]

Inspection of the I_D - V_{G1S} curve of Fig. 5 offers an insight to the possible crossmodulation as a function of gain-reduction performance. When both channels of the 3N200 are fully conducting current, as shown by the V_{G2S} = 4-volt curve, the device approximately follows a square-law characteristic. If the I_D - V_{G1S} curve was ideal, the third-order term would be zero; but in practical cases, the third-order term and crossmodulation have some low values. When the gain is reduced, by the application of bias to Gate No. 2, the square-law characteristic changes to a curve with a knee. Sharp curvatures usually result in larger high-order terms and poorer crossmodulation performance can be expected at lower gain conditions. If in Fig. 6, Circuit A, we assume a fixed bias (V_{G1S}) of approximately +0.4 volt, then the expected variation in crossmodulation is determined at the points where the ordinate at V_{G1S} = +0.4 volt crosses the curves. Crossmodulation performance at values of V_{G2S} = +4 volts to cutoff is as follows: good (low crossmodulation) at +4 volts, poorer at +2 volts, poorest at +1 volt, and again improves from zero volts to cutoff.

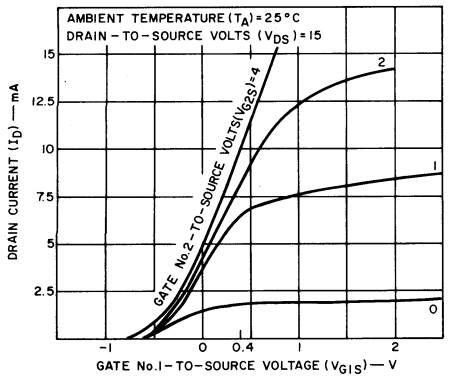


Fig. 5 – Drain current (I_D) vs. gate No. 1-to-source voltage (V_{G1S})

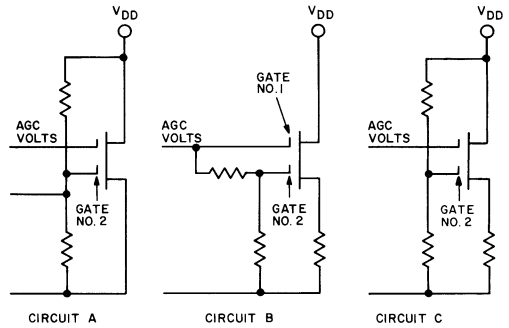


Fig. 6 – Biasing circuits using the 3N200

Curve A, Fig. 7 shows a curve of the undesired signal with a crossmodulation factor of 0.01 as a function of gain reduction. The curve indicates performance is poorest when gain reduction is in the 3- to 15-dB region; this region represents a Gate No. 2-voltage range of approximately 0.5 volt to 2 volts. The exception to the poor crossmodulation perform-

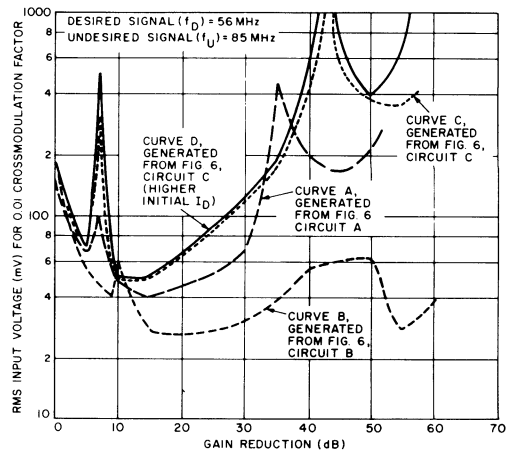


Fig. 7 – Crossmodulation vs. gain reduction using biasing circuits shown in Fig. 6

ance in this range is the sharp peak which occurs at the 5-dB level and is due to a curve inversion that takes place just prior to the knee. Beyond the 15-dB level, crossmodulation generally shows an improvement.

If Gate No. 1 is also reverse biased in conjunction with Gate No. 2 in the manner shown in Fig. 6, Circuit B, then the overall performance is poorer because the Gate No. 1 voltage will tend to follow the knee of each curve. This occurrence is evident in Fig. 7, Curve B. If Gate No. 1 is biased as shown in Fig. 6, Circuit C, the Gate No. 1-to-Source voltage intercepts the Gate No. 2 curves where the curvature is less severe, indicating as shown by Fig. 7, Curve C an improvement in crossmodulation performance. A further slight improvement is possible by the use of a higher initial operating drain current, which effectively moves the intercepts to the right on each curve. This improvement is indicated in Fig. 7, Curve D.

The curves in Fig. 7 establish that the biasing arrangement which provides optimum crossmodulation performance is the one in which Gate No. 1 forward bias increases as Gate No. 2 controls the gain. This biasing arrangement is easily accomplished by the use of a fixed Gate No. 1 voltage and a source resistor. As the Gate No. 2 bias voltage reduces the drain current, there is also a decrease in source voltage and an increase in the Gate No. 1-to-Source voltage. The gate-to-source voltage ratings must not be exceeded under any circumstances.

Summary

An RF amplifier, ideally, should provide high gain, a low-noise figure, and low crossmodulation. The 3N200 offers a good compromise in providing these three features. As indicated in the section on "Stability Considerations" a mismatch at the circuit input to a higher conductance level, provides an improved noise figure. The same mismatch condition also improves crossmodulation performance. The input signal at the gate of the device, when mismatched as indicated above, is lower than if it is power matched. The same ratio applies to any undesired signal and, thus, reduces the possibility of crossmodulation interference.

Appendix

The drain current of a device is established by the relationship

$$I_D = g_{fs} V_{G1S} + I_{DS}$$

where:

I_{DS} = drain current

at:

$V_{G1S} = 0$, $V_{G2S} = +4$ volts.

If a source resistor is used, as shown in Fig. A1, the ga No. 1-to-source voltage is

$$V_{G1S} = V_{G1} - I_D R_S$$

then

$$I_D = g_{fs} (V_{G1} - I_D R_S) + I_{DS} \quad \text{or}$$

$$I_D = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}}{1 + g_{fs} R_S}$$

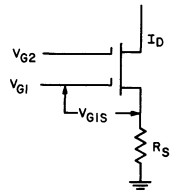


Fig. A1 — Bias circuit using the 3N200

The typical curves in Fig. A2 show drain current v Gate No. 1-to-Source Voltage as a function of I_{DS} leve These curves are almost linear when the typical operatir drain current is in the 10-milliampere region. For th remainder of the analysis a linear relationship will t assumed for the required range of quiescent current. Th assumption of linearity dictates that g_{fs} is a constant.

The required range of drain current is $I_{D2} - I_{D1}$

where:

$$I_{D2} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(\text{max.})}{1 + g_{fs} R_S}$$

$$I_{D1} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(\text{min.})}{1 + g_{fs} R_S}$$

$$\Delta I_D = I_{D2} - I_{D1} = \frac{I_{DS}\,(\text{max.}) - I_{DS}\,(\text{min.})}{1 + g_{fs} R_S} = \frac{\Delta I_{DS}}{1 + g_{fs} R}$$

Solving the above equation for R_S gives

$$R_S = \frac{(\Delta I_{DS}/\Delta I_D) - 1}{g_{fs}}$$

where:

g_{fs} is equal to the expected minimum value at th required I_D

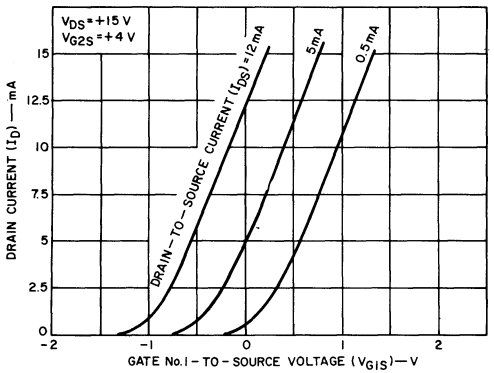


Fig. A2 – Drain current vs. gate No. 1-to-source voltage

References:

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3. R. A. Santilli, "RF and IF Amplifier Design Considerations", IEEE Transactions on Broadcast and TV Receivers, Nov. 1967
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TA5235	LIC	CA3014	129	SSD-201A	62
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TA5254	LIC	CA3030	316	SSD-201A	507
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TA5457	LIC	CA3045	341	SSD-201A	221
TA5458	LIC	CA3046	341	SSD-201A	221
TA5460AV	COS/MOS	CD4016AK	479	SSD-203A	78
TA5507	LIC	CA3050	361	SSD-201A	372
TA5513	LIC	CA3026	388	SSD-201A	336
TA5516	LIC	CA3039	343	SSD-201A	166
TA5517C	LIC	CA3064	396	SSD-201A	84
TA5519V	COS/MOS	CD4008AK	479	SSD-203A	43
TA5523A	LIC	CA3048	377	SSD-201A	250
TA5537	LIC	CA3049T	611	SSD-201A	363
TA5551	COS/MOS	CD4000AK	479	SSD-203A	24
TA5553	COS/MOS	CD4007AK	479	SSD-203A	24
TA5554	COS/MOS	CD4001AK	479	SSD-203A	24
TA5555	COS/MOS	CD4002AK	479	SSD-203A	24
TA5556B	COS/MOS	CD4006AK	479	SSD-203A	31
TA5561	LIC	CA3047A	360	SSD-201A	488
TA5562	LIC	CA3047	360	SSD-201A	488
TA5578V	COS/MOS	CD4014AK	479	SSD-203A	68
TA5579V	COS/MOS	CD4015AK	479	SSD-203A	73
TA5580V	COS/MOS	CD4018AK	479	SSD-203A	89
TA5615A	LIC	CA3059	490	SSD-201A	380
TA5625A	LIC	CA3066	466	SSD-201A	125
TA5628C	LIC	CA3089E	561	SSD-201A	46
TA5634	LIC	CD2154	402	SSD-201A	455
TA5645	LIC	CA3060E	537	SSD-201A	466
TA5649A	LIC	CA3070	468	SSD-201A	143
TA5652V	COS/MOS	CD4019AK	479	SSD-203A	94
TA5655	LIC	CA3051	361	SSD-201A	372
TA5660V	COS/MOS	CD4009AK	479	SSD-203A	48
TA5668V	COS/MOS	CD4010AK	479	SSD-203A	48
TA5672	LIC	CA3052	387	SSD-201A	28
TA5675V	COS/MOS	CD4013AK	479	SSD-203A	62
TA5677V	COS/MOS	CD4044AK	590	SSD-203A	214
TA5681V	COS/MOS	CD4011AK	479	SSD-203A	55
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TA5683V	COS/MOS	CD4021AK	479	SSD-203A	104
TA5684V	COS/MOS	CD4017AK	479	SSD-203A	84
TA5690X	LIC	CD2501E	392	SSD-201A	437
TA5702B	LIC	CA3071	468	SSD-201A	143
TA5716W	COS/MOS	CD4057AD	Prel.	SSD-203A	254
TA5718	LIC	CA3054	388	SSD-201A	336
TA5721X	LIC	CD2500E	392	SSD-201A	437
TA5733	LIC	CA3053	382	SSD-201A	344
TA5752	LIC	CA3067	466	SSD-201A	125
TA5757	LIC	CA3076	430	SSD-201A	70
TA5758B	LIC	CA3085	491	SSD-201A	409
TA5776V	COS/MOS	CD4020AK	479	SSD-203A	99
TA5785X	LIC	CD2503E	392	SSD-201A	437
TA5786X	LIC	CD2502E	392	SSD-201A	437
TA5790	LIC	CA3060D	537	SSD-201A	466
TA5795	LIC	CA3058	490	SSD-201A	380
TA5797	LIC	CA3741T	531	SSD-201A	501
TA5799A	LIC	CA3084	482	SSD-201A	178
TA5807	LIC	CA3078T	535	SSD-201A	479
TA5814	LIC	CA3065	412	SSD-201A	106
TA5816	LIC	CA3080	475	SSD-201A	458
TA5820	LIC	CA3541D	536	SSD-201A	429
TA5842	LIC	CA3088E	560	SSD-201A	42
TA5855A	LIC	CA3091D	534	SSD-201A	417
TA5858	LIC	CA3081	480	SSD-201A	170
TA5866	LIC	CA3075	429	SSD-201A	53
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TA5867W	COS/MOS	CD4023AD	479	SSD-203A	55
TA5867X	COS/MOS	CD4023AE	479	SSD-203A	55
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TA5873V	COS/MOS	CD4028AK	503	SSD-203A	135
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TA5897X	LIC	CD2501E	392	SSD-201A	437
TA5898X	LIC	CD2503E	392	SSD-201A	437
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TA6037	LIC	CA3748CT	531	SSD-201A	501
TA5037A	LIC	CA3748T	531	SSD-201A	501
TA6044	LIC	CA3086	483	SSD-201A	234
TA6051	LIC	CA3079	490	SSD-201A	380
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TA7365	TRI	40669	364	SSD-206A	73
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TA7374	MOS/FET	3N159	326	SSD-201A	618
TA7375	MOS/FET	3N154	335	SSD-201A	596
TA7381	PWR	2N6098	485	SSD-204A	111
TA7382	PWR	2N6099	485	SSD-204A	111
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