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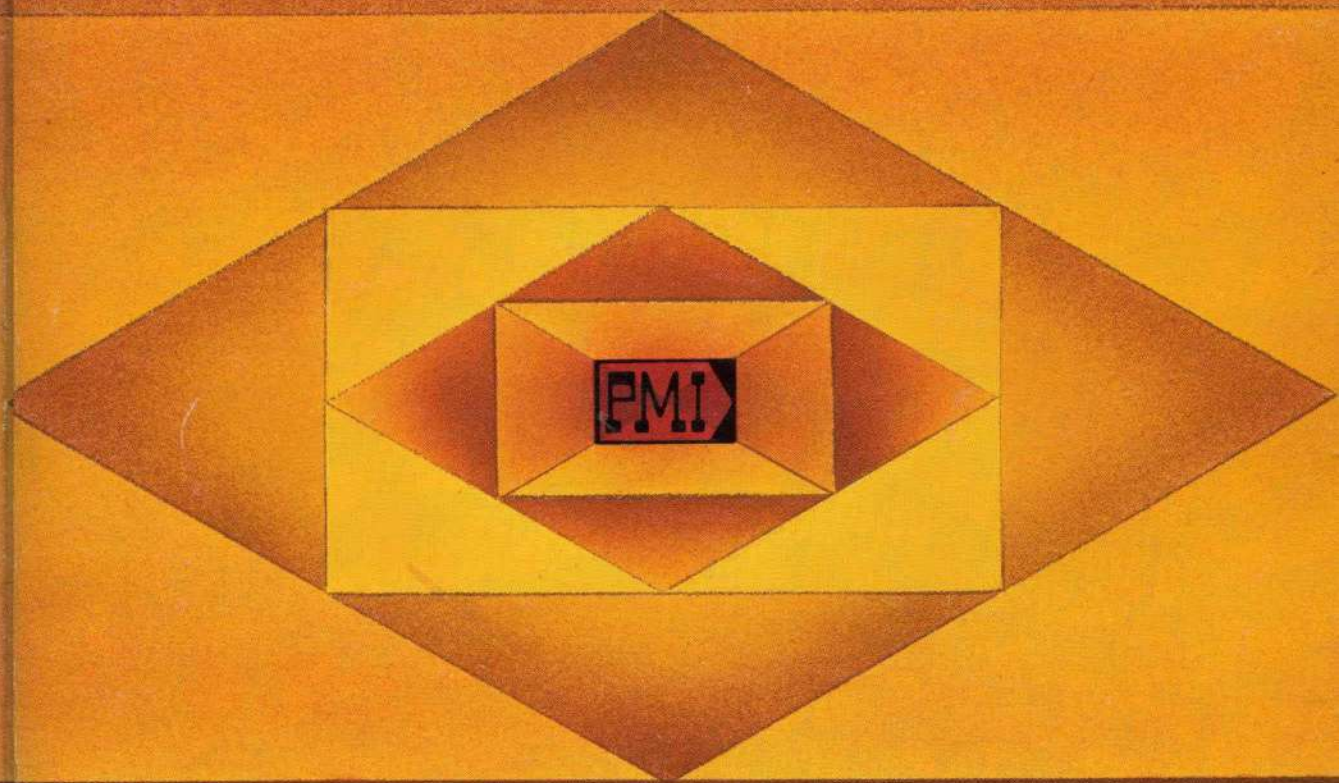
PRECISION MONOLITHICS

1977 - 1978



LINEAR & CONVERSION I.C. PRODUCTS

PMI®

PRECISION MONOLITHICS

PMI®

INTRODUCTION

This catalog contains complete technical data and information on Precision Monolithics' full line of linear and conversion products. In addition to data sheets, an expanded applications section, guaranteed chip specifications section, cross references, functional replacement guides, selection guides, package information, and definitions are provided.

Precision Monolithics' continued dedication to providing state-of-the-art products has resulted in 16 new products since the previous edition. New products include 11 operational amplifiers, 4 D/A converters, and BIFET analog multiplexers. There are 3 second-source BIFET op amps, 3 Precision BIFET op amps, 2 precision low power op amps, and both second-source and precision quad op amps. New D/A converters include Sign Plus 10 Bits, Two's Complement 10 Bit, 2-Digit BCD and 12 Bit multiplying types. A similar increase in new products is expected in the coming year. To keep informed, please fill out the Registration Card at the back of this catalog and return it to PMI, and we will send all new data sheets and application notes as they become available.

Contact the PMI sales office, representative, or distributor listed at the back of this catalog for further assistance.

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PMI reserves the right to make changes to the products contained in this catalog to improve performance, reliability, or manufacturability.

Although every effort has been made to insure accuracy of the information contained in this catalog, PMI assumes no responsibility for inadvertent errors.

PMI assumes no responsibility for the use of any circuits described herein and makes no representation that they are free of patent infringement.

A BOURNS Subsidiary

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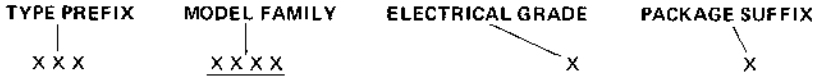
ORDERING INFORMATION

Proprietary and second source products are available with a choice of electrical specifications, packages and operating temperature ranges. This section explains the PMI part numbering system. For specific ordering information such as available electrical grade and package combinations, see the specific product data sheet.

CMP = Precision Voltage Comparator
DAC = Digital to Analog Converter
MAT = Matched Transistors
OP = Proprietary Operational Amplifier
PM = Second Source — Industry Standard Specs
REF = Precision Voltage Reference
SSS = Superior Second Source — Improved Specs



EXAMPLES

OPERATIONAL AMPLIFIERS

OP-01 = High Speed Inverting
OP-02 = Precision Low Cost
OP-04 = Precision Low Cost Matched Dual
OP-05 = Precision Low Drift
OP-07 = Precision Low Offset Voltage
OP-10 = Precision Matched Dual
OP-14 = Precision Low Cost Matched Dual
SSS725 = Improved Instrumentation Op Amp
SSS741 = Improved General Purpose Op Amp
SSS747 = Improved General Purpose Dual Op Amp
SSS1408 = Improved 8-Bit D/A Converter
SSS1458 = Improved General Purpose Dual Op Amp
PM108 = Low Current Op Amp
PM725 = Instrumentation Op Amp
PM741 = General Purpose Op Amp
PM747 = General Purpose Dual Op Amp
PM1458 = General Purpose Dual Op Amp

COMPARATORS

CMP-01 = High Speed
CMP-02 = Low Input Current

D/A CONVERTERS

DAC-01 = 6 Bit Voltage Output
DAC-02 = 10 Bit + Sign Voltage Output
DAC-03 = 10 Bit Low Cost Voltage Output
DAC-04 = 10 Bit Two's Complement
DAC-08 = 8 Bit Universal High Speed
DAC-76 = 8 Bit Companding
DAC-100 = 10 Bit Current Output

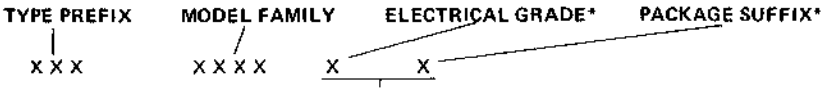
VOLTAGE REFERENCES

REF-01 = +10V Adjustable
REF-02 = +5V Adjustable

MATCHED TRANSISTORS

MAT-01 = Ultra-matched Monolithic Transistors

ORDERING INFORMATION



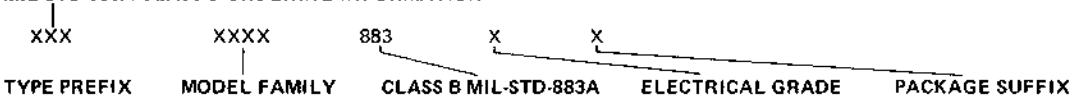
See the specific data sheet for available combinations.

*Except DAC-100. See the DAC-100 data sheet.

PACKAGE SUFFIX:

PACKAGE	DESCRIPTION	PACKAGE	DESCRIPTION	PACKAGE	DESCRIPTION
H	6 Pin TO-78	L	10 Pin Hermetic Flatpack	Y	14 Pin Hermetic Dip
J	8 Pin TO-99	M	14 Pin Hermetic Flatpack	Q	16 Pin Hermetic Dip
K	10 Pin TO-100	N	24 Pin Hermetic Flatpack	X	18 Pin Hermetic Dip
		P	8 Pin Epoxy B Mini Dip	V	24 Pin Hermetic Dip

MIL-STD-883A CLASS B ORDERING INFORMATION



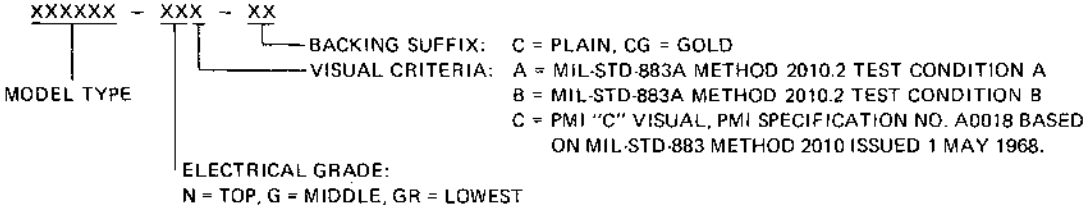
All PMI -55° to +125°C devices are available in versions with screening to Class B of MIL-STD-883A as standard. A complete list is included in the HI-REL section of this catalog. For all products except DAC-100, the part number construction is as shown below; for DAC-100, see the DAC-100 data sheet.

Example: To order OP-01FJ with 883B screening.

1. Basic Device Part Number: OP-01FJ
2. MIL-STD-883A Class B Version: OP01-883-FJ

CHIP ORDERING INFORMATION

All PMI chips are available with either plain backing or, at extra cost, 1-micron thich eutectic-bonded gold backing. Electrical performance is specified at 25°C for all products in the data sheet section of this catalog. Visual inspection criteria is as listed below:



For price and delivery information or quotations for special devices, contact the nearest PMI sales office or representative listed in the back of this catalog.

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Q.A. PROGRAM

MANUFACTURING AND SCREENING PROCEDURES

INTRODUCTION

Precision Monolithics, Inc., in establishing standard procedures for Manufacturing; Screening, Qualification, and Quality Conformance, has incorporated the requirements of both MIL-STD-883A, Notice 2 of March 1976, and MIL-Q-9858A. All PMI military temperature range devices meet or exceed Class C requirements, and, in addition, devices meeting and/or exceeding Class B requirements are available off-the-shelf as standard catalog items. Requests for devices with Class A or other special requirements are invited. The internal procedures designed to control and guarantee production of these devices are described herein.

PMI standard "883" parts designate devices which have been subjected to 100% screening in accordance with Method 5004 of MIL-STD-883A, Class B.

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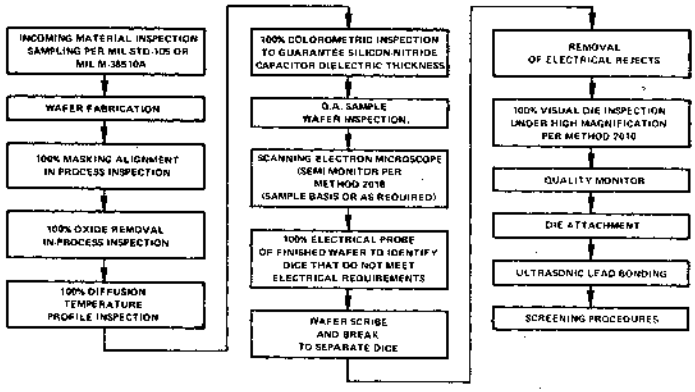
Quality Conformance Testing (Groups A, B, C, D) in accordance with Method 5005 of MIL-STD-883A is available on special order.

STANDARD MANUFACTURING PROCEDURE FOR ALL DEVICES



SCREENING LEVELS

MIL-STD-883A DEFINES 3 LEVELS OF MICROELECTRONIC SCREENING:

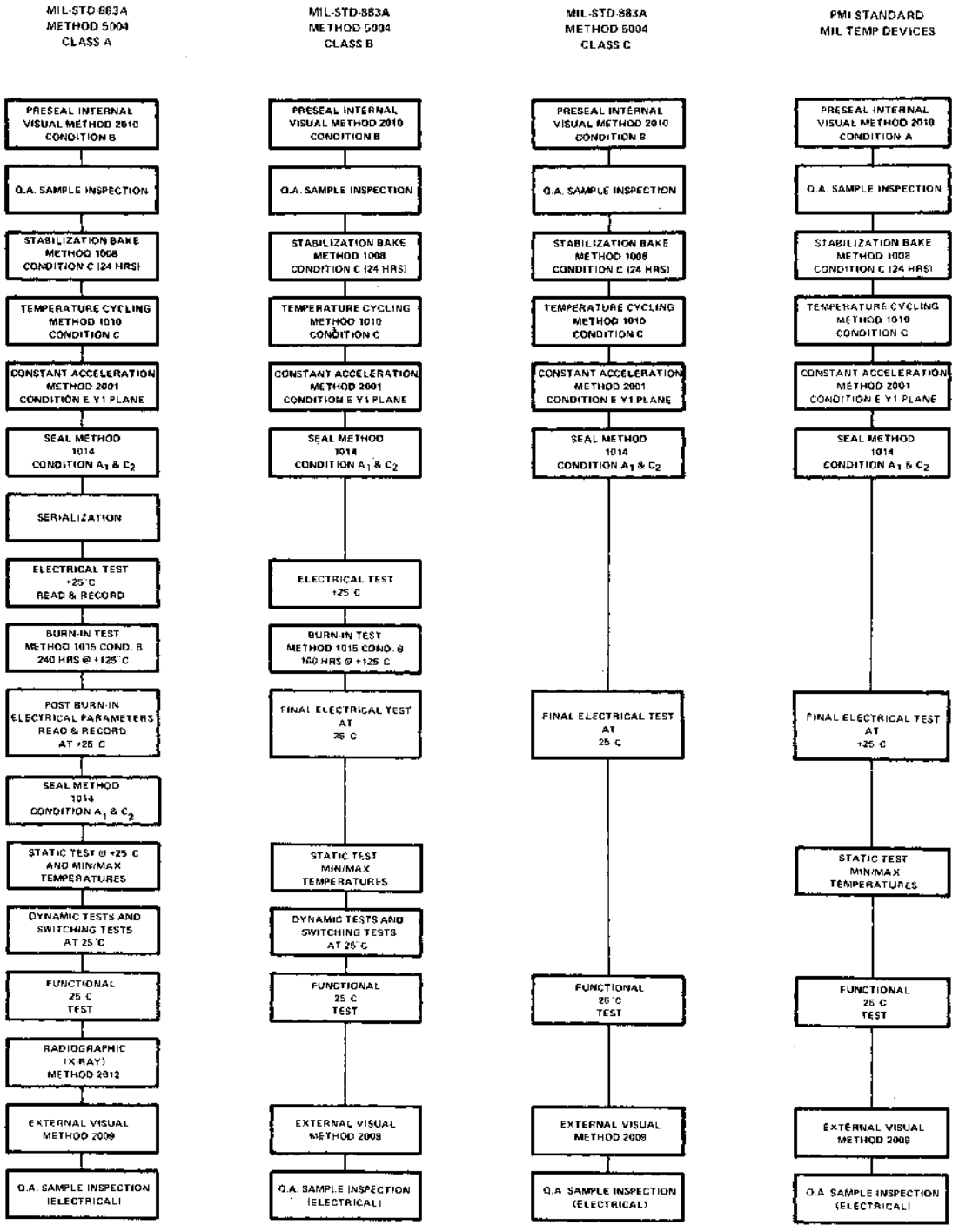
***CLASS A –** Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.

***CLASS B –** Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is vital.

***CLASS C –** Devices intended for use where maintenance and replacement can be readily accomplished and down time is not a critical factor. (All PMI Mil Temp Range devices meet or exceed Level C.)

Screening procedures for all 3 classes and for Precision Monolithics standard military temperature range devices are shown on the following page.

SCREENING PROCEDURES



QUALIFICATION AND QUALITY CONFORMANCE PROCEDURES

MIL-STD-883A Method 5005 establishes Qualification and Quality Conformance Procedures for the 3 classes of devices and divides these procedures into group A, B, C&D tests: "The full requirements of group A, B, C and D tests and inspections are intended for use in initial device qualification, requalification in the event of product or process change and periodic testing for retention of qualification. Group A and B tests and inspections are intended for quality conformance inspection of individual inspection lots as a condition for acceptance for delivery."

Group A, B, C and D quality conformance tests are performed using a sample size determined from the LTPD table below. An initial sample size corresponding to zero rejects (an acceptance number of 0) is normally used; if necessary the sample size will be increased once to a higher number to meet the LTPD requirement for the class of device under test.

LOT TOLERANCE PERCENT DEFECTIVE (LTPD) TABLE (PER MIL-M-38510A)

ACCEPTANCE NUMBER*	LTPD 20	LTPD 15	LTPD 10	LTPD 7	LTPD 5	LTPD 3
	Minimum Sample Size					
0	11	15	22	32	45	76
1	18	25	38	55	77	129
2	25	34	52	75	105	176
3	32	43	65	94	132	221
4	38	52	78	113	158	265

*Maximum allowable number of failures.

GROUP A ELECTRICAL TESTS: REFERENCE MIL-STD-883A METHOD 5005
(Electrical tests per applicable data sheet specifications)

SUBGROUP	TEST DESCRIPTION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
1	Static tests at 25°C	5	5	5
2	Static tests at maximum rated operating temperature	7	7	10
3	Static tests at minimum rated operating temperature	7	7	10
4	Dynamic tests at 25°C	5	5	5
7	Functional tests at 25°C	5	5	5
9	Switching tests at 25°C	7	7	10

GROUP B TESTS FOR CLASS A DEVICES

TEST	MIL-STD-883		CLASS A QUANTITY/(ACCEPT NO.)	
	METHOD	CONDITION	LOT 1	LOT 2 AND SUBSEQUENT
Subgroup 1				
Physical dimensions	2016		2(0)	2(0)
Subgroup 2 2/				
(a) Resistance to solvents	2015		3(0)	3(0)
(b) Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document	2(0)	2(0)
(c) Bond strength	2011		2(0) 7/	2(0) 7/
(1) Thermocompression		(1) Test condition C or D		
(2) Ultrasonic		(2) Test condition C or D		
(3) Flip-chip		(3) Test condition F		
(4) Beam lead		(4) Test condition H		
(d) Die shear test	2019	Per table I of method 2019 for the applicable die size	3(0)	3(0)

GROUP B TESTS FOR CLASS A DEVICES – CONTINUED

TEST	MIL-STD-883		CLASS A QUANTITY/ACCEPT NO.)	
	METHOD	CONDITION	LOT 1	LOT 2 AND SUBSEQUENT
Subgroup 3				
Solderability 3/	2003	Soldering temperature of 260 ± 10°C	LTPD = 15	LTPD = 15
Subgroup 4				
Lead integrity	2004	Test condition B_2, lead fatigue	2(0)	2(0)
Seal	1014	As applicable		
(a) Fine				
(b) Gross 4/				
Subgroup 5 6/				
(a) Gate 1				
(1) Electrical parameters		Group A, subgroup 1, 2, 3. Read and record		
(2) Steady state life (accelerated)	1005	Group A, subgroups 4-11: Attributes Condition F, 250°C 120 continuous hours minimum		
(3) Electrical parameters		Group A, subgroups 1, 2, 3. Read and record	40(8)	10(2)
(b) Gate 2				
(1) Steady state life (accelerated)	1005	Condition F, 250°C, 250 hours minimum including actual gate 1 life test duration		
(2) Seal				
a. Fine				
b. Gross 4/				
(3) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record Group A, subgroups 4-11: Attributes	40(16) 5/	10(4) 5/
Subgroup 6 2/				
(a) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record		
(b) Temperature cycling	1010	Condition C 100 cycles/min.	12(0)	5(0)
(c) Constant acceleration	2001	Test Condition E: Y_1 axis followed by one other axis, X or Z.		
(d) Seal	1014		or	or
(1) Fine				
(2) Gross 4/			20(1)	8(1)
(e) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record		

1 Electrical reject devices from the same inspection may be used for all subgroups when end point measurements are not required.

2 For class A lot quality conformance testing, all samples for subgroup B2 must have been through the complete sequence of subgroup B6 tests.

3 All devices must have been through the temperature/time exposure in burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

4 When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as a minimum.

5 Sample quantity for acceptance purposes is the incoming sample for gate 1 and the accept number applies to the total failures from both gate 1 and gate 2.

6 The alternate removal-of-bias provisions of paragraph 3.2.1 of methods 1005 and 1015 shall not apply for test temperatures above 125°C.

7 Pull ten (10) wires minimum per device or pull all wires if ten are not available.

GROUP B TESTS FOR CLASSES B AND C

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASSES B & C LTPD
Subgroup 1			
Physical dimensions	2016		2 devices (no failures)
Subgroup 2			
(a) Resistance to solvents	2015		3 devices (no failures)
(b) Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document.	1 device (no failures)
(c) Bond strength 2/	2011		15
(1) Thermocompression		(1) Test condition C or D	
(2) Ultrasonic or wedge		(2) Test condition C or D	
(3) Flip-chip		(3) Test condition F	
(4) Beam lead		(4) Test condition H	
Subgroup 3			
Solderability 3/	2003	Soldering temperature of 260 ± 10°C.	15

1 Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.

2 Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.

3 All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

GROUP C (DIE-RELATED TESTS) (FOR CLASSES B AND C ONLY)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD
Subgroup 1			
Operating life test 1/	1005	Test condition to be specified (1000 hours)	5
End point electrical parameters		As specified in the applicable device specification	
Subgroup 2			
Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E min. (see 3) Y_1 axis followed by one other axis X or Z.	
SEAL	1014	As applicable	
Fine			
Gross 3/			
Visual examination	2		
End point electrical parameters		As specified in the applicable device specification.	

1 See 40.4 of appendix B of MIL-M-38510.

2 Visual examination shall be in accordance with method 1010.

3 When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.

GROUP D (PACKAGE RELATED TESTS) (FOR ALL CLASSES)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2 4/			
Lead integrity	2004	Test condition B2 (lead fatigue)	15
Seal	1014	As applicable	
(a) Fine			
(b) Gross 6/			
Subgroup 3 1/			
Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum.	15
Temperature cycling	1010	Test condition C, 100 cycles minimum.	
Moisture resistance	1004		
Seal	1014	As applicable.	
(a) Fine			
(b) Gross 6/			
Visual examination	2/		
End point electrical parameters		As specified in the applicable device specification.	
Subgroup 4 1/			
Mechanical shock	2002	Test condition B	15
Vibration variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E (see 3)	
Seal	1014	As applicable	
(a) Fine			
(b) Gross 6/			
Visual examination	3/		
End point electrical parameters		As specified in the applicable device specification.	
Subgroup 5 4/			
Salt atmosphere	1009	Test condition A	15
Visual examination	5/		

1 Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical."

2 Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.

3 Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.

MODELS AVAILABLE WITH MIL-STD-883A CLASS B PROCESSING STANDARD

DIGITAL-TO-ANALOG CONVERTERS

DAC-01-883-Y
DAC01-883-BY
DAC-01-883-FY
DAC05-883-AX1 (or X2)
DAC05-883-BX1 (or X2)
DAC05-883-CX1 (or X2)
DAC06-883-AX
DAC-883-BX
DAC06-883-CX
DAC06-883-AQ
DAC08-883-Q
DAC20-883-AQ
DAC20-883-Q
DAC76-883-BX
DAC76-883-X
DAC-100 (NOTE)
SSS1508A-883-BQ

NOTE: See the DAC-100 data sheet for available models.

PRECISION VOLTAGE REFERENCES

REF01-883-AJ
REF01-883-J
REF02-883-AJ
REF02-883-J

PRECISION VOLTAGE COMPARATORS

CMP01-883-J
CMP01-883-Y
CMP02-883-J
CMP02-883-Y

MATCHED DUAL TRANSISTORS

MAT01-883-AH
MAT01-883-H
MAT01-883-FH
MAT01-883-GH

PRECISION OPERATIONAL AMPLIFIERS

OP01-883-J
OP01-883-Y
OP01-883-FY
OP01-883-FJ
OP01-883-GJ
OP01-883-GY
OP02-883-AJ
OP02-883-AY
OP02-883-J
OP02-883-Y
OP05-883-AJ
OP05-883-AY
OP05-883-J
OP05-883-Y
OP07-883-AJ
OP07-883-AY
OP07-883-J
OP07-883-Y
OP08-883-AJ
OP08-883-BJ
OP08-883-CJ
OP09-883-AY
OP09-883-BY
OP10-883-AY
OP10-883-Y
OP11-883-AY
OP11-883-BY
OP12-883-AJ
OP12-883-BJ
OP12-883-CJ
OP15-883-AJ
OP15-883-BJ
OP15-883-CJ
OP16-883-AJ
OP16-883-BJ
OP16-883-CJ
OP17-883-AJ
OP17-883-BJ
OP17-883-CJ
SSS725-883-AJ
SSS725-883-AY
SSS725-883-J
SSS725-883-Y
PM725-883-J
PM725-883-Y
PM108-883-AJ
PM108-883-J

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

SSS741-883-J
SSS741-883-Y
SSS741-883-GJ
SSS741-883-GY
PM741-883-J
PM741-883-Y
SSS747-883-K
SSS747-883-Y
SSS747-883-GK
SSS747-883GY
PM747-883-K
PM747-883-Y
SSS1558-883-J
PM1558-883-J
PM4136-883-Y

GENERAL PURPOSE FET INPUT OPERATIONAL AMPLIFIERS

PM155-883-AJ
PM155-883-J
PM156-883-AJ
PM156-883-J
PM157-883-AJ
PM157-883-J

DUAL MATCHED HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

OP04-883-Y
OP04-883-K
OP14-883-AJ
OP14-883-J

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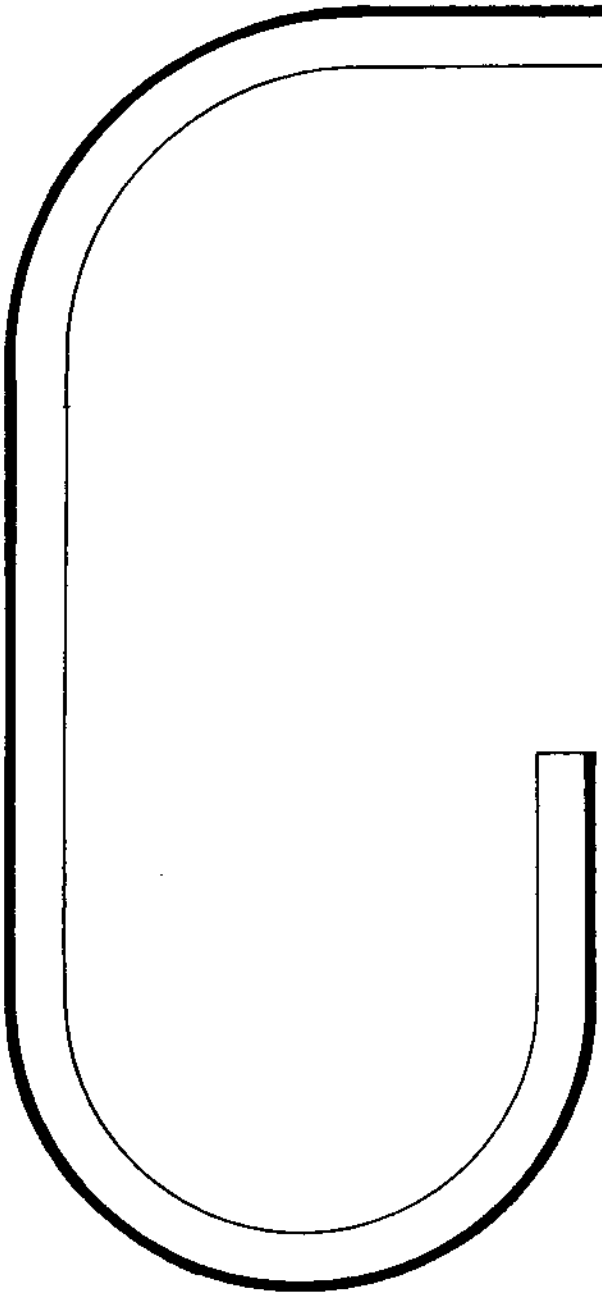

INTERCHANGEABILITY GUIDE

FAIRCHILD	PMI DIRECT REPLACEMENT	PMI IMPROVED DIRECT REPLACEMENT	TEMP RANGE	PACKAGE
LM108AH	PM108AJ	OP-08AJ	MIL	TO-99
LM108H	PM108J	OP-08BJ	MIL	TO-99
LM208H	PM208J	OP-08BJ	IND	TO-99
LM308AH	PM308AJ	OP-08EJ	COM	TO-99
LM308H	PM308J	OP-08FJ	COM	TO-99
725AHM	SSS725J	SSS725AJ	MIL	TO-99
725HM	PM725J	SS725J	MIL	TO-99
725HC	PM725CJ	SSS725EJ	COM	TO-99
725EHC		SS725EJ	COM	TO-99
725PC	PM725CP		COM	MINI-DIP
741HM	PM741J	SSS741GJ	MIL	TO-99
741HC	SSS741CJ	OP-02CJ	COM	TO-99
741DM	PM741Y	SSS741GY	MIL	DIP
741DC	SSS741CY	OP-02CY	COM	DIP
741AHM	OP-02J	OP-02AJ	MIL	TO-99
741EHC	OP-02CJ	OP-02EJ	COM	TO-99
741ADM	OP-02Y	OP-02AY	MIL	DIP
741EDC	OP-02CY	OP-02EY	COM	DIP
747DM	PM747Y	SSS747GY	MIL	DIP
747DC	SSS747CY	OP-04CY	COM	DIP
747HM	PM747K	SSS747GK	MIL	TO-100
747HC	SSS747CK	OP-04CK	COM	TO-100
747ADM		SSS747Y	MIL	DIP
747EDC		SSS747BY	COM	DIP
747AHM		SSS747K	MIL	TO-100
747EHC		SSS747BK	COM	TO-100
801ADM		DAC-08AQ	MIL	DIP
801DM		DAC-08Q	MIL	DIP
801EDC		DAC-08EQ	COM	DIP
801CDC		DAC-08CQ	COM	DIP
802DM		SSS1508A-8Q	MIL	DIP
802ADC		SSS1408A-8Q	COM	DIP
802BDC		SSS1408A-7Q	COM	DIP
802CDC		SSS1408A-6Q	COM	DIP

NATIONAL SEMICONDUCTOR	PMI DIRECT REPLACEMENT	PMI IMPROVED DIRECT REPLACEMENT	TEMP RANGE	PACKAGE
LM108AH	PM108AJ	OP-08AJ	MIL	TO-99
LM108H	PM108J	OP-08BJ	MIL	TO-99
LM208H	PM208J	OP-08BJ	IND	TO-99
LM308AH	PM308AJ	OP-08EJ	COM	TO-99
LM308H	PM308J	OP-08FJ	COM	TO-99
LF155AH	PM155AJ	OP-15AJ	MIL	TO-99
LF155H	PM155J	OP-15BJ	MIL	TO-99
LF255H	PM255J	OP-15BJ	IND	TO-99
LF355AH	PM355AJ	OP-15EJ	COM	TO-99
LF355H	PM355J	OP-15GJ	COM	TO-99
LF156AH	PM156AJ	OP-16AJ	MIL	TO-99
LF156H	PM156J	OP-16BJ	MIL	TO-99
LF256	PM256J	OP-16BJ	IND	TO-99
LF356AH	PM356AJ	OP-16EJ	COM	TO-99
LF356H	PM356J	OP-16GJ	COM	TO-99
LF157AH	PM157AJ	OP-17AJ	MIL	TO-99
LF157H	PM157J	OP-17BJ	MIL	TO-99
LF257H	PM257J	OP-17BJ	IND	TO-99
LF357AH	PM357AJ	OP-17EJ	COM	TO-99
LF357H	PM357J	OP-17GJ	COM	TO-99
LM725AH	SSS725J	SSS725AJ	MIL	TO-99
LM725H	PM725J	SSS725J	MIL	TO-99
LM725CH	PM725CJ	SSS725CJ	COM	TO-99
LM725D	PM725Y	SSS725Y	MIL	DIP
LM725CN	PM725CP		COM	MINI-DIP
LM741H	PM741J	SSS741GJ	MIL	TO-99
LM741CH	SSS741CJ	OP-02CJ	COM	TO-99
LM741D	PM741Y	SSS741GY	MIL	DIP
LM741CD	SSS741CY	OP-02CY	COM	DIP
LM747H	PM747J	SSS747GK	MIL	TO-100
LM747CH	SSS747CK	OP-04CK	COM	TO-100
LM747F		SSS747GM	MIL	FLATPACK
LM747CF		SSS747BM	COM	FLATPACK
LM747D	PM747Y	SSS747GY	MIL	DIP
LM747CD	SSS747CY	OP-04CY	COM	DIP
LM1458H	SSS1458	OP-14CJ	COM	TO-99
LM1558H	PM1558	SSS1558	MIL	TO-99
LF11508		MUX-88	MIL	DIP
LMDAC08		DAC-08	MIL	DIP

RAYTHEON	PMI DIRECT REPLACEMENT	PMI IMPROVED DIRECT REPLACEMENT	TEMP RANGE	PACKAGE
LM108AH	PM108AJ	OP-08AJ	MIL	TO-99
LM108H	PM108J	OP-08BJ	MIL	TO-99
LM208H	PM208J	OP-08BJ	IND	TO-99
LM308AH	PM308AJ	OP-08EJ	COM	TO-99
LM308H	PM308J	OP-08FJ	COM	TO-99
RM725T	PM725J	SSS725J	MIL	TO-99
RC725T	PM725CJ	SSS725CJ	COM	TO-99
RM741T	PM741J	SSS741GJ	MIL	TO-99
RC741T	SSS741CJ	OP-02CJ	COM	TO-99
RM741D	PM741Y	SSS741GY	MIL	TO-99
RC741D	SSS741CY	OP-02CY	COM	TO-99
RC741DP		SSS741CY	COM	TO-99
RM747T	PM747K	SSS747K	MIL	TO-100
RC747T	SSS747CK	OP-04CK	COM	TO-100
RM747D	PM747Y	SSS747Y	MIL	DIP
RC747D	SSS747CY	OP-04CY	COM	DIP
RC747DP		SSS747CY	COM	DIP
RM1558T	PM1558	SSS1558	MIL	TO-99
RC1458T	SSS1458	OP-14CJ	COM	TO-99
RM4136	PM4136Y	OP-09BY	MIL	DIP
RC4136	PM4136CY	OP-09FY	COM	DIP
TEXAS INSTRUMENTS				
SN52558L	PM1558	SSS1558	MIL	TO-99
SN72558L	SSS1458	OP-14CJ	COM	TO-99
SN52741L	PM741J	SSS741GJ	MIL	TO-99
SN52741J	PM741Y	SSS741GY	MIL	DIP
SN72741L	SSS741CJ	OP-02CJ	COM	TO-99
SN72741J	SSS741CY	OP-02CY	COM	DIP
SN52747L	PM747K	SSS747GK		TO-100
SN52747J	PM747Y	SSS747GY		DIP
SN52747Z		SSS747GM		FLATPACK
SN72747L		SSS747CK		TO-100
SN72747J		SSS747CY		DIP
TL081ACL		OP-16FJ	COM	TO-99
TL081CL		OP-16GJ	COM	TO-99
TL081AML		OP-16BJ	MIL	TO-99
TL081ML		OP-16CJ	MIL	TO-99

ADVANCED MICRO DEVICES	PMI DIRECT REPLACEMENT	PMI IMPROVED DIRECT REPLACEMENT	TEMP RANGE	PACKAGE
SSS725AJ	SSS725AJ		MIL	TO-99
SSS725J	SSS725J		MIL	TO-99
SSS725BJ	SSS725BJ		IND	TO-99
SSS725EJ	SSS725EJ		COM	TO-99
SSS741J	SSS741J	OP-02AJ	MIL	TO-99
SSS741CJ	SSS741CJ	OP-02EJ	COM	TO-99
SSS747K	SSS747K	OP-04AK	MIL	TO-100
SSS747P	SSS747Y	OP-04AY	MIL	DIP
SSS747M	SSS747M		MIL	FLATPACK
SSS747CK	SSS747CK	OP-04CK	COM	TO-100
SSS747CP	SSS747CY	OP-04CY	COM	DIP
SSS1508A-8Q	SSS1508A-8Q		MIL	DIP
SSS1408A-8Q	SSS1408A-8Q		COM	DIP
SSS1408A-7Q	SSS1408A-7Q		COM	DIP
SSS1408A-6Q	SSS1408A-6Q		COM	DIP
AM1508L8		SSS1508A-8Q	MIL	DIP
AM1408L8		SSS1408A-8Q	COM	DIP
AM1408L7		SSS1408A-7Q	COM	DIP
AM1408L6		SSS1408A-6Q	COM	DIP
DAC-08AQ	DAC-08AQ		MIL	DIP
DAC-08Q	DAC-08Q		MIL	DIP
DAC-08HQ	DAC-08HQ		COM	DIP
DAC-08EQ	DAC-08EQ		COM	DIP
DAC-08CQ	DAC-08CQ		COM	DIP
ANALOG DEVICES				
AD562SD/BIN		SSS562-SD-BIN	MIL	DIP
AD562SD/BCD		SSS562-SD-BCD	MIL	DIP
AD562AD/BIN		SSS562-AD-BIN	IND	DIP
AD562AD/BCD		SSS562-AD-BCD	IND	DIP
AD562KD/BIN		SSS562-KD-BIN	COM	DIP
AD562KD/BCD		SSS562-KD-BCD	COM	DIP
SIGNETICS				
SE5009		DAC-08AQ	MIL	DIP
SE5008		DAC-08Q	MIL	DIP
NE5008		DAC-08EQ	COM	DIP
NE5007		DAC-08CQ	COM	DIP

RCA	PMI DIRECT REPLACEMENT	PMI IMPROVED DIRECT REPLACEMENT	TEMP RANGE	PACKAGE
CA108AT		PM108AJ	MIL	TO-99
CA108T		PM108J	MIL	TO-99
CA208AT		PM208AJ	IND	TO-99
DA208T		PM208J	IND	TO-99
CA308AT		PM308AJ	COM	TO-99
CA308T		PM308J	COM	TO-99
CA741T	PM741J	SSS741GJ	MIL	TO-99
CA741CT	SSS741CJ	OP-02CJ	COM	TO-99
CA747T	PM-747K	SSS747K	MIL	TO-100
CA747CT	SSS747CK	OP-04CK	COM	TO-100
CA747E	PM747Y	SSS747Y	MIL	DIP
CA747CE	SSS747CY	OP-04CY	COM	DIP
CA1458T	SSS1458	OP-14CJ	COM	TO-99
CA1558T	PM1558	SSS1558	MIL	TO-99
MOTOROLA				
MC1741G	PM741J	SSS741GJ	MIL	TO-99
MC1741L	PM741Y	SSS741GY	MIL	DIP
MC1741CG	SSS741CJ	OP-02CJ	COM	TO-99
MC1741CL	SSS741CY	OP-02CY	COM	DIP
MC1558G	PM1558	SSS1558	MIL	TO-99
MC1458G	SSS1458	OP-14EJ	COM	TO-99
MC1458CG	SSS1458	OP-14CJ	COM	TO-99
MC1508L-8		SSS1508A-8Q	MIL	DIP
MC1408L-8		SSS1408A-8Q	COM	DIP
MC1408L-7		SSS1408A-7Q	COM	DIP
MC1408L-6		SSS1408A-6Q	COM	DIP

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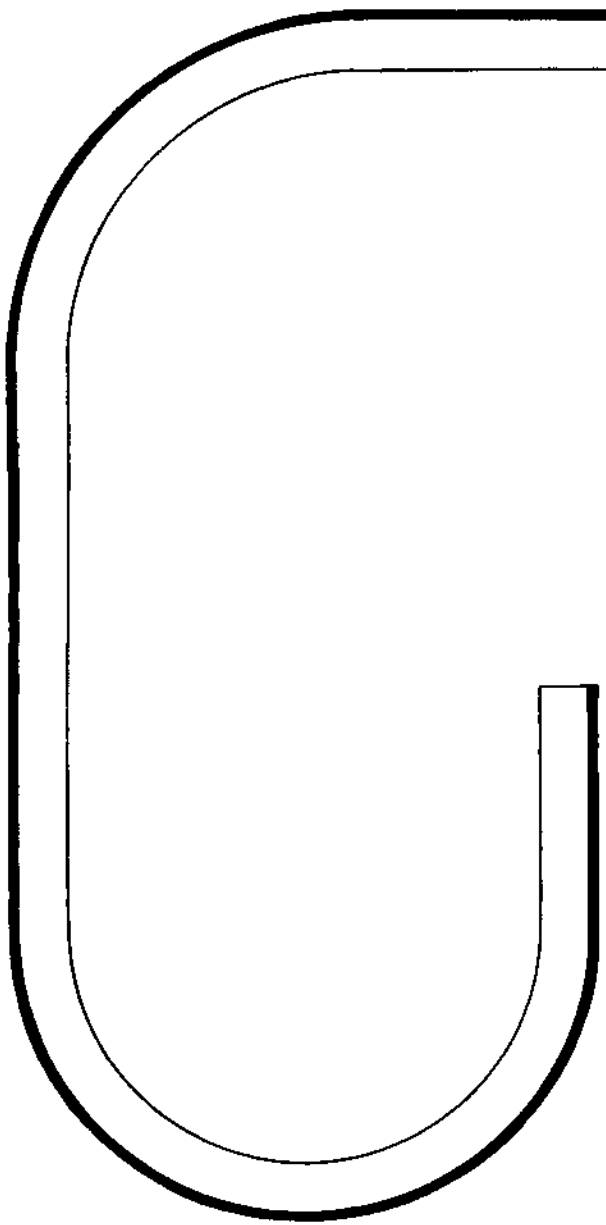

FUNCTIONAL EQUIVALENT GUIDE

THE FOLLOWING TABLES SHOW PMI DESIGN ALTERNATIVES TO OTHER MANUFACTURERS' DEVICES: IC'S, HYBRIDS, AND MODULES. THESE ARE USUALLY NOT DIRECT PIN-FOR-PIN ELECTRICAL AND MECHANICAL REPLACEMENTS, BUT RATHER, THEY ARE FUNCTIONAL EQUIVALENTS. PERFORMANCE AND SPECIFICATIONS ARE SIMILAR.

ANALOG DEVICES	DEVICE DESCRIPTION	PMI NEAREST EQUIVALENT	APPLICATION COMMENTS
AD504	PRECISION OP AMP	OP-05	NULLED.
AD509	HIGH SPEED OP AMP	OP-16	FAST SETTLING.
AD510	PRECISION OP AMP	OP-05	NULLED.
AD510	PRECISION OP AMP	OP-07	UNNULLED.
AD559	8-BIT MULTIPLYING D/A CONVERTER	DAC-08	MULTIPLYING.
AD580	VOLTAGE REFERENCE BANDGAP +2.5V	REF-02	REF-02 IS +5V REFERENCE.
AD741	IMPROVED 741 OP AMP	OP-02	PIN-FOR-PIN REPLACEMENT.
AD810	MATCHED TRANSISTOR PAIR	MAT-01	PIN-FOR-PIN REPLACEMENT.
AD818	MATCHED TRANSISTOR PAIR	MAT-01	LOG AMP APPLICATIONS.
AD2700	HYBRID +10V REFERENCE	REF-01	REF-01 IS IC AND LOW POWER.
AD7520	10-BIT MULTIPLYING DAC-CMOS	DAC-08	8-BIT APPLICATIONS
AD7520	10-BIT MULTIPLYING DAC-CMOS	DAC-100	10-BIT NON-MULTIPLYING APPLICATIONS.
CMOS MULTIPLEXERS	SEVERAL, CMOS TYPES	MUX-88	8 CHANNEL
FET OP AMPS	SEVERAL FET OP AMPS	OP-15/16/17	SELECT PMI DEVICE ACCORDING TO THE APPLICATION.

BURR BROWN

BB3505	HIGH SPEED OP AMP	OP-16	HIGHEST SPEED APPLICATIONS.
BB3506	HIGH SPEED OP AMP	OP-15	MEDIUM SPEED APPLICATIONS.
DAC-80/85	12-BIT DAC'S	SSS562	USE SSS562 WITH EXTERNAL REFERENCE.

HARRIS SEMICONDUCTOR	DEVICE DESCRIPTION	PMI NEAREST EQUIVALENT	APPLICATION COMMENTS
HA-2510	HIGH SPEED OP AMP	OP-16	PMI OP-15/16/17 REPLACE SEVERAL HARRIS TYPES IN SOME APPLICATIONS.
HA-2900	CHOPPER-STABILIZED PRECISION OP AMP	OP-07	SEE AN-13 ALSO.
HA-4741	QUAD OP AMP	OP-11	OP-11 HAS MUCH LOWER OFFSET VOLTAGE.

NATIONAL SEMICONDUCTOR			
LH0044	HYBRID PRECISION OP AMP	OP-07	MOST APPLICATIONS.
LH0044	HYBRID PRECISION OP AMP	OP-12	APPLICATIONS WHERE LESS THAN 1mA SUPPLY CURRENT IS REQUIRED.
LH0070	HYBRID +10V REFERENCE	REF-01	REF-01 MUCH LOWER POWER.
LM110/310	VOLTAGE FOLLOWER	OP-12	CONNECT OP-12 AS A FOLLOWER. LOW SPEED APPLICATIONS.
LM110/310	VOLTAGE FOLLOWER	OP-15/16	CONNECT OP-15/16 AS A FOLLOWER. HIGH SPEED APPLICATIONS.
LM111/311	VOLTAGE COMPARATOR	CMP-01	HIGH SPEED APPLICATIONS.
LM111/311	VOLTAGE COMPARATOR	CMP-02	LOW INPUT CURRENT APPLICATIONS.
LM114/115	MATCHED TRANSISTOR PAIR	MAT-01	PIN-FOR-PIN REPLACEMENT.
LM148	QUAD OP AMP	OP-11	OP-11 PIN-FOR-PIN WITH LOWER OFFSET VOLTAGES.
LM194/394	MATCHED TRANSISTOR PAIR	MAT-01	

CROSS REFERENCE – MAT-01 TO MONOLITHIC DUAL TRANSISTORS (I_C = 10μA)

DEVICE	BV_{CEO} MIN (V)	V_{os} MAX (mV)	TCV_{os} MAX (μV/°C)	h_{FE} MIN	I_{os} MAX (nA)	TCI_{os} MAX (pA/°C)
MAT-01AH	**45**	**0.1**	**0.5**	**500**	**0.6**	**90**
MAT-01H	**60**	**0.1**	**0.5**	**330**	**0.8**	**110**
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**3.2**	**150**
MAT-01GH	**45**	**0.5**	**1.8**	**250**	**3.2**	**150**
LM114A	45	0.5	2.0	500	2.0	–
LM114	45	2.0	10	250	10	–
LM115A	60	0.5	2.0	250	2.0	–
LM115	60	2.0	10	250	10	–
AD810	35	3.0	15	100	2.0	600
AD811	45	1.5	7.5	200	10	300
AD812	35	1.0	5.0	400	2.5	300
AD813	45	0.5	2.5	200	5	300
AD818	20	1.0	5.0	200	10	300

CROSS REFERENCE – MAT-01 TO 2N TYPES (I_C = 10μA)

DEVICE	BV_{CEO} MIN (V)	V_{OS} MAX (mV)	TCV_{OS} MAX (μV/°C)	h_{FE} MIN	$\%h_{FE}$ MATCH MAX	I_{OS} MAX (nA)	TCI_{OS} MAX (pA/°C)
MAT-01GH	**45**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

Notes: 1. TCI_{OS} Max and I_{OS} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of the above are physically interchangeable pin-for-pin with MAT-01 series.

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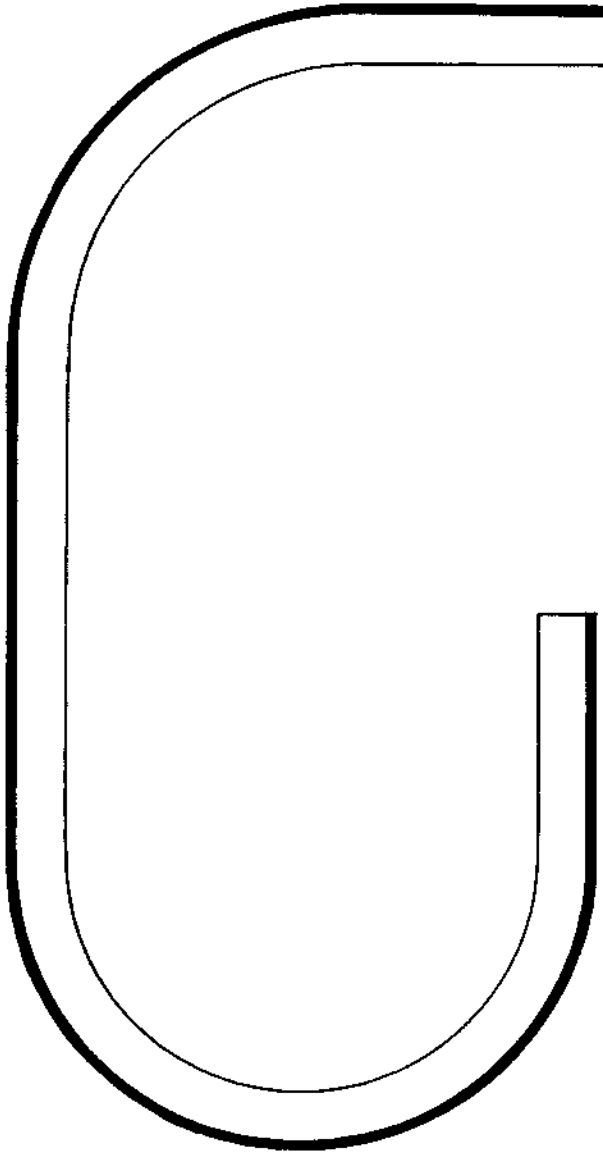

INTRODUCTION TO PMI OPERATIONAL AMPLIFIERS

This section includes operational amplifiers suitable for most applications. Selection guides give key Min/Max specifications for singles, duals, and quads. This product line includes precision, superbeta, BIFET, and general purpose devices that provide a very wide range of performance parameters for both 0° to 70°C and -55° to +125°C operating temperature ranges.

New op amps introduced in the past year include: precision BIFETS (OP-15, OP-16, OP-17); second source BIFETS (PM155A, PM156A, PM157A); precision low power improved 108 types (OP-08, OP-12); second source quads (PM4136); and precision matched quads (OP-09, OP-11). All PMI military temperature range operational amplifiers are available with MIL-STD-883A Class B processing.

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SINGLE BIFET OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_J = 25°C	MAX, T_J = 125°C
OP-15A	50 pA	5.0 nA
OP-16A	50 pA	5.0 nA
OP-17A	50 pA	5.0 nA
PM-155A	50 pA	25 nA
PM-156A	50 pA	25 nA
PM-157A	50 pA	25 nA
OP-15B	100 pA	7.5 nA
OP-16B	100 pA	7.5 nA
OP-17B	100 pA	7.5 nA
PM-155	100 pA	50 nA
PM-156	100 pA	50 nA
PM-157	100 pA	50 nA
OP-15C	200 pA	10 nA
OP-16C	200 pA	10 nA
OP-17C	200 pA	10 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_J = 25°C	MAX, T_J = 70°C
OP-15E	50 pA	0.4 nA
OP-16E	50 pA	0.4 nA
OP-17E	50 pA	0.4 nA
PM-355A	50 pA	5.0 nA
PM-356A	50 pA	5.0 nA
PM-357A	50 pA	5.0 nA
OP-15F	100 pA	0.6 nA
OP-16F	100 pA	0.6 nA
OP-17F	100 pA	0.6 nA
OP-15G	200 pA	0.8 nA
OP-16G	200 pA	0.8 nA
OP-17G	200 pA	0.8 nA
PM-355	200 pA	8.0 nA
PM-356	200 pA	8.0 nA
PM-357	200 pA	8.0 nA

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_J = 25°C	MAX, T_J = 125°C
OP-15A	10 pA	4.0 nA
OP-16A	10 pA	4.0 nA
OP-17A	10 pA	4.0 nA
PM-155A	10 pA	10 nA
PM-156A	10 pA	10 nA
PM-157A	10 pA	10 nA
OP-15B	20 pA	6.0 nA
OP-16B	20 pA	6.0 nA
OP-17B	20 pA	6.0 nA
PM-155	20 pA	20 nA
PM-156	20 pA	20 nA
PM-157	20 pA	20 nA
OP-15C	50 pA	9.0 nA
OP-16C	50 pA	9.0 nA
OP-17C	50 pA	9.0 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_J = 25°C	MAX, T_J = 70°C
OP-15E	10 pA	0.3 nA
OP-16E	10 pA	0.3 nA
OP-17E	10 pA	0.3 nA
PM-355A	10 pA	1.0 nA
PM-356A	10 pA	1.0 nA
PM-357A	10 pA	1.0 nA
OP-15F	20 pA	0.45 nA
OP-16F	20 pA	0.45 nA
OP-17F	20 pA	0.45 nA
OP-15G	50 pA	0.65 nA
OP-16G	50 pA	0.65 nA
OP-17G	50 pA	0.65 nA
PM-355	50 pA	2.0 nA
PM-356	50 pA	2.0 nA
PM-357	50 pA	2.0 nA

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX, T_A = 125°C
OP-15A	110 pA	9.0 nA
OP-16A	130 pA	11 nA
OP-17A	130 pA	11 nA
OP-15B	200 pA	14 nA
OP-16B	250 pA	18 nA
OP-17B	250 pA	18 nA
OP-15C	400 pA	19 nA
OP-16C	500 pA	25 nA
OP-17C	500 pA	25 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX, T_A = 70°C
OP-15E	110 pA	0.75 nA
OP-16E	130 pA	0.9 nA
OP-17E	130 pA	0.9 nA
OP-15F	200 pA	1.1 nA
OP-16F	250 pA	1.4 nA
OP-17F	250 pA	1.4 nA
OP-15G	400 pA	1.5 nA
OP-16G	500 pA	2.0 nA
OP-17G	500 pA	2.0 nA

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX, T_A = 125°C
OP-15A	22 pA	7.0 nA
OP-16A	25 pA	8.5 nA
OP-17A	25 pA	8.5 nA
OP-15B	40 pA	11 nA
OP-16B	50 pA	14.5 nA
OP-17B	50 pA	14.5 nA
OP-15C	100 pA	17 nA
OP-16C	125 pA	22 nA
OP-17C	125 pA	22 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX, T_A = 70°C
OP-15E	22 pA	0.55 nA
OP-16E	25 pA	0.7 nA
OP-17E	25 pA	0.7 nA
OP-15F	40 pA	0.8 nA
OP-16F	50 pA	1.1 nA
OP-17F	50 pA	1.1 nA
OP-15G	100 pA	1.2 nA
OP-16G	125 pA	1.7 nA
OP-17G	125 pA	1.7 nA

SINGLE BIFET OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX, T_A = FULL
OP-15A	0.5 mV	0.9 mV
OP-16A	0.5 mV	0.9 mV
OP-17A	0.5 mV	0.9 mV
OP-15B	1.0 mV	2.0 mV
OP-16B	1.0 mV	2.0 mV
OP-17B	1.0 mV	2.0 mV
PM-155A	2.0 mV	2.5 mV
PM-156A	2.0 mV	2.5 mV
PM-157A	2.0 mV	2.5 mV
OP-15C	3.0 mV	4.5 mV
OP-16C	3.0 mV	4.5 mV
OP-17C	3.0 mV	4.5 mV
PM-155	5.0 mV	7.0 mV
PM-156	5.0 mV	7.0 mV
PM-157	5.0 mV	7.0 mV

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX, T_A = FULL
OP-15E	0.5 mV	0.75 mV
OP-16E	0.5 mV	0.75 mV
OP-17E	0.5 mV	0.75 mV
OP-15F	1.0 mV	1.5 mV
OP-16F	1.0 mV	1.5 mV
OP-17F	1.0 mV	1.5 mV
PM-355A	2.0 mV	2.3 mV
PM-356A	2.0 mV	2.3 mV
PM-357A	2.0 mV	2.3 mV
OP-15G	3.0 mV	3.8 mV
OP-16G	3.0 mV	3.8 mV
OP-17G	3.0 mV	3.8 mV
PM-355	10 mV	13 mV
PM-356	10 mV	13 mV
PM-357	10 mV	13 mV

MILITARY TEMPERATURE RANGE

SUPPLY CURRENT		INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})	
DEVICE	MAX, T_A = 25°C	DEVICE	MAX, T_A = FULL
OP-15A	4 mA	OP-15A	5.0 µV/°C
OP-15B	4 mA	OP-16A	5.0 µV/°C
PM-155A	4 mA	OP-17A	5.0 µV/°C
PM-155	4 mA	PM-155A	5.0 µV/°C
OP-15C	5 mA	PM-156A	5.0 µV/°C
OP-16A	7 mA	PM-157A	5.0 µV/°C
OP-16B	7 mA	OP-15B	10 µV/°C
OP-17A	7 mA	OP-16B	10 µV/°C
OP-17B	7 mA	OP-17B	10 µV/°C
PM-156A	7 mA	OP-15C	*15 µV/°C
PM-156	7 mA	OP-16C	*15 µV/°C
PM-157A	7 mA	OP-17C	*15 µV/°C
PM-157	7 mA		
OP-16C	8 mA		
OP-17C	8 mA		

COMMERCIAL TEMPERATURE RANGE

SUPPLY CURRENT		INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})	
DEVICE	MAX, T_A = 25°C	DEVICE	MAX, T = FULL
OP-15E	4 mA	OP-15E	5.0 µV/°C
OP-15F	4 mA	OP-16E	5.0 µV/°C
PM-355A	4 mA	OP-17E	5.0 µV/°C
PM-355	4 mA	PM-355A	5.0 µV/°C
OP-15G	5 mA	PM-356A	5.0 µV/°C
OP-16E	7 mA	PM-357A	5.0 µV/°C
OP-16F	7 mA	OP-15F	10 µV/°C
OP-17E	7 mA	OP-16F	10 µV/°C
OP-17F	7 mA	OP-17F	10 µV/°C
PM-356A	7 mA	OP-15G	*15 µV/°C
PM-357A	7 mA	OP-16G	*15 µV/°C
OP-16G	8 mA	OP-17G	*15 µV/°C
OP-17G	8 mA	PM-355	N/S
PM-356	10 mA	PM-356	N/S
PM-357	10 mA	PM-357	N/S

*Parameter not 100% tested. 90% of all units meet these specifications.
N/S — Not specified.

MILITARY TEMPERATURE RANGE
SLEW RATE

DEVICE	MIN, T_A = 25°C
OP-17A	*45 V/µsec
PM-157A	*40 V/µsec
OP-17B	*35 V/µsec
PM-157	*30 V/µsec
OP-17C	*25 V/µsec
OP-16A	18 V/µsec
OP-16B	12 V/µsec
OP-15A	10 V/µsec
PM-156A	10 V/µsec
OP-16C	9.0 V/µsec
OP-15B	7.5 V/µsec
PM-156	7.5 V/µsec
OP-15C	5.0 V/µsec
PM-155A	3.0 V/µsec

COMMERCIAL TEMPERATURE RANGE
SLEW RATE

DEVICE	MIN, T_A = 25°C
OP-17E	*45 V/µsec
PM-357A	*40 V/µsec
OP-17F	*35 V/µsec
OP-17G	*25 V/µsec
OP-16E	18 V/µsec
OP-16F	12 V/µsec
OP-15E	10 V/µsec
PM-356A	10 V/µsec
OP-16G	9.0 V/µsec
OP-15F	7.5 V/µsec
OP-15G	5.0 V/µsec
PM-355A	5.0 V/µsec
PM-355	N/S
PM-356	N/S
PM-357	N/S

*Closed Loop Gain = 5
N/S — Not specified.

SINGLE LOW POWER OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-08A	2.0 nA	3.0 nA
OP-08B	2.0 nA	3.0 nA
OP-12A	2.0 nA	3.0 nA
OP-12B	2.0 nA	3.0 nA
PM-108A	2.0 nA	3.0 nA
PM-108	2.0 nA	3.0 nA
OP-08C	5.0 nA	10.0 nA
OP-12C	5.0 nA	10.0 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-08E	2.0 nA	2.6 nA
OP-12E	2.0 nA	2.6 nA
OP-08F	4.0 nA	5.2 nA
OP-12F	4.0 nA	5.2 nA
OP-08G	5.0 nA	6.5 nA
OP-12G	5.0 nA	6.5 nA
PM-308A	7.0 nA	10.0 nA
PM-308	7.0 nA	10.0 nA

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-08A	0.2 nA	0.4 nA
OP-08B	0.2 nA	0.4 nA
OP-12A	0.2 nA	0.4 nA
OP-12B	0.2 nA	0.4 nA
PM-108A	0.2 nA	0.4 nA
PM-108	0.2 nA	0.4 nA
OP-08C	0.5 nA	1.0 nA
OP-12C	0.5 nA	1.0 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-08E	0.2 nA	0.3 nA
OP-12E	0.2 nA	0.3 nA
OP-08F	0.4 nA	0.6 nA
OP-12F	0.4 nA	0.6 nA
OP-08G	0.5 nA	0.7 nA
OP-12G	0.5 nA	0.7 nA
PM-308A	1.0 nA	1.5 nA
PM-308	1.0 nA	1.5 nA

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-08A	0.15 mV	0.35 mV
OP-12A	0.15 mV	0.35 mV
OP-08B	0.30 mV	0.60 mV
OP-12B	0.30 mV	0.60 mV
PM-108A	0.50 mV	1.0 mV
OP-08C	1.0 mV	2.0 mV
OP-12C	1.0 mV	2.0 mV
PM-108	2.0 mV	3.0 mV

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-08E	0.15 mV	0.26 mV
OP-12E	0.15 mV	0.26 mV
OP-08F	0.30 mV	0.45 mV
OP-12F	0.30 mV	0.45 mV
PM-308A	0.50 mV	0.73 mV
OP-08G	1.0 mV	1.4 mV
OP-12G	1.0 mV	1.4 mV
PM-308	7.5 mV	10.0 mV

MILITARY TEMPERATURE RANGE

SUPPLY CURRENT		INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})	
DEVICE	MAX, T_A = 25°C	DEVICE	MAX OVER TEMPERATURE
OP-08A	0.6 mA	OP-08A	2.5 µV/°C
OP-08B	0.6 mA	OP-12A	2.5 µV/°C
OP-12A	0.6 mA	OP-08B	3.5 µV/°C
OP-12B	0.6 mA	OP-12B	3.5 µV/°C
PM-108A	0.6 mA	PM-108A	5.0 µV/°C
PM-108	0.6 mA	OP-08C	10 µV/° C
OP-08G	0.8 mA	OP-12C	10 µV/° C
OP-12G	0.8 mA	PM-108	15 µV/° C

COMMERCIAL TEMPERATURE RANGE

SUPPLY CURRENT		INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})	
DEVICE	MAX, T_A = 25°C	DEVICE	MAX, OVER TEMPERATURE
OP-08E	0.6 mA	OP-08E	2.5 µV/°C
OP-08F	0.6 mA	OP-12E	2.5 µV/°C
OP-12E	0.6 mA	OP-08F	3.5 µV/°C
OP-12F	0.6 mA	OP-12F	3.5 µV/°C
OP-08G	0.8 mA	PM-308A	5.0 µV/°C
OP-12G	0.8 mA	OP-08G	10 µV/°C
PM-308A	0.8 mA	OP-12G	10 µV/°C
PM-308	0.8 mA	PM-308	30 µV/°C

SINGLE LOW POWER OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, $T_A = 25°C$ $R_L \geq 10K\Omega$	MIN OVER TEMPERATURE
OP-08A	80 V/mV	*40 V/mV
OP-08B	80 V/mV	*40 V/mV
OP-12A	80 V/mV	*40 V/mV
OP-12B	80 V/mV	*40 V/mV
PM-108A	80 V/mV	**40 V/mV
PM-108	50 V/mV	**25 V/mV
OP-08C	40 V/mV	*15 V/mV
OP-12C	40 V/mV	*15 V/mV

*$R_L \geq 5K\Omega$
**$R_L \geq 10K\Omega$

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, $T_A = 25°C$ $R_L \geq 10K\Omega$	MIN OVER TEMPERATURE $R_L \geq 10K\Omega$
OP-08E	80 V/mV	60 V/mV
OP-08F	80 V/mV	60 V/mV
OP-12E	80 V/mV	60 V/mV
OP-12F	80 V/mV	60 V/mV
PM-308A	80 V/mV	60 V/mV
OP-08G	40 V/mV	25 V/mV
OP-12G	40 V/mV	25 V/mV
PM-308	25 V/mV	15 V/mV

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, $T_A = 25°C$	MIN OVER TEMPERATURE
OP-08A	*50 V/mV	**40 V/mV
OP-08B	*50 V/mV	**40 V/mV
OP-12A	*50 V/mV	**40 V/mV
OP-12B	*50 V/mV	**40 V/mV
OP-08C	N/S	**15 V/mV
OP-12C	N/S	**15 V/mV

*$R_L \geq 2K\Omega$
**$R_L \geq 5K\Omega$
N/S — Not specified.

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, $T_A = 25°C$ $R_L \geq 2K\Omega$	MIN OVER TEMPERATURE $R_L \geq 2K\Omega$
OP-08E	50 V/mV	25 V/mV
OP-12E	50 V/mV	25 V/mV
OP-08F	30 V/mV	15 V/mV
OP-12F	30 V/mV	15 V/mV
OP-08G	N/S	N/S
OP-12G	N/S	N/S

MILITARY TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, $T_A = 25°C$	MIN OVER TEMPERATURE
OP-08A	104 dB	100 dB
OP-08B	104 dB	100 dB
OP-12A	104 dB	100 dB
OP-12B	104 dB	100 dB
OP-08C	84 dB	80 dB
OP-12C	84 dB	80 dB
PM-108A	N/S	96 dB
PM-108	N/S	85 dB

COMMERCIAL TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, $T_A = 25°C$	MIN OVER TEMPERATURE
OP-08E	104 dB	100 dB
OP-12E	104 dB	100 dB
OP-08F	102 dB	100 dB
OP-12F	102 dB	100 dB
OP-08G	84 dB	80 dB
OP-12G	84 dB	80 dB
PM-308A	N/S	96 dB
PM-308	N/S	80 dB

N/S — Not specified.

SINGLE PRECISION OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-07A	0.025 mV	0.06 mV
OP-07	0.075 mV	0.20 mV
SSS725A	0.10 mV	0.18 mV
OP-05A	0.15 mV	0.24 mV
OP-05	0.50 mV	0.70 mV
SSS725	0.50 mV	0.70 mV
OP-02A	0.50 mV	1.0 mV
PM-725	1.0 mV	1.5 mV
OP-02	2.0 mV	3.0 mV

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-07E	0.075 mV	0.13 mV
OP-07C	0.15 mV	0.25 mV
OP-07D	0.15 mV	0.25 mV
SSS725E	0.50 mV	0.60 mV
OP-05E	0.50 mV	0.60 mV
OP-02E	0.50 mV	1.0 mV
OP-05C	1.3 mV	1.6 mV
SSS725C	1.3 mV	1.6 mV
OP-02C	2.0 mV	3.0 mV
PM-725C	2.5 mV	3.5 mV

MILITARY TEMPERATURE RANGE

UNNULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})		NULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OSN})	
DEVICE	TCV_{os} MAX	DEVICE	TCV_{osn} MAX
OP-07A	0.6 µV/°C	OP-05A	0.5 µV/°C
SSS725A	0.8 µV/°C	OP-07A	0.6 µV/°C
OP-05A	0.9 µV/°C	SSS725A	0.6 µV/°C
OP-07	1.3 µV/°C	OP-05	1.0 µV/°C
OP-05	2.0 µV/°C	SSS725	1.0 µV/°C
SSS725	2.0 µV/°C	OP-07	1.3 µV/°C
PM-725	5.0 µV/°C		
OP-02A	*8.0 µV/°C		
OP-02	*10.0 µV/°C		

COMMERCIAL TEMPERATURE RANGE

UNNULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})		NULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OSN})	
DEVICE	TCV_{os} MAX	DEVICE	TCV_{osn} MAX
OP-07E	1.3 µV/°C	OP-05E	0.6 µV/°C
OP-07C	*1.8 V/°C	SSS725E	0.6 µV/°C
OP-05E	*2.0 V/°C	OP-07E	1.3 µV/°C
SSS725E	*2.0 V/°C	OP-05C	*1.5 µV/°C
OP-07D	*2.5 V/°C	SSS725C	*1.5 µV/°C
OP-05C	*4.5 V/°C	OP-07C	*1.6 µV/°C
SSS725C	*4.5 V/°C	OP-07D	*2.5 µV/°C
OP-02E	*8.0 V/°C		
OP-02C	* 10 V/°C		

*Parameter is not 100% tested.

90% of all units meet these specifications.

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
SSS725A	1.0 nA	4.0 nA
OP-05A	2.0 nA	4.0 nA
OP-07A	2.0 nA	4.0 nA
OP-02A	2.0 nA	5.0 nA
OP-05	2.8 nA	5.6 nA
OP-07	2.8 nA	5.6 nA
OP-02	5.0 nA	10 nA
SSS725	5.0 nA	18 nA
PM-725	20 nA	40 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-02E	2.0 nA	4.0 nA
OP-05E	3.8 nA	5.3 nA
OP-07E	3.8 nA	5.3 nA
SSS725E	5.0 nA	7.0 nA
OP-02C	5.0 nA	10 nA
OP-05C	6.0 nA	8.0 nA
OP-07C	6.0 nA	8.0 nA
OP-07D	6.0 nA	8.0 nA
SSS725C	13 nA	25 nA
PM-725C	35 nA	50 nA

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-05A	2.0 nA	4.0 nA
OP-07A	2.0 nA	4.0 nA
OP-05	3.0 nA	6.0 nA
OP-07	3.0 nA	6.0 nA
OP-02A	30 nA	55 nA
OP-02	50 nA	100 nA
SSS725A	70 nA	120 nA
SSS725	80 nA	180 nA
PM-725	100 nA	200 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-05E	4.0 nA	5.5 nA
OP-07E	4.0 nA	5.5 nA
OP-05C	7.0 nA	9.0 nA
OP-07C	7.0 nA	9.0 nA
OP-07D	12 nA	14 nA
OP-02E	30 nA	55 nA
OP-02C	50 nA	100 nA
SSS725E	80 nA	100 nA
SSS725C	110 nA	180 nA
PM-725C	125 nA	250 nA

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MILITARY TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

DEVICE	T_A = 25°C MIN (dB)	T_A = 25°C MAX (μV/V)	OVER TEMPERATURE MIN (dB)	OVER TEMPERATURE MAX (μV/V)
SSS725A	114 dB	2.0 μV/V	106 dB	5.0 μV/V
SSS725	106 dB	5.0 μV/V	102 dB	8.0 μV/V
OP-05A	100 dB	10 μV/V	94 dB	20 μV/V
OP-05	100 dB	10 μV/V	94 dB	20 μV/V
OP-07A	100 dB	10 μV/V	94 dB	20 μV/V
OP-07	100 dB	10 μV/V	94 dB	20 μV/V
PM-725	100 dB	10 μV/V	94 dB	20 μV/V
OP-02A	90 dB	30 μV/V	84 dB	60 μV/V
OP-02	90 dB	30 μV/V	84 dB	60 μV/V

COMMERCIAL TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

DEVICE	T_A = 25°C MIN (dB)	T_A = 25°C MAX (μV/V)	OVER TEMPERATURE MIN (dB)	OVER TEMPERATURE MAX (μV/V)
SSS725E	106 dB	5.0 μV/V	103 dB	7.0 μV/V
SSS725C	100 dB	10 μV/V	96 dB	15 μV/V
OP-05E	94 dB	20 μV/V	90 dB	30 μV/V
OP-07E	94 dB	20 μV/V	90 dB	30 μV/V
OP-05C	90 dB	30 μV/V	86 dB	50 μV/V
OP-07C	90 dB	30 μV/V	86 dB	50 μV/V
OP-07D	90 dB	30 μV/V	86 dB	50 μV/V
OP-02E	90 dB	30 μV/V	84 dB	60 μV/V
OP-02C	90 dB	30 μV/V	84 dB	60 μV/V
PM-725C	89 dB	35 μV/V	N/S	N/S

MILITARY TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
SSS725A	120 dB	114 dB
SSS725	120 dB	110 dB
OP-05A	114 dB	110 dB
OP-05	114 dB	110 dB
OP-07A	110 dB	106 dB
OP-07	110 dB	106 dB
PM-725	110 dB	100 dB
OP-02A	90 dB	84 dB
OP-02	90 dB	84 dB

COMMERCIAL TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
SSS725E	120 dB	115 dB
OP-05E	110 dB	107 dB
PM-725C	110 dB	100 dB
OP-07E	106 dB	103 dB
OP-05C	100 dB	97 dB
OP-07C	100 dB	97 dB
SSS725C	100 dB	97 dB
OP-07D	94 dB	94 dB
PM-725C	94 dB	N/S
OP-02E	90 dB	84 dB
OP-02C	90 dB	84 dB

N/S — Not specified.

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
SSS725A	1000 V/mV	700 V/mV
SSS725	1000 V/mV	500 V/mV
PM-725	1000 V/mV	250 V/mV
OP-05A	300 V/mV	200 V/mV
OP-07A	300 V/mV	200 V/mV
OP-05	200 V/mV	150 V/mV
OP-07	200 V/mV	150 V/mV
OP-02A	100 V/mV	50 V/mV
OP-02	50 V/mV	25 V/mV

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
SSS725E	1000 V/mV	800 V/mV
SSS725C	500 V/mV	300 V/mV
PM-725C	250 V/mV	125 V/mV
OP-05E	200 V/mV	180 V/mV
OP-07E	200 V/mV	180 V/mV
OP-05C	120 V/mV	100 V/mV
OP-07C	120 V/mV	100 V/mV
OP-07D	120 V/mV	100 V/mV
OP-02E	100 V/mV	50 V/mV
OP-02C	50 V/mV	25 V/mV

SINGLE GENERAL PURPOSE OPERATIONAL AMPLIFIER SELECTION GUIDE

INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-02A	0.5 mV	1.0 mV
OP-01	0.7 mV	1.0 mV
OP-02	2.0 mV	3.0 mV
OP-01F	2.0 mV	3.0 mV
SSS741	2.0 mV	3.0 mV
OP-01G	5.0 mV	6.0 mV
SSS741G	5.0 mV	6.0 mV
PM-741	5.0 mV	6.0 mV

INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-02E	0.5 mV	1.0 mV
OP-01H	0.7 mV	1.0 mV
OP-02C	2.0 mV	3.0 mV
OP-01E	2.0 mV	3.0 mV
OP-01C	5.0 mV	6.0 mV
SSS741C	6.0 mV	7.5 mV

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-01	2.0 nA	4.0 nA
OP-02A	2.0 nA	5.0 nA
OP-01F	5.0 nA	10 nA
OP-02	5.0 nA	10 nA
SSS741	5.0 nA	10 nA
OP-01G	20 nA	40 nA
SSS741G	25 nA	50 nA
PM-741	200 nA	500 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-01H	2.0 nA	4.0 nA
OP-02E	2.0 nA	4.0 nA
OP-01E	5.0 nA	10 nA
OP-02C	5.0 nA	10 nA
OP-01C	20 nA	40 nA
SSS741C	25 nA	50 nA

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-02A	100 V/mV	50 V/mV
SSS741	100 V/mV	50 V/mV
OP-01	50 V/mV	30 V/mV
OP-02	50 V/mV	25 V/mV
OP-01F	50 V/mV	25 V/mV
SSS741G	50 V/mV	25 V/mV
PM-741	50 V/mV	25 V/mV
OP-01G	25 V/mV	15 V/mV

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-02E	100 V/mV	50 V/mV
OP-01H	50 V/mV	30 V/mV
OP-02C	50 V/mV	25 V/mV
OP-01E	50 V/mV	25 V/mV
OP-01C	25 V/mV	15 V/mV
SSS741C	25 V/mV	15 V/mV

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-01	30 nA	50 nA
OP-02A	30 nA	55 nA
OP-02	50 nA	100 nA
OP-01F	50 nA	100 nA
SSS741	50 nA	100 nA
OP-01G	100 nA	200 nA
SSS741G	100 nA	200 nA
PM-741	500 nA	1500 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-02E	30 nA	50 nA
OP-01H	30 nA	50 nA
OP-02C	50 nA	100 nA
OP-01E	50 nA	100 nA
OP-01C	100 nA	200 nA
SSS741C	100 nA	200 nA

MILITARY TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

	T_A = 25°C		OVER TEMPERATURE	
DEVICE	MIN (dB)	MAX (μV/V)	MIN (dB)	MAX (μV/V)
OP-01	90 dB	30 μV/V	90 dB	30 μV/V
OP-02A	90 dB	30 μV/V	84 dB	60 μV/V
OP-02	90 dB	30 μV/V	84 dB	60 μV/V
OP-01F	80 dB	100 μV/V	80 dB	100 μV/V
OP-01G	80 dB	100 μV/V	80 dB	100 μV/V
SSS741	80 dB	100 μV/V	80 dB	100 μV/V
SSS741G	76 dB	150 μV/V	76 dB	150 μV/V
PM-741	76 dB	150 μV/V	76 dB	150 μV/V

COMMERCIAL TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

	T_A = 25°C		OVER TEMPERATURE	
DEVICE	MIN (dB)	MAX (μV/V)	MIN (dB)	MAX (μV/V)
OP-01H	90 dB	30 μV/V	90 dB	30 μV/V
OP-02E	90 dB	30 μV/V	84 dB	60 μV/V
OP-02C	90 dB	30 μV/V	84 dB	60 μV/V
OP-01E	80 dB	100 μV/V	80 dB	100 μV/V
OP-01C	80 dB	100 μV/V	80 dB	100 μV/V
SSS741C	76 dB	150 μV/V	N/S	N/S

MILITARY TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-01	90 dB	90 dB
OP-02A	90 dB	84 dB
OP-02	90 dB	84 dB
OP-01F	80 dB	80 dB
OP-01G	80 dB	80 dB
SSS-741	80 dB	80 dB
SSS741G	70 dB	70 dB
PM-741	70 dB	70 dB

COMMERCIAL TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-01H	90 dB	90 dB
OP-02E	90 dB	84 dB
OP-02C	90 dB	84 dB
OP-01E	80 dB	80 dB
OP-01C	80 dB	80 dB
SSS741C	70 dB	N/S

DUAL PRECISION OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10A	0.50 mV	0.70 mV
OP-10	0.50 mV	0.70 mV
OP-04A	0.75 mV	1.5 mV
OP-14A	0.75 mV	1.5 mV
OP-04	2.0 mV	3.0 mV
OP-14	2.0 mV	3.0 mV

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10E	0.50 mV	0.60 mV
OP-04E	0.75 mV	1.5 mV
OP-14E	0.75 mV	1.5 mV
OP-10C	1.3 mV	1.6 mV
OP-04C	2.0 mV	3.0 mV
OP-14C	2.0 mV	3.0 mV

MILITARY TEMPERATURE RANGE

UNNULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})		NULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OSN})	
DEVICE	TCV_{os} MAX	DEVICE	TCV_{osn} MAX
OP-10A	2.0 µV/°C	OP-10A	1.0 µV/°C
OP-10	*2.0 µV/°C	OP-10	*1.0 µV/°C
OP-04A	*8.0 µV/°C		
OP-14A	*8.0 µV/°C		
OP-04	*10 µV/°C		
OP-14	*10 µV/°C		

*Parameter not 100% tested.
90% of all units meet these specifications.

COMMERCIAL TEMPERATURE RANGE

UNNULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})		NULLED INPUT OFFSET VOLTAGE DRIFT (TCV_{OSN})	
DEVICE	MAX OVER TEMPERATURE	DEVICE	MAX OVER TEMPERATURE
OP-10E	*2.0 µV/°C	OP-10E	*1.0 µV/°C
OP-10C	*4.5 µV/°C	OP-10C	*1.5 µV/°C
OP-04E	*8.0 µV/°C		
OP-14E	*8.0 µV/°C		
OP-04C	*10 µV/°C		
OP-14C	*10 µV/°C		

*Parameter not 100% tested. 90% of all units meet this specification.

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04A	2.0 nA	5.0 nA
OP-14A	2.0 nA	5.0 nA
OP-10A	2.8 nA	5.6 nA
OP-10	2.8 nA	5.6 nA
OP-04	5.0 nA	10 nA
OP-14	5.0 nA	10 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04E	2.0 nA	4.0 nA
OP-14E	2.0 nA	4.0 nA
OP-10E	3.8 nA	5.3 nA
OP-04C	5.0 nA	10 nA
OP-14C	5.0 nA	10 nA
OP-10C	6.0 nA	8.0 nA

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10A	3.0 nA	6.0 nA
OP-10	3.0 nA	6.0 nA
OP-04A	50.0 nA	100 nA
OP-14A	50.0 nA	100 nA
OP-04	75.0 nA	125 nA
OP-14	75.0 nA	125 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10E	4.0 nA	5.5 nA
OP-10C	7.0 nA	9.0 nA
OP-04E	50.0 nA	50 nA
OP-14E	50.0 nA	50 nA
OP-04C	75.0 nA	125 nA
OP-14C	75.0 nA	125 nA

DUAL PRECISION OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-10A	110 dB	106 dB
OP-10	110 dB	106 dB
OP-04A	90 dB	84 dB
OP-04	90 dB	84 dB
OP-14A	90 dB	84 dB
OP-14	90 dB	84 dB

COMMERCIAL TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-10E	106 dB	103 dB
OP-10C	100 dB	97 dB
OP-04E	90 dB	84 dB
OP-14E	90 dB	84 dB
OP-04C	90 dB	84 dB
OP-14C	90 dB	84 dB

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-10A	200 V/mV	150 V/mV
OP-10	200 V/mV	150 V/mV
OP-04A	100 V/mV	50 V/mV
OP-14A	100 V/mV	50 V/mV
OP-04	50 V/mV	25 V/mV
OP-14	50 V/mV	25 V/mV

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10E	200 V/mV	180 V/mV
OP-10C	120 V/mV	100 V/mV
OP-04E	100 V/mV	50 V/mV
OP-14E	100 V/mV	50 V/mV
OP-04C	50 V/mV	25 V/mV
OP-14C	50 V/mV	25 V/mV

MILITARY TEMPERATURE RANGE

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS})

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10A	0.18 mV	0.3 mV
OP-10	0.5 mV	0.9 mV
OP-04A	1.0 mV	1.5 mV
OP-14A	1.0 mV	1.5 mV
OP-04	2.0 mV	3.0 mV
OP-14	2.0 mV	3.0 mV

COMMERCIAL TEMPERATURE RANGE

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS})

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-10E	0.5 mV	0.70 mV
OP-04E	1.0 mV	1.5 mV
OP-14E	1.0 mV	1.5 mV
OP-04C	2.0 mV	3.0 mV
OP-14C	2.0 mV	3.0 mV
OP-10C	N/S	N/S

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; (V_{OSA}–V_{OSB}).

DUAL GENERAL PURPOSE OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04A	.75 mV	1.5 mV
OP-14A	.75 mV	1.5 mV
OP-04	2.0 mV	3.0 mV
OP-14	2.0 mV	3.0 mV
SSS747	2.0 mV	3.0 mV
SSS747G	5.0 mV	6.0 mV
SSS1558	5.0 mV	6.0 mV
PM-747	5.0 mV	6.0 mV
PM-1558	5.0 mV	6.0 mV

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04E	.75 mV	1.5 mV
OP-14E	.75 mV	1.5 mV
OP-04C	2.0 mV	3.0 mV
OP-14C	2.0 mV	3.0 mV
SSS747C	5.0 mV	6.0 mV
SSS1458	5.0 mV	6.0 mV

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04A	2.0 nA	5.0 nA
OP-14A	2.0 nA	5.0 nA
OP-04	5.0 nA	10 nA
OP-14	5.0 nA	10 nA
SSS747	5.0 nA	10 nA
SSS747G	25 nA	50 nA
SSS1558	25 nA	50 nA
PM-747	200 nA	500 nA
PM-1558	200 nA	500 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04E	2.0 nA	4.0 nA
OP-14E	2.0 nA	4.0 nA
OP-04C	5.0 nA	10 nA
OP-14C	5.0 nA	10 nA
SSS747C	25 nA	50 nA
SSS1458	25 nA	50 nA

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-04A	100 V/mV	50 V/mV
OP-14A	100 V/mV	50 V/mV
SSS747	100 V/mV	50 V/mV
OP-04	50 V/mV	25 V/mV
OP-14	50 V/mV	25 V/mV
SSS747G	50 V/mV	25 V/mV
SSS1558	50 V/mV	25 V/mV
PM-747	50 V/mV	25 V/mV
PM-1558	50 V/mV	25 V/mV

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-04E	100 V/mV	50 V/mV
OP-14E	100 V/mV	50 V/mV
OP-04C	50 V/mV	25 V/mV
OP-14C	50 V/mV	25 V/mV
SSS1458	50 V/mV	25 V/mV
SSS747C	50 V/mV	25 V/mV

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04A	50 nA	100 nA
OP-14A	50 nA	100 nA
SSS747	50 nA	100 nA
OP-04	75 nA	125 nA
OP-14	75 nA	125 nA
SSS747G	100 nA	200 nA
SSS1558	100 nA	200 nA
PM-747	500 nA	1500 nA
PM-1558	500 nA	1500 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-04E	50 nA	50 nA
OP-14E	50 nA	50 nA
OP-04C	75 nA	125 nA
OP-14C	75 nA	125 nA
SSS747C	100 nA	200 nA
SSS1458	100 nA	200 nA

MILITARY TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

DEVICE	T_A = 25°C MIN (dB)	MAX (μV/V)	OVER TEMPERATURE MIN (dB)	MAX (μV/V)
OP-04A	90 dB	30 μV/V	84 dB	60 μV/V
OP-14A	90 dB	30 μV/V	84 dB	60 μV/V
OP-04	90 dB	30 μV/V	84 dB	60 μV/V
OP-14	90 dB	30 μV/V	84 dB	60 μV/V
SSS747	80 dB	100 μV/V	80 dB	100 μV/V
SSS747G	76 dB	150 μV/V	76 dB	150 μV/V
SSS1558	76 dB	150 μV/V	76 dB	150 μV/V
PM-747	76 dB	150 μV/V	76 dB	150 μV/V
PM-1558	76 dB	150 μV/V	N/S	N/S

COMMERCIAL TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

DEVICE	T_A = 25°C MIN (dB)	MAX (μV/V)	OVER TEMPERATURE MIN (dB)	MAX (μV/V)
OP-04E	90 dB	30 μV/V	84 dB	60 μV/V
OP-14E	90 dB	30 μV/V	84 dB	60 μV/V
OP-04C	90 dB	30 μV/V	84 dB	60 μV/V
OP-14C	90 dB	30 μV/V	84 dB	60 μV/V
SSS747C	76 dB	150 μV/V	76 dB	150 μV/V
SSS1458	76 dB	150 μV/V	76 dB	150 μV/V

MILITARY TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-04A	90 dB	84 dB
OP-14A	90 dB	84 dB
OP-04	90 dB	84 dB
OP-14	90 dB	84 dB
SSS747	80 dB	80 dB
SSS747G	70 dB	70 dB
SSS1558	70 dB	70 dB
PM-747	70 dB	70 dB
PM-1558	70 dB	N/S

N/S — Not specified.

COMMERCIAL TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-04E	90 dB	84 dB
OP-14E	90 dB	84 dB
OP-04C	90 dB	84 dB
OP-14C	90 dB	84 dB
SSS747C	70 dB	70 dB
SSS1458	70 dB	70 dB

QUAD OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-09A	90 dB	90 dB
OP-11A	90 dB	90 dB
OP-09B	90 dB	90 dB
OP-11B	90 dB	90 dB
PM-4136	76 dB	N/S

N/S — Not specified.

COMMERCIAL TEMPERATURE RANGE
POWER SUPPLY REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-09E	90 dB	90 dB
OP-11E	90 dB	90 dB
OP-09F	90 dB	90 dB
OP-09F	90 dB	90 dB
PM-4136C	70 dB	N/S

N/S — Not specified.

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE MATCH (ΔV_{OS})

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09A	0.75 mV	1.0 mV
OP-11A	0.75 mV	1.0 mV
OP-09B	2.0 mV	2.5 mV
OP-11B	2.0 mV	2.5 mV

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA}-V_{OSB}$). Example: Using amplifier A as reference then $\Delta V_{OS} = V_{OSN}-V_{OSA}$.

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE MATCH (ΔV_{OS})

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09E	0.75 mV	1.0 mV
OP-11E	0.75 mV	1.0 mV
OP-09F	2.0 mV	2.5 mV
OP-11F	2.0 mV	2.5 mV

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA}-V_{OSB}$). Example: Using amplifier A as reference then $\Delta V_{OS} = V_{OSN}-V_{OSA}$.

MILITARY TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-09A	100 dB	100 dB
OP-11A	100 dB	100 dB
OP-09B	100 dB	100 dB
OP-11B	100 dB	100 dB
PM-4136	70 dB	N/S

N/S — Not specified.

COMMERCIAL TEMPERATURE RANGE
COMMON MODE REJECTION RATIO

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-09E	100 dB	100 dB
OP-11E	100 dB	100 dB
OP-09F	100 dB	100 dB
OP-11F	100 dB	100 dB
PM-4136C	70 dB	N/S

N/S — Not specified.

MILITARY TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-09A	100 V/mV	100 V/mV
OP-11A	100 V/mV	100 V/mV
OP-09B	100 V/mV	100 V/mV
OP-11B	100 V/mV	100 V/mV
PM-4136	50 V/mV	25 V/mV

COMMERCIAL TEMPERATURE RANGE
OPEN LOOP GAIN

DEVICE	MIN, T_A = 25°C	MIN OVER TEMPERATURE
OP-09E	100 V/mV	100 V/mV
OP-11E	100 V/mV	100 V/mV
OP-09F	100 V/mV	100 V/mV
OP-11F	100 V/mV	100 V/mV
PM-4136C	20 V/mV	15 V/mV

QUAD OPERATIONAL AMPLIFIER SELECTION GUIDE

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09A	0.5 mV	1.0 mV
OP-11A	0.5 mV	1.0 mV
OP-09B	2.5 mV	3.5 mV
OP-11B	2.5 mV	3.5 mV
PM-4136	5.0 mV	6.0 mV

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09E	0.5 mV	0.8 mV
OP-11E	0.5 mV	0.8 mV
OP-09F	2.5 mV	3.0 mV
OP-11F	2.5 mV	3.0 mV
PM-4136C	6.0 mV	7.5 mV

MILITARY TEMPERATURE RANGE
INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})

DEVICE	TCV_{OS} MAX
OP-09A	*10 µV/°C
OP-11A	*10 µV/°C
OP-09B	*15 µV/°C
OP-11B	*15 µV/°C

*Parameter is not 100% tested. 90% of all units meet these specifications

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET VOLTAGE DRIFT (TCV_{OS})

DEVICE	MAX, T_A = 25°C
OP-09E	*10 µV/°C
OP-11E	*10 µV/°C
OP-09F	*15 µV/°C
OP-11F	*15 µV/°C

*Parameter not 100% tested. 90% of all units meet these specifications

MILITARY TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09A	20 nA	40 nA
OP-11A	20 nA	40 nA
OP-09B	50 nA	80 nA
OP-11B	50 nA	80 nA
PM-4136	200 nA	500 nA

COMMERCIAL TEMPERATURE RANGE
INPUT OFFSET CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09E	20 nA	30 nA
OP-11E	20 nA	30 nA
OP-09F	50 nA	60 nA
OP-09F	50 nA	60 nA
PM-4136C	200 nA	300 nA

MILITARY TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09A	300 nA	375 nA
OP-11A	300 nA	375 nA
OP-09B	500 nA	650 nA
OP-11B	500 nA	650 nA
PM-4136	500 nA	1500 nA

COMMERCIAL TEMPERATURE RANGE
INPUT BIAS CURRENT

DEVICE	MAX, T_A = 25°C	MAX OVER TEMPERATURE
OP-09E	300 nA	350 nA
OP-11E	300 nA	350 nA
OP-09F	500 nA	550 nA
OP-11F	500 nA	550 nA
PM-4136C	500 nA	800 nA

OP-01

INVERTING HIGH SPEED OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-01 Series of monolithic High Speed Operational Amplifiers combines high slew rate, fast settling time output performance with excellent D.C. input characteristics.

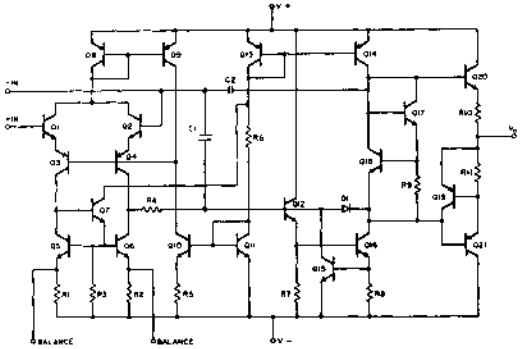
An internal feed-forward frequency compensation network provides simplicity of application—no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice in input bias current or power consumption. 250kHz power bandwidth is attained with a small signal bandwidth of 2.5 MHz, allowing non-critical board layout. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10kΩ potentiometer.

The low offset voltage, input bias current and offset voltage drift vs. temperature provide accurate D.C. performance in applications such as channel preamplifiers, fast integrators and precision summing amplifiers. The fast output response makes the OP-01 ideal in state-variable filters, servo drivers, waveform generators, analog computing amplifiers, and D/A converter output amplifiers.

FEATURES

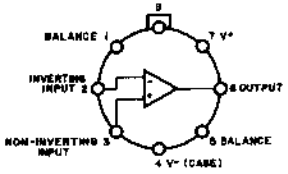
- Fast Settling Time . . . . . 1 μsec to 0.1%
- High Slew Rate . . . . . 18 V/μsec
- Power Bandwidth. . . . . 250 kHz
- Low Power Consumption . . . . . 90 mW Max
- Excellent D.C. Specifications
- Internally Compensated
- Ideal DAC Output Amplifier
- MIL-STD-883 Processing Available
- Fits Standard 741 Sockets
- Low Cost

SIMPLIFIED SCHEMATIC

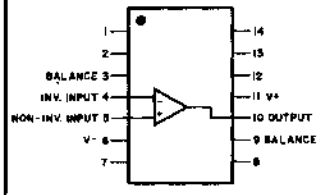


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW

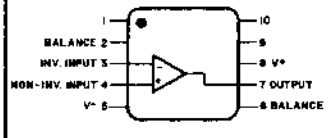


TO-99 (J-Suffix)
ORDER: OP-01J
OP-01FJ
OP-01GJ
OP-01HJ
OP-01EJ
OP-01CJ



14 PIN DIP (Y-Suffix)*
ORDER: OP-01Y
OP-01FY
OP-01GY
OP-01HY
OP-01EY
OP-01CY

*Formerly "P" Suffix



10 PIN FLATPACK (L-Suffix)
ORDER: OP-01L
OP-01FL
OP-01GL

ABSOLUTE MAXIMUM RATINGS

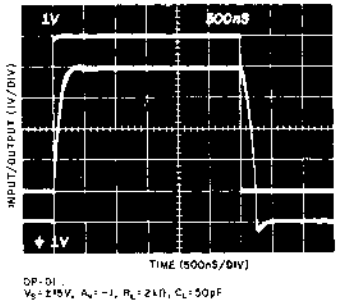
Total Supply Voltage		Short Circuit Duration	Indefinite
OP-01, OP-01F, OP-01E, OP-01H	±22V	Operating Temperature Range	
OP-01G, OP-01C	±20V	OP-01, OP-01F, OP-01G	−55°C to +125°C
Power Dissipation (see note)	500mW	OP-01H, OP-01E, OP-01C	0°C to +70°C
Differential Input Voltage	±30V	Storage Temperature Range	−65°C to +150°C
Input Voltage	±15V	Lead Temperature (Soldering, 60 Sec)	300°C

NOTE: Maximum Package Power Dissipation vs. ambient temperature

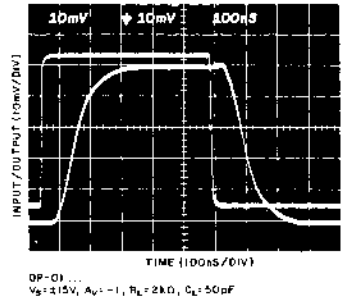
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (P, Y)	100°C	10.0mW/°C
Flat Pack (L)	62°C	5.7mW/°C

TYPICAL PERFORMANCE CURVES

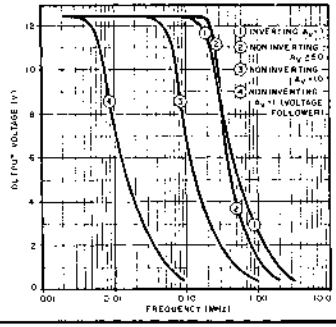
LARGE SIGNAL PULSE RESPONSE



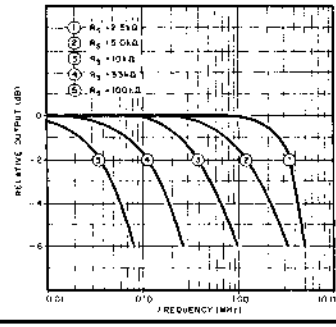
SMALL SIGNAL PULSE RESPONSE



LARGE SIGNAL OUTPUT SWING VS. FREQUENCY



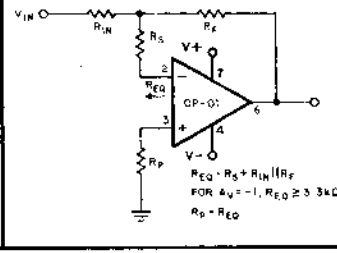
UNITY GAIN-BANDWIDTH VS. SOURCE RESISTANCE



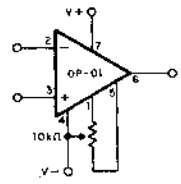
APPLICATIONS INFORMATION

The OP-1 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high gain non-inverting applications. Unity gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal, and proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent inverting terminal resistance is defined as $R_{IN} \| R_F$. A total equivalent input terminal resistance ≈3.3kΩ will assure stability in all closed loop gain configurations including unity gain. Should $R_{IN} \| R_F \approx 3.3k\Omega$, a resistor ($R_S$) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast Inverting Amplifier Diagram.) Lower values of total equivalent resistance may be used to improve bandwidth in higher closed loop gain configurations, as indicated by the Open Loop Gain vs. Frequency plot.

FAST INVERTER CIRCUIT

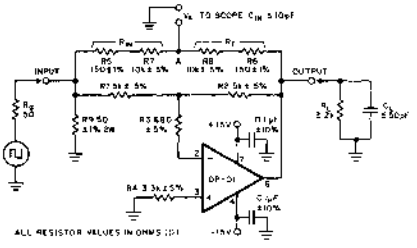


OFFSET NULLING CIRCUIT



ELECTRICAL CHARACTERISTICS			OP-01 OP-01H			OP-01F OP-01E			OP-01G OP-01C			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.3	0.7	–	1.0	2.0	–	2.0	5.0	mV
Input Offset Current	I_{OS}		–	0.5	2.0	–	1.0	5.0	–	2.0	20	nA
Input Bias Current	I_B		–	18	30	–	20	50	–	25	100	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O$=±10V	50	100	–	50	100	–	25	75	–	V/mV
Power Consumption	P_D	V_{OUT} = 0	–	40	60	–	50	90	–	50	90	mW
Settling Time to 0.1% (Summing Node Error)		A_V = –1 (Note) V_{IN} = 5V	–	0.7	1.0	–	0.7	1.0	–	0.7	1.0	µsec
Slew Rate			–	18	–	–	18	–	–	18	–	V/µs
Large Signal Bandwidth			–	250	–	–	250	–	–	250	–	kHz
Small Signal Bandwidth			–	2.5	–	–	2.5	–	–	2.5	–	MHz
Risetime (Note)		A_V = –1 V_{IN}=50mV	–	150	–	–	150	–	–	150	–	nsec
Overshoot (Note)			–	2	–	–	2	–	–	2	–	%
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C for OP-01, OP-01F, OP-01G and 0°C ≤ T_A ≤ +70°C for OP-01H, OP-01E, OP-01C, unless otherwise specified.												
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.4	1.0	–	1.5	3.0	–	3.0	6.0	mV
Input Offset Current	I_{OS}		–	1.0	4.0	–	2.0	10	–	4.0	40	nA
Input Bias Current	I_B		–	30	50	–	40	100	–	50	200	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM}=±CMVR $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S=± 5V to ±20V $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O$=±10V	30	60	–	25	60	–	15	50	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	V V
Offset Voltage Drift	TCV_{OS}	$R_S \leq 5k\Omega$	–	2.0	8.0	–	3.0	10.0	–	5.0	20.0	µV/°C
NOTE: R_L = 2kΩ, C_L = 50pF. See Settling Time Test Circuit.												

SETTLING TIME TEST CIRCUIT



Settling time may be measured using the circuit shown; this circuit incorporates the "false sum node" technique to produce more accurate, repeatable results. For a 5 volt input step, 0.1% settling will be achieved when the false sum node settles to within +2.5mV of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe (≤10pF, including stray). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in ≤20 ns with ringing less than 2.5mV after 0.5µs. 0.1% measurements require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.

OP-02

HIGH PERFORMANCE GENERAL PURPOSE OPERATIONAL AMPLIFIER

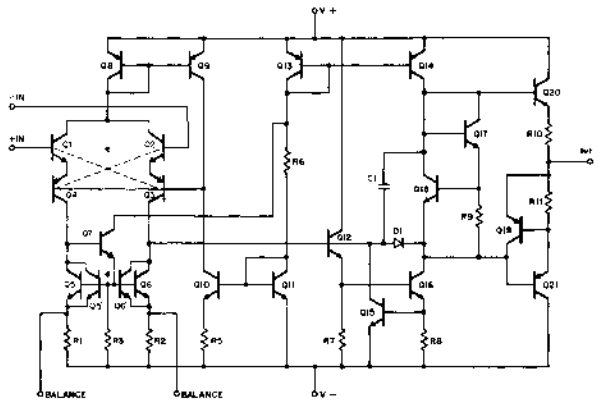
GENERAL DESCRIPTION

The OP-02 Series of High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-02 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. OP-02's with MIL-STD-883 processing are available. For dual high performance matched general purpose operational amplifiers, refer to the OP-04 and OP-14 data sheets.

FEATURES

- Excellent D.C. Input Specifications
- Fits Standard 741 Socket
- Internally Compensated
- Low Noise . . . . . 0.65 µVp-p Typ
- Low Drift (TCV_{OS}) . . . . . 8 µV/°C Max
- "Premium" 741 Replacement
- 0°C/+70°C and –55°C/+125°C Models
- MIL-STD-883 Processing Available
- Silicon-Nitride Passivation
- Low Cost

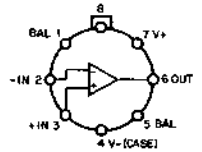
SIMPLIFIED SCHEMATIC



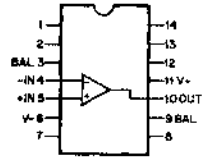
*Q1, Q2, Q3 & Q4 FORM A THERMALLY CROSS-COUPLED TRANSISTOR QUAD. Q5, Q6, Q8 & Q9 COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

PIN CONNECTIONS AND ORDERING INFORMATION

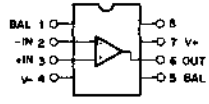
TOP VIEW



TO-99 (J-Suffix)
ORDER:
OP-02AJ
OP-02J
OP-02EJ
OP-02CJ



14 PIN HERMETIC DIP (Y-Suffix)
ORDER:
OP-02AY
OP-02Y
OP-02EY
OP-02CY



EPOXY B MINI-DIP (P-Suffix)
ORDER:
OP-02CP

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

ORDER: OP02-883-AJ
OP02-883-AY
OP02-883-J
OP02-883-Y

ABSOLUTE MAXIMUM RATINGS

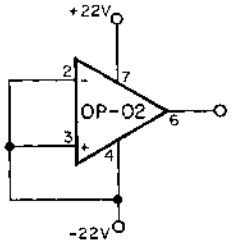
Supply Voltage	±22V	Operating Temperature Range	
Power Dissipation (see note)	500mW	OP-02A, OP-02	−55°C to +125°C
Differential Input Voltage	±30V	OP-02E, OP-02C	0°C to +70°C
Input Voltage	Supply Voltage	Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Indefinite	Lead Temperature (Soldering, 60 Sec)	300°C

NOTE: Maximum Package Power Dissipation vs. ambient temperature.

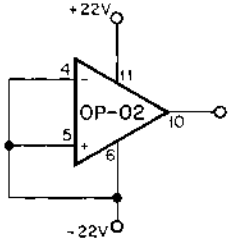
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (Y)	100°C	10.0mW/°C

BURN-IN CIRCUITS

TO-99 (J) PACKAGE
MINI-DIP (P) PACKAGE

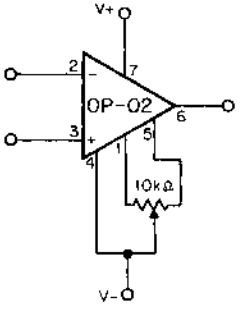


DIP (Y) PACKAGE

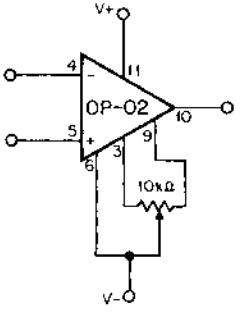


OFFSET NULLING CIRCUITS

TO-99 (J) PACKAGE
MINI-DIP (P) PACKAGE



DIP (Y) PACKAGE



OP-02 DEFINITIONS

INPUT OFFSET VOLTAGE (V_{os})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT OFFSET CURRENT (I_{os})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

MAXIMUM OUTPUT VOLTAGE SWING (V_{om})
The peak output voltage that can be obtained without clipping.

LARGE SIGNAL VOLTAGE GAIN (A_{vo})
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{os})
The ratio of the change in the offset voltage to the change in temperature producing it.

AVERAGE OFFSET CURRENT DRIFT (TCI_{os})
The ratio of the change in the offset current to the change in temperature producing it.

POWER DISSIPATION (P_d)
The total power dissipated in the amplifier with the output at zero volts and no load.

UNITY GAIN CLOSED LOOP BANDWIDTH (BW)
The frequency at which the magnitude of the small signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

INPUT NOISE VOLTAGE (e_{np-p})
The peak to peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage in a 1 Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak to peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1 Hz band surrounding a specified value of frequency.

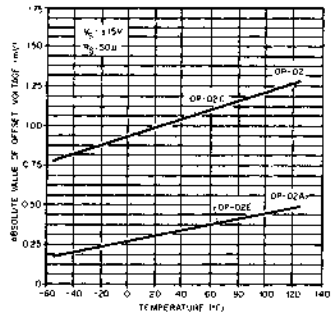
ELECTRICAL CHARACTERISTICS			OP-02A			OP-02			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.5	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	30	–	20	50	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_O = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz		0.65	–	–	0.65	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	–	25 22 21	–	–	25 22 21	–	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	–	1.4 0.7 0.4	–	–	1.4 0.7 0.4	–	$pA/\sqrt{Hz}$
Slew Rate (Note 1)	SR		0.25	0.5	–	0.25	0.5	–	V/µs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV		200	300		200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.5	1.0	–	1.4	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	µV/°C
Input Offset Current	I_{os}		–	1.0	5.0		2.0	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	75	–	15	150	pA/°C
Input Bias Current	I_B		–	30	55	–	40	100	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	50	100	–	25	60	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V

Note 1. Parameter is not 100% tested. 90% of all units meet these specifications.

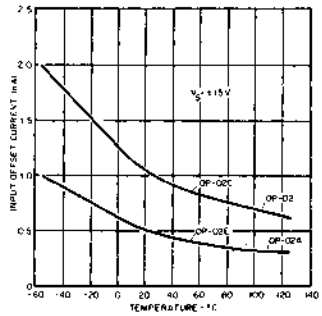
ELECTRICAL CHARACTERISTICS			OP-02E			OP-02C			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.5	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	30	–	20	50	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_O = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.25	0.5	–	0.25	0.5	–	V/μs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.4	1.0	–	1.2	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	μV/°C
Input Offset Current	I_{os}		–	0.7	4.0	–	1.4	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	120	–	15	250	pA/°C
Input Bias Current	I_B		–	22	50	–	25	100	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	50	200	–	25	150	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

TYPICAL PERFORMANCE CURVES

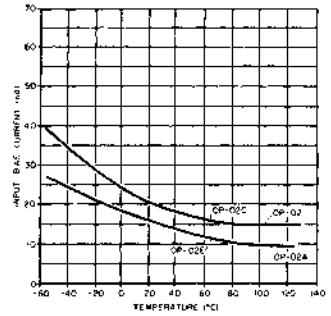
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



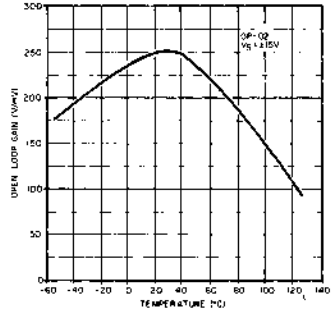
INPUT OFFSET CURRENT VS TEMPERATURE



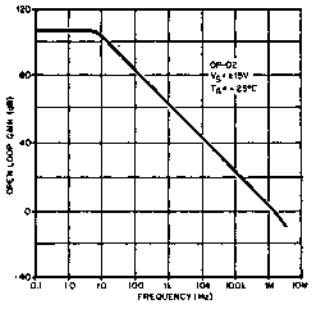
INPUT BIAS CURRENT VS TEMPERATURE



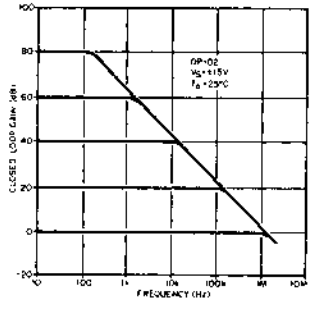
OPEN LOOP GAIN VS TEMPERATURE



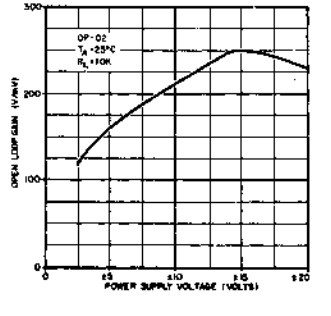
OPEN LOOP FREQUENCY RESPONSE



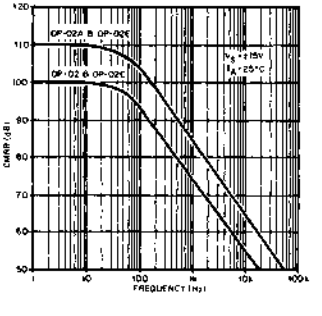
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



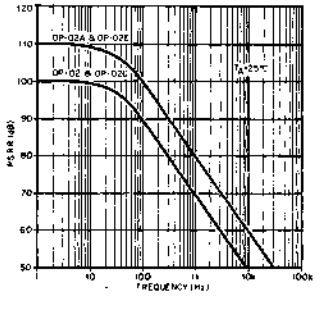
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



CMRR VS FREQUENCY

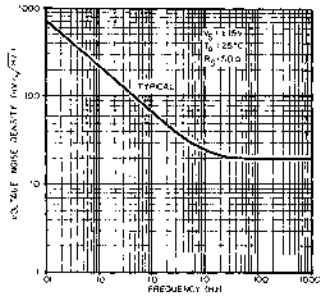


PSRR VS FREQUENCY

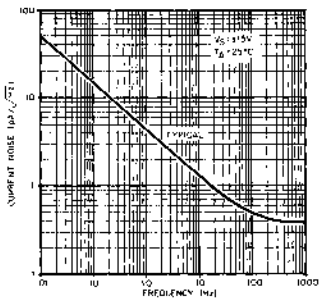


TYPICAL PERFORMANCE CURVES

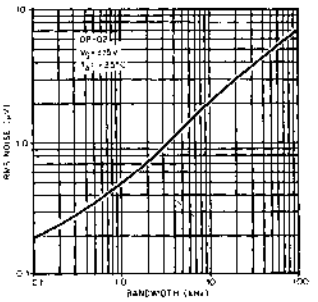
INPUT SPOT NOISE VOLTAGE VS FREQUENCY



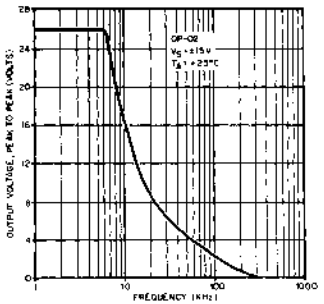
INPUT SPOT NOISE CURRENT VS FREQUENCY



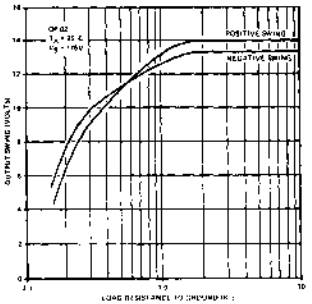
INPUT WIDEBAND NOISE VS BANDWIDTH (.1 Hz TO FREQUENCY INDICATED)



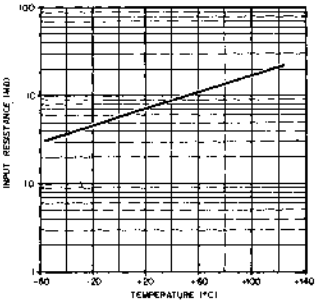
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



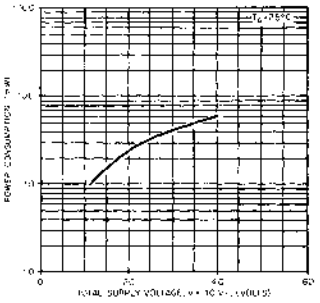
OUTPUT VOLTAGE VS LOAD RESISTANCE



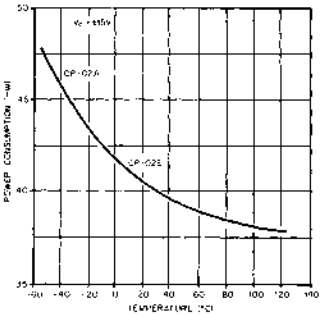
INPUT RESISTANCE VS TEMPERATURE



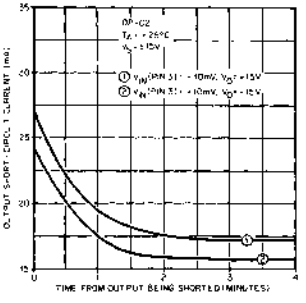
POWER CONSUMPTION VS POWER SUPPLY



POWER CONSUMPTION VS TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT VS TIME



OP-04

DUAL MATCHED HIGH PERFORMANCE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

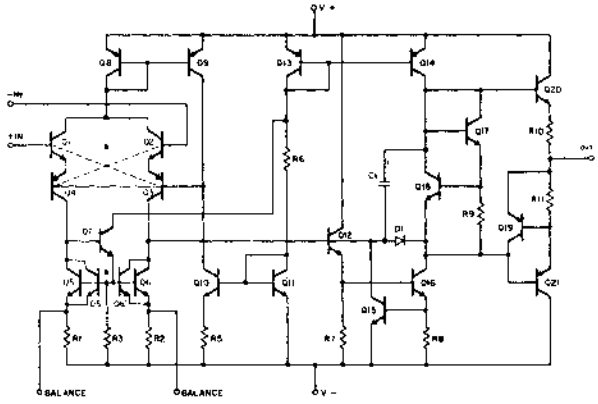
The OP-04 Series of Dual Matched High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard 747 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-04 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. For more stringent requirements, refer to the OP-10 Dual Matched Instrumentation Operational Amplifier data sheet.

FEATURES

- **Excellent D.C. Input Specifications**
- **Matched V_{OS} and CMRR**
- **Fits Standard 747 Socket**
- **Internally Compensated**
- **Low Noise**
- **Low Drift**
- **Low Cost**
- **0°C/+70°C and −55°C/+125°C Models**
- **Silicon-Nitride Passivation**
- **Models With MIL-STD-883A Class B Processing Available From Stock**

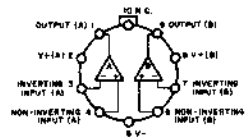
SIMPLIFIED SCHEMATIC

(1/2 OF CIRCUIT SHOWN)



PIN CONNECTIONS AND ORDERING INFORMATION

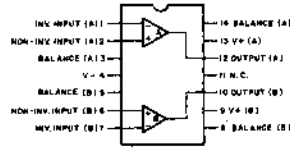
TOP VIEW



TO-100 (K-Suffix)

ORDER: OP-04AK
OP-04K
OP-04EK
OP-04CK

14 PIN HERMETIC DIP (Y-Suffix)



ORDER: OP-04AY
OP-04Y
OP-04EY
OP-04CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: OP04-883-AK
OP04-883-K
OP04-883-AY
OP04-883-Y

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	− 5° to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

OP-04A, OP-04	−55°C to +125°C
OP-04E, OP-04C	0°C to +70°C

Note 1: Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
DUAL-IN-LINE (Y)	100°C	10.0mW/°C
TO-100 (K)	80°C	7.1mW/°C

MATCHING CHARACTERISTICS

	OP-04A OP-04E					OP-04 OP-04C			

These specifications apply for V_S = ±15V, T_A = 25°C, $R_S \leq 100\Omega$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage Match	ΔV_{OS}			0.3	1.0	–	1.0	2.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± CMVR	94	106	–	94	106	–	dB
These specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C for OP-04A and OP-04, 0°C ≤ T_A ≤ 70°C for OP-04E and OP-04C, $R_S \leq 100\Omega$, unless otherwise noted.									
Input Offset Voltage Match	ΔV_{OS}		–	0.5	1.5	–	1.5	3.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± CMVR	90	100	–	90	100	–	dB

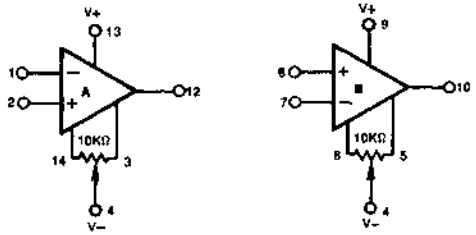
MATCHING PARAMETER DEFINITIONS

COMMON MODE REJECTION RATIO MATCH (ΔCMRR)
The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B.
ΔCMRR in dB = 20 $\log_{10}$ (ΔCMRR in volt/volt).

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$).

OFFSET NULLING CIRCUITS

DIP (Y) PACKAGE ONLY



OP-04 DEFINITIONS

INPUT OFFSET VOLTAGE (V_{OS})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT OFFSET CURRENT (I_{OS})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

MAXIMUM OUTPUT VOLTAGE SWING (V_{om})
The peak output voltage that can be obtained without clipping.

LARGE SIGNAL VOLTAGE GAIN (A_{vo})
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

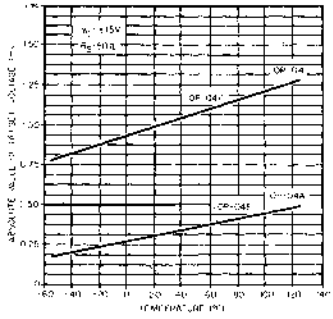
ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-04A			OP-04			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.75	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	50	–	20	75	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_O = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz		0.65	–	–	0.65	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Channel Separation	CS		100	–	–	100	–	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.5	0.5	–	0.5	0.7	–	V/µs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.5	1.5	–	1.4	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	µV/°C
Input Offset Current	I_{os}		–	1.0	5.0	–	2.0	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	75	–	15	150	pA/°C
Input Bias Current	I_B		–	30	100	–	40	125	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	50	100	–	25	60	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V

Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.

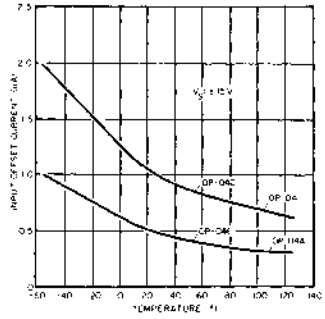
ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-04E			OP-04C			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.75	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	50	–	20	75	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110		90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250		50	200	–	V/mV
Power Consumption	P_d	V_O = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz		0.65		–	0.65		µV p-p
Input Noise Voltage Density	e_n	f_O 10Hz f_O = 100Hz f_O = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Channel Separation	CS		100	–	–	100	–	–	dB
Input Noise Current Density	i_n	f_O 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.5	0.7	–	0.5	0.7	–	V/µs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.4	1.5	–	1.2	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	µV/°C
Input Offset Current	I_{os}		–	0.7	4.0	–	1.4	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	120	–	15	250	pA/°C
Input Bias Current	I_B		–	22	50	–	25	125	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	50	200	–	25	150	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

TYPICAL PERFORMANCE CURVES (Each Amplifier)

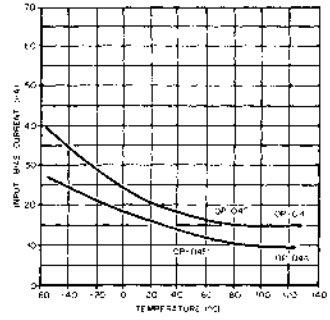
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



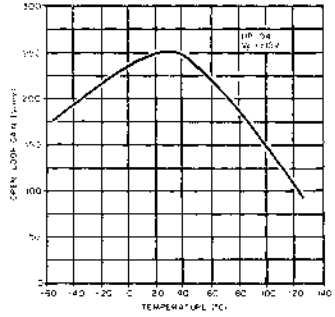
INPUT OFFSET CURRENT VS TEMPERATURE



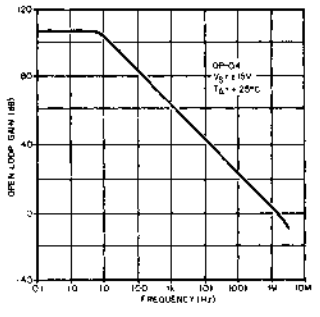
INPUT BIAS CURRENT VS TEMPERATURE



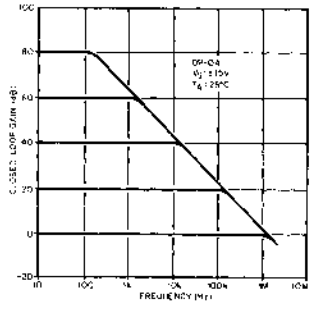
OPEN LOOP GAIN VS TEMPERATURE



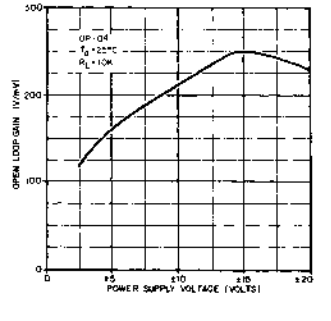
OPEN LOOP FREQUENCY RESPONSE



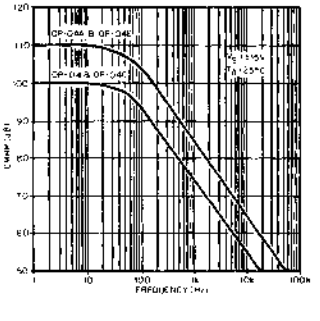
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



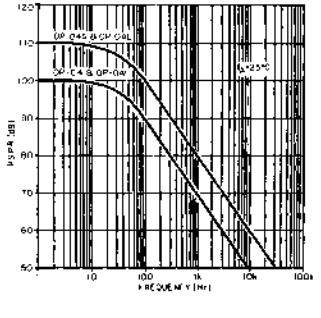
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



CMRR VS FREQUENCY

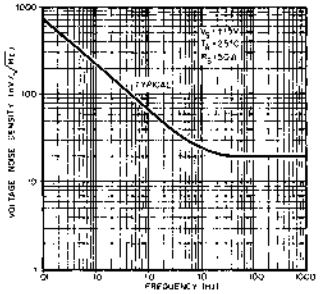


PSRR VS FREQUENCY

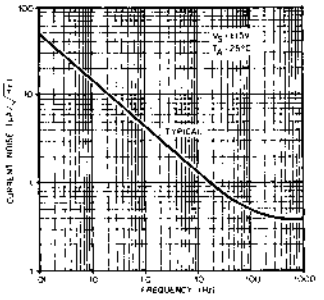


TYPICAL PERFORMANCE CURVES (Each Amplifier)

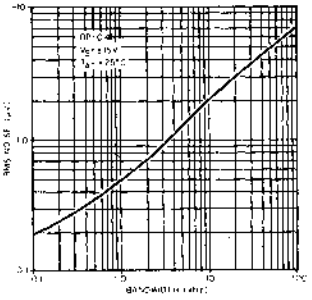
INPUT SPOT NOISE VOLTAGE VS FREQUENCY



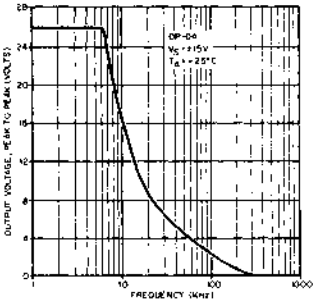
INPUT SPOT NOISE CURRENT VS FREQUENCY



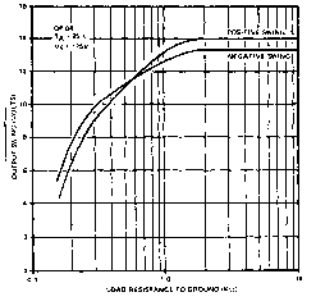
INPUT WIDEBAND NOISE VS BANDWIDTH (.1 Hz TO FREQUENCY INDICATED)



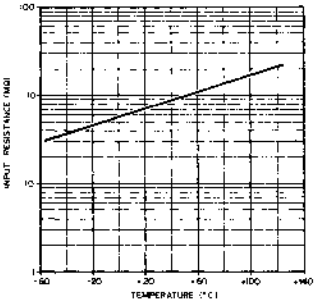
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



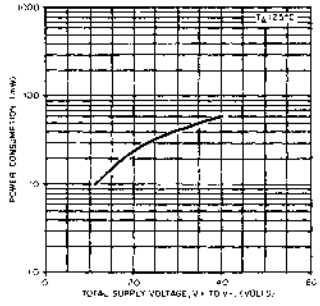
OUTPUT VOLTAGE VS LOAD RESISTANCE



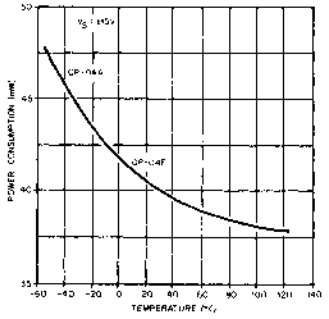
INPUT RESISTANCE VS TEMPERATURE



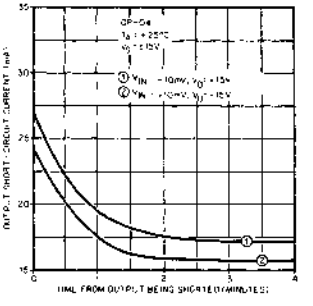
POWER CONSUMPTION VS POWER SUPPLY



POWER CONSUMPTION VS TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT VS TIME



OP-05

INSTRUMENTATION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-05 Series of monolithic Instrumentation Operational Amplifiers combines superlative performance in low signal level applications with the flexibility and ease of application of a fully protected, internally compensated op amp. OP-05 characteristics include low offset voltage and bias current and high gain, input impedance, CMRR and PSRR.

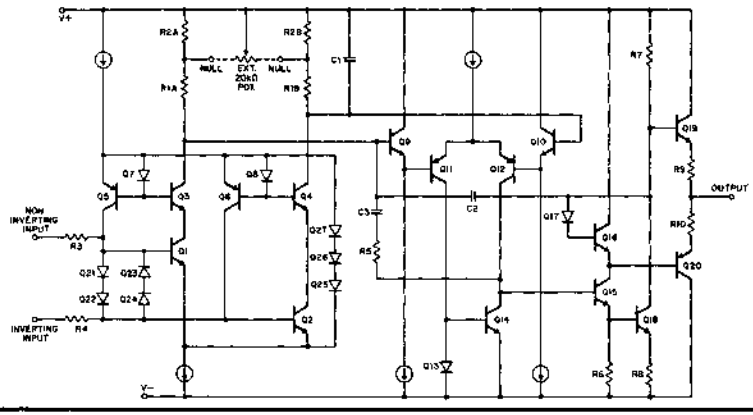
The OP-05 is a direct replacement in 725, 108A and unnulled 741 sockets allowing instant system performance improvement without redesign.

The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high gain active filters, buffers, integrators, and sample and hold amplifiers. For dual matched versions, refer to the OP-10 data sheet.

FEATURES

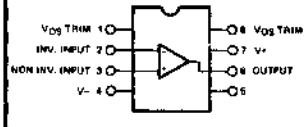
- Low Noise . . . . . 0.6μV p-p Max., 0.1 to 10Hz
- Low Drift vs. Temp . . . . . 0.5μV/°C Max
- Low Drift vs. Time . . . . . 0.3μV/Month Typ
- Low Bias Current . . . . . 2.0nA Max
- Low V_{OS} . . . . . 0.15mV Max
- High CMRR . . . . . 114dB Min
- High PSRR . . . . . 100dB Min
- High Gain . . . . . 300,000 Min
- High R_{in} Diff . . . . . 30MΩ Min
- High R_{in} CM . . . . . 200GΩ Typ
- High Slew Rate . . . . . 0.17 V/μsec Typ
- Internally Compensated . . . . . Stable to 500pF Load
- Easy to Use . . . . . Fully Protected
- Easy Offset Nulling . . . . . Single 20kΩ Pot
- Fits 725, 108A and 741 Sockets

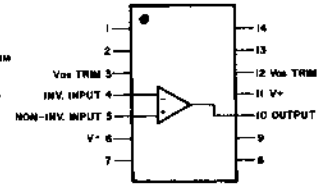
SIMPLIFIED SCHEMATIC

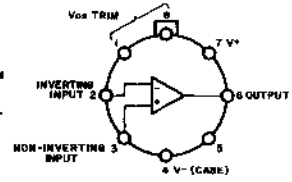


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW







Military Temperature Range Devices With MIL-STD-883A Class B Processing:

ORDER: OP05-883-AJ
OP05-883-AY
OP05-883-J
OP05-883-Y

EPOXY 8 MINI-DIP (P-Suffix)
ORDER: OP-05CP

14 PIN DIP (Y-Suffix)
ORDER: OP-05AY OP-05EY
OP-05Y OP-05CY

TO-99 (J-Suffix)
ORDER: OP-05AJ OP-05EJ
OP-05J OP-05CJ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation (Note 1)	500mW	Operating Temperature Range	
Differential Input Voltage	±30V	OP-05A, OP-05	−55°C to +125°C
Input Voltage (Note 2)	±22V	OP-05E, OP-05C	0°C to +70°C
Output Short Circuit Duration	Indefinite	Lead Temperature Range (Soldering, 60 sec)	300°C

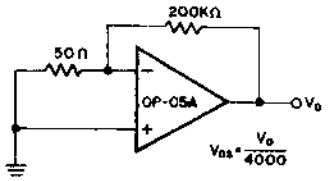
NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

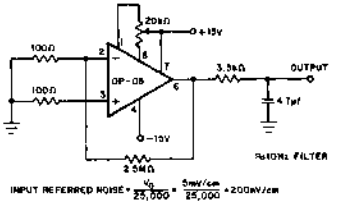
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (Y)	100°C	10.0mW/°C
Flat Pack (L)	62°C	5.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

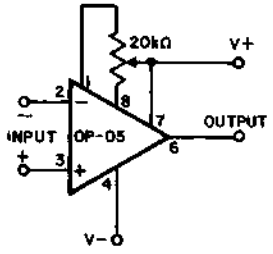
OFFSET VOLTAGE TEST CIRCUIT



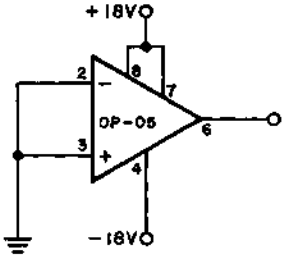
LOW FREQUENCY NOISE TEST CIRCUIT



OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

OP-05 Series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, OP-05 may be fitted to unnulled 741 Series sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

ELECTRICAL CHARACTERISTICS			OP-05A			OP-05			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.2	0.5	mV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 1)	—	0.2	1.0	—	0.2	1.0	µV/Mo
Input Offset Current	I_{OS}		—	.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f_O = 100Hz (Note 2)	—	10.0	13.0	—	10.0	13.0	
		f_O = 1000Hz (Note 2)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz (Note 2)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		fo = 100Hz (Note 2)	—	0.14	0.23	—	0.14	0.23	
		fo = 1000Hz (Note 2)	—	0.12	0.17	—	0.12	0.17	
Input Resistance - Differential Mode	R_{in}		30	80	—	20	60	—	MΩ
Input Resistance - Common Mode	R_{inCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	CMVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	110	—	100	110	—	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	300	500	—	200	600	—	V/mV
		$R_L \geq 500\Omega$, V_O = ±.5V, V_S = ±3V	150	500	—	150	500	—	
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	Ω
Power Consumption	Pd		—	90	120	—	90	120	mW
		V_S = ±3V	—	4	6	—	4	6	
Offset Adjustment Range		R_p = 20kΩ	—	4	—	—	4	—	mV
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{OS}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}		—	0.3	0.9	—	0.7	2.0	µV/°C
With External Trim	TCV_{OSn}	R_p = 20kΩ	—	0.2	0.5	—	0.3	1.0	µV/°C
Input Offset Current	I_{OS}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}		—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		—	8	25	—	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	106	—	94	106	—	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	200	400	—	150	400	—	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

NOTE 1: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV. Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Parameter is not 100% tested; 90% of units meet this specification.

ELECTRICAL CHARACTERISTICS			OP-05E			OP-05C			
These specifications apply for V_s = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}		--	0.2	0.5	--	0.3	1.3	mV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 1)	--	0.3	1.5	--	0.4	2.0	µV/Mo
Input Offset Current	I_{os}		--	1.2	3.8	--	1.8	6.0	nA
Input Bias Current	I_B		--	±1.2	+4.0	--	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	--	0.35	0.6	--	0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	--	10.3	18.0	--	10.5	20.0	nV/√Hz
		f_o = 100Hz (Note 2)	--	10.0	13.0	--	10.2	13.5	
		f_o = 1000Hz (Note 2)	--	9.6	11.0	--	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	--	14	30	--	15	35	pAp-p
Input Noise Current Density	i_n	f_o = 10Hz (Note 2)	--	0.32	0.80	--	0.35	0.90	pA/√Hz
		f_o = 100Hz (Note 2)	--	0.14	0.23	--	0.15	0.27	
		f_o = 1000Hz (Note 2)	--	0.12	0.17	--	0.13	0.18	
Input Resistance – Differential Mode	R_{in}		15	50	--	8	33	--	MΩ
Input Resistance – Common Mode	R_{inCM}		--	160	--	--	120	--	GΩ
Input Voltage Range	CMVR		±13.5	±14.0	--	±13.0	±14.0	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	123	--	100	120	--	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	94	107	--	90	104	--	dB
Large Signal Voltage Gain	A_{vo}	R_L ≥ 2kΩ, V_o = ±10V	200	500	--	120	400	--	V/mV
		R_L ≥ 500Ω, V_o = ±.5V, V_s = ±3V	150	500	--	100	400	--	
Maximum Output Voltage Swing	V_{oM}	R_L ≥ 10kΩ	±12.5	±13.0	--	±12.0	±13.0	--	V
		R_L ≥ 2kΩ	±12.0	±12.8	--	±11.5	±12.8	--	
		R_L ≥ 1kΩ	±10.5	±12.0	--	--	±12.0	--	
Slewing Rate	SR	R_L ≥ 2kΩ	--	0.17	--	--	0.17	--	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	--	0.6	--	--	0.6	--	MHz
Open Loop Output Resistance	R_o	V_o = 0, I_o = 0	--	60	--	--	60	--	Ω
Power Consumption	P_d		--	90	120	--	95	150	mW
		V_s = ±3V	--	4	6	--	4	8	
Offset Adjustment Range		R_p = 20kΩ	--	4	--	--	4	--	mV
The following specifications apply for V_s = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}		--	0.25	0.6	--	0.35	1.6	mV
Average Input Offset Voltage Drift									µV/°C
Without External Trim	TCV_{os}	(Note 2)	--	0.7	2.0	--	1.2	4.5	
With External Trim	TCV_{osn}	R_p = 20kΩ	--	0.2	0.6	--	0.4	1.5 (Note 2)	
Input Offset Current	I_{os}		--	1.4	5.3	--	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{os}	(Note 2)	--	8	35	--	12	50	pA/°C
Input Bias Current	I_B		--	±1.5	±5.5	--	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	--	13	35	--	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	--	±13.0	±13.5	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	107	123	--	97	120	--	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	90	104	--	86	100	--	dB
Large Signal Voltage Gain	A_{vo}	R_L ≥ 2kΩ, V_o = ±10V	180	450	--	100	400	--	V/mV
Maximum Output Voltage Swing	V_{oM}	R_L ≥ 2kΩ,	±12.0	±12.6	--	±11.0	±12.6	--	V

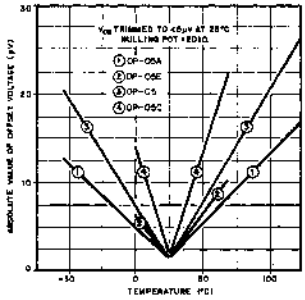
NOTE 1: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV.

Parameter is not 100% tested; 90% of units meet this specification.

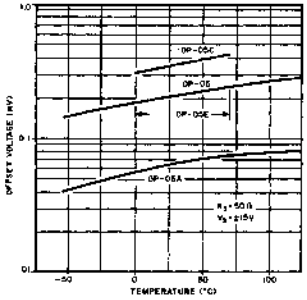
NOTE 2: Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

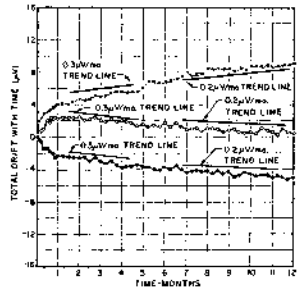
TRIMMED OFFSET VOLTAGE VS TEMPERATURE



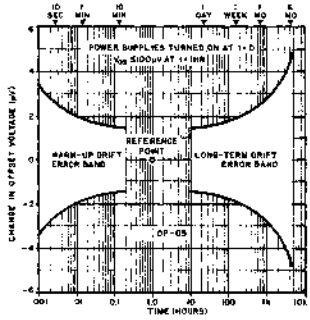
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



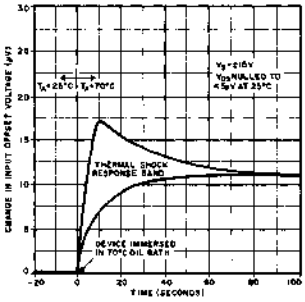
TYPICAL OFFSET VOLTAGE STABILITY VS TIME



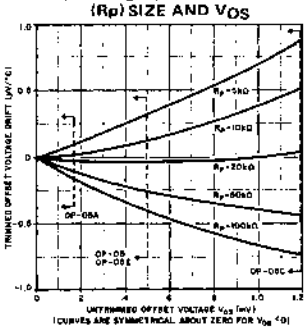
OFFSET VOLTAGE DRIFT WITH TIME



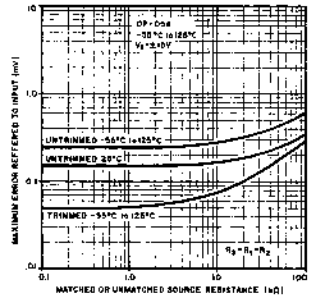
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



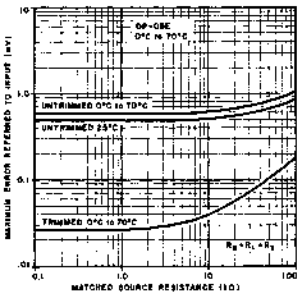
TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER (Rp) SIZE AND V_{OS}



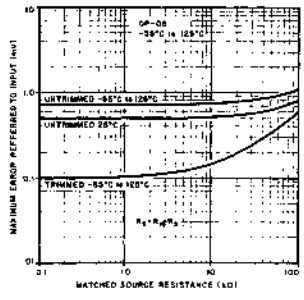
MAXIMUM ERROR VS SOURCE RESISTANCE



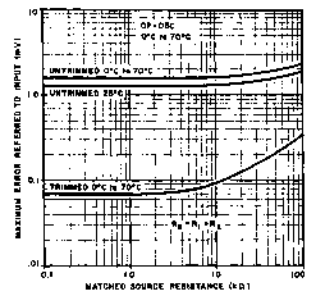
MAXIMUM ERROR VS SOURCE RESISTANCE



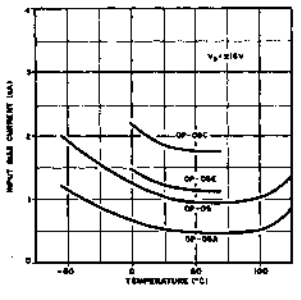
MAXIMUM ERROR VS SOURCE RESISTANCE



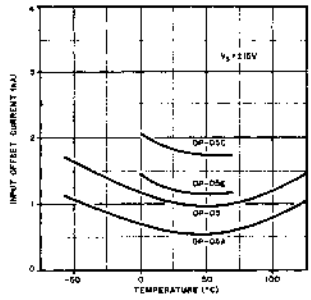
MAXIMUM ERROR VS SOURCE RESISTANCE



INPUT BIAS CURRENT VS TEMPERATURE

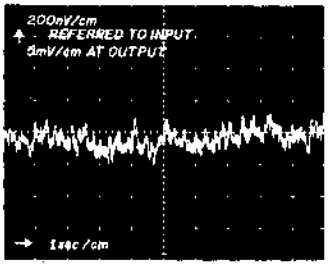


INPUT OFFSET CURRENT VS TEMPERATURE

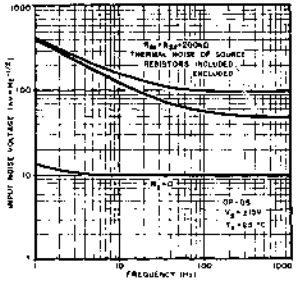


TYPICAL PERFORMANCE CURVES

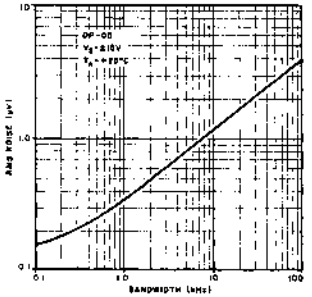
OP-05 LOW FREQUENCY NOISE



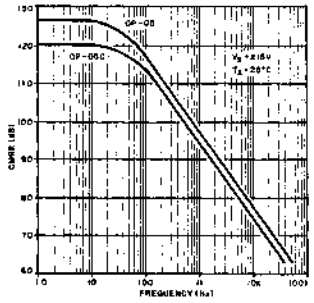
INPUT SPOT NOISE VOLTAGE VS FREQUENCY



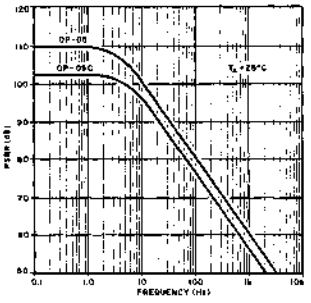
INPUT WIDEBAND NOISE VS BANDWIDTH (.1Hz TO FREQUENCY INDICATED)



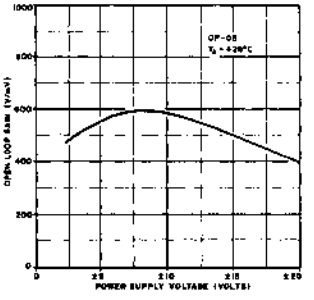
CMRR VS FREQUENCY



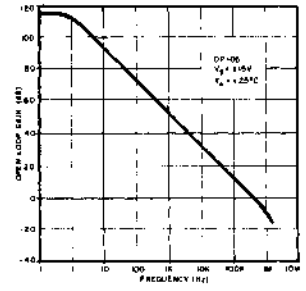
PSRR VS FREQUENCY



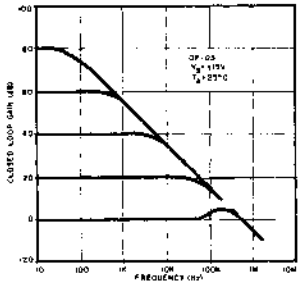
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



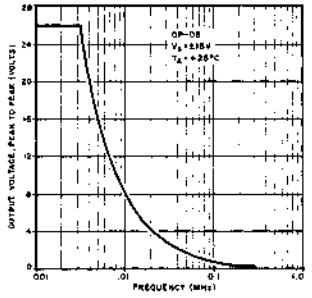
OPEN LOOP FREQUENCY RESPONSE



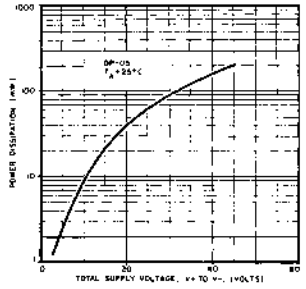
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



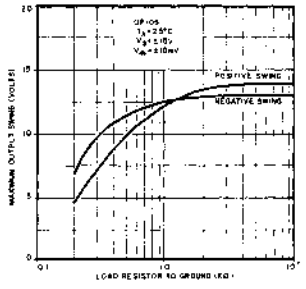
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



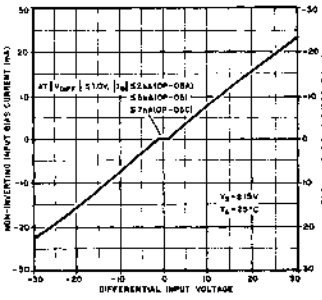
POWER CONSUMPTION VS POWER SUPPLY



OUTPUT POWER VS LOAD



INPUT BIAS CURRENT VS DIFFERENTIAL INPUT VOLTAGE



OP-07

ULTRA-LOW OFFSET VOLTAGE OP AMP

GENERAL DESCRIPTION

The OP-07 Series represents a breakthrough in monolithic operational amplifier performance—Vos of 10μV, TC Vos of 0.2μV/°C and long term stability of 0.2μV/month are achieved by a low noise, chopper-less bipolar input transistor amplifier circuit. Complete elimination of external components for offset nulling, frequency compensation and device protection permits extreme miniaturization and optimization of system Mean-Time-Between-Failure Rates in high performance aerospace/defense and industrial applications. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

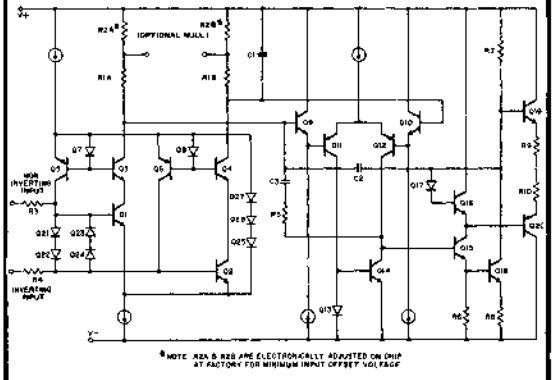
True differential inputs with wide input voltage range and outstanding common mode rejection provide maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

Low cost, high volume production of OP-07 is achieved by electronic adjustment of an on-chip offset trimming network during initial factory testing. The OP-07 provides unparalleled performance for low noise, high accuracy amplification of very low level signals in transducer applications. Other applications include use in stable integrators, precision summing amplifiers for analog computation and test equipment and in ultra-precise voltage threshold detectors and comparators. The OP-07 is recommended as a replacement for modular and monolithic chopper-stabilized amplifiers where reductions in cost, noise, size and power consumption are required. Devices are available in chip form for use in hybrid circuitry. The OP-07 is a direct replacement for 725, 108A/308A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer.

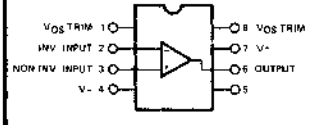
FEATURES

- Ultra-Low Vos . . . . . 10 μV
- Ultra-Low Vos Drift . . . . . 0.2 μV/°C
- Ultra-Stable vs Time . . . . . 0.2 μV/Month
- Ultra-Low Noise . . . . . 0.35 μVp-p
- No External Components Required
- Replaces Chopper amps at Lower Cost
- Single Chip Monolithic Construction
- High Common Mode Input Range . . . . . ±14.0V
- Wide Supply Voltage Range . . . . . ±3V to ±18V
- Fits 725, 108A/308A, 741,AD510 Sockets

SIMPLIFIED SCHEMATIC

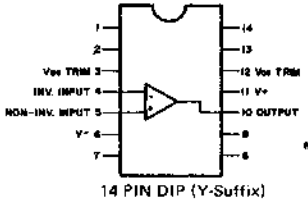


PIN CONNECTIONS AND ORDERING INFORMATION

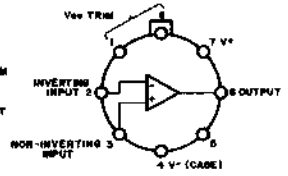


EPOXY 8 MINI-DIP (P-Suffix)
ORDER: OP-07CP

TOP VIEW



14 PIN DIP (Y-Suffix)
ORDER: OP-07AY OP-07CY
OP-07Y
OP-07EY



TO-99 (J-Suffix)
ORDER: OP-07AJ OP-07CJ
OP-07J OP-07DJ
OP-07EJ

Military Temperature Range Devices with MIL-STD-883A Class B Processing

ORDER: OP07-883-AJ
OP07-883-AY
OP07-883-J
OP07-883-Y

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Storage Temperature Range	-65°C to +150°C
Internal Power Dissipation (Note 1)	500mW	Operating Temperature Range	
Differential Input Voltage	±30V	OP-07A, OP-07	-55°C to +125°C
Input Voltage (Note 2)	±22V	OP-07E, OP-07C, OP-07D	0°C to +70°C
Output Short Circuit Duration	Indefinite	Lead Temperature Range (Soldering, 60 sec)	300°C

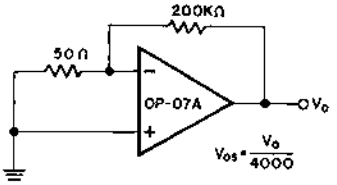
NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

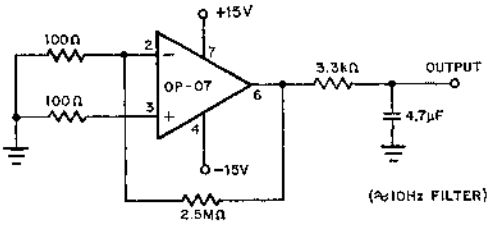
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (Y)	100°C	10.0mW/°C
Flat Pack (L)	62°C	5.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

OFFSET VOLTAGE TEST CIRCUIT



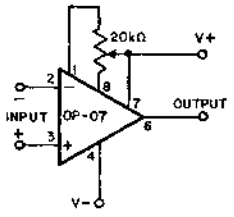
LOW FREQUENCY NOISE TEST CIRCUIT



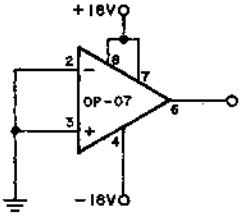
INPUT REFERRED NOISE = $\frac{V_o}{25,000} = \frac{5mV/cm}{25,000} = 200nV/cm$

SEE NOISE PHOTO-PAGE 6

OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

OP-07 Series units may be fitted directly to 725, 108A/308A and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OP-07 may be fitted to unnulled 741-type sockets; however if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see diagram above).

The OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-07A Min	OP-07A Typ	OP-07A Max	OP-07 Min	OP-07 Typ	OP-07 Max	Units
Input Offset Voltage	V_{os}	(Note 1)	—	10	25	—	30	75	µV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	µV/Mo
Input Offset Current	I_{os}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f_O = 100Hz (Note 3)	—	10.0	13.0	—	10.0	13.0	
		f_O = 1000Hz (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz (Note 3)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		fo = 100Hz (Note 3)	—	0.14	0.23	—	0.14	0.23	
		fo = 1000Hz (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance - Differential Mode	R_{in}		30	80	—	20	60	—	MΩ
Input Resistance - Common Mode	R_{inCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	110	—	100	110	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_O = ±10V	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, V_O = ±.5V, V_S = ±3V	150	500	—	150	500	—	
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	Ω
Power Consumption	Pd		—	75	120	—	75	120	mW
		V_S = ±3V	—	4	6	—	4	6	
Offset Adjustment Range		R_p = 20kΩ	—	±4	—	—	±4	—	mV

The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Input Offset Voltage	V_{os}	(Note 1)	—	25	60	—	60	200	µV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{os}		—	0.2	0.6	—	0.3	1.3	µV/°C
With External Trim	TCV_{osn}	R_p = 20kΩ	—	0.2	0.6	—	0.3	1.3	µV/°C
Input Offset Current	I_{os}		—	0.8	4.0	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{os}		—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		—	8	25	—	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	106	—	94	106	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_O = ±10V	200	400	—	150	400	—	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.6	—	V

NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV — Parameter is not 100% tested; 90% of units meet this specification.

NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

ELECTRICAL CHARACTERISTICS			OP-07E			OP-07C			OP-07D			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	(Note 1)	–	30	75	–	60	150	–	60	150	µV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	–	0.3	1.5	–	0.4	2.0	–	0.5	3.0	µV/Mo
Input Offset Current	I_{OS}		–	0.5	3.8	–	0.8	6.0	–	0.8	6.0	nA
Input Bias Current	I_B		–	±1.2	±4.0	–	±1.8	±7.0	–	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	–	0.35	0.6	–	0.38	0.65	–	0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	–	10.3	18.0	–	10.5	20.0	–	10.5	20.0	nV/√Hz
		f_O = 100Hz (Note 3)	–	10.0	13.0	–	10.2	13.5	–	10.2	13.5	
		f_O = 1000Hz (Note 3)	–	9.6	11.0	–	9.8	11.5	–	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	–	14	30	–	15	35	–	15	35	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 3)	–	0.32	0.80	–	0.35	0.90	–	0.35	0.90	pA/√Hz
		f_O = 100Hz (Note 3)	–	0.14	0.23	–	0.15	0.27	–	0.15	0.27	
		f_O = 1000Hz (Note 3)	–	0.12	0.17	–	0.13	0.18	–	0.13	0.18	
Input Resistance — Diff. Mode	R_{in}		15	50	–	8	33	–	7	31	–	MΩ
Input Resistance — Common Mode	R_{inCM}		–	160	–	–	120	–	–	120	–	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	–	±13.0	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	–	100	120	–	94	110	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	107	–	90	104	–	90	104	–	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	200	500	–	120	400	–	120	400	–	V/mV
		R_L ≥ 500Ω, V_O = ±5V, V_S = ±3V	150	500	–	100	400	–	–	–	–	
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10kΩ	±12.5	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
		R_L ≥ 2kΩ	±12.0	±12.8	–	±11.5	±12.8	–	±11.5	±12.8	–	
		R_L ≥ 1kΩ	±10.5	±12.0	–	–	±12.0	–	–	–	–	
Slewing Rate	SR	R_L ≥ 2kΩ	–	0.17	–	–	0.17	–	–	0.17	–	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.6	–	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	60	–	–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±3V	–	75	120	–	80	150	–	80	150	mW
			–	4	6	–	4	8	–	4	8	
Offset Adjustment Range		R_p = 20kΩ	–	±4	–	–	±4	–	–	±4	–	mV
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	(Note 1)	–	45	130	–	85	250	–	85	250	µV
Average Input Offset Voltage Drift								(Note3)			(Note3)	
Without External Trim	TCV_{OS}		–	0.3	1.3	–	0.5	1.8	–	0.7	2.5	µV/°C
With External Trim	TCV_{OSn}	R_p = 20kΩ	–	0.3	1.3	–	0.4	1.6 (Note3)	–	0.7	2.5 (Note3)	
Input Offset Current	I_{OS}		–	0.9	5.3	–	1.6	8.0	–	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 3)	–	8	35		12	50	–	12	50	pA/°C
Input Bias Current	I_B		–	±1.5	±5.5	–	±2.2	±9.0	–	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 3)	–	13	35	–	18	50	–	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	103	123	–	97	120	–	94	106	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	90	104	–	86	100	–	86	100	–	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	180	450	–	100	400	–	100	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 2kΩ	±12.0	±12.6	–	±11.0	±12.6	–	±11.0	±12.6	–	V

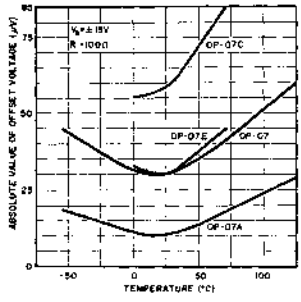
NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV — Parameter is not 100% tested; 90% of units meet this specification.

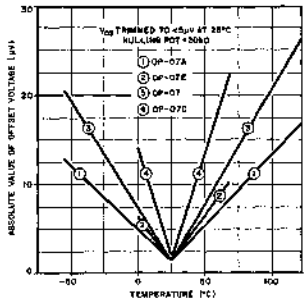
NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

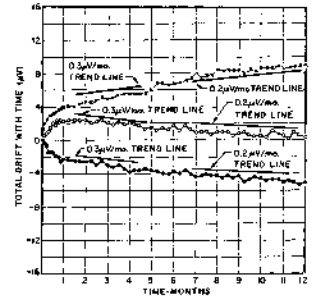
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



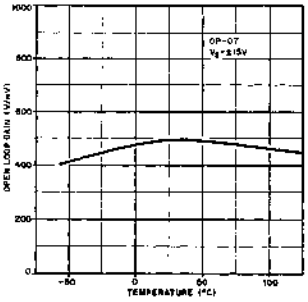
TRIMMED OFFSET VOLTAGE VS TEMPERATURE



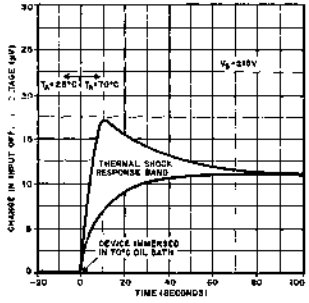
OFFSET VOLTAGE STABILITY VS TIME



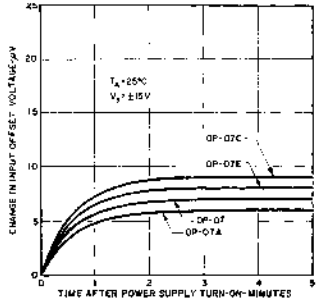
OPEN LOOP GAIN VS TEMPERATURE



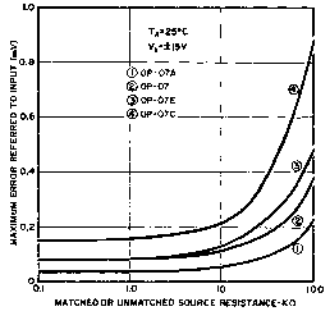
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



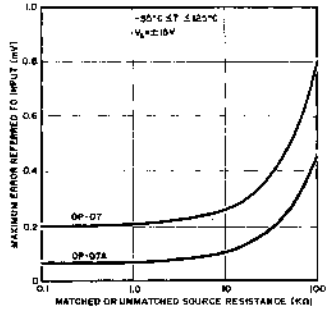
WARM-UP DRIFT



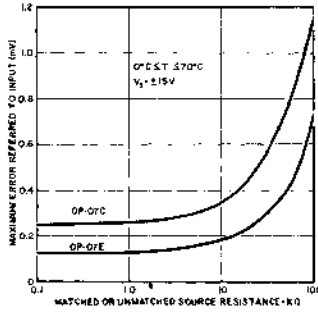
MAXIMUM ERROR VS SOURCE RESISTANCE



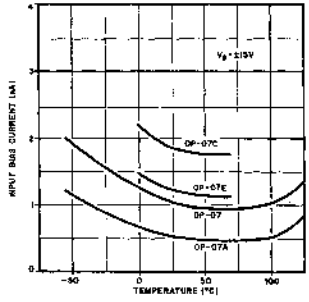
MAXIMUM ERROR VS SOURCE RESISTANCE



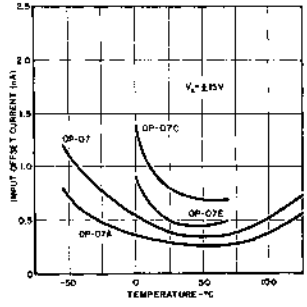
MAXIMUM ERROR VS SOURCE RESISTANCE



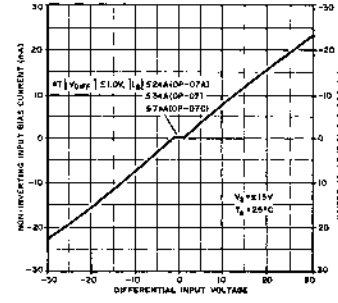
INPUT BIAS CURRENT VS TEMPERATURE



INPUT OFFSET CURRENT VS TEMPERATURE

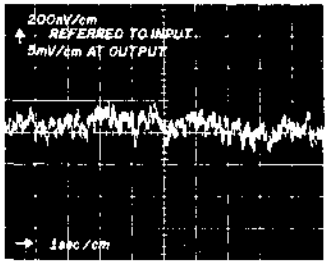


INPUT BIAS CURRENT VS DIFFERENTIAL INPUT VOLTAGE

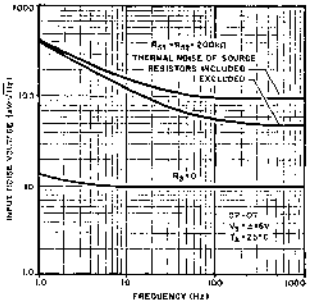


TYPICAL PERFORMANCE CURVES

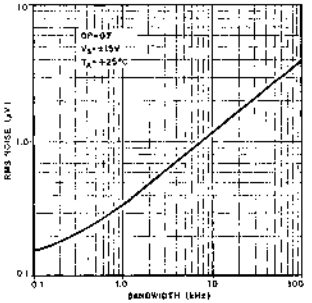
OP-07 LOW FREQUENCY NOISE



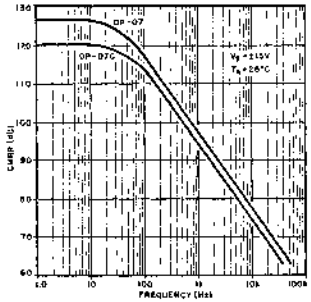
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



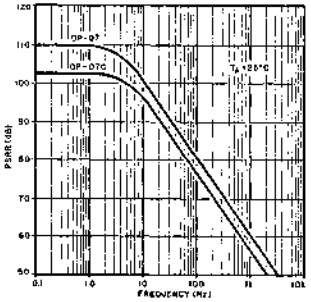
INPUT WIDEBAND NOISE VS BANDWIDTH (.1Hz TO FREQUENCY INDICATED)



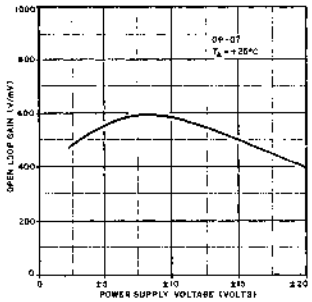
CMRR VS FREQUENCY



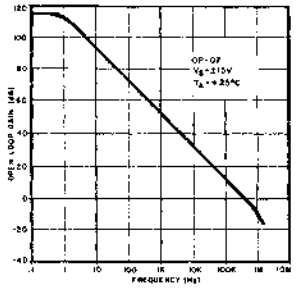
PSRR VS FREQUENCY



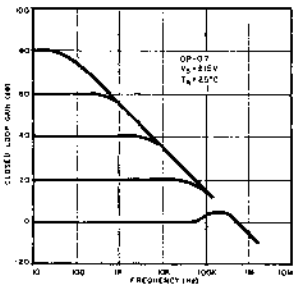
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



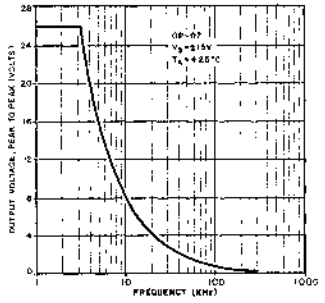
OPEN LOOP FREQUENCY RESPONSE



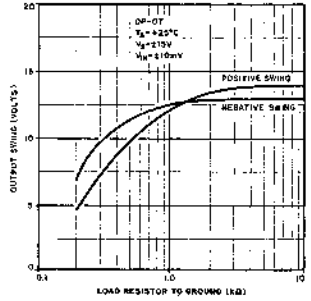
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



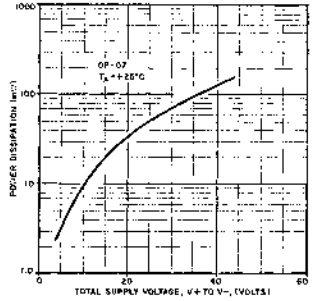
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



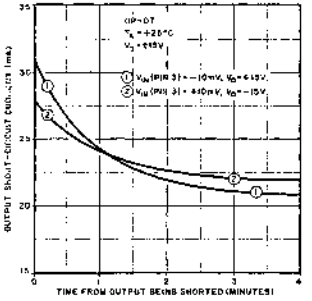
OUTPUT VOLTAGE VS. LOAD RESISTANCE



POWER CONSUMPTION VS POWER SUPPLY



OUTPUT SHORT-CIRCUIT CURRENT VS TIME



OP-08

PRECISION LOW INPUT CURRENT OP AMP

GENERAL DESCRIPTION

The PMI OP-08 is an improved version of the popular LM108A low power op amp. The OP-08 has a three times lower offset voltage and a two times lower offset voltage drift. The total worst case input offset voltage over −55°C to +125°C for the OP-08 is only 350μV, while the 108A has 900μV to 1000μV for these conditions. In addition the OP-08 drives a 2kΩ load. This is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super beta process and on-chip-zener-zap trimming capabilities. For devices with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

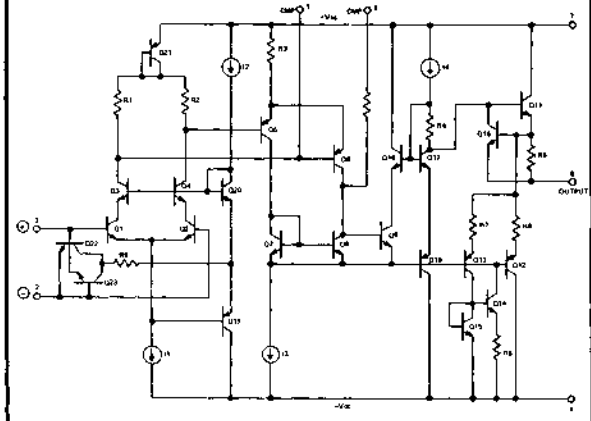
FEATURES

- Low Offset Voltage . . . . . 150μV Max.
- Low Offset Voltage Drift . . . . . 2.5μV/°C Max.
- Five Times PM108A Load Current . . . . . 5 mA Min.

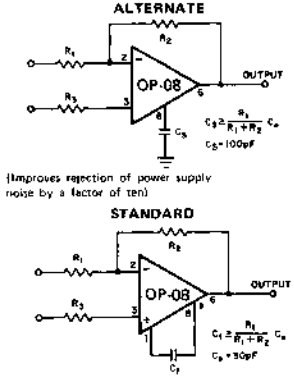
Plus the Outstanding PM108A Features

- Low Offset Current . . . . . 200 pA Max.
- Low Bias Current . . . . . 2.0 nA Max.
- Low Power Consumption . . . . 18 mW max. @ ±15V
- High Common Mode Input Range . . . . ±13.5V Min.
- MIL-STD-883A Class B Processing Available
- Silicon-Nitride Passivation

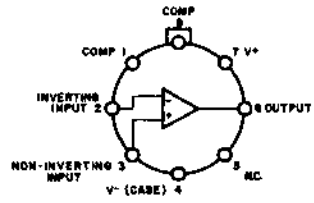
SIMPLIFIED SCHEMATIC



COMPENSATION CIRCUITS



PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)

ORDER: OP-08AJ
OP-08BJ
OP-08CJ
OP-08EJ
OP-08FJ
OP-08GJ

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP08-883-AJ
OP08-883-BJ
OP08-883-CJ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
OP-08A, OP-08B, OP-08C	±20V
OP-08E, OP-08F, OP-08G	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
OP-08A, OP-08B, OP-08C	-55°C to +125°C
OP-08E, OP-08F, OP-08G	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
(Soldering, 60 sec)	300°C

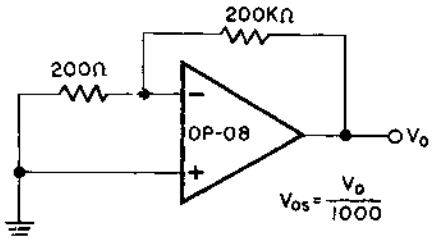
NOTE 1: Maximum package power dissipation vs. ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C

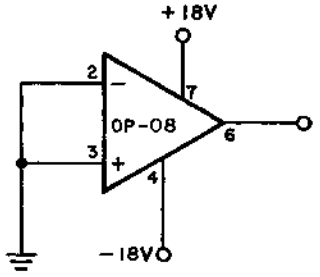
NOTE 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.

NOTE 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

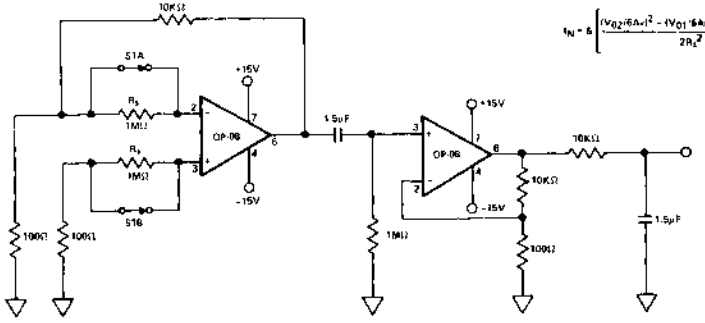
OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



LOW FREQUENCY NOISE TEST CIRCUIT (0.1 TO 10 Hz)



$$e_N = 6\left[\frac{(V_{O2}/6A_{V1})^2 - (V_{O1}/6A_{V1})^2 - 2(4kT)R_S}{2R_S^2}\right]^{1/2}$$

NOTES: 1. S1 CLOSED MEASURES e_n (V_{O1}).
2. S1 OPEN MEASURES e_n AND I_n (V_{O2}). I_n IS COMPUTED FROM THE TWO MEASUREMENTS.
3. COMPENSATION COMPONENTS NOT SHOWN BUT THEY ARE CONNECTED.
4. SEE NOISE PHOTO OF e_n IN TYPICAL PERFORMANCE CURVES SECTION.

ELECTRICAL CHARACTERISTICS			OP-08A			OP-08B			OP-08C			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}		–	0.07	0.15	–	0.18	0.30	–	0.25	1.0	mV
Input Offset Current	I_{OS}		–	0.05	0.20	–	0.05	0.20	–	0.08	0.50	nA
Input Bias Current	I_B		–	0.80	2.0	–	0.80	2.0	–	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.9	–	–	0.9	–	–	0.9	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	22 21 20	– – –	– – –	22 21 20	– – –	– – –	22 21 20	– – –	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	3	–	–	3	–	–	3	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{in}		26	70	–	26	70	–	10	60	–	MΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	104	120	–	104	120	–	84	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	104	120	–	104	120	–	84	116	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10K\Omega$, V_O = ±10V $R_L \geq 2K\Omega$, V_O = ±10V	80 50	300 150	– –	80 50	300 150	– –	40 –	250 100	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Slewing Rate	SR	$R_L \geq 2K\Omega$	–	0.12	–	–	0.12	–	–	0.12	–	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.80	–	–	0.80	–	–	0.80	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	200	–	–	200	–	–	200	–	Ω
Power Consumption	Pd	V_S = ±15V V_S = ±5V	– –	9 3	18 6	– –	9 3	18 6	– –	12 4	24 8	mW
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}		–	0.12	0.35	–	0.28	0.60	–	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	–	1.0	3.5	–	1.5	10	µV/°C
Input Offset Current	I_{OS}		–	0.12	0.40	–	0.12	0.40	–	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	–	0.50	2.5	–	1.0	5.0	pA/°C
Input Bias Current	I_B		–	1.2	3.0	–	1.2	3.0	–	1.8	10	nA
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	100	110	–	100	110	–	80	106	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	100	110	–	100	110	–	80	106	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 5K\Omega$, V_O = ±10V	40	120	–	40	120	–	15	80	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$ $R_L \geq 5K\Omega$	±13.0 ±10.0	±14.0 ±13.0	– –	±13.0 ±10.0	±14.0 ±13.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Power Consumption	Pd		–	9	18	–	9	18	–	15	24	mW

ELECTRICAL CHARACTERISTICS			OP-08E			OP-08F			OP-08G			

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

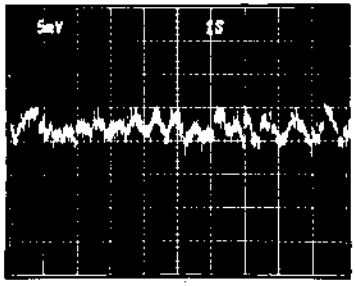
Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}		–	0.07	0.15	–	0.18	0.30	–	0.25	1.0	mV
Input Offset Current	I_{OS}		–	0.05	0.20	–	0.07	0.40	–	0.08	0.50	nA
Input Bias Current	I_B		–	0.80	2.0	–	0.90	4.0	–	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.9	–	–	0.9	–	–	0.9	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	22 21 20	– – –	– – –	22 21 20	– – –	– – –	22 21 20	– – –	nV/$\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	3	–	–	3	–	–	3	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	pA/$\sqrt{Hz}$
Input Resistance – Differential Mode	R_{in}		26	70	–	13	60	–	10	50	–	MΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	104	120	–	102	120	–	84	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	104	120	–	102	120	–	84	116	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq$ 10KΩ, V_O = ±10V $R_L \geq$ 2KΩ, V_O = ±10V	80 50	300 150	– –	80 30	300 120	– –	40 –	250 100	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq$ 10KΩ $R_L \geq$ 2KΩ	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Slewing Rate	SR	$R_L \geq$ 2KΩ	–	0.12	–	–	0.12	–	–	0.12	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.80	–	–	0.80	–	–	0.80	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	200	–	–	200	–	–	200	–	Ω
Power Consumption	Pd	V_S = ±15V V_S = ±5V	– –	9 3	18 6	– –	9 3	18 6	– –	12 4	24 8	mW

The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.10	0.26	–	0.23	0.45	–	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	–	1.0	3.5	–	1.5	10	μV/°C
Input Offset Current	I_{OS}		–	0.08	0.30	–	0.11	0.60	–	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	–	1.0	5.0	–	1.0	5.0	pA/°C
Input Bias Current	I_B		–	1.0	2.6	–	1.2	5.2	–	1.4	6.5	nA
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	–	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	100	116	–	100	116	–	80	112	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	100	116	–	100	116	–	80	112	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq$ 2KΩ, V_O = ±10V $R_L \geq$ 10KΩ, V_O = ±10V	25 60	100 200	– –	15 60	100 200	– –	– 25	80 150	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq$ 10KΩ $R_L \geq$ 2KΩ	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Power Consumption	P_D		–	9	18	–	9	18	–	15	24	mW

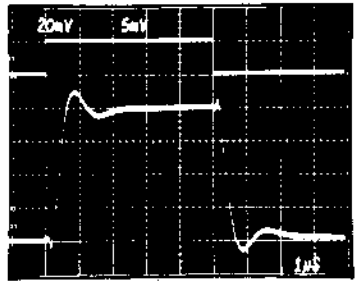
TYPICAL PERFORMANCE CURVES

LOW FREQUENCY NOISE

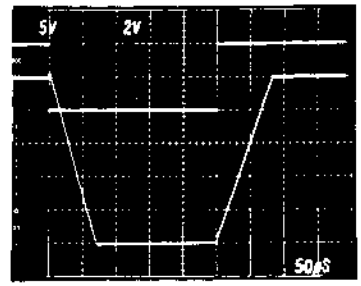


R_S = 0, BW = 0.1Hz to 10Hz
5 mV/div AT OUTPUT
0.5 μV/div REFERRED TO INPUT

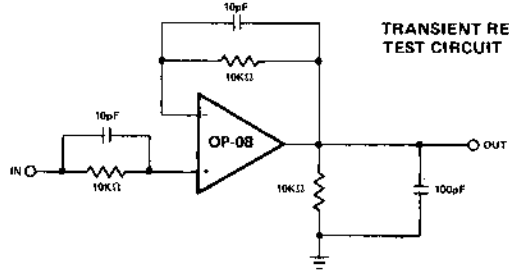
SMALL SIGNAL TRANSIENT RESPONSE



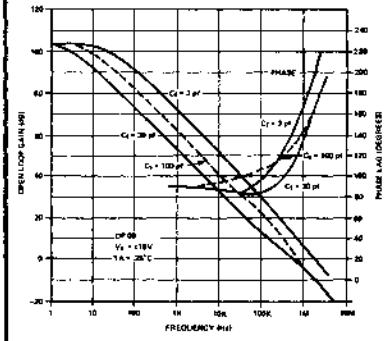
LARGE SIGNAL TRANSIENT RESPONSE



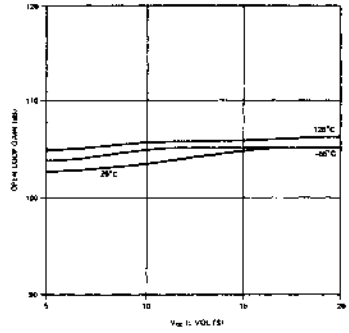
TRANSIENT RESPONSE TEST CIRCUIT



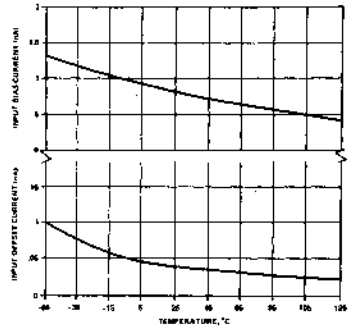
OPEN LOOP GAIN (A_{VO}) AND PHASE VS. FREQUENCY



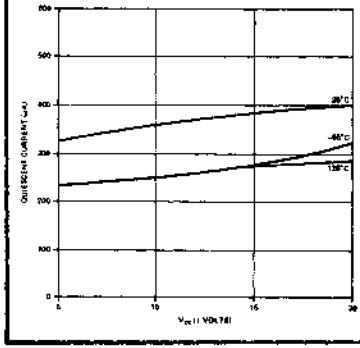
OPEN LOOP GAIN (Avo) VS. SUPPLY VOLTAGE (Vcc) WITH TEMPERATURE AS A PARAMETER



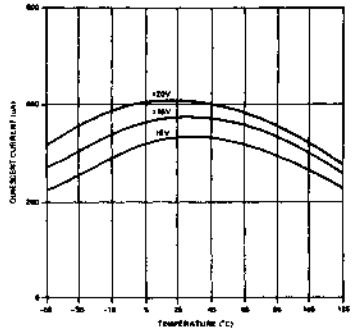
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VS. TEMPERATURE



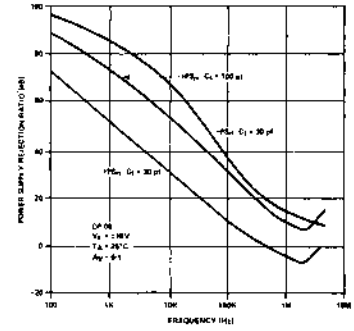
QUIESCENT CURRENT (ISY) VS. SUPPLY VOLTAGE WITH TEMPERATURE AS A PARAMETER



QUIESCENT CURRENT (ISY) VS. TEMPERATURE WITH SUPPLY VOLTAGE AS A PARAMETER



POWER SUPPLY REJECTION RATIO (PSRR) VS. FREQUENCY

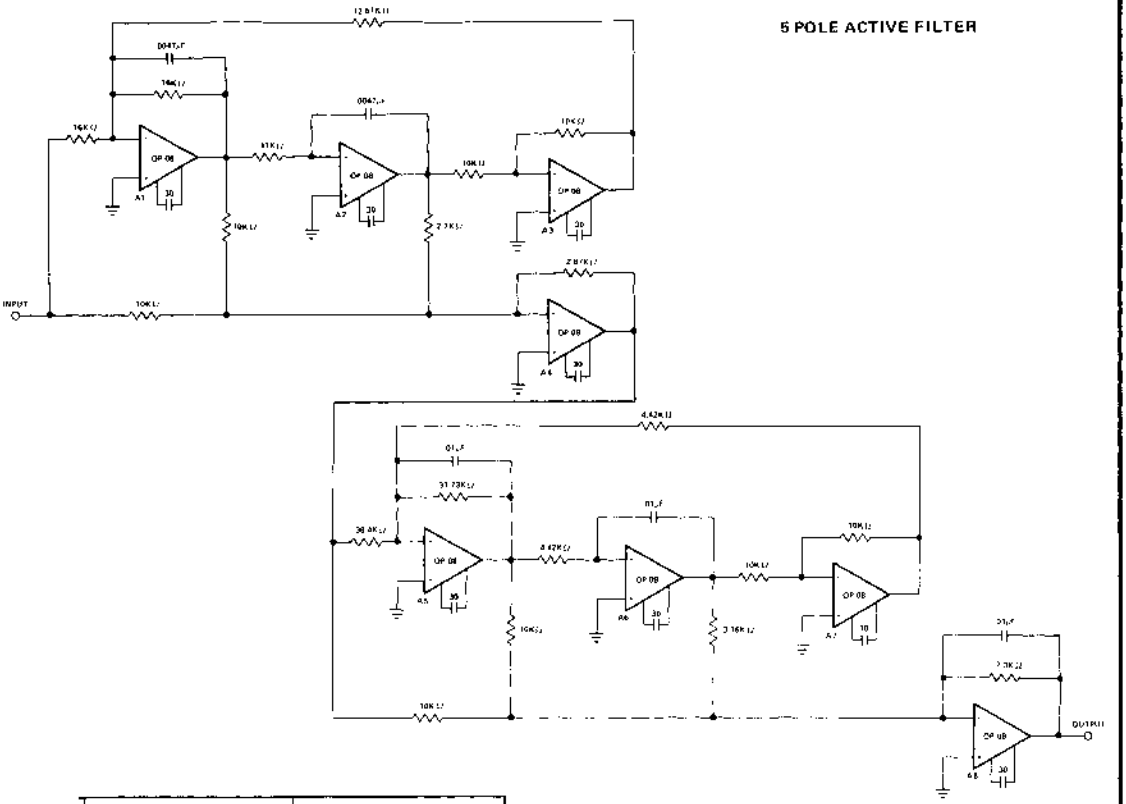


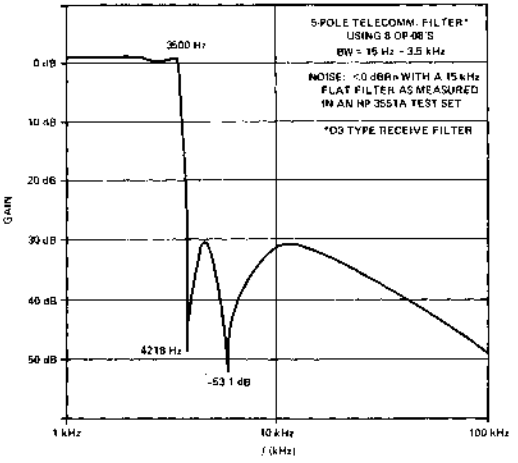
APPLICATIONS INFORMATION

The OP-08 series has extremely low input offset and bias currents; the user is cautioned that stray printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to fully realize the OP-08 performance. It is suggested that effects of board leakage be minimized by encircling the input pins with a conductive guard ring operated at a potential close to that of the inputs. This guard ring should be driven by a low impedance source such as the amplifier's output for non-inverting circuits, or be tied to ground for inverting circuits.

TYPICAL APPLICATIONS

5 POLE ACTIVE FILTER

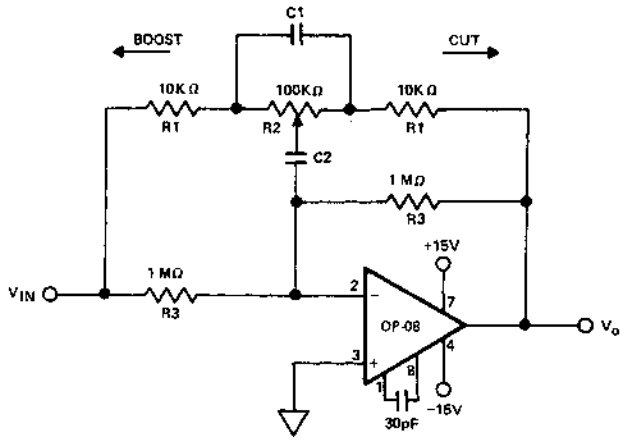




The above realization of a type D3 receive filter is accomplished using eight OP-08's. As can be seen from the response curve, the >30 dB attenuation in the stop band requirement has been met. In addition, the noise performance of <0 dBRn has been measured. One of the unique features of the OP-08 is its low supply current of 600 μA max. Thus the total supply drain for all eight op amps is only 4.8 mA.

TYPICAL APPLICATIONS

OCTAVE EQUALIZER

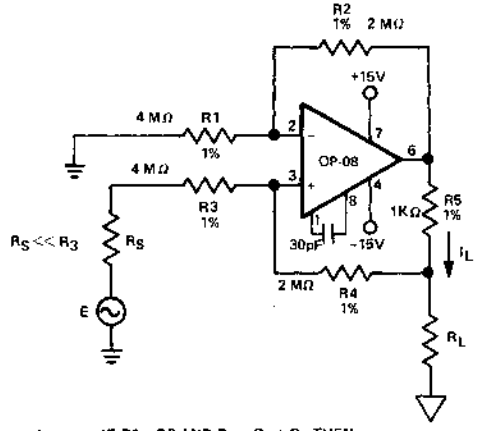


The above circuit is one section of an octave equalizer used in audio systems. The table shows the values of C1 and C2 needed to achieve the given center frequencies. This circuit is capable of 12 dB boost or cut as determined by the position of R2.

Because of the low input bias current of the OP-08 the resistors could be scaled up by a factor of ten, and thereby reduce the values of C1 and C2 at the low frequency end. In addition ten sections as shown above will only draw a combined supply current of 6 mA maximum.

f_o (Hz)	C_1	C_2
32	0.18μF	0.018μF
64	0.1μF	0.01μF
125	0.047μF	0.0047μF
250	0.022μF	0.0022μF
500	0.012μF	0.0012μF
1k	0.0056μF	560pF
2k	0.0027μF	270pF
4k	0.0015μF	150pF
8k	680pF	68pF
16k	360pF	36pF

BILATERAL CURRENT SOURCE



$$i_L \cong \frac{E R_4}{R_3 R_5}$$

IF R1 = R3 AND $R_2 = R_4 + R_5$ THEN i_L IS INDEPENDENT OF VARIATIONS IN R_L.

The above circuit will produce the above current relationship to within 2% using 1% values for R1 through R5. This includes variations in R_L from 10Ω to 2000Ω. The use of large resistors for R1 through R4 minimizes the error due to R_L variations. The large resistors are possible because of the excellent input bias current performance of the OP-08.

OP-09

QUAD MATCHED 741-TYPE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-09 provides four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-09 is pin compatible with the RM4136 and RC4136 amplifiers. The amplifiers are matched for common mode rejection ratio and offset voltage. These parameters are very important in the design of instrumentation amplifiers. In addition the amplifier is designed to have equal positive-going and negative-going slew rates. This is a very important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift and excellent long term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost.

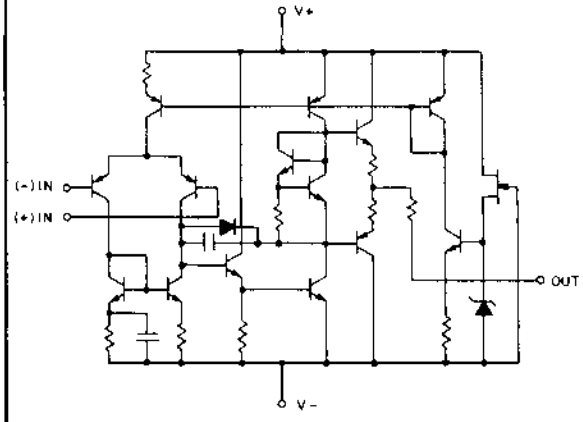
FEATURES

- Guaranteed V_{OS} . . . . . 500μ V MAX.
- Guaranteed Matched CMRR . . . . . 94 dB MIN.
- Guaranteed Matched V_{OS} . . . . . 750 μV MAX.
- RM4136/RC4136 Direct Replacements
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short Circuit Protection
- Low Input Bias Current

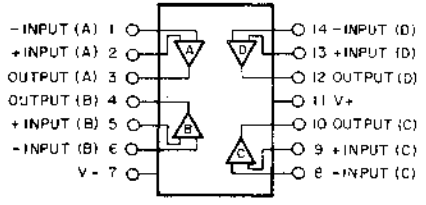
The OP-09 is ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance. OP-09's with processing per the requirements of MIL-STD-883A are available. For dual-741-type versions, see the OP-04 and OP-14 data sheets.

EQUIVALENT SCHEMATIC

(1/4 CIRCUIT SHOWN)



PIN CONNECTIONS



TOP VIEW

ORDERING INFORMATION

ORDER: OP-09AY, OP-09BY — -55°C TO +125°C
OP-09EY, OP-09FY — 0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP09-883-AY
OP09-883-BY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous (One Amplifier Only)
Storage Temperature Range	−65° to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

OP-09A, OP-09B	−55°C to +125°C
OP-09E, PO-09F	0°C to +70°C

Note 1: Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14 Pin DIP (Y)	80°C	10 mW/°C

MATCHING CHARACTERISTICS

OP-09A OP-09E | OP-09B OP-09F

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, $R_S \leq 100\Omega$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage Match	ΔV_{OS}	(Note 4)	–	0.5	0.75	–	0.8	2.0	mV
Common Mode Rejection Ratio Match (Note 3)	ΔCMRR	$V_{CM} = \pm CMVR$	–	1.0	20	–	1.0	20	μV/V
			94	120	–	94	120	–	dB
These specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-09A and OP-09B, $0°C \leq T_A \leq +70°C$ for OP-09E and OP-09F $R_S \leq 100\Omega$ unless otherwise noted.									
Input Offset Voltage Match	ΔV_{OS}	(Note 4)	–	0.6	1.0	–	1.0	2.5	mV
Common Mode Rejection Ratio Match (Note 3)	ΔCMRR	$V_{CM} = \pm CMVR$	–	3.2	20	–	3.2	20	μV/V
			94	110	–	94	110	–	dB

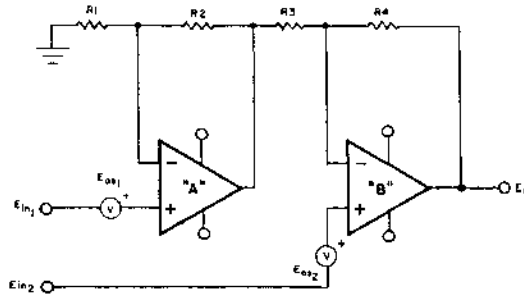
MATCHING PARAMETER DEFINITIONS

COMMON MODE REJECTION RATIO MATCH (ΔCMRR). The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. ΔCMRR in dB = $-20 \log_{10}$ (ΔCMRR in volt/volt). See note 3.

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$). See note 4.

TYPICAL APPLICATION

INSTRUMENTATION AMPLIFIER 2 OP-AMP DESIGN



GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$1)\ E_o = -\left[E_{in1}\left(1 + \frac{R_2}{R_1}\right)\frac{R_4}{R_3}\right] + E_{in2}\left(\frac{R_4}{R_3} + 1\right)$$

With ideal resistors this simplifies to:

$$2)\ E_o = \left(E_{in2} - E_{in1}\right)\left(\frac{R_4}{R_3} + 1\right) \text{ provided } \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

COMMON MODE REJECTION

Because the dual op amp has a high common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching. This device eliminates the need for special op amp selections in many instrumentation amplifier applications.

DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage (E_{os2}-E_{os1}) will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected.

ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-09A			OP-09B			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.30	0.50	–	0.60	2.5	mV
Input Offset Current	I_{OS}		–	8.0	20	–	25	50	nA
Input Bias Current	I_B		–	180	300	–	300	500	nA
Input Resistance Differential Mode	R_{in}		0.20	0.40	–	0.20	0.40	–	MΩ
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	100	650	–	100	650	–	V/mV
Power Consumption (Note 2)	P_d	V_O = 0V	–	123	180	–	123	180	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.7	–	–	0.7	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	18 14 12	– – –	– – –	18 14 12	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	17	–	–	17	–	pA p-p
Channel Separation	CS		100	130	–	100	130	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.8 1.5 1.2	– – –	– – –	1.8 1.5 1.2	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.70	1.0	–	0.70	1.0	–	V/µs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	11	16	–	11	16	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	1.5	2.0	–	1.5	2.0	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	80	120	–	80	120	nsec
Overshoot (Note 1)			–	15	25	–	15	25	%
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.40	1.0	–	1.0	3.5	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 10k\Omega$	–	2.0	10	–	4.0	15	µV/°C
Input Offset Current	I_{OS}		–	20	40	–	40	80	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.10	0.30	–	0.30	0.60	nA/°C
Input Bias Current	I_B			200	375	–	400	650	nA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \geq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	100	250	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Power Consumption (Note 2)	P_d	V_O = 0V	–	115	200	–	115	200	mW

NOTE 1: Parameter is not 100% tested. 90% of all units meet these specifications.

NOTE 2: Total dissipation for all 4 amplifiers in package.

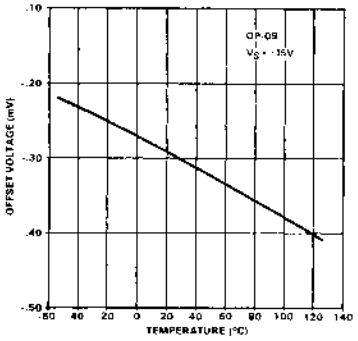
NOTE 3: Match exists between any two amplifiers.

NOTE 4: Using amplifier A as reference then $\Delta V_{OS} = V_{OSn} - V_{OSA}$.

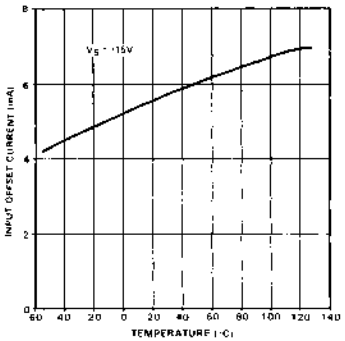
ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-09E			OP-09F			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.30	0.50	–	0.60	2.5	mV
Input Offset Current	I_{OS}		–	8.0	20	–	25	50	nA
Input Bias Current	I_B		–	180	300	–	300	500	nA
Input Resistance Differential Mode	R_{in}		0.20	0.40	–	0.20	0.40	–	MΩ
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	100	650	–	100	650	–	V/mV
Power Consumption (Note 2)	P_d	V_O = 0V	–	123	180	–	123	180	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.7	–	–	0.7	–	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	18 14 12	– – –	– – –	18 14 12	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	17	–	–	17	–	pA p-p
Channel Separation	CS		100	130	–	100	130	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.8 1.5 1.2	– – –	– – –	1.8 1.5 1.2	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.70	1.0	–	0.70	1.0	–	V/μs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	11	16	–	11	16	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	1.5	2.0	–	1.5	2.0	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	80	120	–	80	120	nsec
Overshoot (Note 1)			–	15	25	–	15	25	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.40	0.80	–	0.80	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 10k\Omega$	–	2.0	10	–	4.0	15	μV/°C
Input Offset Current	I_{OS}		–	20	30	–	40	60	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.10	0.30	–	0.30	0.60	nA/°C
Input Bias Current	I_B		–	200	350	–	400	550	nA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	100	250	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Power Consumption (Note 2)	P_d	V_O = 0V	–	115	200	–	115	200	mW

TYPICAL PERFORMANCE CURVES

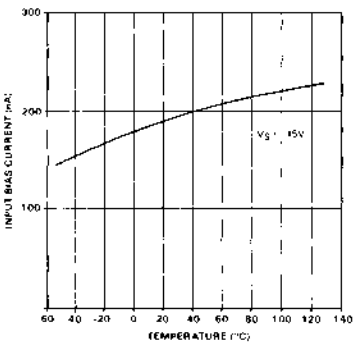
OFFSET VOLTAGE VS TEMPERATURE



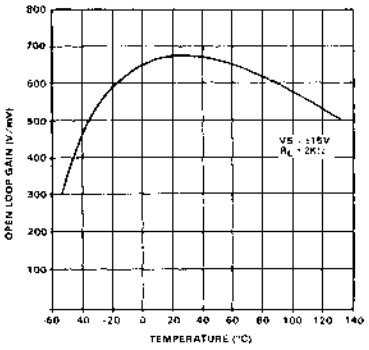
OFFSET CURRENT VS TEMPERATURE



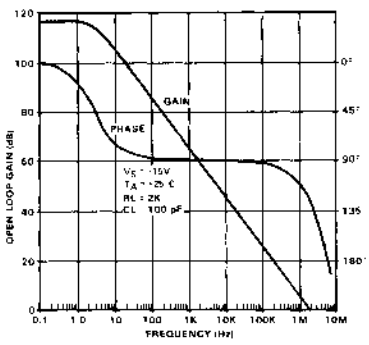
BIAS CURRENT VS TEMPERATURE



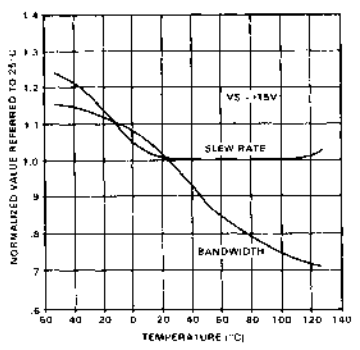
OPEN LOOP GAIN VS TEMPERATURE



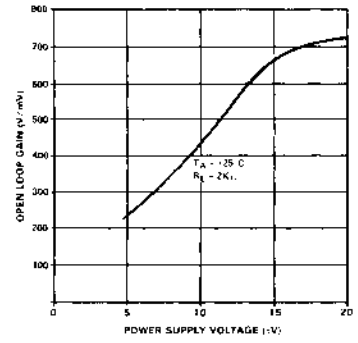
OPEN LOOP FREQUENCY & PHASE RESPONSE



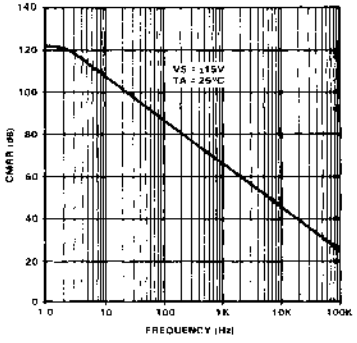
NORMALIZED A/C PARAMETERS VS TEMPERATURE



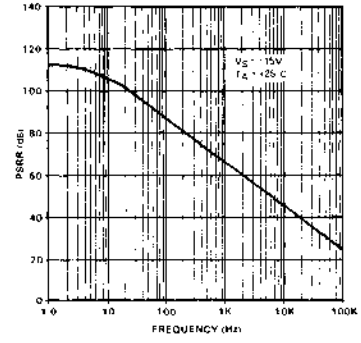
OPEN LOOP GAIN VS SUPPLY VOLTAGE



CMRR VS FREQUENCY

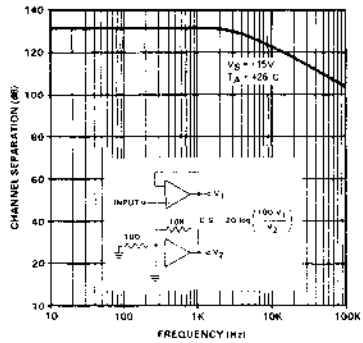


PSRR VS FREQUENCY

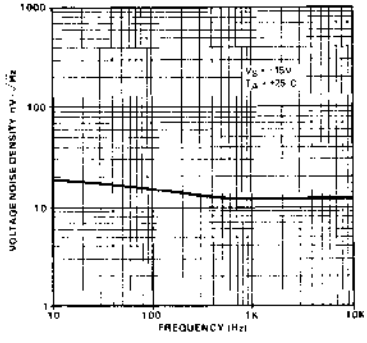


TYPICAL PERFORMANCE CURVES

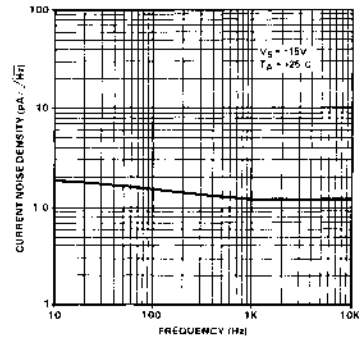
CHANNEL SEPARATION VS FREQUENCY



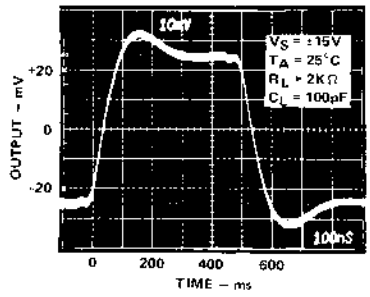
SPOT NOISE VOLTAGE VS FREQUENCY



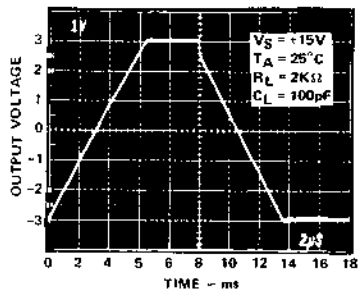
SPOT NOISE CURRENT VS FREQUENCY



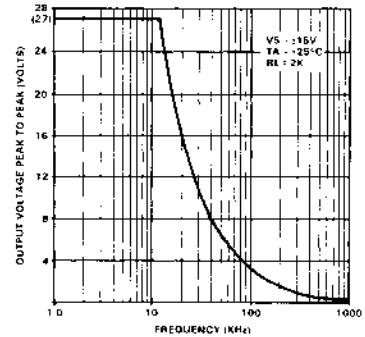
TRANSIENT RESPONSE



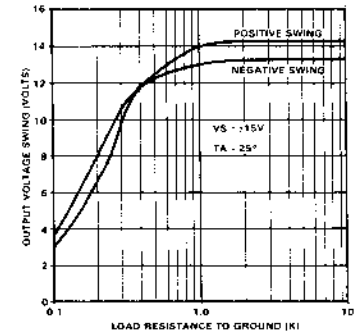
VOLTAGE FOLLOWER PULSE RESPONSE



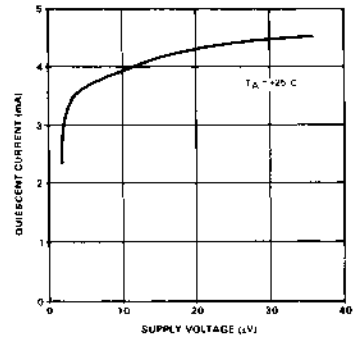
MAX UNDISTORTED OUTPUT VS FREQUENCY



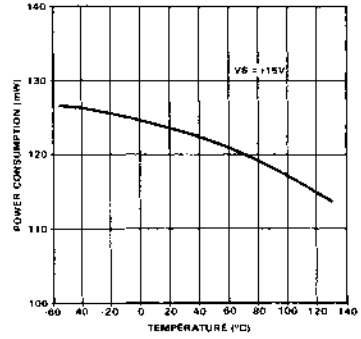
OUTPUT VOLTAGE VS LOAD RESISTANCE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



POWER CONSUMPTION VS TEMPERATURE



OP-10

DUAL MATCHED INSTRUMENTATION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-10 Series of Dual Matched Instrumentation Operational Amplifiers consists of two independent monolithic high performance operational amplifiers in a single 14-pin Dual-in-Line package. For the first time, extremely tight matching of critical parameters is provided between channels of a dual operational amplifier, whereas previous dual op amp designs have made no attempt towards matching.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels enables realization of extremely high performance instrumentation amplifier designs without resorting to laborious and expensive selection and matching of discrete amplifiers. The designer is assured of achieving the full performance guaranteed by the specification as the common package eliminates the unavoidable temperature differentials incurred by all designs utilizing separately housed amplifiers.

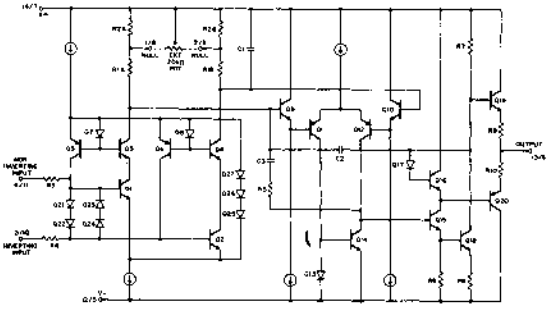
Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common mode and power supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current and are completely compensated and protected.

FEATURES

- Extremely Tight Matching
- Excellent Individual Amplifier Parameters
- Tight Offset Voltage Match . . . . . 0.18mV Max
- Tight Offset Voltage Match vs. Temp. . 0.8 $\mu V/^{\circ}C$ Max
- Tight Common Mode Rejection Match . . 114 dB Min
- Tight Power Supply Rejection Match . . . 100 dB Min
- Tight Bias Current Match. . . . . 2.8 nA Max
- Low Noise . . . . . 0.6 μVp-p Max
- Low Bias Current . . . . . 3.0 nA Max
- High Common Mode Input Impedance . . 200GΩ Typ
- High Channel Separation . . . . . 126 dB Min
- Internally Compensated. . . . . Easy to Use
- Compact . . . . . 14 Pin Dip Package

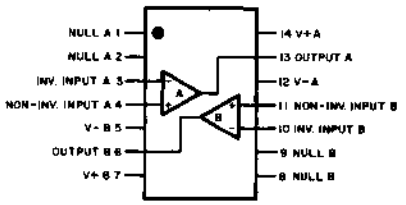
SIMPLIFIED SCHEMATIC

1/2 OP-10)



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



14 PIN CERAMIC DIP (Y-Suffix)

ORDER: OP-10AY OP-10EY
OP-10Y OP-10CY

NOTE: Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Storage Temperature Range	-65°C to +150°C
Internal Power Dissipation (Note 1)	500mW	Operating Temperature Range	
Differential Input Voltage	±30V	OP-10A, OP-10	-55°C to +125°C
Input Voltage (Note 2)	±22V	OP-10E, OP-10C	0°C to +70°C
Output Short Circuit Duration	Indefinite	Lead Temperature Range (Soldering, 60 sec)	300°C

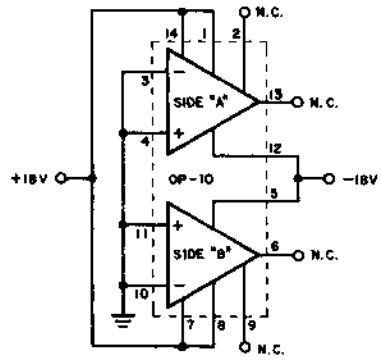
NOTES:

1: Maximum package power dissipation vs. ambient temperature.

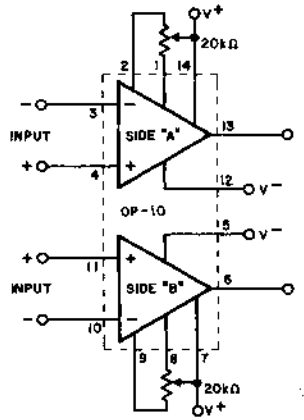
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
Dual-in-Line (Y)	106°C	11.3mW/°C

2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



MATCHING PARAMETER DEFINITIONS

INPUT OFFSET VOLTAGE MATCH (ΔV_{os}) The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$). In Fig. 1 if $V_{OSA} = V_{OSB}$, the net differential offset voltage at the output of the amplifier pair equals zero.

INPUT OFFSET VOLTAGE TRACKING ($TC\Delta V_{os}$) The ratio of the change in ΔV_{os} to the change in temperature producing it.

AVERAGE NON-INVERTING BIAS CURRENT (I_B^+) The average of the side A and side B non-inverting input bias currents;

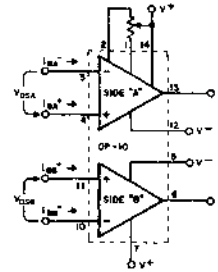
$$\frac{I_{BA}^{+} + I_{BB}^{+}}{2}$$

NON-INVERTING INPUT OFFSET CURRENT (I_{os}^+) The difference between the non-inverting input bias currents of side A and side B; ($I_{BA}^{+} - I_{BB}^{+}$).

INVERTING INPUT OFFSET CURRENT (I_{os}^-) The difference between the inverting input bias currents of side A and side B; ($I_{BA}^{-} - I_{BB}^{-}$).

AVERAGE DRIFT OF NON-INVERTING BIAS CURRENT (TCI_B^+) The ratio of the change in non-inverting bias current to the change in temperature producing it.

AVERAGE DRIFT OF NON-INVERTING OFFSET CURRENT (TCI_{os}^+) The ratio of the change in non-inverting offset current to the change in temperature producing it.



COMMON MODE REJECTION RATIO MATCH ($\Delta CMRR$) The difference between the common-mode rejection ratios (expressed in volt /volt) of side A and side B. $\Delta CMRR$ in dB = 20 $\log_{10}$ (Δ CMRR in volt/volt)

SUPPLY VOLTAGE REJECTION RATIO MATCH ($\Delta PSRR$) The difference between the power supply rejection ratios (expressed in volt /volt) of side A and side B. $\Delta PSRR$ in dB = 20 $\log_{10}$ (Δ PSRR in volt/volt)

CHANNEL SEPARATION The ratio of the change in input offset voltage of one channel to the change in output voltage in the second channel producing it.

SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual Matched Operational Amplifiers provide the engineer a powerful tool for the solution of a number of difficult circuit design problems including true instrumentation amplifiers, extremely low drift, high common mode rejection D.C. amplifiers, low D.C. drift active filters, dual tracking voltage references and many other demanding applications. These designs are based on the principle that careful matching between two operational amplifiers can, to a large extent, eliminate the effect of D.C. errors inherent in the individual amplifiers.

Reference to the circuit shown in Fig. 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical; if the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters – offset voltage, offset voltage drift, inverting and non-inverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential mode, are extremely high and can also be tightly matched, an important feature not possible with single operational amplifier circuits. Common mode rejection can be made exceptionally high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than those due to noise or drift with temperature. (For example, consider the case of two op amps, each with 80 dB (100μV/V) CMRR. However, if the CMRR of one device is +100μV/V while CMRR of the other is −100μV/V for a net 200μV/V CMRR match, the resultant input referred error over a 10V common-mode input signal will be 2mV.)

POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V− supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset trimming terminals are provided for each amplifier of the OP-10 – however, guaranteed performance over temperature can be obtained by trimming only one side (side A) to match the offset of the other for a net differential offset of zero. (See Fig. 1) This is due to the specific procedure used during factory testing of the devices; however, results which are essentially the same may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 is designed to provide lowest drift performance when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be considerably more than adequate for most applications. Where finer resolution of trimming is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the sensitivity to offset vs. potentiometer position may be reduced by using the circuit of Fig. 2.

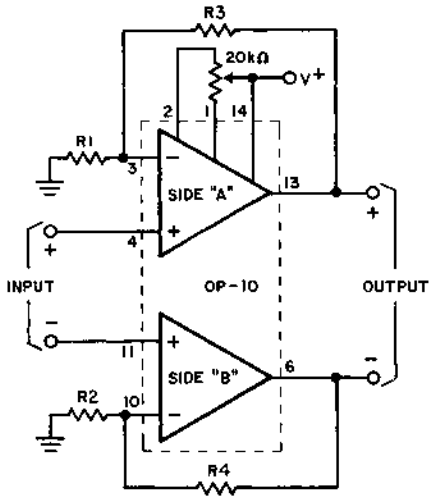


FIGURE 1

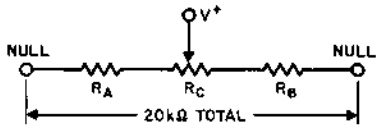


FIGURE 2

Model	Null Range	Fixed Resistors R_A, R_B	Potentiometer R_C
OP-10AY, OP-10Y, OP-10EY	±1.2mV	5.1kΩ	10.0kΩ

MATCHING CHARACTERISTICS			OP-10AY			OP-10Y			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage Match	ΔV_{os}		—	0.07	0.18	—	0.12	0.5	mV
Average Non-Inverting Bias Current	I_B^+		—	±1.0	±3.0	—	±1.3	±4.5	nA
Non-Inverting Offset Current	I_{os}^+		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	I_{os}^-		—	0.8	2.8	—	1.1	4.5	nA
Common Mode Rejection Ratio Match	$\Delta CMRR$	V_{CM} = ±CMVR	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	V_S = ±3V to ±18V	100	112	—	94	110	—	dB
Channel Separation			126	140	—	126	140	—	dB
These specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage Match	ΔV_{os}		—	0.10	0.30	—	0.20	0.90	mV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{os}$		—	0.45	1.3	—	0.9	2.5 (Note 1)	µV/°C
With External Trim	$TC\Delta V_{osn}$	Rp = 20kΩ Channel A only See Page 3.	—	0.3	0.8	—	0.4	1.2 (Note 1)	µV/°C
Average Non-Inverting Bias Current	I_B^+		—	±2.0	±6.0	—	±2.4	±8.0	nA
Average Drift of Non-Inverting Bias Current	TCI_B^+		—	10	40	—	15	—	pA/°C
Non-Inverting Offset Current	I_{os}^+		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Non-Inverting Offset Current	TCI_{os}^+		—	12	50	—	18	—	pA/°C
Inverting Offset Current	I_{os}^-		—	2.0	6.5	—	2.4	9.0	nA
Common Mode Rejection Ratio Match	$\Delta CMRR$	V_{CM} = ±CMVR	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	V_S = ±3V to ±18V	94	105	—	90	103	—	dB

NOTE 1: Parameter not 100% tested; 90% of all units meet these specifications

INDIVIDUAL AMPLIFIER CHARACTERISTICS			OP-10AY			OP-10Y			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}		--	0.2	0.5	--	0.2	0.5	mV
Input Offset Voltage Stability	V_{os}/Time	(Note 1)	--	2.5	9	--	2.5	9	µV/Mo
Input Offset Current	I_{os}		--	1.0	2.8	--	1.0	2.8	nA
Input Bias Current	I_B		--	±1.0	±3.0		±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	--	0.35	0.6	--	0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2) f_o = 100Hz (Note 2) f_o = 1000Hz (Note 2)	-- -- --	10.3 10.0 9.6	18.0 13.0 11.0	-- -- --	10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	--	14	30	--	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz (Note 2) fo = 100Hz (Note 2) fo = 1000Hz (Note 2)	-- -- --	0.32 0.14 0.12	0.80 0.23 0.17	-- -- --	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance - Differential Mode	R_{in}		20	60	--	20	60	--	MΩ
Input Resistance - Common Mode	R_{inCM}		--	200	--	--	200	--	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	--	±13.0	±14.0	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	126	--	110	126	--	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	110	--	100	110	--	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±.5V V_S = ±3V	200 150	500 500	-- --	200 150	500 500	-- --	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	-- -- --	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	-- -- --	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	--	0.17	--	--	0.17	--	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	--	0.6	--	--	0.6	--	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	--	60	--	--	60	--	Ω
Power Consumption	Pd	 V_S = ±3V	-- --	90 4	120 6	-- --	90 4	120 6	mW
Offset Adjustment Range		R_p = 20kΩ	--	±4	--	--	±4	--	mV
Input Capacitance	C_{in}		--	8	--	--	8	--	pF
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{os}		--	0.3	0.7	--	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{os} TCV_{osn}	 R_p = 20kΩ	 -- --	 0.7 0.3	 2.0 1.0	 -- --	 0.7 0.3	 2.0 (Note 2) 1.0 (Note 2)	 µV/°C µV/°C
Input Offset Current	I_{os}		--	1.8	5.6	--	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{os}		--	8	50	--	8	50	pA/°C
Input Bias Current	I_B		--	+2.0	±6.0	--	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		--	13	50		13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	--	±13.0	±13.5	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	--	106	123	--	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	106	--	94	106	--	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	150	400	--	150	400	--	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±12.0	±12.6	--	+12.0	±12.6	--	V

NOTE 1: Exclude first hour of operation to allow for stabilization of external circuitry. Parameter is not 100% tested; 90% of all units meet this specification.

NOTE 2: Parameter is not 100% tested; 90% of all units meet these specifications.

MATCHING CHARACTERISTICS			OP-10EY			OP-10CY			
These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage Match	ΔV_{os}		—	0.12	0.5	—	0.3	—	mV
Average Non-Inverting Bias Current	I_B+		—	±1.3	±4.5	—	±2.0	—	nA
Non-Inverting Offset Current	$I_{os}+$		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	$I_{os}-$		—	1.1	4.5	—	1.8	—	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm CMVR$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_s = \pm 3V$ to $\pm 18V$	94	110	—	—	106	—	dB
Channel Separation			126	140	—	120	137	—	dB
These specifications apply for $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.									
Input Offset Voltage Match	ΔV_{os}		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{os}$		—	0.9	2.3 (Note 1)	—	1.3	—	µV/°C
With External Trim	$TC\Delta V_{osn}$	Rp = 20kΩ Channel A only See Page 3	—	0.3	0.9	—	0.6	—	µV/°C
Average Non-Inverting Bias Current	I_B+		—	±2.0	±6.0	—	±2.8	—	nA
Average Drift of Non-Inverting Bias Current	TCI_B+		—	12	40 (Note 1)	—	18	—	pA/°C
Non-Inverting Offset Current	$I_{os}+$		—	2.0	6.0	—	2.8	—	nA
Average Drift of Non-Inverting Offset Current	$TCI_{os}+$		—	15	50 (Note 1)	—	20	—	pA/°C
Inverting Offset Current	$I_{os}-$		—	2.0	6.0	—	2.8	—	nA
Common Mode Rejection Ratio Match	ΔCMRR		103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR		90	105	—	—	102	—	dB

NOTE 1: Parameter not 100% tested; 90% of all units meet these specifications.

INDIVIDUAL AMPLIFIER CHARACTERISTICS			OP-10EY			OP-10CY			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}		--	0.2	0.5	--	0.3	1.3	mV
Input Offset Voltage Stability	V_{os}/Time	(Note 1)	--	2.5	9	--	3.5	--	µV/Mo
Input Offset Current	I_{os}		--	1.2	3.8	--	1.8	6.0	nA
Input Bias Current	I_B		--	±1.2	±4.0	--	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	--	0.35	0.6	--	0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	--	10.3	18.0	--	10.5	20.0	nV/√Hz
		f_o = 100Hz (Note 2)	--	10.0	13.0	--	10.2	13.5	
		f_o = 1000Hz (Note 2)	--	9.6	11.0	--	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	--	14	30	--	15	35	pAp-p
Input Noise Current Density	i_n	f_o = 10Hz (Note 2)	--	0.32	0.80	--	0.35	0.90	pA/√Hz
		f_o = 100Hz (Note 2)	--	0.14	0.23	--	0.15	0.27	
		f_o = 1000Hz (Note 2)	--	0.12	0.17	--	0.13	0.18	
Input Resistance – Differential Mode	R_{in}		15	50	--	8	33	--	MΩ
Input Resistance – Common Mode	R_{inCM}		--	160	--	--	120	--	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	--	±13.0	±14.0	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ± CMVR	106	123	--	100	120	--	dB
Power Supply Rejection Ratio	PSRR	V_S = ± 3V to ± 18V	94	107	--	90	104	--	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_O = ± 10V	200	500	--	120	400	--	V/mV
		$R_L \geq 500\Omega$, V_O = ± 5V, V_S = ± 3V	150	500	--	100	400	--	
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$	±12.5	±13.0	--	±12.0	±13.0	--	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	--	±11.5	±12.8	--	
		$R_L \geq 1k\Omega$	±10.5	±12.0	--	--	±12.0	--	
Slewing Rate	SR	$R_L \geq 2k\Omega$	--	0.17	--	--	0.17	--	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	--	0.6	--	--	0.6	--	MHz
Open Loop Output Resistance	R_o	V_O = 0, I_O = 0	--	60	--	--	60	--	Ω
Power Consumption	P_d		--	90	120	--	96	150	mW
		V_S = ± 3V	--	4	6	--	4	8	
Offset Adjustment Range		R_p = 20kΩ	--	±4	--	--	±4	--	mV
Input Capacitance	C_{in}		--		--	--	8	--	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}		--	0.25	0.6	--	0.35	1.6	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{os}	(Note 2)	--	0.7	2.0	--	1.2	4.5	µV/°C
With External Trim	TCV_{osn}	R_p = 20kΩ (Note 2)	--	0.3	1.0	--	0.4	1.5	
Input Offset Current	I_{os}		--	1.4	5.3	--	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{os}	(Note 2)	--	8	35	--	12	50	pA/°C
Input Bias Current	I_B		--	±1.5	±5.5	--	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	--	13	35	--	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	--	±13.0	±13.5	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ± CMVR	103	123	--	97	120	--	dB
Power Supply Rejection Ratio	PSRR	V_S = ± 3V to ± 18V	90	104	--	86	100	--	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_O = ± 10V	180	450	--	100	400	--	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$,	±12.0	±12.6	--	±11.0	±12.6	--	V

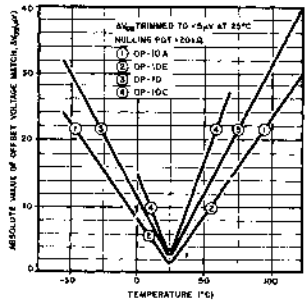
NOTE 1: Exclude first hour of operation to allow for stabilization of external circuitry. Parameter is not 100% tested; 90% of all units meet this specification.

NOTE 2: Parameter is not 100% tested; 90% of all units meet these specifications.

TYPICAL PERFORMANCE CURVES

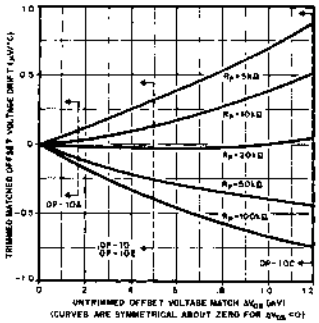
MATCHING CHARACTERISTIC

TRIMMED OFFSET VOLTAGE MATCH VS TEMPERATURE



MATCHING CHARACTERISTIC

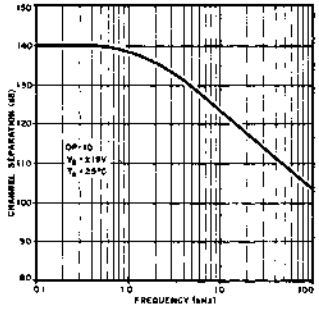
TRIMMED MATCHED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POT (R_P) SIZE AND ΔV_{OS}



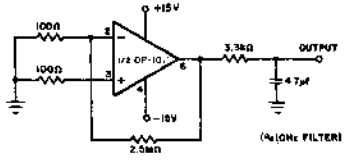
(CURVES ARE SYMMETRICAL ABOUT ZERO FOR ΔV_{OS} <0)

MATCHING CHARACTERISTIC

CHANNEL SEPARATION VS FREQUENCY



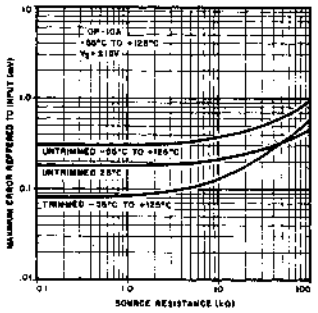
LOW FREQUENCY NOISE TEST CIRCUIT



INPUT REFERRED NOISE = $\frac{V_O}{25,000} = \frac{5mV/cm}{25,000} = 200nV/cm$

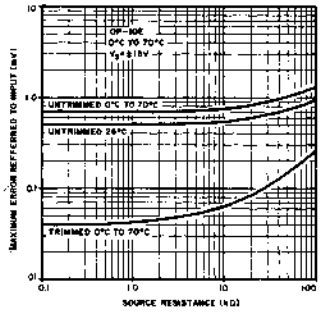
MATCHING CHARACTERISTIC

MAXIMUM INPUT ERROR VS SOURCE RESISTANCE

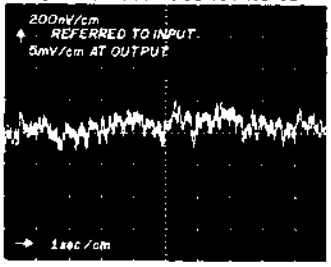


MATCHING CHARACTERISTIC

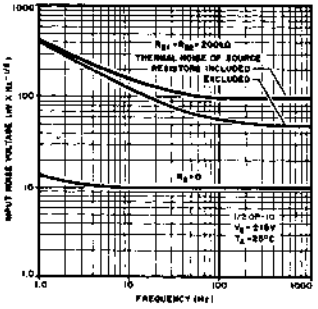
MAXIMUM INPUT ERROR VS SOURCE RESISTANCE



OP-10 LOW FREQUENCY NOISE

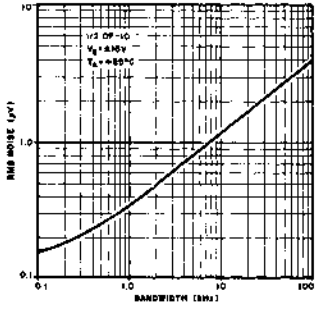


TOTAL INPUT NOISE VOLTAGE VS FREQUENCY

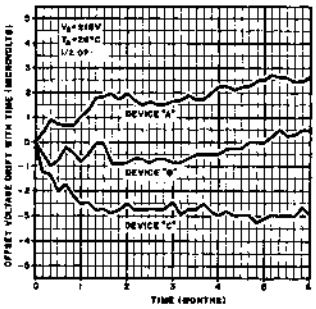


INPUT WIDEBAND NOISE VS BANDWIDTH

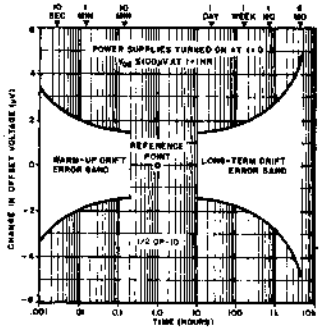
(.1Hz TO FREQUENCY INDICATED)



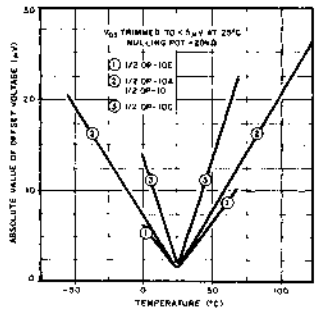
TYPICAL OFFSET VOLTAGE STABILITY VS TIME



OFFSET VOLTAGE DRIFT WITH TIME

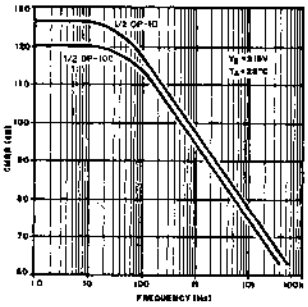


TRIMMED OFFSET VOLTAGE VS TEMPERATURE

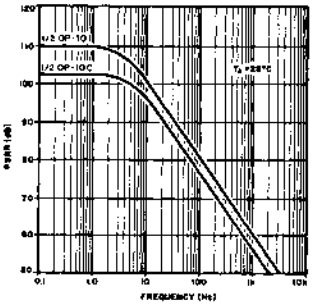


TYPICAL PERFORMANCE CURVES

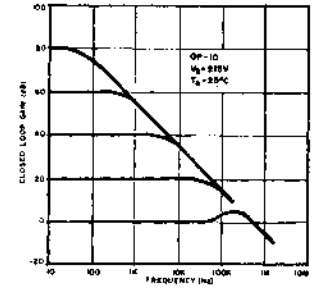
CMRR VS FREQUENCY



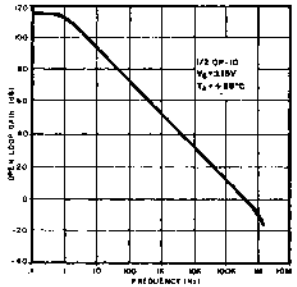
PSRR VS FREQUENCY



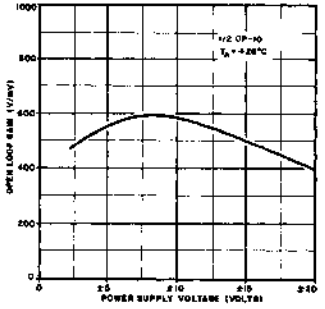
CLOSED LOOP RESPONSE
FOR VARIOUS GAIN CONFIGURATIONS



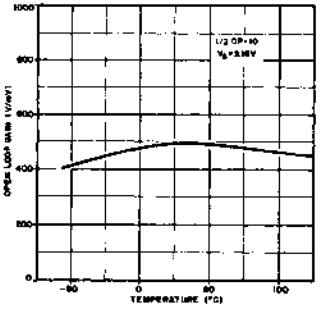
OPEN LOOP FREQUENCY RESPONSE



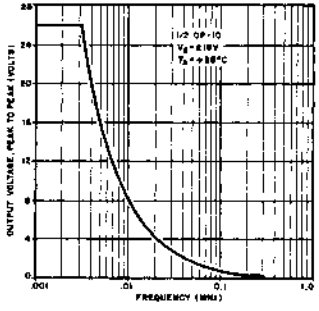
OPEN LOOP GAIN VS POWER
SUPPLY VOLTAGE



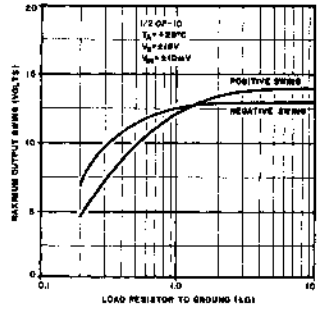
OPEN LOOP GAIN VS TEMPERATURE



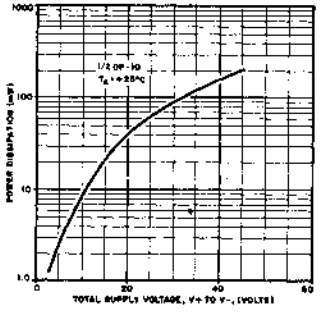
MAXIMUM UNDISTORTED OUTPUT
VS FREQUENCY



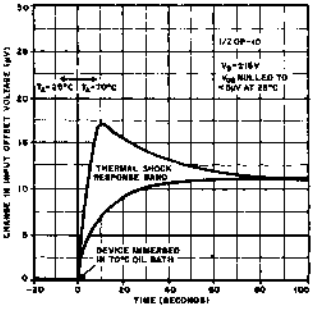
OUTPUT SWING VS LOAD



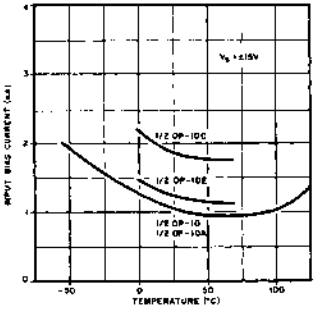
POWER CONSUMPTION VS
POWER SUPPLY



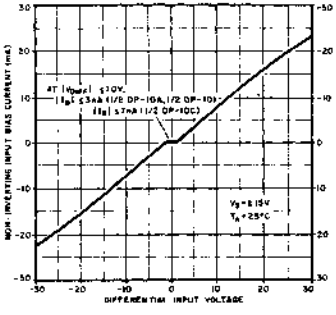
OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



INPUT BIAS CURRENT VS
TEMPERATURE

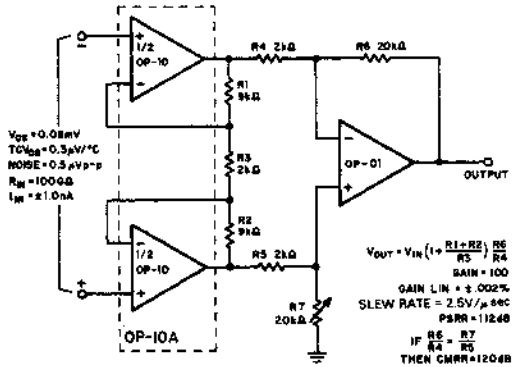


INPUT BIAS CURRENT VS
DIFFERENTIAL INPUT VOLTAGE



APPLICATIONS INFORMATION

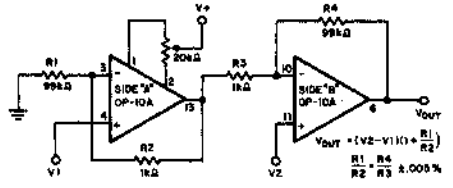
TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER



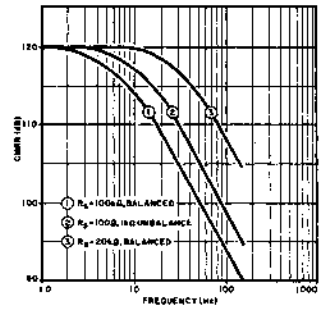
INSTRUMENTATION AMPLIFIERS USING OP-10

Instrumentation Amplifiers with performance surpassing those costing many hundreds of dollars can be easily and compactly built using the OP-10. Typical performance for a 2 and 3-amplifier design are given in the table. The 3-amplifier design, while more complex, has the advantages of convenient overall gain adjustment by trimming a single resistor (R_3) and of wide common-mode voltage handling capability at any overall gain, plus improved gain linearity. Slew rate, small signal bandwidth and full power bandwidth are also superior and may be further improved by choosing a high-speed op-amp such as the OP-01 series for the output op-amp.

INSTRUMENTATION AMPLIFIER 2 OP-AMP DESIGN



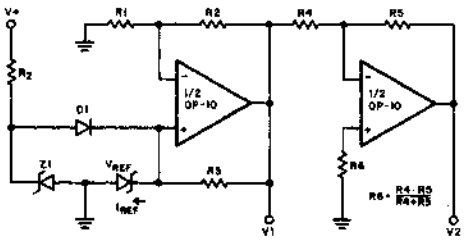
CMRR VS FREQUENCY
INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)



TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS
GAIN = 100

PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	.004%	.001% (OP-05) .002% (OP-01)
Initial Input Offset Voltage	70μV	75μV
vs. Temp (amplifier A nulled with 20K pot)	0.3μV/°C	0.3μV/°C
vs. Time	3.5μV/month	3.5μV/month
Input Bias Current	±1.0nA	±1.0nA
vs. Temp.	10pA/°C	10pA/°C
Input Offset Current	0.8nA	0.8nA
vs. Temp.	12pA/°C	12pA/°C
Input Impedance		
Differential	80GΩ	100GΩ
Common Mode	100GΩ	100GΩ
Input Noise Voltage (.1 to 10Hz)	0.5μV p-p	0.5μV p-p
Input Noise Current (.1 to 10Hz)	14pA p-p	14pA p-p
Common Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small Signal (−3dB)	6.0kHz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5kHz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	.17V/μs	0.17 V/μsec (OP-05) 4.0 V/μsec (OP-01)

PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10



Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs temperature and time and have excellent power supply rejection.

In the circuit shown, R_3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z, Z_1, and D_1.

$V_{Z1} \leq V_{REF} + 2.0V$ $\qquad$ $V1 = V_{REF}\left(1+\frac{R2}{R1}\right)$

$I_{REF} = (V1 - V_{REF})/R3$ $\qquad$ $V2 = V1\left(\frac{-R5}{R4}\right)$

Output Impedance (ΔI_L: 1.0mA − 5.0mA) . . . . . $0.25 \cdot 10^{-3}\Omega$

OP-11

QUAD MATCHED 741-TYPE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-11 provides four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148 and LM348 amplifiers. The amplifiers are matched for common mode rejection ratio and offset voltage. These parameters are very important in the design of instrumentation amplifiers. In addition the amplifier is designed to have equal positive-going and negative-going slew rates. This is a very important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift and excellent long term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost.

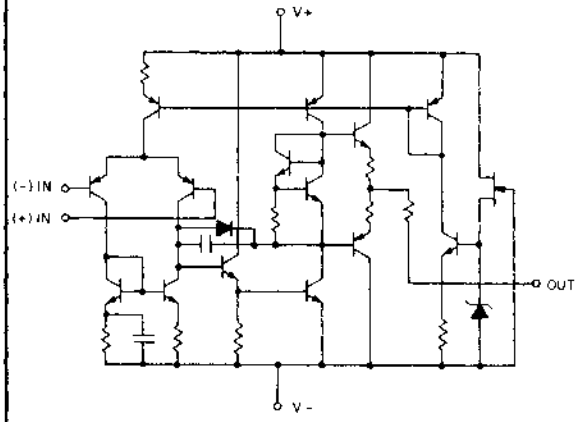
FEATURES

- Guaranteed V_{OS} . . . . . 500μ V MAX.
- Guaranteed Matched CMRR . . . . . 94 dB MIN.
- Guaranteed Matched V_{OS} . . . . . 750 μV MAX.
- LM148/LM348 Direct Replacements
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short Circuit Protection
- Low Input Bias Current

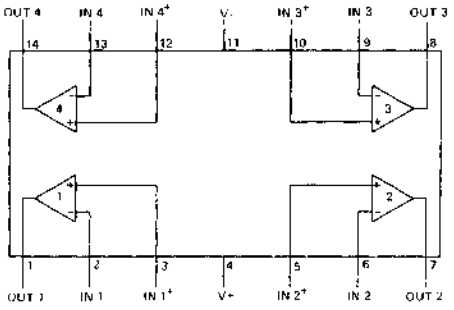
The OP-11 is ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance. OP-11's with processing per the requirements of MIL-STD-883A are available. For dual-741-type versions, see the OP-04 and OP-14 data sheets.

EQUIVALENT SCHEMATIC

(1/4 CIRCUIT SHOWN)



PIN CONNECTIONS



TOP VIEW

ORDERING INFORMATION

ORDER: OP-11AY, OP-11BY] –55°C TO +125°C
ORDER: OP-11EY, OP-11FY] 0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP11-883-AY
OP11-883-BY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous (One Amplifier Only)
Storage Temperature Range	−65° to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

OP-11A, OP-11B	−55°C to +125°C
OP-11E, OP-11F	0°C to +70°C

Note 1: Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14 Pin DIP (Y)	80°C	10 mW/°C

MATCHING CHARACTERISTICS

	OP-11A OP-11E			OP-11B OP-11F			

These specifications apply for V_S = ±15V, T_A = 25°C, $R_S \leq 100\Omega$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage Match	ΔV_{OS}	(Note 4)	–	0.5	0.75	–	0.8	2.0	mV
Common Mode Rejection Ratio Match (Note 3)	ΔCMRR	V_{CM} = ±CMVR	– 94	1.0 120	20 –	– 94	1.0 120	20 –	µV/V dB

These specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C for OP-11A and OP-11B, 0°C ≤ T_A ≤ +70°C for OP-11E and OP-11F $R_S \leq 100\Omega$ unless otherwise noted.

Input Offset Voltage Match	ΔV_{OS}	(Note 4)	–	0.6	1.0	–	1.0	2.5	mV
Common Mode Rejection Ratio Match (Note 3)	ΔCMRR	V_{CM} = ±CMVR	– 94	3.2 110	20 –	– 94	3.2 110	20 –	µV/V dB

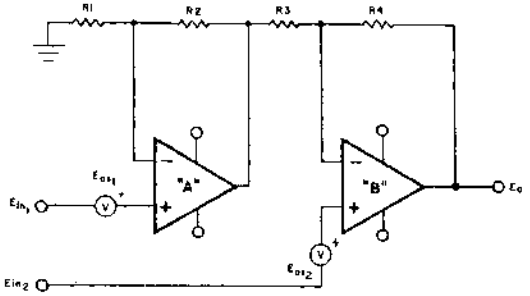
MATCHING PARAMETER DEFINITIONS

COMMON MODE REJECTION RATIO MATCH (ΔCMRR). The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. ΔCMRR in dB = $-20 \log_{10}$ (ΔCMRR in volt/volt). See note 3.

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$). See note 4.

TYPICAL APPLICATION

INSTRUMENTATION AMPLIFIER 2 OP-AMP DESIGN



GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$1)\ E_o = -\left[E_{in1}\left(+1\ \frac{R_2}{R_1}\right)\ \frac{R_4}{R_3}\right] + E_{in2}\left(\frac{R_4}{R_3} + 1\right)$$

With ideal resistors this simplifies to:

$$2)\ E_o = \left(E_{in2} - E_{in1}\right)\left(\frac{R_4}{R_3} + 1\right) \text{ provided } \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

COMMON MODE REJECTION

Because the dual op amp has a high common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching. This device eliminates the need for special op amp selections in many instrumentation amplifier applications.

DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage (E_{OS2}–E_{OS1}) will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected.

ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-11A			OP-11B			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.30	0.50	–	0.60	2.5	mV
Input Offset Current	I_{OS}		–	8.0	20	–	25	50	nA
Input Bias Current	I_B		–	180	300	–	300	500	nA
Input Resistance Differential Mode	R_{in}		0.20	0.40	–	0.20	0.40	–	MΩ
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	100	650	–	100	650	–	V/mV
Power Consumption (Note 2)	P_d	V_O = 0V	–	123	180	–	123	180	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.7	–	–	0.7	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	18 14 12	– – –	– – –	18 14 12	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	17	–	–	17	–	pA p-p
Channel Separation	CS		100	130	–	100	130	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.8 1.5 1.2	– – –	– – –	1.8 1.5 1.2	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.70	1.0	–	0.70	1.0	–	V/µs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	11	16	–	11	16	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	1.5	2.0	–	1.5	2.0	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	80	120	–	80	120	nsec
Overshoot (Note 1)			–	15	25	–	15	25	%
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.40	1.0	–	1.0	3.5	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 10k\Omega$	–	2.0	10	–	4.0	15	µV/°C
Input Offset Current	I_{OS}		–	20	40	–	40	80	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.10	0.30	–	0.30	0.60	nA/°C
Input Bias Current	I_B		–	200	375	–	400	650	nA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	100	250	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Power Consumption (Note 2)	P_d	V_O = 0V	–	115	200	–	115	200	mW

NOTE 1: Parameter is not 100% tested. 90% of all units meet these specifications.

NOTE 2: Total dissipation for all 4 amplifiers in package.

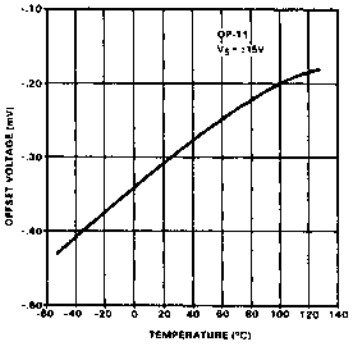
NOTE 3: Match exists between any two amplifiers.

NOTE 4: Using amplifier 1 as reference then $\Delta V_{OS} = V_{OSn} - V_{OS1}$.

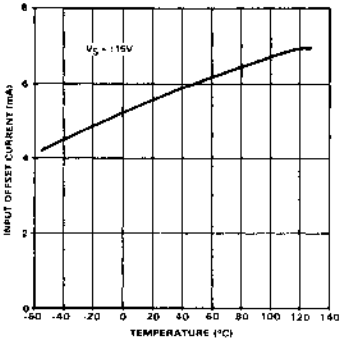
ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-11E			OP-11F			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_S \leq 10k\Omega$	–	0.30	0.50	–	0.60	2.5	mV
Input Offset Current	I_{os}		–	8.0	20	–	25	50	nA
Input Bias Current	I_B		–	180	300	–	300	500	nA
Input Resistance Differential Mode	R_{in}		0.20	0.40	–	0.20	0.40	–	MΩ
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	650	–	100	650	–	V/mV
Power Consumption (Note 2)	P_d	V_O = 0V	–	123	180	–	123	180	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.7	–	–	0.7	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	18 14 12	– – –	– – –	18 14 12	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	17	–	–	17	–	pA p-p
Channel Separation	CS		100	130	–	100	130	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.8 1.5 1.2	– – –	– – –	1.8 1.5 1.2	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.70	1.0	–	0.70	1.0	–	V/µs
Large Signal Bandwidth (Note 1)		V_O = 20Vp-p	11	16	–	11	16	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	1.5	2.0	–	1.5	2.0	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	80	120	–	80	120	nsec
Overshoot (Note 1)			–	15	25	–	15	25	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_S \leq 10k\Omega$	–	0.40	0.80	–	0.80	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_S \leq 10k\Omega$	–	2.0	10	–	4.0	15	µV/°C
Input Offset Current	I_{os}		–	20	30	–	40	60	nA
Average Input Offset Current Drift	TCI_{os}		–	0.10	0.30	–	0.30	0.60	nA/°C
Input Bias Current	I_B		–	200	350	–	400	550	nA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	250	–	100	250	–	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Power Consumption (Note 2)	P_d	V_O = 0V	–	115	200	–	115	200	mW

TYPICAL PERFORMANCE CURVES

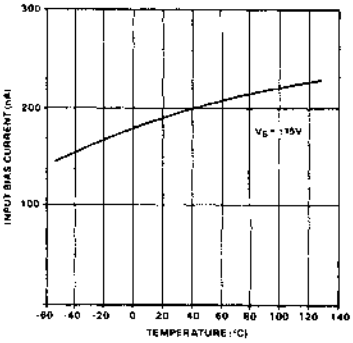
OFFSET VOLTAGE VS TEMPERATURE



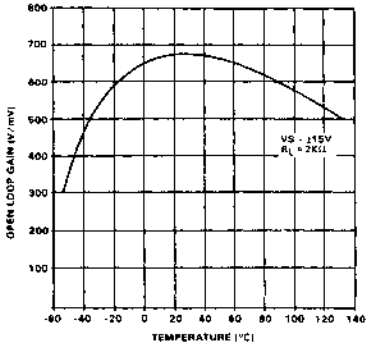
OFFSET CURRENT VS TEMPERATURE



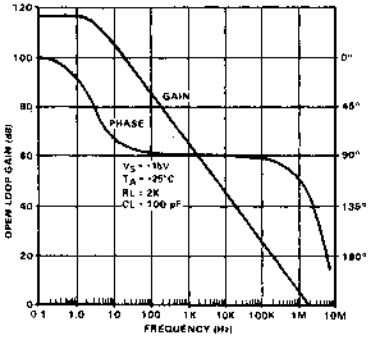
BIAS CURRENT VS TEMPERATURE



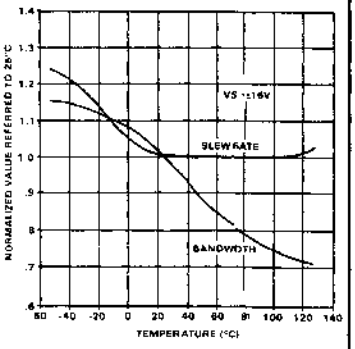
OPEN LOOP GAIN VS TEMPERATURE



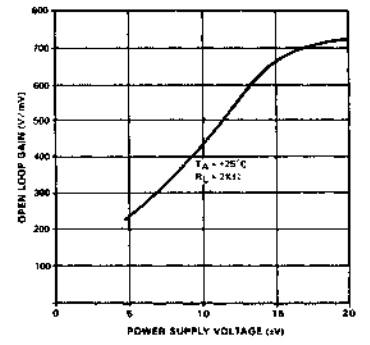
OPEN LOOP FREQUENCY & PHASE RESPONSE



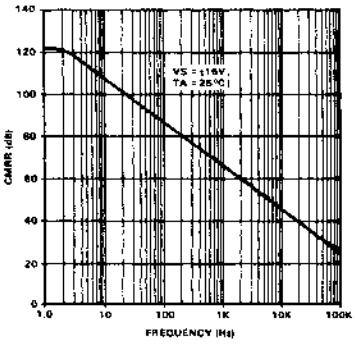
NORMALIZED A/C PARAMETERS VS TEMPERATURE



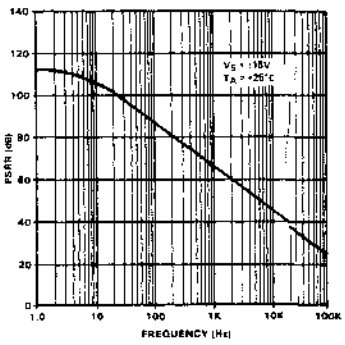
OPEN LOOP GAIN VS SUPPLY VOLTAGE



CMRR VS FREQUENCY

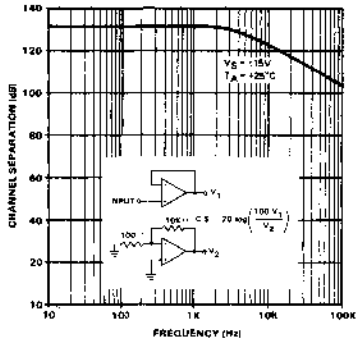


PSRR VS FREQUENCY

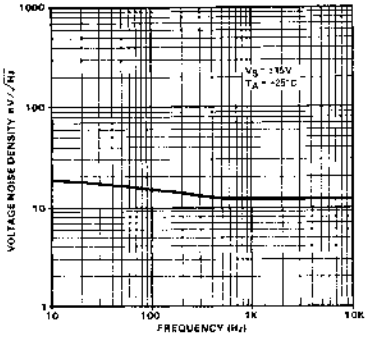


TYPICAL PERFORMANCE CURVES

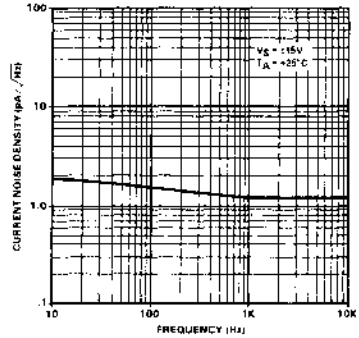
CHANNEL SEPARATION VS FREQUENCY



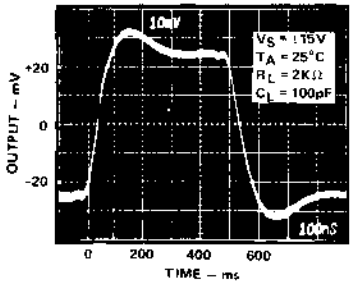
SPOT NOISE VOLTAGE VS FREQUENCY



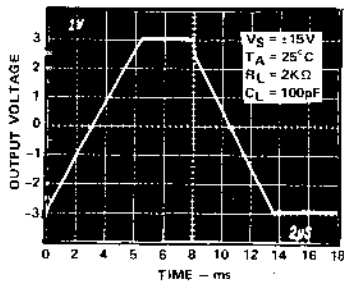
SPOT NOISE CURRENT VS FREQUENCY



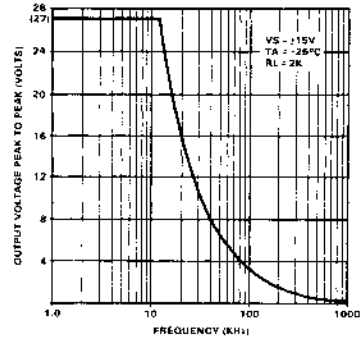
TRANSIENT RESPONSE



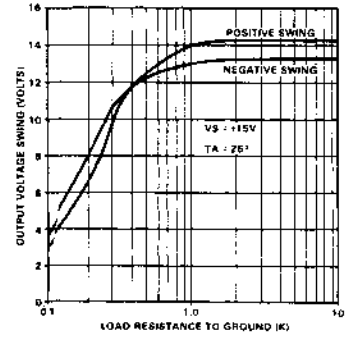
VOLTAGE FOLLOWER PULSE RESPONSE



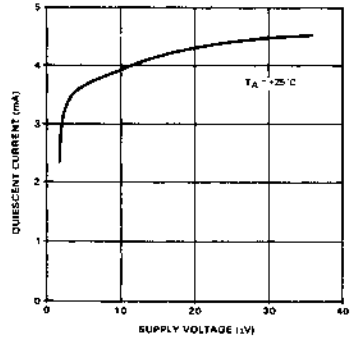
MAX UNDISTORTED OUTPUT VS FREQUENCY



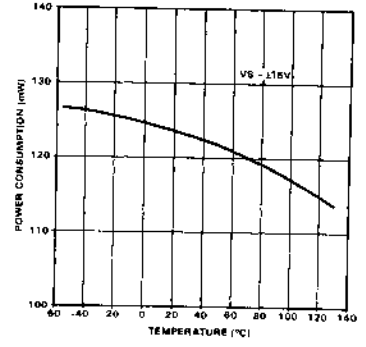
OUTPUT VOLTAGE VS LOAD RESISTANCE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



POWER CONSUMPTION VS TEMPERATURE



OP-12

PRECISION LOW INPUT CURRENT OP AMP

INTERNALLY COMPENSATED

GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 x 58 mils. Additionally, the OP-12 has a three times lower offset voltage and a two times lower offset voltage drift. The total worst case input offset voltage over −55°C to +125°C for the OP-12 is only 350μV while the 108A has 900μV to 1000μV for these conditions. In addition the OP-12 drives a 2kΩ load. This is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications

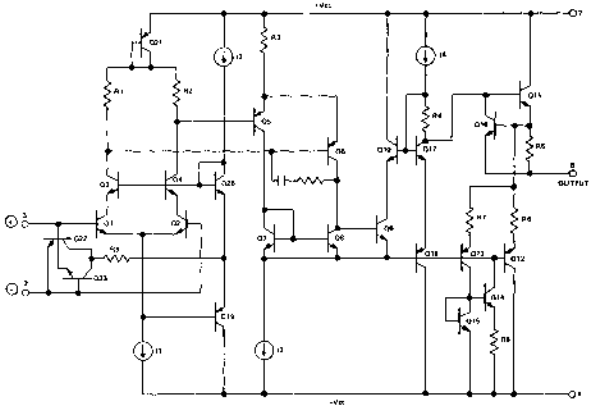
FEATURES

- Low Offset Voltage . . . . . 150μV Max.
- Low Offset Voltage Drift . . . . . 2.5μV/°C Max.
- Five Times PM108A Load Current . . . . . 5 mA Min.
- Internal Frequency Compensation

Plus the Outstanding PM108A Features

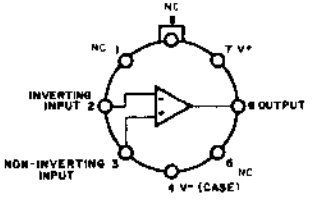
- Low Offset Current . . . . . 200 pA Max.
- Low Bias Current . . . . . 2.0 nA Max.
- Low Power Consumption . . . . 18 mW max. @ ±15V
- High Common Mode Input Range . . . . ±13.5V Min.
- MIL-STD-883A Class B Processing Available
- Silicon-Nitride Passivation

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: OP-12AJ
OP-12BJ
OP-12CJ
OP-12EJ
OP-12FJ
OP-12GJ

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP12-883-AJ
OP12-883-BJ
OP12-883-CJ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
OP-12A, OP-12B, OP-12C	±20V
OP-12E, OP-12F, OP-12G	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
OP-12A, OP-12B, OP-12C	-55°C to +125°C
OP-12E, OP-12F, OP-12G	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

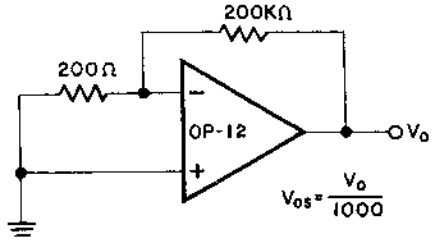
NOTE 1: Maximum package power dissipation vs. ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C

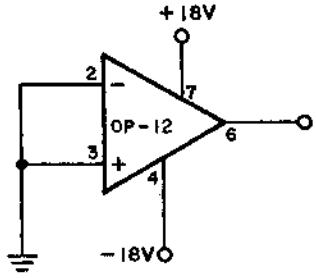
NOTE 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.

NOTE 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

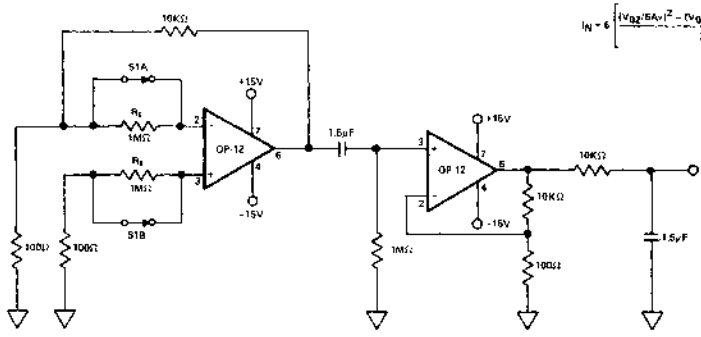
OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



LOW FREQUENCY NOISE TEST CIRCUIT (0.1 TO 10 Hz)



NOTES: 1. S1 CLOSED MEASURES e_n (V_{O1}).
2. S1 OPEN MEASURES e_n AND i_n (V_{O2}). i_n IS COMPUTED FROM THE TWO MEASUREMENTS.
3. SEE NOISE PHOTO OF e_n IN TYPICAL PERFORMANCE CURVES.

ELECTRICAL CHARACTERISTICS			OP-12A			OP-12B			OP-12C			

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}		–	0.07	0.15	–	0.18	0.30	–	0.25	1.0	mV
Input Offset Current	I_{OS}		–	0.05	0.20	–	0.05	0.20	–	0.08	0.50	nA
Input Bias Current	I_B		–	0.80	2.0	–	0.80	2.0	–	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.9	–	–	0.9	–	–	0.9	–	µV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	22 21 20	– – –	– – –	22 21 20	– – –	– – –	22 21 20	– – –	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	3	–	–	3	–	–	3	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	$pA/\sqrt{Hz}$
Input Resistance – Differential Mode	R_{in}		26	70	–	26	70	–	10	50	–	MΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	104	120	–	104	120	–	84	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	104	120	–	104	120	–	84	116	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq$ 10KΩ, V_O = ±10V $R_L \geq$ 2KΩ, V_O = ±10V	80 50	300 150	– –	80 50	300 150	– –	40 –	250 100	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq$ 10KΩ $R_L \geq$ 2KΩ	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Slewing Rate	SR	$R_L \geq$ 2KΩ	–	0.12	–	–	0.12	–	–	0.12	–	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.80	–	–	0.80	–	–	0.80	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	200	–	–	200	–	–	200	–	Ω
Power Consumption	Pd	V_S = ± 15V V_S = ±5V	– –	9 3	18 6	– –	9 3	18 6	– –	12 4	24 8	mW

The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.12	0.35	–	0.28	0.60	–	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	–	1.0	3.5	–	1.5	10	µV/°C
Input Offset Current	I_{os}		–	0.12	0.40	–	0.12	0.40	–	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	–	0.50	2.5	–	1.0	5.0	pA/°C
Input Bias Current	I_B		–	1.2	3.0	–	1.2	3.0	–	1.8	10	nA
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	100	110	–	100	110	–	80	106	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	100	110	–	100	110	–	80	106	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq$ 5KΩ, V_O = ±10V	40	120	–	40	120	–	15	80	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq$ 10KΩ $R_L \geq$ 5KΩ	±13.0 ±10.0	±14.0 ±13.0	– –	±13.0 ±10.0	±14.0 ±13.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Power Consumption	Pd		–	9	18	–	9	18	–	15	24	mW

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

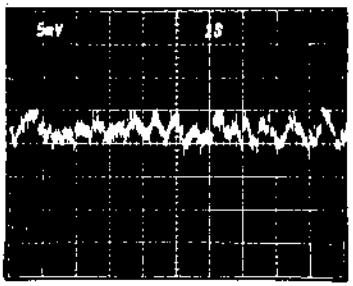
Parameter	Symbol	Test Conditions	OP-12E Min	OP-12E Typ	OP-12E Max	OP-12F Min	OP-12F Typ	OP-12F Max	OP-12G Min	OP-12G Typ	OP-12G Max	Units
Input Offset Voltage	V_{OS}		–	0.07	0.15	–	0.18	0.30	–	0.25	1.0	mV
Input Offset Current	I_{OS}		–	0.05	0.20	–	0.07	0.40	–	0.08	0.50	nA
Input Bias Current	I_B		–	0.80	2.0	–	0.90	4.0	–	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.9	–	–	0.9	–	–	0.9	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	22 21 20	– – –	– – –	22 21 20	– – –	– – –	22 21 20	– – –	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	3	–	–	3	–	–	3	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{in}		26	70	–	13	60	–	10	50	–	MΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	104	120	–	102	120	–	84	116	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	104	120	–	102	120	–	84	116	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10K\Omega$, $V_O = \pm 10V$ $R_L \geq 2K\Omega$, $V_O = \pm 10V$	80 50	300 150	– –	80 30	300 120	– –	40 –	250 100	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Slewing Rate	SR	$R_L \geq 2K\Omega$	–	0.12	–	–	0.12	–	–	0.12	–	V/μsec
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	–	0.80	–	–	0.80	–	–	0.80	–	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	–	200	–	–	200	–	–	200	–	Ω
Power Consumption	Pd	$V_S = \pm 15V$ $V_S = \pm 5V$	– –	9 3	18 6	– –	9 3	18 6	– –	12 4	24 8	mW

The following specifications apply for $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.10	0.26	–	0.23	0.45	–	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	–	1.0	3.5	–	1.5	10	μV/°C
Input Offset Current	I_{OS}		–	0.08	0.30	–	0.11	0.60	–	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	–	1.0	5.0	–	1.0	5.0	pA/°C
Input Bias Current	I_B		–	1.0	2.6	–	1.2	5.2	–	1.4	6.5	nA
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	–	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	100	116	–	100	116	–	80	112	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	100	116	–	100	116	–	80	112	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, $V_O = \pm 10V$ $R_L \geq 10K\Omega$, $V_O = \pm 10V$	25 60	100 200	– –	15 60	100 200	– –	– 25	80 150	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Power Consumption	P_D		–	9	18	–	9	18	–	15	24	mW

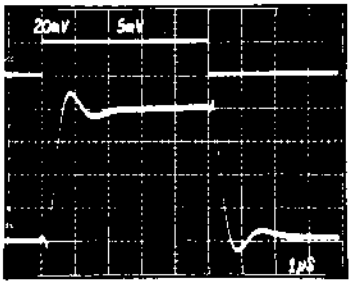
TYPICAL PERFORMANCE CURVES

LOW FREQUENCY NOISE

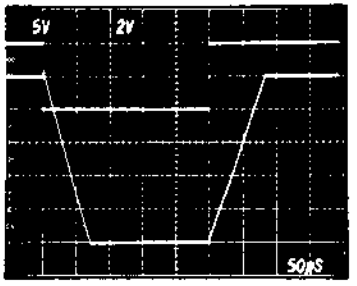


R_S = 0, BW = 0.1Hz to 10Hz
5 mV/div AT OUTPUT
0.5 µV/div REFERRED TO INPUT

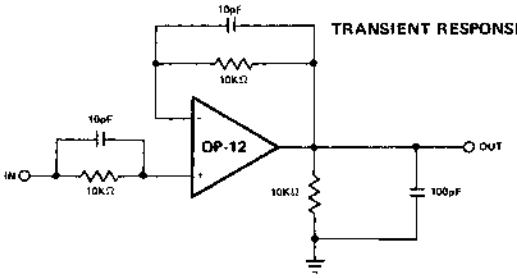
SMALL SIGNAL TRANSIENT RESPONSE



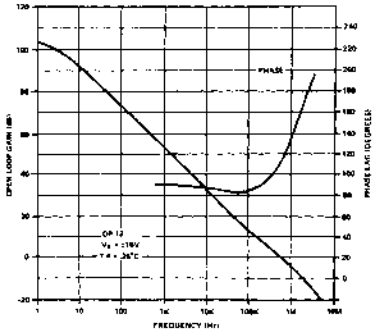
LARGE SIGNAL TRANSIENT RESPONSE



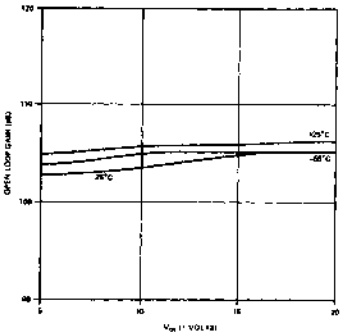
TRANSIENT RESPONSE TEST CIRCUIT



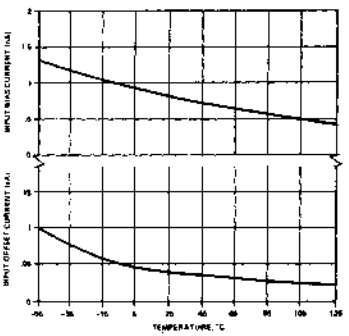
OPEN LOOP GAIN (A_{VO}) AND PHASE VS. FREQUENCY



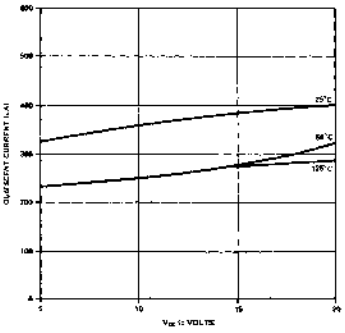
OPEN LOOP GAIN (Avo) VS. SUPPLY VOLTAGE (Vcc) WITH TEMPERATURE AS A PARAMETER



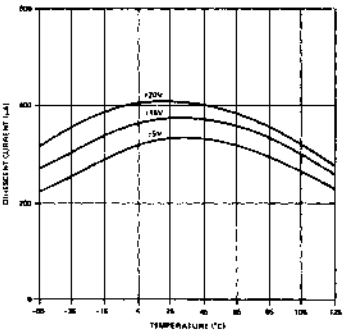
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VS. TEMPERATURE



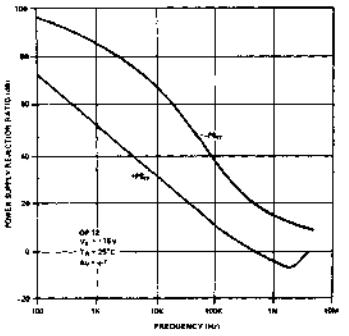
QUIESCENT CURRENT (ISY) VS. SUPPLY VOLTAGE WITH TEMPERATURE AS A PARAMETER



QUIESCENT CURRENT (ISY) VS. TEMPERATURE WITH SUPPLY VOLTAGE AS A PARAMETER



POWER SUPPLY REJECTION RATIO (PSRR) VS. FREQUENCY



APPLICATION INFORMATION

The OP-12 series has extremely low input offset and bias currents; the user is cautioned that stray printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to fully realize the OP-12 performance. It is suggested that effects of board leakage be minimized by encircling the input pins with a conductive guard ring operated at a potential close to that of the inputs. This guard ring should be driven by a low impedance source such as the amplifier's output for non-inverting circuits, or be tied to ground for inverting circuits.

OP-12 DEFINITIONS

INPUT OFFSET VOLTAGE (V_{OS})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT OFFSET CURRENT (I_{OS})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

INPUT RESISTANCE (R_{in})
The ratio of the small-signal change in input voltage to the change in input current at either input terminal with the other grounded.

SUPPLY CURRENT (I_{sy})
The current required from the power supply to operate the amplifier with no load and the output at zero volts.

MAXIMUM OUTPUT VOLTAGE SWING (V_{oM})
The peak output voltage that can be obtained without clipping.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{OS})
The ratio of the change in the offset voltage to the change in temperature producing it.

AVERAGE BIAS CURRENT DRIFT (TCI_B)
The ratio of the change in the bias current to the change in temperature producing it.

INPUT NOISE VOLTAGE (e_{np-p})
The peak to peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage in a 1Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak to peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1Hz band surrounding a specified value of frequency.

OPEN LOOP OUTPUT RESISTANCE (R_O)
The small signal driving point resistance of the output terminal with respect to ground at a specified quiescent dc output voltage and current.

POWER CONSUMPTION (P_D)
The power required to operate the amplifier with no load and the output at zero volts

OP-14

DUAL MATCHED HIGH PERFORMANCE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

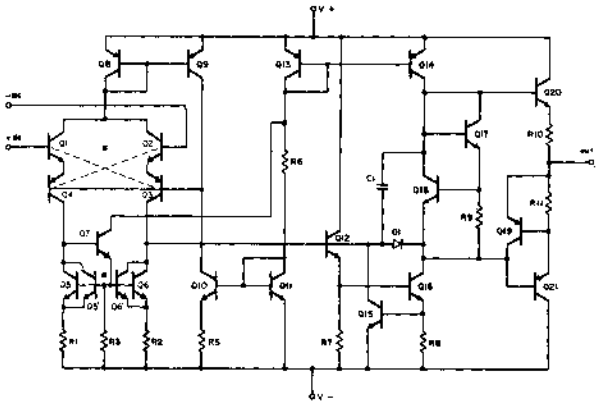
The OP-14 Series of Dual Matched High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard 1458/1558 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR, and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-14 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. For similar devices with nulling capability, refer to the OP-04 data sheet.

FEATURES

- Excellent D.C. Input Specifications
- Matched V_{OS} and CMRR
- Fits Standard 1458/1558 Socket
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- 0°C/+70°C and −55°C/+125°C Models
- Silicon-Nitride Passivation
- Models With MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC

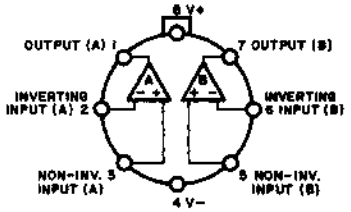
(1/2 OF CIRCUIT SHOWN)



*Q1, Q2, Q3 & Q4 FORM A THERMALLY CROSS-COUPLED TRANSISTOR QUAD. Q5, Q6, Q8 & Q8' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)
ORDER: OP-14AJ
OP-14J
OP-14EJ
OP-14CJ

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: OP14-883-AJ
OP14-883-J

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65° to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

OP-14A, OP-14	−55°C to +125°C
OP-14E, OP-14C	0°C to +70°C

Note 1: Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C

MATCHING CHARACTERISTICS

	OP-14A OP-14E					OP-14 OP-14C			
These specifications apply for V_S = ±15V, T_A = 25°C, $R_S \leq 100\Omega$, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage Match	ΔV_{OS}		–	0.3	1.0	–	1.0	2.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± CMVR	94	106	–	94	106	–	dB
These specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C for OP-14A and OP-14, 0°C ≤ T_A ≤ 70°C for OP-14E and OP-14C, $R_S \leq 100\Omega$ unless otherwise noted.									
Input Offset Voltage Match	ΔV_{OS}		–	0.5	1.5	–	1.5	3.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± CMVR	90	100	–	90	100	–	dB

MATCHING PARAMETER DEFINITIONS

COMMON MODE REJECTION RATIO MATCH (ΔCMRR). The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. ΔCMRR in dB = 20 $\log_{10}$ (ΔCMRR in volt/volt).

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$).

OP-14 DEFINITIONS

INPUT OFFSET VOLTAGE (V_{OS})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT OFFSET CURRENT (I_{OS})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

MAXIMUM OUTPUT VOLTAGE SWING (V_{OM})
The peak output voltage that can be obtained without clipping.

LARGE SIGNAL VOLTAGE GAIN (A_{VO})
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{OS})
The ratio of the change in the offset voltage to the change in temperature producing it.

AVERAGE OFFSET CURRENT DRIFT (TCI_{OS})
The ratio of the change in the offset current to the change in temperature producing it.

POWER DISSIPATION (P_d)
The total power dissipated in the amplifier with the output at zero volts and no load.

UNITY GAIN CLOSED LOOP BANDWIDTH (BW)
The frequency at which the magnitude of the small signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3 dB below unity.

INPUT NOISE VOLTAGE (e_{np-p})
The peak-to-peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage in a 1 Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak-to-peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1 Hz band surrounding a specified value of frequency.

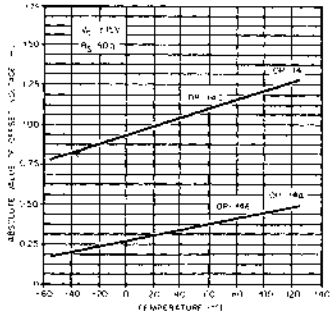
ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-14A			OP-14			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.75	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	50	–	20	75	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_o = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Channel Separation	CS		100	–	–	100	–	–	dB
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.5	0.7	–	0.5	0.7	–	V/µs
Large Signal Bandwidth (Note 1)		V_o = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.5	1.5	–	1.4	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	µV/°C
Input Offset Current	I_{os}		–	1.0	5.0	–	2.0	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	75	–	15	150	pA/°C
Input Bias Current	I_B		–	30	100	–	40	125	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	50	100	–	25	60	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V

Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.

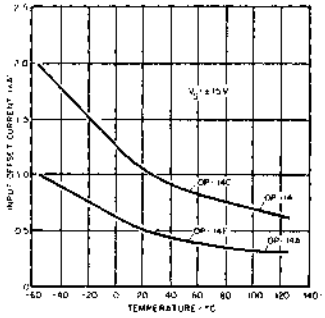
ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-14E			OP-14C			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.75	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	50		20	75	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_o = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Channel Separation	CS		100	–	–	100	–	–	dB
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.5	0.7	–	0.5	0.7	–	V/μs
Large Signal Bandwidth (Note 1)		V_o = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.4	1.5	–	1.2	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	μV/°C
Input Offset Current	I_{os}		–	0.7	4.0	–	1.4	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	120	–	15	250	pA/°C
Input Bias Current	I_B		–	22	50	–	25	125	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	50	200	–	25	150	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

TYPICAL PERFORMANCE CURVES (Each Amplifier)

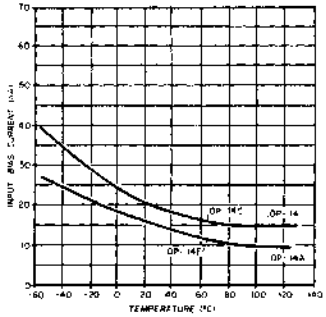
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



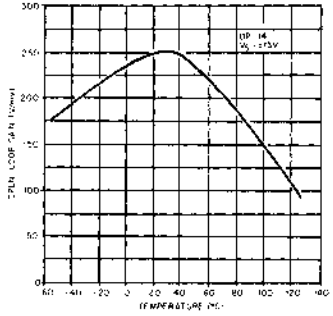
INPUT OFFSET CURRENT VS TEMPERATURE



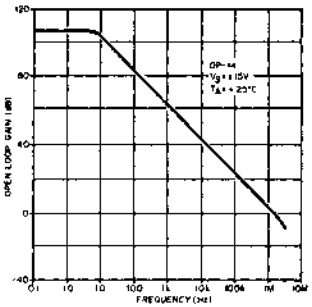
INPUT BIAS CURRENT VS TEMPERATURE



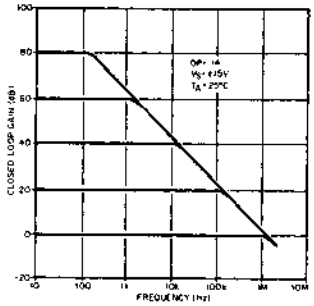
OPEN LOOP GAIN VS TEMPERATURE



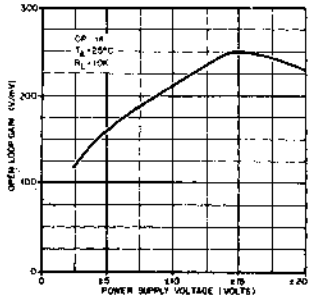
OPEN LOOP FREQUENCY RESPONSE



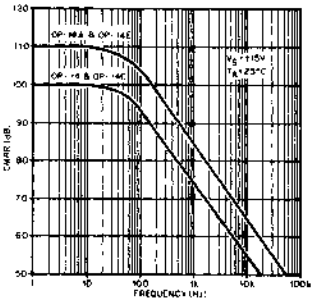
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



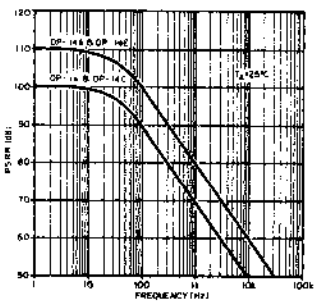
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



CMRR VS FREQUENCY

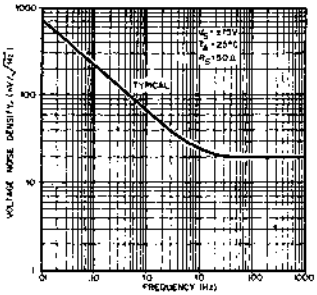


PSRR VS FREQUENCY

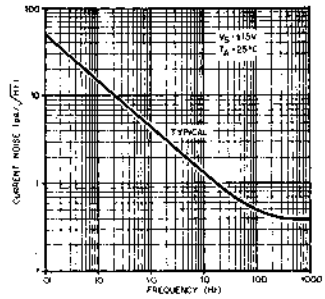


TYPICAL PERFORMANCE CURVES (Each Amplifier)

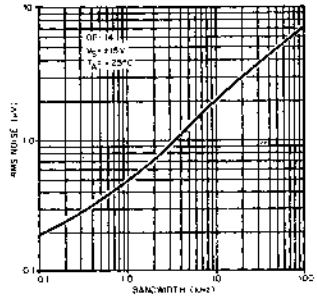
INPUT SPOT NOISE VOLTAGE VS FREQUENCY



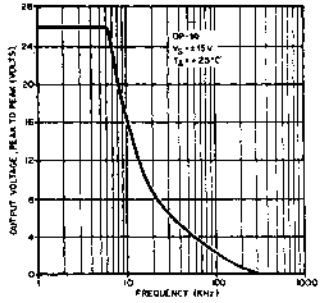
INPUT SPOT NOISE CURRENT VS FREQUENCY



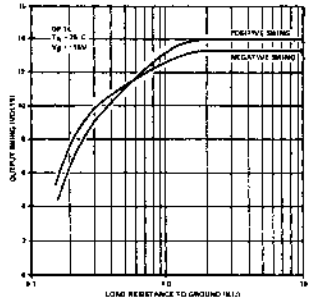
INPUT WIDEBAND NOISE VS BANDWIDTH (.1 Hz TO FREQUENCY INDICATED)



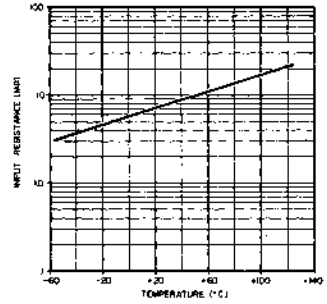
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



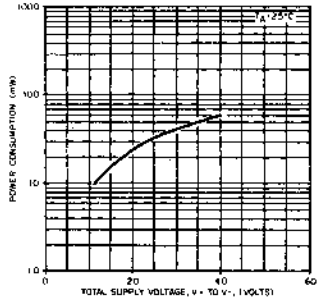
OUTPUT VOLTAGE VS LOAD RESISTANCE



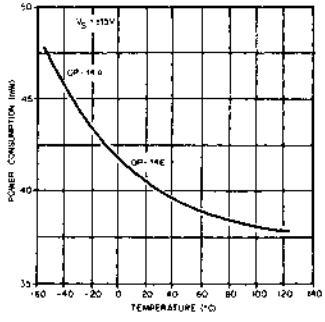
INPUT RESISTANCE VS TEMPERATURE



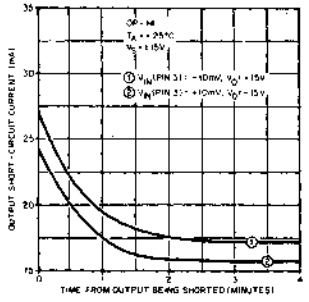
POWER CONSUMPTION VS POWER SUPPLY



POWER CONSUMPTION VS TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT VS TIME



OP-15

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

LOW SUPPLY CURRENT

GENERAL DESCRIPTION

The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition the OP-15 offers the speed of the 156A op amp with 155A dissipation. To further enhance the excellent input parameters, the OP-15 uses bias current compensation to maintain low input bias current at elevated temperatures.

The OP-15 was designed to provide real precision performance along with its high speed. For example the 500μV offset voltage yields less than 1/2 LSB error in a 12 bit, 5V DAC. Although the OP-15 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST-EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved BI-FET process coupled with on-chip zener-zap offset trimming.

Most high speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that 500μV is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

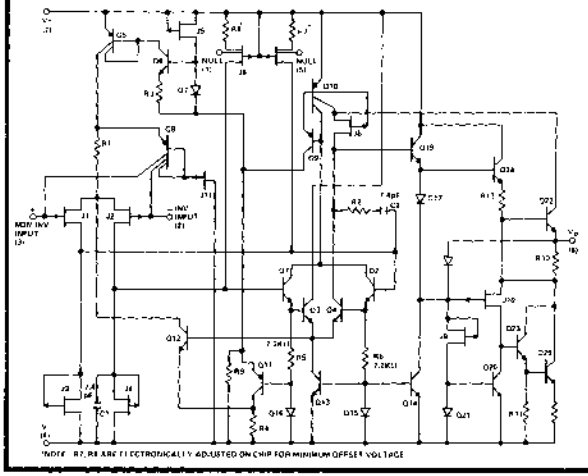
The combination of low input offset voltage of 500μV MAX., slew rate of 17V/μsec, and settling time of 900nsec–to 0.1%–makes the OP-15 a true precision, high speed op amp. The additional features of low supply current coupled with an input bias current of 9nA at 125°C ambient (not junction) temperature makes the OP-15 useful in a wide range of applications.

Applications include high speed amplifiers for current output DAC's, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-16 and OP-17 data sheets.

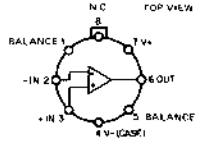
FEATURES

- High Slew Rate 17V/μs
- Fast Settling to ±0.1% . . . . . 900 nsec
- Low Input Offset Voltage . . . . . 500 μV MAX
- Low Input Offset Voltage Drift . . . . . 2.0 μV/°C
- 156 Speed with 155 Dissipation
- Wide Bandwidth . . . . . 6 MHz
- Minimum Slew Rate Guaranteed on All Models
- Temperature Compensated Input Bias Currents*
- Guaranteed Input Bias Current @ 125°C. . 9nA MAX
- Bias Current Specified WARMED UP Over Temp.
- Internal Compensation
- Low Input Noise Current . . . . . 0.01 pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- Models With MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

ORDER: OP-15AJ, OP-15BJ, OP-15CJ	-55°C TO +125°C
OP-15EJ, OP-15FJ, OP-15GJ	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP15-883-AJ
ORDER OP15-883-BJ
OP15-883-CJ

*PATENT APPLIED FOR

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP-15A, OP-15B, OP-15E, OP-15F: ±22V
- OP-15C, OP-15G: ±18V

Internal Power Dissipation
- All Devices: 500mW
  (The TO-99(J) package must be derated based on a thermal resistance of 150° C/W junction to ambient or 45° C/W junction to case.)

Operating Temperature Range
- OP-15A, OP-15B, OP-15C: −55°C to +125°C
- OP-15E, OP-15F, OP-15G: 0°C to +70°C

Maximum Junction Temperature (T_J)
- All Devices: +150°C

Differential Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F: ±40V
- OP-15C, OP-15G: ±30V

Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F: ±20V
- OP-15C, OP-15G: ±16V

  (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: −65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-15A Min	OP-15A Typ	OP-15A Max	OP-15B Min	OP-15B Typ	OP-15B Max	OP-15C Min	OP-15C Typ	OP-15C Max	Units
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	$T_J = 25°C$ (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	22	–	5.0	40	–	5.0	100	
Input Bias Current	I_B	$T_J = 25°C$ (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	18	110	–	18	200	–	18	400	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, $V_O = \pm10V$	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	$R_L = 10K$	±12	±13	–	±12	±13	–	±12	±13	–	V
		$R_L = 2K$	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	2.7	4.0	–	2.7	4.0	–	2.8	5.0	mA
Slew Rate	SR	$A_{VCL} = +1.0$	10	17	–	7.5	16	–	5.0	15	–	V/μsec
Gain Bandwidth Product	GBW		4.0	6.0	–	3.5	5.7	–	3.0	5.4	–	MHz
Closed Loop Bandwidth	CLBW	$A_{VCL} = +1.0$	–	14	–	–	13	–	–	12	–	MHz
Settling Time	t_s	to 0.01%	–	2.2	–	–	2.3	–	–	2.4	–	μs
		to 0.05% (Note 2)	–	1.1	–	–	1.1	–	–	1.2	–	
		to 0.10%	–	0.9	–	–	0.9	–	–	1.0	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to $\pm20V$	86	100	–	86	100	–	–	–	–	dB
		$V_S = \pm10V$ to $\pm15V$	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	$f_O = 100Hz$	–	20	–	–	20	–	–	20	–	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	$f_O = 100Hz$	–	0.01	–	–	0.01	–	–	0.01	–	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for $V_S = \pm15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.												
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	0.4	0.9	–	0.7	2.0	–	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	$R_P = 100K\Omega$	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current (Note 1)	I_{OS}	$T_J = 125°C$	–	0.6	4.0	–	0.8	6.0	–	1.0	9.0	nA
		$T_A = 125°C$	–	0.8	7.0	–	1.2	11	–	1.5	17	
		Device Operating										
Input Bias Current (Note 1)	I_B	$T_J = 125°C$	–	1.2	5.0	–	1.5	7.5	–	1.8	10	nA
		$T_A = 125°C$	–	1.7	9.0	–	2.2	14	–	2.7	19	
		Device Operating										
Input Voltage Range	CMVR		±10.4	+14.6 −11.3	–	±10.4	+14.6 −11.3	–	±10.25	+14.6 −11.3	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	85	97	–	85	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm10V$,to $\pm20V$	85	97	–	85	97	–	–	–	–	dB
		$V_S = \pm10V$ to $\pm15V$	–	–	–	–	–	–	80	93	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, $V_S = \pm10V$	35	120	–	30	110	–	25	100	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-15E Min	OP-15E Typ	OP-15E Max	OP-15F Min	OP-15F Typ	OP-15F Max	OP-15G Min	OP-15G Typ	OP-15G Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	22	–	5.0	40	–	5.0	100	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	18	110	–	18	200	–	18	400	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2KΩ, V_S = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	2.7	4.0	–	2.7	4.0	–	2.8	5.0	mA
Slew Rate	SR	A_{VCL} = +1.0	10	17	–	7.5	16	–	5.0	15	–	V/μsec
Gain Bandwidth Product	GBW		4.0	6.0	–	3.5	5.7	–	5.0	5.4	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	14	–	–	13	–	–	12	–	MHz
Settling Time	t_s	to 0.01%	–	2.2	–	–	2.3	–	–	2.4	–	μs
		to 0.05% (Note 2)	–	1.1	–	–	1.1	–	–	1.2	–	
		to 0.10%	–	0.9	–	–	0.9	–	–	1.0	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.3	0.75	–	0.55	1.5	–	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = +70°C (Note 1)	–	0.04	0.30	–	0.06	0.45	–	0.08	0.65	nA
		T_A = +70°C Device Operating	–	0.06	0.55	–	0.08	0.80	–	0.10	1.2	
Input Bias Current	I_B	T_J = +70°C (Note 1)	–	0.10	0.40	–	0.12	0.60	–	0.14	0.80	nA
		T_A = +70°C Device Operating	–	0.13	0.75	–	0.16	1.1	–	0.19	1.5	
Input Voltage Range	CMVR		±10.4	+14.7 −11.4	–	±10.4	+14.7 −11.4	–	±10.25	+14.7 −11.4	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	98	–	85	98	–	80	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	98	–	85	98	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	94	–	
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2K, V_S = ±10V	65	200	–	50	180	–	35	130	–	V/mV
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10KΩ	±12	±13	–	±12	±13	–	±12	+13	–	V

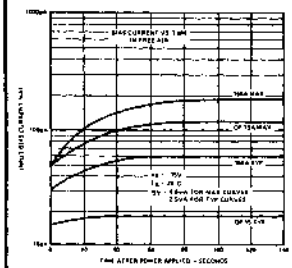
NOTE 1: Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs. time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temp. value *via* the curves of I_B vs. T_J and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

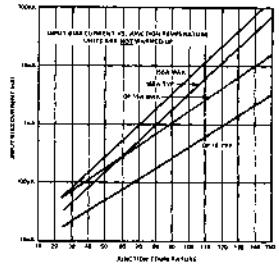
NOTE 3: Parameter is not 100% tested. 90% of all units meet these specifications.

TYPICAL PERFORMANCE CURVES

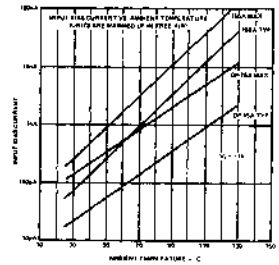
BIAS CURRENT VS. TIME IN FREE AIR



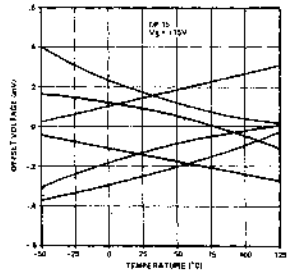
INPUT BIAS CURRENT VS. JUNCTION TEMPERATURE UNITS ARE NOT WARMED-UP



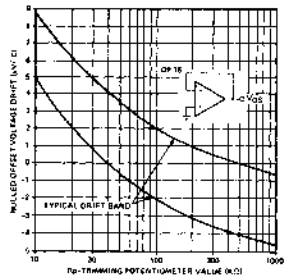
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)



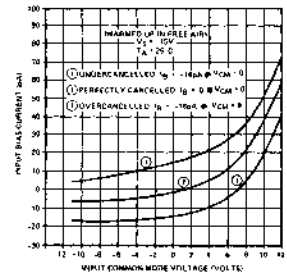
OFFSET VOLTAGE VS TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



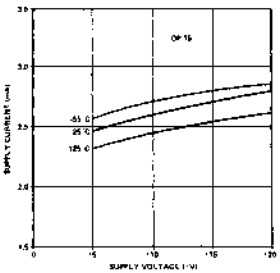
NULLED OFFSET VOLTAGE DRIFT VS POTENTIOMETER SIZE



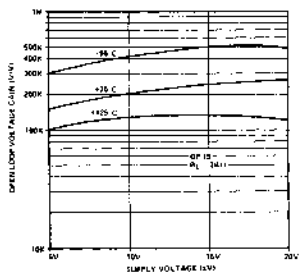
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



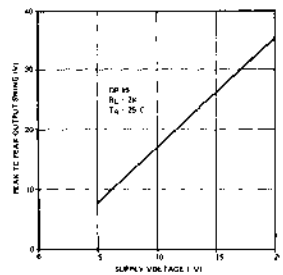
SUPPLY CURRENT VS SUPPLY VOLTAGE



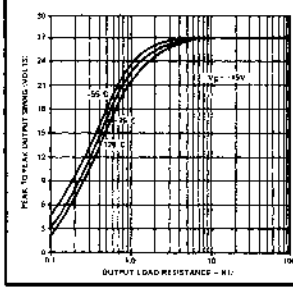
OPEN LOOP VOLTAGE GAIN



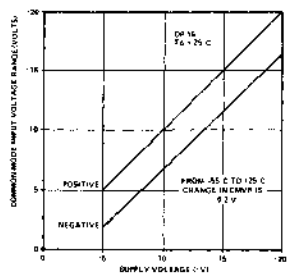
VOLTAGE SWING VS SUPPLY VOLTAGE



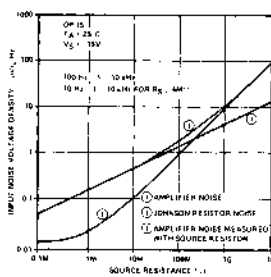
OUTPUT VOLTAGE VS LOAD RESISTANCE



COMMON MODE INPUT VOLTAGE RANGE

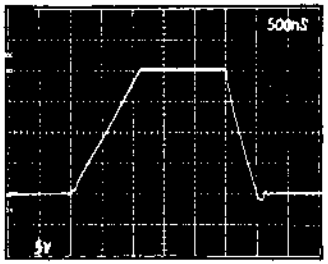


VOLTAGE NOISE VS SOURCE RESISTANCE

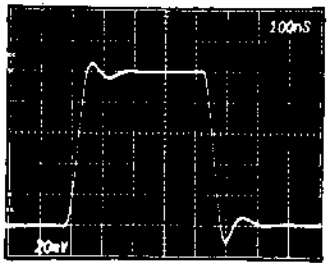


TYPICAL PERFORMANCE CURVES

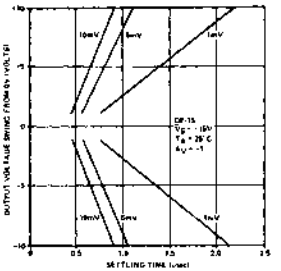
LARGE SIGNAL TRANSIENT RESPONSE



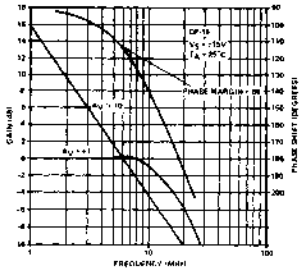
SMALL SIGNAL TRANSIENT RESPONSE



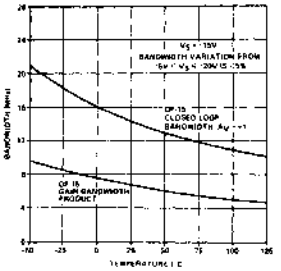
SETTLING TIME



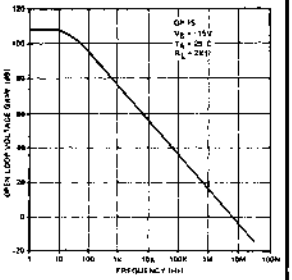
CLOSED LOOP BANDWIDTH AND PHASE SHIFT VS FREQUENCY



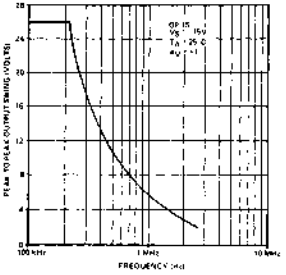
BANDWIDTH VS TEMPERATURE



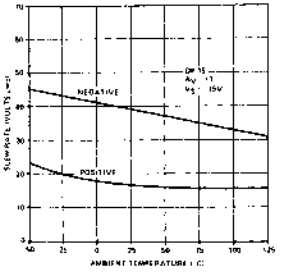
OPEN LOOP FREQUENCY RESPONSE



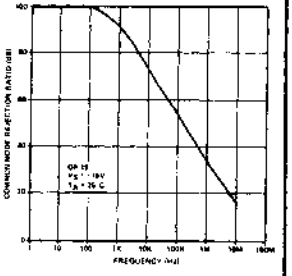
UNDISTORTED OUTPUT SWING



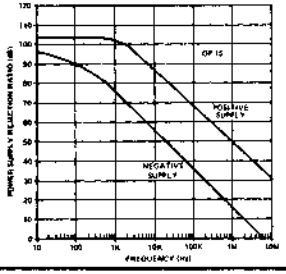
SLEW RATE VS TEMPERATURE



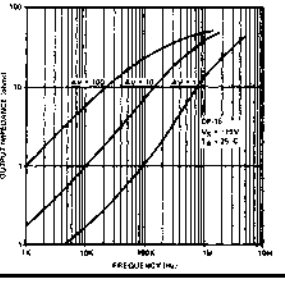
COMMON MODE REJECTION RATIO VS FREQUENCY



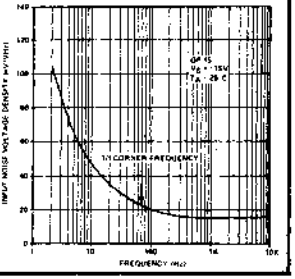
POWER SUPPLY REJECTION VS FREQUENCY



OUTPUT IMPEDANCE VS FREQUENCY

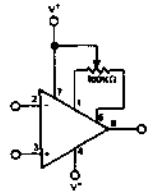


VOLTAGE NOISE VS FREQUENCY



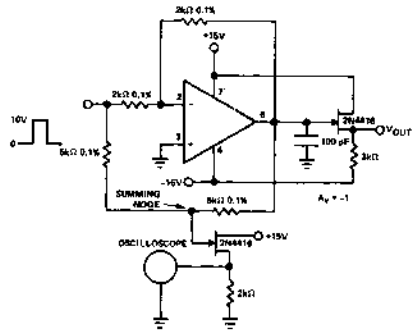
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10KΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100KΩ POTENTIOMETER.

SETTLING TIME TEST CIRCUIT



APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

OP-16

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

WIDE BANDWIDTH

GENERAL DESCRIPTION

The OP-16 offers a performance combination not usually found in the same op amp—high speed and low input offset voltage. Not only does the OP-16 out-perform the 156A in speed and error band, but it is clearly superior to several more costly hybrid and dielectrically-isolated op amps. In addition, the OP-16 uses bias current compensation to maintain low input bias current at elevated temperatures.

The OP-16 was designed to provide real precision performance along with its high speed. For example the 500μV offset voltage yields less than 1/2 LSB error in a 12 bit, 5V DAC. Although the OP-16 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST-EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved Bi-FET process coupled with on-chip zener-zap offset trimming.

Most high speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that 500μV is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

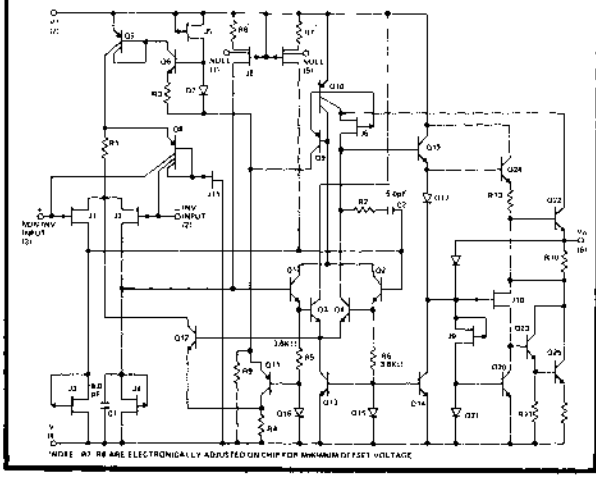
The combination of low input offset voltage of 500μV MAX., slew rate of 25V/μsec, and settling time of 700nsec—to 0.1%—makes the OP-16 a true precision, high speed op amp. Because of the input bias current compensation, the maximum input bias current at 125°C ambient (not junction) temperature is only 11nA. This kind of performance makes the OP-16 useful in a wide range of applications.

Applications include high speed amplifiers for current output DAC's, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-15 and OP-17 data sheets.

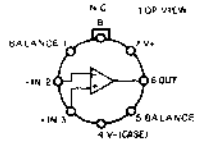
FEATURES

- High Slew Rate 25V/μs
- Fast Settling to ±0.1% . . . . . 700 nsec
- Low Input Offset Voltage . . . . . 500 μV MAX
- Low Input Offset Voltage Drift . . . . . 2.0 μV/°C
- Wide Bandwidth . . . . . 8 MHz
- Minimum Slew Rate Guaranteed on All Models
- Temperature Compensated Input Bias Currents*
- Guaranteed Input Bias Current @ 125°C. .11nA MAX
- Bias Current Specified WARMED UP Over Temp.
- Internal Compensation
- Low Input Noise Current . . . . . 0.01 pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- Models With MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

ORDER: OP-16AJ OP-16BJ OP-16CJ	-55°C TO +125°C
OP-16EJ OP-16FJ OP-16GJ	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP16-883-AJ
OP16-883-BJ
OP16-883-CJ

*PATENT APPLIED FOR

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP-16A, OP-16B, OP-16E, OP-16F: ±22V
- OP-16C, OP-16G: ±18V

Internal Power Dissipation
- All Devices: 500mW
  - (The TO-99(J) package must be derated based on a thermal resistance of 150° C/W junction to ambient or 45° C/W junction to case.)

Operating Temperature Range
- OP-16A, OP-16B, OP-16C: –55°C to +125°C
- OP-16E, OP-16F, OP-16G: 0°C to +70°C

Maximum Junction Temperature (T_J)
- All Devices: +150°C

Differential Input Voltage
- OP-16A, OP-16B, OP-16E, OP-16F: ±40V
- OP-16C, OP-16G: ±30V

Input Voltage
- OP-16A, OP-16B, OP-16E, OP-16F: ±20V
- OP-16C, OP-16G: ±16V
  - (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for V_s = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-16A Min	OP-16A Typ	OP-16A Max	OP-16B Min	OP-16B Typ	OP-16B Max	OP-16C Min	OP-16C Typ	OP-16C Max	Units
Input Offset Voltage	V_{OS}	R_s = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_s = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +1.0	18	25	–	12	24	–	9.0	23	–	V/μsec
Gain Bandwidth Product	GBW		6.0	8.0	–	5.5	7.6	–	5.0	7.2	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	19	–	–	18	–	–	17	–	MHz
Settling Time	t_s	to 0.01%	–	1.7	–	–	1.7	–	–	1.8	–	μs
		to 0.05% (Note 2)	–	0.9	–	–	0.9	–	–	1.0	–	
		to 0.10%	–	0.7	–	–	0.7	–	–	0.8	–	
Input Voltage Range	CMVR		±10.5	+14.8 –11.5	–	±10.5	+14.8 –11.5	–	±10.3	+14.8 –11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_s = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_s = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_s = 50Ω	–	0.4	0.9	–	0.7	2.0	–	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_p = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = 125°C (Note 1)	–	0.6	4.0	–	0.80	6.0	–	1.0	9.0	nA
		T_A = 125°C	–	1.0	8.5	–	1.3	14.5	–	1.7	22	
		Device Operating										
Input Bias Current	I_B	T_J = 125°C (Note 1)	–	1.2	5.0	–	1.5	7.5	–	1.8	10	nA
		T_A = 125°C	–	2.0	11	–	2.5	18	–	3.0	25	
		Device Operating										
Input Voltage Range	CMVR		±10.4	+14.6 –11.3	–	±10.4	+14.6 –11.3	–	±10.25	+14.6 –11.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	97	–	85	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±10V to ±20V	85	97	–	85	97	–	–	–	–	dB
		V_s = ±10V to ±15V	–	–	–	–	–	–	80	93	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_s = ±10V	35	120	–	30	110	–	25	100	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

ELECTRICAL CHARACTERISTICS			OP-16E			OP-16F			OP-16G			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_O = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
			±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +1.0	18	25	–	12	24	–	9.0	23	–	V/μsec
Gain Bandwidth Product	GBW		6.0	8.0	–	5.5	7.6	–	5.0	7.2	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	19	–	–	18	–	–	17	–	MHz
Settling Time	t_S	to 0.01%	–	1.7	–	–	1.7	–	–	1.8	–	μs
		to 0.05% (Note 2)	–	0.9	–	–	0.9	–	–	1.0	–	
		to 0.10%	–	0.7	–	–	0.7	–	–	0.8	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.3	0.75	–	0.55	1.5	–	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = +70°C (Note 1)	–	0.04	0.30	–	0.06	0.45	–	0.08	0.65	nA
		T_A = +70°C Device Operating	–	0.07	0.70	–	0.10	1.1	–	0.15	1.7	
Input Bias Current	I_B	T_J = +70°C (Note 1)	–	0.10	0.40	–	0.12	0.60	–	0.14	0.80	nA
		T_A = +70°C Device Operating	–	0.15	0.90	–	0.20	1.4	–	0.25	2.0	
Input Voltage Range	CMVR		±10.4	+14.7 −11.4	–	±10.4	+14.7 −11.4	–	±10.25	+14.7 −11.4	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	98	–	85	98	–	80	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	98	–	85	98	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	94	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	65	200	–	50	180	–	35	160	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

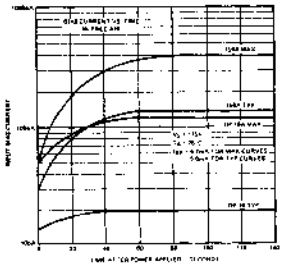
NOTE 1: Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs. time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temp. value via the curves of I_B vs. T_J and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

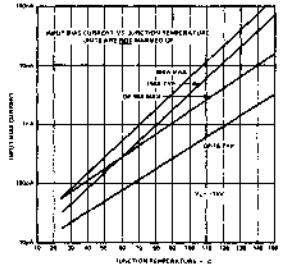
NOTE 3: Parameter is not 100% tested. 90% of all units meet these specifications.

TYPICAL PERFORMANCE CURVES

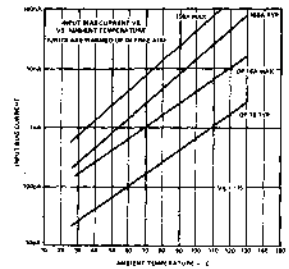
BIAS CURRENT VS. TIME IN FREE AIR



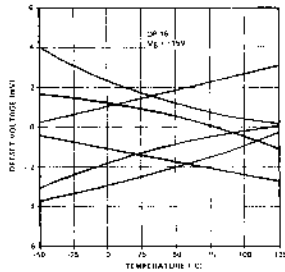
INPUT BIAS CURRENT VS. JUNCTION TEMPERATURE UNITS ARE NOT WARMED-UP



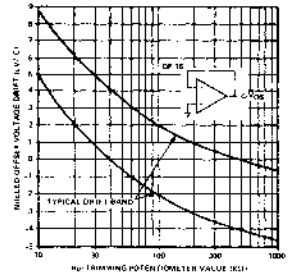
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)



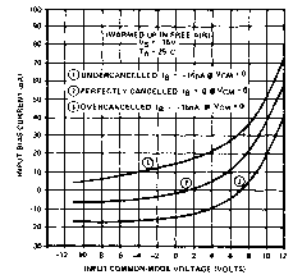
OFFSET VOLTAGE VS TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



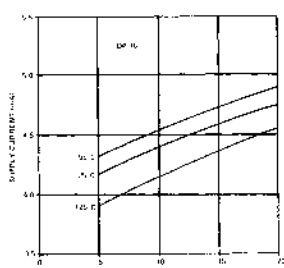
NULLED OFFSET VOLTAGE DRIFT VS POTENTIOMETER SIZE



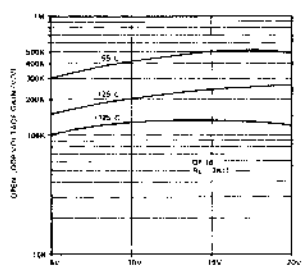
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



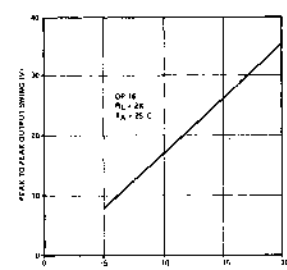
SUPPLY CURRENT VS SUPPLY VOLTAGE



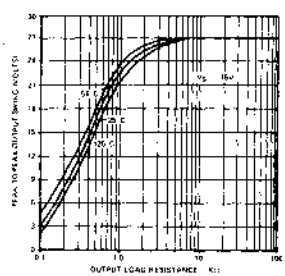
OPEN LOOP VOLTAGE GAIN



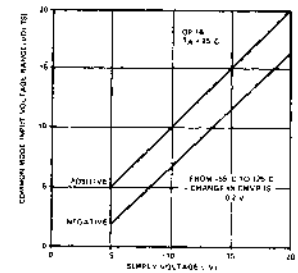
VOLTAGE SWING VS SUPPLY VOLTAGE



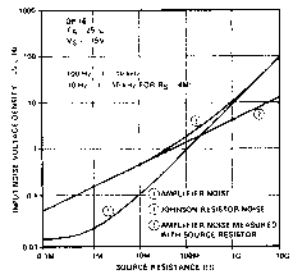
OUTPUT VOLTAGE VS LOAD RESISTANCE



COMMON MODE INPUT VOLTAGE RANGE

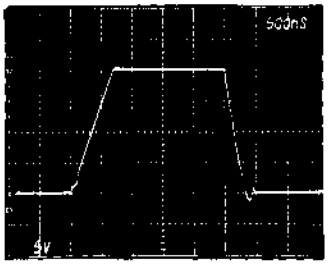


VOLTAGE NOISE VS SOURCE RESISTANCE

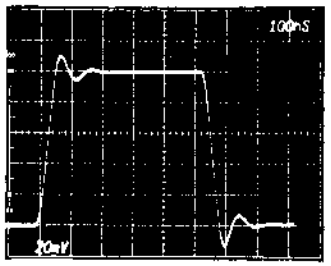


TYPICAL PERFORMANCE CURVES

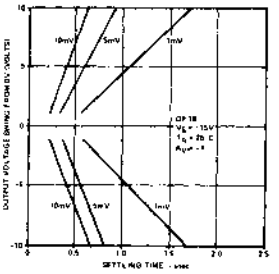
LARGE SIGNAL TRANSIENT RESPONSE



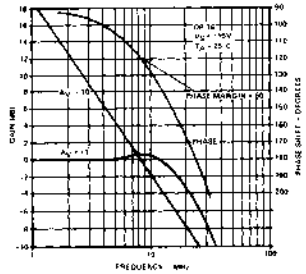
SMALL SIGNAL TRANSIENT RESPONSE



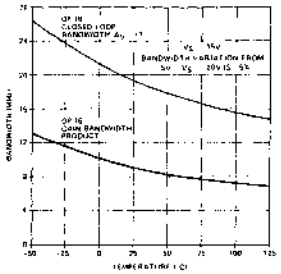
SETTLING TIME



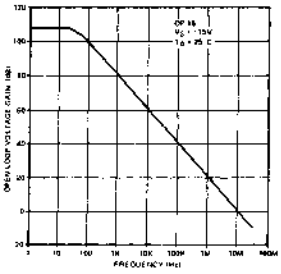
CLOSED LOOP BANDWIDTH AND PHASE SHIFT VS FREQUENCY



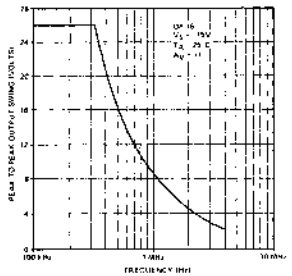
BANDWIDTH VS TEMPERATURE



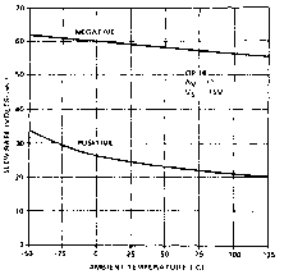
OPEN LOOP FREQUENCY RESPONSE



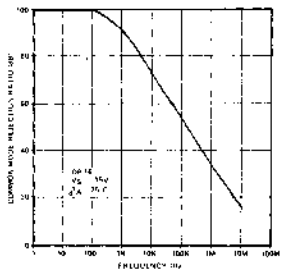
UNDISTORTED OUTPUT SWING



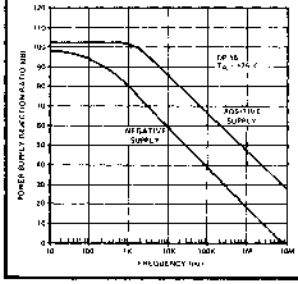
SLEW RATE VS TEMPERATURE



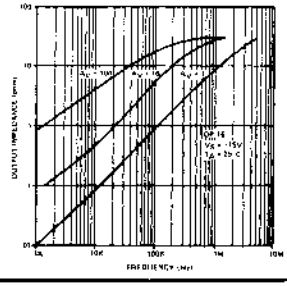
COMMON MODE REJECTION RATIO VS FREQUENCY



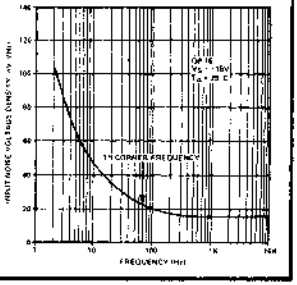
POWER SUPPLY REJECTION VS FREQUENCY



OUTPUT IMPEDANCE VS FREQUENCY

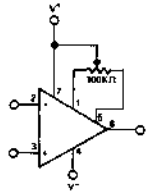


VOLTAGE NOISE VS FREQUENCY



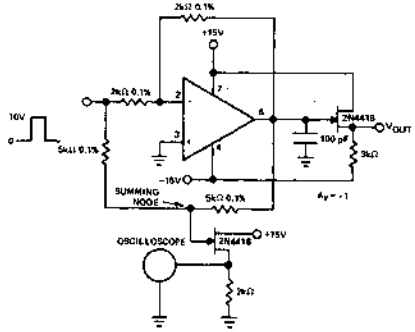
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10KΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100KΩ POTENTIOMETER

SETTLING TIME TEST CIRCUIT



APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

OP-17

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

WIDE BANDWIDTH DECOMPENSATED (A_{VMIN} = 5)

GENERAL DESCRIPTION

With an unusual performance combination of 400nsec settling time and an input offset voltage of 500μV MAX., the OP-17 clearly outperforms the 157A op amp. In addition, the OP-17 is superior in both cost and performance to several dielectrically-isolated and hybrid op amps. Bias current compensation provides low input bias current at elevated temperatures.

The OP-17 was designed to provide real precision performance along with its high speed. For example the 500μV offset voltage yields less than 1/2 LSB error in a 12 bit, 5V DAC. Although the OP-17 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST-EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved BI-FET process coupled with on-chip zener-zap offset trimming.

Most high speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that 500μV is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

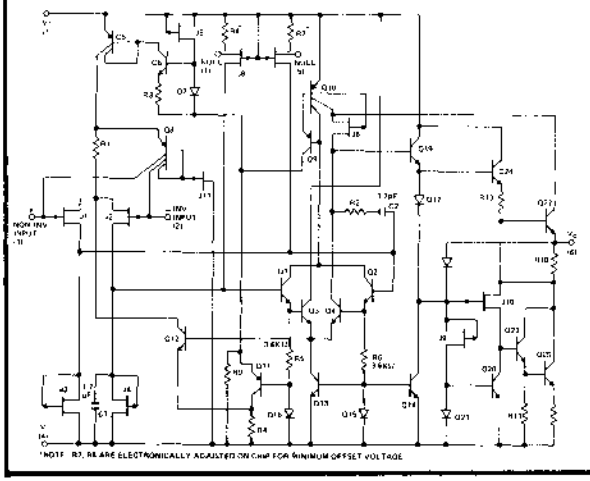
The combination of low input offset voltage of 500μV MAX., slew rate of 70V/μsec, and settling time of 400nsec to 0.1% makes the OP-17 a true precision, high speed op amp. Because of the input bias current compensation, the maximum input bias current at 125°C ambient (not junction) temperature is only 11nA. This kind of performance makes the OP-17 useful in a wide range of applications.

Applications include high speed amplifiers for current output DAC's, active filters, and photocell amplifiers. For unity gain fast follower applications see the OP-15 and OP-16 precision JFET op amp data sheets.

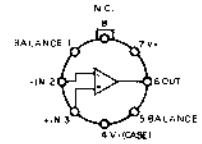
FEATURES

- High Slew Rate 70V/μs
- Fast Settling to ±0.1% . . . . . 400 nsec
- Low Input Offset Voltage . . . . . 500 μV MAX
- Low Input Offset Voltage Drift . . . . . 2.0 μV/°C
- Big Gain Bandwidth Product . . . . . .30 MHz
- Minimum Slew Rate Guaranteed on All Models
- Temperature Compensated Input Bias Currents*
- Guaranteed Input Bias Current @ 125°C . .11nA MAX
- Bias Current Specified WARMED UP Over Temp.
- Internal Compensation
- Low Input Noise Current . . . . . 0.01 pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- Models with MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

ORDER: OP-17AJ, OP-17BJ, OP-17CJ	-55°C TO +125°C
OP-17EJ, OP-17FJ, OP-17GJ	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: OP17-883-AJ
OP17-883-BJ
OP17-883-CJ

*PATENT APPLIED FOR

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP-17A, OP-17B, OP-17E, OP-17F: ±22V
- OP-17C, OP-17G: ±18V

Internal Power Dissipation
- All Devices: 500mW
  (The TO-99(J) package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.)

Operating Temperature Range
- OP-17A, OP-17B, OP-17C: −55°C to +125°C
- OP-17E, OP-17F, OP-17G: 0°C to +70°C

Maximum Junction Temperature (T_J)
- All Devices: +150°C

Differential Input Voltage
- OP-17A, OP-17B, OP-17E, OP-17F: ±40V
- OP-17C, OP-17G: ±30V

Input Voltage
- OP-17A, OP-17B, OP-17E, OP-17F: ±20V
- OP-17C, OP-17G: ±16V
  (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: −65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-17A Min	OP-17A Typ	OP-17A Max	OP-17B Min	OP-17B Typ	OP-17B Max	OP-17C Min	OP-17C Typ	OP-17C Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2KΩ, V_S = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +5.0	45	70	–	35	66	–	25	62	–	V/μsec
Gain Bandwidth Product	GBW		20	30	–	15	28	–	11	26	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +5.0	–	11	–	–	10	–	–	9	–	MHz
Settling Time	t_s	to 0.01%	–	1.5	–	–	1.5	–	–	1.6	–	μs
		to 0.05% (Note 2)	–	0.5	–	–	0.5	–	–	0.6	–	
		to 0.10%	–	0.4	–	–	0.4	–	–	0.5	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.4	0.9	–	0.7	2.0	–	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = 125°C (Note 1)	–	0.6	4.0	–	0.8	6.0	–	1.0	9.0	nA
		T_A = 125°C	–	1.0	8.5	–	1.3	14.5	–	1.7	22	
		Device Operating										
Input Bias Current	I_B	T_J = 125°C (Note 1)	–	1.2	5.0	–	1.5	7.5	–	1.8	10	nA
		T_A = 125°C	–	2.0	11	–	2.5	18	–	3.0	25	
		Device Operating										
Input Voltage Range	CMVR		±10.4	+14.6 −11.3	–	±10.4	+14.6 −11.3	–	±10.25	+14.6 −11.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	97	–	85	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	97	–	85	97	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	93	–	
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2K, V_S = ±10V	35	120	–	30	110	–	25	100	–	V/mV
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10KΩ	±12	±13	–	±12	±13	–	±12	±13	–	V

ELECTRICAL CHARACTERISTICS			OP-17E			OP-17F			OP-17G			
These specifications apply for V_s = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2KΩ, V_O = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +5.0	45	70	–	35	66	–	25	62	–	V/μsec
Gain Bandwidth Product	GBW		20	30	–	15	28	–	11	26	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +5.0	–	11	–	–	10	–	–	9	–	MHz
Settling Time	t_S	TO 0.01%	–	1.5	–	–	1.5	–	–	1.6	–	μs
		TO 0.05% (Note 2)	–	0.5	–	–	0.5	–	–	0.6	–	
		TO 0.10%	–	0.4	–	–	0.4	–	–	0.5	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM}= ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.3	0.75	–	0.55	1.5	–	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = +70°C (Note 1)	–	0.04	0.30	–	0.06	0.45	–	0.08	0.65	nA
		T_A = +70°C Device Operating	–	0.07	0.70	–	0.10	1.1	–	0.15	1.7	
Input Bias Current	I_B	T_J = +70°C (Note 1)	–	0.10	0.40	–	0.12	0.60	–	0.14	0.80	nA
		T_A = +70°C Device Operating	–	0.15	0.90	–	0.20	1.4	–	0.25	2.0	
Input Voltage Range	CMVR		±10.4	+14.7 −11.4	–	±10.4	+14.7 −11.4	–	±10.25	+14.7 −11.4	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	98	–	85	98	–	80	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	98	–	85	98	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	94	–	
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2K, V_S = ±10V	65	200	–	50	180	–	35	160	–	V/mV
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10KΩ	±12	±13	–	±12	±13	–	±12	±13	–	V

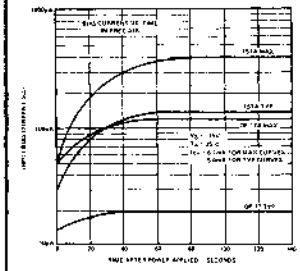
NOTE 1: Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs. time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temp. value via the curves of I_B vs. T_J and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a gain of five inverter connection using 2KΩ and 400Ω resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

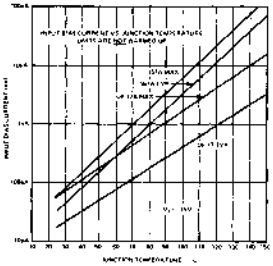
NOTE 3: Parameter is not 100% tested. 90% of all units meet these specifications.

TYPICAL PERFORMANCE CURVES

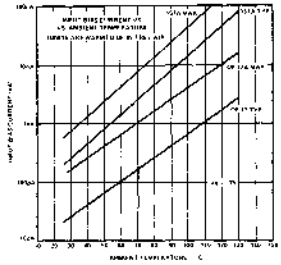
BIAS CURRENT VS. TIME IN FREE AIR



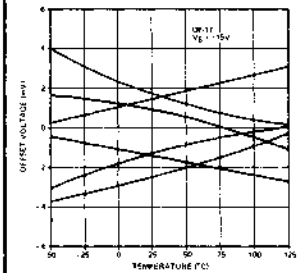
INPUT BIAS CURRENT VS. JUNCTION TEMPERATURE UNITS ARE NOT WARMED-UP



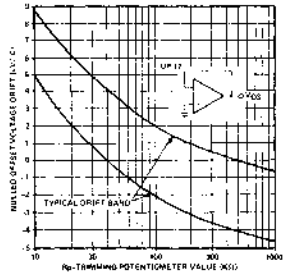
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)



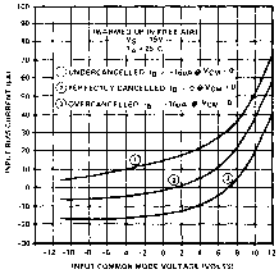
OFFSET VOLTAGE VS TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



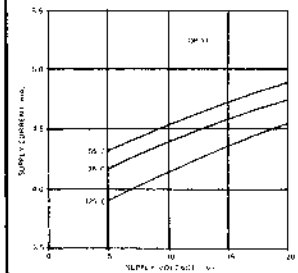
NULLED OFFSET VOLTAGE DRIFT VS POTENTIOMETER SIZE



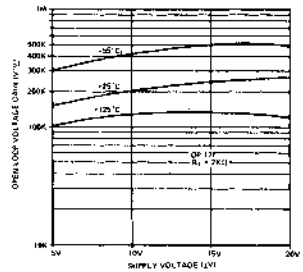
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



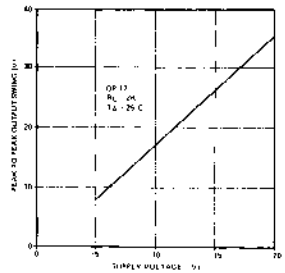
SUPPLY CURRENT VS SUPPLY VOLTAGE



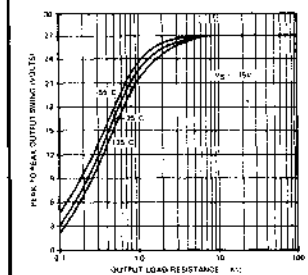
OPEN LOOP VOLTAGE GAIN



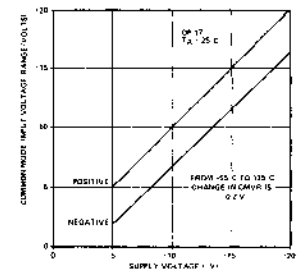
VOLTAGE SWING VS SUPPLY VOLTAGE



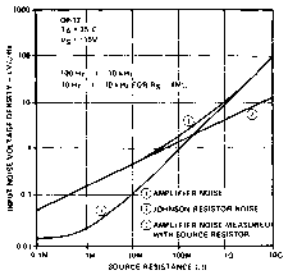
OUTPUT VOLTAGE VS LOAD RESISTANCE



COMMON MODE INPUT VOLTAGE RANGE

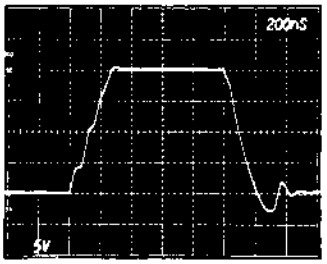


VOLTAGE NOISE VS SOURCE RESISTANCE

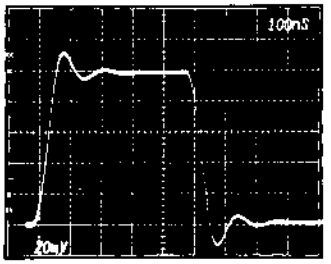


TYPICAL PERFORMANCE CURVES

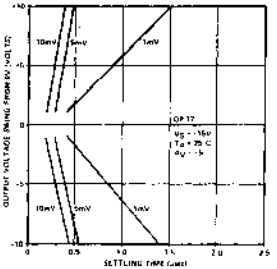
LARGE SIGNAL TRANSIENT RESPONSE



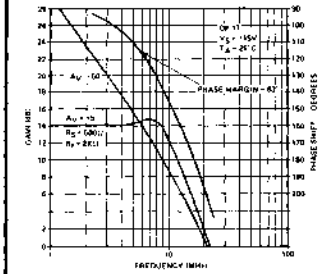
SMALL SIGNAL TRANSIENT RESPONSE



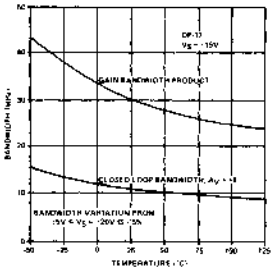
SETTLING TIME



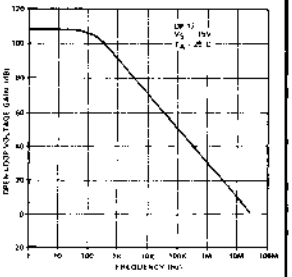
CLOSED LOOP BANDWIDTH AND PHASE SHIFT VS FREQUENCY



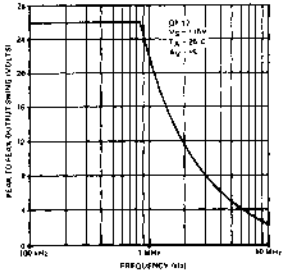
BANDWIDTH VS TEMPERATURE



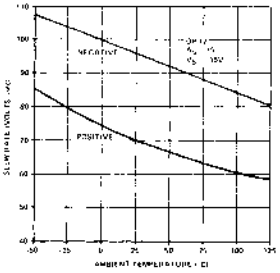
OPEN LOOP FREQUENCY RESPONSE



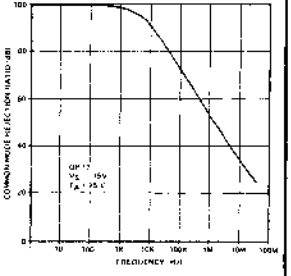
UNDISTORTED OUTPUT SWING



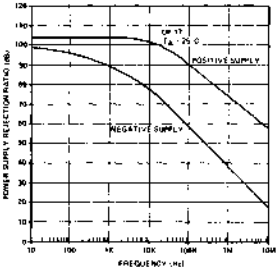
SLEW RATE VS TEMPERATURE



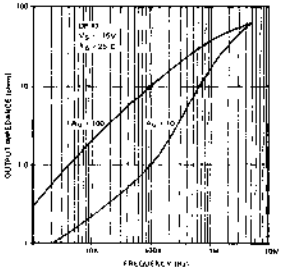
COMMON MODE REJECTION RATIO VS FREQUENCY



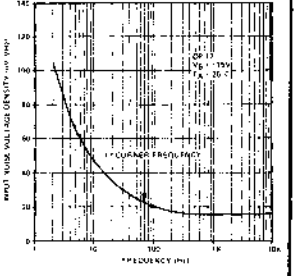
POWER SUPPLY REJECTION VS FREQUENCY



OUTPUT IMPEDANCE VS FREQUENCY



VOLTAGE NOISE VS FREQUENCY



SSS725

INSTRUMENTATION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

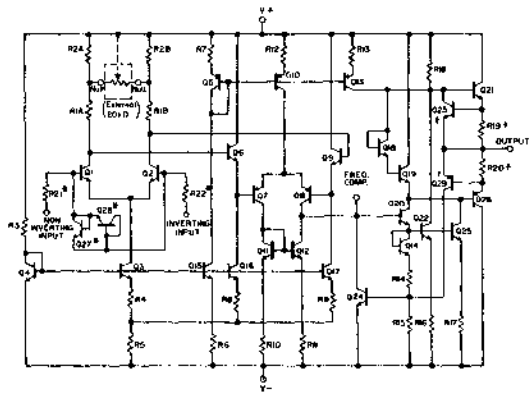
The SSS725 Series of monolithic Instrumentation Operational Amplifiers is specifically designed for accurate high-gain amplification of low level input signals in the presence of large common mode voltages. Superior DC input characteristics include very low offset voltage and current, extremely high open loop gain, low 1/f and wideband noise and a complete absence of "popcorn" noise. The extremely low offset voltage drift is further improved by an advanced nulling technique that provides optimum TCV_{OS} performance when V_{OS} has been nulled to zero. Very high common mode and power supply rejection enable accurate performance in the presence of large spurious signals.

Flexible external compensation provides wide bandwidth and high slew rate operation in high closed-loop gain applications. The superior long term stability, and compatibility with MIL-STD-883 processing make the SSS725 an excellent choice for high reliability process control and aerospace applications, including strain gauge and thermocouple amplifiers, low noise audio amplifiers and instrumentation amplifiers. The SSS725 Series are direct replacements for all 725 types providing superior DC and noise performance plus the unique feature of **complete input differential voltage and output short circuit protection**. Further improvements in input performance plus **complete internal frequency compensation** are available: request the OP-05 Instrumentation and OP-07 Ultra-low Offset Voltage Operational Amplifier data sheets.

FEATURES

- **Very High Voltage Gain . . . . . 1,000 kV/V Min**
- **Low Offset Voltage and Offset Current**
- **Low Drift vs. Temperature (TCV_{OS}). . 0.8 $\mu V/^{\circ}C$ Max**
- **Low Input Voltage and Current Noise**
- **Low Offset Voltage Drift with Time**
- **High Common Mode Rejection . . . . . 120 dB Min**
- **High Power Supply Rejection . . . . . 2 $\mu V/V$ Max**
- **Wide Supply Range . . . . . ±1.5V to ±22V**
- **±30V Input Overvoltage Protection**
- **MIL-STD-883 Processing Available**

SIMPLIFIED SCHEMATIC

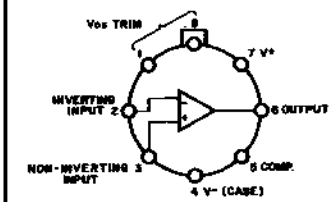


*Q27, Q28, R21, R22 COMPRISE THE INPUT PROTECTION CIRCUIT

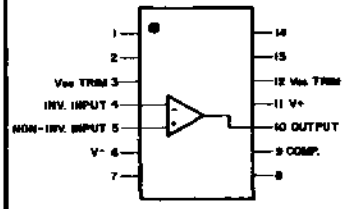
†Q25, Q29, R19, R20 COMPRISE THE OUTPUT PROTECTION CIRCUIT.

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW

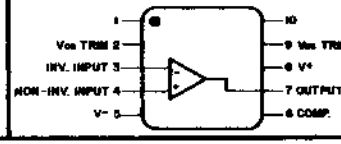


TO-99 (J-Suffix)
ORDER: SSS725AJ
SSS725J
SSS725BJ
SSS725EJ
SSS725CJ



14 PIN DIP (Y-Suffix)*
ORDER: SSS725AY
SSS725Y
SSS725BY
SSS725EY
SSS725CY

*Formerly "P" Suffix



10 PIN FLATPACK
(L-Suffix)
ORDER: SSS725AL
SSS725L
SSS725BL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Operating Temperature Range	
Internal Power Dissipation (Note 1)	500mW	SSS725A, SSS725	−55°C to +125°C
Differential Input Voltage	±30V	SSS725B	−25°C to +85°C
Input Voltage (Note 2)	±22V	SSS725E, SSS725C	0°C to +70°C
Output Short Circuit Duration	Indefinite		
Storage Temperature Range	−65°C to +150°C	Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

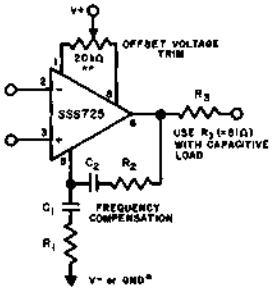
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
DUAL-IN-LINE (Y)	100°C	10.0mW/°C
FLAT (L)	62°C	5.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

FREQUENCY COMPENSATION

COMPENSATION CIRCUIT



COMPENSATION VALUES

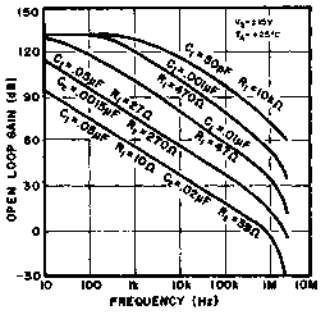
Avcl	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10000	10K	50pF	–	–
1000	470	.001	–	–
100	47	.01	–	–
10	27	.05	270	.0015
1	10	.05	39	.02

*The compensation network (R_1, C_1) should be returned to the V-terminal. If the network is returned to ground, serious degradation of power supply rejection performance with frequency will occur. See typical curves, page 6 (PSRR vs FREQUENCY).

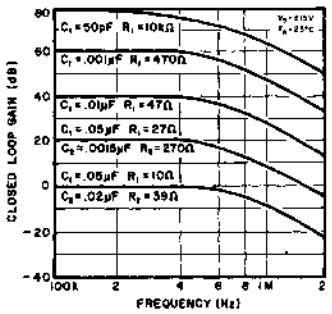
** The trimming potentiometer should be 20KΩ for optimum nulled offset voltage drift. See page 6 for change in drift caused by potentiometers ranging from 5KΩ to 100KΩ.

TYPICAL DYNAMIC PERFORMANCE CURVES

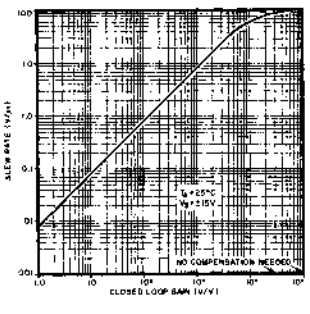
OPEN LOOP RESPONSE FOR VALUES OF COMPENSATION



CLOSED LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION



SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS



ELECTRICAL CHARACTERISTICS			SSS725A			SSS725			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 20k\Omega$	—	0.06	0.1	—	0.2	0.5	mV
Input Offset Current	I_{os}		—	0.3	1.0	—	0.75	5.0	nA
Input Bias Current	I_B		—	30	70	—	30	80	nA
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 1) f_O = 100Hz (Note 1) f_O = 1000Hz (Note 1)	— — —	9.0 8.0 7.0	15.0 9.0 7.5	— — —	9.0 8.0 7.0	15.0 9.0 7.5	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f_O = 10Hz (Note 1) f_O = 100Hz (Note 1) f_O = 1000Hz (Note 1)	— — —	0.5 0.25 0.15	1.2 0.6 0.25	— — —	0.5 0.25 0.15	1.2 0.6 0.25	$pA/\sqrt{Hz}$
Input Resistance	R_{in}		0.8	1.8	—	0.7	1.8	—	MΩ
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	1,000,000	3,000,000	—	1,000,000	3,000,000	—	V/V
Output Voltage Swing	V_{om}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0	±13.0 ±12.8 ±12.5	— — —	±12.5 ±12.0 ±11.0	±13.0 ±12.8 ±12.5	— — —	V V V
Input Voltage Range	CMVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$R_s \leq 20k\Omega$	120	126	—	120	126	—	dB
Power Supply Rejection Ratio	PSRR	$R_s \leq 20k\Omega$	—	0.5	2.0	—	1.0	5.0	μV/V
Power Consumption	P_d		—	90	105	—	105	120	mW
Large Signal Voltage Gain	A_{vo}	$R_L \geq 500\Omega$ V_O=±0.5V V_S=±3V	100,000	600,000	—	100,000	600,000	—	V/V
Power Consumption	P_d	V_S=±3V	—	4	6	—	4	6	mW
The following specifications apply for V_S = ±15V, -55°C $\leq T_A \leq$ +125°C, unless otherwise noted.									
Input Offset Voltage (Without external trim)	V_{os}	$R_s \leq 20k\Omega$	—	0.08	0.18	—	0.3	0.7	mV
Average Input Offset Voltage Drift (without external trim)	TCV_{os}	R_S=50Ω (Note 2)	—	0.3	0.8	—	0.7	2.0	μV/°C
Average Input Offset Voltage Drift (with external trim)	TCV_{osn}	R_S=50Ω (Note 2)	—	0.2	0.6	—	0.28	1.0	μV/°C
Input Offset Current	I_{os}	T_AMAX T_AMIN	— —	0.25 0.8	1.0 4.0	— —	0.6 2.0	4.0 18.0	nA nA
Average Input Offset Current Drift	TCI_{os}		—	3	20	—	8	90	pA/°C
Input Bias Current	I_B	T_AMAX T_A MIN	— —	22 40	60 120	— —	25 45	70 180	nA nA
Common Mode Rejection Ratio	CMRR	$R_s \leq 20k\Omega$	114	124	—	110	122	—	dB
Power Supply Rejection Ratio	PSRR	$R_s \leq 20k\Omega$	—	1.0	5.0	—	2.0	8.0	μV/V
Large Signal Voltage Gain	A_{vo}	V_O=±10V; $R_L \geq 2k\Omega$ T_AMAX T_AMIN	1,000,000 700,000	3,500,000 2,000,000	— —	1,000,000 500,000	3,500,000 1,800,000	— —	V/V
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$,	±12.0	±12.6	—	±12.0	±12.6	—	V

Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.

Note 2: Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.

ELECTRICAL CHARACTERISTICS			SSS725B			
These specifications apply for $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 20k\Omega$	— —	0.3	0.75	mV
Input Offset Current	I_{os}		— —	0.75	5.0	nA
Input Bias Current	I_B		— —	30	80	nA
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 1) f_o = 100Hz (Note 1) f_o = 1000Hz (Note 1)	— — — — — —	9.0 8.0 7.0	15.0 9.0 7.6	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f_o = 10Hz (Note 1) f_o = 100Hz (Note 1) f_o = 1000Hz (Note 1)	— — — — — —	0.5 0.25 0.15	1.2 0.6 0.25	$pA/\sqrt{Hz}$
Input Resistance	R_{in}		0.7	1.8	— —	MΩ
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1,000,000	3,000,000	— —	V/V
Output Voltage Swing	V_{om}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0	±13.0 ±12.8 ±12.5	— — — — — —	V V V
Input Voltage Range	CMVR		±13.5	±14.0	— —	V
Common Mode Rejection Ratio	CMRR	$R_s \leq 20k\Omega$	110	115	— —	dB
Power Supply Rejection Ratio	PSRR	$R_s \leq 20k\Omega$	— —	1.0	5.0	μV/V
Power Consumption	P_d		— —	90	120	mW
Large Signal Voltage Gain	A_{vo}	$R_L \geq 500\Omega$ $V_O = \pm 0.5V$ $V_S = \pm 3V$	100,000	600,000	— —	V/V
Power Consumption	P_d	$V_S = \pm 3V$	— —	4	6	mW
The following specifications apply for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.						
Input Offset Voltage (Without external trim)	V_{os}	$R_s \leq 20k\Omega$	— —	0.4	1.0	mV
Average Input Offset Voltage Drift (without external trim)	TCV_{os}	R_S=50Ω (Note 2)	— —	1.0	7.8 (Note 1)	μV/°C
Average Input Offset Voltage Drift (with external trim)	TCV_{osn}	R_S=50Ω (Note 2)	— —	0.3	1.0 (Note 1)	μV/°C
Input Offset Current	I_{os}	T_A MAX T_A MIN	— — — —	0.7 1.3	5.0 14.0	nA nA
Average Input Offset Current Drift	TCI_{os}		— —	6	90 (Note 1)	pA/°C
Input Bias Current	I_B	T_A MAX T_A MIN	— — — —	30 40	80 150	nA nA
Common Mode Rejection Ratio	CMRR	$R_S \leq 20k\Omega$	106	113	— —	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 20k\Omega$	— —	2.0	8.0	μV/V
Large Signal Voltage Gain	A_{vo}	$V_O = \pm 10V$, $R_L \geq 2k\Omega$ T_A MAX T_A MIN	1,000,000 500,000	3,500,000 2,300,000	— — — —	V/V
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±12.6	— —	V

Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.

Note 2: Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.

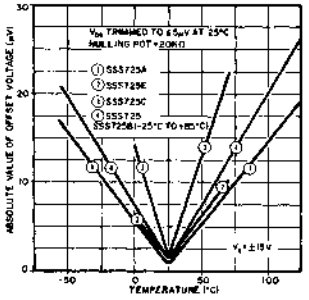
ELECTRICAL CHARACTERISTICS			SSS725E			SSS725C			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{OS}		—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 1) f_O = 100Hz (Note 1) f_O = 1000Hz (Note 1)	— — —	9.0 8.0 7.0	15.0 9.0 7.5	— — —	9.0 8.0 7.0	15.0 9.0 7.5	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f_O = 10Hz (Note 1) f_O = 100Hz (Note 1) f_O = 1000Hz (Note 1)	— — —	0.5 0.25 0.15	1.2 0.6 0.25	— — —	0.6 0.3 0.2	1.4 0.7 0.3	$pA/\sqrt{Hz}$
Input Resistance	R_{in}		0.7	1.8	—	0.5	1.5	—	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	1,000,000	3,000,000	—	500,000	3,000,000	—	V/V
Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0	±13.0 ±12.8 ±12.5	— — —	±12.0 ±11.5 —	±13.0 ±12.8 ±12.0	— — —	V V V
Input Voltage Range	CMVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 20k\Omega$	120	126	—	100	115	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 20k\Omega$	—	1.0	5.0	—	2.0	10	μV/V
Power Consumption	P_d		—	90	120	—	110	150	mW
Large Signal Voltage Gain	A_{VO}	$R_L \geq 600\Omega$ V_O ±0.5V V_S ±3V	100,000	600,000	—	60,000	600,000	—	V/V
Power Consumption	P_D	V_S ±3V	—	4	6	—	4	8	mW
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20k\Omega$	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (without external trim)	TCV_{OS}	R_S 50Ω (Note 2)	—	0.7	2.0 (Note 1)	—	1.4	4.5 (Note 1)	μV/°C
Average Input Offset Voltage Drift (with external trim)	TCV_{OSn}	R_S 50Ω (Note 2)	—	0.2	0.6	—	0.5	1.5 (Note 1)	μV/°C
Input Offset Current	I_{OS}	T_A MAX T_A MIN	— —	0.65 0.9	5.0 7.0	— —	2.0 3.0	15 25	nA nA
Average Input Offset Current Drift	TCI_{OS}		— —	4	40 (Note 1)	— —	14	150 (Note 1)	pA/°C
Input Bias Current	I_B	T_A MAX T_A MIN	— —	30 35	80 100	— —	35 45	110 180	nA nA
Common Mode Rejection Ratio	CMRR	$R_S \leq 20k\Omega$	115	118	—	97	113	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 20k\Omega$	—	1.5	7.0	—	3.0	15	μV/V
Large Signal Voltage Gain	A_{VO}	V_O ±10V; $R_L \geq 2k\Omega$ T_AMAX T_AMIN	1,000,000 800,000	3,200,000 2,700,000	— —	400,000 300,000	3,200,000 2,700,000	— —	V/V
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.

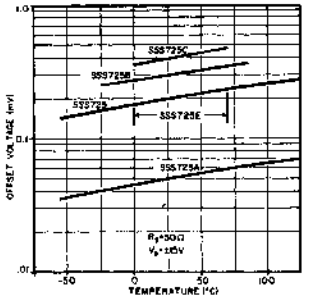
Note 2: Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.

TYPICAL PERFORMANCE CURVES

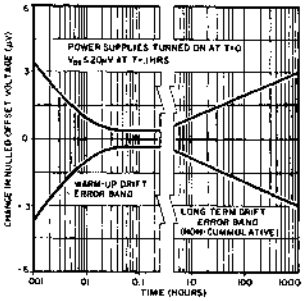
TRIMMED OFFSET VOLTAGE VS TEMPERATURE



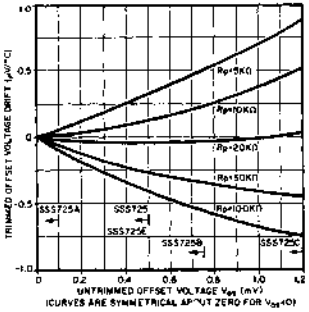
OFFSET VOLTAGE VS TEMPERATURE



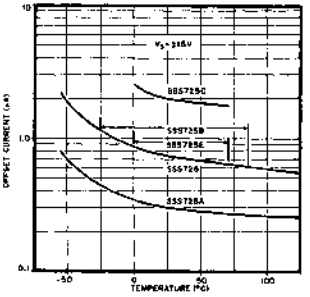
OFFSET VOLTAGE DRIFT WITH TIME



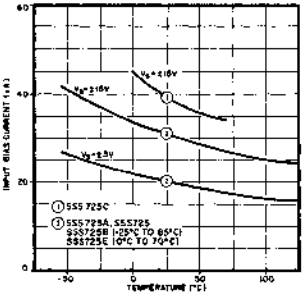
TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER (Rp) SIZE AND V_{OS}



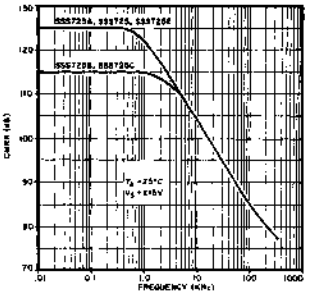
OFFSET CURRENT VS TEMPERATURE



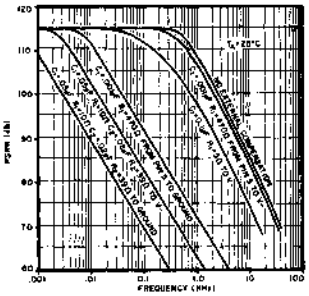
INPUT BIAS CURRENT VS TEMPERATURE



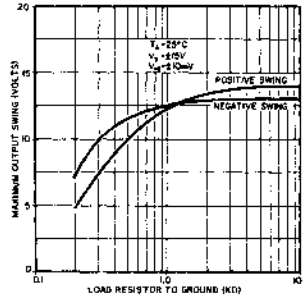
CMRR VS FREQUENCY



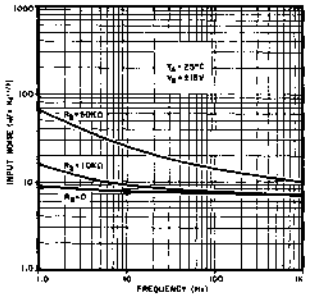
PSRR VS FREQUENCY (SSS725, SSS725B, SSS725E)



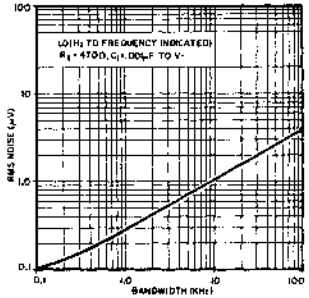
OUTPUT POWER



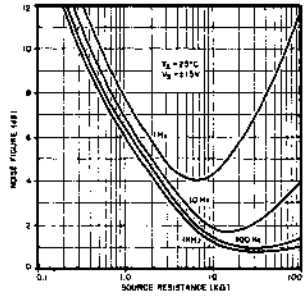
TYPICAL INPUT NOISE VOLTAGE



INPUT WIDEBAND NOISE VS BANDWIDTH



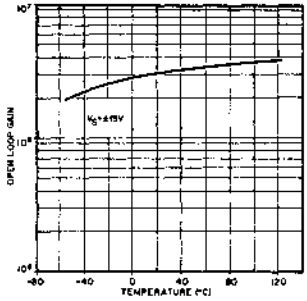
NOISE FIGURE VS SOURCE RESISTANCE



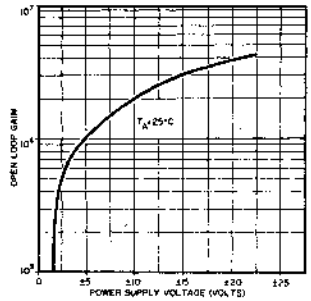
Note: For further information refer to AN-15, "Minimization of Noise in Operational Amplifier Applications."

TYPICAL PERFORMANCE CURVES

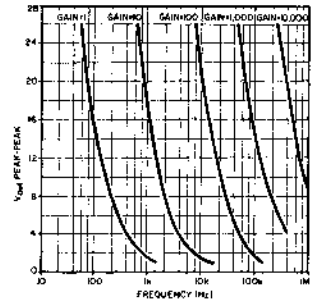
OPEN LOOP GAIN VS TEMPERATURE



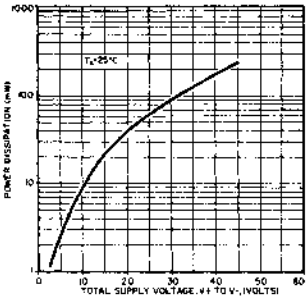
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



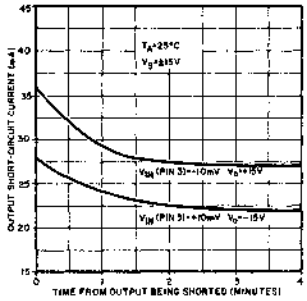
MAXIMUM UNDISTORTED OUTPUT



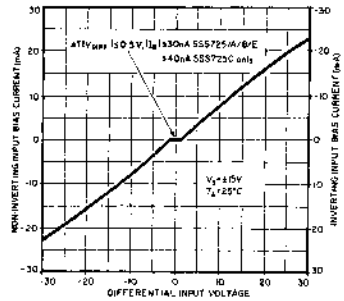
POWER CONSUMPTION VS SUPPLY VOLTAGE



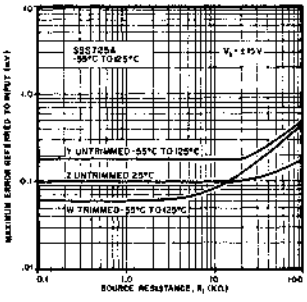
OUTPUT SHORT-CIRCUIT CURRENT

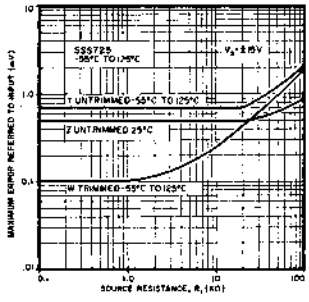


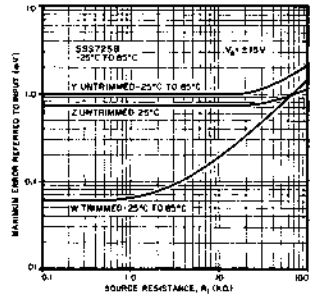
INPUT BIAS CURRENT VS DIFFERENTIAL INPUT VOLTAGE

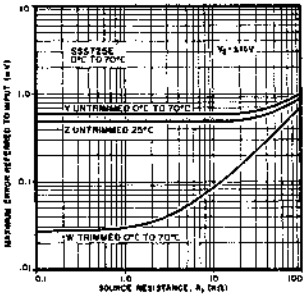


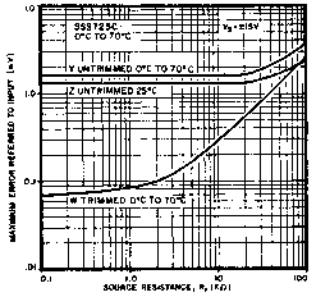
GUARANTEED PERFORMANCE CURVES











These graphs depict maximum error referred to the input as a function of source resistance (R_1). Curves W are shown with V_{OS} trimmed at +25°C and include errors due to V_{OS} and I_{OS} over the indicated temperature range. Curves Y and Z plot maximum errors with V_{OS} not trimmed.

SSS741

COMPENSATED OPERATIONAL AMPLIFIER

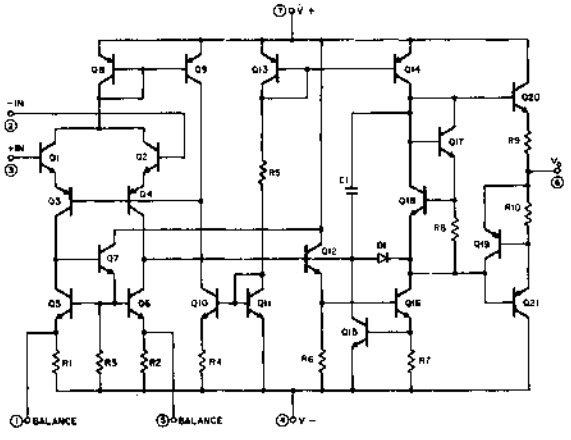
GENERAL DESCRIPTION

The SSS741 Series of Internally Compensated Operational Amplifiers provides significant performance improvement while retaining full pin-for-pin interchangeability with industry-standard general-purpose types. Improved offset voltage, bias current, bandwidth and noise performance enable immediate system performance upgrading without redesign and eliminate costly special selections. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. The SSS741 Series is ideal for use in summing amplifiers, integrators, active filters and in other circuits where improved dynamic performance and accuracy are required. SSS741's with processing per the requirements of MIL 38510/883 are available. For dual versions, see the SSS747 Series data sheet. For very high performance general purpose operational amplifiers, refer to the OP-02 Series data sheet.

FEATURES

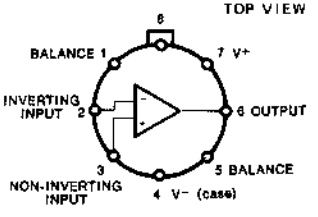
- Improved DC Specifications
- Low Input Bias Current. . . . . 50 nA Max
- High Large Signal Voltage Gain . . . Up to 100 kV/V
- Internal Frequency Compensation
- Large Common Mode Voltage Range . . . . . ±12V
- Low Power Consumption . . . . . 85 mW Max
- Continuous Short Circuit Protection
- MIL-STD-883A Processing Available
- Silicon-Nitride Passivation

SCHEMATIC DIAGRAM

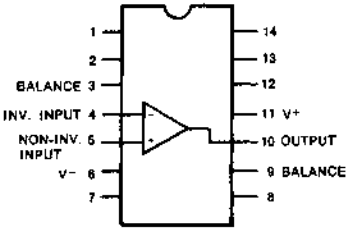


CIRCLED NUMBERS CORRESPOND TO TO-99 PIN CONFIGURATION

PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)
ORDER: SSS741J
SSS741GJ
SSS741BJ
SSS741CJ



14 PIN DIP (Y-Suffix)
ORDER: SSS741Y
SSS741GY
SSS741BY
SSS741CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: SSS741-883-J SSS741-883-GJ
SSS741-883-Y SSS741-883-GY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- SSS741, SSS741B, SSS741G ±22V
- SSS741C ±18V

Internal Power Dissipation (Note 1) 500 mW
Differential Input Voltage ±30V
Input Voltage Supply Voltage
Output Short Circuit Duration Indefinite
Storage Temperature Range −65°C to +150°C

Operating Temperature Range
- SSS741, SSS741G −55°C to +125°C
- SSS741B −25°C to +85°C
- SSS741C 0°C to +70°C

Lead Temperature Range (Soldering, 60 sec) 300°C

NOTES:

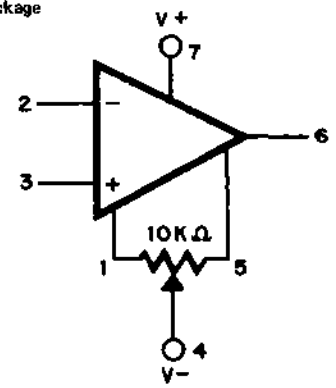
Note 1: Maximum package power dissipation vs. ambient temperature

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
DUAL-IN-LINE (Y)	100°C	10.0mW/°C

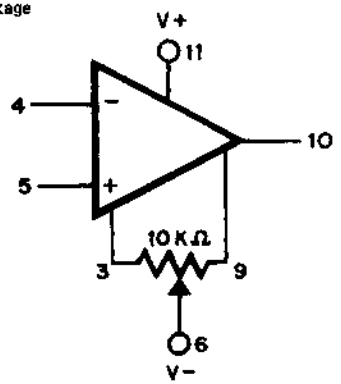
ELECTRICAL CHARACTERISTICS			SSS741		SSS741G		
These specifications apply for T_A = 25°C			±5V ≤ V_S ≤ ±20V unless otherwise noted		±5V ≤ V_S ≤ ±15V unless otherwise noted		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S ≤ 50kΩ	–	3.0	–	3.0	mV
Input Offset Current	I_{OS}		–	25	–	25	nA
Input Bias Current	I_B		–	100	–	100	nA
Input Resistance	R_{IN}		1.0	–	1.0	–	MΩ
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_S = ±15V V_O = ±10V	25,000	–	25,000	–	V/V
Output Voltage Swing	V_{OM}	V_S = ±15V R_L ≥ 10kΩ R_L ≥ 2kΩ	±12 ±10	– –	±12 ±10	– –	V V
Input Voltage Range	CMVR	V_S = ±15V	±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	R_S ≤ 50kΩ	70	–	70	–	dB
Power Supply Rejection Ratio	PSRR	R_S ≤ 50kΩ	–	150	–	150	μV/V
Power Consumption	P_D	V_S = ±15V	–	85	–	85	mW
The following specifications apply for −55°C ≤ T_A ≤ +125°C			±5V ≤ V_S ≤ ±20V unless otherwise noted		±5V ≤ V_S ≤ ±15V unless otherwise noted		
Input Offset Voltage	V_{OS}	R_S ≤ 50kΩ	–	3.0	–	6.0	mV
Input Offset Current	I_{OS}		–	10	–	50	nA
Input Bias Current	I_B		–	100	–	200	nA
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_S = ±15V V_O = ±10V	50,000	–	25,000	–	V/V
Output Voltage Swing	V_{OM}	R_L ≥ 10kΩ R_L ≥ 2kΩ V_S = ±15V	±12 ±10	–	±12 ±10	–	V V
Common Mode Rejection Ratio	CMRR	R_S ≤ 50kΩ	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	R_S ≤ 50kΩ	–	100	–	150	μV/V

BALANCING CIRCUIT

J-Package



Y-Package



ELECTRICAL CHARACTERISTICS			SSS741B		SSS741C		
These specifications apply for $T_A = 25°C$			$\pm5V \leq V_S \leq \pm20V$ unless otherwise specified		$V_S = \pm15V$		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	3.0	–	6.0	mV
Input Offset Current	I_{OS}		–	5.0	–	25	nA
Input Bias Current	I_B		–	50	–	100	nA
Input Resistance	R_{IN}		2.0	–	1.0	–	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_S = \pm15V$ $V_O = \pm10V$	50,000	–	25,000	–	V/V
Output Voltage Swing	V_{OM}	$V_S = \pm15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	– –	±12 ±10	– –	V V
Input Voltage Range	CMVR	$V_S = \pm15V$	±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	100	–	150	μV/V
Power Consumption	P_D	$V_S = \pm15V$	–	85	–	85	mW
The following specifications apply for $-25°C \leq T_A \leq +85°C$ – SSS741B $0°C \leq T_A \leq +70°C$ – SSS741C			$\pm5V \leq V_S \leq \pm20V$ unless otherwise specified		$V_S = \pm15V$		
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	4.0	–	7.5	mV
Input Offset Current	I_{OS}		–	10	–	50	nA
Input Bias Current	I_B		–	100	–	200	nA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_S = \pm15V$ $V_O = \pm10V$	25,000	–	15,000	–	V/V
Output Voltage Swing	V_{OM}	$V_S = \pm15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	– –	±12 ±10	– –	V V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	80	–	–	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	100	–	–	μV/V

SSS747

DUAL COMPENSATED OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

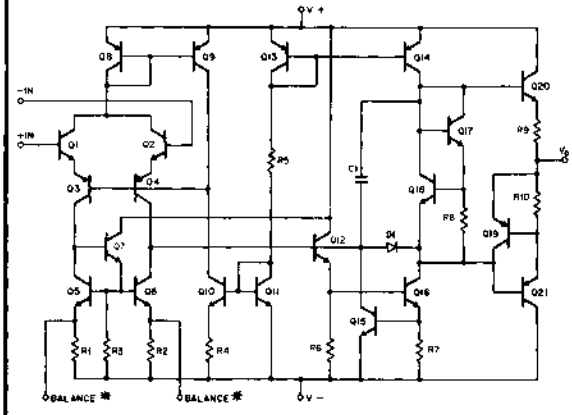
The SSS747 Series of Internally Compensated Dual Operational Amplifiers provides significant performance improvements while retaining full pin-for-pin interchangeability with industry-standard general-purpose types. Improved offset voltages, bias current, bandwidth and noise performance enable immediate system performance upgrading without redesign and eliminate costly special selections. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. The SSS747 is ideal for use in summing amplifiers, integrators, active filters and in other circuits where improved performance and accuracy are required. For very high performance dual operational amplifiers with the same pinout as SSS747, see the OP-04 data sheet.

FEATURES

- Improved D.C. Specifications
- Low Input Bias Current
- High Large Signal Voltage Gain
- Internal Frequency Compensation
- Large Common Mode Voltage Range
- Low Power Consumption
- Continuous Short Circuit Protection
- MIL-STD-883A Processing Available
- Silicon-Nitride Passivation

SCHEMATIC DIAGRAM

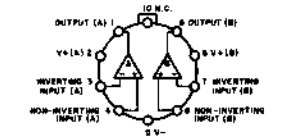
(1/2 OF CIRCUIT SHOWN)



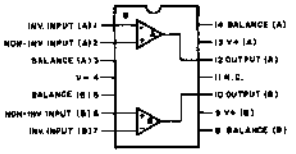
* DIP AND FLATPACK ONLY

PIN CONNECTIONS AND ORDERING INFORMATION

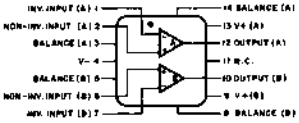
TOP VIEW



TO-100 (K-Suffix)
ORDER: SSS747K
SSS747GK
SSS747BK
SSS747CK



14 PIN DIP (Y-Suffix)
ORDER: SSS747Y
SSS747GY
SSS747BY
SSS747CY



14 LEAD
FLATPACK (M-Suffix)
ORDER: SSS747M
SSS747GM
SSS747BM

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: SSS747-883-K SSS747-883-GK
SSS747-883-Y SSS747-883-GY
SSS747-883-M SSS747-883-GM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to 150°C
Operating Temperature Range	
SSS747, SSS747G	−55°C to +125°C
SSS747B	−25°C to +85°C
SSS747C	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

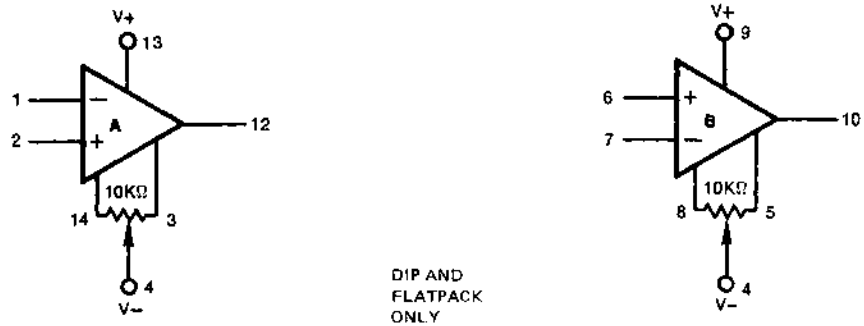
PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
DUAL-IN-LINE (Y)	100°C	10.0mW/°C
TO-100 (K)	80°C	7.1mW/°C
14-LEAD FLATPACK (M)	62°C	5.7mW/°C

ELECTRICAL CHARACTERISTICS (Each Amplifier)

These specifications apply for T_A = 25°C.

Parameter	Symbol	Test Conditions	SSS747 ±5V ≤ V_S ≤ ±20V unless otherwise noted Min	SSS747 Max	SSS747G ±5V ≤ V_S ≤ ±15V unless otherwise noted Min	SSS747G Max	Units
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	2.0	–	5.0	mV
Input Offset Current	I_{OS}		–	5.0	–	25	nA
Input Bias Current	I_B		–	50	–	100	nA
Input Resistance	R_{IN}		2.0	–	1.0	–	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_S = ±15V V_O = ±10V	100,000	–	50,000	–	V/V
Output Voltage Swing	V_{OM}	V_S = ±15V $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	– –	±12 ±10	– –	V V
Input Voltage Range	CMVR	V_S = ±15V	+12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	100	–	150	μV/V
Power Consumption	P_D	V_S = ±15V	–	85	–	85	mW
Channel Separation	CS		100	–	80	–	dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C.			±5V ≤ V_S ≤ ±20V unless otherwise noted		±5V ≤ V_S ≤ ±15V unless otherwise noted		
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	3.0	–	6.0	mV
Input Offset Current	I_{OS}		–	10	–	50	nA
Input Bias Current	I_B		–	100	–	200	nA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_S = ±15V V_O = ±10V	50,000	–	25,000	–	V/V
Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ V_S = ±15V	±12 ±10	–	±12 ±10	–	V V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	100	–	150	μV/V

BALANCING CIRCUIT



ELECTRICAL CHARACTERISTICS (Each Amplifier)			SSS747B		SSS747C		
These specifications apply for $T_A = 25°C$.			$\pm5V \leq V_S \leq \pm20V$ unless otherwise specified		$\pm5V \leq V_S \leq \pm15V$ unless otherwise specified		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	3.0	–	5.0	mV
Input Offset Current	I_{OS}		–	5.0	–	25	nA
Input Bias Current	I_B		–	50	–	100	nA
Input Resistance	R_{IN}		2.0	–	1.0	–	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_S = \pm15V$ $V_O = \pm10V$	50,000	–	50,000	–	V/V
Output Voltage Swing	V_{OM}	$V_S = \pm15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	– –	±12 ±10	– –	V V
Input Voltage Range	CMVR	$V_S = \pm15V$	±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	100	–	150	μV/V
Power Consumption	P_D	$V_S = \pm15V$	–	85	–	85	mW
Channel Separation	CS		100	–	80	–	dB
The following specifications apply for $-25°C \leq T_A \leq +85°C$ – SSS747B and $0°C \leq T_A \leq +70°C$ – SSS747C.			$\pm5V \leq V_S \leq \pm20V$ unless otherwise specified		$\pm5V \leq V_S \leq \pm15V$ unless otherwise specified		
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	4.0	–	6.0	mV
Input Offset Current	I_{OS}		–	10	–	50	nA
Input Bias Current	I_B		–	100	–	200	nA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_S = \pm15V$ $V_O = \pm10V$	25,000	–	25,000	–	V/V
Output Voltage Swing	V_{OM}	$V_S = \pm15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	–	±12 ±10	–	V V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	100	–	150	μV/V

SSS1458/1558

DUAL COMPENSATED OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

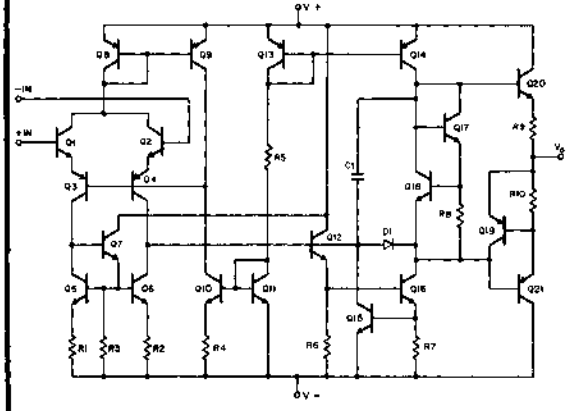
The SSS1458/1558 Series of Internally Compensated Dual Operational Amplifiers provides significant performance improvements while retaining full pin-for-pin interchangeability with industry-standard types. Improved offset voltages, bias current, bandwidth and noise performance enable immediate system performance upgrading without redesign and eliminate costly special selections. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. The SSS1458/1558 is ideal for use in summing amplifiers, integrators, active filters and in other circuits where improved performance and accuracy are required. For very high performance dual operational amplifiers with the same pinout as SSS1458/1558, see the OP-14 data sheet.

FEATURES

- Improved D.C. Specifications
- Low Input Bias Current . . . . . <100nA
- High Large Signal Voltage Gain . . . . . >50,000
- Internal Frequency Compensation
- Large Common Mode Voltage Range . . . . . >±12V
- Low Power Consumption . . . . . <85mW
- Continuous Short Circuit Protection
- MIL-STD-883A Processing Available
- Silicon-Nitride Passivation . . . . . Low Noise

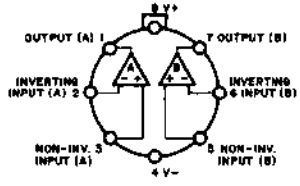
SCHEMATIC DIAGRAM

(1/2 OF CIRCUIT SHOWN)



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: SSS1558J
SSS1458J

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Lead Temperature Range (Soldering, 60 sec)	300°C
Internal Power Dissipation (Note)	500 mW	Operating Temperature Range	
Differential Input Voltage	±30V	SSS1558	−55°C to +125°C
Input Voltage	Supply Voltage	SSS1458	0°C to +70°C
Output Short Circuit Duration	Indefinite		
Storage Temperature Range	−65°C to +150°C	NOTE: Derate at 7.1 mW/°C above 80°C.	

ELECTRICAL CHARACTERISTICS (Each Amplifier)			SSS1558		SSS1458		
These specifications apply for T_A = 25°C and ±5V ≤ V_S ≤ ±15V, unless otherwise noted.							
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	5.0	–	5.0	mV
Input Offset Current	I_{OS}		–	25	–	25	nA
Input Bias Current	I_B		–	100	–	100	nA
Input Resistance	R_{IN}		1.0	–	1.0	–	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_S = ±15V V_O = ±10V	50,000	–	50,000	–	V/V
Output Voltage Swing	V_{OM}	V_S = ±15V $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	– –	±12 ±10	– –	V V
Input Voltage Range	CMVR	V_S = ±15V	±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	70	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	150	–	150	μV/V
Power Consumption	P_D	V_S = ±15V	–	85	–	85	mW
Channel Separation	CS		80	–	80	–	dB
The following specifications apply for ±5V ≤ V_S ≤ ±15V, −55°C ≤ T_A ≤ +125°C for SSS1558, and 0°C ≤ T_A ≤ +70°C for SSS1458 unless otherwise noted.							
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	6.0	–	6.0	mV
Input Offset Current	I_{OS}		–	50	–	50	nA
Input Bias Current	I_B		–	200	–	200	nA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_S = ±15V V_O = ±10V	25,000	–	25,000	–	V/V
Output Voltage Swing	V_{OM}	V_S = ±15V $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	–	±12 ±10	–	V V
Common Mode Rejection Ratio	CMRR	$R_S \leq 50k\Omega$	70	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50k\Omega$	–	150	–	150	μV/V

PM108A

LOW INPUT CURRENT OPERATIONAL AMPLIFIER

PM108A / PM208A / PM308A / PM108 / PM208 / PM308

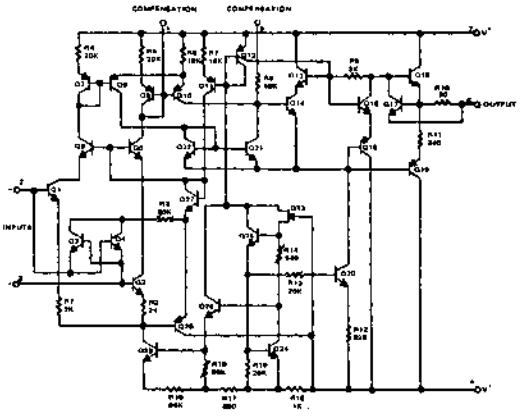
GENERAL DESCRIPTION

The PM108A Series of precision monolithic operational amplifiers features extremely low input offset and bias currents. Although directly interchangeable with industry-standard types, Precision Monolithics' advanced processing technique provides a significant improvement in input noise voltage. Low supply current drain over a wide power supply range makes the PM108A attractive in battery operated and other low power applications. Low offset current and low bias current provide excellent performance in high impedance circuits such as long period integrators, sample-and-holds, and with piezoelectric and capacitive transducers.

FEATURES

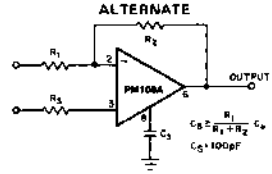
- Low Offset Current . . . . . 200pA Max
- Low Bias Current . . . . . 2.0nA Max
- Low Power Consumption . . . . . 18mW Max @ ±15V
- Low Offset Voltage Drift . . . . . 5.0μV/°C Max
- High Common Mode Input Range . . . . ±13.5V Min
- MIL-STD-883A Class B Processing Models Available
- Silicon-Nitride Passivation

SIMPLIFIED SCHEMATIC



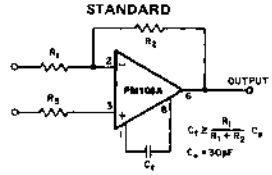
COMPENSATION CIRCUITS

ALTERNATE



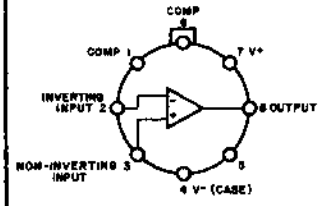
(Improves rejection of power supply noise by a factor of ten)

STANDARD



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: PM108AJ/PM108J
PM208AJ/PM208J
PM308AJ/PM308J

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: PM108-883-AJ
PM108-883-J

ABSOLUTE MAXIMUM RATINGS

NOTE 1: Maximum package power dissipation vs. ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C

NOTE 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.

NOTE 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS

These specifications apply for $\pm 5V \leq V_S \leq \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

Parameter	Symbol	Conditions	PM308A Min	PM308A Typ	PM308A Max	PM308 Min	PM308 Typ	PM308 Max	Units
Input Offset Voltage	V_{os}		–	0.3	0.5	–	2.0	7.5	mV
Input Offset Current	I_{os}		–	0.2	1.0	–	0.2	1.0	nA
Input Bias Current	I_B		–	1.5	7.0	–	1.5	7.0	nA
Input Resistance	R_{in}		10	40	–	10	40	–	MΩ
Large Signal Voltage Gain	A_{vo}	$V_s = \pm 15V$, $V_{out} = \pm 10V$, $R_L \geq 10k\Omega$	80	300	–	25	300	–	V/mV
Supply Current	I_s	$I_{out} = 0$, $V_{out} = 0$	–	0.3	0.8	–	0.3	0.8	mA
The following specifications apply for $\pm 5V \leq V_s \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ unless otherwise noted.									
Input Offset Voltage	V_{os}		–	0.4	0.73	–	3.0	10.0	mV
Average Input Offset Voltage Drift	TCV_{os}		–	1.0	5.0	–	6.0	30	µV/°C
Input Offset Current	I_{os}		–	0.3	1.5	–	0.3	1.5	nA
Average Input Offset Current Drift	TCI_{os}		–	2.0	10	–	2.0	10	pA/°C
Input Bias Current	I_B		–	2.0	10	–	2.0	10	nA
Large Signal Voltage Gain	A_{vo}	$V_s = \pm 15V$, $V_{out} = \pm 10V$, $R_L \geq 10k\Omega$	60	200	–	15	100	–	V/mV
Output Voltage Swing	V_{oM}	$V_s = \pm 15V$, $R_L = 10k\Omega$	±13	±14	–	±13	±14	–	V
Input Voltage Range	CMVR	$V_s = \pm 15V$	±14	–	–	±14	–	–	V
Common Mode Rejection Ratio	CMRR		96	110	–	80	100	–	dB
Supply Voltage Rejection Ratio	PSRR		96	110	–	80	96	–	dB
Supply Current	I_s	$V_{out} = 0$, $T_A = MAX$	–	0.23	–	–	0.23	–	mA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		Operating Temperature Range	
PM108A, 108, 208A, 208	±20V	PM108A, PM108	−55°C to +125°C
PM308A, 308	±18V	PM208A, PM208	−25°C to +85°C
Internal Power Dissipation (Note 1)	500mW	PM308A, PM308	0°C to +70°C
Differential Input Current (Note 2)	±10mA	Storage Temperature Range	−65°C to +150°C
Input Voltage (Note 3)	±15V	Lead Temperature Range	
Output Short Circuit Duration	Indefinite	(Soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for $\pm 5V \leqslant V_s \leqslant \pm 20V$ and $T_A = 25°C$ unless otherwise noted.

Parameter	Symbol	Conditions	PM108A PM208A Min	PM108A PM208A Typ	PM108A PM208A Max	PM108 PM208 Min	PM108 PM208 Typ	PM108 PM208 Max	Units
Input Offset Voltage	V_{os}		–	0.3	0.5	–	0.7	2.0	mV
Input Offset Current	I_{os}		–	0.05	0.2	–	0.05	0.2	nA
Input Bias Current	I_B		–	0.8	2.0	–	0.8	2.0	nA
Input Resistance	R_{in}		30	70	–	30	70	–	MΩ
Large Signal Voltage Gain	A_{vo}	$V_s = \pm 15V$, $V_{out} = \pm 10V$, $R_L \geqslant 10k\Omega$	80	300	–	50	300	–	V/mV
Supply Current	I_s	$I_{out} = 0$, $V_{out} = 0$	–	0.3	0.6	–	0.3	0.6	mA
The following specifications apply for $\pm 5V \leqslant V_S \leqslant \pm 20V$, $-55°C \leqslant T_A \leqslant +125°C$ for PM108 and PM108A, $-25°C \leqslant T_A \leqslant +85°C$ for PM208 and PM208A, unless otherwise noted.									
Input Offset Voltage	V_{os}		–	0.4	1.0	–	1.0	3.0	mV
Average Input Offset Voltage Drift	TCV_{os}		–	1.0	5.0	–	3.0	15	µV/°C
Input Offset Current	I_{os}		–	0.1	0.4	–	0.1	0.4	nA
Average Input Offset Current Drift	TCI_{os}		–	0.5	2.5	–	0.5	2.5	pA/°C
Input Bias Current	I_B		–	1.0	3.0	–	1.0	3.0	nA
Large Signal Voltage Gain	A_{vo}	$V_s = \pm 15V$, $V_{out} = \pm 10V$ $R_L \geqslant 10k\Omega$	40	200	–	25	200	–	V/mV
Output Voltage Swing	V_{oM}	$V_s = \pm 15V$, $R_L = 10k\Omega$	±13	±14	–	±13	±14	–	V
Input Voltage Range	CMVR	$V_s = \pm 15V$	±13.5	–	–	±13.5	–	–	V
Common Mode Rejection Ratio	CMRR		96	110	–	85	100	–	dB
Supply Voltage Rejection Ratio	PSRR		96	110	–	80	96	–	dB
Supply Current	I_s	$V_{out} = 0$, $T_A = MAX$	–	0.15	0.4	–	0.15	0.4	mA

PM155A

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIER

PM155A/PM355A/PM155/PM255/PM355

LOW SUPPLY CURRENT

GENERAL DESCRIPTION

The PM155 Series provides low input current, high slew rate, and direct interchangeability with LF155 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. A JFET-input design enables operation with ±40V input voltages eliminating the blowout problems associated with MOSFET devices.

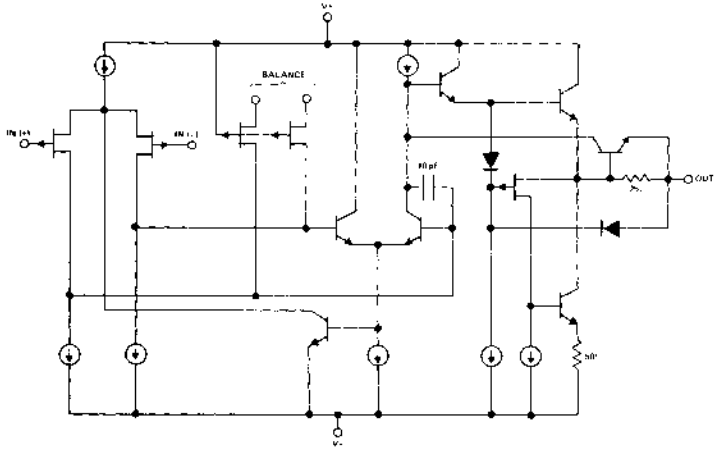
High accuracy, low supply current, and low cost make the PM155 Series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common mode rejection ratio or input offset voltage drift. Dynamic specifications include a slew rate of 5V/μsec, a 2.5MHz gain bandwidth product, and settling time to within ±0.01% of final value of 4.0μsec. In addition, low input voltage noise and current noise plus a low 1/f noise corner frequency allow this amplifier to be used in a variety of low noise, low power applications.

FEATURES

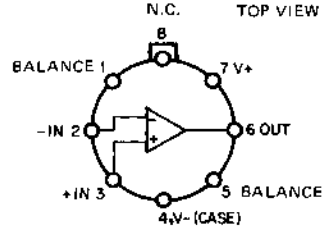
- LF155 Series Direct Replacements
- Low Input Bias and Offset Currents
- Low Supply Current 2mA
- Fast Settling to ±0.01% 4.0μsec
- Internal Compensation
- Low Input Offset Voltage 1.0mV
- Low Input Offset Voltage Drift . . . . . 3.0μV/°C
- Low Input Noise Current . . . . . 0.01pA/√Hz
- High Common Mode Rejection Ratio 100dB
- High Open Loop Gain 106dB
- Models With MIL-STD-883A Class B
- Processing Available From Stock

Applications include instrumentation amplifiers, integrators, log amps, photocell amplifiers, and notch filters. For other JFET operational amplifiers, see the PM156A and PM157A data sheets

SIMPLIFIED SCHEMATIC DIAGRAM



PIN CONNECTIONS



TO-99 (J-Suffix)

ORDERING INFORMATION

ORDER: PM155AJ
PM155J
PM255J
PM355AJ
PM355J

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: PM155-883-AJ
PM155-883-J

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- PM155A, PM155, PM255, PM355A: ±22V
- PM355: ±18V

Internal Power Dissipation
- PM155A, PM155: 670mW
- PM255: 570mW
- PM355A, PM355: 500mW

(The TO-99(J) package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.)

Operating Temperature Range
- PM155A, PM155: -55°C to +125°C
- PM255: -25°C to +85°C
- PM355A, PM355: 0°C to +70°C

Maximum Junction Temperature (T_j)
- PM155A, PM155: +150°C
- PM255: +115°C
- PM355A, PM355: +100°C

Differential Input Voltage
- PM155A, PM155, PM255, PM355A: ±40V
- PM355: ±30V

Input Voltage
- PM155A, PM155, PM255, PM355A: ±20V
- PM355: ±16V

(Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: -65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for $\pm15V \leq V_S \leq \pm20V$, $T_A = +25°C$ unless otherwise noted.

Parameter	Symbol	Test Conditions	PM155A Min	PM155A Typ	PM155A Max	PM355A Min	PM355A Typ	PM355A Max	Units
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	1.0	2.0	–	1.0	2.0	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)	–	3.0	10	–	3.0	10	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)	–	30	50	–	30	50	pA
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$, $R_L = 2K\Omega$	50	200	–	50	200	–	V/mV
Supply Current	I_S	$V_S = \pm15V$	–	2.0	4.0	–	2.0	4.0	mA
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm15V$	3.0	5.0	–	3.0	5.0	–	V/μsec
Gain Bandwidth Product	GBW	$V_S = \pm15V$	–	2.5	–	–	2.5	–	MHz
Settling Time to 0.01%	t_S	$V_S = \pm15V$ (Note 2)	–	4.0	–	–	4.0	–	μsec
Input Noise Voltage	e_n	$R_S=100\Omega$, f=100Hz, $V_S=\pm15V$	–	25	–	–	25	–	$nV\sqrt{Hz}$
		$R_S=100\Omega$, f=1000Hz, $V_S=\pm15V$	–	20	–	–	20	–	$nV\sqrt{Hz}$
Input Noise Current	i_n	f = 100Hz, $V_S = \pm15V$	–	0.01	–	–	0.01	–	$pA\sqrt{Hz}$
		f = 1000Hz, $V_S = \pm15V$	–	0.01	–	–	0.01	–	$pA\sqrt{Hz}$
Input Capacitance	C_{in}		–	3.0	–	–	3.0	–	pF

These specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ for PM155A, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$ for PM355A, unless otherwise noted.

Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	–	–	2.5	–	–	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	–	3.0	5.0	–	3.0	5.0	μV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\frac{\Delta TCV_{OS}}{\Delta V_{OS}}$	$R_S = 50\Omega$	–	0.5	–	–	0.5	–	μV/°C per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	–	–	10	–	–	1.0	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (Note 1)	–	–	25	–	–	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_S=\pm15V$, $V_O=\pm10V$, $R_L=2K\Omega$	25	–	–	25	–	–	V/mV
Output Voltage Swing	V_{OM}	$V_S = \pm15V$, $R_L = 10K\Omega$	±12	±13	–	±12	±13	–	V
		$V_S = \pm15V$, $R_L = 2K\Omega$	±10	±12	–	±10	±12	–	V
Input Voltage Range	CMVR	$V_S = \pm15V$	±11	+15.1 -12.0	–	±11	+15.1 -12.0	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	85	100	–	85	100	–	dB
Power Supply Rejection Ratio	PSRR	(Note 3)	85	100	–	85	100	–	dB

NOTE 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum. I_B and I_{OS} are measured at $V_{CM} = 0$.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value form the time a 10V step input is applied to the inverter. See settling time test circuit on page 4.

NOTE 3: Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS

These specifications apply for T_A = +25°C, ±15V ≤ V_s ≤ ±20V for PM155 and PM255, V_s = ±15V for PM355, unless otherwise noted.

Parameter	Symbol	Test Conditions	PM155 PM255 Min	PM155 PM255 Typ	PM155 PM255 Max	PM355 Min	PM355 Typ	PM355 Max	Units
Input Offset Voltage	V_{os}	R_S = 50Ω	–	3.0	5.0	–	3.0	10	mV
Input Offset Current	I_{os}	T_j = 25°C (Note 1)	–	3.0	20	–	3.0	50	pA
Input Bias Current	I_B	T_j = 25°C (Note 1)	–	30	100	–	30	200	pA
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{vo}	V_s = ±15V, V_O = ±10V, R_L = 2KΩ	50	200	–	25	200	–	V/mV
Supply Current	I_s		–	2.0	4.0	–	2.0	4.0	mA
Slew Rate	SR	A_{VCL} = +1, V_s = ±15V	–	5.0	–	–	5.0	–	V/μsec
Gain Bandwidth Product	GBW	V_s = ±15V	–	2.5	–	–	2.5	–	MHz
Settling Time to 0.01%	t_s	V_s = ±15V (Note 2)	–	4.0	–	–	4.0	–	μsec
Input Noise Voltage	e_n	R_S=100Ω, f=100Hz, V_s=±15V	–	25	–	–	25	–	$nV\sqrt{Hz}$
		R_S=100Ω, f=1000Hz, V_s=±15V	–	20	–	–	20	–	$nV\sqrt{Hz}$
Input Noise Current	i_n	f = 100Hz, V_s = ±15V	–	0.01	–	–	0.01	–	$pA\sqrt{Hz}$
		f = 1000Hz, V_s = ±15V	–	0.01	–	–	0.01	–	$pA\sqrt{Hz}$
Input Capacitance	C_{in}		–	3.0	–	–	3.0	–	pF

These specifications apply for ±15V ≤ V_s ≤ ±20V for PM155 and PM255, V_s = ±15V for PM355, -55°C ≤ T_A ≤ +125°C for PM155, -25°C ≤ T_A ≤ +85°C for PM255, 0°C ≤ T_A ≤ +70°C for PM355, unless otherwise noted.

Input Offset Voltage	V_{os}	R_S = 50Ω, PM155	–	–	7.0	–	–	–	mV
		R_S = 50Ω, PM255	–	–	6.5	–	–	–	mV
		R_S = 50Ω, PM355	–	–	–	–	–	13	mV
Input Offset Voltage Drift	TCV_{os}	R_S = 50Ω	–	5.0	–	–	5.0	–	μV/°C
Change in Input Offset Drift with V_{os} Adjust	$\frac{\Delta TCV_{os}}{\Delta V_{os}}$	R_S = 50Ω	–	0.5	–	–	0.5	–	μV/°C per mV
Input-Offset Current (Note 1)	I_{os}	PM155, T_j ≤ +125°C	–	–	20	–	–	–	nA
		PM255, T_j ≤ +85°C	–	–	1.0	–	–	–	nA
		PM355, T_j ≤ +70°C	–	–	–	–	–	2.0	nA
Input Bias Current (Note 1)	I_B	PM155, T_j ≤ +125°C	–	–	50	–	–	–	nA
		PM255, T_j ≤ +85°C	–	–	5.0	–	–	–	nA
		PM355, T_j ≤ +70°C	–	–	–	–	–	8.0	nA
Large Signal Voltage Gain	A_{vo}	V_s=±15V, V_o=±10V, R_L=2KΩ	25	–	–	15	–	–	V/mV
Output Voltage Swing	V_{om}	V_s = ±15V, R_L = 10KΩ	±12	±13	–	±12	±13	–	V
		V_s = ±15V, R_L = 2KΩ	±10	±12	–	±10	±12	–	V
Input Voltage Range	CMVR	V_s = ±15V	±11	+15.1 -12.0	–	±10	+15.1 -12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	(Note 3)	85	100	–	80	100	–	dB

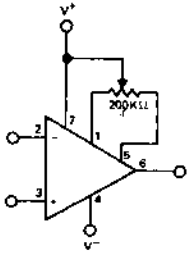
NOTE 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum. I_B and I_{os} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit on page 4.

NOTE 3: Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

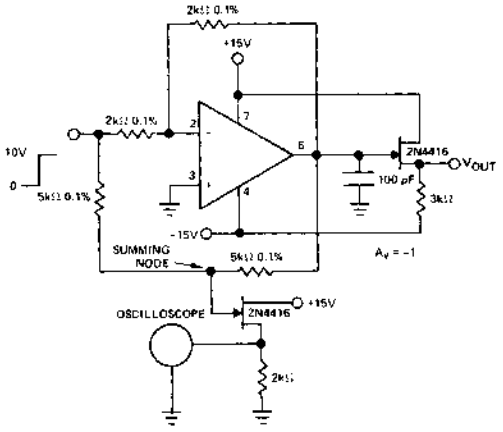
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: For potentiometers with a temperature coefficient ≤100ppm/°C, the added TCV_{OS} with nulling is ≈0.5μV/°C/mV of adjustment.

SETTLING TIME TEST CIRCUIT



APPLICATION INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM155 JFET input stage can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V− can result in a destroyed unit.

If both inputs exceed the negative common mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PM156A

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIER

PM156A/PM356A/PM156/PM256/PM356
WIDE BANDWIDTH

GENERAL DESCRIPTION

The PM156 Series provides low input current, high slew rate, and direct interchangeability with LF156 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. A JFET-input design enables operation with ±40V input voltages eliminating the blowout problems associated with MOSFET devices.

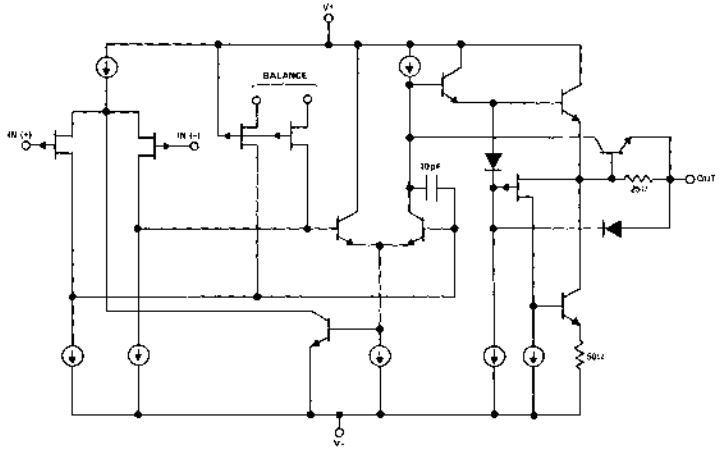
High accuracy, excellent dynamic performance, and low cost make the PM156 Series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common mode rejection ratio or input offset voltage drift. Dynamic specifications include a slew rate of 12V/μsec, a 5MHz gain bandwidth product, and settling time to within ±0.01% of final value of 1.5μsec. In addition, low input voltage noise and current noise plus a low 1/f noise corner frequency allow this amplifier to be used in a variety of low noise, wide bandwidth applications.

FEATURES

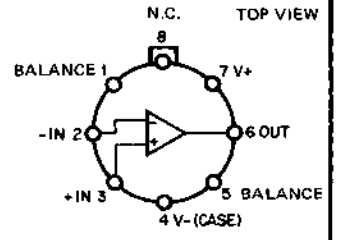
- LF156 Series Direct Replacements
- Low Input Bias and Offset Currents
- High Slew Rate 12V/μsec
- Fast Settling to ±0.01% 1.5μsec
- Internal Compensation
- Low Input Offset Voltage 1.0mV
- Low Input Offset Voltage Drift . . . . . 3.0μV/°C
- Low Input Noise Current . . . . . 0.01pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- High Open Loop Gain 106dB
- Models With MIL-STD-883A Class B Processing Available From Stock

Applications include high speed D/A converter summing amplifiers, integrators, log amps, photocell amplifiers, and active filters. For higher speed (decompensated) models, see the PM157 data sheet.

SIMPLIFIED SCHEMATIC DIAGRAM



PIN CONNECTIONS



TO-99 (J-Suffix)

ORDERING INFORMATION

ORDER: PM156AJ
PM156J
PM256J
PM356AJ
PM356J

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: PM156-883-AJ
PM156-883-J

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- PM156A, PM156, PM256, PM356A ±22V
- PM356 ±18V

Internal Power Dissipation
- PM156A, PM156 670mW
- PM256 570mW
- PM356A, PM356 500mW

(The TO-99(J) package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.)

Operating Temperature Range
- PM156A, PM156 –55°C to +125°C
- PM256 –25°C to +85°C
- PM356A, PM356 0°C to +70°C

Maximum Junction Temperature (T_j)
- PM156A, PM156 +150°C
- PM256 +115°C
- PM356A, PM356 +100°C

Differential Input Voltage
- PM156A, PM156, PM256, PM356A ±40V
- PM356 ±30V

Input Voltage
- PM156A, PM156, PM256, PM356A ±20V
- PM356 ±16V

(Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration Indefinite

Storage Temperature Range –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for ±15V ≤ V_S ≤ ±20V, T_A = +25°C unless otherwise noted.

Parameter	Symbol	Test Conditions	PM156A Min	PM156A Typ	PM156A Max	PM356A Min	PM356A Typ	PM356A Max	Units
Input Offset Voltage	V_{os}	R_S = 50Ω	–	1.0	2.0	–	1.0	2.0	mV
Input Offset Current	I_{os}	T_j = 25°C (Note 1)	–	3.0	10	–	3.0	10	pA
Input Bias Current	I_B	T_j = 25°C (Note 1)	–	30	50	–	30	50	pA
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{vo}	V_S = ±15V, V_O = ±10V, R_L = 2KΩ	50	200	–	50	200	–	V/mV
Supply Current	I_S	V_S = ±15V	–	5.0	7.0	–	5.0	7.0	mA
Slew Rate	SR	A_{VCL} = +1, V_S = ±15V	10	12	–	10	12	–	V/μsec
Gain Bandwidth Product	GBW	V_S = ±15V	4.0	4.5	–	4.0	4.5	–	MHz
Settling Time to 0.01%	t_s	V_S = ±15V (Note 2)	–	1.5	–	–	1.5	–	μsec
Input Noise Voltage	e_n	R_S=100Ω, f =100Hz, V_S = ±15V	–	15	–	–	15	–	nV $\sqrt{Hz}$
		R_S=100Ω, f=1000Hz, V_S=±15V	–	12	–	–	12	–	nV $\sqrt{Hz}$
Input Noise Current	i_n	f = 100Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
		f = 1000Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
Input Capacitance	C_{in}		–	3.0	–	–	3.0	–	pF

These specifications apply for ±15V ≤ V_S ≤ ±20V, -55°C ≤ T_A ≤ +125°C and T_{HIGH} = +125°C for PM156A, 0°C ≤ T_A ≤ +70°C and T_{HIGH} = +70°C for PM356A, unless otherwise noted.

Input Offset Voltage	V_{os}	R_S = 50Ω	–	–	2.5	–	–	2.3	mV
Input Offset Voltage Drift	TCV_{os}	R_S = 50Ω	–	3.0	5.0	–	3.0	5.0	μV/°C
Change in Input Offset Drift with V_{os} Adjust	$\frac{\Delta TCV_{os}}{\Delta V_{os}}$	R_S = 50Ω	–	0.5	–	–	0.5	–	μV/°C per mV
Input Offset Current	I_{os}	T_j ≤ T_{HIGH} (Note 1)	–	–	10	–	–	1.0	nA
Input Bias Current	I_B	T_j ≤ T_{HIGH} (Note 1)	–	–	25	–	–	5.0	nA
Large Signal Voltage Gain	A_{vo}	V_S=±15V, V_O=±10V, R_L=2KΩ	25	–	–	25	–	–	V/mV
Output Voltage Swing	V_{om}	V_S = ±15V, R_L = 10KΩ	±12	±13	–	±12	±13	–	V
		V_S = ±15V, R_L = 2KΩ	±10	±12	–	±10	±12	–	V
Input Voltage Range	CMVR	V_S = ±15V	±11	+15.1 −12.0	–	±11	+15.1 −12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	100	–	85	100	–	dB
Power Supply Rejection Ratio	PSRR	(Note 3)	85	100	–	85	100	–	dB

NOTE 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit on page 4.

NOTE 3: Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS

PM156 / PM256 / PM356

These specifications apply for T_A = +25°C, ±15V ≤ V_S ≤ ±20V for PM156 and PM256, V_S = ±15V for PM356, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	3.0	5.0	–	3.0	10	mV
Input Offset Current	I_{OS}	T_j = 25°C (Note 1)	–	3.0	20	–	3.0	50	pA
Input Bias Current	I_B	T_j = 25°C (Note 1)	–	30	100	–	30	200	pA
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V, R_L = 2KΩ	50	200	–	25	200	–	V/mV
Supply Current	I_S		–	5.0	7.0	–	5.0	10	mA
Slew Rate	SR	A_{VCL} = +1, V_S = ±15V	7.5	12	–	–	12	–	V/μsec
Gain Bandwidth Product	GBW	V_S = ±15V	–	5.0	–	–	5.0	–	MHz
Settling Time to 0.01%	t_s	V_S = ±15V (Note 2)	–	1.5	–	–	1.5	–	μsec
Input Noise Voltage	e_n	R_S=100Ω, f = 100Hz, V_S = ±15V	–	15	–	–	15	–	nV $\sqrt{Hz}$
		R_S=100Ω, f = 1000Hz, V_S = ±15V	–	12	–	–	12	–	nV $\sqrt{Hz}$
Input Noise Current	i_n	f = 100Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
		f = 1000Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
Input Capacitance	C_{in}		–	3.0	–	–	3.0	–	pF

These specifications apply for ±15V ≤ V_S ≤ ±20V for PM156 and PM256, V_S = ±15V for PM356, -55°C ≤ T_A ≤ +125°C for PM156, -25°C ≤ T_A ≤ +85°C for PM256, 0°C ≤ T_A ≤ +70°C for PM356, unless otherwise noted.

Input Offset Voltage	V_{OS}	R_S = 50Ω, PM156	–	–	7.0	–	–	–	mV
		R_S = 50Ω, PM256	–	–	6.5	–	–	–	mV
		R_S = 50Ω, PM356	–	–	–	–	–	13	mV
Input Offset Voltage Drift	TCV_{OS}	R_S = 50Ω	–	5.0	–	–	5.0	–	μV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\frac{\Delta TCV_{OS}}{\Delta V_{OS}}$	R_S = 50Ω	–	0.5	–	–	0.5	–	μV/°C per mV
Input Offset Current (Note 1)	I_{OS}	PM156, T_j ≤ +125°C	–	–	20	–	–	–	nA
		PM256, T_j ≤ +85°C	–	–	1.0	–	–	–	nA
		PM356, T_j ≤ +70°C	–	–	–	–	–	2.0	nA
Input Bias Current (Note 1)	I_B	PM156, T_j ≤ +125°C	–	–	50	–	–	–	nA
		PM256, T_j ≤ +85°C	–	–	5.0	–	–	–	nA
		PM356, T_j ≤ +70°C	–	–	–	–	–	8.0	nA
Large Signal Voltage Gain	A_{VO}	V_S=±15V, V_O=±10V, R_L=2KΩ	25	–	–	15	–	–	V/mV
Output Voltage Swing	V_{OM}	V_S = ±15V, R_L = 10KΩ	±12	±13	–	±12	±13	–	V
		V_S = ±15V, R_L = 2KΩ	±10	±12	–	±10	±12	–	V
Input Voltage Range	CMVR	V_S = ±15V	±11	+15.1 -12.0	–	±10	+15.1 -12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	(Note 3)	85	100	–	80	100	–	dB

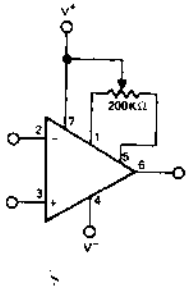
NOTE 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit on page 4.

NOTE 3: Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

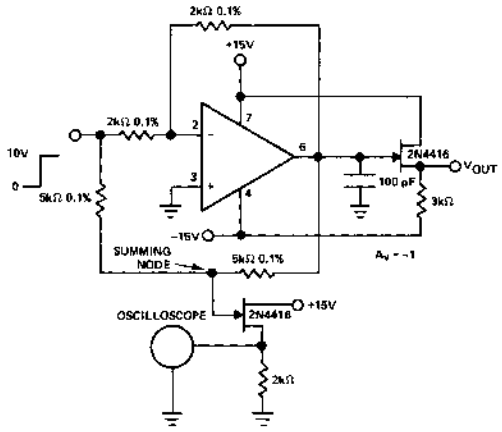
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: For potentiometers with a temperature coefficient ≤100ppm/°C, the added TCV_{OS} with nulling is ≈0.5μV/°C/mV of adjustment.

SETTLING TIME TEST CIRCUIT



APPLICATION INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM156 JFET input stage can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V− can result in a destroyed unit.

If both inputs exceed the negative common mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PM157A

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIER

PM157A/PM357A/PM157/PM257/PM357
WIDE BANDWIDTH DECOMPENSATED ($A_{V_{MIN}}$ = 5)

GENERAL DESCRIPTION

The PM157 Series provides low input current, high slew rate, and direct interchangeability with LF157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. A JFET-input design enables operation with ±40V input voltages eliminating the blowout problems associated with MOSFET devices.

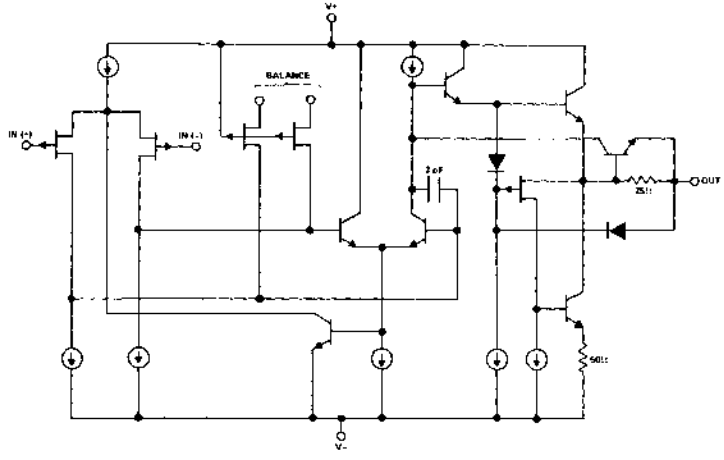
High accuracy, excellent dynamic performance, and low cost make the PM157 Series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common mode rejection ratio or input offset voltage drift. Dynamic specifications include a slew rate of 50V/μsec, a 20MHz gain bandwidth product, and 1.5μsec settling time. (Decompensation results in a closed loop gain minimum of 5.) Low input voltage and current noise and a low 1/f noise corner frequency allow the PM157 to be used in many low noise, high frequency applications.

FEATURES

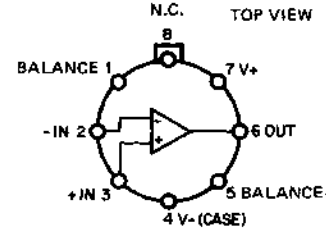
- LF157 Series Direct Replacements
- Wide Bandwidth 20MHz
- High Slew Rate 50V/μsec
- Fast Settling to ±0.01% 1.5μsec
- Internal Compensation . . . . . .
- Low Input Bias and Offset Currents
- Low Input Offset Voltage 1.0mV
- Low Input Offset Voltage Drift . . . . . 3.0μV/°C
- Low Input Noise Current . . . . . 0.01pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- Models With MIL-STD-883A Class B Processing Available From Stock

Applications include high frequency active filters, high speed peak detectors, and large power bandwidth gain stages. For unity-gain compensated models, refer to the PM156 data sheet.

SIMPLIFIED SCHEMATIC DIAGRAM



PIN CONNECTIONS



TO-99 (J-Suffix)

ORDERING INFORMATION

ORDER: PM157AJ
PM157J
PM257J
PM357AJ
PM357J

Military Temperature Range Devices With MIL-STD-883A Class B Processing

ORDER: PM157-883-AJ
PM157-883-J

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- PM157A, PM157, PM257, PM357A ±22V
- PM357 ±18V

Internal Power Dissipation
- PM157A, PM157 670mW
- PM257 570mW
- PM357A, PM357 500mW

(The TO-99(J) package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/S junction to case.)

Operating Temperature Range
- PM157A, PM157 −55°C to +125°C
- PM257 −25°C to +85°C
- PM357A, PM357 0°C to +70°C

Maximum Junction Temperature (T_j)
- PM157A, PM157 +150°C
- PM257 +115°C
- PM357A, PM357 +100°C

Differential Input Voltage
- PM157A, PM157, PM257, PM357A ±40V
- PM357 ±30V

Input Voltage
- PM157A, PM157, PM257, PM357A ±20V
- PM357 ±16V

(Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration Indefinite

Storage Temperature Range −65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for ±15V ≤ V_S ≤ ±20V, T_A = +25°C unless otherwise noted.

Parameter	Symbol	Test Conditions	PM157A Min	PM157A Typ	PM157A Max	PM357A Min	PM357A Typ	PM357A Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	1.0	2.0	–	1.0	2.0	mV
Input Offset Current	I_{OS}	T_j = 25°C (Note 1)	–	3.0	10	–	3.0	10	pA
Input Bias Current	I_B	T_j = 25°C (Note 1)	–	30	50	–	30	50	pA
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V, R_L = 2KΩ	50	200	–	50	200	–	V/mV
Supply Current	I_S	V_S = ±15V	–	5.0	7.0	–	5.0	7.0	mA
Slew Rate	SR	A_{VCL} = 5, V_S = ±15V	40	50	–	40	50	–	V/μsec
Gain Bandwidth Product	GBW	V_S = ±15V	15	20	–	15	20	–	MHz
Settling Time to 0.01%	t_s	V_S = ±15V (Note 2)	–	1.5	–	–	1.5	–	μsec
Input Noise Voltage	e_n	R_S=100Ω, f=100Hz, V_S = ±15V	–	15	–	–	15	–	nV $\sqrt{Hz}$
		R_S=100Ω, f=1000Hz, V_S = ±15V	–	12	–	–	12	–	nV $\sqrt{Hz}$
Input Noise Current	i_n	f = 100Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
		f = 1000Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
Input Capacitance	C_{in}		–	3.0	–	–	3.0	–	pF
These specifications apply for ±15V ≤ V_S ≤ ±20V, −55°C ≤ T_A ≤ +125°C and T_{HIGH} = +125°C for PM157A, 0°C ≤ T_A ≤ +70°C and T_{HIGH} = +70°C for PM357A, unless otherwise noted.									
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	–	2.5	–	–	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	R_S = 50Ω	–	3.0	5.0	–	3.0	5.0	μV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\frac{\Delta TCV_{OS}}{\Delta V_{OS}}$	R_S = 50Ω	–	0.5	–	–	0.5	–	μV/°C per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	–	–	10	–	–	1.0	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (note 1)	–	–	25	–	–	5.0	nA
Large Signal Voltage Gain	A_{VO}	V_S=±15V, V_O=±10V, R_L=2KΩ	25	–	–	25	–	–	V/mV
Output Voltage Swing	V_{OM}	V_S = ±15V, R_L = 10KΩ	±12	±13	–	±12	±13	–	V
		V_S = ±15V, R_L = 2KΩ	±10	±12	–	±10	±12	–	V
Input Voltage Range	CMVR	V_S = ±15V	±11	+15.1 −12.0	–	±11	+15.1 −12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	100	–	85	100	–	dB
Power Supply Rejection Ratio	PSRR	(Note 3)	85	100	–	85	100	–	dB

NOTE 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a A_V = −5 connection with R_F = 2KΩ. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit on page 4.

NOTE 3: Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS

			PM157 PM257			PM357			
These specifications apply for T_A = +25°C, ±15V ≤ V_S ≤ ±20V for PM157 and PM257, V_S = ±15V for PM357, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	3.0	5.0	–	3.0	10	mV
Input Offset Current	I_{OS}	T_j = 25°C (Note 1)	–	3.0	20	–	3.0	50	pA
Input Bias Current	I_B	T_j = 25°C (Note 1)	–	30	100	–	30	200	pA
Input Resistance	R_{IN}		–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V R_L = 2KΩ	50	200	–	25	200	–	V/mV
Supply Current	I_S		–	5.0	7.0	–	5.0	10	mA
Slew Rate	SR	A_{VCL} = 5, V_S = ±15V	30	50	–	–	50	–	V/μsec
Gain Bandwidth Product	GBW	V_S = ±15V	–	20	–	–	20	–	MHz
Settling Time to 0.01%	t_S	V_S = ±15V (Note 2)	–	1.5	–	–	1.5	–	μsec
Input Noise Voltage	e_n	R_S=100Ω, f = 100Hz, V_S = ±15V	–	15	–	–	15	–	nV $\sqrt{Hz}$
		R_S=100Ω, f = 1000Hz, V_S = ±15V	–	12	–	–	12	–	nV $\sqrt{Hz}$
Input Noise Current	i_n	f = 100Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
		f = 1000Hz, V_S = ±15V	–	0.01	–	–	0.01	–	pA $\sqrt{Hz}$
Input Capacitance	C_{in}		–	3.0	–	–	3.0	–	pF
These specifications apply for ±15V ≤ V_S ≤ ±20V for PM157 and PM257, V_S = ±15V for PM357, −55°C ≤ T_A ≤ +125°C for PM157, −25°C ≤ T_A ≤ +85°C for PM257, 0°C ≤ T_A ≤ +70°C for PM357, unless otherwise noted.									
Input Offset Voltage	V_{OS}	R_S = 50Ω, PM157	–	–	7.0	–	–	–	mV
		R_S = 50Ω, PM257	–	–	6.5	–	–	–	mV
		R_S = 50Ω, PM357	–	–	–	–	–	13	mV
Input Offset Voltage Drift	TCV_{OS}	R_S = 50Ω	–	5.0	–	–	5.0	–	μV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\frac{\Delta TCV_{OS}}{\Delta V_{OS}}$	R_S = 50Ω	–	0.5	–	–	0.5	–	μV/°C per mV
Input Offset Current (Note 1)	I_{OS}	PM157, T_j ≤ +125°C	–	–	20	–	–	–	nA
		PM257, T_j ≤ +85°C	–	–	1.0	–	–	–	nA
		PM357, T_j ≤ +70°C	–	–	–	–	–	2.0	nA
Input Bias Current (Note 1)	I_B	PM157, T_j ≤ +125°C	–	–	50	–	–	–	nA
		PM257, T_j ≤ +85°C	–	–	5.0	–	–	–	nA
		PM357, T_j ≤ +70°C	–	–	–	–	–	8.0	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V, R_L = 2KΩ	25	–	–	15	–	–	V/mV
Output Voltage Swing	V_{OM}	V_S = ±15V, R_L = 10KΩ	±12	±13	–	±12	±13	–	V
		V_S = ±15V, R_L = 2KΩ	±10	±12	–	±10	±12	–	V
Input Voltage Range	CMVR	V_S = ±15V	±11	+15.1 −12.0	–	±10	+15.1 −12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	(Note 3)	85	100	–	80	100	–	dB

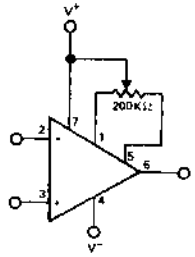
NOTE 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a A_V = −5 connection with R_F = 2KΩ. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit on page 4.

NOTE 3: Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

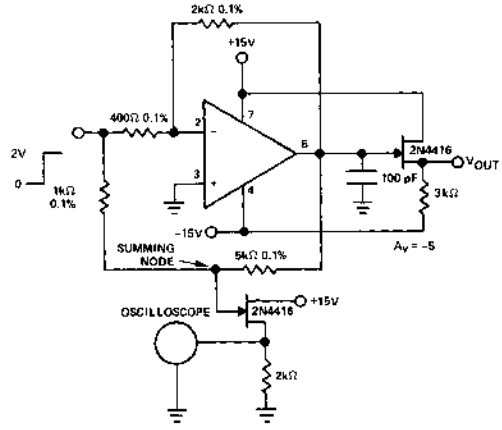
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: For potentiometers with a temperature coefficient ≤100ppm/°C, the added TCV_{OS} with nulling is ≈0.5μV/°C/mV of adjustment.

SETTLING TIME TEST CIRCUIT



APPLICATION INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM157 JFET input stage can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V− can result in a destroyed unit.

If both inputs exceed the negative common mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PM-725

INSTRUMENTATION OPERATIONAL AMPLIFIER

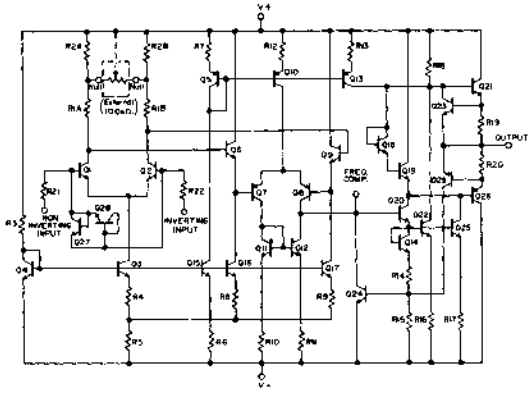
GENERAL DESCRIPTION

The PM725 Series of monolithic Instrumentation Operational Amplifiers provides industry-standard 725 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. For improved specifications, see the SSS725 Series data sheet. For devices with internal frequency compensation request the OP-05 Instrumentation and OP-07 Ultra-low Offset Voltage Operational Amplifier data sheets.

FEATURES

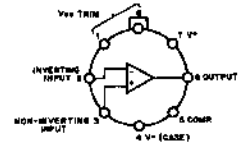
- Extremely High Voltage Gain . . . . . 3M Typ
- Low Offset Voltage and Offset Current
- Low Drift with Temperature
- Low Input Voltage And Current Noise
- High Common Mode Rejection . . . . . 110db min
- High Power Supply Rejection . . . . . 10μv/v max
- Silicon-Nitride Passivation
- Differential Input Overvoltage Protection

SIMPLIFIED SCHEMATIC

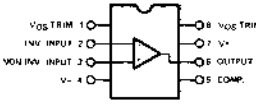


PIN CONNECTIONS AND ORDERING INFORMATION

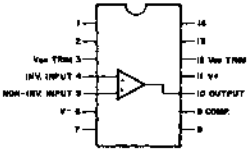
TOP VIEW



TO-99 (J-Suffix)
ORDER: PM-725J
PM-725CJ



EPOXY B MINI-DIP
(P-Suffix)
ORDER: PM725CP



14 PIN DIP (Y Suffix)
ORDER: PM-725Y
PM-725CY

Military Temperature Range Devices
With MIL-STD-883A
Class B Processing:
ORDER: PM725-883-J
PM725-883-Y

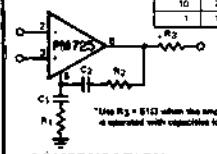
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (See note)	500mW
Differential Input Voltage	±5V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
PM725	−55°C to +125°C
PM725C	0°C to +70°C

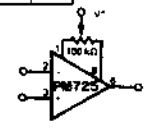
NOTE: For the TO-99(J) package derate at 7.1mW/°C above 80°C; for the DIP(Y) package derate at 10.0mW/°C above 100°C.

COMPENSATION COMPONENT VALUES

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	–	–
1,000	470	001	·	·
100	47	01	·	–
10	27	05	270	0015
1	10	05	39	02



COMPENSATION CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT

ELECTRICAL CHARACTERISTICS			PM725			PM725C			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage (Without external trim)	V_{os}	$R_S \leq 10\ k\Omega$		0.5	1.0		0.5	2.5	mV
Input Offset Current	I_{os}			2.0	20		2.0	35	nA
Input Bias Current	I_B			42	100		42	125	nA
Input Noise Voltage	e_n	f_O = 10 Hz		15			15		nV/√Hz
		f_O = 100 Hz		9.0			9.0		nV/√Hz
		f_O = 1 kHz		8.0			8.0		nV/√Hz
Input Noise Current	i_n	f_O = 10 Hz		1.0			1.0		pA/√Hz
		f_O = 100 Hz		0.3			0.3		pA/√H.
		f_O = 1 kHz		0.15			0.15		pA/√Hz
Input Resistance	R_{in}			1.5			1.5		MΩ
Input Voltage Range	CMVR		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2\ k\Omega$, V_O = ±10 V	1,000,000	3,000,000		250,000	3,000,000		V/V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	110	120		94	120		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10\ k\Omega$		2.0	10		2.0	35	µV/V
Output Voltage Swing	V_{om}	$R_L \geq 10\ k\Omega$	±12	±13.5		±12	±13.5		V
		$R_L \geq 2\ k\Omega$	±10	±13.5		±10	±13.5		V
Output Resistance	R_O			150			150		Ω
Power Consumption	Pd			80	105		80	150	mW
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C for PM725, 0°C ≤ T_A ≤ +70°C for PM725C, unless otherwise noted.									
Input Offset Voltage (Without external trim)	V_{os}	$R_S \leq 10\ k\Omega$			1.5			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{os}	R_S = 50Ω		2.0	5.0		2.0		µV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{osn}	R_S = 50Ω		0.6			0.6		µV/°C
Input Offset Current	I_{os}	T_A = MAX		1.2	20		1.2	35	nA
		T_A = MIN		7.5	40		4.0	50	nA
Average Input Offset Current Drift	TCI_{os}			35	150		10		pA/°C
Input Bias Current	I_B	T_A = MAX		20	100			125	nA
		T_A = MIN		80	200			250	nA
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2\ k\Omega$, T_A = MAX	1,000,000			125,000			V/V
		$R_L \geq 2\ k\Omega$, T_A = MIN	250,000			125,000			V/V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	100				115		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10\ k\Omega$			20		20		µV/V
Output Voltage Swing	V_{om}	$R_L \geq 2\ k\Omega$	±10			±10			V

PM-741

COMPENSATED OPERATIONAL AMPLIFIER

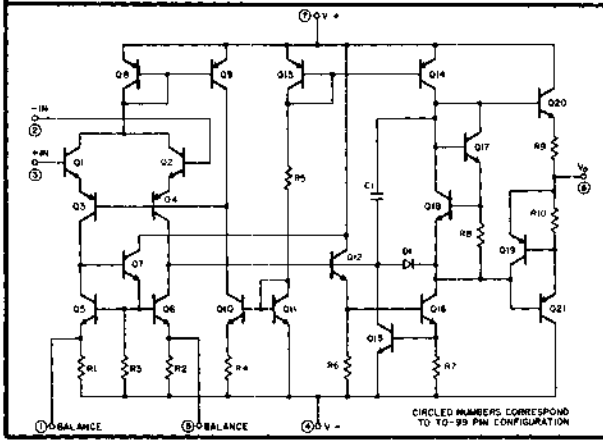
GENERAL DESCRIPTION

The PM741 Series of Internally Compensated Operational Amplifiers provides industry-standard 741 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. For improved specifications, see the SSS741 Series data sheet. For very high performance general purpose op amps, refer to the OP-02 Series data sheet.

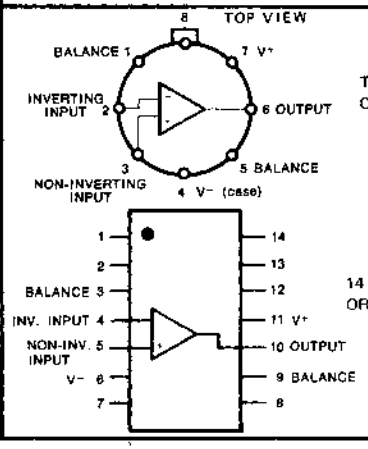
FEATURES

- Industry Standard 741 Specifications
- Internal Frequency Compensation
- Continuous Short Circuit Protection
- MIL-STD-883 Processing Available
- Silicon-Nitride Passivation
- Low Noise

SCHEMATIC DIAGRAM



PIN CONNECTIONS AND ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM741	±22V
PM741C	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
PM741	−55°C to +125°C
PM741C	0°C to +85°C

Note 1. Maximum package power dissipation vs ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
DUAL-IN-LINE (Y)	100°C	10.0mW/°C

ELECTRICAL CHARACTERISTICS

These specifications apply for T_A = 25°C, V_S = ±15V, unless otherwise specified.			PM741		PM741C		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	5.0	–	6.0	mV
Input Offset Current	I_{OS}		–	200	–	200	nA
Input Bias Current	I_B		–	500	–	500	nA
Input Resistance	R_{IN}		0.3	–	0.3	–	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	50,000	–	25,000	–	V/V
Supply Current	I_S		–	2.8	–	2.8	mA
The following specifications apply for −55°C ≤ T_A ≤ +125°C – PM741 and 0°C ≤ T_A ≤ +85°C – PM741C.			V_S = ±15V		V_S = ±15V		
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	6.0	–	7.5	mV
Input Offset Current	I_{OS}		–	500	–	300	nA
Input Bias Current	I_B		–	1.5	–	0.8	µA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	25,000	–	15,000	–	V/V
Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	– –	±12 ±10	– –	V V
Input Voltage Range	CMVR		±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	70	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	77	–	77	–	dB

PM-747

DUAL COMPENSATED OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

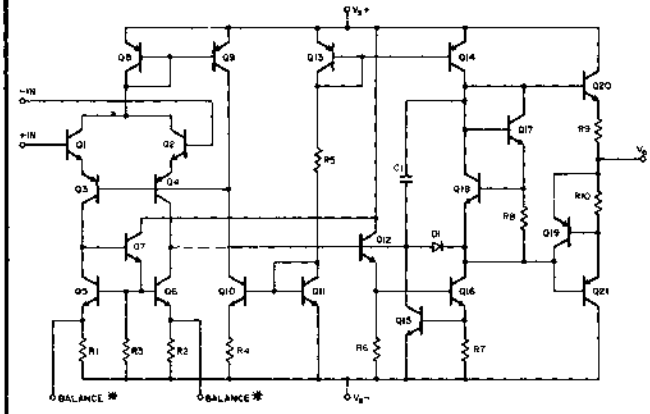
The PM747 Series of Internally Compensated Dual Operational Amplifiers provides industry-standard 747 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. For improved specifications, see the SSS747 Series data sheet. For very high performance dual op amps, refer to the OP-10 Dual Matched Instrumentation Operational Amplifier data sheet.

FEATURES

- Dual PM 741 Internally Compensated Operational Amplifier
- Internal Frequency Compensation
- Continuous Short Circuit Protection
- MIL-STD-883 Processing Available
- Silicon-Nitride Passivation
- Low Noise

SCHEMATIC DIAGRAM

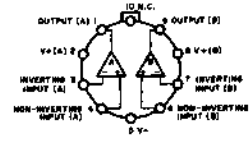
(1/2 OF CIRCUIT SHOWN)



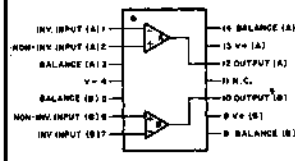
* DIP PACKAGE ONLY

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-100 (K-Suffix)
ORDER: PM747K
PM747CK



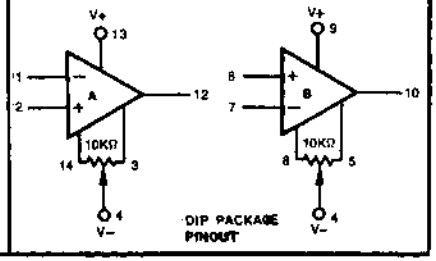
14 PIN DIP (Y-Suffix)
ORDER: PM747Y
PM747CY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM747	±22V
PM747C	±18V
Internal Power Dissipation (See note)	
Metal Can (K) package	500mW
DIP (Y) Package	670mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65° to 150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
PM747	−55°C to +125°C
PM747C	0°C to +70°C

NOTE: For the TO-100(K) package derate at 7.1mW/°C above 80°C; for the DIP(Y) package derate at 10.0mW/°C above 100°C.

BALANCING CIRCUIT



DIP PACKAGE PINOUT

ELECTRICAL CHARACTERISTICS Each Amplifier			PM747			PM747C			
These specifications apply for T_A = 25°C, V_S = ±15V, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10\ k\Omega$	–	1.0	5.0	–	1.0	6.0	mV
Input Offset Current	I_{OS}		–	20	200	–	20	200	nA
Input Bias Current	I_B		–	80	500	–	80	500	nA
Input Resistance	R_{IN}		0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_{IN}		–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range			–	±15	–	–	±15	–	mV
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\ k\Omega$, V_O = ±10 V	50	200	–	25	200	–	V/mV
Output Resistance	R_O		–	75	–	–	75	–	Ω
Output Short Circuit Current	I_{SC}		–	25	–	–	25	–	mA
Supply Current	I_{SY}		–	1.7	2.8	–	1.7	2.8	mA
Power Consumption	P_D	V_S = ±15 V	–	50	85	–	50	85	mW
Transient Response (Unity Gain) Risetime		V_{IN} = 20mV, R_L = 2 kΩ	–	0.3	–	–	0.3	–	μsec
Transient Response (Unity Gain) Overshoot		$C_L \leq 100$ pF	–	5.0	–	–	5.0	–	%
Slew Rate		$R_L \leq 2\ k\Omega$	–	0.7	–	–	0.7	–	V/μsec
Channel Separation	CS		–	120	–	–	120	–	dB
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C for PM747, 0°C ≤ T_A ≤ +70°C for PM747C, unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 10\ k\Omega$	–	1.0	6.0	–	1.0	7.5	mV
Input Offset Current	I_{OS}	T_A = MAX	–	7.0	200	–	7.0	200	nA
		T_A = MIN	–	85	500	–	30	300	nA
Input Bias Current	I_B	T_A = MAX	–	0.03	0.5	–	0.03	0.5	μA
		T_A = MIN	–	0.3	1.5	–	0.10	0.8	μA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	70	90	–	70	90	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10\ k\Omega$	–	30	150	–	30	150	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\ k\Omega$, V_O = ±10 V	25	–	–	15	–	–	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 10\ k\Omega$	±12	±14	–	±12	±14	–	V
		$R_L \geq 2\ k\Omega$	±10	±13	–	±10	±13	–	V
Supply Current	I_{SY}	T_A = MAX	–	1.5	2.5	–	1.5	2.5	mA
		T_A = MIN	–	2.0	3.3	–	2.0	3.3	mA
Power Consumption	P_D	T_A = MAX	–	45	75	–	45	75	mW
		T_A = MIN	–	60	100	–	60	100	mW

PM-1458/1558

DUAL COMPENSATED OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

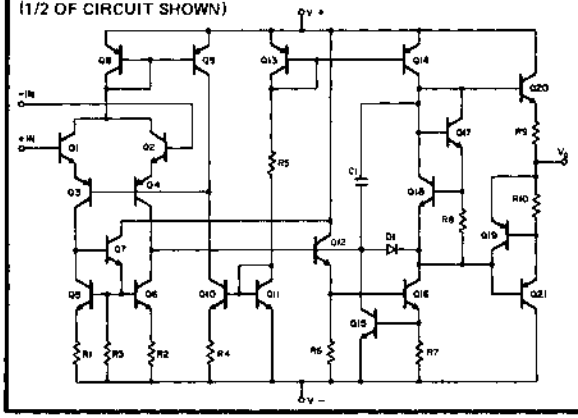
The PM1558 Series of Internally Compensated Dual Operational Amplifiers provides industry-standard 1558 specifications and pin-for-pin compatibility. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost. For improved specifications, refer to the SSS747/1558 Dual Internally Compensated Operational Amplifier data sheet. For precision dual op amps, refer to the OP-10 Dual Matched Instrumentation Operational Amplifier data sheet.

FEATURES

- Dual PM 741 Internally Compensated Operational Amplifier
- Internal Frequency Compensation
- Low Power Consumption
- Continuous Short Circuit Protection
- MIL-STD-883 Processing Available
- Silicon-Nitride Passivation

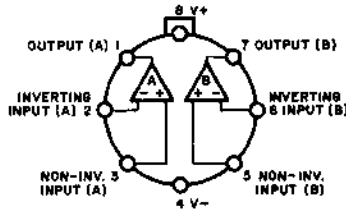
SCHEMATIC DIAGRAM

(1/2 OF CIRCUIT SHOWN)



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99

ORDER: PM1558
PM1458

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
PM1558	±22V
PM1458	±18V
Internal Power Dissipation	
(See note)	500 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65° to 150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

PM1558	−55°C to +125°C
PM1458	0°C to +70°C

For the TO-99(J) package derate at 7.1 mW/°C above 80°C.

TO-99(J)

ELECTRICAL CHARACTERISTICS
Each Amplifier

These specifications apply for $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise noted.

Parameter	Symbol	Test Conditions	PM1558 Min	PM1558 Typ	PM1558 Max	PM1458 Min	PM1458 Typ	PM1458 Max	Units
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{OS}		–	0.03	0.2	–	0.03	0.2	μA
Input Bias Current	I_B		–	0.2	0.5	–	0.2	0.5	μA
Input Resistance	R_{IN}		0.3	2.0	–	0.3	2.0	–	MΩ
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, $V_O = \pm 10V$	50	200	–	20	100	–	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±14	–	±12	±14	–	V
Input Voltage Range	CMVR	$V_S = \pm 15V$	±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	70	90	–	70	90	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	–	30	150	–	30	150	μV/V
Power Consumption both Amplifiers	P_D	$V_O = 0$	–	70	150	–	70	170	mW
Channel Separation	CS		–	120	–	–	120	–	dB
The following specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for PM1558, $0°C \leq T_A \leq +70°C$ for PM1458, unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	–	6.0	–	–	7.5	mV
Input Offset Current	I_{OS}		–	–	0.5	–	–	0.3	μA
Input Bias Current	I_B		–	–	1.5	–	–	0.8	μA
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	–	–	15	–	–	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±10	±13	–	±10	±13	–	V

PM4136

QUAD 741-TYPE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The PM4136 Series provides four 741-type operational amplifiers in a single 14-pin DIP package, pin-compatible with the RM4136 and RC4136. Each of the four amplifiers has the proven SSS741 Series advantages of low noise, low drift and excellent long term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost.

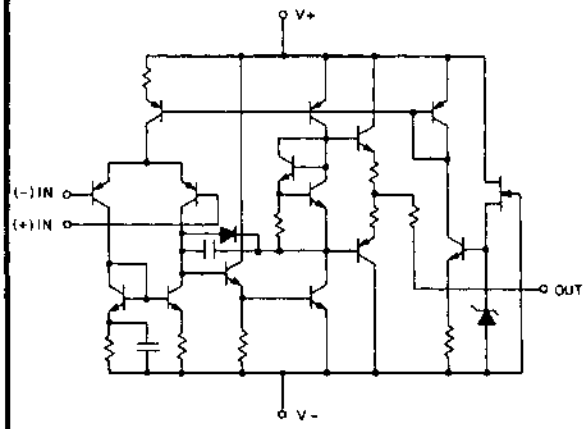
The PM4136 Series is ideal for use in designs requiring minimum space and cost while maintaining SSS741-type performance. PM4136's with processing per the requirements of MIL 38510/883 are available. For dual-741-type versions, see the SSS747/1558 data sheet.

FEATURES

- RM4136/RC4136 Direct Replacements
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short Circuit Protection
- Low Input Bias Current
- Low Input Offset Voltage

EQUIVALENT SCHEMATIC

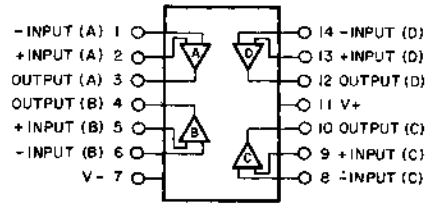
(1/4 CIRCUIT SHOWN)



ORDER: PM4136Y (-55°C to +125°C)
PM4136CY (0°C to +70°C)

Military Temperature Range Devices
With MIL-STD-883A Class B Processing
ORDER: PM4136-883-Y

PACKAGE INFORMATION



TOP VIEW

Supply Voltage	
PM4136	±22V
PM4136C	±18V
Internal Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
PM4136	−55°C to +125°C
PM4136C	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

1. Rating applies for ambient temperature of +25°C; derate linearly at 6.4 mW/°C for ambient temperatures above +25°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground, one amplifier only. I_{SC} = 45mA (typical).

These specifications apply for T_A = +25°C and V_S = ±15V unless otherwise specified.		PM4136			PM4136C			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	$R_S \leq 10k\Omega$	—	0.5	5.0	—	0.5	6.0	mV
Input Offset Current		—	5.0	200	—	5.0	200	nA
Input Bias Current		—	40	500	—	40	500	nA
Input Resistance		0.3	5.0	—	0.3	5.0	—	MΩ
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000	—	20,000	300,000	—	V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14	—	±12	±14	—	V
	$R_L \geq 2k\Omega$	±10	±13	—	±10	±13	—	V
Input Voltage Range		±12	±14	—	±12	±14	—	V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100	—	70	100	—	dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	—	10	150	—	10	150	μV/V
Power Consumption	No load	—	210	340	—	210	340	mW
Transient Response (unity gain) Risetime	V_{IN} = 20 mV R_L = 2kΩ $C_L \leq$ 100 pF	—	0.13	—	—	0.13	—	μs
Transient Response (unity gain) Overshoot	V_{IN} = 20 mV R_L = 2kΩ $C_L \leq$ 100 pF	—	5.0	—	—	5.0	—	%
Unity Gain Bandwidth		—	3.0	—	—	3.0	—	MHz
Slew Rate (unity gain)	$R_L \geq 2k\Omega$	—	1.5	—	—	1.0	—	V/μs
Channel Separation	f = 10 kHz R_S = 1kΩ open loop	—	105	—	—	105	—	dB
(Gain - 100)	f = 10kHz R_S = 1kΩ Gain = 100	—	105	—	—	105	—	dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for PM4136, 0°C ≤ T_A ≤ +70°C for PM4136C, and V_S = ± 15V unless otherwise specified.								
Input Offset Voltage	$R_S \leq 10k\Omega$	—	—	6.0	—	—	7.5	mV
Input Offset Current		—	—	500	—	—	300	nA
Input Bias Current		—	—	1500	—	—	800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing	$R_L \geq 2k\Omega$	±10	—	—	±10	—	—	V
	T_A = High	—	180	300	—	180	300	mW
	T_A = Low	—	240	400	—	240	400	mW

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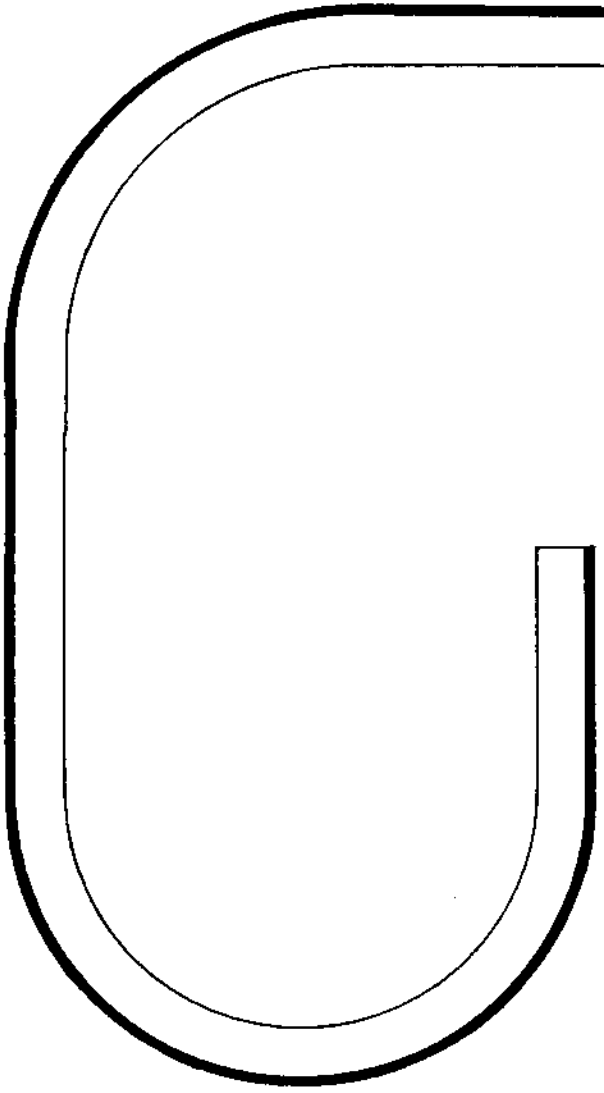

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COMPARATORS

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CMP-02	Low Input Current Precision Comparator	7-7

CMP-01

FAST PRECISION COMPARATOR

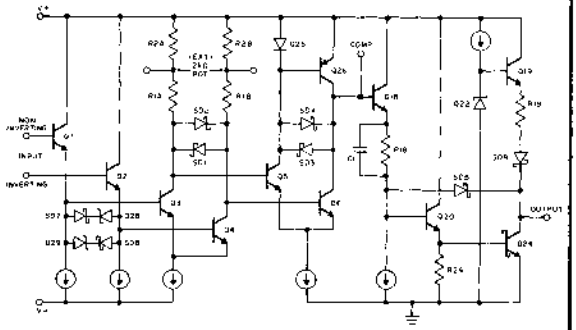
GENERAL DESCRIPTION

The CMP-01 is a monolithic Fast Precision Voltage Comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages, including single 5 volt supply operation. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13 bit A/D converters. The CMP-01 is pin compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

FEATURES

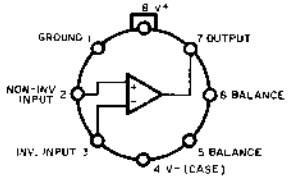
- Fast Response Time . . . . . 110 ns typ., 180 ns Max
- High Input Slew Rate . . . . . .92 V/μS
- Low Offset Voltage . . . . .0.3 mV typ., 0.8 mV Max
- Low Offset Current . . . . . 4 nA typ., 25 nA Max
- Low Offset Drift . . . . . 1.0 μV/°C, 30 pA/°C
- Standard Power Supplies . . . . . ±5V to ±18V
- Guaranteed Operation from Single +5V Supply
- No Pull-up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling. . . . . Single 2kΩ Potentiometer
- Easy to Use. . . . . Free from Oscillations

SIMPLIFIED SCHEMATIC

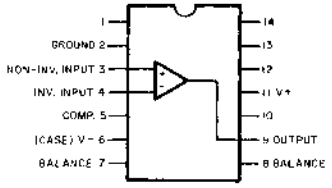


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)
ORDER: CMP-01J
CMP-01EJ
CMP-01CJ



14 PIN HERMETIC DIP (Y-Suffix)
ORDER: CMP-01Y
CMP-01EY
CMP-01CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing
CMP01-883-J
CMP01-883-Y

ABSOLUTE MAXIMUM RATINGS

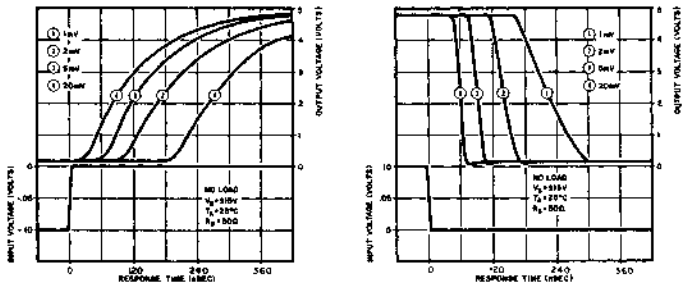
Total Supply Voltage, V+ to V-	36V	Output Sink Current (Continuous Operation)	75 mA
Output to Ground	-5V to +32V	Operating Temperature Range –	
Output to Negative Supply Voltage	50V	CMP-01	-55°C to +125°C
Ground to Negative Supply Voltage	30V	CMP-01E, -01C	0°C to +70°C
Positive Supply Voltage to Ground	30V	Storage Temperature Range	-65°C to +150°C
Positive Supply Voltage to Offset Null	0 to 2V	Lead Temperature (Soldering, 60 Sec)	300°C
Power Dissipation (See Note)	500 mW	Output Short Circuit Duration – to ground	Indefinite
Differential Input Voltage	±11V	to V+	1 min.
Input Voltage (V_S = ±15V)	±15V		

Note: Maximum package power dissipation vs. ambient temperature

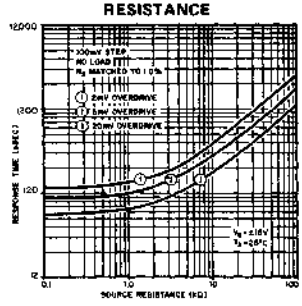
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C
Dual-in-Line (Y)	100°C	10.0 mW/°C

TYPICAL PERFORMANCE CURVES

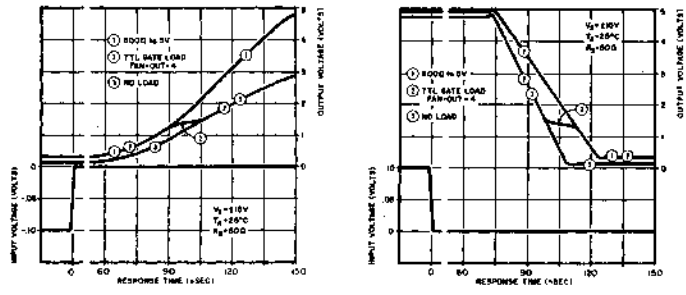
RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



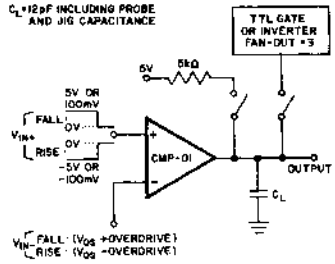
RESPONSE TIME VS SOURCE RESISTANCE



RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



RESPONSE TIME TEST CIRCUIT



ELECTRICAL CHARACTERISTICS			CMP-01			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	mV
Input Offset Current	I_{OS}	(Note 1)	–	4	25	nA
Input Bias Current	I_B		–	350	600	nA
Differential Input Resistance	R_{in}		3.0	14	–	MΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V	200	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		no load (no pull-up)	–	110	180	nsec
		5kΩ to 5V	–	110	–	nsec
		TTL fan-out = 4, no pull-up	–	110	–	nsec
		5V step 5mV overdrive				
		no load (no pull-up)	–	160	–	nsec
		5kΩ to 5V	–	160	–	nsec
		TTL fan-out = 4, no pull-up	–	160	–	nsec
Input Slew Rate			–	92	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, I_O = 320μA	2.4	3.2	–	V
		$V_{in} \geq 3mV$, I_O = 0	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.3	0.45	V
		$V_{in} \leq -10mV$, $I_{sink} \leq 12$ mA	–	0.38	0.5	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	2.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	5.6	8.0	mA
Negative Supply Current	I–	$V_{in} \leq -10mV$	–	1.3	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	103	153	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5	–	mV
These specifications apply for V_{S+} = 5V, V_{S-} = 0V, T_A = 25°C, unless otherwise noted.						
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.5	mV
Input Offset Current	I_{OS}	(Note 1)	–	3	21	nA
Input Bias Current	I_B		–	250	500	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Note 1)	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		5kΩ to 5V	–	150	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	150	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4$ mA	–	0.3	0.45	V
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	2.3	3.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.5	16.0	mW
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.						
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.5	1.6	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	–	0.6	2.8	mV
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	R_S = 50Ω	–	1.5	–	μV/°C
With External Trim	TCV_{OSn}	R_S = 50Ω	–	1.0	–	μV/°C
Input Offset Current	I_{OS}	T_A = +125°C (Note 1)	–	4	25	nA
		T_A = –55°C (Note 1)	–	8	80	nA
Average Input Offset Current Drift	TCI_{OS}	25°C ≤ T_A ≤ +125°C	–	12	–	pA/°C
		–55°C ≤ T_A ≤ 25°C	–	35	–	pA/°C
Input Bias Current	I_B	T_A = +125°C	–	300	600	nA
		T_A = –55°C	–	550	1400	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		T_A = +125°C, no load		160	–	nsec
		T_A = –55°C, no load	–	90	–	nsec
Input Voltage Range	CMVR		±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR		88	106	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, I_O = 200μA	2.4	3.0	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, $I_{sink} > 0$	–	0.20	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.32	0.5	V

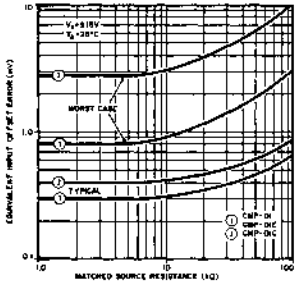
NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

ELECTRICAL CHARACTERISTICS			CMP-01E			CMP-01C			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	–	0.4	2.8	mV
Input Offset Current	I_{OS}	(Note 1)	–	4	25	–	5	80	nA
Input Bias Current	I_B		–	350	600	–	400	900	nA
Differential Input Resistance	R_{in}		3.0	14	–	1.0	10	–	MΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V	200	500	–	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		no load (no pull-up)	–	110	180	–	110	180	nsec
		5kΩ to 5V	–	110	–	–	110	–	nsec
		TTL fan-out = 4, no pull-up	–	110	–	–	110	–	nsec
		5V step 5mV overdrive							
		no load (no pull-up)	–	160	–	–	160	–	nsec
		5kΩ to 5V	–	160	–	–	160	–	nsec
		TTL fan-out = 4, no pull-up	–	160	–	–	160	–	nsec
Input Slew Rate			–	92	–	–	92	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	–	74	98	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, I_O = 320μA	2.4	3.2	–	2.4	3.4	–	V
		$V_{in} \geq 3mV$, I_O = 240μA	–	–		2.4	3.4	–	V
		$V_{in} \geq 3mV$, I_O = 0	2.4	4.8	–	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.16	0.4	–	0.16	0.4	V
		$V_{in} \leq -10mV$, $I_{sink} \leq 6.4$ mA	–	0.31	0.45	–	0.31	0.45	V
Output Leakage Current 1	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	4.0	–	0.05	8.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	5.6	8.0	–	5.6	8.5	mA
Negative Supply Current	I–	$V_{in} \leq -10mV$	–	1.3	2.2	–	1.3	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	103	153	–	103	161	mW
Offset Voltage Adjustment Range		Nulling Pot = 2kΩ	–	±5	–	–	±5	–	mV
These specifications apply for V_{S+} = 5V, V_{S-} = 0V, T_A = 25°C unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.5	–	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	–	3	21	–	4	65	nA
Input Bias Current	I_B		–	250	500	–	300	720	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Note 1)	–	50	–	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		5kΩ to 5V	–	150	–	–	150	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	150	–	–	150	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.8	–	1.8/3.5	1.7/3.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4mA$	–	0.3	0.45	–	0.3	0.45	V
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	2.3	3.2	–	2.4	3.8	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.5	16.0	–	12.0	19.0	mW
The following specifications apply for V_S = ±15V, 0 ≤ T_A ≤ +70°C unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.4	–	0.5	3.5	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	–	0.5	2.4	–	0.6	4.3	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	R_S = 50Ω	–	1.5	–	–	1.8	–	μV/°C
With External Trim	TCV_{OSn}	R_S = 50Ω	–	1.0	–	–	1.2	–	μV/°C
Input Offset Current	I_{OS}	T_A = +70°C (Note 1)	–	4	25	–	5	80	nA
		T_A = 0°C (Note 1)	–	5	45	–	6	120	nA
Average Input Offset Current Drift	TCI_{OS}	25°C ≤ T_A ≤ +70°C	–	12	–	–	12	–	pA/°C
		0°C ≤ T_A ≤ 25°C	–	35	–	–	40	–	pA/°C
Input Bias Current	I_B	T_A = +70°C	–	330	600	–	340	900	nA
		T_A = 0°C	–	400	950	–	450	1200	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V	100	500	–	70	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		T_A = +70°C, no load	–	130	–	–	130	–	nsec
		T_A = 0°C, no load	–	100	–	–	100	–	nsec
Input Voltage Range	CMVR		±12.0	±13.3	–	±12.0	±13.3	–	V
Common Mode Rejection Ratio	CMRR		90	108	–	86	108	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S-} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	–	70	88	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, I_O = 200μA	2.4	3.2	–	2.4	3.2	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.17	0.4	–	0.17	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.3	0.5	–	0.31	0.5	V

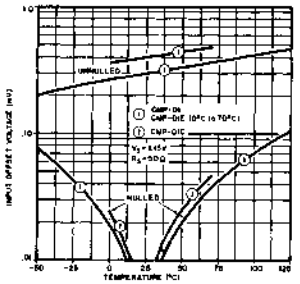
NOTE 1 These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

TYPICAL PERFORMANCE CURVES

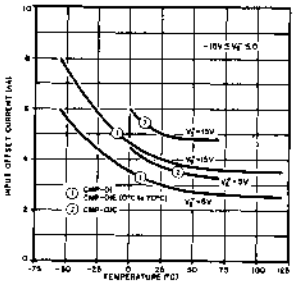
INPUT OFFSET ERROR VS SOURCE RESISTANCE



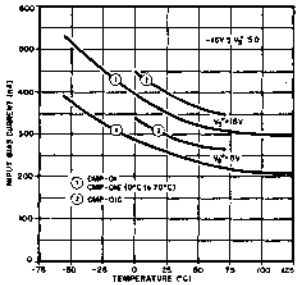
OFFSET VOLTAGE VS. TEMPERATURE



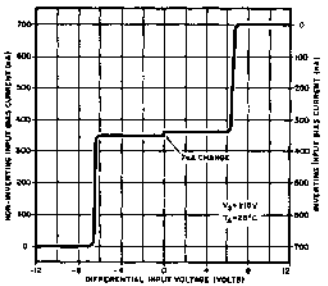
INPUT OFFSET CURRENT VS TEMPERATURE



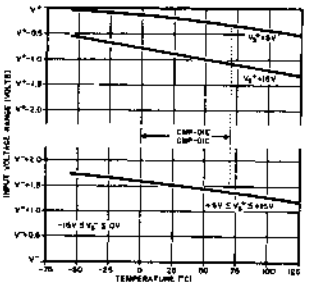
INPUT BIAS CURRENT VS TEMPERATURE



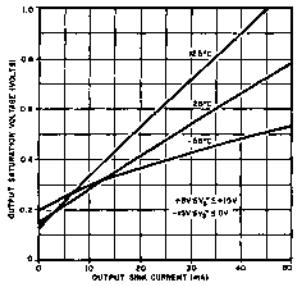
INPUT BIAS CURRENT VS DIFFENTIAL INPUT VOLTAGE



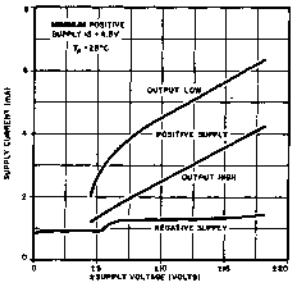
INPUT VOLTAGE RANGE VS TEMPERATURE



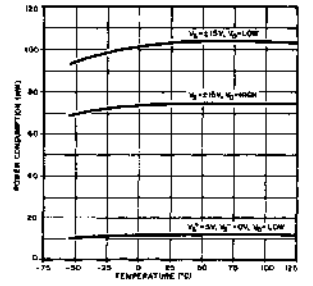
SATURATION VOLTAGE VS SINK CURRENT



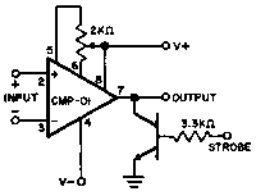
SUPPLY CURRENT VS SUPPLY VOLTAGE



POWER CONSUMPTION VS TEMPERATURE

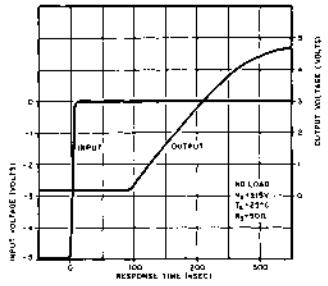


OFFSET TRIMMING AND STROBE CIRCUITRY

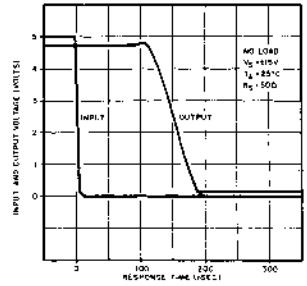


RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE

RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE



RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE

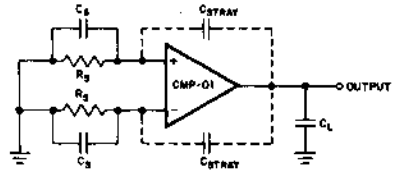


APPLICATION NOTES

The CMP-01 provides *fast* response times even with small input overdrives, to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. D. C. characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g. a ground plane between output and input), capacitive output loading (IC_L), or a capacitor from the compensation terminal to A.C. ground (DIP only). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Positive resistive feedback creating a hysteresis condition can be very effective – see diagram on page 6. Matched bypass capacitors across the input resistors also can eliminate the instability,

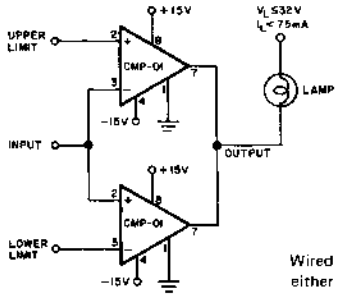
$$\text{and if } C_S \geq 20\ pF\left[\frac{\text{maximum step size}}{\text{minimum overdrive}}\right]$$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.



TYPICAL APPLICATIONS

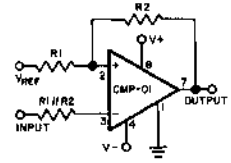
PRECISION, DUAL LIMIT, GO/NO GO TESTER



Wired OR Output is low when either limit is exceeded.

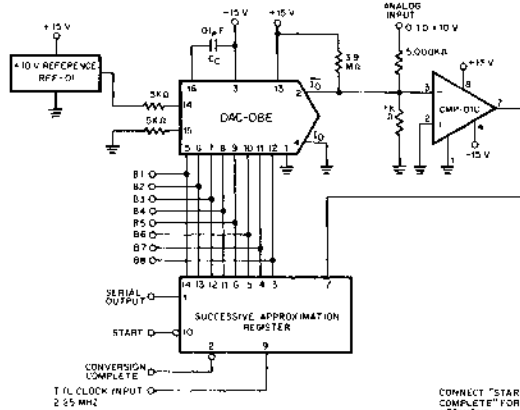
Output is high when input is within limits.

LEVEL DETECTOR WITH HYSTERESIS (Positive Feedback)



$$\text{Hysteresis width} \leq 4V\ \frac{R_1}{R_1 + R_2}$$

3 IC LOW COST A/D CONVERTER



CONNECT "START" TO "CONVERSION COMPLETE" FOR CONTINUOUS CONVERSIONS.

CMP-02

LOW INPUT CURRENT PRECISION COMPARATOR

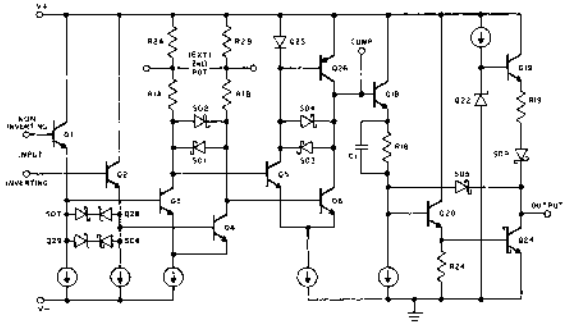
GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-or capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 Fast Precision Comparator data sheet.

FEATURES

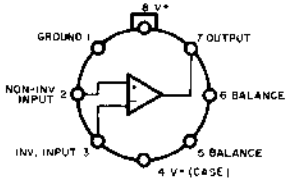
- Low Offset Voltage . . . . . 0.3 mV typ., 0.8 mV Max
- Low Offset Current . . . . . 0.3 nA typ., 3.0 nA Max
- Low Bias Current . . . . . 28 nA typ., 50 nA Max
- Low Offset Drift . . . . . 1.0 $\mu V/^{\circ}C$, 4 $pA/^{\circ}C$
- High Gain . . . . . 200,000 Min
- High CMRR . . . . . 110 dB typ., 94 dB Min
- High Input Impedance . . . . . 16 MΩ
- Fast Response Time . . . . . 190 ns typ., 270 ns Max
- Standard Power Supplies . . . . . ±5V to ±18V
- Guaranteed Operation from Single +5V Supply
- No Pull-up Resistor Required for TTL Drive
- Wired-OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling . . . . . Single 2KΩ Potentiometer
- Easy to Use . . . . . Free from Oscillations

SIMPLIFIED SCHEMATIC

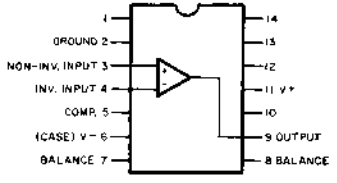


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)
ORDER: CMP-02J
CMP-02EJ
CMP-02CJ



14 PIN HERMETIC DIP (Y-Suffix)
ORDER: CMP-02Y
CMP-02EY
CMP-02CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing
CMP02-883-J
CMP02-883-Y

ABSOLUTE MAXIMUM RATINGS

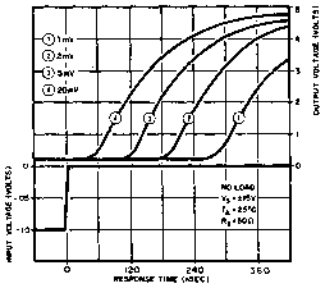
Total Supply Voltage, V+ to V−	36V
Output to Ground	−5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Power Dissipation (See Note)	500 mW
Differential Input Voltage	±11V
Input Voltage (V_S = ±15V)	±15V
Output Sink Current (Continuous Operation)	75 mA
Operating Temperature Range —	
CMP-02	-55°C to +125°C
CMP-02E, -02C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 Sec)	300°C
Output Short Circuit Duration — to ground	Indefinite
to V+	1 min.

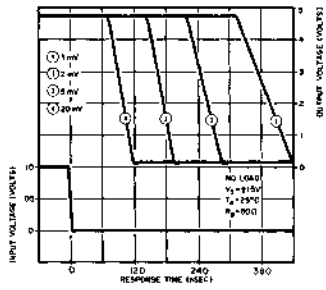
Note: Maximum package power dissipation vs. ambient temperature

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C
Dual-in-Line (Y)	100°C	10.0 mW/°C

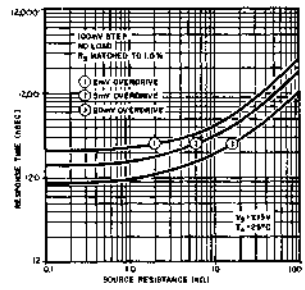
TYPICAL PERFORMANCE CURVES

RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES

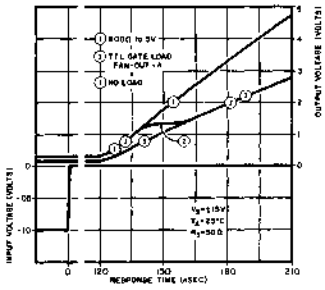


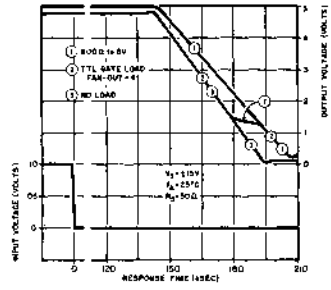


RESPONSE TIME VS SOURCE RESISTANCE

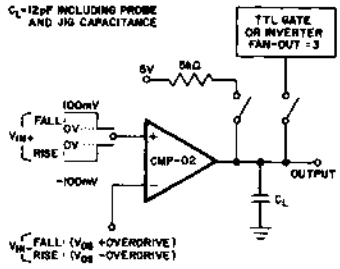


RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS





RESPONSE TIME TEST CIRCUIT



ELECTRICAL CHARACTERISTICS			CMP-02			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	mV
Input Offset Voltage	V_{OS}	$R_S \leq 50K\Omega$ (Note 1)	–	0.3	0.9	mV
Input Offset Current	I_{OS}	(Note 1)	–	0.3	3.0	nA
Input Bias Current	I_B		–	28	50	nA
Differential Input Resistance	R_{in}		5.0	16	–	MΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V	200	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		no load (no pull-up)	–	190	270	nsec
		5kΩ to 5V	–	190	–	nsec
		TTL fan-out = 4, no pull-up	–	190	–	nsec
Input Slew Rate			–	12.5	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, I_O = 320μA	2.4	3.2	–	V
		$V_{in} \geq 3mV$, I_O = 0	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.3	0.45	V
		$V_{in} \leq -10mV$, I_{sink} = 12 mA	–	0.36	0.5	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	2.0	μA
Positive Supply Current	I_+	$V_{in} \leq -10mV$	–	5.5	8.0	mA
Negative Supply Current	I_-	$V_{in} \leq -10mV$	–	1.1	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	99	153	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5.0	–	mV
These specifications apply for V_{S+} = 5V, V_{S-} = 0V, T_A = 25°C, unless otherwise noted.						
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.5	mV
Input Offset Current	I_{OS}	(Note 1)	–	0.25	3.0	nA
Input Bias Current	I_B		–	24	45	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Note 1)	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		5kΩ to 5V	–	250	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	250	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.9	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4$ mA	–	0.30	0.45	V
Positive Supply Current	I_+	$V_{in} \leq -10mV$	–	2.2	3.0	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.0	15.0	mW
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.						
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.5	1.6	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	–	0.6	2.8	mV
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	R_S = 50Ω	–	1.5	–	μV/°C
With External Trim	TCV_{OSn}	R_S = 50Ω	–	1.0	–	μV/°C
Input Offset Current	I_{OS}	T_A = +125°C (Note 1)	–	0.3	4.0	nA
		T_A = −55°C (Note 1)	–	0.6	12.0	nA
Average Input Offset Current Drift	TCI_{OS}	25°C ≤ T_A ≤ +125°C	–	2.0	–	pA/°C
		−55°C ≤ T_A ≤ 25°C	–	4.0	–	pA/°C
Input Bias Current	I_B	T_A = +125°C	–	25	50	nA
		T_A = −55°C	–	45	120	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		T_A = +125°C, no load	–	310	–	nsec
		T_A = −55°C, no load	–	165	–	nsec
Input Voltage Range	CMVR		±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR		88	106	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, I_O = 200μA	2.4	3.0	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.20	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.32	0.5	V

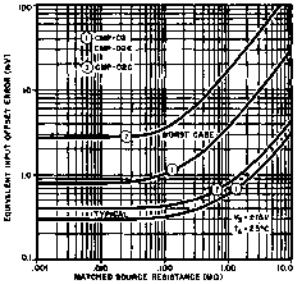
NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

ELECTRICAL CHARACTERISTICS			CMP-02E			CMP-02C			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	–	0.4	2.8	mV
Input Offset Voltage	V_{OS}	$R_S \leq 50K\Omega$ (Note 1)	–	0.3	0.9	–	0.4	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	–	0.3	3.0	–	0.4	15	nA
Input Bias Current	I_B		–	28	50	–	35	100	nA
Differential Input Resistance	R_{in}		5.0	16	–	1.5	12	–	MΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V	200	500	–	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		no load (no pull-up)	–	190	270	–	190	270	nsec
		5kΩ to 5V	–	190	–	–	190	–	nsec
		TTL fan-out = 4, no pull-up	–	190	–	–	190	–	nsec
Input Slew Rate			–	15	–	–	15	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	–	74	98	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, I_O = 320μA	2.4	3.2	–	–	–	–	V
		$V_{in} \geq 3mV$, I_O = 240μA	–	–	–	2.4	3.4	–	V
		$V_{in} \geq 3mV$, I_O = 0	2.4	4.8	–	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.16	0.4	–	0.16	0.4	V
		$V_{in} \leq -10mV$, $I_{sink} \leq 6.4$ mA	–	0.31	0.45	–	0.31	0.45	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	4.0	–	0.05	8.0	μA
Positive Supply Current	I_+	$V_{in} \leq -10mV$	–	5.5	8.0	–	5.6	8.5	mA
Negative Supply Current	I_-	$V_{in} \leq -10mV$	–	1.1	2.2	–	1.2	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	99	153	–	102	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5.0	–	–	±5.0	–	mV
These specifications apply for V_S+ = 5V, V_S- = 0V, T_A = 25°C unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.6	–	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	–	0.25	3.0	–	0.35	14	nA
Input Bias Current	I_B		–	24	45	–	30	90	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Note 1)	–	50	–	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		5kΩ to 5V	–	250	–	–	250	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	250	–	–	250	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.8	–	1.8/3.5	1.7/3.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4$ mA	–	0.3	0.45	–	0.3	0.45	V
Positive Supply Current	I_+	$V_{in} \leq -10mV$	–	2.2	3.0	–	2.3	3.6	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.0	15.0	–	11.5	18.0	mW
The following specifications apply for V_S = ±15V, 0° ≤ T_A ≤ +70°C unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.4	–	0.5	3.5	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	–	0.6	2.4	–	0.6	4.3	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	R_S = 50Ω	–	1.5	–	–	1.8	–	μV/°C
With External Trim	TCV_{OSn}	R_S = 50Ω	–	1.0	–	–	1.2	–	μV/°C
Input Offset Current	I_{OS}	T_A = +70°C (Note 1)	–	0.3	3.0	–	0.4	15	nA
		T_A = 0°C (Note 1)	–	0.4	6.0	–	0.5	25	nA
Average Input Offset Current Drift	TCI_{OS}	25°C ≤ T_A ≤ +70°C	–	2.0	–	–	3.0	–	pA/°C
		0°C ≤ T_A ≤ 25°C	–	4.0	–	–	5.0	–	pA/°C
Input Bias Current	I_B	T_A = +70°C	–	26	50	–	33	100	nA
		T_A = 0°C	–	34	80	–	42	160	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V	100	500	–	70	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		T_A = +70°C, no load	–	225	–	–	225	–	nsec
		T_A = 0°C, no load	–	180	–	–	180	–	nsec
Input Voltage Range	CMVR		+12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR		90	108	–	86	108	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	–	70	88	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, I_O = 200μA	2.4	3.2	–	2.4	3.2	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.17	0.4	–	0.17	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.30	0.5	–	0.31	0.5	V

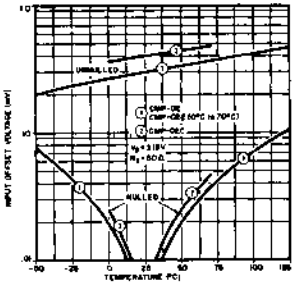
NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

TYPICAL PERFORMANCE CURVES

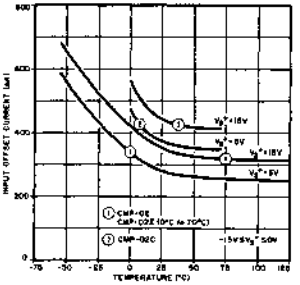
INPUT OFFSET ERROR VS SOURCE RESISTANCE



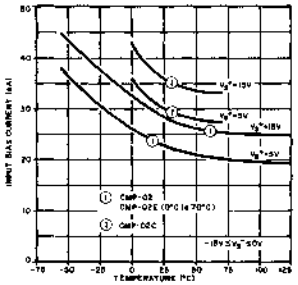
OFFSET VOLTAGE VS TEMPERATURE



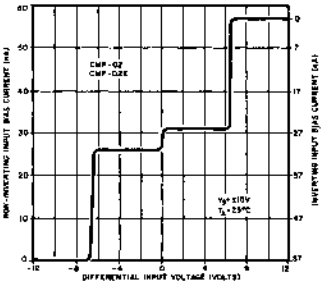
INPUT OFFSET CURRENT VS TEMPERATURE



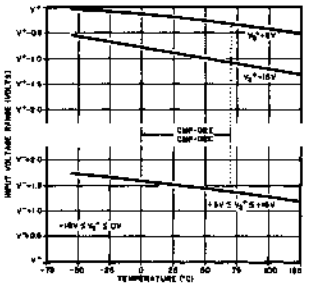
INPUT BIAS CURRENT VS TEMPERATURE



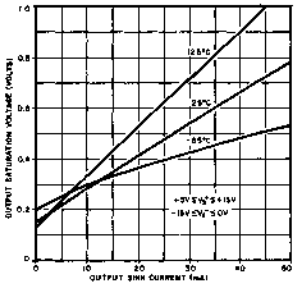
INPUT BIAS CURRENT VS DIFFENTIAL INPUT VOLTAGE



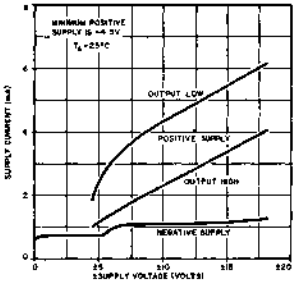
INPUT VOLTAGE RANGE VS TEMPERATURE



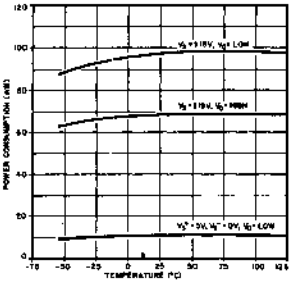
SATURATION VOLTAGE VS SINK CURRENT



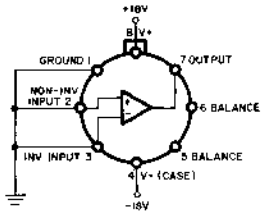
SUPPLY CURRENT VS SUPPLY VOLTAGE



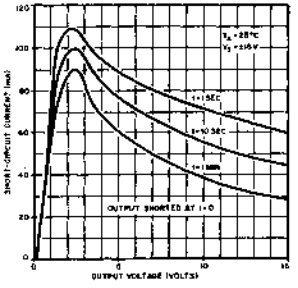
POWER CONSUMPTION VS TEMPERATURE



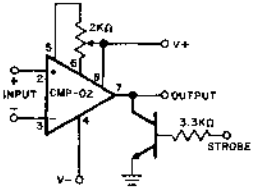
STANDARD BURN-IN CIRCUIT



OUTPUT SHORT-CIRCUIT CURRENT VS OUTPUT VOLTAGE



OFFSET TRIMMING AND STROBE CIRCUITRY

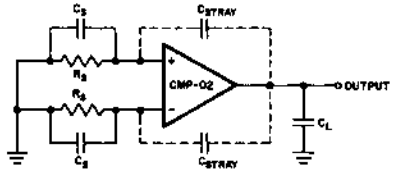


APPLICATION NOTES

The CMP-02 provides fast response times even with small input overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. D. C. characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g. a ground plane between output and input), capacitive output loading (C_L), or a capacitor from the compensation terminal to A.C. ground (DIP only). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Positive resistive feedback creating a hysteresis condition can be very effective – see diagram on page 6. Matched bypass capacitors across the input resistors also can eliminate the instability,

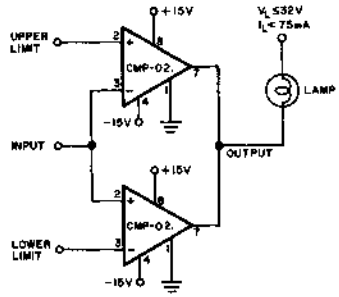
$$\text{and if } C_S \geq 20\text{ pF}\left[\frac{\text{maximum step size}}{\text{minimum overdrive}}\right]$$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.



TYPICAL APPLICATIONS

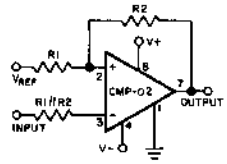
PRECISION, DUAL LIMIT, GO/NO GO TESTER



Wired OR Output is low when either limit is exceeded.

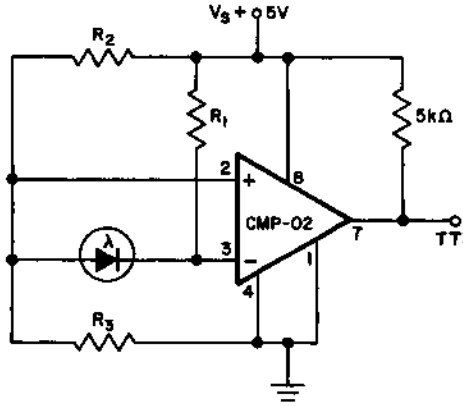
Output is high when input is within limits.

LEVEL DETECTOR WITH HYSTERESIS (Positive Feedback)



$$\text{Hysteresis width} \leq 4V\,\frac{R_1}{R_1 + R_2}$$

PRECISION PHOTODIODE LEVEL DETECTOR



For R_1 = 2.5 MΩ, $R_2 = R_3$ = 5MΩ, the output state changes at a photo diode current ($I_{\lambda T}$) of 0.5μA. (The output changes state at threshold current $I_{\lambda T} = \frac{V_s^+}{2R_2}$ where $R_1 = \frac{R_2}{2}$ and $R_3 = R_2$)

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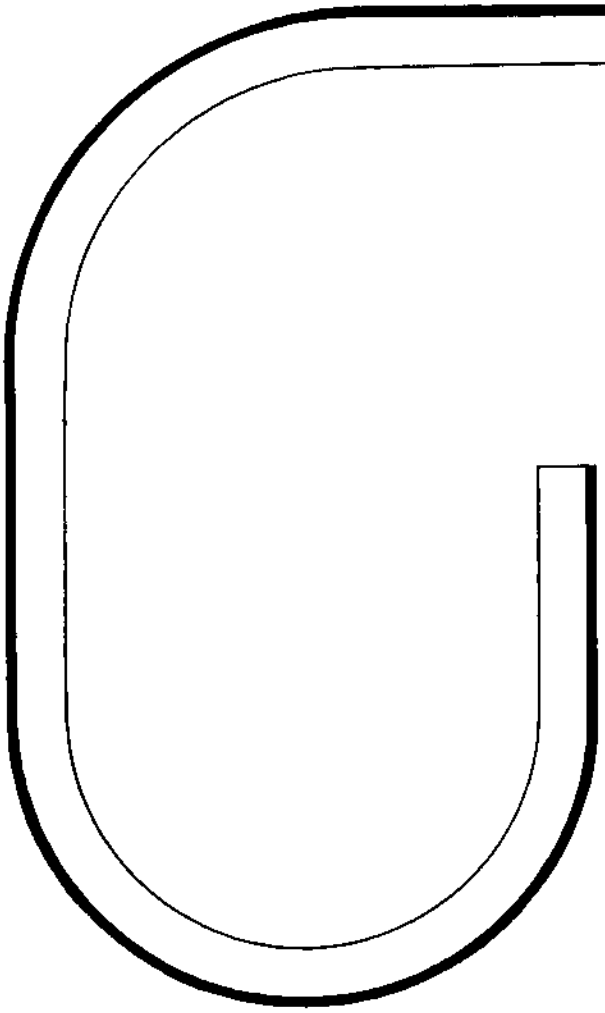

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MATCHED TRANSISTORS

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MAT-01

ULTRA-MATCHED MONOLITHIC DUAL TRANSISTOR

EXCELLENT LOG CONFORMANCE

GENERAL DESCRIPTION

The MAT-01 series are monolithic ultra-tightly matched dual NPN transistors, fabricated using an exclusive Silicon Nitride "Triple-Passivation" process which provides extreme stability of critical parameters versus both temperature and time. Outstanding matching characteristics include offset voltages of 40μV, temperature drift of V_{OS} of 0.15μV/°C and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 @ I_C = 10nano amperes! Excellent logarithmic conformance over a seven decade collector current span suggests application in log/antilog and multiplier/divider circuitry. The very low values of noise voltage and current make the MAT-01 ideal for usage in critical low-level input stages while the 6 pin TO-99 package allows direct replacement of most previous dual transistors for immediate performance improvements. The very high h_{FE} at low collector currents also makes the MAT-01 attractive in all high impedance and micropower circuit designs.

FEATURES

- Tight V_{OS} (V_{BE} Match) . . . . 40μV Typ, 100μV Max
- Low TC V_{OS} . . . . . 0.15μV/°C Typ, 0.5μV/°C Max
- Tight h_{FE} Match . . . . . 0.7% Typ, 3.0% Max
- High h_{FE} . . . . . 770 Typ, 500 Min
- Excellent h_{FE} Linearity from 10nA to 10mA
- High h_{FE} at Low I_C . . . . . 590 Typ @ I_C = 10nA
- Low Noise Voltage . . . . 0.23μVp-p — 0.1Hz to 10Hz
- Excellent Long Term Stability . . 0.2μV/Month, Typ
- High Breakdowns . . . . . 45V and 60V Min
- Precision Logarithmic Conformance
- Direct Replacement for Most Dual Transistors

ABSOLUTE MAXIMUM RATINGS

	MAT-01 AH, GH	MAT-01 H, FH
Collector-Base Voltage (BV_{CBO})	45V	60V
Collector-Emitter Voltage (BV_{CEO})	45V	60V
Collector-Collector Voltage (BV_{CC})	45V	60V
Emitter-Emitter Voltage (BV_{EE})	45V	60V
Emitter-Base Voltage (BV_{EBO}) (Note 1)	5V	5V
Collector Current (I_C)	25mA	25mA
Emitter Current (I_E)	25mA	25mA

	MAT-01 AH, GH	MAT-01 H, FH
Total Power Dissipation		
Case Temperature ≤ 40°C (Note 2)	1.8W	1.8W
Ambient Temperature ≤ 70°C (Note 3)	500mW	500mW
Operating Ambient Temperature	-55°C to +125°C	
Operating Junction Temperature	-55°C to +150°C	
Storage Temperature	-65°C to +150°C	
Lead Temperature (Soldering, 60 sec.)	300°C	

NOTES

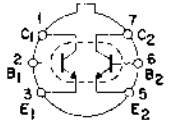
Note 1: Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.

Note 2: Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/°C for case temperatures above 40°C.

Note 3: Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/°C for ambient temperatures above 70°C.

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



Note: Substrate is connected to case.

ORDER: MAT-01AH
MAT-01H
MAT-01FH
MAT-01GH

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: MAT01-883-AH
MAT01-883-H
MAT01-883-FH
MAT01-883-GH

ELECTRICAL CHARACTERISTICS

These specifications apply for V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

			MAT-01AH			MAT-01GH			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Breakdown Voltage	BV_{CEO}		45	–	–	45	–	–	V
Offset Voltage	V_{OS}		–	0.04	0.1	–	0.10	0.50	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	–	2.0	–	–	2.0	–	μV/Month
Long Term	V_{OS}/Time	(Note 2)	–	0.2	–	–	0.2	–	μV/Month
Offset Current	I_{OS}		–	0.1	0.6	–	0.2	3.2	nA
Bias Current	I_B		–	13	20	–	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	–	590	–	–	430	–	
	h_{FE}	I_C = 10μA	500	770	–	250	560	–	
	h_{FE}	I_C = 10mA	–	840	–	–	610	–	
Current Gain Match	Δh_{FE}		–	0.7	3.0	–	1.0	8.0	%
	Δh_{FE}	100nA ≤ I_C ≤ 10mA	–	0.8	–	–	1.2	–	%
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	–	0.23	0.4	–	0.23	0.4	μVp-p
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	–	0.60	–	–	0.60	–	μV_{RMS}
Narrowband Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	–	7.0	9.0	–	7.0	9.0	$nV/\sqrt{Hz}$
		f_o = 100Hz (Note 3)	–	6.1	7.6	–	6.1	7.6	$nV/\sqrt{Hz}$
		f_o = 1000Hz (Note 3)	–	6.0	7.5	–	6.0	7.5	$nV/\sqrt{Hz}$
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	–	0.5	3.0	–	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	–	2.0	15	–	3.0	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0 (Note 4)	–	15	50	–	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0 (Note 4)	–	50	200	–	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 30	–	20	200	–	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	–	0.12	0.20	–	0.12	0.25	V
	$V_{CE(SAT)}$	I_B = 1mA, I_C = 10mA	–	0.8	–	–	0.8	–	V
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	–	450	–	–	450	–	MHz
Output Capacitance	C_{ob}	V_{CE} = 15V, I_E = 0	–	2.8	–	–	2.8	–	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	–	8.5	–	–	8.5	–	pF
The following specifications apply for V_{CB} = 15V, I_C = 10μA, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Offset Voltage	V_{OS}		–	0.06	0.15	–	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 3)	–	0.15	0.50	–	0.35	1.8	μV/°C
Offset Current	I_{OS}		–	0.9	8.0	–	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 3)	–	10	90		15	150	pA/°C
Bias Current	I_B		–	28	60	–	36	130	nA
Current Gain	h_{FE}		167	400	–	77	300	–	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 30V, I_E = 0 (Note 4)	–	15	80	–	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 30V, V_{BE} = 0 (Note 4)	–	50	300	–	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 30V	–	30	200	–	50	400	nA

NOTES:

Note 1: Exclude first hour of operation to allow for stabilization of external circuitry.

Note 2: Parameter describes long term average drift trend after first month of operation.

Note 3: Parameter is not 100% tested; 90% of all units meet this specification.

Note 4: The collector-base (I_{CBO}) and collector-emitter (I_{CEO}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.

ELECTRICAL CHARACTERISTICS

These specifications apply for V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

			MAT-01H			MAT-01FH			
Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Breakdown Voltage	BV_{CEO}		60	–	–	60	–	–	V
Offset Voltage	V_{OS}		–	0.04	0.1	–	0.10	0.50	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	–	2.0	–	–	2.0	–	μV/Month
Long Term	V_{OS}/Time	(Note 2)	–	0.2	–	–	0.2	–	μV/Month
Offset Current	I_{OS}		–	0.1	0.8	–	0.2	3.2	nA
Bias Current	I_B	–	–	15	30	–	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	–	520	–	–	430	–	
	h_{FE}	I_C = 10μA	330	680	–	250	560	–	
	h_{FE}	I_C = 10mA	–	740	–	–	610	–	
Current Gain Match	Δh_{FE}		–	0.7	2.7	–	1.0	8.0	%
	Δh_{FE}	100nA ≤ I_C ≤ 10mA	–	0.8	–	–	1.2	–	%
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	–	0.23	0.4	–	0.23	0.4	μVp-p
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	–	0.60	–	–	0.60	–	μV_{RMS}
Narrowband Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	–	7.0	9.0	–	7.0	9.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	–	6.1	7.6	–	6.1	7.6	$nV/\sqrt{Hz}$
		f_O = 1000Hz (Note 3)	–	6.0	7.5	–	6.0	7.5	$nV/\sqrt{Hz}$
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 45V	–	0.5	3.0	–	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 45V	–	2.0	15.0	–	3.0	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 45V, I_E = 0 (Note 4)	–	15	50	–	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 45V, V_{BE} = 0 (Note 4)	–	50	200	–	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 45	–	20	200	–	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	–	0.12	0.20	–	0.12	0.25	V
	$V_{CE(SAT)}$	I_B = 1mA, I_C = 10mA	–	0.8	–	–	0.8	–	V
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	–	450	–	–	450	–	MHz
Output Capacitance	C_{ob}	V_{CE} = 15V, I_E = 0	–	2.8	–	–	2.8	–	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	–	8.5	–	–	8.5	–	pF
The following specifications apply for V_{CB} = 15V, I_C = 10μA, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Offset Voltage	V_{OS}		–	0.06	0.15	–	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 3)	–	0.15	0.50	–	0.35	1.8	μV/°C
Offset Current	I_{OS}		–	0.9	9.0	–	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 3)	–	11	110	–	15	150	pA/°C
Bias Current	I_B		–	30	95	–	36	130	nA
Current Gain	h_{FE}		105	350	–	77	300	–	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 45V, I_E = 0 (Note 4)	–	15	80	–	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 45V, V_{BE} = 0 (Note 4)	–	50	300	–	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 45V	–	30	200	–	50	400	nA

NOTES:

Note 1: Exclude first hour of operation to allow for stabilization of external circuitry.

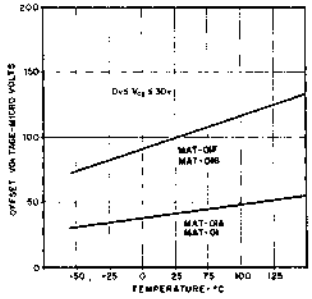
Note 2: Parameter describes long term average drift trend after first month of operation.

Note 3: Parameter is not 100% tested; 90% of all units meet this specification.

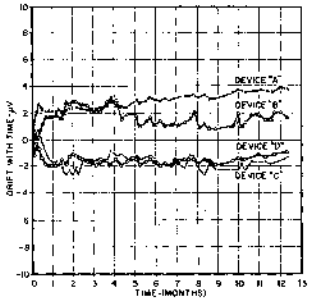
Note 4: The collector-base (I_{CBO}) and collector-emitter (I_{CEO}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.

TYPICAL PERFORMANCE CURVES

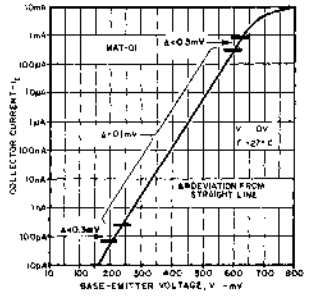
OFFSET VOLTAGE VS. TEMPERATURE



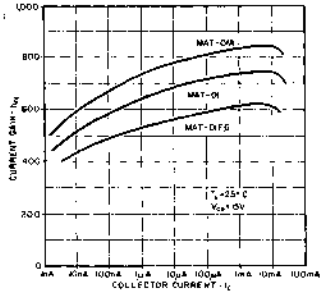
OFFSET DRIFT VS. TIME



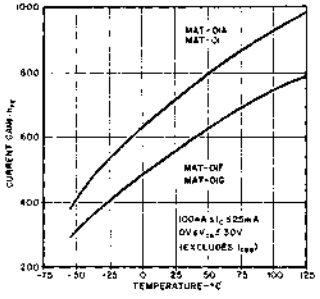
BASE-EMITTER VOLTAGE VS. COLLECTOR CURRENT



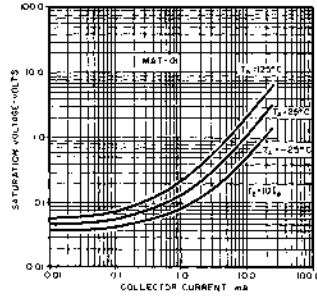
CURRENT GAIN VS. COLLECTOR CURRENT



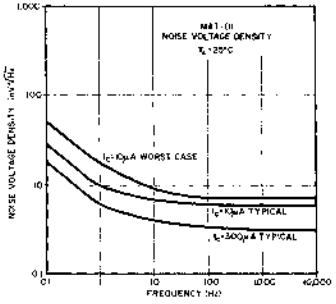
CURRENT GAIN VS. TEMPERATURE



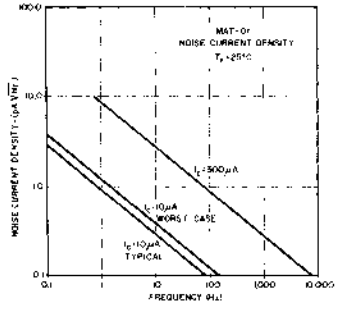
SATURATION VOLTAGE VS. COLLECTOR CURRENT



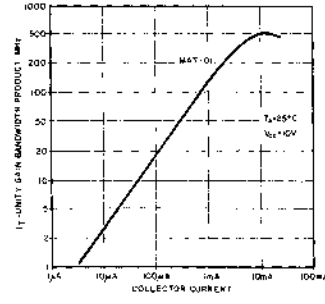
NOISE VOLTAGE DENSITY



NOISE CURRENT DENSITY

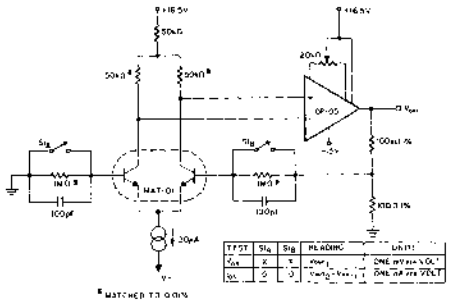


GAIN-BANDWIDTH VS. COLLECTOR CURRENT

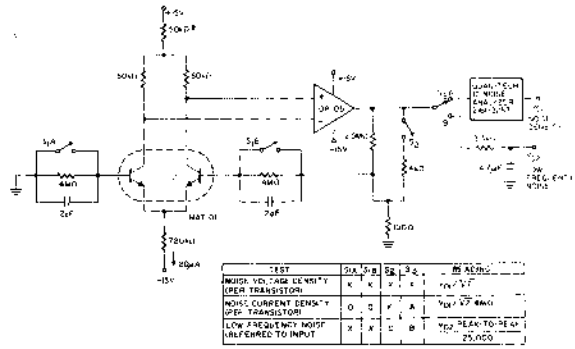


MAT-01 TEST CIRCUITS

MAT-01 MATCHING MEASUREMENT CIRCUIT



MAT-01 NOISE MEASUREMENT CIRCUIT



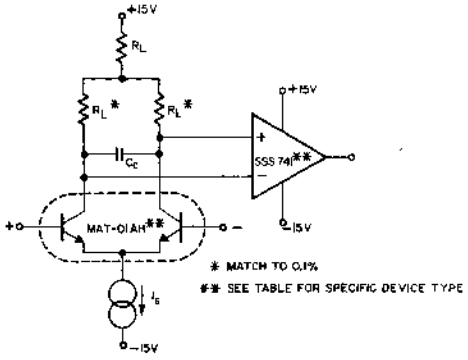
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics; circuit designs should be checked to insure that such reverse bias voltages cannot be applied during transient conditions, such as at circuit turn-on and turn-off.

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input terminals are maintained at the same temperature, preferrably close to the temperature of the device's package.

TYPICAL APPLICATIONS

PRECISION OPERATIONAL AMPLIFIERS

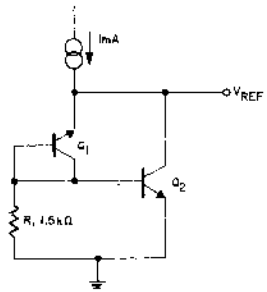


* MATCH TO 0.1%

** SEE TABLE FOR SPECIFIC DEVICE TYPE

	MAT-01AH SSS 741	MAT-01AH SSS 741	MAT-01GH SSS 741C	MAT-01GH SSS 741C
V_{OS} MAX	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} MAX	.6μV/°C	1μV/°C	2μV/°C	4μV/°C
I_{OS} MAX	0.8nA	0.1nA	3.2nA	0.32nA
I_B MAX	20nA	2nA	40nA	4nA
GAIN MIN	2,000,000	2,000,000	800,000	800,000
I_S	20μA	2μA	20μA	2μA
R_L	100kΩ	1MΩ	100kΩ	1MΩ

PRECISION REFERENCE



$V_{REF} \approx 7.0V$

$TCV_{REF} \approx 10ppm/°C$

$R_O \approx 40\Omega$

R_1 may be adjusted to minimize TCV_{REF}. Increasing R_1 will cause a positive change in TCV_{REF}.

Note: h_{FE} of Q1 will be reduced by operation in breakdown mode.

CROSS REFERENCE – MAT-01 TO MONOLITHIC DUAL TRANSISTORS (I_C = 10μA)

DEVICE	BV_{CEO} MIN (V)	V_{os} MAX (mV)	TCV_{os} MAX (μV/°C)	h_{FE} MIN	I_{os} MAX (nA)	TCI_{os} MAX (pA/°C)
MAT-01AH	**45**	**0.1**	**0.5**	**500**	**0.6**	**90**
MAT-01H	**60**	**0.1**	**0.5**	**330**	**0.8**	**110**
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**3.2**	**150**
MAT 01GH	**45**	**0.5**	**1.8**	**250**	**3.2**	**150**
LM114A	45	0.5	2.0	500	2.0	- - -
LM114	45	2.0	10	250	10	- - -
LM115A	60	0.5	2.0	250	2.0	- - -
LM115	60	2.0	10	250	10	- - -
AD810	35	3.0	15	100	2.0	600
AD811	45	1.5	7.5	200	10	300
AD812	35	1.0	5.0	400	2.5	300
AD813	45	0.5	2.5	200	5	300
AD818	20	1.0	5.0	200	10	300

CROSS REFERENCE – MAT-01 TO 2N TYPES (I_C = 10μA)

DEVICE	BV_{CEO} MIN (V)	V_{os} MAX (mV)	TCV_{os} MAX (μV/°C)	h_{FE} MIN	$\%h_{FE}$ MATCH MAX	I_{os} MAX (nA)	TCI_{os} MAX (pA/°C)
MAT-01GH	**45**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

Notes: 1. TCI_{os} Max and I_{os} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of the above are physically interchangeable pin-for-pin with MAT-01 series.

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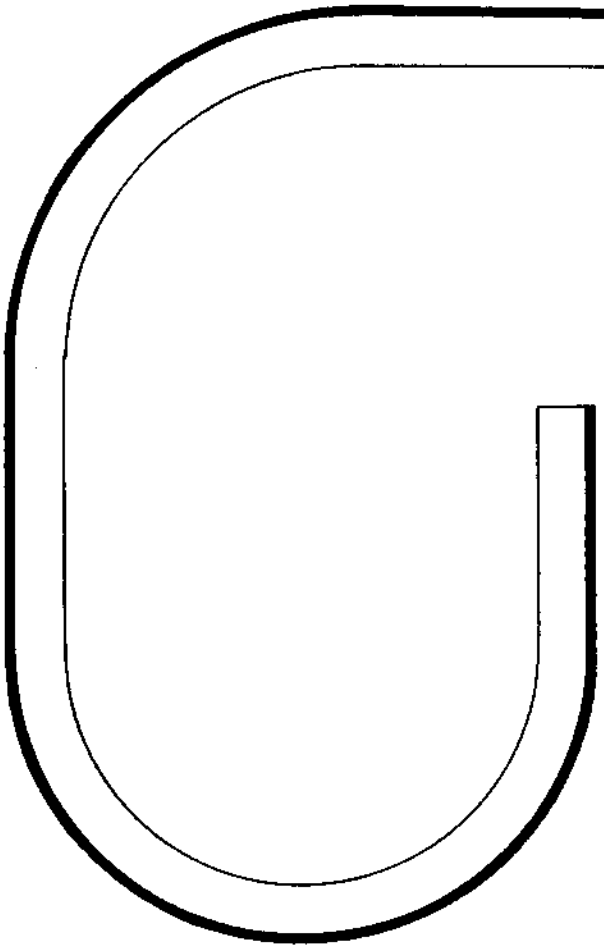

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VOLTAGE REFERENCE

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REF-01

+10V PRECISION VOLTAGE REFERENCE

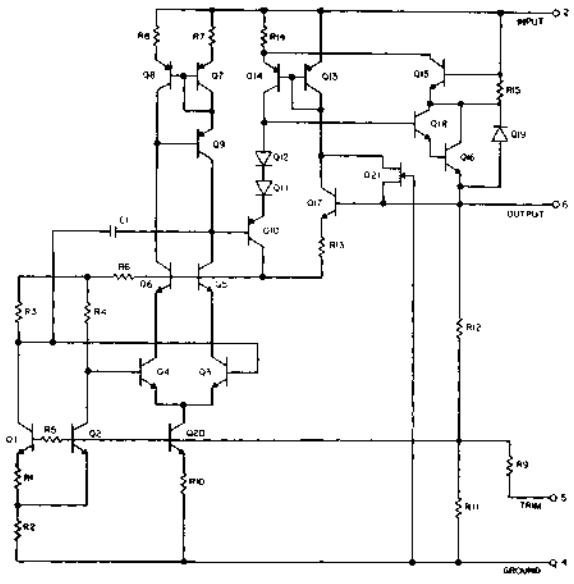
GENERAL DESCRIPTION

The REF-01 Precision Voltage Reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 12 to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-01 an excellent choice whenever a stable voltage reference is required, such as in D/A and A/D converters, in portable instruments, and in digital voltmeters. Full military temperature range devices with screening to MIL-STD-883A are available.

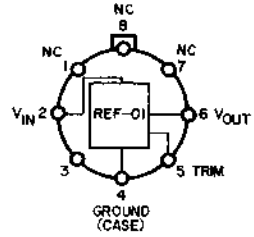
FEATURES

- Adjustable 10 Volt Output . . . . . ±3%
- Excellent Temperature Stability . . . . . 3 ppm/°C
- Low Noise 20μVp-p
- Low Power 15mW
- Wide Input Voltage Range . . . . . 12 to 40V
- High Load Driving Capability 20mA
- No External Components
- Short Circuit Proof
- MIL-STD-883A Screening Available

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)

ORDER: REF-01AJ
REF-01J
REF-01EJ
REF-01HJ
REF-01CJ
REF-01DJ

Military Temperature Range Devices
with MIL-STD-883A Class B Processing:

ORDER: REF01-883-AJ
REF01-883-J

ABSOLUTE MAXIMUM RATINGS

Input Voltage REF-01, A, E, H	40 V	Operating Temperature Range	
REF-01C, D	30 V	REF-01A, REF-01	−55°C to +125°C
Power Dissipation (see note)	500mW	REF-01E, REF-01H, REF-01D REF-01C,	0°C to +70°C
Output Short Circuit Duration (to ground or V_{IN})	Indefinite		
Storage Temperature Range	−65°C to +150°C		
Lead Temperature (Soldering, 60 sec)	300°C		

Note: Derate at 7.1mW/°C above 80°C ambient temperature.

ELECTRICAL CHARACTERISTICS

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	REF-01A Min	REF-01A Typ	REF-01A Max	REF-01 Min	REF-01 Typ	REF-01 Max	Units
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	–	±3.0	±3.3	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	–	20	30	–	20	30	µVp-p
Input Voltage Range	V_{IN}		12	–	40	12	–	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	–	0.005	0.008	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	µsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		−0.3	−0.5	–	−0.3	−0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
The following specifications apply for V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C **and** I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature (Notes 1 and 2)	ΔV_{OT}	0° ≤ T_A ≤ +70°C	–	0.02	0.06	–	0.07	0.17	%
		−55° ≤ T_A ≤ +125°C	–	0.06	0.15	–	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/°C/%
Line Regulation (V_{IN} = 13 to 33V) (Note 4)		0° ≤ T_A ≤ +70°C	–	0.007	0.012	–	0.007	0.012	%/V
		−55° ≤ T_A ≤ +125°C	–	0.009	0.015	–	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0° ≤ T_A ≤ +70°C	–	0.006	0.010	–	0.007	0.012	%/mA
		−55° ≤ T_A ≤ +125°C	–	0.007	0.012	–	0.009	0.015	%/mA

NOTE 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2: ΔV_{OT} specification applies trimmed to 10.000V or untrimmed.

NOTE 3: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O(0°\text{to}+70°C) = \frac{\Delta V_{OT}\ 0°\text{to}+70°C}{70°C}$

and $TCV_O(-55°\text{to}+125°C) = \frac{\Delta V_{OT}\ -55\ \text{to}+125°C}{180°C}$

NOTE 4: Line and Load Regulation specifications include the effects of self heating.

NOTE 5: Parameter is not 100% tested; 90% of units meet this specification.

REF-01 DEFINITIONS

LINE REGULATION
The ratio of the change in output voltage to the change in line voltage producing it.

LOAD REGULATION
The ratio of the change in output voltage to the change in load current producing it.

QUIESCENT CURRENT (I_{SY})
The current required from the supply to operate the device with no load.

OUTPUT TURN-ON SETTLING TIME (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

OUTPUT VOLTAGE NOISE (e_{np-p})
The peak to peak output noise voltage in a specified frequency band.

OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT})
The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

OUTPUT TEMPERATURE COEFFICIENT (TCV_O)
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

ELECTRICAL CHARACTERISTICS

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	REF-01E Min	REF-01E Typ	REF-01E Max	REF-01H Min	REF-01H Typ	REF-01H Max	Units
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	µVp-p
Input Voltage Range	V_{IN}		12	—	40	12	—	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10 mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	µsec
Quiescent Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		–0.3	–0.5	—	–0.3	–0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.

Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.02	0.06	—	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/°C/%
Line Regulation (Note 4)		V_{IN} = 13 to 33V	—	0.007	0.012	—	0.007	0.012	%/V
Load Regulation (Note 4)		I_L = 0 to 8 mA	—	0.006	0.010	—	0.007	0.012	%/mA

NOTE 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

NOTE 3: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

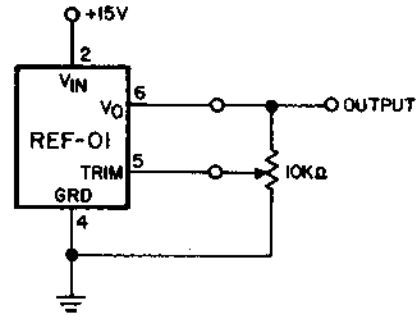
NOTE 4: Line and Load Regulation specifications include the effects of self heating.

NOTE 5: Parameter is not 100% tested; 90% of units meet this specification.

OUTPUT ADJUSTMENT

The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7 ppm/°C for 100mV of output adjustment.



ELECTRICAL CHARACTERISTICS

			REF-01C			REF-01D			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	9.850	10.00	10.150	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	–	±2.0	±3.3	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	–	25	35	–	25	–	µVp-p
Input Voltage Range	V_{IN}		12	–	30	12	–	30	V
Line Regulation (Note 4)		V_{IN} = 13 to 30V	–	0.009	0.015	–	0.012	0.04	%/V
Load Regulation (Note 4)		I_L = 0 to 8 mA	–	0.006	0.015	–	–	–	%/mA
Load Regulation (Note 4)		I_L = 0 to 4 mA	–	–	–	–	0.009	0.04	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	µsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.6	–	1.0	2.0	mA
Load Current	I_L		8	21	–	8	21	–	mA
Sink Current	I_S		–0.2	–0.5	–	–0.2	–0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	–	0.14	0.45	–	0.49	–	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	–	20	65	–	70	–	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (Note 4)		V_{IN} = 13 to 30V	–	0.011	0.018	–	0.020	–	%/V
Load Regulation (Note 4)		I_L = 0 to 5 mA	–	0.008	0.018	–	0.020	–	%/mA

NOTE 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

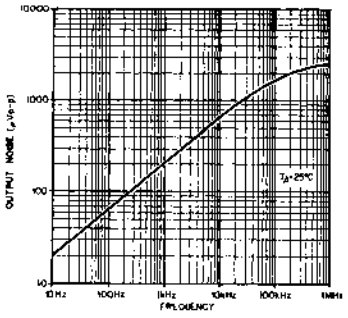
NOTE 3: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

NOTE 4: Line and Load Regulation specifications include the effects of self heating.

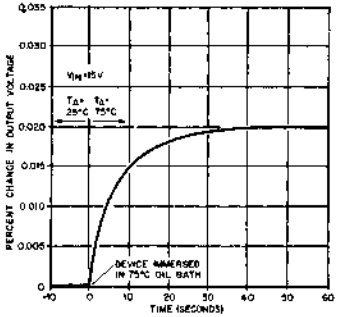
NOTE 5: Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

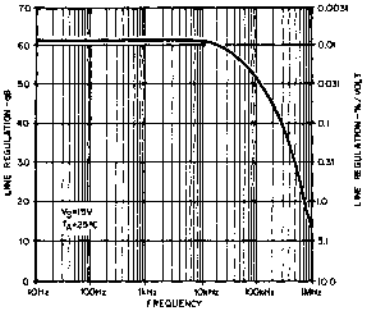
OUTPUT WIDEBAND NOISE VS BANDWIDTH (.1 Hz TO FREQUENCY INDICATED)



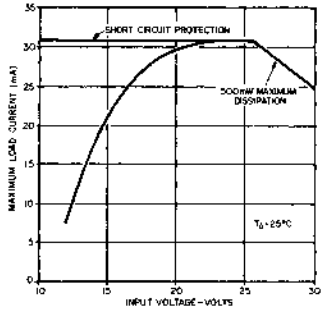
OUTPUT CHANGE DUE TO THERMAL SHOCK



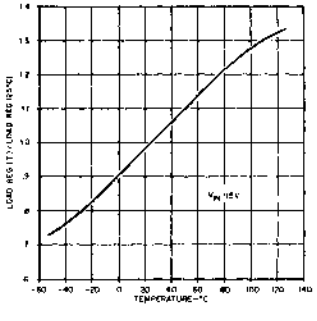
LINE REGULATION VS FREQUENCY



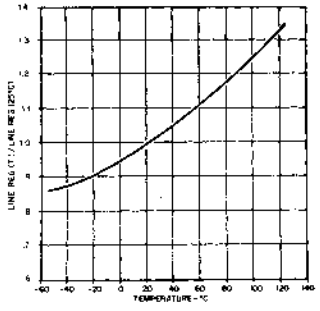
MAXIMUM LOAD CURRENT VS INPUT VOLTAGE



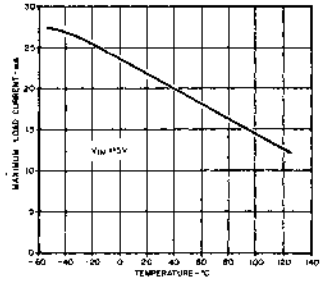
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) VS TEMPERATURE



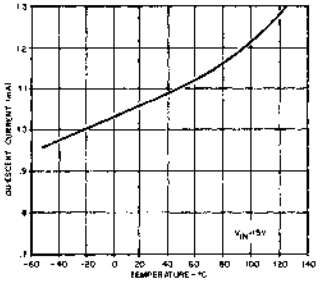
NORMALIZED LINE REGULATION VS TEMPERATURE



MAXIMUM LOAD CURRENT VS TEMPERATURE

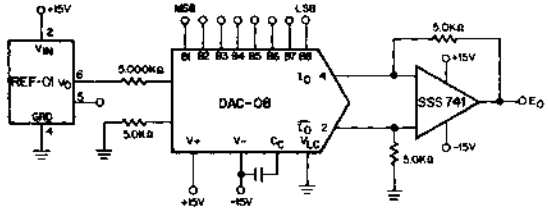


QUIESCENT CURRENT VS TEMPERATURE



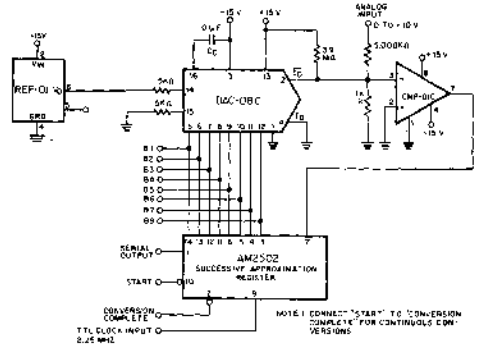
TYPICAL APPLICATIONS

D/A CONVERTER REFERENCE

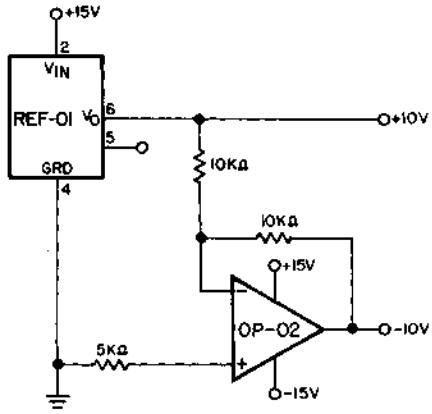


	B1	B2	B3	B4	B5	B6	B7	B8	EO
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE+LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(-) ZERO SCALE	0	1	1	1	1	1	1	1	-0.040
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	-9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	-9.920

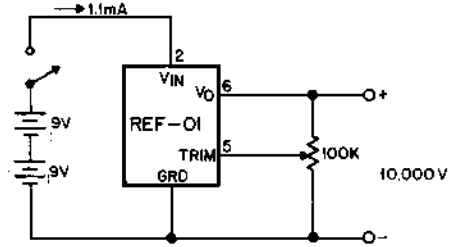
A/D CONVERTER REFERENCE



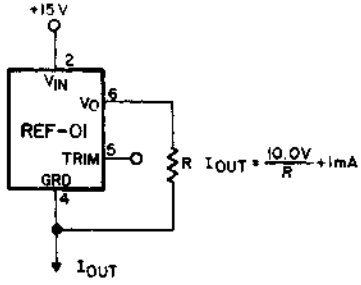
±10V REFERENCE



PRECISION CALIBRATION STANDARD

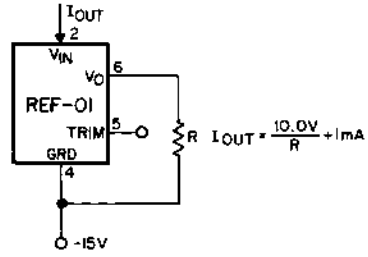


CURRENT SOURCE



VOLTAGE COMPLIANCE: -25V TO +3V

CURRENT SINK



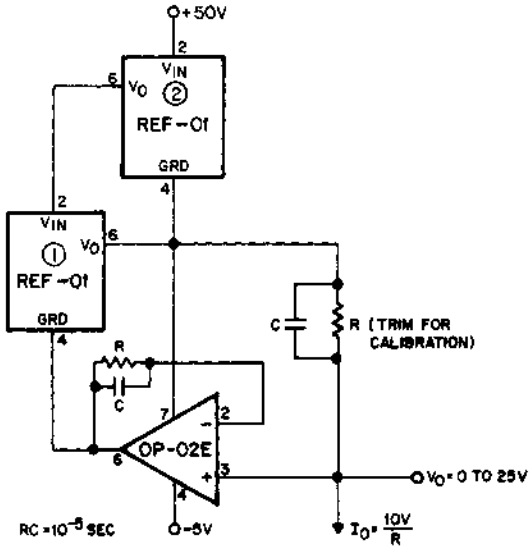
VOLTAGE COMPLIANCE: -3V TO +25V

TYPICAL APPLICATIONS

PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-01 ② keeps the line voltage and power dissipation constant in device ① ; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8 ppm change (3μV/V x 25V/10V) in output current over a 25V range; for example, a 10mA current source can be built (R = 1kΩ) with 300 MΩ output impedance

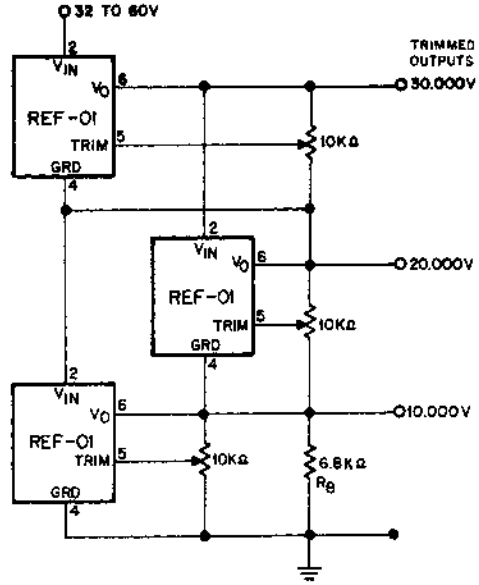
$$\left(R_O = \frac{25V}{8\times10^{-6}\times10mA}\right)$$



REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-01's can be stacked to yield 10.000, 20.000 and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.000 and 20.000 output voltages. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general any number of REF-01's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30, . . . 100V. The line voltage can range from 105 to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



REF-02

+5V PRECISION VOLTAGE REFERENCE/THERMOMETER

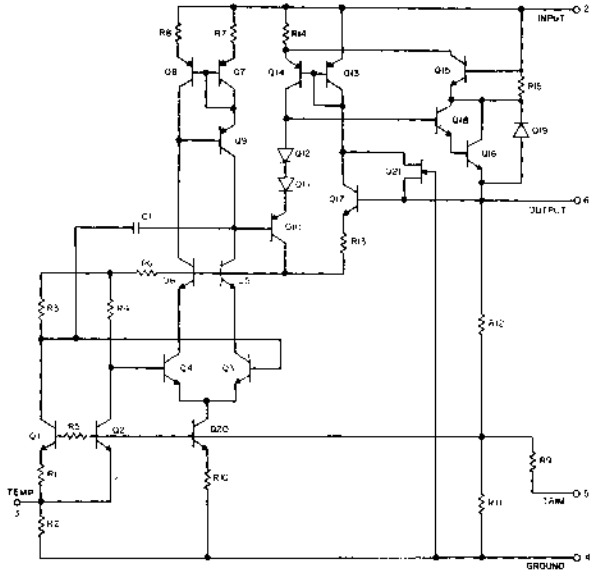
GENERAL DESCRIPTION

The REF-02 Precision Voltage Reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-02 an excellent choice whenever a stable voltage reference is required, such as in D/A and A/D converters, in portable instruments, and in digital voltmeters. The versatility of the REF-02 is illustrated by its use as a monolithic thermometer. (See AN-18, "Thermometer Applications of the REF-02.") For +10V Precision Voltage References see the REF-01 data sheet.

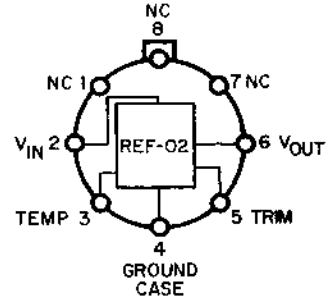
FEATURES

- Temperature Voltage Output . . . . . 2.1 mV/°C
- Adjustable 5 Volt Output . . . . . ±6%
- Excellent Temperature Stability . . . . . 3 ppm/°C
- Low Noise 10μVp-p
- Low Power 15mW
- Wide Input Voltage Range . . . . . 7V to 40V
- High Load Driving Capability 20mA
- No External Components
- Short Circuit Proof
- MIL-STD-883A Screening Available

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)

ORDER: REF-02AJ
REF-02J
REF-02EJ
REF-02HJ
REF-02CJ
REF-02DJ

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

ORDER: REF02-883-AJ
REF02-883-J

ABSOLUTE MAXIMUM RATINGS

Input Voltage REF-02, A, E, H	40 V	Operating Temperature Range	
REF-02C, D	30 V	REF-02A, REF-02	-55°C to +125°C
Power Dissipation (see note)	500mW	REF-02E, REF-02H REF-02C, REF-02D	0°C to +70°C
Output Short Circuit Duration (to ground or V_{IN})	Indefinite		
Storage Temperature Range	-65°C to +150°C	Note: Derate at 7.1mW/°C above 80°C ambient temperature.	
Lead Temperature (Soldering, 60 sec)	300°C		

ELECTRICAL CHARACTERISTICS

			REF-02A			REF-02			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±6.0	–	±3.0	±6.0	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	10	15	–	10	15	µVp-p
Input Voltage Range	V_{IN}		7	–	40	7	–	40	V
Line Regulation (Note 2)		V_{IN} = 8 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 2)		I_L = 0 to 10mA	–	0.005	0.010	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	µsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		–0.3	–0.5	–	–0.3	–0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
Temp Voltage Output	V_T	(Note 3)	–	630	–	–	630	–	mV
The following specifications apply for V_{IN} = +15V, –55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature (Notes 4 and 5)	ΔV_{OT}	0° ≤ T_A ≤ +70°C	–	0.02	0.06	–	0.07	0.17	%
		–55° ≤ T_A ≤ +125°C	–	0.06	0.15	–	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/°C/%
Line Regulation (V_{IN} = 8 to 33V) (Note 2)		0° ≤ T_A ≤ +70°C	–	0.007	0.012	–	0.007	0.012	%/V
		–55° ≤ T_A ≤ +125°C	–	0.009	0.015	–	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 2)		0° ≤ T_A ≤ +70°C	–	0.006	0.010	–	0.007	0.012	%/mA
		–55° ≤ T_A ≤ +125°C	–	0.007	0.012	–	0.009	0.015	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 3)	–	2.1	–	–	2.1	–	mV/°C

NOTE 1: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Line and Load Regulation specifications include the effects of self heating.

NOTE 3: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 4: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

NOTE 5: ΔV_{OT} specification applies trimmed to 5.000V or untrimmed.

NOTE 6: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., TCV_O (0° to +70°C) = $\frac{\Delta V_{OT}\ 0^\circ \text{ to } +70^\circ C}{70^\circ C}$

and TCV_O (–55° to +125°C) = $\frac{\Delta V_{OT}\ -55^\circ \text{ to } +125^\circ C}{180^\circ C}$

REF-02 DEFINITIONS

LINE REGULATION
The ratio of the change in output voltage to the change in line voltage producing it.

LOAD REGULATION
The ratio of the change in output voltage to the change in load current producing it.

QUIESCENT CURRENT (I_{SY})
The current required from the supply to operate the device with no load.

OUTPUT TURN-ON SETTLING TIME (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}

OUTPUT VOLTAGE NOISE (e_{np-p})
The peak to peak output noise voltage in a specified frequency band.

OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT})
The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

OUTPUT TEMPERATURE COEFFICIENT (TCV_O)
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

ELECTRICAL CHARACTERISTICS

			REF-02E			REF-02H			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0 mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±6.0	—	±3.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	10	15	—	10	15	μVp-p
Input Voltage Range	V_{IN}		7	—	40	7	—	40	V
Line Regulation (Note 2)		V_{IN} = 8 to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		I_L = 0 to 10 mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	—	5.0	—	μsec
Quiescent Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temp Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.02	0.06	—	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		V_{IN} = 8 to 33V	—	0.007	0.012	—	0.007	0.012	%/V
Load Regulation (Note 2)		I_L = 0 to 8 mA	—	0.006	0.010	—	0.007	0.012	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTE 1: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Line and Load Regulation specifications include the effects of self heating.

NOTE 3: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 4: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

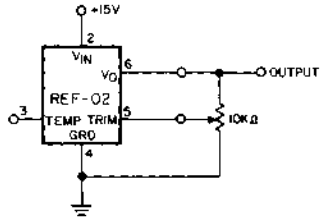
NOTE 5: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

NOTE 6: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

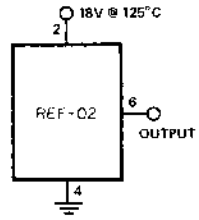
OUTPUT ADJUSTMENT

The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V, or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7 ppm/°C for 100mV of output adjustment.



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS

			REF-02C			REF-02D			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0 mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±6.0	–	+2.0	±6.0	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	12	18	–	12	–	μVp-p
Input Voltage Range	V_{IN}		7	–	30	7	–	30	V
Line Regulation (Note 2)		V_{IN} = 8 to 30V	–	0.009	0.015	–	0.010	0.04	%/V
Load Regulation (Note 2)		I_L = 0 to 8 mA	–	0.006	0.015	–	–	–	%/mA
Load Regulation (Note 2)		I_L = 0 to 4 mA	–	–	–	–	0.015	0.04	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	μsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.6	–	1.0	2.0	mA
Load Current	I_L		8	21	–	8	21	–	mA
Sink Current	I_S		–0.2	–0.5	–	–0.2	–0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
Temp Voltage Output	V_T	(Note 3)	–	630	–	–	630	–	mV
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	–	0.14	0.45	–	0.49	–	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	–	20	65	–	70	–	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (Note 2)		V_{IN} = 8 to 30V	–	0.011	0.018	–	0.012	–	%/V
Load Regulation (Note 2)		I_L = 0 to 5 mA	–	0.008	0.018	–	0.016	–	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 3)	–	2.1	–	–	2.1	–	mV/°C

NOTE 1: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Line and Load Regulation specifications include the effects of self heating.

NOTE 3: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 4: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

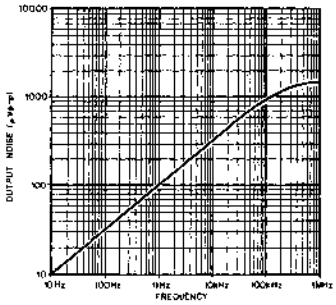
$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

NOTE 5: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

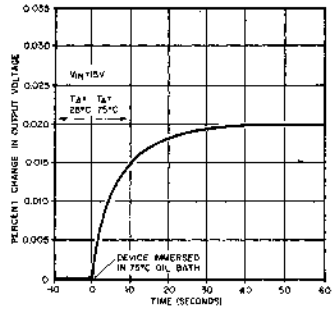
NOTE 6: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

TYPICAL PERFORMANCE CURVES

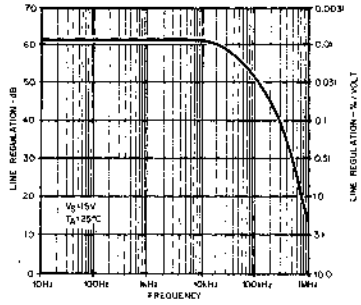
OUTPUT WIDEBAND NOISE VS BANDWIDTH (.1 Hz TO FREQUENCY INDICATED)



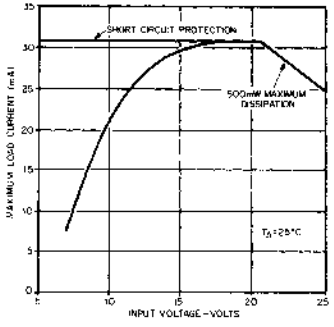
OUTPUT CHANGE DUE TO THERMAL SHOCK



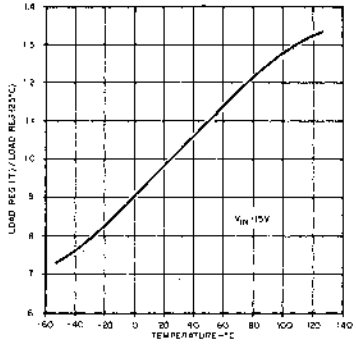
LINE REGULATION VS FREQUENCY



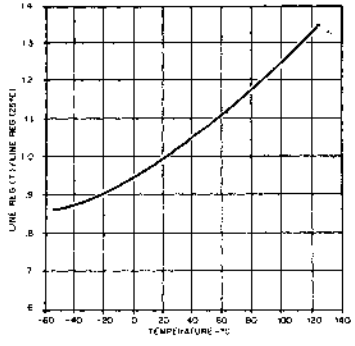
MAXIMUM LOAD CURRENT VS INPUT VOLTAGE



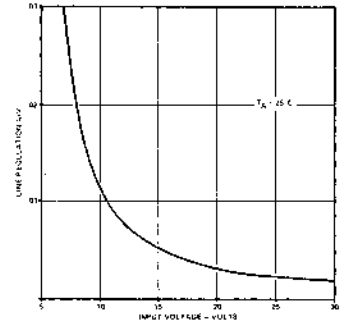
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) VS TEMPERATURE



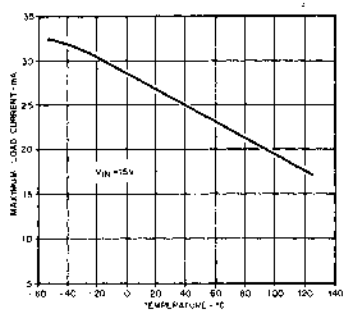
NORMALIZED LINE REGULATION VS TEMPERATURE



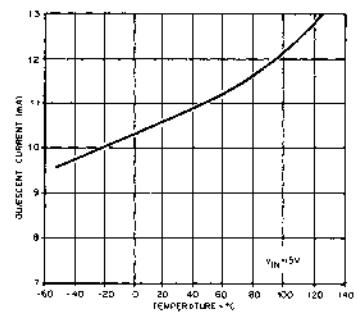
LINE REGULATION VS SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT VS TEMPERATURE

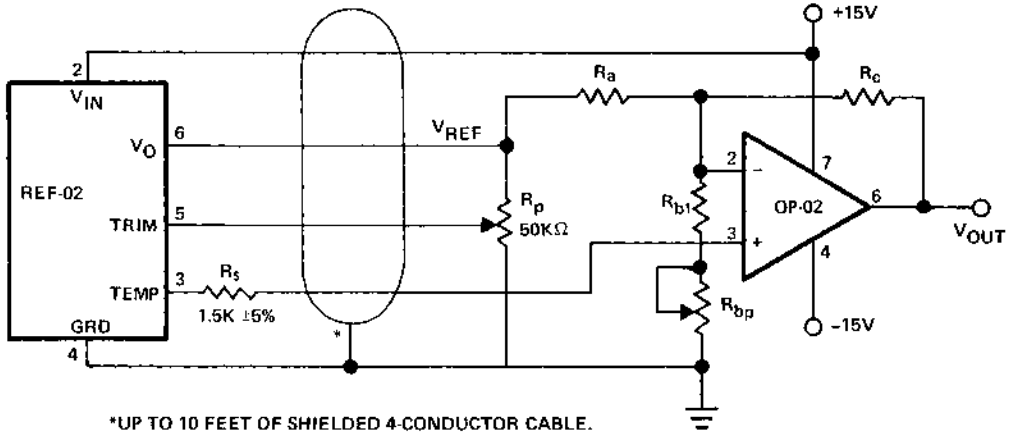


QUIESCENT CURRENT VS TEMPERATURE



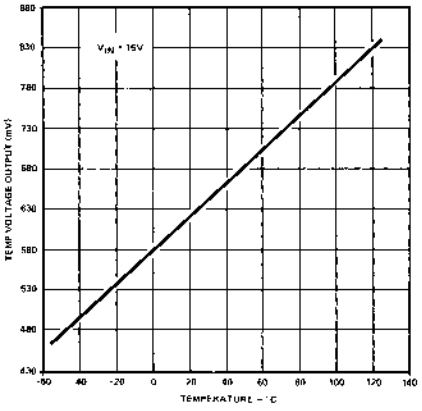
TYPICAL APPLICATIONS

PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



*UP TO 10 FEET OF SHIELDED 4-CONDUCTOR CABLE.

TYPICAL TEMPERATURE VOLTAGE OUTPUT VS TEMPERATURE (REF-02A)



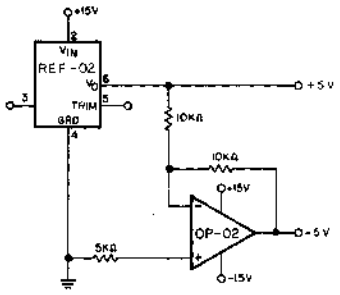
RESISTOR VALUES

TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55° to +125°C	−55° to +125°C	−67°F to +257°C
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (±1% resistor)	9.09KΩ	15KΩ	7.5KΩ
R_{b1} (±1% resistor)	1.5KΩ	1.82KΩ	1.21KΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11KΩ	84.5KΩ	8.25KΩ

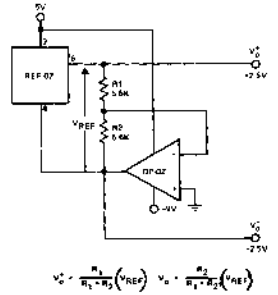
*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if this is a problem.

FOR THEORY OF OPERATION AND CALIBRATION PROCEDURE CONSULT APPLICATION NOTE AN-18, "THERMOMETER APPLICATIONS OF THE REF-02."

±5V REFERENCE

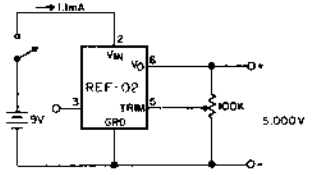


±2.5V REFERENCE



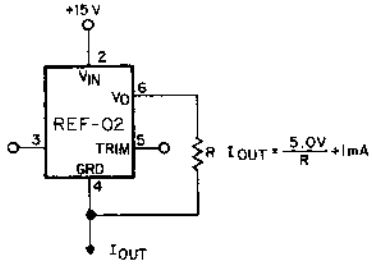
$$V_o^+ = \frac{R_1}{R_1 + R_2}(V_{REF}) \quad V_o^- = \frac{R_2}{R_1 + R_2}(V_{REF})$$

PRECISION CALIBRATION STANDARD



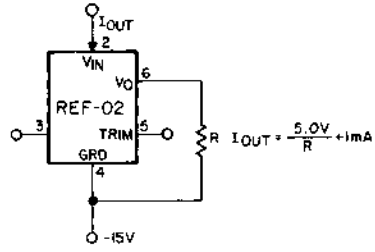
TYPICAL APPLICATIONS

CURRENT SOURCE



VOLTAGE COMPLIANCE: -25V TO +8V

CURRENT SINK

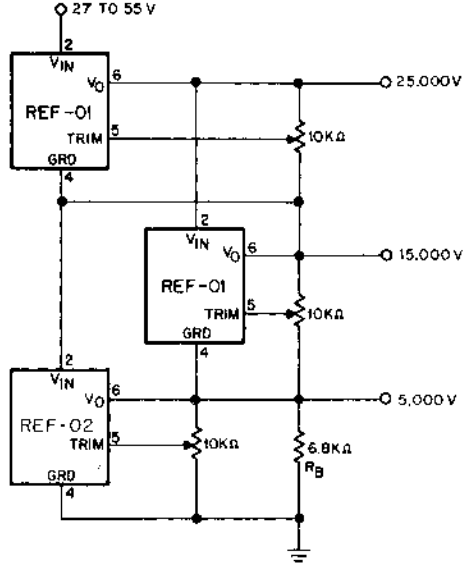


VOLTAGE COMPLIANCE: -8V TO 25V

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-01's and one REF-02 can be stacked to yield 5.000, 15.000 and 25.000V outputs. An additional advantage is near-perfect line regulation of the 5.000 and 15.000 output voltages. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

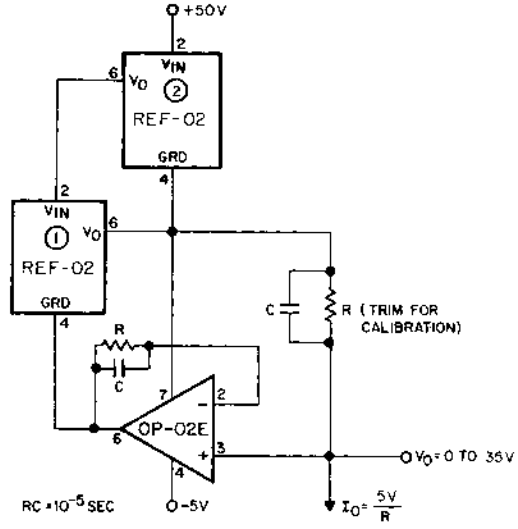
In general any number of REF-01's and REF-02's can be stacked this way. For example, ten devices will yield ten outputs in 5 or 10V steps. The line voltage can range from 100 to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-02 (2) keeps the line voltage and power dissipation constant in device (1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create a 20 ppm change (3μV/V x 35V/5V) in output current over a 35V range; for example, a 5mA current source can be built (R = 1kΩ) with 350 MΩ output impedance:

$$R_O = \left(\frac{35V}{20 \times 10^{-6} \times 5mA}\right)$$



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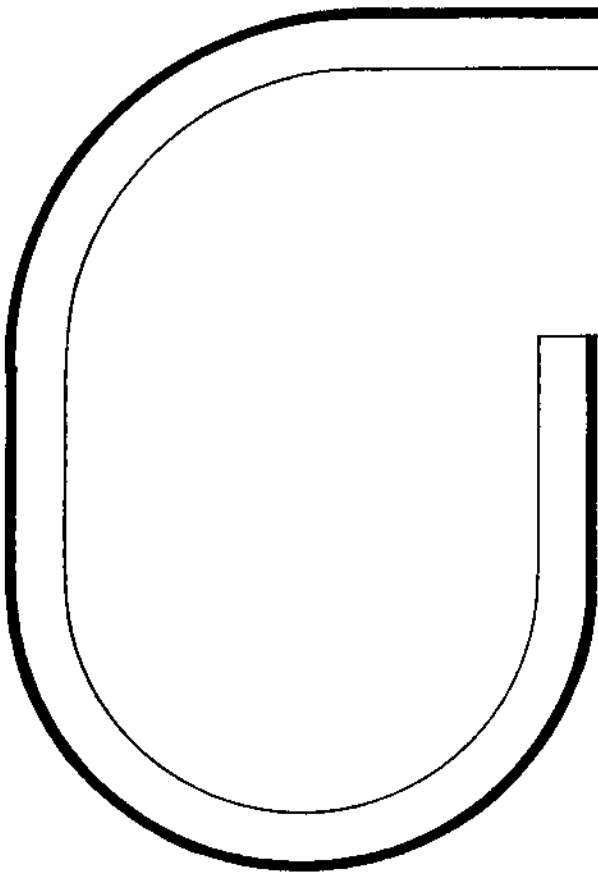

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DIGITAL TO ANALOG CONVERTER SELECTION GUIDE

CURRENT OUTPUT INTERNAL REFERENCE – 10 BIT RESOLUTION

DEVICE	TEMP RANGE FOR SPECIFICATION (°C)	MAXIMUM NONLINEARITY (%FS)	MAX FULL SCALE TEMPCO (ppm/°C)
DAC-100ACQ5	-55/+125	±0.05	60
DAC-100BBQ5	-55/+125	±0.1	30
DAC-100CCQ5	-55/+125	±0.2	60
DAC-100DDQ5	-55/+125	±0.3	120
DAC-100AAQ1 (Q2)	-25/+85	±0.05	15
DAC-100ACQ1 (Q2)	-25/+85	±0.05	60
DAC-100ADQ1 (Q2)	-25/+85	±0.05	120
DAC-100BBQ1 (Q2)	-25/+85	±0.1	30
DAC-100BCQ1 (Q2)	-25/+85	±0.1	60
DAC-100CCQ1 (Q2)	-25/+85	±0.2	60
DAC-100DDQ1 (Q2)	-25/+85	±0.3	120
DAC-100ACQ3 (Q4)	0/+70	±0.05	60
DAC-100BCQ3 (Q4)	0/+70	±0.1	60
DAC-100CCQ3 (Q4)	0/+70	±0.2	60
DAC-100DDQ3 (Q4)	0/+70	±0.3	120

MULTIPLYING CURRENT OUTPUT – 12 BIT RESOLUTION

DEVICE	OPERATING TEMPERATURE RANGE (°C)	MAXIMUM NONLINEARITY (T_A = 25°C)	MAXIMUM GAIN TEMPERATURE COEFFICIENT
SSS562-SD-BIN	-55/+125	±1/4 LSB	±3ppm/°C
SSS562-AD-BIN	-25/+85	±1/2 LSB	±3ppm/°C
SSS562-KD-BIN	0/+70	±1/2 LSB	±3ppm/°C

MULTIPLYING CURRENT OUTPUT – 3 DIGIT RESOLUTION

DEVICE	OPERATING TEMPERATURE RANGE (°C)	MAXIMUM NONLINEARITY (T_A = 25°C)	MAXIMUM GAIN TEMPERATURE COEFFICIENT
SSS562-SD-BCD	-55/+125	±1/10 LSB	±3ppm/°C
SSS562-AD-BCD	-25/+85	±1/2 LSB	±3ppm/°C
SSS562-KD-BCD	0/+70	±1/2 LSB	±3ppm/°C

MULTIPLYING CURRENT OUTPUT 8-BIT RESOLUTION

DEVICE	TEMP RANGE FOR SPECIFICATION (°C)	MAXIMUM NONLINEARITY (% FS)	DUAL HIGH COMPLIANCE OUTPUTS	UNIVERSAL LOGIC INPUTS
DAC-08AQ	-55/+125	±0.1	YES	YES
DAC-08Q	-55/+125	±0.19	YES	YES
DAC-08HQ	0/+70	±0.1	YES	YES
DAC-08EQ	0/+70	±0.19	YES	YES
DAC-08CQ	0/+70	±0.39	YES	YES
SSS1508A-8Q	-55/+125	±0.19	NO	NO
SSS1408A-8Q	0/+75	±0.19	NO	NO
SSS1408A-7Q	0/+75	±0.39	NO	NO
SSS1408A-6Q	0/+75	±0.78	NO	NO

MULTIPLYING CURRENT OUTPUT – 2 DIGIT RESOLUTION

DEVICE	TEMP RANGE FOR SPECIFICATION (°C)	MAXIMUM NONLINEARITY (% FS)	DUAL HIGH COMPLIANCE OUTPUTS	UNIVERSAL LOGIC INPUTS
DAC-20AQ	–55/+125	±1/4 LSB	YES	YES
DAC-20Q	–55/+125	±1/2 LSB	YES	YES
DAC-20EQ	0/+70	±1/4 LSB	YES	YES
DAC-20CQ	0/+70	±1/2 LSB	YES	YES

VOLTAGE OUTPUT INTERNAL REFERENCE

DEVICE	RESOLUTION (BITS)	MONOTONICITY MIN (BITS)	NONLINEARITY MAX (% FS)	TEMPERATURE RANGE FOR SPECIFICATION (°C)
DAC-05A	10+Sign	10	±0.1	–55/+125
DAC-06A	10	10	±0.1	–55/+125
DAC-05E	10+Sign	10	±0.1	0/+70
DAC-06E	10	10	±0.1	0/+70
DAC-02ACX1	10+Sign	10	±0.1	0/+70
DAC-02ACX2	10+Sign	10	±0.1	0/+70
DAC-04ACX2	10	10	±0.1	0/+70
DAC-03ADX1	10	10	±0.1	25
DAC-03ADX2	10	10	±0.1	25
DAC-05B	10+Sign	9	±0.2	–55/+125
DAC-06B	10	9	±0.2	–55/+125
DAC-05F	10+Sign	9	±0.2	0/+70
DAC-06F	10	9	±0.2	0/+70
DAC-02BCX1	10+Sign	9	±0.1	0/+70
DAC-02BCX2	10+Sign	9	±0.1	0/+70
DAC-04BCX2	10	9	±0.1	0/+70
DAC-03BDX1	10	9	±0.1	25
DAC-03BDX2	10	9	±0.1	25
DAC-05C	10+Sign	8	±0.4	–55/+125
DAC-06C	10	8	±0.4	–55/+125
DAC-05G	10+Sign	8	±0.4	0/+70
DAC-06G	10	8	±0.4	0/+70
DAC-02CCX1	10+Sign	8	±0.2	0/+70
DAC-02CCX2	10+Sign	8	±0.2	0/+70
DAC-04CCX2	10	8	±0.2	0/+70
DAC-03CDX1	10	8	±0.2	25
DAC-03CDX2	10	8	±0.2	25
DAC-01AY	6	6	±0.3	–55/+125
DAC-02DDX1	10+Sign	7	±0.4	0/+70
DAC-02DDX2	10+Sign	7	±0.4	0/+70
DAC-04DDX2	10	7	±0.4	0/+70
DAC-03DDX1	10	7	±0.4	25
DAC-03DDX2	10	7	±0.4	25
DAC-01Y	6	6	±0.45	–55/+125
DAC-01BY	6	6	±0.45	–55/+125
DAC-01FY	6	6	±0.45	–55/+125
DAC-01CY	6	6	±0.45	0/+70
DAC-01HY	6	6	±0.45	0/+70
DAC-01DY	6	6	±0.8	0/+70

DAC-01

6 BIT MONOLITHIC D/A CONVERTER

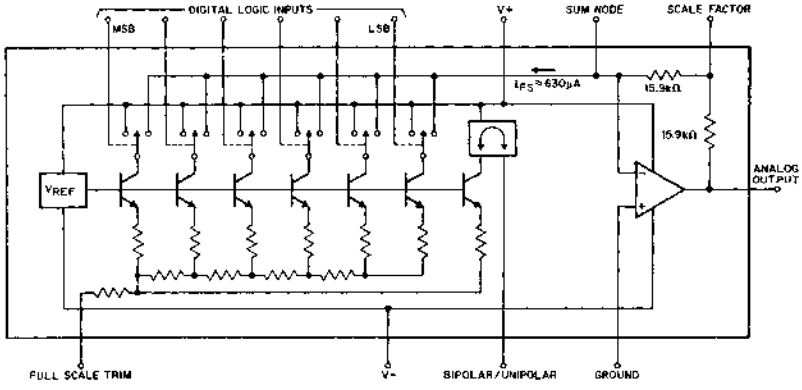
GENERAL DESCRIPTION

The DAC-01 is a complete monolithic 6-bit digital-to-analog converter, incorporating current steering logic, current sources, diffused resistor ladder network, precision voltage reference and fast summing op amp on one chip. Monolithic construction provides small size, light weight, low power consumption and very high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC ever made.

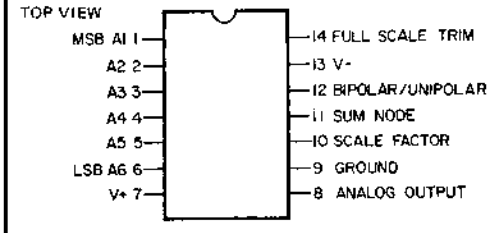
FEATURES

- **Fast** . . . . . 3μsec Settling Time (Max)
- **Complete** . . . . Includes Reference, Ladder, Op Amp
- **Low Power Consumption** . . . . . 250 mW (Max)
- **6-Bit Resolution** . . . . . 7 Bit Accuracy
- **3 Output Options** . . . . . +10V, ±5V, ±10V
- **Standard Power Supplies** . . . . . ±12V to ±18V
- **–55°/+125°C or 0°/70°C Ranges Available**
- **TTL, DTL Compatible Logic Levels**
- **Models With MIL-STD-883A Class B Processing Available From Stock**
- **Low Cost**

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION



14 PIN HERMTIC DIP (Y-Suffix)

ORDER: DAC-01Y DAC-01CY
DAC-01BY DAC-01HY
DAC-01FY DAC-01DY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: DAC01-883-Y
DAC01-883-BY
DAC01-883-FY

ABSOLUTE MAXIMUM RATINGS

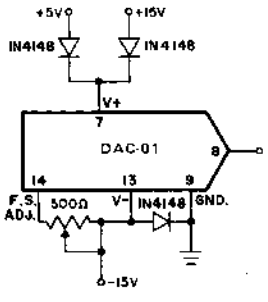
Operating Temperature	
DAC-01, DAC-01B, DAC-01F	−55°C to +125°C
DAC-01C, DAC-01H, DAC-01D	0°C to +70°C
V+ Supply Voltage to Ground	0 to +18V
V− Supply Voltage to Ground	0 to −18V
Logic Input to Ground	−0.7 to +6V
Internal Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C
Lead Soldering Temperature	300°C (60 sec)
Output Short Circuit Duration (Note 2)	Indefinite

NOTE 1: Rating applies up to ambient temperatures of 100°C. For temperatures above 100°C, derate linearly at 10mW/°C.

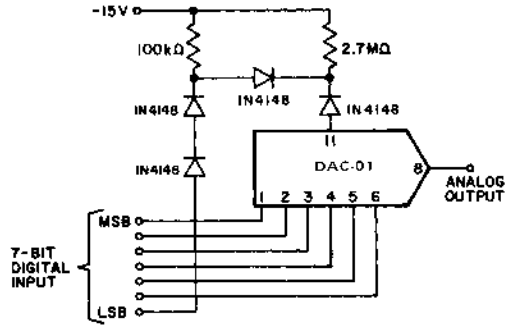
NOTE 2: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

BASIC CIRCUIT CONNECTIONS

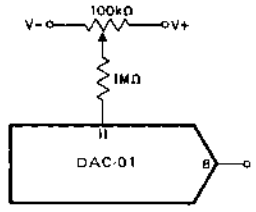
SUPPLY SEQUENCING PROTECTION AND FULL SCALE ADJUSTMENT TECHNIQUE



ADDITION OF 7TH BIT



OPTIONAL ZERO SCALE OR BIPOLAR OFFSET ADJUSTMENT



APPLICATIONS INFORMATION

INPUT CODES—The DAC-01 utilizes standard complementary binary coding for unipolar mode operation (all inputs high produces zero output voltage). Complementary offset binary (bipolar) mode operation may be implemented by shorting pin 11 to pin 12 (all inputs high produces negative full scale output voltage). One's complement coding may be implemented by shorting pin 11 to pin 12 and inverting the MSB before entering pin 1 (all other bits are not inverted). Two's complement coding may be implemented by shorting pin 11 to pin 12, inverting the MSB before entering pin 1, and injecting approximately 5μA into pin 11 (which is at ground potential) by using the "zero scale or bipolar offset adjustment" circuit.

POWER SUPPLIES—Care should be taken to insure that positive voltages are not applied to the logic inputs for more than approximately 300ms before the V+ supply is applied. It is also important that V− not be removed during operation. The addition of three clamping diodes (see fig. above) is recommended where random supply sequences may be encountered. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V−.

FULL SCALE ADJUST—A 500Ω pot from pin 14 to V− can be used to adjust the full scale output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts p-p in bipolar mode. If no pot is used, tie pin 14 to V−.

SCALE FACTOR—For +10 volt or ±5 volt outputs, short pin 10 to pin 11 (adjusts the feedback resistor around the output amplifier). For ±10 volt output, leave pin 10 open. Intermediate output voltages may be obtained by placing a pot between pin 10 and pin 11, but this will seriously degrade the full scale temperature coefficient due to the mismatch between the +1150 ppm/°C tempco of the diffused resistors and the pot tempco.

CAPACITIVE LOADS—When driving capacitive loads greater than 50 pF in Unipolar mode or 30 pF in Bipolar mode a 100 pF capacitor may be placed from pin 11 to ground for added stability.

LOWER RESOLUTION APPLICATIONS—When less than 6 bits of resolution is required, tie off unused bits to a voltage level greater than +2.1 volts. The +5 volt logic supply is usually convenient.

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and over the rated operating temperature range unless otherwise noted.

Parameter	DAC-01	DAC-01B	DAC-01F	DAC-01C	DAC-01H	DAC-01D	Units
Output Options	Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	–55/+125	–55/+125	–55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25°C – Max	±0.40	±0.40	±0.40	±0.40	±0.40	±0.78	%FS
Nonlinearity Over Temperature – Max	±0.45	±0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full Scale Tempco – Max	±80	±120	±80	±160	±160	±160	ppm/°C
Unipolar Zero Scale Output Voltage – Max (Note 1, 2)	25	25	40	25	40	50	mV

These specifications apply for all DAC-01 grades, V_S = ±15V and over the rated operating temperature range unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Unipolar Full Scale Output Voltage (Note 3)	2KΩ load, logic ≤ 0.5V, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.00	–	+11.75	Volts
Bipolar Output Voltage (Note 3)	2KΩ Load, Short pin 11 to pin 12.				
±5 Volt Range	Short pin 13 to pin 14, Short pin 10 to pin 11.				
V_{FS+}	Logic Inputs ≤ 0.5V	+4.93	–	+5.94	Volts
V_{FS-}	Logic Inputs ≥ 2.1V	–5.94	–	–4.93	Volts
±10 Volt Range	Open pin 10				
V_{FS+}	Logic Inputs ≤ 0.5V	+9.86	–	+11.89	Volts
V_{FS-}	Logic Inputs ≥ 2.1V	–11.89	–	–9.86	Volts
Bipolar Offset Voltage (Note 1)	±5 Volt Range	–	±40	±70	mV
±1/2 (I V_{FS+} I–I V_{FS-} I)	±10 Volt Range	–	±80	±140	mV
Resolution		–	–	6	bits
Logic Input "0"		–	–	0.5	Volts
Logic Input "1"		2.1	–	–	Volts
Logic Input Current, Each Input		–	2.2	8	μA
Power Supply Sensitivity	±12V ≤ V_S ≤ ±18V V_{FS} ≅ 10.0 V	–	±0.01	±0.15	%V_{FS}/V
Power Consumption		–	200	250	mW
Settling Time to ±1/2 LSB	2.1V ≤ logic level ≤ 0.5V T_A = 25°C.	–	1.5	3	μsec

NOTES:

1. Zero scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
2. Logic input voltage ≥ 2.1 volts.
3. Full scale is adjustable to precisely 10 volts for unipolar operation and 10 volt or 20 volt p-p bipolar operation with an external 500 ohm potentiometer from pin 14 to V–.

DAC-02

10 BIT PLUS SIGN MONOLITHIC D/A CONVERTER

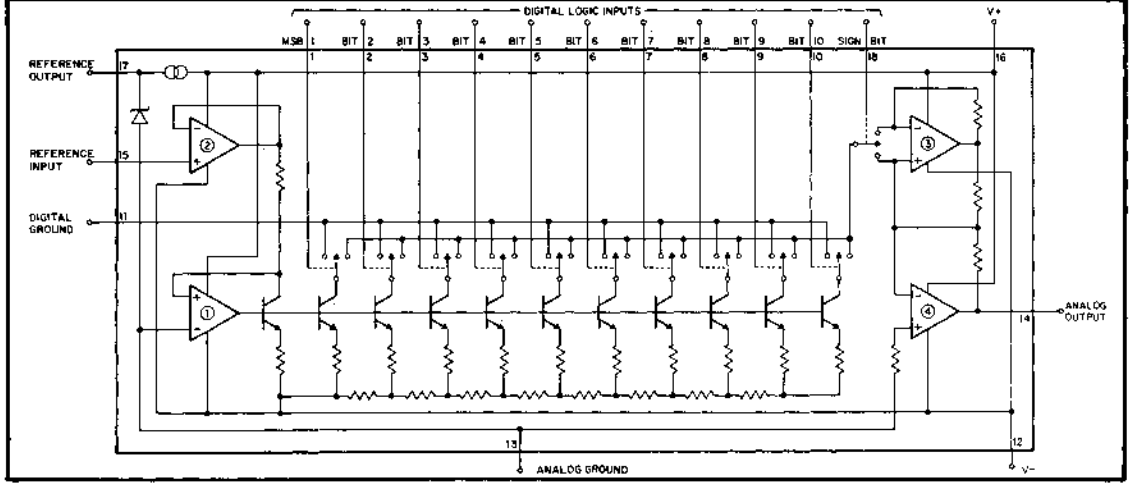
GENERAL DESCRIPTION

The DAC-02 is a complete 10 bit plus sign D/A converter on a single 82 x 148 mil monolithic chip. All elements of a complete sign/magnitude DAC are included—precision voltage reference, current steering logic, current sources, R-2R resistor network, logic controlled polarity switch and high speed internally compensated output op amp. Monotonicity guaranteed over the 0°C to +70°C temperature range is achieved by the untrimmed diffused R-2R resistor ladder network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption, choice of full scale output voltages and sign/magnitude coding assure utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, servo positioning controls, and voice and music digitizing and reconstruction systems.

FEATURES

- **Complete** . . . . . **Includes Reference and Op Amp**
- **Compact** . . . . . **Single 18 Pin DIP Package**
- **Bipolar Output** . . . . . **Sign/Magnitude Coding**
- **Monotonicity Guaranteed**
- **Nonlinearity** . . . . . **±1 LSB**
- **Fast** . . . . . **1.5 μsec Settling Time**
- **Stable** . . . . . **Full Scale Tempco 60 ppm/°C**
- **Low Power Consumption** . . . . . **300 mW Max**
- **TTL, DTL, CMOS Compatible Inputs**
- **Reliable** . . . . . **100% Burned-in 72 Hrs @ +125°C**

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	MONOTONICITY	FS TEMPCO	TEMP RANGE	PACKAGE
DAC-02 ACX1 (or X2)*	10 BITS	60 ppm/°C MAX	0°/+70°C	HERMETIC 18 PIN DIP
DAC-02 BCX1 (or X2)*	9 BITS	60 ppm/°C MAX	0°/+70°C	HERMETIC 18 PIN DIP
DAC-02 CCX1 (or X2)*	8 BITS	60 ppm/°C MAX	0°/+70°C	HERMETIC 18 PIN DIP
DAC-02 DDX1 (or X2)*	7 BITS	150 ppm/°C MAX	0°/+70°C	HERMETIC 18 PIN DIP

*Suffix X1 indicates ±10V out; suffix X2 indicates ±5V out.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C	Internal Reference Output Current	300μA
Storage Temperature Range	−65°C to +150°C	Reference Input Voltage	0 to +10V
V+ Supply to Analog Ground	0 to +18V	Internal Power Dissipation	500 mW
V− Supply to Analog Ground	0 to −18V	Lead Soldering Temperature	300°C (60 sec)
Analog Ground to Digital Ground	0 to ±0.5V	Output Short Circuit Duration	Indefinite
Logic Inputs to Digital Ground	−5V to (V_+ − .7V)	(Short circuit may be to ground or either supply.	

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and over the 0°C to +70°C temperature range, unless otherwise specified.

		GRADES AC, BC, CC			GRADE DD			
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution	Bipolar Output	11	11	11	11	11	11	bits
	Unipolar Output	10	10	10	10	10	10	bits
Monotonicity	0°C to 70°C							
(See Note 1)	Grade AC	10	–	–				bits
	Grade BC	9	–	–				bits
	Grade CC	8	–	–				bits
	Grade DD				7	–	–	bits
	0°C to 70°C							
Nonlinearity	Grade AC	–	–	±0.1				%
(See Note 1)	Grade BC	–	–	±0.1				%
	Grade CC	–	–	±0.2				%
	Grade DD				–	–	±0.4	%
Settling Time	To ±1/2 LSB, 10 Volt Step	–	1.5	–	–	1.5	–	μsec
Full Scale Tempco	Total, Internal Reference Connected	–	–	±60	–	–	±150	ppm/°C
Full Scale Tempco	External Reference	–	±30	–	–	±30	–	ppm/°C
Reference Input Bias Current		–	100	–	–	100	–	nA
Reference Input Impedance		–	200	–	–	200	–	MΩ
Reference Input Slew Rate		–	1.5	–	–	1.5	–	V/μsec
Reference Output Voltage		–	6.7	–	–	6.7	–	V
Zero Scale Offset	Sign Bit High, All Other Logic Inputs Low	–	±5	±10	–	±5	±10	mV
Zero Scale Symmetry	X2 Models (±5V Full Scale)	–	±1	±2.5	–	±1	±5	mV
	X1 Models (±10V Full Scale)	–	±1	±5	–	±1	±10	mV
Full Scale Bipolar Symmetry	(See Definitions) (See Note 2)	–	±30	±60	–	±30	±80	mV
Power Supply Sensitivity	V_S = ±12V to ±18V	–	±0.015	±0.05	–	±0.015	±0.1	% V_{FS}/V
Power Dissipation	I_{OUT} = 0	–	225	300	–	225	350	mW
Logic Input Current	Each Input, −5V to (V_+ − .7V)	–	1	–	–	1	–	μA
Logic Input "0"		–	–	0.8	–	–	0.8	V
Logic Input "1"		2.0	–	–	2.0	–	–	V
Full Scale Output Voltage	(See Note 3)							
±10 Volt Models	V_{FS+} (Sign Bit High)	+10.0	–	+11.5	+10.0	–	+11.5	V
	V_{FS-} (Sign Bit Low)	−11.5	–	−10.0	−11.5	–	−10.0	V
±5 Volt Models	V_{FS+} (Sign Bit High)	+5.00	–	+5.75	+5.00	–	+5.75	V
	V_{FS-} (Sign Bit Low)	−5.75	–	−5.00	−5.75	–	−5.00	V

NOTE 1: This parameter is 100% tested at 0°C, +25°C and +70°C.

NOTE 2: These specifications apply for X1 (±10V) models; for X2 (±5V) models, divide specifications shown by 2.

NOTE 3: Reference Output terminal connected directly to Reference Input terminal, R_L = 2KΩ, all logic inputs ≥ 2.0 V.

DEFINITION OF SPECIFICATIONS*

BIPOLAR FULL SCALE SYMMETRY
The magnitude of the difference between $|V_{FS+}|$ and $|V_{FS-}|$

LOGIC "0"
The (low) logic input voltage necessary to hold a bit OFF.

LOGIC "1"
The (high) logic input voltage necessary to hold a bit ON.

SIGN/MAGNITUDE CODING
The input logic coding used by the DAC-02. The polarity of the output voltage is determined by the logic level of the Sign Bit; the magnitude of the output voltage is determined by the binarily-weighted logic inputs.

ZERO SCALE OFFSET
The output voltage (V_{ZS+}) produced by a positive zero scale input code (1-0000000000)

ZERO SCALE SYMMETRY
The change in the output voltage produced by switching the Sign Bit with all logic bits low ($V_{ZS+}-V_{ZS-}$)

OPERATING INSTRUCTIONS

FULL SCALE ADJUSTMENT—Full Scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor if used or if pot and resistor tempcos match. Alternatively, a single pot of ⩾ 75KΩ may be used.

REFERENCE OUTPUT—For best results, Reference Output current should not exceed 100μA.

USE WITH EXTERNAL REFERENCES—Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-02's to the Reference Output of any one of them.

REFERENCE INPUT BYPASS—Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor.

VARIABLE REFERENCES—Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the Reference Input terminal. The DAC output is then the scaled product of this voltage and the digital input. ±5V output models (X2) must be used if Reference Input voltages will exceed +6.7V in order to prevent saturation of the output amplifier.

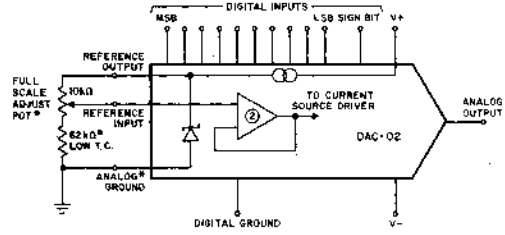
LOWER RESOLUTION APPLICATIONS—For applications not requiring full 10 bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION—Operation as a 10 bit straight binary converter may be implemented by permanently tying the Sign Bit to +5V (for positive Full Scale output) or to ground (for negative Full Scale output).

POWER SUPPLIES—The DAC-02 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V–.

CAPACITIVE LOADING—The output operational amplifier provides stable operation with capacitive loads up to 100pF.

FULL SCALE ADJUSTMENT CIRCUIT



POSITIVE SIGN/MAGNITUDE CODING TABLE

	SIGN BIT	MSB								LSB
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1
+ "HALF" SCALE	1	1	0	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0	0
ZERO SCALE (–)	0	0	0	0	0	0	0	0	0	0
– "HALF" SCALE	0	1	0	0	0	0	0	0	0	0
–FULL SCALE	0	1	1	1	1	1	1	1	1	1

GROUNDING—for optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-02 package, so that the large digital currents do not flow through the analog ground path.

*SEE SECTION 13 FOR COMPLETE D/A CONVERTER DEFINITIONS

DAC-03

8 & 10 BIT LOW COST MONOLITHIC D/A CONVERTER

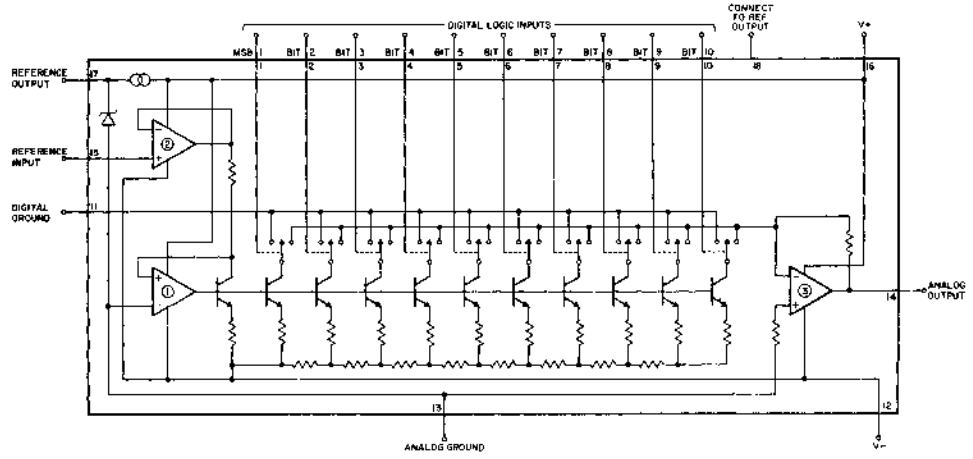
GENERAL DESCRIPTION

The DAC-03 is a complete 10 bit low cost D/A converter on a single 82 x 148 mil monolithic chip. All elements of a complete DAC are included--precision voltage reference, current steering logic, current sources, R-2R resistor network and high speed internally compensated output op amp. The untrimmed diffused R-2R resistor ladder network achieves monotonic operation over a wide temperature range. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption and choice of full scale output voltages assure utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, and servo positioning controls. For bipolar DAC's refer to the DAC-02 and DAC-04 data sheets.

FEATURES

- Monotonicity Guaranteed
- Low Cost
- Complete . . . . . Includes Reference and Op Amp
- Compact . . . . . Single 18 Pin DIP Package
- Fast . . . . . 1.5 μsec Settling Time
- Stable . . . . . Full Scale Tempco 60 ppm/°C
- Standard Power Supplies . . . . . ±12V to ±18V
- Low Power Consumption . . . . . 350 mW Max
- TTL, DTL, CMOS Compatible Inputs
- 5V and 10V Models Available

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	MONOTONICITY	TEMP RANGE	FS TEMPCO	PACKAGE
DAC-03 ADX1 (or X2)*	10 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP
DAC-03 BDX1 (or X2)*	9 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP
DAC-03 CDX1 (or X2)*	8 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP
DAC-03 DDX1 (or X2)*	7 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP

*Suffix X1 indicates +10V output; suffix X2 indicates +5V output.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0° to +70°C	Internal Reference Output Current	300μA
Storage Temperature Range	−65°C to +150°C	Reference Input Voltage	0 to +10V
V+ Supply to Analog Ground	0 to +18V	Internal Power Dissipation	500 mW
V− Supply to Analog Ground	0 to −18V	Lead Soldering Temperature	300°C (60 sec)
Analog Ground to Digital Ground	0 to ±0.5V	Output Short Circuit Duration	Indefinite
Logic Inputs to Digital Ground	−5V to (V_+ − .7V)	(Short circuit may be to ground or either supply.)	

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and T_A = 25°C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Units
Resolution		10	10	10	bits
Monotonicity	Grade AD	10	–	–	bits
	Grade BD	9	–	–	bits
	Grade CD	8	–	–	bits
	Grade DD	7	–	–	bits
Nonlinearity	Grade AD	–	–	±0.1	%
	Grade BD	–	–	±0.1	%
	Grade CD	–	–	±0.2	%
	Grade DD	–	–	±0.4	%
Settling Time	To ±1/2 LSB, 10 Volt Step	–	1.5	–	μsec
Full Scale Tempco	Total, Internal Reference Connected	–	60	–	ppm/°C
Full Scale Tempco	External Reference	–	±40	–	ppm/°C
Reference Input Bias Current		–	100	–	nA
Reference Input Impedance		–	200	–	MΩ
Reference Input Slew Rate		–	1.5	–	V/μsec
Reference Output Voltage		–	6.7	–	V
Zero Scale Offset		–	±1.0	±10	mV
Power Supply Sensitivity	V_S = ±12V to ±18V	–	±.015	±0.1	% V_{FS}/V
Power Dissipation	I_{OUT} = 0	–	225	350	mW
Logic Input Current	(Each Input, −5V to (V_+ − .7V)	–	1	–	μA
Logic Input "0"		–	–	0.8	V
Logic Input "1"		2.0	–	–	V
Full Scale Output Voltage					
10 Volt Models (X1)	(See Note)	+10.0	–	+11.5	V
5 Volt Models (X2)		+5.00	–	+5.75	V

NOTE: Reference Output terminal connected directly to Reference Input terminal and pin 18, R_L = 2KΩ, all logic inputs ≥ 2.0 V.

DEFINITION OF SPECIFICATIONS

SEE SECTION 13 FOR COMPLETE D/A CONVERTER DEFINITIONS

LOGIC "0"
The (low) logic input voltage necessary to hold a bit OFF.

LOGIC "1"
The (high) logic input voltage necessary to hold a bit ON.

ZERO SCALE OFFSET
The output voltage (V_{ZS}) produced by a zero scale input code (0000000000)

APPLICATION NOTES

FULL SCALE ADJUSTMENT—Full Scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≥ 75KΩ may be used.

REFERENCE OUTPUT—For best results, Reference Output current should not exceed 100μA.

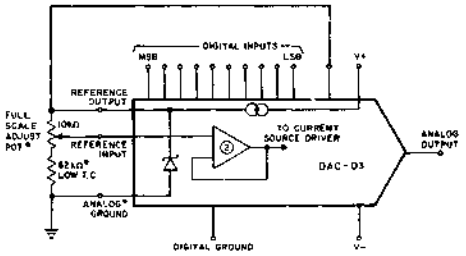
USE WITH EXTERNAL REFERENCES—Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-03's to the Reference Output of any one of them.

REFERENCE INPUT BYPASS—Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor.

LOWER RESOLUTION APPLICATIONS—For applications not requiring full 10 bit resolution, unused logic inputs should be tied to ground.

POWER SUPPLIES—The DAC-03 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V−.

FULL-SCALE ADJUSTMENT CIRCUIT



GROUNDING—for optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-03 package, so that large digital currents do not flow through the analog ground path.

CAPACITIVE LOADING—the output operational amplifier provides stable operation with capacitive loads up to 100pF.

INTERFACING WITH CMOS LOGIC

The DAC-03's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less .7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_{DD} to V+ less .7 volt—since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-03 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

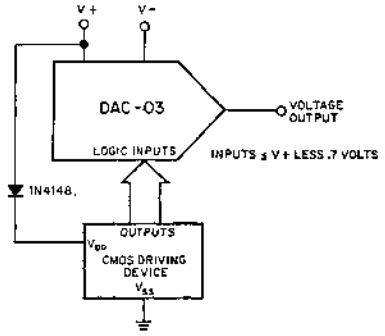


FIGURE 1

DAC-04

TWO'S COMPLEMENT 10 BIT D/A CONVERTER

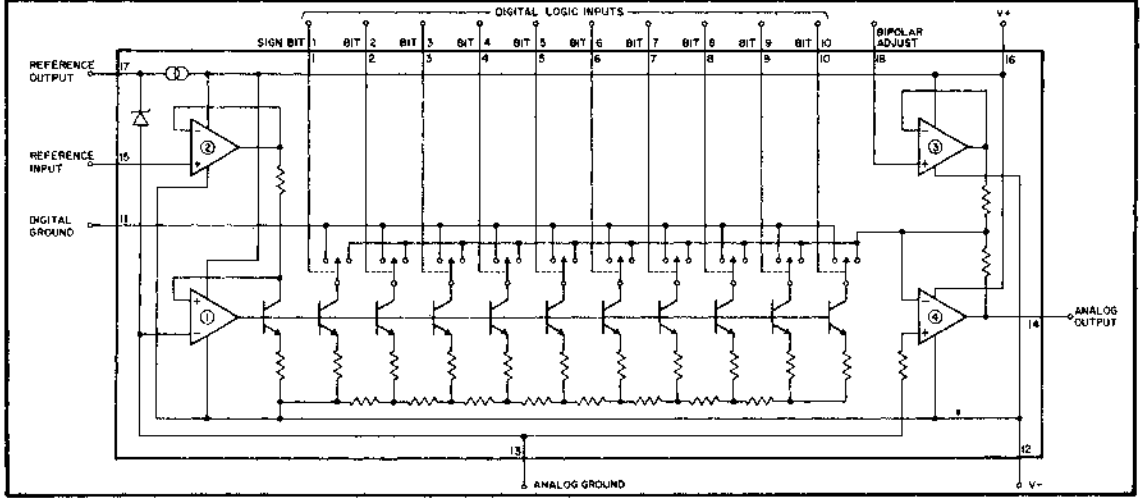
GENERAL DESCRIPTION

The DAC-04 is a complete 10 bit Two's Complement D/A Converter on a single 82 x 148 mil monolithic chip. All elements of a complete bipolar output Two's Complement DAC are included—precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire 0° to+70°Ctemperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The user may also easily implement One's Complement, Straight Offset Binary, or unipolar operation. The ±12V to ±18V power supply range, low power consumption TTL and CMOS compatibility, choice of full scale output voltages and adaptable logic coding capability assure utility in a wide range of applications.

FEATURES

- **Complete** . . . . . **Includes Reference and Op Amp**
- **Compact** . . . . . **Single 18 Pin DIP Package**
- **Bipolar Output** . . . . . **Two's Complement Coding**
- **Monotonicity Guaranteed**
- **Nonlinearity** . . . . . **±1 LSB**
- **Fast** . . . . . **1.5 μsec Settling Time**
- **Standard Power Supplies** . . . . . **±12V to ±18V**
- **Low Power Consumption** . . . . . **300 mW Max**
- **TTL, CMOS Compatible Inputs**
- **Reliable** . . . . . **100% Burned-in 72 Hrs @ +125°C**

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	OUTPUT	MONOTONICITY	FS TEMPCO	TEMP RANGE	PACKAGE
DAC-04ACX2	±5V	10 BITS	90 ppm/°C MAX	0°/+70°C	18 PIN HERMETIC DIP
DAC-04BCX2	±5V	9 BITS	90 ppm/°C MAX	0°/+70°C	18 PIN HERMETIC DIP
DAC-04CCX2	±5V	8 BITS	90 ppm/°C MAX	0°/+70°C	18 PIN HERMETIC DIP
DAC-04DDX2	±5V	7 BITS	150 ppm/°C MAX	0°/+70°C	18 PIN HERMETIC DIP

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0° to +70°C	Internal Reference Output Current	300 μA
Storage Temperature Range	−65°C to +150°C	Reference Input Voltage	0 to +10V
V+ Supply to Analog Ground	0 to +18V	Internal Power Dissipation	500 mW
V− Supply to Analog Ground	0 to −18V	Lead Soldering Temperature	300°C (60 sec)
Analog Ground to Digital Ground	0 to ±0.5V	Output Short Circuit Duration	Indefinite
Logic Inputs to Digital Ground	−5V to (V+ − .7V)	(Short circuit may be to ground or either supply.)	

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and over the 0°C to +70°C temperature range, unless otherwise specified.

		GRADES AC, BC, CC			GRADE DD			
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		10	10	10	10	10	10	bits
Monotonicity	0°C to +70°C							
(See Note 1)	Grade AC	10	–	–				bits
	Grade BC	9	–	–				bits
	Grade CC	8	–	–				bits
	Grade DD				7	–	–	bits
	0°C to +70°C							
Nonlinearity	Grade AC	–	–	±0.1				%
(See Note 1)	Grade BC	–	–	±0.1				%
	Grade CC	–	–	±0.2				%
	Grade DD				–	–	±0.4	%
Settling Time	To ±1/2 LSB, 10 Volt Step	–	1.5	–	–	2.5	–	μsec
Full Scale Tempco	Total, Internal Reference Connected	–	45	90	–	60	150	ppm/°C
Full Scale Tempco	Zero Drift External Reference Applied	–	30	–	–	50	–	ppm/°C
Reference Input Bias Current		–	100	–	–	100	–	nA
Reference Input Impedance		–	200	–	–	200	–	MΩ
Reference Input Slew Rate		–	1.5	–	–	1.5	–	V/μsec
Reference Output Voltage		–	6.7	–	–	6.7	–	V
Unipolar Zero Scale Output Voltage	Short Pin 18 to ground (See Note 2)	–	±5.0	–	–	±5.0	–	mV
Bipolar Offset Voltage	Short Pins 15 and 18 to Pin 17 (See Note 3)	−5.0	-	−0.1	−5.0	–	−0.1	% Range
Power Supply Sensitivity	V_S = ±12V to ±18V	–	±0.015	±0.1	-	±0.15	–	%/V
Power Dissipation	I_{OUT} = 0	–	225	300	–	300	350	mW
Logic Input Current	Each Input, −5V to (V+ − .7V)	–	1.0	–	–	1.0	–	μA
Logic Input "0"		–	–	0.8	–	–	0.8	V
Logic Input "1"		2.0	–	–	2.0	–	–	V
Full Scale Output Range	Short Pin 15 to Pin 17 (See Note 4)	10	–	11.5	10	–	11.5	V

NOTE 1: This parameter is 100% tested at 0°C, +25°C and +70°C

NOTE 2: May be operated in 0 to +10V Unipolar mode by shorting Pin 18 to ground.

NOTE 3: Bipolar Offset Voltage is trimmable to exact Two's or One's Complement condition with the circuit shown on the next page.

NOTE 4: Full Scale Output Voltage is trimmable to exact desired output range of 10V with the circuit shown on the next page.

DEFINITION OF SPECIFICATIONS

SEE SECTION 13 FOR COMPLETE D/A CONVERTER DEFINITIONS

BIPOLAR OFFSET VOLTAGE 1/2(|V_{FS+}|−|V_{FS-}|)
The maximum error due to asymmetry around zero output expressed as a percentage of Full Scale Output Range.

FULL SCALE OUTPUT RANGE
The peak-to-peak voltage swing of the converter's output, i.e. |V_{FS+}|+|V_{FS-}| for bipolar operation, and (V_{FS-}−V_{ZS}) for unipolar operation.

NEGATIVE BIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS-})
The output voltage for 1000000001 input code for Two's Complement coding, or the output voltage for 1000000000 input code for One's Complement coding.

POSITIVE BIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS+})
The output for 0111111111 input code.

UNIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS})
The (positive) output voltage for 0111111111 input code.

UNIPOLAR ZERO SCALE OUTPUT VOLTAGE (V_{ZS})
The output voltage for 1000000000 input code.

OPERATING INSTRUCTIONS

ADJUSTING FOR TWO'S COMPLEMENT CODING

1. Connect Full Scale Adjust and Bipolar Adjust Circuitry as shown in figure.
2. Turn all bits off (V_{FS-}−LSB) − 1 0 0 0 0 0 0 0 0 0
3. Adjust Bipolar Pot for V_{FS-} −LSB at output . . . . −5.0098V
4. Turn all bits on (V_{FS+}) − 0 1 1 1 1 1 1 1 1 1
5. Adjust Full Scale Pot for desired V_{FS+} value . . . . +5.0000V
6. Check Zero Scale Reading (V_{ZS}) − 0 0 0 0 0 0 0 0 0 0
   If this reading is outside desired V_{ZS} range, readjust Bipolar Pot till the output reads 0.0000 V.

TWO'S COMPLEMENT CODING TABLE

	INPUT MSB								LSB	IDEAL OUTPUT
V_{FS+}	0	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} − LSB	0	1	1	1	1	1	1	1	0	+4.990V
+1 LSB	0	0	0	0	0	0	0	0	1	+0.010V
Zero	0	0	0	0	0	0	0	0	0	0.000V
−1 LSB	1	1	1	1	1	1	1	1	1	−0.010V
V_{FS-} + LSB	1	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	1	0	0	0	0	0	0	0	1	−5.000V

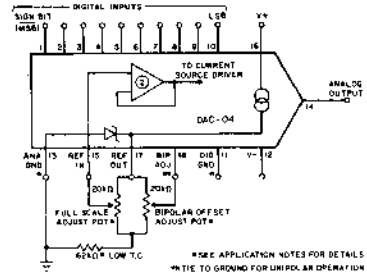
ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Connect Full Scale Adjust and Bipolar Adjust Circuitry as shown in above figure.
2. Turn all bits off (V_{FS-}) − 1 0 0 0 0 0 0 0 0 0
3. Adjust Bipolar Pot for V_{FS-} at output . . . . . −5.0000V
4. Turn all bits on (V_{FS+}) − 0 1 1 1 1 1 1 1 1 1
5. Adjust Full Scale Pot for desired V_{FS+} value . . . . . +5.0000V

ONE'S COMPLEMENT CODING TABLE

	INPUT MSB								LSB	IDEAL OUTPUT
V_{FS+}	0	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} − LSB	0	1	1	1	1	1	1	1	0	+4.990V
+0	0	0	0	0	0	0	0	0	0	+0.005V
−0	1	1	1	1	1	1	1	1	1	−0.005V
V_{FS-} + LSB	1	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	−5.000V

FULL SCALE OUTPUT RANGE AND BIPOLAR OFFSET ADJUSTMENT CIRCUIT



NOTE that two zero states will straddle (±1/2 LSB) the true zero. Therefore the DAC will have symmetrical outputs for both positive and negative full scale.

EXTERNAL ADJUSTMENT NETWORK—Full Scale Output Range and Bipolar Offset may be adjusted by using the circuit shown in the figure above. Best results will be obtained when low tempco pots and resistors are used, or if pot and resistor tempcos match.

IMPLEMENTING STRAIGHT OFFSET BINARY CODING—Straight Offset Binary coding is exactly the same as One's Complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-04 to Straight Offset Binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, and 4 of the One's Complement adjustment procedure shown above.

STRAIGHT OFFSET BINARY CODING TABLE

	INPUT MSB								LSB	IDEAL OUTPUT
V_{FS+}	1	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} − 1 LSB	1	1	1	1	1	1	1	1	0	+4.990V
+1/2 LSB	1	0	0	0	0	0	0	0	0	+0.005V
Zero										
−1/2 LSB	0	1	1	1	1	1	1	1	1	−0.005V
V_{FS-} +1 LSB	0	0	0	0	0	0	0	0	1	−4.990V
V_{FS-}	0	0	0	0	0	0	0	0	0	−5.000V

REFERENCE OUTPUT—For best results, Reference Output current should not exceed 100μA.

OPERATING INSTRUCTIONS - CONT'D

USE WITH EXTERNAL REFERENCES—Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-04's to the Reference Output of any one of them.

POWER SUPPLIES—The DAC-04 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor. Chip users should connect the substrate to V−.

GROUNDING—for optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-04 package, so that large digital currents do not flow through the analog ground path.

CAPACITIVE LOADING—the output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE INPUT BYPASS—Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor.

VARIABLE REFERENCES—Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the Reference Input terminal. The DAC output is then the scaled product of this voltage and the digital input. A reference input of 6.27V will produce approximately nominal output range.

LOWER RESOLUTION APPLICATIONS—For applications not requiring full 10 bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION—Operation as a 10V positive output 10 bit converter may be implemented by permanently tying pin 18 to ground.

DAC-05

11 BIT DIGITAL TO ANALOG CONVERTER
(10 BITS PLUS SIGN)

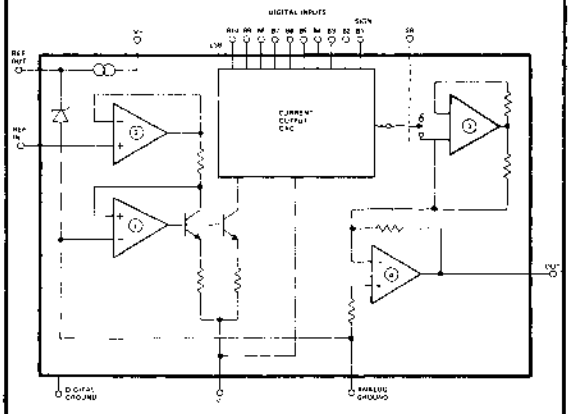
GENERAL DESCRIPTION

The DAC-05 is a complete, monolithic, Sign Plus 10 Bit DAC with a voltage output. A precision voltage reference, a logic-controlled polarity switch, and a high speed (1.5 μsec settling time) output op amp are included. Monotonicity, non-linearity, power consumption, and full scale temperature coefficient are guaranteed over the full operating temperature range. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. Six low cost 0°/70°C and six -55°/+125°C models are available plus six models with MIL-STD-883A Class B processing.

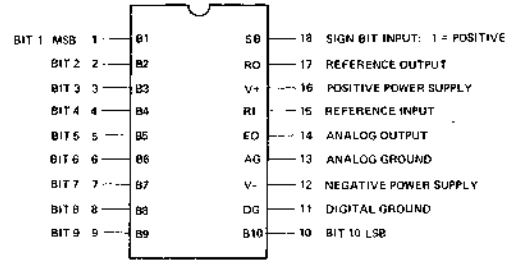
FEATURES

- Complete . . . . . Includes Reference and Op Amp
- Bipolar Output . . . . . Sign/Magnitude Coding
- Fast . . . . . 1.5 μsec Settling Time
- Monotonicity and Nonlinearity Guaranteed
- Reliable . . . . . 100% Burned-in 72 Hrs @+125°C
- Low Power Consumption . . . . . 350 mW Max
- Compact . . . . . Single 18 Pin Hermetic DIP Package
- Choice of Output Ranges . . . . . ±5V or ±10V
- Models with MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



TOP VIEW
18 PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

ORDERING INFORMATION

MODEL	MONOTONICITY	TEMP RANGE
DAC-05AX1 (or 2)	10 BITS	-55°/+125°C
DAC-05BX1 (or 2)	9 BITS	-55°/+125°C
DAC-05CX1 (or 2)	8 BITS	-55°/+125°C
DAC-05EX1 (or 2)	10 BITS	0°/+70°C
DAC-05FX1 (or 2)	9 BITS	0°/+70°C
DAC-05GX1 (or 2)	8 BITS	0°/+70°C

NOTE: Use suffix X1 for ±10V output or suffix X2 for ±5V output.

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

MODEL	MONOTONICITY
DAC 05-883-AX1 (or 2)	10 BITS
DAC 05-883-BX1 (or 2)	9 BITS
DAC 05-883-CX1 (or 2)	8 BITS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
DAC-05A,B,C	-55°C to +125°C
DAC-05E,F,G	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
V-Supply to Analog Ground	0 to -18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	-5V to (V_+ – .7V)
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Internal Power Dissipation	500 mW
Lead Soldering Temperature	300°C (60 sec)
Output Short Circuit Duration	Indefinite

(Short circuit may be to ground or either supply.

ELECTRICAL CHARACTERISTICS – MILITARY GRADES

These specifications apply for V_S = ±15V and T_A = -55°C to +125°C unless otherwise specified.

			DAC-05A			DAC-05B			DAC-05C			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Resolution		Including Sign	11	11	11	11	11	11	11	11	11	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	T_A = 0°C to +70°C	–	–	±0.1	–	–	±0.2	–	–	±0.4	%FS
		T_A = -55°C to +125°C	–	–	±0.2	–	–	±0.3	–	–	±0.5	%FS
Full Scale Tempco	TCV_{FS}	Internal Reference Connected	–	30	60	–	45	90	–	60	120	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Voltage (X1 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+10.0	–	+11.5	+10.0	–	+11.5	+10.0	–	+11.5	V
	V_{FS-}	Sign Bit Low (Note 1)	-11.5	–	-10.0	-11.5	–	-10.0	-11.5	–	-10.0	V
Full Scale Output Voltage (X2 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+5.00	–	+5.75	+5.00	–	+5.75	+5.00	–	+5.75	V
	V_{FS-}	Sign Bit Low (Note 1)	-5.75	–	-5.00	-5.75	–	-5.00	-5.75	–	-5.00	V
Zero Scale Offset (Sign Bit High, All Others Low)	V_{FS+}	T_A = +25°C	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		T_A = -55°C to +125°C	–	2.0	10	–	2.0	10	–	2.0	10	mV
Zero Scale Symmetry (X1 Suffix)		(Note 2)	–	±4.0	±10	–	±4.0	±10	–	±4.0	±10	mV
Zero Scale Symmetry (X2 Suffix)		(Note 2)	–	±2.0	±5.0	–	±2.0	±5.0	–	±2.0	±5.0	mV
Full Scale Bipolar Symmetry (X1 Suffix)		T_A = +25°C (Note 3)	–	±10	±50	–	±10	±50	–	±10	±50	mV
		T_A = -55°C to +125°C	–	±20	±70	–	±20	±70	–	±20	±70	mV
Full Scale Bipolar Symmetry (X2 Suffix)		T_A = +25°C (Note 3)	–	±5.0	±25	–	±5.0	±25	–	±5.0	±25	mV
		T_A = -55°C to +125°C	–	±10	±35	–	±10	±35	–	±10	±35	mV
Settling Time	t_s	To ± ½ LSB, 10V Change	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	±10	–	±1.0	±10	–	±1.0	±10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		T_A = +25°C	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	$\%V_{FS}/V$
		T_A = -55°C to +125°C	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	$\%V_{FS}/V$
Power Dissipation (I_{OUT} = 0)		T_A = +25°C	–	200	300	–	200	300	–	200	300	mW
		T_A = -55°C to +125°C	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference Output terminal connected directly to Reference Input terminal, R_L = 2KΩ, all logic inputs ≥ 2.0 V.

NOTE 2: Zero Scale Symmetry is the change in the output voltage produced by switching the Sign Bit with all logic bits low ($V_{ZS+} - V_{ZS-}$).

NOTE 3: Full Scale Bipolar Symmetry is the magnitude of the difference between $|V_{FS+}|$ and $|V_{FS-}|$.

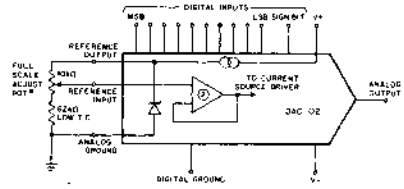
CONNECTION INFORMATION

FULL SCALE ADJUSTMENT – Full Scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≥ 75KΩ may be used.

REFERENCE INPUT BYPASS – Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor.

GROUNDING – For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-05 package, so that the large digital currents do not flow through the analog ground path.

FULL SCALE ADJUSTMENT CIRCUIT



ELECTRICAL CHARACTERISTICS— COMMERCIAL GRADES

These specifications apply for $V_S = \pm 15V$ and $T_A = 0°C$ to $+70°C$ unless otherwise specified.

			DAC-05E			DAC-05F			DAC-05G			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Resolution		Including Sign	11	11	11	11	11	11	11	11	11	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	$T_A = +25°C$	–	–	±0.1	–	–	±0.2	–	–	±0.4	%FS
		$T_A = 0°C$ to $70°C$	–	–	±0.2	–	–	±0.3	–	–	±0.5	%FS
Full Scale Tempco (Note 4)	TCV_{FS}	Internal Reference Connected	–	45	100	–	45	100	–	45	100	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Voltage (X1 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+10.0	–	+11.5	+10.0	–	+11.5	+10.0	–	+11.5	V
	V_{FS-}	Sign Bit Low (Note 1)	-11.5	–	-10.0	-11.5	–	-10.0	-11.5	–	-10.0	V
Full Scale Output Voltage (X2 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+5.00	–	+5.75	+5.00	–	+5.75	+5.00	–	+5.75	V
	V_{FS-}	Sign Bit Low (Note 1)	-5.75	–	-5.00	-5.75	–	-5.00	-5.75	–	-5.00	V
Zero Scale Offset (Sign Bit High, All Others Low)	V_{ZS+}	$T_A = 25°C$	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		$T_A = 0°C$ to $+70°C$	–	2.0	10	–	2.0	10	–	2.0	10	mV
Zero Scale Symmetry (X1 Suffix)		(Note 2)	–	±4.0	±10	–	±4.0	±10	–	±4.0	±10	mV
Zero Scale Symmetry (X2 Suffix)		(Note 2)	–	±2.0	±5.0	–	±2.0	±5.0	–	±2.0	±5.0	mV
Full Scale Bipolar Symmetry (X1 Suffix)		$T_A = +25°C$ (Note 3)	–	±10	±50	–	±10	±50	–	±10	±50	mV
		$T_A = 0°C$ to $+70°C$	–	±20	±70	–	±20	±70	–	±20	±70	mV
Full Scale Bipolar Symmetry (X2 Suffix)		$T_A = +25°C$ (Note 3)	–	±5.0	±25	–	±5.0	±25	–	±5.0	±25	mV
		$T_A = 0°C$ to $+70°C$	–	±10	±35	–	±10	±35	–	±10	±35	mV
Settling Time		To ± ½ LSB, 10V Change	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	±10	–	±1.0	±10	–	±1.0	±10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity ($V_S = \pm 12V$ to $\pm 18V$)		$T_A = +25°C$	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	$\%V_{FS}/V$
		$T_A = 0°C$ to $+70°C$	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	$\%V_{FS}/V$
Power Dissipation ($I_{OUT} = 0$)		$T_A = +25°C$	–	200	300	–	200	300	–	200	300	mW
		$T_A = 0°C$ to $+70°C$	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference Output terminal connected directly to Reference Input terminal, $R_L = 2K\Omega$, all logic inputs ≥ 2.0 V.

NOTE 2: Zero Scale Symmetry is the change in the output voltage produced by switching the Sign Bit with all logic bits low ($V_{ZS+} - V_{ZS-}$).

NOTE 3: Full Scale Bipolar Symmetry is the magnitude of the difference between $|V_{FS+}|$ and $|V_{FS-}|$.

NOTE 4: Parameter is not 100% tested; 90% of units meet this specification.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS - For applications not requiring full 10 bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION – Operation as a 10 bit straight binary converter may be implemented by permanently tying the Sign Bit to +5V (For positive Full Scale output) or to ground (for negative Full Scale output).

POWER SUPPLIES - The DAC-05 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1μF disk capacitor.

CAPACITIVE LOADING - The output operational amplifier provides stable operation with capacitive loads up to 500pF.

REFERENCE OUTPUT - For best results, Reference Output current should not exceed 100μA.

USE WITH EXTERNAL REFERENCES – Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-05's to the Reference Output of any one of them.

SIGN PLUS MAGNITUDE CODING TABLE

	SIGN BIT	MSB									LSB
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1	1
+ "HALF" SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO SCALE (–)	0	0	0	0	0	0	0	0	0	0	0
– "HALF" SCALE	0	1	0	0	0	0	0	0	0	0	0
–FULL SCALE	0	1	1	1	1	1	1	1	1	1	1

DAC-06

TWO'S COMPLEMENT 10 BIT D/A CONVERTER

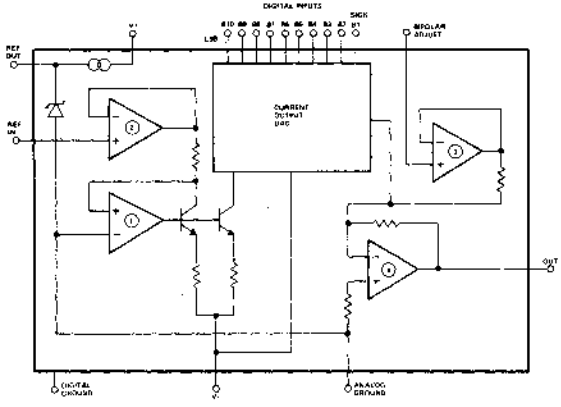
GENERAL DESCRIPTION

The DAC-06 is a complete, monolithic, Two's Complement 10 Bit DAC with a voltage output. A precision voltage reference, R-2R resistor network, bipolar offset circuit, and a high speed (1.5 μsec settling time) output op amp are included. Monotonicity, nonlinearity, power consumption, and full scale temperature coefficient are guaranteed over the full operating temperature range. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. Three low cost 0°/70°C and three -55°/+125°C models are available plus three models with MIL-STD-883A Class B processing.

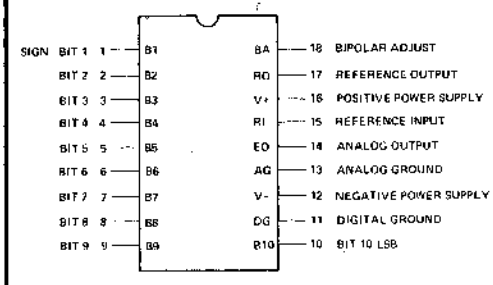
FEATURES

- **Complete** . . . . . **Includes Reference and Op Amp**
- **Bipolar Output** . . . . . **Two's Complement Coding**
- **Fast** . . . . . **1.5 μsec Settling Time**
- **Monotonicity and Nonlinearity Guaranteed**
- **Reliable** . . . . . **100% Burned-in 72 Hrs @ +125°C**
- **Low Power Consumption** . . . . . **350 mW Max**
- **Compact** . . . . **Single 18 Pin Hermetic DIP Package**
- **Models with MIL-STD-883A Class B Processing Available From Stock**

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



TOP VIEW

18 PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

ORDERING INFORMATION

MODEL	MONOTONICITY	TEMP RANGE
DAC-06AX	10 BITS	-55°/+125°C
DAC-06BX	9 BITS	-55°/+125°C
DAC-06CX	8 BITS	-55°/+125°C
DAC-06EX	10 BITS	0°/+70°C
DAC-06FX	9 BITS	0°/+70°C
DAC-06GX	8 BITS	0°/+70°C

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

MODEL	MONOTONICITY
DAC06-883-AX	10 BITS
DAC06-883-BX	9 BITS
DAC06-883-CX	8 BITS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range		Internal Reference Output Current	300μA
DAC-06A, B, C	-55°C to +125°C	Reference Input Voltage	0 to +10V
DAC-06E, F, G	0°C to +70°C	Bipolar Offset Input Voltage	0 to +10V
Storage Temperature Range	-65°C to +150°C	Internal Power Dissipation	500 mW
V+ Supply to Analog Ground	0 to +18V	Lead Soldering Temperature	300°C (60 sec)
V- Supply to Analog Ground	0 to -18V	Output Short Circuit Duration	Indefinite
Analog Ground to Digital Ground	0 to ±0.5V	(Short circuit may be to ground or either supply.)	
Logic Inputs to Digital Ground	-5V to (V_+ - .7V)		

DAC-06 DEFINITIONS

FULL SCALE OUTPUT RANGE—The peak-to-peak voltage swing of the converter's output, i.e. $|V_{FS+}|+|V_{FS-}|$ for bipolar operation, and $(V_{FS}-V_{ZS})$ for unipolar operation.

POSITIVE BIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS+})—The output for 0111111111 input code.

NEGATIVE BIPOLAR FULL SCALE OUTPUT VOLTAGE(V_{FS-})—The output voltage for 1000000001 input code for Two's Complement coding, or the output voltage for 1000000000 input code for One's Complement coding.

UNIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS})—The (positive) output voltage for 0111111111 input code.

UNIPOLAR ZERO SCALE OUTPUT VOLTAGE (V_{ZS})—The output voltage for 1000000000 input code.

BIPOLAR OFFSET VOLTAGE 1/2($|V_{FS+}|-|V_{FS-}|$)—The maximum error due to asymmetry around zero output expressed as a percentage of Full Scale Output Range. (This is adjustable to zero—see Adjustment Procedures on the last page.)

LEAST SIGNIFICANT BIT (LSB)—The smallest incremental output change obtainable, which is ideally equal to the full scale output range divided by 2^{n-1}, where n = number of bits of resolution.

MOST SIGNIFICANT BIT (MSB)—The largest incremental output change obtainable by switching a single logic input, ideally equal to the ideal LSB multiplied by 2^{n-1}, where n = number of bits of resolution. In Two's and One's Complement Converters this MSB is inverted with respect to the other (binary) bits and is used as a sign bit; this feature is incorporated into the DAC-06 design.

MONOTONICITY—Having each successive output state greater than or equal to the preceding one when the DAC is sequenced through all successive states from V_{FS-} to V_{FS+}.

FULL SCALE TEMPERATURE COEFFICIENT—Change in absolute full scale output range in ppm between 25°C and either temperature extreme divided by the corresponding change in temperature.

POWER SUPPLY SENSITIVITY—The ratio of the percentage change in full scale output range to the change in the supply voltage producing it.

ELECTRICAL CHARACTERISTICS – MILITARY GRADES

These specifications apply for V_S = ±15V and T_A = -55°C to +125°C unless otherwise specified.

			DAC-06A			DAC-06B			DAC-06C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			10	10	10	10	10	10	10	10	10	bits
Monotonicity			10	—	—	9	—	—	8	—	—	bits
Nonlinearity	NL	T_A = 0°C to 70°C	0.1	—	—	0.2	—	—	0.4	—	—	%FSR
		T_A = -55°C to +125°C	0.2	—	—	0.3	—	—	0.5	—	—	%FSR
Full Scale Tempco	TCV_{FS}	Internal Reference Connected	—	30	60	—	45	90	—	60	120	ppm/°C
		External Reference Connected	—	30	—	—	30	—	—	30	—	ppm/°C
Full Scale Output Range	FSR	($|V_{FS-}| + |V_{FS+}|$) (Note 1)	10	—	11.5	10	—	11.5	10	—	11.5	V
Unipolar Zero Scale Output Voltage (Pin 18 to Pin 11)	V_{ZS}	T_A = +25°C	—	1.0	5.0	—	1.0	5.0	—	1.0	5.0	mV
		T_A = -55°C to +125°C	—	2.0	10	—	2.0	10	—	2.0	10	mV
Bipolar Offset Voltage (Pin 15 to 18 and 17)		½($|V_{FS+}|-|V_{FS-}|$)	-5.0	—	-0.1	-5.0	—	-0.1	-5.0	—	-0.1	%FSR
Settling Time	t_s	To ±½ LSB, 10 Volt Step	—	1.5	—	—	1.5	—	—	1.5	—	μsec
Reference Input Slew Rate			—	1.5	—	—	1.5	—	—	1.5	—	V/μsec
Reference Input Bias Current			—	100	—	—	100	—	—	100	—	nA
Reference Input Impedance			—	200	—	—	200	—	—	200	—	MΩ
Reference Output Voltage			—	6.7	—	—	6.7	—	—	6.7	—	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ — .7V)	—	±1.0	±10	—	+1.0	±10	—	±1.0	±10	μA
Logic Input "0"	V_{IL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input "1"	V_{IH}		2.0	—	—	2.0	—	—	2.0	—	—	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		T_A = +25°C	—	0.02	0.05	—	0.02	0.05	—	0.02	0.05	%FS/V
		T_A = -55°C to +125°C	—	0.05	0.1	—	0.05	0.1	—	0.05	0.1	%FS/V
Power Dissipation (I_{OUT} = 0)		T_A = +25°C	—	200	300	—	200	300	—	200	300	mW
		T_A = -55°C to +125°C	—	250	350	—	250	350	—	250	350	mW

NOTE 1: Reference output terminal connected to Reference Input terminal and to Bipolar Adjust terminal with R_L = 2KΩ.

CONNECTION INFORMATION

EXTERNAL ADJUSTMENTS – Full Scale Range and Bipolar Symmetry may be adjusted using the connections shown with the procedures on the next page.

REFERENCE INPUT BYPASS – Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input and the Bipolar Offset Adjust inputs with 0.01μF disc capacitors connected to Analog Ground.

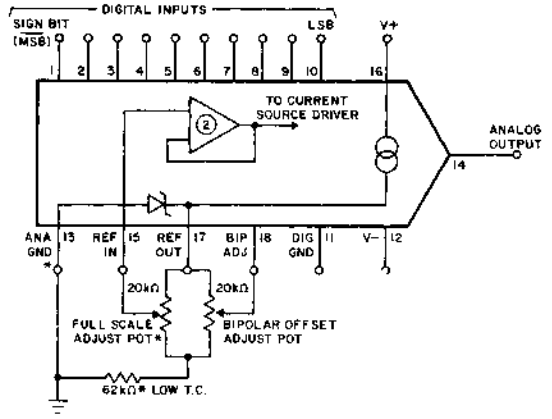
GROUNDING – For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-06 package, so that large digital currents do not flow through the analog ground path.

REFERENCE OUTPUT – For best results, Reference Output current should not exceed 100μA.

USE WITH EXTERNAL REFERENCES – Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-06's to the Reference Output of any one of them.

UNIPOLAR OPERATION – Operation as a 10V positive output 10 bit converter may be implemented by permanently tying pin 18 to ground.

LOWER RESOLUTION APPLICATIONS – For applications not requiring full 10 bit resolution, unused logic inputs should be tied to ground.



NOTE: For unipolar operation, omit the Bipolar offset adjustment potentiometer.

ELECTRICAL CHARACTERISTICS – COMMERCIAL GRADES

These specifications apply for $V_S = \pm 15V$ and $T_A = 0°C$ to $70°C$ unless otherwise specified.

			DAC-06E			DAC-06F			DAC-06G			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Resolution			10	10	10	10	10	10	10	10	10	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	$T_A = +25°C$	0.1	–	–	0.2	–	–	0.4	–	–	%FSR
		$T_A = 0°C$ to $+70°C$	0.2	–	–	0.3	–	–	0.5	–	–	%FSR
Full Scale Tempco (Note 2)	TCV_{FS}	Internal Reference Connected	–	45	100	–	45	100	–	45	100	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Range	FSR	$\lvert V_{FS-}\rvert + \lvert V_{FS+}\rvert$ (Note 1)	10	–	11.5	10	–	11.5	10	–	11.5	V
Unipolar Zero Scale Output Voltage (Pin 18 to Pin 11)	V_{ZS}	$T_A = +25°C$	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		$T_A = 0°C$ to $+70°C$	–	2.0	10	–	2.0	10	–	2.0	10	mV
Bipolar Offset Voltage (Pin 15 to 18 and 17)		$½(\lvert V_{FS+}\rvert - \lvert V_{FS-}\rvert)$	-5.0	–	-0.1	-5.0	–	-0.1	-5.0	–	-0.1	%FSR
Settling Time	t_s	To ±½ LSB, 10 Volt Step	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	± 10	–	±1.0	± 10	–	±1.0	± 10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		$T_A = +25°C$	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	%FS/V
		$T_A = 0°C$ to $+70°C$	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	%FS/V
Power Dissipation (I_{OUT} = 0)		$T_A = +25°C$	–	200	300	–	200	300	–	200	300	mW
		$T_A = 0°C$ to $+70°C$	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference Output terminal connected to Reference Input terminal and to Bipolar Adjust terminal with $R_L = 2K\Omega$.

NOTE 2: Parameter is not 100% tested; 90% of units meet this specification.

ADJUSTMENT PROCEDURES

ADJUSTING FOR TWO'S COMPLEMENT CODING

1. Turn all bits off (V_{FS-}-LSB) — 1 0 0 0 0 0 0 0 0 0
2. Adjust Bipolar Pot for V_{FS-}-LSB at output . . . . . for ±5V operation adjust to -5.0098V.
3. Turn all bits on (V_{FS+}) — 0 1 1 1 1 1 1 1 1 1
4. Adjust Full Scale Pot for desired V_{FS+} value . . . . . for ±5V operation adjust output to +5.0000V.
5. Check Zero Scale Reading (V_{ZS}) — 0 0 0 0 0 0 0 0 0 0
   If this reading is outside desired V_{ZS} range, readjust Bipolar Pot till the output reads 0.0000 V.

TWO'S COMPLEMENT CODING TABLE

	INPUT MSB									LSB	IDEAL OUTPUT
V_{FS+}	0	1	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} − LSB	0	1	1	1	1	1	1	1	1	0	+4.990V
+1 LSB	0	0	0	0	0	0	0	0	0	1	+0.010V
Zero	0	0	0	0	0	0	0	0	0	0	0.000V
−1 LSB	1	1	1	1	1	1	1	1	1	1	-0.010V
V_{FS-}+LSB	1	0	0	0	0	0	0	0	1	0	-4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	1	-5.000V

IMPLEMENTING STRAIGHT OFFSET BINARY CODING – Straight Offset Binary coding is exactly the same as One's Complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-06 to Straight Offset Binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, and 4 of the One's Complement adjustment procedure.

ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Turn all bits off (V_{FS-}) — 1 0 0 0 0 0 0 0 0 0
2. Adjust Bipolar Pot for V_{FS-} at output . . . . . for ±5V operation adjust to -5.0000V.
3. Turn all bits on (V_{FS+}) — 0 1 1 1 1 1 1 1 1 1
4. Adjust Full Scale Pot for desired V_{FS+} value . . . . . for ±5V operation adjust output to +5.0000V.

ONE'S COMPLEMENT CODING TABLE

	INPUT MSB									LSB	IDEAL OUTPUT
V_{FS+}	0	1	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} − LSB	0	1	1	1	1	1	1	1	1	0	+4.990V
+0	0	0	0	0	0	0	0	0	0	0	+0.005V
-0	1	1	1	1	1	1	1	1	1	1	-0.005V
V_{FS-}+LSB	1	0	0	0	0	0	0	0	0	1	-4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	0	-5.000V

NOTE that two zero states will straddle (±½ LSB) the true zero. Therefore the DAC will give symmetrical outputs for both positive and negative full scale.

STRAIGHT OFFSET BINARY CODING TABLE

	INPUT MSB									LSB	IDEAL OUTPUT
V_{FS+}	1	1	1	1	1	1	1	1	1	1	+5.000V
V_{FS+} − 1 LSB	1	1	1	1	1	1	1	1	1	0	+4.990V
+ ½ LSB	1	0	0	0	0	0	0	0	0	0	+0.005V
Zero - ½ LSB	0	1	1	1	1	1	1	1	1	1	-0.005V
V_{FS-}+1 LSB	0	0	0	0	0	0	0	0	0	1	-4.990V
V_{FS-}	0	0	0	0	0	0	0	0	0	0	-5.000V

DAC-08

8 BIT HIGH SPEED MULTIPLYING D/A CONVERTER

UNIVERSAL DIGITAL LOGIC INTERFACE

GENERAL DESCRIPTION

The DAC-08 series of 8 bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 nsec settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8 bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33 mW power consumption attainable at ±5V supplies.

FEATURES

- Fast Settling Output Current . . . . . 85 nsec
- Full Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% Max Over Temp Range
- High Output Impedance and Compliance . . −10V to +18V
- Differential Current Outputs
- Wide Range Multiplying Capability . . . . 1 MHz Bandwidth
- Low FS Current Drift . . . . . ±10ppm/°C
- Wide Power Supply Range . . . . . ±4.5V to ±18V
- Low Power Consumption . . . . . 33 mW @ ±5V
- Low Cost

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883A, Level B are available.

DAC-08 applications include 8 bit, 1 μsec A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT

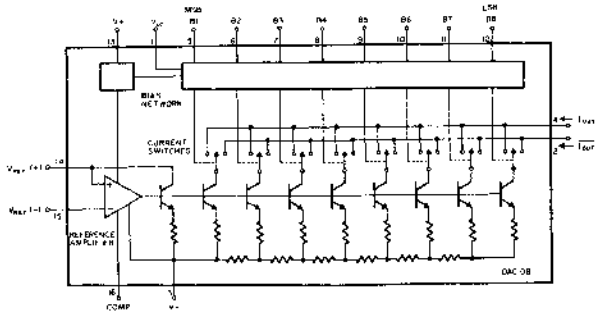
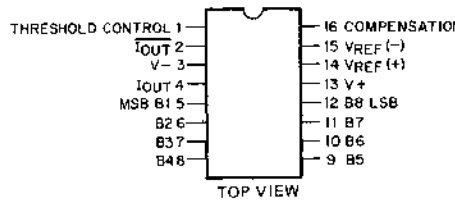


FIGURE 1

ORDERING INFORMATION AND PIN CONNECTION



TOP VIEW

16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE	NONLINEARITY
DAC-08AQ	-55°/+125°C	±0.1%
DAC-08Q	-55°/+125°C	±0.19%
DAC-08HQ	0°/70°C	±0.1%
DAC-08EQ	0°/70°C	±0.19%
DAC-08CQ	0°/70°C	±0.39%

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: DAC-08-883-AQ
DAC-08-883-Q

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Operating Temperature		V+ Supply to V− Supply	36V
DAC-08AQ, Q	−55°C to +125°C	Logic Inputs	V− to V− plus 36V
DAC-08EQ, CQ, HQ	0°C to +70°C	V_{LC}	V− to V+
Storage Temperature	−65°C to +150°C	Analog Current Outputs	See Fig. 12
Power Dissipation	500mW	Reference Inputs (V_{14}, V_{15})	V− to V+
Derate above 100°C	10mW/°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Soldering Temperature	300°C (60 sec)	Reference Input Current (I_{14})	5.0mA

TYPICAL PERFORMANCE PHOTOGRAPHS

FIGURE 2
TRUE AND COMPLEMENTARY OUTPUT OPERATION

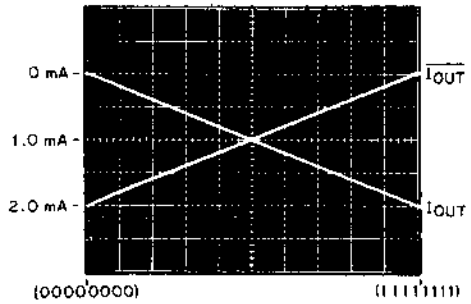
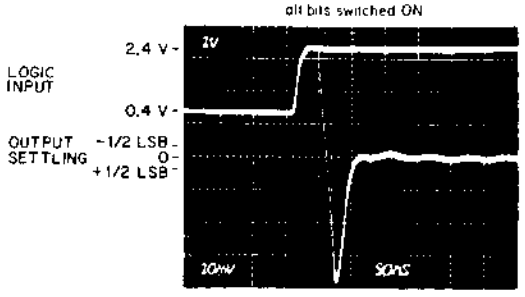


FIGURE 3
FULL SCALE SETTLING TIME



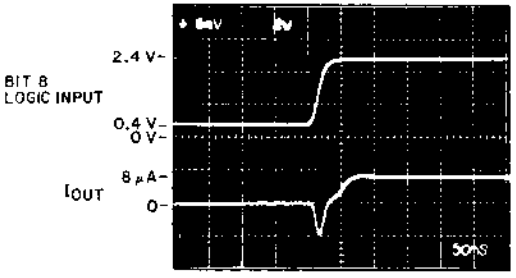
50 nsec/division

SETTLING TIME FIXTURE OF FIGURE 29

I_{FS} = 2mA R_L = 1KΩ

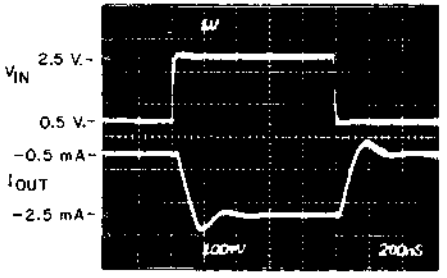
1/2 LSB = 4μA

FIGURE 4
LSB SWITCHING



50 nsec/division

FIGURE 5
FAST PULSED REFERENCE OPERATION



200 nsec/division

SEE FIGURE 27

$R_{EQ} \approx 200\Omega$

$R_L = 100\Omega$

$C_C = 0$

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 2.0 mA, T_A = −55°C to +125°C unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-08A			DAC-08			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			8	8	8	8	8	8	bits
Monotonicity			8	8	8	8	8	8	bits
Nonlinearity		T_A = −55°C to +125°C	–	–	±0.1	–	–	±0.19	% FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF T_A = 25°C	–	85	135	–	85	135	nsec
Propagation Delay Each bit All bits switched	t_{PLH}, t_{PHL}	T_A = 25°C	 – –	 35 35	 60 60	 – –	 35 35	 60 60	 nsec nsec
Full Scale Tempco	TCI_{FS}		–	±10	±50	–	±10	±50	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change <½ LSB R_{OUT} > 20 Megohm typ.	−10	–	+18	−10	–	+18	Volts
Full Scale Current	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4} - I_{FS2}$	–	±0.5	±4.0	–	±1.0	±8.0	µA
Zero Scale Current	I_{ZS}		–	0.1	1.0	–	0.2	2.0	µA
Output Current Range	I_{FSR}	V– = −5.0V V– = −7.0V to −18V	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = 0V	 – 2.0	 – –	 0.8 –	 – 2.0	 – –	 0.8 –	 Volts Volts
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	V_{LC} = 0V V_{IN} = −10V to +0.8V V_{IN} = 2.0V to 18V	 – –	 −2.0 0.002	 −10 10	 – –	 −2.0 0.002	 −10 10	 µA µA
Logic Input Swing	V_{IS}	V– = −15V	−10	–	+18	−10	–	+18	Volts
Logic Threshold Range	V_{THR}	V_S = ±15V	−10	–	+13.5	−10	–	+13.5	Volts
Reference Bias Current	I_{15}		–	−1.0	−3.0	–	−1.0	−3.0	µA
Reference Input Slew Rate	dI/dt	See Figs. 5, 27	4.0	8.0	–	4.0	8.0	–	mA/µsec
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V– = −4.5V to −18V I_{REF} = 1.0 mA	– –	±0.0003 ±0.002	±0.01 ±0.01	– –	±0.0003 ±0.002	±0.01 ±0.01	%/% %/%
Power Supply Current	 I+ I– I+ I– I+ I–	V_S = ±5V, I_{REF} = 1.0 mA V_S = +5V, −15V, I_{REF} = 2.0 mA V_S = ±15V, I_{REF} = 2.0 mA	 – – – – – –	 2.3 −4.3 2.4 −6.4 2.5 −6.5	 3.8 −5.8 3.8 −7.8 3.8 −7.8	 – – – – – –	 2.3 −4.3 2.4 −6.4 2.5 −6.5	 3.8 −5.8 3.8 −7.8 3.8 −7.8	 mA mA mA mA mA mA
Power Dissipation	P_D	±5V, I_{REF} = 1.0 mA +5V, −15V, I_{REF} = 2.0 mA ±15V, I_{REF} = 2.0 mA	– – –	33 108 135	48 136 174	– – –	33 108 135	48 136 174	mW mW mW

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 2.0 mA, T_A = 0°C to 70°C unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-08H			DAC-08E			DAC-08C			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Resolution			8	8	8	8	8	8	8	8	8	bits
Monotonicity			8	8	8	8	8	8	8	8	8	bits
Nonlinearity		T_A = 0°C to 70°C	–	–	±0.1	–	–	+0.19	–	–	±0.39	% FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF T_A = 25°C	–	85	135	–	85	150	–	85	150	nsec
Propagation Delay												
Each bit	t_{PLH}	T_A = 25°C	–	35	60	–	35	60	–	35	60	nsec
All bits switched	t_{PHL}		–	35	60	–	35	60	–	35	60	nsec
Full Scale Tempco	TCI_{FS}		–	±10	±50	–	±10	±50	–	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change < ½ LSB R_{OUT} > 20 Megohm typ.	-10	–	+18	-10	–	+18	-10	–	+18	Volts
Full Scale Current	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000k Ω T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4} - I_{FS2}$	–	±0.5	±4.0	–	±1.0	±8.0	–	±2.0	±16	μA
Zero Scale Current	I_{ZS}		–	0.1	1.0	–	0.2	2.0	–	0.2	4.0	μA
Output Current Range	I_{FSR}	V– = –5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V– = –7.0V to –18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels												
Logic "0"	V_{IL}	V_{LC} = 0V	–	–	0.8	–	–	0.8	–	–	0.8	Volts
Logic "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	Volts
Logic Input Current		V_{LC} = 0V										
Logic "0"	I_{IL}	V_{IN} = –10V to +0.8V	–	-2.0	-10	–	-2.0	-10	–	-2.0	-10	μA
Logic "1"	I_{IH}	V_{IN} = 2.0V to 18V	–	0.002	10	–	0.002	10	–	0.002	10	μA
Logic Input Swing	V_{IS}	V– = –15V	-10	–	+18	-10	–	+18	-10	–	+18	Volts
Logic Threshold Range	V_{THR}	V_S = +15V	-10	–	+13.5	-10	–	+13.5	-10	–	+13.5	Volts
Reference Bias Current	I_{15}		–	–1.0	–3.0	–	-1.0	-3.0	–	-1.0	-3.0	μA
Reference Input Slew Rate	dI/dt	See Figs. 5, 27	4.0	8.0	–	4.0	8.0	–	4.0	8.0	–	mA/μsec
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5V to 18V	–	±0.0003	±0.01	–	±0.0003	±0.01	–	±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V– = –4.5V to –18V	–	±0.002	±0.01	–	±0.002	±0.01	–	±0.002	±0.01	%/%
		I_{REF} = 1.0 mA										
Power Supply Current		V_S = ±5V,										
	I+	I_{REF} = 1.0 mA	–	2.3	3.8	–	2.3	3.8	–	2.3	3.8	mA
	I-		–	–4.3	-5.8	–	-4.3	-5.8	–	-4.3	-5.8	mA
		V_S = +5V, -15V										
	I+	I_{REF} = 2.0 mA	–	2.4	3.8	–	2.4	3.8	–	2.4	3.8	mA
	I-		–	-6.4	-7.8	–	-6.4	-7.8	–	-6.4	-7.8	mA
		V_S = ±15V										
	I+	I_{REF} = 2.0 mA	–	2.5	3.8	–	2.5	3.8	–	2.5	3.8	mA
	I-		–	–6.5	–7.8	–	–6.5	–7.8	–	–6.5	–7.8	mA
Power Dissipation	P_D	±5V, I_{REF} = 1.0 mA	–	33	48	–	33	48	–	33	48	mW
		+5V, -15V, I_{REF} = 2.0 mA	–	108	136	–	103	136	–	108	136	mW
		±15V, I_{REF} = 2.0 mA	–	135	174	–	135	174	–	135	174	mW

TYPICAL PERFORMANCE CURVES

FIGURE 6
FULL SCALE CURRENT VS. REFERENCE CURRENT

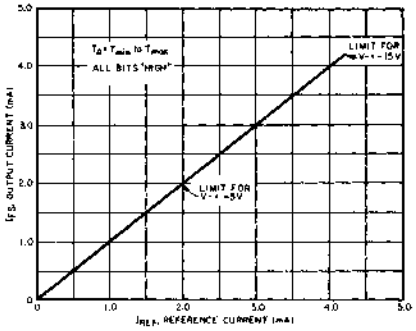


FIGURE 7
LSB PROPAGATION DELAY VS. I_{FS}

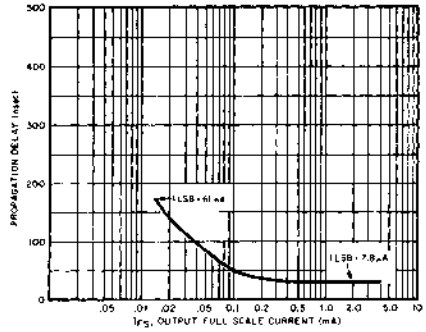
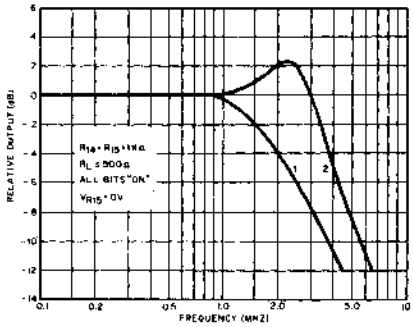
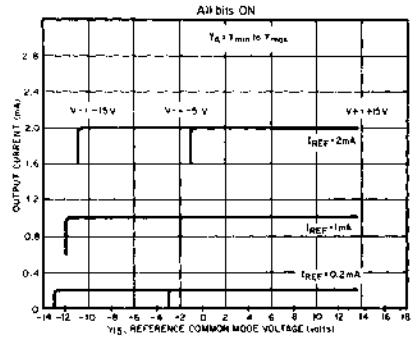


FIGURE 8
REFERENCE INPUT FREQUENCY RESPONSE



CURVE 1 C_C=15pF, V_{IN} = 2.0 Vp-p CENTERED AT +1.0 V, LARGE SIGNAL
CURVE 2 C_C=15pF, V_{IN} = 50mVp-p CENTERED AT +200mV, SMALL SIGNAL

FIGURE 9
REFERENCE AMP COMMON MODE RANGE



NOTE: POSITIVE COMMON MODE RANGE IS ALWAYS (V+) − 1.5 V

FIGURE 10
LOGIC INPUT CURRENT VS. INPUT VOLTAGE

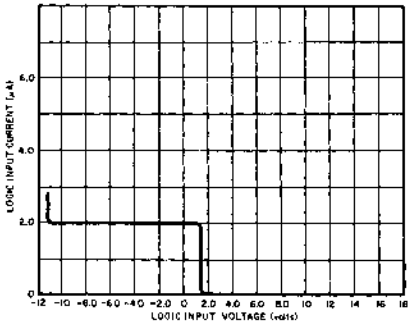
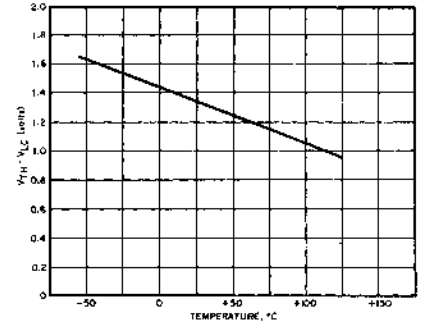


FIGURE 11
$V_{TH} - V_{LC}$ VS. TEMPERATURE



TYPICAL PERFORMANCE CURVES

FIGURE 12
OUTPUT CURRENT VS. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

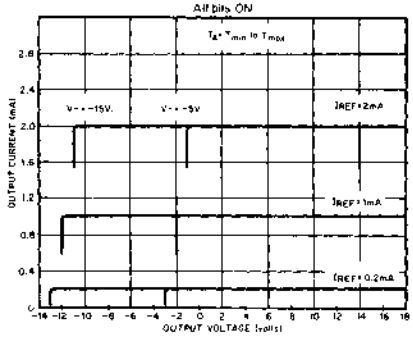


FIGURE 13
OUTPUT VOLTAGE COMPLIANCE VS. TEMPERATURE

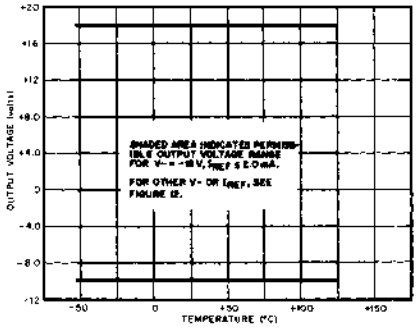
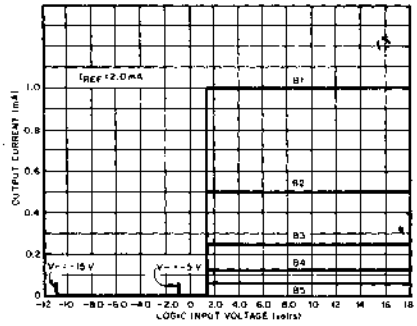


FIGURE 14
BIT TRANSFER CHARACTERISTICS



NOTE: B1 THROUGH B8 HAVE IDENTICAL TRANSFER CHARACTERISTICS, BITS ARE FULLY SWITCHED, WITH LESS THAN ½ LSB ERROR, AT LESS THAN ±100mV FROM ACTUAL THRESHOLD. THESE SWITCHING POINTS ARE GUARANTEED TO LIE BETWEEN 0.8 AND 2.0 VOLTS OVER THE OPERATING TEMPERATURE RANGE (V_{LC} = 0.0V).

FIGURE 15
POWER SUPPLY CURRENT VS. V+

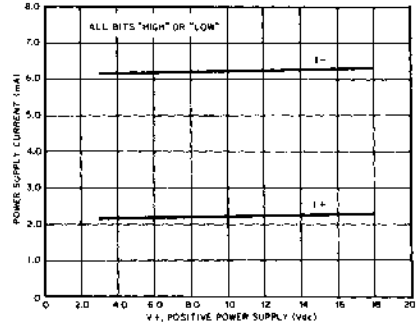


FIGURE 16
POWER SUPPLY CURRENT VS. V–

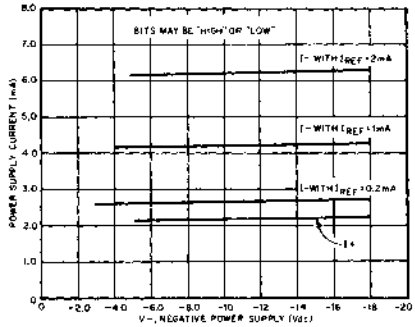
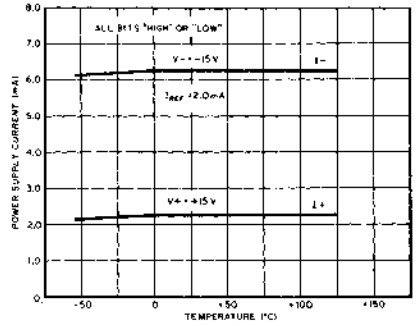
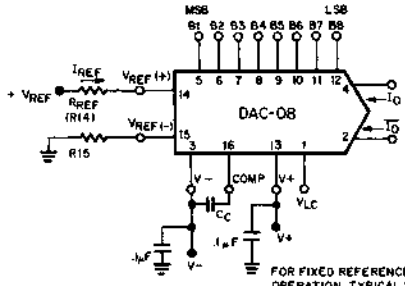


FIGURE 17
POWER SUPPLY CURRENT VS. TEMPERATURE



BASIC CONNECTIONS

FIGURE 18
BASIC POSITIVE REFERENCE OPERATION



FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$

$R_{REF} = 5.000K$

$R_{15} \simeq R_{REF}$

$C_C = 0.01\mu F$

$V_{LC} = 0$ V (GROUND)

$$I_{FS} \simeq \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ FOR ALL LOGIC STATES

FIGURE 19
RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

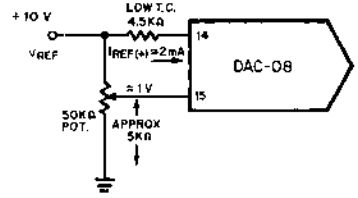
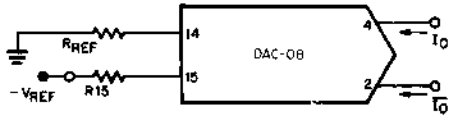


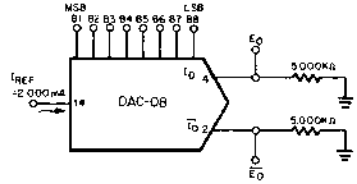
FIGURE 20
BASIC NEGATIVE REFERENCE OPERATION



$$I_{FS} \simeq \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

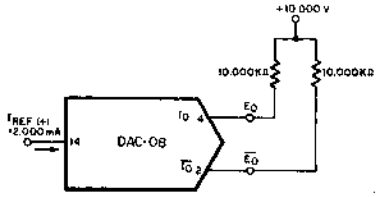
NOTE 1. R_{REF} SETS I_{FS}; R15 IS FOR BIAS CURRENT CANCELLATION.

FIGURE 21
BASIC UNIPOLAR NEGATIVE OPERATION



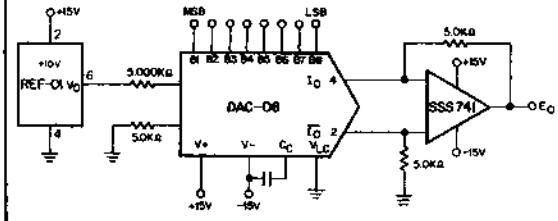
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	.000	-9.960	.000
FULL SCALE +LSB	1	1	1	1	1	1	1	0	1.984	.008	-9.920	-.040
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	.984	-5.040	-4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	-5.000	-4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	.992	1.000	-4.960	-5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	-.040	-9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	-9.960

FIGURE 22
BASIC BIPOLAR OUTPUT OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL SCALE−LSB	1	1	1	1	1	1	1	0	−9.840	+ 9.920
ZERO SCALE+LSB	1	0	0	0	0	0	0	1	−0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	−9.920

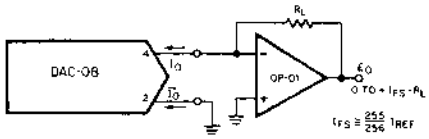
FIGURE 23
SYMMETRICAL OFFSET BINARY OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE−LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	−0.040
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	−9.920

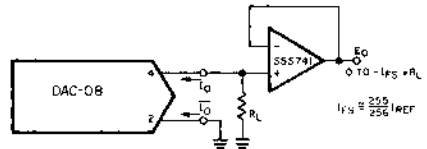
BASIC CONNECTIONS

FIGURE 24
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND

FIGURE 25
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

FIGURE 26
INTERFACING WITH VARIOUS LOGIC FAMILIES

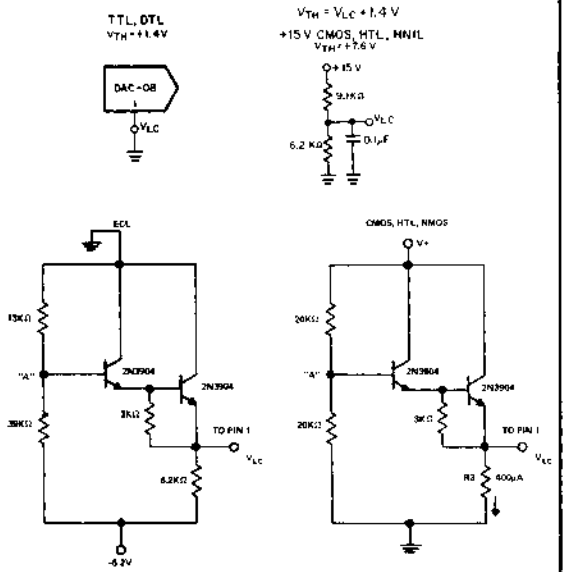


FIGURE 27
PULSED REFERENCE OPERATION

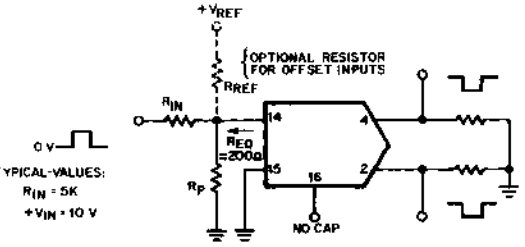
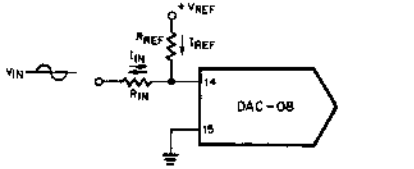
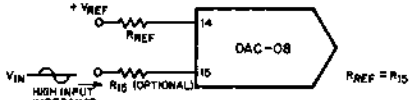


FIGURE 28
ACCOMODATING BIPOLAR REFERENCES



$I_{REF} \geq$ PEAK NEGATIVE SWING OF I_{IN}

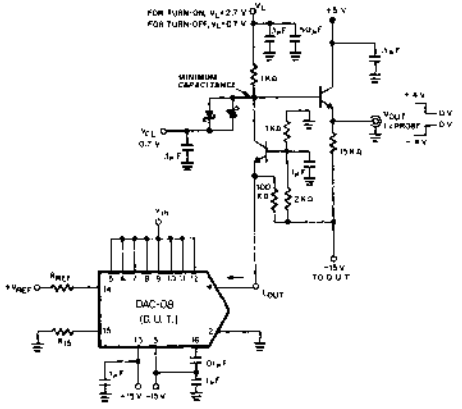
FIGURE A



+V_{REF} MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

FIGURE B

FIGURE 29
SETTLING TIME MEASUREMENT



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications (Fig. 18), an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15 (Fig. 20); reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15 as shown in Fig. 28. The negative common mode range of the reference amplifier is given by: $V_{CM^-} = V-$ plus ($I_{REF} \times 1K\Omega$) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects in shown in Fig. 19.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01 μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 mA to 4 μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0KΩ, minimum values of C_c are 15, 37, and 75 pF. Larger values of R_{14} require proportionately increased values of C_c for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_c values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1 KΩ and C_c = 15 pF, the reference amplifier slews at 4 mA/μsec enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 nsec.

Operation with pulse inputs to the reference amplifier may be accomodated by an alternate compensation scheme shown in Fig. 27. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2mA) occurs in 120nsec when the equivalent impedance at pin 14 is 200 Ω and C_c = 0. This yields a reference slew rate of 16mA/μsec which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 1K\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). Fig. 11 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see Fig. 26. For general setup of the logic control circuit, it should be noted that pin 1 will source 100 μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1 KΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

APPLICATIONS INFORMATION

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} X1 KΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)(V+) + (I+)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10 ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85 nsec at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 nsec for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35 nsec, with each progressively larger bit taking successively longer. The MSB settles in 85 nsec, thus determining the overall settling time of 85 nsec. Settling to 6-bit accuracy requires about 65 to 70 nsec. The output capacitance of the DAC-08 including the package is approximately 15 pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4 μA, therefore a 1 KΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Fig. 29 uses a cascode design to permit driving a 1 KΩ load with less than 5 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

DAC-20

2 DIGIT BCD HIGH SPEED MULTIPLYING DAC
UNIVERSAL DIGITAL LOGIC INTERFACE

GENERAL DESCRIPTION

The DAC-20 series of 2 digit BCD monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design* achieves 85 nsec settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary current outputs with -10V to +18V voltage compliance enable resistive termination, a voltage output without an external op amp.

All DAC-20 series models guarantee full 2 digit monotonicity, and nonlinearities as tight as ±¼ LSB over the entire operating temperature range are available. Nonlinearity is unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

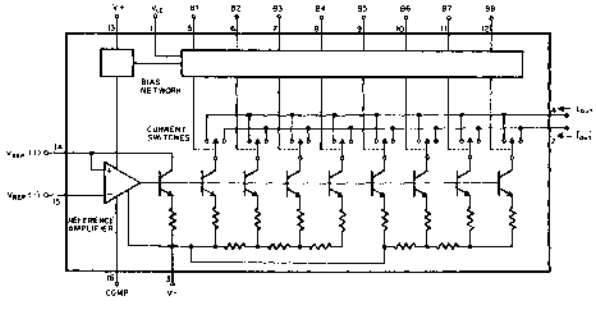
FEATURES

- Fast Settling Output Current . . . . . 85 nsec
- Full Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±¼ LSB Max Over Temp Range
- High Output Impedance and Compliance . . -10V to +18V
- Complementary Current Outputs
- Wide Range Multiplying Capability . . . . 1 MHz Bandwidth
- Low FS Current Drift . . . . . ±10ppm/°C
- Wide Power Supply Range . . . . . ±4.5V to ±18V
- Low Power Consumption . . . . . 37mW @ ±5V
- Low Cost

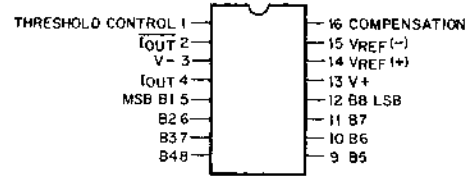
The compact size and low power consumption make the DAC-20 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883A, Level B, are available.

DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ORDERING INFORMATION AND PIN CONNECTION



TOP VIEW
16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE	NONLINEARITY
DAC-20AQ	-55°/+125°C	±¼ LSB
DAC-20Q	-55°/+125°C	±½ LSB
DAC-20EQ	0°/70°C	±¼ LSB
DAC-20CQ	0°/70°C	±½ LSB

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: DAC20-883-AQ
DAC20-883-Q

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Operating Temperature Range		V+ Supply to V- Supply	36V
DAC-20AQ, Q	-55°C to +125°C	Logic Inputs	V- to V- plus 36V
DAC-20EQ, CQ	0°C to +70°C	V_{LC}	V- to V+
Storage Temperature Range	-65°C to +150°C		
Power Dissipation	500mW	Reference Inputs (V_{14}, V_{15})	V- to V+
Derate above 100°C	10mW/°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Soldering Temperature	300°C (60 sec)	Reference Input Current (I_{14})	5.0mA

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 2.0 mA, T_A = -55°C to +125°C for DAC-20A and DAC-20, T_A = 0°C to +70°C for DAC-20E and DAC-20C, unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-20A, DAC-20E			DAC-20, DAC-20C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		BCD 0 to 99 steps	2	2	2	2	2	2	digits
Monotonicity		BCD 99 steps	2	2	2	2	2	2	digits
Nonlinearity	NL	FS = 1001 1001	–	–	±1/4	–	–	±1/2	LSB
Settling Time	t_S	To +½LSB (±0.5% FS) all bits switched ON or OFF, T_A = 25°C	–	85	135	–	85	150	nsec
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C							
Each bit			–	35	60	–	35	60	nsec
All bits switched			–	35	60	–	35	60	nsec
Full Scale Tempco	TCI_{FS}		–	±10	±50	–	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change <½LSB (<0.5% FS) R_{OUT} > 20 Megohm typ. I_{REF} = 1.0mA	-10	–	+18	-10	–	+18	Volts
Full Scale Current (Digital Input 1001 1001)	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = 25°C	1.96	1.98	2.00	1.92	1.98	2.04	mA
Zero Scale Current	I_{ZS}		–	0.1	2.5	–	0.2	5.0	µA
Output Current Range	I_{FSR}	V- = -5.0V	0	2.0	2.2	0	2.0	2.2	mA
		V- = -7.0V to -18V	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels									
Logic "0"	V_{IL}	V_{LC} = 0V	–	–	0.8	–	–	0.8	Volts
Logic "1"	V_{IH}		2.0	–	–	2.0	–	–	Volts
Logic Input Current		V_{LC} = 0V							
Logic "0"	I_{IL}	V_{IN} = -10V to +0.8V	–	-2.0	±10	–	-2.0	±10	µA
Logic "1"	I_{IH}	V_{IN} = 2.0V to 18V	–	0.002	±10	–	0.002	±10	µA
Logic Input Swing	V_{IS}	V- = -15V	-10	–	+18	-10	–	+18	Volts
Logic Threshold Range	V_{THR}	V_S = ±15V	-10	–	+13.5	-10	–	+13.5	Volts
Reference Bias Current	I_{15}		–	-1.0	-3.0	–	-1.0	-3.0	µA
Reference Input Slew Rate	dI/dt		4.0	8.0	–	4.0	8.0	–	mA/µsec
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5V to 18V	–	±0.0003	±0.03	–	±0.0003	±0.03	%/%
	$PSSI_{FS-}$	V- = -4.5V to -18V	–	±0.002	±0.03	–	±0.002	±0.03	%/%
		I_{REF} = 1.0mA							
Power Supply Current		V_S = ±5V, I_{REF} = 1.0 mA							
	I+		–	2.3	3.8	–	2.3	3.8	mA
	I-		–	-5.0	-6.5	–	-5.0	-6.5	mA
		V_S = ±15V, I_{REF} = 2.0 mA							
	I+		–	2.5	3.8	–	2.5	3.8	mA
	I-		–	-7.8	-9.1	–	-7.8	-9.1	mA
Power Dissipation	P_D	V_S = ±5V, I_{REF} = 1.0 mA	–	37	52	–	37	52	mW
		V_S = ±15V, I_{REF} = 2.0 mA	–	152	194	–	152	194	mW

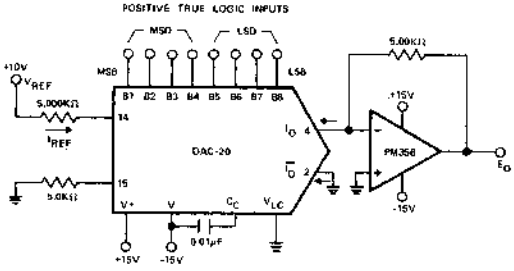
BASIC OUTPUT CONNECTIONS

With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned off at pin 4 and on at pin 2 ($\overline{I_O}$) which is used for negative true or "negative logic" D/A converters.

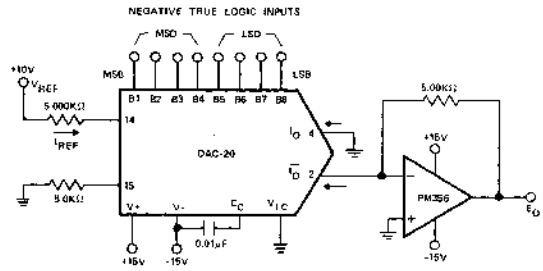
The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF}. A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by V- plus (I_{REF} X800Ω) plus 2.5V.

POSITIVE VOLTAGE OUTPUT

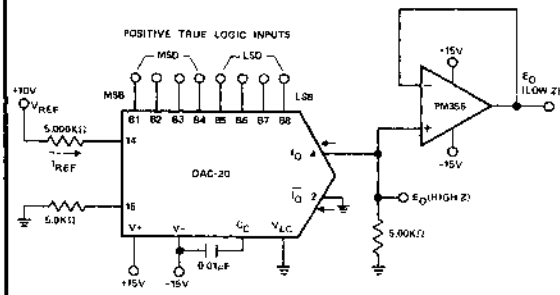


NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99 (FS)	1001	1001	1.98mA	+9.9V

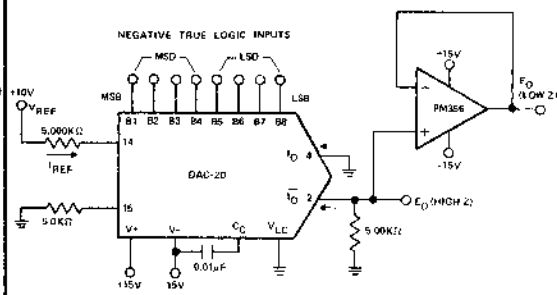


NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99 (FS)	0110	0110	1.98mA	+9.9V

NEGATIVE VOLTAGE OUTPUT



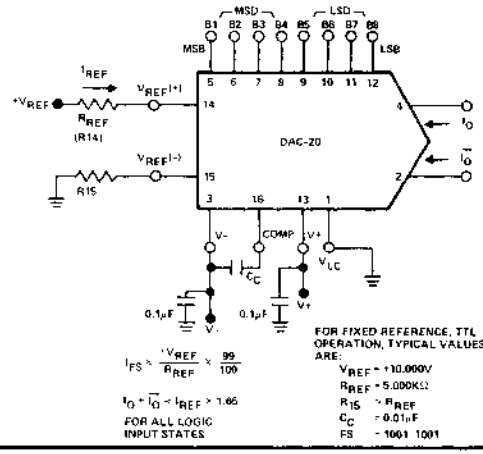
NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	I_o	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	-1.0V
20	0010	0000	0.40mA	-2.0V
30	0011	0000	0.60mA	-3.0V
40	0100	0000	0.80mA	-4.0V
80	1000	0000	1.60mA	-8.0V
99 (FS)	1001	1001	1.98mA	-9.9V



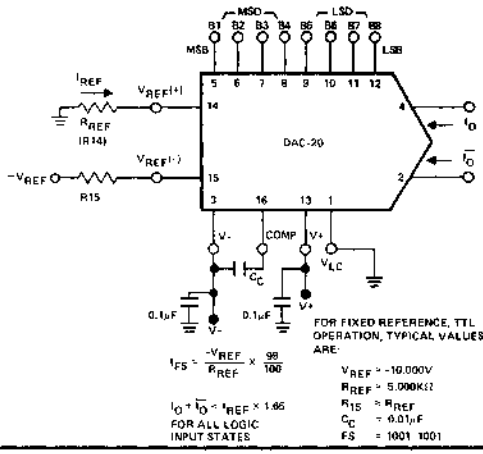
NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	$\overline{I_o}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	-1.0V
20	1101	1111	0.40mA	-2.0V
30	1100	1111	0.60mA	-3.0V
40	1011	1111	0.80mA	-4.0V
80	0111	1111	1.60mA	-8.0V
99 (FS)	0110	0110	1.98mA	-9.9V

REFERENCE OPERATION

POSITIVE



NEGATIVE



REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = 99/100 \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications an external positive reference voltage forces current through R_{14} into the $V_{REF}(+)$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at pin 15; reference current flows from ground through R_{14} into $V_{REF}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

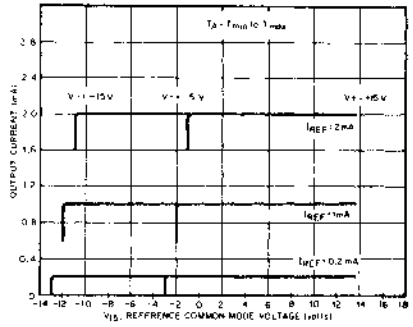
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference such as the PMI REF-01 is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14.

The reference amplifier must be compensated by using a capacitor from pin 16 to V-. For fixed reference operation, a 0.01 μF capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

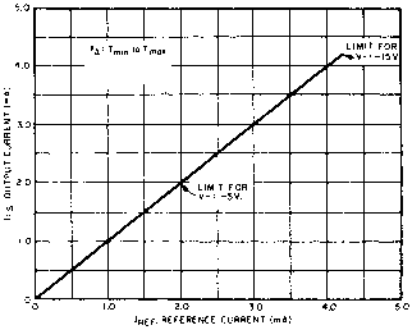
TYPICAL REFERENCE PERFORMANCE CURVES

REFERENCE AMP COMMON MODE RANGE (DIGITAL INPUT 1001 1001)



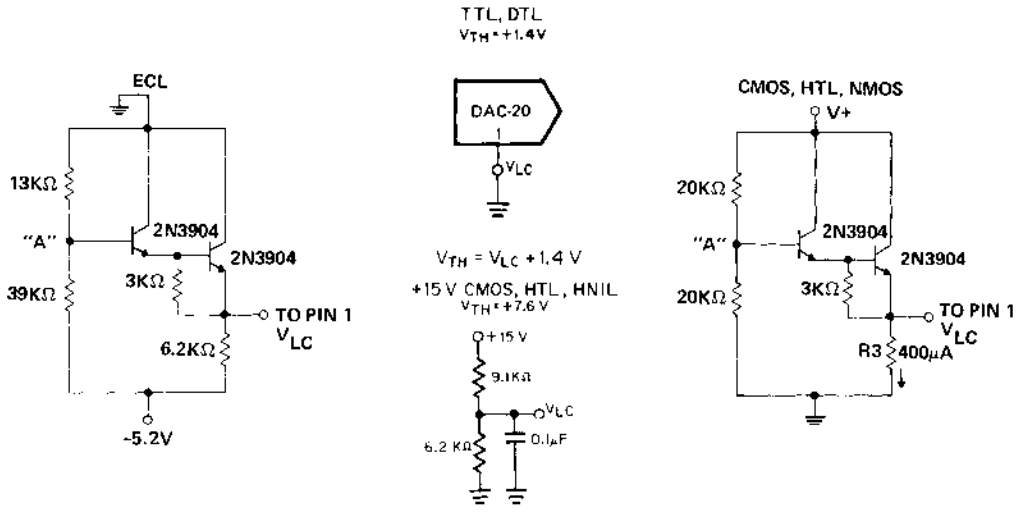
NOTE: Positive common mode range is always (V+)−1.5V; negative common mode range is V- plus(I_{REF} X 800Ω) plus 2.5V.

FULL SCALE CURRENT VS. REFERENCE CURRENT (DIGITAL INPUT 1001 1001)



NOTE: The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

LOGIC INPUT OPERATION AND INTERFACING



LOGIC THRESHOLD CONTROL

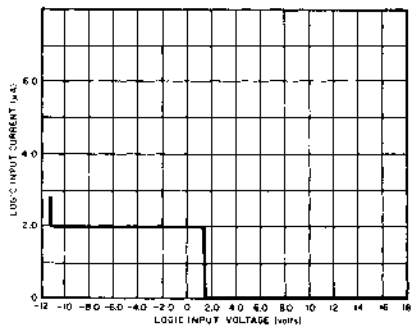
The DAC-20 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V- = -15V, the logic inputs may swing between -10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-20 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V- plus (I_{REF} X 800Ω) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}).

The logic input threshold is 1.4V above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see the figure above. Pin 1 will source 100μA typically, so the external circuitry must be designed to accommodate this current.

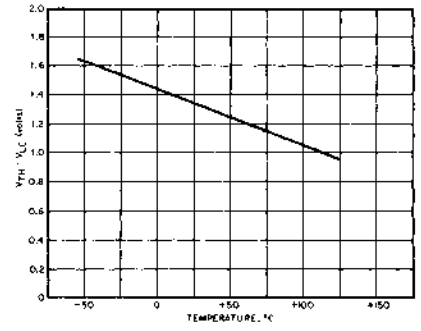
Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1 KΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

TYPICAL PERFORMANCE CURVES

LOGIC INPUT CURRENT VS. INPUT VOLTAGE

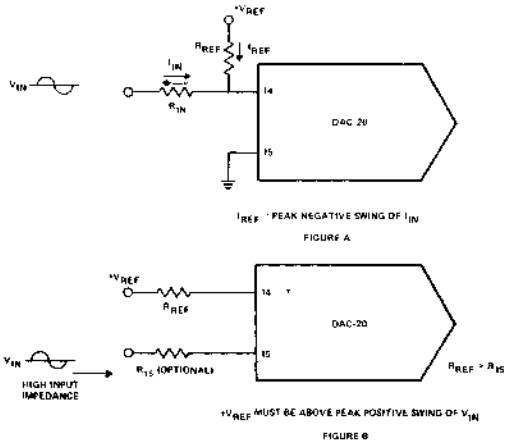


$V_{TH} - V_{LC}$ VS. TEMPERATURE

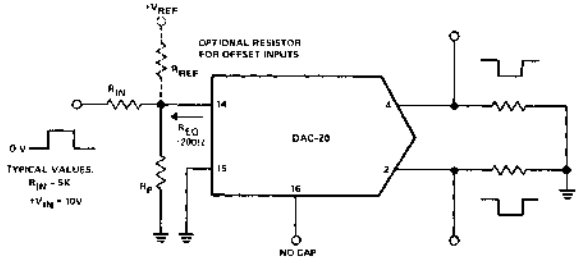


MULTIPLYING OPERATION

ACCOMODATING BIPOLAR REFERENCES



PULSED REFERENCE OPERATION



The DAC-20 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 mA to 4 μA. Monotonic operation is maintained over a typical range of I_{REF} from 100 μA to 4.0 mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: V_{CM-} = V- plus (I_{REF} X 800Ω) plus 2.5V. The positive common mode range is V+ less 1.5V.

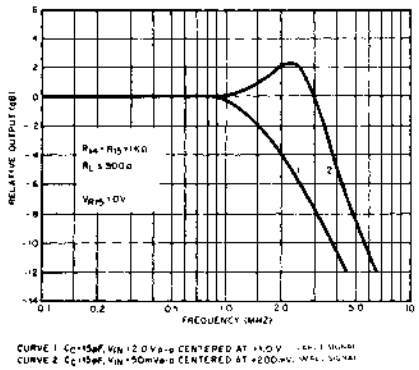
AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0KΩ, minimum values of C_C are 15, 37, and 75 pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1 KΩ and C_C = 15 pF, the reference amplifier slews at 4 mA/μsec enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 nsec.

Operation with pulse inputs to the reference amplifier may be accomodated by the alternate compensation scheme shown above. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2 mA) occurs in 120 nsec when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16 mA/μsec which is relatively independent of R_{IN} and V_{IN} values.

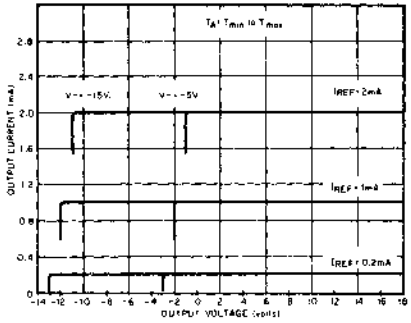
TYPICAL PERFORMANCE CURVES

REFERENCE INPUT FREQUENCY RESPONSE (DIGITAL INPUT 1001 1001)



CURVE 1: C_C=15pF, V_{IN} = 2.0 Vp-p CENTERED AT +1.0 V
CURVE 2: C_C=15pF, V_{IN} = 50mVp-p CENTERED AT +200mV

OUTPUT CURRENT VS. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE) (DIGITAL INPUT 1001 1001)



POWER SUPPLY CONSIDERATIONS

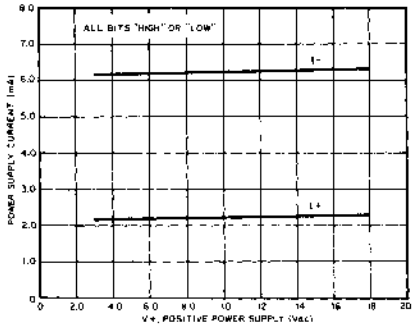
The DAC-20 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-20 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

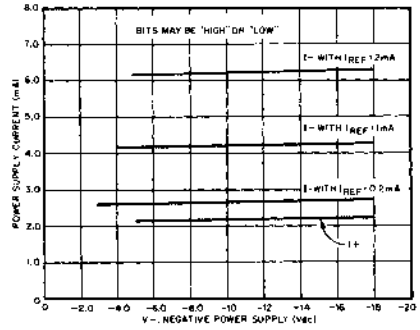
Power consumption may be calculated as follows:
$P_d = (I+)\ (V+) + (I+)\ (V-) + (2\ I_{REF})\ (V-)$. A useful feature of the DAC-20 design is that supply current is constant and independent of input logic states; this reduces the size of the power supply bypass capacitors.

TYPICAL PERFORMANCE CURVES

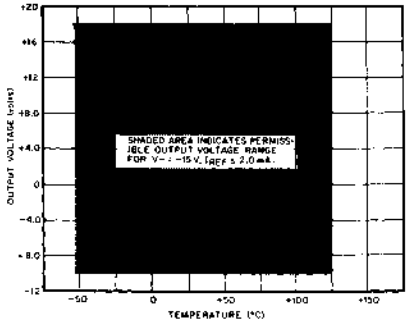
POWER SUPPLY CURRENT VS. V+



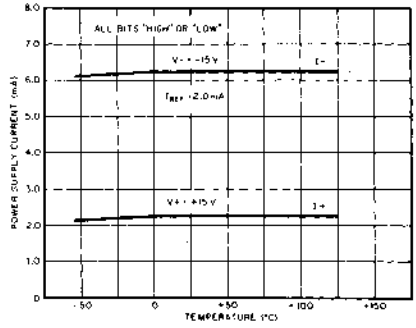
POWER SUPPLY CURRENT VS. V-



OUTPUT VOLTAGE COMPLIANCE VS. TEMPERATURE



POWER SUPPLY CURRENT VS. TEMPERATURE



APPLICATIONS INFORMATION

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-20 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10 ppm/°C, with zero scale output current and drift essentially negligible compared to ½ LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-20 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME OPTIMIZATION

The DAC-20 is capable of extremely fast settling times, typically 85 nsec at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The output capacitance of the DAC-20 including the package is approximately 15 pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 µF capacitors at the supply pins provide full transient protection.

DAC-100

8 & 10 BIT DIGITAL-TO-ANALOG CONVERTER

GENERAL DESCRIPTION

The DAC-100 is a complete 10 bit resolution Digital-to-Analog converter constructed on two monolithic chips in a single 16-pin DIP or 24-pin flatpack. Featuring excellent non-linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, 10 current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output and by matched bipolar offset and feedback resistors which are included for use with an external op amp for voltage output applications. Although all units have 10-bit resolution, a wide choice of nonlinearity and tempco options is provided to allow price/performance optimization.

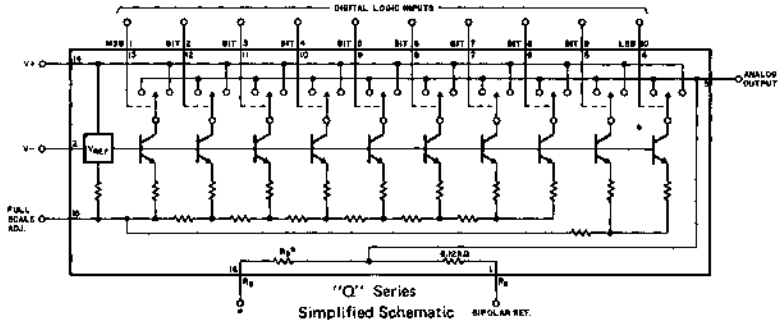
The small size, wide operating temperature range, low power consumption and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed Analog-to-Digital converters.

FEATURES

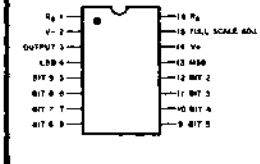
- **Complete** . . . . . **Internal Reference**
- **Flexible** . . . . . **0 to 2mA Output**
- **Fast Settling** . . . . **225nsec (8 Bits), 375nsec (10 Bits)**
- **Stable** . . . . . **Tempcos to ±15ppm/°C Max**
- **0°C/+70°C, −25°C/+85°C, −55°C/+125°C Models Available**
- **TTL and DTL Compatible Logic Inputs**
- **Wide Supply Range** . . . . . **±6V to ±18V**
- **8 and 10 Bit Versions Available**
- **MIL-STD-883A Class B Processing Models Available**
- **Low Cost Q3, Q4 Series**

SIMPLIFIED SCHEMATIC AND PIN CONNECTIONS — 16 LEAD HERMETIC DIP

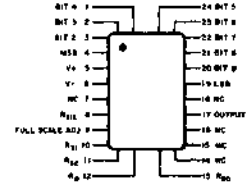
*For 10V or ±5V Operation
R_S = 4.88kΩ (Package Q1, Q3, Q5)
For 5V or ±2.5V Operation,
R_S = 2.44kΩ (Package Q2, Q4 or Q6)



TOP VIEW



16 PIN HERMETIC
DUAL-IN-LINE
(Q-Suffix)



24 PIN HERMETIC
FLATPACK
(N-Suffix)

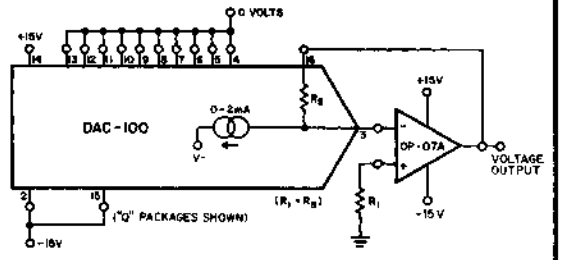
GENERAL INFORMATION

1. The DAC-100 series are digital-to-analog current converters; voltage outputs are implemented by using an external operational amplifier with the internally-provided feedback resistor. For clarity and convenience, most specifications will reference full scale output voltage rather than full scale output current, assuming an "ideal" op amp has been utilized for conversion (See test circuit at right).

2. The logic coding used for driving the DAC-100 should be complementary binary or offset complementary binary to obtain unipolar and bipolar analog outputs, respectively.

3. As shown in the ordering information below, the DAC-100 series provides a wide variety of worst-case nonlinearity and full-scale tempco combination options. All devices have 10 bits of resolution; the nonlinearity options of ±0.05%, ±0.1%, ±0.2% and ±0.3% guarantee monotonic operation for resolutions of 10, 9, 8, and 7 bits respectively. When less than the full 10 bits are utilized, the unused logic inputs must be connected to a "high" logic level (>2.1 V).

FULL SCALE TEST CIRCUIT



DEFINITION: Full Scale Tempco is defined as the change in output voltage measured in the circuit above and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

NOTE: Since R_S precisely tracks the internal R-2R ladder network over temperature, the absolute I_{FS} Tempco of ±120ppm/°C is cancelled by R_S when the output voltage is used as in the above circuit

ORDERING INFORMATION

ORDER NUMBER: DAC-100 X X X X

NONLINEARITY		F.S. TEMPCO		PACKAGE		TEMP RANGE AND OUTPUT VOLTAGE
A	±0.05% MAX	A	15 ppm/°C MAX	Q	16 Pin HERMETIC DUAL-IN-LINE	as shown below
B	±0.1% MAX*	B	30 ppm/°C MAX*	N	24 Pin HERMETIC FLATPACK	
C	±0.2% MAX	C	60 ppm/°C MAX			
D	±0.3% MAX	D	120 ppm/°C MAX			

*NOTE: For DAC-100 BBQ5 and DAC-100 BBQ6 only; nonlinearity is ±0.1% over -25°C to +85°C and ±0.12% over -55°C to +125°C. Full Scale Tempco is 30 ppm/°C over -25°C to +85°C and 40 ppm/°C over -55°C to +125°C.

COMBINATION AVAILABILITY CHART (Temperature Range/Package Option Suffix)

Model	-55°/+125°C 883A Class B		-25°/+85°C 883A Class B		-25°/+85°C		0°/+70°C	
	10V ±5V	5V ±2.5V	10V ±5V	5V ±2.5V	10V ±5V	5V ±2.5V	10V ±5V	5V ±2.5V
DAC-100AA	–	–	N9		Q1	Q2	–	–
DAC-100AB	–	–	N9		Q1	Q2	–	–
DAC-100AC	Q5	Q6	N9		Q1	Q2	Q3	Q4
DAC-100BB	Q5	Q6	N9		Q1	Q2	–	–
DAC-100BC	Q5	Q6	N9		Q1	Q2	Q3	Q4
DAC-100CC	Q5	Q6	N9		Q1	Q2	Q3	Q4
DAC-100DD	–	–	N9		Q1	Q2	Q3	Q4

ABSOLUTE MAXIMUM RATINGS

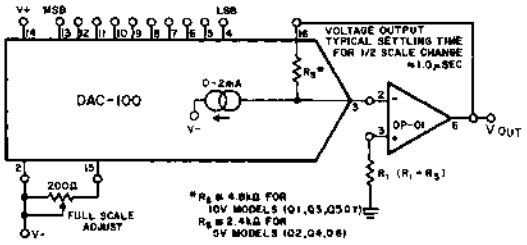
V+ Supply to V– Supply	0 to +36V	Operating Temperature Range	
V+ Supply to Output	0 to +18V	Q3, Q4	0°C to +70°C
V– Supply to Output	0 to –18V	All others	–55°C to +125°C
Logic Inputs to Output	–1V to +6V		
Power Dissipation (Note 1)	500mW	Storage Temperature Range	
		Q and N Packages	–65°C to +150°C
NOTES:			
1. Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.		Lead Temperature (Soldering)	
		Q and N Packages	+300°C (60 sec)

ELECTRICAL CHARACTERISTICS

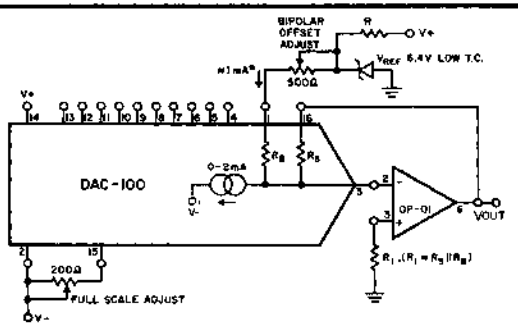
These specifications apply for V_s = ±15V, –25°C ≤ T_A ≤ +85°C for Q1, Q2, and N9 devices; 0°C ≤ T_A ≤ +70°C; for Q3 and Q4, –55°C ≤ T_A ≤ +125°C for Q5 and Q6 devices, unless otherwise specified. (See BBQ5, Q6 note on previous page under Ordering Information.)

Parameter	Conditions	Min	Typ	Max	Units
Resolution		10	10	10	bits
Nonlinearity (For nonlinearity/tempco combinations, see Availability chart.)	"A" option (± ½ LSB –10 bits) "B" option (± ½ LSB –9 bits) "C" option (± ½ LSB –8 bits) "D" option (± ¾ LSB –8 bits)	– – – –	– – – –	± 0.05 ± 0.1 ± 0.2 ± 0.3	% I_{FS} % I_{FS} % I_{FS} % I_{FS}
Full Scale Tempco (See Full Scale Test Circuit.)	"A" option "B" option "C" option "D" option	– – – –	– – – –	± 15 ± 30 ± 60 ±120	ppm/°C ppm/°C ppm/°C ppm/°C
Settling Time T_A = 25°C	to ±0.05% FS to ±0.1% FS to ±0.2% FS to ±0.4% FS to ±0.8% FS	– – – – –	– – – – –	375 300 225 150 100	ns ns ns ns ns
Full Scale Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0) V with a 200Ω (Trimpot®) between FS Adjust and V–.)	Connect FS Adjust to V– 10V Models (Q1, Q3, Q5, N9) 5V Models (Q2, Q4, Q6) V_{IN} = 0.0V	 10 5	 – –	 11.1 5.55	 V V
Zero Scale Output Voltage	V_{IN} = 2.1V	–	–	0.013	% FS
Logic Inputs High Low	Measured with respect to output pin	 2.1 –	 – –	 – 0.7	 V V
Logic Input Current, Each Input	V_{IN} = 0 to +6V	–	–	5	µA
Logic Input Resistance	V_{IN} = 0 to +6V	–	3	–	MΩ
Logic Input Capacitance		–	2	–	pF
Output Resistance		–	500	–	kΩ
Output Capacitance		–	13	–	pF
Applied Power Supplies: V+ V–	 Linearity within specification Linearity within specification	 +6 –6	 – –	 +18 –18	 V V
Power Supply Sensitivity	V_s = ±6V to ±18V	–	–	±0.10	% per volt
Power Consumption Q3, Q4 models All other models	 V_s = ±15V V_s = ±6V V_s = ±15V	 – – –	 200 80 200	 300 100 250	 mW mW mW

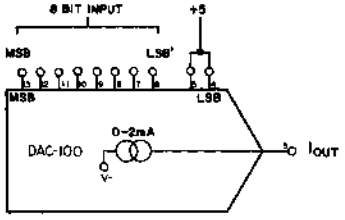
BASIC CONNECTIONS



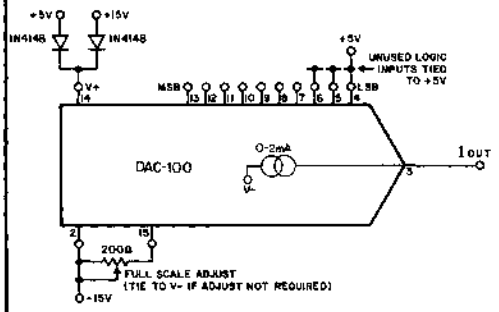
BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT



BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT



REDUCED RESOLUTION APPLICATION



POWER SUPPLY SEQUENCE PROTECTION CIRCUIT

APPLICATIONS INFORMATION

FULL SCALE OUTPUT ADJUSTMENT – The output current of the DAC-100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the Full Scale Adjust pin and V–. Adjustment should be made with an input of all "zeroes."

LOWER RESOLUTION APPLICATIONS – The DAC-100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs *must* be tied to the high logic for proper operation. "Floating" logic inputs can cause improper operation.

LOGIC CODING – The DAC-100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full scale output, while an all "ones" input produces a zero scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input level turns the bit "off," low logic input level turns the bit "on."

LOGIC COMPATIBILITY – The input logic levels are directly compatible with DTL and TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

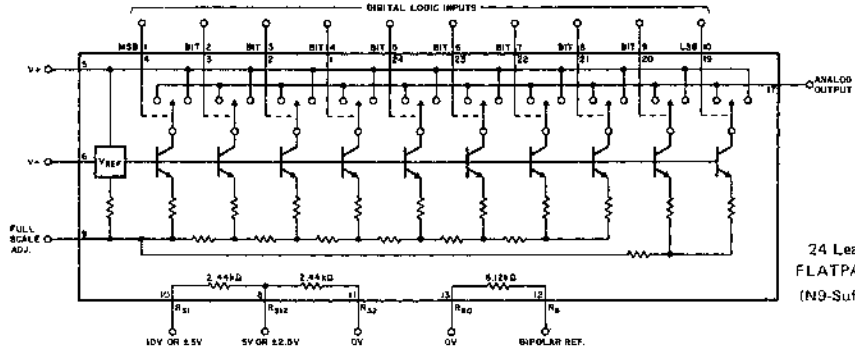
NONLINEARITY (NL). The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of Full Scale Range (FSR) or given in terms of LSB value. The end points are zero scale output to full scale output for unipolar operation and minus full scale to positive full scale for bipolar operation.

BIPOLAR OPERATION – The DAC-100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

POWER SUPPLY SEQUENCING – IMPORTANT – Occasional early DAC-100 devices may suffer temporary malfunction and possible permanent damage if voltage is present at the logic inputs before the V+ supply is available. A simple protection circuit may be implemented by using two silicon diodes to clamp the V+ terminal to the logic supply. DAC-100 devices with date codes of 7547 and later incorporate design changes which eliminate this effect and require no special precautions or protective circuitry.

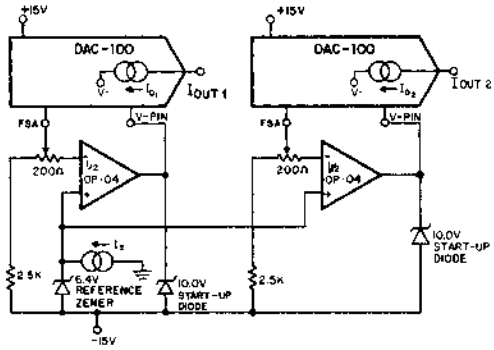
VOLTAGE AT OUTPUT PIN – The DAC-100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output ground is a convenient way of clamping the output to this limit.

SIMPLIFIED SCHEMATIC AND PIN CONNECTIONS – 24 LEAD FLATPACK

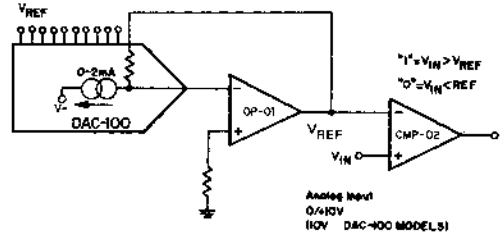


24 Lead
FLATPACK
(N9-Suffix)

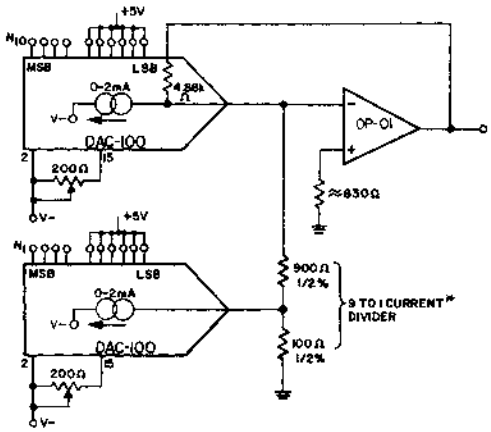
TYPICAL APPLICATIONS



EXTERNAL REFERENCE CONNECTION

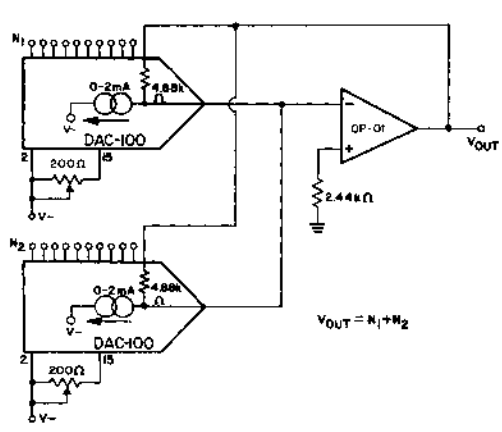


DIGITALLY PROGRAMMED LEVEL DETECTOR



BINARY-CODED-DECIMAL D/A CONVERSION

*(CAN BE EXPANDED TO 3 DIGITS BY ADDITION OF A THIRD DAC-100 AND 99 TO 1 CURRENT DIVIDER)



ANALOG SUM OF TWO DIGITAL NUMBERS

INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about 1μA of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed: logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

Switching is accomplished by forward biasing Q4, a diode-connected transistor, for the bit "on" condition and back biasing Q4 in the "off" condition. For the "on" condition ($V_{IN} \leqslant .7$ volts), Q3 is "off"—all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V-. In the "off" condition ($V_{IN} \geqslant 2.1$ volts), Q3 is "on", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

$$1)BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS inputs is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts, DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

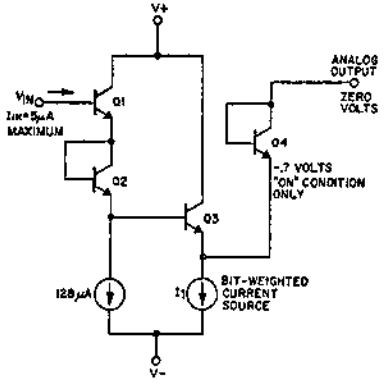
HIGH LEVEL CMOS INTERFACING

The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts—clearly satisfying the input stage voltage rule.

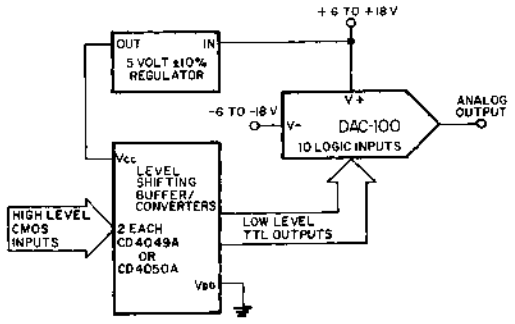
In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or noninverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100-to-CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive 3-terminal IC regulator can supply several level shifting devices.

NOTE: For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."



DAC–100 LOGIC INPUT STAGE



BLOCK DIAGRAM – CMOS TO DAC-100 INTERFACE

SSS562

12 BIT MULTIPLYING D/A CONVERTER

GENERAL DESCRIPTION

The SSS562 is a 12-bit monolithic multiplying Digital-to-Analog converter consisting of a reference current amplifier, an R-2R ladder network, range and offset scaling resistors, and 12 high speed current switches. Improvements over the AD562 include faster settling time, lower power dissipation, greater negative power supply range, and wider voltage compliance. The SSS562 is directly interchangeable with the AD562.

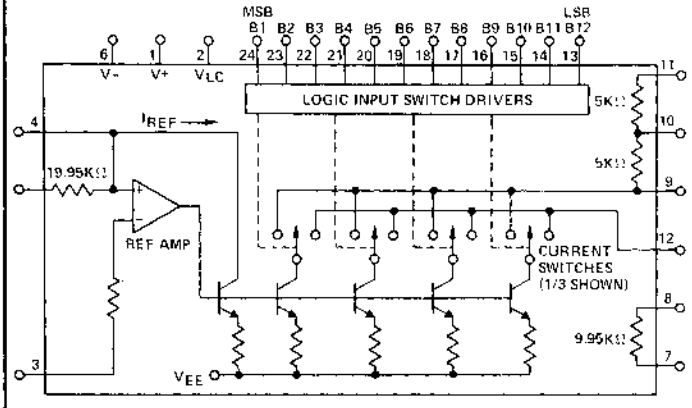
The SSS562 uses a unique trimming method, selective shorting of zener diodes by avalanche migration, to achieve 13 bit accuracy rather than laser trimming. Reliability of this trimming method has been proven in several other PMI products with over 3 years of reliability history. The SSS562 is recommended for 12 bit accuracy D/A applications where single chip reliability, small size and low cost are primary considerations.

FEATURES

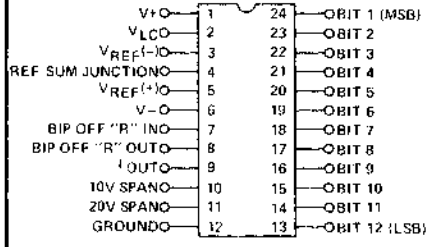
- Single Chip Monolithic Construction*
- Binary and BCD Models
- Nonlinearity to ±1/4 LSB (Max)
- Improved Settling Time . . . . . 1.5 μsec (Max)
- Fits AD562 Socket Directly
- Guaranteed Monotonicity
- High Speed Multiplying Capability
- TTL and CMOS Logic Input Compatibility
- Low Power Consumption
- Low Cost
- MIL-STD-883A Level B Models Available

For improved specifications and greater applications flexibility, see the DAC-12 High Speed Multiplying D/A Converter data sheet.

EQUIVALENT CIRCUIT



PIN CONNECTIONS



TOP VIEW

24-PIN HERMETIC DUAL IN-LINE

(Y-Suffix)

ORDERING INFORMATION

MODEL NUMBER	ADI MODEL NO.	TEMP RANGE
SSS562-SD-BIN	AD562SD/BIN	-55°/+125°C
SSS562-883-BIN	AD562SD/BIN/883	-55°/+125°C
SSS562-SD-BCD	AD562SD/BCD	-55°/+125°C
SSS562-883-BCD	AD562SD/BCD/883	-55°/+125°C
SSS562-AD-BIN	AD562AD/BIN	-25°/+85°C
SSS562-AD-BCD	AD562AD/BCD	-25°/+85°C
SSS562-KD-BIN	AD562KD/BIN	0°/+70°C
SSS562-KD-BCD	AD562KD/BCD	0°/+70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: SSS562-883-BIN
SSS562-883-BCD

*PATENTS APPLIED FOR

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range		Positive Power Supply (V_{CC})	36V– V_{EE}
SSS562-SD	–55°C to +125°C	Negative Power Supply (V_{EE})	36V– V_{CC}
SSS562-AD	–25°C to +85°C	V_{CC} to V_{EE}	36V
SSS562-KD	0°C to +70°C	Logic Inputs	V_{EE} to V_{EE} + 36V
Storage Temperature Range	–65°C to +150°C	Summing Junction (Pin 4)	V_{EE} to V_{CC}
Power Dissipation	500mW	CMOS/TTL Threshold (Pin 2)	V_{EE} to V_{CC}
Derate above 100°C	10mW/°C	I_{OUT} (Pin 9)	+18 to –12V
Lead Soldering Temperature	300°C (60 sec)	Span Resistors	36V

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, V_{REF} = +10.0000V, T_A = +25°C, unless otherwise specified.

			SSS562SD			SSS562AD			SSS562KD			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution (Binary Models)		T_A = Full	12	12	12	12	12	12	12	12	12	Bits
Monotonicity (Binary Models)		T_A = Full	12	—	—	12	—	—	12	—	—	Bits
Nonlinearity (Binary Models)	NL		—	—	±1/4	—	—	±1/2	—	—	±1/2	LSB
Resolution (BCD Models)		T_A = Full	3	3	3	3	3	3	3	3	3	Digits
Monotonicity (BCD Models)		T_A = Full (999 Steps)	3	—	—	3	—	—	3	—	—	Digits
Nonlinearity (BCD Models)	NL		—	—	±1/10	—	—	±1/2	—	—	±1/2	LSB
Settling Time	t_s	To ±1/2 LSB, All bits ON or OFF, current into short circuit.	—	—	1.5	—	—	1.5	—	—	1.5	µsec
Major Carry Switching Transient		To 90% complete	—	200	—	—	200	—	—	200	—	nsec
Voltage Noise (All bits ON)	E_n	0.1Hz to 10Hz	—	30	—	—	30	—	—	30	—	µVp-p
Output Voltage Compliance	V_{OC}		–2.5	—	+10	–2.5	—	+10	–2.5	—	+10	V
Output Current Range		Unipolar (0 to –2mA)	—	±10	—	—	±10	—	—	±10	—	%
		Bipolar (–1mA to +1mA)	—	±10	—	—	±10	—	—	±10	—	%
Output Resistance			—	2.0	—	—	2.0	—	—	2.0	—	MΩ
Output Capacitance			—	30	—	—	30	—	—	30	—	pF
Zero Scale Current	I_{ZS}	All bits OFF	—	—	0.01	—	—	0.01	—	—	0.01	%FS
Logic Inputs –TTL, V_{CC} = +5V, Pin 2 Open Circuit	V_{IH}	I_{IN} = 100nA (Max)	2.0	—	—	2.0	—	—	2.0	—	—	V
	V_{IL}	I_{IN} = –100µA (Max)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Inputs –CMOS, 4.75V ≤ V_{CC} ≤ 15.8V, Pin 2 to Pin 1	V_{IH}	I_{IN} = 100nA (Max)	70	—	—	70	—	—	70	—	—	% V_{CC}
	V_{IL}	I_{IN} = –100µA (Max)	—	—	30	—	—	30	—	—	30	% V_{CC}
Reference Voltage Input	Z_{IN}	20KΩ (Nominal)	—	±10	—	—	±10	—	—	±10	—	%
	V_{RR}	Range (Nominal)	0	—	±10	0	—	±10	0	—	±10	V
External Adjustment Range		(See following page)	—	±0.25	—	—	±0.25	—	—	±0.25	—	%
Power Supply Range	V+	I_+ = 10mA (Typ)	4.75	—	15.8	4.75	—	15.8	4.75	—	15.8	V
	V–	I_- = –15mA (Typ)	–16.5	—	–13.5	–16.5	—	–13.5	–16.5	—	–13.5	V
Power Supply Sensitivity of Gain		V+ = +5V	—	—	1.0	—	—	1.0	—	—	1.0	ppmFS/%
		V+ = +15V	—	—	1.0	—	—	1.0	—	—	1.0	ppmFS/%
		V– = –15V	—	—	2.0	—	—	2.0	—	—	2.0	ppmFS/%
The following specifications apply for V_S = ±15V, V_{REF} = +10.0000V, –55°C ≤ T_A ≤ +125°C for SSS562SD, –25°C ≤ T_A ≤ +85°C for SSS562AD, 0°C ≤ T_A ≤ +70°C for SSS562KD, unless otherwise specified.												
Zero Scale Temperature Coefficient	TC_{ZS}	Leakage Current	—	—	2.0	—	—	1.0	—	—	1.0	ppmFS /°C
Bipolar Offset Temperature Coefficient			—	—	4.0	—	—	4.0	—	—	4.0	ppmFS /°C
Gain Temperature Coefficient		Excludes V_{REF}	—	—	3.0	—	—	3.0	—	—	3.0	ppmFS /°C
Differential Nonlinearity Temperature Coefficient			—	2.0	—	—	2.0	—	—	2.0	—	ppmFS /°C

MULTIPLYING ELECTRICAL CHARACTERISTICS AT T_A = +25°C (ALL MODELS)

Parameter	Description	Typ	Units
Quadrants	Two-quadrant: bipolar operation is achieved using the digital inputs only.	–	–
Reference Voltage	Unipolar. Digital input multiplies reference voltage.	0 to +10	V
Accuracy	10 bits for reduced reference voltage of +1V.	±0.05	%FS
Reference Feedthrough (Unipolar Mode)	All bits OFF, 0 to +10V (p-p) sinewave frequency for 1/2 LSB (p-p) feedthrough.	2.0	KHz
Output Slew Rate	All bits ON, 10V step change in reference voltage.	1.0	mA/μsec
Output Settling Time	All bits ON, 10V step change in reference voltage, to ±0.01% FS.	5.0	μsec
Reference Amplifier Bandwidth	Closed loop, small signal.	1.0	MHz

ADJUSTMENT PROCEDURES AND TABLE

BIPOLAR OFFSET

With all bits OFF, adjust R1 until op amp output is –2.5V on ±2.5V range, –5.0V on ±5.0V range, or –10.0V on ±10.0V range.

UNIPOLAR OFFSET

With all bits OFF, adjust R4 until op amp output is 0V. R1 and the connection from pin 8 to pin 9 are not required.

BIPOLAR BCD GAIN

Turn bits 2 and 4 ON, Turn bits 1, 3, 5 through 12 OFF. Adjust R2 until op amp output is 0V.

BIPOLAR BINARY GAIN

Turn bit 1 (MSB) ON. Turn bits 2 through 12 OFF. Adjust R2 until output is 0V.

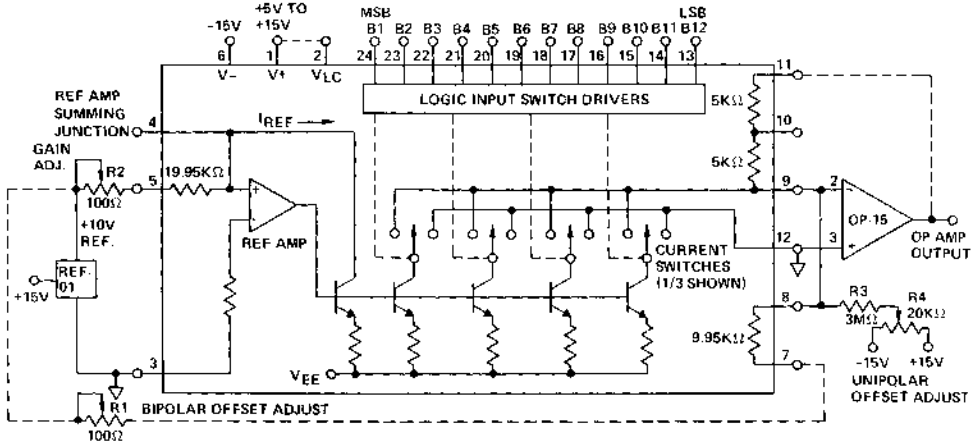
UNIPOLAR BCD GAIN

Turn bits 1, 4, 5, 8, 9, 12 ON (Code 1001 1001 1001, BCD 999). Adjust R2 until op amp output is +4.995V for 0 to +5.0V range, or +9.990V for 0 to +10.0V range.

UNIPOLAR BINARY GAIN

Turn all bits ON. Adjust R2 until op amp output is +4.9988V for 0 to +5.0V range, or +9.9976V for 0 to +10.0V range.

RANGE	OP AMP	CONNECTIONS	OFFSET ADJUST
–2.5V to +2.5V	Out to Pin 10	Pin 11 to Pin 9	R1 as below
–5.0V to +5.0V	Out to Pin 10	N.C. to Pin 11	R1 as below
–10.0V to +10.0V	Out to Pin 11	N.C. to Pin 10	R1 as below
0 to +5.0V	Out to Pin 10	Pin 11 to Pin 9	R4 as below
0 to +10.0V	Out to Pin 10	N.C. to Pin 11	R4 as below



NOTES: 1. FOR TTL AND DTL INPUTS, CONNECT +5V TO PIN 1; PIN 2 MAY BE GROUNDED OR LEFT OPEN.
2. FOR LOW VOLTAGE CMOS, CONNECT +5V TO PIN 1; SHORT PIN 2 TO PIN 1.
3. FOR HIGH VOLTAGE CMOS, CONNECT +15V TO PIN 1; SHORT PIN 2 TO PIN 1.

SSS1508A/1408A

8 BIT MULTIPLYING D/A CONVERTER

GENERAL DESCRIPTION

The SSS1508A/1408A are 8 bit monolithic multiplying Digital-to-Analog Converters consisting of a reference current amplifier, an R-2R ladder, and eight high speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full scale output current of 1.992 mA would result from a reference input current of 2.0mA.

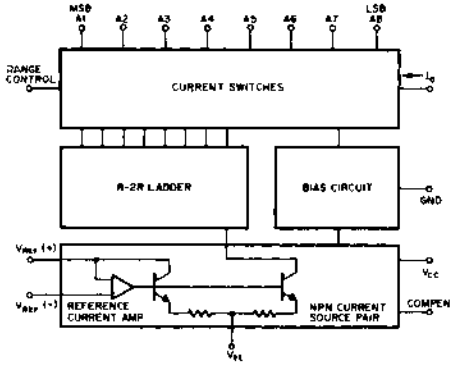
The SSS1508A/1408A is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building Tracking and Successive Approximation Analog-to-Digital Converters.

FEATURES

- **Improved Direct Replacement For MC1508/MC1408**
- **0.19% Nonlinearity Max Over Temperature Range**
- **Improved Settling Time . . . . . 250 nsec, Typ.**
- **Improved Power Consumption . . . . . 157 mW, Typ.**
- **Compatible With TTL, CMOS Logic**
- **Standard Supply Voltages +5.0V and −5.0V to −15V**
- **Output Voltage Swing . . . . . +0.5V to −5.0V**
- **High Speed Multiplying Input . . . . . 4.0 mA/μsec**

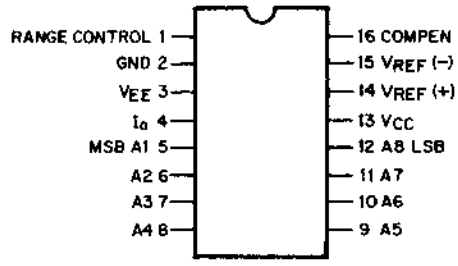
For significantly improved speed and applications flexibility the user's attention is directed to the DAC-08 8 bit High Speed Multiplying D/A Converter data sheet. For D/A converters which include precision voltage references on the chip please refer to the DAC-02, DAC-04 and DAC-100 data sheets.

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE	RELATIVE ACCURACY
SSS1508A-8Q	−55/+125°C	± 0.19%
SSS1408A-8Q	0/+75°C	± 0.19%
SSS1408A-7Q	0/+75°C	± 0.39%
SSS1408A-6Q	0/+75°C	± 0.78%

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: SSS1508A-883-8Q

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

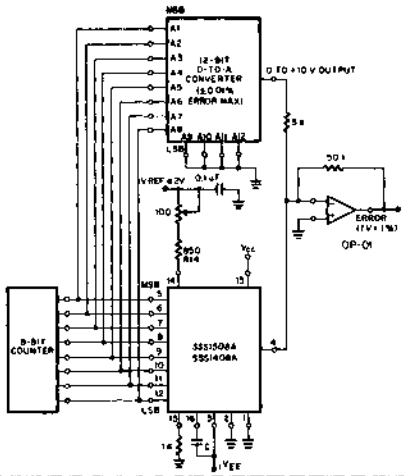
Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+5.5 −16.5	Vdc Vdc
Digital Input Voltage	V_5 thru V_{12}	+5.5,0	Vdc
Applied Output Voltage	V_O	+0.5,−5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{CC}, V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range SSS1508A-8 SSS1408A	T_A	 −55 to +125 0 to +75	 °C °C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{Vref}{R14}$ = 2.0 mA, SSS1508A-8: T_A = −55°C to +125°C, SSS1408A T_A = 0°C to +75°C unless otherwise noted. All digital inputs at high logic level.)

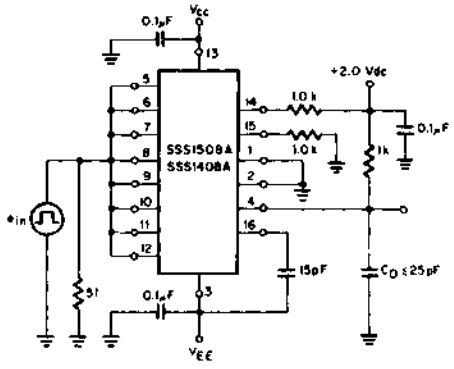
Parameter	Conditions	Symbol	Min	Typ	Max	Units
Relative Accuracy (Error relative to full scale I_{O_i}) SSS1508A-8, SSS1408A-8 SSS1408A-7 SSS1408A-6		E_r	 – – –	 – – –	 ±0.19 ±0.39 ±0.78	 % IFS % IFS % IFS
Settling Time to within 1/2 LSB (includes t_{PLH})	(T_A = +25°C)	t_S	–	250	–	ns
Propagation Delay Time	T_A = +25°C	t_{PLH},t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	±20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"		 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	 Vdc Vdc
Digital Input Current (MSB)	High Level, V_{IH} = 5.0V Low Level, V_{IL} = 0.8V	I_{IH} I_{IL}	– –	0 −0.4	0.04 −0.8	mA mA
Reference Input Bias Current (Pin 15)		I_{15}	–	−1.0	−3.0	μA
Output Current Range	V_{EE} = −5.0V V_{EE} = −6.0 to −15V	I_{OR}	0 0	2.0 2.0	2.1 4.2	mA mA
Output Current	V_{ref} = 2.000V, R14 = 1000Ω	I_O	1.9	1.99	2.1	mA
Output Current (All bits low)		$I_{O(min)}$	–	0	4.0	μA
Output Voltage Compliance (E_r ≤ 0.19% at T_A = +25°C)	I_{ref} = 1mA V_{EE} = −5 V_{EE} below −10V	V_O	– –	– –	−0.6, +0.5 −5.0, +0.5	Vdc Vdc
Reference Current Slew Rate		SRI_{ref}	–	4.0	–	mA/μs
Output Current Power Supply Sensitivity		$PSSI_{O-}$	–	0.5	2.7	μA/V
Power Supply Current	(All bits low)	I_{CC} I_{EE}	– –	+9 −7.5	+14 −13	mA mA
Power Supply Voltage Range	(T_A = +25°C)	V_{CCR} V_{EER}	+4.5 −4.5	+5.0 −15	+5.5 −16.5	Vdc Vdc
Power Dissipation All bits low V_{EE} = −5.0 Vdc V_{EE} = −15 Vdc All bits high V_{EE} = −5.0 Vdc V_{EE} = −15 Vdc		P_d	 – – – –	 82 157 70 132	 135 265 – –	 mW mW mW mW

APPLICATIONS

RELATIVE ACCURACY TEST CIRCUIT

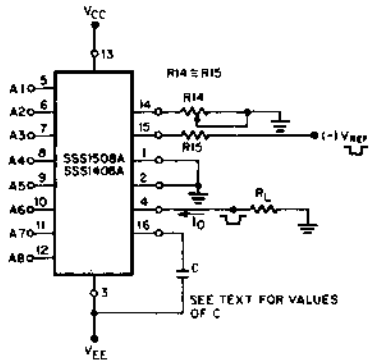


TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT

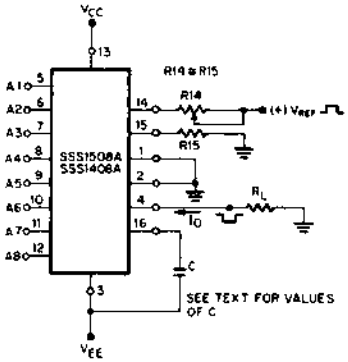


*t_D FOR SETTLING TIME MEASUREMENT. (ALL BITS SWITCHED LOW TO HIGH)

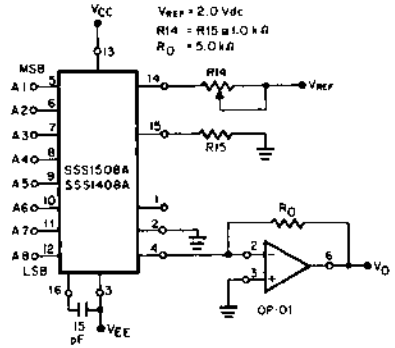
USE WITH NEGATIVE V_{REF}



USE WITH POSITIVE V_{REF}



USE WITH CURRENT–TO–VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

ADJUST V_{REF}, R14 OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS.

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive voltage are shown on page 3. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to +0.5 volts when V_{EE} = −5V due to the current switching methods employed in the SSS1508A-8.

The negative output voltage compliance of the SSS1508A-8 is extended to −5.0V volts where the negative supply voltage is more negative than −10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7.0 volts, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the SSS1508A-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the SSS1508A-8 has a very low full scale current drift with temperature.

The SSS1508A-8/SSS1408A Series is guaranteed accurate to within ±1/2 LSB at a full scale output current of 1.992 mA. This coresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB (8.0 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown on page 3. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the SSS1508A-8 accuracy is essentially the same between 1.5 and 2.5 mA. Then the SSS1508A-8 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the SSS1508A-8.

MULTIPLYING ACCURACY

The SSS1508A-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the additional error contributions are less than 1.6 μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the SSS1508A-8 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 250 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250 ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

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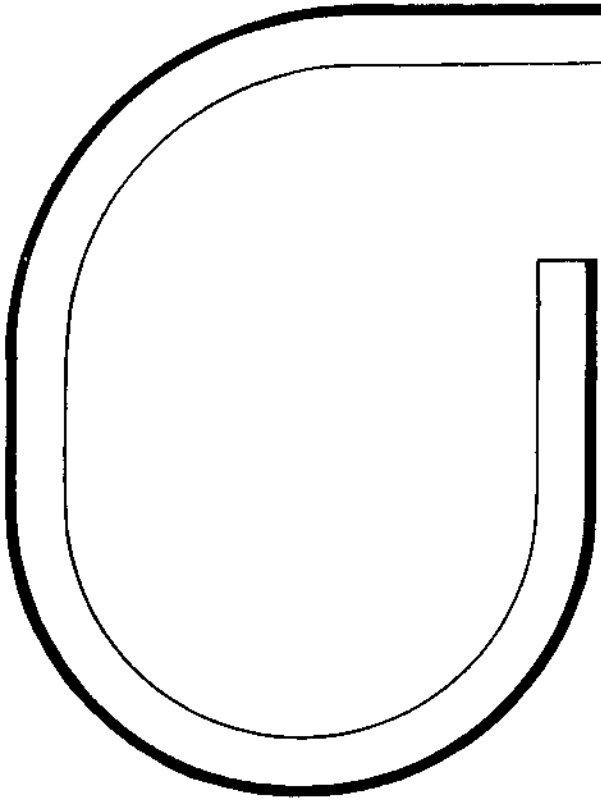

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D/A CONVERTERS – COMPANDING

PRODUCT	TITLE	PAGE
DAC-76	COMDAC™ Companding D/A Converter	11-1

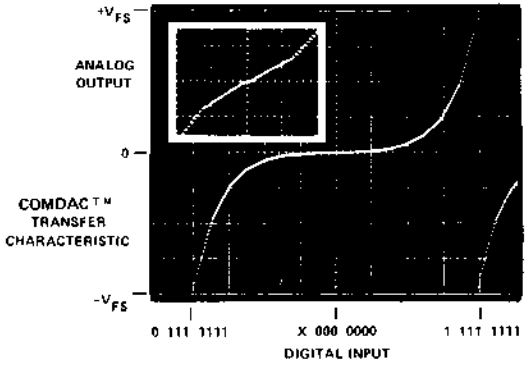
DAC-76

COMDAC™ COMPANDING D/A CONVERTER

MONOLITHIC LOGARITHMIC DAC

FEATURES

- Sign Plus 12 Bit Range With Sign Plus 7 Bit Coding
- 12 Bit Accuracy and Resolution Around Zero
- Sign Plus 72dB Dynamic Range
- True Current Outputs: –5V to +18V Compliance
- Tight Full Scale Tolerance Eliminates Calibration
- Low Full Scale Drift Over Temperature
- Conforms With Bell System μ-255 Companding Law
- Multiplying Reference Inputs
- Low Power Consumption and Low Cost
- Ideal for PCM, Audio, and 8 Bit μP Applications
- Outputs Multiplexed for Time Shared Applications

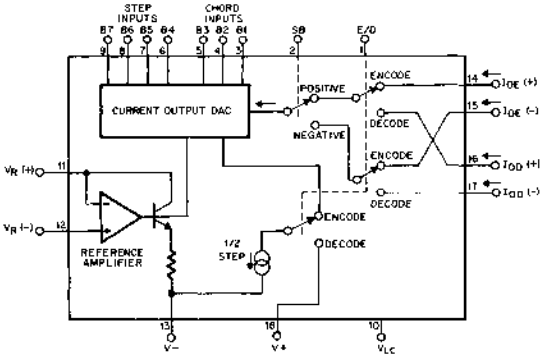


GENERAL DESCRIPTION

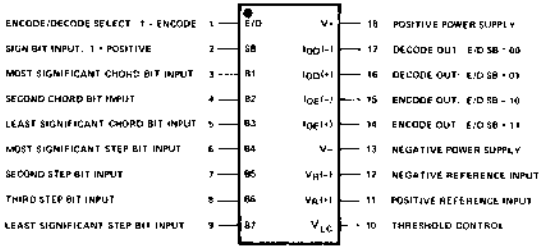
The DAC-76 monolithic COMDAC™ D/A Converter provides the dynamic range of a sign + 12-bit DAC in a sign + 7-bit format. A companding (compression/expansion) transfer function is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. Accuracy is assured by specifying chord end point values, chord nonlinearity, and monotonicity over the full operating temperature range.

The 8-bit format with a sign + 72dB dynamic range is especially useful in control systems using 8-bit microprocessors, RAM's and ROM's. Low distortion multiplying capability and conformance with the Bell System μ-255 logarithmic law for PCM transmission make the DAC-76 ideal for use in audio applications. Other applications include servo controls, stress and vibration analysis, digital recording and speech synthesis. Additional applications are listed on the last page.

EQUIVALENT CIRCUIT



ORDERING INFORMATION AND PIN CONNECTIONS



TOP VIEW

18 PIN HERMETIC DUAL-IN-LINE (X-Suffix)

MODEL	TEMP RANGE	ACCURACY
DAC-76BX	–55°/+125°C	±1/2 STEP
DAC-76X	–55°/+125°C	±1 STEP
DAC-76EX	0°/+70°C	±1/2 STEP
DAC-76CX	0°/+70°C	±1 STEP

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

DAC76-883-BX
DAC76-883-X

COMPANDING PRINCIPLES

BACKGROUND

Companding or signal compression and signal expansion is widely used. In FM broadcasting companding is performed by de-emphasis and pre-emphasis. In analog systems companding is performed by log and antilog amplifiers. But in data conversion and transmission, companding has been limited to the telecommunications industry. They recognized the need to efficiently represent analog signals with the fewest possible number of digital bits. With just 8 bits, the standard format of microprocessors, RAM's, ROM's and registers, telecommunications companding systems achieve very low signal-to-quantizing distortion over a 40dB range of speech amplitudes by using the Bell System μ-255 logarithmic companding law.

BELL μ-255 LOGARITHMIC CHARACTERISTIC

The output of the DAC-76 is an approximation to the μ-255 law which can be expressed as:

$Y = 0.18 \ln (1 + \mu x)$ where:

X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS} with values from −1 to +1.

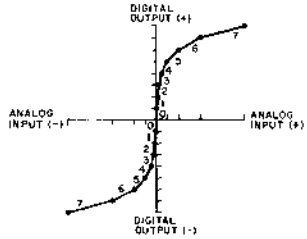
Y = Output signal level of the encoder

μ = 255

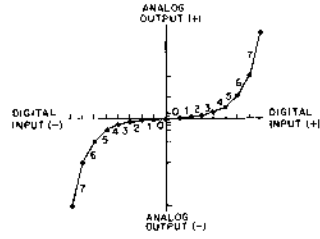
This law is implemented by the DAC-76 with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. A dynamic range of 72dB in both polarities is achieved with 8 bit coding.

TRANSFER CHARACTERISTICS

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



The system transfer characteristics above result when the DAC-76 is used for signal compression (A/D conversion) and for signal expansion (D/A conversion). As one would expect, when the curves are superimposed their average is a straight line because compression and expansion must be equal and opposite.

Both transfer characteristics show outputs divided into 8 chords in both polarities with 16 equal steps in each chord. Note that each chord endpoint is approximately 6dB down from the next higher chord's endpoint and that the chord slopes are binarily-related.

The table below relates step size in each chord to other commonly-encountered measurements and to the equivalent, conventional, binary-coded DAC. Step size (except in Chord 0) is about 0.3dB and is an almost constant percentage of reading. In addition, there is a 1 1/2 step change between the maximum code in each chord and the minimum code in the next chord to smooth the chord transitions and to conform with existing telecommunication specifications.

The following three pages contain electrical specifications, the DC test circuit, tables of ideal chord endpoint currents for both encode and decode modes, and parameter definitions.

STEP SIZE SUMMARY TABLE DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE IN μA WITH 2007.75 μA F.S.	STEP SIZE AS A % OF FULL SCALE	STEP SIZE IN dB AT CHORD ENDPOINTS	STEP SIZE AS A % OF READING AT CHORD ENDPOINTS	RESOLUTION & ACCURACY OF EQUIVALENT BINARY DAC
0	2	0.5	0.025%	0.60	6.67%	SIGN + 12 BITS
1	4	1.0	0.05%	0.38	4.30%	SIGN + 11 BITS
2	8	2.0	0.1%	0.32	3.65%	SIGN + 10 BITS
3	16	4.0	0.2%	0.31	3.40%	SIGN + 9 BITS
4	32	8.0	0.4%	0.29	3.28%	SIGN + 8 BITS
5	64	16	0.8%	0.28	3.23%	SIGN + 7 BITS
6	128	32	1.6%	0.28	3.20%	SIGN + 6 BITS
7	256	64	3.2%	0.28	3.19%	SIGN + 5 BITS

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 528 μA, −55°C ≤ T_A ≤ +125°C, and for all 4 outputs unless otherwise specified.

Note. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5 μA, while in the last chord near full scale (C_7) step size is 64 μA.

			DAC-76B			DAC-76			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or −	128	–	–	128	–	–	Steps
Chord Endpoint Accuracy		Error relative to ideal values at I_{FS} = 2007.75μA	–	–	+1/2	–	–	±1	Step
Step Nonlinearity		Step error within chord	–	–	±1/2	–	–	±1	Step
Encode Current		Additional Output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time	t_S	To within ±1/2 step	–	500	–	–	500	–	nsec
Full Scale Drift	ΔI_{FS}	Full Temperature Range	–	±1/20	±1/4	–	±1/10	±1/2	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤ 1/2 step	−5	–	+18	−5	–	+18	Volts
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$ $I_{FS}(E)$	V_{REF} = 10.000V T_A=25°C R11 = 18.94 kΩ R12 20 kΩ	– –	– –	±1/2 ±1/2	– –	– –	±1 ±1	Step Step
Full Scale Symmetry Error	$I_O(+)-I_O(-)$	Decode or Encode Pair	–	±1/40	±1/8	–	±1/20	±1/4	Step
Zero Scale Current	I_{ZS}	Measured at Selected Output with 000 0000 Input	–	1/40	1/4	–	1/20	1/2	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/D and SB	–	5.0	50	–	5.0	50	nA
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = 0V	 – 2.0	 – –	 0.8 –	 – 2.0	 – –	 0.8 –	 Volts Volts
Logic Input Current	I_{IN}	V_{IN} = −5V to +18V	–	–	40	–	–	40	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	–	+18	−5	–	+18	Volts
Reference Bias Current	I_{12}		–	−1.0	−4.0	–	−1.0	−4.0	μA
Reference Input Slew Rate	dI/dt		–	0.25	–	–	0.25	–	mA/μsec
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+=4.5 to 18V, V−=−15V V−=−10.8V to −18V, V+=15V	– –	±1/20 ±1/10	±1/2 ±1/2	– –	±1/20 ±1/10	±1/2 ±1/2	Step Step
Power Supply Current	I+ I−	V_S=+5V, −15V, I_{FS}=2.0 mA	– –	2.7 −6.7	4.0 −8.8	– –	2.7 −6.7	4.0 −8.8	mA mA
Power Supply Current	I+ I−	V_S = ±15V, I_{FS} = 2.0 mA	– –	2.7 −6.7	4.0 −8.8	– –	2.7 −6.7	4.0 −8.8	mA mA
Power Dissipation	P_D	V_S=+5V,−15V, I_{FS}=2.0mA V_S=±15V, I_{FS}=2.0mA	– –	114 141	152 192	– –	114 141	152 192	mW mW

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 528 µA, 0°C ≤ T_A ≤ +70°C, and for all 4 outputs unless otherwise specified.

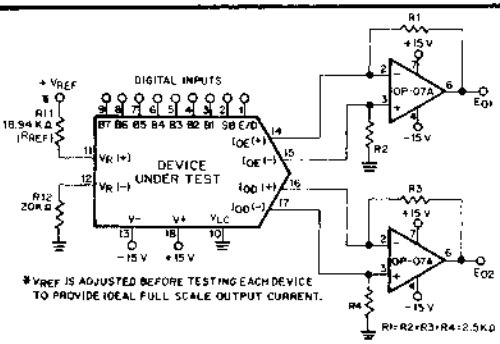
Note: In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5 µA, while in the last chord near full scale (C_7) step size is 64 µA.

			DAC-76E			DAC-76C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or –	128	–	–	128	–	–	Steps
Chord Endpoint Accuracy		Error relative to ideal values at I_{FS} = 2007.75µA	–	–	±1/2	–	–	±1	Step
Step Nonlinearity		Step error within chord	–	–	±1/2	–	–	±1	Step
Encode Current		Additional Output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time	t_s	To within ±1/2 step	–	500	–	–	500	–	nsec
Full Scale Drift	ΔI_{FS}	Full Temperature Range	–	+1/20	±1/4	–	±1/10	±1/2	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤ 1/2 step	–5	–	+18	–5	–	+18	Volts
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$ $I_{FS}(E)$	V_{REF} = 10.000V T_A=25°C R11 = 18.94 kΩ R12 = 20 kΩ	– –	– –	±1/2 ±1/2	– –	– –	±1 ±1	Step Step
Full Scale Symmetry Error	$I_O(+)-I_O(-)$	Decode or Encode Pair	–	±1/40	±1/8	–	±1/20	±1/4	Step
Zero Scale Current	I_{ZS}	Measured at Selected Output with 000 0000 Input	–	1/40	1/4	–	1/20	1/2	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/D and SB	–	5.0	50	–	5.0	50	nA
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = 0V	 – 2.0	 – –	 0.8 –	 – 2.0	 – –	 0.8 –	 Volts Volts
Logic Input Current	I_{IN}	V_{IN} = –5V to +18V	–	–	40	–	–	40	µA
Logic Input Swing	V_{IS}	V– = –15V	–5	–	+18	–5	–	+18	Volts
Reference Bias Current	I_{12}		–	–1.0	–4.0	–	–1.0	–4.0	µA
Reference Input Slew Rate	dI/dt		–	0.25	–	–	0.25	–	mA/µsec
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5 to 18V, V– = –15V V– = –10.8V to –18V, V+ = 15V	– –	±1/20 ±1/10	–1/2 ±1/2	– –	±1/20 ±1/10	+1/2 ±1/2	Step Step
Power Supply Current	I+ I–	V_S = +5V, –15V, I_{FS} = 2.0 mA	– –	2.7 –6.7	4.0 –8.8	– –	2.7 –6.7	4.0 –8.8	mA mA
Power Supply Current	I+ I–	V_S = ±15V, I_{FS} = 2.0 mA	– –	2.7 –6.7	4.0 –8.8	– –	2.7 –6.7	4.0 –8.8	mA mA
Power Dissipation	P_D	V_S = +5V, –15V, I_{FS} = 2.0mA V_S = ±15V, I_{FS} = 2.0mA	– –	114 141	152 192	– –	114 141	152 192	mW mW

ABSOLUTE MAXIMUM RATINGS

V+ Supply to V– Supply	36V	Operating Temperature	
V_{LC} Swing	V– plus 8V to V+	DAC-76B, DAC-76	–55°C to +125°C
Analog Current Outputs	V– plus 8V to V– plus 36V	DAC-76E, DAC-76C	0°C to +70°C
Reference Inputs	V– to V+	Storage Temperature	–65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation	500mW
Reference Input Current	1.25 mA	Derate above 100°C	10mW/°C
Logic Inputs	V– plus 8V to V– plus 36V	Lead Soldering Temperature	300°C (60 sec)

OUTPUT CURRENT DC TEST CIRCUIT



*VREF IS ADJUSTED BEFORE TESTING EACH DEVICE TO PROVIDE IDEAL FULL SCALE OUTPUT CURRENT.

LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	I_{OE} (+)	(E_{O1}/R1)
2	1	0	I_{OE} (–)	(E_{O1}/R2)
3	0	1	I_{OD} (+)	(E_{O2}/R3)
4	0	0	I_{OD} (–)	(E_{O2}/R4)

NOTE:—Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

SPECIFICATION PARAMETER DEFINITIONS

STEP NONLINEARITY: Step size deviation from ideal within a chord.

ENCODE CURRENT: The difference between I_{OE}(+) and I_{OD}(+) or the difference between I_{OE}(–) and I_{OD}(–) at any code.

FULL SCALE DRIFT: The change in output current over the full operating temperature with V_{REF} = 10.000V, R11 = 18.94KΩ, and R12 = 20KΩ.

FULL SCALE SYMMETRY ERROR: The difference between I_{OD}(–) and I_{OD}(+) or the difference between I_{OE}(–) and I_{OE}(+) at full scale output.

OUTPUT VOLTAGE COMPLIANCE: The maximum output voltage swing at any current level which causes <1/2 step change in output current.

CHORDS: Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS: The maximum code in each chord. Used to specify accuracy.

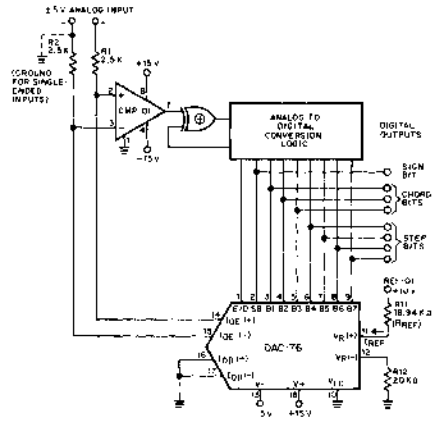
STEPS: Increments in each chord which divide it into 16 equal levels.

OUTPUT LEVEL NOTATION: Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

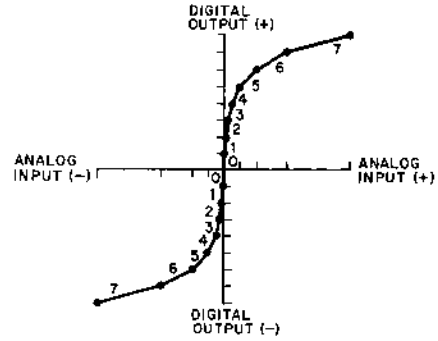
DYNAMIC RANGE: Ratio of the largest output ($I_{7,15}$) to the smallest output excluding zero ($I_{0,1}$) expressed in dB. This can be measured peak or peak-to-peak with the same result.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-76 requires a comparator, an exclusive-or gate, and a successive approximation register—the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one significant difference from regular A/D converters.

In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale. The standard 1/2 step bias used in conventional ADC's to keep quantizing error below ±1/2 step cannot be easily furnished by the user of a compressing ADC. For this reason, the DAC has a 1/2 step greater output in the encode mode than it has in the decode mode. This may be seen clearly by comparing the normalized encode and decode output tables at any code point.

ENCODING SEQUENCE

An encoding sequence begins with the Sign Bit comparison and decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". Therefore, no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-or gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. (A more complete schematic is shown in the applications section.)

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made. Successive removal is necessary because the 1/2 step encode decision level current is drawn from the sum node, rather than sourced into it.

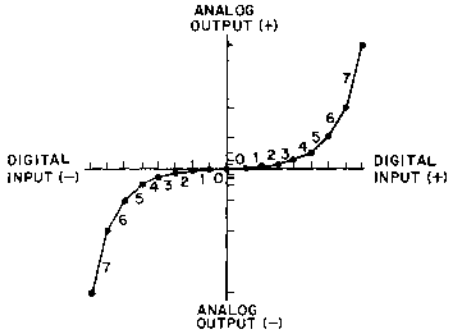
NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S+17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

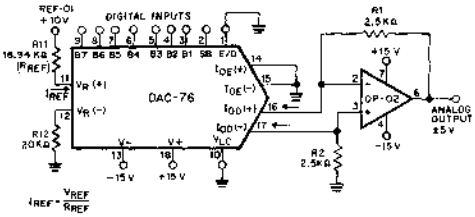
STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



BASIC DECODE CONNECTIONS



	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_O
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	−5.019V

DECODE OPERATION

D/A conversion with the DAC-76 may be illustrated by using an operational amplifier connected to the decode outputs as a balanced load. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

The encode and decode tables may be used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 times I_{FS} of 2007.75μA equals 85.75μA. Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode it is 2039.75μA because the additional 1/2 step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4KΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

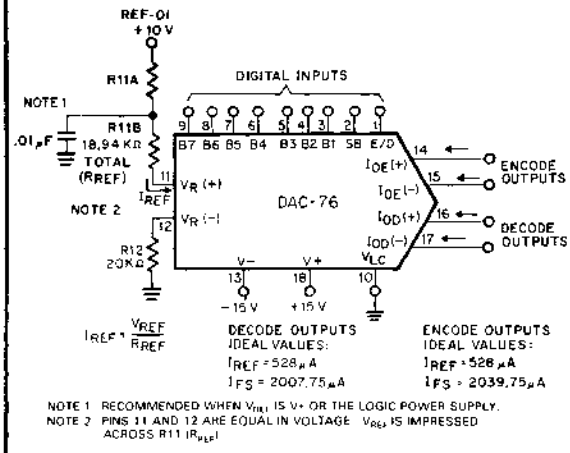
$I_{C,S} = 2|2^C (S+16.5) - 16.5|$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

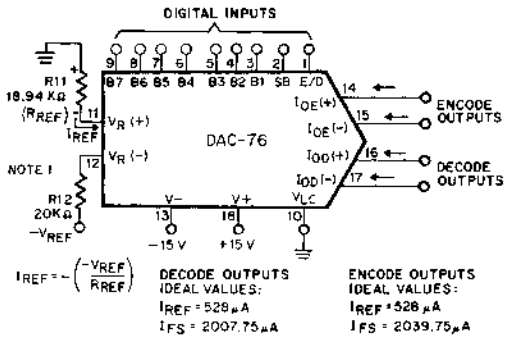
REFERENCE AMPLIFIER OPERATION

POSITIVE REFERENCE OPERATION



NOTE 1 RECOMMENDED WHEN V_{IN+} IS V+ OR THE LOGIC POWER SUPPLY.
NOTE 2 PINS 11 AND 12 ARE EQUAL IN VOLTAGE V_{REF} IS IMPRESSED ACROSS R11 (R_{REF})

NEGATIVE REFERENCE OPERATION



NOTE 1 PINS 11 AND 12 ARE EQUAL IN VOLTAGE V_{REF} IS IMPRESSED ACROSS R11 (R_{REF})

REFERENCE AMPLIFIER SETUP

The DAC-76 is a multiplying D/A converter in which the output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

In positive reference applications an external positive reference voltage forces current through R11 into the $V_R(+)$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at pin 12; reference current flows from ground through R11 into $V_R(+)$, as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

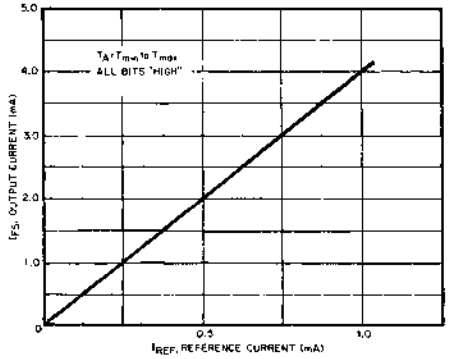
REFERENCE RECOMMENDATIONS

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full scale temperature coefficient performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}.) For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}; but if desired, full scale trimming may be accomplished by selecting R11 or by using a potentiometer for R11.

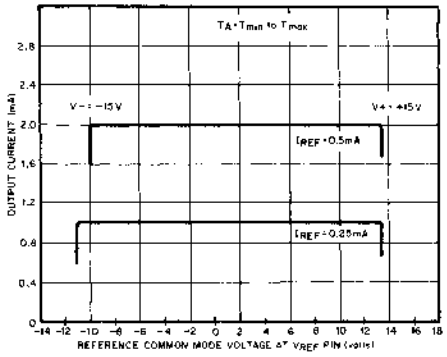
Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. While the recommended operating range of DC reference currents is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range allowing the DAC-76 to be used in many multiplying applications. For variable reference applications, see section entitled "Multiplying Operation."

TYPICAL PERFORMANCE CURVES

OUTPUT FULL SCALE CURRENT VS. REFERENCE INPUT CURRENT



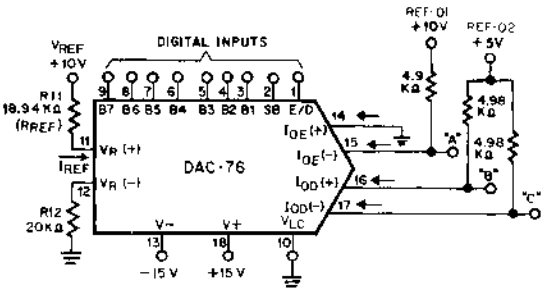
REFERENCE AMPLIFIER INPUT COMMON MODE RANGE



NOTE: POSITIVE COMMON MODE RANGE IS ALWAYS (V+) − 1.5 V

TRUE CURRENT OUTPUT OPERATION

RESISTIVE OUTPUT CONNECTIONS



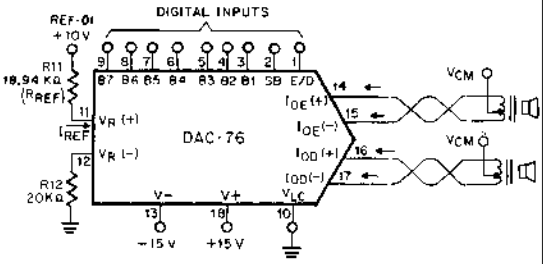
INPUT CODE	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
11 111 1111	0			
11 110 1111	+5.02	N/A	N.A	N.A
11 000 0000	+10.00			
01 111 1111		-5.00	-5.00	-10
01 110 1111		+0.02	+5.00	-4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	-0.02	+4.98
00 111 1111		+5.00	-5.00	+10

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V− / IFS	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE
$V_{OC}(-)\ MIN = IV-I+12I_{REF} \cdot 1.6K\Omega) + 8.4V$

BALANCED LOAD CONNECTIONS



TYPICAL BALANCED LOADS

- TRANSFORMER
- TRANSDUCER
- EARPHONE
- SAMPLE AND HOLD
- CURRENT INPUT FILTER
- TRANSMISSION LINE
- DAC REFERENCE INPUT
- BRIDGE
- OP AMP
- CRT
- SERVO

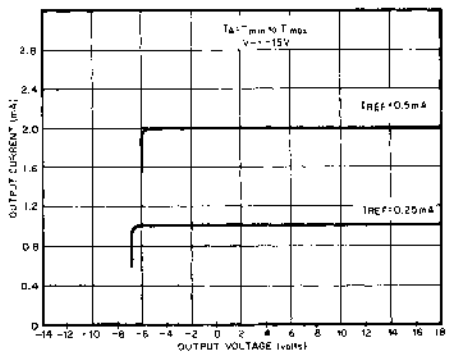
NOTE: THE SUM OF THE COMMON MODE VOLTAGE AND THE DIFFERENTIAL VOLTAGE ACROSS THE LOAD SHOULD BE WITHIN THE -5V TO +18V OUTPUT VOLTAGE COMPLIANCE SPECIFICATION

The DAC-76 has true current outputs with wide voltage compliance enabling fast drive of a variety of single-ended and balanced loads. Positive voltage compliance is +18V, and negative voltage compliance is −5.0V with I_{REF} = 528μA and V− = −15V. Negative voltage compliance for other values of I_{REF} and V− may be calculated using the table above. Typical connections, both single-ended and differential, are shown in the figure above with output voltage tables. Note the differential sign-plus-magnitude relationship between "B" and "C". The differential output voltage is independent of the +5.00 nominal voltage source as long as the $V_{OC}(-)$ minimum values are observed.

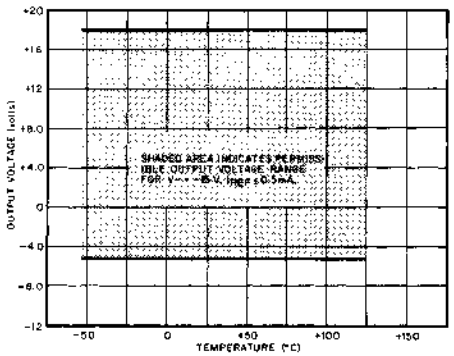
High common mode output range is possible due to the wide output voltage compliance and allows use with transformers or other balanced loads. The terminating impedances may be located a distance away from the DAC-76 allowing transmission of analog quantities as currents rather than voltages and elimination of ground loop errors. Capacitive termination is also possible, performing an "integrate-and-hold" process which is a function of V_{REF}, R_{REF}, the digital input code, and the selection time for a given current output. Resetting of the integrating capacitor may be accomplished with a CMOS switch in parallel with the capacitor. Thus, many applications traditionally requiring op amps may be performed with a high voltage compliance, current output DAC.

TYPICAL PERFORMANCE CURVES

OUTPUT CURRENT VS. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

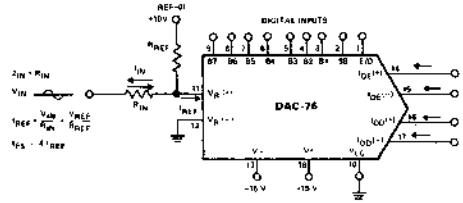


OUTPUT VOLTAGE COMPLIANCE VS. TEMPERATURE

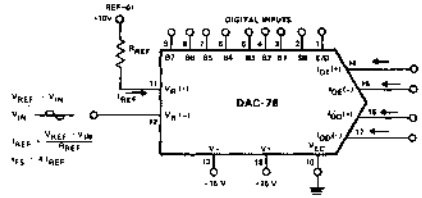


MULTIPLYING OPERATION

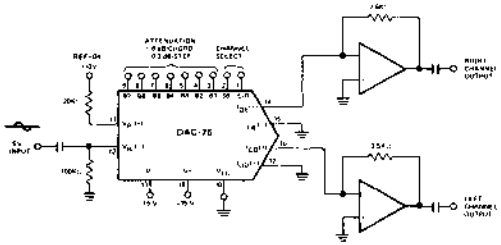
LOW INPUT IMPEDANCE CONNECTION



HIGH INPUT IMPEDANCE CONNECTION

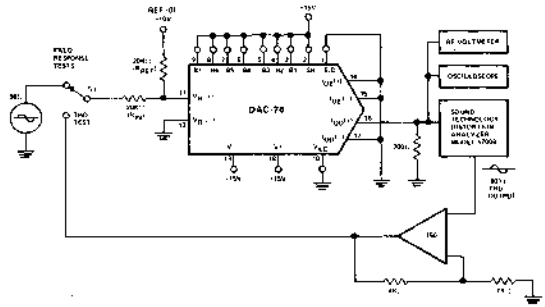


LOGARITHMIC DIGITAL GAIN CONTROL



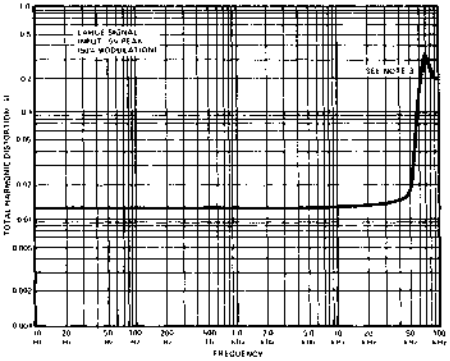
NOTE 1: LOW DISTORTION OUTPUTS ARE PROVIDED OVER A 72dB RANGE
NOTE 2: UP TO 4 CHANNELS OF OUTPUT MAY BE SELECTED BY E/D AND SB LOGIC INPUTS.

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



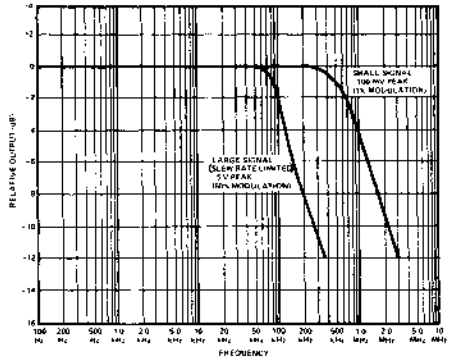
TYPICAL PERFORMANCE CURVES

REFERENCE AMPLIFIER TOTAL HARMONIC DISTORTION VS. FREQUENCY (80 KHz FILTER)



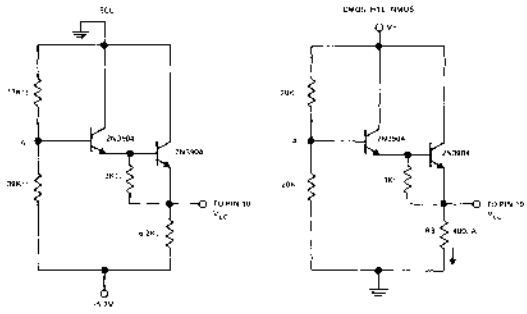
NOTE 1: THD IS NEARLY INDEPENDENT OF LOGIC INPUT CODE
NOTE 2: SIMILAR RESULTS ARE OBTAINED FOR A HIGH INPUT IMPEDANCE CONNECTION USING PIN 12 AS AN INPUT
NOTE 3: INCREASED DISTORTION ABOVE 50kHz IS DUE TO SLEW RATE LIMITING WHICH DETERMINES LARGE SIGNAL BANDWIDTH. FOR AN INPUT OF ±2.5V PEAK (25% MODULATION), BANDWIDTH IS 100kHz.

REFERENCE AMPLIFIER INPUT FREQUENCY RESPONSE



LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, & NMOS LOGIC INPUTS



NOTE 1: SET THE VOLTAGE 'A' TO BE AT THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
NOTE 2: ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY +5V TO +13.5V WHEN OPERATING THE DAC FROM +15V SUPPLIES.

LOGIC INPUTS

The DAC-76 may be interfaced with other-than-TTL logic by placing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V– (pin 13).

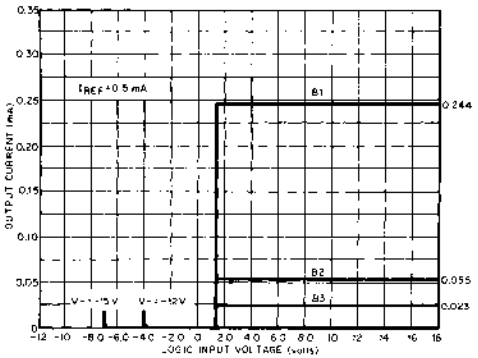
POWER SUPPLIES

As shown in the curves below, power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with V– between –15V and –11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between –15V and the V– supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common mode positive voltage range in the same manner.

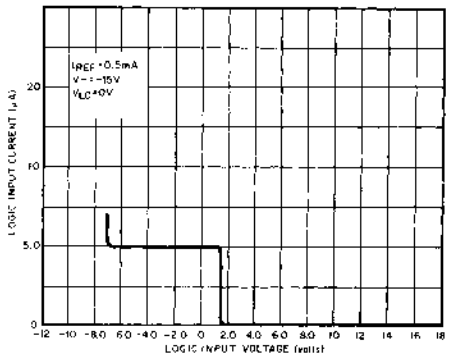
TYPICAL PERFORMANCE CURVES

BIT TRANSFER CHARACTERISTICS



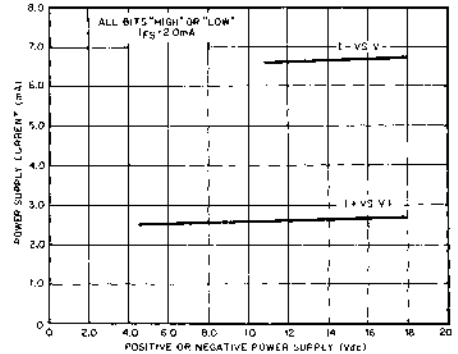
NOTE: ALL BITS ARE FULLY SWITCHED WITH LESS THAN 1.25 SUPPLY RIPPLE AT SWITCHING POINTS WHICH ARE GUARANTEED TO LIE BETWEEN 0.7V AND 2.0V OVER THE OPERATING TEMPERATURE RANGE.

LOGIC INPUT CURRENT VS. INPUT VOLTAGE AND LOGIC INPUT RANGE

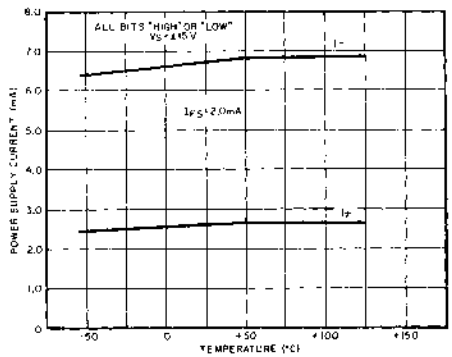


NOTE: LOGIC INPUT VOLTAGE RANGE IS INDEPENDENT OF THE POSITIVE POWER SUPPLY, AND LOGIC INPUTS MAY SWING ABOVE THE SUPPLY.

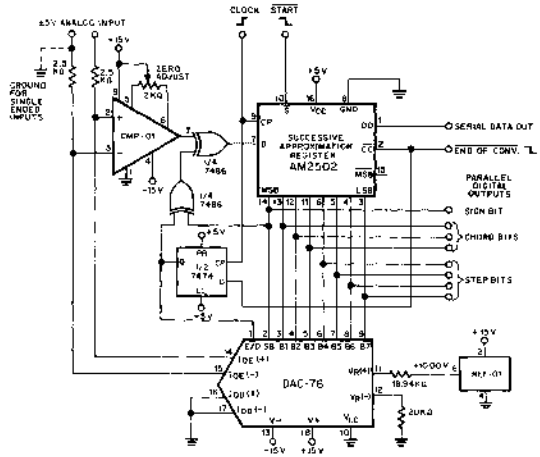
POWER SUPPLY CURRENTS VS. POWER SUPPLY VOLTAGES



POWER SUPPLY CURRENTS VS. TEMPERATURE



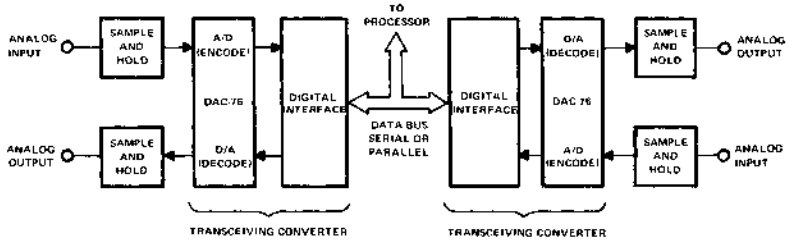
DETAILED ENCODE CONNECTIONS



NOTES:

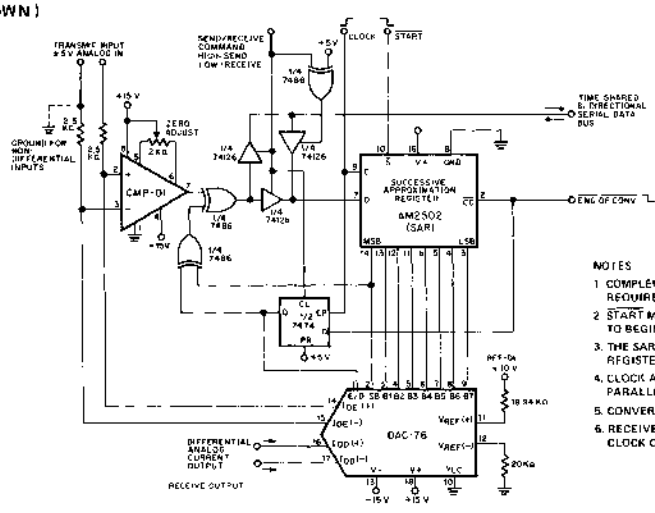
1. CONNECT $\overline{\text{END OF CONV}}$ TO $\overline{\text{START}}$ FOR CONTINUOUS OPERATION.
2. FOR NON CONTINUOUS OPERATION, HOLD $\overline{\text{START}}$ LOW FOR ONE CLOCK CYCLE. CONVERSIONS BEGIN ON THE NEXT LOW TO HIGH TRANSITION OF THE CLOCK AFTER $\overline{\text{START}}$ GOES HIGH.
3. CONVERSION IS COMPLETED IN 9 CLOCK CYCLES.

TRANSCEIVING CONVERTER – TWO WAY DATA TRANSMISSION



SERIAL DATA TRANSCEIVING CONVERTER

(1/2 OF SYSTEM SHOWN)

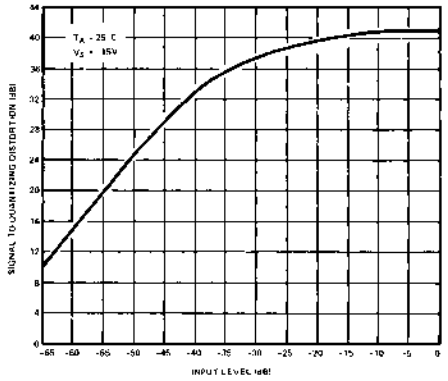


NOTES

1. COMPLEMENTARY SEND/RECEIVE COMMANDS ARE REQUIRED FOR THE TWO ENDS.
2. $\overline{\text{START}}$ MUST BE HELD LOW FOR ONE CLOCK CYCLE TO BEGIN A SEND OR RECEIVE CYCLE.
3. THE SAR IS USED AS A SERIAL IN/PARALLEL OUT REGISTER IN THE RECEIVE MODE.
4. CLOCK AND $\overline{\text{START}}$ MAY BE CONNECTED IN PARALLEL AT BOTH ENDS.
5. CONVERSION IS COMPLETED IN 9 CLOCK CYCLES.
6. RECEIVE OUTPUT IS AVAILABLE FOR ONE FULL CLOCK CYCLE

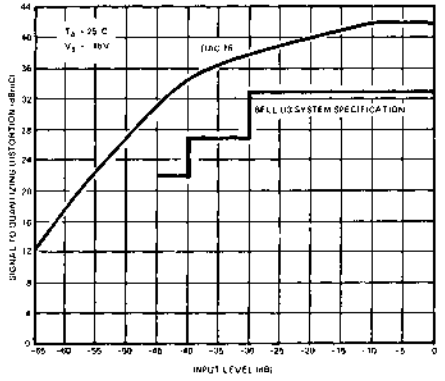
TYPICAL SIGNAL TO QUANTIZING DISTORTION CURVES

SIGNAL TO QUANTIZING DISTORTION VS. INPUT LEVEL (3 kHz FLAT FILTER)



NOTE: 0dB IS 3.5V rms +3dB IS 5.0V OR FULL SCALE CODE (111 1111).

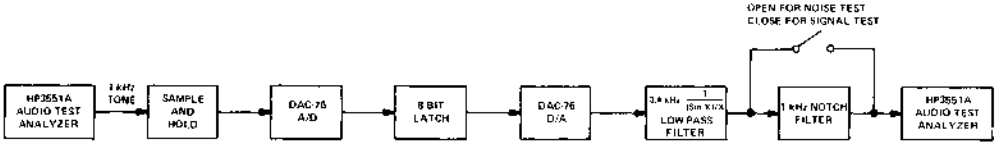
SIGNAL TO QUANTIZING DISTORTION VS. INPUT LEVEL (C-MESSAGE WEIGHTING FILTER & BELL SPEC)



NOTES:
1. 0dB IS -3.5V rms +3dB IS -5.0V OR FULL SCALE CODE (111 1111)
2. C-MESSAGE WEIGHTING FILTER PROVIDES A FREQUENCY RESPONSE CHARACTERISTIC WHICH SIMULATES THE PERCEIVED RESPONSE OF THE HUMAN EAR TO TELEPHONE NOISE.

Note: Quantizing distortion is the difference between the original signal and the processed signal (i.e., after encoding and decoding).

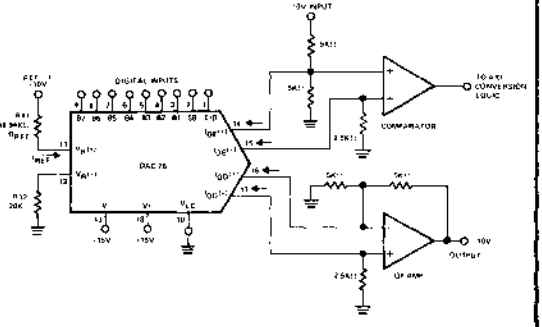
SIGNAL TO QUANTIZING DISTORTION TEST CIRCUIT BLOCK DIAGRAM



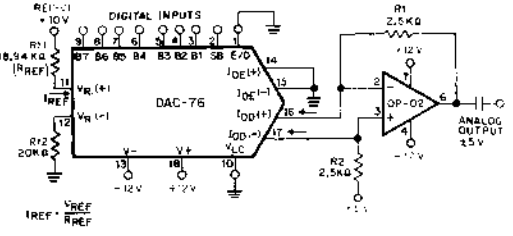
NOTES:
1. 8 kHz SAMPLING CONDITIONS: 62.5 μsec SAMPLE PERIOD, 62.5 nsec A/D CONVERSION TIME
2. AUDIO TEST ANALYZER CONTAINS A C MESSAGE FILTER AND A 3 kHz FLAT FILTER

OUTPUT COMPLIANCE EXTENSION CONNECTIONS

±10V RANGE ENCODE/DECODE CONNECTIONS



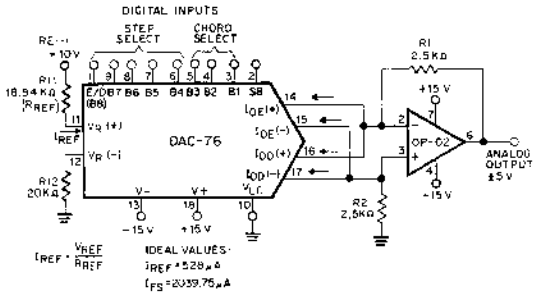
COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



IDEAL VALUES:
I_{REF} = 528 μA
I_{FS} = 2007.75 μA

EXTENSION TO SIGN PLUS 78dB DYNAMIC RANGE

EXTENDED RANGE CONNECTIONS



EXTENDED RANGE OPERATION

When used as a D/A converter only, the DAC-76 range may be extended from sign + 72dB to sign + 78dB by using the encode output current to insert additional levels halfway between each step. By connecting $I_{OD}(+)$ to $I_{OE}(+)$ and $I_{OD}(-)$ to $I_{OE}(-)$, the E/D logic input functions as a fifth step bit input. Full scale positive now becomes 1 111 11111; full scale negative is 0 111 11111. Each chord is divided into 32 steps instead of the former 16 steps, effectively increasing dynamic range by 6dB.

The accompanying table summarizes the new chord and step characteristics obtained in the extended connection shown above.

SUMMARY TABLE FOR 3 CHORD BITS AND 5 STEP BITS

CHORD	STEP (μA)	RANGE (μA)	STEP (mV)	RANGE (V)
0	0.25	0 to 7.75	0.625	0 to 0.019
1	0.5	8.25 to 23.75	1.25	0.021 to 0.059
2	1.0	24.75 to 55.75	2.5	0.062 to 0.139
3	2.0	57.75 to 119.75	5.0	0.144 to 0.299
4	4.0	123.75 to 247.75	10	0.309 to 0.619
5	8.0	255.75 to 503.75	20	0.639 to 1.259
6	16	519.75 to 1015.75	40	1.299 to 2.539
7	32	1047.75 to 2039.75	80	2.619 to 5.099

ADDITIONAL DECODE OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

CHORD SIZE SUMMARY TABLE DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	CHORD ENDPOINTS NORMALIZED TO FULL SCALE	CHORD ENDPOINTS IN μA WITH 2007.75μA F.S.	CHORD ENDPOINTS AS A PERCENT OF FULL SCALE	CHORD ENDPOINTS IN dB DOWN FROM FULL SCALE
0	30	7.5	0.37%	-48.55
1	93	23.25	1.16%	-38.73
2	219	54.75	2.73%	-31.29
3	471	117.75	5.86%	-24.63
4	975	243.75	12.1%	-18.32
5	1983	495.75	24.7%	-12.15
6	3999	999.75	49.8%	-6.06
7	8031	2007.75	100%	0

DECODE OUTPUT EXPRESSED IN DB DOWN FROM FULL SCALE (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	–	-47.73	-38.18	-30.82	-24.20	-17.90	-11.74	-5.65
1	0001	-72.07	-46.73	-37.51	-30.24	-23.66	-17.37	-11.22	-5.13
2	0010	-66.05	-45.84	-36.88	-29.70	-23.15	-16.87	-10.73	-4.65
3	0011	-62.53	-45.03	-36.30	-29.18	-22.66	-16.40	-10.27	-4.19
4	0100	-60.03	-44.29	-35.75	-28.70	-22.21	-15.96	-9.83	-3.75
5	0101	-58.10	-43.61	-35.24	-28.24	-21.77	-15.53	-9.41	-3.33
6	0110	-56.51	-42.98	-34.75	-27.80	-21.36	-15.13	-9.01	-2.94
7	0111	-55.17	-42.39	-34.29	-27.39	-20.96	-14.74	-8.63	-2.56
8	1000	-54.01	-41.84	-33.85	-26.99	-20.58	-14.37	-8.26	-2.19
9	1001	-52.99	-41.32	-33.44	-26.61	-20.22	-14.02	-7.91	-1.84
10	1010	-52.07	-40.83	-33.04	-26.25	-19.87	-13.68	-7.57	-1.51
11	1011	-51.25	-40.37	-32.66	-25.90	-19.54	-13.35	-7.25	-1.18
12	1100	-50.49	-39.93	-32.29	-25.57	-19.22	-13.03	-6.93	-0.87
13	1101	-49.80	-39.51	-31.95	-25.25	-18.91	-12.73	-6.63	-0.57
14	1110	-49.15	-39.11	-31.61	-24.94	-18.61	-12.43	-6.34	-0.28
15	1111	-48.55	-38.73	-31.29	-24.63	-18.32	-12.15	-6.06	0

DECODE OUTPUT EXPRESSED IN PERCENT OF FULL SCALE (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	0.411	1.23	2.88	6.16	12.7	25.9	52.2
1	0001	0.025	0.461	1.33	3.08	6.56	13.5	27.5	55.4
2	0010	0.050	0.511	1.43	3.27	6.96	14.3	29.1	58.6
3	0011	0.075	0.560	1.53	3.47	7.36	15.1	30.7	61.7
4	0100	0.100	0.610	1.63	3.67	7.76	15.9	32.3	64.9
5	0101	0.125	0.660	1.73	3.87	8.16	16.7	33.9	68.1
6	0110	0.149	0.710	1.83	4.07	8.56	17.5	35.5	71.3
7	0111	0.174	0.760	1.93	4.27	8.96	18.3	37.0	74.5
8	1000	0.199	0.809	2.03	4.47	9.35	19.1	38.6	77.7
9	1001	0.224	0.859	2.13	4.67	9.75	19.9	40.2	80.9
10	1010	0.249	0.909	2.23	4.87	10.1	20.7	41.8	84.1
11	1011	0.274	0.959	2.33	5.07	10.5	21.5	43.4	87.2
12	1100	0.299	1.01	2.43	5.27	10.9	22.3	45.0	90.4
13	1101	0.324	1.06	2.53	5.47	11.3	23.1	46.6	93.6
14	1110	0.349	1.11	2.63	5.67	11.7	23.9	48.2	96.8
15	1111	0.374	1.16	2.73	5.86	12.1	24.7	49.8	100
STEP SIZE		0.025	0.050	0.100	0.199	0.398	0.797	1.59	3.19

APPLICATIONS

The DAC-76 is ideal in applications which require a wide dynamic range and can be characterized by an accuracy specification based on percent of reading rather than percent of full scale. The nonlinear characteristic is also useful in control systems when a decreasing slope or a constant rate of change (constant second derivative) is needed as a system approaches zero level or a given set point.

INSTRUMENTATION AND CONTROL

- Data Acquisition -- Data Transceiver
- Microprocessor Interface
- PCM Data Recording -- Biological, Automotive, Aviation
- Function Generation
- PCM Telemetry
- Servo Controls - Phase Locked Loop and Set Point Controls
- Transducer Interface -- Seismic, Strain Gauge

TELECOMMUNICATIONS

- Telephony -- PCM Codec
- Two-Way Radio
- Intercom Systems
- Radar Systems
- Secure Voice Communications

AUDIO

- Music Distribution
- Digital Recording
- Constant dB Attenuator
- Analog Multiplexer
- Digitally-Controlled Gain
- Voice Synthesis and Identification
- Variable Speed Recording and Playback
- Reverberation and Special Effects

ADDITIONAL CIRCUIT APPLICATIONS

- Logarithmic Attenuator
- Four Quadrant Multiplier
- Line Driver
- dB Meter
- Analog or Digital Compressor and Expander
- Four Channel Multiplexer

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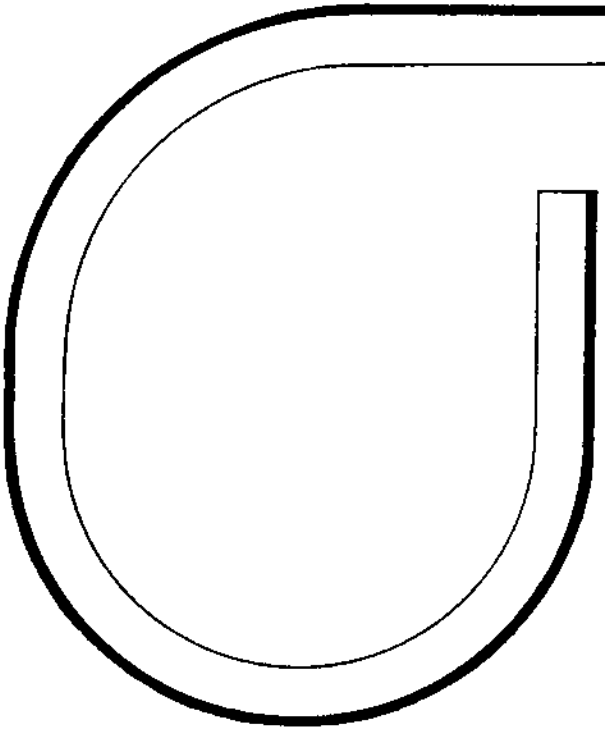

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MULTIPLEXERS

PRODUCT	TITLE	PAGE
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PRELIMINARY

MUX-88

PROTECTED 8 CHANNEL BI-FET ANALOG MULTIPLEXER

GENERAL DESCRIPTION

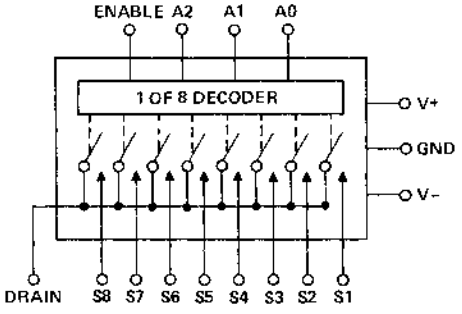
The MUX-88 is a monolithic 8 channel analog multiplexer which connects a single output to 1 of the 8 analog inputs depending upon the state of a 3-bit binary address. Disconnection of the output is provided by a logical "0" at the enable input, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance BI-FET technology, this device features overvoltage protection that is fail safe with power loss, while offering low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. This multiplexer does not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pullup resistors.

FEATURES

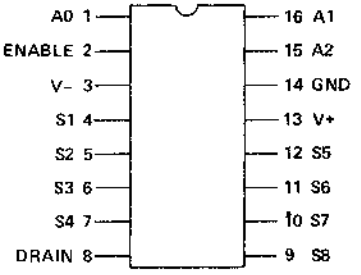
- Pin Compatible With DG508, HI-508A, LF11508
- JFET Switches Rather Than CMOS
- No Static Discharge Blow-out Problem
- No SCR Latch-up Problems
- Analog Inputs Overvoltage Protected ±20V Beyond Normal Ratings
- Fail Safe With Power Loss
- Low "ON" Resistance . . . . . 220Ω TYP
- Low Output Leakage Current . . . . . 100nA MAX
- Digital Inputs Compatible With TTL and CMOS
- No Pullup Resistors Required To Insure Break-Before-Make Action With TTL Inputs

FUNCTIONAL DIAGRAM AND TRUTH TABLE



A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PIN CONNECTIONS AND ORDERING INFORMATION



TOP VIEW

16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE
MUX-88AQ	-55°C TO +125°C
MUX-88BQ	-55°C TO +125°C
MUX-88EQ	-25°C TO +85°C
MUX-88FQ	-25°C TO +85°C

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Operating Temperature Range, MUX-88AQ, BQ	−55°C to +125°C	Max Junction Temperature	150°C
Operating Temperature Range, MUX-88EQ, FQ	−25°C to +85°C	V+ Supply to V− Supply	36V
Storage Temperature Range	−65°C to +150°C	V+ Supply to Ground	18V
Power Dissipation	500mW	Logic Input Voltage	−4V to V+ Supply
Derate above 100°C	10mW/°C	Analog Input Voltage	V− Supply −20V to V+ Supply +15V
Lead Soldering Temperature	300°C (60 sec)	Max Current Through Any Pin	25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = 15V, V− = −15V and T_A = 25°C unless otherwise specified.

			MUX-88A			MUX-88B			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100µA	–	220	260	–	300	370	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_D ≤ 10V, I_S = 100µA	–	–	1.6	–	–	4.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100µA	–	8.0	20	–	15	30	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = −11V (Note 1)	–	0.01	0.1	–	0.01	0.1	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = −11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	1.0	10	–	1.0	10	µA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	4.0	10	–	4.0	10	µA
Digital Input Capacitance	C_{DIG}		–	3.0	–	–	3.0	–	pF
Switching Time	t_{TRAN}	Figure 1 (Note 2)	–	1.0	1.3	–	1.5	2.1	µsec
Output Settling Time	t_S	10V step to .025%	–	2.9	–	–	2.9	–	µsec
Break-Before-Make Delay	t_{DLY}	Figure 3	–	0.8	–	–	1.0	–	µsec
Enable Delay "ON"	$t_{ON(EN)}$	Figure 2	–	1.0	–	–	1.2	–	µsec
Enable Delay "OFF"	$t_{OFF(EN)}$	Figure 2	–	0.2	–	–	0.2	–	µsec
"OFF" Isolation	ISO_{OFF}	(Note 3)	–	−80	–	–	−80	–	dB
Crosstalk	CT	(Note 3)	–	−80	–	–	−80	–	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	12	–	–	12	–	pF
Input to Output Capacitance	$C_{DS(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	0.2	–	–	0.2	–	pF
Positive Supply Current (All Digital Inputs Grounded)	$I+$	V+ = 15V	–	10	12	–	6.0	8.0	mA
		V+ = 5V	–	8.0	–	–	5.0	–	mA
Negative Supply Current (All Digital Inputs Grounded)	$I-$	V− = −15V	–	3.0	3.8	–	2.0	3.0	mA
		V− = −5V	–	2.5	–	–	1.8	–	mA
These specifications apply for V+ = 15V, V− = −15V and −55°C ≤ T_A ≤ +125°C unless otherwise specified.									
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100µA	–	–	370	–	–	480	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_D ≤ 10V, I_S = 100µA	–	–	2.4	–	–	6.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100µA	–	10	30	–	15	45	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = −11V (Note 2)	–	–	10	–	–	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = −11V (Note 2)	–	–	100	–	–	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 2)	–	–	100	–	–	100	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	–	20	–	–	20	µA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	–	20	–	–	20	µA
Positive Supply Current	$I+$	All Digital Inputs Grounded	–	–	15	–	–	11	mA
Negative Supply Current	$I-$	All Digital Inputs Grounded	–	–	5.0	–	–	4.0	mA

ELECTRICAL CHARACTERISTICS NOTES

NOTE 1: Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

NOTE 2: Lots are sample tested to this parameter. The measurement conditions of FIGURE 1 insure worst case transition time.

NOTE 3: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with R_L = 1K, C_L = 7pF, V_s = 3V RMS, F = 100 kHz.

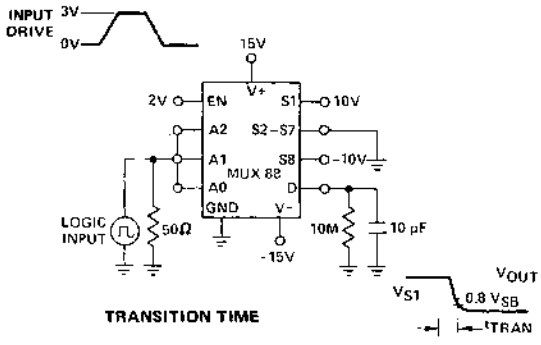
ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = 15V, V– = –15V and T_A = 25°C unless otherwise specified.

			MUX-88E			MUX-88F			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100μA	–	220	260	–	300	370	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_D ≤ 10V, I_S = 100μA	–	–	1.6	–	–	4.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100μA	–	8.0	20	–	15	30	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = –11V (Note 1)	–	0.01	0.1	–	0.01	0.1	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = –11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	1.0	10	–	1.0	10	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	4.0	10	–	4.0	10	μA
Digital Input Capacitance	C_{DIG}		–	3.0	–	–	3.0	–	pF
Switching Time	t_{TRAN}	Figure 1 (Note 2)	–	1.0	1.3	–	1.5	2.1	μsec
Output Settling Time	t_S	10V step to .025%	–	2.9	–	–	2.9	–	μsec
Break-Before-Make Delay	t_{DLY}	Figure 3	–	0.8	–	–	1.0	–	μsec
Enable Delay "ON"	$t_{ON(EN)}$	Figure 2	–	1.0	–	–	1.2	–	μsec
Enable Delay "OFF"	$t_{OFF(EN)}$	Figure 2	–	0.2	–	–	0.2	–	μsec
"OFF" Isolation	ISO_{OFF}	(Note 3)	–	–80	–	–	–80	–	dB
Crosstalk	CT	(Note 3)	–	–80	–	–	–80	–	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	12	–	–	12	–	pF
Input to Output Capacitance	$C_{DS(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	0.2	–	–	0.2	–	pF
Positive Supply Current (All Digital Inputs Grounded)	I+	V+ = 15V	–	10	12	–	6.0	8.0	mA
		V+ = 5V	–	8.0	–	–	5.0	–	mA
Negative Supply Current (All Digital Inputs Grounded)	I–	V– = –15V	–	3.0	3.8	–	2.0	3.0	mA
		V– = –5V	–	2.5	–	–	1.8	–	mA
These specifications apply for V+ = 15V, V– = –15V and –25°C ≤ T_A ≤ 85°C unless otherwise specified.									
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100μA	–	–	370	–	–	480	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_D ≤ 10V, I_S = 100μA	–	–	2.4	–	–	6.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100μA	–	10	30	–	15	45	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = –11V (Note 2)	–	–	10	–	–	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = –11V (Note 2)	–	–	100	–	–	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 2)	–	–	100	–	–	100	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	–	20	–	–	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	–	20	–	–	20	μA
Positive Supply Current	I+	All Digital Inputs Grounded	–	–	15	–	–	11	mA
Negative Supply Current	I–	All Digital Inputs Grounded	–	–	5.0	–	–	4.0	mA

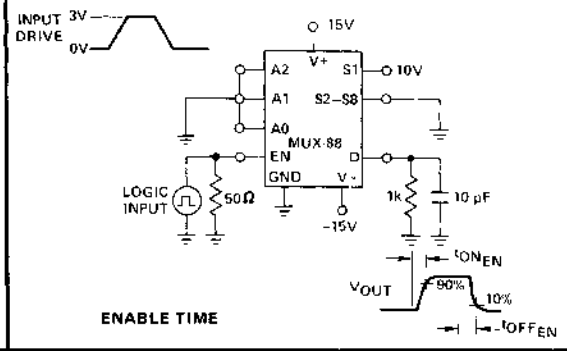
A.C. TEST CIRCUITS AND PERFORMANCE CHARACTERISTICS

FIGURE 1



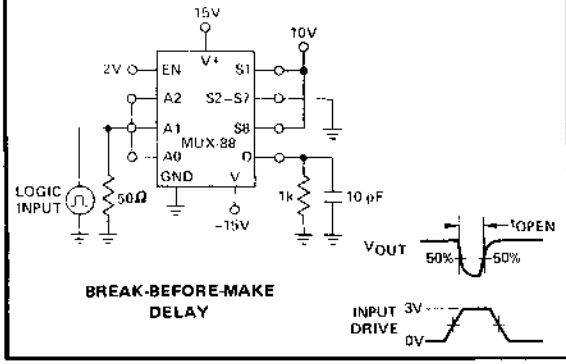
TRANSITION TIME

FIGURE 2



ENABLE TIME

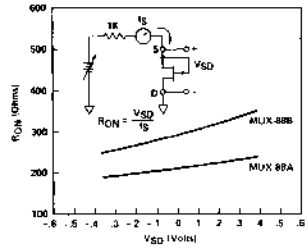
FIGURE 3



BREAK-BEFORE-MAKE DELAY

FIGURE 4

"ON" RESISTANCE CHARACTERISTICS
$T_A = 25°C$



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFET's in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about .1 μA) as the input voltage is raised above ≈1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of –15V to +11V with V_{SUPPLY} = ±15V. Input voltages up to ±20V beyond this normal input range are permissible with device power on. Input voltages of up to +11V and lower than –15V are allowable with device power off. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply) otherwise leakage currents will increase and a normally "OFF" switch may be falsely turned "ON". Although the output voltage will be erroneous, damage to the multiplexer will not result because the switch "ON" resistance greatly increases and the I_{DSS} of the JFET protects the switch (Figure 4). When operating with negative input voltages, current through an "ON" switch must be externally limited to prevent the voltage drop across the switch from exceeding –0.4V source to drain. This is not a problem generally, for in most applications the multiplexer output will be connected to a high impedance load.

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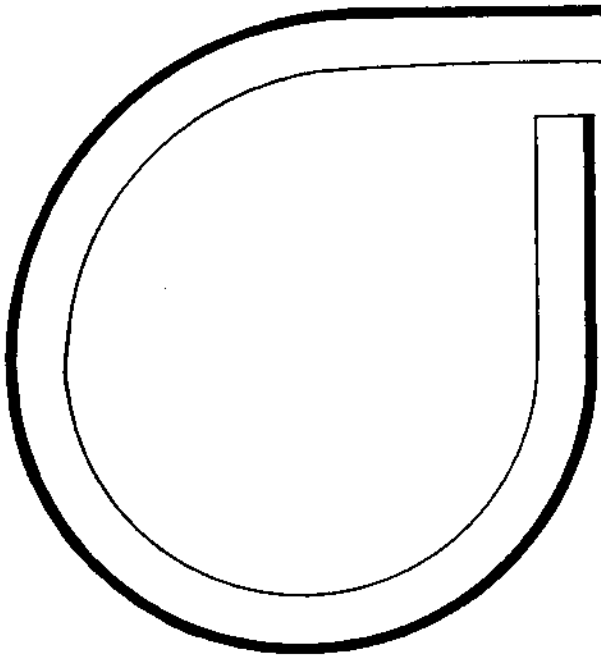


OPERATIONAL AMPLIFIER DEFINITIONS

AVERAGE BIAS CURRENT DRIFT (TCI_B)
The ratio of the change in the bias current to the change in temperature producing it.

AVERAGE OFFSET CURRENT DRIFT (TCI_{os})
The ratio of the change in the offset current to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{os})
The ratio of the change in the offset voltage to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT WITH EXTERNAL TRIMMING (TCV_{osn})
The ratio of the change in the offset voltage to the change in temperature producing it, with the offset voltage trimmed to zero at room temperature.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

COMMON-MODE INPUT RESISTANCE (R_{inCM})
The ratio of the input voltage range to the change in input bias current over this range.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT NOISE CURRENT (i_{np-p})
The peak to peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1Hz band surrounding a specified value of frequency.

INPUT NOISE VOLTAGE (e_{np-p})
The peak to peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage in a 1Hz band surrounding a specified value of frequency.

INPUT OFFSET CURRENT (I_{os})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT OFFSET VOLTAGE (V_{os})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

INPUT RESISTANCE (R_{in})
The ratio of the small-signal change in input voltage to the change in input current at either input terminal with the other grounded.

LARGE SIGNAL VOLTAGE GAIN (A_{vo})
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

MAXIMUM OUTPUT VOLTAGE SWING (V_{oM})
The peak output voltage that can be obtained without clipping.

OPEN LOOP OUTPUT RESISTANCE (R_O)
The small signal driving point resistance of the output terminal with respect to ground at a specified quiescent dc output voltage and current.

POWER DISSIPATION (P_d)
The total power dissipated in the amplifier with the output at zero volts and no load.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

SLEW RATE (SR)
The ratio of a change in output voltage to the minimum time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative-going changes.

SUPPLY CURRENT (I_{sy})
The current required from the power supply to operate the amplifier with no load and the output at zero volts.

UNITY GAIN CLOSED LOOP BANDWIDTH (BW)
The frequency at which the magnitude of the small signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

MATCHING OPERATIONAL AMPLIFIER DEFINITIONS

INPUT OFFSET VOLTAGE MATCH (ΔV_{os}). The difference between the offset voltages of side A and side B: ($V_{OSA} - V_{OSB}$).

COMMON MODE REJECTION RATIO MATCH (ΔCMRR). The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. ΔCMRR in db = $-20 \log_{10}$ (ΔCMRR in volt/volt).

COMPARATOR DEFINITIONS

COMMON MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT RESISTANCE (R_{in})
The resistance looking into either input terminal with the other grounded.

DIFFERENTIAL INPUT VOLTAGE
The range of voltage between the input terminals for which operation within specifications is assured.

INPUT BIAS CURRENT (I_B)
The average of the two input currents, with the inputs tied together.

INPUT OFFSET CURRENT (I_{OS})
The difference in the currents into the two input terminals when the output is within a specified voltage range.

INPUT OFFSET VOLTAGE (V_{OS})
The voltage between the input terminals when the output is within a specified voltage range.

INPUT SLEW RATE
The maximum rate of change in differential and/or common-mode input voltage which the input stage can follow. The comparator's total response time for any input voltage step with arbitrary overdrive is equal to the sum of the response time for the small signal (100mV) step with the same overdrive, plus the slewing time (= initial differential input voltage divided by input slew rate).

INPUT VOLTAGE RANGE (CMVR)
The range of common mode voltage on the input terminals for which operation within specifications is assured.

OUTPUT LEAKAGE CURRENT (I_{LEAK})
The current into the output terminal with a given output voltage and input drive equal to or greater than a specified value.

OFFSET VOLTAGE ADJUSTMENT RANGE
The change in offset voltage that can be obtained by adjusting a specified external nulling potentiometer.

OUTPUT SINK CURRENT (I_{sink})
The maximum negative current that can be delivered by the comparator.

OVERDRIVE
The input step voltage of specified size drives the comparator from some initial input voltage to an input level just barely in excess of that required to bring the output from its high or low state to the logic threshold voltage. This excess is defined as the voltage overdrive.

POSITIVE OUTPUT VOLTAGE (V_{OH})
The high output voltage level with a given load and input drive equal to or greater than a specified value.

POWER SUPPLY REJECTION RATIO (PSRR)
The ratio of the maximum change in input offset voltage to the specified change in power supply voltage.

RESPONSE TIME (t_r)
The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4V when the loading logic circuitry is not used.

SATURATION VOLTAGE (V_{SAT})
The low output voltage level with a given sink current and input drive less than or equal to a specified value.

SUPPLY CURRENTS
The currents required from the positive or negative supplies to operate the comparator with no output load. The currents will vary with input voltage, but are maximum when the output is low, and, therefore, are specified with the input drive less than or equal to a given value.

VOLTAGE GAIN (A_V)
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

MATCHED TRANSISTOR PAIR DEFINITIONS

AVERAGE OFFSET CURRENT DRIFT (TCI_{os})
The ratio of the change in I_{os} to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{os})
The ratio of the change in V_{os} to the change in temperature producing it.

BIAS CURRENT (I_B)
The average of the base currents at a specified collector voltage and current.

BROADBAND NOISE VOLTAGE (e_{nRMS})
The root-mean-square noise voltage referred to the input in a specified bandwidth at a specified collector voltage and current.

CURRENT GAIN MATCH (Δh_{FE})
The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the lower of the two h_{FE}'s.

$$\left(1 - \frac{h_{FE_1}}{h_{FE_2}}\right) \times 100$$

NOISE VOLTAGE ($e_{np\text{-}p}$)
The peak-to-peak noise voltage referred to the input in a specified bandwidth at a specified collector voltage and current.

NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage referred to the input in a 1Hz band surrounding a specified frequency, measured at a specified collector voltage and current.

OFFSET CURRENT (I_{os})
The difference between the base currents at a specified collector voltage and current.

OFFSET CURRENT CHANGE ($\Delta I_{os}/\Delta V_{CB}$)
The ratio of the change in offset current to the change in collector-base voltage producing it.

OFFSET VOLTAGE (V_{os})
The difference between the base-emitter voltages ($V_{be_1} - V_{be_2}$) at a specified collector voltage and current.

VOLTAGE REFERENCE DEFINITIONS

LINE REGULATION
The ratio of the change in output voltage to the change in line voltage producing it including the effects of self heating.

LOAD REGULATION
The ratio of the change in output voltage to the change in load current producing it including the effects of self heating.

OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT})
The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of the typical output voltage.

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{V_O \text{ (Typical)}} \times 100$$

OUTPUT TEMPERATURE COEFFICIENT (TCV_O)
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C. For example: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O(0^\circ \text{ to } +70^\circ C) = \frac{\Delta V_{OT}\ 0^\circ \text{ to } +70^\circ C}{70^\circ C}$$

$$\text{and } TCV_O(-55^\circ \text{ to } +125^\circ C) = \frac{\Delta V_{OT}\ -55 \text{ to } +125^\circ C}{180^\circ C}$$

OUTPUT TURN-ON SETTLING TIME (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

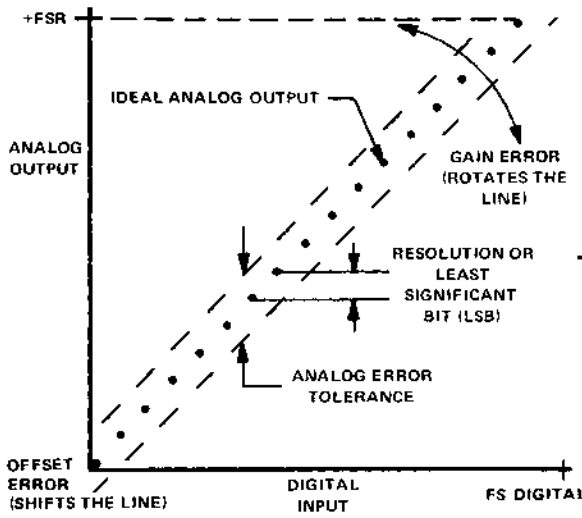
OUTPUT VOLTAGE NOISE ($e_{np\text{-}p}$)
The peak to peak output noise voltage in a specified frequency band.

QUIESCENT CURRENT (I_{SY})
The current required from the supply to operate the device with no load.

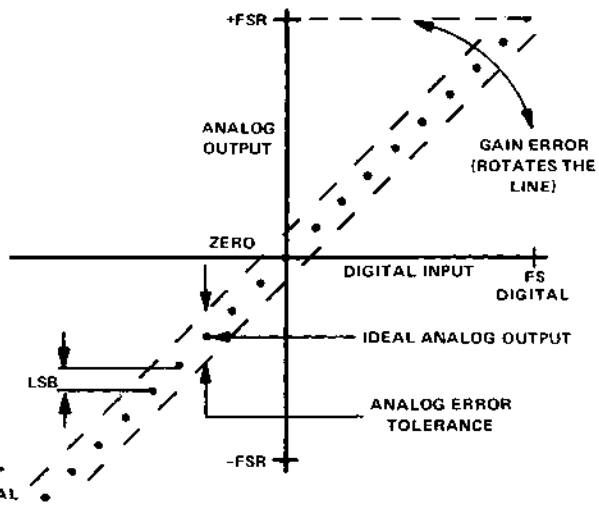
LINEAR DIGITAL-TO-ANALOG CONVERTER TERMS AND DEFINITIONS

D/A Converters accept either a binary-coded or BCD-coded digital input code and convert this input to an equivalent analog voltage or current as an output. PMI's D/A Converters utilize the current-switched ladder network design principle which provides fast settling and reduced switching transients. D/A Converters are classified according to the type of analog output range i.e. bipolar or unipolar (See Figures below):

UNIPOLAR D/A CONVERTERS



BIPOLAR D/A CONVERTERS



DISCUSSION OF ERRORS

Transfer accuracy in a D/A Converter is generally determined by measuring deviation of the actual analog output from the ideal expected output. In general, the adjustable analog output errors of a D/A Converter are full-scale or gain error and offset or zero-scale error. Nonadjustable D/A Converter errors include nonlinearity, differential nonlinearity, zero-scale symmetry, zero and full-scale temperature drift coefficients and power-supply sensitivity. The most meaningful nonadjustable error term in a D/A Converter is NONLINEARITY. The next most important nonadjustable error terms are full-scale drift and differential-nonlinearity. A D/A Converter that has a specified maximum nonlinearity of ±1/2 LSB over temperature will also be guaranteed to be monotonic. PMI specifies maximum nonlinearity over temperature for every D/A Converter (except the DAC-03) to assure the designer of precision performance for the most demanding applications.

DIGITAL-TO-ANALOG CONVERTER
A circuit for converting a digital code word into discrete analog quantities according to a prescribed relationship.

LEAST SIGNIFICANT BIT (LSB)
The smallest incremental analog output change obtainable and is equal to the full scale output range divided by 2^{n-1}, where n = number of bits.

$$LSB = \frac{FSR}{(2^n)-1}$$

MOST SIGNIFICANT BIT (MSB)
The largest incremental analog output change obtainable by switching a single logic bit input. It is ideally equal to:

$$MSB = FSR\left(\frac{2^{(n-1)}}{(2^n)-1}\right)$$

where n = number of bits.

FULL SCALE RANGE (FSR)
The output analog signal span expressed in units of voltage or current.

ZERO SCALE OFFSET ERROR (ZS)
The measured analog output when the digital input code corresponds to an analog value of zero. Usually expressed as a percentage of nominal Full Scale Range but also expressed in ppm, LSB's, or given in units of current or voltage.

ZERO SCALE SYMMETRY ERROR
For a Sign-Magnitude D/A converter, zero scale symmetry is the change in the analog output produced by switching the sign bit with a zero code input to the magnitude bits. This quantity is expressed in units of current, voltage, or in fractions of an LSB.

RESOLUTION
The number of states (2^n) that the output range may be divided or resolved into, where n = number of bits. Generally this is expressed in number of bits.

NONLINEARITY (NL)
The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of Full Scale Range (FSR) or given in terms of LSB value. The end points are zero scale output to full scale output for unipolar operation and minus full scale to positive full scale for bipolar operation.

DIFFERENTIAL NONLINEARITY (DNL)
The maximum deviation of the analog output between any two adjacent output states from the ideal value.

Differential nonlinearity error is expressed as percent of full scale range or in terms of LSB value. For example, a differential linearity error specification of ±1/2 LSB implies that the output step size for adjacent digital input codes is 1 ± 1/2 LSB or 1/2 to 3/2 LSB.

MONOTONICITY
A converter is monotonic if the analog output increases or remains the same for an increase in value of the digital input code.

GAIN ERROR
The difference between the actual output Full Scale Range and the ideal Full Scale Range expressed as a percent of Full Scale Range or in terms of LSB value.

SETTLING TIME
The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. Usually specified for a Full Scale Range change and measured from the 50% point of the logic input change to the time the output reaches final value within the specified error band.

GLITCH
A switching transient appearing in the output during a code transition. Its value is expressed in volts or current and time duration at the base.

RELATIVE ACCURACY
Another term for nonlinearity.

POWER SUPPLY SENSITIVITY
The change in the Full Scale Range of the converter due to a change in the power supply value. This may be expressed as a percent of Full Scale Range per one percent change in the power supply or as a percent of Full Scale Range per volt of power supply change. Normally this is specified at D.C., but is sometimes specified over a given frequency range.

FULL SCALE TEMPERATURE COEFFICIENT OR GAIN DRIFT
This is the change in the Full Scale Range from the 25°C value and either temperature extreme divided by the corresponding change in temperature and is expressed in ppm/°C.

MISCELLANEOUS TEMPERATURE COEFFICIENTS
Although nonlinearity and differential nonlinearity should be specified as a worst case error over temperature, some manufacturers do specify a drift component on these terms. As in gain drift, they are specified as the change from the 25°C values to either temperature extreme divided by the corresponding change in temperature and expressed in ppm of FSR/°C.

OUTPUT VOLTAGE COMPLIANCE
The voltage range over which the current output of a digital-to-analog converter meets the specified error limits. If the error limit is not specified, the voltage range is not a true compliance specification but merely a range over which the converter will be functional.

D/A CONVERTERS BY OUTPUT TYPE

CURRENT OUTPUT D/A CONVERTERS
The output of the converter is a true digitally controlled current source or sink which has a high output impedance and a voltage compliance within which the converter meets the specified error limits.

RESISTIVE OUTPUT D/A CONVERTER
The output of the converter is a current, but has a low output resistance (typically 1-20 K ohm) and nearly zero output voltage compliance.

VOLTAGE OUTPUT D/A CONVERTER
The output of the converter is a voltage source, and is characterized by low output impedance and a specified load driving capability.

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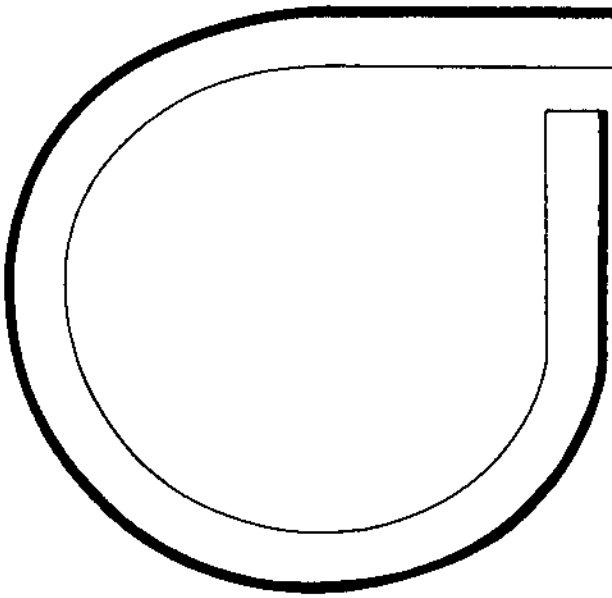

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Monolithic Chips

GENERAL DESCRIPTION

The superior performance of most Precision Monolithics products is available to the hybrid microcircuit designer. All chips are 100% electrically tested for all guaranteed DC parameters at 25°C and are 100% visually inspected to MIL-STD-883 visual criteria. Each chip is protected with our "Triple Passivation" Process incorporating an advanced Silicon Nitride ion barrier plus a thick glass coating over the metallization. Chips are packaged in waffle-pack carriers with an anti-static shield and cushioning strip placed over the active surface to assure extra protection during shipment. Precision Monolithics chips provide the highest performance available coupled with lowest overall finished costs.

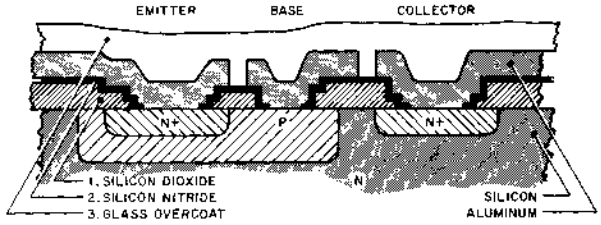
FEATURES

- Highest Yields . . . . . 25°C Parameters Guaranteed
- Highest Performance. . . . . Tight specifications
- Highest Reliability—Exclusive "Triple Passivation" Process
- Wide Temperature Range Operations
- Excellent Die Attach. . .Thick Gold or Standard Backing
- 100% Visually Inspected to MIL-STD-883 Criteria
- Tight Distributions . . . . . Precision Process Control
- Carefully Packaged . . . . . .No Loss During Shipment
- Guaranteed Dimensions . . . . . ±3 mils
- Guaranteed Pad Size . . . . . 4 mils

TRIPLE PASSIVATION

Triple Passivation is a three-step process which provides superior reliability and protection for all Precision Monolithics integrated circuits. First, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third ep is the thick glass overcoat layer which leaves only the bonding pads exposed. This "glassivation" protects the chip from damage during assembly and is especially important in minimizing yield loss during shipment and assembly of chips for hybrid circuits.

PRECISION MONOLITHICS
TRIPLE PASSIVATED™
INTEGRATED CIRCUIT PROCESS



QUALITY ASSURANCE

Precision Monolithics believes that quality and reliability must be built into the product; no amount of testing can replace these inherent properties. For this reason, all devices are fabricated and processed to MIL-STD-883 requirements as standard practice with many exclusive processes and controls added to improve quality and reliability. The integrity of aluminum metallization is confirmed by sampling wafer lots using a Scanning Electron Microscope (SEM) examination per Method 2018 specifications. QA testing of dice is provided by normal production testing of packaged devices.

ORDERING INFORMATION

All PMI chips are available with either plain backing or, at extra cost, 1-micron thick eutectic-bonded gold backing. Electrical performance is specified at 25°C for all products in the data sheet section of this catalog. Visual inspection criteria is as listed below:

XXXXXX – XXX – XX

- XX — BACKING SUFFIX: C = PLAIN, CG = GOLD
- XXX — VISUAL CRITERIA:
  - A = MIL-STD-883A METHOD 2010.2 TEST CONDITION A
  - B = MIL-STD-883A METHOD 2010.2 TEST CONDITION B
  - C = PMI "C" VISUAL, PMI SPECIFICATION NO. A0018 BASED ON MIL-STD-883 METHOD 2010 ISSUED 1 MAY 1968.
- XXXXXX — MODEL TYPE
- ELECTRICAL GRADE: N = TOP, G = MIDDLE, GR = LOWEST

For price and delivery information or quotations for special devices, contact the nearest PMI sales office or representative listed in the back of this catalog.

MECHANICAL INFORMATION

Dimensions

All dimensions are nominal and in mils (10^{-3} inches). Die thickness is nominally 10 mils ±1 mil. Tolerance on die dimensions is ± 3 mils.

Metallization

Aluminum metallization with a nominal thickness of 10,000 angstroms is standard for all devices.

Bonding Pads

Minimum bonding pad size is 4.0 mils X 4.0 mils for all devices.

TESTING

Visual Inspection

All chips are 100% visually inspected to the applicable visual criteria per MIL-STD-883.

Devices with visual inspection to test condition A, MIL-STD-883A Method 2010.2 are available on special order only.

Electrical Testing

All dice are 100% tested to the DC specifications listed in the data sheet section of this catalog. Sample assembly and testing in standard packages to specified LTPD of units from customer's dice lot are available at extra cost.

ASSEMBLY PROCEDURES

Proper shipping and storage, die attachment, and bonding are required to take advantage of the full performance built into PMI devices. PMI provides this information but cannot assume responsibility for technology and interface problems in applying chips, nor guarantee results in using the suggested processing methods; this information is for user assistance only and is to be used at the user's own discretion.

STORAGE

Assembly begins with storage, because chips which are metallized with aluminum will slowly oxidize if exposed to air. This action is very slow, but eventually a thin layer of aluminum oxide will form on the bonding pads. To keep oxidation to a minimum, PMI chips are stored in a temperature and humidity controlled nitrogen atmosphere at the factory until shipment; they are never stored at any other point in the sales and distribution chain.

Oxidation is a more serious problem with thermal compression gold ball bonding than it is with ultrasonic aluminum wire bonding. Ultrasonic aluminum wire bonding can penetrate a thicker layer of aluminum oxide than gold ball bonding. If thermal compression gold ball bonding is used, the devices should be bonded within a few weeks after shipment. Storage under dry nitrogen conditions is highly recommended for chips to be used with either type of bonding.

SHIPPING

Protection during shipment is provided by the waffle-pack carrier and its antistatic shield and cushioning strip. In addition the waffle pack is vacuum-sealed in a polyethylene bag.

EUTECTIC DIE ATTACHMENT CONDITIONS

The die-attach area of the package should be gold plated. While preforms are not generally required, they may be necessary in some cases depending on die size and the thickness of the package's gold plating. If required, preforms of approximately 0.65 or 0.90 mm diameter with a composition of gold-silicon 98/2 are recommended.

The heater-block used should have a sufficiently large thermal mass plus adequate control to assure a constant package temperature of 420°C ± 10°C during the die-attach operation. Inert gas protection, nitrogen with a flow of approximately 30 liters/hour, is also recommended.

EUTECTIC DIE ATTACHMENT PROCEDURE

For ease of handling in die attachment, dice should first be transferred from their waffle packs to flat glass or metal plates. Allow the package to soak a sufficient time to acquire a uniform temperature. (Where necessary place a preform on the mounting surface.)

Using suitable tweezers, carefully pick up the die from the supply plate, orient properly and gently scrub in a circular or back-and-forth motion until eutectic melt is visible completely around the die. Eutectic melt should be visible completely around the periphery of the die. There should be no evidence of balling or flaking of die-attach material. After completing the die-attach operation remove the package from the heater block.

The die should be level and flat with respect to the package surface. Die attach material should not touch the top surface of the die or stand vertically above the edge of the die.

CONDUCTIVE EPOXY DIE ATTACHMENT

A solvent and other contaminant-free conductive epoxy should be used, specifically designed for die-attach use. Manufacturer's instructions should be carefully followed. While PMI uses eutectic die-attach exclusively, conductive epoxy die-attach can be used, although this technique is not as well-established.

ULTRASONIC ALUMINUM WIRE BONDING

PMI uses ultrasonic aluminum wire bonding and recommends its use for best performance. It is also more economical than gold-ball bonding. For specific procedures with either method, the detailed operation instructions of the manufacturer of the specific bonding equipment used should be carefully followed. A suitable wire for ultrasonic bonding is Aluminum-Silicon alloy 99/1, Diameter .001", elongation 0.5 - 2% tensile strength 14 - 16g; but again, specific instructions/recommendations related to the bonding equipment used should be observed. An average bond pull strength of 4 - 6g, and a minimum limit of 2g should be maintained to assure mechanical bond quality.

UNUSED PADS

All pads marked with (•) are not to be bonded to by user. These pads are used by the factory for testing or adjusting (zener zap) electrical parameters.

ASSEMBLY SPECIFICATION A0018A
DIE INSPECTION – TEST INSPECTION C

I. OBJECTIVE

The purpose of this specification is to check the workmanship of monolithic microcircuits. (Procured as individual dice) to detect and eliminate die with defects which could lead to device failures in normal application.

II. POLICY

2.1 All die will be wafer probed at +25°C to ensure meeting electrical performance parameters.

2.2 When Test Condition C for visual inspection is specified, die shall be 100% inspected in accordance with the following procedure.

III. PROCEDURE

3.1 Each die shall be examined in a suitable sequence of observations and at the specified magnification to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition. The order in which criteria are presented is not a required order of examination. Inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface.

3.2 If a specified visual inspection requirement is in conflict with circuit design topology or construction which has been documented in the detail specification or design documentation and approved by the qualifying activity, the latter shall prevail. All references herein to silicon oxide or oxide shall also apply to silicon nitride or any other underlying passivation or material used in fabricating monolithic microcircuits. Wherever the criteria of "0.1 mil of oxide or metal" is used, a discernible line shall satisfy this requirement. After visual inspection, devices shall be stored in a dry, dust free, positive-pressure, inert, controlled environment.

3.3 Test Condition C visual examination shall be conducted on all monolithic microcircuits. The order of examination required in 3.3.1 through 3.3.5 may be varied at the discretion of the inspector. The inspection shall be performed within the range of 75X to 150X, unless otherwise specified.

3.3.1 Metallization

No die shall be acceptable that exhibits the following defects in the operating metallization:

3.3.1.1 Scratches, missing metallization

No scratches shall be acceptable in the interconnecting metallization which reduce the width of the conducting stripe by three-fourths or more of the minimum design width, provided the scratch exposes silicon oxide at any point along its length. Scratches, exposing silicon oxide, occurring in metallization contact cut areas shall not be acceptable if they leave three-fourths or more of the contact area isolated from the metallization. Scratches, exposing oxide and occurring on metallization bonding pads shall not be acceptable if they occur in such a manner as to isolate three-fourths or more of the bond area from the metallization. Missing metallization reducing the width by three-fourths of its narrowest designed width shall be cause for rejection.

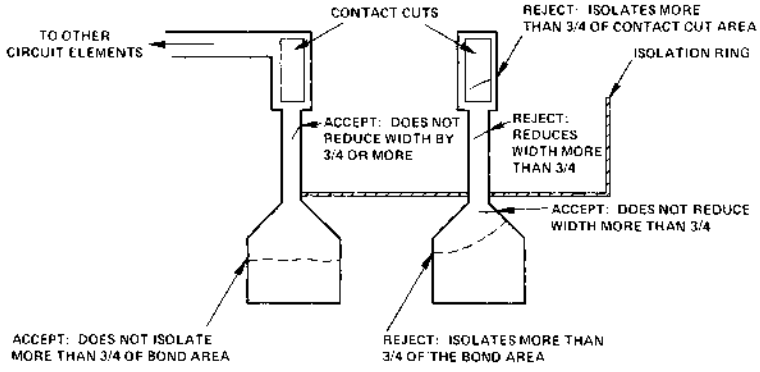


FIGURE 1

3.3.1.2 Metallization adherence

Any metallization lifting, peeling, or blistering that results in less than 1/4 of the minimum design width remaining undisturbed.

3.3.1.3 Bridged metallization

Reject all material on which silicon oxide is not visible between metallization stripes. Such reductions may be caused by smears, photolithographic defects or conductive foreign material (see figures 2 & 3).

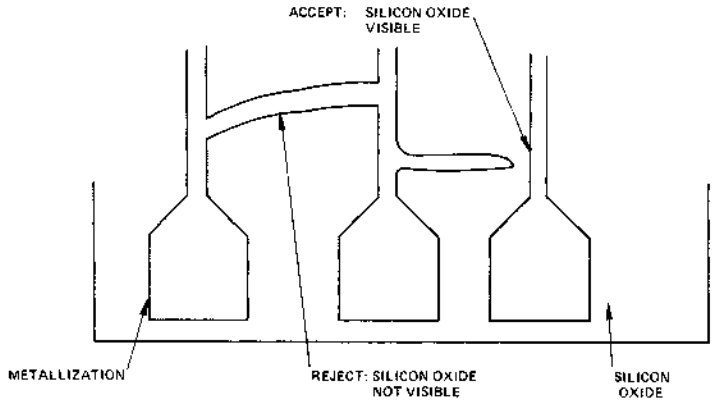


FIGURE 2

3.3.2 Foreign Material

Unattached metallic, abrasive or conductive material on the surface of the die shall not be acceptable. Attached metallic or conductive material shall not be acceptable on the surface of the die if silicon oxide is not visible between the particle and any adjacent metallization. A particle shall be considered attached if it cannot be removed by a nitrogen blow (20 psi). Conductive foreign material attached to the top surface of the overcoat shall be acceptable. This inspection will be conducted at low magnification (30X-60X).

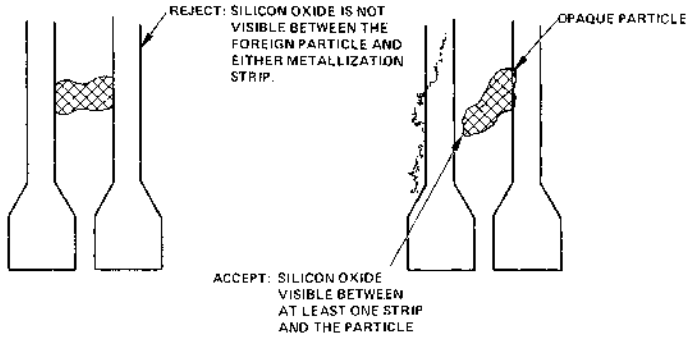


FIGURE 3

3.3.3 Scribing and die defects

No device shall be acceptable that exhibits:

(a) Less than 0.1 mil of passivation visible between operating metallization or bond periphery and edge of the die.

NOTE: Criteria of 3.3.3(a) can be excluded for peripheral metallization including bonding pads where the metallization is at the same potential as the die.

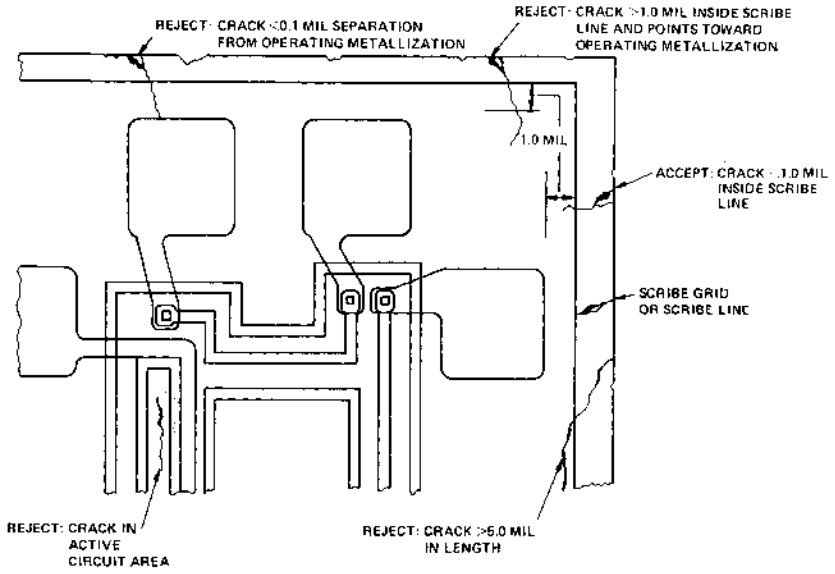
(b) A chipout in the active circuit area.

(c) Any crack in the active circuit area or a crack that exceeds 5.0 mils in length (see figure 4).

(d) Any crack that comes closer than 0.1 mil to any operating metallization or other active circuit area on the die (see figure 4).

(e) A crack, that exceeds 1.0 mil in length, inside the scribe grid or scribe line that points toward operating metallization or functional circuit elements (see figure 4).

(f) Any attached piece of an adjacent die protruding more than .003" (3 mils) from the edge of the die.



SCRIBING AND DIE DEFECTS
FIGURE 4

3.3.4 Overcoat

Overcoat is defined as a dielectric layer (glassivation) applied after metallization. No device shall be considered acceptable which exhibits any overcoat void which bridges any two operating circuit metallization areas or any operating circuit metallization to bare silicon. No device shall be acceptable that has glassivation covering more than 50% of any active bonding pad.

3.3.5 Probing

All bonding pads shall be inspected for evidence of probing. Any die having any active unprobed bonding pads shall be rejected.

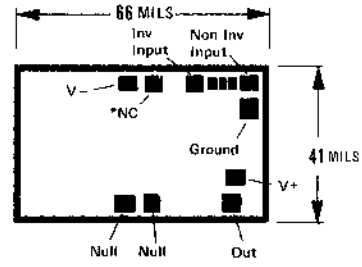
3.3.6 Dimensions

The length and width dimensions of the chip shall be inspected and must be within ±.003" of the catalog dimensions.

CMP-01
FAST PRECISION COMPARATOR

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Total Supply Voltage, V+ to V−	36V
Output to Ground	−5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Output Sink Current (Continuous Operation)	75 mA
Differential Input Voltage	±11V
Input Voltage (V_S = ±15V)	±15V
Output Short Circuit Duration – to ground	Indefinite
to V+	1 min.

CHIP LAYOUT AND DIMENSIONS



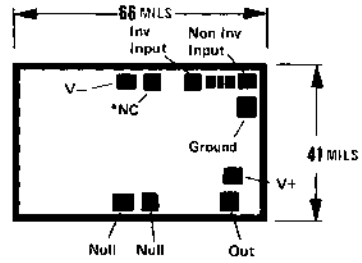
ELECTRICAL SPECIFICATIONS AT 25°C			CMP01-N		CMP01-G		
These specifications apply for V_S = ±15V unless otherwise noted.							
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5\,k\Omega$	–	0.8	–	2.8	mV
Input Offset Current	I_{OS}		–	25	–	80	nA
Input Bias Current	I_B		–	600	–	900	nA
Differential Input Resistance	R_{in}		3.0	–	1.0	–	MΩ
Input Voltage Range	CMVR		±12.5	–	±12.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	94	–	90	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	–	74	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, I_O = 320µA	2.4	–	–	–	V
		$V_{in} \geq 3mV$, I_O = 240µA	–	–	2.4	–	V
Saturation Voltage	V_{SAT}	I_{sink} = 6.4 mA	–	0.45	–	0.45	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_o = 30V	–	4.0	–	8.0	µA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	8.0	–	8.5	mA
Negative Supply Current	I−	$V_{in} \leq -10mV$	–	2.2	–	2.2	mA
Power Consumption	P_D	$V_{in} \leq -10mV$	–	153	–	161	mW
These specifications apply for V_S+ = 5V and V_S− = 0V unless otherwise noted.							
Input Offset Voltage	V_{OS}	$R_S \leq 5\,k\Omega$	–	1.5	–	3.5	mV
Input Offset Current	I_{OS}		–	21	–	65	nA

TYPICAL ELECTRICAL CHARACTERISTICS (V_S = ±15V)			CMP01-N	CMP01-G	
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{os}	R_S = 50Ω	1.5	1.8	µV/°C
Average Input Offset Current Drift	TCI_{os}		35	40	pA/°C
Response Time (T_A = +25°C)	t_r	100mV step, 5mV overdrive no load (no pull-up)	90	90	nsec

CMP-02
LOW INPUT CURRENT PRECISION COMPARATOR

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Total Supply Voltage, V+ to V−	36V
Output to Ground	−5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Output Sink Current (Continuous Operation)	75 mA
Differential Input Voltage	±11V
Input Voltage (V_S = ±15V)	±15V
Output Short Circuit Duration — to ground	Indefinite
to V+	1 min.

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			CMP02-N		CMP02-G		
These specifications apply for V_S = ±15V unless otherwise noted.							
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5\ k\Omega$	–	0.8	–	2.8	mV
		$R_S \leq 50\ k\Omega$	–	0.9	–	3.0	mV
Input Offset Current	I_{OS}		–	3.0	–	15	nA
Input Bias Current	I_B		–	50	–	100	nA
Differential Input Resistance	R_{in}		5.0	–	1.5	–	MΩ
Input Voltage Range	CMVR		±12.5	–	±12.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	94	–	90	–	dB
Power Supply Rejection Ratio	PSRR	5V ≤ V_S + ≤18V −18V ≤ V_S − ≤0V	80	–	74	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, I_o = 320μA	2.4	–	–	–	V
		$V_{in} \geq 3mV$, I_o = 240μA	–	–	2.4	–	V
Saturation Voltage	V_{SAT}	I_{sink} = 6.4 mA	–	0.45	–	0.45	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_o = 30V	–	4.0	–	8.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	8.0	–	8.5	mA
Negative Supply Current	I−	$V_{in} \leq -10mV$	–	2.2	–	2.2	mA
Power Consumption	P_D	$V_{in} \leq -10mV$	–	153	–	161	mW
These specifications apply for V_S+ = 5V and V_S− = 0V unless otherwise noted.							
Input Offset Voltage	V_{OS}	$R_S \leq 5\ k\Omega$	–	1.5	–	3.5	mV
Input Offset Current	I_{OS}		–	3.0	–	14	nA

TYPICAL ELECTRICAL CHARACTERISTICS (V_S = ±15V)			CMP02-N	CMP02-G	
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{os}	R_S = 50Ω	1.5	1.8	μV/°C
Average Input Offset Current Drift	TCI_{os}		4.0	5.0	pA/°C
Response Time (T_A = +25°C)	t_r	100mV step, 5mV overdrive no load (no pull-up)	160	160	nsec

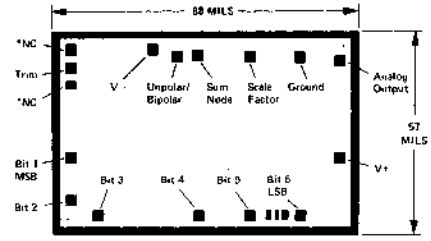
DAC-01
6 BIT MONOLITHIC D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	−65°C to +150°C
V+ Supply Voltage to Ground	0 to +18V
V− Supply Voltage to Ground	0 to −18V
Logic Input to Ground	−0.7 to +6V
Output Short Circuit Duration	Indefinite

NOTE: Short circuit may be to ground or either supply. Rating applies to +150°C chip temperature.

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

Parameter	Symbol	Test Conditions	DAC01-N BIPOLAR AND UNIPOLAR Min	DAC01-N BIPOLAR AND UNIPOLAR Max	DAC01-GR UNIPOLAR ONLY Min	DAC01-GR UNIPOLAR ONLY Max	Units
Nonlinearity		V_S = ±15V	—	±0.4	—	±0.4	%
Internal Reference Voltage	V_{MCR}	V_S = ±15V	6.65	6.76	6.4	6.9	V
Zero Scale Voltage	V_{ZS}	V_S = ±15V	—	±.021	—	±.035	V

ELECTRICAL SPECIFICATIONS AT 25°C IN COMMON TO ALL GRADES

These specifications apply for V_S = ±15V unless otherwise noted.

Parameter	Test Conditions	Min	Max	Units
Unipolar Full Scale Output Voltage (All Models)	2KΩ load, logic ≤ 0.0V, short V− to Full Scale Trim, Unipolar/ Bipolar to Ground, and Scale Factor to Sum Node.	10.00	11.75	V
Bipolar Output Voltage	2KΩ Load, Short Sum Node to Unipolar/Bipolar.			
±5 Volt Range (Except DAC-01-GR)	Short V− to Full Scale Trim and Scale Factor to Sum Node.			
V_{FS+}	Logic Inputs = 0V	+4.93	+5.94	V
V_{FS-}	Logic Inputs = 3.0V	−5.94	−4.93	V
±10 Volt Range (Except DAC-01-GR)	Open Scale Factor			
V_{FS+}	Logic Inputs = 0V	+9.78	+11.89	V
V_{FS-}	Logic Inputs = 3.0V	−11.89	−9.78	V
Bipolar Offset Voltage ±1/2 (I V_{FS+} I−I V_{FS-} I)	±5 Volt Range	—	±70	mV
	±10 Volt Range	—	±140	mV
Resolution		6	6	bits
Logic Input "0"		—	0.5	V
Logic Input "1"		2.1	—	V
Logic Input Current, Each Input	V_{IN} = +2.1V	—	±8.0	µA
Power Supply Rejection	+12V ≤ V_S ≤ ±18V V_{FS} ≅ 10.0 V	—	0.15	%FS/V
Power Consumption	No Load	—	250	mW

TYPICAL ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	DAC-01-N Typical	DAC01-G Typical	DAC01-GR Typical	Units
Settling Time	t_s	To ±1/2 LSB	1.5	1.5	1.5	µsec
Full Scale Tempco	TCV_{FS}	V_S = ±15V	60	90	90	ppm/°C

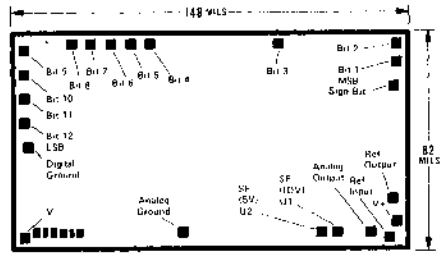
DAC-02
10 BIT PLUS SIGN D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	-65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
V- Supply to Analog Ground	0 to -18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	-5V to (V_+ – .7V)
Internal Reference Output Current	300 μA
Reference Input Voltage	0 to +10V
Output Short Circuit Duration	Indefinite

(Short circuit may be to ground or either supply.)

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for V_S = ±15V and +10V Full Scale Output unless otherwise noted.

Parameter	Test Conditions	DAC02-N Min	DAC02-N Max	DAC02-G Min	DAC02-G Max	DAC02-GR Min	DAC02-GR Max	Units
Resolution Bits 11 and 12 not normally used	Bipolar Output	13	13	13	13	13	13	bits
	Unipolar Output	12	12	12	12	12	12	bits
Monotonicity		9	–	8	–	7	–	bits
Nonlinearity		–	±0.1	–	±0.2	–	±0.4	% FS
Zero Scale Offset	Sign Bit High, All Other Inputs Low	–	±10	–	±10	–	±10	mV
Zero Scale Symmetry	±10V Full Scale	–	±5.0	–	±5.0	–	±10	mV
Full Scale Bipolar Symmetry	±10V Full Scale	–	±60	–	±60	–	±80	mV
Power Supply Rejection	V_S = +12V to ±18V	–	0.05	–	0.05	–	0.1	% V_{FS}/V
Power Dissipation	I_{OUT} = 0	–	300	–	300	–	350	mW
Logic Input "0"		–	0.8	–	0.8	–	0.8	V
Logic Input "1"		2.0	–	2.0	–	2.0	–	V
Full Scale Output Voltage	V_{FS+} (Sign Bit High)	10	11.5	10	11.5	10	11.5	V
	V_{FS-} (Sign Bit Low)	-11.5	-10	-11.5	-10	-11.5	-10	V

TYPICAL ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and +10V Full Scale Output unless otherwise noted.

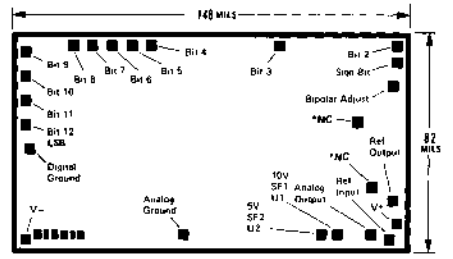
Parameter	Symbol	Test Conditions	DAC02-N Typical	DAC02-G Typical	DAC02-GR Typical	Units
Full Scale Tempco	TCV_{FS}	Internal Reference	60	60	90	ppm/°C
Settling Time (T_A = 25°C)	t_s	To ±1/2 LSB 10 Volt Step	1.5	1.5	1.5	μsec
Logic Input Current		T_A = 25°C	1.0	1.0	1.0	μA

NOTE: Voltage Output Range programmable by connecting SF[1](10V) to Analog Output for 10 volt range. Jumper from SF[2](5V) to Analog Output sets device to 5 volt range.

DAC-04
TWO'S COMPLEMENT 10 BIT D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
V+ Supply to Analog Ground	0 to +18V
V- Supply to Analog Ground	0 to -18V
Analog Ground to Digital Ground	0 to ±0.5V
Logic Inputs to Digital Ground	-5V to (V_+ – .7V)
Internal Reference Output Current	300μA
Reference Input Voltage	0 to +10V
Output Short Circuit Duration	Indefinite
(Short circuit may be to ground or either supply)	

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C		DAC04-N		DAC04-G		DAC04-GR		
These specifications apply for V_S = ±5V Full Scale Output unless otherwise noted.								
Parameter	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Resolution	Bipolar Output	12	12	12	12	12	12	bits
Monotonicity		9	–	8	–	7	–	bits
Nonlinearity		–	±0.1	–	±0.2	–	±0.4	% FS
Bipolar Offset Voltage	Short Reference Input to Reference Output and Bipolar Adjust	-5.0	-0.1	-5.0	-0.1	-5.0	-0.1	% range
Power Supply Rejection	V_S = ±12V to ±18V	–	0.1	–	0.1	–	–	$\%V_{FS}/V$
Power Dissipation	I_{OUT} = 0	–	300	–	300	–	350	mW
Logic Input "0"		–	0.8	–	0.8	–	0.8	V
Logic Input "1"		2.0	–	2.0	–	2.0	–	V
Full Scale Output Voltage	Short Reference Input to Reference Output	10.0	11.5	10.0	11.5	10.0	11.5	V

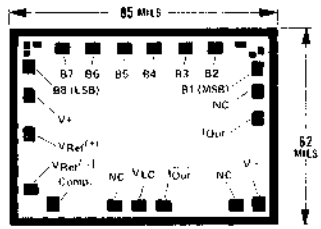
TYPICAL ELECTRICAL CHARACTERISTICS		DAC04-N	DAC04-G	DAC04-GR	
These specifications apply for V_S = ±15V and ±5V Full Scale Output unless otherwise noted.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Full Scale Tempco	TCV_{FS}	Internal Reference	60	60	90	ppm/°C
Settling Time (T_A = 25°C)	t_s	To ±½LSB 10 Volt Step	1.5	1.5	1.5	μsec
Logic Input Current		T_A = 25°C	1.0	1.0	1.0	μA

NOTE: See DAC-02 note

DAC-08
8 BIT HIGH SPEED MULTIPLYING D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
V+ Supply to V- Supply	36V
Logic Inputs	V- to V- plus 36V
V_{LC}	V- to V+
Reference Inputs	V- to V+
Reference Input Differential Voltage	±18V
Reference Input Current	5.0mA

CHIP LAYOUT AND DIMENSIONS



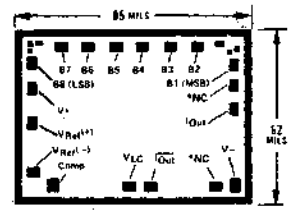
ELECTRICAL SPECIFICATIONS AT 25°C			DAC08-N		DAC08-G		DAC08-GR		
These specifications apply for V_S = ±15V and I_{REF} = 2.0 mA unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Resolution			8	8	8	8	8	8	bits
Monotonicity			8	8	8	8	8	8	bits
Nonlinearity			–	±0.1	–	±0.19	–	±0.39	% FS
Output Voltage Compliance	V_{OC}	Full scale current change < ½ LSB	-10	+18	-10	+18	-10	+18	V
Full Scale Current	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ	1.94	2.04	1.94	2.04	1.94	2.04	mA
Full Scale Symmetry	I_{FSS}		–	±8.0	–	±8.0	–	±16	μA
Zero Scale Current	I_{ZS}		–	2.0	–	±4.0	–	4.0	μA
Output Current Range	I_{FSR}	V- = -5.0V V- = -7.0V to -18V	0 0	2.1 4.2	0 0	2.1 4.2	0 0	2.1 4.2	mA mA
Logic "0" Input Level	V_{IL}		–	0.8	–	0.8	–	0.8	V
Logic "1" Input Level	V_{IH}		2.0	–	2.0	–	2.0	–	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	V_{LC} = 0V V_{IN} = -10V to +0.8V V_{IN} = 2.0V to 18V	 – –	 ±10 ±10	 – –	 ±10 ±10	 – –	 +10 ±10	 μA μA
Logic Input Swing	V_{IS}	V- = -15V	-10	+18	-10	+18	-10	+18	V
Reference Bias Current	I_{15}		–	-3.0	–	-3.0	–	-3.0	μA
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V- = -4.5V to -18V I_{REF} = 1.0 mA	– –	0.01 0.01	– –	0.01 0.01	– –	0.01 0.01	%/% %/%
Power Supply Current	I+ I-	V_S = ±18V I_{REF} = 2.0 mA	– –	3.8 -7.8	– –	3.8 7.8	– –	3.8 -7.8	mA mA
Power Dissipation	P_D	V_S = -18V I_{REF} = 2.0 mA	–	174	–	174	–	174	mW

TYPICAL ELECTRICAL CHARACTERISTICS			DAC-08N	DAC-08G	DAC-08GR	
These specifications apply for V_S = ±15V and I_{REF} = 2.0 mA unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Reference Input Slew Rate	dI/dt		8.0	8.0	8.0	mA/μsec
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any bit	35	35	35	nsec
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF, T_A = 25°C	100	100	100	nsec

DAC-20
2 DIGIT BCD HIGH SPEED MULTIPLYING DAC

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
V+ Supply to V− Supply	36V
Logic Inputs	V− to V− Plus 36V
V_{LC}	V− to V+
Reference Inputs	V− to V+
Reference Input Differential Voltage	±18V
Reference Input Current	5.0mA

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			DAC-20-N		DAC-20-G		
These specifications apply for V_S = ±15V and I_{REF} = 2.0 mA unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.							
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Resolution		BCD 0 to 99 steps	2	2	2	2	Digits
Monotonicity		BCD 99 steps	2	2	2	2	Digits
Nonlinearity	NL	FS = 1001 1001	–	±1/4	–	±1/2	LSB
Output Voltage Compliance	V_{OC}	Full scale current change <1/2 LSB	−10	+18	−10	+18	V
Full Scale Current	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ	1.96	2.00	1.92	2.04	mA
Zero Scale Current	I_{ZS}		–	2.5	–	5.0	μA
Output Current Range	I_{FSR}	V− = −5.0V V− = −7.0V to −18V	0 0	2.1 4.2	0 0	2.1 4.2	mA mA
Logic "0" Input Level	V_{IL}		–	0.8	–	0.8	V
Logic "1" Input Level	V_{IH}		2.0	–	2.0	–	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	V_{LC} = 0V V_{IN} = −10V to +0.8V V_{IN} = 2.0V to 18V	 – –	 ±10 ±10	 – –	 ±10 ±10	 μA μA
Logic Input Swing	V_{IS}	V− = −15V	−10	+18	−10	+18	V
Reference Bias Current	I_{15}		–	−3.0	–	−3.0	μA
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V I_{REF} = 1.0mA	– –	±0.03 ±0.03	– –	±0.03 ±0.03	%/% %/%
Power Supply Current	I+ I−	V_S = ±18V I_{REF} ≤ 2.0 mA	– –	3.8 −7.8	– –	3.8 −7.8	mA mA
Power Dissipation	P_D	V_S = ±18V I_{REF} ≤ 2.0 mA	–	194	–	194	mW

TYPICAL ELECTRICAL CHARACTERISTICS			DAC-20-N	DAC-20-G	
These specifications apply for V_S = ±15V and I_{REF} = 2.0 mA unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Units**
Reference Input Slew Rate	dI/dt		8.0	8.0	mA/μsec
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any bit	35	35	nsec
Settling Time	t_s	To ±1/2 LSB, all bits switched ON or OFF, T_A = 25°C	100	100	nsec

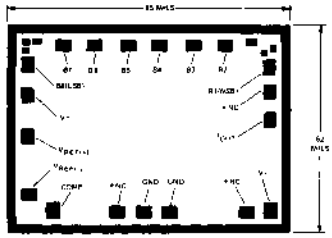
1408A
8 BIT HIGH SPEED MULTIPLYING D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	-65°C to +150°C
V+ Supply	+5.5V
V- Supply	-16.5V
Logic Inputs	0 to +5.5V
Applied Output Voltage (V_O)	+0.5V to -5.2V
Reference Inputs	V- to V+
Reference Input Current	5.0mA

NOTE: No range control required.

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

1408A–G

These specifications apply for V+ = 5V, V- = -15V, I_{REF} = 2.0mA unless otherwise specified.

Parameter	Symbol	Test Conditions		Min	Max	Units
Resolution				8	8	bits
Monotonicity				8	8	bits
Nonlinearity				–	±0.19	% FS
Output Voltage Compliance	V_{OC}	Full scale current change <½ LSB	V- = -5V	-0.6	+0.5	V
			$V_{below-10V}$	-5.0	+0.5	V
Full Scale Current	I_{FS}	V_{REF} = 2.000V, R_{14}, R_{15} = 1.000kΩ		1.9	2.1	mA
Zero Scale Current	I_{ZS}	(All bits low)		–	4.0	μA
Output Current Range	I_{FSR}	V- = -5.0V V- = -6.0 to -15V		– –	2.1 4.2	mA mA
Logic "0" Input Level	V_{IL}			–	0.8	V
Logic "1" Input Level	V_{IH}			2.0	–	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	 Low Level, V_{IL} = 0.8V High Level, V_{IH} = 5.0V		 – –	 ±10 ±10	 μA μA
Reference Bias Current	I_{15}			–	-3.0	μA
Output Current Power Supply Sensitivity	$PSSI_{O-}$			–	2.7	μA/V
Power Supply Current (All bits low)	I+ I-			– –	+14 -13	mA mA
Power Supply Voltage Range	V+ (R) V- (R)			+4.5 -4.5	+5.5 -16.5	mA mA
Power Dissipation (All bits low)	P_D	V- = -5.0V V- = -15V		– –	135 265	mW mW

TYPICAL ELECTRICAL CHARACTERISTICS

1408A–G

These specifications apply for V+ = +5V, V- = -15V, V_{LC} and $\overline{I_{OUT}}$ connected to ground, and I_{REF} = 2.0mA, unless otherwise specified. Output characteristics refer to I_{OUT} only.

Parameter	Symbol	Test Conditions	Typical	Units
Reference Input Slew Rate	di/dt		4.0	mA/μsec
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any bit	30	nsec
Settling Time	t_s	To ± ½LSB, all bits switched ON or OFF, T_A = 25°C	250	nsec

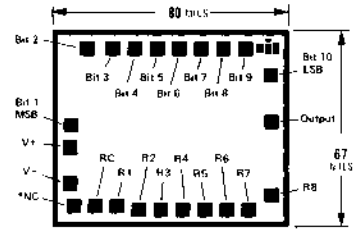
DAC-100
8 & 10 BIT TWO-CHIP D/A CONVERTER
DAI-01 10 BIT D/A CURRENT SOURCE WITH REFERENCE

A COMPLETE 10 BIT D/A CONVERTER EQUIVALENT TO THE DAC-100 SERIES IS COMPRISED OF ONE DAI-01 PLUS ONE DAR-01 SERIES CHIP

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	-65°C to +150°C
V+ Supply to V- Supply	0 to +36V
V+ Supply to Output	0 to +18V
V- Supply to Output	0 to -18V
Logic Inputs to Output	-1V to +6V

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

ELECTRICAL SPECIFICATIONS AT 25°C			DAI01-N		DAI01-G		DAI01-GR		
These specifications apply when connected to an ideal DAR-01.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Nonlinearity		V_S = ±15V	—	±0.05	—	±0.05	—	±0.2	%
Internal Reference Voltage	V_{MCR}	V_S = ±15V	6.600	6.825	6.45	6.90	6.45	6.90	V

ELECTRICAL SPECIFICATIONS AT 25°C IN COMMON TO ALL GRADES

These specifications apply for V_S = ±15V and when connected to an ideal DAR-01 unless otherwise noted.

Parameter	Test Conditions	Min	Max	Units
Resolution		10	10	bits
Full Scale Output Current	All bits low, V- connected to FS Adjust	1840	2274	µA
Zero Scale Output Current	All bits high, V- connected to FS Adjust	—	±0.25	µA
Logic Input "0"	Measured with respect to output	—	0.7	V
Logic Input "1"	Measured with respect to output	2.1	—	V
Supply Current	All bits high, V- connected to FS Adjust	—	8.33	mA
Power Supply Rejection	V_S = ±6V to ±18V	—	0.1	%FS/V

TYPICAL ELECTRICAL CHARACTERISTICS

TYPICAL ELECTRICAL CHARACTERISTICS		DAI01-N	DAI01-G	DAI01-GR	
These specifications apply for V_S = ±15V, and when connected to an ideal DAR-01 unless otherwise noted.					
Parameter	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Full Scale Tempco	(Note)	±60	±120	±120	ppm/°C

NOTE: Full Scale Tempco is defined as the change in output voltage measured in the test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

DAC-100
8 & 10 BIT TWO-CHIP D/A CONVERTER
DAR-01 10 BIT RESISTOR NETWORK

A COMPLETE 10 BIT D/A CONVERTER EQUIVALENT TO THE DAC-100 SERIES IS COMPRISED OF ONE DAI-01 PLUS ONE DAR-01 SERIES CHIP.

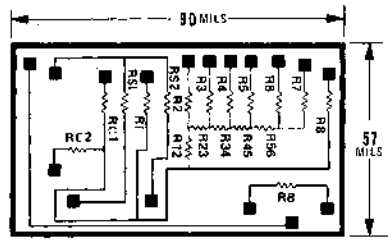
ABSOLUTE MAXIMUM RATINGS

Chip Temperature	-65°C to +150°C
Voltage Across Any Resistor	15V

NOMINAL RESISTOR VALUES

R1 thru R7	3.2KΩ	RC2	9.956KΩ
R8	12.8KΩ	RS1, RS2	2.44KΩ
R12 thru R56	1.6KΩ	RB	6.12KΩ
RC1	1.6KΩ		

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

ELECTRICAL SPECIFICATIONS AT 25°C	DAR01-N	DAR01-G	DAR01-GR	

The following specifications apply for the R2R Ladder Network comprised of R1-R8, R12, R23, R34, R45, and R56 when connected to an ideal DA1-01.

Parameter	Test Conditions	Maximum	Maximum	Maximum	Units
Nonlinearity	VR1 = 3.2V	±0.035	±0.05	±0.1	%

ELECTRICAL SPECIFICATIONS AT 25°C IN COMMON TO ALL GRADES

The following specifications apply with VR1 = 3.2V.

Parameter	Test Conditions	Minimum	Maximum	Units
Resistance R1	Absolute Measurement	2.56	3.84	KΩ
Ratio RC1 to R1	Ideal = 1 to 1	-1.0	+1.0	%
Ratio R1 to RS1	Ideal = 1.31147 to 1	-1.0	+1.0	%
Ratio R1 to RS2	Ideal = 1.31147 to 1	-1.0	+1.0	%
Ratio RB to R1	Ideal = 1.9125 to 1	-1.0	+1.0	%

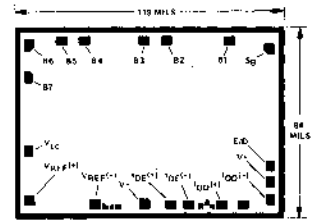
TYPICAL ELECTRICAL CHARACTERISTICS IN COMMON TO ALL GRADES

Parameter	Conditions	Typical	Units
Absolute Temperature Coefficient	All resistors	±120	ppm/°C
Tracking Temperature Coefficient	All resistors with respect to R1	3.0	ppm/°C

DAC-76
COMDAC™ COMPANDING D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
V+ Supply to V− Supply	36V
V_{LC} Swing	V− plus 8V to V+
Analog Current Outputs	V− plus 8V to V− plus 36V
Reference Inputs	V− to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25 mA
Logic Inputs	V− plus 8V to V− plus 36V

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

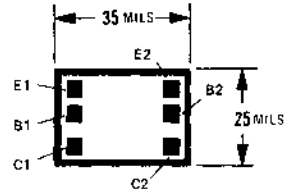
These specifications apply for V_S = ±15V, I_{REF} = 528 µA, and for all 4 outputs unless otherwise specified.

Parameter	Symbol	Test Conditions	DAC76-N Min	DAC76-N Max	DAC76-G Min	DAC76-G Max	Units
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	dB
Monotonicity		Sign Bit + or −	128	—	128	—	Steps
Chord Endpoint Accuracy		Error relative to ideal values at I_{FS} = 2007.75µA	—	±1/2	—	±1	Step
Step Nonlinearity		Step error within chord	—	±1/2	—	+1	Step
Encode Current		Additional Output Encode/Decode = 1	3/8	5/8	1/4	3/4	Step
Output Voltage Compliance	V_{OC}	$\Delta I_{FS} \leq$ 1/2 step	−5.0	+18	−5.0	+18	Volts
Full Scale Current Deviation From Ideal	$I_{FS}(D)$ $I_{FS}(E)$	V_{REF} = 10.000V R11 = 18.94 kΩ R12 = 20 kΩ	— —	±1/2 ±1/2	— —	±1 ±1	Step Step
Full Scale Symmetry Error	$I_O(+)-I_O(-)$	Decode or Encode Pair	—	±1/8	—	±1/4	Step
Zero Scale Current	I_{ZS}	Measured at Selected Output with 000 0000 Input	—	±1/4	—	±1/2	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/D and SB	—	50	—	50	nA
Output Current Range	I_{FSR}		0	4.2	0	4.2	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = 0V	 — 2.0	 0.8 —	 — 2.0	 0.8 —	 Volts Volts
Logic Input Current	I_{IN}	V_{IN} = −5V to +18V	—	40	—	40	µA
Logic Input Swing	V_{IS}	V− = −15V	−5	+18	−5	+18	Volts
Reference Bias Current	I_{12}		—	−4.0	—	−4.0	µA
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5 to 18V, V− = −15V V− = −10.8V to −18V, V+ = 15V	— —	±1/2 ±1/2	— —	±1/2 ±1/2	Step Step
Power Supply Current	I+ I−	V_S = +5V, −15V, I_{FS} = 2.0 mA	— —	4.0 −8.8	— —	4.0 −8.8	mA mA
Power Supply Current	I+ I−	V_S = ±15V, I_{FS} = 2.0 mA	— —	4.0 −8.8	— —	4.0 −8.8	mA mA
Power Dissipation	P_D	V_S = +5V, −15V, I_{FS} = 2.0 mA V_S = ±15V, I_{FS} = 2.0 mA	— —	152 192	— —	152 192	mW mW

MAT-01
ULTRA-MATCHED MONOLITHIC DUAL TRANSISTOR

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Emitter-Base Voltage (BV_{EBO})	5V
Collector Current (I_C)	25mA
Emitter Current (I_E)	25mA
Collector-Base Voltage (BV_{CBO})	45V
Collector-Emitter Voltage (BV_{CEO})	45V
Collector-Collector Voltage (BV_{CC})	45V
Emitter-Emitter Voltage (BV_{EE})	45V

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			MAT01-N		
These specifications apply for V_{CB} = 15V and I_C = 10μA unless otherwise noted.					
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Units**
Breakdown Voltage	BV_{CEO}		45	–	V
Offset Voltage	V_{OS}		–	0.5	mV
Offset Current	I_{OS}		–	3.2	nA
Bias Current	I_B		–	40	nA
Current Gain	h_{FE}		250	–	–
Current Gain Match	Δh_{FE}		–	8.0	%
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	–	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	–	70	pA/V
Collector-Base-Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0	–	200	pA
Collector-Emitter-Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0	–	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	–	0.25	V

TYPICAL ELECTRICAL CHARACTERISTICS			MAT01-N	
These specifications apply for V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.				
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Units**
Average Offset Voltage Drift	TCV_{OS}		0.35	μV/°C
Average Offset Current Drift	TCI_{OS}		15	pA/°C
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1)	2.0	μV/Mo
		Long Term (Note 2)	0.2	μV/Mo

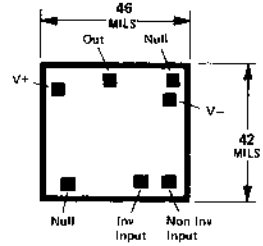
NOTE 1: Exclude first hour of operation to allow for stabilization of external circuitry.

NOTE 2: Parameter describes long term average drift trend after first month of operation.

OP-01
HIGH SPEED OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Total Supply Voltage	
OP01-N and OP01-G	±22V
OP01-GR	±20V
Differential Input Voltage	±30V
Input Voltage	±15V
Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



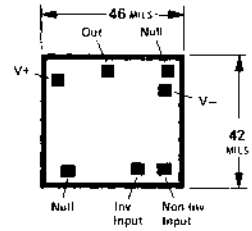
ELECTRICAL SPECIFICATIONS AT 25°C			OP01-N		OP01-G		OP01-GR		
These specifications apply for V_S = ±15V unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.7	–	2.0	–	5.0	mV
Input Offset Current	I_{OS}		–	2.0	–	5.0	–	20	nA
Input Bias Current	I_B		–	30	–	50	–	100	nA
Input Voltage Range	CMVR		±12.0	–	±12.0	–	±12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 50k\Omega$	90	–	80	–	80	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V $R_S \leq 50k\Omega$	90	–	80	–	80	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	– –	±12.5 ±12.0	– –	±12.5 ±12.0	– –	V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	50	–	50	–	25	–	V/mV
Power Consumption	P_D	V_{OUT} = 0	–	60	–	90	–	90	mW

TYPICAL ELECTRICAL CHARACTERISTICS			OP01-N	OP01-G	OP01-GR	
These specifications apply for V_S = +15V, T_A = 25°C unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Slew Rate	SR	A_{VCL} = -1	18	18	18	V/µs
Settling Time to 0.1%		V_{IN} = 5V A_V = -1 R_L = 2kΩ C_L = 50pF	1.0	1.0	1.0	µsec
Large Signal Bandwidth			250	250	250	KHz
Small Signal Bandwidth			2.5	2.5	2.5	MHz
Risetime		V_{IN} = 50mV A_V = -1 R_L = 2kΩ C_L = 50pF	150	150	150	nsec

OP-02 (IMPROVED 741) COMPENSATED OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
OP02-N and OP02-G	±22V
OP02-GR	±18V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			OP02-N		OP02-G		OP02-GR		
			V_S = ±15V unless otherwise specified		±5V ≤ V_S ≤ ±20V unless otherwise specified		V_S = ±15V unless otherwise specified		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.5	–	2.0	–	6.0	mV
Input Offset Current	I_{OS}		–	2.0	–	5.0	–	200	nA
Input Bias Current	I_B		–	30	–	50	–	500	nA
Input Voltage Range	CMVR	V_S = ±15V	±12.0	–	±12.0	–	±12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 50k\Omega$	90	–	80	–	70	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V $R_S \leq 50k\Omega$	90	–	80	–	76	–	dB
Maximum Output Voltage Swing (V_S = ±15V)	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12.0 ±12.0	– –	±12.0 ±10.0	– –	±12.0 ±10.0	– –	V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V V_S = ±15V	100	–	50	–	25	–	V/mV
Power Consumption	P_D	V_{OUT} = 0, V_S = ±15V	–	60	–	85	–	85	mW
Slew Rate	SR	R_L = 2kΩ, C_L = 100pF	0.25	–	0.25	–	–	–	V/μs

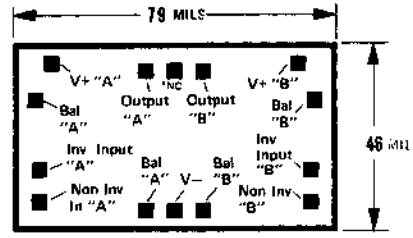
TYPICAL ELECTRICAL CHARACTERISTICS			OP02-N	OP02-G	OP-02-GR	
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Risetime		A_V = +1 V_{IN} = 20mV R_L = 2kΩ C_L = 50pF	200	200	200	nsec
Overshoot		A_V = +1 V_{IN} = 20mV R_L = 2kΩ C_L = 50pF	5.0	5.0	5.0	%

OP-04 (IMPROVED 747) DUAL OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
OP04-N and OP04-G	±22V
OP04-GR	±18V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for each amplifier unless otherwise noted.

Parameter	Symbol	Test Conditions	OP04-N V_S = ±15V unless otherwise specified Min	OP04-N Max	OP04-G ±5V ≤ V_S ≤ ±20V unless otherwise specified Min	OP04-G Max	OP04-GR V_S = ±15V unless otherwise specified Min	OP04-GR Max	Units
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.75	–	2.0	–	6.0	mV
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 100\Omega$	–	1.0	–	–	–	–	mV
Input Offset Current	I_{OS}		–	2.0	–	5.0	–	200	nA
Input Bias Current	I_B		–	50	–	50	–	500	nA
Input Voltage Range	CMVR	V_S = ±15V	±12.0	–	±12.0	–	±12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 50k\Omega$	90	–	80	–	70	–	dB
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±CMVR $R_S \leq 100\Omega$	94	–	–	–	–	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V $R_S \leq 50k\Omega$	90	–	80	–	76	–	dB
Maximum Output Voltage Swing (V_S = ±15V)	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12.0 ±12.0	– –	±12.0 ±10.0	– –	±12.0 ±10.0	– –	V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V V_S = ±15V	100	–	100	–	25	–	V/mV
Power Consumption (Both Amplifiers)	P_D	V_{OUT} = 0 V_S = ±15V	–	120	–	170	–	170	mW
Slew Rate	SR	R_L = 2kΩ, C_L = 100pF	0.4	–	0.4	–	–	–	V/μs
Channel Separation	CS		100	–	100	–	–	–	dB

TYPICAL ELECTRICAL CHARACTERISTICS

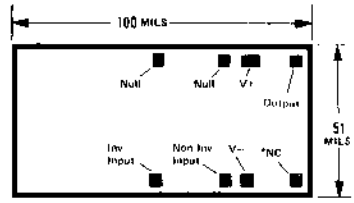
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP04-N Typical	OP04-G Typical	OP04-GR Typical	Units
Risetime		A_V = +1 V_{IN} = 20mV R_L = 2kΩ, C_L = 50pF	200	200	200	nsec
Overshoot		A_V = +1 V_{IN} = 20mV R_L = 2kΩ, C_L = 50pF	5.0	5.0	5.0	%

OP-05
COMPENSATED INSTRUMENTATION OP AMP

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			OP05-N		OP05-G		OP05-GR		
These specifications apply for V_S = ±15V unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}		–	0.5	–	0.5	–	1.3	mV
Input Offset Current	I_{OS}		–	±2.8	–	±3.8	–	±6.0	nA
Input Bias Current	I_B		–	±3.0	–	±4.0	–	±7.0	nA
Input Resistance Differential Mode	R_{IN}		20	–	15	–	8.0	–	MΩ
Input Voltage Range	CMVR		±13.5	–	±13.5	–	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	114	–	110	–	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	–	94	–	90	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	– – –	±12.5 ±12.0 ±10.5	– – –	±12.0 ±11.5 –	– – –	V V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	200	–	200	–	120	–	V/mV
Differential Input Voltage			–	±30	–	±30	–	±30	V
Power Consumption (V_{OUT} = 0V)	P_D	V_S = ±15V	–	120	–	120	–	150	mW

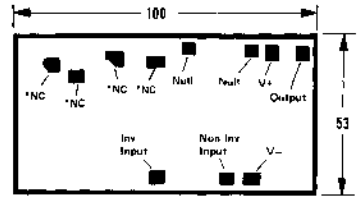
TYPICAL ELECTRICAL CHARACTERISTICS		OP05-N	OP05-G	OP05-GR	
These specifications apply for V_S = ±15V.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.7	0.7	1.2	µV/°C
Nulled Input Offset Voltage Drift	TCV_{OSN}	$R_S \leq 50\Omega$ R_P = 20kΩ	0.3	0.3	0.4	µV/°C
Average Input Offset Current Drift	TCI_{OS}		8.0	8.0	12	pA/°C

OP-07
ULTRA-LOW OFFSET VOLTAGE OP AMP

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for V_S = ±15V unless otherwise noted.

Parameter	Symbol	Test Conditions	OP07-N Min	OP07-N Max	OP07-G Min	OP07-G Max	OP07-GR Min	OP07-GR Max	Units
Input Offset Voltage	V_{OS}		–	95	–	150	–	1300	µV
Input Offset Current	I_{OS}		–	±2.8	–	±6.0	–	±6.0	nA
Input Bias Current	I_B		–	±3.0	–	±7.0	–	±7.0	nA
Input Resistance Differential Mode	R_{IN}		20	–	8.0	–	8.0	–	MΩ
Input Voltage Range	CMVR		±13.0	–	±13.0	–	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	–	100	–	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	–	90	–	90	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	– – –	±12.0 ±11.5 –	– – –	±12.0 ±11.5 –	– – –	V V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	200	–	120	–	120	–	V/mV
Differential Input Voltage			–	±30	–	±30	–	±30	V
Power Consumption (V_{OUT} = 0V)	P_D	V_S = ±15V	–	120	–	120	–	150	mW

TYPICAL ELECTRICAL CHARACTERISTICS

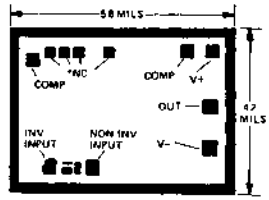
These specifications apply for V_S = ±15V.

Parameter	Symbol	Test Conditions	OP07-N Typical	OP07-G Typical	OP07-GR Typical	Units
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.5	1.2	µV/°C
Nulled Input Offset Voltage Drift	TCV_{OSN}	$R_S \leq 50\Omega$ R_P = 20kΩ	0.3	0.4	0.4	µV/°C
Average Input Offset Current Drift	TCI_{OS}		8.0	12	12	pA/°C

OP-08
PRECISION LOW INPUT CURRENT OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Supply Voltage	
OP-08-N	±20V
OP-08-GR and G	±18V
Differential Input Current	±10mA
Input Voltage	±15V Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



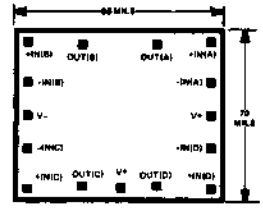
ELECTRICAL SPECIFICATIONS AT 25°C			OP-08-N		OP-08-G		OP-08-GR		
These specifications apply for V_S = ±15V, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}		–	0.3	–	0.3	–	1.0	mV
Input Offset Current	I_{OS}		–	0.2	–	0.4	–	0.5	nA
Input Bias Current	I_B		–	2.0	–	4.0	–	5.0	nA
Input Voltage Range	CMVR		±14	–	±14	–	±14	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ± CMVR	104	–	102	–	84	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V	104	–	102	–	84	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±13 ±10	–	±13 ±10	–	±13 ±10	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, V_O = 10V $R_L \geq 2k$	– 50	–	– 30	–	40 –	–	V/mV
Input Resistance	R_{in}		25	–	13	–	10	–	MΩ
Supply Current	I_S	I_{out} = 0, V_{out} = 0	–	0.6	–	0.6	–	0.8	mA

TYPICAL ELECTRICAL CHARACTERISTICS			OP-08-N	OP-08-G	OP-08-GR	
These specifications apply for V_S = ±15V.						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{os}		1.0	1.0	1.5	µV/°C
Average Input Offset Current Drift	TCI_{os}		0.5	1.0	1.0	pA/°C

OP-09
QUAD OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Supply Voltage	
OP-09N, OP-09G	±22V
Differential Input Voltage	±30V
Input Voltage	±15V
(For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.)	
Output Short Circuit Duration to Ground	Continuous
(One amplifier only, I_{SC} = 45mA typical.)	

CHIP LAYOUT AND DIMENSIONS

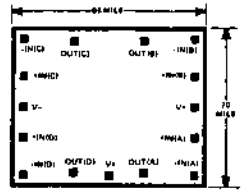


ELECTRICAL SPECIFICATIONS AT 25°C			OP-09-N		OP-09-G		
These specifications apply for each amplifier unless otherwise noted.			V_S = ±15V unless otherwise specified		V_S = ±15V unless otherwise specified		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	–	0.5	–	2.5	mV
Input Offset Current	I_{OS}		–	20	–	50	nA
Input Bias Current	I_B		–	300	–	500	nA
Input Voltage Range	CMVR		±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR, $R_S \leq 10k\Omega$	100	–	100	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	90	–	90	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	12	–	12	–	V
		$R_L \geq 2k\Omega$	11	–	11	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	100	–	100	–	V/mV
Power Consumption (Four Amplifiers)	P_D	V_{OUT} = 0, No Load	–	180	–	180	mW

TYPICAL CHARACTERISTICS			OP-09-N	OP-09-G	
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Units**
Slew Rate	SR	A_V = 1, $R_L \geq 2k\Omega$	1.0	1.0	V/μsec
Unity Gain Bandwidth	GBW		2.0	2.0	MHz
Channel Separation	CS	A_V = 100, f = 10kHz R_S = 1kΩ	120	120	dB

NOTE: Either or both V+ pads may be used without any change in performance.

OP-11
QUAD OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS		CHIP LAYOUT AND DIMENSIONS
Junction Temperature (T_j)	−65°C to +150°C	
Supply Voltage		
OP-11N, OP-11G	±22V	
Differential Input Voltage	±30V	
Input Voltage	±15V	
(For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.)		
Output Short Circuit Duration to Ground	Continuous	
(One amplifier only, I_{SC} = 45mA typical.)		

ELECTRICAL SPECIFICATIONS AT 25°C			OP-11-N		OP-11-G		
These specifications apply for each amplifier unless otherwise noted.			V_S = ±15V unless otherwise specified		V_S = ±15V unless otherwise specified		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10K\Omega$	–	0.5	–	2.5	mV
Input Offset Current	I_{OS}		–	20	–	50	nA
Input Bias Current	I_B		–	300	–	500	nA
Input Voltage Range	CMVR		±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR, $R_S \leq 10k\Omega$	100	–	100	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	90	–	90	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±12	–	±12	–	V
		$R_L \geq 2k\Omega$	±11	–	±11	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	100	–	100	–	V/mV
Power Consumption (Four Amplifiers)	P_D	V_{OUT} = 0, No Load	–	180	–	180	mW

TYPICAL CHARACTERISTICS			OP-11-N	OP-11-G	
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Units**
Slew Rate	SR	A_V = 1, $R_L \geq 2k\Omega$	1.0	1.0	V/μsec
Unity Gain Bandwidth	GBW		2.0	2.0	MHz
Channel Separation	CS	A_V = 100, f = 10kHz R_S = 1kΩ	120	120	dB

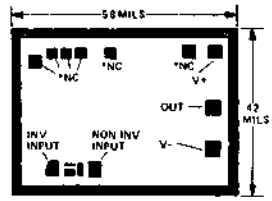
NOTE: Either or both V+ pads may be used without any change in performance.

OP-12
PRECISION LOW INPUT CURRENT OPERATIONAL AMPLIFIER

INTERNALLY COMPENSATED

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Supply Voltage	
OP-12-N and OP-12-G	±20V
OP-12-GR	±18V
Differential Input Current	±10mA
Input Voltage	±15V Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for V_S = ±15V, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-12-N Min	OP-12-N Max	OP-12-G Min	OP-12-G Max	OP-12-GR Min	OP-12-GR Max	Units
Input Offset Voltage	V_{OS}		–	0.3	–	0.3	–	1.0	mV
Input Offset Current	I_{OS}		–	0.2	–	0.4	–	0.5	nA
Input Bias Current	I_B		–	2.0	–	4.0	–	5.0	nA
Input Voltage Range	CMVR		±14	–	±14	–	±14	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	104	–	102	–	84	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V	104	–	102	–	84	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±13	–	±13	–	±13	–	V
		$R_L \geq 2k\Omega$	±10	–	±10	–	±10	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, V_O = ±10V	–	–	–	–	40	–	V/mV
		$R_L \geq 2k\Omega$	50		30		–		
Input Resistance	R_{in}		25	–	13	–	10	–	MΩ
Supply Current	I_S	I_{out} = 0, V_{out} = 0	–	0.6	–	0.6	–	0.8	mA

TYPICAL ELECTRICAL CHARACTERISTICS

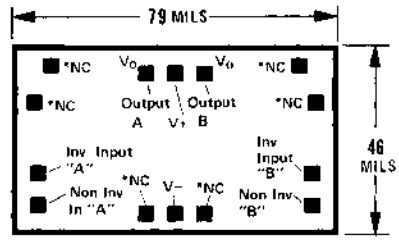
These specifications apply for V_S = ±15V,

Parameter	Symbol	Test Conditions	OP-12-N Typical	OP-12-G Typical	OP-12-GR Typical	Units
Average Input Offset Voltage Drift	TCV_{os}		1.0	1.0	1.5	µV/°C
Average Input Offset Current Drift	TCI_{os}		0.5	1.0	1.0	pA/°C

OP-14 (IMPROVED 1458)
DUAL OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
OP14-N and OP14-G	±22V
OP14-GR	±18V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



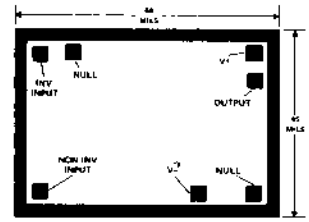
ELECTRICAL SPECIFICATIONS AT 25°C			OP14-N		OP14-G		OP14-GR		
These specifications apply for each amplifier unless otherwise noted.			V_S = +15V unless otherwise specified		+5V ≤ V_S ≤ ±20V unless otherwise specified		V_S = +15V unless otherwise specified		
Parameter	Symbol	Test Conditions	Min	Max	Min	Max	Min	Max	Units
Input Offset Voltage	V_{OS}	R_S ≤ 50kΩ	–	0.75	–	2.0	–	6.0	mV
Input Offset Voltage Match	ΔV_{OS}	R_S ≤ 100Ω	–	1.0	–	–	–	–	mV
Input Offset Current	I_{OS}		–	2.0	–	5.0	–	200	nA
Input Bias Current	I_B		–	50	–	50	–	500	nA
Input Voltage Range	CMVR	V_S = ±15V	±12.0	–	±12.0	–	±12.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR R_S ≤ 50kΩ	90	–	80	–	70	–	dB
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±CMVR R_S ≤ 100Ω	94	–	–	–	–	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V R_S ≤ 50kΩ	90	–	80	–	76	–	dB
Maximum Output Voltage Swing (V_S = ±15V)	V_{OM}	R_L ≥ 10kΩ R_L ≥ 2kΩ	±12.0 ±12.0	– –	+12.0 ±10.0	– –	±12.0 ±10.0	– –	V V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V V_S = ±15V	100	–	100	–	25	–	V/mV
Power Consumption (Both Amplifiers)	P_D	V_{OUT} = 0 V_S = ±15V	–	120	–	170	–	170	mW
Slew Rate	SR	R_L = 2kΩ, C_L = 100pF	0.4	–	0.4	–	–	–	V/μs
Channel Separation	CS		100	–	100	–	–	–	dB

TYPICAL ELECTRICAL CHARACTERISTICS			OP14-N	OP14-G	OP14-GR	
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.						
Parameter	Symbol	Test Conditions	Typical	Typical	Typical	Units
Risetime		A_V = +1 V_{IN} = 20mV R_L = 2kΩ, C_L = 50pF	200	200	200	nsec
Overshoot		A_V = +1 V_{IN} = 20 mV R_L = 2kΩ, C_L = 50pF	5.0	5.0	5.0	%

OP-15
PRECISION, LOW POWER JFET INPUT OP AMP

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Supply Voltage	
OP-15-N, OP-15-G	±22V
OP-15-GR	±18V
Differential Input Voltage	
OP-15-N, OP-15-G	±40V
OP-15-GR	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



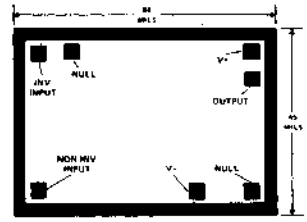
ELECTRICAL SPECIFICATIONS AT 25°C			OP-15-N		OP-15-G		OP-15-GR		
These specifications apply for T_j = +25°C, ±15V, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.5	–	1.0	–	3.0	mV
Large Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 2KΩ	100	–	75	–	50	–	V/mV
Input Voltage Range	CMVR	V_S = ±15V	±10.5	–	±10.5	–	±10.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	–	86	–	82	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	–	86	–	–	–	dB
		V_S = ±10V to +15V	–	–	–	–	82	–	dB
Maximum Output Voltage Swing	V_{OM}	R_L = 10KΩ	12	–	12	–	12	–	V
		R_L = 2KΩ	11	–	11	–	11	–	V
Supply Current	I_{SY}		–	4.0	–	4.0	–	50	mA

TYPICAL ELECTRICAL CHARACTERISTICS			OP-15-N	OP-15-G	OP-15-GR	
These specifications apply for V_S = ±15V, T_j = 25°C						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift without ext trim	TCV_{OS}	R_p = 100KΩ	2.0	3.0	4.0	µV/°C
With ext trim	TCV_{OSN}		2.0	3.0	4.0	
Input Offset Current	I_{OS}		3.0	3.0	3.0	pA
Input Bias Current	I_B		15	15	15	pA
Slew Rate	SR	A_{VCL} = +1	17	16	15	V/µsec
Settling Time	t_s	to 0.01%	2.2	2.3	2.4	µs
		to 0.05%	1.1	1.1	1.2	
		to 0.10%	0.9	0.9	1.0	
Gain Bandwidth Product	GBW		6.0	5.7	5.4	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1	14	13	12	MHz
Input Noise Voltage Density	e_n	f = 100Hz	20	20	20	$nV/\sqrt{Hz}$
		f = 1000Hz	15	15	15	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f = 100	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1000	0.01	0.01	0.01	$pA/\sqrt{Hz}$
Input Capacitance	C_{in}		3	3	3	pF

OP-16
WIDE BANDWIDTH PRECISION JFET INPUT OP AMP

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Supply Voltage	
OP-16N, OP-16G	±22V
OP-16GR	±18V
Differential Input Voltage	
OP-16N, OP-16G	±40V
OP-16GR	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



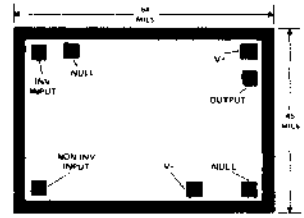
ELECTRICAL SPECIFICATIONS AT 25°C			OP-16N		OP-16G		OP-16GR		
These specifications apply for T_j = +25°C, V_s = ±15V, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_s = 50Ω	–	0.5	–	1.0	–	3.0	mV
Large Signal Voltage Gain	A_{VO}	V_o = ±10V, R_L = 2KΩ	100	–	75	–	50	–	V/mV
Input Voltage Range	CMVR		±10.5	–	±10.5	–	±10.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	–	86	–	82	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±10V to ±20V	86	–	86	–	–	–	dB
		V_s = ±10V to ±15V	–	–	–	–	82	–	dB
Maximum Output Voltage Swing	V_{OM}	R_L = 10KΩ	12	–	12	–	12	–	V
		R_L = 2KΩ	11	–	11	–	11	–	V
Supply Current	I_{SY}		–	7.0	–	7.0	–	8.0	mA

TYPICAL ELECTRICAL CHARACTERISTICS			OP-16N	OP-16G	OP-16GR	
These specifications apply for V_S = ±15V, T_j = 25°C						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift						
Without Ext Trim	TCV_{OS}		2.0	3.0	4.0	µV/°C
With Ext Trim	TCV_{OSN}	R_p = 100KΩ	2.0	3.0	4.0	µV/°C
Input Offset Current	I_{OS}		3.0	3.0	3.0	pA
Input Bias Current	I_B		15	15	15	pA
Slew Rate	SR	A_{VCL} = +1	25	24	23	V/µsec
Settling Time	t_s	to 0.01%	1.7	1.7	1.8	µs
		to 0.05%	0.9	0.9	1.0	
		to 0.10%	0.7	0.7	0.8	
Gain Bandwidth Product	GBW		8.0	7.6	7.2	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1	19	18	17	MHz
Input Noise Voltage Density	e_n	f = 100Hz	20	20	20	nV/√Hz
		f = 1000Hz	15	15	15	nV/√Hz
Input Noise Current Density	i_n	f = 100	0.01	0.01	0.01	pA/√Hz
		f = 1000	0.01	0.01	0.01	pA/√Hz
Input Capacitance	C_{in}		3	3	3	pF

OP-17
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65° C to +150° C
Supply Voltage	
OP-17-N, OP-17-G	±22V
OP-17-GR	±18V
Differential Input Voltage	
OP-17-N, OP-17-G	±40V
OP-17-GR	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25° C

These specifications apply for T_j = +25° C, V_S = ±15V, unless otherwise noted

			OP-17-N		OP-17-G		OP-17-GR		
Parameter	Symbol	Test Conditions	Min	Max	Min	Max	Min	Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.5	–	1.0	–	3.0	mV
Large Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 2KΩ	100	–	75	–	50	–	V/mV
Input Voltage Range	CMVR	V_S = ±15V	±10.5	–	±10.5	–	±10.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	–	86	–	82	–	dB
Power Supply Rejection Ratio	PSRR	V_S = +10V to +20V	86	–	86	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	82	–	dB
Maximum Output Voltage Swing	V_{OM}	R_L = 10KΩ	12	–	12	–	12	–	V
		R_L = 2KΩ	11	–	11	–	11	–	V
Supply Current	I_{SY}		–	7.0	–	7.0	–	8.0	mA

TYPICAL ELECTRICAL CHARACTERISTICS

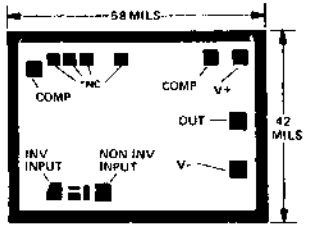
These specifications apply for V_S = ±15V, T_j = 25° C

			OP-17-N	OP-17-G	OP-17-GR	
Parameter	Symbol	Test Conditions	Typical	Typical	Typical	Units
Average Input Offset Voltage Drift without ext trim	TCV_{OS}	R_p = 100KΩ	2.0	3.0	4.0	μV/°C
Drift with ext trim	TCV_{OSN}		2.0	3.0	4.0	
Input Offset Current	I_{OS}		3.0	3.0	3.0	pA
Input Bias Current	I_B		15	15	15	pA
Slew Rate	SR	A_{VCL} = 5	70	66	62	V/μsec
Settling Time	t_s	to 0.01%	1.5	1.5	1.6	μs
		to 0.05%	0.5	0.5	0.6	
		to 0.10%	0.4	0.4	0.5	
Gain Bandwidth Product	GBW		30	28	26	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +5	11	10	9	MHz
Input Noise Voltage Density	e_n	f = 100Hz	20	20	20	$nV/\sqrt{Hz}$
		f = 1000Hz	15	15	15	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f = 100	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1000	0.01	0.01	0.01	$pA/\sqrt{Hz}$
Input Capacitance	C_{in}		3	3	3	pF

108
LOW INPUT CURRENT OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
108-N and 108-G	±20V
108-GR	±18V
Differential Input Current (See PM108A data sheet)	±10mA
Input Voltage (See PM108A data sheet)	±15V, Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for ±5V ≤ V_S ≤ ±20V for 108-N, ±5V ≤ V_S ≤ ±15V for 108-G and108-GR, unless otherwise noted.

Parameter	Symbol	Test Conditions	108-N Min	108-N Max	108-G Min	108-G Max	108-GR Min	108-GR Max	Units
Input Offset Voltage	V_{OS}		–	0.5	–	2.0	–	7.5	mV
Input Offset Current	I_{OS}		–	0.2	–	1.0	–	1.0	nA
Input Bias Current	I_B		–	2.0	–	7.0	–	7.0	nA
Input Voltage Range	CMVR	V_S = ±15V	±14	–	±14	–	±14	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR, V_S = ±15V	96	–	85	–	80	–	dB
Power Supply Rejection Ratio	PSRR	V_S = +5 to +20V	96	–	–	–	–	–	dB
		V_S = ±5 to ±15V	–	–	80	–	80	–	dB
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10kΩ, V_S = ±15V	±13	–	±13	–	±13	–	V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 10kΩ, V_O = ±10V, V_S = ±15V	80	–	50	–	25	–	V/mV
Input Resistance	R_{in}		25	–	8.5	–	8.5	–	MΩ
Supply Current	I_S	I_{out} = 0, V_{out} = 0	–	0.6	–	0.8	–	0.8	mA

TYPICAL ELECTRICAL CHARACTERISTICS

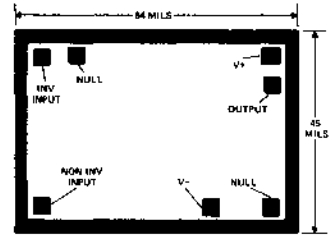
These specifications apply for V_S = ±15V.

Parameter	Symbol	Test Conditions	108-N Typical	108-G Typical	108-GR Typical	Units
Average Input Offset Voltage Drift	TCV_{os}		1.0	3.0	6.0	µV/°C
Average Input Offset Current Drift	TCI_{os}		1.0	2.0	2.0	pA/°C

155
LOW POWER JFET INPUT OP AMP

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
155-N and 155-G	±22V
155-GR	±18V
Differential Input Voltage	
155-N and 155-G	±40V
155-GR	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



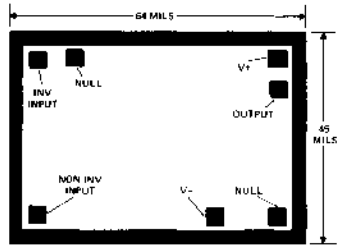
ELECTRICAL SPECIFICATIONS AT 25°C			155-N		155-G		155-GR		
These specifications apply for T_j = +25°C, ±15V ≤ V_S ≤ ±20V for 155-N and 155-G, ±15V for 155-GR, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	2.0	–	5.0	–	10	mV
Large Signal Voltage Gain	A_{VO}	V_O = ±10V, V_S = ±15V R_L = 2KΩ	50	–	50	–	25	–	V/mV
Input Voltage Range	CMVR	V_S = ±15V	±11	–	±11	–	±11	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	–	85	–	80	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	–	85	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	80	–	dB
Maximum Output Voltage Swing	V_{OM}	V_S = ±15V, R_L = 10KΩ	12	–	12	–	12	–	V
		V_S = ±15V, R_L = 2KΩ	10	–	10	–	10	–	V
Supply Current	I_S	V_S = ±15V, V_O = 0	–	4.0	–	4.0	–	4.0	mA

TYPICAL ELECTRICAL CHARACTERISTICS			155-N	155-G	155-GR	
These specifications apply for V_S = ±15V.						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{OS}	R_S ≤ 50Ω	4.0	5.0	6.0	µV/°C
Input Offset Current	I_{OS}		3.0	4.0	5.0	pA
Input Bias Current	I_B		30	30	40	pA
Slew Rate	SR	A_{VCL} = +1	5.0	5.0	5.0	V/µsec
Settling Time to 0.01%	t_s		4.0	4.0	4.0	µsec
Gain Bandwidth Product	GBW		2.5	2.5	2.5	MHz

156
WIDE BANDWIDTH JFET INPUT OP AMP

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
156-N and 156-G	±22V
156-GR	±18V
Differential Input Voltage	
156-N and 156-G	±40V
156-GR	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



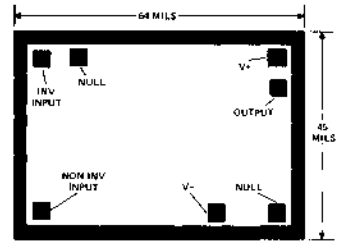
ELECTRICAL SPECIFICATIONS AT 25°C			156-N		156-G		156-GR		
These specifications apply for T_j = +25°C, ±15V ≤ V_S ≤ ±20V for 156-N and 156-G, V_S = ±15V for 156-GR, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	2.0	–	5.0	–	10	mV
Large Signal Voltage Gain	A_{VO}	V_O = ±10V, V_S = ±15V, R_L = 2KΩ	50	–	50	–	25	–	V/mV
Input Voltage Range	CMVR	V_S = ±15V	±11	–	±11	–	±11	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	–	85	–	80	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	–	85	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	80	–	dB
Maximum Output Voltage Swing	V_{OM}	V_S = ±15V, R_L = 10KΩ	12	–	12	–	12	–	V
		V_S = +15V, R_L = 2KΩ	10	–	10	–	10	–	V
Supply Current	I_S	V_S = ±15V, V_O = 0	–	7.0	–	7.0	–	10	mA

TYPICAL ELECTRICAL CHARACTERISTICS		156-N	156-G	156-GR	
These specifications apply for V_S = ±15V.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{OS}	R_S ≤ 50Ω	4.0	5.0	6.0	µV/°C
Input Offset Current	I_{OS}		3.0	4.0	5.0	pA
Input Bias Current	I_B		30	30	40	pA
Slew Rate	SR	A_{VCL} = +1	12	12	12	V/µsec
Settling Time to 0.01%	t_s		1.5	1.5	1.5	µsec
Gain Bandwidth Product	GBW		5.0	5.0	5.0	MHz

157
JFET INPUT OPERATIONAL AMPLIFIER
WIDE BANDWIDTH DECOMPENSATED (A_V = 5)

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
157-N and 157-G	±22V
157-GR	±18V
Differential Input Voltage	
157-N and 157-G	±40V
157-GR	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous

CHIP LAYOUT AND DIMENSIONS



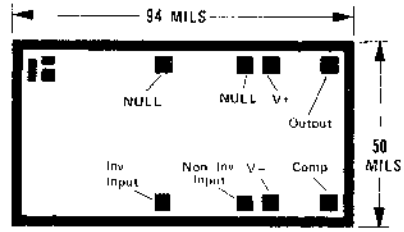
ELECTRICAL SPECIFICATIONS AT 25°C			157-N		157-G		157-GR		
These specifications apply for T_j = +25°C, +15V ≤ V_S ≤ +20V for 157-N and 157-G, V_S = ±15V for 157-GR, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	2.0	–	5.0	–	10	mV
Large Signal Voltage Gain	A_{VO}	V_O = ±10V, V_S = ±15V, R_L = 2KΩ	50	–	50	–	25	–	V/mV
Input Voltage Range	CMVR	V_S = ±15V	±11	–	±11	–	±11	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	–	85	–	80	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	–	85	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	80	–	dB
Maximum Output Voltage Swing	V_{OM}	V_S = ±15V, R_L = 10KΩ	12	–	12	–	12	–	V
		V_S = +15V, R_L = 2KΩ	10	–	10	–	10	–	V
Supply Current	I_S	V_S = ±15V, V_O = 0	–	7.0	–	7.0	–	10	mA

TYPICAL ELECTRICAL CHARACTERISTICS		157-N	157-G	157-GR	
These specifications apply for V_S = ±15V.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Average Input Offset Voltage Drift	TCV_{OS}	R_S ≤ 50Ω	4.0	5.0	6.0	µV/°C
Input Offset Current	I_{OS}		3.0	4.0	5.0	pA
Input Bias Current	I_B		30	30	40	pA
Slew Rate	SR	A_{VCL} = 5	50	50	50	V/µsec
Settling Time to 0.01%	t_s	A_{VCL} = 5	1.5	1.5	1.5	µsec
Gain Bandwidth Product	GBW		20	20	20	MHz

725
INSTRUMENTATION OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for V_S = ±15V unless otherwise noted.

Parameter	Symbol	Test Conditions	725-N Min	725-N Max	725-G Min	725-G Max	725-GR Min	725-GR Max	Units
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	–	0.5	–	1.3	–	2.5	mV
Input Offset Current	I_{OS}		–	5.0	–	13	–	35	nA
Input Bias Current	I_B		–	80	–	110	–	125	nA
Input Resistance Differential Mode	R_{IN}		0.7	–	0.5	–	–	–	MΩ
Input Voltage Range	CMVR		±13.5	–	±13.5	–	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 20k\Omega$	120	–	100	–	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V $R_S \leq 20k\Omega$	–	5.0	–	10	–	35	μV/V
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	+12.5 +12.0 ±11.0	– – –	±12.0 ±11.5 –	– – –	±12.0 ±10.0 –	– – –	V V V
Lareg Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ V_O = ±10V	1000	–	500	–	250	–	V/mV
Differential Input Voltage			–	±30	–	±30	–	±30	V
Power Consumption (V_{OUT} = 0V)	P_D	V_S = ±15V	–	105	–	150	–	150	mW

TYPICAL ELECTRICAL CHARACTERISTICS

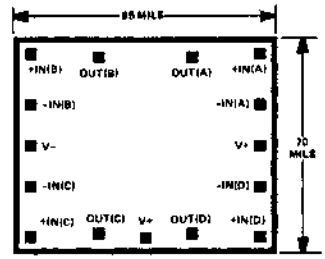
These specifications apply for V_S = ±15V.

Parameter	Symbol	Test Conditions	725-N Typical	725-G Typical	725-GR Typical	Units
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.7	1.4	2.0	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSN}	$R_S \leq 50\Omega$ R_P = 20kΩ	0.3	0.5	0.6	μV/°C
Average Input Offset Current Drift	TCI_{OS}		10	14	14	pA/°C

4136
QUAD OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	-65°C to +150°C
Supply Voltage	
4136-N and 4136-G	±22V
4136-GR	±18V
Differential Input Voltage	±30V
Input Voltage	±15V
(For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.)	
Output Short Circuit Duration to Ground	Continuous
(One amplifier only, I_{SC} = 45mA typical.)	

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			4136-G		4136-GR		
These specifications apply for each amplifier unless otherwise noted.			V_S = ±15V unless otherwise specified		V_S = ±15V unless otherwise specified		
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 10K\Omega$	–	5.0	–	6.0	mV
Input Offset Current	I_{OS}		–	200	–	200	nA
Input Bias Current	I_B		–	500	–	500	nA
Input Voltage Range	CMVR		±12	–	±12	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR, $R_S \leq 10k\Omega$	70	–	70	–	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	–	150	–	150	µV/V
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±12	–	±12	–	V
		$R_L \geq 2k\Omega$	+10	–	±10	–	V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	50,000	–	20,000	–	V/V
Power Consumption (Four Amplifiers)	P_D	V_{OUT} = 0, No Load	–	340	–	340	mW

TYPICAL CHARACTERISTICS			4136-G	4136-GR	
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.					
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Units**
Slew Rate	SR	A_V = 1, $R_L \geq 2k\Omega$	1.5	1.5	V/µsec
Unity Gain Bandwidth	GBW		3.0	3.0	MHz
Channel Separation	CS	A_V = 100, f = 10KHz R_S = 1kΩ	105	105	dB

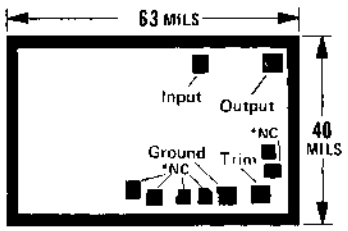
NOTE: Either or both V+ pads may be used without any change in performance.

REF-01
+10V PRECISION VOLTAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS

Junction Temperature (T_j)	-65°C to +150°C
Input Voltage	
REF01-N and REF01-G	40V
REF01-GR	30V
Output Short Circuit Duration (to ground or V_{IN})	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C

These specifications apply for V_{IN} = +15V unless otherwise noted.

Parameter	Symbol	Test Conditions	REF01-N Min	REF01-N Max	REF01-G Min	REF01-G Max	REF01-GR Min	REF01-GR Max	Units
Output Voltage	V_O	I_L = 0	9.90	10.10	9.85	10.15	9.80	10.20	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	–	-2.7	–	–	–	%
Input Voltage Range	V_{IN}		13	40	13	30	13	30	V
Line Regulation		V_{IN} = 13 to 33V	–	0.01	–	–	–	–	%/V
		V_{IN} = 13 to 30V	–	–	–	0.015	–	0.04	%/V

TYPICAL ELECTRICAL CHARACTERISTICS

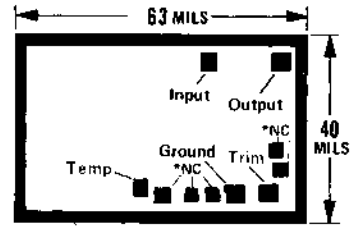
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	REF01-N Typical	REF01-G Typical	REF01-GR Typical	Units
Load Regulation		I_L = 0 to 10 mA	0.006	–	–	%/mA
		I_L = 0 to 8 mA	–	0.006	0.10	%/mA
Output Voltage Noise	e_{np-p}	0.1 Hz to 10 Hz	20	25	25	μVp-p
Turn-on Settling Time	t_{on}	To ±0.1% of final value	5.0	5.0	5.0	μsec
Quiescent Current	I_{SY}	No load	1.0	1.0	1.0	mA
Load Current	I_L		21	21	21	mA
Sink Current	I_S		0.5	0.5	0.5	mA
Short Circuit Current	I_{SC}	V_O = 0	30	30	30	mA
Output Voltage Temperature Coefficient	TCV_O		10	20	50	ppm/°C

REF-02
+5V PRECISION VOLTAGE REFERENCE/THERMOMETER

ABSOLUTE MAXIMUM RATINGS	
Junction Temperature (T_j)	−65°C to +150°C
Input Voltage	
REF02-N and REF02-G	40V
REF02-GR	30V
Output Short Circuit Duration (to ground or V_{IN})	Indefinite

CHIP LAYOUT AND DIMENSIONS



ELECTRICAL SPECIFICATIONS AT 25°C			REF02-N		REF02-G		REF02-GR		
These specifications apply for V_{IN} = +15V unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Output Voltage	V_O	I_L = 0	4.95	5.05	4.925	5.075	4.90	5.10	V
Output Adjust Range	ΔV_{trim}	R_P = 10kΩ	±3.0	—	±3.0	—	—	—	%
Input Voltage Range	V_{IN}		7	40	7	30	7	30	V
Line Regulation		V_{IN} = 8 to 33V	—	0.01	—	—	—	—	%/V
		V_{IN} = 8 to 30V	—	—	—	0.015	—	0.04	%/V

TYPICAL ELECTRICAL CHARACTERISTICS			REF02-N	REF02-G	REF02-GR	
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Typical**	**Typical**	**Units**
Temp Voltage Output	V_T	(Note)	630	630	630	mV
Temp Voltage Output Temperature Coefficient	TCV_T	(Note)	2.1	2.1	2.1	mV/°C
Output Voltage Temperature Coefficient	TCV_O		10	20	50	ppm/°C
Load Regulation		I_L = 0 to 10mA	0.006	—	—	%/mA
		I_L = 0 to 8mA	—	0.006	.010	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	25	25	µVp-p
Turn-on Settling Time	t_{on}	To +0.1% of final value	5.0	5.0	5.0	µsec
Quiescent Current	I_{SY}	No load	1.0	1.0	1.0	mA
Load Current	I_L		21	21	21	mA
Sink Current	I_S		0.5	0.5	0.5	mA
Short Circuit Current	I_{SC}	V_O = 0	30	30	30	mA

NOTE: On Temp Output, limit load current to ±50nA and load capacitance to 30pF. See AN-18 for detailed REF-02 thermometer applications information.

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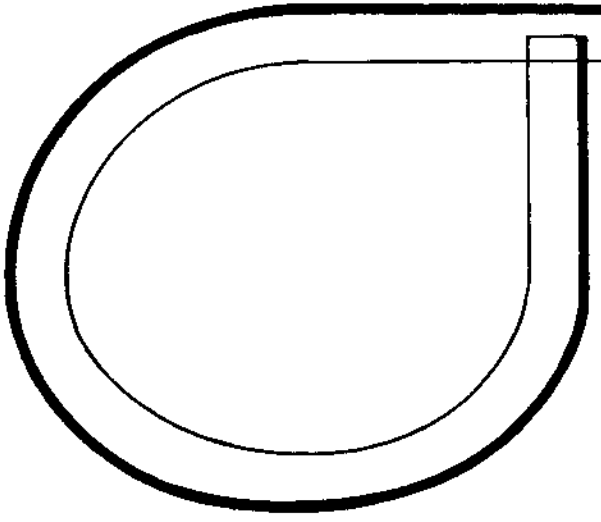

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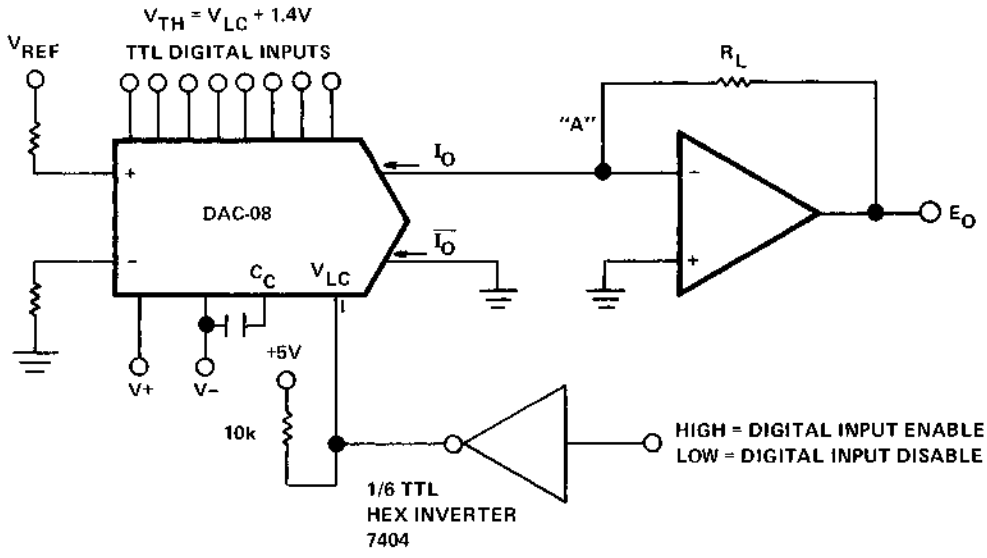
APPLICATION BRIEF NO. 1

AUTHOR Bob Blair and Donn Soderquist

TITLE: STROBING THE DAC-08 UNDER LOGIC CONTROL

CIRCUIT



FEATURE SUMMARY

- Digital inputs are treated as all zeros by increasing the logic threshold to +6.4V.
- Single Line Logic Control
- Handy in Multiplying Applications
- When more than one DAC is connected to point "A" – party line connection – strobing is simple.
- Higher speed and simpler than the alternative method of disabling which is accomplished by reducing V_{REF} to zero.

Note: Recovery when logic inputs are enabled may be slower when DAC is on +5V supply due to bias line saturation. This should be checked in the actual application.

DESCRIPTION

Since the PMI DAC-08 has a variable logic input threshold, strobing the output is easily accomplished using the circuit above. Normally, for TTL thresholds, pin 1 (V_{LC}) is grounded; but if it is connected instead to a hex inverter with a pullup resistor to +5V, all digital inputs effectively become zeros. All current flows in $\overline{I_O}$; no current flows in I_O no matter what the digital input code may be. When the hex inverter's output is low, normal TTL input logic threshold and operation is restored.

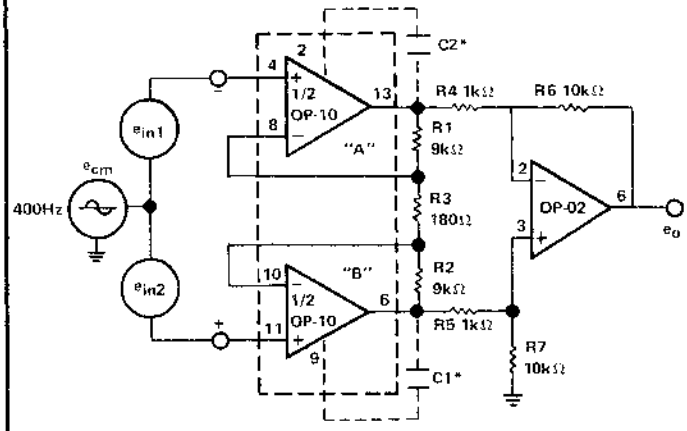
APPLICATION BRIEF NO. 2

AUTHORS Donn Soderquist and George Erdi

TITLE: OP-10 INSTRUMENTATION AMPLIFIER CMRR VERSUS FREQUENCY IMPROVEMENT

CIRCUIT

TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER



*Selected 5pF to 100pF

1) $e_o = (e_{in1} - e_{in2})\, A_{VCL}$

2) $A_{VCL} = \left(1 + \frac{R1+R2}{R3}\right)\left(\frac{R6}{R4}\right) = 1000$

3) $CMRR = 20 \log \frac{e_{cm}\,(A_{VCL})}{e_o}$ @ DC

4) If $\frac{R6}{R4} = \frac{R7}{R5}$, CMRR @ DC = 120 dB

5) At 400Hz CMRR is a function of the difference in frequency response of side "A" and side "B".

6) Use of C1 or C2, selected using the procedure below, matches the frequency response of side "A" and side "B" thereby maximizing CMRR at 400Hz.

FEATURE SUMMARY

- Addition of one selected capacitor improves CMRR at 400Hz to >95dB.
- OP-10 Side "A" and Side "B" bandwidths are matched
- Circuit uses existing nulling pins as frequency compensation connections.
- Added capacitor is in the range of 5pF to 100pF.

CAPACITOR SELECTION PROCEDURE

1. Connect e_{in1} to e_{in2} and to a 400Hz ±10V signal source.
2. While observing e_o with an oscilloscope, try different values of C1 or C2 until e_o is at a minimum.
3. Permanently install the selected capacitor.

DESCRIPTION

Common mode rejection ratio (CMRR) versus frequency of the familiar three op-amp instrumentation amplifier can be optimized by matching the frequency responses of the input differentially-connected pair of op amps. The circuit shown uses one selected capacitor (to reduce the frequency response of the faster op amp) which is connected between an output and one of the pins usually used for nulling ΔV_{OS}.

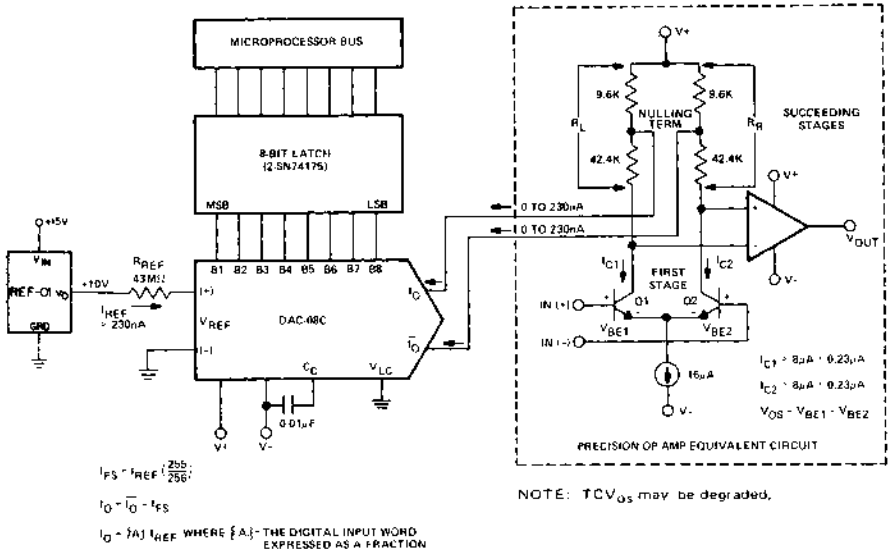
Eight devices were tested in this connection. Improvement to greater than 95dB @ 400Hz was achieved on all devices, an improvement of 1 to 20dB over performance without the selected capacitor.

APPLICATION BRIEF NO. 3

AUTHOR Charles Vinn

TITLE: DIGITAL NULLING OF OP-05 AND SSS725

CIRCUIT



$I_{FS} = I_{REF}\left(\frac{255}{256}\right)$

$I_O + \overline{I_O} = I_{FS}$

$I_O = [A]\, I_{REF}$ WHERE $[A]$ = THE DIGITAL INPUT WORD EXPRESSED AS A FRACTION

NOTE: TCV_{OS} may be degraded.

FEATURE SUMMARY

- Digitally-controlled offset nulling is achieved by imbalancing the first stage collector currents of a precision op amp.
- Greater than 1.5 mV of offset voltage may be nulled to zero with 5μV resolution at 25°C.
- This application is especially useful in microprocessor-controlled systems where stringent error budgets exist.
- Circuit uses the nulling terminals with a DAC-08 substituted for the conventional nulling potentiometer.

DESCRIPTION

The input offset voltage of a precision op amp (OP-05 or OP-07) may be nulled to <5μV using the complementary current outputs of a DAC-08 to change the ratio of collector currents in the first stage. With V_{OS} being defined as the voltage which must be applied between the input terminals to force V_{OUT} to zero and assuming all errors to be in the first stage, V_{OS} may be expressed as:

1) $V_{OS} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}$ where

k = Boltzmann's constant = 1.38×10^{-23} joules/°K
T = Absolute temperature, °K
q = Charge of an electron = 1.6×10^{-19} coulomb
I_S = Theoretical reverse-saturation current
I_C = Collector Current

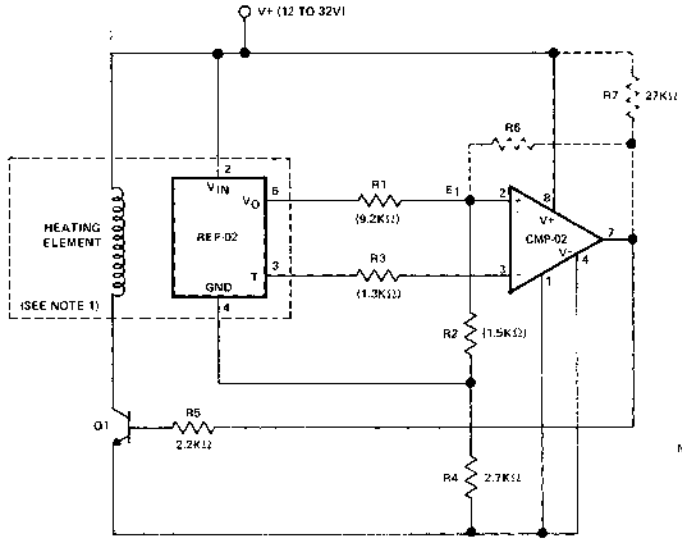
Changing the ratio I_{C1}/I_{C2} over a ± 3% range results in an input offset voltage nulling range of greater than 1.5mV at 25°C.

APPLICATION BRIEF NO. 4

AUTHOR Bob Blair

TITLE: REF-02 TEMPERATURE CONTROLLER

CIRCUIT



NOTES:
1. REF-02 SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
2. NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 60 C.
3. R3 = R1∥R2∥R6

FEATURE SUMMARY

- Variable Temperature Control
- Adjustable Hysteresis
- 12 To 32V Power Supply
- 2 IC Design
- Low Cost

DESCRIPTION

In the circuit above, temperature control is achieved using the REF-02 +5V Reference/Thermometer and a CMP-02 Precision Low Input Current Comparator. The CMP-02 turns on a heating element driver (Q1) whenever the present temperature drops below a setpoint temperature determined by the ratio of R1 to R2. The circuit also provides adjustable hysteresis and single supply operation.

HYSTERESIS DETERMINATION

R6 and R7 set hysteresis. With R7 = 27KΩ, R6 may be calculated:

$$R6 \cong \frac{[(V+) - 4V]}{(2.1mV/^{\circ}C)\ (\text{Hysteresis width in } ^{\circ}C)}$$

SETPOINT DETERMINATION

With R2 = 1.5KΩ, the value of R1 may be found for any desired temperature using the following procedure:

$$E_1 \cong (\text{Desired Temp} - 25^{\circ}C)\ (2.1mV/^{\circ}C) + 630\ mV$$

$$R1 \cong R2\left(\frac{5 - E_1}{E_1}\right)$$

AN-6

A LOW COST, HIGH-PERFORMANCE TRACKING A/D CONVERTER

INTRODUCTION

The availability of low-cost IC D/A converters, comparators and up/down counters makes possible construction of tracking A/D converters having high performance and reliability despite their small size and low cost. These A/D converters are suitable for a wide range of applications such as transducer and audio digitizing, infinite sample and holds, and servo-control loops. This paper describes an 8-bit tracking A/D converter that can be built using Precision Monolithics, Inc., DAC100CCQ3 D/A converter, CMP-01CJ Fast Precision Comparator and 4 bit MSI up/down counters.

TYPES OF A/D CONVERTERS

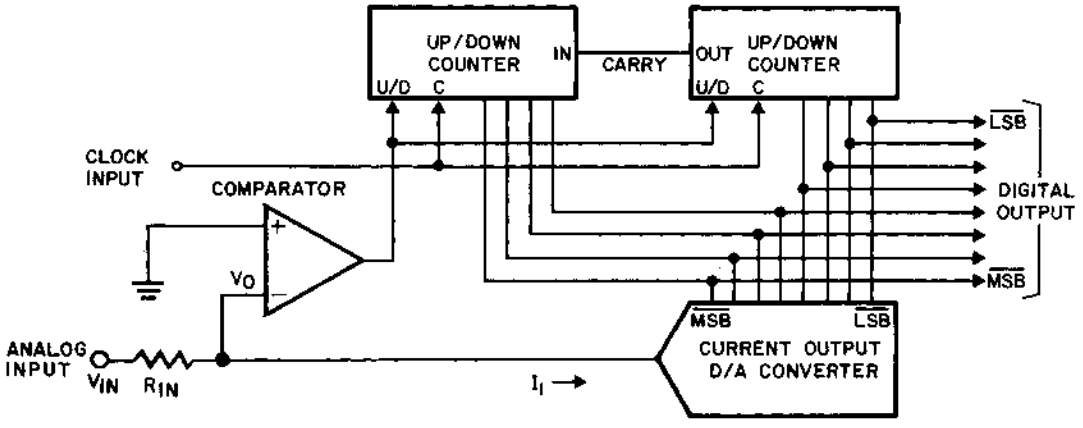
There are several popular styles of A/D converters (ADC) based on using a D/A converter in a feedback configuration. The three most common are: ramp or count-up, tracking or servo, and successive approximation.

Ramp types produce one conversion per each 2N clock counts for an "n" bit converter and are suitable only for very slowly changing analog data; additionally, the data can be taken out only at the end of the conversion period. Successive approximation types are quite fast, requiring only "n+1" clock counts for conversion. They are capable of encoding fast-moving analog signals if an external sample-and-hold circuit is used to stop the analog data; again, the digital output is true only at the end of the conversion period.

For many applications, tracking ADC's can provide adequate speed while costing approximately the same as simple ramp types. Additional advantages are that no sample-and-hold circuit is required and that the digital data is continuously available at the output.

BASIC OPERATION

The tracking A/D is a relatively simple system, both in concept and in practice. The basic design requires three major elements: an up/down counter, a current output D/A converter, and a voltage comparator (see Fig. 1). The voltage at the comparator's input will be the result of the analog input voltage minus the DAC output sink current times R_{in} ($V_o = V_{in} - I_1 \cdot R_{in}$). Assuming a perfect comparator, if the output voltage (V_o) is above ground, the comparator's output will be low, causing the up/down counter to increase the DAC's output sink current by one LSB. (The counter actually counts down one count; this results from the DAC's utilization of complementary logic, i.e., an all-zero input produces maximum DAC output current.) The comparator continues to examine the voltage for polarity, and always drives the counter's code in the direction which causes the output voltage to approach zero. Once a balance is achieved, the loop is "locked", and tracks the analog input signal so long as the loop slew rate is not exceeded. When the loop is balanced, the converter's output is the binary-coded equivalent of the analog input.

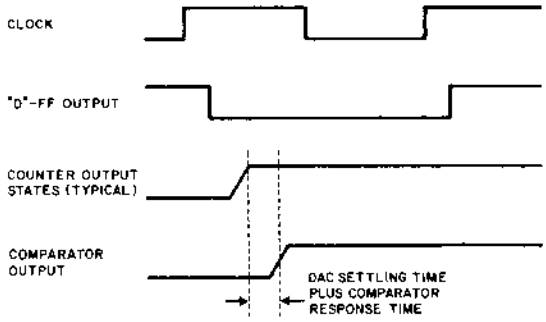


BASIC TRACKING A/D BLOCK DIAGRAM
FIGURE 1

When encoding a DC input signal, the digital output will "dither" or alternate between the two adjacent states which span the theoretically correct output value. This is of little consequence as all A/D converters have a similar error, known as the "quantizing" error.

In the actual circuit design, a "type-D" flip-flop is inserted between the comparator and the counter's up/down input. This is to insure adequate set-up time between the comparator's output change and the counter's next stage change.

Loop timing can be seen in Fig. 2. After the positive clock transition, the counter changes to its next state and drives the DAC to its new output. After the DAC has settled and the comparator has come to its final state, the next positive clock transition loads the comparator's new state into the flip-flop and the cycle repeats.



SYSTEM TIMING DIAGRAM
FIGURE 2

FINAL CIRCUIT DESIGN

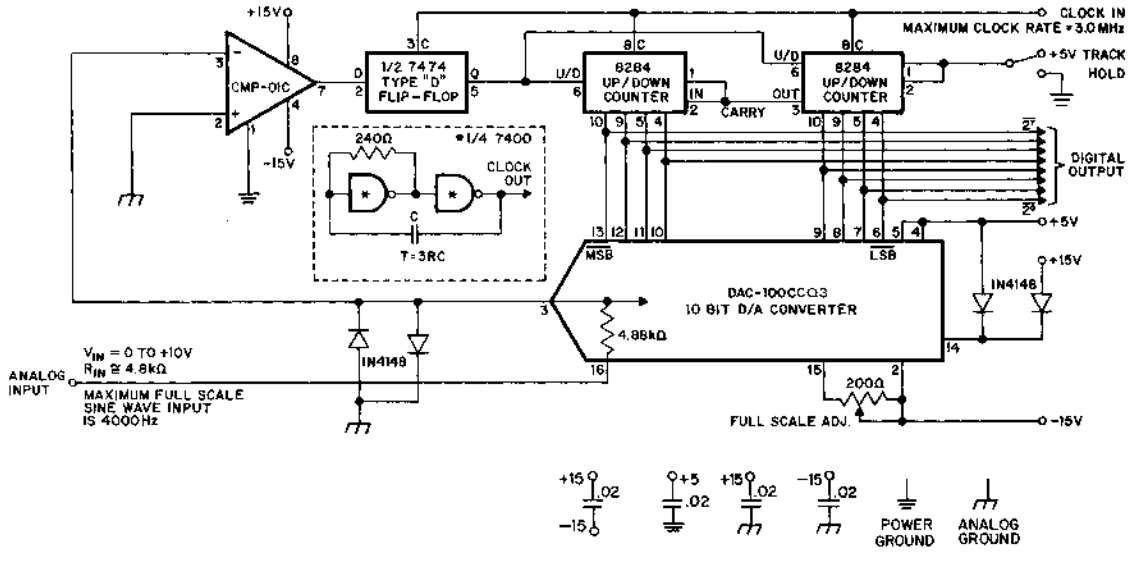
The completed 8 bit tracking A/D design is shown in Fig. 3. The digital output is available in complemented form, as the DAC-100 utilizes complementary logic. Diode clamps insure the DAC output remains near zero despite input and turn-on transients. For this 8 bit design, the two least significant digital inputs of the 10 bit DAC are not required and are connected to +5V, thus turning them off. Diodes are also used to insure that a positive voltage is applied to the V+ pin (pin 14) as soon as the +5V supply comes up. The clock, although extremely simple, is quite stable over a wide range of temperatures and supply voltages. Several layouts were tried, with no perceptible differences in performance. (See Fig. 4)

TRIMMING

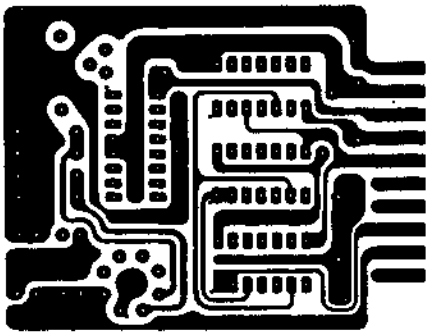
The circuit requires only one trimming operation. The full-scale output current of the DAC is adjusted to produce proper encoding at full scale input. Although several schemes are possible, the simplest is to place +10.0V at the input, and trim the 200Ω Full Scale Adjust pot to produce a low output at the 7 most significant bits with the LSB alternating states (dithering) at the clock frequency.

VOLTAGE OUTPUT APPLICATIONS

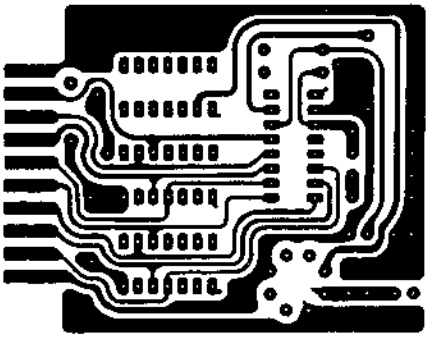
The basic tracking A/D uses a "current-comparison" technique; the analog voltage is not reconstructed at the comparator's input, thus eliminating the need for an op amp to convert the DAC-100's current output to a voltage. For applications such as infinite (no-droop) analog sample-and-hold circuits, the OP-01CJ, a low cost, fast slewing, fast settling op amp with internal compensation can be added as in Fig. 5. This configuration also provides very high input impedances, without requiring an extra buffer amplifier. The reconstructed analog voltage is available at the output of the op amp; gating the counter "off" stores the data in analog form.



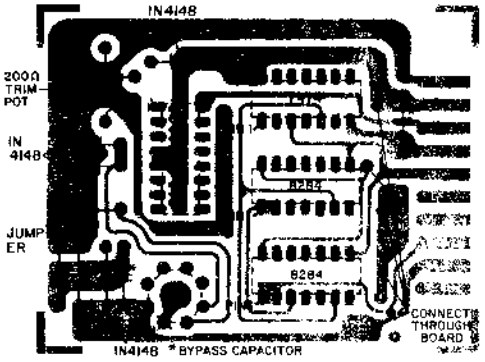
COMPLETE SCHEMATIC – 8 BIT TRACKING A/D CONVERTER
FIGURE 3



FRONT



BACK



FRONT

CONNECTOR

FRONT	BACK	
ANALOG GND	ANALOG GND	
+5V	DIGITAL OUTPUT	$\overline{2^7}$
ANALOG IN		$\overline{2^6}$
DIGITAL GND		$\overline{2^5}$
CLOCK		$\overline{2^4}$
N.C.		$\overline{2^3}$
N.C.		$\overline{2^2}$
TRACK & HOLD		$\overline{2^1}$
+15V		$\overline{2^0}$
N.C.	−15V	

ACTUAL SIZE PRINTED CIRCUIT LAYOUT – CIRCUIT OF FIG. 3
FIGURE 4

8 BIT TRACKING A/D PARTS LIST

Quantity	Description
1	DAC-100CCQ3 D/A Converter
1	CMP-01CJ Comparator
2	8284 Up/Down Counters
1	7474 Dual D-Type Flip-Flop
1	7400 Quad Gate
1	200Ω Trimpot, Bourns 3359P
4	IN4148 Diodes
5	Ceramic Capacitors
1	Carbon Composition Resistor
1	PC Board

TRACKING A/D CONVERTER WAVEFORMS

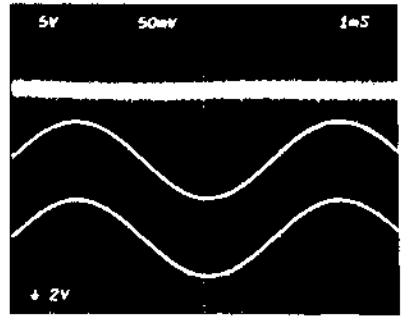
These scope photos were taken to indicate the waveforms observed at the comparator input during normal and abnormal operation of the converter. The output analog voltage trace was generated by applying the encoded digital output to a second D/A converter.

NORMAL OPERATION

Comparator Input

Analog Input

Reconstructed Analog Input

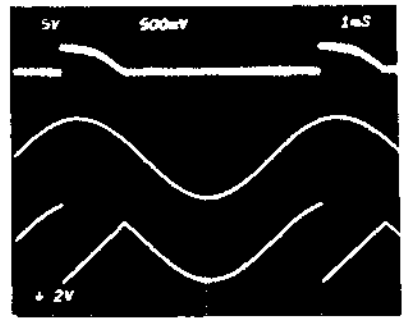


INPUT OVER-RANGE

Comparator Input

Analog Input

Reconstructed Analog Input

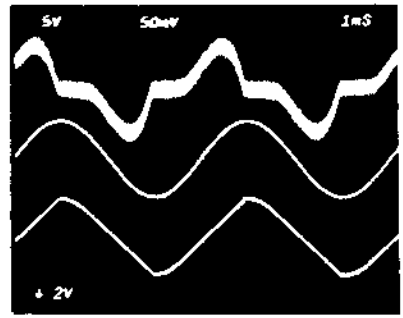


SLEW RATE LIMITING

Comparator Input

Analog Input

Reconstructed Analog Input



BIPOLAR OPERATION

Bipolar operation (±5V) can be obtained by injecting a current equal to 1/2 the full scale current into the DAC-100 sum line. This can be accomplished by applying +6.4V to the internal bipolar resistor of the DAC-100 (pin 1)—a 500Ω trimpot in series will allow precise adjustment of bipolar symmetry. To trim, apply –5.0V at the input and adjust the 500Ω symmetry-trimpot to produce a high output at all bits, with the normal "dither" in the LSB only. Next, ground the input and adjust the Full Scale trimpot to produce an output which alternates between 10000000 and 01111111.

0 TO +5V OPERATION

Operation with 5 volt full scale inputs (0V to +5V or ±2.5V) can be obtained by specifying the DAC-100 CCQ4.

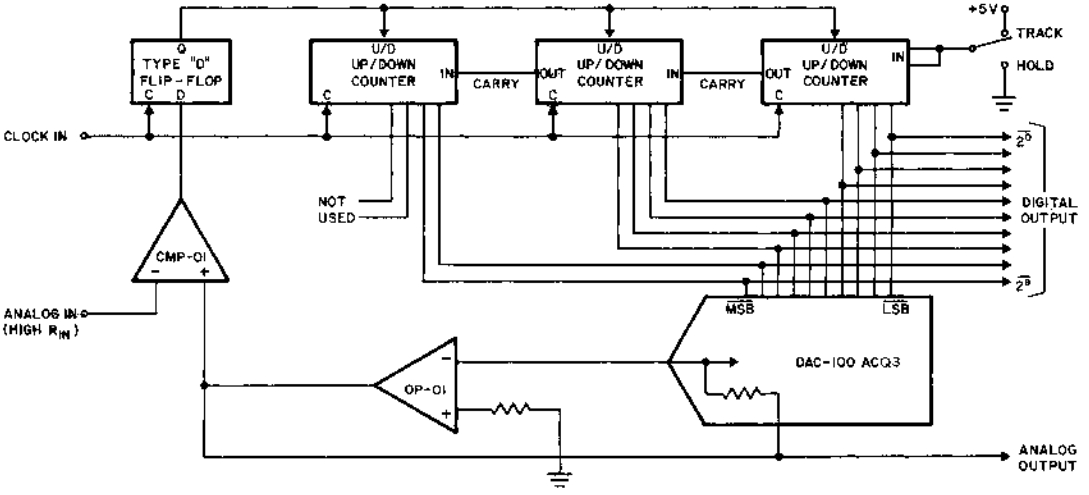
0.05% APPLICATIONS

Applications requiring 10 bits of resolution with 0.05% linearity can be implemented by adding a third up/down counter and utilizing all 10 inputs of an DAC-100ACQ3 (or Q4). See Fig. 5.

PERFORMANCE

Performance of the completed converter is quite impressive despite the low cost and small size. Using clock rates of 3.0 MHz, 10Vp-p signals can be accurately tracked to frequencies of about 4.0 kHz; higher frequencies can be accommodated by reducing the peak-to-peak amplitude.

Fully monotonic operation is obtained from 0° to 70°C; this is achieved because the DAC-100CQ3 is guaranteed to have ±1/2 LSB linearity to 8 bits (0.2%) over this temperature range, and the DAC-100ACQ3 has ±1/2 LSB linearity to 10 bits (0.05%).



10 BIT VOLTAGE OUTPUT A/D CONVERTER BLOCK DIAGRAM

FIGURE 5

All D.C. static errors can be attributed to the analog components only; the comparator makes no contribution to linearity errors, but its Vos and Vos drift with temperature are a consideration in the zero scale and full scale performance, and especially so in bipolar applications. The worst case DAC-100 zero error over 0°C to 70°C is 0.6mV; adding to this the 3.5mV max Vos of the CMP-01C results in a worst case zero scale error of 4.1mV, which is acceptably small compared to the value of 1/2 LSB (19.5mV) for the 8 bit A/D.

Because the Vos drift of the CMP-01C is typically only 1.8μV/°C even without offset trimming, the full scale drift will be almost entirely a function of the DAC-100CC tempco—60ppm/°C maximum.

For 10 bit applications, the comparator Vos becomes significant; the CMP-01C can be nulled, or the 0.8V max Vos CMP-01E can be utilized without nulling. Nulling of the comparator is not required in bipolar applications; this is accomplished by the bipolar symmetry trimming.

Other performance characteristics of the completed converter are listed in Table 1.

MILITARY TEMPERATURE RANGE OPERATION

Operation over wider temperature ranges can be obtained by simply specifying appropriate temperature range components. The simplicity of the all IC design coupled with the compatibility with MIL-M-38510 processing assures high reliability in military applications.

CONCLUSION

Extremely compact, low power consumption, all IC tracking A/D converters are made possible by combining Precision Monolithics, Inc. DAC-100 series 10 bit D/A converter, CMP-01 series comparator, and commercially available MSI up/down counters. Layout, construction and adjustment are noncritical. The simplicity and low cost of the tracking A/D converter invites usage in many new applications, including single channel digitizing at remote transducer locations.

TABLE 1
PERFORMANCE DATA

	8 Bit	10 Bit
Nonlinearity (0°C to +70°C)	0.2% max	0.05% max
Full Scale Tempco (0°C to +70°C)	60 ppm max	60 ppm max
Zero Scale Error (0°C to +70°C)	.10 LSB max	.20 LSB max*
Zero Scale Error Comparator Trimmed (0°C to +70°C)	.02 LSB	.08 LSB
Full Scale Voltages	0V to +10V, ±5V	0V to +10V ±5V
	0V to +5V, ±2.5V	0V to +5V, ±2.5V
Power Supply Rejection (0°C to +70°C)	.02% per % max	.02% per % max
Power Consumption (V_S = ±15V, +5V)	1.4W max	1.77W max

*untrimmed CMP-01E

APPENDIX – USEFUL DATA & FORMULAE

	10V full scale	5V full scale
LSB – 8 bits	39.1mV	19.5mV
10 bits	9.85mV	4.92mV

Loop Slew Rate = Clock Frequency × V_{LSB} = $f_C \times V_{LSB}$

Max Clock Frequency = $1/(T_A + T_B + T_C + T_D + T_E)$

WHERE: T_A = Flip-Flop Propagation Delay

T_B = Minimum Counter Set-Up Time

T_C = Counter Propagation Delay

T_D = D/A converter Settling Time (to n-bits)

T_E = Comparator Response Time

$$\text{Min Clock Frequency} = \frac{\pi \cdot Vin_{p\text{-}p} \cdot f_{in}\ max}{V_{LSB}}$$

PMI®

Application Notes

AN-10

SIMPLE PRECISION MILLIVOLT REFERENCE USES NO ZENERS

by

Donn Soderquist

A low output impedance millivolt source is frequently required in test systems, for generating small currents with moderate resistance values, and for general laboratory use. An excellent millivolt source can be built using only two parts; an instrumentation op amp and a potentiometer. The op amp is connected as a unity-gain buffer (Fig. 1) and the output is adjusted to the required voltage using the offset nulling terminals. The amplifier must have suitable characteristics such as low long term drift, freedom from chopper and "popcorn" noise, good power supply rejection and low offset voltage drift with temperature. To achieve low output impedance the op amp must have high gain around zero output voltages, and should have negligible thermal-induced drift for stable performance under varying load conditions. Use of a high performance bipolar input op amp such as the Precision Monolithics OP-05CJ provides low drift without chopper noise. With a typical initial offset voltage of 0.3mV, outputs from about −3.5mV to +3.5mV can be achieved. Adjusting the offset of the OP-05CJ to a value other than zero will create a drift equal to 3.3μV/°C per millivolt of output setting. The circuit's low frequency noise will be less than 0.65μV pk-pk with an output impedance of less than one milliohm. Long term drift will be much less than 3.5μV per month and power supply rejection is about 10μV/Volt.

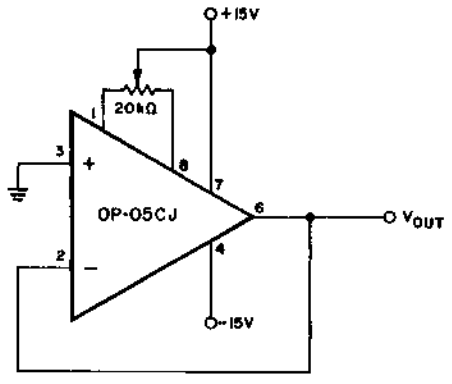


FIGURE 1
ZENERLESS PRECISION MILLIVOLT SOURCE

Application Notes

AN-11

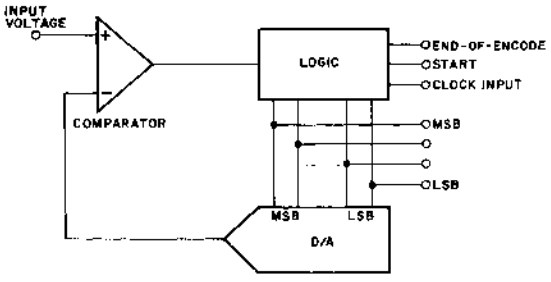
A LOW COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

by
Donn Soderquist

Successive Approximation Analog-to-Digital Converters have often been considered to be complex, expensive and troublesome circuits to produce. This application note describes a high-speed 8 bit successive approximation A/D easily constructed using only 3 readily available IC's. Precision Monolithics' DAC-100 Digital-to-Analog Converter, CMP-01 Fast Precision Voltage Comparator, a Successive Approximation Register plus a handful of discrete components complete the design. Despite the simplicity, the A/D is capable of 8 bit conversions in 6 μsec, and can easily be expanded to 10 bit resolution operation.

FEEDBACK A/D CONVERTERS

Most popular A/D Converters built today use a Digital-to-Analog Converter as part of a feedback or servo loop. Three of the most common types are the Ramp, Tracking, and Successive-Approximation; these differ primarily in the type of programming logic circuitry used to drive the D/A converter. All three types perform a comparison between the analog input and the output of a D/A converter; the logic changes the D/A output so that it approaches the analog input—when they are equal, the input to the DAC is the correct digitally encoded number (Fig. 1).



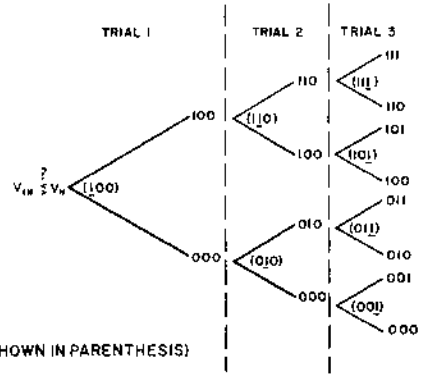
BASIC FEEDBACK A/D CONVERTER
FIGURE 1

The Ramp or Count-up type ADC uses up-counters for the programming logic. A start command clears the counters which then count up until the comparator output changes. The user must allow 2^n clock periods to insure a complete conversion; therefore only very slowly varying data may be converted.

Tracking A/D converters use up/down counters for the programming logic; the comparator output forces the counters to "track" the changes in the analog input. Once initial "lock" is acquired the correct digital output is continuously available, and the converter may be capable of encoding fairly fast-moving input siganls without requiring a sample and hold circuit. (Complete details on the construction of this type of converter are available in Precision Monolithics Application Note "A Low Cost, High Performance Tracking A/D Converter", AN-6).

Tracking ADC's are at their best when used to encode a single signal with a well-behaved maximum slew rate; multiplexed or video signals have large discontinuities which cause large errors while the tracking loop moves to acquire a new "lock" on the signal.

Successive Approximation A/D Converters are attractive for their rapid conversion rates and have found wide acceptance in video and multiplexed data systems. Recently-announced IC's provide the three basic converter building blocks in integrated form, reducing the cost and complexity of this approach to a figure at or below that of the ramp and tracking types. The great advantage of the SA ADC is that complete "n"-bit conversions can be accomplished typically in N + 1 clock periods—for a 10 bit converter this would be a speed improvement of about 100 times over the ramp type.

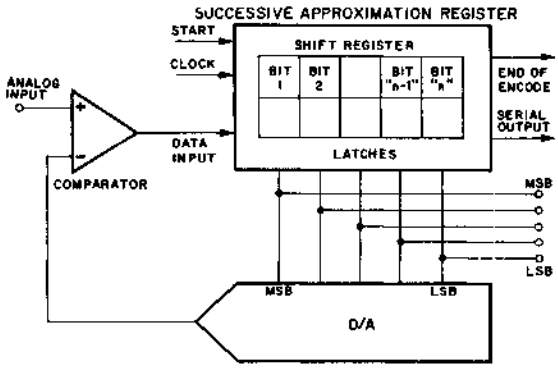


FLOW DIAGRAM FOR 3 BIT SUCCESSIVE APPROXIMATION A/D CONVERSION
FIGURE 2

BASIC SUCCESSIVE APPROXIMATION A/D CONVERSION

An SA ADC operates by comparing the analog input to a series of "trial" conversions; the first trial compares the input to the value of the most significant bit (MSB) or approximately half of full scale. Figure 2 shows the progression of trials for a 3-bit converter. If the input is greater than the MSB value, the MSB is retained and the converter moves on to "trying" the next most significant bit, or approximately three-quarters full scale. If the input had been less than the MSB, the logic would have turned the MSB off before going on to the next most significant bit, or one-quarter full scale. This "branching" continues until each successively smaller bit has been tried, with the entire process taking "n_{+1}" trials.

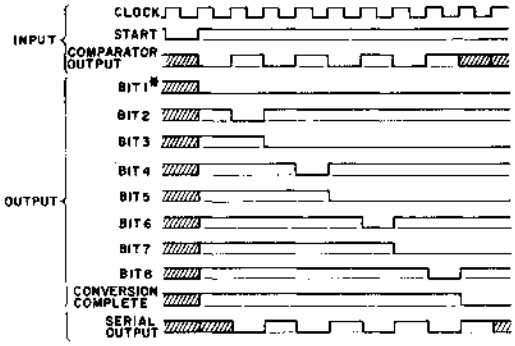
To implement the logic for the successive approximation algorithm, a configuration similar to Fig. 3 may be employed wherein a start command places a "one" in the first bit of a shift register. This sets the first latch to "one", and turns on the DAC's MSB. If the comparator output remains low, the "one" will remain in the latch; if not, the latch will be reset to zero before the next bit trial begins. The next clock cycle causes the shift register to place a "one" in the second bit and a similar process continues till all bits have been tried. After the last bit's trial, the end-of-encode output changes state indicating the parallel data is ready to be used. A useful feature of successive approximation conversion is that the correctly converted data is also available in serial form; this is handy for transmission of data on a single bus.



SUCCESSIVE APPROXIMATION A/D CONVERTER

FIGURE 3

The complete sequence of events is demonstrated in the timing diagram of Fig. 4. Note that "negative true" logic is shown; the DAC-100 employs a complementary binary code and the AM2502 produces a "low" output during each bit's trial, thus producing the standard successive approximation routine starting with the MSB trial and working towards the LSB trial. All events are initiated during positive-going clock transitions; the conversion process starts when the $\overline{S}$ input is held low, which also causes the $\overline{CC}$ (Conversion Completed) output to go high. After all bits have been tried, the last positive clock transition returns the $\overline{CC}$ to a low state, indicating the conversion has completed.



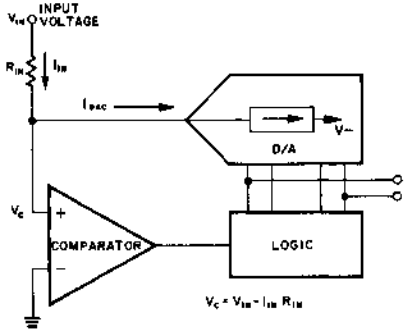
*NOTE: NEGATIVE TRUE LOGIC IS USED.
SHADED AREAS INDICATE LEVEL DEPENDS UPON PREVIOUS STATE
INPUT = +6.66 VOLTS, FULL SCALE = +10 VOLTS

TIMING DIAGRAM

FIGURE 4

"CURRENT" COMPARISON

The previous discussion has indicated that the function of the comparator was to perform a comparison between the analog input voltage and the output voltage of the D/A converter. Higher speed conversions may be achieved by using the output of a fast current output DAC directly. This may be implemented as shown in Fig. 5, where the comparator examines the polarity of ($V_{IN} - I_{IN}R_{IN}$). The "current comparison" method eliminates the need for a current-to-voltage converting op amp which is by far the slowest element in most D/A converters.

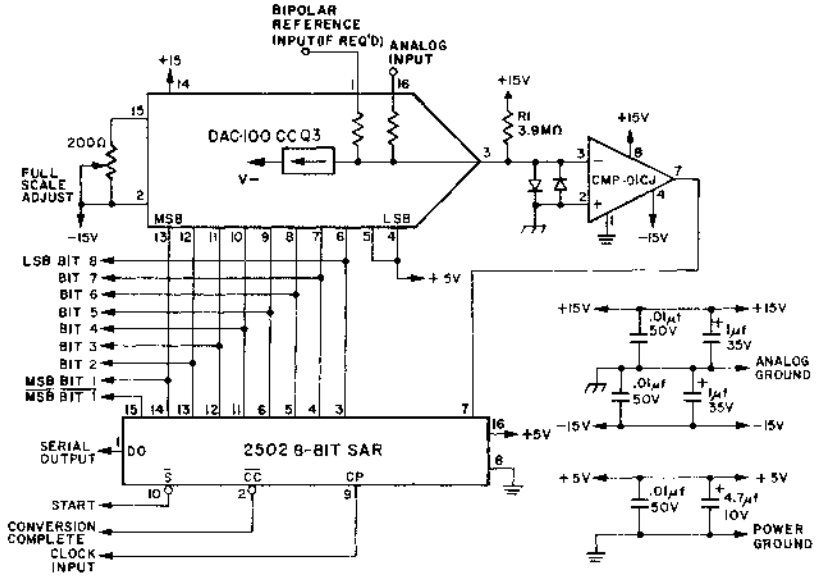


"CURRENT COMPARISON" A/D INPUT

FIGURE 5

COMPLETE CIRCUIT

The schematic for the complete 8-bit A/D converter is shown in Fig. 6. It is seen that the complete circuit adds very few components to the basic 3 IC's of the block diagram. A 200Ω potentiometer is used to adjust the full scale output and R1 is used to inject a +1/2 LSB value current into the sum node. This insures that adjacent code point transitions occur at 1/2 LSB points for minimum overall error. The clamp diodes minimize settling time and prevent large inputs from damaging the DAC output. For an 8-bit, 10 volt system the CMP-01CJ's maximum offset voltage is less than 1/10 LSB and should not require nulling.

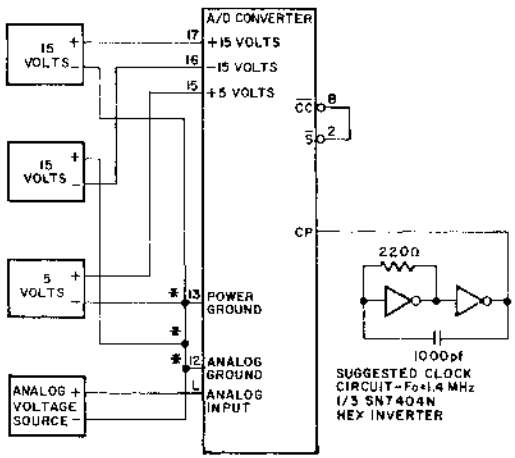


COMPLETE 8 BIT A/D SCHEMATIC

FIGURE 6

LAYOUT

A suggested layout for an 8-bit converter is shown in Fig. 8. This layout demonstrates some of the basic rules of good A/D converter practice: analog wiring is kept as short as possible and is separated from digital lines; the DAC output trace is especially short and directly connected to the comparator input and clamping diodes. Generous power supply bypassing has been employed using both disc and electrolytic capacitors. Other layouts can be easily designed because of the extreme simplicity of this circuit.



NOTE: PIN NUMBERS SHOWN REFER TO PC CARD TERMINALS
*COMMON GROUNDING POINT−REFER TO TEXT

GROUNDING AND SUPPLY HOOKUP

FIGURE 7

GROUNDING

For optimum noise rejection, digital (power) ground currents should not flow in signal input ground return lines. Analog and power grounds should be connected as close as possible to the A/D converter input connector. Fig. 7 illustrates a typical system installation showing the ground connections.

SERIAL OUTPUT

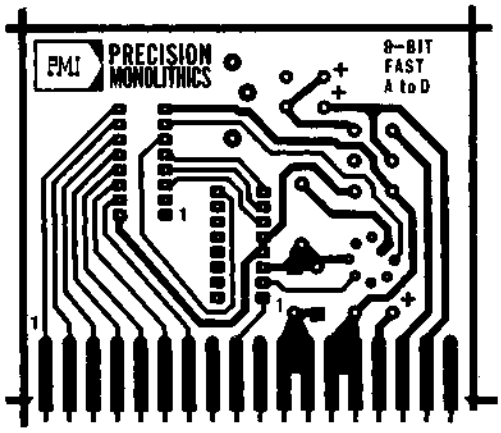
The digital output is available in serial NRZ (non-return-to-zero) format at the data output (DO) shortly after each positive-going clock transition. Serial output is especially convenient in applications where system wiring must be minimized, such as in one A/D per channel systems. Performing the A/D conversion process in close proximity to the signal source has the advantage of reducing errors associated with transmission of low level analog signals; instead, digitally encoded signals are transmitted with their inherent low error rates and ease of multiplexing.

BIPOLAR OPERATION

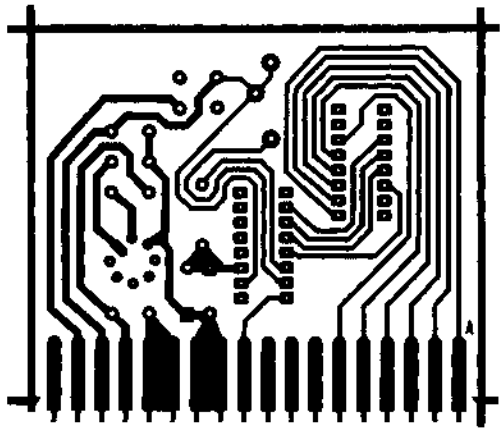
Bipolar operation can be obtained by injecting a current equal to 1/2 full scale into the sum node. This can be accomplished by applying +6.4 volts through a 500 ohm potentiometer to the internal bipolar resistor of the DAC-100. Both Bit 1 and $\overline{\text{Bit 1}}$ are available so 2's complement or offset binary coding may be obtained as desired.

0 TO +5V, ±2.5V OPERATION

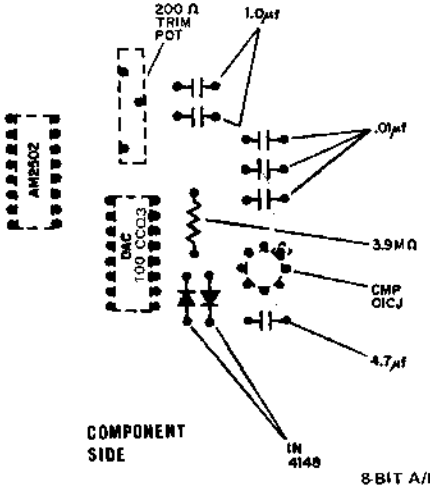
Operation with 5V Full Scale Inputs (0 to +5V, ±2.5V) may be obtained by specifying DAC-100 models with a Q4 suffix.



COMPONENT SIDE



TRACE SIDE



8-BIT A/D LAYOUT

FIGURE 8

CONNECTOR PIN CONNECTIONS

18	N.C.	V	N.C.
17	+15 Volts	U	+15 Volts
16	−15 Volts	T	−15 Volts
15	+5 Volts	S	+5 Volts
14	Power Ground ⏚	R	Power Ground ⏚
13	Power Ground ⏚	P	Power Ground ⏚
12	Analog Ground ⏚	N	Analog Ground ⏚
11	Analog Ground ⏚	M	Analog Ground ⏚
10	N.C.	L	Analog Input
9	Bipolar Reference Voltage Input	K	N.C.
8	N.C.	J	N.C.
7	$\overline{\text{Bit 1}}$	H	N.C.
6	Bit 1	F	Bit 5
5	Bit 2	E	Bit 6
4	Bit 3	D	Bit 7
3	Bit 4	C	Bit 8
2	$\overline{S}$ Start	B	$\overline{CC}$ Conversion Completed
1	Clock Input	A	DO Serial Output

CALIBRATION

For unipolar, 8-bit, 10 volt full scale calibration apply +9.941 volts (Full scale −3/2 LSB) to the input. Adjust the gain potentiometer until the digital output is alternating between "0000 0000" and "0000 0001". This calibrates the converter at a transition point insuring correct outputs over the analog input range. No zero adjust is necessary due to the low comparator input offset voltage (V_{OS}), virtually zero output offset of the DAC and the correct +1/2 LSB bias established by R1.

For 8-bit, ±5 volt full scale offset binary operation, first perform the unipolar calibration as described above with the bipolar reference removed. Next connect the +6.4 volt bipolar reference through the 500 ohm potentiometer to the bipolar input resistor. With −5.000 volts as an analog input, adjust the 500 ohm potentiometer until the digital output is alternating between "1111 1111" and "1111 1110". For calibration at lower bit resolutions refer to Table I.

PERFORMANCE

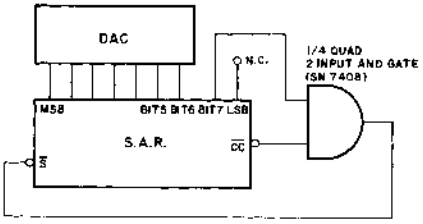
Performance of the completed converter for 6, 7 and 8 bit resolution applications is shown in Table II. To assure fully monotonic operation in 8 bit applications the DAC-100CC grade with its maximum nonlinearity of 0.2% from 0° to 70°C should be specified. Applications requiring 8-bit resolution with 0.3% or less linearity may utilize the lower cost DAC-100DD types.

All D.C. static errors can be attributed to the analog components only; the comparator makes no contribution to nonlinearity but its 25°C V_{OS} and V_{OS} drift with temperature are a consideration in the zero scale and full scale performance, and especially so in bipolar applications. The worst case DAC-100 zero error over 0° to 70°C is 0.6mV; adding to this the 3.5mV max V_{OS} of the CMP-01C results in a worst case zero scale error of 4.1mV, which is acceptably small compared to the value of 1/2 LSB (19.5mV) for the 8 bit A/D.

Because the V_{OS} drift of the CMP-01C is typically only 1.8μV/°C even without offset trimming, the full scale drift will be almost entirely a function of the DAC-100CC tempco—60ppm/°C maximum. (Tempco of DAC-100DD models is 120ppm/°C.)

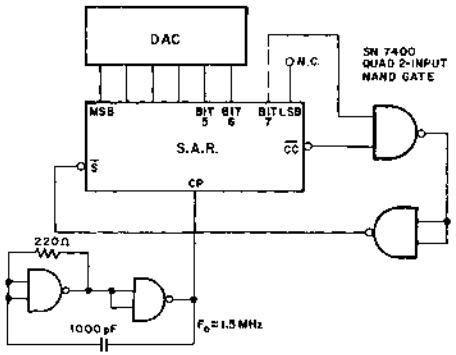
REDUCED RESOLUTION APPLICATIONS

Encoding time may be reduced in applications not requiring the full 8 bit resolution. In convert-on-command applications, the negative-going transition of the (N+1) bit may be used as the Conversion Completed ($\overline{CC}$) signal; the register will continue to step through the remaining bits so the $\overline{CC}$ level will be present for one clock period only. For continuous conversion applications, the register may be truncated by applying a low



SHORT-CYCLED CONTINUOUS CODING
(6 BITS SHOWN)
FIGURE 9A

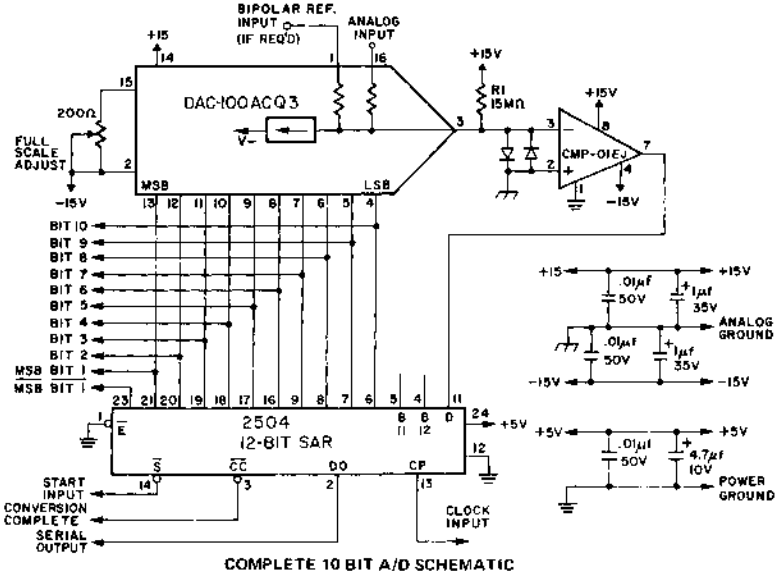
level to the $\overline{S}$ input; however, caution must be observed to prevent possible stalling on power-up: the $\overline{S}$ input should be generated by either the $\overline{CC}$ or bit (N+1) going to a low state. Figure 9 demonstrates a 6 bit, continuous-encoding application. Since reducing the resolution increases the size of the LSB, the value of R1 and the full scale calibration point should be changed accordingly, as shown in Table I. Additional speed in reduced resolution applications may be achieved by increasing the clock frequency.



SHORT-CYCLED CONTINUOUS ENCODING
(ALTERNATE METHOD INCLUDING CLOCK)
FIGURE 9B

10 BIT APPLICATIONS

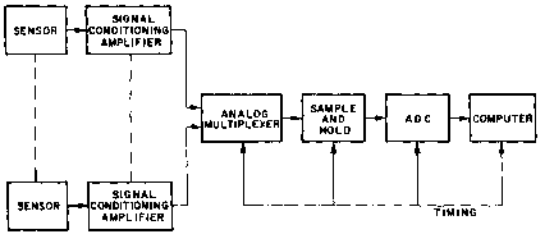
The basic 8-bit converter may easily be expanded to 10 bits by using a 2504 12 bit Successive Approximation Register; it may be allowed to step through all 12 bits or short-cycled as described above (Fig. 9A,9B). All DAC-100 Series devices have 10-bit resolution; for applications requiring 10 bit monotonic performance the DAC-100ACQ3 or Q4 grades with maximum nonlinearity of ±0.05% (0° to 70°C) should be specified; for less demanding applications the ±0.1% DAC-100BCQ3 (Q4) grades are recommended. Due to the 10mV LSB size, comparator V_{OS} can provide significant zero error. This can be eliminated in unipolar applications by nulling the CMP-01CJ or specifying the 0.8mV offset CMP-01EJ. No initial V_{OS} improvement is required in bipolar applications, as this error will be eliminated during the bipolar calibration procedure. The offsetting resistor (R1) should be 15MΩ for 10 bit applications, with the full scale calibration voltage of +9.985 for unipolar applications.



COMPLETE 10 BIT A/D SCHEMATIC
FIGURE 10

SYSTEM CONSIDERATIONS

When integrating the A/D Converter into a system, consideration must be given to several factors to assure best performance. First, the analog signal to be encoded should not change more than 1/2 LSB during the encoding process; a sample-and-hold circuit should be used if required to hold changes to 1/2 LSB or preferably, much less (Fig. 11). Second, proper grounding of the system is essential to prevent errors due to system noise. The preferred method is to connect the analog signal ground and digital power ground together at only one point, right at the A/D's connector. This will insure that digital ground currents do not flow in the analog ground line.



TYPICAL MULTIPLEXED DATA ACQUISITION SYSTEM
FIGURE 11

LOWER POWER CONSUMPTION

Power consumption may easily be reduced from 935 mW maximum to about 310 mW with two minor design changes. The D/A and comparator power supplies can be reduced from ±15 volts to ±6 volts and the low power TTL AM25LO2PC logic function may be specified. Digital output fanout is reduced to 3 standard TTL loads. The value of R1 must also be lowered accordingly to maintain the same +1/2 LSB bias current to the sum node.

MILITARY TEMPERATURE RANGE OPERATION

Operation over wider temperature ranges can be obtained by simply specifying appropriate temperature range components. The simplicity of the three IC designs coupled with the compatibility of the devices with MIL-STD-883A processing assures high reliability in military applications.

CONCLUSION

Extremely compact, rugged, low power consumption successive approximation A/D converters are made possible by combining 3 IC's: PMI's DAC-100 Series 10-bit D/A, CMP-01 comparator, and a Successive Approximation Register. This simple, low cost design opens up new applications such as one A/D per channel operation in data acquisition systems.

PARTS LIST FOR 8 BIT A/D CONVERTER

±0.3% maximum nonlinearity, FS tempco 120ppm/°C

1	DAC-100DDQ3 (or Q4)
1	CMP-01CJ
1	AM2502PC (Advanced Micro Devices) or Equivalent
1	Pot-200Ω Bourns #3006P-1-201
1	4.7 μf CAP- Mallory #TDC475M010EL
2	1.0 μf CAP- Mallory #TDC105M035EL
2	Diode, 1N4148
3	.01 μf CAP-Centralab #CK-103
1	PC Board
1	Resistor 3.9MΩ 5% 1/4W

For ±0.2% maximum nonlinearity, FS tempco 60ppm/°C use DAC-100CCQ3 (or $\overline{Q4}$)

PARTS LIST FOR 10 BIT A/D CONVERTER

±0.1% maximum nonlinearity, FS tempco 60ppm/°C

1	DAC-100BCQ3 (or Q4)
1	CMP-01EJ
1	AM2504PC (Advanced Micro Devices) or Equivalent
1	Pot-200Ω Bourns #3006P-1-201
1	4.7 μf CAP Mallory #TDC475M010EL
2	1.0 μf CAP Mallory #TPC105M035EL
2	Diode, 1N4148
3	.01 μf CAP- Centralab #CK-103
1	PC Board
1	Resistor 15MΩ 5% 1/4W

For ±0.05% maximum nonlinearity, FS tempco 60ppm/°C use DAC-100ACQ3 (or Q4)

TABLE I – REDUCED RESOLUTION APPLICATION DATA

Resolution Desired		Offset Current Value (1/2 LSB)	Conversion Complete Indicator	Full Scale Calibration Point	LSB (10 VFS)
8 Bits	3.9 MΩ	3.9 μA	$\overline{CC}$	9.941V	39 mV
7 Bits	2 MΩ	7.8 μA	Bit 8	9.883V	78 mV
6 Bits	1 MΩ	15.6 μA	Bit 7	9.766V	156 mV
5 Bits	470 KΩ	31.3 μA	Bit 6	9.531V	313 mV
4 Bits	240 KΩ	62.5 μA	Bit 5	9.163V	625 mV

TABLE II – PERFORMANCE DATA

Resolution D/A	6-Bits DAC-100DDQ3	7-Bits DAC-100DDQ3	8-Bits DAC-100CCQ3
0° to 70° Maximum Nonlinearity	±0.3%	±0.3%	±0.2%
0° to 70°C Full Scale Tempco Max.	120ppm/°C	120ppm/°C	60ppm/°C
Zero Scale Error Max.	±0.05 LSB	±0.1 LSB	±0.2 LSB
Conversion Time 1.5 MHz Clock	4.7 μsec	5.3 μsec	6.0 μsec

Unipolar Reference	Internal
Bipolar Reference	External +6.4 Volts
Input Impedance (+10V or ±5V Scale)	5KΩ Nominal
Input Impedance (+5V or ±2.5V Scale)	2.5KΩ Nominal
Quantizing Error	±1/2 LSB
Output Code Unipolar	Complementary Binary
Output Code Bipolar	Complementary Offset Binary
Clock	External
Logic Output Drive Capability	6 TTL Loads
Analog Power Supply Range	±6V to ±18V
Digital Power Supply Range	+5 Volts ±5%
Power Consumption ±15V and +5V Supplies	935 mW Max.

TEMPERATURE MEASUREMENT METHOD BASED ON MATCHED TRANSISTOR PAIR REQUIRES NO REFERENCE

by
Jim Simmons and Donn Soderquist

Most remote temperature measurements are made with thermistors or thermocouples as the sensing elements. This article shows how the function can be accomplished by using the intrinsic properties of a well-matched monolithic transistor pair. The method is attractive for its simplicity accuracy, and long-term stability. Of particular utility is the fact that the output is inherently linear and is directly useable without special linearizing circuitry.

Thermocouples can require both linearizing circuitry and reference junction making them difficult to apply. Linear outputs may be achieved with composite thermistor-resistor networks but long-term stability is difficult to predict. Ordinary silicon diodes, when operated as temperature sensors, require constant current drive and extensive calibration. The matched transistor pair method has none of these drawbacks.

BASIC THEORY

Matched transistor pairs have predictable relationships which make temperature measurements possible. To develop these relationships, let us consider the fundamental properties of a single transistor. The well known relationship between collector current and base-emitter voltage for a single transistor is:

$$1)\ V_{be} = \frac{kT}{q} \log_e \left(\frac{I_C}{I_S}\right) \quad \text{provided } I_C/I_S >> 1$$

where

k = Boltzmann's constant = 1.38×10^{-23} joules/°K
T = absolute temperature, °K
q = charge of an electron = 1.6×10^{-19} coulomb
I_S = theoretical reverse-saturation current ≅ 1.87×10^{-14} A
I_C = collector current

Consider the difference in base-emitter voltages, ΔV_{be}, of two transistors operated at the same temperature:

$$2)\ \Delta V_{be} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$$

This expression may be rewritten to:

$$3)\ \Delta V_{be} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{S1}}{I_{S2}}\right)$$

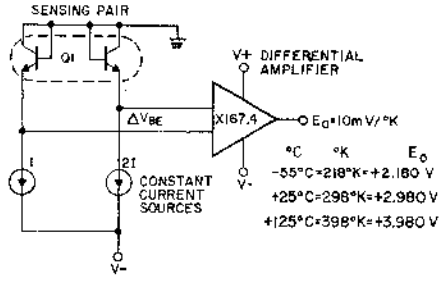
The values of I_{S1} and I_{S2} are a strong function of processing and geometry variables, and are very nearly identical in a well-matched monolithic transistor pair. As I_{S1} and I_{S2} approach equality ($\log_e 1 = 0$), the second term can be eliminated. For an ideal pair the expression becomes:

$$4)\ \Delta V_{be} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}}\right)$$

Note that if the ratio of collector currents I_{C1} to I_{C2} is made constant, ΔV_{be} will be proportional to absolute temperature alone. No absolute values of current are required because only a stable current ratio must be maintained. For a fixed ratio of 2 to 1 the expression is:

$$5)\ \frac{\Delta V_{be}}{\Delta T} = 5.973 \times 10^{-5} = 59.73 \mu V/°K$$

This predictable differential base-emitter voltage relationship allows a matched transistor pair to be used as a temperature sensor. A complete temperature measuring system can be built with a matched pair, two constant current sources, and a differential amplifier as shown in Figure 1.



BASIC TEMPERATURE SENSOR

FIGURE 1

SYSTEM DESIGN CONSIDERATIONS

To illustrate this concept, let us design a system to provide accurate temperature measurement over the range of −55°C to +125°C (218°K to 398°K). Other goals are: ease of calibration, long-term stability, standard resistor values, and small physical size. In addition, the system should be capable of operation with the sensing matched pair located up to 100 feet from the current sources and differential amplifier. A system achieving these goals is detailed below.

SENSING MATCHED PAIR

Any mismatch will cause performance to deviate from the ideal case shown in Eq. 4, the most critical parameter being average offset voltage drift (TCV_{OS}). This quantity, multiplied by the largest temperature excursion (100°K) and the differential amplifier gain (167.4), will be the output error and is shown in Table 1 for typical TCV_{OS} specifications.

Clearly, system accuracy is directly related to the degree of matching of the sensing pair. A Precision Monolithics MAT-01H with its typical TCV_{OS} of .15μV/°C was specified in order to minimize this error factor.

CONSTANT CURRENT SOURCES

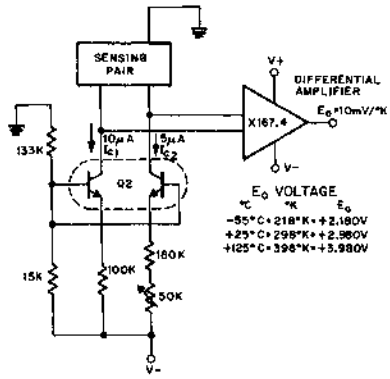
Two currents of a precise 2 to 1 ratio are provided by this section. Several considerations make 5μA and 10μA good choices as nominal operating currents for I_{C2} and I_{C1} respectively. Most monolithic matched transistor pairs are specified at I_C = 10μA. Input bias currents associated with the differential amplifier can be ignored because 5μA is three orders of magnitude larger. Resistor values are small enough to keep physical size and cost reasonable. Finally, the quiescent currents do not develop significant voltage drops in 100 feet of ordinary shielded-pair cable.

The two most important current source transistor matching characteristics required are h_{FE} and V_{OS} long-term stability, assuming that this part of the circuit is not subjected to wide temperature variations. If the system is to have good power supply and ripple rejection, the h_{FE} match must be maintained over a range of operating currents. These characteristics will insure a constant 2 to 1 ratio of I_{C1} to I_{C2} is maintained.

With the circuit as shown in Figure 2, the total system has measured power supply rejection of 1°K/volt. Once calibrated, long-term changes in V_{OS} will change the current ratio, and, in turn, the output. A Precision Monolithics MAT-01GH was selected for Q2 because it has the desired combination of specified long-term stability (.2μV/month) and close h_{FE} matching, typically 1%.

TCV_{OS}	Error in °K over 100°
.15μV/°C	.251°K
.5 μV/°C	.837°K
1.0μV/°C	1.67°K
2.0μV/°C	3.34°K
2.5μV/°C	4.19°K
5.0μV/°C	8.37°K
10 μV/°C	16.7°K

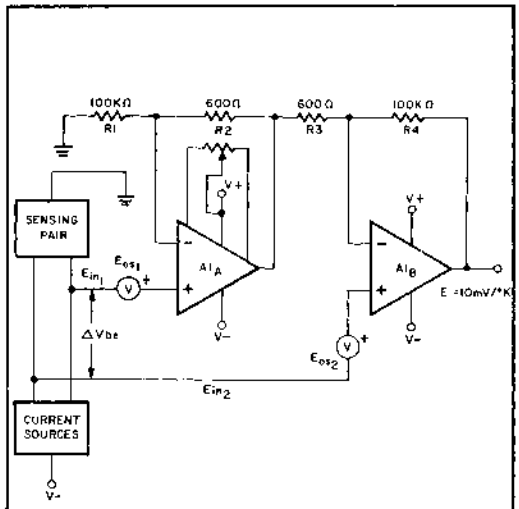
TABLE 1



BASIC TEMPERATURE SENSOR
FIGURE 1

DIFFERENTIAL AMPLIFIER

The sensing pair and constant current sources provide a differential voltage (ΔV_{be}) which is directly proportional to absolute temperature. The amplifier must acquire this voltage difference in the presence of common mode voltages, amplify it by 167.4, and change it from a differential to a single-ended signal. Excellent performance is obtained using the circuit of Figure 3.



DIFFERENTIAL AMPLIFIER DESIGN
FIGURE 3

The two op-amp differential amplifier configuration is widely used wherever high input impedance and fixed gain are required. This amplifier uses a dual matched instrumentation operational amplifier designed and specified for differential applications, the Precision Monolithics OP-10CY.

GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$6)\ E_o = \left[E_{in_1}\left(1 + \frac{R_2}{R_1}\right)\frac{R_4}{R_3}\right] + E_{in_2}\left(\frac{R_4}{R_3} + 1\right)$$

With ideal resistors this simplifies to:

$$7)\ E_o = (E_{in2} - E_{in1})\left(\frac{R4}{R3} + 1\right) \text{ provided } \frac{R1}{R2} = \frac{R4}{R3}$$

In this system, $(E_{in1} - E_{in2})$ has been previously defined as ΔV_{be}. The actual expression for E_o may be written as:

$$8)\ E_o = \Delta V_{be}\left(\frac{R4}{R3} + 1\right) \text{ but } \frac{\Delta V_{be}}{\Delta T} = 5.973 \times 10^{-5} \text{ (Eq. 5)}$$

Therefore, the ideal overall system output expression is:

$$9)\ E_o = (5.973 \times 10^{-5})\left(\frac{R4}{R3} + 1\right) T$$

COMMON MODE REJECTION

At 25°C (298°K), ΔV_{be} is 17.8 mV, while the individual sensing pair base-emitter voltages are about 520 mV. There is a need to reject the 520 mV, common mode input voltage while accurately amplifying the differential input voltage, ΔV_{be}. At −55°C (218°K), the situation becomes more difficult with ΔV_{be} of 13 mV, and 696 mV, of common mode voltage. Keeping in mind that this is a best case disregarding any extraneous cable pickup, it can be observed that the requirement for high common mode rejection is very real.

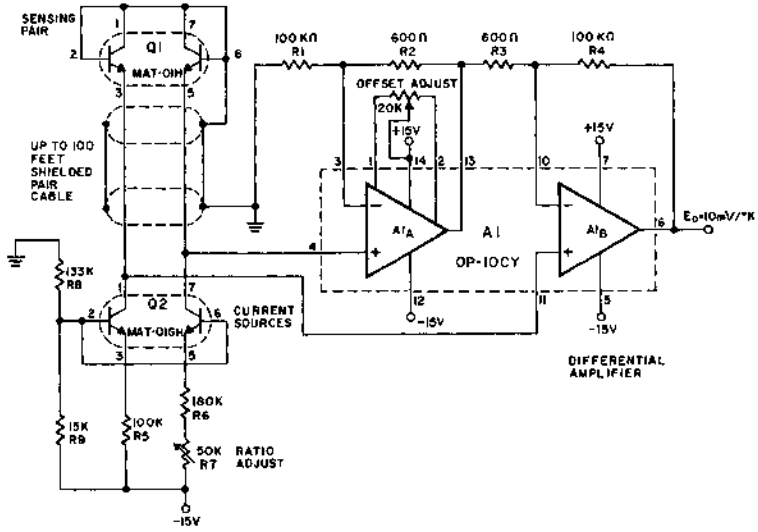
Because the dual op amp has a specified 117 dB common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching. This device eliminates the need for special opamp selections in this stringent differential amplifier application.

Resistor selections can be avoided by using readily available .01% tolerance precision resistors, resulting in a worst-case ratio match of .04%. This ratio match, in combination with the dual op amp's performance, results in greater than 100 dB common mode rejection at the amplifier's input.

Long-term stability of the resistors must approach the initial ratio match or degradation of common mode rejection can occur over time. The resistors chosen are specified at ±50ppm/3 years and ±5ppm/°C thereby assuring stability versus time and temperature.

DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage $(E_{os1} - E_{os2})$ will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected. The OP-10CY provides the additional convenience that only a single offset adjustment is necessary to provide the required ΔV_{os} match; this adjustment at the same time provides minimum $TC\Delta V_{os}$ of the differential amplifier.



COMPLETE SCHEMATIC
FIGURE 4

INSTALLATION

Ordinary shielded pair cable, with #22 or larger conductors, is satisfactory for most remote temperature measuring applications. Good thermal conductivity from the sensing pair's case to the environment being measured is essential to avoid incorrect readings. When this circuit is used for temperature control, thermally-conductive epoxy works especially well in attaching the sensing pair to the device being controlled.

CALIBRATION PROCEDURE

This is an easy two-step procedure. First, short the differential amplifier inputs and adjust the offset potentiometer until the output reads zero volts. Remove the input short. Second, with the sensing pair at a known temperature (room temperature is suitable), adjust the ratio potentiometer for a correct differential amplifier output reading. Having the capability of room temperature calibration makes this circuit much more convenient to calibrate than other types.

OVERALL ACCURACY

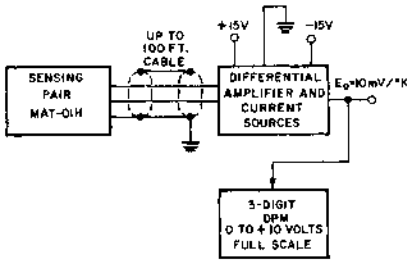
This circuit, with the components as specified, is capable of ±1°K accuracy over the full military temperature range of −55°C to +125°C (218°K to 398°K). Optimum accuracy is obtained with the differential amplifier and constant current sources in a controlled environment remote from the sensing pair. Maintenance of high accuracy over long periods of time is achieved because all components used in this design have long-term stability specified.

APPLICATIONS

The circuit's output, as measured by a 10-volt full scale digital panel meter, makes a digital thermometer. DPM's with BCD outputs may be used in applications requiring simultaneous direct readout and digital outputs for control purposes.

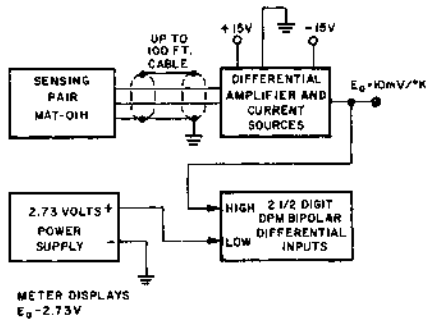
CONCLUSIONS

Accurate temperature measurement and control systems are easily and economically built using the predictable characteristics of modern monolithic matched transistor pairs. This method offers long-term stability, excellent linearity, simple calibration, and high performance in severe environments.



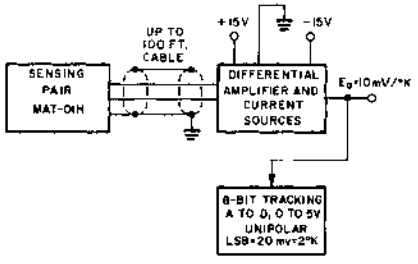
°C °K E_0
-55°C=218°K=2.18V
+25°C=298°K=2.98V
+125°C=398°K=3.98V

BASIC DIGITAL THERMOMETER WITH READOUT IN DEGREES KELVIN (°K)
FIGURE 5



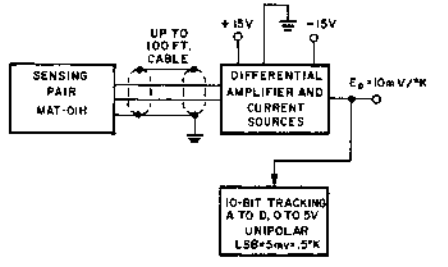
-55°C= -.55 V
+25°C= +.25 V
+125°C= +1.25 V

DIGITAL THERMOMETER WITH READOUT IN °C
FIGURE 6



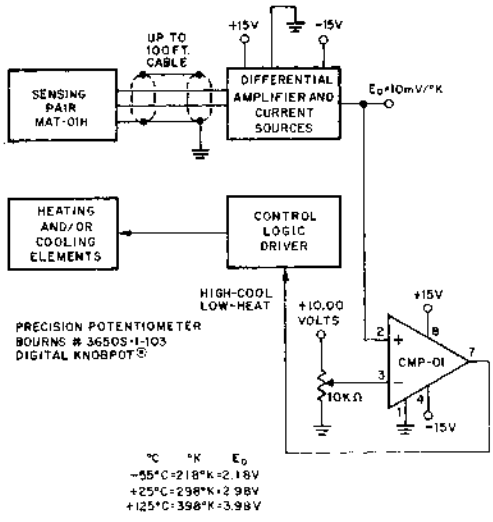
°C °K E_0
-55°C=218°K=2.18V
+25°C=298°K=2.98V
+125°C=398°K=3.98V

BINARY-CODED TEMPERATURE READINGS WITH 2° RESOLUTION
FIGURE 7

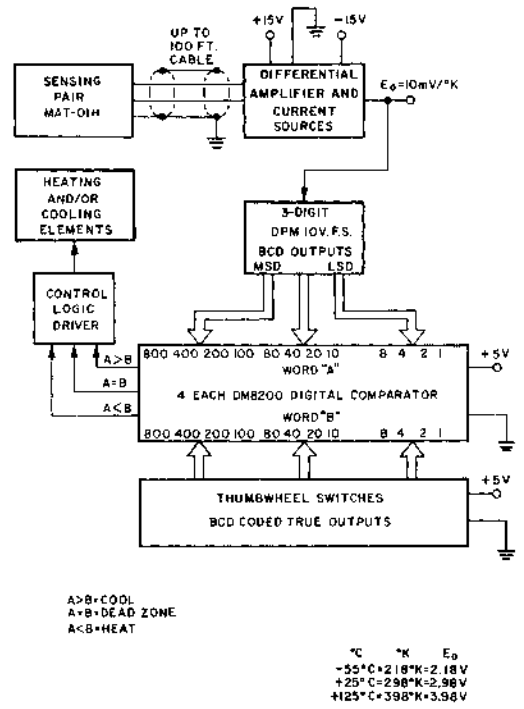


°C °K E_0
-55°C=218°K=2.18V
+25°C=298°K=2.98V
+125°C=398°K=3.98V

BINARY-CODED TEMPERATURE READINGS WITH 5° RESOLUTION
FIGURE 8



TEMPERATURE CONTROLLER – DIGITAL DIAL CONTROLLED
FIGURE 9



TEMPERATURE CONTROLLER – DIGITAL THERMOMETER
FIGURE 10

PARTS LIST

1.	Q1	MAT-01H, Matched Transistor Pair Precision Monolithics, Inc.
2.	Q2	MAT-01GH, Matched Transistor Pair Precision Monolithics, Inc.
3.	A1	OP-10CY, Dual Instrumentation Op Amp Precision Monolithics, Inc.
4.	R1, R4	Resistor, 600 ohms, .01% General Resistance Econistor
5.	R2, R3	Resistor, 100Kohms, .01% General Resistance Econistor
6.	R5	Resistor, 100Kohms, .1% General Resistance Econistor
7.	R6	Resistor, 180Kohms, .1% General Resistance Econistor
8.	R7	Potentiometer, 50Kohms, 10% Bourns #3006P-1-503
9.	R8	Resistor, 133Kohms, 1% RN55C1333F
10.	R9	Resistor, 15Kohms, 1% RN55C1502F
11.	R10	Potentiometer, 20Kohms, 10% Bourns #3006P-1-203

THE OP-07 ULTRA-LOW OFFSET VOLTAGE OP AMP— A BIPOLAR OP AMP THAT CHALLENGES CHOPPERS. ELIMINATES NULLING

by

Donn Soderquist & George Erdi

The OP-07, a new bipolar-input monolithic operational amplifier, provides chopper-stabilized amplifier performance at bipolar prices. Input offset voltage, the major error contribution in most designs, is reduced to a maximum of 25μV by a new computer-controlled on-chip trimming technique. Such low V_{OS} eliminates the nulling potentiometer requirement of most op amp circuits, greatly reducing system complexity while improving reliability. A description of this amplifier's design and performance is given, followed by an applications section showing how superior input specifications can simplify high-accuracy analog design.

IMPORTANCE OF LOW INPUT OFFSET VOLTAGE

In many applications, the initial input offset voltage of operational amplifiers causes more inaccuracy than all other error factors combined. The other significant error parameters, such as bias and offset currents, open-loop gain, and common mode rejection, have come closer to theoretically ideal performance than has V_{OS}. For this reason, most operational amplifiers, monolithic and modular, are provided with terminals to allow the user to adjust this offset voltage to zero—a costly and potentially unreliable procedure, which in many cases degrades performance of TCV_{OS}. Monolithic op amp manufacturers have constantly strived for improvement in V_{OS} from μA709 and μA741 at 5000μV, to the μA725 at 1000μV in 1969, to the OP-05A at 150μV in 1972. The OP-07A at 25μV maximum V_{OS} is a significant milestone in monolithic bipolar operational amplifier design.

Temperature stability is also important since the benefits of low initial V_{OS} are quickly lost if a small change in operating temperature causes substantial V_{OS} drift. Good long-term V_{OS} stability is required to avoid periodic re-calibrations and degradation of system performance over time. Until now, chopper-stabilized or externally-nulled monolithic op amps have been the usual choices despite the disadvantages of high noise and/or external components. The OP-07 design achieves the desired combination of low V_{OS}, low TCV_{OS}, long-term V_{OS} stability, low bias current, and low noise. It provides performance comparable to chopper-stabilized amplifiers with the further advantages of freedom from chopper-frequency noise and external component requirements.

LOW V_{OS} AMPLIFIERS

Some of the more common methods for optimizing V_{OS} performance have been chopper-stabilized amplifiers, bipolar amplifiers nulled to zero initial V_{OS}, and combinational amplifiers constructed with a matched transistor pair followed by a standard bipolar op amp. Each approach to the V_{OS} problem is a compromise between allowable error, reliability and price. The purpose of this discussion is to show how the OP-07 provides superior performance, higher reliability, and reduced size at a lower overall cost.

CHOPPER-STABILIZED AMPLIFIERS

In the past, designers have been forced to use chopper-stabilized amplifiers in applications requiring less than 100μV initial V_{OS}. The OP-07 is a cost-effective alternative, providing chopper-type performance with 741 ease-of-application. Use of a bipolar input op amp eliminates the usual chopper problems of high noise, large physical size, and limited common-mode input voltage range.

Low initial input offset voltage specifications lose their significance if noise and long-term drift are of the same magnitude. Although the monolithic choppers have lower average input bias currents, the chopping action produces very large spikes in the input currents and prevents their use with large or unbalanced source resistors. For this reason, most chopper manufacturers carefully avoid specifying noise currents above 10Hz. The bias current remains below 4nA over the full military temperature range, and being free from chopper spikes, enables use in high impedance circuitry.

Another chopper-related problem is that input signals often interact with chopping frequency components and their harmonics. This interaction can cause errors due to intermodulation, producing slowly varying offset voltages usually below 20Hz. Chopper frequency switching transients can also cause electromagnetic interference frequently requiring special shielding and input guarding methods to protect adjacent circuitry. Modular choppers can have input overload recovery times as high as five seconds and require up to ten external components to effectively eliminate this problem. Monolithic choppers require expensive, large external components, such as two .1μF teflon dielectric capacitors, for wide temperature range operation. These problems are eliminated by the OP-07.

NULLED BIPOLAR AMPLIFIERS

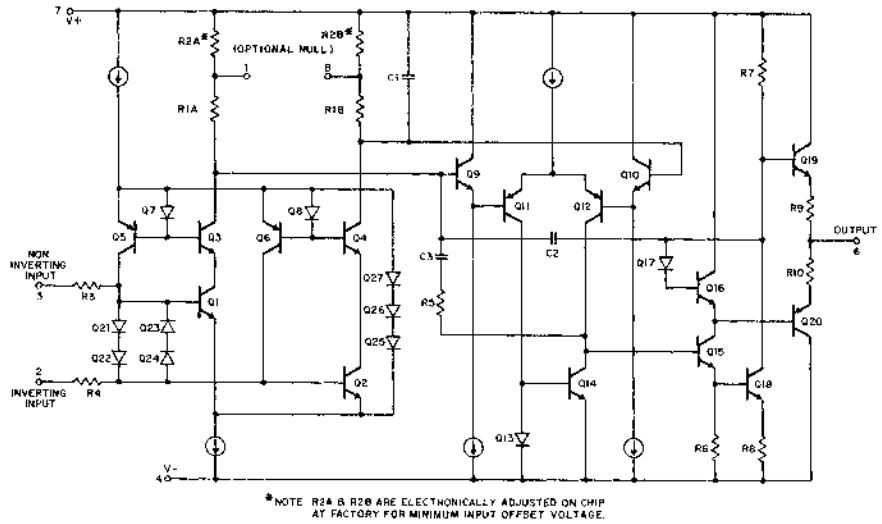
The major disadvantage of most high performance bipolar op amps is that their high initial V_{OS} must be adjusted to zero with a nulling potentiometer or trimming resistors. In certain amplifiers, this is also a requirement in order to optimize TCV_{OS} performance. Selected or adjusted components require special test labor, take up much-needed space, decrease reliability, and add to system complexity. "Maintainability" is poor—field replacements or renulling due to long-term V_{OS} and resistance changes must be performed by a skilled technician with sophisticated test equipment. Use of an internally-nulled OP-07 avoids all of these problems since it is a complete, fully-interchangeable device, and does not require zeroing to optimize TCV_{OS}.

COMBINATIONAL AMPLIFIERS

This is one of the oldest methods, usually implemented with a heated-substrate matched transistor pair in a differential-input gain stage followed by a conventional op amp. This method requires four precision resistors, a nulling potentiometer, external frequency compensation, and up to 360mW of heater power. TCV_{OS} is only about $2\mu V/^{\circ}C$ despite the temperature control for the input pair. The OP-07 provides improved performance in all parameters as well as lower cost, elimination of calibration labor, lower noise and a tremendous reduction in total power consumption.

CIRCUIT DESCRIPTION

The three-stage design concept of previous Precision Monolithics' instrumentation quality op amps was retained for the OP-07 because, using this design, nulling of V_{OS} simultaneously optimizes TCV_{OS}. (This relationship is not the case for the more commonly used two-stage "741"-type amplifier.) There are additional advantages of high gain, low noise, and predictable long-term stability. Low input bias current is achieved by bias current cancellation; i.e., currents are generated equal in magnitude but opposite in direction to the base currents of the input transistors Q1 and Q2 in the simplified schematic of Figure 1.

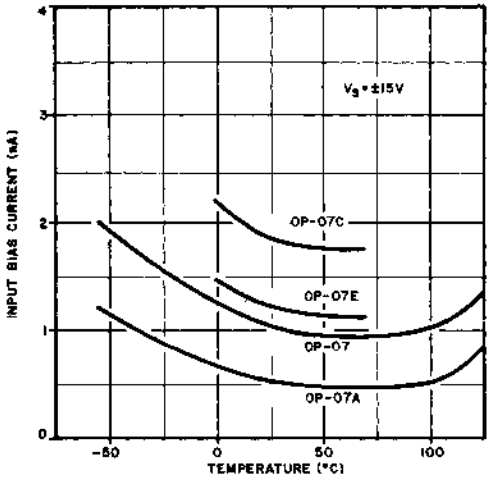


OP-07 SIMPLIFIED SCHEMATIC
FIGURE 1

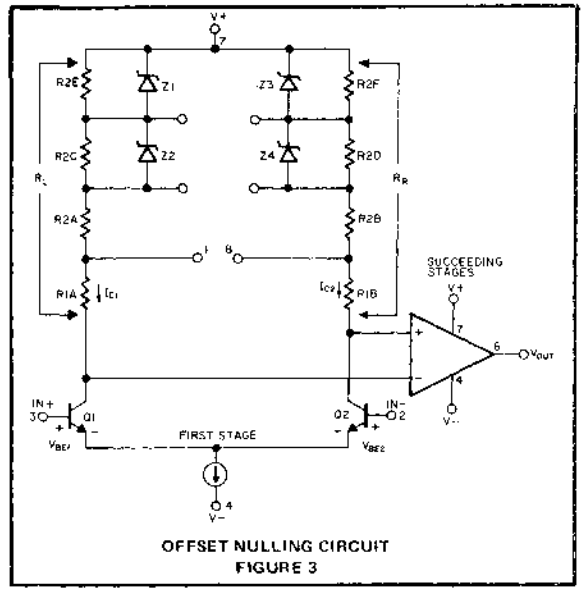
INPUT STAGE

To achieve lowest initial V_{OS}, TCV_{OS} and noise, a simple differential input pair, Q1 and Q2, was chosen. V_{OS} nulling resistors R2A and R2B are electronically adjusted and will be covered separately in the trimming discussion. R3 and R4, in conjunction with Q21-Q24, provide input differential overvoltage protection.

The symmetry of the input stage allows examination of only one side to demonstrate bias current cancellation. Base drive for the input transistor, Q1, is provided by Q5 and the external circuitry; the difference between Q5's collector current and Q1's base current being the input bias current. Q1 and Q3 are h_{FE}-matched transistors operating at similar collector currents and, therefore, the base current of Q1 is approximately equal to the base current of Q3. Q3's base current is supplied by Q7, a diode-connected PNP transistor closely matched to Q5. Together Q5 and Q7 form a current mirror (turnaround) and the collector current of Q5 will equal the base current of Q3. In this manner almost all base current for Q1 is provided by Q5 and precise bias current cancellation is achieved. Careful design has enabled this cancellation to be effective over a wide temperature range. (Fig. 2).



INPUT BIAS CURRENT VS. TEMPERATURE
FIGURE 2



OFFSET NULLING CIRCUIT
FIGURE 3

FOLLOWING STAGES

The first stage output is buffered by emitter followers Q9 and Q10, and applied to a high-gain differential stage, Q11 and Q12. Its output, the junction of Q12, Q14, Q15, and R5, drives a short-circuit-protected complementary emitter follower power output stage.

COMPENSATION

Frequency compensation of the OP-07 is accomplished using three capacitors. Feedforward capacitor C3 bypasses the second stage lateral pnp's at high frequencies and, therefore, the excessive phase-shift normally associated with these transistors is circumvented. The dominant pole of the amplifier is set by C_2 which feeds back around the second and driver stages and rolls off the open loop response at 20dB decade. The presence of C_1 ensures that the high frequency signal path is single-ended by rolling off the response of one side of the input stage. The total internal capacitance on the 100 X 53 mil chip is 210pF, a remarkable amount for a monolithic device.

LAYOUT

The circuit layout has thermal symmetry, a concept which has been used quite extensively on precision amplifier designs since its inception in 1969.[†] Variations in power dissipation in the driver and output stages, and the resultant thermal gradients affect the critical input transistors identically, thereby preventing offset voltage changes at the input.

INTERNAL NULLING TECHNIQUE

To understand the nulling technique some fundamental relationships should be examined using the equivalent circuit of Fig. 3. (Errors caused by the second stage are effectively divided by the first stage gain and will be neglected in this discussion.) V_{OS} is defined as the voltage which must be applied between the input terminals to obtain zero voltage at the amplifier's output. Referring to Fig. 3:

[†]Editor's note: This concept was originally introduced by George Erdi during his employment at Fairchild Semiconductor Research and Development.

1) $V_{OS} = V_{be1} - V_{be2}$, V_{out} = zero

With an error free second stage it may be assumed that the input transistor collectors are equal in potential.

2) $I_{C1}R_L = I_{C2}R_R$ and $\frac{I_{C1}}{I_{C2}} = \frac{R_R}{R_L}$

3) $V_{be} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right)$, $V_{be2} = \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$.

Provided $I_C/I_S >> 1$.

Substituting in Eq. 1:

4) $V_{OS} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$

Rewriting:

5) $V_{OS} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}\right)$

Substituting from Eq. 2:

6) $V_{OS} = \frac{kT}{q} \log_e \left(\frac{R_R}{R_L} \cdot \frac{I_{S2}}{I_{S1}}\right)$

For V_{OS} = zero:

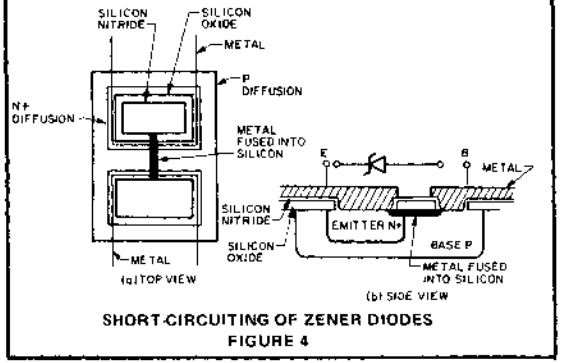
7) $\frac{R_R}{R_L} \cdot \frac{I_{S2}}{I_{S1}} = 1$

Where:

k = Boltzmann's constant = 1.38×10^{-23} joules/°K
T = Absolute temperature, °K
q = Charge of an electron = 1.6×10^{-19} coulomb
I_S = Theoretical reverse saturation current
I_C = Collector Current

Therefore, by adjusting the ratio of $\frac{R_R}{R_L}$ the inherent processing-related differences in I_{S1} and I_{S2} which cause V_{be} differentials may be cancelled. Earlier amplifier designs achieved the adjustment of collector resistance by an external nulling potentiometer between Pin 1 and Pin 8 with its wiper connected to Pin 7 (Fig. 1).

In the OP-07, permanent nulling is accomplished by shorting out a small percentage of R_R or R_L as determined by a computer programmed with Eq. 6 and a lookup table. This is done by reading V_{OS} before trimming, comparing its magnitude and polarity with a lookup table value, and shorting out one of the normally nonconducting zener diodes. The short is created by passing a high current pulse through the selected zener, fusing its metal contacts into the silicon as shown in Figure 4. High volume production is achieved through automation, with initial device testing at wafer probe including V_{OS} trimming requiring less than one second.



SHORT-CIRCUITING OF ZENER DIODES
FIGURE 4

Through this technique, V_{OS} of the entire "raw" OP-07 distribution can be nulled to less than 150 μV, with the majority being under 75 μV. Prime grade yields are high, providing adequate numbers of OP-07A devices with a V_{OS} maximum of 25 μV.

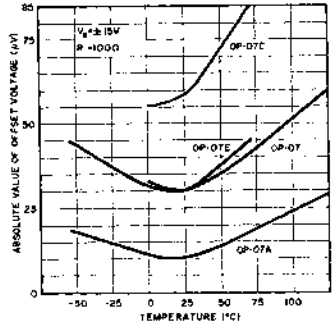
PERFORMANCE

The specifications in Table I and curves of Figure 5 show noise, initial V_{OS}, and long-term stability performance unsurpassed by any other monolithic op amp. This device is free of the common problems of latchup, noise, compensation capacitors, and narrow power supply limitations. Power supply rejection ratio (PSRR) exceeds 100dB over the unusually wide range of ±3 to ±18 volts. Common-mode rejection is specified over a full ±13 volt input range allowing small signal amplification in high noise environments and use in inverting, noninverting, and differential applications. The amplifier is completely self-contained—no external compensation or protection components are required. It is an excellent replacement for chopper-stabilized amplifiers where reductions in cost, noise, size, and power consumption are desired, and for monolithic op amps where elimination of the offset nulling potentiometer is desirable.

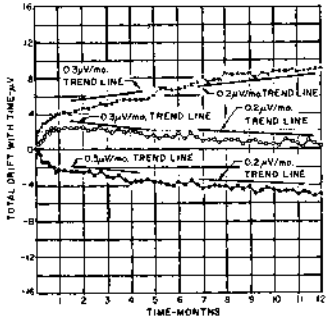
OP-07 PERFORMANCE @ V_S = ±15V, T_A = 25°C

Parameter	Typical	Min/Max	Units
Offset voltage, V_{OS}	10	25	µV
drift with temperature	0.2	0.6	µV/°C
drift with time	0.2	1.0	µV/mo
Offset current, I_{OS}	0.3	2.0	nA
drift with temperature	5	25	pA/°C
Input bias current, I_B	±0.7	±2.0	nA
drift with temperature	8	25	pA/°C
Noise voltage 0.1Hz to 10Hz	0.35	0.6	µV p-p
Noise current 0.1Hz to 10Hz	14	30	pA p-p
Input resistance – differential	80	30	MΩ
Input resistance – common mode	200	–	GΩ
Common-mode rejection	126	110	dB
Power supply rejection	110	100	dB
Voltage gain	500	300	V/mV
Slew-rate	0.25	–	V/µsec
Unity gain bandwidth	1.2	–	MHz

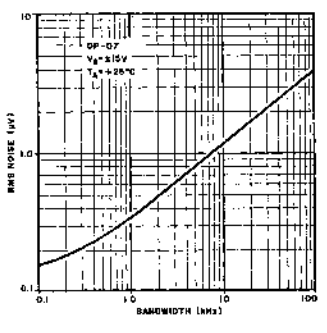
OP-07A PERFORMANCE
TABLE I



UNTRIMMED OFFSET VOLTAGE
VS. TEMPERATURE
FIGURE 5A



OFFSET VOLTAGE STABILITY
VS. TIME
FIGURE 5B



INPUT WIDEBAND NOISE VS.
BANDWIDTH
(.1Hz TO FREQUENCY INDICATED)
FIGURE 5C

The pinout of the OP-07 allows direct replacement of 725, 108, and OP-05 types without circuit changes while 741 devices may be replaced by removal of the nulling potentiometer. HA-2900 series chopper-stabilized amplifiers may be replaced by removing the two .1μf capacitors and the 1500pf capacitor whenever cost or noise reductions are required. Table II is included to show comparative performance in wide temperature range applications.

TABLE II

MILITARY TEMPERATURE RANGE PERFORMANCE COMPARISON

Manufacturer's Part Number	V_{OS} Max -55°/+125°C	TCV_{OS} Max -55°/+125°C (Unnulled)	Voltage Noise Typical F=10Hz	Current Noise Typical F=10Hz	I_{Bias} Max -55°/+125°C	Long-Term Drift Typical
OP-07A	60μV	.6μV/°C	10.3nV/$\sqrt{Hz}$	.32pA/$\sqrt{Hz}$	4nA	.2μV/mo
OP-07	200μV	1.3μV/°C	10.3nV/$\sqrt{Hz}$	.32pA/$\sqrt{Hz}$	6nA	.2μV/mo
HA-2900	60μV	.6μV/°C	900nV/$\sqrt{Hz}$	Not Specified (Chopper)	1nA	Not Specified
OP-05A	240μV	.9μV/°C	10.3nV/$\sqrt{Hz}$	.32pA/$\sqrt{Hz}$	4nA	.2μV/mo
OP-05	700μV	2.0μV/°C	10.3nV/$\sqrt{Hz}$	.32pA/$\sqrt{Hz}$	6nA	.2μV/mo
μA725	1500μV	5.0μV/°C	15mV/$\sqrt{Hz}$	1.0pA/$\sqrt{Hz}$	200nA	Not Specified
LM108A	1000μV	6.0μV/°C	43nV/$\sqrt{Hz}$	Not Specified	3nA	Not Specified

Table III compares various OP-07 versions with competitive op amps over the 0°/70°C temperature range. An absence of noise and long-term stability specifications for some amplifiers should caution potential users of possible deficiencies in those areas. This same comment would apply to "typical-only" specifications since accurate predictions of circuit performance can only be made with a fully specified device.

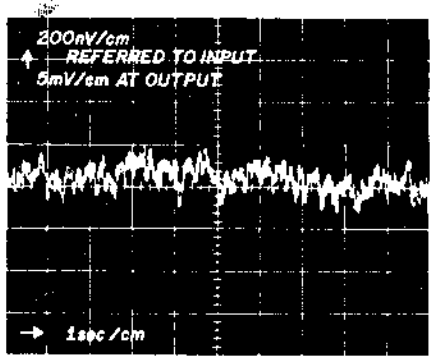
TABLE III

COMMERCIAL TEMPERATURE RANGE PERFORMANCE COMPARISON

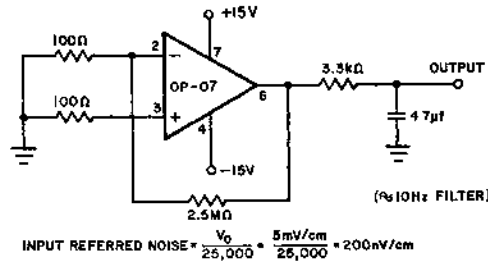
Manufacturer's Part Number		V_{OS} Max. 0°/70°C	Long Term Drift Typical	Long Term Drift Maximum	Voltage Noise Typical 0.1Hz to 10Hz	Voltage Noise Maximum 0.1Hz to 10Hz
OP-07A	(M)	45μV	.2μV/mo	1.0μV/mo	.35μV p-p	.6μV p-p
OP-07	(M)	130μV	.2μV/mo	1.0μV/mo	.35μV p-p	.6μV p-p
OP-07E	(C)	130μV	.3μV/mo	1.5μV/mo	.35μV p-p	.6μV p-p
OP-07C	(C)	250μV	.4μV/mo	2.0μV/mo	.38μV p-p	.65μV p-p
LM108A	(M)	726μV	Not Specified	Not Specified	Not Specified	Not Specified
HA-2900 Chopper-Stabilized	(M)	60μV	Not Specified	Not Specified	35μV p-p	Not Specified
HA-2906 Chopper-Stabilized	(C)	80μV	Not Specified	Not Specified	35μV p-p	Not Specified
AD504M	(C)	545μV	10μV/mo	Not Specified	Not Specified	.6μV p-p
AD508L	(C)	612μV	Not Specified	10μV/mo	1.0μV p-p	Not Specified
Typical Inverting-Only Chopper Module	(C)	95μV	2.0μV/mo	Not Specified	1.7μV p-p	Not Specified

M = -55°/+125°C Range Device
C = 0°/+70°C Range Device

NOISE PERFORMANCE



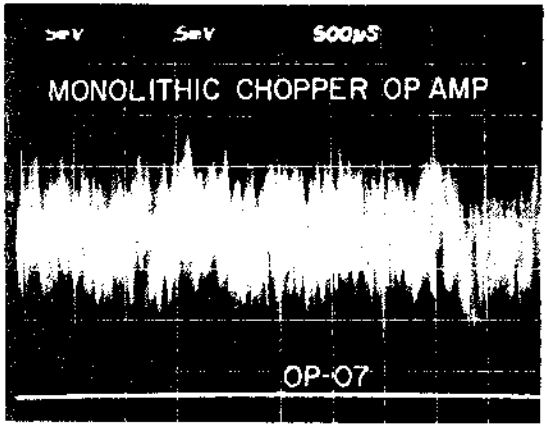
LOW FREQUENCY NOISE
FIGURE 6A

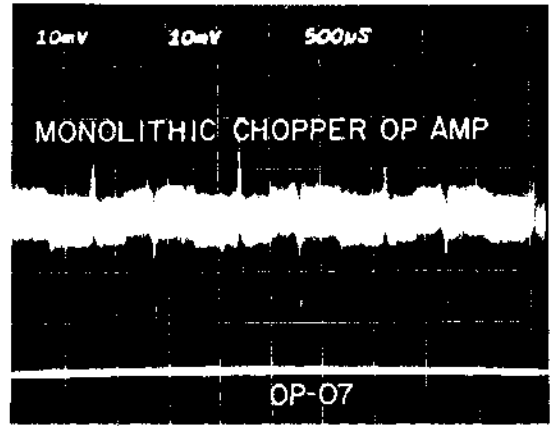


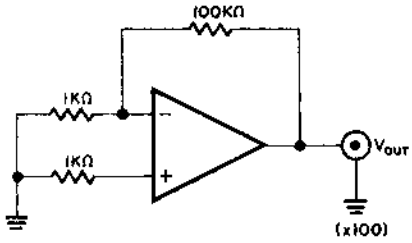
LOW FREQUENCY NOISE TEST CIRCUIT
FIGURE 6B

The low frequency noise photograph in Figure 6A shows .35μVp-p input voltage noise (0.1Hz to 10Hz), the best performance available in an instrumentation op amp at this writing. The wideband voltage noise comparison photograph (Fig. 7A) shows relative performance of a OP-07 and a monolithic chopper in the same X100 configuration; the chopper is seen to have at least 200μVp-p noise referred to the input. Clearly, low V_{OS} specifications are not very meaningful if input voltage noise is the predominant error factor.

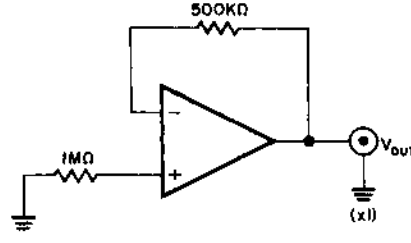
Chopper-frequency noise is a common mode current noise occurring at the chopping frequency due to switching transients. The effect of a 500Kohm source mismatch is shown in the wideband current noise photograph comparing a OP-07 with a monolithic chopper in the non-inverting buffer application (Fig. 7B). High source impedance circuits require low input noise currents, which as the photograph illustrates, can be larger than input bias current with certain operational amplifiers.







WIDEBAND VOLTAGE NOISE VS CHOPPER
FIGURE 7A



WIDEBAND CURRENT NOISE VS CHOPPER
FIGURE 7B

LONG TERM V_{OS} DRIFT

Input offset voltage drift over time has three components. Warmup drift, first month drift, and trend line stability.

Warmup drift is a change in V_{OS} occurring in the first few minutes of operation. In order to produce high volumes of OP-07's, V_{OS} is measured .5 seconds after application of power using automated test equipment. The pass limits are "guard-banded" or made small enough with respect to the V_{OS} maximum specification to compensate for not having directly observed warmup drift. In addition, offset voltage on the OP-07A selection is measured five minutes after power supply application at 25°C, –55°C and +125°C.

The first month stability, defined as changes in V_{OS} from one hour to 30 days, is typically 2.5μV. Even with closely maintained equipment, individual measurements with time can suffer from inaccuracies on the order of a half-microvolt due to low frequency noise and slight temperature variations. Fortunately, over a large number of measurements these errors tend to integrate out, and an accurate trend line can be defined.

The trend line is defined as the drift per month averaged over the month one to month twelve period, and is generally an order of magnitude better than the first month drift (Fig. 5B). Over 1.7 million device hours of testing and characterization have been logged in order to accurately specify long-term V_{OS} stability. Results indicate an average trend line drift of 0.2μV/month-outstanding stability performance for any amplifier, regardless of its technological approach.

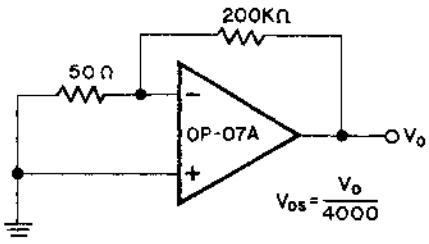
LONG-TERM V_{OS} TESTING CONDITIONS

The deceptively simple circuit of Fig. 8 is used for long-term V_{OS} stability testing. Three absolutely essential conditions must exist for accurate measurements: still air, power supply accuracy, and long-term temperature control.

All components, including sockets and solder joints, are enclosed in a metal box to eliminate air movement and temperature gradients. Thermoelectric error voltages may be generated if the dissimilar metal junctions formed by solder joints and socket contacts are at different temperatures. This effect is minimized by using "low thermal" solder (70% Cadmium, 30% Tin) and nonmetallic flux, such as Kester #1544, to avoid ionic contamination.

Although the power supply rejection ratio (PSRR) of the OP-07 is extremely high, nevertheless it should be considered as a potential error factor in long-term V_{OS} testing. The power supplies are verified to be at ±15 volts ±10mV before each set of weekly readings. This removes any possible significant errors due to the PSRR specification of 110dB (3μV/Volt).

All long-term V_{OS} testing is performed in a controlled laboratory environment of 30°C to eliminate TCV_{OS}, 0.2μV/°C, as an error possibility.



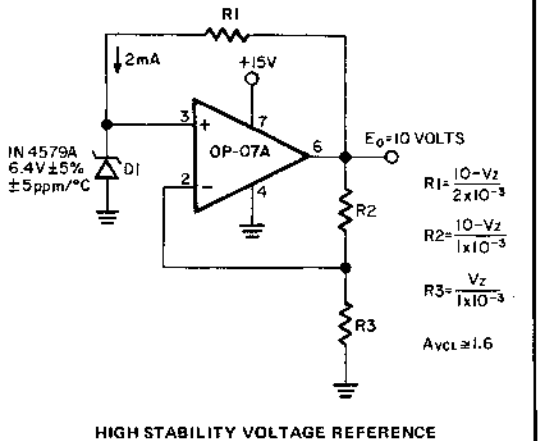
LONG TERM OFFSET VOLTAGE TEST CIRCUIT
FIGURE 8

APPLICATIONS OF OP-07

HIGH STABILITY VOLTAGE REFERENCE

The simple bootstrapped voltage reference circuit of Figure 9 provides a precise 10 volts virtually independent of changes in power supply voltage, ambient temperature, and output loading. Correct zener operating current of exactly 2mA is maintained by R1 a selected 5ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: The 5ppm/°C temperature coefficient of D1, 1ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of 5μV/°C contributes .8ppm/°C of output error while the OP-07 at .3μV/°C (0.5ppm/°C) effectively eliminates TCV_{OS} as an error consideration.

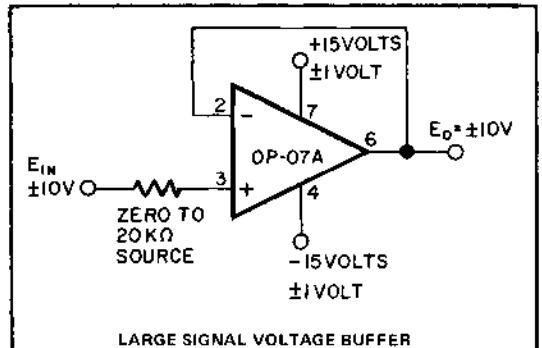


HIGH STABILITY VOLTAGE REFERENCE
FIGURE 9

Perhaps the most easily overlooked accuracy requirement in this and many other critical circuits, is long-term V_{OS} stability. In this circuit, a 741 drifting at 100μV/mo would cause 200ppm/year of output drift—a very large amount. This type of problem is particularly troublesome in potted subassemblies where periodic recalibration is impossible. Use of the OP-07 at 1μV/mo maximum avoids this potentially troublesome condition.

LARGE SIGNAL BUFFER—.005% WORST-CASE ACCURACY

Unity gain large-signal buffers are one of the most common applications of operational amplifiers. The low V_{OS} and high CMRR of the OP-07 provide high accuracy, and small physical size is achieved due to the complete absence of external components. Performance over the appropriate temperature range is shown for the various OP-07 selections. Note that the errors on Table IV are absolute worst-case numbers, a combination that would be extremely unlikely in actual practice. A figure closer to expected overall performance based on the RMS sum of typical errors is also included. Typical mil temp range error for the OP-07A is 44μV—far smaller than most other amplifiers' input offset voltage error alone.



LARGE SIGNAL VOLTAGE BUFFER
FIGURE 10

TABLE IV

LARGE SIGNAL VOLTAGE BUFFER ERROR ANALYSIS

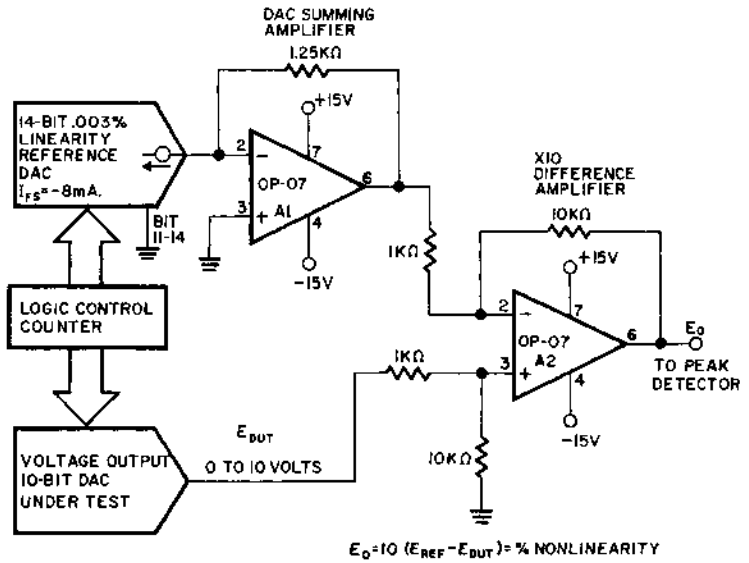
Error Source	OP-07A −55°/+125°		OP-07 −55°/+125°		OP-07E 0°/+70°		OP-07C 0°/+70°	
	Min/Max	Typical	Min/Max	Typical	Min/Max	Typical	Min/Max	Typical
V_{OS}[1]	60μV	25μV	200μV	60μV	130μV	45μV	250μV	85μV
I_{Bias}[1]	80μV	20μV	120μV	40μV	110μV	30μV	180μV	44μV
CMRR[1]	50μV	7μV	50μV	7μV	70μV	7μV	141μV	10μV
PSRR[1]	40μV	10μV	40μV	10μV	63μV	13μV	100μV	20μV
Gain[1]	50μV	25μV	67μV	25μV	56μV	22μV	100μV	25μV
ΔV_{OS} 5 years	60μV	12μV	60μV	12μV	90μV	18μV	120μV	24μV
Total	340μV	44μV*	537μV	78μV*	519μV	63μV*	891μV	104μV*
Percent Full Scale	.0034%	.0005%*	.0054%	.0008%*	.0052%	.0006%*	.009%	.001%*

*RMS Calculation

[1]Full operating temperature range specifications.

CALIBRATION-FREE DAC TESTING SYSTEM

The circuit of Figure 11 is part of an automated test system used for measuring 6-bit to 10-bit DAC nonlinearity at each possible digital input code combination. It detects the largest difference between a 14-bit linear reference DAC and a unit under test, and generates an output voltage that is directly proportional to nonlinearity as a percentage of full scale.



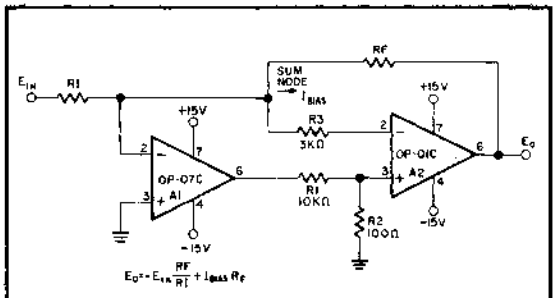
D/A CONVERTER TEST SYSTEM
FIGURE 11

Reference DACs are frequently supplied having current-output only, with selection of a summing amplifier left up to the user. Summing amplifier characteristics must not cause degradation of reference DAC linearity, full-scale, or zero scale performance or erroneous testing could occur. In addition, V_{OS} errors are direct zero scale output errors, so both long term V_{OS} stability and drift over temperature are important. Using a OP-07, total E_{ref} errors due to op amp performance are estimated at less than 100μV or .2LSB on a 14-bit base, permanently eliminating zero calibration while maintaining test system accuracy. Summing amplifier applications requiring higher speed should use the composite amplifier of Figure 12.

Another OP-07 is used in the difference amplifier for high common mode rejection and V_{OS} stability. This op amp is well-suited for critical test system circuits, providing accurate measurements, high reliability, and calibration-free operation.

COMPOSITE SUMMING AMPLIFIER WITH HIGH SLEW RATE AND LOW V_{OS}

The circuit configuration of Figure 12 is a method for obtaining a 18V/μsec slew rate with OP-07 V_{OS} characteristics. V_{OS} of A2 (3mV) is continuously nulled by forcing the sum node to equal V_{OS} of A1 through a secondary feedback loop formed by R1, R2, A2's input stage, and R3. An error due to I_{Bias} of A2 limits practical values of feedback resistances to a maximum of 5KΩ in most applications; a fast FET input op amp could be used as A2 to reduce the circuit's bias current to approximately 2nA. The circuit is also good as a current-output DAC summing amplifier because zero scale offset adjustments are not required and high speed is preserved. Composite connections such as this are generally quite cost-effective compared to single op amps having both high slew rate and good V_{OS} specifications



HIGH SPEED, LOW V_{OS} COMPOSITE AMPLIFIER
FIGURE 12

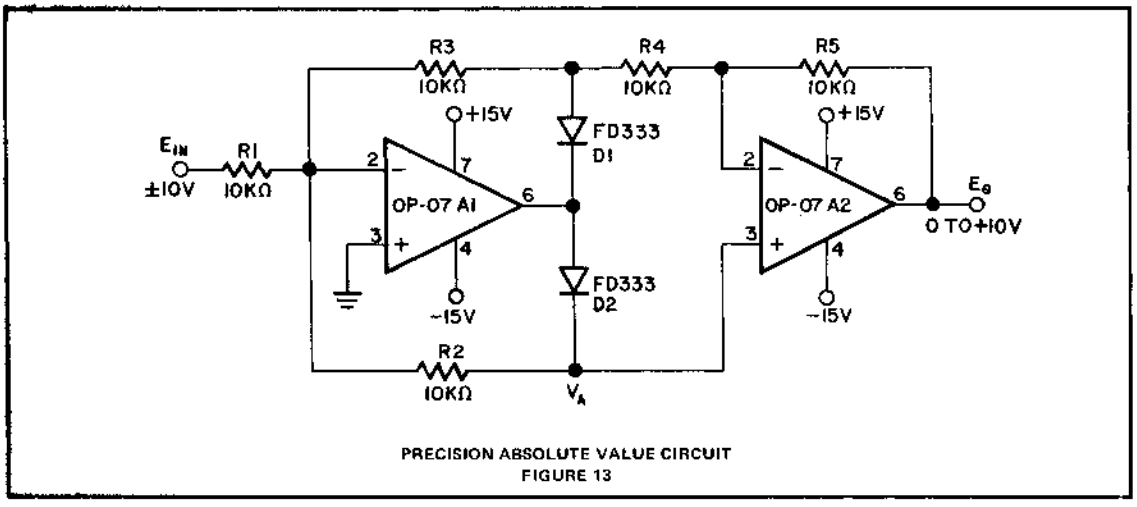
ABSOLUTE VALUE CIRCUIT WITH MINIMUM ERROR

This circuit provides precise full-wave rectification by inverting negative-polarity input voltages and operating as a unity-gain buffer for positive-polarity inputs. It is useful for conditioning inputs to unipolar A to D's, positive peak detectors, single quadrant multipliers, and magnitude-only measurement systems. A polarity indication for sign plus magnitude applications is present at the output of A1.

For a positive input, the circuit operates as two stages of inverting unity-gain amplification. As the input goes positive, the output of A1 becomes negative, turning D2 off and D1 on, clamping the junction of R3 and R4 at $-E_{in}$. V_A is at zero volts because D2 is off and only insignificant A2 bias current flows in R2. A2 operates as a second inverting unity-gain stage and E_o equals E_{in}.

For negative inputs, the first stage gain to point V_A is -2/3 because D2 is on, D1 is off, and 1/3 of the input current, $E_{in}/R1$, flows in R3 and R4. The second stage is operated in a non-inverting gain of 1.5 configuration with V_A as its input, giving an over-all circuit gain of -1.

Using conventional op amps, input offset voltage is usually the predominent error factor because it is doubled and added to E_{in}. For example, with E_{in} of 100mV, only .5mV of V_{os} will cause 1% output error. Clearly, A1 and A2 must be low V_{os} op amps to achieve high accuracy over the full input voltage range. By using a OP-07, performance is mainly a function of resistor ratio matching and diode leakages. Gain errors due to resistor matching will typically be less than .03% when R2-R4 are within .01% of R1's value. Low leakage diodes should be used to prevent errors from reverse current flow in R2 or R3 which would appear as V_{os} error of A2.



PRECISION ABSOLUTE VALUE CIRCUIT
FIGURE 13

PRECISION ABSOLUTE VALUE CIRCUIT

Positive Input

1) $V_A = 0$, D2 off, D1 on

2) $E_O = \left(\frac{-E_{in}R3}{R1}\right) \cdot \left(\frac{-R5}{R4}\right)$

$= E_{in}\frac{R3\,R5}{R1\,R4}$

3) With R1=R3=R4=R5:

$E_O = E_{in}$

4) V_{os} error included:

$E_O = E_{in} + 2V_{os2}$

Negative Input

1) D1 off, D2 on

2) $\frac{-E_{in}}{R1} = \frac{V_A}{R2} + \frac{V_A}{R3+R4}$

3) $E_O = V_A\left(1 + \frac{R5}{R3+R4}\right)$

4) With R3=R4=R5:

$E_O = 1.5V_A$

5) $E_O = -\frac{(R2)(R3+R4)(1.5)E_{in}}{R1(R2+R3+R4)}$

6) With R1=R2=R3=R4:

$E_O = -E_{in}$

7) V_{os} error included:

$E_O = -E_{in} + 1.5V_{os2} - .5V_{os1}$

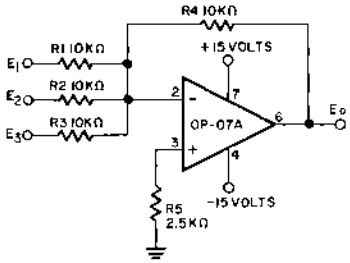
8) For Both Inputs:

$E_O = +|E_{in}|$

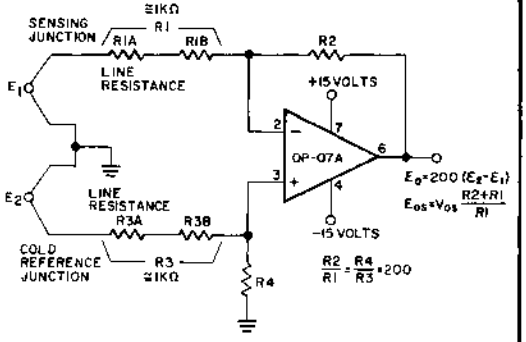
PRECISION SUMMING AMPLIFIER WITH NO ADJUSTMENTS

Figure 14 shows the basic op amp connection for analog computation, a precision summing amplifier. Analog computers use several of these stages connected in combinations to produce continuous outputs that are a function of multiple input variables. Single-stage accuracy is important because errors accumulate throughout a system and determine its over-all performance. Some analog computers require time-consuming and annoying recalibration of each stage at weekly or monthly intervals to compensate for long-term V_{OS} drift. This circuit, with 1μV to 2μV per month maximum change in V_{OS}, completely eliminates periodic calibration while insuring long-term accuracy.

Single-stage maximum full scale errors contributed by the op amp range from .001% for a OP-07A to .004% for a OP-07C. This makes resistor-related errors of ratio matching and temperature tracking the major accuracy considerations. Instrumentation quality operational amplifiers with ultra-low V_{OS} allow simple construction of high performance summing and differencing amplifiers.



ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER
FIGURE 14



HIGH STABILITY THERMOCOUPLE AMPLIFIER
FIGURE 15

INSTRUMENTATION AMPLIFIERS FOR THERMOCOUPLES

Thermocouples are very low voltage output temperature transducers requiring differential DC amplification before linearization and display. Typical full scale outputs are under 50mV with some types having as low as 5μV/°C sensitivity.

These very small input signals often have sizable common mode voltages present because thermocouples are frequently located in high-noise industrial environments. The single op-amp instrumentation amplifier of Figure 15 has the high common mode rejection and long-term accuracy required for this stringent application.

The amplifier achieves about 100dB of common mode voltage rejection over a full ±13 volt range when the ratios of R2/R1 and R4/R3 are matched within .01%. R1B and R3B are usually around 1KΩ, a value large in respect to line resistance but small enough to make voltage drops from input bias currents negligible. Input voltages and V_{OS} are both amplified by 200 so V_{OS} changes, either long-term or due to temperature, can cause direct output error. For example, with a 5μV/°C thermocouple, the OP-07A holds this error factor to .5°C/year and 1°C for an amplifier operating temperature range of 100°C (-25°C to +75°C)—a typical industrial environment. For 0°C to 70°C applications, the low-cost OP-07C holds output error due to a change in V_{OS} below 1°C/year and 2°C over the full commercial operating temperature range.

The circuit is useful whenever small differential signals from low-impedance sources must be accurately amplified in the presence of large common mode voltages.

CONCLUSIONS

The OP-07 Ultra-Low Offset Voltage Operational Amplifier is a cost-effective monolithic alternative to the chopper-stabilized amplifier and is suitable for a wide variety of critical applications. An internal trimming procedure achieves significant improvements over previous bipolar designs in offset voltage, noise levels, and long-term stability at a moderate cost. For the first time, a complete precision IC op amp is available requiring no external components whatsoever for general application, thus increasing reliability by decreasing system complexity. The adjustment-free, fully interchangeable device allows tremendous simplification of calibration and field servicing procedures. This is a most powerful and cost-effective design tool—chopper-type performance and bipolar prices with 741 ease-of-operation.

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(1) Erdi, G. "Minimizing Offset Voltage Drift with Temperature in Monolithic Operational Amplifiers." Proceedings of the National Electronic Conference, Volume 25, 1969.

(2) Erdi, G. "A Low Drift, Low Noise Monolithic Operational Amplifier for Low Level Signal Processing." Fairchild Semiconductor Application Brief #136, July 1969.

Application Notes

AN-14

INTERFACING PRECISION MONOLITHICS DIGITAL–TO–ANALOG CONVERTERS WITH CMOS LOGIC

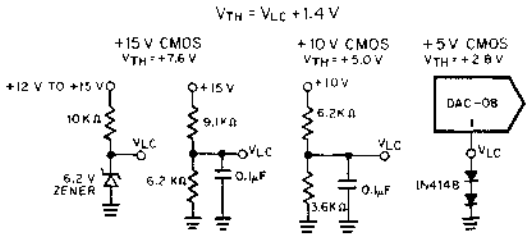
by
Donn Soderquist

The rise in popularity of CMOS logic has created a demand for digital-to-analog converters with CMOS-compatible logic inputs. The low current logic input stages in all Precision Monolithics DAC's allow simple CMOS interfacing in most applications. Since interfacing is easily achieved, the proven advantages of low cost and high speed are available to both TTL and CMOS system designers. This application note discusses interfacing methods and rules for both voltage and current output types and describes several typical CMOS system applications.

INTERFACING THE DAC-08

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} • 1 KΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). It should be noted that pin 1 will source approximately 100μA; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a resistive divider, as in Fig. 1, it should be bypassed to ground by a 0.1μF capacitor.



DAC-08 CMOS INTERFACING WITH TRUE CMOS THRESHOLD

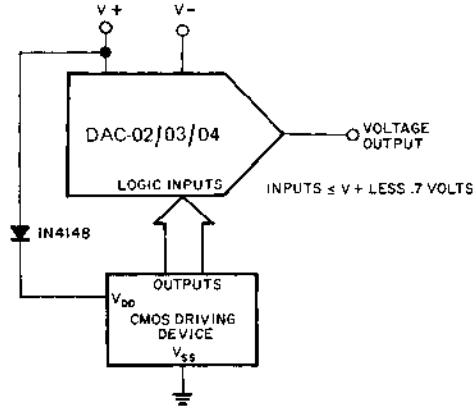
FIGURE 1

INTERFACING THE DAC-02, DAC-03, AND DAC-04

Three complete voltage output monolithic DAC's are described in this section: the DAC-02 and DAC-03, 10-bit plus sign devices, and the DAC-04, a 10-bit two's complement coded converter. These DAC's are well-suited to use in CMOS systems as their complete, internal temperature-compensated references eliminate the external reference voltage requirement, a major source of power dissipation, drift, and cost in some CMOS compatible designs.

These DAC's have logic input stages which require about 1μA and are capable of operation with inputs between -5 volts and V+ less .7 volt. This wide input voltage range allows direct CMOS interfacing in many applications, the exception being where the CMOS logic and D/A converter must use the same power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 2. The diode limits V_{DD} to V+ less .7 volt–since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, these high-speed DAC's require either no interfacing components, or, at most, a single inexpensive diode for full CMOS compatibility.

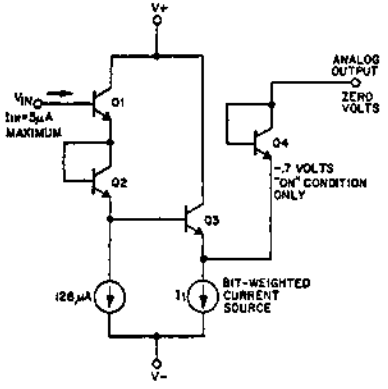


DAC-02/03/04 CMOS INTERFACING

FIGURE 2

INTERFACING THE DAC-100 AND DAC-01

The DAC-100, a complete 10-bit monolithic fast current output DAC is available in a wide range of electrical grades and packages. This device requires only about 1μA of input current into each logic stage. Similar logic input stages are used in the DAC-01, a complete voltage output 6-bit DAC. One rule must be observed when interfacing these DAC's with CMOS inputs: logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.



DAC-100 LOGIC INPUT STAGE
FIGURE 3

DAC100 LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown in Figure 3. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

Switching is accomplished by forward biasing Q4, a diode-connected transistor, for the bit "on" condition and back biasing Q4 in the "off" condition. For the "on" condition ($V_{IN} \leqslant .7$ volts), Q3 is "off"—all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V-. In the "off" condition ($V_{IN} \geqslant 2.1$ volts), Q3 is "on", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

$$(1)\ BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC100 operation with CMOS inputs is easily achieved as demonstrated in the following applications section.

CMOS COMPATIBLE OPERATION OF DAC-100 WITH ±6 VOLT POWER SUPPLIES

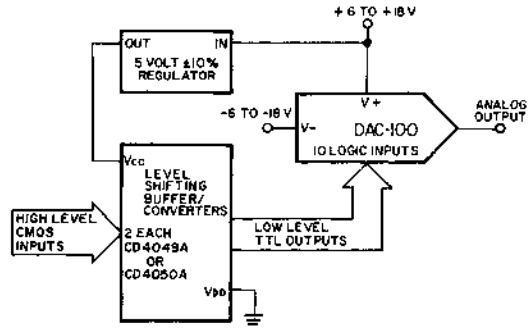
This is the most convenient method of interfacing a DAC-100 with CMOS logic. At ±6 volts, DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

HIGH LEVEL CMOS INTERFACING

The block diagram in Figure 4 illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with a DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts—clearly satisfying the input stage voltage rule.

In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or noninverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100-to-CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive 3-terminal IC regulator can supply several level shifting devices. Next, we will examine a complete circuit using all of these concepts in a high-speed CMOS compatible DAC.

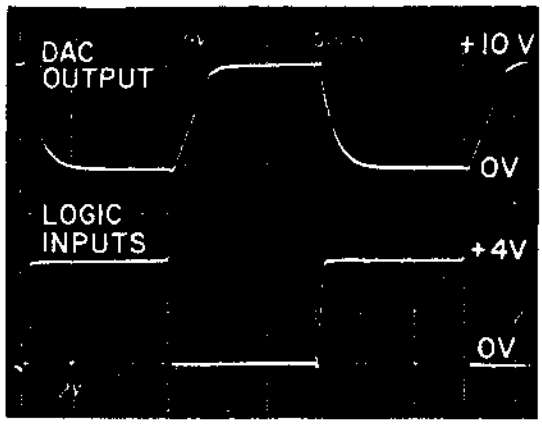


BLOCK DIAGRAM – CMOS TO DAC-100 INTERFACE
FIGURE 4

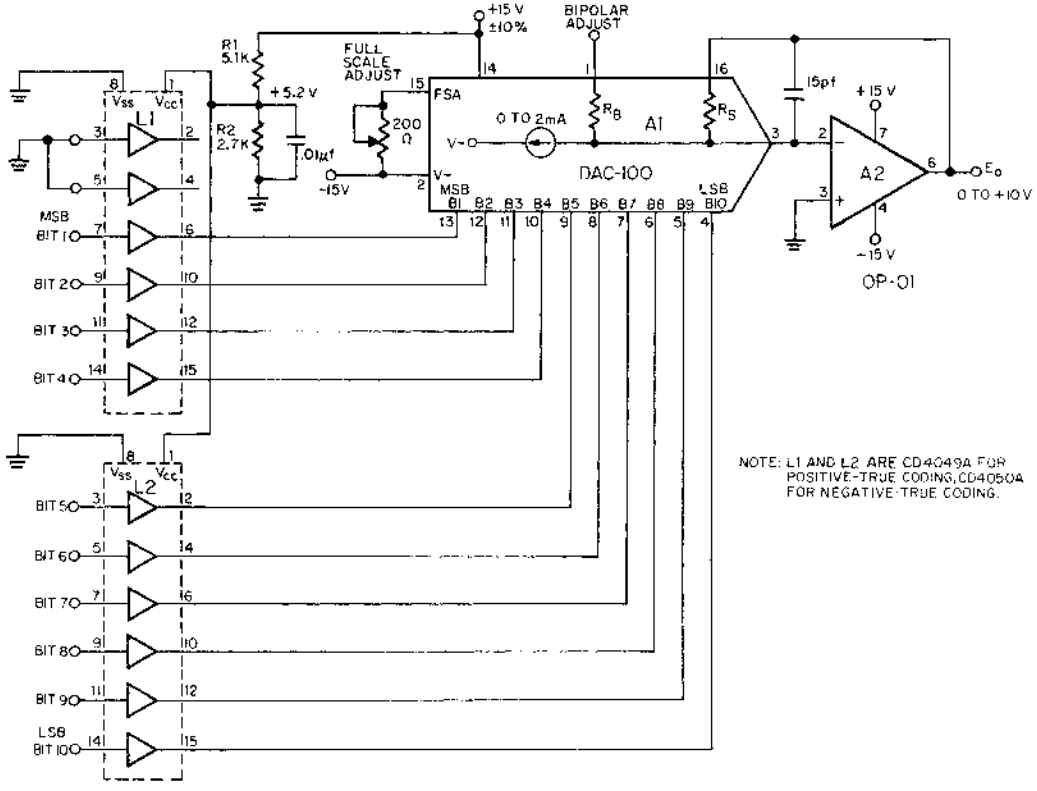
COMPLETE CMOS COMPATIBLE DAC

The complete, 10-bit, voltage output DAC in Figure 5 has CMOS input compatibility, high speed, and low cost. Current output from the DAC-100 is accurately converted to a voltage by the Precision Monolithics OP-01, a high speed op amp which has been specifically designed for the DAC summing amplifier application. Input offset voltage of this op amp is typically 2mV., eliminating the requirement for zero scale adjustment .

The dynamic performance, as shown in the photograph, is quite good. Slew rate is 18V/μsec while settling time to ±.05% of full scale requires less than 1.5μsec. DC performance is also good since DAC-100 nonlinearity is specified over the entire temperature range. In addition, the internal temperature-compensated voltage reference provides minimum full scale drift and decreases overall circuit complexity.

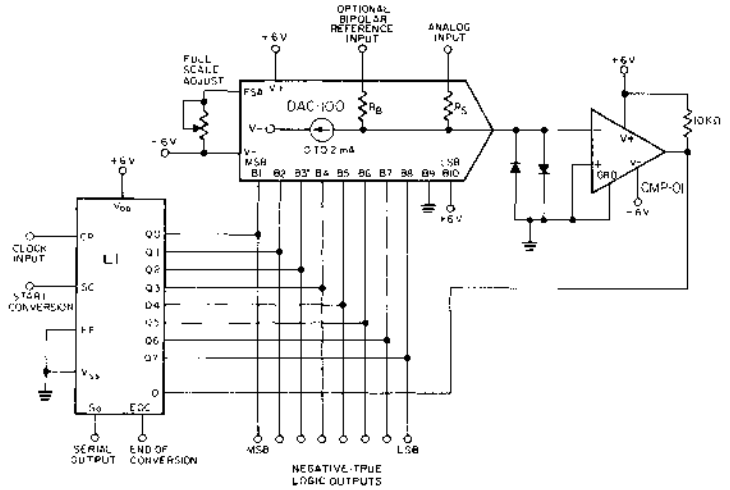


DYNAMIC PERFORMANCE



NOTE: L1 AND L2 ARE CD4049A FOR POSITIVE-TRUE CODING, CD4050A FOR NEGATIVE-TRUE CODING.

INTERFACING DAC-100 WITH ±15 VOLT CMOS SYSTEMS
FIGURE 5



8-BIT CMOS COMPATIBLE THREE IC SUCCESSIVE APPROXIMATION A TO D CONVERTER

FIGURE 6

LOW COST THREE IC CMOS COMPATIBLE A/D CONVERTER

The diagram in Figure 6 is a modification of a previously published application note circuit substituting CMOS logic for TTL. All necessary logic for A to D conversion is contained in L1, a MC14559 CMOS successive approximation register. A conversion sequence is initiated by applying a positive pulse, with a width greater than one clock cycle, to the "Start Conversion" input. The analog input, applied to R_S and converted to a current, is compared successively to 1/2 scale, then 1/4 scale, and the remaining binarily decreasing bit weights until it has been resolved within ±1/2 LSB. At this time, "End of Conversion" changes to a logic "1" and the parallel answer is present in negative-true, binary-coded format at the register outputs.

Tracking A to D's may be similarly constructed using CD4029A up/down counters, a DAC 100, and a CMP-01 fast precision comparator.

CONCLUSION

Precision Monolithics D/A converters may be easily incorporated into CMOS systems. Low current logic input stage designs allow simple interfacing with a minimum of external components. The low power dissipation, high speed output and low cost make this line of monolithic DAC's attractive in CMOS system designs.

Application Notes

AN-15

MINIMIZATION OF NOISE IN OPERATIONAL AMPLIFIER APPLICATIONS

by
Donn Soderquist

INTRODUCTION

Since operational amplifier specifications such as input offset voltage and input bias current have improved tremendously in the past few years, noise is becoming an increasingly important error consideration. To take advantage of today's high performance op amps, an understanding of the noise mechanisms affecting op amps is required. This paper examines noise contributions, both internal and external to an op amp, and provides practical methods for minimizing their effects.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrowband or wideband, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 1, an 11-decade frequency spectrum chart. Some preliminary observations can be made: noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency. Noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

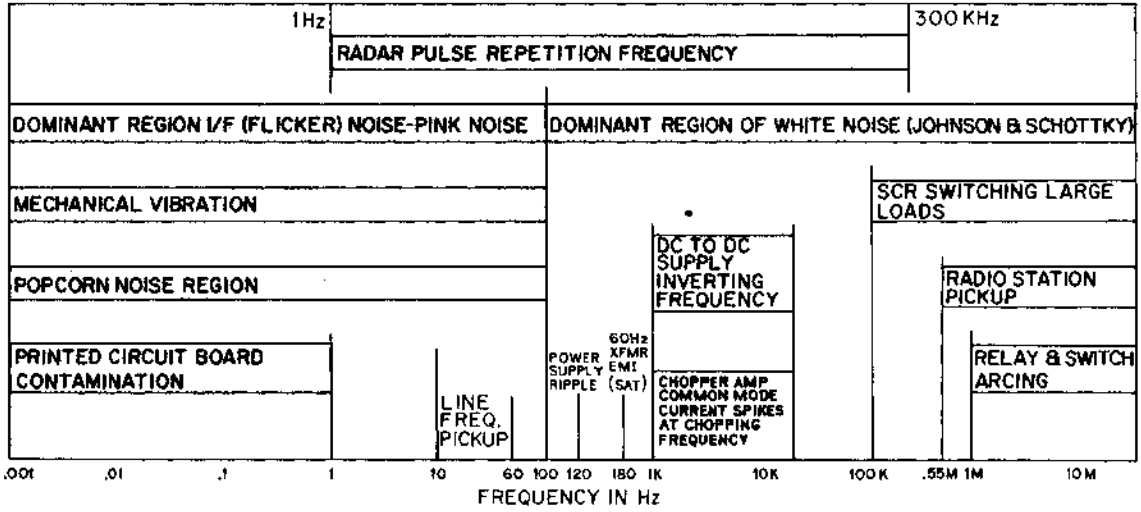


FIGURE 1

FREQUENCY SPECTRUM OF NOISE SOURCES AFFECTING OPERATIONAL AMPLIFIER PERFORMANCE

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be identified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16msec sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, Tektronix® manufactures several preamplifiers with variable bandwidth and frequency which allow quick noise source frequency identification. Another basic identification tool is the simple low pass filter as shown in Figure 2, where the bandpass is calculated by:

$$1) \quad f_O \cong \frac{1}{2\pi RC}$$

With such a filter, measurement bandpass can be changed from 10Hz to 100KHz (C = 4.7μF to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1—the external noise chart.

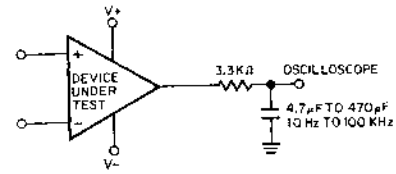


FIGURE 2
NOISE FREQUENCY ANALYSIS RC LOW PASS FILTER

TABLE 1 EXTERNAL NOISE SOURCE CHART

Source	Nature	Causes	Minimization Methods
60Hz Power	Repetitive Interference	Powerlines physically close to op amp inputs. Poor CMRR at 60Hz. Power Transformer primary-to-secondary capacitive coupling.	Reorientation of power wiring. Shielded transformers. Single point grounding. Battery power.
120Hz Ripple	Repetitive	Full wave rectifier ripple on op amp's supply terminals. Inadequate ripple consideration. Poor PSRR at 120Hz.	Thorough design to minimize ripple. RC decoupling at the op amp. Battery power.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio Stations	Standard AM Broadcast Through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay and Switch Arcing	High frequency burst at switching rate	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed Circuit Board Contamination	Random Low Frequency	Dirty boards or sockets.	Thorough cleaning at time of soldering followed by a bakeout and humidity sealant.
Radar Transmitters	High Frequency Gated At Radar Pulse Repetition Rate	Radar transmitters from long range surface search to short range navigational—especially near airports.	Shielding. Output filtering of frequencies >> PRR.
Mechanical Vibration	Random < 100Hz	Loose connections, intermittent metallic contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper Frequency Noise	Common Mode Input Current At Chopping Frequency	Abnormally high noise chopper amplifier in system.	Balanced source resistors. Use bipolar input op amps instead. Use premium low noise chopper.

POWER SUPPLY RIPPLE

Power supply ripple at 120Hz is not usually thought of as a noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply rejection ration (PSRR), the regulator's ripple rejection ratio, and finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 74dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than .5mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to .5V.

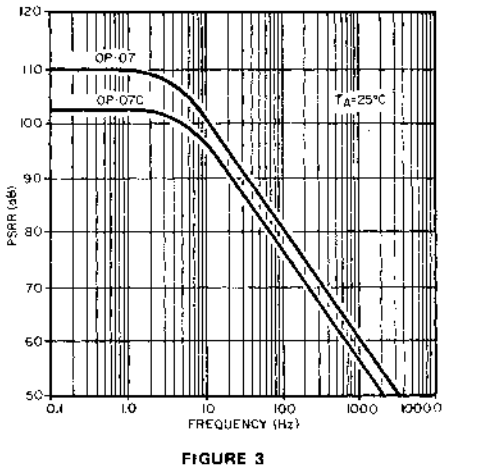


FIGURE 3
PSRR VS FREQUENCY (OP-07, OP-07C)

Externally-compensated low noise op amps can provide improved 120Hz PSRR in high closed-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 4. When compensated for a closed-loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies allowing low ripple-noise operation in exceptionally severe environments.

POWER SUPPLY DECOUPLING

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator outputs typically contain at least 150μV of noise in the 100Hz to 10KHz range; switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 5, will adequately filter most wideband noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage at the op amp's supply pins.

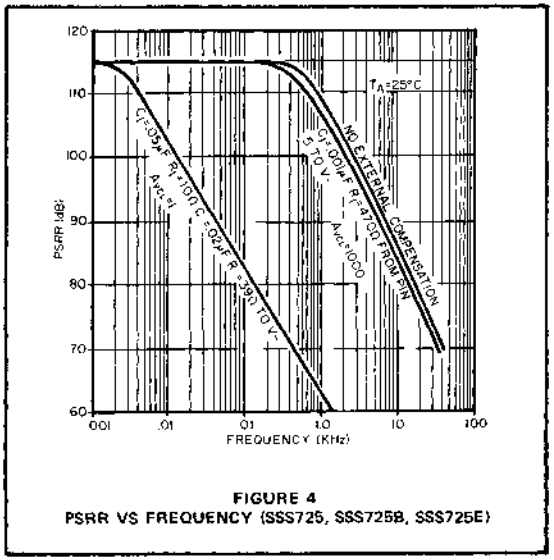


FIGURE 4
PSRR VS FREQUENCY (SSS725, SSS725B, SSS725E)

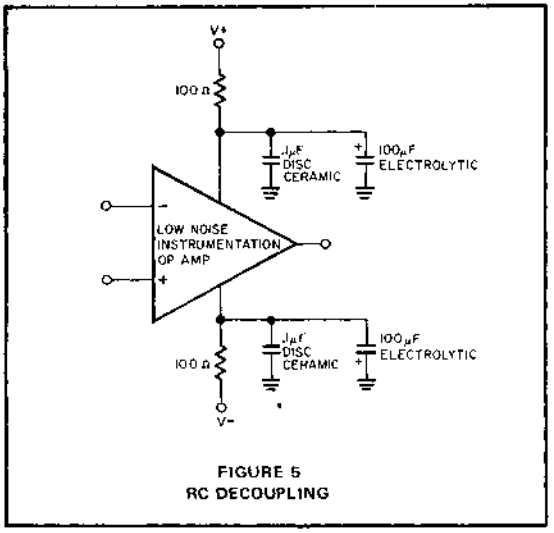


FIGURE 5
RC DECOUPLING

POWER SUPPLY REGULATION

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 110dB (3μV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp and through careful selection and application of the associated components.

OP AMP NOISE SPECIFICATIONS

Most completely specified low noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth and low frequency noise over a range of .1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp-associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

RANDOM NOISE CHARACTERISTICS

Op amp-associated noise currents and voltages are random. They are aperiodic and uncorrelated to each other and have Gaussian amplitude distributions, the highest noise amplitudes having the lowest probability. Gaussian amplitude distribution allows random noises to be expressed as rms quantities; multiplying a Gaussian rms quantity by six results in a peak to peak value that will not be exceeded 99.73% of the time (this is a handy rule-of-thumb for noise calculations).

The two basic types of op amp-associated noises are white noise and flicker noise (1/f). White noise contains equal amounts of power in each Hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each *decade* of bandwidth. This is best illustrated by spectral noise density plots such as in Figures 6 and 7. Above a certain corner frequency, white noise dominates; below that frequency flicker (1/f) noise is dominant. Low noise corner frequencies distinguish low noise op amps from general purpose devices.

SPECTRAL NOISE DENSITY

To utilize Figures 6 and 7, let us consider the definition of spectral noise density: the square root of the rate of change of mean-square noise voltage (or current) with frequency (Eq. 2).

$$2A)\quad e_n^2 = \frac{d}{df}\,(E_n)^2$$

$$2B)\quad i_n^2 = \frac{d}{df}\,(I_n)^2$$

$$3A)\quad E_n = \sqrt{\int_{f_L}^{f_H} e_n^2\, df}$$

$$3B)\quad I_n = \sqrt{\int_{f_L}^{f_H} i_n^2\, df}$$

Where: e_n, i_n = Spectral noise density
E_n, I_n = Total rms noise
f_H = Upper frequency limit
f_L = Lower frequency limit

Conversely, the rms noise value within a given frequency band is the square root of the definite integral of the spectral noise density over that frequency band (Eq. 3). This means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

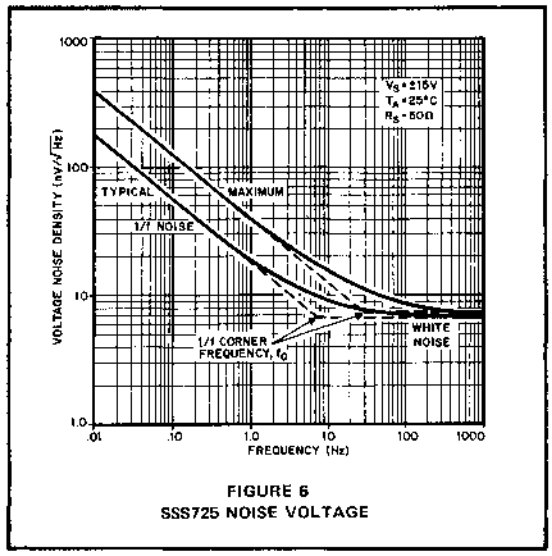


FIGURE 6
SSS725 NOISE VOLTAGE

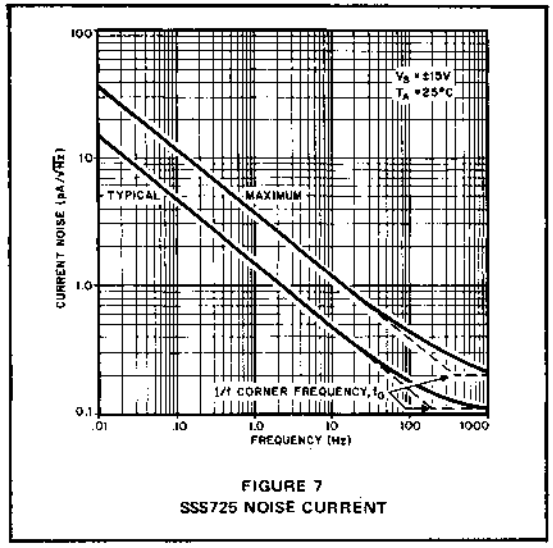


FIGURE 7
SSS725 NOISE CURRENT

WHITE NOISE

White noise sources are defined to have a noise content that is equal in each Hertz of bandwidth, and Eq. 3 may be rewritten for white noise sources as:

$$4)\quad E_n\,(w) = e_n\sqrt{f_H - f_L} \qquad 5)\quad I_n\,(w) = i_n\sqrt{f_H - f_L}$$

It is therefore convenient to express spectral noise density in $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$ where $f_H - f_L = 1$ Hz. When $f_H \geq 10\,f_L$, the white noise expressions may be further reduced to:

$$6)\quad E_n\,(w) = e_n\sqrt{f_H} \qquad 7)\quad I_n\,(w) = i_n\sqrt{f_H}$$

FLICKER NOISE

Since flicker noise content is equal in each decade of bandwidth, total flicker noise may be calculated if noise in one decade is known. The .1 Hz to 1 Hz decade noise content (K) is widely used for this purpose because the white noise contribution below 10 Hz is usually negligible.

8) $E_n(f) \cong K\sqrt{\frac{1}{f}}$ 9) $I_n(f) \cong K\sqrt{\frac{1}{f}}$

When substituted in Eq. 3, the expressions may be rewritten to:

10) $E_n(f) = K\sqrt{\ln\left(\frac{f_H}{f_L}\right)}$ 11) $I_n(f) = K\sqrt{\ln\left(\frac{f_H}{f_L}\right)}$

FLICKER NOISE AND WHITE NOISE

When corner frequencies are known, simplified expressions for total voltage and current noise (E_N and I_N) may be written:

12) $E_N(f_H - f_L) = e_n\sqrt{f_{oe}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$

13) $I_N(f_H - f_L) = i_n\sqrt{f_{ci}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$

Where: e_n = White noise voltage in a 1 Hz bandwidth
i_n = White noise current in a 1 Hz bandwidth
f_{oe} = Voltage noise corner frequency
f_{ci} = Current noise corner frequency
f_H = Upper frequency limit
f_L = Lower frequency limit

The two most important internally generated noise minimization rules are derived from Eq. 12 and 13: limit the circuit bandwidth and use operational amplifiers with low corner frequencies.

NOISE SUMMATION

In the spectral density discussion, the concepts of white noise and flicker noise were introduced. In Figure 8, the complete input-referred op amp noise model, internal white and flicker noise sources are combined into three equivalent input noise generators, E_N, I_{N1} and I_{N2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1}, and E_{t2}. Total rms input-referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage sources over that bandwidth.

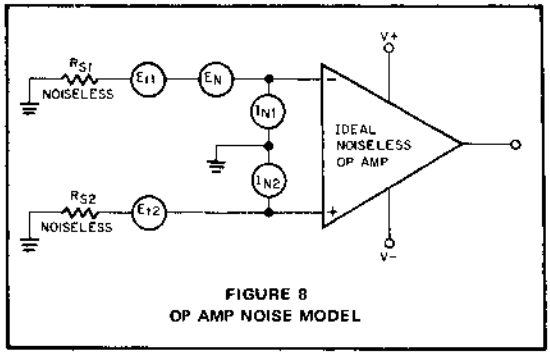


FIGURE 8
OP AMP NOISE MODEL

14) $E_{NT}(f_H - f_L) = \sqrt{E_N^2 + (I_{N1}\cdot R_{S1})^2 + (I_{N2}\cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$

Minimization of total noise requires an understanding of the mechanisms involved in each of the five generators. First, the white noise mechanisms, thermal and shot, are discussed, followed by the low frequency noise mechanisms, flicker and popcorn.

THERMAL NOISE

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits this is the type of noise produced by the source resistances in series with each input. Its rms value over a given bandwidth is calculated by:

15) $E_t = \sqrt{4kTR(f_H - f_L)}$

Where: k = Boltzmann's constant = 1.38×10^{-23} joules/°K
T = Absolute temperature, °Kelvin
R = Resistance in ohms
f_H = Upper frequency limit in Hertz
f_L = Lower frequency limit in Hertz

At room temperature Eq. 15 simplifies to:

16) $E_t = 1.28 \times 10^{-10}\sqrt{R(f_H - f_L)}$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from $r_{bb'}$, the base-spreading resistances in the input stage transistors. These noises are included in E_N, the total equivalent input voltage noise generator.

SHOT NOISE

Shot noise (Schottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons). In Figure 8, I_{N1} and I_{N2}, above the 1/f frequency, are shot noise currents which are related to the amplifier's DC input bias currents:

17) $I_{sh} = \sqrt{2qI_{BIAS}(f_H - f_L)}$

Where: I_{sh} = RMS shot noise value in amps
q = Charge of an electron = 1.59×10^{-19}
I_{BIAS} = Bias current in amps
f_H = Upper frequency limit in Hertz
f_L = Lower frequency limit in Hertz

At room temperature Eq. 17 simplifies to:

18) $I_{sh} = 5.64 \times 10^{-10}\sqrt{I_{BIAS}(f_H - f_L)}$

Shot noise currents also flow in the input stage emitter dynamic resistances (r_e), producing input noise voltages. These voltages, along with the $r_{bb'}$ thermal noise, make up the white noise portion of E_N, the total equivalent input noise voltage generator.

FLICKER NOISE

In limited bandwidth applications, flicker (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltage noise. Eq. 19 illustrates this relationship:

$$19) \quad \frac{i_{n\ \text{second stage}}}{g_{m\ \text{first stage}}} = e_{n\ \text{input}}$$

Another critical factor is corner frequency. For minimum noise the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 9, low noise corner frequencies distinguish low noise op amps from ordinary industry-standard 741 types.

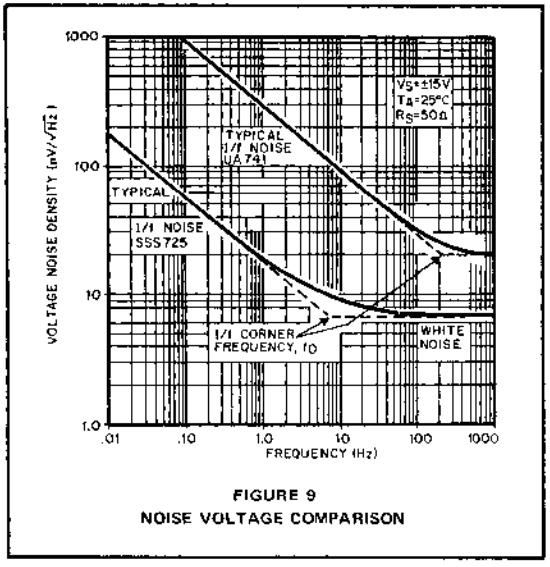


FIGURE 9
NOISE VOLTAGE COMPARISON

The photograph in Figure 10, taken using the test circuit of Figure 11, illustrates the flicker noise performance of the OP-07. This device demonstrates proper attention to low noise circuit design and wafer processing and achieves a remarkable 0.35μV peak to peak input voltage noise in the 0.1 Hz to 10 Hz bandwidth.

POPCORN NOISE

Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100 Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Precision Monolithics minimizes this problem through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation."

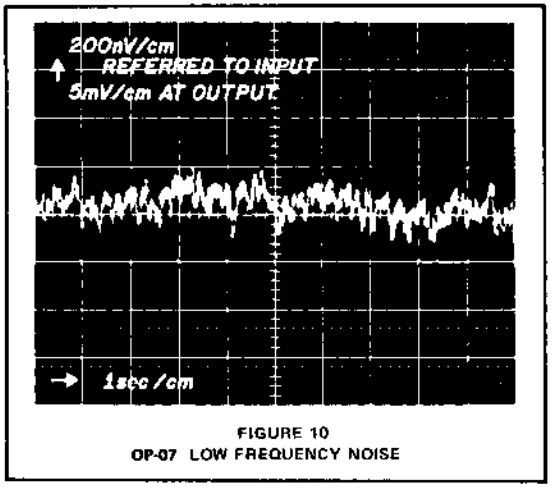


FIGURE 10
OP-07 LOW FREQUENCY NOISE

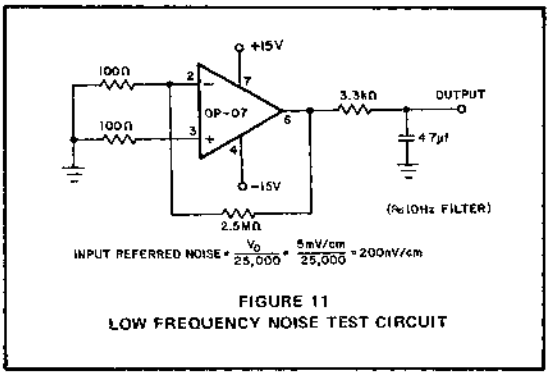


FIGURE 11
LOW FREQUENCY NOISE TEST CIRCUIT

To begin the process, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third step is the thick glass overcoat which leaves only the bonding pads exposed. A cutaway view of a finished device is shown in Figure 12.

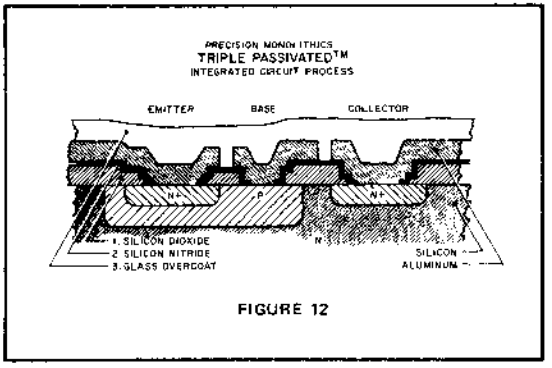


FIGURE 12

Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be eliminated from almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay. At Precision Monolithics the low noise process alternative is used to manufacture high volumes of cost-effective low noise op amps.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated for a given application. To illustrate the method, noise information from the Precision Monolithics OP-07 data sheet is reproduced in Figure 13. The first step is to determine the current and voltage noise corner frequencies so that the E_N and I_N terms of Eq. 14 may be calculated using Eq. 12 and 13.

CORNER FREQUENCY DETERMINATION

In the input spot noise versus frequency curves of Figure 13, it may be seen that voltage noise (R_s = 0) begins to rise at about 10Hz. Lines projected from the horizontal (white noise) portion and sloped (flicker noise) portion intersect at 6 Hz, the voltage noise corner frequency (f_{ce}). In the center curve, excluding thermal noise from the source resistance, current noise multiplied by 200KΩ is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 60Hz, the current noise corner frequency (f_{ci}). Eq. 12 and 13 also require e_n and i_n for calculation of E_N and I_N. To find e_n and i_n, use the data sheet specification a decade or more above the respective corner frequencies; in this case e_n is $9.6nV/\sqrt{Hz}$ (1000Hz), and i_n is $0.12pA/\sqrt{Hz}$ (1000 Hz).

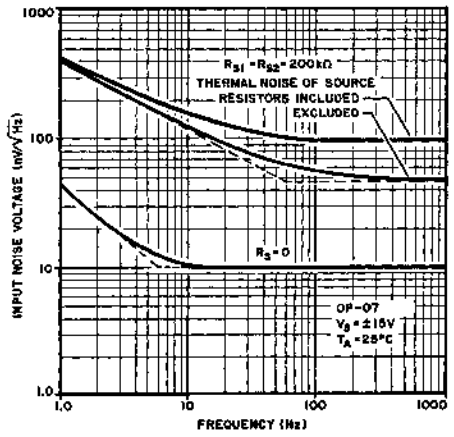


FIGURE 13A
INPUT SPOT NOISE VOLTAGE VS FREQUENCY

ELECTRICAL CHARACTERISTICS			OP-07A			OP-07			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		f_o = 100Hz	—	10.0	13.0	—	10.0	13.0	
		f_o = 1000Hz	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		fo = 100Hz	—	0.14	0.23	—	0.14	0.23	
		fo = 1000Hz	—	0.12	0.17	—	0.12	0.17	
Input Offset Voltage	V_{os}		—	10	25	—	30	75	µV
Long Term Input Offset Voltage Stability	V_{os}/Time		—	0.2	1.0	—	0.2	1.0	µV/Mo
Input Offset Current	I_{os}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±7	±20	—	±10	±30	nA

INPUT NOISE VOLTAGE (e_{np-p})
The peak to peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage in a 1Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak to peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1Hz band surrounding a specified value of frequency.

FIGURE 13B

BANDWIDTH OF INTEREST

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, $f_H - f_L$. At this time, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies and bandwidth are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

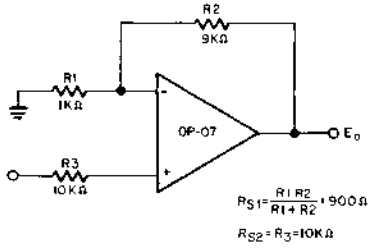


FIGURE 14A
NOISE ANALYSIS CIRCUIT

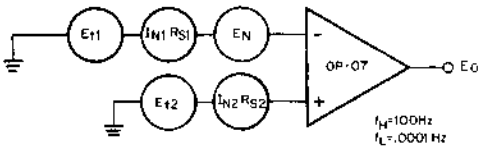


FIGURE 14B
NOISE ANALYSIS EQUIVALENT CIRCUIT

TYPICAL APPLICATION EXAMPLE

Figure 14A shows a typical X10 gain stage with a 10KΩ source resistance. In Figure 14B, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

Using Eq. 16: $E_t = \sqrt{R\,(f_H - f_L)}$

$E_{t1} = 1.28 \times 10^{-10}\sqrt{(900\Omega)(100\,Hz)} = .04\mu Vrms$

$E_{t2} = 1.28 \times 10^{-10}\sqrt{(10K\Omega)(100\,Hz)} = .128\mu Vrms$

Next, calculate I_N using Eq. 13:

$$I_N = i_n\sqrt{f_{ci}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= .12pA\sqrt{60\ln\frac{100\,Hz}{.0001\,Hz} + 100 - .0001}$$

$$= 3.66pArms$$

and:

$I_{N1}\cdot R_{S1} = 3.66pA\,(900\Omega) = .0033\mu Vrms$

$I_{N2}\cdot R_{S2} = 3.66pA\,(10K\Omega) = .0366\mu Vrms$

Finally, E_N from Eq. 12:

$$E_N = e_n\sqrt{f_{ce}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 9.6nV\sqrt{6\ln\frac{100\,Hz}{.0001\,Hz} + 100 - .0001}$$

$$= .130\mu Vrms$$

Substituting in Eq. 14:

$$14)E_{NT}(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + I_{N2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(.130\mu V)^2 + (.0033\mu V)^2 + (.0366\mu V)^2 + (.04\mu V)^2 + (.128\mu V)^2}$$

$$= 0.19\mu Vrms$$

Total input-referred noise = 1.14μV peak to peak (.0001 Hz to 100 Hz).

741 CALCULATION EXAMPLE

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 14 is useful. Once again the starting point is corner frequency determination, using the data sheet curves of Figure 15: f_{ce} = 200Hz; f_{ci} = 2KHz; $e_n \cong 20nV/\sqrt{Hz}$; $i_n = .5pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_N and I_N are calculated to be 1μVrms and 83pArms respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Eq. 14 as shown below:

$$14) E_{NT}(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + I_{N2}^2 R_{S2}^2 + E_{+1}^2 + E_{+2}^2}$$

Substituting in Eq. 14:

$$= \sqrt{(1\mu V)^2 + (.075\mu V)^2 + (.83\mu V)^2 + (.04\mu V)^2 + (.128\mu V)^2}$$

$$= 1.3\mu Vrms$$

Total input-referred noise = 7.8μV peak to peak (.0001Hz to 100Hz).

This is 6.8 times that of the low noise op amp example.

The calculation examples illustrate three rules for minimizing noise in operational amplifier applications:

RULE 1. Use an op amp with low corner frequencies.

RULE 2. Keep source resistances as low as possible.

RULE 3. Limit circuit bandwidth to signal bandwidth.

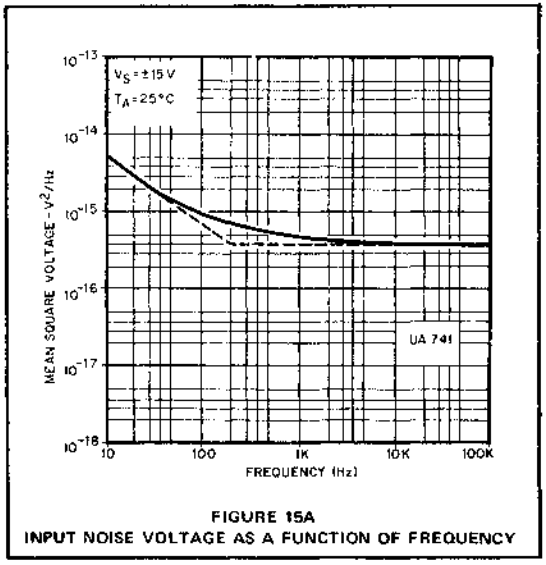


FIGURE 15A
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

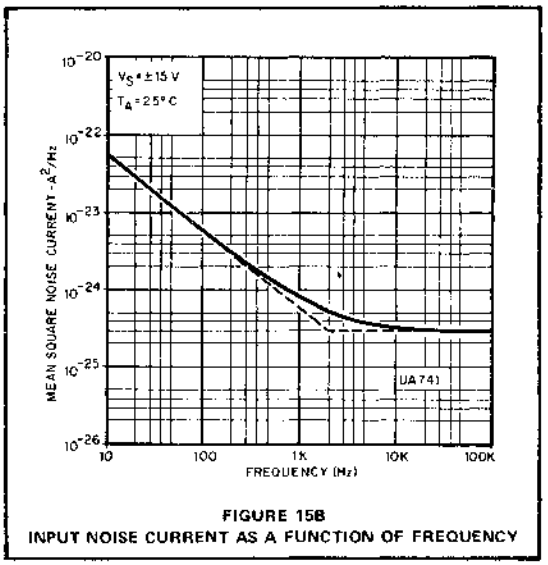


FIGURE 15B
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

BANDWIDTH

Effective circuit bandwidth must not be much greater than signal bandwidth or amplification of undesirable high frequency noise components will occur. Throughout the preceding calculations, an assumption of "bandwidth-of-interest" was made, while in actual application the amplifier's bandwidth must be considered.

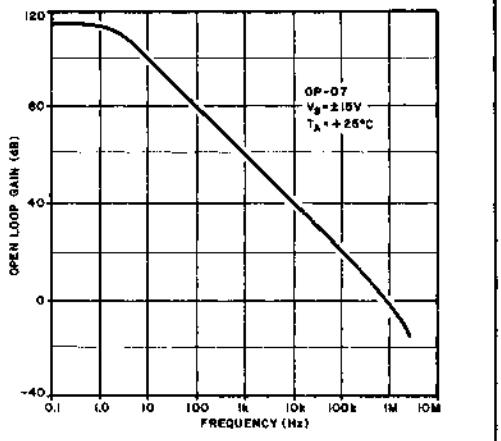


FIGURE 16A
OPEN LOOP FREQUENCY RESPONSE

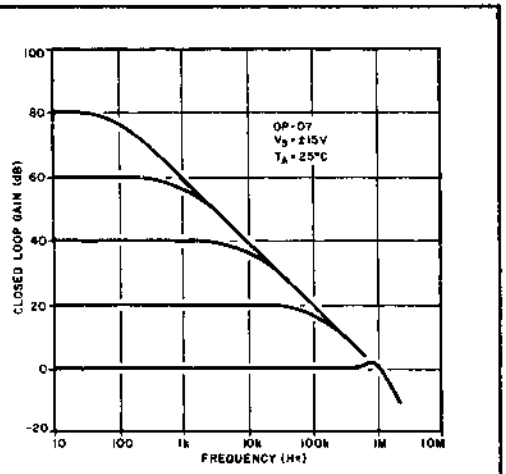


FIGURE 16B
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

In Figure 16, the OP-07 frequency response curves show a rolloff of 20dB/decade; integration of the area under the curve will show the effective circuit noise bandwidth to be 1.57 times the 3dB bandwidth. In most closed-loop gain configurations, the amplifier's bandwidth may be greater than required, and output filtering, such as in Figure 17, could be used. As an alternate to output filtering, an integrating capacitor may be connected across the feedback resistor. Bandwidth may also be limited in some applications by overcompensating an externally-compensated low noise op amp, such as the SSS725.

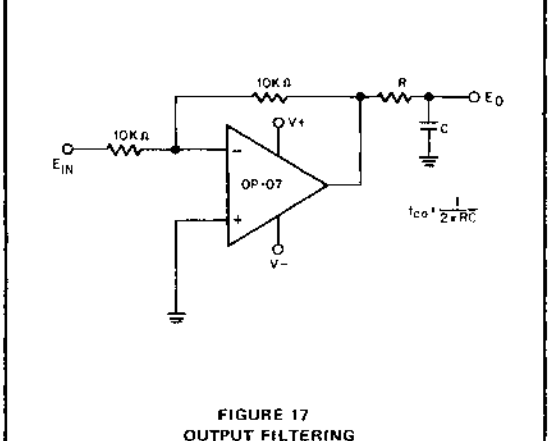


FIGURE 17
OUTPUT FILTERING

MISCELLANEOUS NOISE MINIMIZATION METHODS

Certain other noise mechanisms merit consideration: Use metal film resistors; carbon resistors exhibit "excess noise," with both 1/f and white noise content being related to DC applied voltage. The use of balanced source resistors, while sometimes good for DC error purposes, will increase noise; the balancing resistor is not required for op amps such as the OP-07, since $I_{OS} \approx I_B$. Keep noise in its proper perspective; minimize it without introducing additional DC errors. Use low noise op amps with overall DC specifications that will satisfy the application.

SUMMARY

A summary of the major points to consider is as follows:

1) Minimize externally generated noise.
2) Choose an amplifier with low 1/f noise corner frequencies.
3) Limit the circuit bandwidth to signal bandwidth.
4) Eliminate excessive resistance in the input circuit.

CONCLUSION

Recent improvements in IC op amp DC specifications have made noise an important error consideration. From data sheet information and source resistance values, total input-referred noise over a given bandwidth can be easily calculated. Total noise can be minimized by a thorough understanding of the various noise-generation mechanisms.

Application Notes

AN-16

LOW COST, HIGH SPEED ANALOG-TO-DIGITAL CONVERSION WITH THE DAC-08

by
Donn Soderquist & John Schoeff

Today's fast computer and microprocessor-controlled systems frequently require A/D converters which will complete a conversion in one cycle time.

Until now, these high speed A/D converters have been expensive and difficult to build. Most designers have therefore chosen to purchase modular A/D converters typically ranging in price from $100 to $400. This application note describes three less costly A/D designs, with total conversion times of 4μsec, 2μsec, and 1μsec. These designs are implemented with the DAC-08, a recently announced high speed monolithic Digital-to-Analog converter. A discussion of basic successive approximation is given, followed by practical circuit designs.

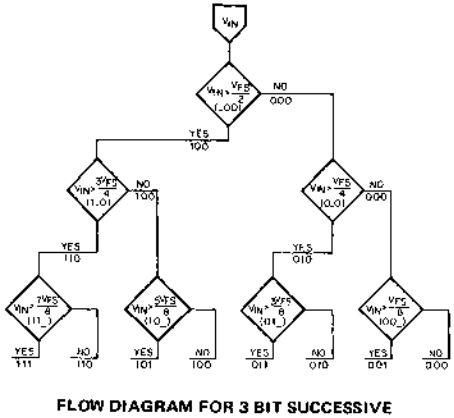
SUCCESSIVE APPROXIMATION A/D ADVANTAGES

Successive approximation A/D conversion is the most popular choice in many systems today because it achieves high conversion rates at very low cost. Other methods, such as Tracking (Servo) or Staircase (Ramp), require up to "2^n" clock cycles per conversion, where "n" is the number of bits of resolution, while successive approximation requires only "n+1" clock cycles. Finally, a designer can easily construct his A/D with readily available standard IC's.

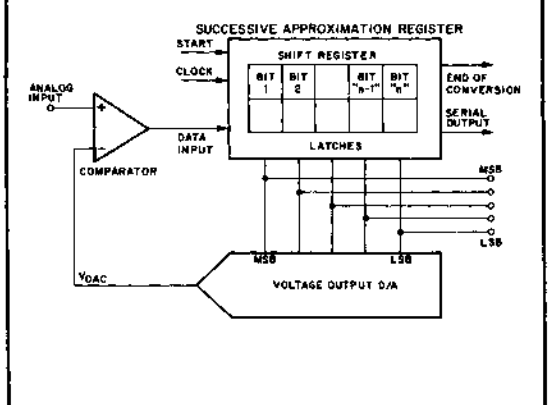
BASIC SUCCESSIVE APPROXIMATION A/D CONVERSION

A successive approximation A/D converter operates by comparing the analog input to a series of "trial" conversions; the first trial compares the input to the value of the most significant bit (MSB) or approximately half of full scale. Fig. 1 shows the progression of trials for a 3-bit converter. If the input is greater than the MSB value, the MSB is retained and the converter moves on to "trying" the next most significant bit, or approximately three-quarters full scale. If the input had been less than the MSB, the logic would have turned the MSB off before going on to the next most significant bit, or one-quarter full scale. This "branching" continues until each successively smaller bit has been tried, with the entire process taking "n" trials.

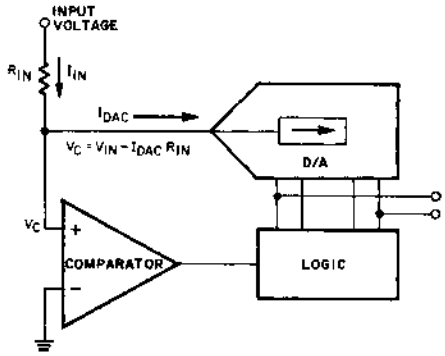
To implement the logic for the successive approximation algorithm, a configuration similar to Fig. 2 may be employed, wherein a start command places a "one" in the first bit of a shift register. This sets the first latch to "one" and turns on the DAC's MSB. If the comparator output remains low, the "one" will remain in the latch; if not, the latch will be reset to zero before the next bit trial begins. The next clock cycle causes the shift register to place a "one" in the second bit, and a similar process continues till all bits have been tried. After the last bit's trial, the end-of-conversion output changes state indicating the parallel data is ready to be used.



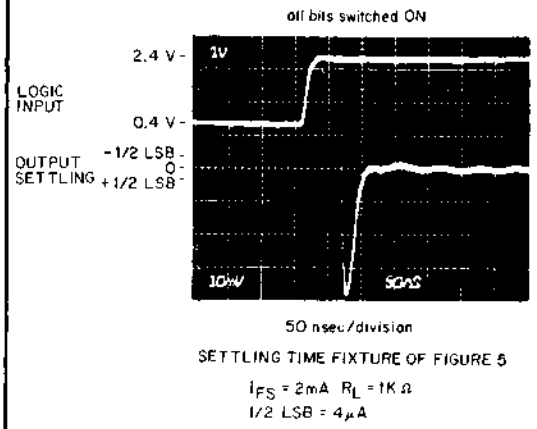
FLOW DIAGRAM FOR 3 BIT SUCCESSIVE APPROXIMATION A/D CONVERSION
FIGURE 1



SUCCESSIVE APPROXIMATION A/D CONVERTER
FIGURE 2



CURRENT COMPARISON A/D INPUT
FIGURE 3



50 nsec/division

SETTLING TIME FIXTURE OF FIGURE 5

I_{FS} = 2mA R_L = 1KΩ
1/2 LSB = 4μA

OUTPUT SETTLING TIME
FIGURE 4

CURRENT COMPARISON

The previous discussion indicated that the function of the comparator was to perform a comparison between the analog input voltage and the output voltage of the DAC. Higher speed conversions may be achieved by using the output of a fast current output DAC directly. This may be implemented as shown in Fig. 3, where the comparator examines the polarity of $(V_{IN} - I_{DAC}R_{IN})$. Current comparison eliminates the need for a current-to-voltage converting op amp which is by far the slowest element in most D/A converters.

DYNAMIC CONSIDERATIONS

The time required to complete an 8 bit successive approximation A/D conversion is determined by the length of 8 trials and their associated comparator decisions, plus one clock cycle. To minimize these periods, three dynamic considerations must be made:

1. DAC output current settling time to ±1/2LSB.
2. Comparator propagation delay with the available overdrive.
3. Logic propagation delay and setup time requirements.

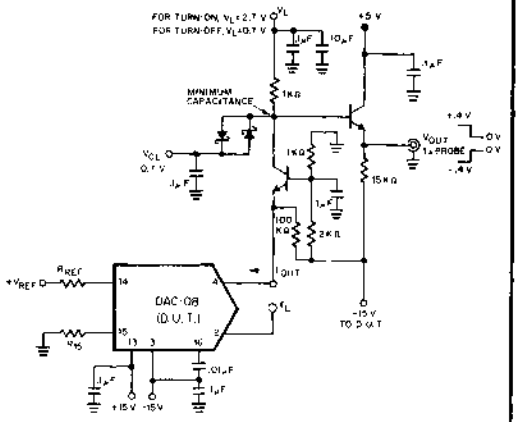
For example, with a 500nsec DAC, a 500nsec comparator, and 100nsec of logic delay, each of these cycles would require 1.1μsec. An 8 bit conversion would take 9 clock periods, or 10μsec. To design a fast A/D, each of these delays must be made as short as possible. In the next few paragraphs, practical methods of minimizing these delays are discussed.

DAC CURRENT SETTLING TIME

The DAC-08 is a low cost monolithic current output DAC with 85nsec full scale settling time and is ideal for use in high speed A/D converter designs. The internal logic switch design enables propagation delays of 35nsec for each of the 8 bits. Settling time of the LSB to within ±1/2LSB of final value is therefore 35nsec, with each successively more significant bit taking progressively longer. The MSB settles in 85nsec; it is the dominant factor of full scale settling time. This performance is illustrated in the scope photo of Fig. 4, taken at the output of the test circuit of Fig. 5.

A major factor affecting settling time is the RC time constant formed by the load resistance (R_L) and the DAC output capacitance (C_O) plus any stray capacitance present at the summing node. Settling to within ±1/2LSB at 8 bits (±.2% full scale) requires 6.2 RC time constants. For the DAC-08, the output capacitance is 15pF; as a result the output RC time constant is a major factor influencing settling time when R_L is greater than 500Ω and dominates when R_L exceeds 900Ω.

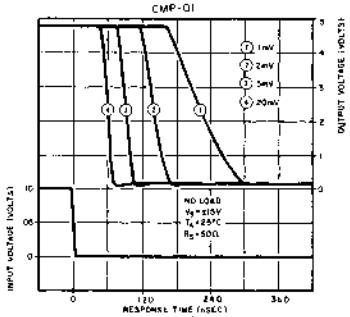
This situation produces difficult requirements. Optimum DAC settling time occurs when $R_L \leq 500\Omega$, but for full scale currents of 2mA, 1/2LSB is only 4μA. Thus, with a 500Ω equivalent resistance, the voltage at the DAC output corresponding to 1/2LSB is only 2mV and is inadequate for high speed operation of many comparators. For this reason, R_L is usually larger than 500Ω, which is a necessary compromise between DAC settling time and comparator input overdrive requirements.



SETTLING TIME MEASUREMENT
FIGURE 5

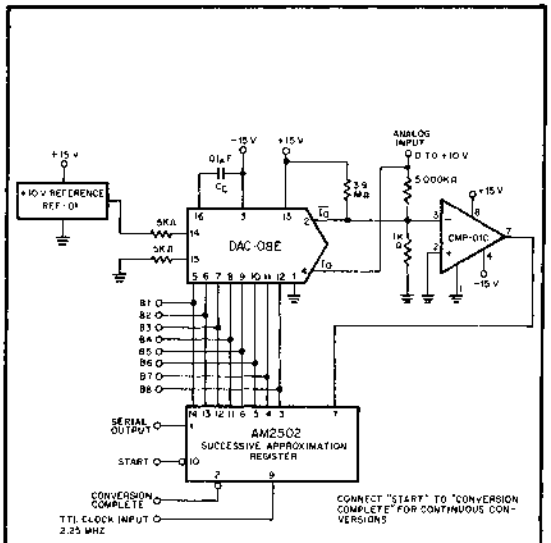
COMPARATOR CONSIDERATIONS

All comparators respond fastest to large differential input voltages (high overdrive). This phenomenon is shown in Fig. 6, a graph of response time vs. input voltage for the Precision Monolithics' CMP-01. This low cost comparator provides DC characteristics compatible with 10 and 12 bit A/D converters and has adequate speed for 4μsec 8 bit converters.



RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES
FIGURE 6

For 2μsec and 1μsec designs, the AM686 was selected. It provides 12nsec propagation delay with 2.5mV overdrive, Schottky TTL outputs, and DC input specifications adequate for an 8 bit A/D. Ultra-high speed requires considerable power. Maximum supply currents are 42mA from the +5V supply and 34mA from the −5V supply.



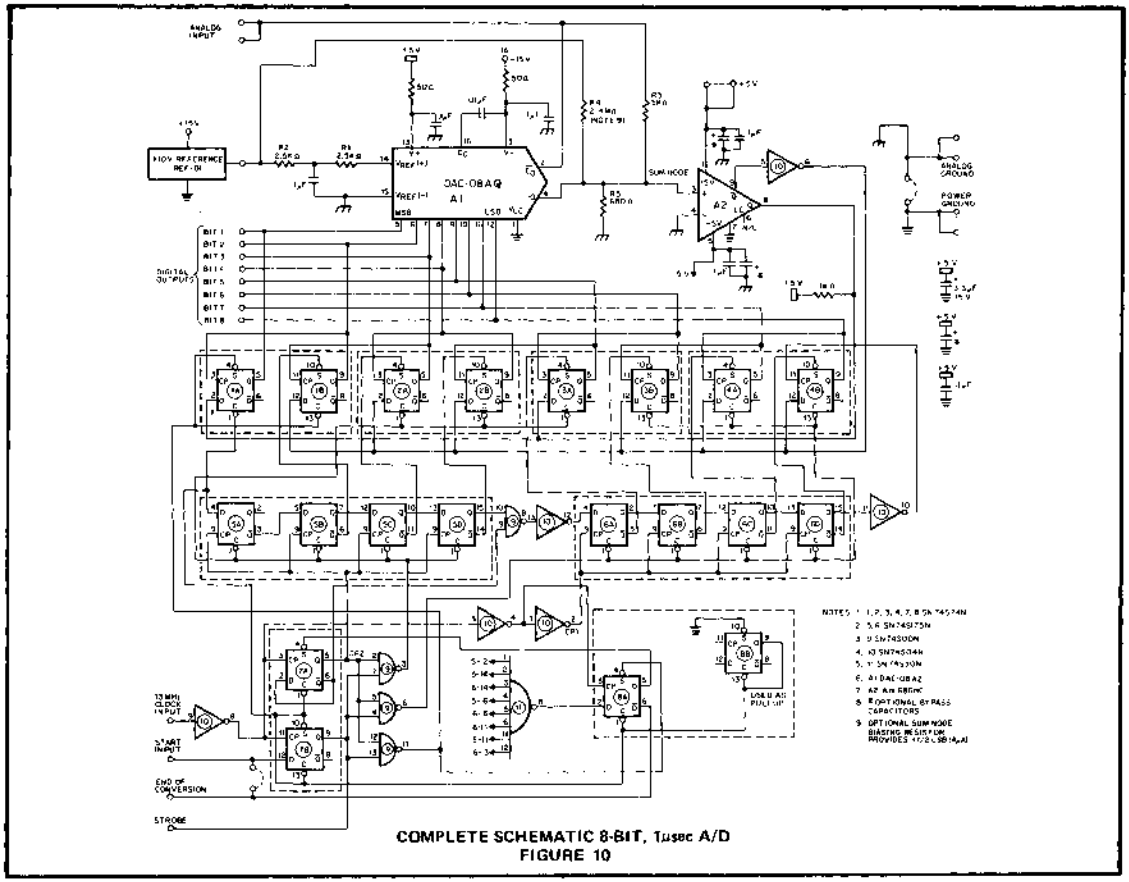
3 IC LOW COST A/D CONVERTER
FIGURE 7

LOGIC CONSIDERATIONS

A single DIP package, the AM2502 Successive Approximation Register, contains the logic for 8 bit A/D converters operating at 2μsec or greater conversion times. (Detailed descriptions of A/D's constructed with the AM2502 and Precision Monolithics DAC's are contained in AN-11, available upon request.) A 1μsec A/D requires special logic design using Schottky TTL and will be described in the detailed circuit description.

PRACTICAL 3 IC A/D'S

When the required conversion time is ≥ 2μsec, the DAC-08's fast settling time enables very simple and low cost designs. A 4μsec design is shown in Fig. 7. At additional cost and increased power dissipation, changing the comparator to an AM686 results in a 2μsec A/D. Every nanosecond counts in a 1μsec A/D, and the circuit necessarily increases in complexity. However, with the DAC-08, Schottky TTL logic, and attention to layout, a 1μsec A/D can be constructed at low cost.



COMPLETE SCHEMATIC 8-BIT, 1μsec A/D
FIGURE 10

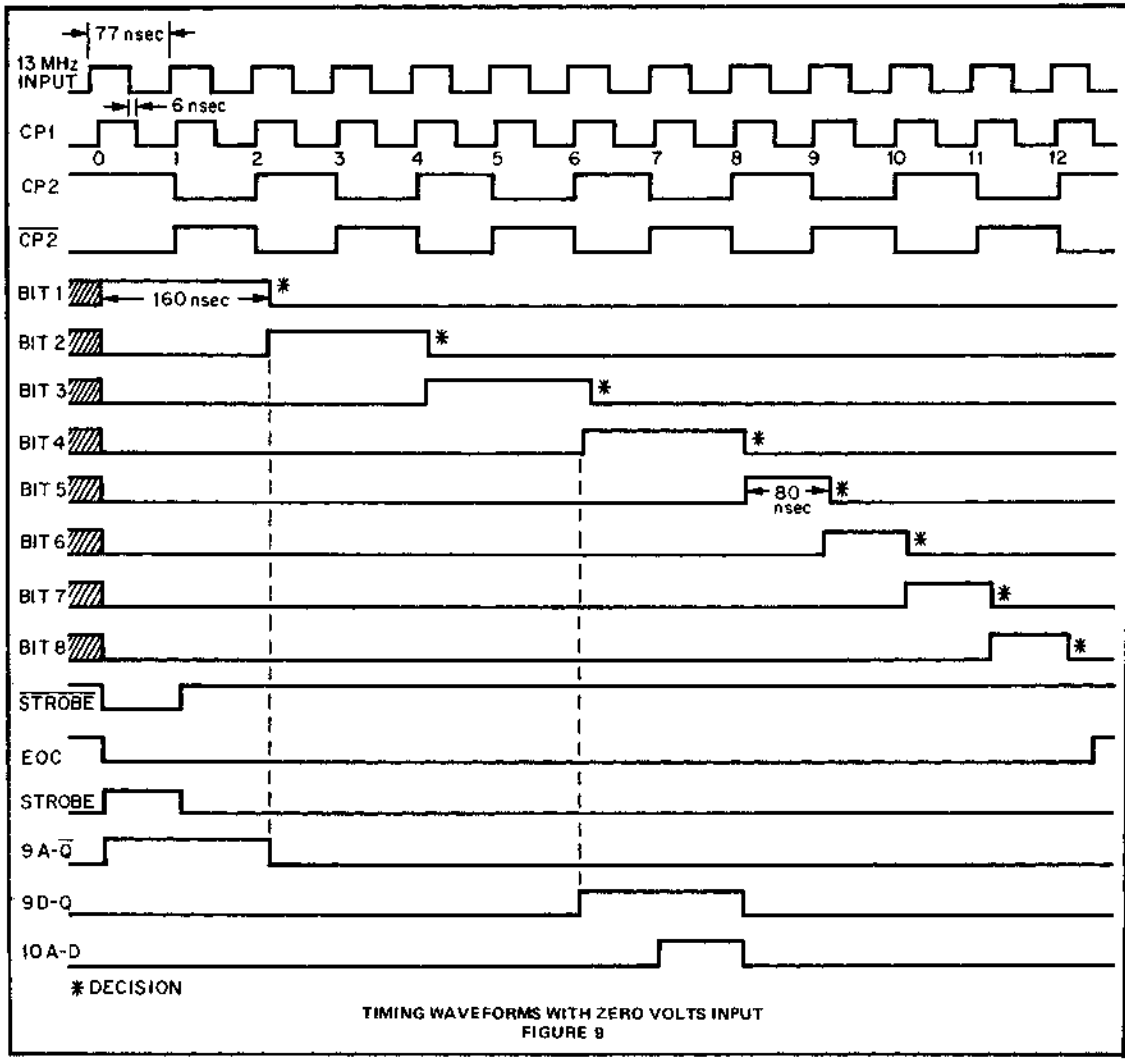
ANALOG DESIGN

The DAC-08 AQ is useful in this design for several reasons. Its output full scale current is guaranteed to be 1.992mA ±8μA, when a 10.000V reference is connected to a 5.000KΩ resistor in series with pin 14. In this design, the 5KΩ is split to allow bypassing without capacitively loading the 10 volt source. For slightly higher speed, the total resistance may be reduced to 2.5KΩ, thereby increasing I_O full scale to 3.984mA, allowing a lower sum node resistance and lower RC time constant. (The DAC itself does not settle faster at 4mA full scale current.) The DAC-08A maximum nonlinearity of ±0.1% full scale enables faster settling time to within ±1/2LSB (±0.2% full scale) for each bit trial than would be the case using a DAC with ±0.2% nonlinearity. Using the ±0.2% nonlinearity DAC-08 or DAC-08E provides cost savings at an overall increase in conversion time. Both true and complementary current outputs are provided, and their summation is always $I_{full\ scale}$. In this design, $\overline{I_O}$ is connected to the analog input. Since $I_O + \overline{I_O}$ is constant, and I_O flows in R3, the DC input current is constant. Holding the A/D input current constant reduces buffer amplifier output impedance requirements. The buffer amplifier used in this application must have sufficient bandwidth to hold V_{IN} constant during a 1μsec A/D conversion.

CALIBRATION AND ACCURACY

In many applications calibration is not required. With a 10.000V reference and ±0.05% tolerance resistors, the worst case full scale error is ±0.15%. The zero scale error is totally dependent upon comparator input offset voltage and input bias current, and, in most cases, it may be tolerated. If the errors are not tolerable, then the following calibration procedure may be used.

Calibration of the A/D is done first at zero scale, then at full scale. The zero transition is set by R4, a resistor connected to the +10 volt reference. For 10V full scale, the desired transition point between a code of 0000 0000 and 0000 0001 is at +20mV (+1/2LSB). With an ideal comparator, R4 would be 2.56MΩ (10 volts/3.9μA). Since comparators are less than ideal, R4 must also cancel out the comparator's input offset errors. With +20mV applied at the analog input and using a low clock rate, select R4 to cause the output code to fluctuate between 0000 0000 and 0000 0001. (Do not install a pot for R2 or R4 since it will increase capacitance and inductance at the sum node.) Full scale is calibrated by applying +9.940V to the analog input and trimming R2 until the output code fluctuates between 1111 1110 and 1111 1111. Alternatively, the reference voltage source may be adjusted for the same effect. This will be a small adjustment due to the DAC-08A's tight output full scale current relationship with the reference voltage. Once calibrated, accuracy is a function of temperature-induced drifts only.



TIMING WAVEFORMS WITH ZERO VOLTS INPUT
FIGURE 9

A TYPICAL CONVERSION CYCLE

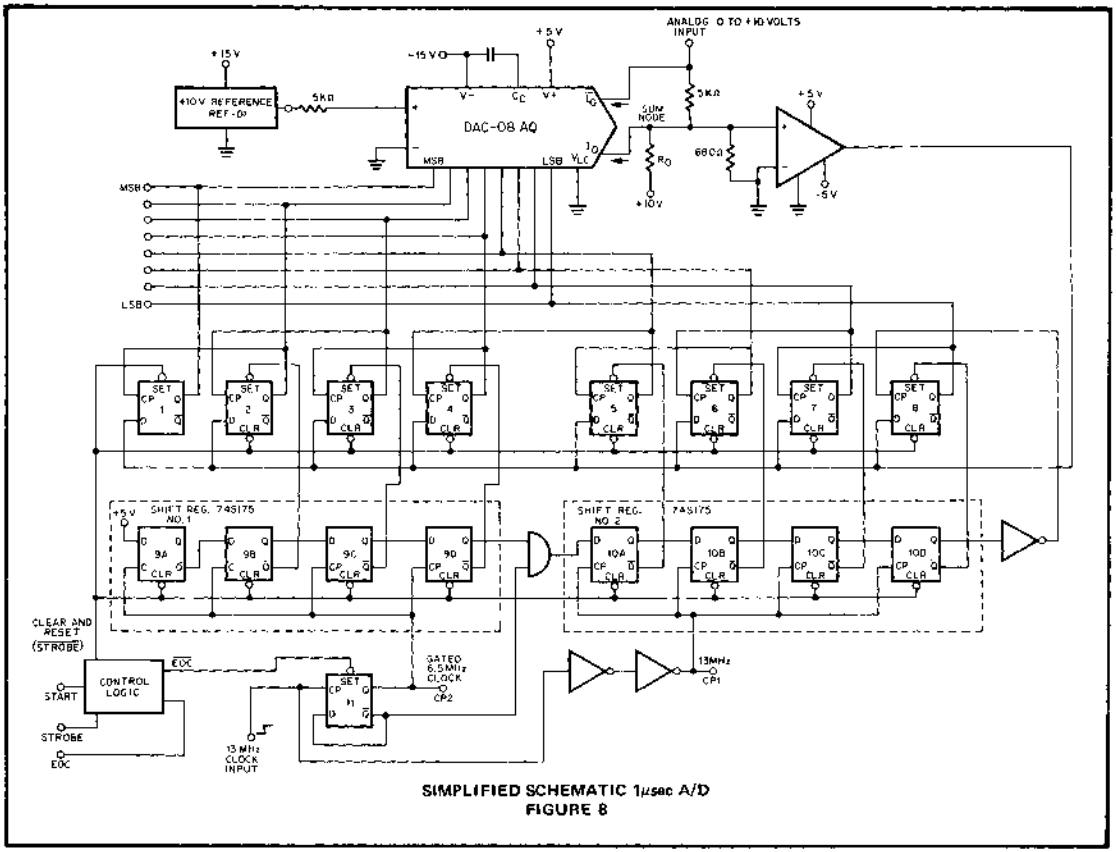
A conversion is initiated by a high level at the Start input when the input 13MHz clock makes a low to high transition. Approximately 9nsec later, the control logic generates a clear and reset pulse ($\overline{Strobe}$), which causes several events: the 8 output flip-flops are cleared except for the MSB flip-flop 1 which is set to a "one"; both shift registers are cleared; the DAC has Bit 1 turned on, all others are off. The conditions for the first trial at half scale are now established.

As the DAC output settles, the comparator continuously examines the polarity at its non-inverting input. For this case, with zero volts at the Analog Input, the comparator finds a negative voltage present; its output therefore is low. This low is applied to the "D" inputs of all 8 output flip-flops. Recall that 74S74 flip-flop outputs won't change until they are clocked by a positive transition at their CP inputs. At the time labeled 1 on the CP1 waveform, the reset and clear pulse, $\overline{Strobe}$, returns high.

Shift Register No. 1 waits for a positive-going transition of CP2. At 2 time CP2 goes high, transferring a "one" from 9A-$\overline{Q}$ to 9B-Q; 9B-$\overline{Q}$ goes low, setting 2-Q high and clocking the comparator's "zero" into the Bit 1 flip-flop. The other 6 flip-flops do nothing, because they are not clocked. Bit 1's answer is now latched, and Bit 2, 1/4 full scale, is being tried. The process continues with the shift register causing each bit to be tried from Bit 2 to Bit 8. After the Bit 8 decision, the EOC output goes high, indicating that the answer in parallel format is available at the 8 bit outputs.

OUTPUT INTERFACING

In continuous conversion operation, the most common connection, EOC is connected to the Start input. While the answer is available whenever EOC is high, it is convenient to use the positive-going edge of the Strobe output as a clock for two 74S175 quad "D" flip-flops used as an 8 bit storage latch. Since Strobe goes high before another conversion cycle begins, there is ample setup time for the latch; the answer has been steady for over 35nsec.



SIMPLIFIED SCHEMATIC 1μsec A/D
FIGURE 8

OVERALL DESIGN

Due to the bit settling time range of the DAC-08 from 85nsec for Bit 1 to 35nsec for Bit 8, progressively decreasing trial-and-decision periods would be ideal. Practically, such a timing sequence is difficult to generate at low cost, so a compromise was made: The first four bits allow 160nsec for each trial-and-decision, while the last four bits allow 80nsec. This may be seen in the waveforms of Fig. 9. The timing sequence is generated by shifting a "one" through two shift registers with in-phase clocks, one at 6.5MHz derived from the other at 13MHz.

Standard 74 Schottky TTL logic was selected for speed, compatibility with the AM686 comparator, ready availability, and price.

A useful characteristic of the DAC-08 is its capability to directly interface with all popular logic families including TTL, CMOS, and ECL. For this design the DAC-08's logic control pin (pin 1) is grounded to provide the proper TTL logic threshold. A design utilizing ECL could provide slightly faster conversion time at increased power consumption.

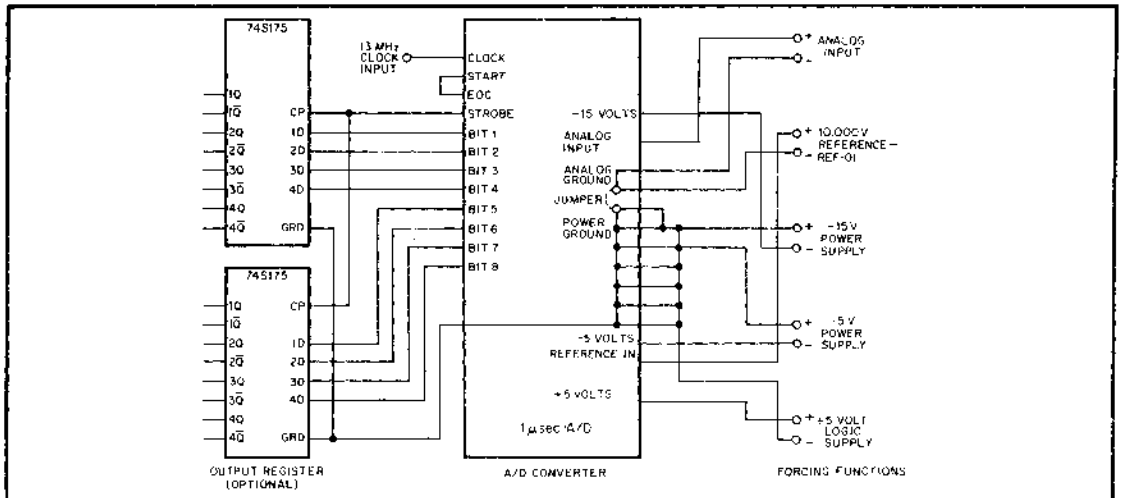
LOGIC DESIGN

The primary logic design element is the 74S series positive-edge-triggered "D" flip-flop. This type of flip-flop is useful in A/D designs because of several properties:

1. The propagation delay from Set to Q going high is only 3nsec.
2. The information on the D input is transferred to the Q output only at a positive-going edge of CP.
3. Changes at the D input (comparator settling changes) are ignored when CP is in a steady state.

74S74 dual "D" flip-flops are used for the 8 output latches and for the control logic, and 74S175 quad "D" flip-flops are used for the two shift registers.

Flip-flops 2 through 8 in the simplified schematic (Fig. 8) perform two functions. Typical operation can be understood by examining the operation of flip-flop 2. When set by an input from Shift Register No. 1, the Q output of flip-flop No. 2 goes high, which starts the trial of bit 2 and acts as a clock for flip-flop 1, transferring the comparator's output state, which is the result of trial 1, to Q of flip-flop 1. This basic connection, using the beginning of a new trial to clock the previous bit trial, is used on all 8 output flip-flops. The start of each bit trial is precisely coincident with clocking of the previous bit answer; so no time is wasted, and logic delays are reduced to setup times only.



TYPICAL SYSTEM CONNECTION
FIGURE 11

PRINTED CIRCUIT BOARD LAYOUT RULES

For A/D designs generally, and high speed designs in particular, layout is important. Some of the more important rules are listed below:

1. Digital ground must be separated from analog ground; they must meet at only one common point.
2. Digital traces should not cross or be routed near sensitive analog areas; this is especially important near the sum node.
3. With Schottky TTL logic, the digital ground and V_{CC} traces should be large and contain provisions for generous bypassing.
4. The trace from the DAC output to comparator input (sum node) should be short, and it should be guarded by analog ground.
5. All analog components should be located as close as possible to the edge connector so that the input analog traces will be short.
6. The comparator's outputs should be routed away from its inputs, to minimize capacitive coupling and possible oscillation.

SYSTEM CONSIDERATIONS

Typical system connections are shown in Figure 11. Digital grounds and analog grounds meet at one point only keeping large power supply return currents away from the sensitive analog ground portion of the A/D system. Start is connected to EOC for continuous conversions, and Strobe is used to clock the parallel answer into an output register at the end of each conversion.

CONCLUSION

The DAC-08 high speed monolithic D/A converter greatly simplifies construction of high speed A/D converters. Designs using only three IC's achieve 2μsec and 4μsec conversions, and 1μsec conversions can be attained with additional logic. Techniques have been presented which allow the user to construct low cost, high speed A/D converters.

Application Notes

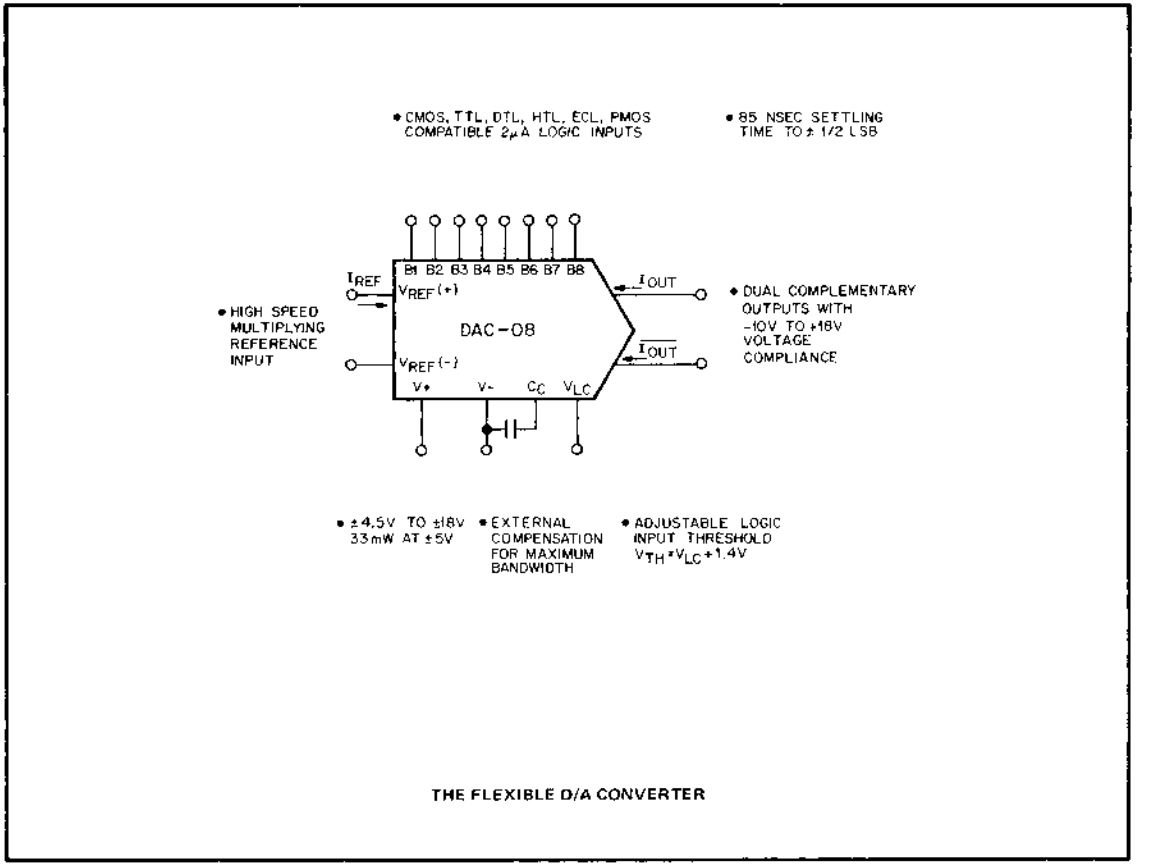
AN-17

DAC-08 APPLICATIONS COLLECTION

by
John Schoeff & Donn Soderquist

There has been a trend in recent years toward providing totally dedicated Digital-to-Analog Converters with limited applications versatility. This application note describes a new type of monolithic DAC designed for an extremely broad range of applications, the Precision Monolithics DAC-08.

Several unique design features of this low cost DAC combine to provide total applications flexibility. Principal among them are: dual complementary, true current outputs; universal logic inputs capable of interfacing with any logic family; 85 nsec settling time; high speed multiplying capability; and finally, the ability to use any standard system power supply voltages. A description of these features is given followed by specific applications using each feature.



THE FLEXIBLE D/A CONVERTER

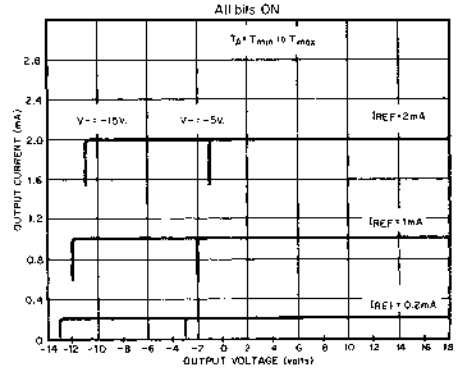
OUTPUT

HIGH VOLTAGE COMPLIANCE CURRENT OUTPUTS

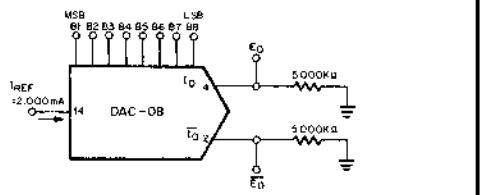
Many older current-output DAC's actually have resistive outputs which must be terminated in a virtual ground. The DAC-08, however, is a true digitally-controlled current source with an output impedance typically exceeding 20 megohms.

Its outputs can swing between −10V and +18V with little or no effect on full scale current or linearity. Some of the applications that require high output voltage compliance include:

1) Precise current transmission over long distances.
2) Programmable current sources.
3) Analog meter movement driving.
4) Resistive termination for a voltage output without an op amp.
5) Capacitive termination for digitally-controlled integrators.
6) Inductive termination with balanced transformers, transducers and headsets.

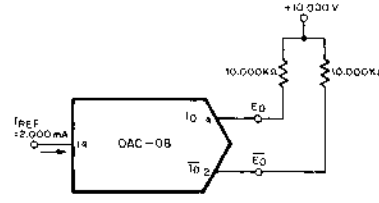


OUTPUT CURRENT VS. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



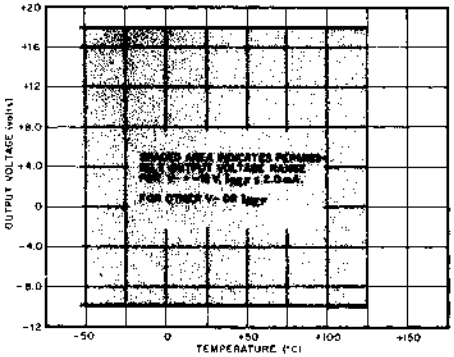
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	.000	-9.960	.000
FULL SCALE-LSB	1	1	1	1	1	1	1	0	1.984	.008	-9.920	-.040
HALF SCALE+LSB	1	0	0	0	0	0	0	1	1.008	.984	-5.040	+4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	-5.000	+4.960
HALF SCALE-LSB	0	1	1	1	1	1	1	1	.992	1.000	-4.960	+5.000
ZERO SCALE+LSB	0	0	0	0	0	0	0	1	.008	1.984	-.040	+9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	+9.960

BASIC UNIPOLAR NEGATIVE OPERATION

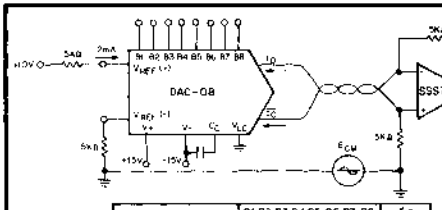


	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL SCALE-LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
ZERO SCALE+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+0.080
ZERO SCALE-LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	−9.920

BASIC BIPOLAR OUTPUT OPERATION



OUTPUT VOLTAGE COMPLIANCE VS. TEMPERATURE



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE-LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	−0.040
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	−9.920

- PROVIDES ISOLATION FROM GROUND LOOPS
- SYMMETRICAL ±10V OUTPUT
- USEFUL WITHIN SYSTEMS OR BETWEEN BOARDS
- TRUE COMPLEMENTARY/DIFFERENTIAL CURRENT TRANSMISSION
- HIGH SPEED ANALOG SIGNAL TRANSMISSION

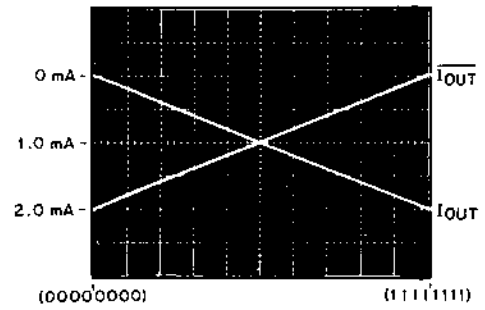
HIGH NOISE IMMUNITY CURRENT TO VOLTAGE CONVERSION

DUAL COMPLEMENTARY OUTPUTS

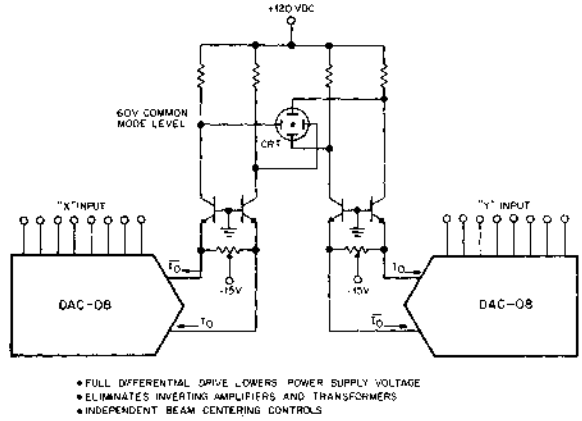
Conventional DAC's have a single output, so they cannot drive balanced loads and are limited to a single input code polarity. The DAC-08 was designed to overcome these limitations

Input coding of positive binary or complementary binary is obtained by a choice of outputs, I_O for positive-true or $\overline{I_O}$ for negative-true. In many applications both are used either independently or in combination. Dual complementary outputs allow some very unusual and useful DAC applications:

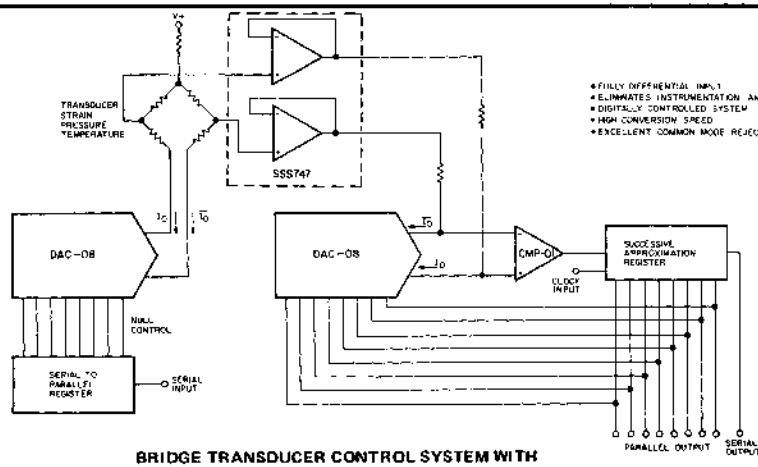
1) CRT display driving without transformers.
2) Differential transducer control systems.
3) Differential line driving.
4) High speed waveform generation.
5) Digitally controlled offset nulling of op amps.



TRUE AND COMPLEMENTARY OUTPUT OPERATION



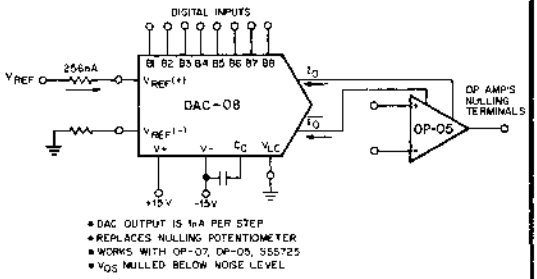
CRT DISPLAY DRIVER



BRIDGE TRANSDUCER CONTROL SYSTEM WITH FULL DIFFERENTIAL INPUT

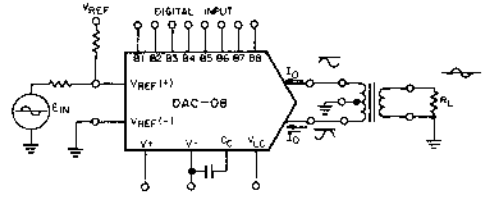
OUTPUT

DUAL COMPLEMENTARY OUTPUTS



- DAC OUTPUT IS 1mA PER STEP
- REPLACES NULLING POTENTIOMETER
- WORKS WITH OP-07, OP-05, 555725
- V_{OS} NULLED BELOW NOISE LEVEL

DIGITALLY CONTROLLED OFFSET NULLING



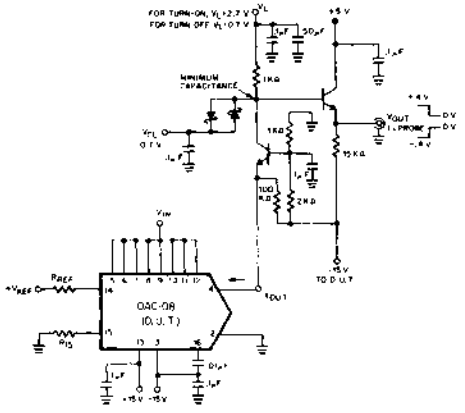
- BIPOLAR OUTPUT WITH OFFSET BINARY CODING
- PROVIDES DC ISOLATION BETWEEN SOURCE AND LOAD
- HIGH VOLTAGE OUTPUT CAPABILITY
- USEFUL WITH PULSE OR SINE WAVE REFERENCE INPUT
- USEFUL WITH PULSE OR SINE FUNCTION DIGITAL INPUT

BALANCED TRANSFORMER DRIVE

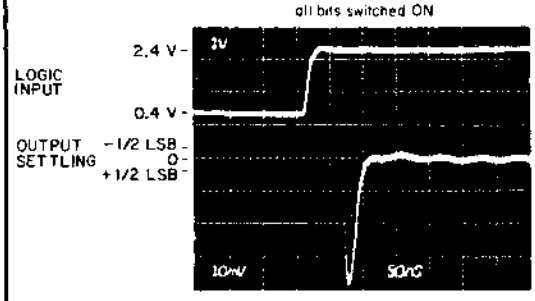
HIGH SPEED

Sub-microsecond settling times are common in current-output DAC's. Many DAC's settle in 500 nsec; 300 nsec is not unusual. But 85 nsec settling time for a low cost DAC is exceptional, and this characteristic allows use of the DAC-08 in formerly difficult and expensive-to-build applications:

1) 1μsec, 2μsec and 4μsec A/D's. (These are completely described in AN-16, available upon request)
2) 15 MHz Tracking A/D's.
3) ECL compatible applications.
4) Video displays requiring a low-glitch DAC.
5) Radar pulse height analysis sytems.



SETTLING TIME MEASUREMENT CIRCUIT

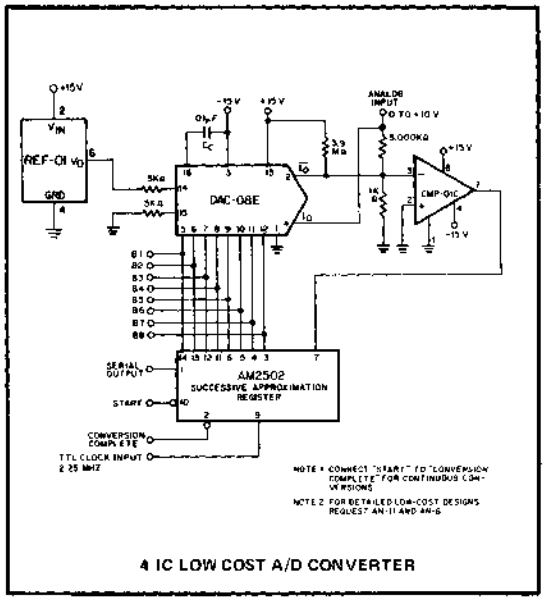


50 nsec/division

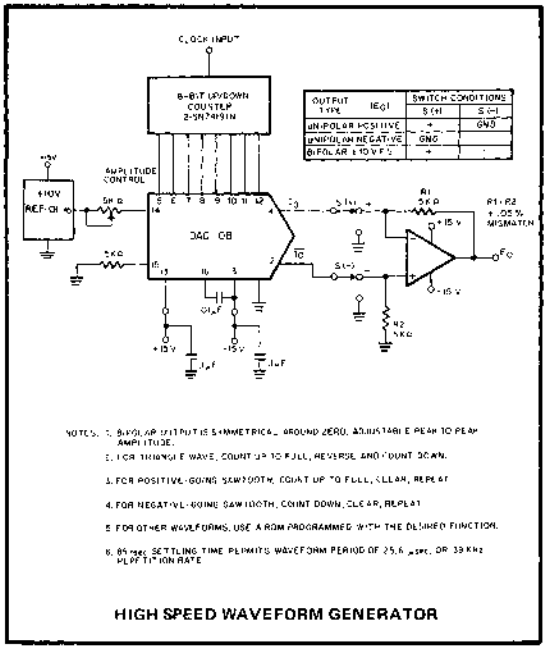
I_{FS} = 2mA R_L = 1K Ω
1/2 LSB = 4μA

FULL SCALE SETTLING TIME

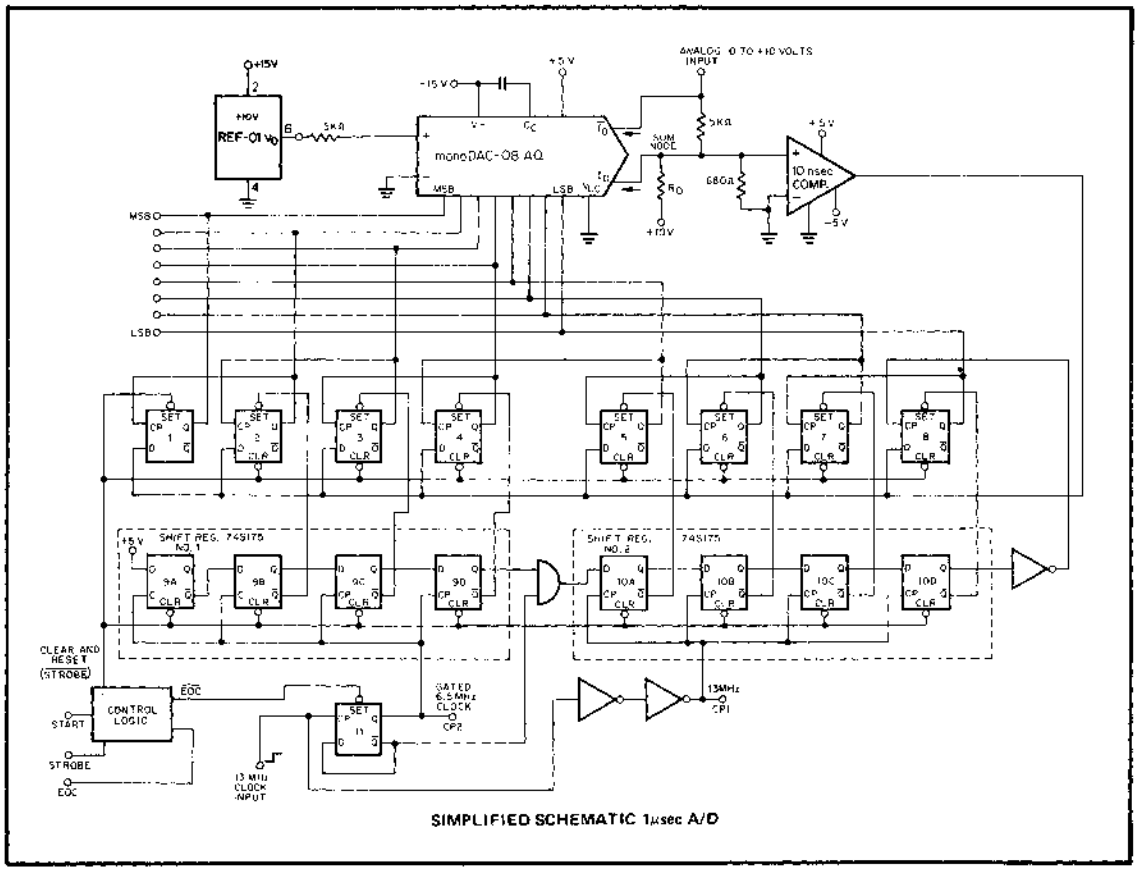
HIGH SPEED



4 IC LOW COST A/D CONVERTER



HIGH SPEED WAVEFORM GENERATOR



SIMPLIFIED SCHEMATIC 1μsec A/D

LOGIC INPUTS

ADJUSTABLE INPUT LOGIC THRESHOLD

Most DAC's have TTL or CMOS compatible inputs which require complicated interfaces for use with ECL, PMOS, NMOS or HTL logic. By contrast, the DAC-08, with typical logic input current of 2μA and an adjustable input logic threshold, interfaces easily with any logic family in use today. The logic input threshold is 1.4V positive with respect to pin 1; for TTL pin 1 is therefore grounded; for other families pin 1 is connected as shown in the interfacing figure. An adjustable threshold and a −10V to +18V input range greatly simplify system design especially with other-than-TTL logic.

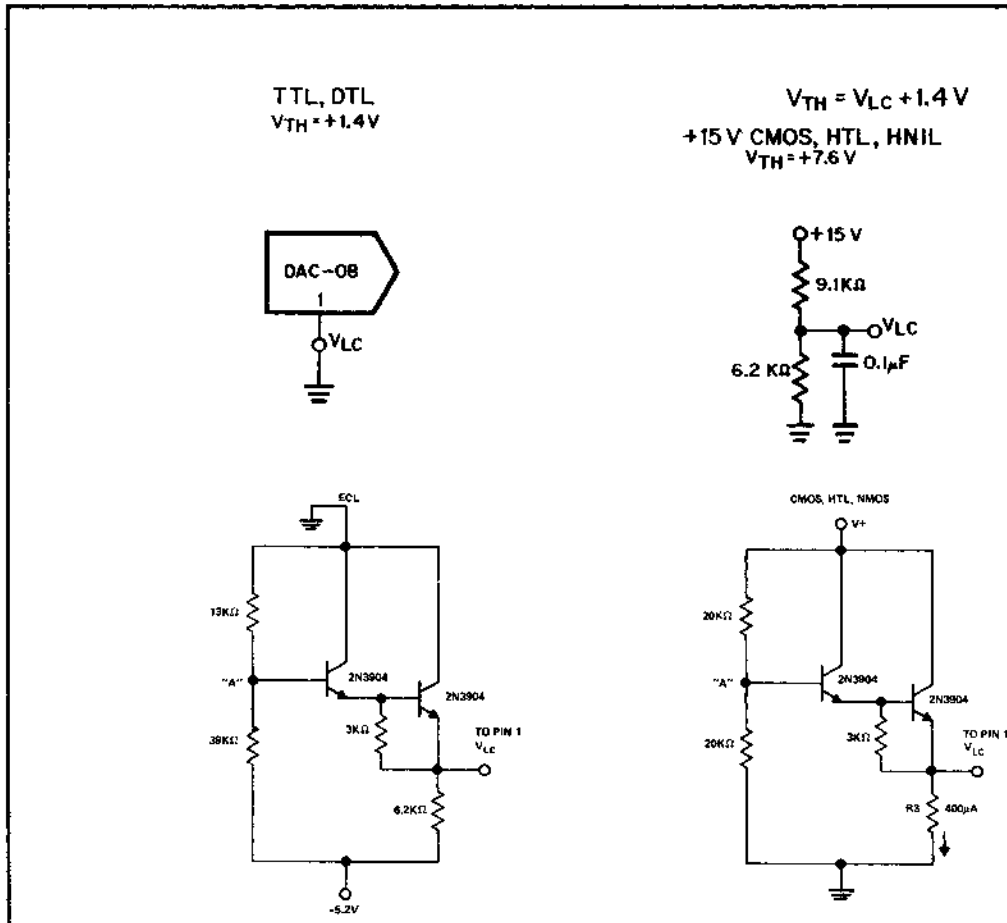
1) ECL applications without level translators.

2) Direct interfaces with Hi-Z RAM outputs.

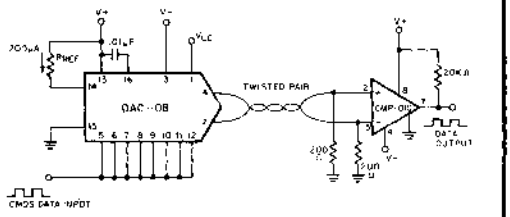
3) CMOS applications without static discharge considerations.

4) HTL or HNIL applications without level translators.

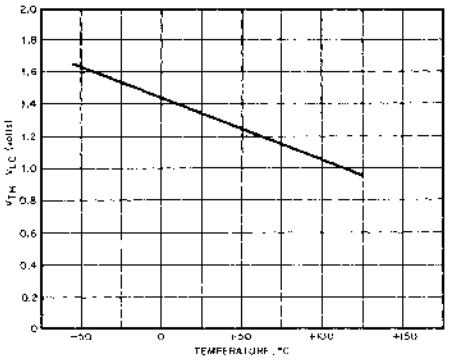
5) System size, weight, and cost reductions.



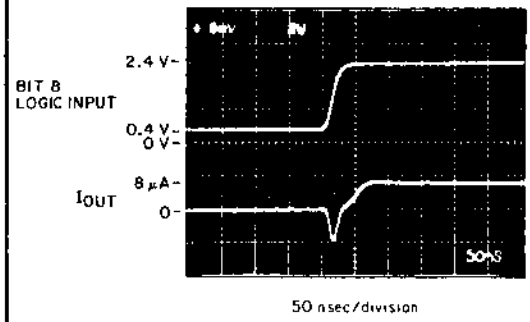
INTERFACING WITH VARIOUS LOGIC FAMILIES



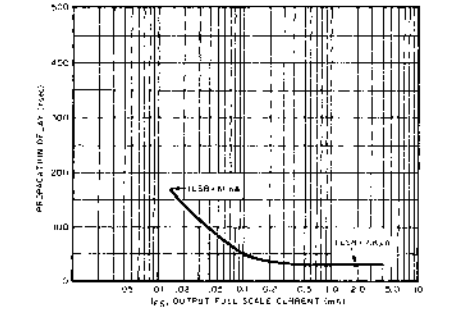
CMOS DIFFERENTIAL LINE DRIVER/RECEIVER



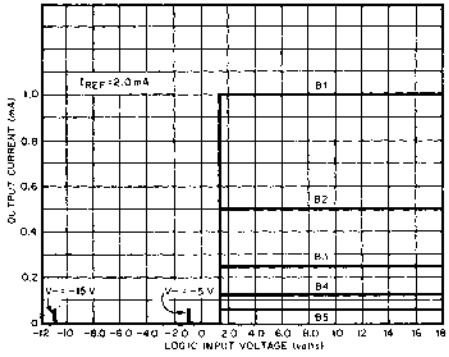
$V_{TH} - V_{LC}$ VS. TEMPERATURE



LSB SWITCHING

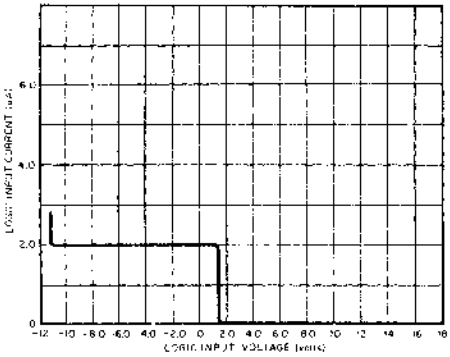


LSB PROPAGATION DELAY VS. I_{FS}



NOTE: B1 THROUGH B8 HAVE IDENTICAL TRANSFER CHARACTERISTICS. BITS ARE FULLY SWITCHED, WITH LESS THAN ½ LSB ERROR, AT LESS THAN ±100mV FROM ACTUAL THRESHOLD. THESE SWITCHING POINTS ARE GUARANTEED TO LIE BETWEEN 0.8 AND 2.0 VOLTS OVER THE OPERATING TEMPERATURE RANGE (V_{LC} = 0.0V).

BIT TRANSFER CHARACTERISTICS



LOGIC INPUT CURRENT VS. INPUT VOLTAGE

MULTIPLYING CAPABILITY

Fixed internal references are included in many DAC's, but they limit the user to non-multiplying, single polarity reference applications and do not allow a single system reference. To achieve the design goals of low cost and total applications flexibility, the DAC-08 uses an external reference. Positive or negative references may be applied over a wide common mode voltage range. In addition, the full scale current is matched to the reference current eliminating calibration in most applications.

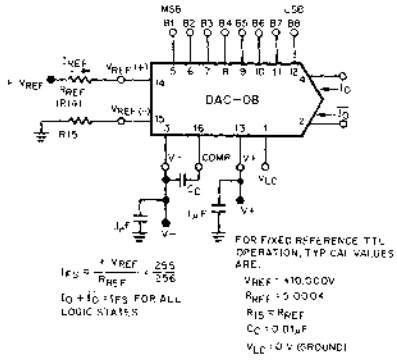
1) Digitally controlled full scale calibration.

2) 8 x 8 multiplication of 2 digital words.

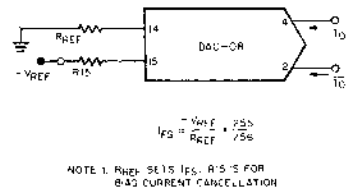
3) Digital Attenuators/Programmable gain amplifiers.

4) Modem transmitters to 1 MHz.

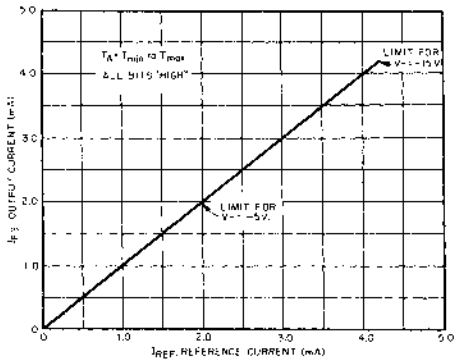
5) Remote shutdown and party line DAC applications.



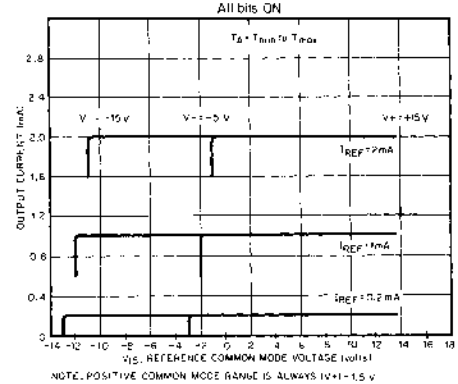
BASIC POSITIVE REFERENCE OPERATION



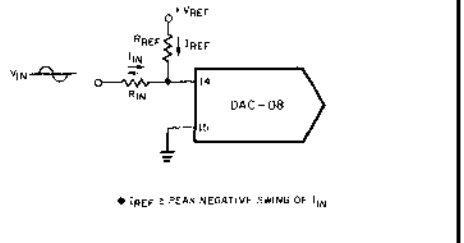
BASIC NEGATIVE REFERENCE OPERATION



FULL SCALE CURRENT VS. REFERENCE CURRENT



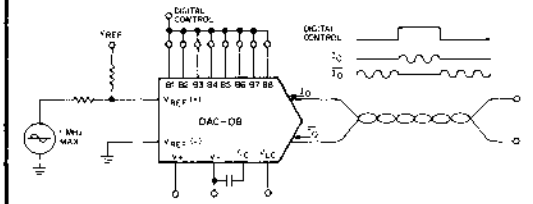
REFERENCE AMP COMMON MODE RANGE



● I_{REF} ≥ PEAK NEGATIVE SWING OF I_{IN}

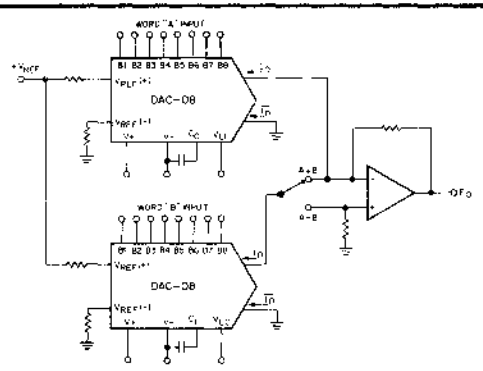
● +V_{REF} MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

ACCOMODATING BIPOLAR REFERENCES



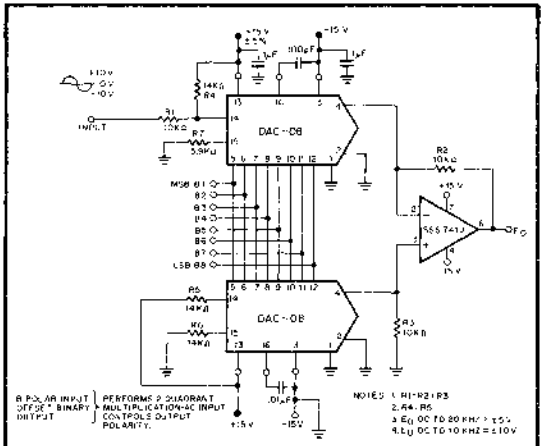
● AC VOLTAGE TO DIFFERENTIAL CURRENT CONVERSION
● DC TO 1MHz INPUT RANGE
● OUTPUT DRIVES TWISTED PAIR DIRECTLY
● CMOS COMPATIBLE

MODEM TRANSMITTER

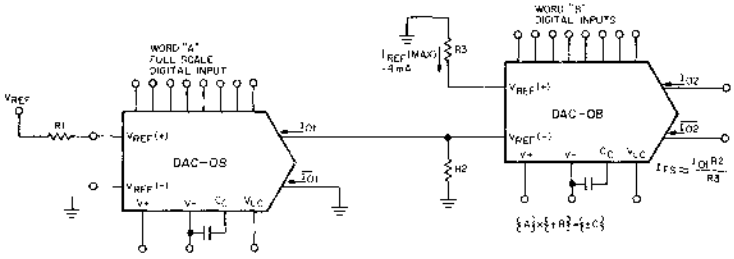


● FAST—85 NSEC PLUS OP AMP SETTLING TIME
● ANY LOGIC FAMILY FOR WORD "A" OR "B"
● BIPOLAR OUTPUT
● ELIMINATES SEVERAL LOGIC PACKAGES

DIGITAL ADDITION OR SUBTRACTION WITH ANALOG OUTPUT



DC-COUPLED DIGITAL ATTENUATOR/ PROGRAMMABLE GAIN AMPLIFIER



● I_{FS} IS THE PRODUCT OF 2 DIGITAL INPUT WORDS
● MAY BE USED AS A 8×8 DIGITAL MULTIPLIER WITH ANALOG OUTPUT
● ELIMINATES D/A AFTER DIGITAL MULTIPLICATION
● FUNCTIONS WITH ANY LOGIC FAMILY
● NOTE: LIMIT WORD "B" INPUT RISE AND FALL TIMES TO 200NSEC MINIMUM

DIGITALLY CONTROLLED FULL SCALE CALIBRATION (MULTIPLIER)

POWER SUPPLIES

POWER SUPPLY REQUIREMENTS

The DAC-08 works with ±4.5V to ±18V supplies allowing use with all standard digital and analog system supply voltages plus most battery voltages. With only 33mW of power dissipation at ±5V and 85nsec settling time, it has a lower speed power product than CMOS DAC's. Power dissipation is almost constant over temperature, and bypassing is accomplished with 0.01μF capacitors—no large electrolytics are required. These power supply requirements allow:

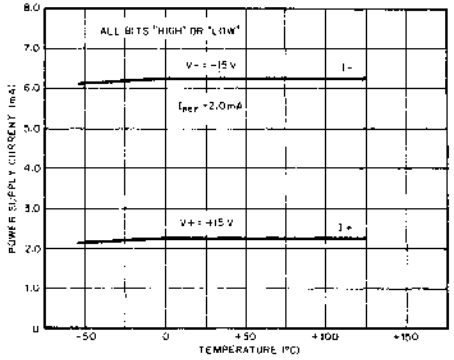
1) Battery operation.

2) Use of unregulated or poorly regulated power supplies.

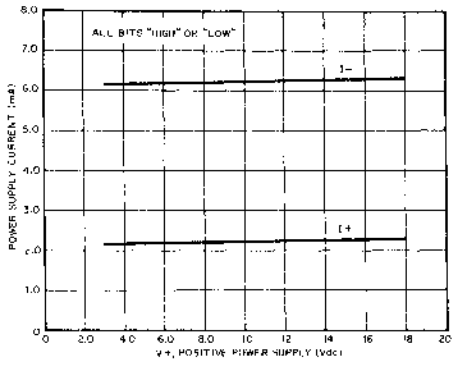
3) Use in space-limited areas due to small bypass capacitors.

4) Use in constant power dissipation applications.

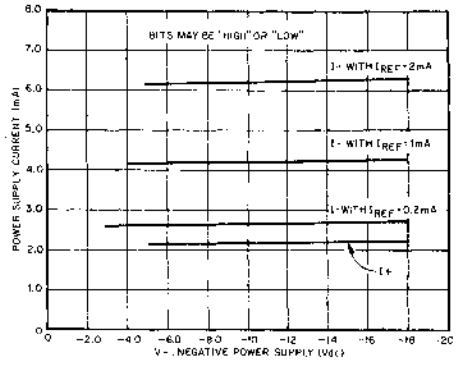
5) Common digital and analog power supplies.



POWER SUPPLY CURRENT VS. TEMPERATURE



POWER SUPPLY CURRENT VS. V+



POWER SUPPLY CURRENT VS. V—

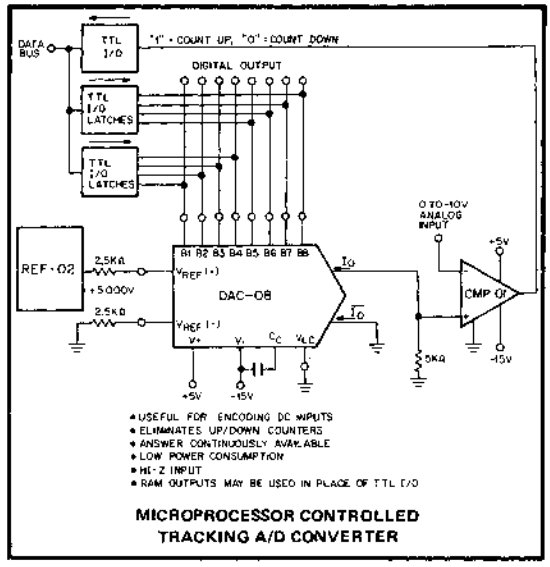
OTHER APPLICATIONS

MICROPROCESSOR APPLICATIONS

The ability to use μP power supply voltages and the ability to interface with any logic family make the DAC-08 especially useful in μP applications:

1) Tracking A/D converters.
2) Successive approximation A/D converters.
3) Direct drive from Hi-Z MOS RAM outputs.

By programming the ROM's with the successive approximation or the tracking A/D algorithm, all of the logic for A/D conversion is contained in the μP. This is a very inexpensive approach, since there is no need for the usual A/D conversion logic packages.



MICROPROCESSOR CONTROLLED TRACKING A/D CONVERTER

OTHER APPLICATIONS: The following list summarizes just a few of the many applications for this flexible DAC. Consult the factory for further information.

A/D CONVERTERS

Tracking (Servo)
Successive Approximation
Ramp (Staircase)
Microprocessor Controlled
Ratiometric (Bridge Balancing)

TEST SYSTEMS

Transistor Tester (Force I_B and I_C)
Resistor Matching (Use both outputs)
Programmable Power Supplies
Programmable Pulse Generators
Programmable Current Source
Function Generators (ROM Drive)

ARITHMETIC OPERATIONS

Analog Division by a Digital Word
Analog Quotient of Two Digital Words
Analog Product of Two Digital Words—Squaring
Addition and Subtraction with Analog Output
Magnitude Comparison of Two Digital Words
Digital Quotient of Two Analog Variables
Arithmetic Operations with Words from Different Logic Families

GRAPHICS AND DISPLAYS

Polar to Rectangular Conversion
CRT Character Generation
Chart Recorder Driver
CRT Display Driver

DATA TRANSMISSION

Modem Transmitter
Differential Line Driver
Party Line Multiplexing of Analog Signals
Multi-level 2-Wire Data Transmission
Secure Communications (Constant Power Dissipation)

CONTROL SYSTEMS

Reference Level Generator for Setpoint Controllers
Positive Peak Detector
Negative Peak Detector
Disc Drive Head Positioner
Microfilm Head Positioner

AUDIO SYSTEMS

Digital AVC and Reverberation
Music Distribution
Organ Tone Generator
Audio Tracking A/D

CONCLUSION

High voltage compliance complementary current outputs, universal logic inputs and multiplying capability make the Precision Monolithics DAC-08 the most versatile monolithic high speed DAC available today.

THERMOMETER APPLICATIONS OF THE REF-02

by
George Erdi

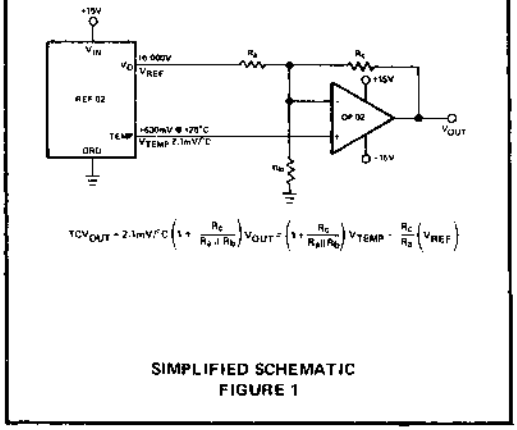
INTRODUCTION

This application note describes electronic thermometer applications of the REF-02 +5V Voltage Reference where the voltage output is a direct measurement of temperature in °C or in °F. These applications use the predictable 2.1mV/°C TEMP output voltage temperature coefficient of the REF-02, a byproduct of a bandgap voltage reference design. Thermometer applications are described first followed by a discussion of bandgap voltage reference theory.

THERMOMETER ESSENTIALS

In addition to a highly linear temperature sensitive component, electronic thermometers should have the following characteristics:

1) Convenient scaling such as 10mV/°C, 100mV/°C, or 10mV/°F.
2) Direct voltage readings such as –0.55V at –55°C, 0V at 0°C, and +1.25V at +125°C.
3) Room temperature calibration.



SIMPLIFIED SCHEMATIC
FIGURE 1

BASIC CIRCUIT IMPLEMENTATION

The simplified schematic in Fig. 1 shows the basic thermometer connections. An operational amplifier, three resistors, and the +5.000V output of the REF-02 function together to level shift and amplify V_{TEMP} allowing V_{OUT} to read in the desired manner. The expression for V_{OUT} is:

$$\text{Eq. 1)} \quad V_{OUT} = \left(1 + \frac{R_c}{R_a \parallel R_b}\right) V_{TEMP} - \frac{R_c}{R_a}(V_{REF})$$

The first term is the gain of the circuit with V_{REF} equal to 0V; the second term is the gain of the circuit with V_{TEMP} equal to 0V. Differentiating Eq. 1 with respect to temperature gives the slope, S, of the output-versus-temperature curve:

$$\text{Eq. 2)} \quad \frac{dV_{OUT}}{dT} = S = m\left(1 + \frac{R_c}{R_a \parallel R_b}\right)$$

$$= 2.1\text{mV/°C}\left(1 + \frac{R_c}{R_a \parallel R_b}\right)$$

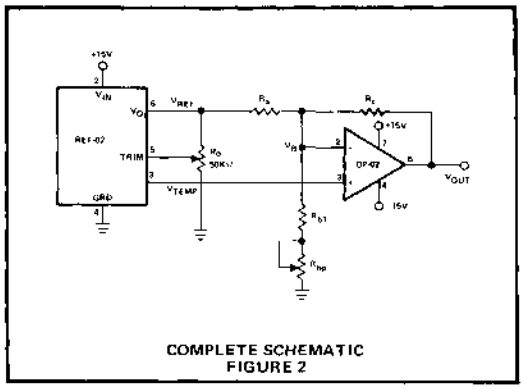
where $m = TCV_{TEMP}$

Thus, the ratio of R_c to $R_a \parallel R_b$ sets the slope of V_{OUT}, and the ratio of R_c to R_a and V_{REF} set the initial output value at 25°C. Table I lists typical scaling ratios for different output scales

TEMPERATURE SCALING RATIOS

V_{REF} = 5.000V, V_{TEMP} = 630mV @ 25°C, TCV_{TEMP} = 2.1mV/°C			
V_{OUT} @ 25°C (77°F)	TCV_{OUT} (Slope)	$\frac{R_c}{R_a}$	$\frac{R_c}{R_a \parallel R_b}$
250mV	10mV/°C	0.55	3.76
2.5V	100mV/°C	5.50	46.6
770mV	10mV/°F	0.926	7.57

TABLE I



COMPLETE SCHEMATIC
FIGURE 2

COMPLETE CIRCUIT

Two potentiometers, R_p and R_{bp}, have been added to the circuit for precise calibration and to allow for the ±1% resistor tolerances. V_{REF} is adjusted by R_p to set the V_{OUT} value at +25°C (77°F); the ratio of R_c to $R_a \parallel R_b$ is adjusted by R_{bp} to set the slope of V_{OUT} versus temperature. Resistor values for typical output scales are shown in Table II.

RESISTOR VALUES

TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55° to +125°C	−55° to +125°C	−67°F to +257°F
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (±1% resistor)	9.09KΩ	15KΩ	8.25KΩ
R_{b1} (±1% resistor)	1.5KΩ	1.82KΩ	1.0KΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11KΩ	84.5KΩ	7.5KΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if this is a problem.

TABLE II

CALIBRATION CONDITIONS

All calibration is conducted in free air. Heatsinking of the REF-02 is unnecessary and is undesirable. The small (2°C) rise in chip temperature of the REF-02 above ambient temperature serves as an error-cancelling factor of some second order effects internal to the REF-02 design. The calibration procedure which follows assumes free air — no heatsinking — calibration.

CALIBRATION PROCEDURE

Calibration is performed at ambient temperature with two adjustments using the following procedure:

Step 1: Measure and record V_{TEMP} and T_A in °C.

Step 2: Calculate the calibration ratio "r" using Eq. 3:

$$\text{Eq. 3)} \quad r \equiv \frac{R_a \parallel R_b}{R_c + R_a \parallel R_b} = \frac{V_{TEMP} \text{ in mV}}{S(T_A + 273)}$$

Where S = TCV_{OUT}, T_A = ambient temperature in °C

Step 3: Turn power off, short V_{REF} terminal to ground, and apply a precise 100mV to the V_{OUT} terminal.

Step 4: Adjust R_{bp} so that V_B = r(100mV); remove short.

Step 5: Turn power on; adjust R_p so that V_{OUT} equals the correct value at ambient temperature.

The system is now calibrated.

CALIBRATION EXAMPLE

Here is an example at T_A = 25°C, S = 10mV/°C, and V_{TEMP} = 632mV:

Step 1: V_{TEMP} = 632mV, T_A = 25°C.

Step 2: Using Eq. 3:

$$r = \frac{V_{TEMP}}{S(T_A + 273)} = \frac{632}{10(25 + 273)} = \frac{632}{2980} = 0.2121$$

Step 3: Apply 100.00mV to V_{OUT} with power off and V_{REF} connected to ground.

Step 4: Adjust R_{bp} so that V_B = r(100mV) = 21.21mV

Step 5: Turn power on and adjust R_p so that V_{OUT} equals +0.25V.

The system is now calibrated.

TRANSDUCER ERROR FACTORS

Error terms are threefold:

1. Slope errors — Deviations from nominal slope. For example, if the slope is 10.04mV/°C instead of 10.00mV/°C, the accuracy due to the slope error is 0.4%.
2. Linearity errors — Deviations in V_{TEMP} versus temperature from straight line performance, a change in V_{TEMP} slope with temperature.
3. Offset error — V_{OUT} deviations due to changes in V_{REF} with temperature.

Since these errors are grade dependent, Table III is provided as an aid in specifying the correct combination of components for a given application. Offset error can be eliminated by using one REF-02 as a temperature sensor only and another REF-02 (operated at a constant temperature) as V_{REF}.

TRANSDUCER PERFORMANCE

Typical system accuracy is ±0.5% over the −55° to +125°C range of a REF-02A. For example, when calibrated at +25°C, the reading of V_{OUT} at +105°C may be 105.4°C, a deviation of 0.5% of the 80° temperature change (+25°C to +105°C).

Although the REF-02 is guaranteed to perform over the −55° to +125°C range only, operation beyond those limits is possible. A large number of devices were measured and found to be functioning satisfactorily over the −150°C to +170°C range, and there was only a slight degradation in accuracy.

REMOTE APPLICATIONS

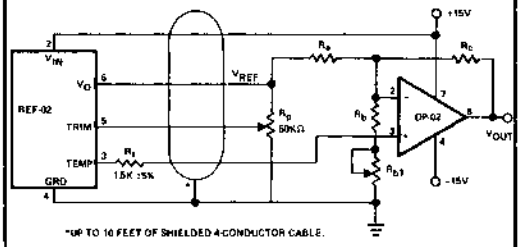
In many applications, the sensor must be located some distance away from the measurement circuitry. One precaution must be taken with the REF-02: a 1.5KΩ resistor

should be connected between pin 3 (TEMP) and its associated cable conductor to isolate this pin from cable capacitances. Remote application of the transducer is illustrated in Fig. 3 with R_S, the isolation resistor.

TYPICAL TRANSDUCER PERFORMANCE VS. GRADE

PARAMETER \ GRADE	REF-02A	REF-02	REF-02E	REF-02H	REF-02C
TEMPERATURE RANGE	-55° to +125°C	-55° to +125°C	0° to +70°C	0° to +70°C	0° to +70°C
SLOPE ERROR	±0.30%	±0.40%	±0.25%	±0.35%	±0.45%
TCV$_{TEMP}$ ERROR	±0.10%	±0.12%	±0.08%	±0.10%	±0.16%
OFFSET ERROR	±0.15%	±0.40%	±0.10%	±0.30%	±0.60%
RMS ERROR SUM	±0.35%	±0.58%	±0.28%	±0.47%	±0.76%
TYPICAL ACCURACY	0.50%	0.75%	0.40%	0.60%	0.90%
OP-02 GRADE RECOMMENDED	OP-02A	OP-02	OP-02E	OP-02C	OP-02C

TABLE III

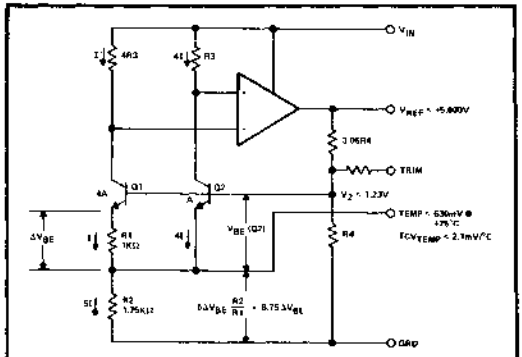


PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR
FIGURE 3

TRANSDUCER SUMMARY

The accuracies indicated compare quite favorably to traditional temperature measurement methods such as thermocouples and thermistors. Ease-of-use, low cost, and high accuracy make this new bandgap method of temperature measurement attractive in a wide range of applications.

The following section describes the bandgap principle in theory and its use in the internal REF-02 design.



REF-02 SIMPLIFIED SCHEMATIC
FIGURE 4

BANDGAP REFERENCE THEORY

Bandgap voltage references [1], [2], [3], use predictable relationships from semiconductor physics to generate a constant voltage. The base-emitter voltage of a transistor (V_{BE}) has a processing and current density dependent negative temperature coefficient of about -2.1mV/°C. Another well known relationship with a positive temperature coefficient is the difference between base-emitter voltages of two transistors operated at different current densities:

Eq. 4) $\Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{J2}{J1} \right)$, where

k = Boltzmann's constant = 1.38×10^{-23} joules/°K

T = absolute temperature, °K

q = charge of an electron = 1.6×10^{-19} coulomb

J = current density

When ΔV_{BE} is amplified and added to V_{BE}, a voltage reference with zero temperature coefficient results if the sum (V_Z) of these two terms equals the linearly-extrapolated band-gap voltage of silicon (V_{go}) at 0°K or -273°C; V_{go} = 1.205V. A more exact calculation, see reference [2], will show that V_Z will have zero temperature coefficient if:

Eq. 5) $V_Z = V_{go} + \frac{kT}{q} = 1.230V$ @ +25°C

The circuit in Fig. 4 generates a ΔV_{BE} of 72mV at 25°C by making the current density of Q2 16 times greater than Q1. Q2 has four times the current of Q1, and Q1 has four times the emitter area of Q2. A ΔV_{BE} of 72mV appears across R1 and is amplified by 8.75 (becoming the TEMP output) and is added to V_{BE} (Q2) to produce a nearly constant V_Z of 1.23V. The -2.1mV/°C of TCV$_{BE}$ is cancelled by the +2.1mV/°C of TCV$_{TEMP}$; and V_Z is amplified by 4.06 to produce an output V_{REF} of 5.000V.

REF-02 TYPICAL NODAL VOLTAGES

VOLTAGE \ TEMPERATURE	T_A = -75°C (T_J = 200°K)	T_A = +25°C (T_J = 300°K)	T_A = +125°C (T_J = 400°K)
$\Delta V_{BE} = \frac{kT}{q} \log_e 16$	48mV	72mV	96mV
$V_{TEMP} = 8.75\ \Delta V_{BE}$	420mV	630mV	840mV
V_{BE} (Q2)	810mV	600mV	390mV
$V_Z = V_{BE} + V_{TEMP}$	1.23V	1.23V	1.23V
$V_{REF} = 1 + \frac{3.06R4}{R4}$ $= 4.06\ V_Z$	5.00V	5.00V	5.00V

TABLE IV

Application Notes

AN-19

DIFFERENTIAL AND MULTIPLYING DIGITAL TO ANALOG CONVERTER APPLICATIONS

by
John Schoeff and Donn Soderquist

INTRODUCTION

The introduction of low cost monolithic D/A converters has simplified data acquisition and control system design. This application note describes several new applications using the multiplying capability and dual complementary current outputs of the Precision Monolithics DAC-08.

THE UNIVERSAL DAC

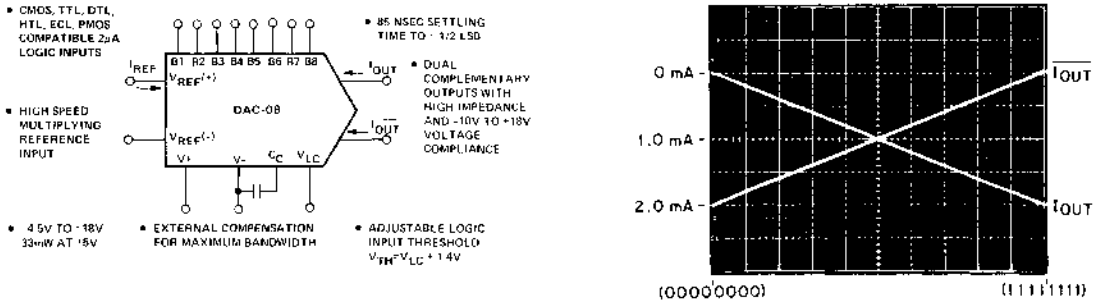


FIGURE 1

MULTIPLYING DAC BASICS

A multiplying DAC has an analog output which is the product of a digital input word and a reference voltage and can be expressed as:

1) $E_O = E_{REF}\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$

For a current reference, current output DAC, the expression becomes:

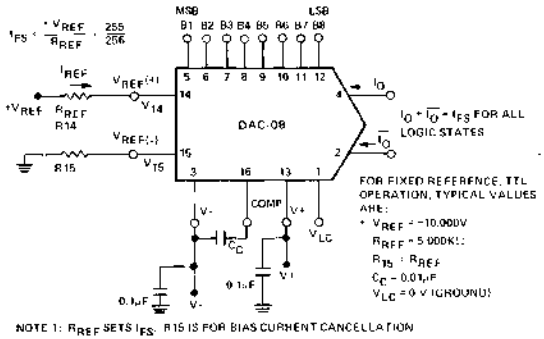
2) $I_O = I_{REF}\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$

The DAC-08 has complementary/differential current outputs, and I_O has a complement expressed as:

3) $\overline{I_O} = I_{FS} - I_O$ for all input logic states.

The relationship of I_{REF} to I_O and $\overline{I_O}$ is illustrated in Fig. 2 and in Fig. 3, the basic DC reference connections. References may be either positive or negative, and a bipolar output voltage may be achieved using the high compliance current outputs alone or with an output operational amplifier. The simplest form of a multiplying DAC accepts a unipolar varying reference input.

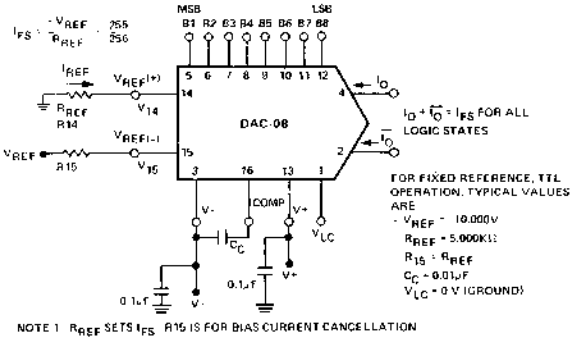
POSITIVE REFERENCE CONNECTION



NOTE 1: R_{REF} SETS I_{FS}. R15 IS FOR BIAS CURRENT CANCELLATION
NOTE 2: PINS 14 AND 15 ARE OP AMP INPUTS, SO $V_{14} \approx V_{15}$

FIGURE 2

NEGATIVE REFERENCE CONNECTION



NOTE 1: R_{REF} SETS I_{FS}. R15 IS FOR BIAS CURRENT CANCELLATION
NOTE 2: PINS 14 AND 15 ARE OP AMP INPUTS, SO $V_{14} \approx V_{15}$

FIGURE 3

BIPOLAR REFERENCES

Operation with bipolar references is achieved by modulating I_{REF} as shown in Fig. 5. To aid in understanding bipolar operation, see the equivalent circuit in Fig. 4. The reference inputs of the DAC-08 are op amp inputs — $V_{REF}(+)$ being the inverting input and $V_{REF}(-)$ being the noninverting input. Excellent gain linearity of the reference amplifier allows multiplying operation over a range of I_{REF} of 4μA to 4mA with monotonic operation from less than 100μA to 4mA.

DAC-08 EQUIVALENT CIRCUIT

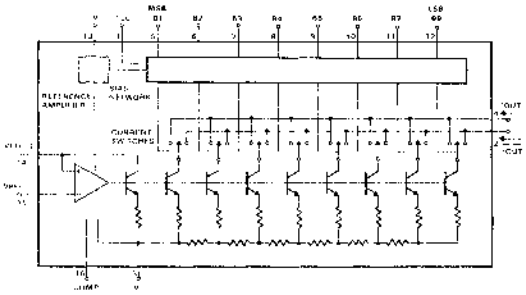


FIGURE 4

REFERENCE AMPLIFIER COMPENSATION

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0KΩ, minimum values of C_C are 15, 37, and 75 pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

FAST PULSED OPERATION

For fastest multiplying response, low values of R_{14} enabling small C_C values should be used. For R_{14} = 1KΩ and C_C = 15pF, the reference amplifier slews at 4mA/μsec enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500nsec. If R_{14} or the parallel equivalent resistance at pin 14 is less than 200Ω, no compensation capacitor is necessary, and a full scale transition requires only 160nsec.

TWO-QUADRANT MULTIPLICATION

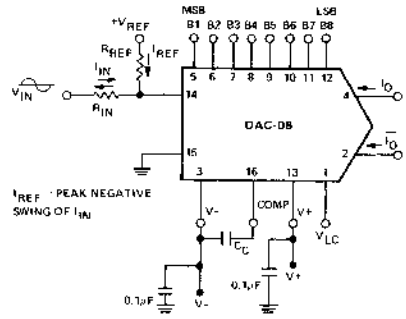
There are two forms of two-quadrant multiplication: bipolar digital, where the digital input word controls output polarity, and bipolar analog, where the analog reference input controls output polarity.

Bipolar digital two-quadrant multiplication is shown in Fig. 6 with the output polarity being controlled by an offset-binary-coded digital input word.

Bipolar analog two-quadrant multiplication is shown in Fig. 7. A bipolar reference voltage is connected to the upper DAC-08 and modulates the reference current by ±1.0mA around a quiescent current of 1.1mA. The lower DAC-08 also has a reference current of 1.1mA; due to the parallel digital inputs, the lower DAC-08 effectively subtracts out the quiescent 1.1mA of the upper DAC-08's reference

BIPOLAR REFERENCE CONNECTIONS

LOW INPUT IMPEDANCE



HIGH INPUT IMPEDANCE

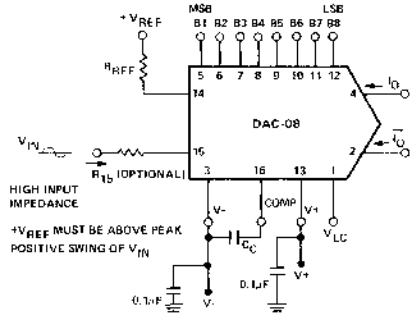
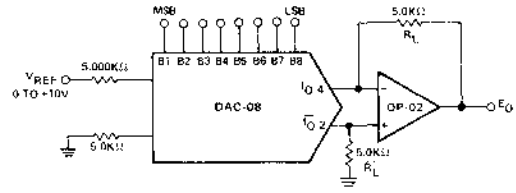


FIGURE 5

BIPOLAR DIGITAL TWO-QUADRANT MULTIPLICATION (SYMMETRICAL OFFSET BINARY)



IF $R_L = \overline{R_L}$ WITHIN ±.05%, OUTPUT IS SYMMETRICAL ABOUT GROUND

	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O(V)
POS. FULL SCALE	1	1	1	1	1	1	1	1	1.992	.000	+9.96
POS. FULL SCALE -LSB	1	1	1	1	1	1	1	0	1.984	.008	+9.88
(+) ZERO SCALE	1	0	0	0	0	0	0	0	1.000	.992	+.040
(-) ZERO SCALE	0	1	1	1	1	1	1	1	.992	1.000	-.040
NEG. FULL SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	-9.88
NEG. FULL SCALE	0	0	0	0	0	0	0	0	.000	1.992	-9.96

FIGURE 6

current at all input codes, since the voltage across R3 varies between -10V and 0V. Thus, the output voltage, E_O, is a product of a digital input word and a bipolar analog reference voltage.

BIPOLAR ANALOG TWO-QUADRANT MULTIPLICATION (DC-COUPLED DIGITAL ATTENUATOR)

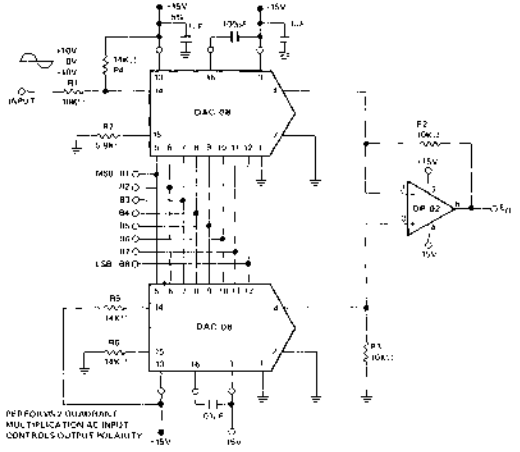


FIGURE 7

FOUR-QUADRANT MULTIPLYING DAC WITH HIGH IMPEDANCE INPUT

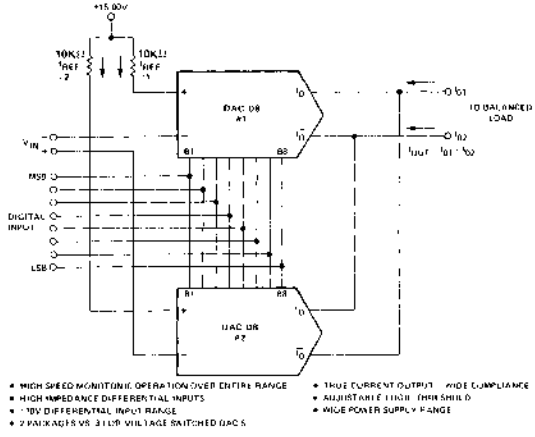


FIGURE 8

FOUR-QUADRANT MULTIPLICATION

Four-quadrant multiplication combines the two forms of two-quadrant multiplication. Output analog polarity is controlled by either the analog input reference or by the offset binary digital input word. One implementation of this function with the DAC-08 is shown in Fig. 8 with output current values listed in Table I.

The four-quadrant multiplying DAC circuit shown accepts a differential voltage input and produces a differential current output. An output op amp is not shown because it is not always required; many applications are more suited for high output compliance (-10V to +18V) differential current outputs. Typical balanced loads include transformers, transducers, transmission lines, bridges and servos.

Operation of the four-quadrant multiplier may be more easily visualized by considering that if either V_{IN} = 0V or the offset binary digital input code is at midscale (corresponding to zero), then a change in the other input will not affect the output. Zero multiplied by any number equals zero.

A common mode current will be present at the output and must be accommodated by the balanced load. A pair of matched resistors may be used at the outputs to shunt most of the common mode current to ground, thus reducing the common mode voltage swing at the output.

TABLE I — FOUR-QUADRANT MULTIPLYING CURRENT VALUES IN FIGURE 8

DIGITAL INPUT	$V_{IN}(+)$	$V_{IN}(-)$	V_{IN} DIFF.	I_{REF} #1 (mA)	I_{REF} #2 (mA)	I_O#1 (mA)	$\overline{I_O}$#2 (mA)	I_{01} (mA)	I_O#2 (mA)	$\overline{I_O}$#1 (mA)	I_{02} (mA)	I_{OUT} DIFF.
1111 1111	+5V	-5V	+10V	2.000	1.000	1.992	0	1.992	0.996	0	0.996	0.996 mA
1000 0000	+5V	-5V	+10V	2.000	1.000	1.000	0.496	1.496	0.500	0.992	1.492	0.004 mA
0111 1111	+5V	-5V	+10V	2.000	1.000	0.992	0.500	1.492	0.496	1.000	1.496	-0.004 mA
0000 0000	+5V	-5V	+10V	2.000	1.000	0	0.996	0.996	0	1.992	1.992	-0.996 mA
1111 1111	0V	0V	0V	1.500	1.500	1.494	0	1.494	1.494	0	1.494	0.000 mA
1000 0000	-10V	-10V	0V	2.500	2.500	1.250	1.240	2.490	1.250	1.240	2.490	0.000 mA
0111 1111	+10V	+10V	0V	0.500	0.500	0.248	0.250	0.498	0.248	0.250	0.498	0.000 mA
0000 0000	0V	0V	0V	1.500	1.500	0	1.494	1.494	0	1.494	1.494	0.000 mA
1111 1111	-5V	+5V	-10V	1.000	2.000	0.996	0	0.996	1.992	0	1.992	-0.996 mA
1000 0000	-5V	+5V	-10V	1.000	2.000	0.500	0.992	1.492	1.000	0.496	1.496	-0.004 mA
0111 1111	-5V	+5V	-10V	1.000	2.000	0.496	1.000	1.496	0.992	0.500	1.492	0.004 mA
0000 0000	-5V	+5V	-10V	1.000	2.000	0	1.992	1.992	0	0.996	0.996	0.996 mA

FOUR-QUADRANT MULTIPLYING DAC TRANSFER FUNCTION

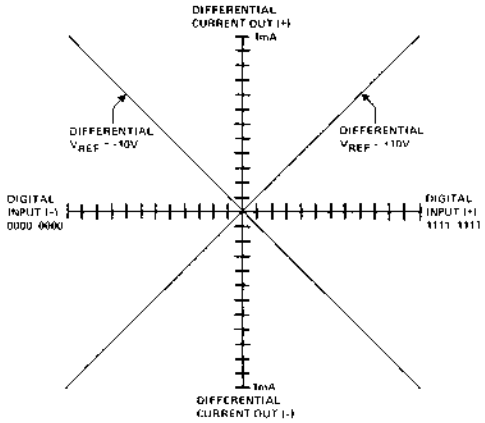


FIGURE 9

FOUR-QUADRANT MULTIPLYING DAC WITH EXTENDABLE INPUT RANGE AND HIGHEST SPEED

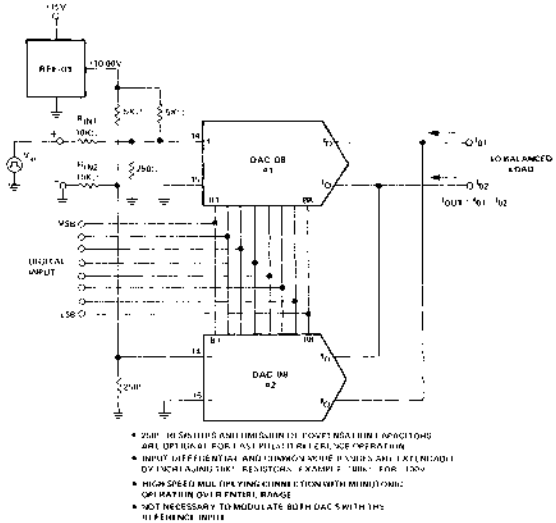


FIGURE 10

HIGHEST SPEED FOUR-QUADRANT MULTIPLYING CONSIDERATIONS

The configuration shown in Fig. 10 makes use of the DAC-08's ability to operate in a fast pulsed reference mode without compensation capacitors. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. This connection yields a reference slew rate of 16mA/μsec which is relatively independent of R_{IN} and V_{IN} values.

Input resistances are not limited to 10KΩ. For example, 100KΩ resistors for R_{IN1} and R_{IN2} allow ±100V reference voltage inputs making this connection especially useful in high common mode voltage environments. Except for different reference treatment, operation and digital input coding are identical in the circuits shown in Fig. 8 and in Fig. 10; both have the transfer function shown in Fig. 9.

AC-COUPLED MULTIPLICATION

Some multiplying DAC applications are more easily achieved with AC coupling. At the same time, a high impedance input is often required to avoid loading a relatively high source impedance. Both requirements are met by the circuits shown in Fig. 11 and Fig. 12 which use the compensation capacitor terminal (C_c) as an input. This is possible because C_c is the base of a transistor whose emitter is one diode drop (0.7V) away from the R-2R ladder network common baseline internal to the DAC-08.

With a full scale input code the output, V_O, is flat to >200KHz and is 3dB down at approximately 1.0MHz making this type of multiplying connection useful even beyond the audio frequency range. Such a connection is illustrated in Fig. 12 operating at 455KHz, the highest recommended operating frequency in this connection.

HIGH INPUT IMPEDANCE AC-COUPLED MULTIPLICATION (AUDIO FREQUENCY DIGITAL ATTENUATOR)

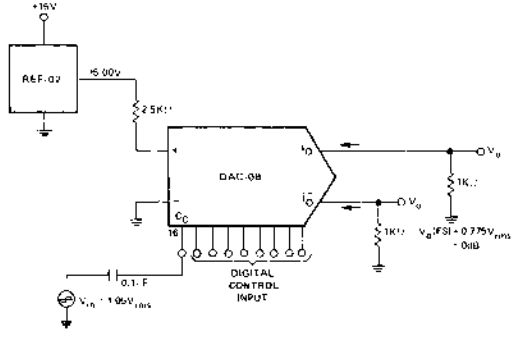


FIGURE 11

HIGH INPUT IMPEDANCE AC-COUPLED MULTIPLICATION (I.F. AMPLIFIER/DIGITAL ATTENUATOR)

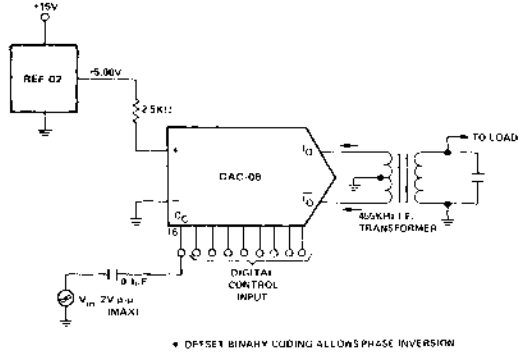


FIGURE 12

DIFFERENTIAL AND RATIOMETRIC A/D CONVERSION

Complementary/differential current-source outputs and multiplying capability allow the DAC-08 to be used in differential and ratiometric A/D converter designs directly without signal conditioning amplifiers. This group of applications begins with the basic differential A/D converter and ratiometric A/D converter connections followed by more specific applications.

These are extremely cost-effective designs due to their low parts count and simplicity. Alternative designs performing identical functions require instrumentation amplifiers for the differential-to-single-ended input signal conditioning and analog multipliers or dividers for the arithmetic functions.

DIFFERENTIAL INPUT A/D CONVERSION BASIC CONNECTIONS

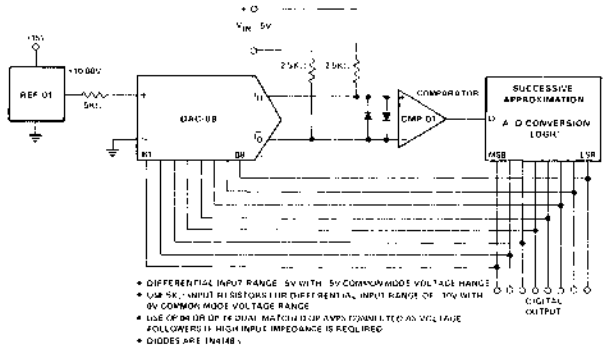


FIGURE 13

DIFFERENTIAL A/D CONVERSION

The circuit in Fig. 13 uses the high voltage compliance current output capability of the DAC-08 and the high common mode voltage rejection of the CMP-01 to construct a differential input ADC without input signal conditioning.

A successive approximation ADC is constructed with four IC's: a REF-01 +10V reference, a 2502-type successive approximation register, a CMP-01 precision voltage comparator, and a DAC-08. As shown, the circuit converts an analog input in less than 2.0μsec. For lower speed requirements, the A/D conversion logic can be the tracking or servo type consisting of up/down counters.

FOUR-QUADRANT RATIOMETRIC A/D CONVERSION BASIC CONNECTIONS

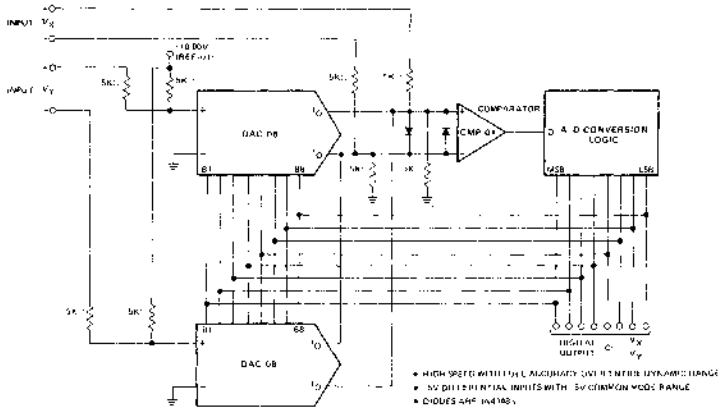


FIGURE 14

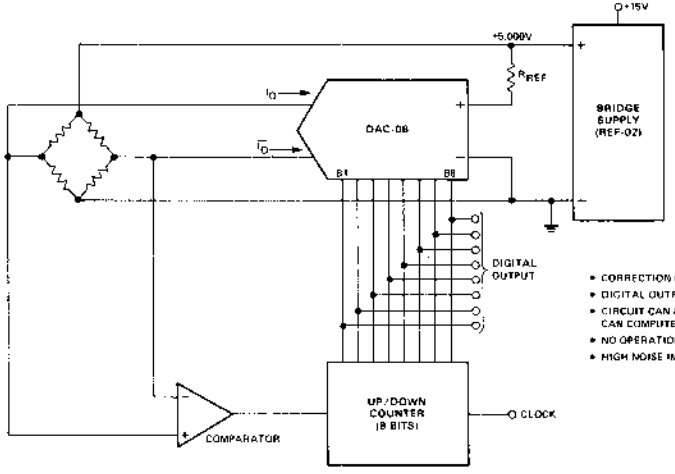
FOUR QUADRANT RATIOMETRIC A/D CONVERSION

Ratiometric A/D conversion with fully differential X and Y inputs is accomplished with the circuit in Fig. 14. Here, one set of inputs, V_X, is connected in a manner similar to the circuit in Fig. 13, and the other set of inputs, V_Y, is connected in a multiplying fashion. Operation is as follows: I_{REF} for both the upper and the lower DAC-08 is modulated between 1mA and 3mA; and the resulting output currents are differentially transformed into voltages by the 5KΩ resistors at the comparator's inputs and compared with the V_X differential input. When the conversion process is complete (comparator inputs differentially nulled to less than 1/2 LSB) a digital output is available which corresponds to the quotient of V_X/V_Y. Thus, four-quadrant ratiometric A/D conversion is achieved with four IC's and without instrumentation amplifiers.

BRIDGE TRANSDUCER NULL

In many control systems, bridges must be nulled, and a digital representation of the bridge's error must be provided for computer monitoring and control. The circuit in Fig. 15 accomplishes both tasks by using the DAC-08 complementary/differential current outputs to null the bridge with the DAC-08 connected in a tracking differential A/D converter configuration. The REF-02 reference voltage source provides both the bridge excitation voltage and the positive reference voltage for the DAC-08. Some of the advantages of this circuit are listed at the bottom of Fig. 15.

BRIDGE TRANSDUCER NULL



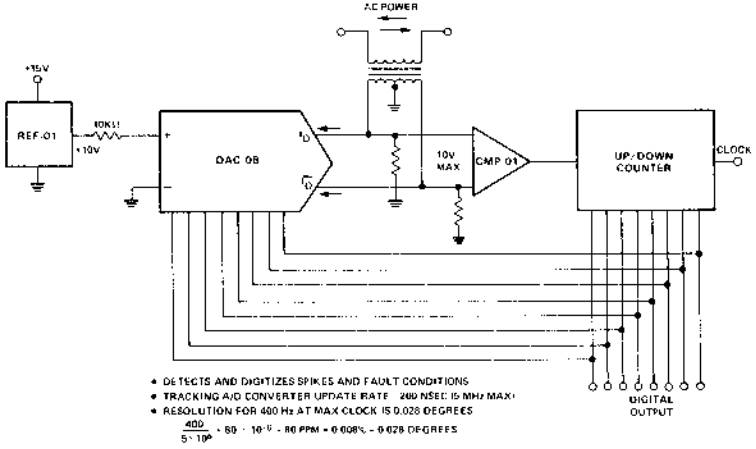
- CORRECTION CURRENT TRACKS BRIDGE SUPPLY SO NULL IS MAINTAINED
- DIGITAL OUTPUT INDICATES PREVIOUS NULLING ERROR
- CIRCUIT CAN ALSO MEASURE BRIDGE RESPONSE TO INPUT VARIABLE – PROCESSOR CAN COMPUTE DIFFERENCE WITH RESPECT TO ZERO ERROR
- NO OPERATIONAL AMPLIFIERS OR SUMMING RESISTORS ARE REQUIRED
- HIGH NOISE IMMUNITY LOGIC COMPATIBILITY (HTL, CMOS)

FIGURE 15

POWER MONITOR

Another differential current-input ADC is shown in Fig. 16 with a transformer-coupled input. An up/down counter, a precision high speed comparator, and the DAC-08 form a tracking A/D converter which continuously monitors the analog input. Two precautions must be observed: the common mode voltage at the comparator's inputs must not exceed ±10V; and the differential voltage must not exceed 11V. Voltage-limiting resistors at the comparator's inputs are recommended.

POWER FAULT MONITOR AND DETECTOR



- DETECTS AND DIGITIZES SPIKES AND FAULT CONDITIONS
- TRACKING A/D CONVERTER UPDATE RATE - 200 NSEC (5 MHz MAX)
- RESOLUTION FOR 400 Hz AT MAX CLOCK IS 0.028 DEGREES

$$\frac{400}{5 \cdot 10^6} \cdot 80 \cdot 10^{-6} \cdot 80 \text{ PPM} = 0.008\% = 0.028 \text{ DEGREES}$$

FIGURE 16

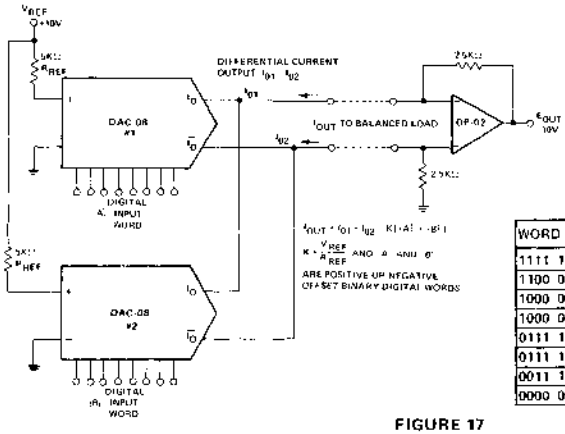
ALGEBRAIC DIGITAL COMPUTATION

Frequently, a digital arithmetic operation (addition, subtraction, multiplication, or division) must be performed, and an analog output must be provided. Traditionally, the arithmetic operations are performed with several IC's, and the output drives a D/A converter. This section describes applications of the DAC-08 as an arithmetic building block, new design approaches that reduce the number of packages required in many applications. Today's low cost, versatile DAC's merit a designer's consideration as arithmetic elements.

One benefit is not immediately apparent and deserves special mention. In all of these applications, the digital input words can be CMOS, TTL, DTL, NMOS, or MECL, because the DAC-08 interfaces with all of those logic families. In fact, the two input words may even be from different logic families to eliminate special level translators or interface circuitry. (See AN-17, "DAC-08 Applications Collection.")

The first arithmetic application is shown in Fig. 17. Two DAC-08's perform a fast algebraic summation with a direct analog output. The circuit works by paralleling the outputs of two DAC-08's and summing their currents while driving a balanced load. The output is the algebraic sum of word "A" and word "B" in all four quadrants.

FOUR-QUADRANT ALGEBRAIC DIGITAL COMPUTATION



WORD "A"	WORD "B"	I_{01}	I_{02}	E_{OUT}
1111 1111	1111 1111	3.984mA	0	+9.96V
1100 0000	1100 0000	3.000mA	0.984mA	+5.04V
1000 0001	0111 1111	2.000mA	1.984mA	+0.04V
1000 0000	0111 1111	1.992mA	1.992mA	0
0111 1111	1000 0000	1.992mA	1.992mA	0
0111 1110	1000 0000	1.984mA	2.000mA	-0.04V
0011 1111	0011 1111	0.984mA	3.000mA	-5.04V
0000 0000	0000 0000	0	3.984mA	-9.96V

FIGURE 17

FOUR-QUADRANT DIGITAL MULTIPLICATION

High speed multiplication of two 8-bit digital words with an analog output usually requires several logic packages and a D/A converter. The circuit in Fig. 18 performs this function using only three IC's.

In Fig. 18 DAC-08 number 1 and number 2 are connected as previously shown, and DAC-08 number 3 provides the analog reference inputs to DAC-08 number 1 and number 2. Those reference inputs are determined by digital input word "A." The circuit's output, I_{01}-I_{02}, is a differential current output which may be used to drive a balanced load.

Four-quadrant multiplication is thus performed by adding one more DAC-08 to the basic four-quadrant multiplying connection.

FOUR-QUADRANT 8 BIT × 8 BIT DIGITAL MULTIPLIER

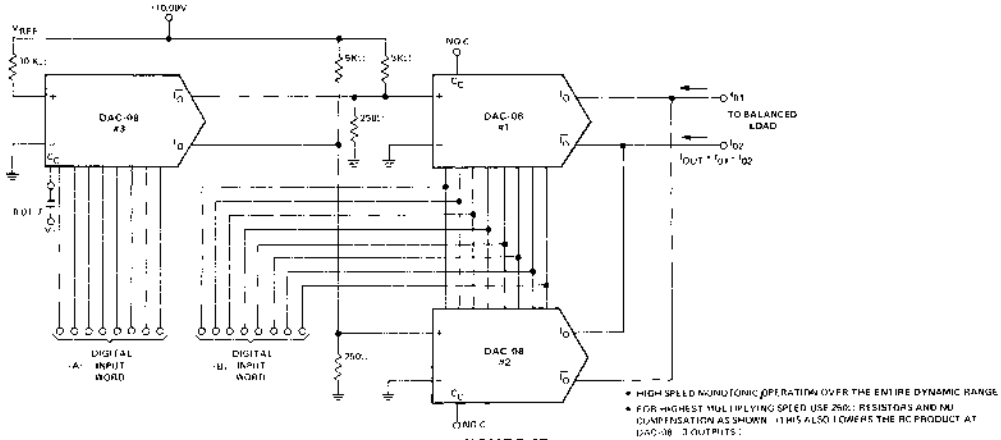


FIGURE 18

OTHER DAC APPLICATIONS

The combination of high voltage compliance complementary current outputs, universal logic inputs, and multiplying capability in a low cost DAC enables widespread application. Consider the following partial list:

A/D CONVERTERS
Tracking (Servo)
Successive Approximation
Ramp (Staircase)
Microprocessor Controlled
Ratiometric (Bridge Balancing)

TEST SYSTEMS
Transistor Tester (Force I_B and I_C)
Resistor Matching (Use both outputs)
Programmable Power Supplies
Programmable Pulse Generators
Programmable Current Source
Function Generators (ROM Drive)

ARITHMETIC OPERATIONS
Analog Division by a Digital Word
Analog Quotient of Two Digital Words
Analog Product of Two Digital Words—Squaring
Addition and Subtraction with Analog Output
Magnitude Comparison of Two Digital Words
Digital Quotient of Two Analog Variables
Arithmetic Operations with Words from Different Logic Families

GRAPHICS AND DISPLAYS
Polar to Rectangular Conversion
CRT Character Generation
Chart Recorder Driver
CRT Display Driver

DATA TRANSMISSION
Modem Transmitter
Differential Line Driver
Party Line Multiplexing of Analog Signals
Multi-level 2-Wire Data Transmission
Secure Communications (Constant Power Dissipation)

CONTROL SYSTEMS
Reference Level Generator for Setpoint Controllers
Positive Peak Detector
Negative Peak Detector
Disc Drive Head Positioner
Microfilm Head Positioner

AUDIO SYSTEMS
Digital AVC and Reverberation
Music Distribution
Organ Tone Generator
Audio Tracking A/D

CONCLUSION

Differential and multiplying applications have been described which use the high voltage compliance, complementary current outputs and the high speed multiplying inputs of the Precision Monolithics DAC-08.

BIBLIOGRAPHY

1) "DAC-08 Applications Collection"
By John Schoeff and Donn Soderquist
Precision Monolithics Application Note #AN-17, 1975

2) "Low Cost, High Speed Analog-to-Digital Conversion With the DAC-08"
By Donn Soderquist and John Schoeff
Precision Monolithics Application Note #AN-16, 1975

3) "Differential and Multiplying Use of Digital-to-Analog Converters"
By Donn Soderquist and John Schoeff
E.E. Times article, June 21, 1976, pp. 40-47

EXPONENTIAL DIGITALLY CONTROLLED OSCILLATOR USING DAC-76

by
Donn Soderquist

Here is a 4-IC, microprocessor-controlled oscillator with a 8159 to 1 frequency range covering 2.5Hz to 20KHz. An exponential, current output IC DAC functioning as a programmable current source alternately charges and discharges a capacitor between precisely-controlled upper and lower limits. This circuit features instantaneous frequency change, operates with +5V ±1V and -15V ±3V supplies, and provides monotonic frequency changes over a 78dB range – the dynamic range of a 13-bit DAC.

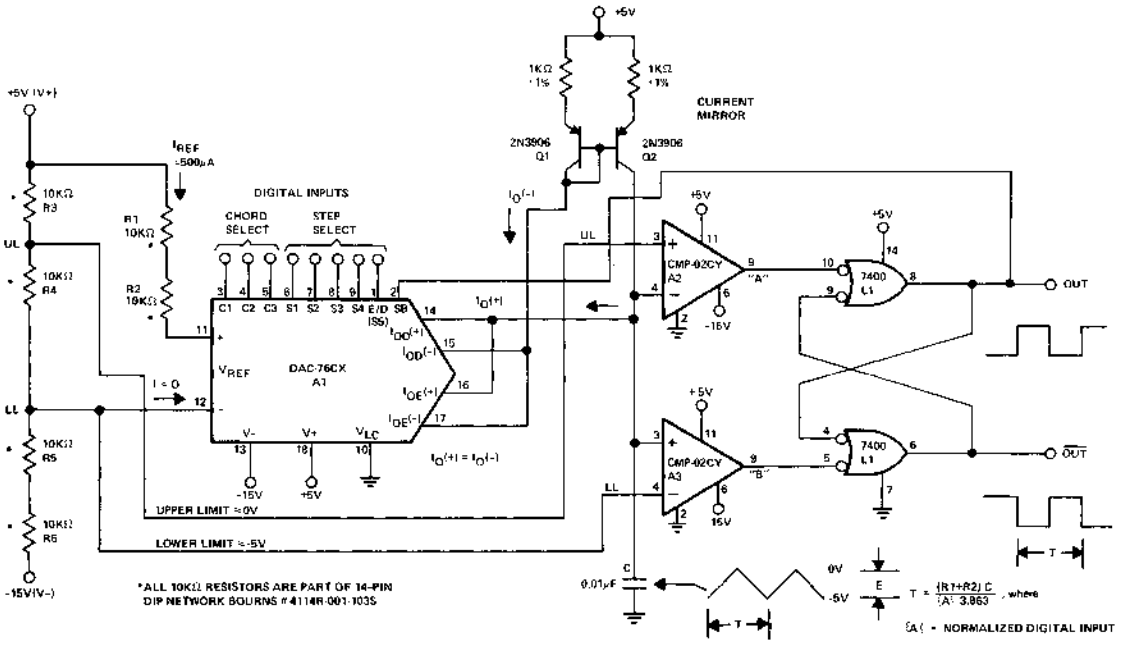
BASIC OPERATION

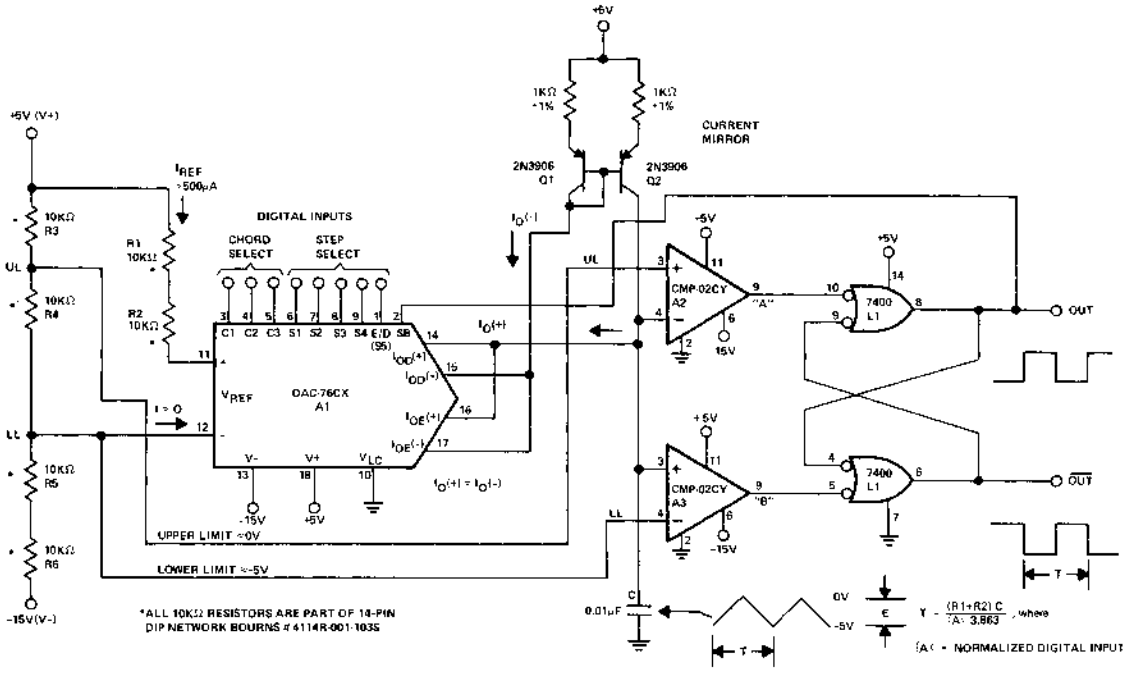
Connected as shown in Fig. 1, the output of the exponential DAC is an 8-chord (or segment) current ranging between 250nA and 2.0mA. The three most significant bits select 1 of 8 binarily-related chords; and the five least significant bits select 1 of 32 linear steps within each chord. This current is switched between the $I_0(+)$ output and the $I_0(-)$ output under the control of a pin labeled SB.

When SB is low, $I_0(-)$ is selected, and the DAC's output current drives a current mirror which ramps the timing capacitor in a positive direction until an upper limit of 0V is sensed by A2. At this time the set-reset flip-flop (L1) is set, SB becomes a "1", and the DAC's output current is switched to the $I_0(+)$ output. Now the capacitor is charged to a lower limit of -5V, the flip-flop is reset, and the cycle repeats itself.

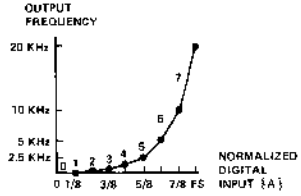
REFERENCE SETUP

The multiplying relationship between the reference current, I_{REF}, and the full scale output of the DAC is 3.863. I_{REF} is set by the voltage between V+ and the lower limit divided by R1+R2. This is so because pin 12, $V_{REF}(-)$, is a high impedance input, namely the noninverting input of an op amp internal to the DAC. Since both I_{REF} and the upper and lower limits are derived by dividing down the power supply voltages, operation (frequency of oscillation) is independent of power supply changes. (See Appendix 1 for a complete derivation of the timing formula.)





OSCILLATOR TRANSFER FUNCTION



WAVEFORMS

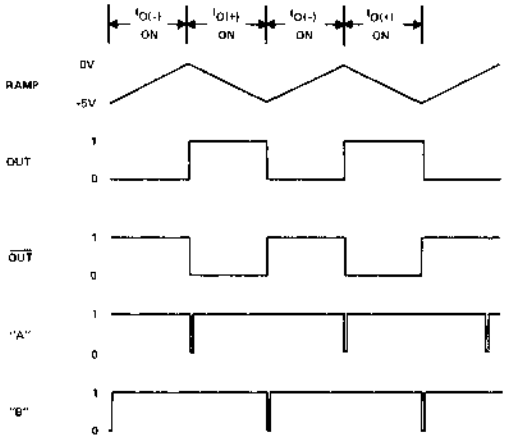


TABLE I
IDEAL OUTPUT FREQUENCY

CHORD (SEGMENT)	DIGITAL INPUT CODE	NORMALIZED DIGITAL INPUT |A|	OUTPUT FREQUENCY	AVERAGE STEP SIZE
0	000 00001	$\frac{1}{8159}$	2.45Hz	2.3Hz
	000 01000	$\frac{8}{8159}$	19.6Hz	
	000 11111	$\frac{31}{8159}$	76.0Hz	
1	001 00000	$\frac{33}{8159}$	80.9Hz	4.8Hz
	001 11111	$\frac{95}{8159}$	233Hz	
2	010 00000	$\frac{99}{8159}$	243Hz	9.5Hz
	010 11111	$\frac{223}{8159}$	547Hz	
3	011 00000	$\frac{231}{8159}$	566Hz	19Hz
	011 11111	$\frac{479}{8159}$	1.17KHz	
4	100 00000	$\frac{495}{8159}$	1.21KHz	38Hz
	100 11111	$\frac{991}{8159}$	2.43KHz	
5	101 00000	$\frac{1023}{8159}$	2.51KHz	76Hz
	101 11111	$\frac{2015}{8159}$	4.94KHz	
6	110 00000	$\frac{2079}{8159}$	5.09KHz	152Hz
	110 11111	$\frac{4063}{8159}$	9.96KHz	
7	111 00000	$\frac{4191}{8159}$	10.3KHz	303Hz
	111 11111	$\frac{8159}{8159}$ = FS	20.0KHz	

FREQUENCY SELECTION

Table I lists ideal output frequencies at the lowest and highest codes of each chord and the average change in frequency produced by a one step change (LSB change) within each chord. For highest accuracy in Chord 0, especially between 2.5Hz and 19.6Hz, comparators with low input current are recommended. The CMP-02CY comparators typically have 35nA of input current; at the lowest code point (000 00001) the DAC output is 250nA; so low input current comparators are essential for best operation. Above 000 01000 (4μA or 19.6Hz) the comparator input currents become less critical.

CONCLUSION

A microprocessor-controlled oscillator has been shown which achieves a 13-bit dynamic range with only 8 bits of control. Monotonic frequency steps over 2.5Hz to 20KHz are provided in a 4-IC low cost design.

REFERENCE

"Eight-Bit Frequency Source Suited for μP Control" by Albert Helfrick, EDN, September 20, 1976, pp. 116-118.

APPENDIX

TIMING EQUATION DERIVATIONS

One of the best features of this design is its insensitivity to power supply changes. The equation derivations are shown to explain how V+ and V- drop out as timing determinations.

With a constant current drive the charge on C changes linearly over a range (E) between an upper limit (UL) and a lower limit (LL) dependent upon the DAC's digital input code, the DAC's output current, and the value of the timing capacitor (C).

Eq. 1) $T = 2\left(\frac{CE}{I}\right)$ where: C = timing capacitor value
E = upper limit – lower limit
I = DAC output current, $I_0(+)$ or $I_0(-)$
T = period

Eq. 2) E = UL - LL where: UL = upper limit
LL = lower limit

Eq. 3) $UL = \frac{R4+R5+R6}{R3+R4+R5+R6}\left[(V+)-(V-)\right]+(V-)$

where: V+ = positive power supply and V- = negative power supply
but: R3=R4=R5=R6

$\therefore UL = \frac{3(V+)+(V-)}{4}$

Eq. 4) $LL = \frac{R5+R6}{R3+R4+R5+R6}\left[(V+)-(V-)\right]+(V-)$

$LL = \frac{(V+)+(V-)}{2}$

Substituting 3 and 4 into 2 and solving for E:

Eq. 5) $E = \frac{(V+)-(V-)}{4}$

Rewriting Eq. 1 and substituting 5:

Eq. 6) $\frac{T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{I}$

The expression for I is:

Eq. 7) $I = 3.863\{A\}I_{REF}$

where: 3.863 is a constant derived from the ratio of I_{REF} to $I_{FULL\ SCALE}$ of the DAC
A = the normalized digital input code
I_{REF} = the reference current

Eq. 8) $I_{REF} = \frac{(V+)-LL}{R1+R2}$

Substituting 4 into 8:

Eq. 9) $I_{REF} = \frac{(V+)-\left[\frac{(V+)+(V-)}{2}\right]}{R1+R2}$

$= \frac{(V+)-(V-)}{2(R1+R2)}$

Substituting 9 and 7 into 6:

Eq. 10) $\frac{T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{3.863\{A\}\left[\frac{(V+)-(V-)}{2(R1+R2)}\right]}$

Multiplying by $\{A\}$ 3.863:

Eq. 11) $\frac{\{A\}3.863T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{\frac{(V+)-(V-)}{2(R1+R2)}}$

$\frac{\{A\}3.863T}{2C} = \frac{R1+R2}{2}$

So, V+ and V- have dropped out as timing considerations.

Solving for T:

Eq 12) $T = \frac{C(R1+R2)}{3.863\{A\}}$ but: C = 0.01μF
R1 = R2 = 10KΩ

Eq. 13) $T = \frac{5.177\times10^{-5}}{\{A\}}$

Finally, the simplified expressions:

Eq. 14) $T \cong \frac{50\mu sec}{\{A\}}$

Eq. 15) f (frequency) $\cong \frac{\{A\}}{50\times10^{-6}} \cong$ 20KHz full scale

3 IC 8 BIT BINARY DIGITAL TO PROCESS CURRENT CONVERTER WITH 4 - 20MA OUTPUT

by
Donn Soderquist

This application note describes a 3 IC, 4 - 20mA process current, digital to analog converter that can be constructed for less than $20 at current 100+ prices. It operates from a -5V ±1V negative power supply and a +23V ±7V positive power supply, has 24V output voltage compliance, and occupies less than 4 square inches of printed circuit board space. Other significant features include TTL logic input compatibility, 8-bit binary coding, 0° to +70° C operation, and 5μsec full scale settling time into a 500Ω load.

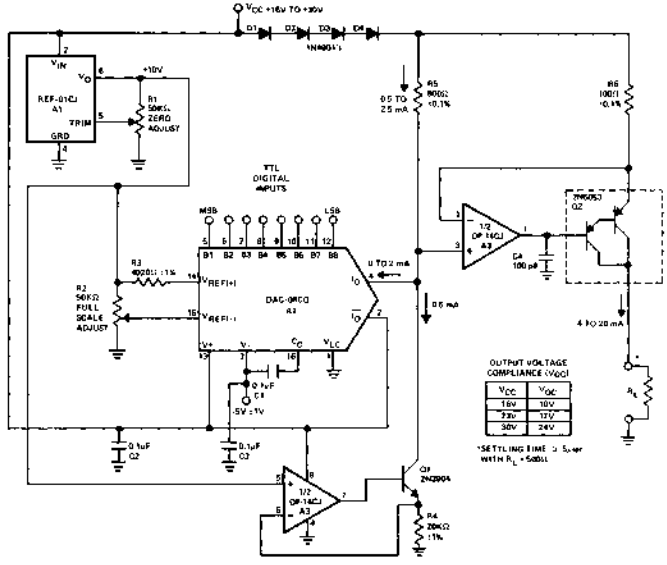
THEORY OF OPERATION

A fixed current of 0.5mA is added to a DAC's output current varying between 0 and 2.0mA and the resulting total current is multiplied by a factor of 8 to produce an output current of 4.0 to 20mA.

In the schematic, first note the REF-01CJ, a +10V adjustable reference. Its output goes to the noninverting input of ½ of A3, a dual precision op amp. The inverting input is within a feedback loop forcing +10V to appear at the top of R4, a 20KΩ resistor; a 0.5mA current will flow in R4 through Q1, a high h_{FE} transistor. The same +10V is applied to R3, the reference input resistor of a multiplying IC D/A converter, the DAC-08. Full scale output current of the DAC will be the difference in voltage between the +10V reference and pin 14 of the DAC divided by R3; pin 15 will be at the same voltage as pin 14 because it is a high impedance point, the noninverting input of an op amp internal to the DAC. After calibration a current of 0 to 2mA (depending on the digital input code) will flow into the DAC's output, pin 4.

Both the DAC's output current and the fixed 0.5mA flow in R5, a 800Ω precision resistor. The voltage developed by that current is applied to the noninverting input of the other ½ of A3 and will also appear across R6, a 100Ω precision resistor. Thus, 8 times the 0.5 to 2.5mA current in R5 flows in R6, or 4 to 20mA. Almost all of this current appears at the output because the 2N6053 is a high h_{FE} device, a power darlington transistor.

Some other components need explanation. C1 provides frequency compensation of the DAC's reference amplifier; C2 and C3 are power supply decoupling (bypass) capacitors; C4 prevents high frequency oscillations. D1 through D4 insure at least 2.5V differential between the op amp's inputs and its positive power supply under all conditions. R1 and R2 are zero scale and full scale adjustments respectively.



CALIBRATION PROCEDURE

Apply +23V ±7V and -5V ±1V to the converter with a current-measuring meter connected between the output and ground. Make the digital inputs all zeros, < +0.8V. Adjust R1 until the output current is 4.0mA. Now change the digital inputs to all ones, > +2.0V. Adjust R2 until the output current is 20mA. Calibration is now completed.

OUTPUT VOLTAGE COMPLIANCE

Output voltage compliance is V_{cc} -6V. For example, at V_{cc} = +16V, the output may go to a maximum of +10V without affecting output current. Thus, a 500Ω resistor would be the maximum load resistor at V_{cc} = +16V. At V_{cc} = +30V, V_{oc} = 24V, and R_L Max = 1.2KΩ.

SCALE MODIFICATION .

Although the values shown are for the more common 4-20mA requirement, operation at 1-5mA or 10-50mA may be achieved by changing some components. For 10-50mA, change R6 to 40Ω; this makes the multiplying factor 20 instead of 8. For 1-5mA, replace the 2N6053 with a 2N5087, and change R6 to 400Ω.

CONCLUSION

A simple, low cost process current converter has been shown with wide application in the controls industry. The design is tolerant of wide power supply variations, has high voltage compliance, and is easily calibrated. Reliability and cost are optimized by using only 3 integrated circuits, the Precision Monolithics DAC-08, REF-01, and OP-14, plus a few readily available discrete components.

REFERENCE

Crowley, B., "Circuit Converts Voltages to 4-20mA For Industrial Control Loops," Electronic Design, Jan. 5, 1976, p. 116.

PARTS LIST

Circuit Symbol(s)	Description
A1	+10V Reference, PMI REF-01CJ
A2	8 Bit DAC, PMI DAC-08CQ
A3	Dual Op Amp, PMI OP-14CJ
C1-C3	0.1μF +80%/-20% 50V, Type CK-104
C4	100pF ±5% Mica, DM10ED101J03
D1-D4	Power Diode, 1N4001
Q1	NPN Transistor, 2N3904
Q2	PNP Power Darlington, Motorola 2N6053
R1-R2	50KΩ Potentiometer, Bourns #3006P-1-503
R3	4020Ω ±1%, RN55C4021F
R4	20KΩ ±1%, RN55C2002F
R5	800Ω ±0.1%, GR #8E16D800
R6	100Ω ±0.1%, GR #8E16D100

SOFTWARE CONTROLLED ANALOG TO DIGITAL CONVERSION USING DAC-08 AND THE 8080A MICROPROCESSOR

by
Will Ritmanich and Wes Freeman

The microprocessor is generally regarded as a flexible replacement for discrete logic devices. Yet most microprocessor-based designs still use numerous isolation and support packages for analog to digital (A/D) conversion, rather than using just software and the processor itself. There are many applications where the minimum system approach is both desirable and feasible. This application note describes a very simple, low cost method of software controlled 8-bit A/D conversion using the Precision Monolithics DAC-08 and the Intel 8080A. Innovative software eliminates the need for peripheral isolation devices. Easily expandable to 10-bit or 12-bit A/D conversions, the technique may be emulated using other microprocessors having separate address and data busses.

8080A I/O INTERFACE CONSIDERATIONS

In order to communicate with any input/output peripheral device, the 8080A must be able to distinguish between its normal memory array and that particular I/O peripheral. Two techniques exist for accomplishing this, each with its own set of advantages and disadvantages.

The basic approach, used especially in large systems requiring greater than 32K memory, assigns the particular peripheral to an I/O "Port." This has the effect of isolating the I/O from the memory bus by the use of additional interface devices (generally the 8255 Programmable Peripheral Interface). Data transfers to and from the peripheral are then enabled by special instructions IN or OUT. This method has the advantage of allowing full 65K memory usage (Figure 1), but requires additional support circuits. Although conceptually simple, it restricts communication to the peripheral through the 8080A Accumulator.

For simple applications or where the full memory addressing capability of the 8080A is not needed, a powerful technique referred to as "Memory-mapped I/O" can be implemented. By utilizing unused portions of memory address space for I/O operations, the full instruction set used to control memory can also be used to operate on peripherals. This creates a powerful "new" capability for dealing with I/O. The major constraint, however, is that the peripheral must now conform to memory bus signals and timing.

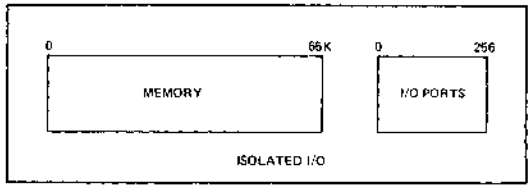


FIGURE 1

I/O CONTROL USING MEMORY MAPPING

The convention used in establishing memory mapped I/O is to assign address line A_{15} as the I/O control flag. Thus, if A_{15} is "zero," then memory is active, and if A_{15} is "one" then I/O is active. This creates a "map" of the memory as shown in Figure 2. Although other address lines could be used for the function, A_{15} is normally used because it is easier to control with software and allows full address capability for the lower 32K of memory.

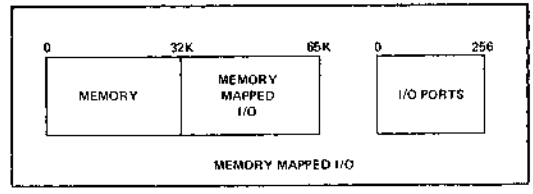


FIGURE 2

MEMORY MAPPED I/O CONTROL SIGNALS

In order to manipulate memory-mapped I/O, it is necessary to generate the appropriate control signals. This is accomplished by gating $\overline{MEMR}$ and $\overline{MEMW}$ with A_{15} as shown in Figure 3. System bus characteristics are preserved and all instructions normally used to operate on memory can now be used on I/O as well.

I/O CONTROL SIGNAL GENERATION

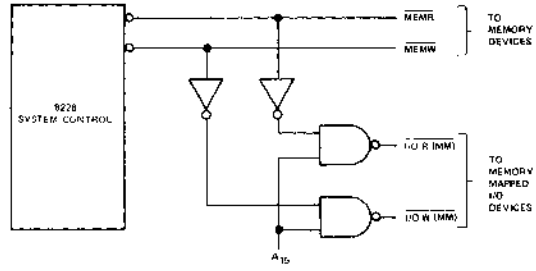


FIGURE 3

SUCCESSIVE APPROXIMATION A/D CONVERSION

Because it provides the best tradeoff between speed and hardware/software complexity, the successive approximation method of A/D conversion has been selected. Figure 4 shows a simple analogy of this approach based on the use of a pan balance.

SUCCESSIVE APPROXIMATIONS ANALOGY

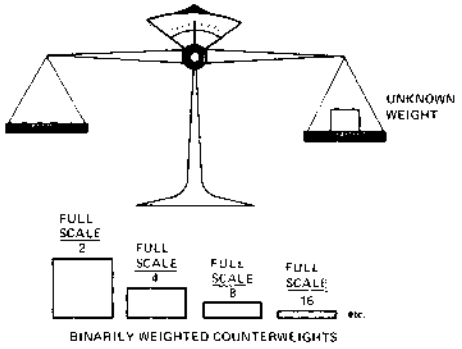


FIGURE 4

To measure some unknown weight, it is placed on one pan of the balance. By successively applying binarily-weighted counterweights to the other pan until the scale is balanced, we can ascertain the portion of the unknown weight compared to that of the known full scale weight. The number of "trials" is made equal to the number of counterweights available by starting with the heaviest counterweight first, and either retaining it or rejecting it based on the comparison to the unknown. This process is repeated for the next heaviest and so on, until all weights have been tried.

Electrically, this can be simulated by sequential comparisons between the output of a digital to analog converter and some unknown analog input. Figure 5 shows the basic circuit configuration.

BASIC SUCCESSIVE APPROXIMATION CIRCUIT

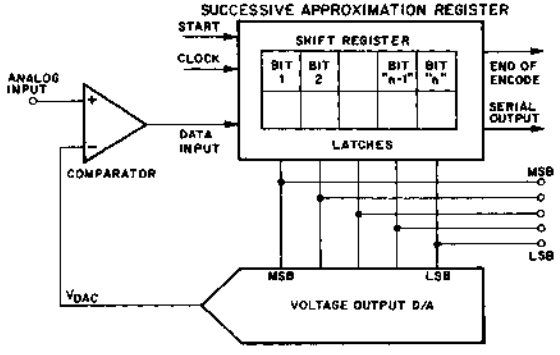


FIGURE 5

At the start of a conversion, the most significant bit (MSB) of the DAC is turned on by the Successive Approximation Register (SAR) producing an output from the DAC equal to one-half full scale. The DAC's output is compared to the analog input by a comparator, and if the DAC output is greater than the unknown input voltage, the MSB is turned off. If, however, the DAC output is less than the unknown input, the MSB is allowed to remain on, and the next most significant bit is tried. Whether or not this second bit should remain on or be turned off is subject to the same criteria as before (Figure 6). This basic procedure is used to test all remaining DAC bit inputs.

FLOW DIAGRAM FOR 3 BIT SUCCESSIVE APPROXIMATION A/D CONVERSION

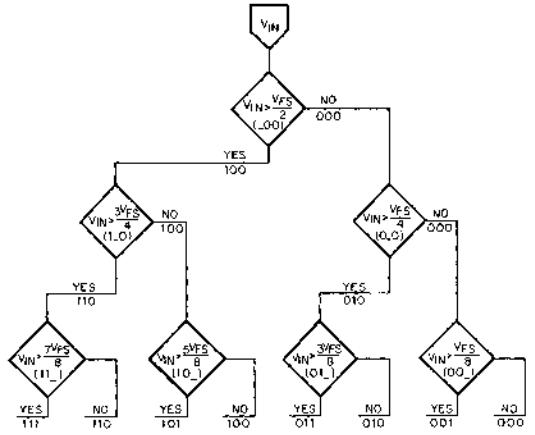


FIGURE 6

LOGIC REPLACEMENT BY THE 8080A

The circuit illustrated in Figure 5 can be simplified by utilizing the logic capability of the 8080A to replace the SAR. The eight lowest order address bits control the data bit inputs to the DAC-08 (Figure 7). Table 1 contains the software used to accomplish this. Figure 8 depicts the corresponding flow diagram.

```
;DAC 08 A/D CONVERSION ROUTINE

START:  LXI   B,08000H  ;LOAD MSB IN B,CLEAR C
        MOV   A,B       ;MSB TO ACC
        MOV   H,A       ;SET MEM/MAP I/O
TEST:   ORA   C         ;ADD LAST TEST VALUE
        MOV   L,A       ;MOVE PRESENT TEST TO L
        MOV   A,M       ;GET COMP OUTPUT
        ANA   A         ;SET FLAGS
        JPO   TOOHI     ;DISCARD PRESENT TEST BIT
        MOV   A,B       ;GET PRESENT TEST BIT
        ORA   C         ;ADD TOTAL SO FAR
        MOV   C,A       ;SAVE TOTAL
TOOHI:  MOV   A,B       ;GET LAST TEST BIT
        RAR             ;ROTATE TOWARD LSB
        MOV   B,A       ;SAVE NEW TEST BIT
        JNC   TEST      ;JUMP IF NOT FINISH
        END             ;FINAL VALUE IS IN C
```

TABLE 1

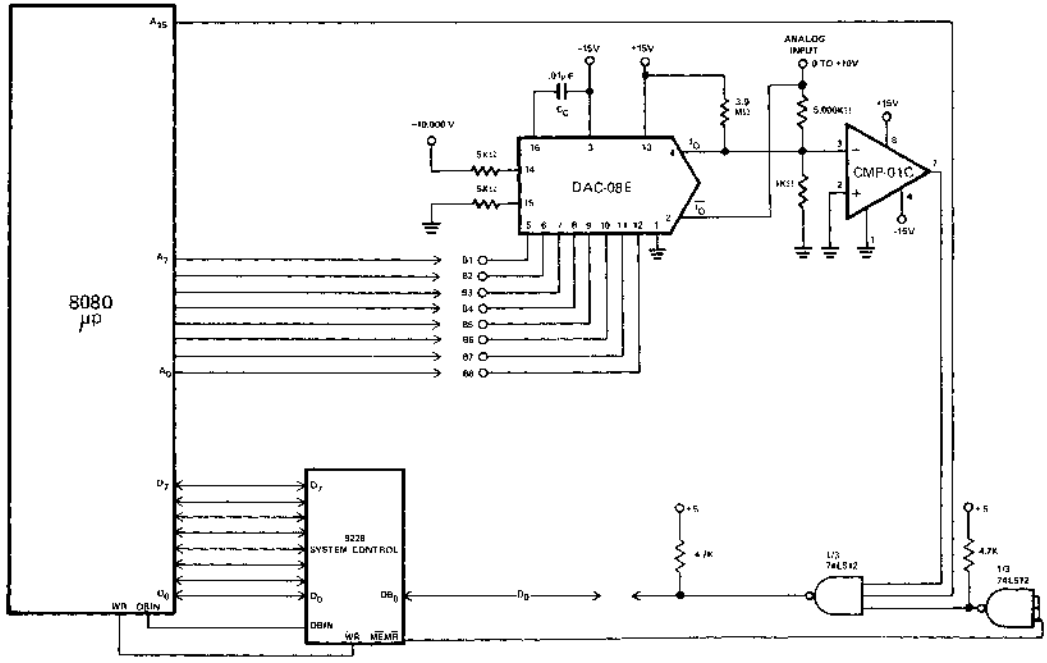


FIGURE 7

This technique accesses the DAC as a 256 X 1 ROM. Conversion time, hardware interface, and program length are minimized due to the fast settling time of the DAC-08 and CMP-01 combination, which is less than the processor cycle time (Figure 9). No "wait" states or (NOP) instructions are required for execution of the program.

The instruction (MOV L, A) moves the test value to the "L" (memory address) register, which controls the 8 lowest order address bits, establishing the trial bit value to the DAC. The applied analog input current is compared to the DAC output current by the CMP-01. The (MOV A, M) instruction gates the trial comparison results provided by the CMP-01 into the 8080A Accumulator. The processor then continues to perform the logical operations required to accomplish the analog to digital conversion. It requires 21 bytes of memory with an 8-bit conversion time ranging from 235 to 285 μsec using a 2.0 MHZ clock. The time varies slightly depending on the analog input, because extra program steps are required if the trial bit must be saved. Quantizing is performed over an analog input range of 0 to +10 volts, although other user-selected encoding ranges can also be used.

EXPANSION

This technique may also be used for A/D conversions of 10 or 12 bits by simply connecting the DAC MSB inputs to the corresponding address lines. The hardware and software savings show a very marked increase because multiple latches and extensive software byte moving operations are eliminated. Thus, for a 10-bit A/D conversion, the DAC "appears" to the 8080A as a 1024 X 1 ROM; a 12-bit DAC "appears" as a 4096 X 1 ROM. In general, the settling time of a 10-bit or 12-bit DAC is greater than the cycle time of the 8080A; however, by using the 8080A READY line to insert "wait" states, the settling time of any DAC can be accommodated.

SOFTWARE CONTROLLED A/D CONVERSION

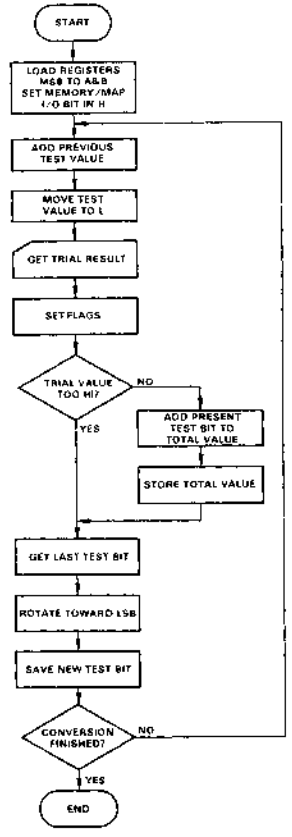
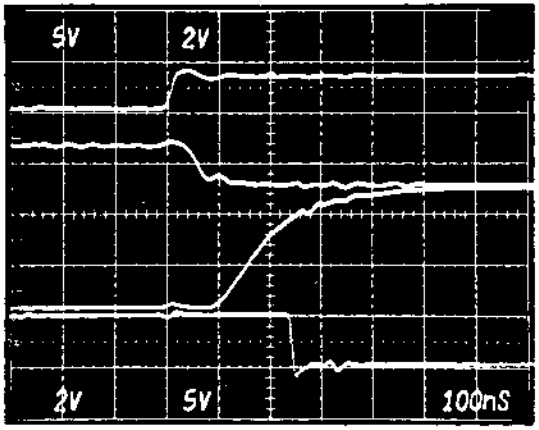


FIGURE 8



TOP TRACE: A15

2ND TRACE: DAC-08 PIN 4

3RD TRACE: CMP-01 OUTPUT

BOTTOM TRACE: 74LS12 OUTPUT

FIGURE 9

CONCLUSION

A low cost A/D conversion technique using DAC-08 and the 8080A microprocessor has been presented. Implementation requires a minimal allocation of memory for program software and very few interface components. The technique permits expansion to control 10-bit or 12-bit A/D conversions.

BIBLIOGRAPHY

1.) "8080 Microcomputer Systems Users Manual," Intel Corporation 9/75.

2.) "A/D Conversion Systems: Let your μP do the Working" by Don Aldridge, EDN, 5/5/76, pp 75-80.

3.) "Low Cost, High Speed Analog to Digital Conversion with the DAC-08," Precision Monolithics Application Note AN-16.

Application Notes

AN-23

DIGITAL-TO-ANALOG CONVERTER GENERATES HYPERBOLIC FUNCTIONS

by
Will Ritmanich, Bob Blair, and Bob Debowey

Measurement and control systems frequently require fine resolution around a setpoint with wide dynamic ranging capability. This can be satisfied by systems designs which use a high resolution, strictly linear approach; but this is costly and often unnecessary. Nonlinear function fitting using multiplying digital-to-analog converters (DAC's) offers a desirable alternative by being both simpler and more cost-effective. This application note describes how extended range hyperbolic functions of the type A/X or –A/X (where "A" indicates an analog constant, while "X" represents a decimally-expressed digital divisor) are easily generated by just two low-cost I.C.'s; an operational amplifier and a multiplying DAC. Circuit configurations are provided for each polarity output along with dynamic performance photographs and general design guidelines for either binary or BCD-coded divisors. At current prices (100+) the configurations shown can be built for less than $10.

THEORY OF OPERATION (A/X)

Figure 1a shows the A/X function circuit which uses a two-digit BCD-coded DAC, the DAC-20EX, and a decompensated, wide-bandwidth op-amp, the OP-17. A constant current, I constant, equal to the value of one least significant bit (LSB), flows into the DAC output terminal, I_O. Simultaneous adjustment of the scale factor and output amplifier offset voltage is enabled by a multi-turn, low tempco potentiometer, R5, which adjusts current $-I_R$ producing voltage $-V_R$ across R2. The LSB value (scale factor) equals $-V_R/R1$.

Zener diode, D_Z, provides a stable reference voltage source. Because feedback for the op amp is through the DAC, capacitors C1 and C2 are added to provide proper phase compensation. Reference resistor R3 is determined by the scale factor and the maximum current allowed into the DAC reference input V_R+. Bias current compensation for the DAC reference amplifier is accomplished by R4.

Figures 1b, 1c, and 1d show dynamic performance of circuit 1a when the digital inputs are swept by an external BCD up-counter with codes of 0000 0001 through 1001 1001 (division by zero is not allowed).

THEORY OF OPERATION (–A/X)

The circuit configuration for the –A/X function is shown in figure 2a. It is quite similar to that of figure 1a with both the DAC reference amplifier and output amplifier terminals reversed. Capacitors C1 and C2 provide phase compensation. Figures 2b, 2c, and 2d show dynamic performance of circuit 2a.

DESIGN CONSIDERATIONS

1) Circuit speed and settling time are dictated by output op amp slew rate, scale factor, and compensation. Use of slower amplifiers considerably increases the illustrated settling times. Effective slew rate of circuit 1a is 3V/μs, while circuit 2a slews 0.6V/μs.

2) Layout and breadboarding of high gain, wide-bandwidth devices necessitates considerable care with a ground plane with single point grounding being highly desirable. Decoupling capacitors located close to the devices' supply inputs are essential.

3) Accuracy of the circuit is within 1% over the 0°C to +70°C temperature range with 1% metal film resistors R1, R2 and R3. DAC linearity becomes an important factor as the divisor decreases; for this reason 1/4 LSB linear DAC's are recommended.

4) Binary coding may be accomplished by subsituting an 8-bit binary-coded DAC-08EX for the two-digit BCD-coded DAC-20EX. In addition to adjusting circuit values however, a higher performance op amp such as the OP-17F is desirable because the output amplifier's input offset voltage drift becomes a more significant error source for overall scale factor stability over temperature. This is due to the increased resolution of the binary coding.

A/X FUNCTION GENERATOR

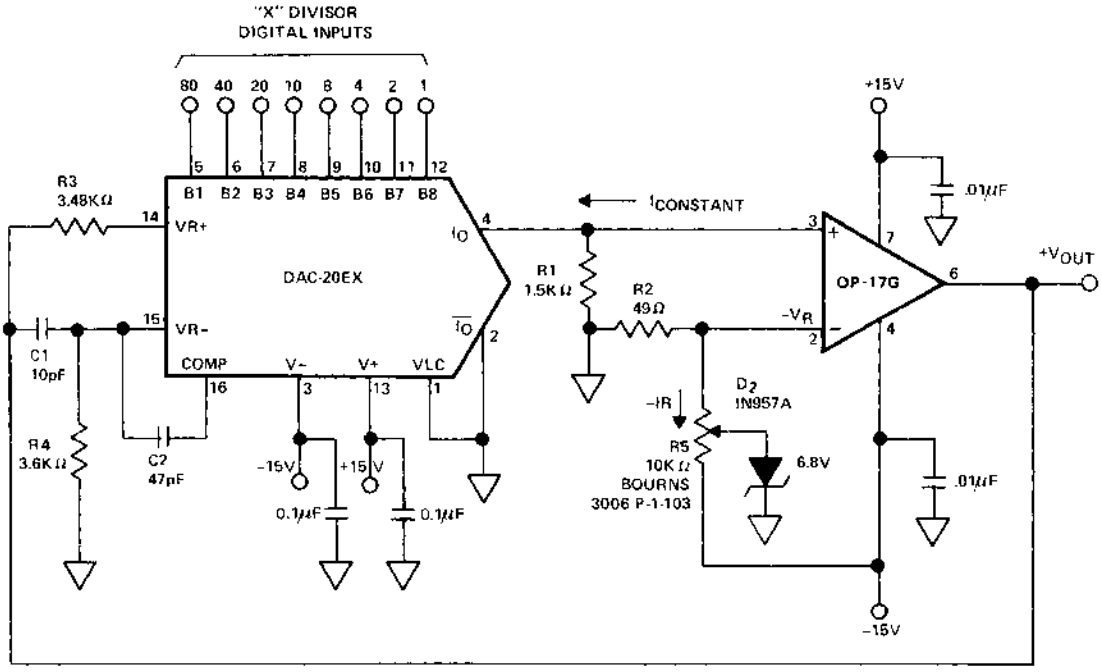


FIGURE 1a

R_1, R_2, R_3 = 1% METAL FILM
ALL CAPS = CERAMIC DISC

GROUND PLANE

A/X FUNCTION GENERATOR

$$I_{constant} = \text{LSB value} = \frac{-V_R}{R_1}$$

$$-V_R = -I_R \cdot R_2$$

$$A \approx I_{constant} \cdot R_3 \cdot X_{FS}$$

$$V_{OUT} \approx \frac{I_{constant} \cdot R_3 \cdot X_{FS}}{X_{div}}$$

where X_{FS} = decimal equivalent of full scale counts

and X_{div} = decimal equivalent of desired divisor

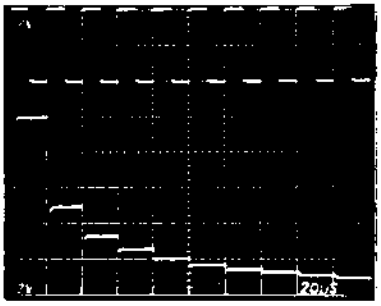


FIGURE 1b

TOP TRACE = CLOCK

LOWER TRACE = $\frac{A}{1}$ THRU $\frac{A}{10}$

(CODES 0000 0001 THRU 0001 0000)

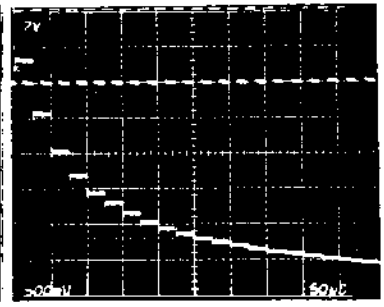


FIGURE 1c

TOP TRACE = CLOCK

LOWER TRACE = $\frac{A}{3}$ THRU $\frac{A}{22}$

(CODES 0000 0011 THRU 0010 0010)

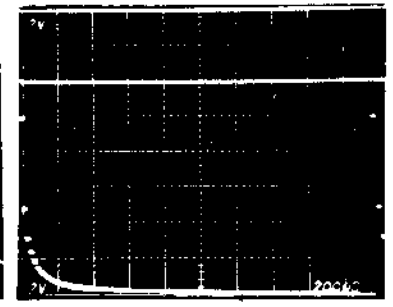


FIGURE 1d

TOP TRACE = CLOCK

LOWER TRACE = $\frac{A}{1}$ THRU $\frac{A}{99}$

(CODES 0000 0001 THRU 1001 1001)

— A/X FUNCTION GENERATOR

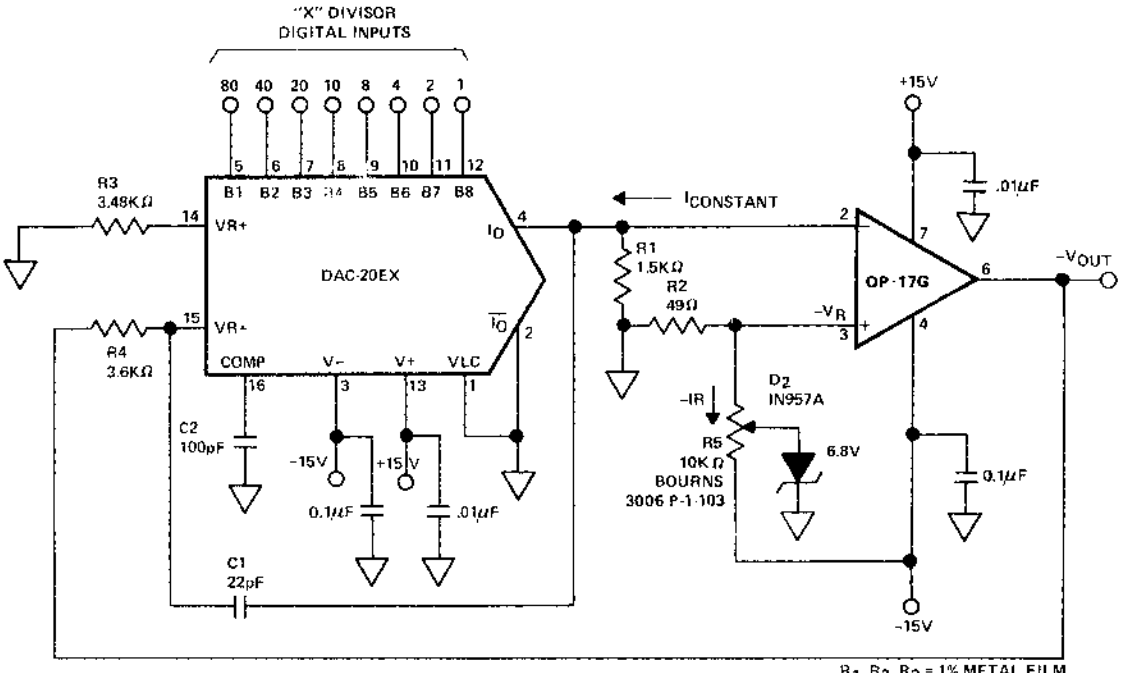


FIGURE 2a

GROUND PLANE

-A/X FUNCTION GENERATOR

$$I_{constant} = \text{LSB value} = \frac{-V_R}{R_1}$$

$$-V_R = -I_R \cdot R_2$$

$$A \approx I_{constant} \cdot R_3 \cdot X_{FS}$$

$$V_{OUT} \approx \frac{I_{constant} \cdot R_3 \cdot X_{FS}}{X_{div}}$$

where X_{FS} = decimal equivalent of full scale counts

and X_{div} = decimal equivalent of desired divisor

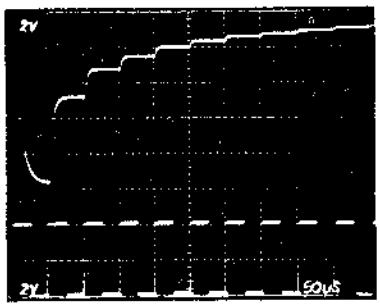


FIGURE 2b

LOWER TRACE = CLOCK

TOP TRACE = $\frac{-A}{1}$ THRU $\frac{-A}{10}$

(CODES 0000 0001 THRU 0001 0000)

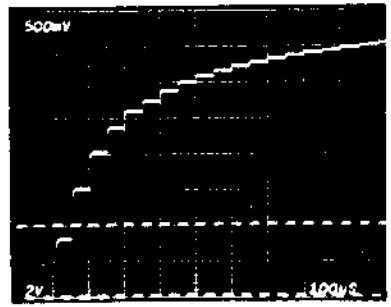


FIGURE 2c

LOWER TRACE = CLOCK

TOP TRACE = $\frac{-A}{3}$ THRU $\frac{-A}{20}$

(CODES 0000 0011 THRU 0010 0000)

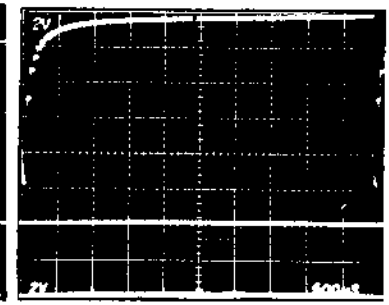


FIGURE 2d

LOWER TRACE = CLOCK

TOP TRACE = $\frac{-A}{1}$ THRU $\frac{-A}{99}$

(CODES 0000 0001 THRU 1001 1001)

SUMMARY

Simple, low cost circuits which generate the hyperbolic functions A/X and -A/X have been presented, together with design guidelines for either binary or BCD-coded divisors.

Application Notes

AN-24

THE OP-17, OP-16, OP-15 AS OUTPUT AMPLIFIERS FOR HIGH SPEED D/A CONVERTERS

by George Erdi

This application note shows how to make high speed, voltage output D/A converters using the DAC-08 and OP-15/16/17 precision bifet op amps. Designs are optimized for highest speed (OP-17), lowest drift (OP-16) and for lowest power (OP-15). Although the DAC-08 is used as an example, the same configurations work with DAC-20 and DAC-76.

Converting the current output of a fast IC DAC to a voltage while maintaining fast settling time is difficult. The full scale current of the DAC-08 settles in 85nsec. It can be terminated with a load resistance, as shown in Figure 1, to give a 10V output. However, in this configuration the settling time will be dominated by the RC time constant of R_1 and the DAC-08's output capacitance ($T=R_1C_O=5K\Omega \times 15pF = 75nsec$). It requires 6.2 time constants to settle within 0.2% of full scale (1/2 least significant bit of an 8 bit converter). Therefore, the settling time is 500nsec including the DAC-08's 35nsec propagation delay.

Due to this RC time constant, current to voltage conversion is usually accomplished with a transimpedance amplifier as shown in Figure 2. The output's response is now limited by the amplifier's slew rate and settling time. However, an additional pole is introduced at $\frac{1}{2\pi R_2 C_1}$, where C_1 is the sum of the DAC's output capacitance and the op amp's input capacitance. The frequency of this pole is likely to be at an inopportune location for fast amplifiers, creating an underdamped response or even oscillation.

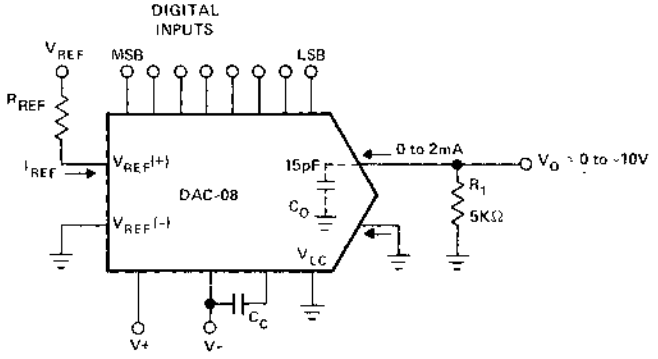


FIGURE 1
DAC-08 WITH RESISTIVE TERMINATION
SETTLING TIME = 500 nsec FOR 0 TO -10V

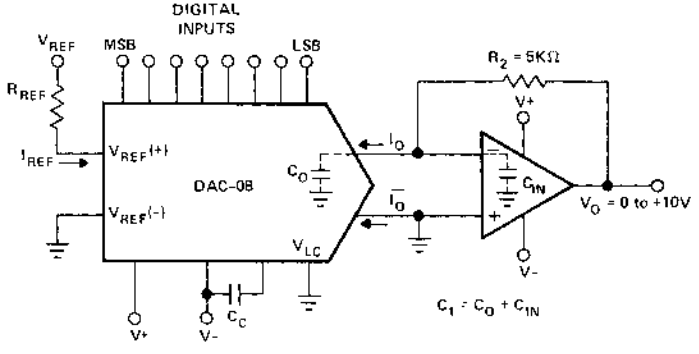


FIGURE 2
VOLTAGE OUTPUT DAC WITH TRANSIMPEDANCE AMPLIFIER

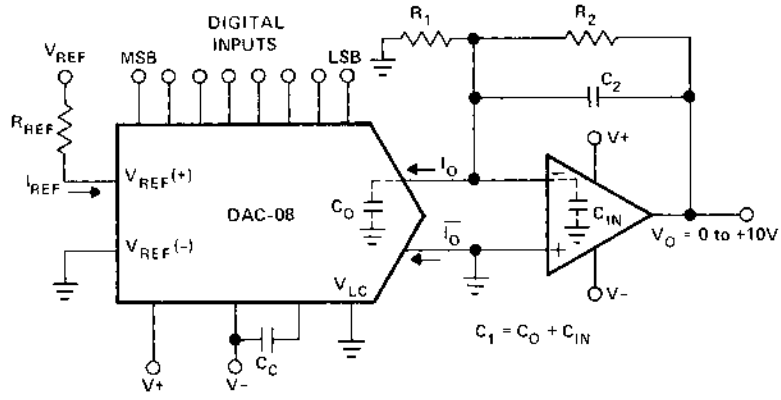


FIGURE 3
VOLTAGE OUTPUT DAC WITH RESPONSE SHAPING

The circuit of Figure 3 resolves this problem. It can be shown that if $R_1C_1 = R_2C_2$, the effect of the two capacitors is completely cancelled, and the overall settling will be determined by the amplifier's behavior only. In addition, C_2 can be varied to fine tune the system's response and minimize settling time to compensate for the op amp's possibly underdamped or overdamped characteristics. The disadvantage of this circuit compared to that of Figure 2 is that all input errors, and in particular input offset voltage (V_{OS}), are amplified by the factor $\left(1 + \frac{R_2}{R_1}\right)$.

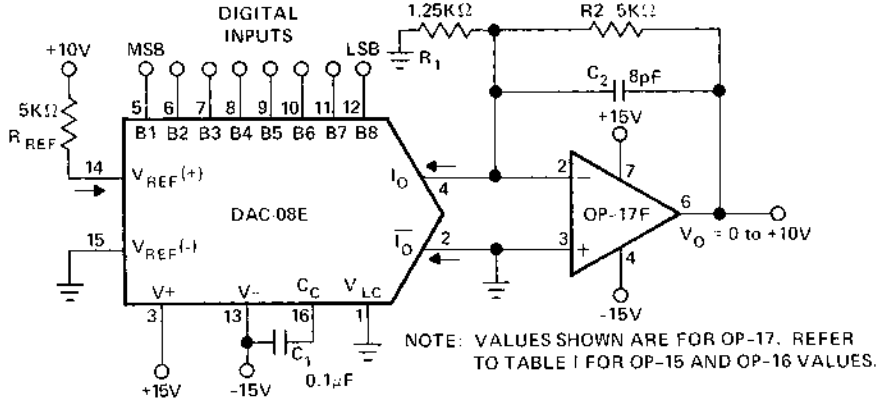


FIGURE 4
0 TO +10V CONNECTION, SETTLING TIME = 380nsec

The optimum speed is obtained – at low cost – by using the OP-17, fast, precision, BIFET-input op amp, stable only at closed-loop gains of five or more. Therefore, the R_1/R_2 ratio is set at four (Figure 4). Settling time to 0.2% is 380nsec with all bits turning on (0 to 10V), or all bits turning off (10V to 0). The last 2.5 volts of the rising wave-form are shown in the photograph of Figure 5. The three grades of the OP-17 are specified at V_{OS}=0.5mV max (OP-17E), 1.0mV max (OP-17F), and 3.0mV max (OP-17G). Even though V_{OS} is multiplied five times its effect is still less than 0.2% or 20mV. The OP-17E's contribution will be only 1/4 LSB even on a 10 bit system. The offset voltage can also be trimmed to zero, then the TCV_{OS}, at 2 to 4μV/°C, typically, will be the limiting factor. The complementary output of the DAC-08 can be used for a –10V to +10V system as depicted in Figure 6. Settling time is only slightly increased because of the time required to slew the additional ten volts. Since 1/2 LSB is now 40mV, the non-slew portion is decreased by 70nsec.

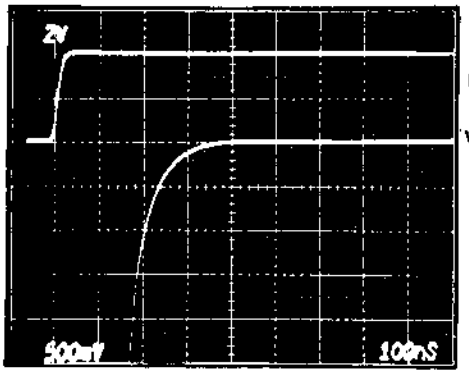


FIGURE 5
SETTLING TIME OF FIGURE 4 CIRCUIT USING OP-17

The OP-16 is slower than the OP-17 but it is stable in unity gain. Therefore, improved output-referred error can be traded off for increased settling time. The OP-15 is a lower power dissipation model, but again this improvement is obtained at the expense of settling time. Table I summarizes the resistor and capacitor values for the various amplifiers in the circuits of Figure 4 and Figure 6, the settling times obtained in these circuits, and the output-referred offset errors.

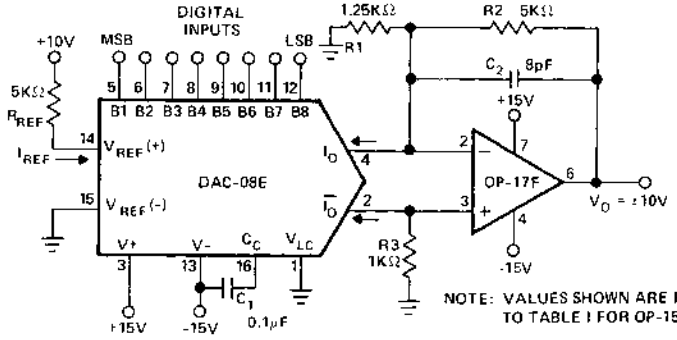


FIGURE 6
±10V CONNECTION, SETTLING TIME = 450nsec

TABLE I
OP-17/16/15 PERFORMANCE AS OUTPUT OP AMP FOR DAC-08

	OP-17		OP-16		OP-15	
	0 to 10V Fig. 4	−10 to +10V Fig. 6	0 to 10V Fig. 4	−10 to +10V Fig. 6	0 to 10V Fig. 4	−10 to +10V Fig. 6
R_1	1.25KΩ	1.25KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_2	5KΩ	5KΩ	5KΩ	5KΩ	5KΩ	5KΩ
R_3	–	1KΩ	–	3.3KΩ	–	3.3KΩ
C_2	8pF	8pF	25pF	40pF	30pF	50pF
Settling time to ±0.2%	380nsec	450nsec	750nsec	1100nsec	900nsec	1350nsec
Slew Time	150nsec	290nsec	400nsec	800nsec	590nsec	1170nsec
1/2 LSB = 0.2%	20mV	40mV	20mV	40mV	20mV	40mV
Closed Loop Gain	5	5	1.5	1.5	1.5	1.5
Offset Error at Output						
E Grade MAX	2.5mV	2.5mV	0.75mV	0.75mV	0.75mV	0.75mV
F Grade MAX	5.0mV	5.0mV	1.5mV	1.5mV	1.5mV	1.5mV
G Grade MAX	15.0mV	15.0mV	4.5mV	4.5mV	4.5mV	4.5mV
SUPPLY CURRENT MAX	7mA	7mA	7mA	7mA	4mA	4mA

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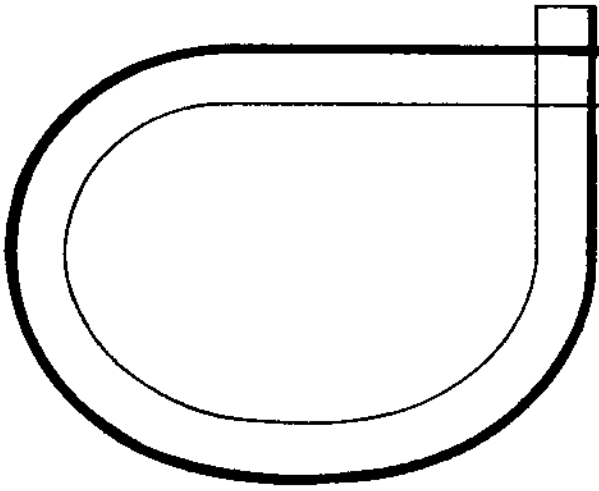
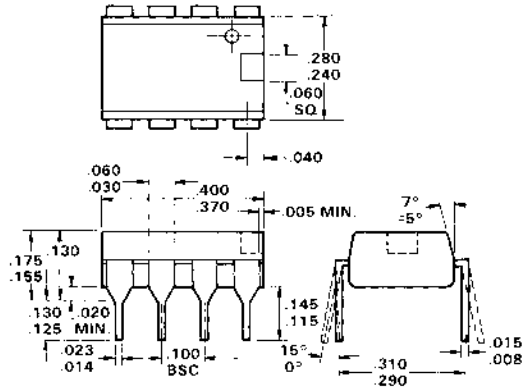


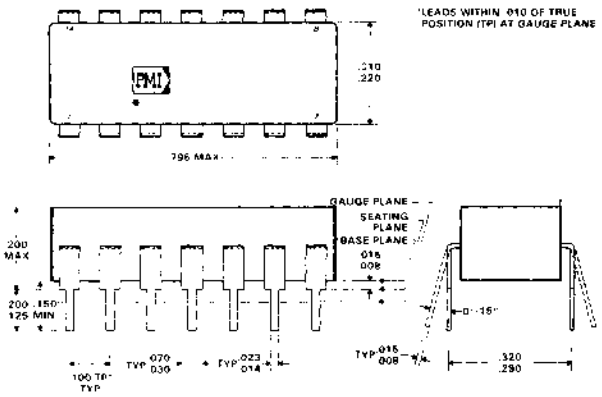
AVAILABLE PACKAGES

PACKAGE	DESCRIPTION
H	6 Pin TO-78
J	8 Pin TO-99
K	10 Pin TO-100
L	10 Pin Hermetic Flatpack
M	14 Pin Hermetic Flatpack
N	24 Pin Hermetic Flatpack
Y	14 Pin Hermetic Dip
Q	16 Pin Hermetic Dip
X	18 Pin Hermetic Dip
V	24 Pin Hermetic Dip
P	Epoxy 8 Mini Dip

MECHANICAL DIMENSIONS – DIP'S

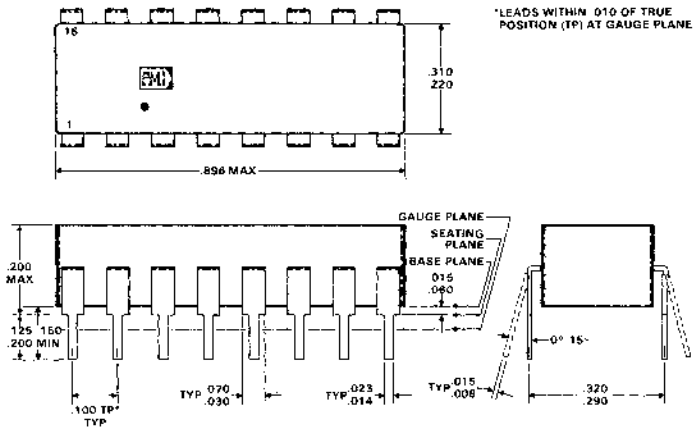


8 PIN EPOXY B MINI DIP

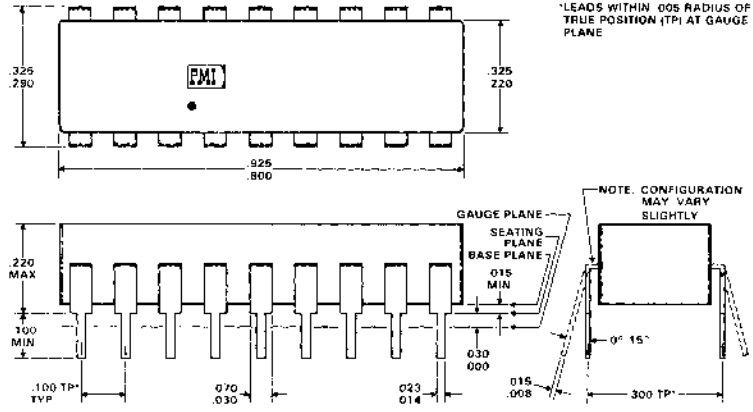


14 PIN HERMETIC DUAL-IN-LINE (Y)

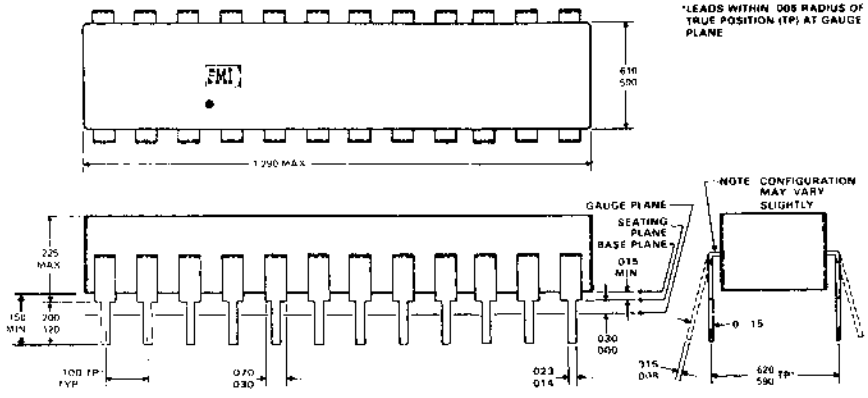
MECHANICAL DIMENSIONS – DIP'S (CONTINUED)



16 PIN HERMETIC DUAL-IN-LINE (O)

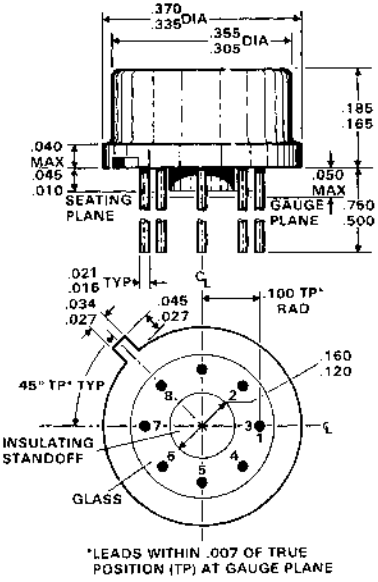


18 PIN HERMETIC DUAL-IN-LINE (X)

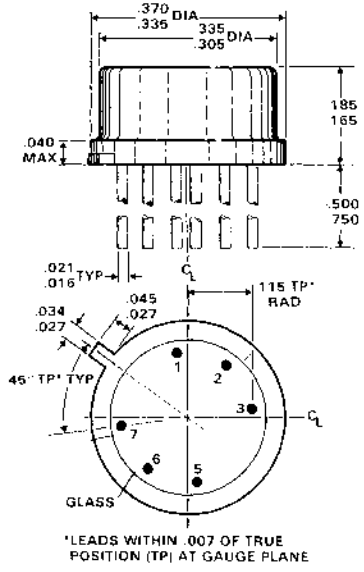


24 PIN HERMETIC DUAL-IN-LINE (V)

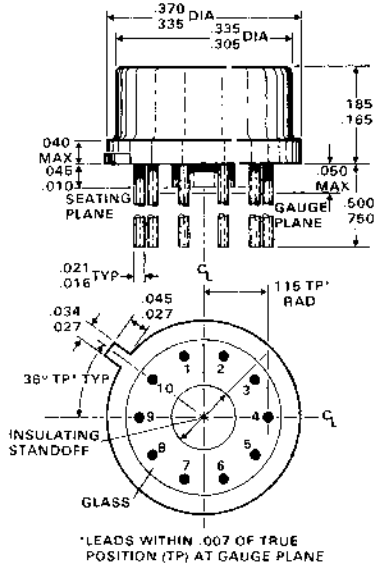
MECHANICAL DIMENSIONS – CANS



TO-99 (J)

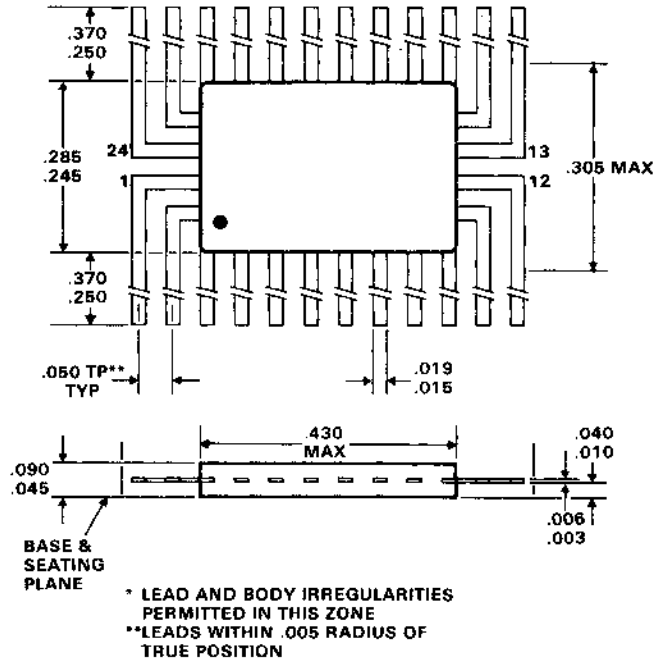


TO-78 (H)

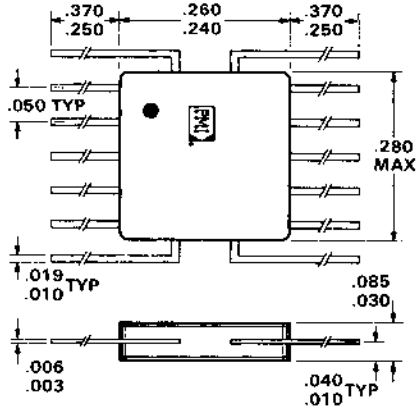


TO-100 (K)

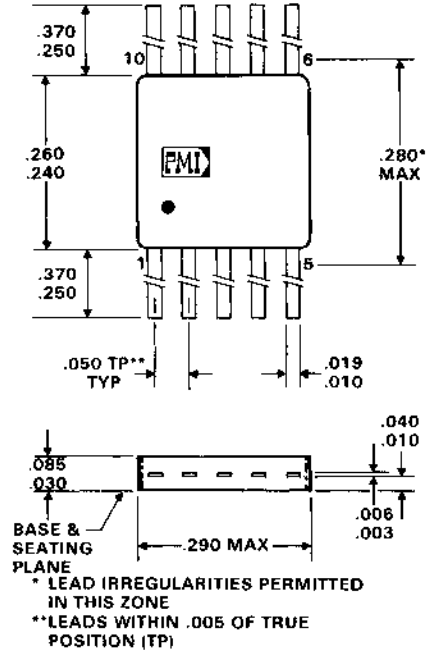
MECHANICAL DIMENSIONS – FLATPACKS



24 PIN HERMETIC FLATPACK (N)



14 PIN HERMETIC FLATPACK (M)



10 PIN HERMETIC FLATPACK (L)

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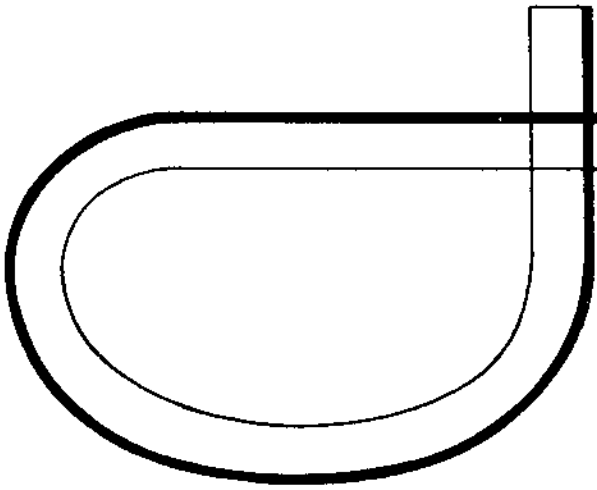

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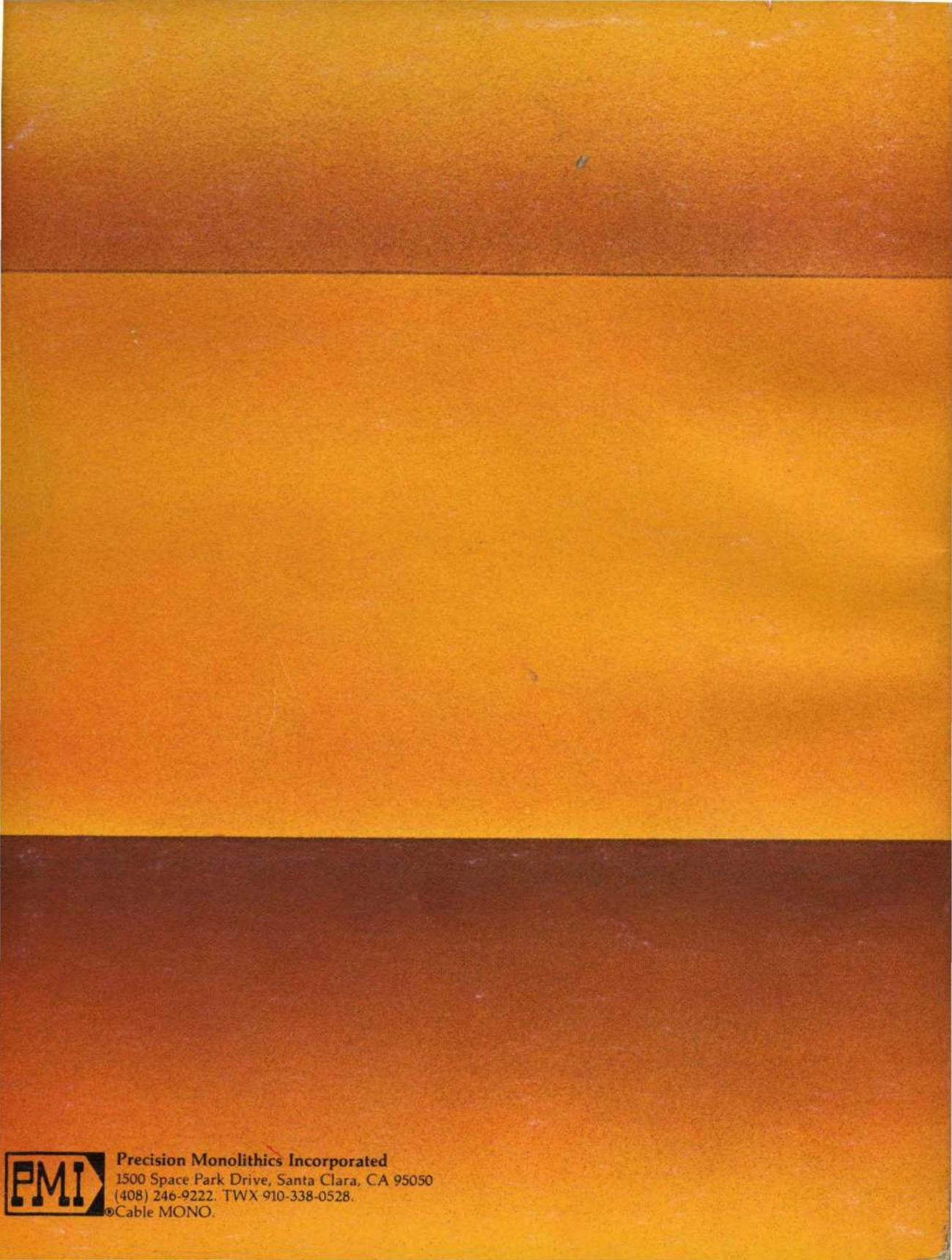

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