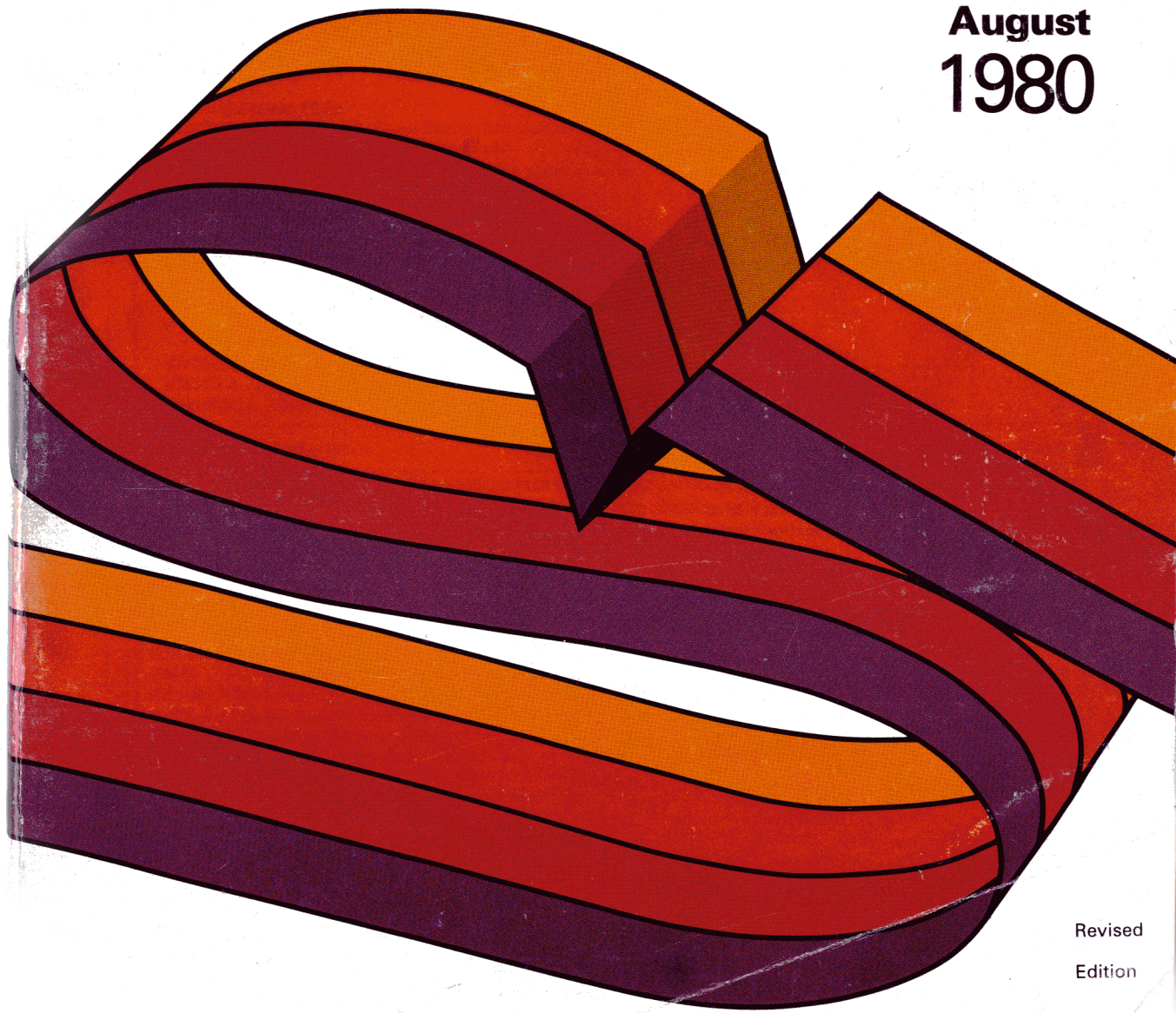
Siliconix

VMOS Power FETs Design Catalogue

August
1980



Revised
Edition

Siliconix

VMOS Power FETs Design Catalog

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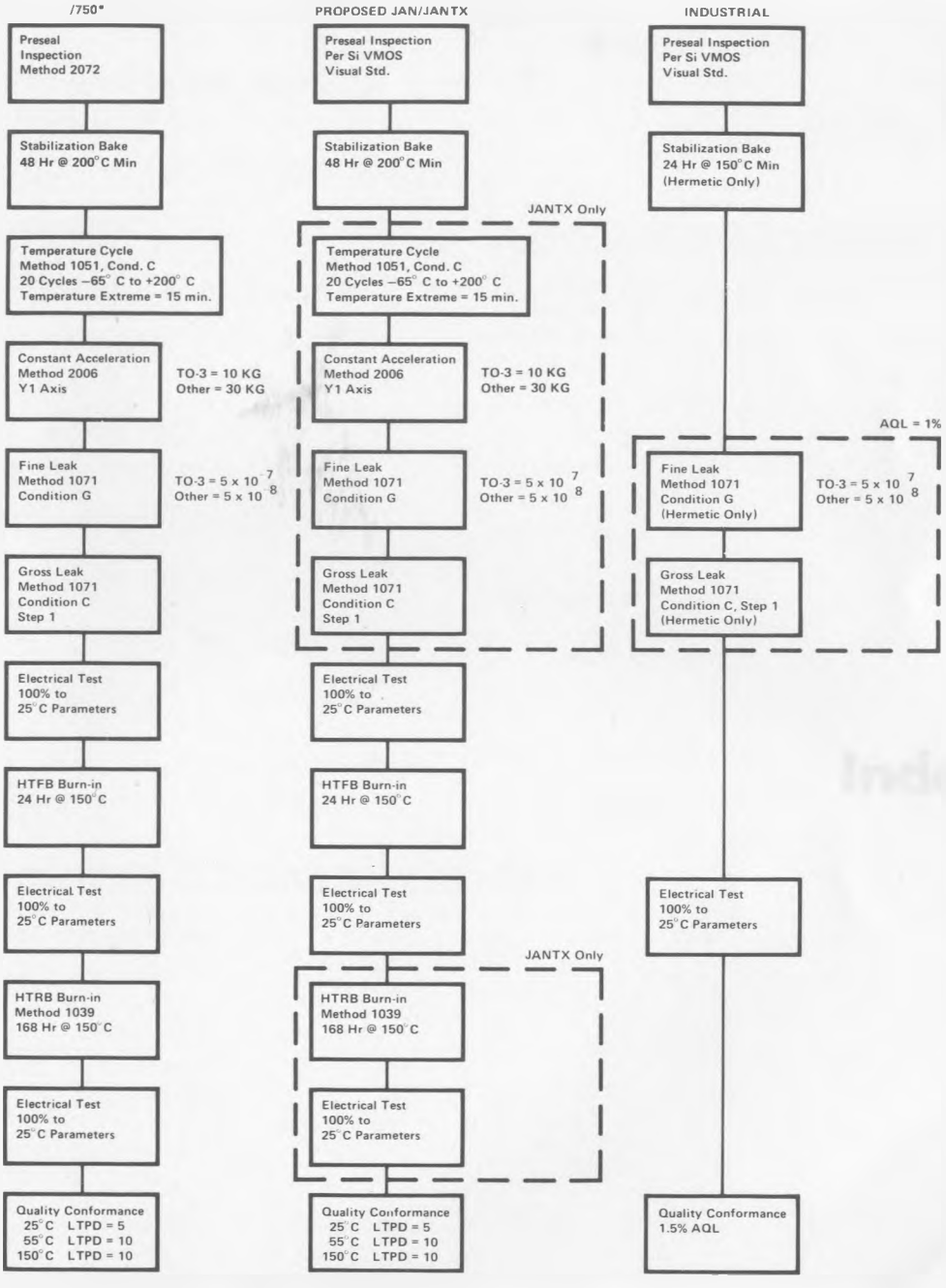
contents

Siliconix

VMOS Selector Guide

$R_{DS(on)}$	BREAKDOWN VOLTAGE										PACKAGE
	35 V		40 V		60 V		80 V		90 V		
	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	
0.4						VN64GA					A, J  TO-3
1.8	2N6656	VN33AJ									
2.5	VN35AA	VN35AJ									
3.0					2N6657	VN66AJ					
3.5					VN67AA	VN67AJ					
4.0									2N6658	VN98AJ	
4.5							VN89AA			VN99AJ	
5.0	VN30AA								VN90AA		
1.8	2N6659	VN33AK									B, K  TO-39
2.5	VN35AB	VN35AK									
3.0					2N6660	VN66AK					
3.5					VN67AB	VN67AK					
4.0									2N6661	VN98AK	
4.5							VN89AB			VN99AK	
5.0	VN30AB								VN90AB		
3.0			VN46AF		VN66AF						F  TO-202
3.5					VN67AF						
4.0							VN88AF				
4.5							VN89AF				
5.0			VN40AF								
5.0	VK1011 (30V)				VN10KM				VK1010 (100V)		M  TO-237
5.0					VQ1000 CJ (Quad)						 14 pin DIP

Process Option Flow Chart



*Similar to JANTXV screening per MIL S 19500 methods per MIL-STD-750

Index

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers
Class A, B, or C
High Dynamic Range Amp

10 W Broadband
12.5 V
10 dB Gain
175 MHz

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

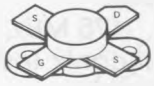
DV XX XXX X

- X — Package Type
- XXX — Power Output (Watts)
- XX — Operating Voltage
- DV — Frequency

Absolute Maximum Ratings (25°C)

Gate-Source Voltage	30V
Drain-Source Voltage	50V
Drain-Gate Voltage	50V
Drain Current	2A
Total Device Dissipation @ 25° Case	40W
θjc for .380 SOE	4.4°C/W
Storage Temperature	−65°C to 150°C

S-Package
See Section 5



.380 SOE
FLANGE

Electrical Characteristics (25°C)

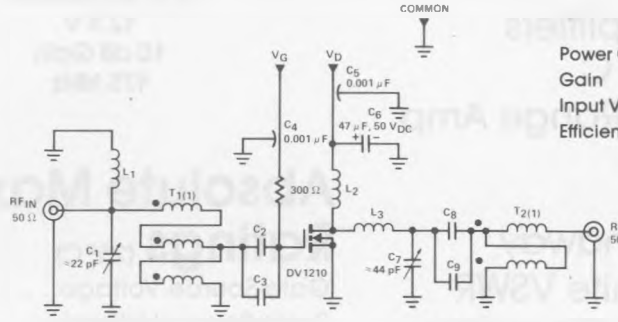
Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	9	10		W	V_{DD} = 12.5 V, I_{DQ} = 1 A P_{IN} = 1 W Max, F = 175 MHz
η(1)	Drain Efficiency	55	60		%	
gm	Transconductance		0.4		Mho	V_{DS} = 12.5 V, I_D = 1 A
C_{oss}	Output Capacity		49			
C_{rss}	Reverse Transfer Capacity		7.5		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{iss}	Input Capacity		41			
Z_{IN}	Input (Series) Impedance		3.1 + j 12.9		Ω	V_{DS} = 12.5 V, P_{IN} = 1 W F = 175 MHz, P_{OUT} = 10 W
Z_{OUT}	Output (Series) Impedance		4.0 + j 4.0			

Note:

(1) All devices 100% power tested in Siliconix test fixture No. RF12175 [10]

Test Fixture/Applications

135 MHz to 175 MHz, 12.5 Volt Amplifier

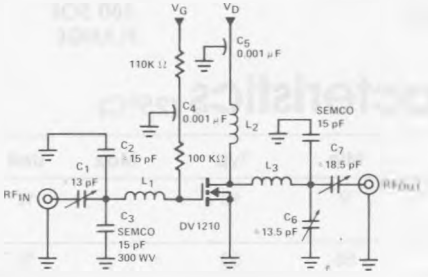


Power Out	10 W
Gain	9.6 dB +0, −0.4 dB
Input VSWR	< 1.5:1
Efficiency	> 55%

Notes: C_1, Arco #462 trimmer capacitor, 5 to 80 pF
C_7, Arco #463 trimmer capacitor, 9 to 180 pF
L_1, 2 turns, #AWG 22 on 1/4" diameter close wound
L_2, 7 turns, #AWG 22 on 1/4" diameter close wound
L_3, 1/2" #AWG 18 buss, 1/2-turn on 1/4" diameter
C_2, C_3, C_8, C_9, 0.01 µF chip capacitors, Johanson P/N 201 L64 N 103 MA
T_1, One turn #22 enamel wire trifilar twisted with 13 crests per inch on one Stackpole balun core #57-0973
T_2, One turn 25 Ω coax wound on two balun cores placed end on end. Stackpole balun cores #57-0973

(1) — Dot indicates winding starts

175 MHz, 12.5 Volt Amplifier
Siliconix Test Fixture #RF12175 [10]



Power Out	10 W
Gain	10 dB
Efficiency	> 60%

Notes: C_1, C_2, C_5, C_6, Arco #462, 5 to 80 pF
L_1, 2 1/2" length of #AWG 12, 1/2 turn on 1/3" diameter
L_2, 8 turns #AWG 22 on 1/4" diameter, close wound
L_3, 1 5/8" length of #AWG 12, 1/2 turn on 1/3" diameter

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers
Class A, B, or C
High Dynamic Range Amp

20 W Broadband
12.5 V
10 dB Gain
175 MHz

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

DV XX XX X
- X — Package Type
- XX — Power Output (Watts)
- XX — Operating Voltage
- DV — Frequency

Absolute Maximum Ratings (25°C)

Gate-Source Voltage..... 30V
Drain-Source Voltage..... 50V
Drain-Gate Voltage..... 50V
Drain Current..... 4A
Total Device Dissipation..... 80W
@ 25° Case
θjc for .380 SOE..... 2.2°C/W

Storage Temperature.... −65°C to 150°C

S - Package
see Section 5

.380 SOE
FLANGE

Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	18	20		W	V_{DD} = 12.5 V, I_{DQ} = 2 A P_{IN} = 2 W Max, F = 175 MHz
η(1)	Drain Efficiency	55	60		%	
g_m	Transconductance		0.8		Mho	V_{DS} = 12.5 V, I_D = 2 A
C_{oss}	Output Capacity		98			
C_{rss}	Reverse Transfer Capacity		15		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{iss}	Input Capacity		82			
Z_{IN}	Input (Series) Impedance		1.6 + j6.5		Ω	V_{DS} = 12.5 V, P_{IN} = 2 W F = 175 MHz, P_{OUT} = 20 W
Z_{OUT}	Output (Series) Impedance		2 + j2			

Note: (1) All devices 100% power tested in Siliconix test fixture No. RF12175 [20]

DV1230T

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers
Class A, B, or C
High Dynamic Range Amp

30 W Broadband
12.5 V
10 dB Gain
175 MHz

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

DV XX XX X
- X — Package Type
- XX — Power Output (Watts)
- XX — Operating Voltage
- DV — Frequency

Absolute Maximum Ratings (25°C)

Gate-Source Voltage..... 30V
Drain-Source Voltage..... 50V
Drain-Gate Voltage..... 50V
Drain Current..... 6A
Total Device Dissipation..... 120W
@ 25° Case
θjc for .500 J0..... 1.5°C/W

Storage Temperature.... −65°C to 150°C

T - Package
see Section 5

.500 J0
FLANGE

Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	27	30		W	V_{DD} = 12.5 V, I_{DQ} = 3 A P_{IN} = 3 W Max, F = 175 MHz
η(1)	Drain Efficiency	55	60		%	
g_m	Transconductance		1.2		Mho	V_{DS} = 12.5 V, I_D = 3 A
C_{oss}	Output Capacity		147			
C_{rss}	Reverse Transfer Capacity		22.5		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{iss}	Input Capacity		123			
Z_{IN}	Input (Series) Impedance		1 + j4.3		Ω	V_{DS} = 12.5 V, P_{IN} = 3 W F = 175 MHz, P_{OUT} = 30 W
Z_{OUT}	Output (Series) Impedance		1.3 + j1.3			

Note: (1) All devices 100% power tested in Siliconix test fixture No. RF12175 [30]

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers
Class A, B, or C
High Dynamic Range Amp

40 W Broadband
12.5 V
10 dB Gain
175 MHz

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

DV XX XXX X
- X — Package Type
- XXX — Power Output (Watts)
- XX — Operating Voltage
- DV — Frequency

Absolute Maximum Ratings (25°C)

Gate-Source Voltage..... 30V
Drain-Source Voltage..... 50V
Drain-Gate Voltage..... 50V
Drain Current..... 8A
Total Device Dissipation..... 160W
@ 25° Case
θjc for .500 J0..... 1.1°C/W

Storage Temperature.... −65°C to 150°C

T- Package
see Section 5

.500 J0
FLANGE

Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	36	40		W	V_{DD} = 12.5 V, I_{DQ} = 4 A P_{IN} = 4 W Max, F = 175 MHz
η(1)	Drain Efficiency	55	60		%	
g_m	Transconductance		1.6		Mho	V_{DS} = 12.5 V, I_D = 4.0 A
C_{oss}	Output Capacity		196		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{rss}	Reverse Transfer Capacity		30			
C_{iss}	Input Capacity		164			
Z_{IN}	Input (Series) Impedance		0.8 + j3.2		Ω	V_{DS} = 12.5 V, P_{IN} = 4 W F = 175 MHz, P_{OUT} = 40 W
Z_{OUT}	Output (Series) Impedance		1.0 + j1.0			

Note: (1) All devices 100% power tested in Siliconix test fixture No. RF12175 [40]

DV2820S (DV1006)

RF Power FETs

Siliconix

n-channel enhancement-mode RF VMOS power FET *designed for...*

Preliminary

25 WATTS
20 W BROADBAND
28 V
10 dB GAIN
175 MHz

HF/VHF/UHF Amplifiers
Class A, B, or C

High Dynamic Range Amplifier

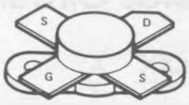
Benefits

Infinite VSWR
No Thermal Runaway
Broadband Capability
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry
S-Parameter Design

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage	40 V
Drain-Source Voltage	80 V
Drain-Gate Voltage	80 V
Drain Current	2 A
Total Device Dissipation @ 25°C Case	40 W
Storage Temperature	−65°C to 150°C
θjc	4.4 °C/W

S-Package
see Section 5



380 SOE
FLANGE

Electrical Characteristics (25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	TEST CONDITIONS
P_{OUT}(1)	POWER OUTPUT	20			W	V_{DD}=28 V, I_{DQ}= 100 mA P_{IN}= 2 W Max, F= 175 MHz
η(1)	DRAIN EFFICIENCY	60			%	
gm	TRANCONDUCTANCE		0.250		Mho	V_{DS}=28 V, I_D= 1A
C_{oss} C_{rss} C_{iss}	OUTPUT CAPACITY REVERSE TRANSFER CAPACITY INPUT CAPACITY		32 4.0 48		pF	V_{DS}= 28 V, V_{GS}= 0
Z_{IN}(2) Z_{OUT}	INPUT (SERIES) IMPEDANCE OUTPUT (SERIES) IMPEDANCE		12.5 - j7.42		Ω	V_{DS}= 28 V, P_{IN} = 0.5 W F_o = 100 MHz, P_{OUT} = 20 W
NF(3)	SMALL SIGNAL NOISE FIGURE		4		dB	F = 175 MHz, V_{DS} 28 V I_D 0.1 A

NOTES:
(1) All devices 100% power tested in Siliconix test fixture No. RF 28175 [20].
(2) Z_{IN} dependent on feedback network.
(3) Noise figure measured with 20 Watt power matched source and load.

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF VMOS power FET *designed for...*

HF/VHF/UHF Amplifiers
Class A, B, or C

High Dynamic Range Amplifier

50 WATTS
40 W BROADBAND
28 V
10 dB GAIN
175 MHz

Benefits

- **Infinite VSWR**
- **No Thermal Runaway**
- **Broadband Capability**
- **Class A, B, or C Operation**
- **Low Noise Figure**
- **High Dynamic Range**
- **Simple Bias Circuitry**
- **S-Parameter Design**

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage	40 V
Drain-Source Voltage	80 V
Drain-Gate Voltage	80 V
Drain Current	4 A
Total Device Dissipation @ 25°Case	80 W
ϕjc	2.2 °C/W
Storage Temperature	−65°C to 150° C

S-Package
see Section 5

380 SOE
FLANGE

Electrical Characteristics (25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	TEST CONDITIONS
P_{OUT}(1)	POWER OUTPUT	40			W	V_{DD}=28 V, I_{DQ}= 0.2 A P_{IN}= 4 W Max, F= 175 MHz
η(1)	DRAIN EFFICIENCY	60			%	
gm	TRANCONDUCTANCE		0.5		Mho	V_{DS}=28 V, I_D= 2A
C_{oss} C_{rss} C_{iss}	OUTPUT CAPACITY REVERSE TRANSFER CAPACITY INPUT CAPACITY		65 8.5 95		pF	V_{DS}= 28 V, V_{GS}= 0
Z_{IN}(2) Z_{OUT}	INPUT (SERIES) IMPEDANCE OUTPUT (SERIES) IMPEDANCE		6.5 - j4.2		Ω	V_{DS}= 28 V, P_{IN} = 1.3 W F_o = 100 MHz, P_{OUT} = 40 W
NF(3)	SMALL SIGNAL NOISE FIGURE		7		dB	F = 175 MHz, V_{DS}=28 V I_D = 0.2 A

NOTES:
(1) All devices 100% power tested in Siliconix test fixture No. RF 28175 [40].
(2) Z_{IN} dependent on feedback network.
(3) Noise figure measured with 40 Watt power matched source and load.

RF Power FETs

Siliconix

n-channel enhancement-mode RF Power FETs designed for...

175 MHz
28-35 V
100 W
10 dB

HF/VHF/UHF Amplifiers Class A, B, or C
High Dynamic Range Amp

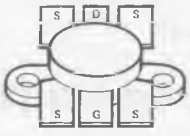
Benefits

Infinite VSWR
No Thermal Runaway
Broadband Capability
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry
S-Parameter Design

Absolute Maximum Ratings (25°C)

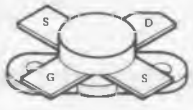
Gate-Source Voltage..... 40 V
Drain-Source Voltage..... 80 V
Drain-Gate Voltage..... 80 V
Drain Current..... 8 A
Total Device Dissipation..... 160 W
@ 25° Case
θjc ..... 1.1°C/W
Storage Temperature..... −65°C to 150°C
Junction Temperature..... 200°C

T-Package



.500 J0 FLANGE

U-Package



.500 SOE FLANGE

see Section 5

DV XX XXX X
- X — Package Type
- XXX — Power Output
- XX — Operating Voltage
- DV — Frequency

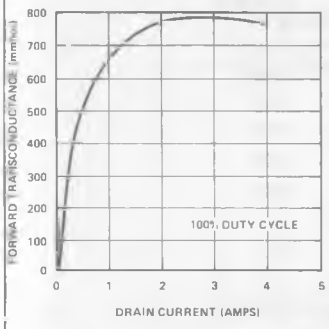
Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	80			W	V_{DS}=28 V, I_{DQ}=0.4 A
η(1)	Drain Efficiency		60		%	P_{IN}=8 W, f=175 MHz
gm	Transconductance		1.0		Mho	V_{DS}=28 V, I_D=4 A
C_{oss}	Output Capacity		130			
C_{rss}	Reverse Transfer Capacity		17		pF	V_{DS}=28 V, V_{GS}=0 V
C_{iss}	Input Capacity		190			
NF(2)	Small Signal Noise Figure		4		dB	f=175 MHz, V_{DS}=28 V I_D=0.4 A

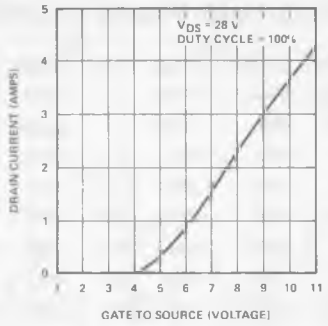
Notes: (1) All devices 100% power tested in Siliconix test fixture No. RF28175 [80]
(2) Noise figure measured with 80 watt power matched source and load

Typical Performance Curves (25°C)

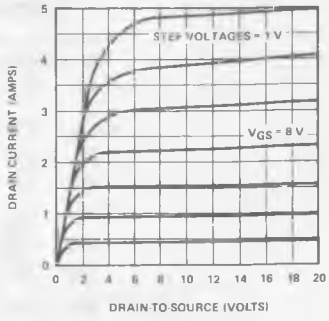
Transconductance vs Drain Current



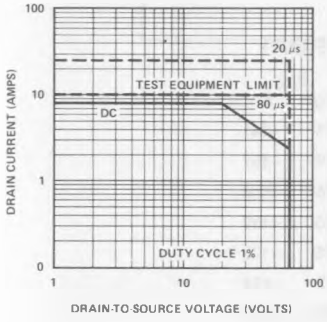
Drain Current vs Gate-to-Source Voltage



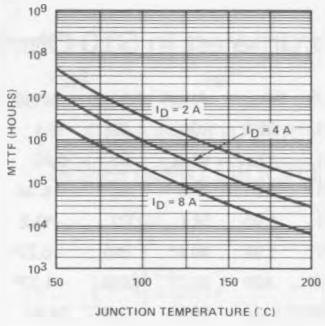
Output Characteristics vs Drain-to-Source Voltage



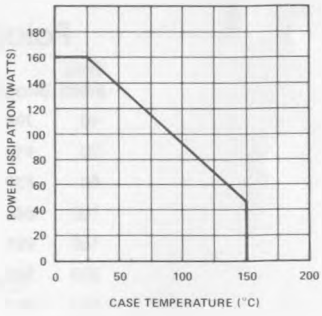
DC and Inductive Safe Operating Region $T_C = 25°C$



MTTF vs Temperature



Power Dissipation vs Case Temperature



Large Signal Series Input Impedance

Frequency	R_S (ohms)	X_S (ohms)
100	0.6	−6.8
110	0.9	−6.0
120	1.0	−5.3
130	1.0	−5.2
140	1.2	−4.8
150	1.2	−4.4
160	1.3	−4.0
170	1.3	−3.7
180	1.2	−3.4
190	1.2	−2.8
200	1.0	−2.6

Conditions:
$R_L = 5.5\ \Omega$
$V_{DS} = 28$ Volts
$I_{DQ} = 1.0$ Amps
$P_{IN} = 10$ Watts

Small Signal 2-Port Parameters

2-Port Y-Parameter Matrix in Millimhos

Freq	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
(MHz)	(Real	Imag)	(Real	Imag)	(Real	Imag)	(Real	Imag)
10	0	10.5	886	−47.5	0	−1.03	4.42	8.34
20	0.897	21.3	881	−37.5	0	−2.05	5.31	15.9
50	6.52	58.3	902	−106	.5	−5.65	7.61	42.5
100	20.1	128	1060	−294	2.13	−11.9	11.0	89.3
150	57.0	207	1220	−565	6.63	−19.8	21.4	134
200	125	322	1450	−964	12.8	−33.4	23.1	191
250	241	340	1230	−1.61	32.5	−48.7	14.9	226
300	520	219	215.5	−2.4	33.6	−96.9	−76.3	371
350	565	124	−243.2	−2.02	43.5	−123	−66.1	417
400	574	4.06	−695.7	−1.72	37.1	−166	−59.3	551
450	509	−35.6	−812.7	−1.35	30.2	−198	−17.0	644
500	477	−11.6	−800.4	−1.27	43.7	−258	−13.8	749

Conditions: 28 V, 1.6 A

Polar S-Parameters in 50.0 Ohm System

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)
10	.798	−134	25.1	106	.00	18.4	.691	−141
20	.819	−154	13.1	91.8	.03	6.42	.819	−157
50	.839	−168	4.51	71.8	.03	−6.34	.766	−166
100	.884	−173	1.95	51.1	.02	−13.2	.835	−169
150	.921	−175°	1.04	40.4°	.016	−6.22°	.888	−172 °
200	.943	−177°	.629	34.2°	.013	−1.27°	.917	−174°
250	.953	−179°	.436	28.3°	.013	24.5°	.939	−175°
300	.959	178°	.309	26.4°	.013	40.4°	.950	−176°
350	.962	178°	.234	24.4°	.015	50.7°	.954	−176°
400	.966	177°	.187	24.3°	.017	58.8°	.957	−177°
450	.963	176°	.157	25.9°	.020	65.5°	.958	−178°
500	.966	176°	.138	27.2°	.029	69.0°	.962	−178°

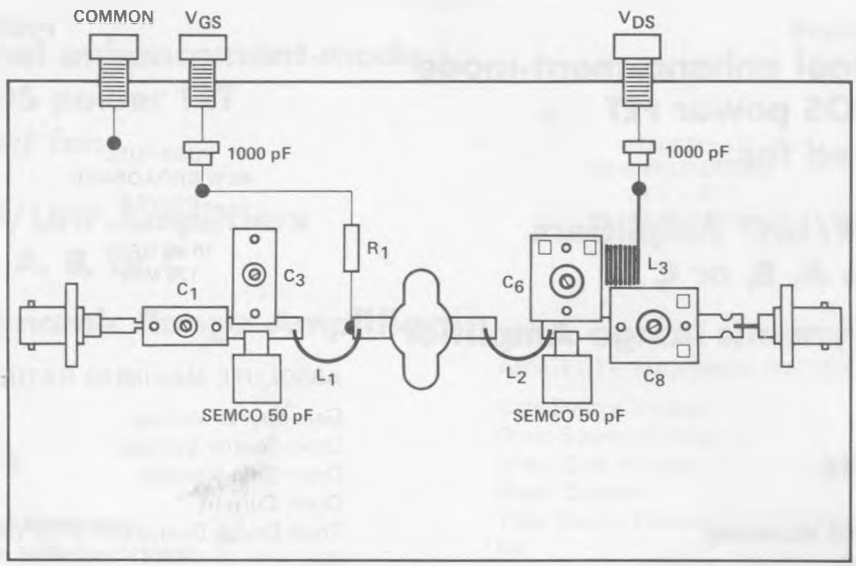
Conditions: 28 V, 1.6 A

CAUTION: Beryllium Oxide — The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide Ceramic, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

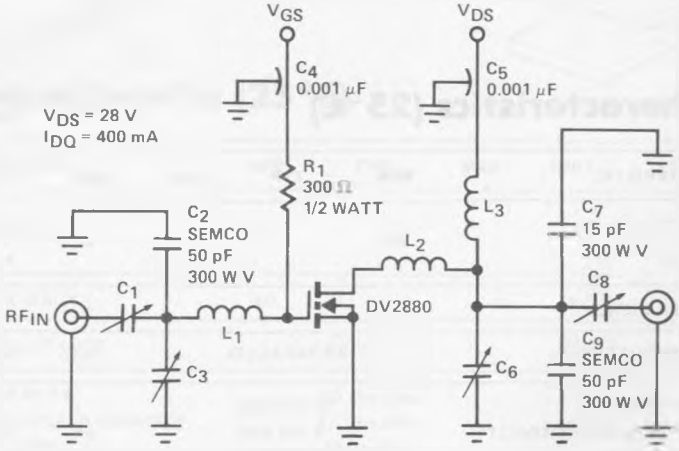
Test Fixture

175 MHz Test Fixture



Scale: 3/4 of original size

175 MHz DV2880 Schematic Diagram



All DV2880's are tested in this test fixture.

Parts List

C_1, C_3, 4 to 40 pF ARCO #422 trimmer capacitors
C_6, C_8, 9 to 180 pF ARCO #463 trimmer capacitors
L_1, 1 3/16" length of #12 AWG (loop 1/2")
L_2, 1" length of #12 (loop 0.4")
L_3, 8 turns #18 AWG enamel on 1/4" diameter, close wound
R_1, 10 KΩ 1/4 watt carbon resistor

DV2840V (DV1110)

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF VMOS power FET *designed for...*

PUSH-PULL
40 W BROADBAND
DRIVER
28 V – 35 V
10 dB GAIN
175 MHz

HF/VHF/UHF Amplifiers Class A, B, or C

High Dynamic Range Amplifier

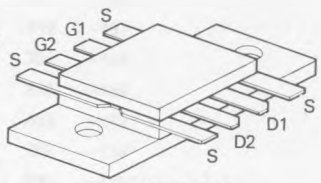
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage	40 V
Drain-Source Voltage	80 V
Drain-Gate Voltage	80 V
Drain Current	4 A
Total Device Dissipation @ 25° Case	80 W
θjc	2.2 °C/W
Storage Temperature	−65° C to 150° C
Max Junction Temp.	+200°C

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

V-Package
see Section 5



PUSH-PULL

Electrical Characteristics (25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	TEST CONDITIONS
P_{OUT}(1)	POWER OUTPUT	40			W	V_{DD}=28 V, I_{DQ}= 0.2 A P_{IN}= 4 W Max, F= 175 MHz
η(1)	DRAIN EFFICIENCY	60			%	
gm(2)	TRANSCONDUCTANCE		0.5 PARALLEL		Mho	V_{DS}=28 V, I_D= 2A
C_{oss}	OUTPUT CAPACITY		28 (Per Side)			
C_{rss}	REVERSE TRANSFER CAPACITY		4 (Per Side)		pF	V_{DS} = 28 V, V_{GS} = 0 V
C_{iss}	INPUT CAPACITY		35 (Per Side)			
NF(3)	SMALL SIGNAL NOISE FIGURE		7.0		dB	V_{DS}=28 V I_D = 0.2 A F = 100 MHz

NOTES:
(1) All devices 100% power tested in Siliconix test fixture No. RF 28175 [PP1].
(2) Measured under pulsed condition with pulse width 300 μsec > 5% duty cycle.
(3) Noise figure measured with 40 Watt power matched source and load.

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF VMOS power FET *designed for...*

PUSH-PULL
80 W BROADBAND
28 V – 35 V
10 dB GAIN
175 MHz

HF/VHF/UHF Amplifiers Class A, B, or C

High Dynamic Range Amplifier

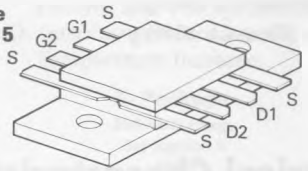
Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage	40 V
Drain-Source Voltage	80 V
Drain Gate Voltage	80 V
Drain Current	8 A
Total Device Dissipation @ 25°Case	160 W
θjc	1.1 °C/W
Storage Temperature	−65°C to 150° C
Max Junction Temp.	+200°C

V-Package
see Section 5



PUSH-PULL

Electrical Characteristics (25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	TEST CONDITIONS
P_{OUT}(1)	POWER OUTPUT	80			W	V_{DD} 28 V, I_{DQ} 0.4 A P_{IN} = 8 W Max, F = 175 MHz
η (1)	DRAIN EFFICIENCY	60			%	
gm(2)	TRANSCONDUCTANCE		1.0 PARALLEL		Mho	V_{DS}=28 V, I_D = 4 A
C_{oss}	OUTPUT CAPACITY		55 (Per Side)			
C_{rss}	REVERSE TRANSFER CAPACITY		8.0 (Per Side)		pF	V_{DS} = 28 V, V_{GS} = 0 V
C_{iss}	INPUT CAPACITY		70 (Per Side)			
NF(3)	SMALL SIGNAL NOISE FIGURE		7.5		dB	V_{DS} 28 V, I_D 0.4 A, F = 100 MHz

NOTES:
(1) All devices 100% power tested in Siliconix test fixture No. RF 28175 [PP2].
(2) Measured under pulsed condition with pulse width 300 μsec > 5% duty cycle.
(3) Noise figure measured with 80 Watt power matched source and load.

DV28120V (DV1112)

RF Power FETs

Siliconix

Preliminary

n-channel enhancement-mode RF VMOS power FET *designed for...*

PUSH-PULL
120 W BROADBAND
28 V – 35 V
10 dB GAIN
175 MHz

HF/VHF/UHF Amplifiers Class A, B, or C

High Dynamic Range Amplifier

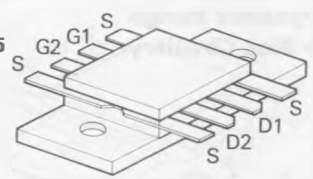
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage	40 V
Drain-Source Voltage	80 V
Drain-Gate Voltage	80 V
Drain Current	12 A
Total Device Dissipation @ 25° Case	240 W
θjc	.73° C/W
Storage Temperature	–65°C to 150°C
Max Junction Temp.	+200°C

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

V-Package
see Section 5



PUSH-PULL

Electrical Characteristics (25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	TEST CONDITIONS
P_{OUT}(1)	POWER OUTPUT	120			W	V_{DD} = 28V, I_{DQ} = 0.6 A P_{IN} = 12 W Max, F = 175 MHz
η(1)	DRAIN EFFICIENCY	60			%	
gm(2)	TRANSCONDUCTANCE		1.5 PARALLEL		Mho	V_{DS} = 28 V, I_D = 6 A
C_{oss}	OUTPUT CAPACITY		85 (Per Side)		pF	V_{DS} = 28 V, V_{GS} = 0 V
C_{rss}	REVERSE TRANSFER CAPACITY		12 (Per Side)		pF	V_{DS} = 28 V, V_{GS} = 0 V
C_{iss}	INPUT CAPACITY		105 (Per Side)		pF	V_{DS} = 28 V, V_{GS} = 0 V
NF(3)	SMALL SIGNAL NOISE FIGURE		8.5		dB	V_{DS}=28 V, I_D = 0.6 A, F = 100 MHz

NOTES:
(1) All devices 100% power tested in Siliconix test fixture No. RF 28175 [PP3].
(2) Measured under pulsed condition with pulse width 300 μsec > 5% duty cycle.
(3) Noise figure measured with 120 Watt power matched source and load.

RF Power FETs

n-channel enhancement-mode VMOS Power FETs *designed for . . .*

- **VHF Broadband Amplifiers**
- **Receiver Front Ends**
- **Class B, C, D, E Amplifiers**
- **Power Oscillators**

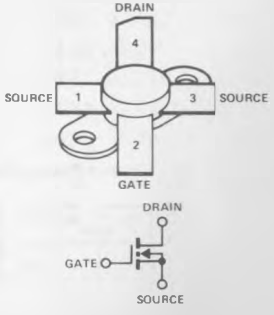
BENEFITS

- Reduces Component Count and Design Time/Effort
  - Withstands Any VSWR
  - High Gain, 10 dB Min @ 200 MHz
  - High Two-Tone Intermodulation Intercept Point
  - Low Small Signal Noise Figure
  - Linear Transfer Characteristics
- Permits Broadband Designs
  - High Input Impedance
  - Low Noise Figure
- Permits Efficient Switching Amplifier Designs
  - High Input Impedance
  - No Storage Delay Time
  - Rise and Fall Time Typically 4 nsec
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage . . . . . .60 V
Maximum Drain-Gate Voltage . . . . . .60 V
Maximum Gate-Source Voltage . . . . . .30 V
Maximum Continuous Drain Current . . . . . 2.0 A
Maximum Dissipation at 25°C Case Temperature . . . . . .25 W
Linear Derating Factor (Derate from 25°C) . . . . 200 mW/°C
Temperature (Operating and Storage) . . . . . –55 to +150°C

S-Package
380-SOE Flange
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	ST	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0, I_D = 10 μA	
2	ST	$I_{D(on)}$	ON-State Drain Current (Note 1)	300			mA	V_{DS} = 25 V, V_{GS} = 5V	
3	DYN	g_{fs}	Forward Transconductance (Note 1)	170	240		m℧	V_{DS} = 24 V, I_D = 0.5 A	
4	DYN	C_{oss}	Common-Source Output Capacitance		34	37	pF	V_{GS} = 0, V_{DS} = 25, f = 1 MHz	(Note 2)
5	DYN	C_{iss}	Common-Source Input Capacitance		32	35	pF	V_{GS} = 0, V_{DS} = 25, f = 1 MHz	(Note 2)
6	DYN	C_{rss}	Reverse Transfer Capacitance		4.8	6.5	pF	V_{GS} = 0, V_{DS} = 25, f = 1 MHz	(Note 2)
7	DYN	G_{ps}	Common-Source Power Gain	10			dB	V_{DS} = 24 V, I_D = 0.2 A, f = 200 MHz	(Note 2)
8	DYN	NF	Small Signal Spot Noise Figure		2.5		dB	V_{DS} = 24 V, I_D = 0.2 A, f = 150 MHz	(Note 2)

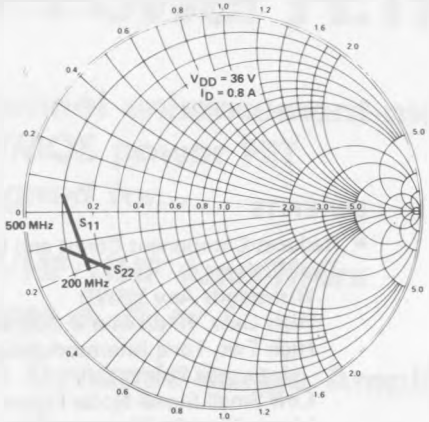
VNAR

NOTES:
1. Pulse test – 80 μsec pulse, 1% duty cycle.
2. Sample test.

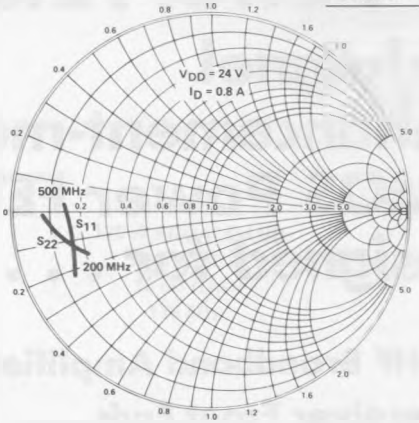
VMP4 PERFORMANCE CHARACTERISTICS

Siliconix

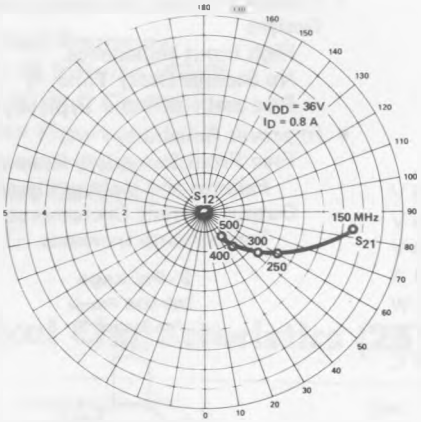
S_{11}/S_{22}



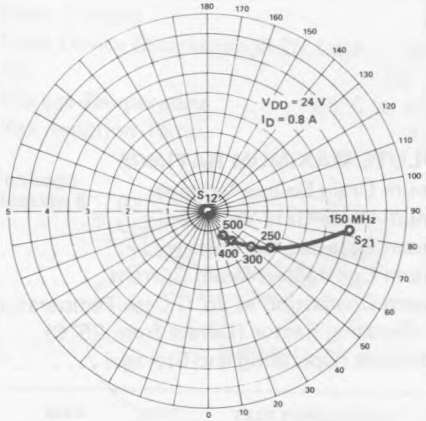
S_{11}/S_{22}



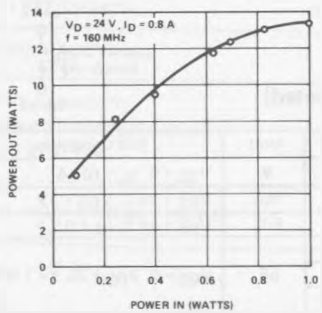
S_{21}/S_{12}



S_{21}/S_{12}

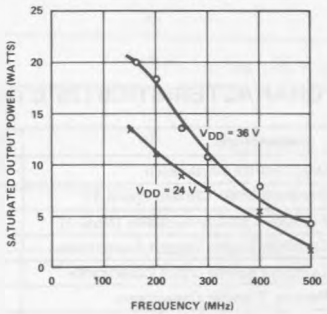


Output Power vs Input Power*



*Conjugate input/output match

Saturated Output Power vs Frequency*
P_{IN} = 1 Watt, I_{DRAIN} = 0.8 A



*Conjugate input/output match

VMP4 PERFORMANCE CHARACTERISTICS (Cont'd)

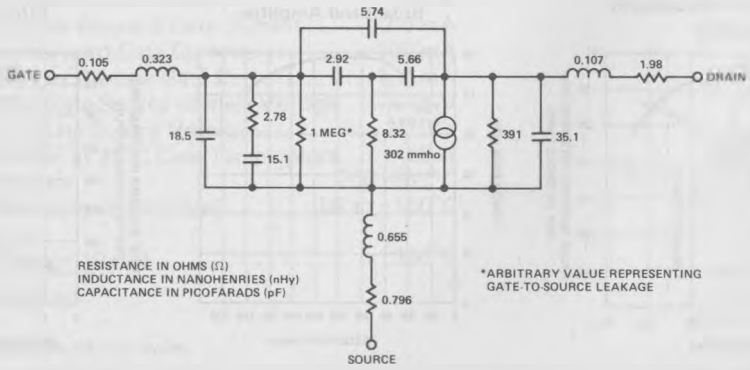
POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S_{11}		S_{21}		S_{12}		S_{22}		S_{21}
	(MAGN	ANGL)	(MAGN	ANGL)	(MAGN	ANGL)	(MAGN	ANGL)	DB
1.00	**1.00**	**–4**	**26.07**	**177.0**	**–48 dB**	**87.3**	**0.78**	**–5**	**28.32**
2.00	1.00	–9	25.98	174.1	0.006	84.3	0.78	–9	28.29
5.00	0.98	–21	25.37	165.4	0.016	75.9	0.77	–23	28.09
10.00	0.94	–41	23.50	152.1	0.029	63.1	0.75	–44	27.42
20.00	0.84	–72	18.76	131.7	0.046	43.6	0.69	–77	25.46
30.00	**0.76**	**–93**	**14.78**	**118.1**	**0.054**	**31.0**	**0.66**	**–99**	**23.39**
40.00	0.72	–107	11.91	108.6	0.058	22.6	0.64	–113	21.52
80.00	0.68	–134	6.30	87.2	0.059	5.5	0.63	–139	15.99
100.00	0.68	–140	4.99	80.4	0.057	1.0	0.64	–144	13.96
150.00	0.72	–148	3.14	67.4	0.049	–4.9	0.68	–151	9.95
200.00	0.76	–153	2.18	57.7	0.039	–4.7	0.72	–156	6.79
300.00	0.83	–161	1.23	44.4	0.025	20.6	0.79	–162	1.79
400.00	0.88	–166	0.78	36.5	0.030	62.0	0.83	–167	–2.10

TWO-PORT Y-PARAMETER MATRIX IN MILLIMHOS

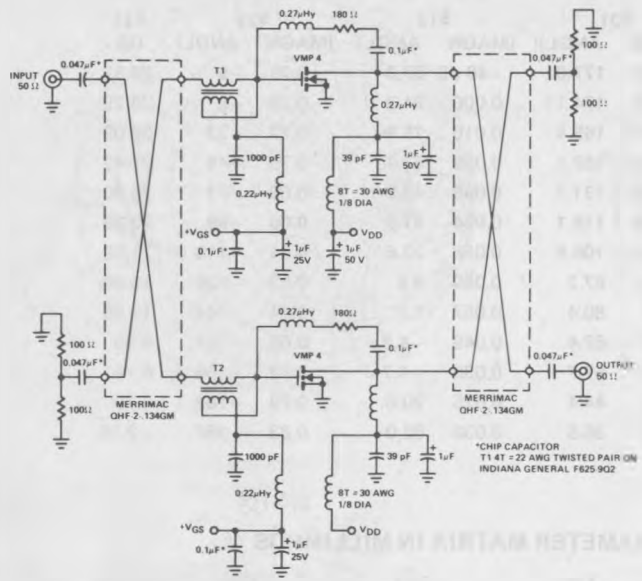
FREQ	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
	(REAL	IMAG)	(REAL	IMAG)	(REAL	IMAG)	(REAL	IMAG)
1.0	**0.00**	**0.28**	**293.40**	**–0.58**	**0.00**	**–0.04**	**2.49**	**0.28**
2.0	0.00	0.56	293.40	–1.16	–0.00	–0.07	2.49	0.56
5.0	0.01	1.41	293.40	–2.89	–0.00	–0.18	2.50	1.41
10.0	0.03	2.81	293.38	–5.79	–0.00	–0.36	2.53	2.81
20.0	0.14	5.62	293.32	–11.58	–0.00	–0.72	2.67	5.62
30.0	**0.31**	**8.43**	**293.23**	**–17.38**	**–0.01**	**–1.07**	**2.89**	**8.43**
40.0	0.54	11.23	293.09	–23.20	–0.01	–1.42	3.21	11.22
80.0	2.17	22.39	292.11	–46.66	–0.04	2.76	5.39	22.24
100.0	3.41	27.92	291.33	–58.57	–0.04	–3.37	7.03	27.60
150.0	7.74	41.47	288.30	–89.10	0.04	–4.66	12.69	40.36
200.0	13.93	54.43	283.21	–120.95	0.43	–5.49	20.51	51.73
300.0	31.89	76.96	263.22	–188.63	3.36	–5.68	41.54	67.76
400.0	55.71	91.32	223.27	–256.91	11.91	–5.18	64.78	70.47

VMP4 Equivalent Circuit

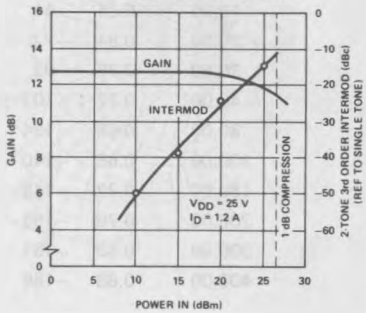


VMP4 PERFORMANCE CHARACTERISTICS (Cont'd)

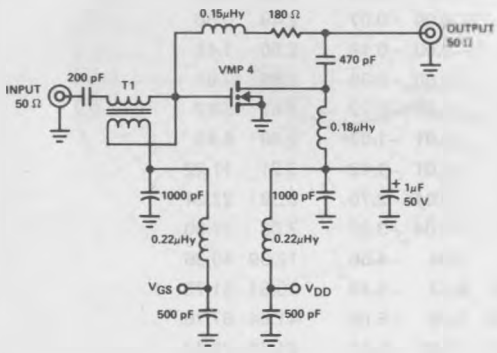
Quadrature Amplifier



Gain & 2-Tone 3rd Order Intermodulation Quadrature (100–160 MHz) Amplifier

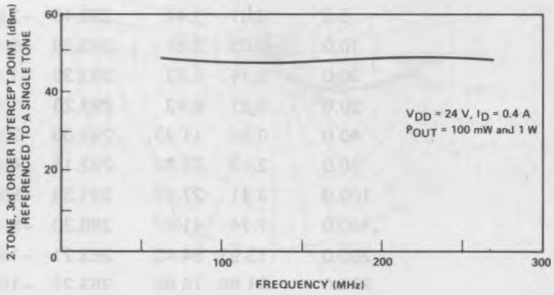


Broadband Amplifier

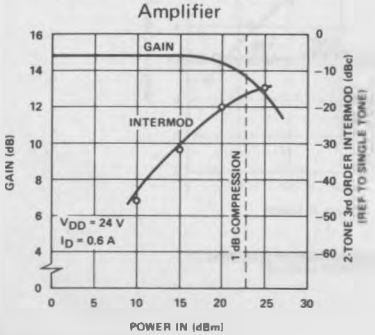


T1 4T #22 AWG TWISTED PAIR ON INDIANA GENERAL F625 9Q2

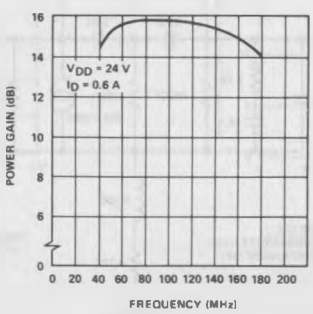
Broadband Amplifier Performance



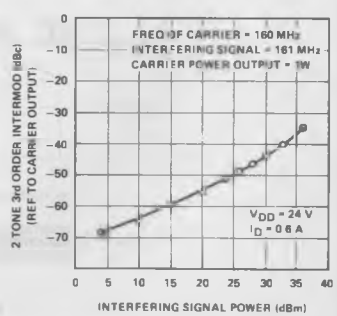
Gain and 2-Tone 3rd Order Intermodulation Broadband Amplifier



Broadband Amplifier



Effects of Interference



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

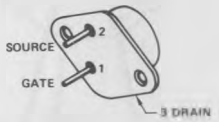
Performance Curves VNAZ
See Section 3

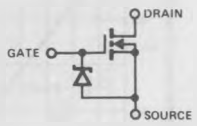
- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **DC to DC Converters**
- **Switching Power Supplies**

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current (I_{GSS} < 100 nA)
  - Threshold Voltage 0.8 to 2.0 V
- Permits More Efficient and Compact Switching Designs
  - Typical T_{ON} and T_{OFF} < 5 nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From a CMOS Logic Gate > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

A-, J- Package
TO-3
See Section 5





ABSOLUTE MAXIMUM RATINGS

*Maximum Drain-Source Voltage	
2N6656	35 V
2N6657	60 V
2N6658	90 V
*Maximum Drain-Gate Voltage	
2N6656	35 V
2N6657	60 V
2N6658	90 V
*Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current (Note 1)	3.0 A
*Maximum Continuous Forward Gate Current	2.0 mA
*Maximum Pulsed Forward Gate Current	100 mA
*Maximum Continuous Reverse Gate Current	100 mA
*Maximum Forward Gate-Source (Zener) Voltage	15 V
*Maximum Reverse Gate-Source Voltage	−0.3 V
*Maximum Dissipation at 25°C Case Temperature	25 W
*Linear Derating Factor	200 mW/°C
*Temperature (Operating and Storage)	−55 to +150°C
*Lead Temperature (1/16" from case for 10 sec)	300°C

*Indicates JEDEC registered data

NOTE:

1. Pulse test — 80 μsec pulse, 1% duty cycle.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

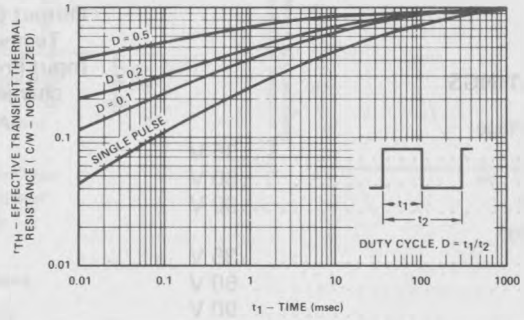
		Characteristic		2N6656			2N6657			2N6658			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2				35			60			90				V_{GS} = 0, I_D = 2.5 mA
3*		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
4*		I_{GSS}	Gate Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
5*						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125 C (Note 2)
6*		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max Rating, V_{GS} = 0
7*						500			500			500		V_{DS} = 0.8 Max Rating, V_{GS} = 0, T_A = 125 C (Note 2)
8					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9*		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 Amp
11					1.0	1.5		1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp
12					0.9			0.9			1.3			V_{GS} = 10 V, I_D = 0.5 Amp
13*					1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 Amp
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 Amp
15*	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0, f = 1 kHz
16		g_{fs}	Forward Transconductance (Note 1)	170	250		170	250		170	250		mΩ	V_{DS} = 24 V, I_D = 0.5 Amp
17*		C_{iss}	Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
18*		C_{ds}	Drain-Source Capacitance (Note 2)			40			40			40		
19		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10		V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
20*						35			35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0 MHz
21*		$t_{d(on)}$	Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
22*		t_r	Rise Time (Note 2)		2	5		2	5		2	5		
23*		$t_{d(off)}$	Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
24*		t_f	Fall Time (Note 2)		2	5		2	5		2	5		

*Indicates JEDEC registered data

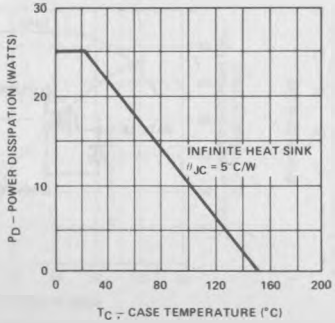
VNAZ

NOTES:
1. Pulse test—80 μsec pulse, 1% duty cycle.
2. Sample test

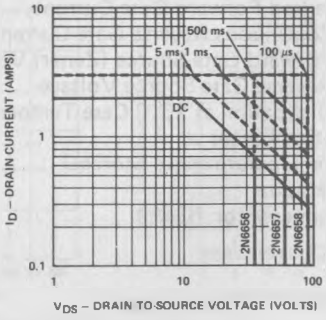
Thermal Response



Power Dissipation vs Case Temperature



DC Safe Operating Region T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Switching Power Supplies**

Performance Curves VNAZ
See Section 3

BENEFITS

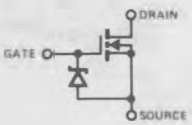
- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current ($I_{GSS} < 100$ nA)
  - Threshold Voltage 0.8 to 2.0 V
- Permits More Efficient and Compact Switching Designs
  - Typical T_{ON} and $T_{OFF} < 5$ nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From a CMOS Logic Gate > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected from Static Discharge

ABSOLUTE MAXIMUM RATINGS

*Maximum Drain-Source Voltage	
2N6659	35 V
2N6660	60 V
2N6661	90 V
*Maximum Drain-Gate Voltage	
2N6659	35 V
2N6660	60 V
2N6661	90 V
*Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
*Maximum Continuous Forward Gate Current	2.0 mA
*Maximum Pulsed Forward Gate Current	100 mA
*Maximum Continuous Reverse Gate Current	100 mA
*Maximum Forward Gate-Source (Zener) Voltage	15 V
*Maximum Reverse Gate-Source Voltage	−0.3 V
*Maximum Dissipation at 25°C Case Temperature	8.33 W
*Linear Derating Factor	67 mW/°C
*Temperature (Operating and Storage)	−55 to +150°C
*Lead Temperature (1/16" from case for 10 seconds)	300°C

*Indicates JEDEC registered data

B-, K- Package
TO-39
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N6659			2N6660			2N6661			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2				35			60			90				V_{GS} = 0, I_D = 2.5 mA
3*		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
4*		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
5*						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125 C (Note 2)
6*		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0
7*						500			500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125 C (Note 2)
8					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9*		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 Amp
11					1.0	1.5		1.0	1.5		1.1	1.6		V_{GS} = 5 V, I_D = 0.3 Amp
12					0.9			0.9			1.3			V_{GS} = 10 V, I_D = 0.5 Amp
13*					1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 Amp
14*		$r_{DS(on)}$	Static Drain-Source ON-State Resistance (Note 1)		1.6	1.8		2.0	3.0		3.0	4.0	Ω	V_{GS} = 10 V, I_D = 1.0 Amp
15*	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0, f = 1 kHz
16		g_{fs}	Forward Transconductance (Note 1)	170	250		170	250		170	250		mΣ	V_{DS} = 24 V, I_D = 0.5 Amp
17*		C_{iss}	Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 25 V, f = 1.0 MHz
18*		C_{ds}	Drain-Source Capacitance (Note 2)			40			40			40		
19		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10		V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
20*						35			35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0 MHz
21*		$t_{d(on)}$	Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
22*		t_r	Rise Time (Note 2)		2	5		2	5		2	5		
23*		$t_{d(off)}$	Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
24*		t_f	Fall Time (Note 2)		2	5		2	5		2	5		

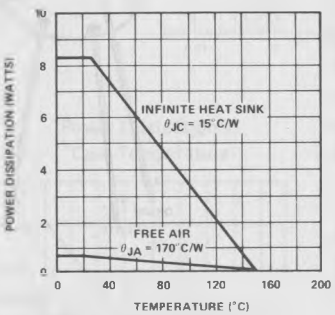
*Indicates JEDEC registered data

VNAZ

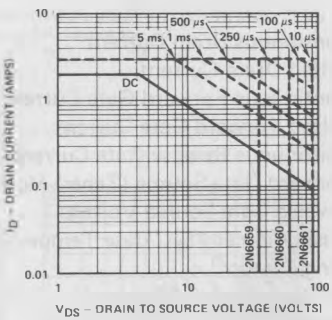
NOTES:

1. Pulse test—80 μsec pulse, 1% duty cycle.
2. Sample test.

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

- **High Speed Line Drivers**
- **TTL to High Current Interface**
- **CMOS to High Current Interface**
- **Transformer Drivers**
- **Relay Drivers**
- **LED Digit Strobe Drivers**

Performance Curves VNK See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	100 V
Maximum Drain-Gate Voltage	100 V
Maximum Continuous Drain Current	0.5 A
Maximum Pulsed Drain Current	1.0 A
Maximum Continuous Forward Gate Current	0.5 mA
Maximum Pulsed Forward Gate Current (Note 1)	10 mA
Maximum Continuous Reverse Gate Current	10 mA
Maximum Forward Gate-Source Voltage	15 V
Maximum Reverse Gate-Source Voltage	0.3 V
Maximum Dissipation at 25°C Ambient Temperature[2]	1 W
Linear Derating Factor	8 mW/°C
Maximum Junction Temperatures	−40°C to +150°C
Maximum Storage Temperatures	−40°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

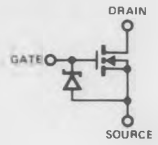
NOTE:

1. Pulse Test — 80 μs pulse, 1% duty cycle.

2. Power dissipation measured with device soldered to a minimum of 1 square inch of 2 ounce copper clad board and with a lead length ≤ 1/8 inch.

M — Package

TO-237
(TO-92 PLUS)
See Section 5



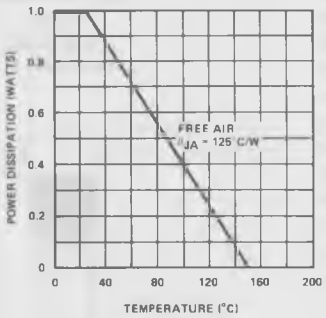
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	100			V	V_{GS} = 0 V, I_D = 100 μA	
2		$V_{GS(th)}$	Gate Threshold Voltage			2.0	V	V_{DS} = V_{GS}, I_D = 15mA	
3		I_{GSS}	Gate-Body Leakage			10	μA	V_{GS} = 10 V, V_{DS} =0	Note 2
4		I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = 60 V, V_{GS} =0	
5		$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25 V, V_{GS} = 5 V	Note 1
6				0.50				V_{DS} = 25 V, V_{GS} = 10 V	
7		$V_{DS(on)}$	Drain-Source ON Voltage			1.2	V	V_{GS} = 5V, I_D = 120mA	
8	DYNAMIC	g_{fs}	Forward Transconductance	100	200		m℧	V_{DS} = 15 V, I_D = 0.5 A	
9		C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
10		C_{oss}	Output Capacitance		16				
11		C_{rss}	Feedback Capacitance		2				
12		t_{ON}	Turn-ON Time		5		ns	See Test Circuit for VNK (Section 3)	
13		t_{OFF}	Turn OFF Time		5				

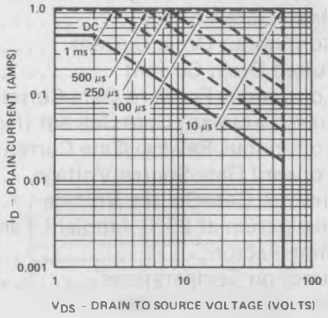
NOTES: 1. Pulse test — 80 μs pulse, 1% duty cycle.
2. Sample test.

VNK

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_A = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

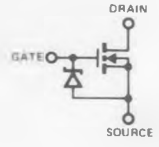
- **High Speed Line Drivers**
- **TTL to High Current Interface**
- **CMOS to High Current Interface**
- **Transformer Drivers**
- **Relay Drivers**
- **LED Digit Strobe Drivers**

Performance Curves VNK
See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

M-Package
TO-237
(TO-92 PLUS)
See Section 5



ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	30 V
Maximum Drain-Gate Voltage	30 V
Maximum Continuous Drain Current	0.5 A
Maximum Pulsed Drain Current	1.0 A
Maximum Continuous Forward Gate Current	0.5 mA
Maximum Pulsed Forward Gate Current (Note 1)	10 mA
Maximum Continuous Reverse Gate Current	10 mA
Maximum Forward Gate-Source Voltage	15 V
Maximum Reverse Gate-Source Voltage	0.3 V
Maximum Dissipation at 25°C Ambient Temperature	1 W
Linear Derating Factor	8 mW/°C
Maximum Junction Temperatures	−40°C to +150°C
Maximum Storage Temperatures	−40°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

NOTE:

1. Pulse Test — 80 μs pulse, 1% duty cycle.

2. Power dissipation measured with device soldered to a minimum of 1 square inch of 2 ounce copper clad board and with a lead length ≤ 1/8 inch.

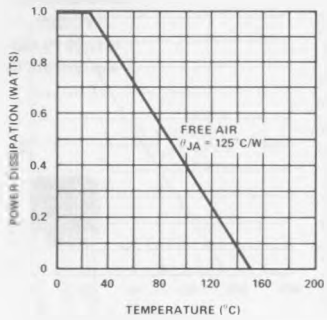
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	30			V	V_{GS} = 0 V, I_D = 100 μA	
2		$V_{GS(th)}$	Gate Threshold Voltage			2.0	V	V_{DS} = V_{GS}, I_D = 5mA	
3		I_{GSS}	Gate-Body Leakage			10	μA	V_{GS} = 10 V, V_{DS} =0	Note 2
4		I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = 30 V V_{GS} =0	
5		$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25 V, V_{GS} = 5 V	Note 1
6				0.50				V_{DS} = 25 V, V_{GS} = 10 V	
7		$V_{DS(on)}$	Drain-Source ON Voltage			2.5	V	V_{GS} = 10 V, I_D = 0.5 A	
8	DYNAMIC	g_{fs}	Forward Transconductance	100	200		m℧	V_{DS} = 15 V, I_D = 0.5 A	
9		C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
10		C_{oss}	Output Capacitance		16				
11		C_{rss}	Feedback Capacitance		2				
12		t_{ON}	Turn-ON Time		5		ns	See Test Circuit for VNK (Section 3)	
13		t_{OFF}	Turn-OFF Time		5				

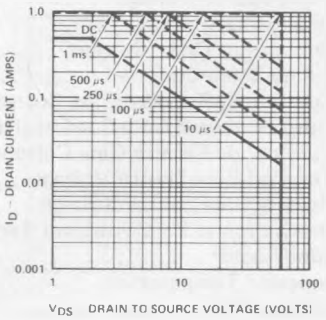
NOTES: 1. Pulse test — 80 μs pulse, 1% duty cycle.
2. Sample test.

VNK

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_A = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

- **High Speed Line Drivers**
- **TTL to High Current Interface**
- **CMOS to High Current Interface**
- **Transformer Drivers**
- **Relay Drivers**
- **LED Digit Strobe Drivers**

Performance Curves VNK See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

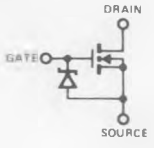
Maximum Drain-Source Voltage	60 V
Maximum Drain-Gate Voltage	60 V
Maximum Continuous Drain Current	0.5 A
Maximum Pulsed Drain Current	1.0 A
Maximum Continuous Forward Gate Current	0.5 mA
Maximum Pulsed Forward Gate Current (Note 1)	10 mA
Maximum Continuous Reverse Gate Current	10 mA
Maximum Forward Gate-Source Voltage	15 V
Maximum Reverse Gate-Source Voltage	0.3 V
Maximum Dissipation at 25°C Ambient Temperature	1 W
Linear Derating Factor	8 mW/°C
Maximum Junction Temperatures	−40°C to +150°C
Maximum Storage Temperatures	−40°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

NOTE:

1. Pulse Test — 80 μs pulse, 1% duty cycle.

M-Package

TO-237
(TO-92 PLUS)
See Section 5



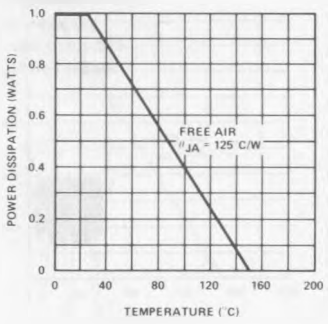
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0 V, I_D = 100 μA	
2		$V_{GS(th)}$	Gate Threshold Voltage	0.3		2.5	V	V_{DS} = V_{GS}, I_D = 1 mA	
3		I_{GSS}	Gate-Body Leakage			10	μA	V_{GS} = 10 V, V_{DS} =0	Note 2
4		I_{DSS}	Zero Gate Voltage Drain Current			10		V_{DS} = 40 V, V_{GS} =0	
5		$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25 V, V_{GS} = 5 V	Note 1
6				0.50				V_{DS} = 25 V, V_{GS} = 10 V	
7		$V_{DS(on)}$	Drain-Source ON Voltage			2.5	V	V_{GS} = 10 V, I_D = 0.5 A	
8	DYNAMIC	g_{fs}	Forward Transconductance	100	200		m℧	V_{DS} = 15 V, I_D = 0.5 A	
9		C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
10		C_{oss}	Output Capacitance		16				
11		C_{rss}	Feedback Capacitance		2				
12		t_{ON}	Turn-ON Time		5		ns	See Test Circuit for VNK (Section 3)	
13		t_{OFF}	Turn-OFF Time		5				

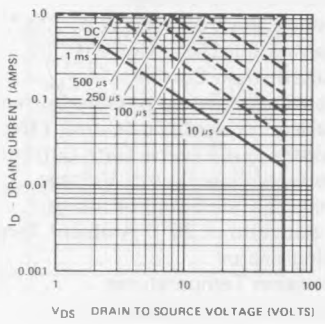
NOTES: 1. Pulse test – 80 μs pulse, 1% duty cycle.
2. Sample test.

VNK

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_A = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Switching Power Supplies**

Performance Curves VNAZ
See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current ($I_{GSS} < 500$ nA)
  - Threshold Voltage 0.8 to 2.0 V
- Permits More Efficient and Compact Switching Supply Designs
  - Typical t_{on} and $t_{off} < 10$ ns
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic Gate > 100
  - Easily Paralleled With Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

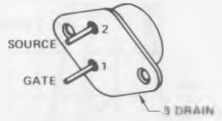
Maximum Drain-Source Voltage	
VN30AA, VN35AA	35 V
VN67AA	60 V
VN89AA	80 V
VN90AA	90 V
Maximum Drain-Gate Voltage	
VN30AA, VN35AA	35 V
VN67AA	60 V
VN89AA	80 V
VN90AA	90 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current (Note 1)	3.0 A
Maximum Continuous Forward Gate Current	2.0 mA
Maximum Pulsed Forward Gate Current	100 mA
Maximum Continuous Reverse Gate Current	100 mA
Maximum Forward Gate-Source (Zener) Voltage	15 V
Maximum Reverse Gate-Source Voltage	-0.3 V
Maximum Dissipation at 25°C Case Temperature	25 W
Linear Derating Factor	200 mW/°C
Temperature (Operating and Storage)	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

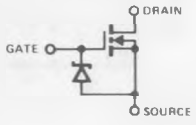
NOTE:

1. Pulse test — 80 μsec pulse, 1% duty cycle.

A-, J- Package

TO-3
See Section 5





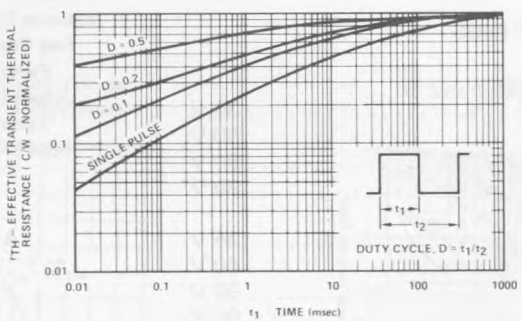
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN30AA			VN35AA			VN67AA			VN89AA			VN90AA			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			35			60			80			90			V	I_D = 10 μA, V_{GS} = 0
2		$V_{GS\ (th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			I_D = 1.0 mA, V_{DS} = V_{GS}
3		I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{GS} = 10 V, V_{DS} = 0
4		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10		V_{DS} = 25 V, V_{GS} = 0
5		$R_{DS\ (on)}$	Drain-Source ON-State Resistance (Note 1)			6.0			4.5			5.1			5.1			6.0	Ω	V_{GS} = 5 V, I_D = 300 mA
						5.0		2.0	2.5		2.2	3.5		3.8	4.5			5.0		V_{GS} = 10 V, I_D = 1.0 A
6		$I_{D\ (on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25 V, V_{GS} = 10 V
7	DYNAMIC	g_{fs}	Forward Transconductance	150	250		150	250		150	250		150	250		150	250		m℧	V_{DS} = 25 V, I_D = 0.5 A
8		C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
9		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10		
10		C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40		
11		t_{on}	Turn-ON Time (Note 2)			10			10			10			10			10	ns	See Switching Time Test Circuit VNAZ, Section 3
12		t_{off}	Turn-OFF Time (Note 2)			10			10			10			10			10		

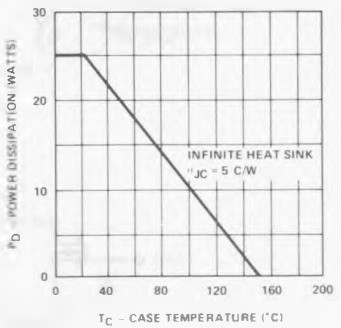
NOTES: 1. Pulse Test – 80 μs, 1% duty cycle
2. Sample Test

VNAZ

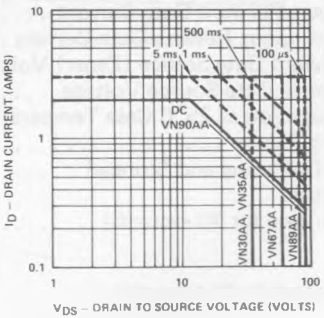
Thermal Response



Power Dissipation vs Case Temperature



DC Safe Operating Region
T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Switching Power Supplies**

Performance Curves VNAZ
See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current ($I_{GSS} < 500$ nA)
- Permits More Efficient and Compact Switching Supply Designs
  - Typical t_{on} and $t_{off} < 10$ ns
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic Gate > 100
  - Easily Paralleled With Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

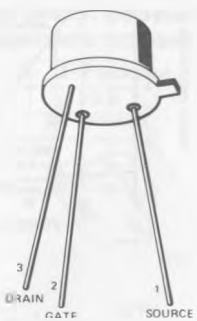
Maximum Drain-Source Voltage	
VN30AB, VN35AB	35 V
VN67AB	60 V
VN89AB	80 V
VN90AB	90 V
Maximum Drain-Gate Voltage	
VN30AB, VN35AB	35 V
VN67AB	60 V
VN89AB	80 V
VN90AB	90 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current (Note 1)	3.0 A
Maximum Continuous Forward Gate Current	2.0 mA
Maximum Pulsed Forward Gate Current	100 mA
Maximum Continuous Reverse Gate Current	100 mA
Maximum Forward Gate-Source (Zener) Voltage	15 V
Maximum Reverse Gate-Source Voltage	−0.3 V
Maximum Dissipation at 25°C Case Temperature	8.33 W
Linear Derating Factor	67 mW/°C
Temperature (Operating and Storage)	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

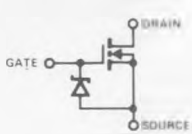
NOTE:

1. Pulse test — 80 μsec pulse, 1% duty cycle.

B-, K- Package

TO-39
See Section 5





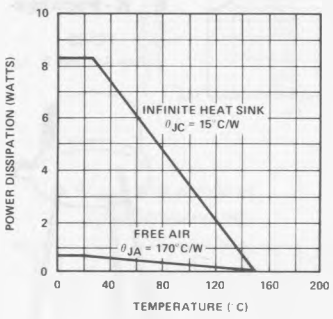
ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		VN30AB			VN35AB			VN67AB			VN89AB			VN90AB			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			35			60			80			90			V	I_D = 10 μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			I_D = 1.0 mA, V_{DS} = V_{GS}
3		I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{GS} = 10 V, V_{DS} = 0
4		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10		V_{DS} = 25 V, V_{GS} = 0
5		$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)			6.0			4.5			5.1			5.1			6.0	Ω	V_{GS} = 5 V, I_D = 300 mA
						5.0		2.0	2.5		2.2	3.5		3.8	4.5			5.0		V_{GS} = 10 V, I_D = 1.0 A
6		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25 V, V_{GS} = 10 V
7	DYNAMIC	g_{fs}	Forward Transconductance		250			250			250			250			250		m℧	V_{DS} = 25 V, I_D = 0.5 A
8		C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
9		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10		
10		C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40		
11		t_{on}	Turn-ON Time (Note 2)			10			10			10			10			10	ns	See Switching Time Test Circuit VNAZ, Section 3
12		t_{off}	Turn-OFF Time (Note 2)			10			10			10			10			10		

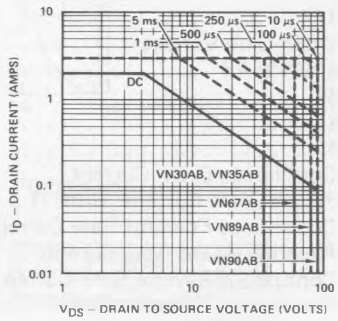
NOTES: 1. Pulse Test – 80 μs, 1% duty cycle
2. Sample Test

VNAZ

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

Performance Curves VNAR
See Section 3

- **RF Power Amplifiers**
- **High Current Analog Switching**
- **Laser Diode Pulsing**
- **Bridge Switching**

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage
- VN33AJ, VN35AJ . . . . . 35 V
- VN66AJ, VN67AJ . . . . . 60 V
- VN98AJ, VN99AJ . . . . . 90 V

Maximum Drain-Gate Voltage
- VN33AJ, VN35AJ . . . . . 35 V
- VN66AJ, VN67AJ . . . . . 60 V
- VN98AJ, VN99AJ . . . . . 90 V

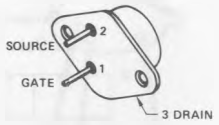
Maximum Continuous Drain Current . . . . . 2.0 A
Maximum Pulsed Drain Current (Note 1) . . . . . 3.0 A
Maximum Gate-Source Voltage . . . . . ±30 V
Maximum Dissipation at 25°C Case Temperature . . . . . 25 W
Linear Derating Factor . . . . . 200 mW/°C
Temperature (Operating and Storage) . . . . . −55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

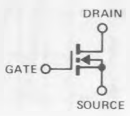
NOTE:
1. Pulse test — 80 μsec pulse, 1% duty cycle.

BENEFITS

- Reduces Component Count and Design Time/Effort
  - Withstands Any VSWR
  - High Gain, 10 dB Min @ 200 MHz
  - High Two-Tone Intermodulation Intercept Point
  - Low Small Signal Noise Figure
  - Linear Transfer Characteristic
- Permits Broadband Designs
  - High Input Impedance
  - Low Noise Figure
- Permits Efficient Switching Power Supply Designs
  - High Input Impedance
  - No Storage Delay Time
  - Rise and Fall Time Typically 4 nsec
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases As Temperature Increases

A-, J-Package
TO-3
See Section 5





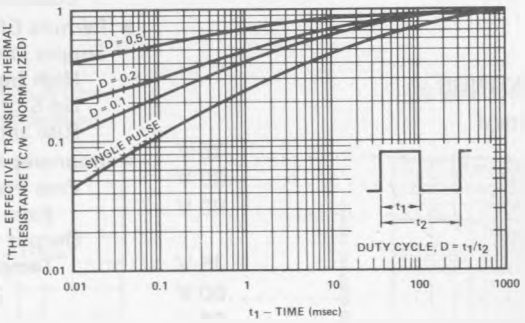
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN33AJ VN35AJ Min	VN33AJ VN35AJ Typ	VN33AJ VN35AJ Max	VN66AJ VN67AJ Min	VN66AJ VN67AJ Typ	VN66AJ VN67AJ Max	VN98AJ VN99AJ Min	VN98AJ VN99AJ Typ	VN98AJ VN99AJ Max	Unit	Test Conditions
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2		$V_{GS(th)}$	Gate-Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
3		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
4						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125°C (Note 2)
5		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0
6						500			500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)
7					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
8		$I_{D(on)}$	ON-State Drain Current	1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25 V, V_{GS} = 10 V
9		$V_{DS(on)}$	Drain-Source Saturation Voltage VN33AJ VN66AJ VN98AJ		1.0			1.0			1.1		V	V_{GS} = 5 V, I_D = 0.3 A
10						1.8			3.0			4.0		V_{GS} = 10 V, I_D = 1.0 A (Note 1)
11			VN35AJ VN67AJ VN99AJ		1.0			1.1			1.2			V_{GS} = 5 V, I_D = 0.3 A
12						2.5			3.5			4.5		V_{GS} = 10 V, I_D = 1.0 A
13	DYNAMIC	g_{fs}	Forward Transconductance	170	250		170	250		170	250		m℧	V_{DS} = 24 V, I_D = 0.5 A
14		C_{iss}	Input Capacitance		33	40		33	40		33	40	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz (Note 2)
15		C_{oss}	Common-Source Output Capacitance		38	45		35	40		32	40		
16		C_{rss}	Reverse Transfer Capacitance		7	10		6	10		5	10		
17		t_{on}	Turn ON Time		3	8		3	8		3	8	ns	See Switching Time Test Circuit VNAR, Section 3 (Note 2)
18		t_{off}	Turn OFF Time		3	8		3	8		3	8		

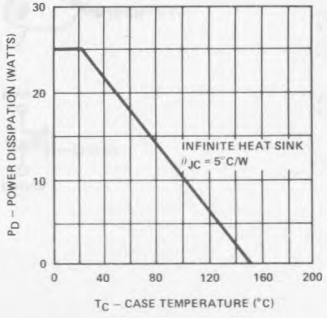
NOTES:
1. Pulse test—80 μs, 1% duty cycle.
2. Sample test.

VNAR

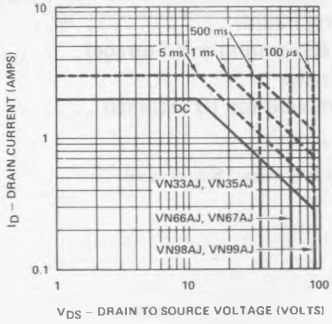
Thermal Response



Power Dissipation vs Case Temperature



DC Safe Operating Region T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

Performance Curves VNAR
See Section 3

- **RF Power Amplifiers**
- **High Current Analog Switching**
- **Laser Diode Pulsing**
- **Bridge Switching**

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage
- VN33AK, VN35AK . . . . . 35 V
- VN66AK, VN67AK . . . . . 60 V
- VN98K, VN99AK . . . . . 90 V

Maximum Drain-Gate Voltage
- VN33AK, VN35AK . . . . . 35 V
- VN66AK, VN67AK . . . . . 60 V
- VN98AK, VN99AK . . . . . 90 V

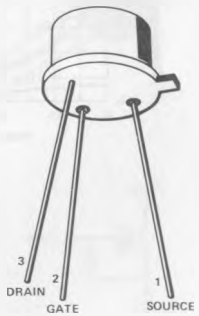
Maximum Continuous Drain Current . . . . . 2.0 A
Maximum Pulsed Drain Current (Note 1) . . . . . 3.0 A
Maximum Gate-Source Voltage . . . . . ±30 V
Maximum Dissipation at 25°C Case Temperature . . . . 8.33 W
Linear Derating Factor . . . . . 67 mW/°C
Temperature (Operating and Storage) . . . . . −55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

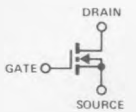
NOTE:
1. Pulse test — 80 μsec pulse, 1% duty cycle.

BENEFITS

- Reduces Component Count and Design Time/Effort
  - Withstands Any VSWR
  - High Gain, 10 dB Min @ 200 MHz
  - High Two-Tone Intermodulation Intercept Point
  - Low Small Signal Noise Figure
  - Linear Transfer Characteristic
- Permits Broadband Designs
  - High Input Impedance
  - Low Noise Figure
- Permits Efficient Switching Power Supply Designs
  - High Input Impedance
  - No Storage Delay Time
  - Rise and Fall Time Typically 4 nsec
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases As Temperature Increases

B-, K- Package
TO-39
See Section 5





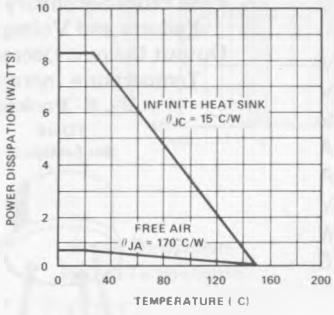
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN33AK VN35AK			VN66AK VN67AK			VN98AK VN99AK			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA	
2		$V_{GS(th)}$	Gate-Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA	
3		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0	
4						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125°C (Note 2)	
5		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
6						500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
7					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0	
8		$I_{D(on)}$	ON-State Drain Current	1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25 V, V_{GS} = 10 V	
9		$V_{DS(on)}$	Drain-Source Saturation Voltage VN33AK VN66AK		1.0			1.0			1.1		V	V_{GS} = 5 V, I_D = 0.3 A	(Note 1)
10			VN98AK			1.8			3.0			4.0		V_{GS} = 10 V, I_D = 1.0 A	
11			VN35AK VN67AK		1.0			1.1			1.2			V_{GS} = 5 V, I_D = 0.3 A	
12			VN99AK			2.5			3.5			4.5		V_{GS} = 10 V, I_D = 1.0 A	
13		g_{fs}	Forward Transconductance	170	250		170	250		170	250		mℑ	V_{DS} = 24 V, I_D = 0.5 A	
14	DYNAMIC	C_{iss}	Input Capacitance		33	40		33	40		33	40	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz (Note 2)	
15		C_{oss}	Common Source Output Capacitance		38	45		35	40		32	40			
16		C_{rss}	Reverse Transfer Capacitance		7	10		6	10		5	10			
17		t_{on}	Turn ON Time		3	8		3	8		3	8	ns	See Switching Time Test Circuit VNAR, Section 3	(Note 2)
18		t_{off}	Turn OFF Time		3	8		3	8		3	8			

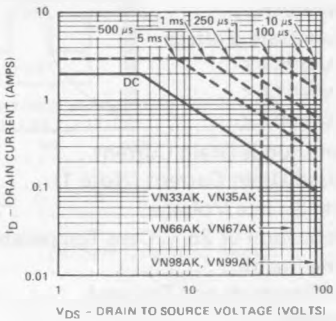
VNAR

NOTES
1. Pulse test—80 μs pulse, 1% duty cycle.
2. Sample test.

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Power Switching**

Performance Curves VNAZ See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

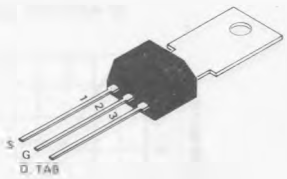
Maximum Drain-Source Voltage	
VN40AF	40 V
VN67AF	60 V
VN89AF	80 V
Maximum Drain-Gate Voltage	
VN40AF	40 V
VN67AF	60 V
VN89AF	80 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
Maximum Continuous Forward Gate Current	2.0 mA
Maximum Pulsed Forward Gate Current (Note 1)	100 mA
Maximum Continuous Reverse Gate Current	100 mA
Maximum Forward Gate-Source (Zener) Voltage	15 V
Maximum Reverse Gate-Source Voltage	−0.3 V
Maximum Dissipation at 25°C Case Temperature	15 W
Linear Derating Factor	120 mW/°C
Temperature (Operating and Storage)	−40 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

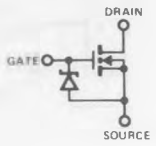
NOTE:

1. Pulse test – 80 μsec pulse, 1% duty cycle.

F - Package

TO-202
See Section 5





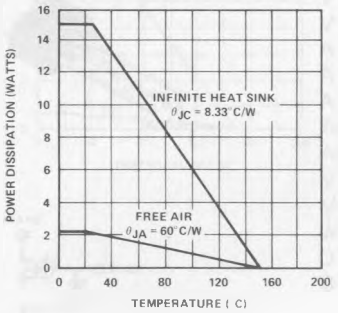
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN40AF			VN67AF			VN89AF			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 500μA
2				40			60			80				V_{GS} = 0, I_D = 2.5 mA
3		$V_{GS(th)}$	Gate Threshold Voltage	0.6	1.2		0.8	1.2		0.8	1.2			V_{DS} = V_{GS}, I_D = 1 mA
4		I_{GSS}	Gate Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10 V, V_{DS} = 0
5						100			100			100		V_{GS} = 10 V, V_{DS} = 0, T_A = 125°C (Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current		10	500		10	500		10	500		V_{DS} = Max. Rating, V_{GS} = 0
7					100	5000		100	5000		100	5000		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)
8					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 A
11					1.0	2.0		1.0	1.7		1.4	1.9		V_{GS} = 5V, I_D = 0.3 A
12					1.0			1.0			1.3			V_{GS} = 10 V, I_D = 0.5 A
13					2.0	5.0		2.0	3.5		3.0	4.5		V_{GS} = 10 V, I_D = 1.0 A
14	DYNAMIC	g_m	Forward Transconductance (Note 1)		250			250			250		mℑ	V_{DS} = 24 V, I_D = 0.5 A
15		C_{iss}	Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 25 V, f = 1.0 MHz
16		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10		
17		C_{oss}	Common-Source Output Capacitance (Note 2)			50			50			50		
18		$t_{d(on)}$	Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
19		t_r	Rise Time (Note 2)		2	5		2	5		2	5		
20		$t_{d(off)}$	Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
21		t_f	Fall Time (Note 2)		2	5		2	5		2	5		

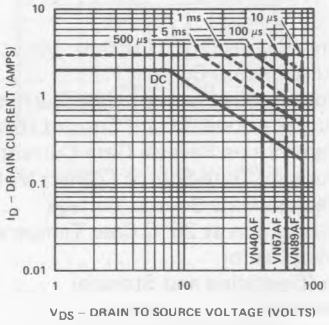
NOTES: 1. Pulse test – 80 μs pulse, 1% duty cycle.
2. Sample test.

VNAZ

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_C = 25°C



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

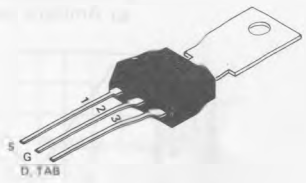
- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Power Switching**

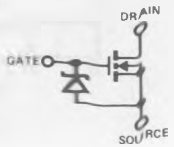
Performance Curves VNAZ
See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

F-Package
TO-202
See Section D





ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	
VN46AF	40 V
VN66AF	60 V
VN88AF	80 V
Maximum Drain-Gate Voltage	
VN46AF	40 V
VN66AF	60 V
VN88AF	80 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
Maximum Continuous Forward Gate Current	2.0 mA
Maximum Pulsed Forward Gate Current (Note 1)	100 mA
Maximum Continuous Reverse Gate Current	100 mA
Maximum Forward Gate-Source (Zener) Voltage	15 V
Maximum Reverse Gate-Source Voltage	−0.3 V
Maximum Dissipation at 25°C Case Temperature	15 W
Linear Derating Factor	120 mW/°C
Temperature (Operating and Storage)	−40 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

NOTE:

1. Pulse test — 80 μsec pulse, 1% duty cycle.

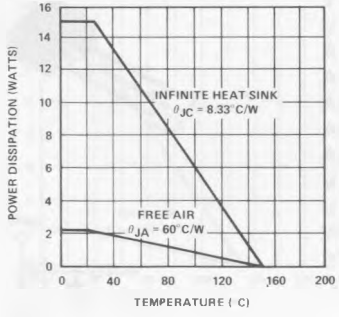
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN46AF			VN66AF			VN88AF			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 500 μA
2				40			60			80				V_{GS} = 0, I_D = 2.5 mA
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.7		0.8	1.7		0.8	1.7			V_{DS} = V_{GS}, I_D = 1 mA
4		I_{GSS}	Gate Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10 V, V_{DS} = 0
5						100			100			100		V_{GS} = 10 V, V_{DS} = 0, T_A = 125°C (Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current		10	500		10	500		10	500		V_{DS} = Max. Rating, V_{GS} = 0
7					100	5000		100	5000		100	5000		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)
8					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 A
11					1.0	1.5		1.0	1.5		1.4	1.7		V_{GS} = 5V, I_D = 0.3 A
12					1.0			1.0			1.3			V_{GS} = 10 V, I_D = 0.5 A
13					2.0	3.0		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 A
14	DYNAMIC	g_m	Forward Transconductance (Note 1)	150	250		150	250		150	250		m℧	V_{DS} = 24 V, I_D = 0.5 A
15		C_{iss}	Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 25 V, f = 1.0 MHz
16		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10		
17		C_{oss}	Common-Source Output Capacitance (Note 2)			50			50			50		
18		$t_{d(on)}$	Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
19		t_r	Rise Time (Note 2)		2	5		2	5		2	5		
20		$t_{d(off)}$	Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
21		t_f	Fall Time (Note 2)		2	5		2	5		2	5		

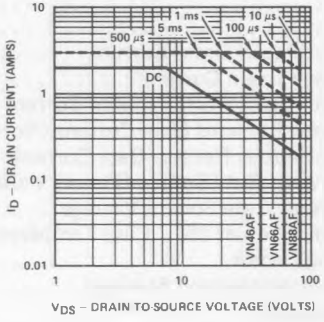
NOTES: 1. Pulse test – 80 μs pulse, 1% duty cycle.
2. Sample test.

VNAZ

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_C = 25°C



n-channel enhancement-mode VMOS Power FET *designed for . . .*

Siliconix

- **Motor Controllers**
- **Switching Power Supplies**
- **Linear Amplifiers**
- **Switching Amplifiers**

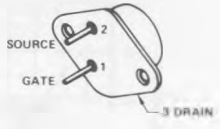
Performance Curves VNG See Section 3

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  Low Drive Current ($I_{GSS} < 100$ nA)
- Permits Very Efficient High Density Switching Designs
  Typical t_{on} and $t_{off} < 50$ nsec

A-, J-Package

TO-3
See Section 5



ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	60 V
Maximum Drain-Gate Voltage	60 V
Maximum Continuous Drain Current	12.5 A
Maximum Pulse Drain Current (Note 1)	15 A
Maximum Gate-Source Voltage	±30 V
Maximum Dissipation at 25°C Case Temperature	80 W
Linear Derating Factor	1.56°C/W
Temperature (Operating and Storage)	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

NOTE:

1. Pulse test — 300 μsec pulse, 1% duty cycle.

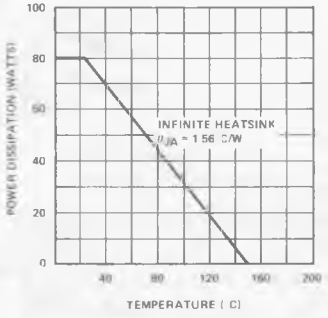
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0V, I_D = 500 μA
2		$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.7	4.0		V_{DS} = V_{GS}, I_D = 10 mA
3		I_{GSS}	Gate-Body Leakage		0.3	100	nA	V_{GS} = 12 V, V_{DS} = 0
4		I_{DSS}	Zero Gate Voltage Drain Current			500	μA	V_{DS} = Max. Rating, V_{GS} = 0
5		$I_{D(on)}$	ON-State Drain Current	12.5			A	V_{DS} = 25 V, V_{GS} = 12 V (Note 1)
6		$R_{DS(on)}$	Drain-Source ON Resistance		0.3	0.4	Ω	V_{GS} = 12 V, I_D = 10 A
7	DYNAMIC	g_{fs}	Forward Transconductance	1.5	2.2		℧	V_{DS} = 20 V, I_D = 5 A (Note 1)
8		C_{iss}	Input Capacitance		700		pF	V_{GS} = 0, V_{DS} = 25 V, f = 1.0 MHz
9		C_{rss}	Reverse Transfer Capacitance		25			
10		C_{oss}	Output Capacitance		325			
11		t_{on}	Turn-ON Time		45		ns	V_{DS} = 10 V, I_D = 10 A (Note 2) R_L = 1 Ω, R_S = 50 Ω
12		t_{off}	Turn-OFF Time		45			

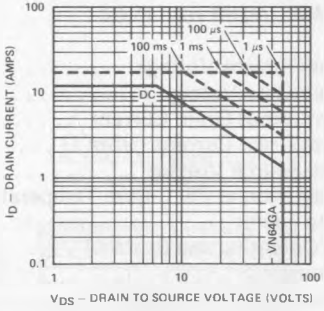
NOTES: 1. Pulse Test — 300 μs, 1% duty cycle
2. See switching time test circuit

VNG

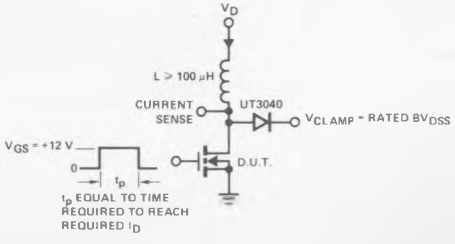
Power Dissipation vs Case or Ambient Temperature



DC and Inductive Safe Operating Region T_C = 25°C



Inductive Safe Operating Area Test Circuit



VMOS costs less than you think.

Now, our VMOS Power FETs are in volume production . . . and available off the shelf, at low prices.
Contemplate how these devices permit simpler circuits with reduced component counts and lower *system* costs.
And after thinking about the exciting ways in which you could exploit VMOS, consider the VN64GA that can drive large loads direct from μP outputs; or the VN10KM that switches within 5 nanoseconds.

Siliconix
europe

The first Quad VMOS

VQ1000CJ

Available now, with 4 independently accessible power FET switches in a single package. Thus, the already low component count for VMOS based systems can be reduced still further... with higher switching densities and lower assembly costs.

This device offers switching capabilities superior to bipolar transistors: free from secondary breakdown and free from thermal runaway. And for lower ON resistance, the 4 FETs can be externally connected in parallel.

Siliconix
europe

quad n-channel enhancement-mode VMOS Power FET array *designed for. . .*

Siliconix

Preliminary Data

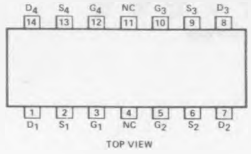
- **Logic to High Current Interface**
- **LED Digit Strobe Drivers**
- **High Speed Line Drivers**

ABSOLUTE MAXIMUM RATINGS (See Page 2 for Power Ratings)

Maximum Drain-Source Voltage . . . . . .60 V
Maximum Drain-Gate Voltage . . . . . .60 V
Maximum Continuous Drain Current (per device) . . . . . 0.3 A
Maximum Pulsed Drain Current (per device) . . . . . 1.0 A
Temperature (Operating and Storage) . . . . . –40 to +150°C
Maximum Forward Gate-Source Voltage . . . . . .15 V
Maximum Reverse Gate-Source Voltage . . . . . 0.3 V

PIN CONFIGURATION

Plastic
Dual In-Line Package
See Section 5



BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted)

	Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0 V, I_D = 100 µA	
2	$V_{GS(th)}$	Gate Threshold Voltage	0.8				V_{GS} = V_{DS}, I_D = 1 mA	
3	I_{GSS}	Gate-Body Leakage			100	nA	V_{GS} = 10 V, V_{DS} = 0	
4	I_{DSS}	Zero Gate Voltage Drain Current			100	µA	V_{DS} = 40 V, V_{GS} = 0	
5	$I_{D(on)}$	ON-State Drain Current	0.20			A	V_{DS} = 25 V, V_{GS} = 5 V	
6			0.5				V_{DS} = 25 V, V_{GS} = 10 V	
7	$V_{DS(on)}$	Drain-Source ON Voltage			1.5	V	V_{GS} = 5 V, I_D = 0.20 A	Note 1
					1.65		V_{GS} = 10 V, I_D = 0.3 A	
8	g_{fs}	Forward Transconductance	100			m℧	V_{DS} = 15 V, I_D = 0.5 A	
9	C_{iss}	Input Capacitance		50		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
10	C_{oss}	Output Capacitance		20				
11	C_{rss}	Feedback Capacitance		3				
12	t_{ON}	Turn-ON Time			10	ns	I_D = 0.3 A, R_L = 23 Ω R_S = 50 Ω	
13	t_{OFF}	Turn-OFF Time			10			

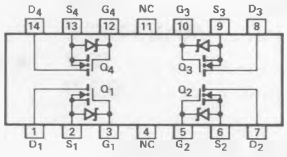
NOTES: 1. Pulse test – 80 µs pulse, 1% duty cycle.
2. Sample test.

VNK

POWER RATINGS

	Each Transistor	All 4 Transistors	Unit
Total Power Dissipation @ T_A = 25°C Derate above 25°C	500	1200	mW
Linear Derating Factor	4.0	9.6	mW/°C
Thermal Resistance	250	104	°C/W
Thermal Coupling Factors:			
Q_1–Q_4 or Q_2–Q_3	50		%
Q_1–Q_2 or Q_3–Q_4	16		%

CONNECTION DIAGRAM



TOP VIEW

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

Where ΔT_{J1} is the change in junction temperature of die 1

$R_{\theta 1 \text{ thru } 4}$ is the thermal resistance of die 1 through 4

$P_{D1 \text{ thru } 4}$ is the power dissipated in die 1 through 4

$K_{\theta 2 \text{ thru } 4}$ is the thermal coupling between die 1 and die 2 through 4

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4} \cdot P_{DT} = 4 P_D$ equation (3) can be further simplified and by substituting into equation (2) results in:

(4) $R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

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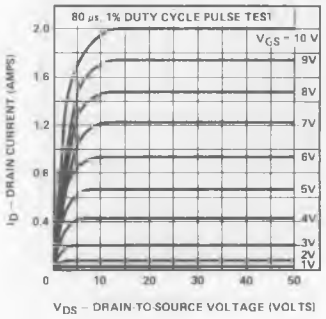
n-channel enhancement-mode VMOS Power FETs

Siliconix

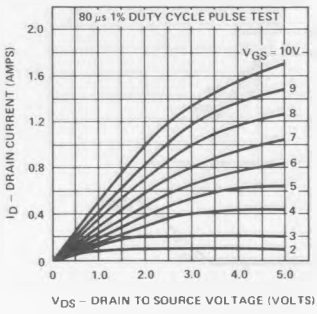
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-3	VN33AJ, VN35AJ, VN66AJ, VN67AJ, VN98AJ, VN99AJ
	TO-39	VN33AK, VN35AK, VN66AK, VN67AK, VN98AK, VN99AK
	380 SOE Flange	VMP4

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

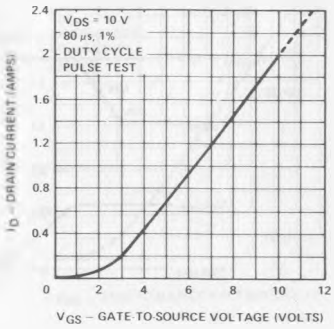
Output Characteristics



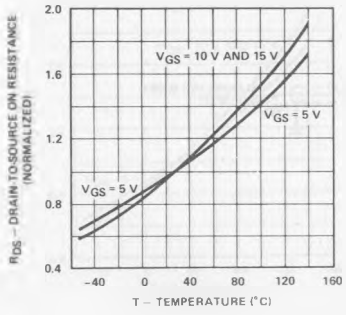
Saturation Characteristics



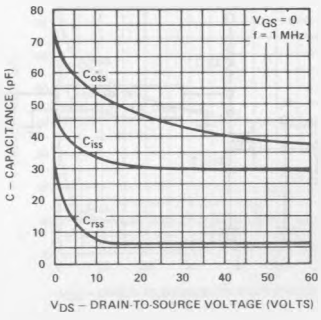
Transfer Characteristic



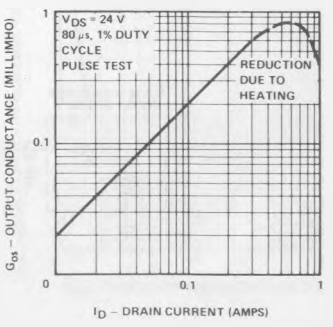
Normalized Drain-to-Source ON Resistance vs Temperature



Capacitance vs Drain-to Source Voltage



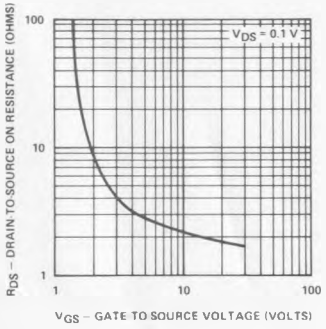
Output Conductance vs Drain Current



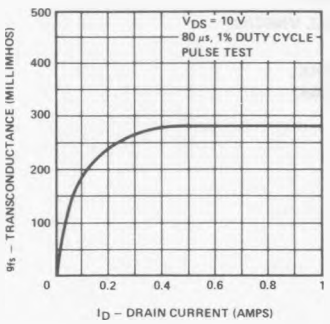
3

TYPICAL PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

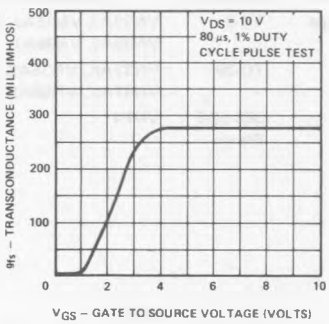
Drain-to-Source ON Resistance vs Gate-to-Source Voltage



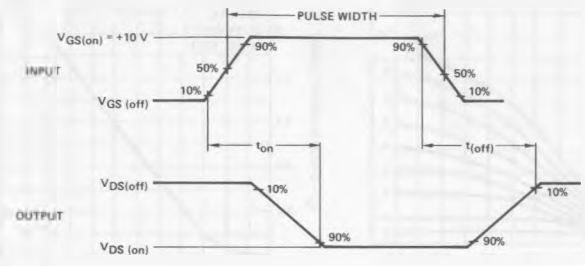
Transconductance vs Drain Current



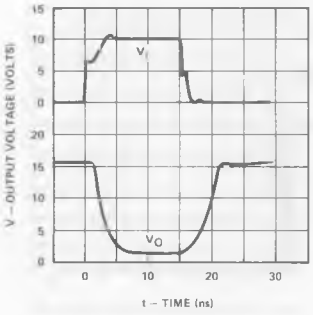
Transconductance vs Gate-to-Source Voltage



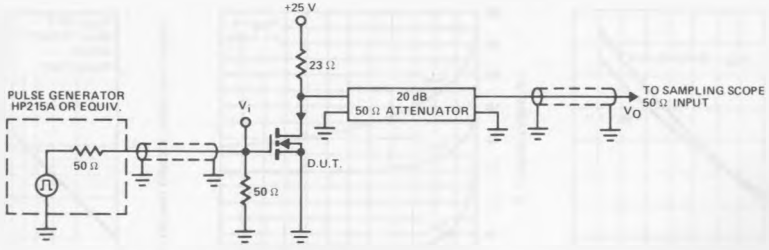
Switching Time Test Waveforms



Switching Waveforms



Switching Time Test Circuit



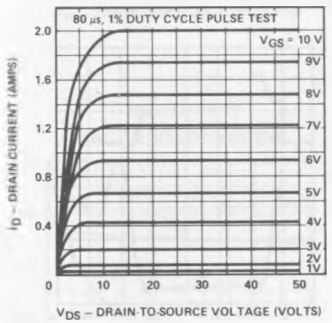
n-channel
enhancement-mode
VMOS Power FETs

Siliconix

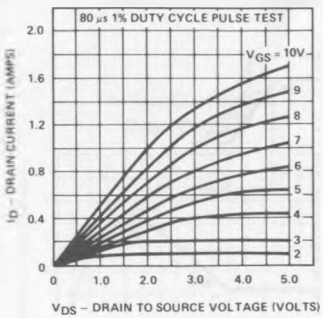
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-3	2N6656, 2N6657, 2N6658, VN30AA, VN35AA, VN67AA, VN89AA, VN90AA
	TO-39	2N6659, 2N6660, 2N6661, VN30AB, VN35AB, VN67AB, VN89AB, VN90AB
	TO-202	VN40AF, VN46AF, VN66AF, VN67AF, VN88AF, VN89AF

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

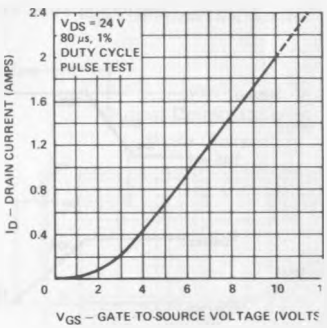
Output Characteristics



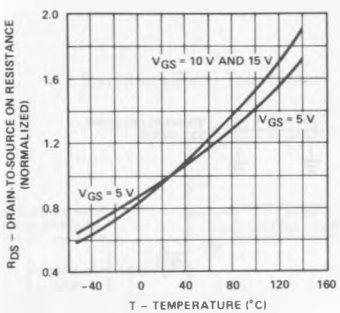
Saturation Characteristics



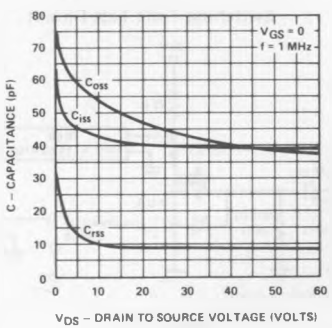
Transfer Characteristic



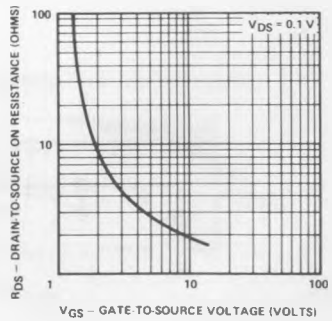
Normalized Drain-to-Source ON Resistance vs Temperature



Capacitance vs Drain-to-Source Voltage

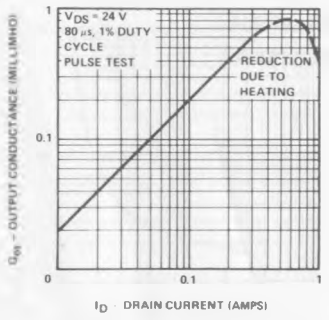


Drain-to-Source ON Resistance vs Gate-to-Source Voltage

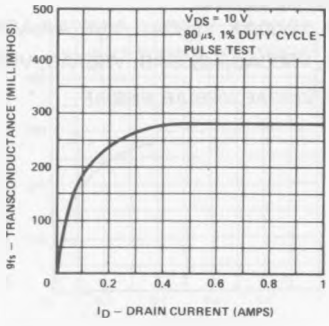


TYPICAL PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

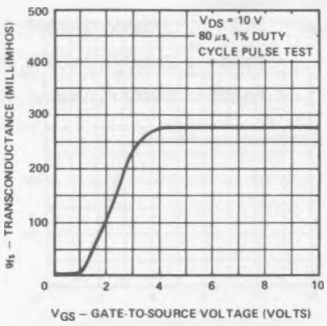
Output Conductance vs Drain Current



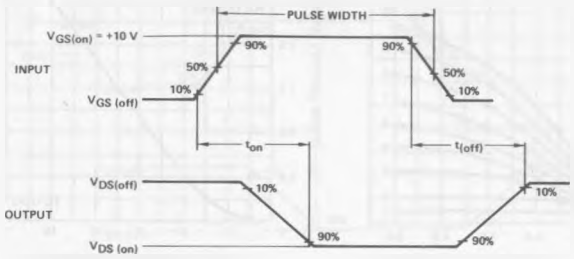
Transconductance vs Drain Current



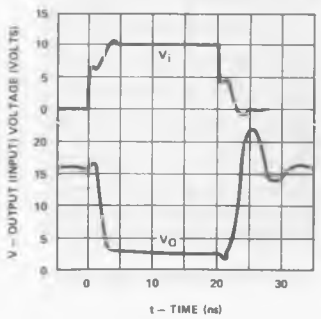
Transconductance vs Gate-to-Source Voltage



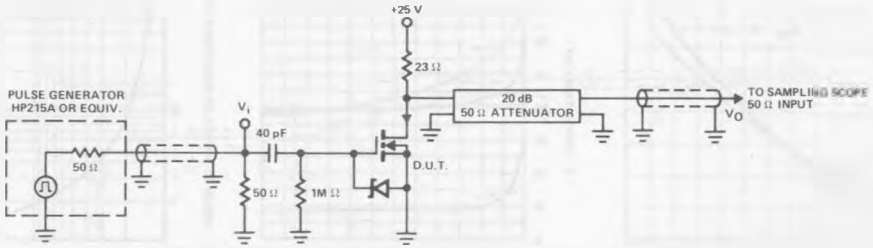
Switching Time Test Waveforms



Switching Waveforms



Switching Time Test Circuit



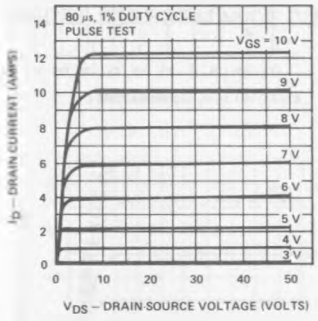
n-channel
enhancement-mode
VMOS Power FETs

Siliconix

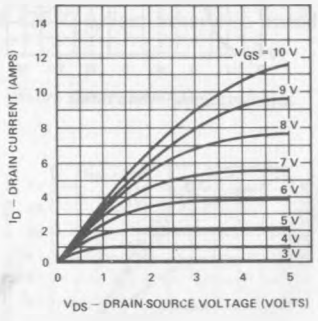
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-3	VN64GA

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

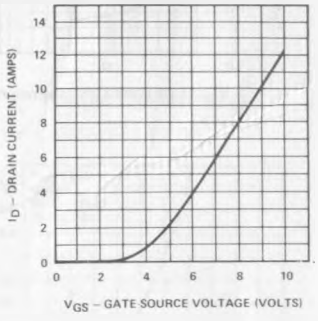
Output Characteristics



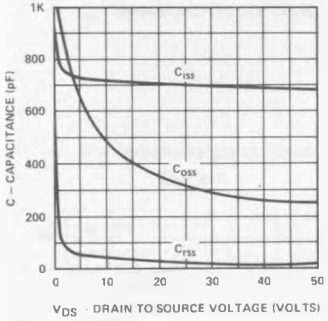
Saturation Characteristics



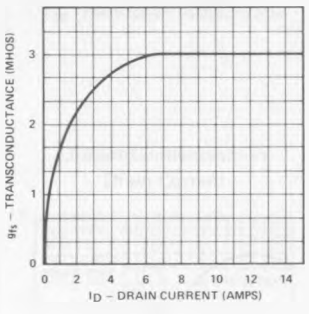
Transfer Characteristic



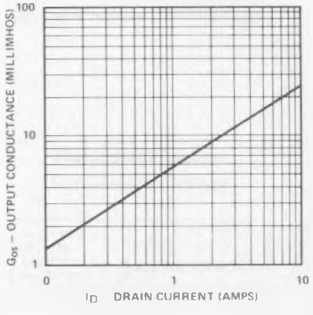
Capacitance vs
Drain-to-Source Voltage



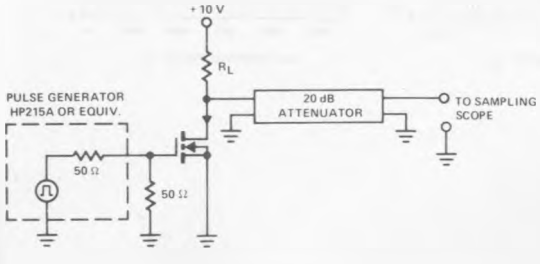
Transconductance vs
Drain Current



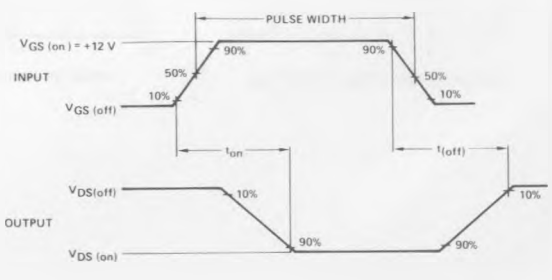
Output Conductance vs
Drain Current



Switching Time Test Circuit

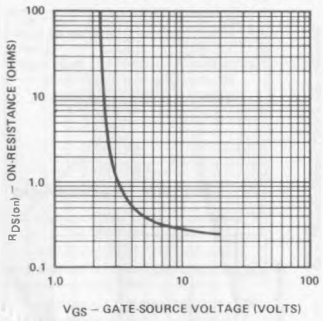


Switching Time Test Waveforms

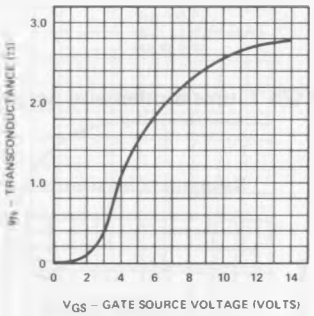


TYPICAL PERFORMANCE CURVES (Cont'd) (25° C unless otherwise noted)

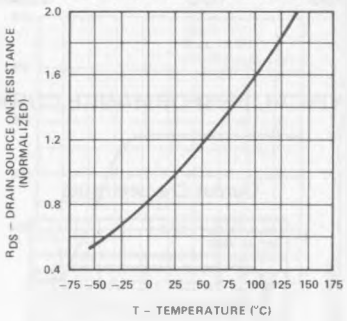
ON-Resistance vs
Gate-Source Voltage



Transconductance vs
Gate-Source Voltage



Normalized Drain-Source
ON-Resistance vs Temperature



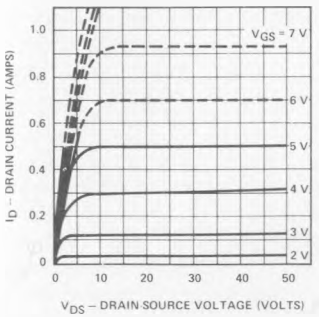
n-channel
enhancement-mode
VMOS Power FETs

Siliconix

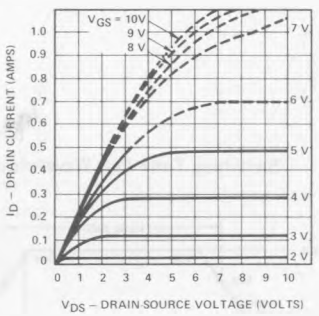
TYPE	PACKAGE	PRINCIPLE DEVICES
Single	TO-237	VN10KM VK1010 VK1011
Quad	14 pin Plastic	VQ1000CJ

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

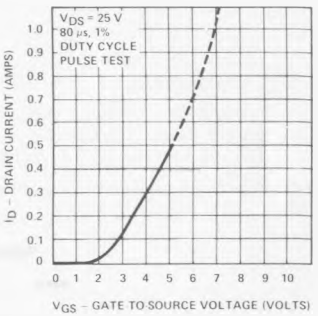
Output Characteristics



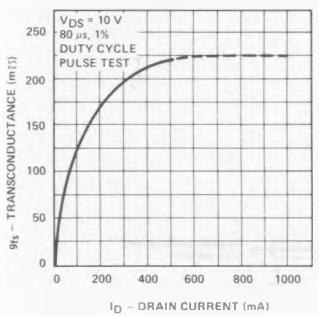
Saturation Characteristics



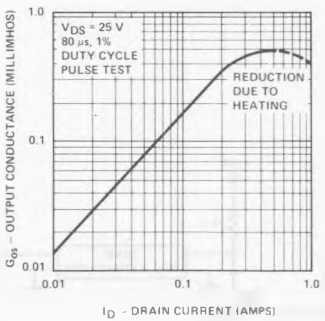
Transfer Characteristics



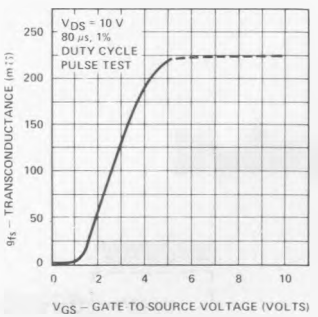
Transconductance vs Drain Current



Output Conductance vs Drain Current

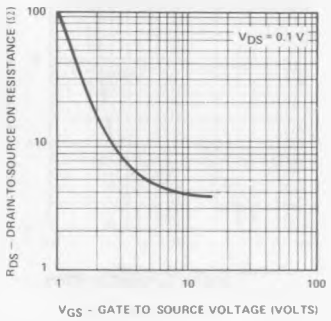


Transconductance vs Gate-Source Voltage

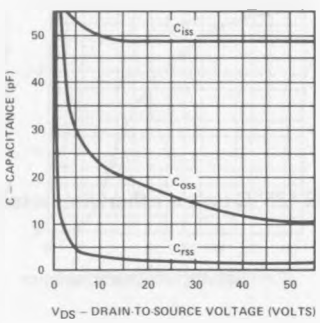


TYPICAL PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

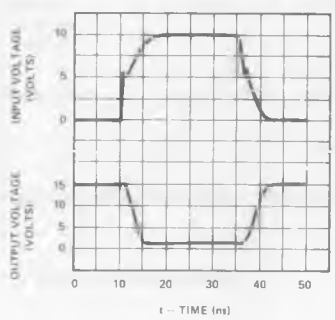
Drain-to-Source ON Resistance vs Gate-to-Source Voltage



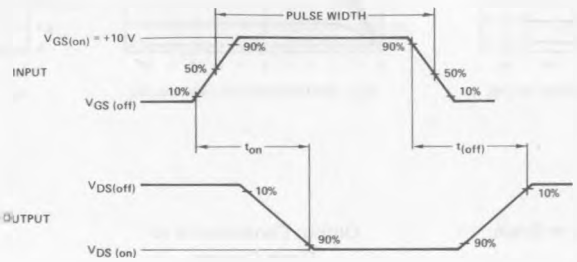
Capacitance vs Drain-to-Source Voltage

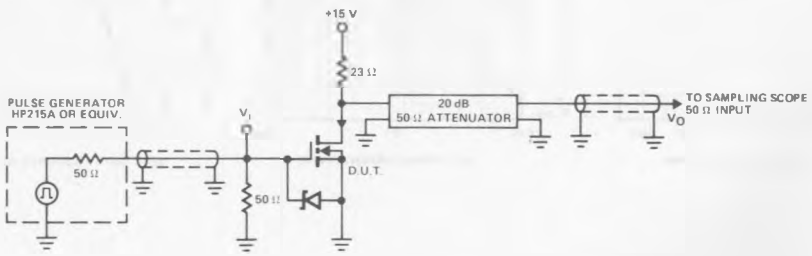


Switching Waveforms



Switching Time Test Waveforms





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What are VMOS Power FETs?

What are VMOS Power FETs?

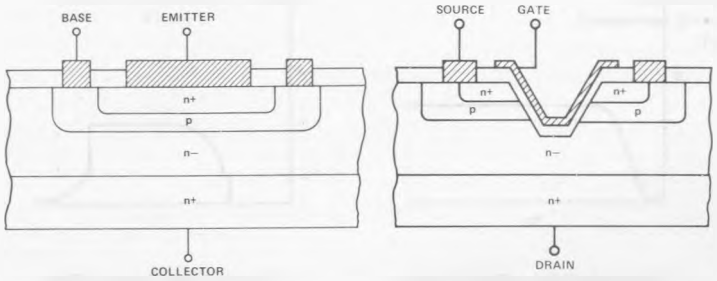
VMOS – Vertical Metal-Oxide-Semiconductor Field-Effect Transistors uniquely combine the advantages of the power bipolar transistor with those of the MOSFET. The result is a high-power, high-voltage, high-gain power transistor with no minority-carrier storage time, no thermal runaway and a greatly inhibited secondary breakdown characteristic, all of which are contributing to the spectacular rise in the popularity of the VMOS power FET.

Construction of VMOS

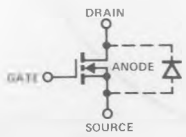
During the initial phase of construction VMOS closely resembles the double-diffused epitaxial power bipolar transistor. Both begin with an n+ substrate and an n– epitaxial into which is first diffused a p and then an n+ layer forming a 4-layer structure. One distinguishing feature of VMOS, as shown in Figure 1, is the anistropically-etched V-groove cut normally to the surface that extends through both the n+, p and into the n– epitaxial region. By virtue of this V-groove an oxide-insulated gate overlays the p-channel providing fail-safe control over the current path. This current path is established in an identical fashion to that of any enhancement-mode MOSFET. A positive gate potential inverts the p-channel and the resulting electron-enhanced n-channel, extending from the n+ source to the n– epi, offers an uninterrupted, low resistance current path devoid of the thermal problems associated with the typical power bipolar transistor.

Another distinguishing feature is the electrical bonding of the uppermost n+ diffusion (source) to the p diffusion (body). In the bipolar model this would tie the base to the emitter; for the VMOS model it ties the source to the body. Without this electrical bond there would exist a parasitic 4-layer npn bipolar in parallel with the VMOS power FET thus masking the beneficial features with the problems encountered with bipolar transistors. However, with this electrical bond, a source-drain parasitic diode appears in parallel with the VMOS power FET. Fortunately by virtue of the polarity of this parasitic diode, as shown in Figure 2, VMOS performance is virtually unaffected under normal operation. This parasitic is of mixed blessing; on the one hand, a parasitic element is undesirable from an aesthetic viewpoint, but practically speaking, a reverse polarity diode intrinsic to the VMOS structure becomes a useful snubbing diode when VMOS is arranged in a totem-pole arrangement such as in motor control applications.

The vertical VMOS structure, like the power bipolar transistor, offers a large surface area for source metal and the entire backside of the chip for the drain. This is of great importance as it allows maximum current carrying capacity unavailable to a nonvertical structure.



A Comparison of a 4-Layer Bipolar Transistor with VMOS
Figure 1



Schematic Representation of VMOS Showing Body-Drain Diode
Figure 2

Controlling the VMOS Power Transistor

Operationally, VMOS is unique among power transistors. Channel conduction is proportional to gate *voltage, not* to any sort of injection current, typical of the bipolar transistor. Whatever input current that does exist beyond that attributed to leakage may be identified as the charging current necessary to overcome the input capacitance in very high-speed switching situations. Because the steady-state gate current is negligible, the familiar parameter, *Beta,* is of little importance. Consequently, VMOS exhibits a high input resistance that makes it ideal for many logic control applications.

VMOS as a Switch: Turning it ON

Driving VMOS from logic requires an appreciation of the gate drive power needed to actuate, or turn *on,* the VMOS power transistor. First, the driver must be able to deliver sufficient current during the transition (from *off* to *on*) to adequately charge the input capacitor in the desired time. Two familiar equations show that to achieve a high speed switch driving the gate from a low impedance, high current source is certainly desirable.

$$t = 2.2\ R_g \cdot C_{in}$$

$$i = C_{in}\ dV/dT$$

where R_g = input resistance
C_{in} = input capacity
dV/dT = rate of voltage change

As this driving voltage ramps upward another phenomenon occurs called *Miller effect.* Once the threshold voltage of the VMOS transistor is passed it begins to draw increasingly heavier drain current. In Figure 3 the rapid rise of drain current with respect to the gate voltage is clearly illustrated. As the drain current rises, the transconductance rises rapidly to saturation as shown in Figure 4. Concurrent with this rise in transconductance is a proportional rise in gain and the once low feedback capacitance now swells to enormous proportions appearing as an addition to the input capacitance.

$$C_{in} = C_{iss} + (1 + A_V)C_{gd}$$

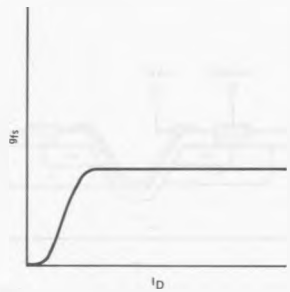
where C_{iss} = common-source input capacitance
C_{gd} = gate-drain capacity
A_V = voltage gain

If the driver is deficient in its reserve of drive current the VMOS transistor's switching speed suffers and the waveform shown in Figure 5 is the inevitable result. On the other hand, if the driver can deliver the required charging current the switching speed is determined solely by just how fast the driver *can* deliver.

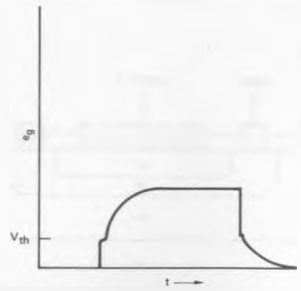
Turning the VMOS Switch OFF

Turn off is another story where the VMOS power transistor outperforms its equivalently-rated power bipolar transistor. VMOS, a majority-carrier transistor begins to turn off immediately upon the removal of gate voltage. Again the speed is limited by the rate of discharge of the input capacitor through the driver. For ultra-high speed switching special charge transfer circuits are recommended for dumping current both into and out of the VMOS gate. Upon the removal of the gate voltage the VMOS power FET 'shuts down' (a fail-safe feature?), the resistance between drain and source rises to a very high value and whatever current flow that remains is limited to leakage. This, of course, precludes that the breakdown voltage is not reached.

Transfer Characteristics of VMOS Showing Linear I_D/V_{GS} Relationship
Figure 3



Transconductance vs Drain Current
Figure 4



Effect in Input Waveform When Miller Effect Loads Driver Excessively
Figure 5

The Characteristics of VMOS

Closer examination of Figure 1 reveals that VMOS, unlike the conventional low power MOSFET, has a very short channel where, as the drain-source current flow increases, electron velocity saturation results. The consequences resulting from this velocity saturation are three-fold: the output characteristics assume a constant-current plateau, the forward transconductance saturates and, most important, a linear transfer characteristic results. All of these effects are shown collectively in Figures 3, 4 and 6.

The Importance of Threshold Voltage

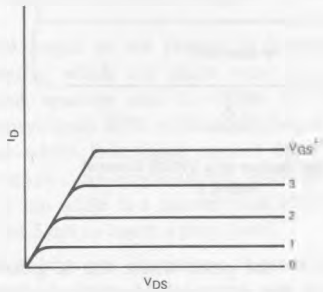
VMOS, an enhancement-mode MOSFET, exhibits what appears as a delayed turn-on when a voltage ramp is applied to the gate. This apparent delay is, in reality, caused by the threshold voltage level, below which the channel remains nonconducting and above which drain current begins. A logic-compatible VMOS is one whose threshold voltage is set so that in the low state [0] the VMOS is *off* and in the high state [1] the VMOS is *on*. It is important to note that a low threshold voltage is undesirable for high power VMOS devices for a number of reasons. High power VMOS transistors generally operate at higher chip temperatures for optimum efficiency. Since threshold is temperature dependent (a coefficient of approximately -5 mV/°C) a high threshold is mandated to assure operation in the enhancement region. Furthermore, high-power devices have large input capacitance which necessitates a substantial drive. The wisdom of a high threshold precludes the possibility of driver noise causing false triggering of the VMOS. This noise immunity is especially important when working in switching power supplies and motor control applications.

Temperature Effects of VMOS

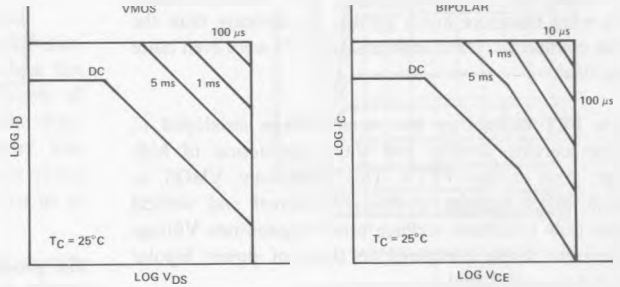
The negative temperature coefficient of gain characteristic of FETs is certainly a valuable asset when using VMOS in linear applications, for it greatly simplifies the biasing circuitry. As a bulk semiconductor the resistance of the silicon exhibits a positive temperature coefficient of 0.6%/°C.

The benefits from this unique thermal property are twofold. VMOS offers an exceptionally stable SOA *(safe operating area)* in comparison to equivalently-rated power bipolar transistors as shown in Figure 7. Secondly, paralleling VMOS for increased current handling presents no problem. Any intrinsic unbalance between VMOS transistors does not result in current hogging because the negative temperature characteristic acts to equalize the current flow.

Always be careful to keep VMOS power transistors within their operating temperature limits. If heat sinks are advisable, use them.



Output Characteristics of VMOS
Figure 6



Typical Safe Operating Area
Comparison Between VMOS and Bipolar
Figure 7

Application Note AN76-3

VMOS-A Breakthrough in Power MOSFET Technology

Lee Shaeffer
Dave Hoffman
Revised

INTRODUCTION

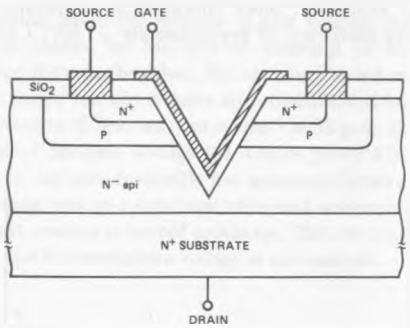
Until several years ago, Field Effect Transistors have been useful only at low (< 1 W) power levels. While possessing many theoretical advantages over their bipolar counterparts, the practical limitations in manufacturing high power devices precluded FET's competing with bipolar transistors and SCR's in power applications. A major limitation was that FET's were strictly horizontal devices, so their current densities were much less than the bipolar's (which utilized vertical current flow). For a given current, then, the FET chip area had to be considerably larger, which meant a lower yield and a resulting higher cost. Medium power FET's were therefore much costlier to fabricate than the bipolar counterparts, and high power FET's were even more impractical.

A new FET technology has recently been developed to increase current density and allow production of high voltage, high current FET's. This technology- VMOS, or Vertical MOS–exploits a diffused channel and vertical current flow to achieve its high power capabilities. Voltage and current levels compared to those of power bipolar devices are now feasible.

The VMOS Technology

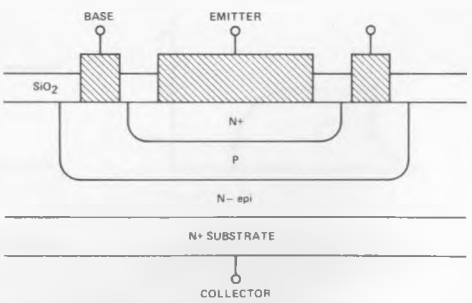
Figure 1 shows a cross section of a VMOS channel. The substrate, which eventually becomes the drain and provides a low resistance current path. is N^+ material. An N^- epi layer increases the drain-source breakdown voltage by absorbing the depletion region from the drain-body junction, which is normally reverse biased. Also, the epi layer greatly reduces the feedback capacitance since the gate overlaps N^- rather than N^+ material.

A P^- body and N^+ source are then diffused into the epi, followed by the preferential etching of a V groove through the source, body, and into the epi. Oxide is then grown and aluminum metalization deposited to form the source connection and gate. Finally, the entire chip is passivated to keep contamination (primarily sodium ions) from penetrating the gate oxide.



The Cross Section of a VMOS Channel
Figure 1

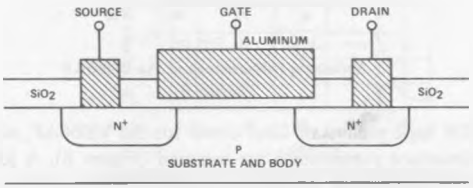
The processing, up to the point where the V groove is etched, is similar to that of the double-diffused epitaxial planar bipolar transistor, shown in Figure 2 for comparison.



A Double-Diffused Epitaxial Planar Transistor, Shown for Comparison
Figure 2

In operation, both the gate and drain are positive with respect to the source (and body). The gate produces an electric field which induces an N-type channel on both surfaces of the body facing the gate, allowing electrons to flow from the source, through the N-type channel, and epi, and into the substrate (drain). Because current flow–in the form of electrons–is entirely through N-type material, the VMOS is a majority carrier device. A greater gate voltage enhances a deeper channel, so the current path from the drain to the source is wider and current flow is increased. For example, the VN66AF VMOS FET conducts about 650 mA with 5 V between the gate and source, and 2 A with 10 V gate-to-source.

Figure 3 shows a conventional horizontal MOSFET. The N^+ source and drain are simultaneously diffused into the P-type substrate, which also serves as the body. Current flows horizontally from source to drain through the channel, which is induced on the top surface of the substrate.



The Cross Section of a Conventional MOSFET
Figure 3

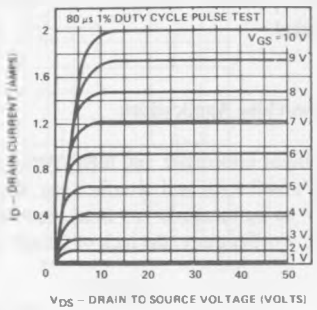
The vertical structure of VMOS gives it several important advantages over conventional MOS:

1. The length of the channel is determined by diffusion depths, which are much more controllable than the mask spacings used to define the channel length of conventional MOS, so the width/length ratio of the channel–which determines current density–is greater. For example, the length of the VN66AF channel is about 1.5 μm while in a conventional MOSFET it must be at least 5 μm to insure a good yield.
2. Each V groove creates two channels, so current density is inherently doubled, for each gate stripe.
3. The substrate forms the drain contact, so drain metal is not needed on top of the chip. This further reduces chip area and keeps the saturation resistance low.
4. The high current density of VMOS results in low chip capacitance, especially the feedback capacitance (gate-drain) since the overlap of the gate and drain are kept to a minimum. Extra gate-drain overlap must be allowed in conventional MOSFET's to guard against mask-misalignment, which increases the source-gate and gate-drain capacitance.
5. The VMOS epi layer absorbs the depletion region from the reverse-biased body-drain P-N diode, and therefore greatly increases the breakdown voltage while it has only a minimal effect on other device parameters (other than adding a series resistance). To fabricate a high voltage MOSFET the body region must be lightly doped

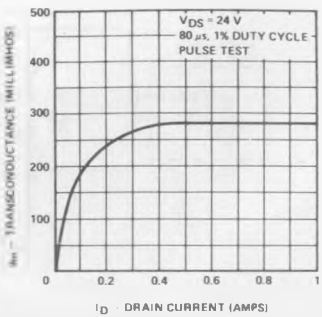
5. (Continued)
so it can absorb the depletion region. The lightly doped material is very sensitive to oxide contamination and good long term stability is hard to achieve. Also, the gate oxide must be thick enough to withstand the entire gate-drain voltage (in VMOS it needs to stand off only about 1/4 of the gate-drain voltage) so a high voltage standard MOSFET lacks transconductance.

VMOS Characteristics

The output characteristics of the VN66AF, plotted in Figure 4, are similar to those of a conventional MOSFET with several exceptions. The vertical scale is amps rather than milliamps, the output conductance is low (the curves are flat rather than sloping) because of the buffering effect of the epi region, and the g_m is constant (the lines are evenly spaced) above 400 mA. The constant g_m, a characteristic of short-channel devices, is due to velocity saturation of the electrons in the channel–increasing the electric field intensity does not increase the drift velocity above a certain threshold. The g_m of a conventional (long channel) MOSFET, on the other hand, is proportional to the gate voltage; drain current is therefore proportional to $(V_{GS})^2$. Figure 5 is a more graphic illustration of the transconductance vs drain current for the VN66AF, showing the high linearity above 400 mA and the square law characteristics below 400 mA.



Output Characteristics of the VN66AF
Figure 4



Transconductance vs Drain Current of the VN66AF
Figure 5

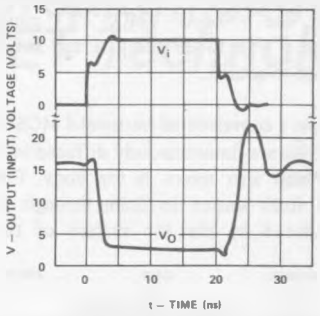
Of the advantages that VMOS has compared to bipolars, many are well known in small signal applications but many others are apparent only at higher power levels. They include:

1. High input impedance–low drive current (typically less than 100 nA). The "beta" of a VMOS device (the output current divided by the input current) is therefore over 10^9. Since the resultant drive power is negligible, VMOS will directly interface to medium high impedance drivers such as CMOS logic or opto isolators.
2. No minority carrier storage time. VMOS is a majority carrier device–its charge carriers are controlled by electric fields, rather than the physical injection and extraction (or recombination) of minority carriers in the active region. The switching delay time is small, several nanoseconds, and is caused primarily by external parasitic elements (series gate inductance). The 2N6657, for example, switches 1 A ON or OFF in 4 nsec, about 10 to 200 times faster than a bipolar.
3. No failure from secondary breakdown or current hogging. Since the temperature coefficient of the VMOS drain to source ON voltage is positive (a bipolar's is negative), VMOS draws less current as the device heats up. If the current density were to increase at one particular point of the channel, the temperature rises and the current decreases. The current automatically equalizes throughout the chip, so no hot spots or current crowding–which eventually leads to failure in a bipolar, can develop. Similarly, current is automatically shared between paralleled devices so no ballasting resistors are needed.

eral Switching Applications

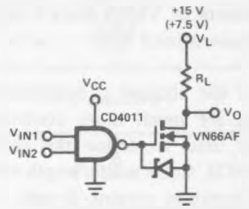
The high input impedance and high speed of VMOS makes it ideal as a switch–it will interface any driver capable of a 5V – 30V swing to nearly any load requiring several amps of current. Furthermore, the lack of failure from secondary breakdown means that it can withstand high voltage and high current simultaneously, so inductive loads are no problem.

The basic switching performance of the VN66AF is shown in Figure 6 while the corresponding test circuit is shown in Figure 7. The 2 nanosecond turn-ON and turn-OFF delay is caused by the input capacitance charging and discharging through the equivalent series inductance of the package and test jig.

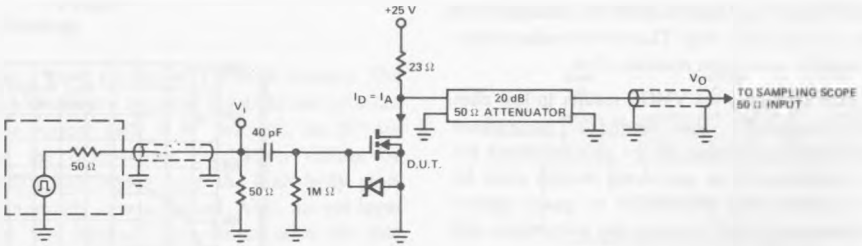


Switching Performance of the VN66AF
Figure 6

CMOS logic makes an ideal driver for the VN66AF, since no interface components are required (Figure 8). A logic low to the input of the CD4011 turns ON VN66AF (V_{GS} = 10 V), while a logic HIGH turns the device OFF (V_{GS} = 0). The steady-state power dissipated by the circuit, exclusive of load current, is a maximum of 55 μW (0.15 μW typ).



A CMOS Gate Driving the VN66AF
Figure 8



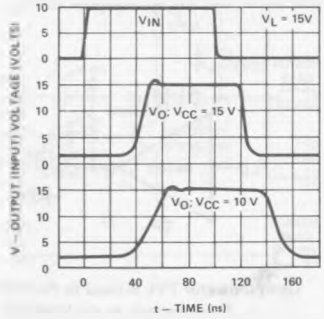
Switching Test Circuit for the VN66AF
Figure 7

Figures 9 and 10 depict the dynamic performance of the circuit shown in Figure 8 when the load is 13 Ω. V_L = 15 V when the logic supply voltage is 10 or 15 V (I_{LOAD} = 1A) and 7.5V for V_{CC} = 5 V (I_{LOAD} = 500 mA). The turn- ON and turn-OFF times when V_{CC} = 10 V are about 60 nsec; increasing V_{CC} to 15 V decreases switching times to 50 nsec, while decreasing V_{CC} to 5 V increases the switching times to 100 nsec. An examination of the output of the CD4011 reveals it is being loaded by 65 pF, the parallel combination of the input and Miller capacitances of the VN66AF.

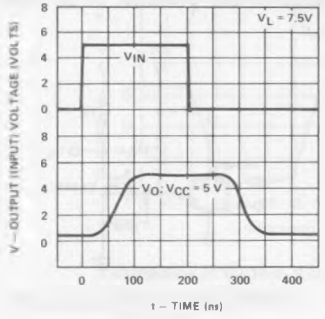
The switching speed is increased when several CMOS gates are paralleled to increase drive current to the VN66AF. For example, when four CD4011 gates are paralleled and V_{CC} is 15 V, switching times are about 25 nsec—most of it propagation delay through the CMOS gate (Figure 11).

Additional peak drive current to the VN66AF is needed to further decrease switching times, which is apparent when you consider that 50 mA of gate current is needed to charge or discharge the 65 pF effective input capacitance in 10 ns.

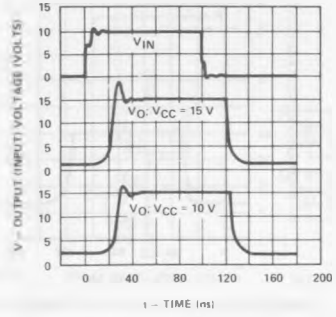
One solution is a MOS clock driver—it is designed to deliver high peak currents to capacitive loads and to translate TTL levels into 15 V swings. Figure 12 is a typical switching circuit whose characteristics are shown in Figure 13.

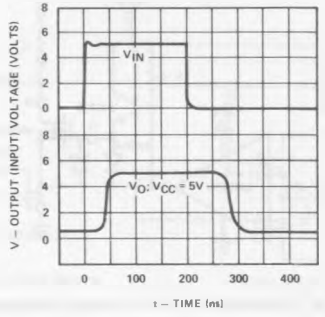


Switching Performance of the VN66AF Driven by the CMOS Gate in Figure 8
Figure 9

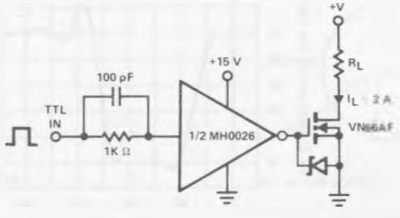


Switching Performance of the VN66AF With A 5 V CMOS Logic Drive
Figure 10

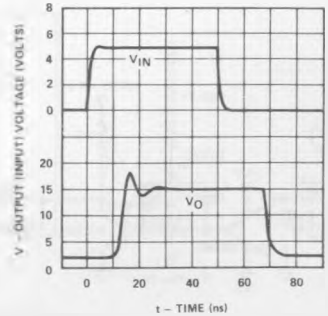




Switching Performance of the VN66AF Driven By Four Paralleled CD4011 Gates
Figure 11



Driving the VN66AF with a MOS Clock Driver
Figure 12

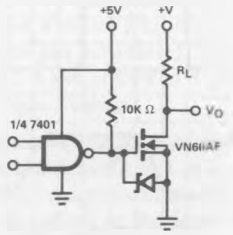


Switching Performance of the VN66AF Driven By a MH0026 MOS Driver
Figure 13

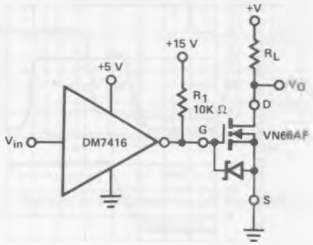
VMOS will also interface to standard TTL, but a pullup resistor is needed to insure sufficient gate enhancement (Figure 14). If no pullup resistor is used, the enhancement to the VMOS will be a mere 3V, and the VMOS will conduct only about 200 mA. On the other hand, with a full 5 V of enhancement on the gate of the VN66AF, it will conduct approximately 500 mA, which is sufficient for many applications.

If more current or a lower ON resistance is needed, more drive voltage must be applied to the VMOS. Figure 15 shows how to use open collector TTL with a 10 or 15 V supply, although now the turn-ON time will depend heavily on the value of R_1 since only it provides current to charge the input capacitance of the VN66AF. If an extremely fast turn-ON time is needed, R_1 must be very small and excessive power will be dissipated when the VN66AF is OFF. To solve this problem, use the totem pole drive circuit shown in Figure 16–it drives the VN66AF with an emitter follower, effectively reducing the capacitance that R_1 must charge (Figure 17).

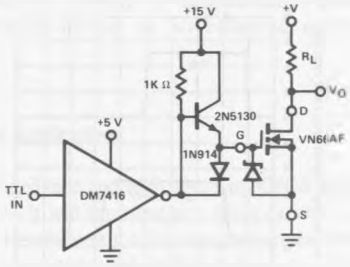
A second method of interfacing TTL to VMOS, the bipolar level shifter, shown in Figure 18, amplifies the TTL output pulse and provides up to 15 V of enhancement to the VN66AF. The AM686 is a high-speed comparator, although any comparator–or for that matter, any TTL gate–could be used instead. For a faster turn-ON time than that shown in Figure 19, or for a lower power dissipation in the OFF state, use the totem-pole driver.



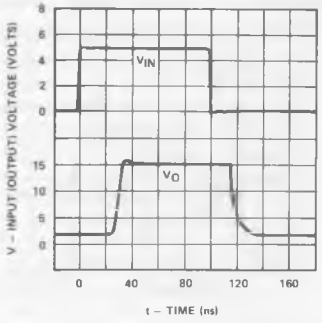
Driving the VN66AF With Standard TTL
Figure 14



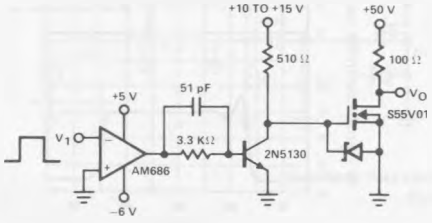
Open Collector TTL is Used to Provide Greater Enhancemant to the VN66AF
Figure 15



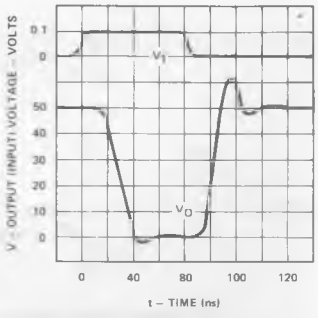
A "Totem Pole" Driver Increases Switching Speed and Reduces Dissipation
Figure 16



Switching Performance of the VN66AF Driven By the "Totem Pole" Open Collector TTL Driver
Figure 17



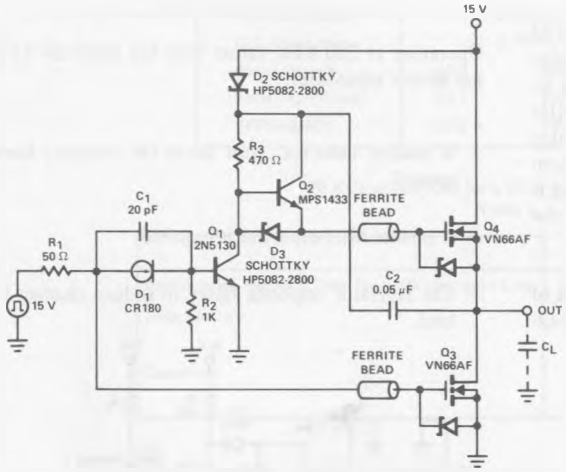
High Current Interface
Figure 18



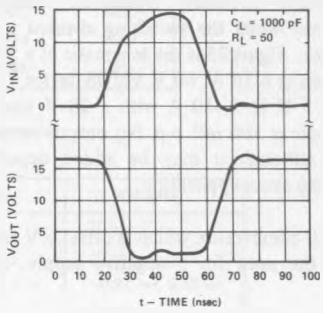
Performance of the High Current Interface
Figure 19

When driving capacitive loads, such as cables or data buses, an active pull-up is required to source current into the load. The high speed line driver shown in Figure 20 uses a second VN66AF with an inverter, to source up to 3 A and switch 15 V across 1000 pF in less than 15 ns. Bootstrap capacitor C_2 provides a 29 V drive to Q_4—14 V greater than its source. Performance of the High Speed Line Driver is shown in Figure 21.

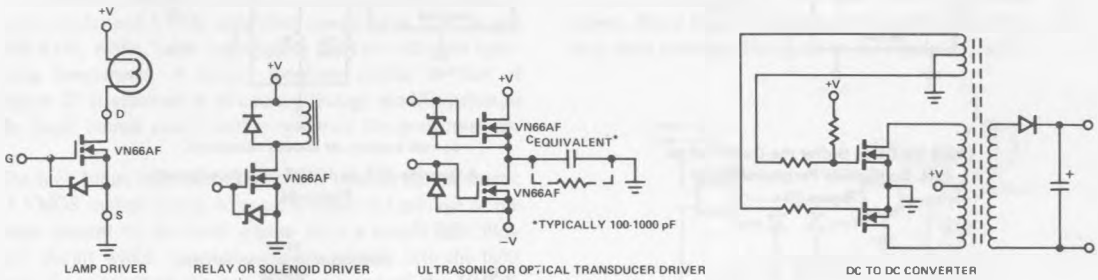
The ease of driving, ruggedness, lack of secondary breakdown and fast switch speeds make VMOS well suited for switching power to a variety of loads, some of which are shown in Figure 22.

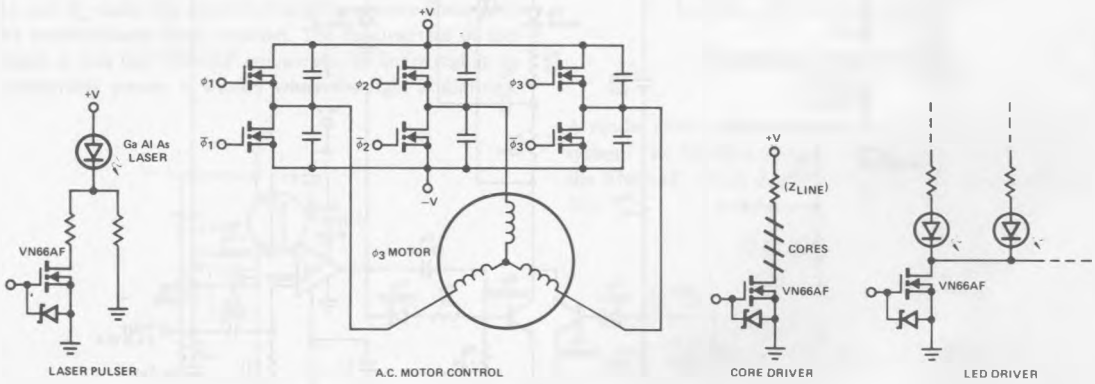


High Speed Line Driver
Figure 20



Performance of the High Speed Line Driver
Figure 21





Several Typical VMOS Applications
Figure 22

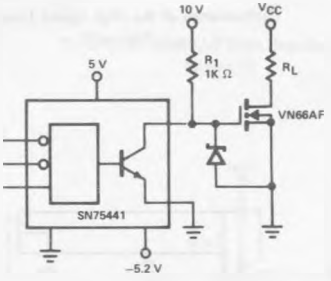
Interfacing VMOS to ECL is not quite as straightforward since ECL levels are inherently incompatible with VMOS drive requirements, but level shifting is still relatively easy. In Figure 23, the VN66AF is used to increase the voltage and current capability of the SN75441 30 V, 150 mA, ECL compatible peripheral driver. An alternate circuit, Figure 24, uses discrete components to translate ECL levels into the 0–10 V swing required for VMOS. Switching times of this circuit are less than 40 nsec into 50 Ω.[4]

The fast switching time of VMOS increases the efficiency of high-frequency switching regulators, since considerable power is lost while the switching element is traversing its active region. Figure 25 is the schematic of a 50 W, 200 KHz regulator using a 10 A, 60 V VMOS device.[5] The regulator output is 5 V at 5–10 A with a 28 V input; maximum output ripple is 100 mV p-p. No output current limiting is included, although it may be added depending on the need and the exact application.

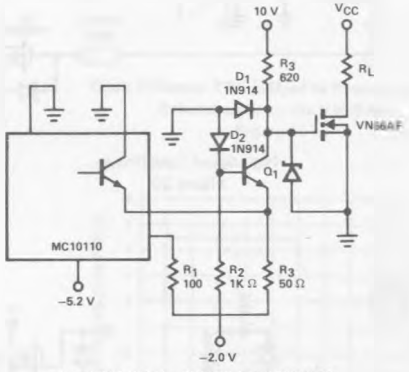
The LM710 comparator, which is offset 6 V from ground to eliminate the need for a negative supply, acts as a self-contained oscillator using L1 as a reactive element and R_8 for hysteresis. C_5 couples the output ripple to the negative input of the comparator, where it is rejected as a common mode signal. D_4, R_4, R_5 and C_1 form a bootstrap circuit which drives the gate 15 V more positive than the 28 V input rail. Six paralleled capacitors filter the output, since the total impedance of one capacitor at 200 KHz is 0.05 Ω and 0.01 Ω is needed to filter the 10 A peak-to-peak current. Q_3 is the heart of a soft startup circuit.

Operation at 200 KHz, rather than the usual 20–25 KHz, has several advantages:

1. A smaller inductor, with lower DC (copper) losses, is needed.
2. A smaller filter capacitor is required.
3. The regulator responds faster to sudden changes in the load.

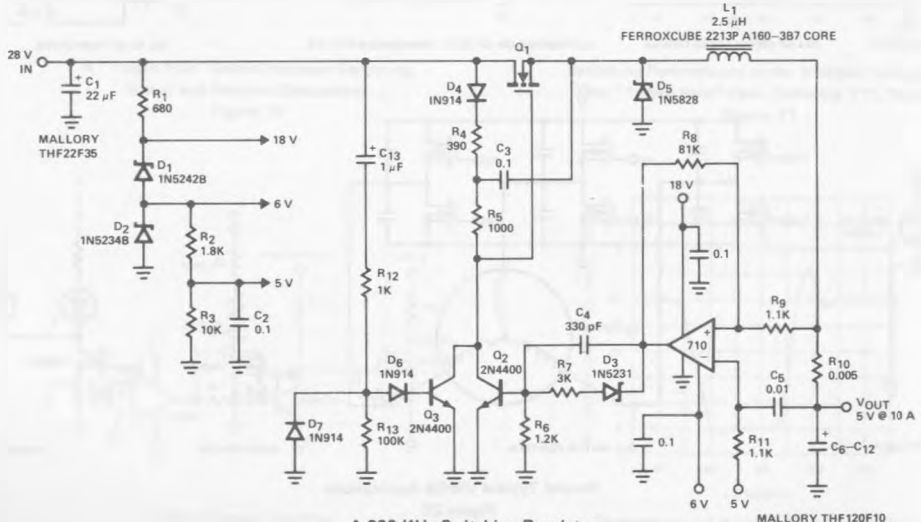


Using VMOS to Buffer the Output of an ECL Compatible Peripheral Driver
Figure 23



Q1 – USE A HIGH fT, RF BIPOLAR TRANSISTOR.

A Discrete ECL to VMOS Interface Circuit
Figure 24



A 200 KHz Switching Regulator
Figure 25

A Comparison of Four Regulators--28 V In, 5 V @ 10 A Out
Table 1

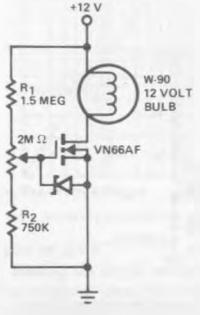
	20 KHz		200 KHz	
	BIPOLAR	VMOS	BIPOLAR	VMOS
Fixed Losses	4.85W			
Drive Power	0.17W	0.44W	1.4W	0.87W
Switching Losses	1.9	0.55	9.6	3.7
Saturation Losses	3.2	7.2	3.2	7.2
A.C. Core Losses	0 06		0.2	
D.C. Coil Losses	0.49		0.13	
Power Output	50.0	50.0	50.0	50.0
Total Input Power	60.7	63.6	69.4	67.0
EFFICIENCY	82%	79%	72%	75%

20 KHz vs 200 KHz for a 50 W Switching Regulator
Table 2

	20 KHz	200 KHz
Approximate Recovery Time for a 40% Change in Load	100 μsec	10 μsec
Inductor Core	3019 pot core ~0.85 in^3, 1.2 oz	2213 pot core ~0.31 in^3, 0.43 oz
Capacitors	8 x 220 μF 1.0 in^3	6 x 120 μF 0.45 in^3

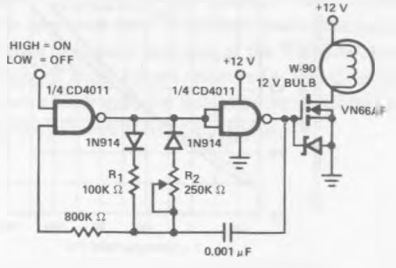
High frequency operation does reduce the overall efficiency somewhat, but not as much as it would in a comparable design using a bipolar or bipolar Darlington transistor as the switching element. Table 1 contains a comparison of both bipolar and VMOS regulators operating at 20 KHz and 200 KHz, while Table 2 compares the two different operating frequencies. A circuit topology similar to that of Figure 25 is assumed in all cases, although modifications to the basic circuit could further optimize the performances.

The high input impedance and linear transfer characteristic of VMOS makes it easy to control either the average or the surge current to the load. Figure 26 is a simple light dimmer circuit which varies the average current into the light bulb by controlling the saturation current of the VMOS. R_1 and R_2 make the control of brightness more linear with the potentiometer shaft rotation. The disadvantage of this circuit is that the VN66AF operates in its linear region, so considerable power is wasted when the light is dimmed.



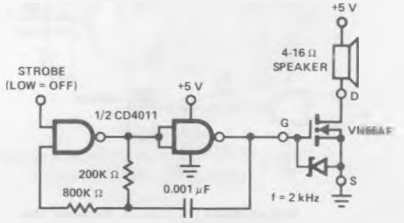
A Linear Light Dimmer Circuit
Figure 26

A more efficient method of varying the average current to the load is with pulse width modulation (Figure 27). The CD4011 oscillates with a duty cycle which is determined by the ratio of R_1 and R_2, and drives the VMOS with 12 V power. Since the VN66AF is either fully ON or fully OFF, very little power is dissipated in the regulator itself.



An Efficient Light Dimmer Circuit
Figure 27

A similar circuit can be used as an inexpensive audio alarm system. The CD4011 gates provide a 2 KHz square wave to the VN66AF, which directly drives an 8 Ω speaker (Figure 28).



A 2 KHz Audio Alarm
Figure 28

Drive Considerations

While the VN66AF can drive nearly any load of 2 A or less (3 A under pulsed conditions), the gate must be driven with a high enough enhancement voltage to support the required current. Refer back to Figure 4. If the VMOS is driven by TTL and the maximum V_{GS} is 5 V, a maximum drain current of 650 mA will flow regardless of the drain to source voltage. The typical worst case under these conditions is a drain current of 500 mA. If a minimum drain current of 1 A is required, a worst case minimum of 10 V must be applied to the gate (6.25 V will typically be sufficient).

Applying more than the minimum enhancement voltage, 15 V rather than 10 V, for example, has two desirable effects–the ON resistance is reduced, and an extra margin of safety is provided to allow for the decrease in drain current as the VN66AF heats up. It is possible, as the drain current decreases with temperature, for the VN66AF to actually come out of saturation and further increase its dissipation.

Temperature Considerations

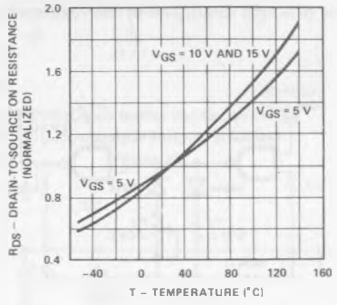
Typically, the $R_{DS(ON)}$ of VMOS increases 0.5 to 0.6%/°C due to the decrease in the mobility of electrons in silicon as temperature increases, which causes a proportional increase in drain-source voltage (Figure 29). If you assume a worst case situation of 0.6%/°C, the ON resistance at a given temperature ($R_{DS(T)}$) can be expressed in terms of the resistance at the ambient temperature ($R_{DS(T_A)}$) by the expression:[4]

$$R_{DS(T)} = R_{DS(T_A)} \bullet 0.006\ \Delta T \qquad (1)$$

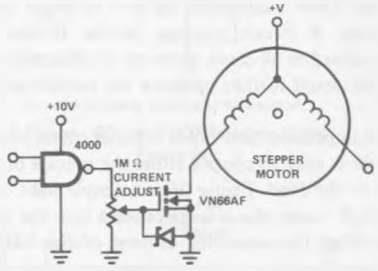
where $\Delta T = T - T_A$, the rise in temperature.

Many loads have undesirably high surge currents when power is first applied–motors and incandescent light bulbs, for instance. The soft-startup circuit in Figures 30 and 31 will minimize or eliminate these current surges,, which, in the case of the incandescent light bulb, will increase its life considerably. Adjust the 1M Ω potentiometer in Figure 30 until the desired maximum current is obtained, or use a fixed divider if a wider tolerance is allowable. R_1 and C_1 in Figure 31 have a 0.1 second time constant to increase the input drive voltage–and hence the drain current–of the VN66AF gradually.

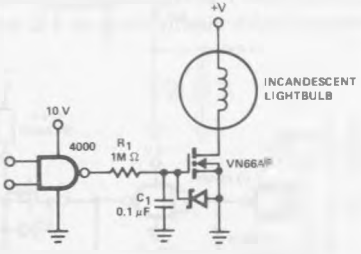
This increase in ON resistance may lead to problems unless certain design precautions are taken. In a typical switching situation, such as that of Figure 32, the current passing through the ON switch is nearly constant. In this example, one amp of current passes through the VN66AF and causes it to heat up. As the ON resistance goes up the voltage drop across the VN66AF increases, and the dissipation climbs further.



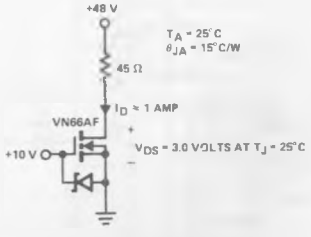
$R_{DS(ON)}$ vs Temperature of the 2N6660
Figure 29



A Circuit which Current Limits the Drive to the Motor
Figure 30



A Soft-Start-Up Circuit Reduces the Cold Current of the Bulb
Figure 31



A Typical Switching Circuit
V_{DS} Increases as the VN66AF Heats Up
Figure 32

If inadequate heat sinking is used, the ON resistance and junction temperatures will increase until the resistance is stabilized by extra charge carriers which are thermally generated in the channel. Since this occurs above the maximum safe junction temperature of 150°C and the long term reliability may be impaired, it is desirable to anticipate this increase in ON resistance and temperature.

There are two ways to do this. The first, a rough rule of thumb, is to add an extra 50% to the actual power dissipation figure before calculating heat sink requirements. For example, if 1 A flows through a device whose ON resistance is 3 Ω at 25°C, the calculated power is 3 W. Now simply calculate the heat sink requirements using 4.5 W as the total dissipation to arrive at a close approximation of the actual heat sinking required at moderate and high temperatures (it will be conservative if the temperature rise is slight).

To calculate the heat sink requirements more precisely, express the rise in junction temperature, ΔT, in terms of the power dissipation and the junction to ambient thermal resistance, θ_{JA}:

$$\Delta T = I^2 R_{DS(T)} \theta_{JA} \qquad (2)$$

which can be combined with Equation 1 and rearranged as:

$$\Delta T\, e^{-0.006\Delta T} = I^2 R_{DS(T_A)} \theta_{JA}. \qquad (3)$$

This is the classical expression for the temperature rise of any fixed resistor, with the addition of the exponential term.

Solve Equation 3 with the values shown in Figure 29 to find the actual junction temperature.

$$\Delta T\, e^{-0.006\Delta T} = (1A)^2(3.0\ \Omega)(15°C/W)$$
$$= 45°C$$

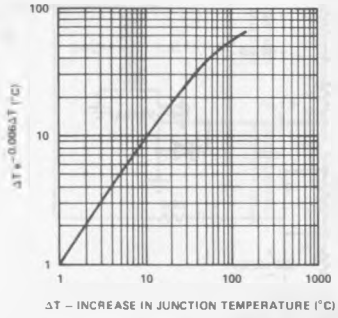
Next, find ΔT in Figure 33, by locating 45°C on the vertical axis. The actual rise in junction temperature, 70°C is located on the horizontal axis. T_J is therefore 95°C.

Figure 33, a plot of $\Delta Te{-}0.006\Delta T$ vs ΔT, is useful in finding the actual temperature rise of the VN66AF when the power dissipation at 25°C junction temperature is known.

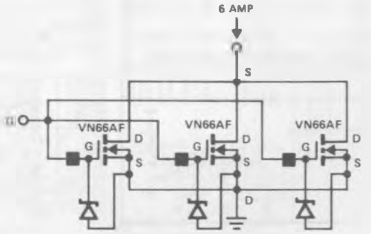
You can also use Figure 33 to find the required heat sinking when the power dissipation maximum allowable junction temperature is specified. For example, if the ambient temperature in Figure 29 is increased to 50°C, $R_{DS(T_A)}$ becomes 3.5 Ω and the normalized power 3.5 W. If the maximum junction temperature is specified as 125°C (ΔT = 75°C), $\Delta Te{-}0.006\Delta T$ must be less than 48°C and $\theta_{JA} < 13.7°C/W$. A heat sink with $\theta_{JA} < -3.7°C/W$ should be used, since θ_{JC} of the VN66AF is 10°C/W. Note that if the rule of thumb were used and 50% added to the 3.5 W figure, the θ_{JA} would be calculated as 14.3°C/W, quite close considering the approximations involved.

Parallel and Series Operation

The current handling capability of VMOS may be increased quite easily by simply paralleling several devices (Figure 34). No ballasting resistors or thermal matching networks are needed because the currents tend to equalize. If a particular device starts to draw more current, it heats up more and conducts less current than it would otherwise. For example, an initial unbalance of ±20% (the typical worst case figure) will reduce to ±14% if the junction temperatures are allowed to approach their maximum limits. Because of the excellent high frequency response of the VN66AF, however, ferrite beads or small valued resistors (≈ 100 Ω to 1000 Ω) in series with each gate are necessary to suppress spurious high frequency (~300 MHz) oscillations.



A plot of $\Delta T\, e^{-0.006\Delta T}$ vs ΔT is useful in finding the actual temperature rise of the VN66AF when the power dissipation at 25°C junction temperature is known
Figure 33



Paralleling VN66AF's Increases the Maximum Current Handling Capability
Figure 34

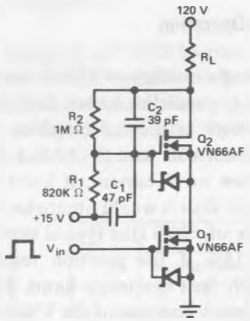
Devices may be connected in series to increase breakdown voltage, as shown in Figure 35. R_1 and R_2 are large because the drive current to the gate of Q_2 is small, while C_1 and C_2 form a capacitive divider which dynamically balances the gate drive and also insures fast switching times by converting charge to the gate of Q_2. C_1/C_2 should be approximately equal to R_2/R_1, with allowance for stray capacitance and the enhancement voltage of Q_2. The bottom of the divider chain is returned to 15 V, rather than ground, to insure sufficient enhancement for Q_2 when the devices are ON. By properly selecting resistor and capacitor values, any number of VMOS may be series connected in this manner.

Amplifier Applications

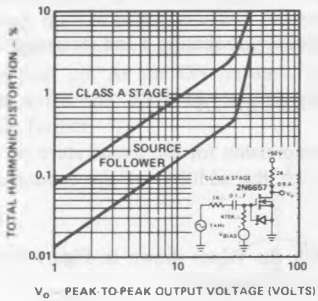
The constant g_m region of VMOS makes it well suited for linear applications, since distortion is low over a wide dynamic range when properly biased. Figure 36 is a graph of the harmonic distortion vs output voltage for a simple class A test circuit employing the 2N6657, a 25 W TO-3 version of the VN66AF. Inherent distortion rises almost linearly with output voltage at low signal levels, but then rises more sharply as the positive signal peaks extend into the non-linear g_m region and the negative peaks saturate the device. The gain of the circuit is about 6.5, equal to $g_m R_L$ (0.27 mmho x 24 Ω).

Using the 2N6657 as a source follower reduces the distortion by a factor of 5.5, which is slightly less than the amount by which the gain is reduced. Figure 37 shows that the frequency response of a simple class "A" stage is flat to almost 10 MHz.

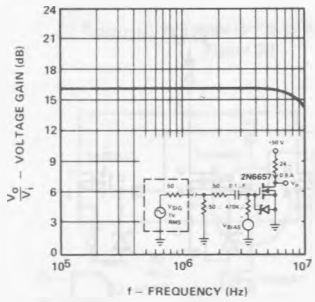
The simple audio amplifier shown in Figure 38 is equivalent to the audio output stage of many inexpensive radios, televisions, and phonographs. Power output is about 4 W from 100 Hz to 15 kHz. The design is greatly simplified by the use of an output transformer, and distortion is kept relatively low (2% at 3 W) by 10 dB of negative feedback. No thermal stabilization components are needed since the positive temperature coefficient of the drain-source ON voltage makes thermal runaway impossible.



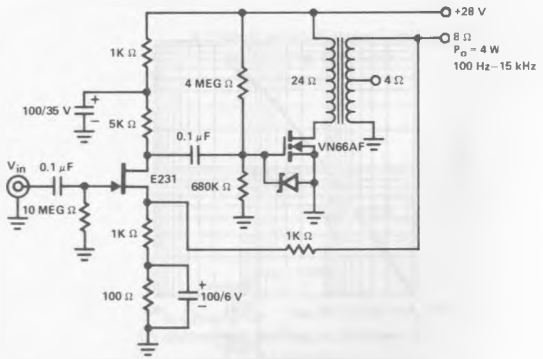
The Breakdown Voltage May Be Doubled By Connecting Device in Series
Figure 35



Harmonic Distortion vs Voltage Output for a Simple Class A Stage and a Source Follower
Figure 36



Frequency Response of a Simple Class A Stage
Figure 37

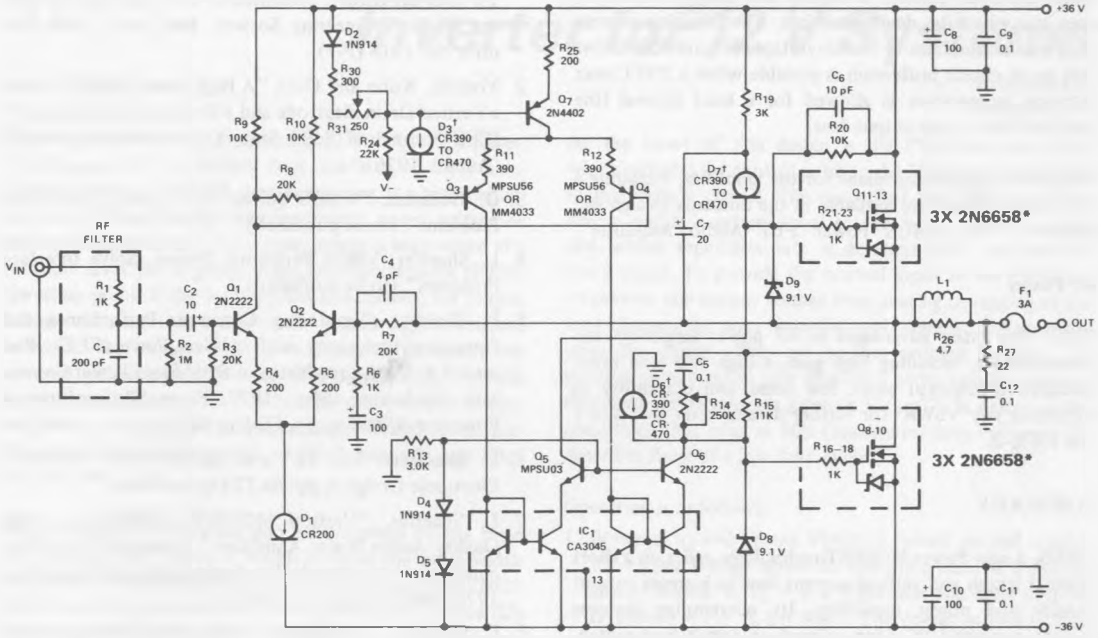


A Simple Audio Power Amplifier
Figure 38

Figure 39 shows a high fidelity 40 W audio amplifier suitable for high quality stereo or quadraphonic systems. This amplifier has low open loop distortion, relatively small amounts of negative feedback (22 dB), and good open loop frequency response (400 KHz) to minimize transient intermodulation distortion. Closed loop frequency response (exclusive of the input filter) is flat to 4 MHz, and the slew rate is over 100 V/μs. The frequency response and performance of the amplifier, which is operated class AB with an idling current of 300 mA, are shown in Figure 40.

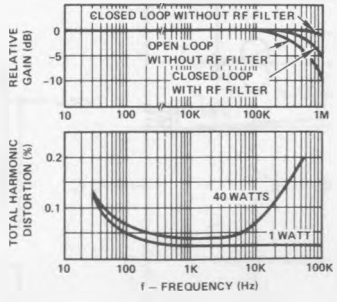
Since only N-channel VMOS devices are presently available, a quasi-complementary design is necessary and some means are required for matching the characteristics of the common source and common drain output stages.

The most effective method is to use a resistor (R_{15} in Figure 39) to provide local feedback from the drain back to the gate of the common source stage and then drive the gate with a modulated current source.



†CURRENT REGULATORS D_3, D_6 AND D_7 CAN USE ANY VALUE FROM CR390 TO CR470, BUT ALL 3 ON A PC BOARD MUST USE THE SAME VALUE.
*SIMILAR PERFORMANCE CAN BE OBTAINED USING PLASTIC POWER TAB TRANSISTORS. SUBSTITUTE 4 X VN88AF S AND TO 202 HEAT SINKS FOR THE OUTPUT. KEEP THE SUP PLIES BELOW THE VN88AF 80V BV_{DSS}

A High Quality 40 W VMOS Amplifier
Figure 39



Gain and Distortion vs Frequency of the VMOS Amp
Figure 40

Figure 41 depicts this technique and compares it to the corresponding circuit for an actual source follower. An analysis of the circuits reveals that both have the same values of gain and output impedance, which insures a good match between the positive and negative waveforms during class AB operation. Exact matching is insured by R_{14} and C_6 (Figure 39). Functional output protection is provided by the zener diode which limits the output current and device dissipation by limiting the gate enhancement. Clamping the gate-to-source voltage at a maximum of 9 V limits the drain current at slightly less than 2 A at 25°C, even less when the devices are hot. The resulting current limit versus the drain-to-source voltage, (Figure 42), shows that short circuit protection is possible when a 200°C max junction temperature is allowed for a brief interval (the time constant of the output fuse)

Complete construction plans for the amplifier, including a P.C. board layout, are available in the Siliconix Design Aid DA76-1, "The VMOS Power FET Audio Amplifier".

RF Power

VMOS has many advantages in RF power amplifiers and pre-amplifiers, including high gain, a high two-tone intermodulation intercept point, low noise, and the ability to withstand any VSWR for further details, refer to TA76-1 and TA76-2.

SUMMARY

VMOS, a new Power MOSFET technology, relies on a short channel length and vertical current flow to increase current density and power capability. Its outstanding features include negligable DC drive current, extremely fast switching times, no minority carrier storage time, a complete lack of secondary breakdown and current hogging, and low distortion. VMOS devices are being designed into numerous power applications, including both general purpose and high speed switchers, high quality audio amplifiers and switching regulators.

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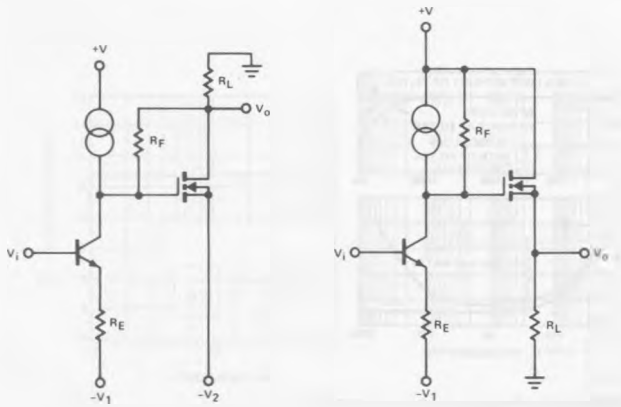
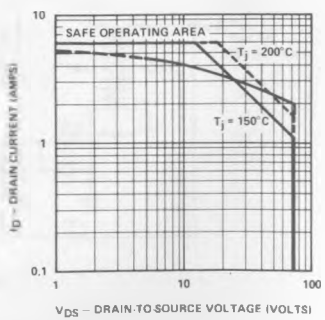


A Quasi Source Follower and a Real Source Follower
Figure 41



Current Output vs Drain-to-Source Voltage
3 2N6658's in Parallel, when V_{GS} = 9 V
Figure 42

Application Note AN79-1

A 500 kHz Switching Inverter for 12 V Systems

Barry Harvey
January 1979

This note describes the design of a 12 V to ±20 V inverter. The design is of the flyback type, made much more practical by the use of VMOS devices running at a high switching rate. It is an energy transfer circuit, not a voltage or current transfer circuit; the output power is maintained at a constant level for a given pulse width-modulator (PWM) operating point. If the load requires less current, the output voltage will soar. Conversely, if the output current demand increases, the output voltage will sag to maintain the constant output power (V x I). This contrasts sharply with conventional circuits that deliver a constant output voltage per PWM operating point. Maintaining constant power permits simplified circuitry with reduced magnetic and filter requirements.

The principles of operation may be described by the basic circuit shown in Figure 1, which includes the pulse width modulator (PWM) control circuit; the high frequency VMOS Power Switch; the flyback circuit inductor (L), diode (D) and capacitor (C); and an error amplifier.

At the heart of this design is the PWM control circuit which provides the control pulse to the VMOS Power Switch in the flyback circuit. The output of the PWM is a pulse whose width is proportional to the input control voltage and whose repetition rate is determined by an external clock signal. To provide the control input to the PWM and to prevent the output voltage from soaring or sagging as the load changes the error amplifier and reference voltage complete the design. They act as the feedback loop in this control circuit much like that of a servo control system. Pertinent waveforms are given in Figure 2; 2a describes the conditions that exist at 50% (maximum) duty cycle and 2b describes those at a low duty cycle.

Operation is as follows:

1. Between t_0 and t_1 the VMOS is turned on and applies the supply voltage across L. The drain current is closely approximated as $I_L = t \times V_S/L$ and the final current I_L (peak) = $(t_1 - t_0)\ V_S/L$. The energy stored in L is $E_L = (t_1^2 - t_0^2)\ V_S^2/2L$.

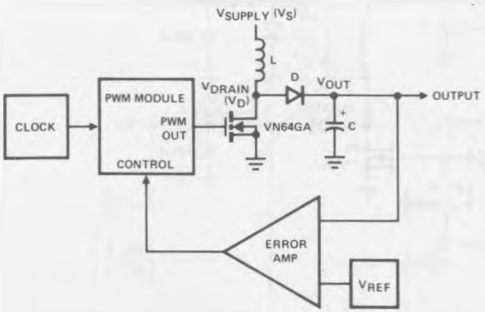


Figure 1.

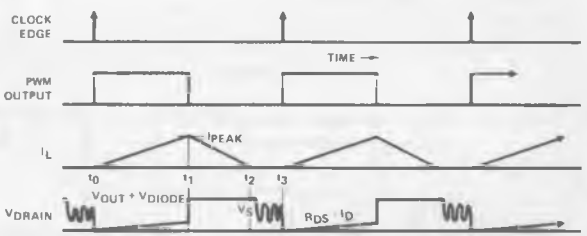


Figure 2a.

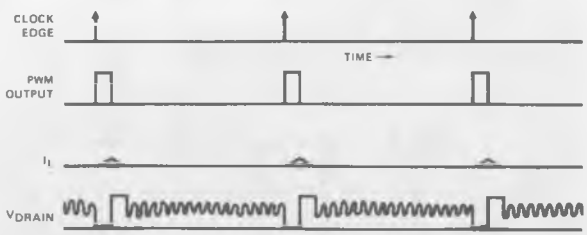


Figure 2b.

2. At the instant of t_1 the VN64GA is turned off and its drain voltage increases to the voltage on C plus the forward voltage drop of D because of the inductor L. This works well when V_{OUT} is much larger than V_S and permits nearly all of the energy stored in L to be transferred to C with no large current or voltage spikes.
3. Between t_2 and t_3, no net DC current flows through L, and V_{DRAIN} tends toward V_{SUPPLY}, although a ringing will occur between L and the capacitance of the VMOS and D. The cycle is repeated at a frequency f_{CLOCK}, such that the power drawn from V_S is $(1/2\,(t_1 - t_0)^2\,V^2_S)/f_{CLOCK}$.

If we let the duty cycle $\delta = \dfrac{t_1 - t_0}{t_3 - t_0} = (t_1 - t_0)\,f_{CLOCK}$, where $f_{CLOCK} \equiv \dfrac{1}{t_3 - t_0}$, then $P_{IN} = \dfrac{\delta\,V^2_S\,(t_1 - t_0)}{2}$.

If $\delta = 1/2$ max, then P_{IN} max $= V^2_S/8L\,f_{CLOCK}$.

The peak current through the VMOS will closely be $\dfrac{4\,P_{OUT}}{\eta V_S}$; and the value of inductor L will be $\eta V^2_S/8\,f_{CLOCK}\,P_{OUT}$, where η is the overall power efficiency of the circuit.

The power losses in the circuit are, in order of importance:

A. $(I_D)^2\,R_{DS}$ loss in the VMOS switch
B. $I_{LOAD}\,V_F$ loss in the catch diode D
C. Transient charge losses in D due to a slow turn-on characteristic. This actually allows many volts of forward bias on D just at time T_1 while the diode is attempting to turn-on. Turn-off losses are not important in this circuit.
D. Loss in L due to hysteresis and saturation effects. The inductor is required to pass all of $I = 4P_{OUT}/\eta\,V_{SUPPLY}$, which usually results in magnetic saturation and losses. Fortunately, the higher frequencies allow fewer turns on L, reducing the number of turns and I_{SUPPLY} product, and the core material of L can be high-frequency ferrite, which is less prone to saturation (for a given inductance).
E. Simple $C_{STRAY}\,V^2_{OUT}\,f_{CLOCK}$ losses, where C_{STRAY} includes C_{DS} of the VMOS and C_D of the rectifier.

Figure 3 is the schematic of a simple 35 watt inverter designed to produce ±20 V regulated outputs from 12–16 volt inputs. U_1 is a simple Schmitt-trigger oscillator with a nominal 50% duty cycle. This duty cycle waveform buffered into Q_5 by Q_4 and U_2 through U_6 runs the system at full output power.

The duty cycle is reduced to stabilize the output voltage by the feedback amplifier Q_2 and its 18 V zener. Q_1 and its associated diodes switch Q_2's discharge current away from C during the discharge period of the transformers field, and allow it to shorten the period in which primary current is drawn through the transformer. Q_3 and its 21 V zener prevent the output from soaring (if a fault condition occurs in the feedback regulator) by simply clamping Q_5's gate drive.

L is wound on a ferrite core; I used a wideband toroid 1 1/2" in diameter with a cross-sectional area of about 1/10 in^2. The resistance of the winding should be held to less than 1/20 Ω; #22 wire is adequately large.

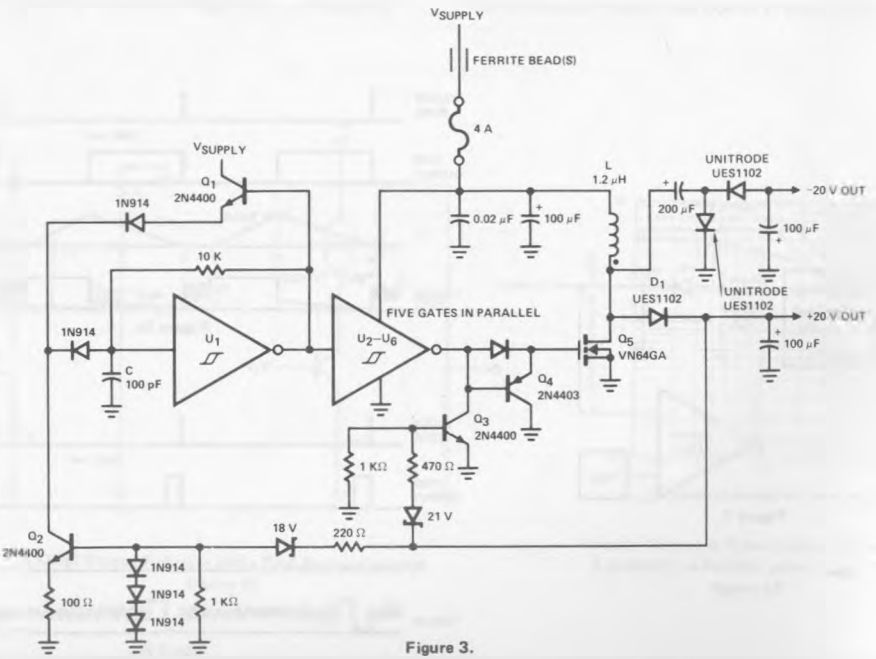


Figure 3.

VMOS in microprocessor stepper motor control

E. Davies

In this case, an RCA 1802 CMOS microprocessor was used to generate the necessary waveforms to control a 4-phase stepper motor. Other microprocessors could well be used with slightly modified interfacing and software. Fig. 1 shows a basic stepper motor control unit. Control signals (see Fig. 2) are imposed on gates 1 through 4 of the VN64GA VMOS Power FETs, allowing current to flow in the appropriate phases of the stepper motor. As each VMOS phase switch is turned ON, the phase current builds up as the back emf of the winding is overcome. One method of speeding up this current build-up is to increase the motor supply voltage and insert series resistors R_s to limit the maximum phase current. This technique, known as "overdrive", improves motor torque at higher stepping rates. Fig. 3 shows how the torque/speed characteristic is improved by employing overdrive. However, conventional overdrive exhibits poor operating efficiency due to the power consumed in the lossy series resistors. Efficiency can be considerably increased by using chopper drive techniques.

Fig. 1. A basic stepper motor control unit.

Box 1 1802 Software Listing

8000	F8*		AE	80C7	D0**
	80		65		F8
	B0		D6		FE
	F8		3D		AB
	FF		3B		F8
	AE		EB		FF
	2E		7E		AD
	F8		73		EB
	FF		60		6E
	AF		AE	D0	F8
	2F		36		F0
	8F		40		F2
	3A		30		F6
	0A		28		5D
	8E				F6
	3A	40	37		F6
10	06		3B		ED
	F8		3F		F4
	E5		42		5D
	A6		D7		EB
	F8		8E		F8
	C8		35		0F
	A7		53		F2
	F8		EB		ED
	80		76		F4
	B6		73	E0	AD
	B7		60		30
	F8		AE		C7
	00		65		D0
	B8		D6	E4	D0†
	B9		2D		F8
	BA	50	8D		FF
20	BB		32		AB
	BC		3B		EB
	BD		3D		6F
	BE		5E		FA
	BF		EB		0F
	F8		7E		FD
	99		73		0A
	AE		60		AA
	8E		AE		F8
	34		65	F0	B0
	29		D6		A9
	35		2D		29
	34		8D		89
	EB		32		3A
	76		3B		F2
	73	60	30		2A
30	60		45		8A
					3A
					EF
					30
					E4

PROGRAM HELD AT LOCATION 8000 in 2708 PROM.

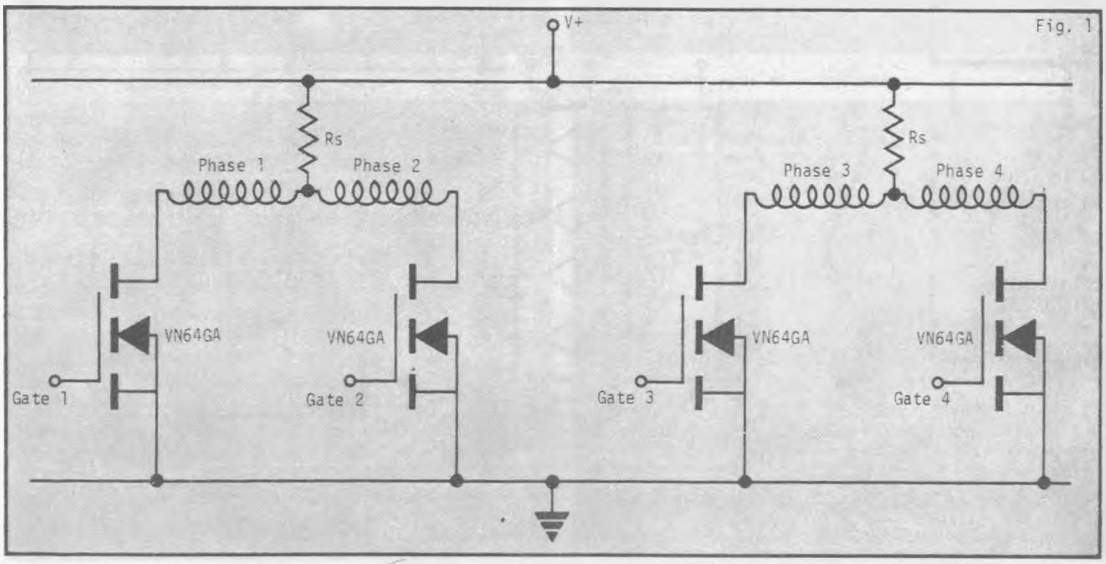
**MAIN PROGRAM **B.C.D. — HEX SUBROUTINE*

†DELAY SUBROUTINE

VMOS-μP chopper drive controller

The control functions are determined by the software which is held in the ROM. A 2708 PROM is a useful evaluation vehicle during program development.

Bits 1 through 4 of the microprocessor's output bus are fed in via AND gates (74C08) and level



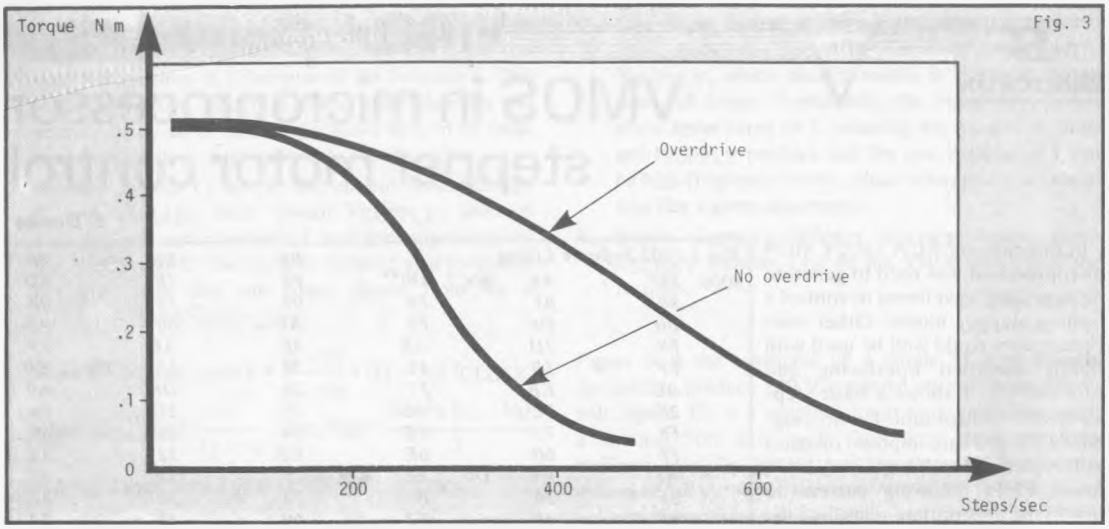


Fig. 3 Typical stepper motor torque speed characteristics with and without "overdrive".

wheel switches. On command, the microprocessor will output this number of bytes at one of its output ports.

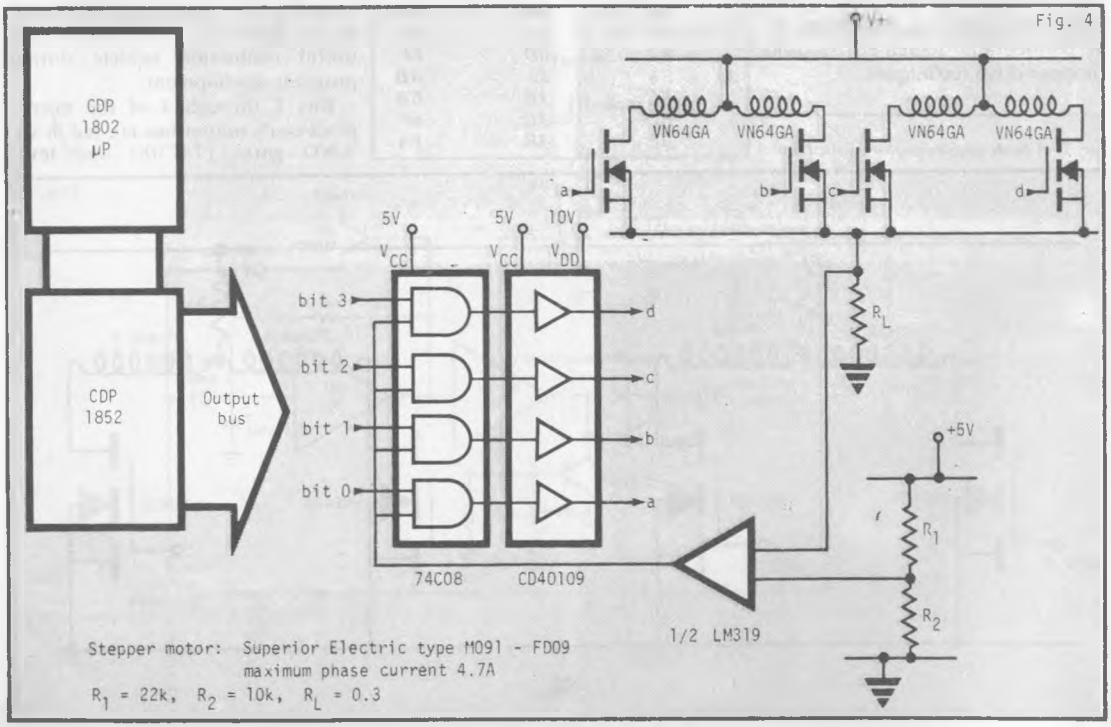
The four least significant bits of the microprocessor output bus are used to control the appropriate VMOS power switches, which in turn drive the stepper motor. The four most significant bits of the output bus may be left redundant or used to drive a second stepper motor in synchronism with the first.

Any one of a range of motor speeds may be selected by a one digit thumbwheel switch.

Readily implemented software modifications allow control features to be improved and extra facilities added. Such features could include larger ranges of pre-programmed step changes and speed run-up sequences to achieve higher maximum motor step rates. The microprocessor offers the end user the option to change motor control functions by simple changes in software. Moreover, Original Equipment Manufacturers can reduce costs by producing standard hardware packages to cover a range of applications.

VMOS offers the OEM a cost effective power switch suitable for interface to such microprocessor-based modules. □

Fig. 4: Switch mode controller employing phase current sensing to block μP control signals to the VMOS power FET array.



Gate 1	Gate 2	Gate 3	Gate 4
High	Low	Low	High
Low	Low	High	High
Low	High	High	Low
High	High	Low	Low

High = 10 volts Low = 0 volts

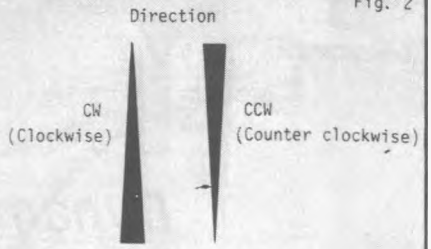


Fig. 2

Fig. 2 Control Signal Combinations.

shifters (CD40109) to the gates of the VN64GA VMOS Power FETs.

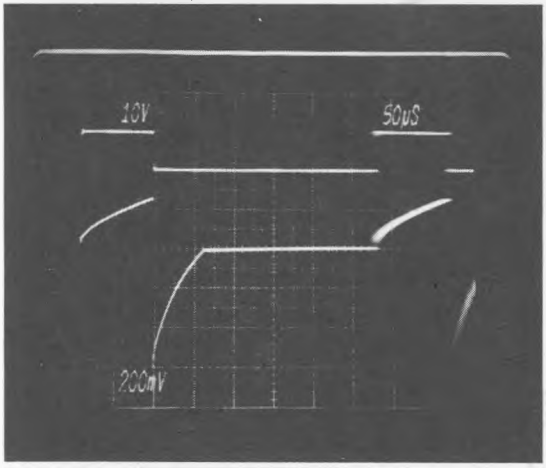
The switching threshold of the comparator LM319 is set equal to $R_L \times I_{MAX}$ such that the control signals present on the microprocessor output are blocked when the phase current of the motor reaches its rated value.

Pics. A-D shows typical waveforms produced in the steady state (motor stationary) by the circuit shown in Fig. 4. The positive supply can be increased to +60 V to optimise the torque/speed characteristic of the system.

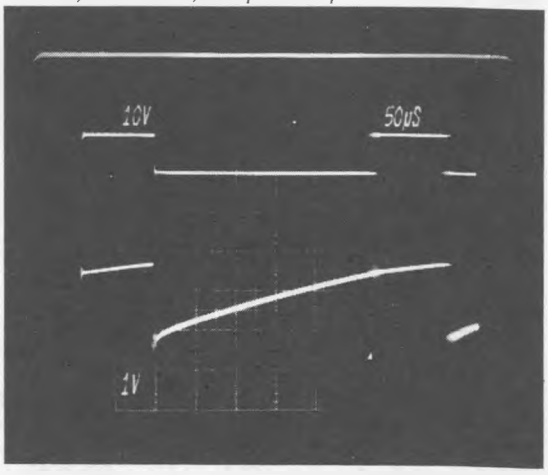
The high switching speed of VMOS ensures that switch transition losses are small. The high input impedance of VMOS implies low current drive requirements. Thus, power dissipation in the control circuitry is reduced and overall efficiency is increased.

Box 1 shows a section of 1802 software which develops the necessary stepper motor drive waveforms. Facilities offered by such a program are run/step, direction, speed and programmable number of steps. The software shown in Box 1 allows a number of steps up to a maximum of 99 to be programmed via thumb-

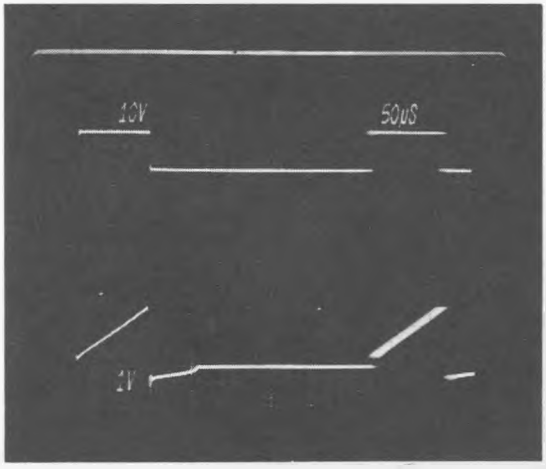
Pic. A: i) Gate volts ii) Drain volts.



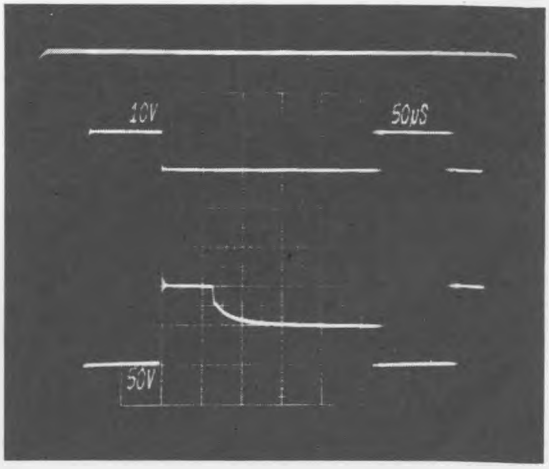
Pic. B: i) Gate volts ii) Comparator o/p.



Pic. C: i) Gate volts ii) Source volts.



Pic. D: i) Gate volts ii) Supply current 10 mA/mV.



Application Note AN79-3

Dynamic Input Characteristics of VMOS Power Switch

Arthur Evans/
Dave Hoffman
January 1979

INTRODUCTION

The driver-power requirement for a VMOS switch is a function of how fast we want to turn it ON and OFF.

The DC input resistance of a VMOS Power FET is in excess of 10^{12} ohms. When used as a switch, the power required to keep it ON or OFF is negligible. However, energy is required to change it from one state to the other. The turn-ON and turn-OFF speeds will determine the input power requirement.

If the FET equivalent input capacitance, C_{in} and the change in V_{gs} are known, the required energy can be estimated:

$$W = 1/2\ C_{in}\ \Delta V_{gs}^2 \text{ watt-seconds} \quad (1)$$

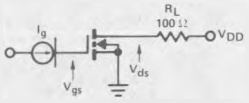
C_{in} is a function of V_{gs} and V_{ds}. During switching it changes during the transition from the ON state to the OFF state. Typically the capacity characteristics specified on the FET data sheet are given for a fixed bias condition. This may present a problem in trying to estimate C_{in} for the above energy equation.

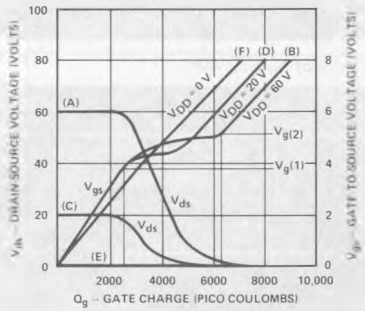
A better method is to determine the gate charge, Q_g, as a function of V_{gs}. The difference in Q_g for the ON state and the OFF state will give the energy required to make the change:

$$W = 1/2\ (\Delta Q_g)\ (\Delta V_{gs}) \text{ watt-seconds} \quad (2)$$

Figure 1 shows V_{gs} vs Q_g characteristics of a VMOS type VN64GA. These curves were obtained by using a switched, constant-current drive for the gate.

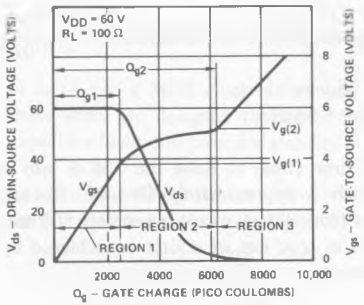
CURVE	V_{DD}	CHARACTERISTIC
A	60 V	V_{ds} vs Q_g
B	60 V	V_{gs} vs Q_g
C	20 V	V_{ds} vs Q_g
D	20 V	V_{gs} vs Q_g
E	0 V	V_{ds} vs Q_g
F	0 V	V_{gs} vs Q_g





VMOS Input (V_{gs}) and Output (V_{ds}) Characteristics
Figure 1

The curves for V_{DD} = 60 volts are reproduced in Figure 2 for further discussion. Three regions are obvious on the input characteristic curve. In region 1 V_{gs} is below threshold and the FET is OFF. In region 2, as V_{gs} exceeds V_{g1}, drain current begins to increase until, at V_{g2}, V_{ds} saturation is reached. In region 3 V_{ds} is saturated and no further change in I_D or V_{ds} occurs.



VMOS Input and Output Characteristics
Figure 2

Capacitance in region 1 is fairly constant as indicated by the constant slope. Its value is approximately:

$$C_{in(1)} = \frac{Q_{g1}}{V_{g1}} \qquad (3)$$

$$= \frac{2450\ pC}{3.8\ V} = 645\ pF$$

In region 2, C_{in} increases because the FET begins to turn ON and V_{ds} begins to change, thus increasing the rate of change of V_{gd}. The MILLER EFFECT on C_{gd} causes C_{in} to increase. This effect stops after the device is fully ON and V_{ds} ceases to change. The approximate capacitance in this region is:

$$C_{in(2)} = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} \qquad (4)$$

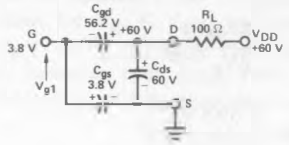
$$= \frac{(6250 - 2450)\ pC}{(5.1 - 3.8)\ V} = 2923\ pF$$

In region 3 V_{ds} is saturated at a low value and is no longer changing. The FET channel is ON and C_{in} is higher than it is in region 1, but not as high as in region 2. No MILLER EFFECT is occurring. The characteristic shows:

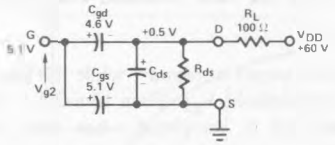
$$C_{in(3)} = \frac{\Delta Q_g}{\Delta V_{gs}} = 875\ pF \qquad (5)$$

$C_{in(1)}$ and $C_{in(3)}$ correspond to C_{iss}, and are approximately equal to C_{gs} + C_{gd}. They differ in magnitude because of the differences in V_{dg} in regions 1 and 3. Figure 3 shows the bias conditions for C_{gs} and C_{gd} at the end of region 1 ($V_{gs} = V_{g1}$) and at the beginning of region 3 ($V_{gs} = V_{g2}$) (we assumed $V_{ds(sat)} \simeq 0.5$ V).

Bias condition at end of region 1

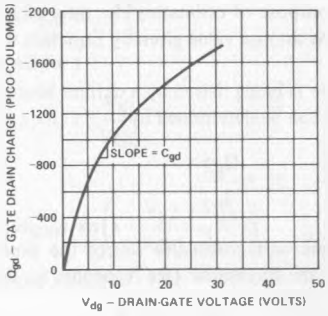


Bias condition at start of region 3



Bias Conditions for C_{gd}, C_{gs} and C_{ds}
Figure 3

There is a large change in the bias on C_{gd}. In region 1 the drain area under the gate is depleted of carriers, thus C_{gd} is greatly reduced. In region 3 the drain region under the gate is flooded with carriers because the device is ON, thus is much greater. Figure 4 shows the characteristic Q_{dg} vs V_{gd} for a typical VN64GA.



Gate-Drain Capacitance Characteristic
Figure 4

The typical C_{iss} given in the VN64GA specification sheet is 640 pF. This agrees with $C_{in(1)}$ estimated above from Figure 3. In both cases the device is OFF and C_{gd} has a large reverse bias.

In region 2, where the FET is in the process of switching, C_{in} is approximately:

$$C_{in(2)} \simeq C_{iss} - A_V C_{rss} \qquad (6)$$

Where $A_V = \Delta V_{ds}/\Delta V_{gs}$, and $C_{rss} = C_{gd}$.

For our example, using typical values for C_{iss} and C_{rss} from the data sheet and ΔV_{ds} as indicated in Figure 3, we get:

$$C_{in(2)} = C_{iss} - \frac{\Delta V_{ds}}{\Delta V_g} C_{rss} \quad (7)$$

$$= 640 - \left(\frac{-59.5\ V}{1.3\ V}\right) 50$$

$$= 2928\ pF$$

which agrees with the value estimated with Figure 2 and Equation 4.

A turn-ON delay occurs in region 1 while the gate is being charged up to threshold V_{g1}. Then turn-ON of the FET channel starts and is completed when V_{ds} saturation occurs at V_{g2}.

Overdrive is occuring in region 3. The excess charge in region 3 causes a turn-OFF delay. Turn-ON and turn-OFF delays could be decreased by pre-biasing the gate to a V_{gs} just below V_{g1} and by avoiding overdriving into region 3. This, however, would decrease the switching circuit noise-margin and would require closer control of the gate drive voltage and $V_{gs(th)}$ of the VMOS.

Figure 2 shows that $C_{in(1)}$ and $C_{in(3)}$ are fairly constant. $C_{in(2)}$ increases as V_{ds} decreases because C_{gd} increases. For the purpose of estimating the time of region 2 we can assume the average value given by Equation 4.

If the gate is being driven by a current source, I_g, the times t_1 and t_2 can be determined by:

$$t_1 = \frac{Q_{g1}}{I_g}; \quad t_2 = \frac{Q_{g2}}{I_g} \quad (8)$$

For drivers with a resistive source the times can be estimated by the Equations: (see Appendix for derivation)

$$t_1 = -\frac{Q_1}{V_{g1}} R_{gen}\ \ell n\left(1 - \frac{V_{g1}}{V_{GG}}\right) \quad (9)$$

$$t_2 - t_1 = -\frac{Q_2 - Q_1}{V_{g2} - V_{g1}} R_{gen}\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad (10)$$

where V_{GG} is driver open-circuit voltage and R_{gen} is driver output resistance.

For example, assume a 10 volt driver has an output resistance, R_{gen}, of 10,000 ohms. From the input characteristic curve of Figure 2 we get:

$Q_{g1} = 2450$ pC,
$Q_{g2} = 6250$ pC,
$V_{g1} = 3.8$ volts
$V_{g2} = 5.1$ volts.

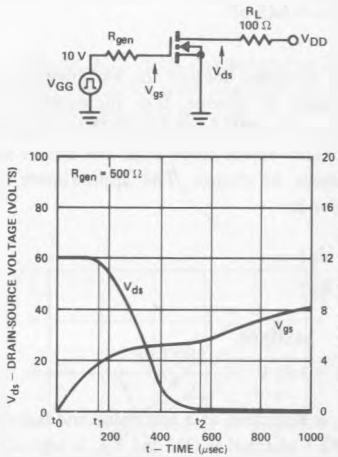
Using Equations 9 and 10 we calculate:

$t_1 = 3.08\ \mu sec$
$t_2 - t_1 = 6.88\ \mu sec$

Turn-ON time (time to drive the VMOS into saturation) is t_2 which is approximately 10 μsec. Reducing R_1 to 500 ohms reduces t_{ON} to approximately 500 nsec. Further reductions in t_{ON} can of course be achieved by reducing R_1 even more.

Turn-OFF times can be calculated in a similar manner. From the ON state V_{gs} starts at V_{GG}. A delay occurs until V_{gs} drops to V_{g2}. Below V_{g2}, V_{ds} begins to come out of saturation, and the FET will be completely OFF when V_{gs} drops below the threshold voltage V_{g1}.

Figure 5 shows input and output characteristics for R_{gen} = 500 ohms. Measured t_1 and t_2 were four to eleven percent higher than the calculated values. Measured and calculated times are shown in Table I.



VMOS Switch Characteristics
Figure 5

TABLE I

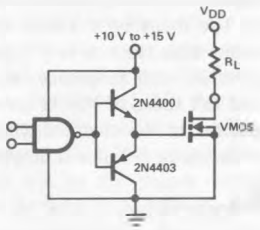
TIME	R_{gen} = 10,000 Ω		R_{gen} = 500 Ω	
	CALCULATED	MEASURED	CALCULATED	MEASURED
t_1	3.08 μsec	3.2 μsec	154 nsec	160 nsec
$t_2 - t_1$	6.88 μsec	7.2 μsec	344 nsec	395 nsec
t_2	9.96 μsec	10.4 μsec	498 nsec	555 nsec

Since gate input-power is needed only during the switching transitions, a driver that has low stand-by power but is capable of supplying high current pulses during switching transitions is desirable if high-speed switching is needed. For the VN64GA as shown in Figure 2, 6250 pC is needed to charge the gate to V_{g2} which drives the output to saturation. Equation 8 shows that to achieve a t_{ON} of 20 nsec:

$$I_g = \frac{6250 \cdot 10^{-12}\ C}{20 \cdot 10^{-9}\ s} = 313\ mA.$$

One solution is to use a MOS clock driver such as the MH0026. These units are designed to deliver high peak currents to capacitive loads and have low standby power.

Another solution is to buffer the logic driver with a complementary emitter-follower as shown in Figure 6.



Driver with Emitter-Follower Buffer
Figure 6

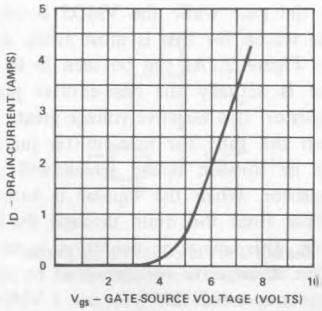
Effect of Drain Load on Q_{g2}

The characteristics presented thus far were with a drain load resistance of 100 ohms. With V_{DD} = 60 volts the maximum I_D = 600 mA.

For different values of $I_{D(max)}$ the required V_{g2} can be obtained from the FET transfer characteristic curve I_D vs V_{gs}. Then with this value of V_{g2}, Q_2 can be estimated from the appropriate V_{DD} curve of Figure 1.

For example, assume a saturated load current of 2 amperes is needed and V_{DD} is 60 volts. The transfer curve of Figure 7 indicates for I_D = 2 amperes that $V_{gs} \simeq 6$ volts. The 60 volt V_{DD} curve of Figure 1 (curve B) shows that Q_g is about 7000 pC.

The drain load has practically no effect on Q_{g1} and thus no effect on t_1.



VNG Transfer Characteristic
Figure 7

APPENDIX

In the derivation of Equation 9 and 10 we assumed that $C_{in(1)}$ is constant for $V_{gs} \leq V_{g(1)}$ and that $C_{in(2)}$ is constant for $V_{g(1)} \leq V_{gs} \leq V_{g(2)}$. Figure A1 shows a pulse generator having an open circuit voltage V_{GG} and an output resistance R_{gen}, driving a capacitor C_{in}.

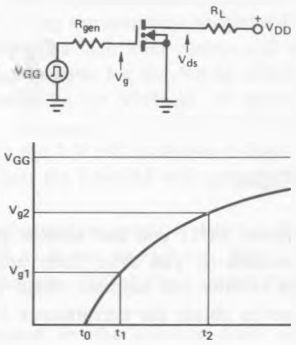


Figure A-1

For a constant C_{in}, V_g as a function of time is:

$$V_g(t) = V_{GG}\left[1 - \exp\left(\frac{-t}{R_{gen}\ C_{in}}\right)\right] \quad (A1)$$

$$\frac{V_g(t)}{V_{GG}} = \left[1 - \exp\left(\frac{-t}{R_{gen}\ C_{in}}\right)\right] \quad (A2)$$

Solving Equation A2 for t_1:

$$t_1 = (C_{in(1)}\ R_{gen})\ \ell n\ 1 - \frac{V_{g1}}{V_{GG}} \quad (A3)$$

The time: $t_2 - t_1$

$$t_2 - t_1 = (C_{in(2)}\ R_{gen})\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad (A4)$$

In our example from Figure 2

$$C_{in(1)} = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g1}}{V_{g(1)}} \quad (A5)$$

and

$$C_{in(2)} = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g2} - Q_{g1}}{V_{g(2)} - V_{g(1)}} \quad (A6)$$

therefore:

$$t_1 - t_0 = \frac{Q_{g1}}{V_{g(1)}}\ R_{gen}\ \ell n\left(1 - \frac{V_{g(1)}}{V_{GG}}\right) \quad (A7)$$

and

$$t_2 - t_1 = \left[\frac{Q_{g(2)} - Q_{g(1)}}{V_{g(2)} - V_{g(1)}}\right] R_{gen}\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad (A8)$$

Since C_{in} changes at $V_{g(1)}$ we use this two-step method to determine the total turn-ON time t_2.

Application Note AN79-4

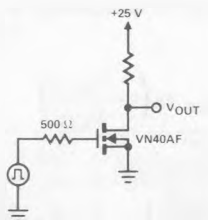
Driving VMOS Power FETs

Dave Hoffman
January 1979

INTRODUCTION

Using VMOS Power FETs you can achieve performance never before possible—if you drive them properly. This article describes circuits and suggests design methods to be used in order to obtain the performance from VMOS that you need.

When designing with VMOS there are some facts that must be kept in mind in order to get optimum results with every circuit. The first fact is that VMOS is a very high frequency device. The cut-off frequency for all VMOS FETs is several hundred megahertz. Most power designers are not used to designing with extremely high frequency devices because with bipolars the frequency response decreases as the power increases. The very high frequency response of VMOS is the basis for many of its advantages but it must be kept in mind while designing. With improper circuit design VMOS can oscillate. This oscillation can be eliminated, though, by exercising two simple precautions. First, minimize lead and trace lengths whenever possible, especially leads associated with the gate of the FET. If it is not possible to have short leads to the gate place a ferrite bead on the gate lead or a small resistor in series with the gate. The ferrite bead or the resistor must be very close to the gate. Second, because of the extremely high input impedance of VMOS (in excess of 10^{12} Ω) drive circuits may be designed which are very high impedance. Under these conditions it is possible for the gate node to get enough positive feedback from the gate-to-drain capacitance or just from stray fields in the circuit to cause oscillation. This must be kept in mind in the design of the circuit.



A Typical VMOS Switching Circuit
Figure 1

When driving VMOS it must be kept in mind that the dynamic input impedance is very different than the static input impedance. The input of a VMOS device is capacitive. The DC input impedance is very high but the AC input impedance varies with frequency. Because of this effect, the rise and fall times of VMOS are dependent on the output impedance of the circuit driving it. The first approximation of the rise or fall time is simply

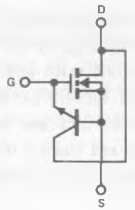
$$t_r \text{ or } t_f = 2.2 \cdot R_{OUT} \cdot C_{iss} \quad (1)$$

where R_{OUT} is the output impedance of the drive circuit. This equation is valid only if the drain load resistance is much larger than R_{OUT}. Knowing this fact, along with the fact that there is no storage or delay time with VMOS, it is very easy to calculate the rise and fall times and set them to any desired value. For example, if you wanted to calculate the 10% to 90% rise or fall time for the circuit shown in Figure 1 using Equation 1 the rise time is equal to:

$$t_r = (2.2)\,(500)\,(50 \times 10^{-12}) = 55 \text{ nsec}$$

The dynamic input characteristics of VMOS are covered very thoroughly in Siliconix' application note AN79-3.[1]

A last thing to remember when you are driving VMOS is the input protection zener diode. When putting a positive voltage on the gate with respect to the source, the maximum voltage rating of the zener diode should not be exceeded. It is more important, however, that you do not forward bias the zener diode by putting a negative voltage on the gate while the VMOS is operating in a circuit. The reason for this is most easily explained by referring to Figure 2. As can be seen in the figure, the zener diode is actually the base-emitter junction of a bipolar transistor. If a negative voltage greater than 0.6 V is placed on the gate, the base-emitter junction of the bipolar will be forward biased which will turn on the bipolar transistor. When the bipolar is turned on, current will flow from the drain through the bipolar and out the gate. This operating condition is very likely to be destructive. If negative voltages must be placed on the gate it is recommended that you use a VMOS part that does not have an input zener diode. Non-zenered equivalents are available for most of Siliconix' zenered devices.



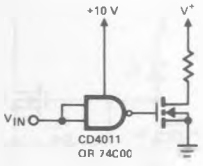
A Parasitic NPN Transistor in Zener Protected MOSFETS
Figure 2

Of all operating modes the common-source configuration is the simplest to drive. Because of the high input impedance of VMOS it can be driven directly from many logic families. When driving from a CMOS gate as shown in Figure 3, rise and fall times of about 60 nsec can be expected due to the limited source and sink currents available from the CMOS gate.[2] If faster rise and fall times are required there are several ways to obtain them. One easy way is if there are extra gates in the package that is driving the VMOS simply put the extra gates in parallel with the gate already being used. The additional current available will cut down the rise and fall times. If no extra gates are available an emitter-follower buffer can be used as shown in Figure 4. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as emitter-followers there will still be no storage time to worry about and the frequency limit will be determined by either the CMOS gate or the f_T of the bipolars, whichever comes first.

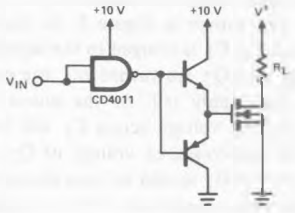
VMOS can also be driven directly from TTL gates. Because the output voltage of TTL is limited, the output current of the VMOS will be limited to some value less than its maximum rated current. The output current that can be expected can be determined from the transfer characteristic of the device being used. For example, if a TTL gate is driving VN46AF the minimum output current of the VMOS will be approximately 250 mA. This value was obtained by using the minimum output voltage of the TTL gate (3.2 V) for a high level output and referring to the transfer characteristic for the VNAZ which is the VMOS geometry used in the VN46AF. If more than 250 mA is required the output of a standard VMOS gate can be pulled up to the 5 V rail as shown in Figure 5. With a full 5 V on the gate the VN46AF will typically sink 600 mA.

For very high speeds a capacitive driver such as the MH0026 can be used as shown in Figure 6. With this drive configuration typical rise and fall times are less than 10 nsec.

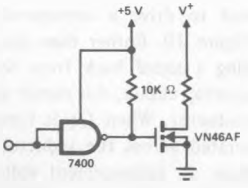
When operated in the common-drain mode VMOS is somewhat more difficult to drive than when in the common-source mode. Because of VMOS' high input impedance, though, it is considerably easier to drive common-drain than a bipolar would be when operated common collector. Common-drain circuits can be used when the load needs to be connected to ground, when an active pull-up and pull-down is required (totem pole circuit), or in bridge type circuits. For the purpose of this discussion all examples will be shown with totem pole circuits.



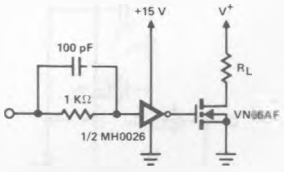
Driving VMOS with a CMOS Gate
Figure 3



An Emitter-Follower Circuit Will Decrease VMOS Rise and Fall Times
Figure 4

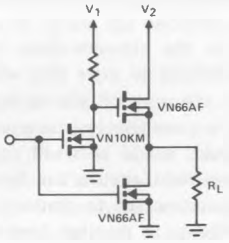


Pulling Up a TTL Output Will Increase the Sink Current of the VMOS
Figure 5



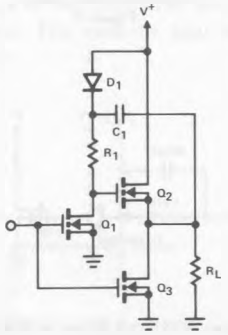
Using an MOS Clock Driver to Drive VMOS
Figure 6

The difficulty with common-drain circuits occurs because as the voltage across the load increases the enhancement voltage of the common-drain device decreases. Referring to Figure 7, as the voltage across R_L approaches V_2 the enhancement voltage for the upper VN66AF decreases. If V_1 is not greater than V_2 then the voltage across R_L can never reach V_2. For this reason whenever a common-drain circuit is used it is always necessary to have or to generate a voltage that is greater than the voltage which is desired to be impressed across the load. The amount the voltage has to be above the desired drain voltage is dependent upon the current the VMOS must source and can be determined from the transfer characteristic of the VMOS being used. If no supply voltage is available other than the one the load is to be pulled up to, one can be generated. This can be done very easily because of the very low drive current requirements of the VMOS.

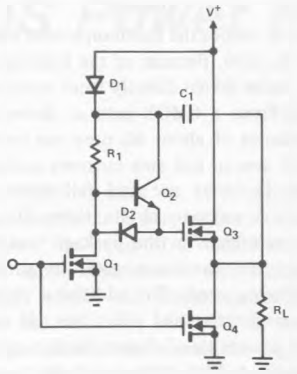


VMOS in Totem-Pole Configuration
Figure 7

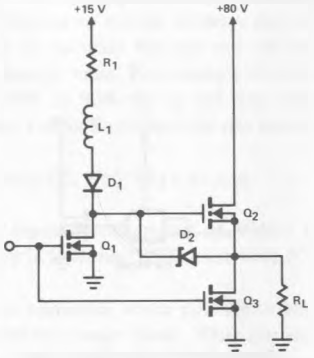
One way of generating the required gate voltage is the bootstrap circuit shown in Figure 8. In the circuit, when Q_1 and Q_3 are on, C_1 is charged to the supply rail through D_1. When Q_1 and Q_3 are turned off, the gate voltage on Q_2 goes to the supply rail. As the source of Q_2 begins to pull R_L up, the voltage across C_1 will be maintained, therefore, the gate-to-source voltage of Q_2 will be maintained. The size of C_1 should be large enough so that when it charges the gate capacitance of Q_2 a minimum voltage equal to the required enhancement voltage of Q_2 will be maintained across it. A good rule of thumb is to make C_1 equal to ten times the C_{iss} of the FET. Figure 9 shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit Q_2 acts as an emitter-follower to increase the peak gate current to Q_3. D_2 will be forward biased when Q_1 turns on and serves as a low impedance path to discharge the gate of Q_3.



VMOS Bootstrap Circuit
Figure 8



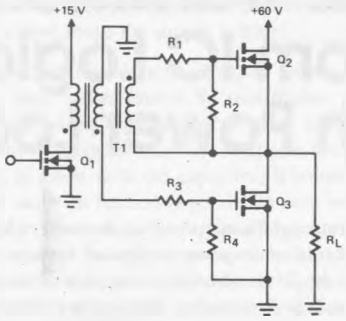
Bootstrap Circuit with Emitter-Follower for Improved Rise Times
Figure 9



Inductive Kickback Drive Circuit
Figure 10

Another method to drive a common-drain VMOS FET is shown in Figure 10. Rather than charging a capacitor and then feeding a signal back from the output as was done in the bootstrap circuit, this circuit stores the required charge in an inductor. When Q_1 is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain an enhancement voltage equal to the voltage of zener diode D_2 across the VMOS FET. Once the Q_2 has been fully turned on and the voltage on R_L is at the rail a negligible amount of energy is required to keep Q_2 on. Q_2 will remain on until Q_1 is turned on, or until the leakage currents of Q_1 and D_2 discharge the gate capacitance of Q_2.

Another method that can be used to drive a common-drain VMOS is transformer drive. A transformer drive circuit is shown in Figure 11. In this circuit the transformer is used in the flyback mode when turning on the upper FET. R_1 and R_3 are used to suppress ringing and R_2 and R_4 are used to assist with turn-off of the FETs. When driving with a transformer, care must be taken to design the transformer so that the secondary inductance in conjunction with the input capacitance of the FET does not create ringing of oscillation problems.



Transformer Drive Circuit for VMOS
Figure 11

SUMMARY

The very high input impedances of VMOS Power FETs greatly simplify the drive requirements as compared to bipolars. The input drive requirements for both common-source and common-drain configurations were discussed in detail. With common-source circuits the requirement that needs to be kept in mind is the rise and fall time required. With common-drain circuits a method of maintaining an adequate enhancement voltage must be considered in addition to required rise and fall time requirements.

REFERENCES

1. A. Evans, D. Hoffman, "Dynamic Input Characteristics of a VMOS Power Switch" AN79-3.

2. D. Hoffman, L. Schaeffer, "VMOS – A Breakthrough in Power MOSFET Technology" AN76-3.

Using VMOS Transistors to Interface from IC Logic to High Power Loads

Bill Roehr

VMOS transistors are an ideal element to interface power loads to integrated circuit logic. Although circuit design is simple, there are a few rules and precautions to observe in order to minimize power dissipation and to have reliable operation, which are not obvious at first glance.

Topics considered are (1) the nature of the load, (2) general driving requirements of VMOS, and (3) the output characteristics of the logic element.

LOAD CONSIDERATIONS

Freedom from second breakdown limitations makes driving highly inductive or capacitive loads a natural application for VMOS. Inductive loads include transformers, solenoids or relays. High current inrush loads such as incandescent lamps, pulse forming networks, and motors also are generally handled easily. Some attention must be given to the load characteristics, however.

In common with bipolar semiconductor devices, VMOS transistors can be damaged if their voltage ratings are exceeded. Although their avalanche energy capability is much better than that of bipolar transistors, it is not good design practice to have the VMOS absorb inductive energy unless the part is rated for this type of service. The spikes generated from inductive loads may have tremendous energy content and usually some means of limiting their amplitude must be provided.

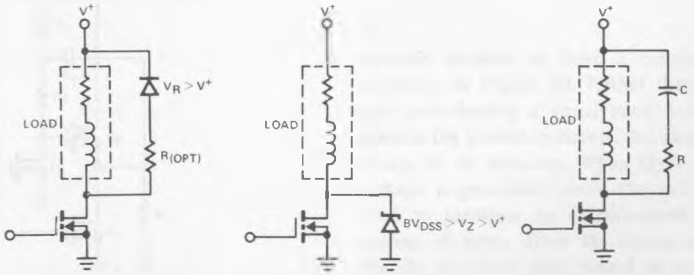
In addition the transient power generated during the turn-on and turn-off intervals must be determined in order to check for excessive channel temperatures. Highly inductive loads may generate significant power on turn-off, whereas capacitive-like loads cause power surges on turn-on. The power waveform should be obtained, a suitable rectangular model derived, and peak junction temperature computed using techniques discussed elsewhere[1,2]. This calculation is especially important for incandescent lamp and motor loads as their current surges last from tens to thousands of milliseconds which causes a significant surge in the temperature of the VMOS power driver.

Inductive Loads

Usually with inductive loads the peak voltage spike should be limited to a value below the breakdown rating of the transistor. Three techniques are commonly employed: free-wheeling diodes, peak clipping and snubbing. Typical circuits are shown in Figure 1.

The spikes caused by most electromechanical inductive loads such as solenoids or relays are effectively handled by the free-wheeling diode in part (a). The low impedance of the diode usually causes the current to have a long decay time, however, which may be intolerable in some applications. Speed may be traded for overshoot voltage, by using a resistance, R, in series with the diode[3].

The free-wheeling diode may be an inexpensive rectifier such as the 1N4002. However, junction rectifiers do exhibit a turn-on transient which may allow excessive overshoot if the VMOS transistor is being driven off rapidly. For high speed switching, a Schottky or low voltage ion-implant rectifier is required; the ordinary fast recovery rectifier does not have a fast turn-on time.



(a) Free Wheeling Diode Clipper (b) Zener Diode Clipper (c) R-C Snubbing

Methods of Limiting Inductive Spikes
Figure 1

Often the safest and least expensive limiting technique is to use a zener diode as shown in part (b). The zener responds in picoseconds and can protect the VMOS from supply transients as well as the inductive spike; consequently, zener limiting is particularly attractive on raw power buses. In a manner similar to using a resistor in series with a free-wheeling diode, faster decay of load current is achieved by clipping at a level above the supply voltage.

The R-C snubber is commonly used in power conversion circuits to limit spikes caused by transformer leakage inductance and wiring inductance. It also reduces power dissipation by shaping the load line to appear more resistive. Resistor R, in series with the capacitor, is required to limit the current surge on turn-on (a good idea even when VMOS is used) and to insure that the circuit is adequately damped. Since the circuit is basically a resonant tank, it will exhibit a damped oscillation unless the circuit Q is 1/2 or less. Values are usually empirically determined. The peak voltage across the network will not exceed that calculated using the energy relationship: $1/2\ LI^2 = 1/2\ CV^2$. Solving for the voltage, it is found that

$$V = I\sqrt{L/C}$$

The resonant frequency can be calculated from the usual relationship and R selected so that $Q \simeq 1/2$ by using

$$R = 4\pi fL$$

The equations and experience indicate that larger values of C lower the peak voltage and resonant frequency and consequently the resistor R also must be reduced. An optimum value exists for a given L-C combination which results in minimum overshoot. Another consideration is to minimize the power dissipation in the transistor; various techniques are discussed elsewhere[4,5].

Capacitive and High Inrush Loads

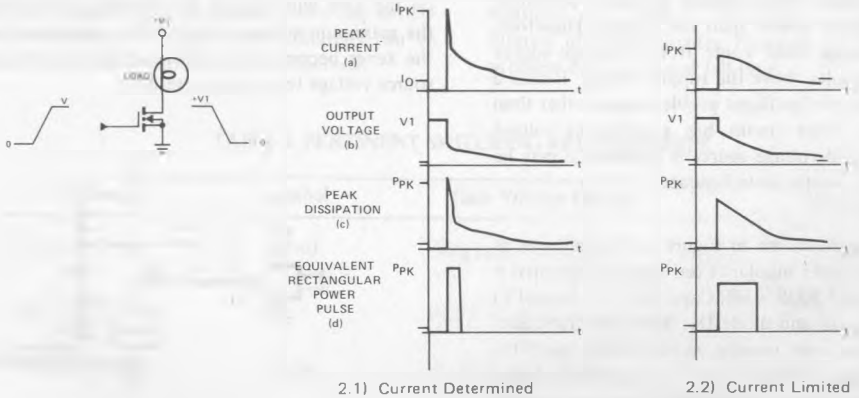
Usually no auxiliary circuitry is required with capacitive-like loads. Although VMOS has no failure mode akin to secondary breakdown, it is necessary to observe the safe area curves of the VMOS transistor in order to avoid excessive temperature excursion during current inrush. When inrush power is excessive, usually increasing the gate drive will reduce it and may hold it within bounds. A lamp circuit and waveforms are shown in Figure 2.

Figure 2.1 illustrates the typical transient current, voltage and transistor dissipation of an incandescent lamp load being driven by a VMOS circuit that is not drive limited – it can supply all the current that the load demands while maintaining operation in the ohmic region. Under these conditions, the output voltage quickly swings from its off state (V_1) to on state in a time dictated by the transient gate drive current and the VMOS capacitances. The peak current is a function of the lamp's cold resistance and decays quasi-exponentially as the lamp filament heats and resistance increases.

The transistor dissipation waveform is similar to the power waveform of Figure 2.1(c); this can be equated to the rectangular power pulse of 2.1(d) to simplify peak and average power calculations.

The case where the power transistor is drive limited (where it cannot supply all of the peak current that the load demands) usually – but not always – results in greater transistor dissipation. This is illustrated in the transient waveforms of Figure 2.2 where the peak current is much less than in the previous example, but also where transistor operation does not enter the ohmic region initially during the switching transition. The resulting power dissipation pulse is greater and may be destructive.

VMOS transistors make ideal drivers for incandescent lamps because they can handle high current surges without failure caused by secondary breakdown. Lamp drivers may need to handle two types of surges, cold resistance inrush and flashover.



2.1) Current Determined by Load

2.2) Current Limited by Gate Drive

Waveforms When Driving an Incandescent Lamp, High Inrush Loads Develop Similar Waveforms
Figure 2

Cold resistance inrush occurs on all lamps during turn-on; the peak is between 12 and 18 times the steady state current. Furthermore, the inrush current may be from 2 to 5 times rated current 5 milliseconds after power application. The inrush depends somewhat upon the lamp's design and the cold temperature of the bulb, which in turn is dependent upon the lamp's operating duty cycle and ambient temperature. Since the turn-on surge is a repetitive transient, for maximum VMOS reliability, it is usually desirable to have sufficient gate drive to place the operating point in the ohmic region during the surge in order to minimize VMOS power dissipation.

The flashover surge occurs during failure of a gas-filled lamp. (All lamps over 60 watts designed for 120 or higher voltage lines contain some gas for improved efficiency and life). As the filament burns out, an arc is developed causing an extremely high surge on the order of 80 to 200 amperes with a baseline of 2 to 4 milliseconds. Coping with this surge is a real problem for the circuit designer when bipolar devices, such as junction transistors or thyristors, are used. If a device rated adequately for the steady state and inrush current is used, the flashover surge will cause failure. If a device rated to handle the flashover is used, cost is usually out of bounds because the device ratings far exceed those required for normal use. Semiconductor fuses can be used, but these are quite expensive. With VMOS power devices, the flashover surge will not cause failure even though the junction temperature may momentarily exceed its rating.

Driving Grounded Loads

In many cases, the load is connected to ground and cannot be arranged as shown in Figures 1 and 2. Driving a grounded load forces the VMOS to be used in a source follower circuit. The difficulty with a follower is that, to keep the VMOS in the ohmic region with a large drain current flow, the gate must be about 10 volts above the source potential, which is only slightly lower than the supply. Therefore, the gate drive voltage must come from a voltage source which is about 10 volts above the supply voltage. If such a voltage is available, no significant problem exists other than insuring that the driver circuit has a sufficient voltage rating. When no fixed voltage source is available, it may be generated using the bootstrap technique.

A bootstrap circuit is shown in Figure 3. Operation is as follows: when the driver bipolar is on, the gate potential is near ground and the VMOS is off. Capacitor C is charged to V_{DD} through the load and diode D_1. When the driver goes off, the gate voltage rises, turning on the VMOS transistor which raises the source potential. If C is many times larger than the input capacitance of the VMOS, it acts as a voltage source in series with the VMOS source terminal potential, thereby providing a gate-source voltage close in value to V_{DD}. The capacitor C will lose charge with time through the reverse resistance of diode D_1, so that it becomes impractically large if the load must be held on more than a few seconds, unless a strobing technique is used as discussed in the following paragraph. However, many loads, such as hammer drivers in high speed printers, are actuated for under a millisecond so that capacitors in the range of 0.1 μF are adequate. In cases when the load is a solenoid, it may be permissible for the VMOS to come out of the ohmic region as a result of a partial loss of gate drive after the solenoid has pulled in, because the hold-in current is very low. However, the power dissipation of the VMOS may increase significantly unless the drop in gate drive reduces drain current to a rather low value.

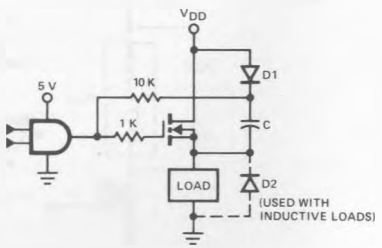
When the load must remain actuated at full power for a long period of time, a pulsed signal may be applied to the drive circuit instead of a DC level. When load current is to flow, the driver is off, except for occasional brief on periods during which the VMOS source voltage drops to ground allowing C to recharge to V_{DD}. The source for this strobe signal could be a system clock signal or the AC line. The higher the pulse repetition frequency, the smaller C may become, but C should usually be at least ten times the C_{iss} of the VMOS device to avoid transferring more than 10% of the charge on C to the VMOS gate during turn-on.

GENERAL DRIVING CONSIDERATIONS

Regardless of the type of logic or network used to drive a VMOS transistor, consideration must be given to VMOS properties such as:

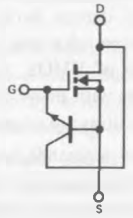
1. The input protection zener diode
2. The high frequency response
3. The capacitive input impedance

The input protection zener diode integral with some devices places restrictions on the drive levels. The positive voltage on the gate with respect to the source should not exceed the maximum voltage rating of the zener diode nor should the zener become forward biased by allowing the gate-to-source voltage to become negative.



Driving Loads Connected to Ground by Using Bootstrapping
Figure 3

The reasons for these restrictions are evident from the circuit of Figure 4 where it is seen that the zener is actually the base-emitter junction of a bipolar transistor whose collector is connected to the drain. Consequently, the zener exhibits a negative resistance characteristic similar to the BV_{CEO} of a transistor. Above a few hundred micro-amperes, the voltage may switch from, for example, 20 volts to 8 volts. The lower voltage will limit the amount of current available from the VMOS transistor and excessive dissipation in the zener and drive circuitry may occur.



A Parasitic npn Transistor in Zener Protected MOSFETS
Figure 4

If the drive circuit can cause a negative gate-source voltage – a common situation with a source follower driving a capacitive load – the bipolar becomes turned on in the forward direction causing a flow of current from the drain terminal to the gate terminal. Damage to the device from excessive current may result if the impedance of the current loop is very low, but this is usually not a problem unless the drain-source voltage is high enough to cause the bipolar to operate in a $BV_{CEO(SUS)}$ mode. Since the BV_{DSS} rating of the FET is essentially the BV_{CBO} rating of the bipolar, $BV_{CEO(SUS)}$ is approximately one half of BV_{DSS}. Consequently, a second breakdown failure of the zener bipolar may occur when the drain-source terminal voltage exceeds one half of BV_{DSS}. If negative gate voltages are unavoidable a VMOS part that does not have an input zener diode should be used.

The carrier transit time through the channel is under 1 ns for most VMOS structures resulting in cut-off frequencies on the order of a gigahertz. Consequently, very fast switching is readily achieved, but parasitic oscillations can be troublesome if certain precautions are not observed.

Usually oscillations are prevented by observing one or more of the following guidelines:

1. Keep lead and trace lengths short.
2. Place ferrite beads on the gate lead close to the gate terminal or use a resistor of 10 to 1000 ohms in series with the gate.
3. Avoid a layout which may couple output signal to the input.
4. Surround the VMOS transistor with a ground plane and shield output from input.

Since VMOS gate input resistance is essentially infinite, many VMOS transistors can be driven from a CMOS or TTL output. However the input impedance of VMOS is capacitive and the drain current essentially follows the voltage on the gate. Although switching speed, per se, is not important when driving a lamp or electromechanical load, the limited transient current available from the logic element may result in switching slow enough to cause significant transient power dissipation, particularly when a number of VMOS stages are being driven in parallel. Accordingly, a transient analysis of some sort is usually required.

A fairly simple, yet quite accurate analysis is to use a charge control approach as described by Evans and Hoffman[6]. For any particular time interval,

$$\Delta t = \frac{(\Delta V_{GS})\,(C_{in})}{I_G}$$

where

ΔV_{GS} is the gate-source voltage change

C_{in} is the effective input (gate-source) capacitance

I_G is the average gate current during switching

(all values must be determined for the time interval of interest).

Table I shows the appropriate quantities to use in the equation. For completeness, turn-on and turn-off delay relations are included, but these intervals are rarely of interest in power circuits. However, dissipation may be a problem during rise and fall time.

4

TABLE I. PERTINENT SWITCHING RELATIONSHIPS

Interval	Symbol	Gate Voltage Change	Capacitance
Turn-On Delay	$t_{d(on)}$	$V_{G(TH)} - V_{G(off)}$	C_{iss}
Rise Time	t_r	$V_{G\,@\,I_{D1(on)}} - V_{G(TH)}$	$C_{iss} + \frac{\Delta V_{DS}}{\Delta V_{GS}} C_{rss}$
Turn-Off Delay	$t_{d(off)}$	$V_{G(on)} - V_{G\,@\,I_{D2(on)}}$	C_{iss}
Fall Time	t_f	$V_{G\,@\,I_{D2(on)}} - V_{G(TH)}$	$C_{iss} + \frac{\Delta V_{DS}}{\Delta V_{GS}} C_{rss}$

Capacitance values used are the average values as V_G varies over the ranges shown for the time interval of interest. Appropriate V_{DS} values must also be used to determine the capacitance. Key V_{GS} points are:

$V_{G(off)}$	=	Off state gate voltage prior to turn-on
$V_{G(TH)}$	=	Threshold gate voltage
$V_G @ I_{D1(on)}$	=	V_G corresponding to the peak value of drain current for capacitive or resistive loads or the value of drain current when the drain voltage enters the ohmic region for inductive loads.
$V_{G(on)}$	=	On-state gate voltage prior to turn-off
$V_G @ I_{D2(on)}$	=	V_G corresponding to the value of drain current flowing prior to turn-off.

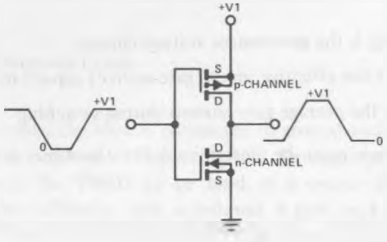
Driving From CMOS Logic

The widely used CMOS logic elements are ideal for direct coupling to VMOS power transistors because CMOS can operate with supplies up to 15 volts, a level which provides ample drive for VMOS. Since VMOS switching speed and transient load handling capability is related to the output impedance of the drive source, a brief examination of the CMOS circuit follows.

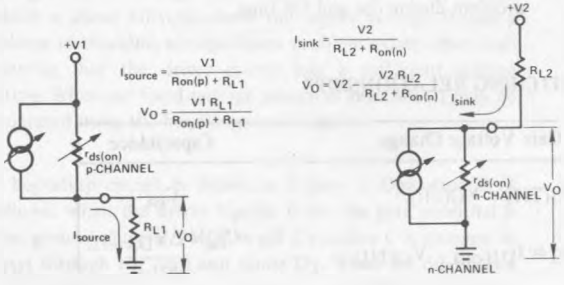
All CMOS circuits usually have an output configuration as shown by the inverter of Figure 5. The inverter consists of a p-channel MOSFET connected in series with an n-channel FET (drain-to-drain) with the gates tied together and driven from a common signal – hence, the name CMOS (complementary MOS). When the input signal goes positive (+V), the p-channel FET is essentially off and conducts only I_{DSS} (picoamperes). The n-channel unit is forward biased but since only I_{DSS} is available from the p-channel, V_{DS} is very low. Conversely, when the input goes low (zero), the p-channel device is turned full on, the n-channel device is off, and the output will be very near +V. Since the current (without a load) is extremely small, the inverter dissipates almost no power in either stable state; the only dissipated power of consequence occurs during the switching transitions as capacitances are charged. Due to the extremely high input impedance of VMOS, the CMOS gate has the capability of interfacing with many VMOS power transistors when only static conditions are considered.

The DC resistance between drain and source when the device is turned on is generally labeled "ON resistance, R_{ON}" or $r_{DS(on)}$. However the CMOS gate has a limited output capability determined by the gain of the n and p-channel devices. Equivalent circuits of the CMOS output are shown in Figure 6.

A look at the characteristic curves of CMOS transistors will provide insight into the dynamic driving source impedance presented to the VMOS gate. Figure 7 shows the characteristic curves of n-channel and p-channel enhancement mode transistors typically found in CMOS circuits. Referring to the curve of V_{GS} = 15 V (gate-to-source voltage) for the n-channel transistor, note that for a constant drive voltage

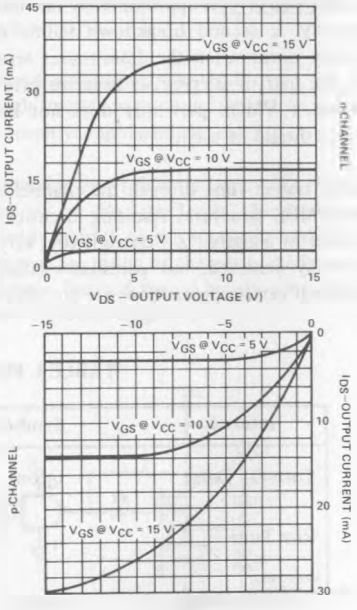


CMOS Inverter
Figure 5



(a) Sourcing Current (b) Sinking Current

CMOS Source/Sink Capabilities
Figure 6

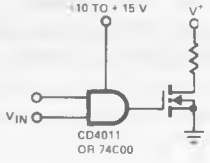


Transistor Output Characteristics
of a CMOS Inverter
Figure 7

V_{GS}, the transistor behaves like a current source for drain-to-source voltages greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor – on the order of a volt or two). For a V_{DS} below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Similar curves are obtained for lower values of V_{GS} except that the magnitude of the current is significantly smaller and, in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The p-channel transistor exhibits similar, but complemented, characteristics with less gain and a more gradual transition from a current source to a resistor.

When driving a capacitive load the initial voltage change across the load will be a ramp due to the current source characteristic, followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. For fastest turn-on and therefore lower dissipation in the VMOS transistor, the peak output current should be achieved while the CMOS inverter is operating in the constant current mode. To accomplish this, the maximum current from the VMOS is that which corresponds to a V_{GS} that is a few volts below the CMOS supply voltage, V_1. From Figure 7, note that operating the CMOS driver at higher V_{CC} will have a profound effect on VMOS switching speed because the CMOS output current increases roughly as the square of V_{GS} and the voltage where rounding occurs has been pushed to a higher level.

Therefore, the optimum interface from CMOS to VMOS is shown in Figure 8. In this configuration, the turn-on current is supplied from the p-channel FET which has the poorest characteristics of the CMOS pair, but when operating at 15 volts, serious rounding of the VMOS gate waveform can usually be made to occur at a level above that required to handle the load current. The turn-off current is supplied from the n-channel FET; it maintains good drive capability down to the threshold voltage of the VMOS gate which minimizes tailing of the VMOS drain current.

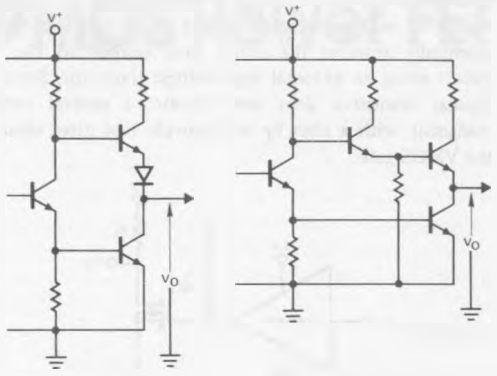


Driving VMOS with a CMOS Gate
Figure 8

Driving from TTL Logic

The lower logic levels used in TTL make it much less satisfactory than CMOS for direct coupling to VMOS; however, TTL can be directly coupled to VMOS when lower output currents are required, or some additional circuitry can be added to make the match more universally applicable. The coupling problems are readily appreciated by analyzing the output circuit of TTL.

Figure 9 shows the totem pole output circuit configurations commonly used in TTL. When the driver is off, the output is high, however, the output is slightly over two diode drops below the supply voltage for either configuration. Since the nominal supply is 5 volts, the output is approximately 3.5 volts, a level too low to fully utilize a VMOS transistor.

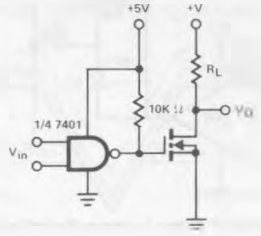


(a) Medium-Speed TTL Output Configuration (5400/7400 Families)

(b) High-Speed TTL Output Configuration

Basic TTL Output Configurations
Figure 9

When the driver is on, the lower output transistor is also on; the output is low, on the order of a few tenths of a volt. The low level is satisfactory to ensure VMOS cutoff, in most cases, but the high level needs to be raised.

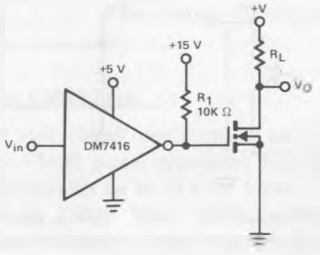


Driving the VMOS With Standard TTL
Figure 10

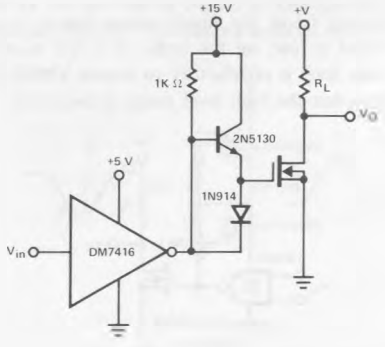
A method of boosting the TTL output level is shown in Figure 10. The external resistor allows the full supply voltage to be applied to the VMOS gate, but in doing so, the TTL output transistor becomes cut-off as the level increases above 3.5 volts. Consequently the high drive capability and low output impedance of TTL is not effectively utilized, as the drive to the final value of gate voltage must come solely from the pull-up resistor. To maintain a reasonably fast rise time, it is necessary to limit the peak drain current to the value obtained for a particular VMOS type when the gate voltage is at 3.5 volts: the additional 1.5 volts is used as overdrive to place the operating point in the ohmic region.

4

Full utilization of VMOS transistors is achieved with open collector TTL as shown in Figure 11. The open collector circuits do not have the top transistors and the lower transistors are designed to be used with supplies up to 15 volts. The VMOS rise time is now mainly dependent upon the external resistor used. For fast rise time, the lower resistance values required may cause objectionable dissipation when the TTL output is low; use of the circuit of Figure 12 will provide high speed and low dissipation. It essentially restores the totem pole output to the TTL circuit using an external high voltage transistor. Since the bipolar transistor does not saturate, a general purpose transistor with a high f_T will provide fast drive signal to the VMOS gate.



Open Collector TTL is Used to Provide Greater Enhancement Voltage
Figure 11



A "Totem Pole" Driver Increases Switching Speed and Reduces Dissipation
Figure 12

SUMMARY

VMOS power FETs can easily interface power loads to integrated circuit logic. Spikes from inductive loads usually must be limited to a level below the breakdown voltage of the VMOS transistor. High inrush, capacitive-like loads usually require high gate drive to place operation in the ohmic region during inrush.

To avoid deleterious operation and insure fast switching, consideration must be given to the VMOS input protection zener diode – if present – and capacitive input impedance. Direct coupling to CMOS is usually very satisfactory if the IC supply is 10 to 15 volts. With T^2L, open collector elements are usually required to obtain sufficient gate voltage for the VMOS.

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Applications of the VN10KM VMOS Power FET

Bill Roehr

The VN10KM is the industries' lowest cost VMOS FET available. This low cost allows the designer to utilize the benefits of VMOS transistors in several cost-sensitive applications.

As an aid in stimulating use of the VN10KM, this application note first describes its characteristics in particular and then the general characteristics of VMOS devices which make them such ideal active elements. After discussing load and driving considerations, several circuit applications which are particularly suited to the VN10KM are then described.

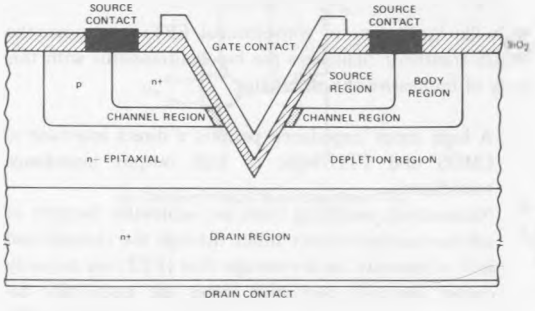
Features of the VN10KM Transistor

The chip is housed in a plastic TO-237 package which is constructed similarly to a TO-92 but has a small metal tab protruding from the top. The tab increases power dissipation at room temperature from the usual 300-600 mW of the TO-92 to 1 watt.

Although the VN10KM package is small, the chip inside can handle big jobs. Capable of producing 1 ampere peak current and blocking 60 volts, the transistor has a maximum $r_{ds(on)}$ of 5Ω and a minimum g_{fs} of 0.1 mho, in addition to the usual VMOS characteristics.

VMOS Technology and Characteristics

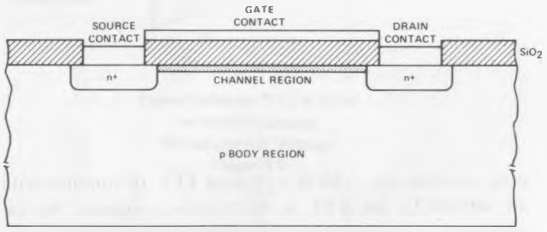
VMOS technology has been described in detail in the literature[1,2,3]; however, for the convenience of the reader unfamiliar with VMOS, a summary follows. A familiarity with VMOS construction aids in understanding the fundamental characteristics of VMOS Transistors. Figure 1 shows cross sections of a VMOS n-channel FET. In common with all MOSFETs the FET is built into a parasitic bipolar transistor which is electrically in parallel with the FET. The V groove cut into the structure forms the MOSFET gate. To keep the bipolar inactive, its base is shorted to its emitter. This also stabilizes the threshold voltage of the FET, since the body region is not electrically floating.



V-Groove VMOS Transistor Cross Section
Figure 1

Referring to Figure 1, to cause current to flow in an n-channel device, the gate is made positive with respect to the source and body causing electrons to be attracted into the p-region surface under the gate. Above a certain voltage (the threshold voltage) the p-type silicon surface inverts, forming an n-type channel, thereby creating a low resistance path from source to drain. The p-type body is made short to provide high gain, therefore it cannot support significant voltage at the drain without punch-through occurring. The n-type epitaxial layer is used to provide sufficient depletion region for the drain-source voltage.

The conventional MOSFET is constructed horizontally as shown in Figure 2. The n+ source and drain regions are simultaneously diffused into the p-type substrate. The channel region occurs on the top surface of the substrate. Even though this structure is admirably suited to complex digital integrated circuit fabrication, a number of undesirable attributes occur which make it unattractive for linear applications and rule it out of power applications. The length of the channel is determined by the tolerances of the masks used to define the source and drain patterns. Since these are not controllable to a fine degree, the channels must be relatively long, resulting in fairly low gain per unit area, a high on-state resistance ($r_{ds(on)}$); and a square law transfer curve. In contrast, the V-groove VMOS channel is determined by diffusion so that a short channel is achieved (shorter by a factor of 3 or so) which increases the gain, reduces $r_{ds(on)}$, and provides a linear transfer curve.



Cross Section of a Conventional n-Channel MOSFET Showing Channel Region Under the Top Surface
Figure 2

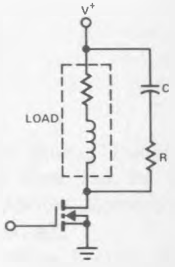
With the limitations of conventional FETs overcome, the VMOS transistor challenges the bipolar transistor with this array of impressive characteristics:

1. A high input impedance permits a direct interface to CMOS and TTL logic or high output impedance transducers.
2. Nanosecond switching times are achievable because of sub-nanosecond-transit times through the channel and lack of minority carrier storage time (FETs are majority carrier devices). Switching times are essentially determined by the speed with which the input capacitance is charged.
3. Power handling capability is determined basically by the package thermal properties. Except at low currents, the temperature coefficient of gain is negative: coupled with lack of a mechanism to cause current concentrations, second breakdown is unknown in FETs unless their voltage ratings are exceeded.
4. A nearly linear transfer curve results in low distortion in audio amplifiers and low splatter in RF amplifiers. Furthermore, the curvature present at low current levels approximates a square law characteristic which results in generation of less troublesome even harmonics rather than odd harmonics.

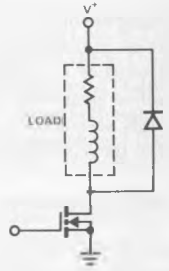
Load Considerations

Freedom from second breakdown limitations makes driving highly inductive or capacitive loads a natural application for VMOS. Loads of this nature include ultrasonic transducers, solenoids, or relays. High inrush loads such as incandescent lamps, pulse forming networks, and motors also pose no problems.

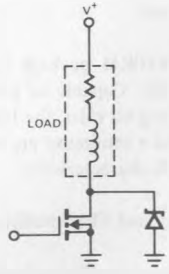
Care should be taken with inductive loads, however, to limit the peak voltage spike to a value below the breakdown rating of the transistor. Three techniques are commonly employed: R-C snubbing, free-wheeling diodes, and peak clipping. Typical circuits are shown in Figure 3.



(a) R-C Snubbing



(b) Free-Wheeling Diode Clipper



(c) Zener Diode Clipper

Methods of Limiting Inductive Spikes
Figure 3

The R-C snubber in part (a) can be satisfactory if the constants are properly chosen. R may be omitted if not required to keep the circuit adequately damped to avoid excessive ringing. In some cases, considerable overshoot is acceptable as long as the peaks are below the 60 volt rating of the VN10KM.

The free-wheeling diode of part (b) may use an inexpensive rectifier such as the 1N4002. However, junction rectifiers do exhibit a turn-on transient which may allow excessive overshoot if the VMOS transistor is being driven off rapidly. For high speed switching, a Schottky or low voltage ion-implant rectifier is required; the ordinary fast recovery rectifier does not have a fast turn-on time.

Perhaps the safest and least expensive limiting technique is to use a zener diode as shown in part (c). The zener responds in picoseconds and can protect the VMOS from supply transients as well as the inductive spike.

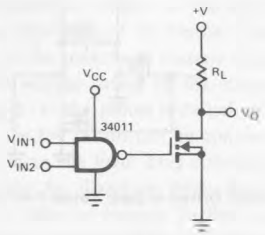
Resistive and capacitive loads usually require no auxiliary circuitry. The VMOS transistor will limit the peak current to a value determined by the gate drive voltage; furthermore there is no failure mode akin to secondary breakdown. It is well, however, to observe the Safe Area curve of the VMOS transistor in order to avoid excessive temperature excursion during current inrush.

Interfacing VMOS to Integrated Circuit Logic

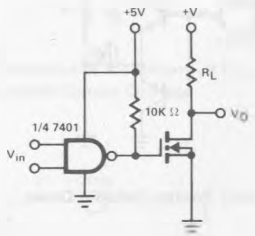
The high input impedance and high speed of the VN10KM make it ideal in many switching applications. It will interface to any driver capable of a 5 V swing or more to nearly any load requiring under a half-amp of current, while standing off up to 60 volts in the off state. When very high speed is not required, VMOS may be directly coupled to CMOS or TTL logic as shown in Figure 4.

A typical CMOS circuit is shown in part (a). A logic low to the input of the 34011 turns the VMOS transistor on and a logic high turns the VMOS off. A V_{CC} of 10 volts is required in order to assure handling 0.5 amp; the turn-on and turn-off times are about 60 ns under these conditions.

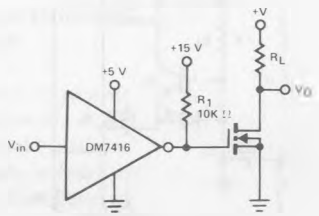
The VN10KM will also interface with TTL. As shown in part (b) standard TTL requires a resistor to pull its output to 5 volts; the guaranteed drain current of the VN10KM with 5 V enhancement is 250 mA. If more current is needed, open collector TTL can be used with a 10 to 15 V supply as shown in part (c). Turn-on time will depend on the value of R_1 since it provides the current to charge the FET input capacitance. If a fast turn-on time is needed, R_1 must be small and excessive power will be dissipated when the VMOS is off. Techniques for increasing the switching speed of VMOS transistors are discussed in the next section.



(a) A CMOS Gate Driving VMOS



(b) Driving VMOS With Standard TTL



(c) Using Open Collector TTL to Provide Greater Enhancement

Direct Coupling of VMOS to IC Logic
Figure 4

High Speed Drive Techniques

In digital or high frequency applications of VMOS transistors, it is often necessary to have fast switching performance. VMOS speed is essentially determined by the rate at which the input capacitance can be charged, therefore a scheme to provide a low driving source impedance is needed. Several circuits to accomplish this are shown in Figure 5.

Circuit (a) shows an emitter-follower buffer between the VMOS and the CMOS gate. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as non-saturated emitter-followers, storage time is not present and the frequency limit will be determined by either the CMOS gate or the f_T of the bipolars, whichever is lower.

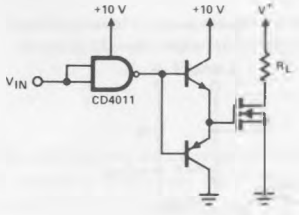
Another technique is to use a clock driver IC such as the DS0026 as shown in circuit (b). With this circuit, turn-on and turn-off times of 30 ns are achieved.

When a high speed pulse into a capacitive load is required, a totem pole arrangement of the VMOS devices is suggested. However, in order to drive the upper VMOS device into its ohmic region, the drive voltage must exceed the collector supply voltage by several volts. In terms of the notations in Figure 5(c), $V_1 > V_2 + V_{GS}$ where V_{GS} is determined by the load current and the characteristics of the VMOS transistor being used. In situations where V_2 is the highest supply in the system, a bootstrap technique can be used to generate the required gate drive voltage. It is relatively easy to do because only a short pulse of drive current is required to charge the VMOS input capacitance.

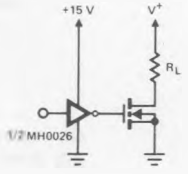
The circuit of Figure 5(d) uses a capacitor storage bootstrapping technique. When Q_1 and Q_3 are on, C_1 is charged to the supply rail through D_1. When Q_1 and Q_3 are turned off, the gate voltage on Q_2 goes to the supply rail. As the source of Q_2 begins to pull R_L up, the voltage across C_1 will be maintained, therefore, the gate-to-source voltage of Q_2 will be maintained. The size of C_1 should be large enough so that when it charges the gate capacitance of Q_2 a minimum voltage equal to the required enhancement voltage of Q_2 will be maintained across it. A good rule of thumb is to make C_1 equal to ten times the C_{iss} of the FET.

Figure 5(e) shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit Q_2 acts as an emitter-follower to increase the peak gate current to Q_3. D_2 will be forward biased when Q_1 turns on and serves as a low impedance path to discharge the gate of Q_3.

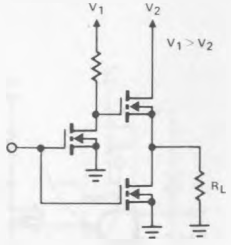
Another method to drive a common-drain VMOS FET is shown in Figure 5(f). Rather than charging a capacitor and



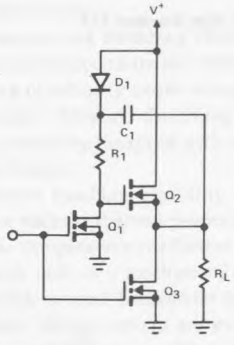
(a) Complementary Emitter-Follower Driver



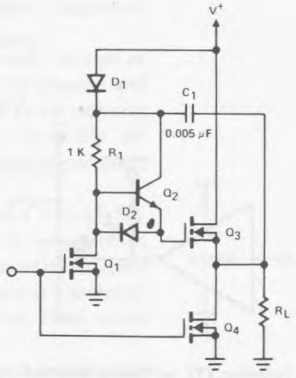
(b) Clock Driver



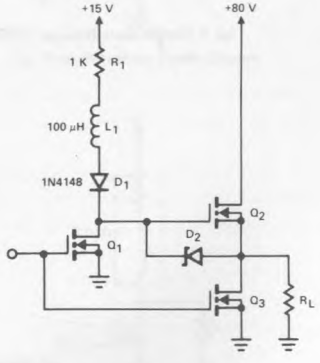
(c) VMOS Driven in Basic Totem-Pole Configuration



(d) VMOS Driver With Bootstrap Circuit for Totem-Pole Outputs



(e) Bootstrap Circuit with Emitter-Follower for Improved Rise Times



(f) Inductive Kickback Drive Circuit

High Speed Drive Schemes
Figure 5

then feeding a signal back from the output as was done in the capacitor bootstrap circuit, this circuit stores the required energy in an inductor. When Q_1 is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain enhancement voltage equal to the voltage of zener diode D_2 across the VMOS FET. Once Q_2 has been fully turned on and the voltage on R_L is at the rail a negligible amount of energy is required to keep Q_2 on. Q_2 will remain on until Q_1 is turned on, or until the leakage currents of Q_1 and D_2 discharge the gate capacitance of Q_2. The values shown permit the VN10KM to drive load currents up to 0.5A at a PRF as high as 10 MCS.

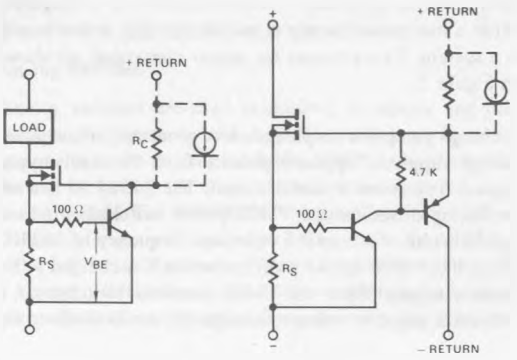
Current Regulators

Current regulators find wide use as high impedance loads and current sources for differential amplifiers, zener diode references, and capacitors in timing circuits. FETs are attractive for use in current regulators because of their high output impedance and relative insensitivity to temperature variations. Use of VMOS devices permits higher current outputs to be achieved than possible with the more widely used junction FETs; however, some provision must be made to forward gate bias the VMOS transistor. The various circuits in Figure 6 show techniques of achieving current sources of different degrees of accuracy at the expense of increasing circuit complexity.

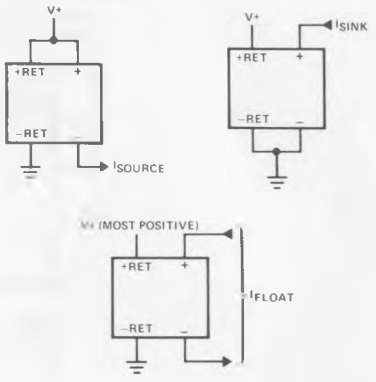
The simple circuit of part (a) uses the base-emitter diode of a bipolar transistor as a reference voltage. The feedback action of the connection is such that the bipolar collector voltage – which is the VMOS gate voltage – forces the VMOS device to draw a current of approximately 0.65 volt/R_S. The collector resistor of the npn simply provides a bias for linear operation of the bipolar. This circuit is good from 30 mA to the maximum current rating of the VMOS transistor. The voltage rating of the circuit is that of the VMOS transistor. If the minus terminal of the circuit is to be grounded, the (+) return can be connected to a positive supply, rather than the load. This connection improves the current accuracy by diverting away the variable current flowing in the collector resistor, further improves the output impedance by preventing base-emitter voltage variation due to a variable collector current, and reduces the knee voltage required to obtain the required output current. Use of a current diode of the J500 family in place of the collector resistor provides superior performance, particularly when the return must be connected to the load.

The circuit of part (b) utilizes a pnp transistor to increase loop gain and thereby improve the regulation of the collector current of the npn device. Both (+) and (–) returns are available for connection to a fixed supply in order to improve the accuracy of the output current. Techniques of using the returns for positive or negative current sources as well as a floating source are shown in part (c).

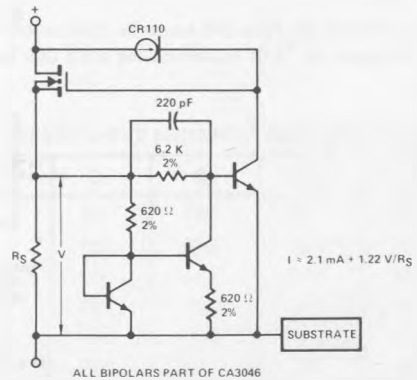
The last circuit of part (d) uses a band gap reference instead of a base-emitter junction for better temperature stability. It performs well as a two-terminal regulator without the need of returns.



(a) Simple Current Source (b) Improved Current Source



(c) Connection of the Returns of Circuit b for More Accurate Output Currents



(d) Accurate and Temperature Stable Current Source

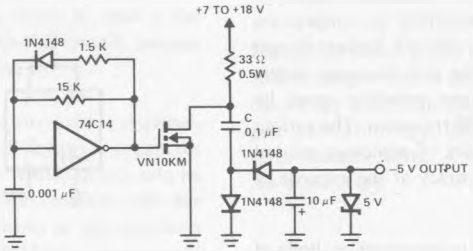
VMOS Current Regulator Schemes
Figure 6

Power Converters

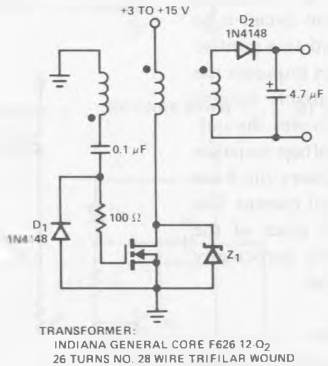
Often a low-power supply is needed for only a few boards in a system. Two schemes for power conversion are shown on Figure 7.

A charge pump is a simple means of generating a low-power voltage supply of opposite polarity from the main supply. Figure 7(a) shows a useful circuit. The 74C14 IC is a self oscillating driver for the VMOS power switch. It produces a pulse width of 6.5 μs at a repetition frequency of 100 KC. When the VMOS device is off, capacitor C is charged to the positive supply. When the VMOS transistor switches on, C delivers a negative voltage through the series diode to the output. The zener serves as a dissipative regulator. Because the VMOS transistor switches fast, operation at high frequencies allows the capacitors in the system to be small.

A low-power converter suitable for deriving a higher voltage from a main system rail in an on-board application is shown in Figure 7(b). It uses the core characteristics to determine frequency. With the transformer shown, operating frequency is 250 KC. Diode D_1 prevents negative spikes from occurring at the VMOS gate, the 100Ω resistor is a parasitic suppressor, and Z_1 serves as a dissipative voltage regulator for the output and also clips the drain voltage to a level below the rated VMOS breakdown voltage.



(a) Positive Input/Negative Output Charge Pump



(b) Self Oscillating Flyback Converter

High Frequency Power Converters for On-Board Use
Figure 7

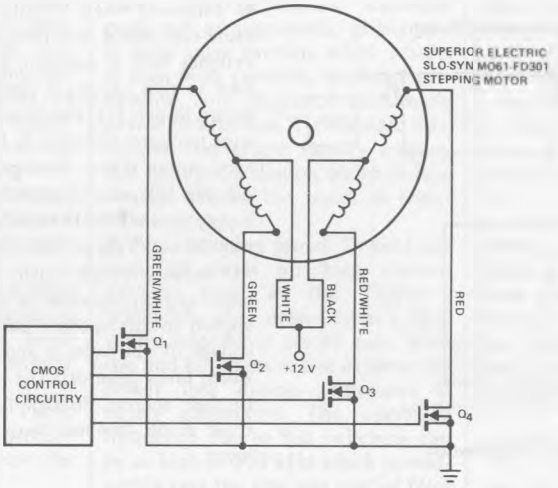
Stepping Motor Drive

Stepping motors find wide use in disk drives and machine control. VMOS transistors are ideal motor drivers because of their freedom from second breakdown. The circuit in Figure 8 shows how simple a motor drive becomes when using VMOS transistors. Note that snubbing networks are not used because load line shaping is not necessary with VMOS and the inductance of the motor is fairly low so that the inductive spike is small.

The VMOS gates are tied directly to the outputs of the CMOS control circuitry. The logic is arranged to sequence the motor in accordance with the needs of the application. As an example, the table of Figure 8 shows the switching sequence of the VMOS switches required to achieve clockwise rotation of the particular motor chosen.

Analog Switches

Analog switches are used extensively in sample and hold circuits, multiplexers, and A to D converters. From the many electronic devices available, VMOS transistors come closest to having the ideal characteristics required of an analog switch. The VN10KM, for example, offers a 5Ω on-state resistance, as compared to 30Ω or more for a JFET or a 0.1 volt or so offset voltage plus a few ohms resistance for a bipolar. VMOS devices also offer a nearly infinite resistance when off and low capacitance between the terminals.



Stepping Motor Driver
Figure 8

SLO-SYN Stepping Motors operate on phase-switched DC power. The motor shaft advances 200 steps per revolution (1.8° per step) when a four-step input sequence (full-step mode) is used and 400 steps per revolution (0.9° per step) when an eight-step input sequence (half-step mode) is used.

FOUR-STEP INPUT SEQUENCE† (FULL-STEP MODE)

STEP	Q_1	Q_2	Q_3	Q_4
1	ON	OFF	ON	OFF
2	ON	OFF	OFF	ON
3	OFF	ON	OFF	ON
4	OFF	ON	ON	OFF
1	ON	OFF	ON	OFF

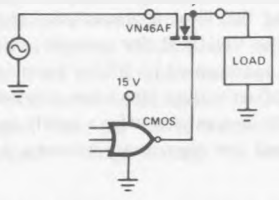
†Provides CW rotation as viewed from nameplate end of motor. To reverse direction of motor rotation perform switching steps in the following order: 1, 4, 3, 2, 1

EIGHT-STEP INPUT SEQUENCE† (HALF-STEP MODE)

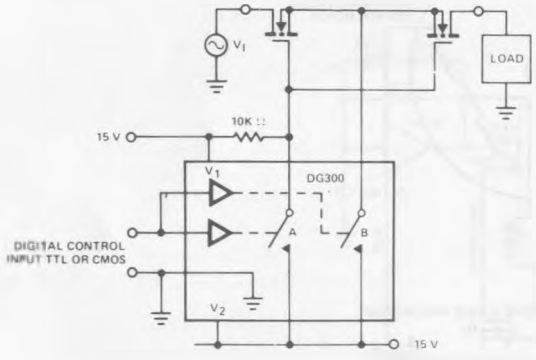
STEP	Q_1	Q_2	Q_3	Q_4
1	ON	OFF	ON	OFF
2	ON	OFF	OFF	OFF
3	ON	OFF	OFF	ON
4	OFF	OFF	OFF	ON
5	OFF	ON	OFF	ON
6	OFF	ON	OFF	OFF
7	OFF	ON	ON	OFF
8	OFF	OFF	ON	OFF
1	ON	OFF	ON	OFF

†Provides CW rotation as viewed from nameplate end of motor. To reverse direction of motor rotation perform switching steps in the following order: 1, 8, 7, 6, 5, 4, 3, 2, 1

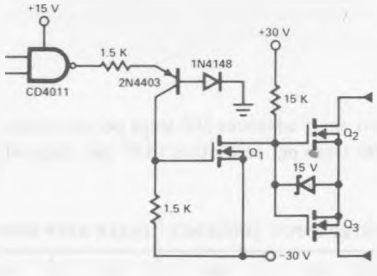
Analog switch circuits using VMOS transistors are shown in Figure 9. For signals which are always positive, the simple circuit of part (a) suffices. To keep the on-state resistance low and essentially constant with signal currents up to 200 mA, the gate voltage must exceed the signal peaks by at least 5 volts.



(a) +10 V Unidirectional VMOS Analog Switch



(b) ±10 V Bidirectional Analog Switch



(c) ±25 Volt Analog Switch

Various Types of Analog Switches
Figure 9

To permit both positive and negative signal inputs to be used, two VN10KM devices are connected in series as shown in part (b). In this manner, the drain source diodes are back to back and can block either polarity voltage.

When the internal switches of the DG300 analog gate are off, gate drive is applied through the 10K resistor. The VMOS switches are turned off by shorting the gates to the source when the DG300 switches on. In addition, the −15 volt supply is applied to the gate and source. The supply causes an AC ground at this point which virtually eliminates any feedthrough of the input signal through the VMOS capacitance and maintains reverse bias on the drain-body diodes.

In situations where variations in $r_{ds(on)}$ with signal level cause objectional distortion, a means of driving the VMOS switches with a constant gate to source voltage must be used so that $r_{ds(on)}$ is constant. A means of doing this is shown in part (c). The bipolar transistor serves merely as a level translator from the IC logic to the FET gate. When the logic output is low, the bipolar and the driver FET, Q_1, are off; the 15K resistor provides gate drive from the +30 volt supply to the VMOS switches. The zener maintains a constant 15 volt V_{GS} provided the input signal does not exceed +15 volts, although signals to 25 volts can be handled if some $r_{ds(on)}$ variation is tolerable. When a logic *high* is applied to the bipolar it turns on and also turns on Q_1 A voltage of −30 volts is applied to the gates of Q_2 and Q_3 which turns them off. The gates of Q_2 and Q_3 are shorted to their sources through the forward conduction of the zener diode, thus maintaining a high off impedance to the signal.

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2. Lee Schaeffer, "VMOS – A Breakthrough in Power MOSFET Technology", Application Note AN76-3, Siliconix, inc., Santa Clara, CA 1976.
3. Bill Roehr, "VMOS – A Giant Step Toward the Ideal," Fairchild Journal of Semiconductor Progress, Jan. - Feb. 1979, Fairchild Camera and Instrument Corp., Mountain View, CA.

Designs for VMOS push-pull converters

P. Regan and *P. Dewsbury*

In modern electronic systems involving microprocessor control, for example, the power requirements would typically consist of a DC supply of, say, 5 V for logic circuitry, and various low current supplies for linear circuits. Until recently, these supplies have been derived from inefficient series pass or linear regulators, but now switch mode power supplies are taking over, due to their low internal losses, small size, cost effectiveness, weight reduction and higher reliability. The majority of present switch mode power supply designs use fast bipolar transistors operating at typical switching frequencies of 20-50 kHz. VMOS power transistors now available can offer improved performance in such designs.

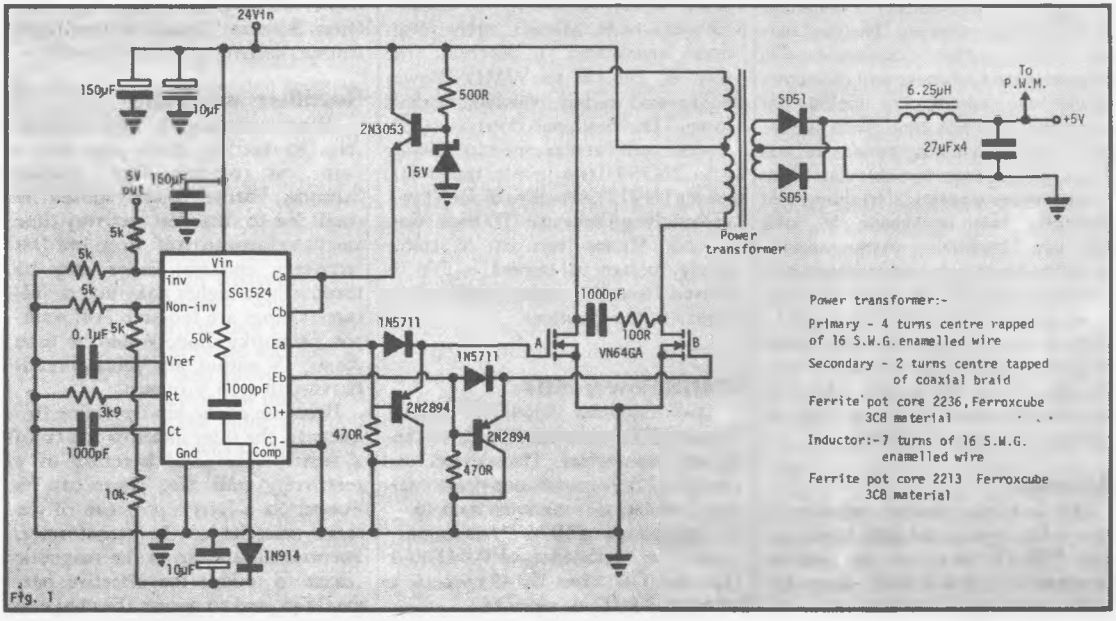
The VMOS Power FET properties which are of greatest significance in power supply design have been described in Reference 1. Briefly they are:

- No secondary breakdown. There is no need for complicated protection circuitry. R-C snubber networks will suffice.
- High input impedance. Drive circuits are made simpler and more efficient, hence commercial pulse width modulation control circuits can be used, and because their outputs are driving essentially capacitive loads, dissipation is low.
- Lack of minority storage time. Turn-off storage delay time can prove fatal in bipolar transistor push-pull arrangements, giving rise to pulse edge overlap, which results in high peak currents, excessive dissipation, core saturation and finally device destruction. To alleviate this, bipolar converters usually employ anti-saturation clamps, which reduce storage effects, but result in lower efficiency.
- Fast switching speed. Typical rise and fall times for high current devices such as the Siliconix VN64GA, when driven from a 50 Ω source impedance are 45 nsec. With rise and fall times as fast as these the power loss during transitions is nearly eliminated. The operating frequency due to fast switching can be as high as 500 kHz which considerably cuts the size and cost of filter components.
- No current hogging. To achieve greater power outputs, VMOS Power FETs can be connected directly in parallel, without the need for compensation networks.

To utilise the fast switching properties of VMOS Power FETs, a 100 kHz switch mode power supply has been designed. Design objectives were to keep the power supply as simple as possible whilst retaining high efficiency. These objectives proved to be easily achieved using VMOS, as will be shown in this article.

To simplify final testing and evaluation procedures, it was decided that the prototype design should provide a single output rail only. A 5 V, 20 A output was chosen and could be used, for example, to power logic circuitry. As a later refinement, additional windings were added to the transformer secondary to give ±19 V, 1 A output lines which, if series regulators are used, could provide +15 V supplies for operational amplifiers, etc. The +15 V rail could also be used to provide supply current for the converter control circuitry, after start-up. The converter was designed to operate from input voltages between 18 V and 28 V, and could conve-

Fig. 1: Prototype DC-DC converter.



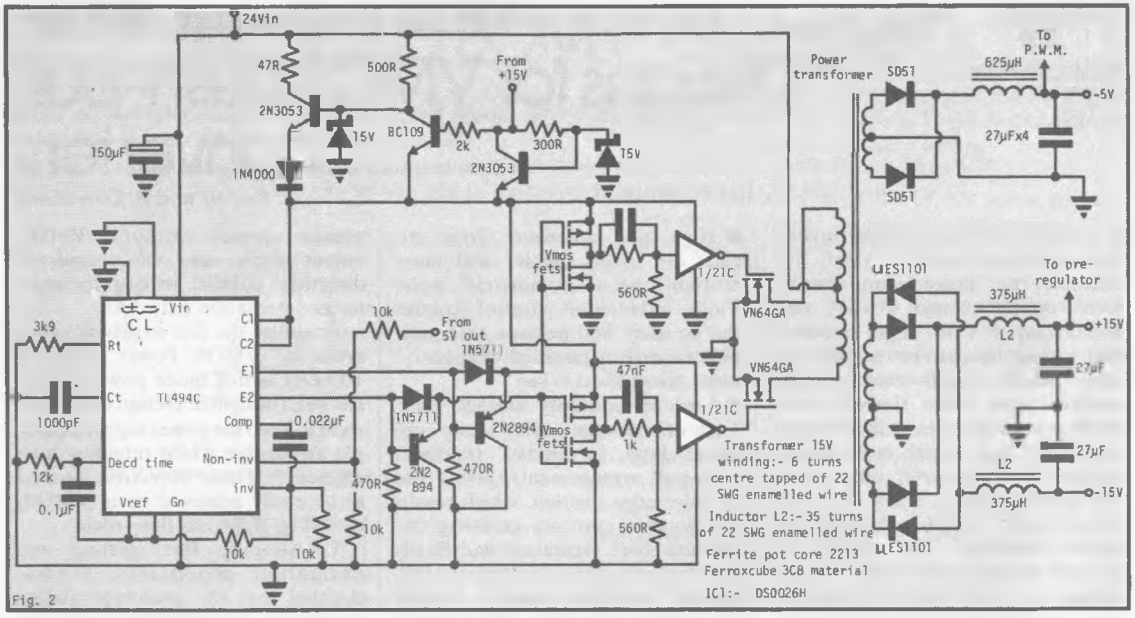


Fig. 2

niently be powered by a 24 V battery, as provided in many mobile environments.

The converter was divided into five main parts: the control circuitry consisting of a pulse width modulator; an interface section consisting of driver circuitry; the switching VMOS; the power transformer; and finally the output rectifiers and filters.

Pulse width modulator

Several types of pulse width modulation IC are available, but the Silicon General SG1524 was chosen because of its general availability from multiple sources. The two output drivers are n-p-n transistors with uncommitted emitters and collectors which are capable of sinking or sourcing 100 mA and with active pull down, switching speeds of less than 100 nsec can be achieved. It has a maximum operating frequency of 300 kHz, with provision for soft start-up frequency compensation and can function at any voltage between 8 and 40 V. This is not the only such control device on the market. Others which could be used, with suitable modifications to the circuits, are the Texas Instruments TL494C and the Ferranti ZN1066E, both of which are readily available.

Interface

The interface section provides a means for driving the gate inputs of the VMOS devices. A simple arrangement proved quite successful in the prototype arrangement.

Fig. 2: Modified 100 kHz push-pull converter.

One disadvantage of the SG1524 control IC is the high output transistor saturation voltage (maximum 2 V). When connected in grounded emitter mode with the gate of a VMOS device connected to the collector, the 2 V logic "0" level would be greater than the minimum threshold voltage of the VN64GA. There are several ways of overcoming this problem (for example, by using pulse transformer coupling). For the prototype unit, the output transistors of the pulse width modulation IC are connected as emitter followers with external active pull-down transistors, to decrease the turn off time of the VMOS Power FETs and reduce switching speed losses. The basic pull down circuit is a totem pole arrangement consisting of a 2N2894 (fast p-n-p transistor) and a 1N5711 Schottky diode. Typical switching times are 100 nsec turn on and 50 nsec turn off. A stable supply voltage of around +15 V is derived from the input supply via a linear series regulator.

VMOS Power FETs

Two Siliconix VN64GA VMOS Power FETs were used to drive the power transformer. This device can handle 12.5 A continuous drain current and has a maximum drain to source voltage of 60 V. It has a maximum "on" resistance of 0.4 Ω and rise and fall times of 45 nsec in a standard 50 Ω test circuit.

Transformer

Of the many shapes, sizes and types of transformer cores available, a ferrite pot core was chosen for several reasons, but mainly because of all the materials available, ferrite offers the best high frequency characteristics. The Ferroxcube 3C8 material was chosen because it has high saturation flux density (4000 G) and high initial permeability (2700) making it well suited for high frequency converter design. Very similar material properties may be found in ferrites produced by other manufacturers, e.g. type N27 from Siemens. Details of the transformer design appear in Appendix A.

Rectifiers and filters

When switching at high frequencies, the rectifier diodes must have a very fast recovery time. Ideally Schottky barrier diodes should be used, due to their fast recovery time and low forward volt drop, but fast recovery epitaxial diodes may be used, where higher peak-inverse voltage ratings are required. For example, Schottky diodes would be used for a 5 V output, and epitaxial rectifiers with ±15 V outputs.

Because of the high operating frequency, the filter inductors will be of a small value and therefore of a relatively small size. These can be wound on a ferrite pot core of the same material as the transformer, but with an air gap in the magnetic circuit to reduce the effective permeability and so permit the choke to

handle a high average DC current.

Again because of the high frequency of operation, the filter capacitor value will be small. To give low output voltage ripple, several high frequency electrolytic capacitors may be connected in parallel, thus reducing the effective series resistance and inductance components. Design details for the filter components are given in Appendix B.

Practical considerations

The circuit of the prototype DC-DC converter is shown in Fig. 1. It is a transformer coupled push-pull converter operating with a VMOS transistor switching frequency of 100 kHz.

The transformer was wound on a 3C8 ferrite pot core size 3622. This consisted of two halves of identical cores which when clamped together produce the magnetic circuit. The primary winding consists of four turns, centre-tapped and the 5 V secondary winding is two turns, centre-tapped. When winding a transformer with such a low number of turns, leakage inductance presents a major problem. This inductance is created by the difficulty of achieving close coupling between windings and gives rise to high voltage spikes at switching. These spikes could rise to above the breakdown voltage rating of the VMOS transistors. To reduce this, the primary winding was wound inside the 5 V secondary, which consisted of co-axial braid. When the leakage inductance of this assembly was measured, it was found to be 60 nH.

The VMOS transistors were mounted on a common heatsink and isolated from the grounded heatsink by Beryllia-ceramic spacers, which present low capacitance, typically 20 pF, between transistor case and heatsink, and do not affect switching speeds. (See Note 1.)

The rest of the circuit was mounted on a double sided printed circuit board. High frequency construction techniques were used throughout. The top face copper of the printed circuit board was used as a ground plane and proved advantageous for achieving low impedance circuit grounds. The inductance and resistance of all tracks carrying high current were minimised by using tinned copper braid. Connections to the drains of the VMOS transistors were kept as short as possible and equal in length. To minimise pulse edge ringing effects, co-axial cable

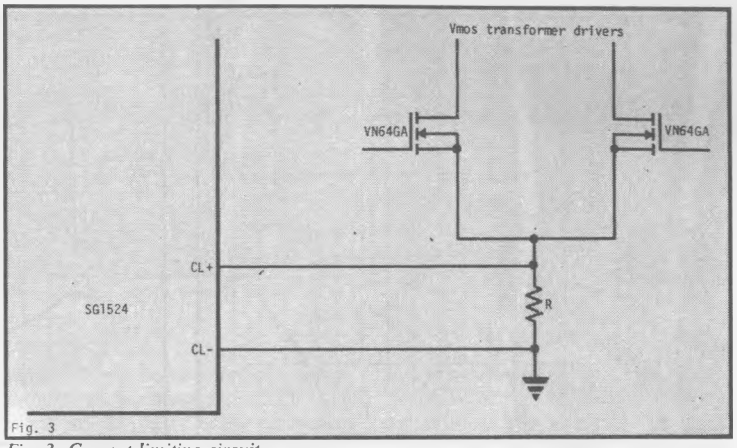


Fig. 3: Current limiting circuit.

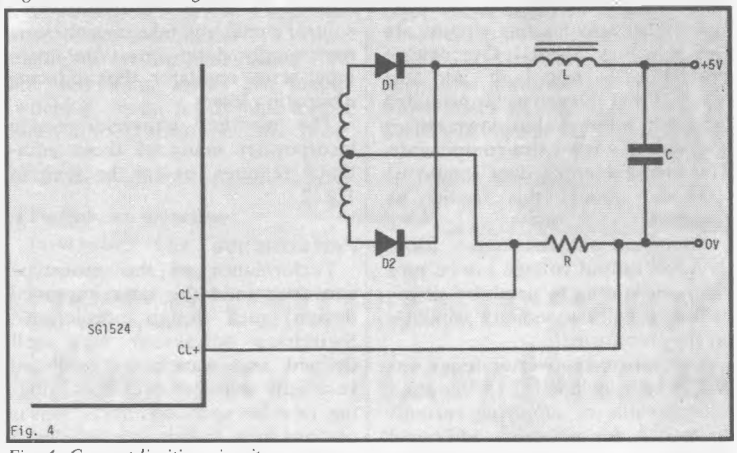


Fig. 4: Current limiting circuit.

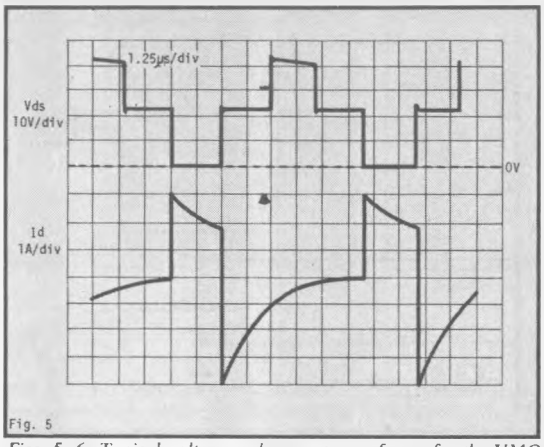
was used to connect the VMOS gates to the switching interface.

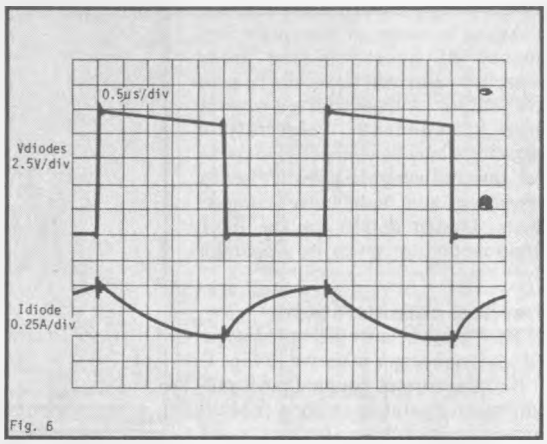
Alternative circuit features

Use of alternative PWM control circuits: A modified 100 kHz push-pull converter, incorporating several improvements, was designed using the Texas Instruments TL494C. These are shown in Fig. 2. Although the TL494 presents a lower output saturation voltage (1.3 V maximum), this is still a little higher than the 1.0 V minimum threshold voltage of the VN64GA, so the pulse width modulator output stage is connected as before in emitter follower mode with active pull down.

These outputs then drive a Siliconix VQ7254CJ complementary 2 A quad VMOS device (currently under development — see note 2) connected in push-pull inverter configuration. Each VMOS inverter then drives a MOS clock driver inverter, via a potential divider arrangement. The MOS clock driver inverter is capable of sinking and sourcing transition currents of up to ±1.5 A when driving capacitive loads. Typical rise and fall times of 40 nsec are possible with a 1000 pF load. The clock driver input is TTL compatible. This second stage of inversion is necessary but any suitable high current inverter, such as a complementary VMOS arrangement or a compound npn-pnp emitter follower, may be used. The DS0026 clock driver was chosen to illustrate the application of commercially available compatible ICs.

Current limiting and overvoltage protection: Current limiting and overvoltage protection may be easily achieved. There is a current limiting capability incorporated in the SG1524 IC. Its operation depends on sensing a voltage drop across a low value resistor in any suitable current path, and reducing pulse duty cycle when a pre-determined limit is exceeded. Suitable sensing points would be in the secondary return line or in the common source connection in the primary circuit. The resistor should be non-inductive or circuit instability may result. Two





Figs. 5, 6: Typical voltage and current waveforms for the VMOS drains and rectifier cathodes.

suitable current limiting circuits are shown in Figs. 3 and 4. Overvoltage protection is not built into the SG1524, but this can easily be added using the internal shut down circuit and adding a few extra components. The manufacturer's data should be consulted should this facility be required.

Additional output voltages: More than one output voltage can be provided, according to need, by simply including extra secondary windings on the transformer.

An improved converter design was built which included ±15 V output rails, capable of supplying currents up to 1 A for powering additional circuitry, e.g. operational amplifiers. The additional winding consisted of six turns, centre-tapped. The output voltages, after rectifying and filtering, are around ±19 V. Simple series linear regulation may then be used to produce stable ±15 V supplies.

The +15 V supply line can serve a further purpose. After turn-on, the converter runs up to full operation within a time defined by soft start components within the control circuitry. After run up, the stable +15 V rail may be fed back to the control circuit and take over the current supply duties from the main input series regulator, thus reducing dissipation losses.

The modified converter design incorporates many of these additional features, as can be seen in Fig. 2.

Performance

Performance of the prototype converter (and the later improved design) met design predictions. Switching behaviour was well defined and waveforms exhibited very little transient overshoot, ringing, or other spurious effects. This is obvious from examination of Figs. 5 and 6 which show typical voltage and current waveforms for the VMOS drains and rectifier cathodes. Even with a DC input voltage of 28 V, drain voltage overshoot was less than the 60 V rating of the VN64GA, over the whole operating current range, and with the RC snubber network removed.

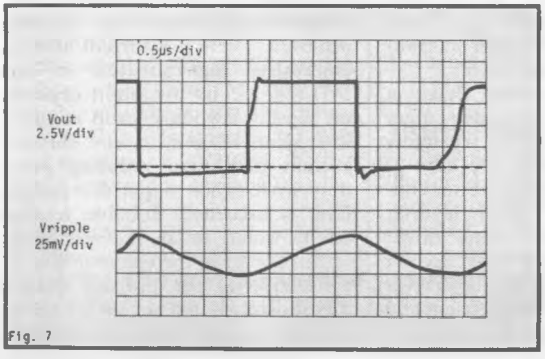
It will be seen later that the power losses in the Schottky rectifiers exceeded those in the VMOS power transistors. However, only a minimum of heatsinking was employed for the rectifiers. Schottky diodes exhibit a negative temperature coefficient of forward voltage, VF, and so the rectifiers were allowed to run up to a reasonably high operating temperature to reduce their power losses.

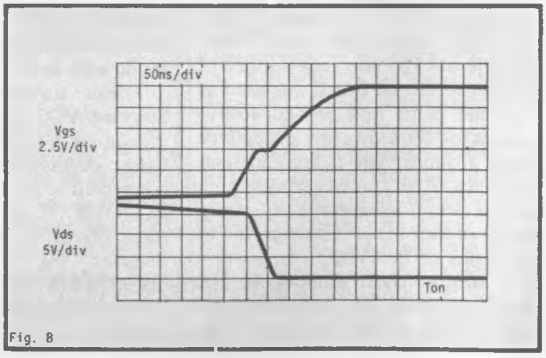
DC performance: Line regulation was good, the output voltage changing only 2 mV for a change in input voltage from 18 to 28 V. This represents a power supply rejection ratio of greater than 70 dB. Load regulation was excellent, with no change in output voltage being detectable over the whole operating current range.

Output voltage ripple never exceeded 50 mV at peak-to-peak, as can be seen from Fig. 7, and was well within the design requirement of 100 mV peak-to-peak.

Switching performance: Figs. 8 and 9 show typical turn-on and turn-off characteristics for VMOS gate and drain voltages on the prototype converter. Figs. 10 and 11 show the improvements achieved on the converter of Fig. 2. Drain voltages and currents are depicted. Switching times have been reduced to 50 nsec, reducing the power losses

Fig. 7: Output voltage ripple. *Fig. 8 Typical turn-on characteristics for VMOS gate and drain voltages on the prototype*





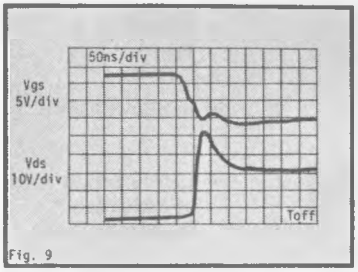
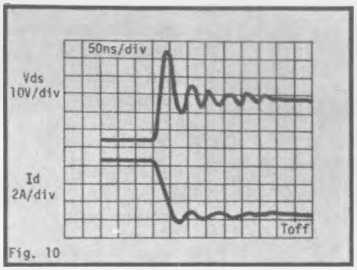
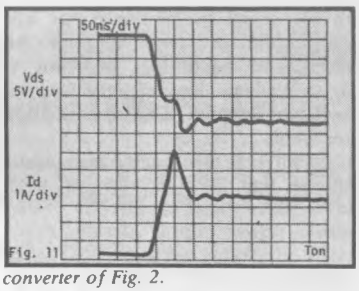


Fig. 9: Typical turn-off characteristics for VMOS gate & drain voltages on the prototype converter.





Figs. 10, 11: Improvements achieved on the converter of Fig. 2.

in the VMOS devices.

Efficiency: Efficiency and switching duty cycles were measured for changes in output load current. The results are shown in Fig. 12 and relate to the prototype circuit of Fig. 1. Efficiencies of better than 80 per cent were achieved for output currents of 5 A to 12 A. The maximum output current available is 25 A, with an efficiency of 60 per cent. This is achieved with the nominal supply voltage of 24 V and maximum device duty cycle (45 per cent). Such efficiency performance compares very favourably with that of a series linear regulator, which would only exhibit around 20 per cent efficiency at a load current of 25 A.

These performance features are summarised in Table 1.

Conclusions

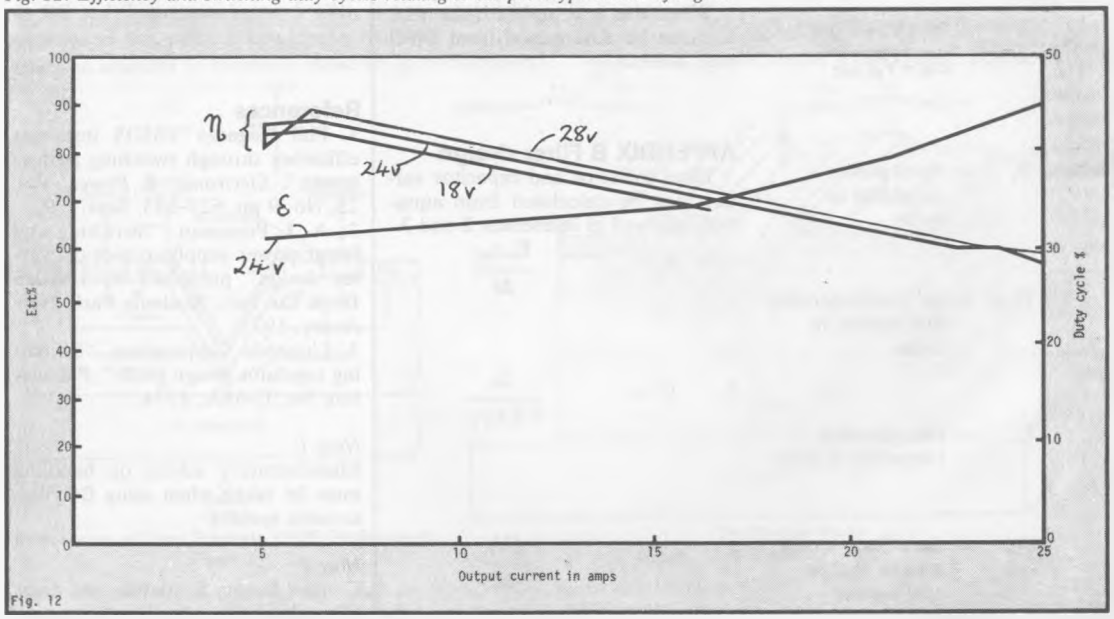
Determination of losses at any given output current reveals that more power is lost due to power rectifier forward voltage effects than is lost in VMOS transistor saturation losses. For example, at 10 A output, total power lost is 9.7 W. Diode forward losses account for 5.2 W and VMOS saturation losses are 2.7 W. The remaining losses are mainly switching losses, ferrite and copper losses in the transformer and choke, and losses in the control circuitry.

The future promises considerable reduction in the saturation losses of VMOS devices as newer structures offer on-resistances several times lower than those exhibited by the VN64GA. However, there can be very little improvement in the forward losses of Schottky rectifiers, which will become the limiting factor

Table 1

Performance parameter	Designed	Actual	Units
Input voltage range	18 to 28	18 to 28	V
Output voltage (nom.)	5	5	V
Output current range	1 to 20	1 to 25	A
Max. output power	100	>125	W
P.S.R.R.	—	>70	dB
Load regulation	—	≪0.01	mV/A
Output ripple (max.)	100	50	mVp-p
Efficiency 5 A to 25 A	—	87 to 60	%
Switching frequency	100	99.8 (adjustable)	kHz

Fig. 12: Efficiency and switching duty cycles relating to the prototype circuit of Fig. 1.



in efficiency performance for low output voltage power supplies. An alternative rectifying structure is needed which eliminates the forward voltage problem of silicon junction rectifiers.

In all other respects, this report shows that VMOS devices have many advantages to offer in switch mode power supply design, especially in terms of high frequency switching, lower switching losses, circuit simplicity and reliability, together with reduced circuit size and weight. As power MOS technology develops, more efficient and higher power handling converters will become commonplace.

APPENDIX A Transformer design

The design criteria have been well described in Reference 2 (chapter 8). The relevant design equations are:

1. $P_o = \dfrac{1.47\, B_{max}.f\, A_e.A_c \times 10^{-3}}{D_{cma}}$

2. $N_p = \dfrac{(E_{dc} - V_{ds\ SAT}) \times 10^8}{4.f.A_e.B_{max}}$

3. $N_s = \dfrac{N_p\,(V_o + V_d)}{E_{dc} - V_{ds\ SAT}}$

where P_o = input power capability in watts

B_{max} = the peak operating flux density in teslas

f = the operating frequency in hertz

A_e = the effective core area in square centimetres

A_c = the effective core winding area, also in square centimetres

D_{cma} = coil current density in circular mils.

N_p = number of primary turns

N_s = number of secondary turns

E_{dc} = the supply voltage

V_o = output voltage

V_d = the voltage drop across the diode

Firstly, using equation 1, one must calculate the value of $A_e.A_c$ to determine the size of transformer core. P_o can be roughly calculated and a value of D_{cma} fixed. This can be anywhere between 200 and 1000 circular mils. Then using equation 2, the number of primary turns are calculated, and finally using equation 3, the secondary turns are calculated.

When this is completed, the wire size can be determined from SWG wire tables.

APPENDIX B Filter design

Filter inductor and capacitor values may be calculated from equations derived in references 2 and 3.

4. $L = \dfrac{E_o.t_{off}}{\Delta i}$

5. $C = \dfrac{\Delta i}{8.f.\Delta V_c}$

6. $esr = \dfrac{\Delta V_c}{\Delta i}$

where L = inductance in Henries

E_o = output voltage

t_{off} = $t_{on} = \frac{1}{2}$ period of oscillation in seconds

Δi = peak-to-peak ripple current in Amps

C = capacitance in Farads

f = ripple frequency in Hertz

esr = equivalent series resistance of filter capacitor in Ohms

ΔV_c = peak-to-peak ripple voltage

When calculating the filter components, it is important to remember that the frequency of the output voltage after rectification is twice that of the operating frequency. Using equations 4, 5 and 6, these components can be calculated for the required output ripple limits.

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3. Unitrode Corporation. "Switching regulator design guide", Publication No. U-68A, 1974.

Note 1:
Manufacturers' advice on handling must be taken when using Berylliaceramic spacers.

Note 2:
Contact factory for details and dates of availability.

Application Note AN80-2

Meet the V-MOSFET Model

A modeling of the V-MOSFET transistor for high frequency design

Ed Oxner

Vertical MOS transistors for high frequency applications have, within the past year, mushroomed in popularity partly because of the inherent temperature-related advantages unique to the technology. Such advantages include no thermal runaway, no current hogging and, to a lesser extent, a greatly reduced secondary breakdown phenomenon. As a result of this increased popularity it is important that a model be available that allows the designer the freedom to use CAD (Computer Aided Design) techniques for design optimization. Although VMOS models have been offered by several investigators, none has achieved a fully satisfactory representation that offers viable results over wide ranges of frequencies[1,2].

The principal deficiency of these earlier models appears to lie in the heretofore neglect of the parasitic bipolar transistor inherent in a vertical channel MOS structure [although not discussed in this paper, the published models of the double-diffused DMOS transistor also suffer from this same neglect[3]]. This parasitic npn bipolar transistor arises from the interaction of the p-channel (base), the n+ source (emitter) and the n– drain drift epitaxy (collector).

At DC and frequencies below 5 MHz, it appears that the elements of this parasitic npn bipolar transistor have little affect on amplifier performance. However, as the frequency rises that continued neglect of including this parasitic transistor into the model becomes increasingly severe.

Device Design

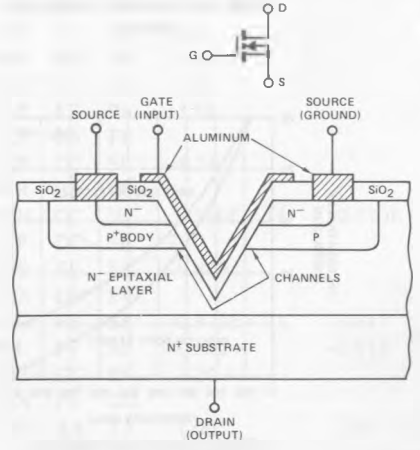
Much has been written offering the casual reader a basic understanding of VMOS design[4,5]. Beginning as a four-layer bipolar transistor all similarity ends when a V-groove is anistropically etched vertically into the structure providing access to the p-channel for an overlay metal gate. Such design offers an opportunity for high-frequency performance not easily possible with planar silicon MOS technology.

To effectively reduce the parasitic npn bipolar transistor effect the p-channel (base) is shorted to the n+ source (emitter) as shown in Figure 1. Generally with the base tied to the emitter an npn bipolar transistor remains in a non-conducting state.

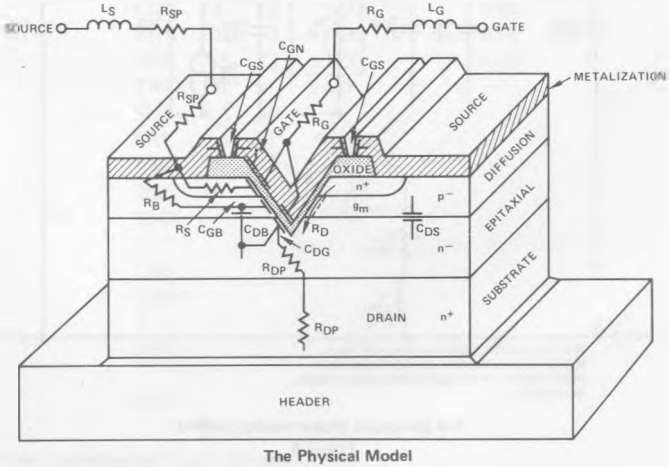
DEVICE SIMULATION

The Physical Model

Once a physical model has been constructed, achieving a workable schematic model is easy. Figure 2 shows the basic



Cross-Section of Drain Substrate VMOS Configuration
Figure 1



The Physical Model
Figure 2

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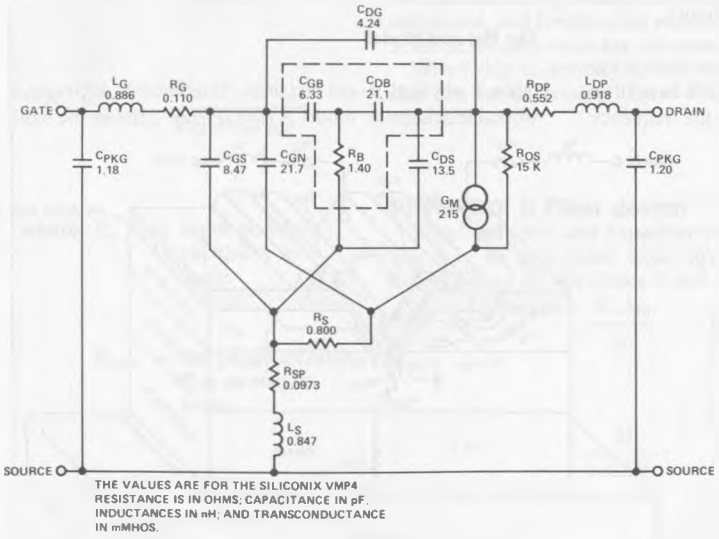
four-layer structure: An n+ substrate – the wafer itself – with an n– epitaxy into which has been diffused, first a p doped layer and then into this p layer n+ diffusion. Needless to say, this figure is not to scale! Left alone this would be the beginning of a typical bipolar transistor. A V-groove, suitable oxide and an overlay metal for gate and source completes the physical model. The model is then mounted on a header – in the case for the Siliconix VMP4 a flanged 380 SOE high-frequency package – and, finally, lead bonds attach the source and gate to their respective package terminals. Adding the parasitic capacitors and resistors is obvious. The result is a physical model of the VMOS high-frequency transistor, VMP4.

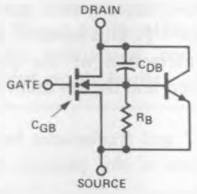
The Schematic Model

Using the physical model one can trace the entire electrical path and place all the parasitic elements that comprise the schematic model of the VMOS transistor. Figure 3 identifies each element of the schematic model. The element, R_{OS} ($1/G_{OS}$), represents the output resistance (conductance) which cannot be physically realized. L_G, L_S and L_{DP} are not intrinsic (that is, not part of the actual semiconductor element) but represent the package parasitic inductances of the Siliconix VMP4. R_G and R_{SP} represent resistive losses in both the gate and source metallizations as well as the lead losses. C_{GS} differs from C_{GN} in that the former is the field capacitance whereas the latter is that parasitic capacitance existing between the gate metal and the n+ source diffusion.

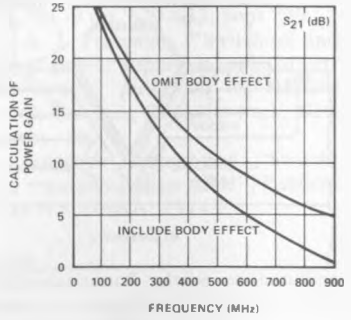
The parasitic npn bipolar transistor evident in Figure 1 must be considered as contributing parasitic elements (R_B, C_{GB} and C_{DB}) as well as being a potential parasitic generator; that is, contributing a finite Beta as an active element. The last is, indeed, possible and some explanation is necessary. Although the VMOS source is metallically tied to the base to reduce the effects of this parasitic npn bipolar transistor, it so happens that the resistivity of the p diffusion, that forms both the VMOS channel and the parasitic transistor's base, has a finite resistance (measured as ohms-per-square). Although at the point of metallic contact the base-to-emitter resistance is effectively zero, nonetheless as the distance is removed from the short the bulk resistance increases, so Figure 1 can be 'corrected' as shown in Figure 4. Should a voltage exist across this base resistance, R_B, it is conceivable that the parasitic npn bipolar transistor can turn on. One obvious means of placing a voltage across this resistance is by coupling the output voltage on the drain through the drain-base capacitor, C_{DB}. However, it was determined that this parasitic npn bipolar transistor, acting as an independent parasitic generator is effectively muted having been found not to be a major contributor to the performance of the VMP4 at HF through VHF (400 MHz). Nevertheless, the contribution of the npn bipolar transistor's parasitic elements, R_B, C_{GB} and C_{BD}, as an RC feedback network are of paramount importance as illustrated in Figure 5 where the intrinsic gain, S_{21} (dB), of the VMOS model is computed both with and without the contribution of these parasitic elements.



The Schematic Model VMOS (VMP4)
Figure 3



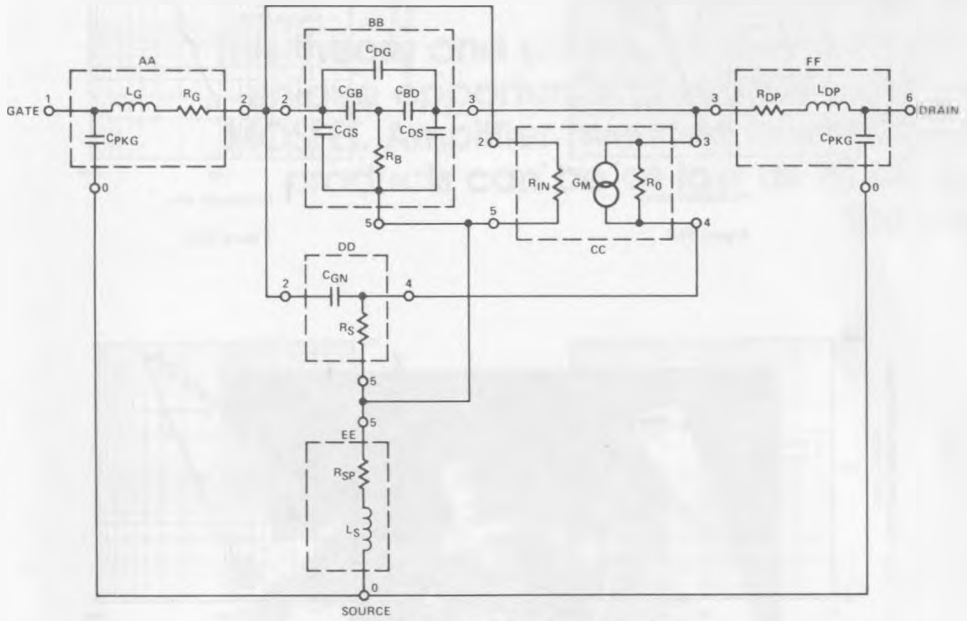
VMOS with a Parasitic npn Bipolar
Figure 4



Effect of Including/Excluding The Body Resistance in the Calculation of S_{21}(dB)
Figure 5

Experimental Results

Measured scattering parameters were used as the basis for establishing an exact model. Nodal analysis using the Circuit Optimization Program, Compact[6] working with 15 variables allowed the interconnection of 3 and 4 port networks as illustrated in Figure 6. In the Compact program variables are identified as negative quantities. The final program used to determine the values of each element of the VMP4 transistor is listed in Figure 7. Please be aware that one does not simply insert measured S-parameters and let the program crank numbers endlessly. No indeed. First you have to have a good idea of 'where you're coming from,' and use good judgment as to the initial values. Compact's values are an optimization of the initial data to arrive at parameter-fitting model.



Nodal Analysis Flow Chart For Compact Synthesis
Figure 6

```
CAP  AA  PA   1.18
SRL  BB  SE  -0.110      -0.886
CAX  AA  BB
CAP  BB  PA  -8.47
CAP  CC  SE  -6.33
RES  DD  PA  -1.40
CAP  EE  SE -21.10
CAP  FF  PA -13.50
CAX  BB  FF
CAP  CC  SE  -4.24
PAR  BB  CC
GEN  CC  VC   0.100E + 11   0.150E + 05   215
CAP  DD  SE -21.7
RES  EE  PA  -0.800
CAX  DD  EE
SRL  EE  SE  -0.973E- 01   -0.847
SRL  FF  SE  -0.552        -0.918
CAP  GG  PA   1.20
CAX  FF  GG
CON  AA  T3   1.00         2.00   0.0
CON  BB  T3   2.00                3.00   5 00
CON  CC  T4   2.00                5.00   4.00   3.00
CON  DD  T3   2.00                4.00   5.00
CON  EE  T2   5.00                0.00
CON  FF  T3   3.00                6.00   0.0
DEF  AA  T2   1.00                6.00
TWO  BB  S1  50.0
SET  AA  BB
PRI  AA  S1  50.0
END
200
END
0.77  -146.3  2.14  57.5  0.035  -6.0  0.759  -146.6
END
0.001
1     1      1     0.627
END

EOF:
```

Compact Program Including the Parasitic Elements of npn Bipolar in a Nodal Analysis
Figure 7

R_{IN} (in Figure 6) is used simply as a sense element required to realize a 4-port generator. To reduce its effect, a value of 1E10 ohms was assigned. S-parameters measured at 200 MHz were entered into the program and the computed Y-parameters were then compared with measured values and found to be in close agreement as shown in Figure 8.

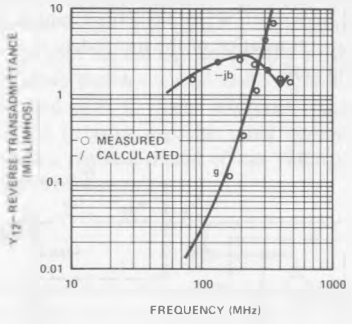


Figure 8(a)

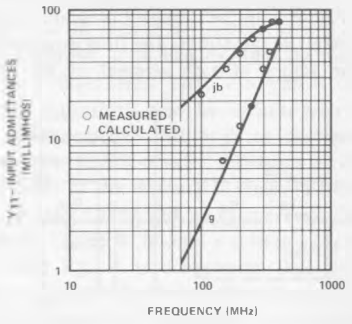


Figure 8(b)

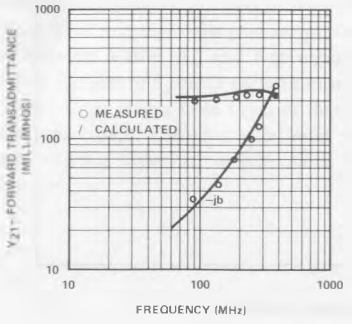


Figure 8(c)

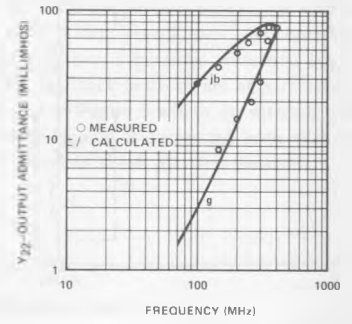


Figure 8(d)

VMP4
Figure 8

CONCLUSIONS

This model offers a designer an excellent start in computer aided design of amplifiers and what-not. To ease the burden of transferring these data into your Compact program, the Siliconix VMP4 S-parameter data file is available in the Compact library under the manufacturer's code 'SIX' and device code 'AA.'

Compact is presently available from 6 networks: NCSS; Control Data/Cybernet; GE/Honeywell; United Computing Systems; Tymshare; and, Computility/Call Data.

Finally, I would like to acknowledge the sacrificing work of my close associate, Larry Leighton for his efforts in assisting the development of this model.

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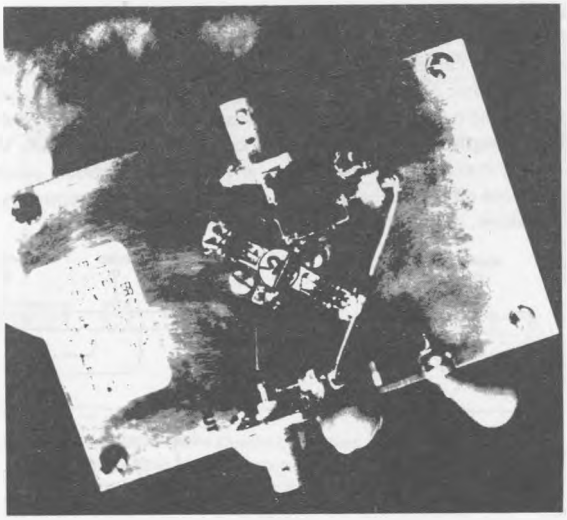
Build a Broadband Ultralinear VMOS Amplifier

This theory and construction article offers a unique opportunity to use the new power MOSFET. Amplifier two-tone intermodulation products can be as low as 70 dB below the carrier.

Ed Oxner
KB6QJ



A broadband amplifier using the VMP4 VMOS. It has a range from 1-70 MHz.

The high-frequency vertical MOS power transistor is nearest to being the most truly ubiquitous transistor ever to appear in the marketplace. Not only can VMOS perform in the conventional AM and SSB amplifiers, but because of no minority-carrier storage time, it provides superb performance in high-efficiency switch-mode Class E and F amplifiers. In fulfillment of the definition of *ubiquitous*, the VMOS transistor can be used interchangeably either as a power transistor or as a small-signal low-noise transistor.

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What Is VMOS?

VMOS, or more properly, vertical metal-oxide semiconductor field effect transistor, evolved from the double-diffused epitaxial bipolar technology and it's easy to see this evolution in Figure 1. The obvious differences are the V-groove gate region, which has been anisotropically etched into the structure, and the joining of the source (emitter) to the base to assure that the parasitic npn bipolar transistor remains cut off during operation.

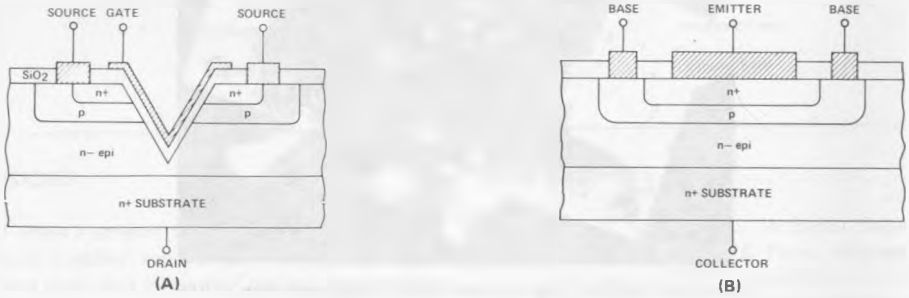
The VMOS substrate of n+ material forms the drain. The n– epitaxial (epi) layer offers increased breakdown and, especially important for high-frequency performance, greatly reduced feedback capacitance. This epi layer also enhances the possibilities for the development of very high-voltage high-frequency power transistors which will soon revolutionize transmitter design.

Unlike the more familiar DMOS (double-diffused MOS) technology where a cross section may be viewed (Figure 2) and compared to the VMOS cross-section (Figure 1), for each VMOS V-groove gate, two channels are formed which offer increased current density and, of utmost importance, halving the typical source-drain dynamic ON resistance of the DMOS alternative. Much like DMOS, also a majority-carrier semiconductor with no minority carriers by virtue of the fact that current flow, in the form of electrons, is entirely through the n-type material (the p-channel becoming inverted by the gate bias), the length of the channel plays a critical role in influencing the maximum F_T that is obtainable. Setting aside the deleterious effects of the parasitic elements inherent in any transistor, the calculated F_T for a silicon short-channel device such as either DMOS or VMOS approaches 20 GHz! Of course one cannot set aside these parasitic elements, and as a consequence, the theoretical limits are unattainable.

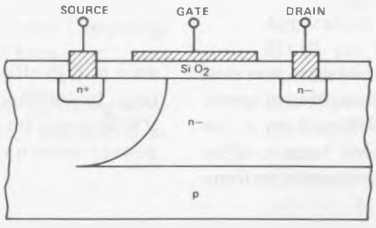
Why Use VMOS?

Like all FETs, whether they be junction or MOS, VMOS is a majority-carrier transistor by virtue of the fact that electron flow is entirely through n-type material (speaking, of course, for an n-channel device; for a p-channel device the electron flow would be entirely through p-type material, the n-channel having inverted by virtue of the negatively biased gate-potential). Consequently, an FET is somewhat analogous to an electric field-controlled bulk semiconductor resistor, and therefore, has a positive temperature coefficient. That is, as this semiconductor warms, its resistance rises. This is directly contrary to any bipolar transistor, for its temperature coefficient, by the same definition, would be negative.

All bipolar transistor failure can be traced directly to this negative coefficient which contributes to thermal stress: secondary breakdown, thermal runaway and current crowding. Since both DMOS and VMOS have the opposite characteristic under thermal stress, none of these failures occur. Consequently, with VMOS one does not experience any deleterious effects caused by either paralleling multiple VMOS power transistors or from severely mismatching the load.



A Comparison of Similarities Between a Vertical MOSFET and a Four-Layer Bipolar Transistor (B). EPI Indicates the Epitaxial Layer
Figure 1



Cross Section of a Double-Diffused DMOS Transistor
Figure 2

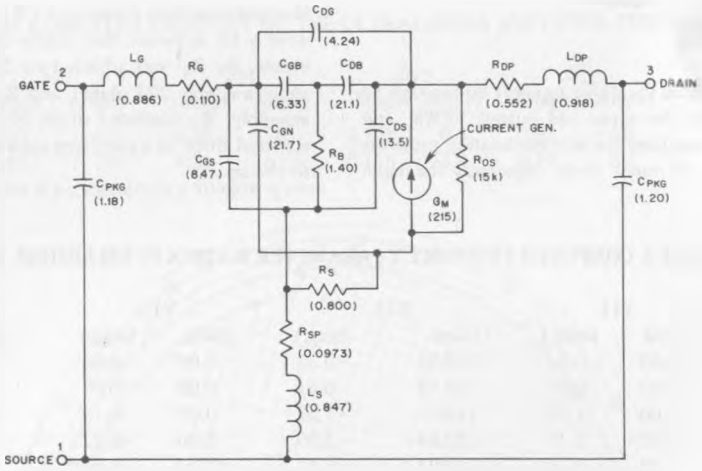
How to Use VMOS

VMOS is an insulated-gate MOSFET differing greatly from the common dual-gate MOSFET. The typical dual-gate MOSFET handles a few milliamperes of drain current whereas VMOS can handle *amperes*. Because of its mass – and coupled with mass, a much higher parasitic capacitance – there is little fear of an inadvertently blown gate. Because of the higher input capacitance, no gate-protection diode is necessary for protection in handling. To allay any arguments to the contrary, in over three years I have not experienced any failures stemming from gate puncture arising from mishandling.

VMOS is a Type C FET, an enhancement-mode MOSFET. That means it remains fully off when either zero bias or negative bias is applied to the non-zenered gate (negative bias *cannot* be applied to a zenered VMOS gate). With the application of a positive potential beyond the threshold voltage (specified as between 0.8 V and 2.0 V), drain current will flow. Once a certain quiescent current is reached, any further increase in gate voltage results in a linear increase in the DC drain current. Biasing VMOS is different than biasing bipolar transistors simply because VMOS only requires a positive potential to activate drain-to-source current flow. A cursory glance at a typical bias network might not appear too different but, unlike the bipolar transistor which requires a moderate to heavy base current, VMOS biasing requires no current at the gate. Consequently, the RF isolation between the gate and the bias network can be a simple high-value carbon resistor. Such a method was used in the video amplifier design described in this article, where a 27 KΩ resistor ties between the 4.7 KΩ voltage divider and the 20 V zener diode.

Modeling the VMOS VMP4

The equivalent circuit for the VMOS transistor has been previously published and is repeated in Figure 3. This

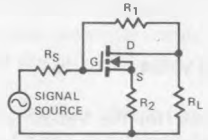


The Vertical-MOS VMP4 Circuit Equivalent. Values in Parentheses are for this Siliconix Unit. Resistance is in Ohms, Capacitance in pF, Inductance in nH and Transconductance is in mmhos. Identification of the Elements (left to right) is Tabulated Below.
Figure 3

C_{PKG}	Input and output capacitances of the VMOS package.
L_G	Gate inductance.
R_G	Gate resistance.
C_{GS}	Field capacitance.
C_{GN}	Capacitance from gate to n–.
C_{GB}	Capacitance from gate to body.
C_{DG}	Capacitance from drain to gate.
R_B	Body resistance of P diffusion.
C_{DB}	Capacitance from drain to body.
R_{OS}	The element R_{OS} ($1/G_{OS}$) represents the output resistance (conductance) which cannot be physically realized.
R_{DP}	Drain resistance of die attach material and package.
L_{DP}	Drain inductance of package material.
L_S	Source inductance.
R_{SP}	Source resistance.
R_S	n^+ diffusion resistance.

L_G, L_S and L_{DP} are not intrinsic (that is not part of the actual semiconductor element) but represent the package parasitic inductances of the Siliconix VMP4. R_G and R_{SP} represent resistive losses in both the gate and source metallizations as well as the lead losses. C_{GS} differs from C_{GN} in that the former is the field capacitance existing between the gate metal and the n+ source diffusion.

model, when properly simulated to include the parasitic npn bipolar transistor elements using a computer simulation program (COMPACT), offered excellent correlation with measured data over a reasonably wide bandwidth. Values of two-port admittance parameters obtained from the computer simulation are offered in Table I. For frequencies below 100 MHz these values must be considered as approximate because the characteristic break-frequency typical of all common-source connected amplifiers using FETs and MOSFETs was not included in the simulation. However, for general design the values in Table I offer the circuit designer sufficient accuracy so that, in all probability, little or no tweaking of the finished circuit is required for optimum performance.



The Simplified Circuit of a Broadband Video Amplifier
Figure 4

Designing the Amplifier

The design goals included the desire to cover 80 through 10 meters with flat gain, low input and output VSWR, and perfect linearity. That is, have the intermodulation products as low as possible. To meet these objectives the basic equivalent circuit shown in Figure 4 was chosen. The resistances, R_S and R_L, represent generator (source) resistance and load resistance, both 50 ohms for this design. Feedback resistor R_1 and source resistor R_2 combine to flatten the gain response and set the input resistance to match 50 ohms. R_1 and R_2 are determined by using the following formulas.

$$R_1 = \frac{\sqrt{R_S R_L}}{2} \cdot \left[\sqrt{G} + \sqrt{G + 4\left(1 + \sqrt{G} \cdot \frac{R_S + R_L}{2\sqrt{R_S R_L}}\right)}\right] \quad (1)$$

$$R_2 = \left(\frac{R_S R_L}{R_1}\right) - \frac{1}{G_M} \quad (2)$$

where

G is the desired stage gain for the amplifier, and

G_M is the forward transconductance value of the transistor expressed in mhos. (Y_{21} real)

Manipulating these formulas for R_1 and R_2, values obtained were a bit different than easily obtained standard resistor values. So R_1 was adjusted to 270 ohms (the calculated value was only 273 ohms), and R_2 to 5 ohms. In the final assembly, R_2 consisted of six 30-ohm resistors in parallel, soldered three to a side from each source lead on the VMP4 to chassis.

TABLE I. COMPUTED TWO-PORT Y-PARAMETER MATRIX IN MILLIMHOS, VMP4

	Y11		Y21		Y12		Y22	
Freq.	(Real	Imag.)	(Real	Imag.)	(Real	Imag.)	(Real	Imag.)
1.0	0.00	0.24	210.58	−0.30	0.00	−0.03	0.07	0.25
2.0	0.00	0.48	210.58	−0.61	0.00	−0.05	0.07	0.50
5.0	0.00	1.20	210.59	−1.52	0.00	−0.13	0.07	1.24
10.0	0.02	2.39	210.64	−3.05	0.00	−0.27	0.09	2.48
20.0	0.09	4.78	210.84	−6.11	0.00	−0.53	0.17	4.95
30.0	0.20	7.17	211.18	−9.19	0.01	−0.80	0.31	7.43
50.0	0.56	11.97	212.25	−15.47	0.02	−1.31	0.74	12.41
100.0	2.32	24.09	217.24	−32.49	0.11	−2.50	2.88	24.95
120.0	3.42	29.00	220.13	−40.12	0.18	−2.91	4.21	30.01
140.0	4.78	33.94	223.51	−48.43	0.28	−3.27	5.86	35.11
160.0	6.42	38.92	227.33	−57.56	0.43	−3.57	7.85	40.21
180.0	8.40	43.91	231.53	−67.69	0.64	−3.79	10.24	45.31
200.0	10.75	48.88	236.01	−79.01	0.94	−3.93	13.07	50.36
220.0	13.52	53.79	240.62	−91.74	1.36	−3.98	16.39	55.30
240.0	16.73	58.58	245.17	−106.10	1.92	−3.92	20.25	60.06
260.0	20.45	63.15	249.36	−122.30	2.69	−3.76	24.69	64.52
280.0	24.67	67.39	252.81	−140.54	3.71	−3.50	29.72	68.54
300.0	29.40	71.16	255.01	−160.94	5.06	−3.17	35.35	71.95
320.0	34.56	74.26	255.36	−183.50	6.81	−2.81	41.48	74.52
340.0	40.05	76.52	253.13	−208.04	9.04	−2.49	47.97	76.04
360.0	45.63	77.74	247.61	−234.10	11.81	−2.31	54.55	76.29
380.0	51.00	77.81	238.15	−260.90	15.16	−2.40	60.87	75.12
400.0	55.76	76.70	224.34	−287.36	19.10	−2.93	66.44	72.51

The next step, which for most amateurs may not be possible, is to simulate the performance using a computerized optimization program, in this case one called COMPACT (Computer Optimization of Microwave Passive and Active CircuiTs). For those interested in the details, the basic program is offered in Table II and the final analysis showing the theoretical performance of the video amplifier is given in Table III. If we remember that scattering parameters are reflection coefficients, the values of S_{11} (input) and S_{22} (output) suggest that a reasonably good match should be possible. The expanded Smith Chart projections in Figure 5 offer easy visualization of the expected results across the 2 MHz to 30 MHz bandwidth. The overall anticipated performance, taken from Table III data, suggests nearly 13 dB forward power gain ($S_{21}{}^2$) and so-so stability (K greater than 1.0).

TABLE II. THE COMPUTERIZED OPTIMIZATION PROGRAM (COMPACT)

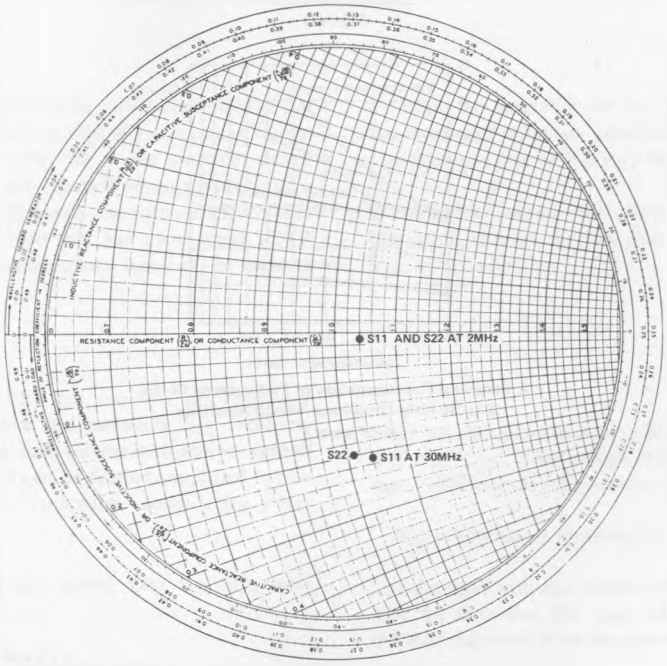
```
RES   AA  SE  -270.0      2     30
TWO   BB  S1    50.0      END
PAR   AA  BB              1.00  -6  20.94  175.5  0.005  85.6  0.99  -6
RES   CC  PA    -5.0      0.81  -72 14.36  125.5  0.054  38.5  0.81  -74
SER   AA  CC              END
PR1   AA  S1    50.0      EOF:
END
```

This program simulates amplifier performance. See text.

TABLE III. COMPUTER PRINTOUT OF THE ULTRALINEAR AMPLIFIER PERFORMANCE

	S_{11}		S_{21}		S_{12}		S_{22}		S_{21}	K
Freq.	(Magn	Angle)	(Magn	Angle)	(Magn	Angle)	(Magn	Angle)	DB	Fact.
2.00	0.02	−17	4.26	178.8	0.159	−0.3	0.02	−18	12.58	1.08
30.00	0.10	−79	4.21	161.3	0.156	−2.4	0.10	−82	12.49	1.06

These are polar S parameters in a 50-ohm system.



These Expanded Smith Chart Projections Offer Easy Visualization of the Expected Broadband Amplifier Results Across a 2 to 30 MHz Bandwidth. The plot of the Calculated Values for S_{11} and S_{22} is Shown
Figure 5

After adding the proper biasing and voltage-isolating capacitors, the final operational circuit emerges as shown in Figure 6. Performance is graphically offered in Figure 7. Additional measurements include a 1 dB saturation output power of 3.7 watts and a spot noise-figure measurement of 4 dB at 30 MHz.

There is little explanation needed for the constructor. Layout is not overly critical. Leads should be kept short, in particular for R_1 and the batch paralleling R_2 which, incidentally, should be carbon-composition resistors. The heat sink shown is unquestionably an overkill but using one equal in size to the copperclad board is a great convenience.

I acknowledge the diligent efforts of my colleague, Larry Leighton, WB6BPI. For his contributions to the success of this project, I express my gratitude.

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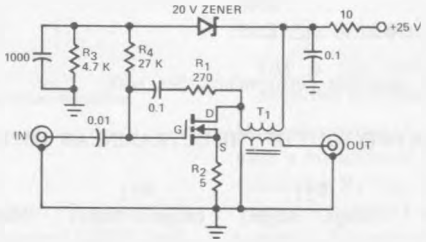
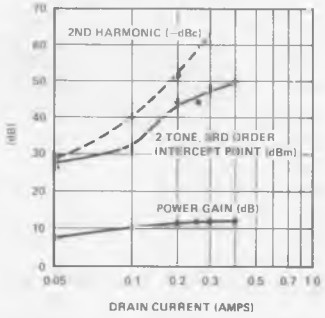
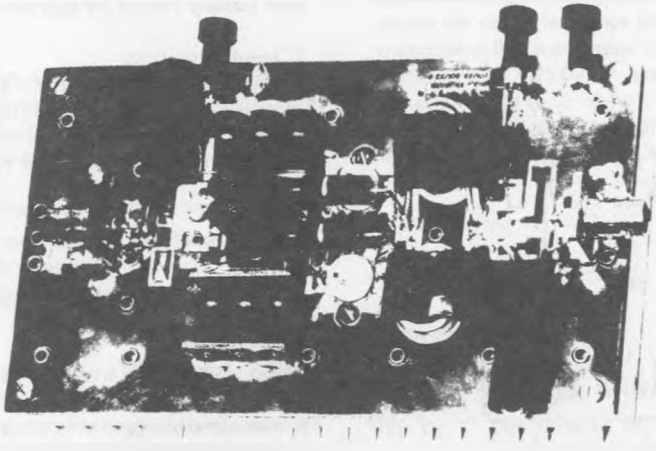


Schematic Diagram of a Broadband Video Amplifier. T_1 Consists of 9-1/2 Turns of No. 30 Enameled Wire Bifilar Wound on a Stackpole No. 57-9130 Balun. Resistance is in Ohms and Capacitance is in μF.
Figure 6



A Graphical Representation of Performance of the 2 to 30 MHz Ultralinear VMOS Amplifier
Figure 7

HF Power Amplifier Design Using VMOS Power FETs



Larry Leighton
Ed Oxner

The goal isn't simply to fit VMOS into an HF amplifier but to first derive a basic equation that will assist us in formulating a technique to simplify HF power amplifier design when using VMOS. Secondly, we will design a power amplifier using a real RF VMOS power transistor. This amplifier should offer both high fixed gain and a low input VSWR across the military communications band of 30 MHz to 88 MHz.

Deriving the Formula

A good VMOS power FET has constant low-frequency gm, high input impedance and unusually low feedback. Because of these unique features the well-known general expression for power gain can be further simplified to provide what amounts to a "cookbook" formula for power amplifier design.

The general expression for power gain for any linear amplifier is:

$$G_P = \frac{|y_{21}|^2 \, \mathrm{Re}(Y_L)}{|Y_L + y_{22}|^2 \, \mathrm{Re}\left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)} \qquad (1)$$

To begin our derivation we first set y_{12} equal to zero and the remaining imaginary admittance terms (b_{11}, b_{21}, b_{22}) also to zero. Later we'll justify this action.

It should be noted that within the general expression (Equation 1) is the formula defining the input admittance, Y_{in}, of the amplifier.

$$Y_{in} = y_{11} \quad \frac{y_{12}\, y_{21}}{y_{22} + Y_L} \qquad (2)$$

Since we opted to equate y_{12} to zero, we immediately find that $Y_{in} = y_{11}$. One design objective is to provide a low input VSWR, or in other words a power match, so

$Y_{in} = Y_S$ (source admittance).

Interestingly, with the reverse transadmittance, y_{12}, set to zero, by definition the input admittance is unaffected by the load, Equation 1 can be rewritten

$$\frac{|y_{21}|^2 \, \mathrm{Re}(Y_L)}{|Y_L + y_{22}|^2 \, \mathrm{Re}(Y_S)} \qquad (3)$$

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Equation 3 can be further simplified by first substituting

$(y_{21})^2 = (g_m)^2$
$\text{Re } Y_L = 1/R_L$
$\text{Re}(y_{22}) = 1/R_{out}$
$\text{Re } Y_S = 1/R_S$

where

R_L is the load resistance;
R_S is the source resistance; and,
g_m is the forward transconductance of the VMOS power transistor.

which results in:

$$G_P = 10 \log \left[\frac{g_m^2 \, R_S}{R_L \left(\frac{1}{R_{out}} + \frac{1}{R_L} \right)^2} \right] \quad (4)$$

Solving for R_S:

$$R_S = \frac{10^{\left(\frac{G_{P(dB)}}{10}\right)} \left[R_L \left(\frac{1}{R_L} + \frac{1}{R_{out}} \right)^2 \right]}{g_m^2} \quad (5)$$

where $R_{out} = 1/\text{Re}(y_{22})$ (taken from Table I of small signal Y parameters).

Now fixing a resistor, R_S, across the gate-to-source terminals of the VMOS FET the gain and input impedance (hence source impedance) are set independent of the operating frequency within the HF bandwidth of the amplifier.

Why Get Excited about VMOS Design?

What with the prospects that power VMOS FETs offer in high-frequency amplifier design, one might conclude that VMOS is the designer's choice. See what you think.

1. Stability
Within the HF region the shunt input impedance loading requirements are constant since the transconductance of the VMOS power FET exhibits little change with frequency. *Very little feedback is required to ensure total stability.*

Because little feedback is required *the overall efficiency is improved* and out-of-band stability is enhanced.

Because VMOS RF power FET admittance parameters are little affected over the operating drain current *small-signal Y parameters become increasingly useful in establishing basic stability criteria for high-power design.*

2. Input Admittance
A stable quiescent drain current (I_D) regardless of drive or operating temperature (T_A) offers a near-constant input impedance *governed mainly by the input impedance of the matching circuit and not by the reflective load impedance.*

3. Gain
Without benefit of feedback and with a fixed load the amplifier offers flat gain across the entire 30 MHz to 90 MHz bandwidth. *Reverse gain exceeds −35 dB.*

4. Power Output
VMOS Power FETs, exhibiting a constant $R_{DS(On)}$ [$V_{DS(sat)} = R_{DS(on)} I_D$] regardless of frequency, will provide a leveled saturated output power. Most importantly: *they can withstand a 20:1 VSWR at any phase angle.*

5. Noise Figure
Because VMOS is a bulk semiconductor without the bipolar's base-emitter diode it appears that the measured small-signal noise figure represents *what can be expected when used in a power amplifier.*

In addition to these are the now well-known thermally-related benefits that VMOS offers: *no thermal runaway* and *no current hogging.*

Frequency Contraints

VMOS FETs possess a finite and frequency invarient input capacitance. There is an upper frequency at which this

TABLE I. TWO-PORT Y-PARAMETER MATRIX IN MILLIMHOS USING DV2880T, 28 V, 1.6 A

Freq.	Y11		Y21	Y12	Y22	
10.0	0.2	10.1	697.2 – 16.0	0.0 – 1.2	14.9	8.2
20.0	0.7	20.1	697.7 – 32.1	0.0 2.3	15.3	16.3
30.0	1.6	30.2	698.5 – 48.4	0.1 – 3.5	16.0	24.5
40.0	2.8	40.3	699.5 – 64.8	0.1 – 4.6	17.0	32.6
50.0	4.4	50.3	700.8 – 81.5	0.2 – 5.6	18.3	40.7
60.0	6.3	60.4	702.4 – 98.5	0.4 – 6.7	19.8	48.8
70.0	8.6	70.5	704.2 – 116.0	0.5 – 7.7	21.7	56.7
80.0	11.4	80.5	706.2 – 133.9	0.7 – 8.6	23.9	64.7
90.0	14.5	90.5	708.4 – 152.3	0.9 – 9.5	26.4	72.5
100.0	18.1	100.4	710.6 – 171.4	1.3 – 10.2	29.3	80.2

capacitance reactance will become appreciable with respect to R_S resulting in mismatch loss. Consequently, any designed increase in gain which also raises R_S (Equation 5) will adversely affect the input Q thus limiting the input frequency response.

Furthermore, as the frequency rises, y_{12} should not be equated to zero. From Equation 2 y_{12} affects Y_{in}, which, in turn, affects R_S which adversely affects mismatch loss. The limiting upper frequency is established by the maximum permissible input VSWR.

Into the Design

Our objective is to design a push-pull amplifier capable of at least 12 dB of power gain and outputting 100 W, at a drain voltage of 28 V across the 30 MHz to 88 MHz band. Input VSWR not to exceed 1.5.

The first step is to define the load line using the classic formula

$$R_L = \frac{[V_{DD} - V_{DS(on)}]^2}{2P} \qquad (6)$$

The Siliconix RF VMOS transistor, DV2880T is rated to output 80 W minimum at a power gain of 10 dB at 175 MHz with total dissipation of 160 W. $R_{DS(on)}$ is typically 0.5 ohm. We felt that this represented a comfortable margin and selected it for our design.

A push-pull design establishes that each VMOS should supply 50 W minimum if we assume that the matching transformers are lossless. With a drain supply of +28 V and the estimated peak drain current of approximately 3.6 A, we can calculate $V_{DS(on)}$:

$$V_{DS(on)} = R_{DS(on)} I_D = 0.5 \times 3.6 = 1.8 \text{ V}.$$

Using Equation 6 the load line is calculated at 6 ohms.

The most convenient way to establish this load line is by using ferrite transmission-line transformers. However, were the load line to output port impedance not an integer ratio, the match would require a more complicated design effort. In this design the 6 ohm load line can be closely achieved with the relatively simple combination of a 1:1 unbalanced-to-balanced balun followed by a 4:1 balanced-to-balanced transformer. Together this combination provides a balanced 6.25-0-6.25 ohms across the drains of the push-pull FETs.

With the drain load design complete, next establish the amplifier's gain and this is done with resistive input loading, R_S. Having gone through the exercise designing the output load we are very close to having the necessary information to calculate R_S. All that remains is to select a value for R_{out} [$Re(y_{22})$] which we take from Table I. To ensure our gain over the entire passband, it's wise to select worse-case $Re(y_{22})$ and that value is found at 90 MHz to be 0.026 mhos, or R_{out} = 38 ohms. Using Equation 5:

$$R_S = \frac{10^{\left(\frac{12}{10}\right)} \left[6.25 \left(\frac{1}{6.25} + \frac{1}{38}\right)^2\right]}{(0.7)^2} = 7 \text{ ohms}.$$

Ideally we would need an input matching structure stepping down from 50 to 7 ohms which for this broadband amplifier would be both costly and unwieldy. Rather than complicate the design let us opt for a 'near match' by using the transmission-line transformer combination 1:1/4:1, 50 ohm unbalanced to 6.25-0-6.25 ohm balanced. By not meeting the value of R_S (6.25 ohms in lieu of the calculated R_S of 7 ohms) we will need to reaffirm what gain to expect from the amplifier. Using Equation 4:

$$G_P = 10 \log \left[\frac{(0.7)^2 6.25}{6.25 \left(\frac{1}{38} + \frac{1}{6.25}\right)^2}\right] = 11.5 \text{ dB}.$$

PARTS LIST

RFC – Ferroxcube P/N VK200 09/3B

T_1, T_6 – Two turns of RG-196 A/μ 50 Ω coax wound on three balun cores placed end on end cores are Stackpole P/N 57-0973.

T_2, T_3 – Two turns #22 twisted pair, four turns per inch, wound on two balun core. Core is Stackpole P/N 57-1503.

T_4, T_5 – Three turns of 25 Ω coax wound on 6 torroid cores. Cores are configured similar to balun style core, three cores per side. Two 50 Ω coax RG-196 A/μ were paralleled to simulate 25 Ω coax. Cores are Indiana General P/N F627-8-Q2.

The Matching Transformers

For both the input and output balanced-to-unbalanced 1:1 baluns, 2 turns of RG-196 A/μ coaxial were wound through 3 Stackpole balun cores, 57-0973, placed end-to-end. The drain load 4:1 transformer was wound with 3 turns of *parallel-connected* RG-196 A/μ (for an equivalent 25 ohms) through a balun-style core made by using 6 Indiana General torroidal cores, F627-8-Q2, 3 cores per side. The input 4:1 transformer was wound with 2 turns of twisted (4 turns per inch) #22 AWG Beldsol 8051 through a pair of Stackpole baluns 57-1503, also placed end-to-end.

Building the Amplifier

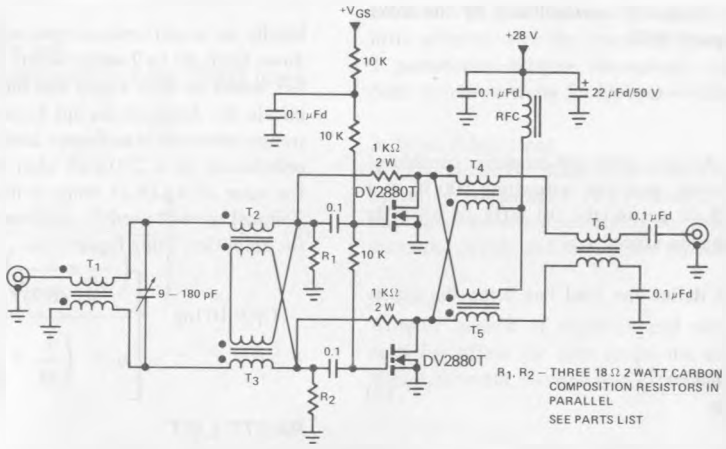
The construction is uncomplicated. Two problems are worth mentioning. First, the shunting resistors, R_S, made of 3

parallel-wired 2 W composition resistors (R_1 and R_2 in Figure 1) appear slightly inductive and fortuitously help compensate for the input capacitance of the VMOS transistors at the high end of the passband. Secondly, the input matching transformer requires a compensating trimmer capacitor, C_1.

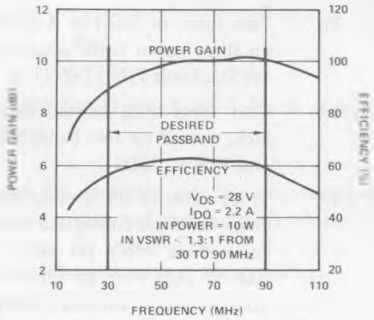
CONCLUSIONS

The performance of the finished amplifier (Figures 2 through 5) confirms the usefulness of Equation 5 in establishing both the desired gain and input VSWR. The latter is especially gratifying since VMOS power transistors offer a high input resistance across the HF band. The combined loss of the matching transformers amounts to 1 dB.

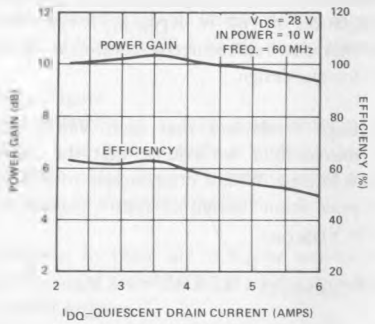
In operating the amplifier into a high output mismatch you will observe low level spurious oscillations which can be effectively removed by adding 1 KΩ feedback resistors. These resistors will not affect gain, gain flatness or input VSWR.



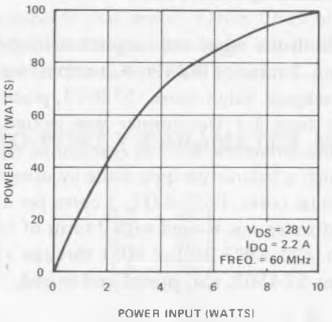
100 Watt Broadband VMOS Power Amplifier Using Siliconix DV2880T FETs
Figure 1



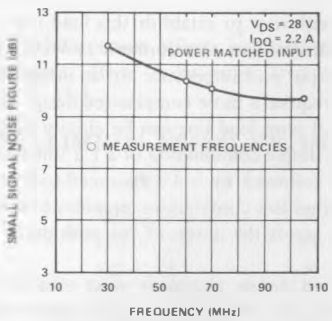
Power Gain and Efficiency vs Frequency
Figure 2



Power Gain and Efficiency vs I_{DQ}
Figure 3



Power Output vs Power Input
Figure 4



Small Signal Noise Figure vs Frequency
Figure 5

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mechanical data

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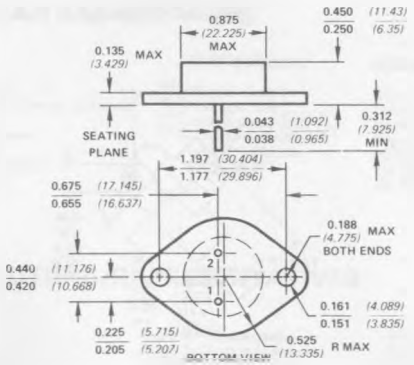
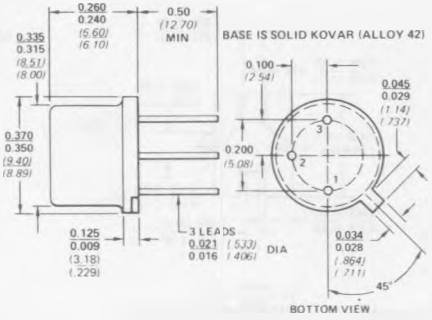
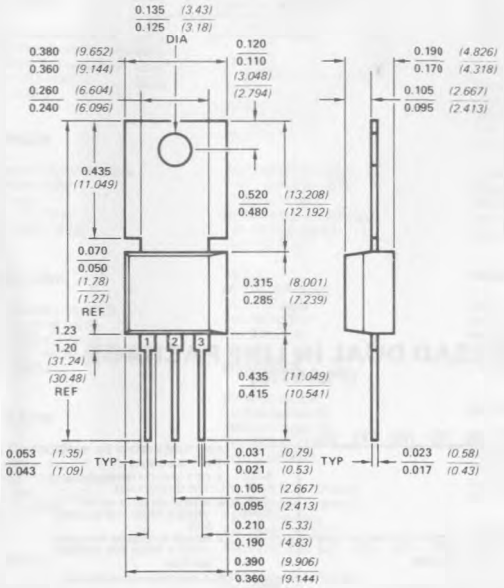
A, J Package
TO-3



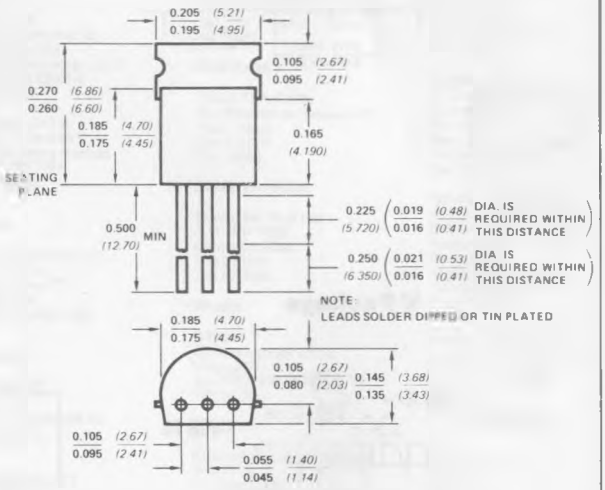
B, K Package
TO-39



F Package
TO-202



M Package
TO-237



S Package
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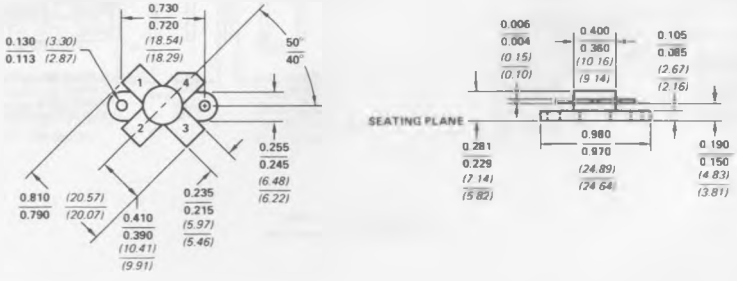
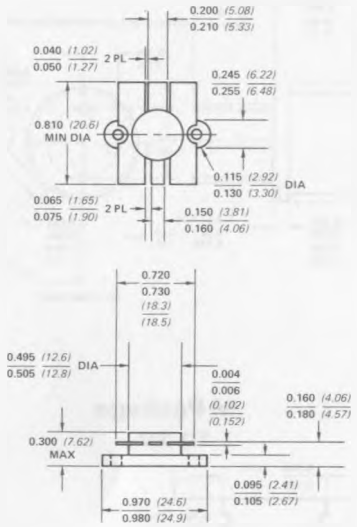


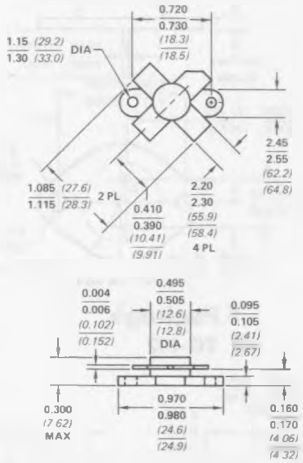
ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

mechanical data cont'd

T Package
.500 — JO Flange



U Package
.500 - SOE Flange



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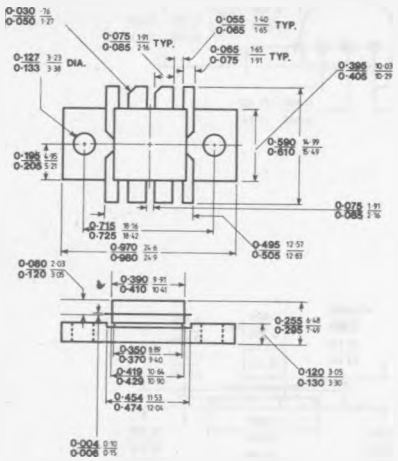

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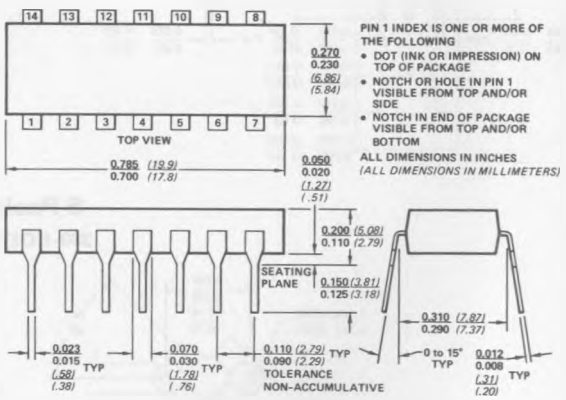

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