

Semiconductor Reference Guide

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INTRODUCTION

This SEMICONDUCTOR REFERENCE HANDBOOK is intended to be just that—a reference handbook. It is not a definitive text book on semiconductors. It is a compilation of data on Radio Shack's line of prime-quality ARCHER semiconductors. Every ARCHER device covered in this Handbook is guaranteed prime—they are not "fall-outs" or "seconds"; all are top-quality, with known JEDEC, EIA or manufacturer's numbers.

At the back of the book is a cross-reference listing for replacement of Transistors, Diodes and other interchangeable semiconductor devices. The total number of cross-referenced devices exceeds 100,000. These cross-reference/replacement listings are computer-selected and are based on careful analysis of important parameters of the listed devices.

NOTE: If you can't find a replacement listing for a device you require, refer to the specification listings of the appropriate ARCHER family device. Often you will be able to make suitable replacements based on the information

presented.

Each ARCHER replacement should meet or exceed the required parameters. However, due to differences in Quality Control and Manufacturing procedures (which often allow for or result in broad parameter variations), and because many of the ARCHER devices are capable of better performance than the original, Radio Shack does not guarantee, nor does it imply, that the listed items will provide an exact replacement in **every** instance. Therefore we recommend that you check the voltage and current requirements of the circuit (and other pertinent specifications) before replacement and compare with the specifications listed for that particular ARCHER device.

HOW TO USE THIS BOOK

This book has been prepared to aid in BOTH replacement and original applications of Semiconductor devices. The information included will be invaluable for the service technician as well as the circuit designer (whether he be an engineer, hobbyist, student or

electronics experimeter).

We have included hints on handling Semiconductor devices, operating considerations, and some simple tests to aid you in evaluating the quality of the device in existing equipment (and thus the need for replacement). Also, a complete section on the specifications for each of the ARCHER devices is included; if there is any question in your mind about replacement equivalents or original use, refer to the appropriate category in the book. You will find the important characteristics specified there.

The next to last section is an extensive listing of replacement and cross reference between other manufacturer's numbers (both JEDEC/EIA 2N—numbers and in-house designations) and the ARCHER devices. This listing provides for the substitution of over 82,000 semiconductors with ARCHER devices.

The final section includes case style drawings and some handy reference notes, a comprehensive glossary of commonly used words, plus symbols and abbreviations.

CARE AND HANDLING OF TRANSISTORS

Most modern transistors are somewhat immune from mechanical shock; however, it is always a good idea to keep them from excessive mechanical shocks, especially the metal-case type (avoid dropping, etc). When cutting transistor leads, use scissor-type cutting tools (rather than diagonal cutting tools which use a crimping action). Crimp-type cutting tools produce a mechanical shock along the lead which when transmitted to the semiconductor chip or material can cause fracture. Consider the force with which the cut lead flies off the crimp-type cutting tool and you have a good idea of the intensity of the equal and opposite force which acts on the lead going into the device.

It is always a good practice to use a heat-sink tool on a transistor lead when soldering (use a low-wattage iron—30-watts or less). Heat from soldering can cause problems (especially with certain types of semiconductor devices). Thus, to be sure, always use a heat-sink on the lead when soldering. Gripping the lead with long nose pliers between the solder connection and the case of the device makes a good heat-sink; or use a tool designed for such use.

SILICON OR GERMANIUM?

The quickest way to determine if a transistor is germanium or silicon type, is to check the normal emitter-base voltage drop. With NPN devices, if the base is approximately 0.25 volts positive with respect to the emitter, it is a germanium type. If the voltage is about 0.65 volts, it is a silicon type. For PNP devices, the voltage will be the same value, but opposite in polarity (0.25 volts for germanium and 0.65 for silicon).

OPERATING CONSIDERATIONS

Before replacing an original-equipment device with the recommended Archer Type:

(A) Compare the lead or terminal arrangement of the Archer replacement device with the lead or terminal arrangement of the original device. If these arrangements are different, and the original transistor is a "plug in" type, bend the leads of the ARCHER device so that the base, emitter and collector leads will mate with the original transistor leads. Trim the leads after soldering in place.

CAUTION: Be particularly careful about "pin-circle" and "in-line" lead break-out type transistors. Often one manufacturer makes a type with "in-line" leads, while another may make the same type with "pin-circle" configuration. Doublecheck both the original and the replacement device before soldering or plugging in transistors.

BOTTOM VIEW

PIN-CIRCLE

IN-LINE





(B) Certain considerations are involved whenever an original equipment transistor is replaced by one having a different type designation. When an ARCHER series transistor is used to replace an original equipment device in an untuned amplifier stage operating at a low signal level such as the untuned RF-amplifier (antenna) stage of a radio receiver, or a low-level AF amplifier stage, it is generally unnecessary to make any circuit adjustment to assure proper performance of the equipment. However, when a replacement is made in a turned RF amplifier stage, it is always advisable to check the alignment of the associated tuned circuits to assure proper tracking and to achieve the required gain without loss of stability.

(C) When replacements are made in stages operating at relatively high power levels, such as Class A and Class B AF output stages of automobile radio receivers, phonographs and AF-amplifier systems, the transistor bias should be checked and adjusted, if necessary, to protect the ARCHER replacement transistors against excessive dissipation and to minimize distortion. Means for making adjustments are generally provided in the equipment, and the necessary instructions are usually given in the equipment manufacturer's service data.

(D) When installing an ARCHER transistor as a substitute for an original equipment type in an FM tuner. TV tuner, or other circuits operating at frequencies in the VHF or UHF regions, it is extremely important not to change any of the lead lengths or position of the original circuit. Before removing the original transistor, carefully note its position with respect to other circuit components as well as the lengths and placement of the transistor leads, and duplicate these details as closely as possible with the ARCHER replacement transistor. Failure to observe this precaution can result in improper tuning or circuit instability. The same holds true for any replacement of Integrated Circuits, specially in FM radios and TV Receivers. Failure to

observe this precaution can result in damage in the device. Transistor substitution in tuned circuits will often require realignment of the circuit.

SILICON VS SELENIUM RECTIFIERS

Silicon rectifiers are inherently more efficient than selenium or other metallic-oxide type rectifiers. When a silicon rectifier is used to replace a selenium rectifier in the power supply of a typical line-operated radio or TV receiver, the silicon rectifier will frequently deliver higher DC output voltage than the original device.

In some cases, this higher supply voltage may improve the performance of the equipment. However, in many other cases, it may immediately or eventually damage filter capacitors and/or other components which were designed to withstand only the voltage delivered by the original selenium rectifier. To prevent such damage, it is generally advisable to insert a power type resistor in series with the silicon rectifier either on the input side, between the AC supply and the rectifier, or on the output side between the rectifier and the first filter capacitor. The value of this resistor will depend on the required reduction in the DC output voltage and on the DC load current of the equipment. This value may be determined experimentally or calculated from the equation:

$$R = \frac{E}{I}$$

where R is the required resistance in ohms. E the required reduction in DC output voltage in volts and I the DC load current in amperes.

The wattage rating of the resistor should be at least 2 X EI (in no case less than 10 watts).

SOLDERING PRECAUTIONS

Extreme care should always be used in making solder connections to semiconductors. Momentary application of excessive heat, or even prolonged application of a properly heated soldering tool to a semiconductor lead or terminal, can permanently damage the device. Observe the following precautions in soldering a semiconductor lead or terminal:

- 1. Solder as far as possible from the body of the semiconductor.
- 2. Never, apply heat or molten solder to a lead or terminal for longer than 10 seconds or at a point closer than 1/16 inch to the body of the device.
- 3. Use a low voltage iron (30 watts or less) specifically intended for use with transistors or miniature circuit components.
- 4. Keep the surfaces to be soldered clean and the tip of the soldering tool adequately tinned so that the connection can be made as quickly as possible.
- 5. Always use a heat sink on the lead when soldering. Gripping the lead or terminal with longnose pliers between the solder connection and case or body allows the pliers to act as a heat sink, conducting heat away from the internal elements of the device.

ABOUT CASE DIMENSIONS

In some instances, the case of an ARCHER Semi-

conductor may be slightly taller or thicker than that of the original device or have a slightly different shape, particularly if the original device is a foreign type not made to U.S.A. EIA (JEDEC) standards. These mechanical differences should not affect the performance of the equipment in which the replacement is made and normally will not prevent or complicate the installation of the ARCHER replacement device.

You should realize that cross-reference substitution listings are created based on electrical parameters (not necessarily on mechanical size or type). Thus, when you make substitutions based on our listings, check for physical/mechanical compatibility. If space is limited, it would be a good idea to check physical dimensions as well as electrical specs before making substitution.

GENERAL PRECAUTIONS

ARCHER transistor and ARCHER semiconductors should not be inserted or withdrawn from circuits with the power on, because transient currents may cause permanent damage to the device. In some cases ARCHER semiconductors are in metal cans and thus could possibly become shock hazards if they are allowed to operate at a voltage appreciably above or below ground potential.

For the most effective protection, a power transistor should be operated with an adequate heat sink and with the lowest value of resistance or impedance in the emitter-to-base circuit consistent with driving signal considerations. The transistor should be protected against extremely high collector voltage pulses which may be generated when the device is operated with inductive loads particularly when current transients are present.

When replacing a power transistor or rectifier which is attached to the equipment chassis, or to a special heat sink, observe the following precautions:

A. In the case of oxide coated metal washers or wafers, which are frequently used as electrical insulators between the cases of power transistors and the chassis or heat sink, it is important not to scratch, chip or otherwise damage the oxide surface.

B. When installing an ARCHER power transistor, where a mica or oxide coated metal washer was used to insulate the case of the original device electrically from the case, apply a thin coating of Heat Sink Compound (Radio Shack Number 276-1372) between the washer and the chassis or heat sink.

TESTING A TRANSISTOR

Before replacing a transistor you want to be sure it needs to be replaced. Always check the entire circuitry to be sure the transistor requires replacement.

The best method for checking transistors is to use a good transistor checker (dynamic in-circuit and out-of-circuit type). However, a sensitive VOM can give you a good indication of the quality of the device.

I. In-Circuit Testing

A. First, check to see if the emitter-base junction is

forward-biased. An NPN transistor should show the base 0.2 to 0.65 volts positive with respect to the emitter (approximately 0.25 volts for a germanium type and 0.6 volts for silicon). A PNP transistor should show the base 0.2 to 0.65 volts negative with respect to the emitter (0.25 volts for germanium and 0.6 volts for silicon).

B. Check to see if the device is functioning as an amplifier. Short the emitter-base junction to remove forward bias. Voltage at the collector lead should rise to approximately the potential of the collector supply buss line. Any difference is caused by ICES (collector-to-base leakage current). The closer the collector voltage approaches the buss line, the lower ICES is and the better the transistor.

II. Out-of-Circuit Testing

Again, for the best indication of transistor quality, use a good transistor checker. However, an ohmmeter can be used as described here.

Before using the ohmmeter, find out which polarity of the internal ohmmeter battery is connected to which test lead (not all ohmmeters have the + battery polarity connected to the red lead and the - battery polarity connected to the black lead). To determine the polarity of the leads when using the ohmmeter function, use an external voltmeter or study the schematic of your VOM.

Also, remember that in most transistor circuits you are dealing with low voltages and currents (in some cases, very low). Therefore, **NEVER** use RX1 scale (extensive currents can flow through a junction, permanently damaging the transistor). It is best to determine the maximum amount of current available in each resistance range before using an ohmmeter for testing semiconductor junctions.

After you have evaluated your VOM for the above and are sure you will not damage a transistor (with excessive current or voltage in any given ohmmeter range), proceed as follows:

- A. Small Signal PNP Germanium Transistors
 - 1. Connect the positive lead of your ohmmeter to the emitter. Connect the negative lead to the base. You should read 200-500 ohms.
 - 2. Connect the negative lead to the collector. You should read 10K-100K. Shorting collector base, the resistance should decrease.
- B. Small Signal NPN Germanium Transistors Reverse the polarity of the leads; the readings should be approximately the same.
- C. Power PNP Germanium Transistors
 - 1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 35-50 ohms.
 - Connect the negative lead to the collector The reading should be several hundred ohms. Shorting collector to base, the resistance should decrease.
- D. Power NPN Germanium Transistors Reverse the polarity of the leads; the reading should be approximately the same.

- E. Small Signal PNP Silicon Transistors
 - Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 1K-3K.
 - Connect the negative lead to the collector. The reading should be very high (may show as an "open").
- F. Small Signal NPN Silicon Transistors

Reverse the polarity of the leads; the readings should be approximately the same.

- G. Power PNP Silicon Transistors
 - 1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 200-1K.
 - 2. Connect the negative lead to the collector. The reading should be about 1 megohm or more.
- H. Power NPN Silicon Transistors

Reverse the polarity of the leads; the readings should be approximately the same.

The resistance readings noted above can only be approximate; as long as you obtain somewhat **proportionate** readings (emitter-base readings as compared to emitter-collector), you can safely assume the transistor is OK.

HANDLING OF INTEGRATED CIRCUITS

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to static electrical charges (even electrical charges that normally build up on the human body can cause damage). To avoid possible damage to the devices during handling, testing, or actual operation, the following procedures should be observed:

- 1. Except when being tested or in actual operation, the leads of devices should be in contact with a conductive material, to avoid build-up of static charge.
- 2. Soldering iron tips, tools, metal parts of fixtures and handling facilities should be grounded.
- 3. Transient voltages may cause permanent damage to the device if it is removed or inserted with the power on.
- 4. Do not apply signals to the input with the power supply off.
- 5. All unused input leads must be connected to either Vss or VDD (whichever is appropriate for the logic circuit involved).

DIODES AND RECTIFIERS

GENERAL PURPOSE DIODES RATINGS @ 25°C

Catalog Number	PIV (min) V	lf A	Ir (max) @ Vr μA	Vf (max) @ If V	Case Style
276-1101	50	1.000	10	1.6	DO41
276-1102	200	1.000	10	1.6	DO41
276-1103	400	1.000	10	1.6	DO41
276-1104	600	1.000	10	1.6	DO41
276-1114	1000	2.500	200	1.0	A1vm
276-1122	75	0.010	250nA	1.0	A1
276-1123	60	0.085	15	1.0	A1
276-1124	5	0.010	100nA	0.340	A4
276-1141	50	3.000	500	1.2	A3q
276-1143	200	3.000	500	1.2	A3q
276-1144	400	3.000	500	1.2	A3q

ZENER DIODES-1 Watt

Catalog Number	Vz Volts ±10%	lz @ mA	Zz @ lz ohms max	Case Style	
276-561	6.2	41	2	DO41	
276-562	9.1	25	7	DO41	
276-563	12.0	21	9	DO41	
276-564	15.0	17	14	DO41	
276-565	5.1	49	7	DO41	

BRIDGE RECTIFIERS

Catalog Number	PIV (min) V	If (max) A	Case Style
276-1146	50	4	M532a
276-1151	50	1.4	M548
276-1152	100	1.4	M548
276-1161	50	1	Y1
276-1171	100	4	M532a
276-1173	400	4	M532a
276-1180	50	6	M532a
276-1185	50	25	

BIPOLAR TRANSISTORS

Catalog Number	Direct Commercial Equivalent	Mat.	Appli.	Polarity	Power Diss. @25°C Free Air	f _T Typical MHz	V _{CBO}	V _{CEO}	V _{EBO}	l _c Max	l _s Max	h _{FE}	@V _{CE} V	@l _c mA	I _{CBO} at max V _{CB}	Case Style
276-2007	2N1305	G	S.	PNP	150mW	5	30	-	25	300mA	_	40	1	10	Α μ8	TO5
276-2009	MPS2222A	S	G.P.	NPN	500mW	300	75	40	6	800mA	_	50	10	1	10nA	TO92
276-2010	PN2484	S	u.	NPN	360mW	15	60	60	6	50mA		250	5	1	10nA	TO92
276-2016	MPS3904	S	S	NPN	350mW	300	60	40	6	200mA	_	100	10	1	50nA	TO92
276-2017	TIP31	S	P	NPN	40W‡	3	40	40	- 5	3A	1A	10-50	4	3A	300µA	TO220AB-2
276-2020	TIP3055	S	P	NPN	90W‡	3	100	70	7	15A	7A	20	4	4A	1mA	TO220
276-2023	MPS2907	S	S	PNP	400mW	200	60	40	- 6	600mA	-	50	10	1	20nA	TO92
276-2027	MJE34	S	Р	PNP	90W‡	3	40	40	5	10A	3 A	20-100	4	ЗА	220µA	TO220
276-2030	2N3053	8	P	NPN	1W	100	60	40	. 5	700mA	-	50	10	150	-	T05
276-2032	MPS3638	S	RF/IF	PNP	350mW	100	25	25	4	500mA	_	30	3	10	10nA	TO92
276-2041	2N3055	S	P	NPN	115W‡	2.5	100	60	7	15A	7A	50	4	1A	-	TOS
276-2043	MJ2955	S	P	PNP	150W‡	4	100	60	7	15A	7A	70	10	0.5		T03
276-2044	MRF901	S	UHF	NPN	300mW	2500	25	15	2	30mA	-	80	5	5	50nA	MACRO-X
276-2048	2SD313	S	P	NPN	30W‡	8	60	60	5	3 A		40-320	2	1	100µA	TO220
276-2051	28C945	S	G.P.	NPN	250mW	250	60	50	5	100mA	-	60-600	6	1	100nA	TO92J
276-2055	2SC1308	S	SW	NPN	50W‡		1400	400	6	7A	0.8A	3	2	4A	5mA	TO3
276-2058	2N4401	S	G.P.	NPN	350mW	250 min	40	60	6	600mA	-	500	10	1	0.1µA	TO92
276-2059	MPSA06	S	Р	NPN	625mW	100	80	80	4	500mA	-	50 min.	1	100	0.1μΑ	TO92
276-2060	MPSA13	8	P*	NPN	625mW	2	30	30	10	500mA	·	10,000	5	100	100nA	TO92
276-2061	MPSA42	S	G.P.	NPN	625mW	50	300	300	6	500mA	_	40 min.	10	30	0.1μΑ	TO92
276-2068	TIP120	S	P	NPN	65W‡	0.1	60	60	5	5A	120m/	2500	3	500	0.2mA	TO220AB-2

NOTE: All ratings given are for 25°C except where otherwise noted.

‡With heat sink.

MATERIAL:

S-Silicon: G-Germanium

APPLICATION:

S-Switch G.P.—General purpose P-Power amp/switch

RF/IF-RF/IF frequency

*-High Gain Darlington UHF-Ultrahigh frequency LL-Low Level SW-TV Sweep

SPECIAL TRANSISTORS (FET)



SILICON N-CHANNEL JUNCTION **FIELD EFFECT TRANSISTOR**

GENERAL DESCRIPTION

The MPF102 is designed for small signal applications. These include VHF amplifiers and mixers.

ABSOLUTE MAXIMUM RATINGS $(T_A = 25 \degree C \text{ unless otherwise noted})$

Drain-Source Voltage	1
Drain-Gate Voltage	-
Gate-Source Voltage	1
Gate Current10 mA	
Total Device Dissipation	1
Operating Junction Temperature	
Storage Temperature Range	,

PIN CONNECTION





N-CHANNEL LOW POWER HEXFET

IRFD1Z3 276-2073

GENERAL DESCRIPTION

This device combines automatic insertion efficiency, a 1 watt heat sink tab with the HEXFET high performance, quality, and reliability. These space saving HEXDIPs are end-stackable in rows of any length on 100 mil centers. The low profile N-Channel HEXDIPs can be used on boards for cages with 0.5" board spacing.

ABSOLUTE MAXIMUM RATINGS

Drain-to-Source Voltage, V _{DS} 60 ³	V
On-State Resistance, R _{DS(ON)}	Ω
Continuous Drain Current, ID (25°C Case)	A
Pulsed Drain Current, I _{DM}	A
Maximum Power Dissipation, Pp	

PIN CONNECTION



N-CHANNEL MOSFET TRANSISTOR

IRF511 276-2072

GENERAL DESCRIPTION

The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

This transistor also features all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

FEATURES

- Fast switching
- Low drive current
- Ease of paralleling
- No second breakdown
- · Excellent temperature stability

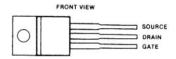
APPLICATIONS

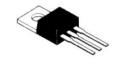
- Switching power supplies
- Motor controls
- Inverters
- Choppers
- Audio amplifiers
- · High energy pulse circuits

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage, V _{DS}
Drain-Gate Voltage ($R_{GS} = 1 M\Omega$), V_{DGR}
Gate-Source Voltage, V _{GS}
Continuous Drain Current, I _D @ T _C ≅ 86°C
Pulsed Drain Current, I _{DM}
Maximum Power Dissipation, PD
Linear Derating Factor
Inductive Current, Clamped, I_{LM} (See Fig. 1) $L = 100 \mu H \dots 8A$
Operating Temperature Range, T ₁
Storage Temperature Range, T _{stg} 55 to +150 °C

PIN CONNECTION





SPECIAL TRANSISTORS (FET)

IRF511 276-2072

TEST CIRCUITS

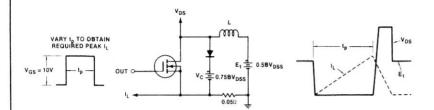


Figure 1—Clamped Inductive Test Circuit and Waveform

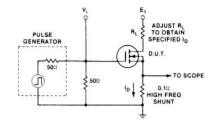
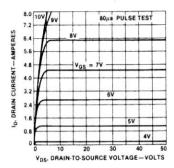
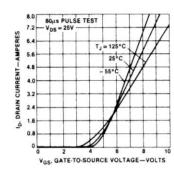


Figure 2—Switching Time Test Circuit

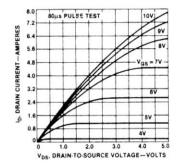
TYPICAL CHARACTERISTICS



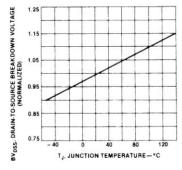
Output Characteristics



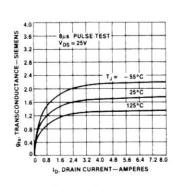
Transfer Characteristics



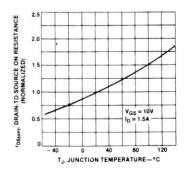
Saturation Characteristics



Breakdown Voltage vs Temperature



Transconductance vs Drain Current



Normalized On-Resistance vs Temperature

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR



GENERAL DESCRIPTION

The 2N3819 is designed for general purpose small-signal applications. It features low capacitance between drain and gate terminals and an excellent high-frequency figure of merit. It achieves a low noise figure and good power gain with low crossmodulation and intermodulation.

ABSOLUTE MAXIMUM RATING $(T_A = 25^{\circ}C \text{ unless otherwise noted})$

A A A A A A A A A A A A A A A A A A A
Gate-Source Breakdown Voltage BV _{GSS} – 40 V
Zero Gate Voltage Drain Current I _{DSS}
Forward Transconductance gfs
Reverse Gate Leakage I _{GSS}
"ON" Resistance r _{DS}
Pinch Off Voltage V _{GS(OFF)} 6.0 V
Output Conductance g _{os}
Feedback Capacitance C _{rss}
Input Capacitance C _{iss}
Power Gain G _{PS}
Power Dissipation

PIN CONNECTION

BOTTOM VIEW

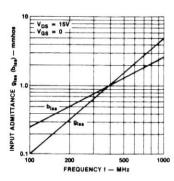


T092

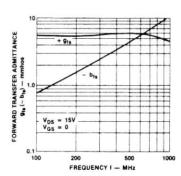


TYPICAL CHARACTERISTICS

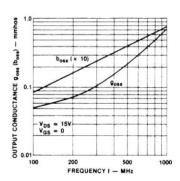
COMMON SOURCE



Input Admittance vs Frequency

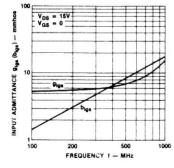


Forward Transfer Admittance vs Frequency

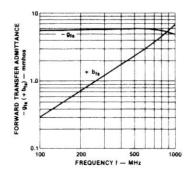


Output Conductance vs Frequency

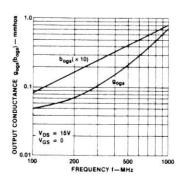
COMMON GATE



Input Admittance vs Frequency



Forward Transfer Admittance vs Frequency

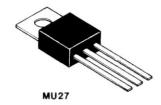


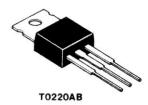
Output Conductance vs Frequency

SPECIAL PURPOSE DEVICES (SCR) (TRIAC) (VARISTOR)

276-1000 276-1001 276-1020 276-1067

THYRISTORS





GENERAL DESCRIPTION

Thyristors and their trigger devices can take numerous forms, but they share these characteristics:

- They are "open circuits," capable of withstanding rated voltage until triggered.
- They become low-impedance current paths when triggered, and remain so, even after the trigger source is removed, until current through that path stops, or is reduced below a minimum "holding" level.

SCRs

Silicon-Controlled Rectifiers (SCRs) are Thyristors intended to switch load currents in one direction only, making them useful for DC and half-wave AC applications as well as full-wave applications, in which bidirectional current is routed in one direction through the SCR via a bridge rectifier.

Catalog Number	lmax A	Vmax V	I _{GT} (max) mA	V _{GT} (max) V	Case Style	
276-1067	6	200	25	1.5	MU27	
276-1020	6	400	25	1.5	MU27	

TRIACs

Triacs are bidirectional Thyristors. in which a single trigger source turns the device on for load current in either direction. Because they do not require a bridge rectifier in order to handle full-wave AC. Triacs are useful in AC power applications that require full source power control capability to be applied to the load.

Catalog Number	lmax A	Vmax V	I _{GT} (max) mA	V _{GT} (max) V	Case Style
276-1001	6	200	50	2.5	TO220AB
276-1000	6	400	50	2.5	MU27

V130LA1 276-571

METAL OXIDE VARISTOR

GENERAL DESCRIPTION

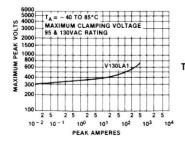
This is a metal oxide varistor and the end of lifetime for the device is defined as a degradation failure which occurs when the device exhibits a shift in the Varistor Voltage at one (1) milliampere exceeding \pm (10% + 1V) of the initial value. This type of failure is normally a result of a decreasing V-I value, but does not prevent the device from continuing to function. However, the device will no longer meet the original specifications.

ABSOLUTE MAXIMUM RATINGS

Voltage (DC) Continuous	175 V
Voltage (RMS) Continuous	130 V
Energy (W _{TM} Joules (10/1000 μs) Transient	$7 W_{TM}$
Peak Current (I _{TM}) Amperes (8/20 µs) Transient	800 A

TYPICAL CHARACTERISTICS

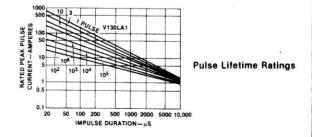
Varistor Voltage (@ 1 mA DC Test Current)	255 V
Maximum Clamping Voltage (V _C @ Test Current) (8/20 μs)	390 V _C
	10 A _{IP}
Typical Capacitance ($f = 0.1 \text{ To } 1 \text{ MHz}$)	180 pF



Transient V-1 Characteristics

PIN CONNECTION





METAL OXIDE VARISTOR

SNR-20A130K 276-568 SNR-14A130K 276-570

GENERAL DESCRIPTION

SNR Varistors for transient voltage suppression are metal oxide devices with industry standard. Their impedance is a nonlinear inverse function of applied voltage. At rated voltage their impedance is high. When a higher voltage transient appears across the varistor, its impedance sharply decreases to a low value. This transient voltage is clamped to a safe level and the energy in the transient is dissipated in the varistor. Characteristics are bi-directional.

ABSOLUTE MAXIMUM RATING

Varistor Voltage (V-I @ 1mA DC) (184V ~ 225V)
Applied Voltage (AC _{RMS})
(DC)
Energy (J) (276-568)
(276-570)
Power (276-568)
(276-570)
Capacitance (PF @ 1 MHz) (276-568)
(276-570)
Peak Pulse Current (8 X 20 μs) 2 Times (276-568)
(276-570)
Storage Temperature40° +125°C
Operating Ambient Temperature

CHARACTERISTICS

MAXIMUM APPLIED VOLTAGE

The maximum RMS of commercial line voltage or sine wave, or the maximum DC voltage which can be applied to the device continuously.

ENERGY

The maximum allowable energy for a single square wave of 2 ms. Its ratings are based on a shift of VARISTOR VOLTAGE of less than $\pm 10\%$ of initial value.

AVERAGE POWER DISSIPATION

The maximum value of average pulse power dissipation for repetitive surge current.

VARISTOR VOLTAGE

The varistor terminal voltage which will be measured with 1mA DC applied.

STANDARD IMPULSE CURRENT WAVEFORM

The impulse of $8x20\mu s$ current waveform is applied as standard impulse current when PEAK PULSE CURRENT and VOLT-AMPERE CHARACTERISTICS are measured.

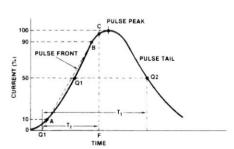
PEAK PULSE CURRENT

The maximum allowable pulse current for 2 impulses of $8x20\mu s$ current waveform with 5 minutes interval. Its ratings are based on a shift of VARISTOR VOLTAGE of less than $\pm 10\%$ of initial value. When impulses are applied more than 2 times the current should be reduced.

PIN CONNECTION



TYPICAL CHARACTERISTICS



 $\begin{array}{lll} T_t & : \mbox{ Virtual time of pulse front } \\ T_t & : \mbox{ Virtual time of pulse tail } \\ 0.1 & : \mbox{ Virtual origin } \\ 0.1 & 0.2 & : \mbox{ Hall points of pulse peak } \\ CF & : \mbox{ Value of pulse peak } \\ \mbox{ Impulse current waveform is conventionally expressed by $T_1 \times T_{LMS}$} \\ \end{array}$

SPECIAL PURPOSE DEVICES (VARISTOR)

SNR-20A130K 276-568 SNR-14A130K 276-570

CHARACTERISTICS (Cont'd)

VOLTAGE-TEMPERATURE COEFFICIENT

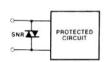
The shift of varistor voltage at ambient temperature between 20°C and 70°C is expressed by $\sqrt{(\%/^{\circ}C)}$

$$\sqrt{(\%^{\circ}C)} = \frac{V_{1}mA (at 70^{\circ}C) - V_{1}mA (at 20^{\circ}C)}{V_{1}mA (at 20^{\circ}C)} \times \frac{1}{50} \times 100$$

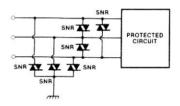
MAXIMUM CLAMPING VOLTAGE

The maximum voltage that will appear across the varistor when an 8X20us current pulse in the current range indicated is applied to the varistor.

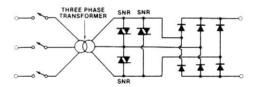
TYPICAL APPLICATIONS



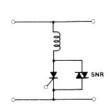
Single Phase Line Surge



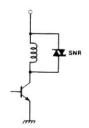
Three Phase Line Surge



Transformer Inductive Surge by Primary Switch Off



Solenoid Inductive Surge by Thyristor Switching



Solenoid Inductive Surge by Transistor Switching

OPTOELECTRONIC (LED) LED INDICATORS

Catalog Number	Direct Commercial Equivalent	Peak Wave Length nM	Color	Forward Voltage V _F (V)	Reverse Voltage V _R (V)	Max DC Forward Current I _F (MA)	Max Pwr Diss P _D (MW)	Fig. No.
276-018	PR5534S	700	RED	2.5	4	100	75	5
276-021	SLP-236B	565	YELLOW	2.8	3	30	70	6
276-022	SLP-236B	565	GREEN	2.8	3	30	70	6
276-025	R9-56	_	RED/GREEN	2.0	3.0	10		8
276-026		650	RED		3	50	100	3
276-033	TLR-147	700	RED	2.1	4	35	100	2
276-037	SLP-235B	565	GREEN	2.8	3	30	70	5
276-041		700	RED	1.75	3	70	140	4
276-068	_	700	RED	1.9	_	30		7
276-069	- ,	560	GREEN	2.1	_	30		7
276-070	SEL-1120R	700	RED	2.5	3	30		1
276-073	W		YELLOW	2.1	_	30	_	7

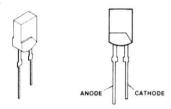


FIGURE 1

Miniature LED with diffused lens. Its features include high brightness—ideal for bar graph display—can be arranged horizontally or vertically.





FIGURE 2

Miniature LED with diffused lens. This LED is compatible with most TTL and transistor circuits. It features a Fresnel lens design.





FIGURE 3

This LED features a frosted diffused lens in a plastic encapsulant. When the device is on, it appears as a large, soft light source, making it ideally suited for front panel applications.



FIGURE 4

This device is a jumbo LED with a diffused lens. It can be used in applications such as pilot and indicator lamps.

CATHODE





FIGURE 5

Subminiature LED with diffused lens. This device has solid state reliability and is compatible with most TTL and transistor circuits.



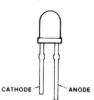


FIGURE 6

This is a frame type solid state LED with a diffused lens.



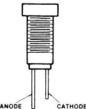
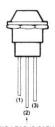


FIGURE 7

This is a subminiature LED indicator with polished chrome reflective holder.



IGURE 8

This is a three terminal LED. The light color radiates "red" when terminals 2 and 3 are used. Green light radiates when terminals 1 and 2 are used.



BLINKING LED

GENERAL DESCRIPTION

Blinking Frequency

In all types of blinking LEDs the blinking frequency with a supply voltage of 5 V and a temperature of 25°C is typically about 3 Hz, varying between 1.3 and 5.2 Hz. It can be measured using a photodiode mounted on the lens of the diode being measured and connected to the high resistance input of a frequency meter. When the measurements are to be made in a temperature enclosure, of course, it is simpler to introduce a small measuring resistance in the supply lead and to take the signal for the counter from this.

Dependence on Supply Voltage

Throughout the range of supply voltage from 4.75 to 7.0 V, the blinking frequency increases with voltage on average of 0.5 Hz, that is at the rate of about 0.2 Hz/V or 7%/V (See Fig. 1). In individual cases the frequency may even remain constant, in others it may increase by more than 1 Hz/V (see the limits of scatter)

If the supply voltage goes below the lower limit of 4.75 V, the oscillator can no longer be relied upon to commence oscillation, especially at low temperatures. This is why when the supply voltage rises slowly the point of commencement of blinking is higher than when switched on normally.

Effect of a Series Resistance

The current through a blinking LED swings back and forth between typically 20 mA in the ON-state and about 0.9 mA in the OFF-state. This circumstance must be kept in mind if it is intended to connect a resistance in series with the diode, whether this is to drive it at a voltage higher than 7 V or to be able to derive an electrical signal. The fluctuating current causes a fluctuating voltage drop across the resistor and thereby a varying voltage on the blinking LED. The frequency and duty cycle of the blinking are both affected by this. It must be ensured that the actual supply voltage does not fall below the minimum level of 4.75 V otherwise there is a possibility that the AFI-circuit of the IC may come into operation.

Fig. 2 shows the blinking frequency as a function of the series resistance. As the value of resistance R_s was increased, so was that of the supply voltage, so as to keep the diode voltage in the ON-state at 5 V and thus also to maintain the current constant. The supply voltage to the circuit can be calculated as $\frac{1}{2} \sum_{i=1}^{n} \frac{1}{2} \sum_{i=1}^{n} \frac{1}{2}$

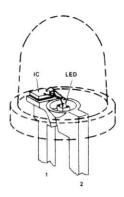
$$V_s = 5 V + (20 \text{ mA} \bullet R_s/k\Omega)$$

Blinking-on Voltage

By "blinking-on voltage" is meant that supply voltage to the blinking LED at which the transition from continuous to blinking emission occurs. With a slowly rising supply voltage this voltage threshold is higher than with a quickly rising one, such as occurs when the blinking LED is inserted into a socket with an already established voltage. The minimum supply voltage of 4.75 V quoted in the data sheet was chosen to ensure reliable commencement of oscillation of the blinking LED at the lowest permissible temperature of -40C and with a slowly-rising supply voltage. The component is not guaranteed to function correctly when operated with a supply voltage below this limit.

The actual blinking-on voltage for slowly-rising voltage supply at 25°C is typically 3.3 V, varying about 2.3 and 4.3 V. The blinking-on voltage is also temperature-dependent, falling with increasing temperature (Fig. 4). A typical blinking LED with a blinking-on voltage of about 3.3 V at 25°C needs about 3.45 V at 40°C and 3.2 V at +70°C. The temperature-coefficient of the blinking-on voltage is thus about -2.3 mV/K or -0.07%/K.

PIN CONNECTION



TYPICAL CHARACTERISTICS

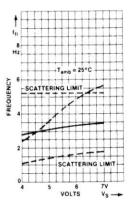


Figure 1

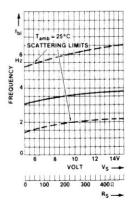


Figure 2

CQX21 276-036B

Blinking-on Voltage (Cont'd)

TYPICAL CHARACTERISTICS (Cont'd)

If the supply voltage of an already blinking LED is slowly reduced, at a certain level the opposite transition from blinking to steady light occurs. This "blinking-off voltage" is from 0.1 V to almost 1 V lower than the blinking-on voltage for slowly rising supply. Blinking starts again at this same voltage if the rise is sudden, as when plugged into a socket. In the transition region, an irregular flickering may occasionally be observed.

Dependence on Supply Voltage

The duty cycle or ON/OFF ratio for all types of blinking LEDs at 5 V is almost exactly 1:1, or otherwise expressed: pulse-duration/period $t_p/T=0.5$. According to the data sheet a tolerance bandwidth from 0.33 to 0.67 must be allowed for, but this, however, is required for only a few individual cases.

As shown by Fig. 5, the duty cycle ratio rises only gradually with increasing supply voltage, on the average between 0.51 and 0.53 at 7 V. In some individual example the ratio is higher at low voltages, falling with increasing voltage (see scatter limit curves).

Effect of Series Resistance

The duty cycle ratio is more strongly affected by resistance than the blinking frequency. From Fig. 6 it can be seen that the ratio, with a supply voltage between 5 and 15 V, increases typically from 0.50 to 0.61 as the resistance increases from 0 to 500Ω . The limit curves show an even greater increase, which means that in individual cases the lengthening of the light phase and shortening of the dark is clearly visible.

The reason for this increase is the characteristic of blinking LEDs described in the section called Dependence on Supply Voltage, namely that with increasing supply voltage the frequency also increases, i.e. both light and dark phases become shorter. With resistance connected in series the voltage in the ON-state is lower, i.e. the light phase becomes longer. In the OFF-state the voltage increases, i.e. the dark phase becomes shorter. Lengthening of the light phase and shortening of the dark, however, means that the duty cycle ratio (= light phase/period) increases with increasing resistance and voltage.

Dependence on Temperature

Of all the parameters of blinking LEDs the duty cycle ratio is the least affected by temperature. The temperature-coefficient of duty cycle can actually be determined only by instrumental measurement (Fig. 7). In a typical blinking LED with a duty cycle ratio of 0.5 at 5 V and 25 °C, the value increase from about 0.497 o 0.502 in the temperature range from -40 to +70 °C, i.e. overall by 0.01%K.

Table 1 gives a review of all temperature-coefficients of the CQX21.

Parameter	Temp.Coef.in%/K
Current, ON-state	-0.35
Current, OFF-state	-0.38
Light intensity	-1.01.8
Blinking frequency	-0.40
BLinking-on voltage	-0.07
Duty cycle	+0.01

Table 1: Temperature-Coefficients of blinking LEDs

As Fig. 3 shows, the blinking frequency falls with increasing temperature. A typical blinking LED with a frequency of 3.0 Hz at 5 V and 25°C blinks at -40°C with a frequency of about 3.8 Hz and at +70°C of 2.5 Hz. In the region around 25°C the temperature-coefficient of frequency is about 0.012 Hz/K or -0.40%/K.

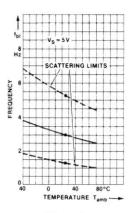


Figure 3

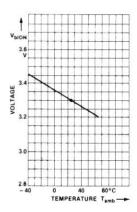


Figure 4

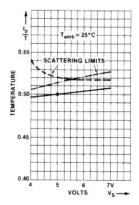


Figure 5

OPTOELECTRONIC (LED)

CQX21 276-036B

TYPICAL CHARACTERISTICS (Cont'd)

TYPICAL APPLICATION	MEANING OF THE BLINKING SIGNAL
Domestic apparatus	
Electric drill	Motor overloaded
Steam iron	Distilled water needed
Ventilating-fan hood	Change filter
Electric oven	Hot-plate overheated
Gas oven	Gas flame extinguished
Freezer	Internal temperature too high
Hand mixer	Motor overloaded
Coffee percolator	Water compartment empty
Coffee grinder	Hopper empty
Oil-fired central heating	Fault
Vacuum cleaner	Bag too full
Telephone	Extension in use
Auto	
Light system	Bulb out of order
Petrol gauge	Tank almost empty
	(continuous light-refill immediately)
Theft alarm	Set out of operation
Hand-brake	Brake applied
Cooling system gauge	Motor overheated
Oil pressure	Oil level too low
Safety belt	Not engaged
Throttle (choke)	Out
Radio/Audio/Television/Video	
TV-receiver	Remote-control unit operating
Cassette-recorder	Tape jammed or at the end
	Ready to record
	continuous light—recording in progress
UHF-HiFi-receiver	Interference due to multi-channel reception
Electronic Instrument	
Functional check	Fault in apparatus or incorrect operation
Calibration	Re-calibration needed
Data-handing	
Computer	Loss of data due to short-term mains break
Printer	No paper
Machines	TTO Pupor
Work-piece	Jammed or in wrong position
Adjustment	Machine incorrectly adjusted
Monitoring	Danger of overheating
	Danger of overneating
Others	Ditii
Buildings	Direction signs

Table 2: Application Examples for Blinking LEDs

ABSOLUTE MAXIMUM RATING

Supply Voltage (V _S) 7 V
ON-State Forward Current (I _F)
Thermal Resistance, Junction Ambient (Z _{THP})
Power Dissipation (V _S ● I _F)
Junction Temperature (T _I)100°C
Ambient Temperature (T _{Amb})70°C
Wavelength (RED) (Ga As on Ga AS)

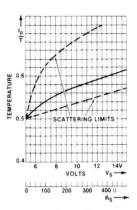


Figure 6

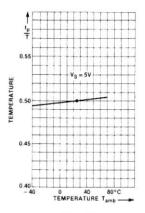
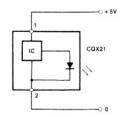
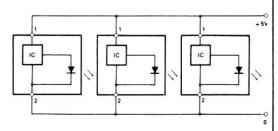


Figure 7

TYPICAL APPLICATION





P-N GALLIUM ALUMINUM ARSENIDE INFRARED- EMITTING DIODE

TIL906-1

GENERAL DESCRIPTION

This is a P-N Gallium Aluminum Arsenide Infrared-Emitting diode designed to emit near infrared radiation when forward biased. Its output is spectrally compatible with silicon sensors and has a high power output with a 20° beam angle.

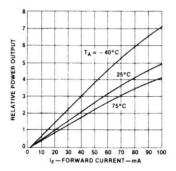
ABSOLUTE MAXIMUM RATINGS

Forward Voltage (Static) (VF)
Reverse Voltage (VA)
Continuous Forward Current at (Or Below)
25°C Free-Air Temperature
Peak Forward Current (See Note 1)
Reverse Current ($V_R = 3 V$)
Radiant Power Output (Po) (IF = 20 mA)
Emission Beam Angle Between
Half-Intensity Points20°
Wave Length at Peak Emission (IF = 20 mA)880 nM
Operating Temperature Range40°C To 80°C
Storage Temperature Range40°C to 100°C
NOTE: 1. This value applies for $t_w \le 10 \mu s$, $f \le 1 kHz$. See Figure 1.

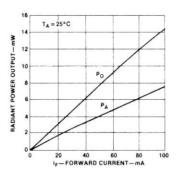
FEATURES

- High power output With a 20° beam angle
- · Output spectrally compatible with silicon sensors

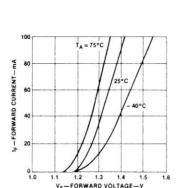
TYPICAL CHARACTERISTICS



Relative Power Output vs Forward Current



Radiant Power Output vs Forward Current

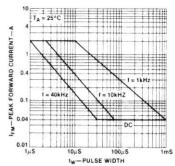


Forward Conduction Characteristics

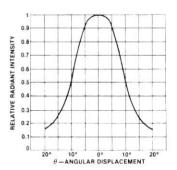
PIN CONNECTION







Peak Forward Current vs Pulse Width Figure 1



Relative Radiant Intensity vs Angular Displacement



OPTOCOUPLER TRIAC DRIVER



GENERAL DESCRIPTION

This device consists of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch and is designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 V peak), high detector standoff voltage, small size, and low cost.

INFRARED EMITTING DIODE MAXIMUM RATINGS

Reverse Voltage 3.0 volts	
Forward Current—Continuous 50 mA	
Total Power Dissipation @ TA = 25°C	

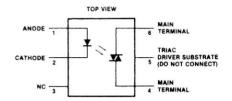
OUTPUT DRIVER MAXIMUM RATINGS

Off-State Output Terminal Voltage	250 Volts
On-State RMS Current TA = 25°C	100 mA
(Full Cycle, 50 to 60 Hz TA = 70°C)	50 mA
Peak Nonrepetive Surge Current	1.2 A
(PW = 10ms. DC = 10%)	
Total Power Dissipation @ TA = 25°C	300 mW
Derate above 25°C	

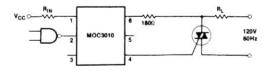
TOTAL DEVICE MAXIMUM RATINGS

Isolation Surge Voltage (1s)
(Peak ac Voltage. 60 Hz. 5 Second Duration)
Total Power Dissipation
Junction Temperature Range40 to +100°C
Ambient Operating Temperature Range40 to +70°C
Storage Temperature Range40 to +150°C
Soldering Temperature (10s)

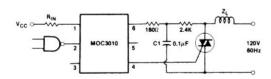
PIN CONNECTION



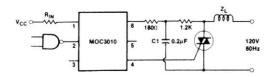
APPLICATIONS



Resistive Load

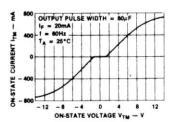


Inductive Load with Sensitive Gate Triac (I_{GT} \leqslant 15mA)

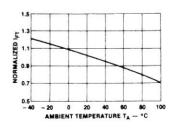


Inductive Load with Non-Sensitive Gate Triac (15mA < I_{GT} < 50mA)

TYPICAL CHARACTERISTICS



On-State Current vs On-State Voltage



Trigger Current vs Temperature



HIGH EFFICIENCY RED BAR GRAPH DISPLAY

MV57164

GENERAL DESCRIPTION

The MV57164 is a 10 segment bar graph display with separate anodes and cathodes for each light segment. The packages are end stackable.

FEATURES

- · Large segments, closely spaced
- End stackable
- Fast switching, excellent for multiplexing
- Low power consumption
- · Directly compatible with IC's
- · Wide viewing angle
- Standard .3" DIP leading spacing

ABSOLUTE MAXIMUM RATINGS

(25°C Free Air Temperature Unless Otherwise Specified)

Power dissipation750mW	
Continuous forward current	
Total	
Per segment 30 mA	
Reverse voltage	
Per segment6.0 V	
Storage and operating temperature40 to +85°C	,
Solder time 5 sec	

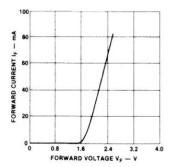
TYPICAL THERMAL CHARACTERISTICS

Thermal resistance junction to free air Φ JA	160° C/W
Wavelength temperature coefficient (case temp)	
Forward voltage temperature coefficient = 2	2.0 mV/°C

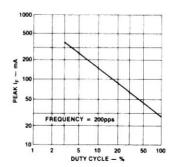
ELECTRO-OPTICAL CHARACTERISTICS

Forward Voltage. 2.5 V Peak emission wavelength. 630nr Spectral line half width 40nr Dynamic resistance	n
Segment	F
Switching Time 400 n Reverse Voltage 6.0 V	

TYPICAL CHARACTERISTICS

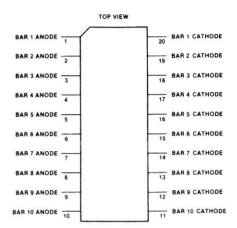


Forward Current vs Forward Voltage

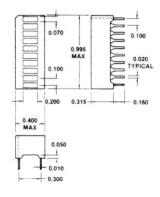


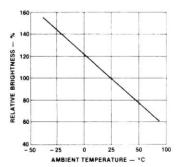
Luminous Intensity vs Forward Current

PIN CONNECTION



DIMENSIONAL DIAGRAM



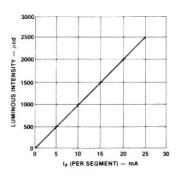


Luminous Intensity vs Ambient Temperature

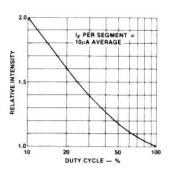
OPTOELECTRONIC (DISPLAY)

MV57164 276-081

TYPICAL CHARACTERISTICS (Cont'd)



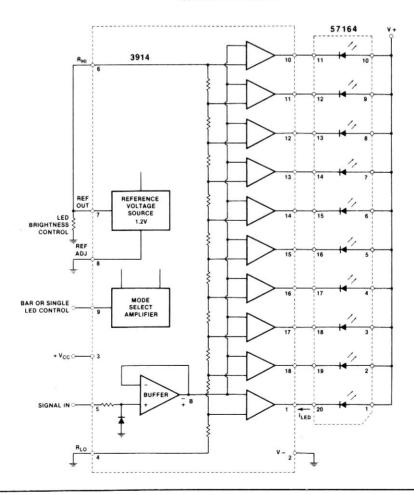
Maximum Peak Current vs Duty Cycle



Luminous Intensity vs Duty Cycle

TYPICAL APPLICATION

Typical Drive Circuit





COMMON CATHODE DISPLAY

MAN74 276-075

GENERAL DESCRIPTION

This is a red .3 inch common cathode RHDP Display device with a brightness or luminous intensity (Per Seq. MIN) of 125 μ cd @ 10mA.

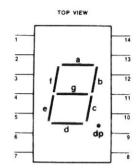
APPLICATIONS

- Instruments
- Test Equipment
- Office Machines
- Computers
- Automobiles
- Clocks/Radios
- Communication Equipment
- Calculators
- CB Radios

ABSOLUTE MAXIMUM RATINGS

Forward Voltage 2 V
Forward Current
Power (P _D)
Wave Length660 nM
Brightness/Luminous Intensity @ 10mA 125 μcd

PIN CONNECTION



OPTOELECTRONIC INDEX BY FUNCTION

FUNCTION	CATALOG NO.	PAGE NO.
DISPLAY	276-053	22
	276-075	21
	276-081	19, 20
DRIVER	276-134	18
EMITTER	276-142	24
	276-143	17
LED (Blinking)	276-036B	14-16
LED (Tri-color)	276-035	23
LED INDICATORS	276-018	13
(Chart)	276-021	13
	276-022	13
	276-025	13
	276-026	13
	276-033	13
	276-037	13
	276-041	13
	276-068	13
	276-069	13
	276-070	13
	276-073	13
PHOTOCELL	276-116	22
PHOTOTRANSISTOR	276-145	23
SOLARCELL	276-124	24

276-053

0.3" SOLID STATE SEVEN SEGMENT DISPLAY



GENERAL DESCRIPTION

The 276-053 is a common anode LED numeric display. The large 0.3" high character size generates a bright continuously uniform 7 segment display. Designed for viewing distances of up to 10 feet, this single digit display has been human engineered to provide a high contrast ratio and wide viewing angle.

FEATURES

- Fits 14 pin DIP socket
- Excellent character appearance—continuous uniform segments; wide viewing angle; high contrast
- IC compatible 1.6 V per segment
- Standard 0.3" DIP lead configuration; PC board or standard socket mountable
- · Both left and right decimal points

APPLICATIONS

- Electronic calculators
- · Frequency counters

TVs

· Digital clocks

Radios

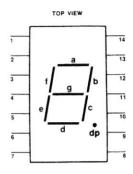
RADIANT CHARACTERISTICS (IF=20mA) $T_A=25$ °C

Luminous Intensity	 	 	250 mcd
Wavelength (Peak)	 	 	655 nM

ABSOLUTE MAXIMUM RATINGS

Power Dissipation T _A =25°C400	0 mW
Average Forward Current/Segment or Decimal Pt. T _A =25°C	5 mA
Peak Forward Current/Segment or Decimal Pt. T _A =12°C	
(Pulse Duration 500 \(\mu \) s)	0 mA
Reverse Voltage per Segment or Decimal Pt	. 6 V
Operating Temperature Range	-85°C
Storage Temperature Range	-85°C
Max Solder Temperature 1/16" Below Seating Plane (t ≤ 5 sec.)	230°C
Max Solder Temperature 1/10 Below Seating 1 and (1	

PIN CONNECTION



COMMON ANODE

PIN	FUNCTION
1	CATHODE a
2	CATHODE f
3	ANODE
4	NO PIN
5	NO PIN
6	CATHODE dp
7	CATHODE e
8	CATHODE d
9	NO CONNECTION
10	CATHODE c
11	CATHODE q
12	NO PIN
13	CATHODE b
14	ANODE

CONNECTIO

PIN	FUNCTION		
1	NO PIN		
2	ANODE		
3	CATHODE-I		
4	CATHODE-q		
5	CATHODE-e		
6	CATHODE-d		
7	NO PIN		
8	NO PIN		
9	ANODE		
10	CATHODE-dp		
11	CATHODE-c		
12	CATHODE-b		
13	CATHODE-a		
14	NO PIN		

276-116

CADMIUM SULPHIDE PHOTOCELL

GENERAL DESCRIPTION

A cadmium sulphide photo cell is a light variable resistor which is most sensitive in the green to yellow portion of the light spectrum. With it you can use light to control many electronic devices. Max. resistance .5 meg., min. resistance 100 ohms, max. voltage 170 V, max. wattage .2 watts. rugged epoxy case.

APPLICATIONS

- Night light
- Light control
- Burglar alarm
- Relay

SPECIFICATIONS

•	ShapeRound
•	Sensitive Area
•	• Weight
•	Resistance at 1 Ftc (2870°K)
•	Typical Resistance 100 Ftc (2870°K)
	Resistance Dark Minimum (1 Minute)

ABSOLUTE MAXIMUM RATINGS

Max. Applied Voltage (ac or dc)	170 V peak
Max. Power Dissipation at 25°C	2 watts
Power DeratingLinearly t	o 0 @ 75°C
Operating Temp. Range	0 to +75°C

CONNECTIONS





TRI-COLOR LIGHT EMITTING DIODE

XC-5491 276-035

GENERAL DESCRIPTION

The XC-5491 tri-state LED provides red, green, and yellow emission in the same package. This LED is a popular .200 diameter, two-leaded package containing a red and green LED chip in inverse parallel. By reversing the polarity of the applied current, the LED will emit red or green light while an AC voltage results in yellow light. The chips used in the XC-5491 are brightness matched so that the light output is uniform. This eliminates the necessity for the special drive circuits previously required with tri-state lamps.

These lamps provide the designer with the capability of efficiently displaying three functions with one indicator. This reduces the number of front panel indicators and simplifies design.

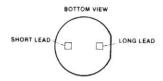
FEATURES

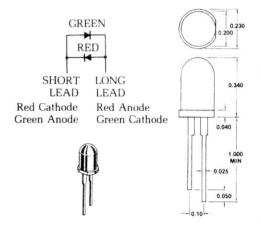
- 3 States—red, green, and vellow
- Equal brightness in all three colors
- Popular T 1¼ size package
- Wire wrappable leads

ABSOLUTE MAXIMUM RATINGS

Forward Current	nΑ
Peak Reverse Voltage	5V
Power Dissipation	
Operating Temperature Range55 to +85	5°C
Lead Solder Temperature	O°C

PIN CONNECTION





INFRARED PHOTOTRANSISTOR

TIL414 276-145

GENERAL DESCRIPTION

The TIL414 is an NPN silicon phototransistor in A T-1 3/4 style case. It provides high speed and high photosensitivity, suitable for IR switching applications.

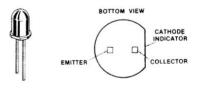
ABSOLUTE MAXIMUM RATINGS

Collector-Emitter Voltage 50	V
Emitter-Collector Voltage	V
Power Dissipation	
Operating Temperature	°C

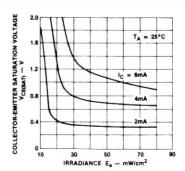
ELECTRICAL CHARACTERISTICS (Typical)

Dark Current ($V_{CE} = 30 \text{ V}$)	. 25 nA
Light Current $(V_{CE} = 5 \text{ V} \bullet E_e = 20 \text{mW/cm}^2) \dots$. 7 mA
Collector-Emitter Saturation	. 0.4 V
Rise Time	
Fall Time	6 μs

PIN CONNECTION



TYPICAL CHARACTERISTICS



Collector-Emitter Saturation Voltage vs Irradiance

276-142 INFRARED EMITTER AND DETECTOR

GENERAL DESCRIPTION

The 276-142 is a pair consisting of an infrared photodetector and an infraredemitting diode. The diode is capable of emitting radiant energy in the infrared region of the spectrum.

FEATURES

- · Spectrally and mechanically matched
- High power efficiency . . . typically 5 percent at 25°C

ABSOLUTE MAXIMUM RATINGS

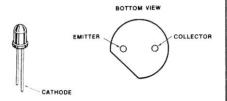
Photodetector

Collector-Emitter Voltage	0V
Collector Current	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature 50m	W
Operating Free-Air Temperature Range40 to +80	$^{\circ}C$
Storage Temperature Range40 to +85	$^{\circ}C$
Lead Temperature 1/16 Inch from Case for 5 Seconds	

Infrared-Emitting Diode

Reverse Voltage	2V
Continuous Forward Current	
Radiant Power Output	W
Wavelength at Peak Emission	

PIN CONNECTION



GRAPHIC SYMBOL



276-124

2.5×5cm SILICON SOLAR CELL

GENERAL DESCRIPTION

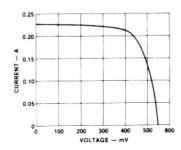
A solar cell is a silicon semiconductor device which converts light energy directly to electricity. A typical $2.5 \times 5 \mathrm{cm}$ cell will produce 0.42 volt and up to .18 amp of usable current. The power generated is affected by the load resistance (circuit powered by cell) strength of sunlight and temperature.

Be extremely careful when soldering leads. Use only a very fine wire (#26 or thinner) and use a small soldering iron (less than 50 watts). Solar cells may be connected in series to produce more voltage and in parallel for more current.

ABSOLUTE MAXIMUM RATINGS

	(Open Circuit):	
Current	(short circuit):0).2A
(Test co	nditions: Full sunlight at noon on a clear day at 25°C (76°F))	

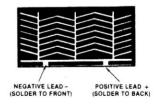
TYPICAL CHARACTERISTICS



Current vs Voltage

CONNECTIONS

FRONT VIEW





RING DETECTOR/DRIVER

TCM1512A 276-1302

GENERAL DESCRIPTION

The TCM1512A integrated circuit is designed for use as an alerting device in the line powered telephone. The IC (with a minimum of external components) is powered and activated by the telephone line's AC "ring" voltage to generate a signal suitable for driving piezo-electric "sound disc" transducers. In a typical telephone application this AC ring voltage can vary from 40 to 150 $V_{\rm RMS}$ over a frequency range of 14 to 68 Hz. The output signal is a square wave alternating between two frequencies in a ratio 1.14:1; and with the average of these two frequencies set at 1250 Hz, a "warble" rate or shift rate of approximately 10 Hz.

During standby (prior to activation) the ringer presents an impedance of 100K or greater to prevent any interference with parallel "offhook" telephones transmitting DTMF or voice frequencies. The IC is designed to handle lightning strikes on the line of 1500 V, 200 μ sec duration. In addition, dial pulses from parallel phones are ignored so a false ringing of the bell (tapping) won't occur.

FEATURES

- On-chip full-wave rectifier
- · High standby impedance
- Built-in lightning protection circuitry
- Built-in anti-"tapping" circuitry
- Built-in regulators
- Built-in static protection
- 0.8 through 2 kHz output frequency range
- Low external component count
- Push-pull drive of piezo transducers

ABSOLUTE MAXIMUM RATINGS

Continuous Input Voltage (Pin 1 ref. to Pin 8) (See note)
Continuous V _{CC} Supply (Pin 6 ref. to Pin 7) (See note)
Package Power Capability @25°C 1 W
Surge SCR On-STate Current (On-Time $\leq 200 \mu sec$)
Continuous Input Current (with SCR Triggered) (See note) 0.5 A _{RMS} .
Operating Ambient Temperature
Storage Ambient Temperature40 to +150°C
NOTE: Normally the IC is fed with an AC signal II and a RV

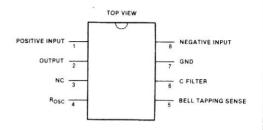
NOTE: Normally the IC is fed with an AC signal through a 2.2K resistor to guarantee compliance with these maximum ratings. Care should be taken when connecting a DC power supply to the IC to prevent the internal SCR from being fired which could result in damage to the IC.

TEST CIRCUIT

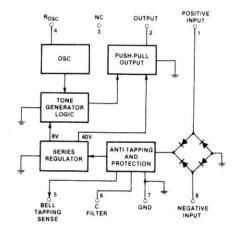
An oscilloscope can be used as the output "test equipment" for all the electrical measurements except output frequency, where a frequency counter should be used.

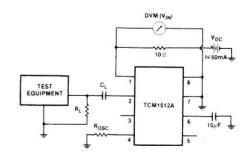
- 1. V_{IN} is the voltage measured across Pins 1 & 8 of the integrated circuit.
- Threshold voltage is the input voltage V_{IN} measured the instant before the output (Pin 2) starts oscillating.
- 3. Care must be taken in attempting to measure SCR characteristics of the integrated circuit so as not to exceed absolute maximum. It is suggested that a curve tracer be used across Pins 1 & 8 with capacitor connection Pin 6 shorted to Pin 7 to simulate a standby transient effect of a discharged 10 μ F filter capacitor.
- DC output currents are measured in the steady state. Peak output current would normally be greater than specified.
- 5. The output frequency is measured across R_L using a frequency counter. The frequency counter measures and displays the average frequency of the output tones F_{AVG} (where F_{AVG} = the average of the high frequency of the low frequency which is integrated by the counter over a long period of time).
- 6. Oscillator drift is the deviation in output frequency due to change in temperature T_A or input voltage V_{IN} compared to the output frequency at $T_A = 25\,^{\circ}\text{C}$ and $V_{IN} = 30\,\text{V}$. R_{OSC} is varied until the average output frequency $F_{AVG} = 1250\,\text{Hz}$.
- 7. For most tests, Pin 5 is left open. Where specified, Pin 5 is activated by connecting a 2.2K resistor across Pins 5 & 6.

PIN CONNECTION



BLOCK DIAGRAM





Test Circuit

TCM1512A 276-1302

TYPICAL CHARACTERISTICS

This first graph shows the typical average output frequency vs. oscillator tuning resistor ($R_{\rm OSC}$). The curve shows the general trend that the IC's follow; however, the values will differ from IC to IC. The curve should not be used as an accurate design tool since IC's could vary more than \pm 10% from the values

given in this graph.

The second graph shows the minimum operating voltage at tip and ring (20 Hz) vs. input capacitance C1 as a function of load resistance. The dashed curve marked "threshold" shows the voltage necessary at tip and ring to produce a voltage between pin 6 and 7 large enough to trip an internal switch and start the output oscillating. However, depending on the load and input capacitance, the minimum operating voltage could be larger than the threshold voltage. The threshold voltage can turn the IC on for an instant until the load drains the 10 μF capacitor across pins 6 and 7 and then the IC would turn off again. Depending on $R_{\rm LOAD}$ and C1, the minimum operating voltage could be the true threshold voltage.

TYPICAL APPLICATIONS

Input Circuitry

The TCM1512A has built-in circuitry to avoid "tapping," a false triggering due to transients. The IC is kept "OFF" (in standby) until the incoming signal has charged the capacitor on pins 6 and 7 to a threshold of approximately 8 volts through an internal zener and 8K resistor.

Connecting pin 5 and pin 6 bypasses the internal zener and thus reduces the threshold voltage, $(V_{\rm IN})$. The connection, if made, should be with a resistor of

not less than 2K.

The ring detector/driver IC has built-in transient protection circuitry which (with appropriate external circuitry) is designed to handle lightning strikes (1500 V/200 μsec) on a phone line. The IC is made up of a high current SCR triggered by a circuit that senses current (typically 70 mA) through the 70 V on-chip zener. The external 2.2K resistor is a necessary component to dissipate the energy when the SCR is turned on. Therefore, with an external resistor of 2.2K, a voltage transient of 224 V (peak) from tip to ring, will fire the SCR. (2200 $\Omega \times 0.07$ A Pk) + 70 V = 224 V (Pk), Note: Caution is required when a DC power supply is connected to the input pins (1 and 8). If the IC is subjected to a transient, it could possibly fire the SCR and would not turn off until the current supplied to it falls below the holding current $I_{\rm H}$. The DC power supply provides constant current and would result in IC destruction.

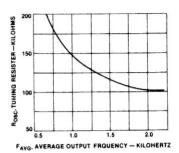
The ring detector/driver IC has a standby impedance of greater than 100K. The IC achieves such a high impedance due to an on-chip series zener which presents a high impedance until its turn-on voltage (6.8V) is reached. However, when the IC reaches its threshold voltage (8V) across pins 6 and 7, an internal switch is closed which bypasses the 6.8 V zener. This allows for more efficient power transfer to the load when the IC is in the operating mode. In the operating mode the IC has an AC impedance determined largely from the output

load.

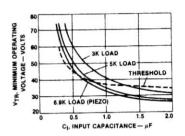
Output Tone Operation

The external resistor R_{OSC} sets the frequency of the IC's oscillator. The oscillator frequency F_{OSC} is then divided by a divide-by-14 counter for the high frequency F_H and a divide-by-16 counter for the low frequency F_L . The output frequencies are then divided by a divide-by-128 counter to establish the "warble rate." The warble rate is the alternation between the high frequency F_H and the low frequency F_L . Therefore, by changing the oscillator resistor R_{OSC} , the pitch of the output tones (F_H/F_L) and the warble rate between the tones can be set to the desired value. Oscillator drift is kept to a minimum (–1% to $\pm 0.5\%$) during varying input voltages and operating temperatures due to an on-chip 10 V regulator and circuit design techniques. Tolerance of the output frequencies (F_H/F_L) from IC to IC are dependent upon IC tolerances and R_{OSC} tolerance and is normally in excess of \pm 10%.

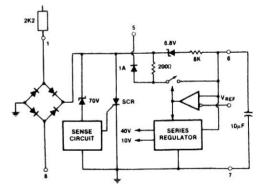
Oscillator Stability: It is recommended that on PCB's, R_{OSC} be located close to pin 4 (short lead) and be surrounded by ground plane. Also, pin 3 (N/C) should be grounded. These measures will prevent capacitive coupling from the output to the master oscillator, which may cause oscillator instability.



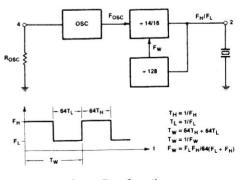
Tuning Resistor vs Average Output Frequency



Minimum Operating Voltage vs input Capacitance



Input Circuitry



Output Tone Operation

TCM1512A 276-1302

TYPICAL APPLICATIONS (Cont'd)

Telephone Application

The primary application for the TCM1512A ring detector/driver IC is in the telephone set.

This TCM1512A ring detector/driver IC is designed for use in telephone sets to detect ring voltages and to drive a piezo-ceramic disc transducer, thus replacing the electromechanical bell. It can produce sound with efficiency comparable to that obtainable from a type 500 set. The typical output signal produces a pleasant but attention drawing sound with an average frequency of 1250 Hz. It is modulated between 1172 Hz and 1339 Hz at a 9.8 Hz warble rate. These output frequencies and the warble rate are adjustable by varying the value of the external Rose.

The network formed by the 1.8 μ F DC blocking capacitor, the 2.2K current limiting resistor, and the diode full wave bridge supply the IC power from the phone lines. The 1.8 μ F capacitor is "standard" with U.K. mechanical telephones and normally part of the hybrid network. The value of the capacitor (C1) affects turn-on time and the minimum input voltage. The incoming rectified AC signal is filtered by an external 10 μ F/100 V capacitor connected between pin 6 and 7. The value of this filter capacitor affects the turn-on time of the IC. More significantly, it is used with internal IC circuitry to suppress "tapping." Tapping is a false ringing of the bell due to pulses on the phone line from rotary dials or pulse dialing IC's.

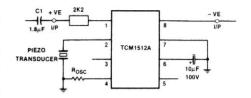
The TCM1512A incorporates a high standby input impedance to assure that "on-hook" telephones will not interfere with parallel (extension) "off-hook" telephones transmitting DTMF or voice frequency signals. Industry standards specify < 100K for voice frequencies (700 Hz - 1.6 kHz) for input voltages up to 3 V_{RMS} . The impedance for operating voltages (during ring) is specified to be < 8K. The TCM1512A meets both of these requirements. The DC blocking capacitor (C1) and the filter capacitor could modify the value of the ringer input impedances. The more closely the load and IC impedance match the line impedance, the greater the power transfer to the load. A potentiometer in series with the piezo load could be useful as a volume control.

The minimum operating voltage at tip and ring can be altered by changing the value of two external components, C1 and R_{LOAD} . C1 is the DC blocking capacitor at tip and ring and R_{LOAD} is the equivalent resistance of the load which may be a piezo transducer or the primary winding of a transformer. In the electromechanical telephone, C1 is fixed at 1.8 μF . However, if one is designing an all electronic telephone C1 and R_{LOAD} could be selected to achieve the desired minimum operating voltage.

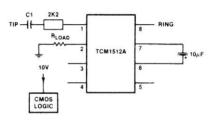
Alarm Circuit

This device contains all the active components necessary to build a security alarm system. A few external capacitors and resistors are required, along with a 16 V or 24 V transformer. The external 20 μF capacitor stores voltage during alternate half-cycles that is added to the next half-cycle's voltage to generate 30 V (Pk) across pins 6 and 7. The voltage doubler allows the IC to turn on with lower supply voltages than are normally required.

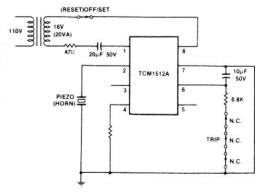
The IC is in standby (Off) when the "trip" switches are in their normally closed position. The 6.8K resistor doesn't allow the 10 μ F capacitor (pins 6 and 7) to charge up to its 11.5 V threshold voltage. The instant the trip switch is opened, the capacitor charges and the alarm sounds. Even if the trip switch is closed, the alarm will continue to sound. This is due to a latch circuit internal to the IC. The alarm is disarmed by opening the reset/set switch. when using a "piezo horn" for a transducer, sound pressure levels of 105 dB or greater can be achieved with as little as 10 mA supply current.



Telephone Application of Ring Detector/Driver



Input/Output Circuitry



Alarm Circuit

4001 276-2401

QUAD TWO-INPUT NOR GATE



GENERAL DESCRIPTION

The 4001 quad 2-Input NOR gate is constructed with MOS P-channel and Nchannel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/ or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and

 V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

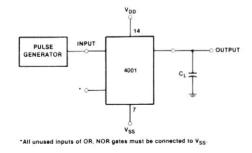
FEATURES

- Quiescent current = 0.5 nA typ/pkg @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Single supply operation-positive or negative
- High fanout > 50
- Input impedance = 10¹² ohms typical
- · Logic swing independent of fanout

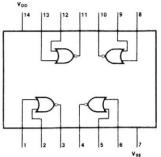
ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply Voltage0.5 to	+16 Vdc
Input Voltage. All Inputs	+0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range40	to +85°C
Storage Temperature Range65 to	+150°C

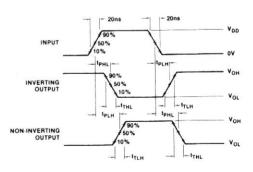
SWITCH TIME TEST CIRCUIT



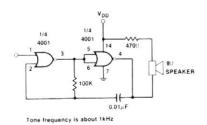
PIN CONNECTION TOP VIEW



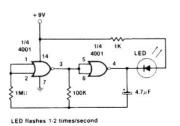
SYNC TIMING WAVEFORMS



TYPICAL APPLICATIONS



Gated Tone Source



LED Flasher



QUAD TWO-INPUT NAND GATE

4011 276-2411

GENERAL DESCRIPTION

The 4011 is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and

 V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FEATURES

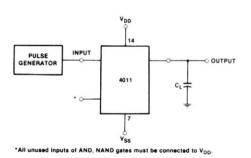
- Quiescent current = 0.5 nA typ/pkg @ 5 Vdc
 Noise immunity = 45% of V_{DD} typical
 Supply voltage range = 3.0 Vdc to 16 Vdc

- Double diode protection on all inputs

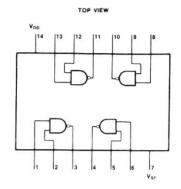
ABSOLUTE MAXIMUM RATINGS (Voltages referenced to Ves)

DC Supply
Input voltage, All Inputs
DC Current Drain per Pin
Operating Temperature Range40 to +85°C
Storage Temperature Range65 to +150°C

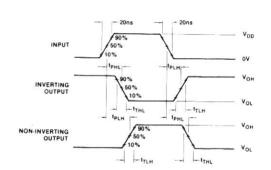
SWITCH TIME TEST CIRCUIT



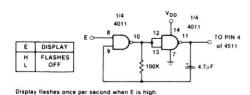
PIN CONNECTION

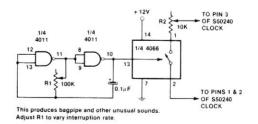


SYNC TIMING WAVEFORMS



TYPICAL APPLICATIONS





Special Effects

276-2413

DUAL TYPE D FLIP-FLOP



GENERAL DESCRIPTION

The 4013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data. (D). Direct Set. (S). Direct Reset. (R). and Clock (C) inputs and complementary outputs (Q and Q). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g.,

either Vss or VDD)

FEATURES

- Static operation
- Quiescent current = 2.0 nA/package typical @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Single supply operation
- Toggle rate = 4 MHz typical @ 5 Vdc
- Logic edge-clocked flip-flop design-logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Capable of driving two-low-power TTL loads. one low-power schottky TTL load or two HTL loads over the rated temperature range.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{SS})

DC Supply Voltage 0.5 to +16 V	dc
Input Voltage. All Inputs	dc
DC Current Drain per Pin	dc
Operating Temperature Range 40 to +85	°C
Storage Temperature Range65 to +150	$^{\circ}C$

TRUTH TABLE

PIN CONNECTION

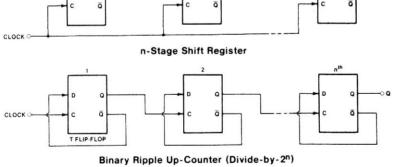
TOP VIEW

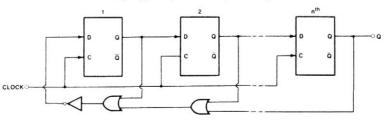
INPUTS				OUTE	UTS
Clock†	Data	Reset	Set	Q	$\bar{\mathbf{Q}}$
_	L	L	L	L	Н
_	Н	L	L	Н	L
	X	L	L	No Ch	ange
X	X	Н	L	L	H
X	X	L	H	Н	L
X	X	Н	Н	Н	Н

X = Don't Care L = Low Level

H = High Level t = Level Change

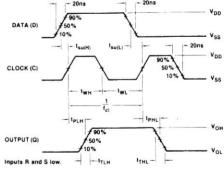
TYPICAL APPLICATIONS



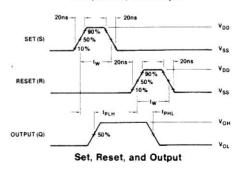


Modified Ring Counter (Divide-by-(n+1))

SYNC TIMING WAVEFORMS



Data, Clock, and Output





DECADE COUNTER/DIVIDER

4017 276-2417

GENERAL DESCRIPTION

The 4017 is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \!\! \leqslant \!\! (V_{in} \text{ or } V_{out}) \!\! \leqslant \!\! V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}

FEATURES

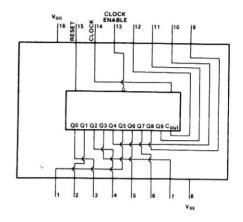
- Fully static operation
- DC clock input circuit allows slow rise times
- Carry out output for cascading
- 12 MHz (typical) operation @ V_{DD} = 10 Vdc
- Quiescent current = 5.0 nA/package typical @ 5 Vdc
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Capable of driving two low-power TTL loads, one low-power schottky TTL load or two HTL loads over the rated temperature range

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply Voltage0.5 to +16 Vd	c
Input Voltage, All Inputs	c
DC Current Drain per Pin	C
Operating Temperature Range40 to +85°	C.
Storage Temperature Range65 to +150°	C

PIN CONNECTION

TOP VIEW



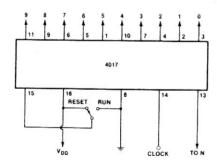
TRUTH TABLE (Positive Logic)

Clock	Clock lock Enable Re		Decode Output = n	
L	X	L	n	
X	Н	L	n	
X	X	Н	QL	
	L	L	n+1	
~_	X	L	n	
X		L	n	
1	~	L	n + 1	

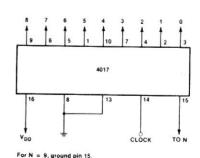
X = Don't Care If n <5 Carry = "H". Otherwise = "L"

L = Low Level H = High Level

TYPICAL APPLICATIONS



Count to N and Halt



19969

Count to N and Recycle

4049 276-2449

INVERTING HEX BUFFER



GENERAL DESCRIPTION

The 4049 hex inverter/buffer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, $V_{\rm CC}$. The input-signal high level ($V_{\rm IH}$) can exceed the $V_{\rm CC}$ supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters ($V_{\rm CC}=5.0$ V, $V_{\rm OL}\leq0.4$ V, $I_{\rm OL}\geq3.2$ mA). Note that pin 16 is not connected internally on this device; consequently connections to this terminal will not affect circuit operation.

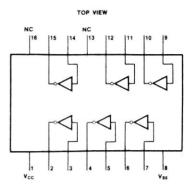
FEATURES

- · High source and sink currents
- · High-to-low level converter
- Quiescent current = 2.0 nA/package typical @ 5 Vdc
- Supply voltage range = 3.0 Vdc to 16 Vdc

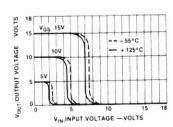
ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

DC Supply Voltage0.5 to +16 V	/dc
Input Voltage. All Inputs	√dc
DC Current Drain per Input Pin	Adc
DC Current Drain per Output Pin	Adc
Operating Temperature Range	5°C
Storage Temperature Range65 to +15	0°C

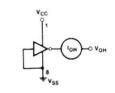
PIN CONNECTIONS

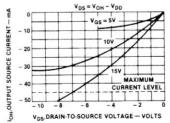


TYPICAL CHARACTERISTICS

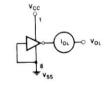


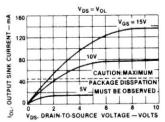
Output Voltage vs Input Voltage





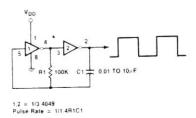
Output Source Current vs Drain-To-Source Voltage



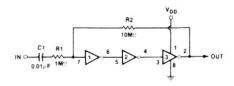


Output Sink Current vs Drain-To-Source Voltage

TYPICAL APPLICATIONS



Clock Pulse Generator



1.2.3 = 1/2 4049 Note that the inverters are used in a LINEAR mod Gain = 82/81

Linear IOX Amplifier



QUAD BILATERAL SWITCH

4066 276-2466

GENERAL DESCRIPTION

The 4066 consists of four independent switches capable of controlling either digital or analog signals. This Quad Bilateral Switch is useful in signal gating. chopper, modulator, demodulator, and CMOS logic implementation.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to

the range $V_{SS} \le (V_{IN} \text{ or } V_{OUT}) \le V_{DD}$.

Unused inputs must always be tied to the appropriate logic voltage level (e.g., either VSS or VDD).

FEATURES

- Wide supply voltage range 3V to 15V
- High noise immunity -0.45 V_{DD} typ
- Wide range of digital and analog switching ±7.5 V_{PEAK}
- "ON" resistance for 15V operation -80Ω typ
- Matched "ON" resistance over 15V signal input $-\Delta R_{ON} = 5\Omega$ typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio-65 dB typ
- High degree of linearity -< 0.4% distortion typ
- Extremely low "OFF" switch leakage -0.1 nA typ Extremely high control input impedance $-10^{12}\Omega$ typ
- Low crosstalk between switches - 50 dB typ
- Frequency response, switch "ON" 40 MHz typ

APPLICATIONS

Analog signal switching/multiplexing

Signal gating

Squelch control

Chopper

Modulator/Demodulator

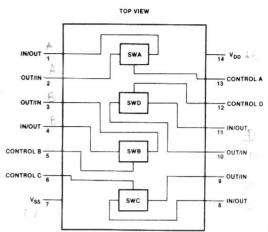
Commutating switch

- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

ABSOLUTE MAXIMUM RATINGS

Supply Voltage0.5V to +18	V
Input Voltage	V
Package Dissipation	W
Operating Temperature Range	$^{\circ}C$
Storage Temperature Range65 to +150	,C
Lead Temperature (Soldering, 10 seconds)	,C

PIN CONNECTION

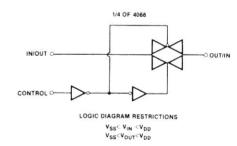


TRUTH TABLES

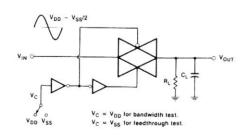
CONTROL	SWITCH
0	OFF
1	ON

$v_{control}$	V_{IN} TO V_{OUT} RESISTANCE
$\frac{V_{SS}}{V_{DD}}$	$> 10^9$ ohms typical 3×10^2 ohms typical

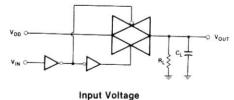
LOGIC DIAGRAM

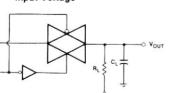


TYPICAL APPLICATIONS



Bandwidth and Feedthrough Attenuation





Propagation Delay Time, Control to Output

PULSE

4116 276-2505

16K DYNAMIC RAM

GENERAL DESCRIPTION

The 4116 is a 16.384×1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the 4116 to be used in page mode operation.

The 4116 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including an RAS-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology is used in the manufacture of the 4116. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the 4116.

FEATURES

- Access times: 150 ns. 200 ns. 300 ns
- Low power; 462mW max
- TTL compatible: all inputs and output
- Gated CAS-noncritical timing
- Read. wire. read-modify-write and RAS-only refresh cycles
- · Page mode operation

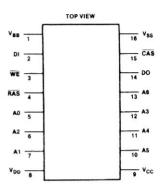
ABSOLUTE MAXIMUM RATINGS

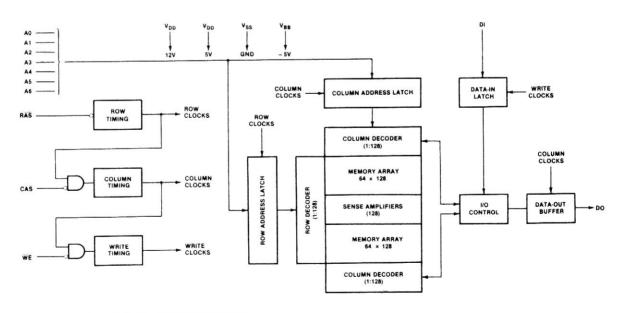
V.
V.
V
V
C
Ü
C

INTERNAL CIRCUIT

MANAMA

PIN CONNECTION







QUAD TWO-INPUT NAND GATE

7400 276-1801

GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipiation. It provides the basic functions used in the implementation of digital integrated circuit systems.

For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

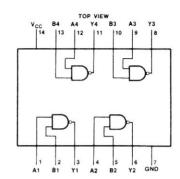
Two possible ways at handling unused inputs are:

- (1) Connect unused inputs to V_{CC} . For all multi-emitter conventional TTL inputs, A 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.
- (2) Connect the unused input to the output of an unused gate that is forced high.

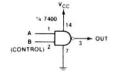
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V _{CC}	•
Input High Voltage	
Input Low Voltage	
Input Clamp Diode Voltage ($V_{CC} = 5.0 \text{ V}$, $I_{IN} = -12 \text{ mA}$)	
Input High CUrrent ($V_{CC} = Max., V_{IN} = 2.4 \text{ V}$)	
Input Low Current ($V_{CC} = Max., V_{IN} = 0.4 \text{ V}$)	
Operating Temperature	,

PIN CONNECTION



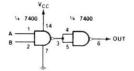
TRUTH TABLE $Y = \overline{AB}$



A	В	OUT
L	L	н
1	H	H
H	L	H
н	н	L





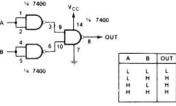




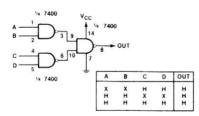
Control Gate

Inverter

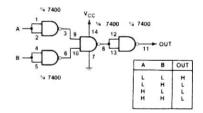
AND Gate



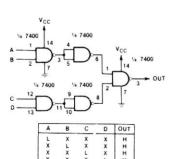




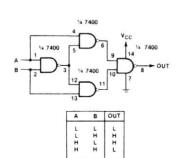
AND-OR Gate



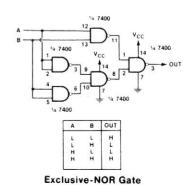
NOR Gate



4-Input NAND Gate



Exclusive-OR Gate



7404 276-1802

HEX INVERTER



GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipation. This hex inverter provides the basic functions used in the implementation of digital integrated circuit systems.

For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

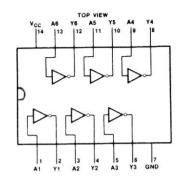
Two possible ways of handling unused inputs are:

- (1) Connect unused inputs to V_{CC} . For all multi-emitter conventional TTL inputs, A 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.
- (2) Connect the unused input to the output of an unused gate that is forced high.

ABSOLUTE MAXIMUM RATINGS

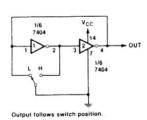
Supply Voltage V _{CC}
Input High Voltage
Input Low Voltage
Input Clamp Diode Voltage (V _{CC} = 5.0 V,I _{IN} = -12 mA)
Input High Current ($V_{CC} = Max., V_{IN} = 2.4 \text{ V}$)
Input Low Current ($V_{CC} = Max., V_{IN} = 0.4 \text{ V}$)
Operating Temperature

PIN CONNECTION



TRUTH TABLE

$$Y = \overline{A}$$



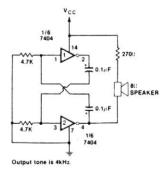
1/6
7404

1N

1/6
1/6
1/6
0UT = IN

1/6
7404

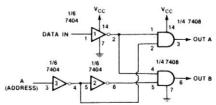
0UT = IN



Bouncefree Switch

Universal Expander

Audio Oscillator



This circuit steers the input bit to the output selected by the address.

DATA	ADDRESS	OUT A	OUT B
L	L	L	н
H	1 1	н	н
L	Н	н	L
н	H	н	н

1-of-2 Demultiplexer



QUAD TWO-INPUT AND GATE

7408 276-1822

GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipation. These gates provide the basic functions used in the implementation of digital integrated circuit systems.

For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

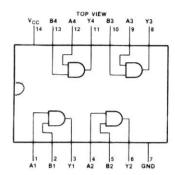
Two possible ways at handling unused inputs are:

- (1) Connect unused inputs to $V_{\rm CC}$. For all multi-emitter conventional TTL inputs, a 1 to 10K ohm current limiting series resistor is recommended, to protect against $V_{\rm CC}$ transients that exceed 5.5 V.
- (2) Connect the unused input to the output of an unused gate that is forced high.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V _{CC}
Input High Voltage
Input Low Voltage
Input Clamp Diode Voltage ($V_{CC} = 5.0 \text{ V}$, $I_{IN} = -12 \text{ mA}$)
Input High Current ($V_{CC} = Max., V_{IN} = 2.4 \text{ V}$)
Input Low Current ($V_{CC} = Max., V_{IN} = 0.4 \text{ V}$)
Operating Temperature

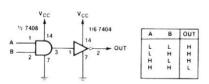
PIN CONNECTION



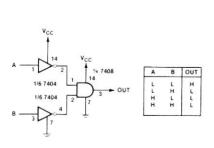
TYPICAL APPLICATIONS



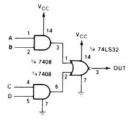
AND Gate Buffer



NAND Gate

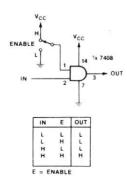


NOR Gate



A	В	C	D	OUT
X	X	X	X	н
L	L	X	X	L
L	L	L	L	L

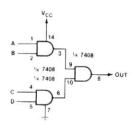
AND-OR-Invert Gate



Digital Transmission Gate

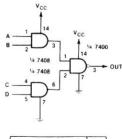
TRUTH TABLE

$$Y = AB$$



А	В	С	D	001
н	н	н	н	н
X	X	×	×	L

4-Input AND Gate



Α	В	C	D	OUT
н	н	н	н	L
X	X	×	X	H

4-Input NAND Gate

7447 276-1805

BCD TO SEVEN-SEGMENT DECODER/DRIVER



GENERAL DESCRIPTION

This versatile binary-coded-decimal 7-segment display driver fulfills a wide variety of requirements for most active high (common cathode) and active low (common anode) light emitting diodes (LED) or lamp displays. It fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate off of a single 5.0V supply. The output will withstand 15 Volts at a maximum leakage current of $250\mu A$.

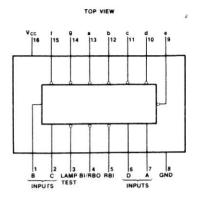
FEATURES

- Lamp-test input
- Leading trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes
- Open collector outputs drive indicators directly

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V _{CC}	.25 V
Continuous Voltage at Outputs a-g	15 V
Logic 1 Input Voltage Mir	i. 2 V
Logic 0 Input Voltage	0.8 V
Logic 0 Output Voltage BI/RBO	0.4 V
Logic 1 Output Voltage at BI/RBO	2.4 V
Power	mW

PIN CONNECTION



TRUTH TABLE

DECIMAL			INPU	TS			BI/RBO†	OUTPUTS					NOTE		
OR FUNCTION	LT	RBI	D	С	В	A	BI/KBO	а	b	С	d	e	f	g	NOTE
0	Н	Н	L	L	L.	L	Н	L	L	L	L	L	L	Н	
1	Н	X	L	L	L	Н	Н	H	L	L	H	H	Η	H	
2	Н	X	L	L	H	L	Н	L	L	H	L	L	Η	L	
3	Н	X	L	L	H	Н	Н	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	Н	H	L	L	H	H	L	L	
5	H	X	L	H	L	Н	Н	L	H	L	L	H	L	L	
6	Н	X	L	H	H	L	Н	H	H	L	L	L	L	L	
7	H	X	L	H	H	Н	Н	L	L	L	H	H	H	H	
8	Н	X	H	L	L	L	Н	L	L	L	L	L	L	L	1
9	Н	X	H	L	L	H	Н	L	L	L	H	H	L	L	
10	Н	X	H	L	Н	L	Н	H	H	H	L	L	H	L	
11	Н	X	Н	L	H	H	Н	H	H	L	L	H	H	L	
12	Н	X	H	H	L	L	Н	H	L	H	H	H	L	L	
13	Н	X	H	Н	L	H	Н	L	H	H	L	Η	L	L	
14	Н	X	H	H	Н	L	Н	H	H	H	L	L	L	L	
15	Н	X	H	H	Н	H	Н	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	Η	H	H	2
RBI	Н	L	L	L	L	L	L	Н	H	H	H	H	H	H	. 3
LT	L	X	X	X	X	X	Н	L	L	L	L	L	L	L	4

H = High Level, L = Low Level, X = Irrelevant

- Notes: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 thru 15 are desired.

 The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
 - 2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are H regardless of the level of any other input.
 - 3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).
 - 4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp test input, all segment outputs are L.



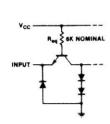


Numerical Designations and Resultant Displays

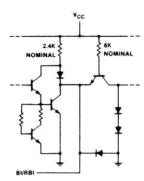
[†] BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

7447 276-1805

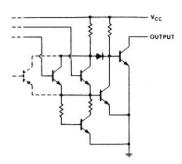
INPUT/OUTPUT EQUIVALENTS



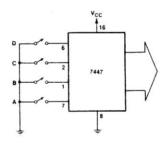
Each Input Except BI/RBO



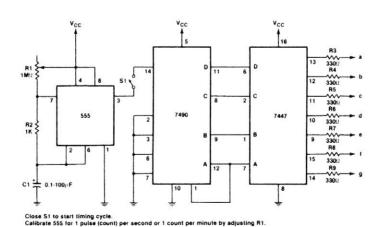
BI/RBO Input



Typical of Outputs a Thru g



Manually Switched Display



0-9 Second/Minute Timer

7490 276-1808

DIVIDE BY 2 OR 5, BCD COUNTER



GENERAL DESCRIPTION

This monolithic BCD counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use maximum count length, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

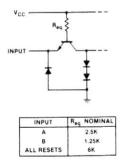
FEATURES

- Low power consumption
- High count rates . . . typically 50MHz
- Choice of counting modes
- Fully TTL and CMOS compatible

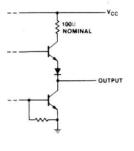
ABSOLUTE MAXIMUM RATINGS

Typical Power Dissipation	5 mW
Count Frequency	2 MHz
High Level Input Voltage (Min)	
Low Level Input Voltage (Max)	.0.8 V
High Level Input Current	ΙΟΟ μΑ
Low Level Output Current (Max)	16 mA
V _{CC} to Ground	- 7.0 V
Voltage Applied to Outputs (Output High) 0.5 to	5.5 V

INPUT/OUTPUT EQUIVALENTS

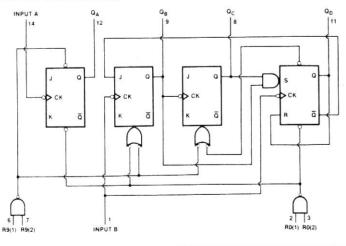




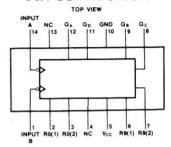


Typical of all Outputs

BLOCK DIAGRAM



PIN CONNECTION



TRUTH TABLES

RESET/COUNT

R	ESET	INPUT	(OUT	PUTS	3	
RO(1)	RO(2)	R9(1)	R9(2)	Q_{D}	$\mathbf{Q}_{\mathbf{C}}$	Q_B	$\mathbf{Q}_{\mathbf{A}}$
Н	Н	L	X	L	L	L	L
Н	Н	X	L	L	L	L	L
X	X	Н	Н	Н	L	L	H
X	L	X	L		COU	JNT	
L	X	L	X		COL	JNT	
L	X	X	L		COL	JNT	
X	L	L	X		COU	JNT	

BCD COUNT SEQUENCE (See Note A)

COUNT	OUTPUTS			
	Q_{D}	Q_{C}	Q_B	Q_A
0	L	L	L	L
1	L	L	L	Н
2	L	L	H	L
3	L	L	H	Н
4	L	Н	L	L
5	L	Н	L	Н
6	L	Н	Н	L
7	L	Н	H	Н
8	Н	L	L	L
9	Н	L	L	Н

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUTS			
	Q_A	Q_D	Q_{C}	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	Н	Н
4	L	H	L	L
5	Н	L	L	L
6	Н	L	L	H
7	Н	L	H	L
8	Н	L	H	H
9	Н	Н	L	L

L = Low Level

H = High Level

Notes

- (A) Output Q_A is connected to input B for BCD count.
- (B) Output Q_D is connected to input A for biquinary count.



771 - 10

QUAD LINE DRIVER

MC1488 276-2520

GENERAL DESCRIPTION

The 1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

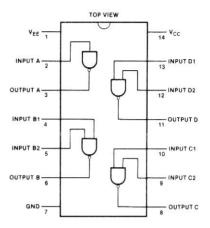
FEATURES

- Current Limited Output ±10 MA typ
- Power-Off Source Impedance 300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range

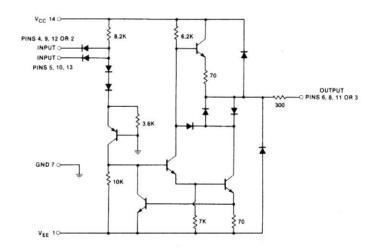
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC})
(V _{EE}) – 15 V
Output Signal Voltage (VO)
Power (PD)
Input Current-Low Logic State (V _{IL} = 0) (See Fig. 8) 1.6 mA
Input Current-High Logic State ($V_{IH} = 5.0V$) (See Fig. 8)
Output Resistance ($V_{CC} = V_{EE} = 0/V_{Ol} = \pm 2.0V$
(See Fig. 11)
Operating Temperature Range (TA)
Storage Temperature Range (T_{stg}) -65 °C To $+175$ °C

PIN CONNECTION



INTERNAL CIRCUIT (¼ of Circuit Shown)



TYPICAL CHARACTERISTICS

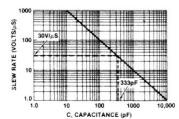


Figure 1—Slew Rate vs Capacitance for I_{SC} = 10mA

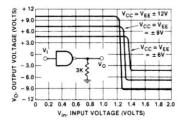


Figure 3—Transfer Characteristics vs Power-Supply Voltage

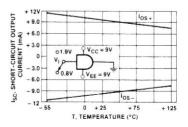


Figure 4—Short-Circuit Output Current vs Temperature

INTERFACE (DRIVER)

MC1488 276-2520

TYPICAL CHARACTERISTICS (Cont'd)

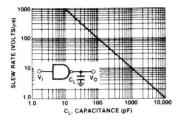


Figure 5—Output Slew Rate vs Load Capacitance

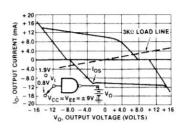


Figure 6—Output Voltage and Current-Limiting Characteristics

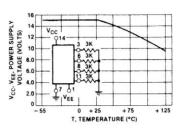
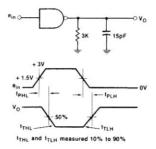


Figure 7 — Maximum Operating Temperature vs Power-Supply Voltage



Switching Response

TEST CIRCUITS

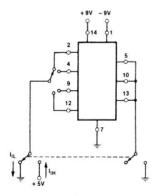


Figure 8 - Input Current

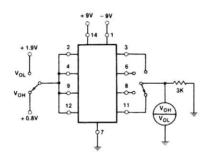


Figure 9- Output Voltage

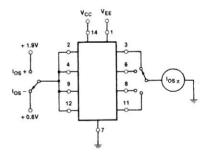


Figure 10 — Output Short-Circuit
Current

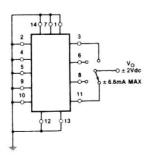


Figure 11 — Output Resistance (Power-Off)

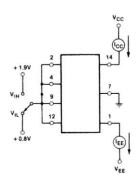


Figure 12 - Power-Supply Currents

MC1488 276-2520

APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The 1488 quad driver and its companion circuit, the 1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "O" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The 1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the 1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each drive output. The required capacitor can be easily determined by using the relationship $C = I_{\rm OS} \times \Delta T/\Delta$ V from which Figure 1 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The 1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \ge 9.0 \text{ V}$; $V_{EE} \le -9.0 \text{ V}$). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the 1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 2, could be used to decouple all the driver packages in a system. (These same diodes will allow the 1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the 1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

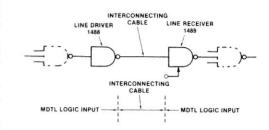
The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

OTHER APPLICATIONS

The 1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting—this enables the circuit designer to define the output voltage levels independing of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the 1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range—as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately —2.5 volts to the minimum specified—15 volts. The 1488 will drive the output to within 2 volts of the postive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL or DTL translation. Figure 15 shows one such combination.



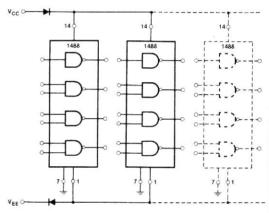


Figure 2—Power Supply Protection
to Meet Power-Off Fault Conditions

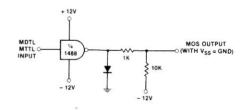


Figure 14—MDTL/MTTL-to-MOS Translator

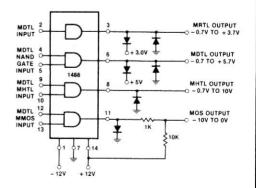


Figure 15—Logic Translator Applications

MC1489 276-2521

QUAD LINE RECEIVER

GENERAL DESCRIPTION

The 1489 monolithic quad line receiver is designed to interface data terminal equipment with data communications equipment in conformance with specificiations of EIA Standard No. RS-232C.

FEATURES

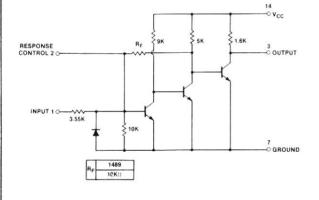
- Input Resistance-3.0 k to 7.0 K ohms
- Input Signal Range-±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
 - a) Logic Threshold Shifting
 - b) Input Noise Filtering

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC})	V
Input Voltage Range (V _{IR}) ±30	V
Output Load Current (I _L)	Α
Power Dissipation (P _D)	
Operating Temperature Range (TA)	C
Storage Temperature Range (T _{stg})65°C To +175°	C

INTERNAL CIRCUIT (4 of Circuit Shown)

OPEN O



Output Voltage and Input

Threshold Voltage

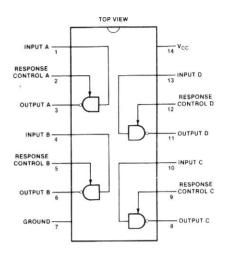
V_{CC} 14 2 4 5 9 10 12 11 7 7

Output Short-Circuit Current

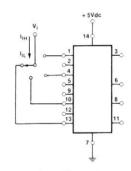
Power-Supply Current

NAMANA.

PIN CONNECTION



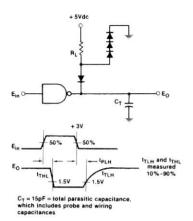
TEST CIRCUITS



Input Current

MC1489 276-2521

TYPICAL CHARACTERISTICS



Switching Response

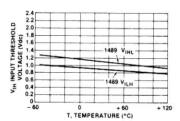


Figure 3—Input Threshold Voltage vs Temperature

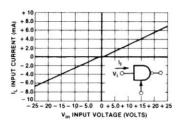


Figure 1-Input Current

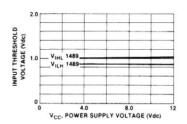


Figure 4—Input Threshold vs Power—Supply Voltage

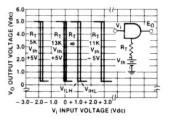


Figure 2—Input Threshold Voltage Adjustment

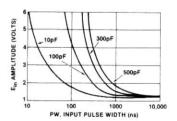


Figure 5 —Turn-on Threshold vs Capacitance from Response Control Pin to Gnd

APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The 1488 quad driver and its companion circuit, the 1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed here. The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The 1489 circuits meet these requirements with a maximum open circuit voltage of one $V_{\rm RE}$.

The receiver shall detect a voltage between -3.0 and -25 volts as a logic "1" and input between +3.0 and +25 volts as a logic "0". On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1". For this reason, the input hysteresis thresholds of the 1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative of logic "1" input.

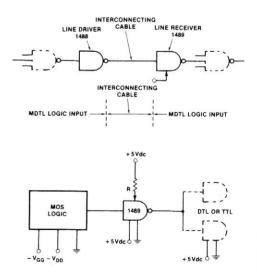


Figure 7 — Typical Translator Application — MOS to DTL or TTL



DUAL OPERATIONAL AMPLIFIERS QUAD OPERATIONAL AMPLIFIERS

GENERAL DESCRIPTION

The TLC27M4 and TLC27M2 consist of low-cost low-power quad and dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the silicon-gate LinCMOS™ process, giving them stable input offset voltage that is available with a 2 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, these devices are ideally suited for battery-powered or energy-conserving applications.

Because of the extremely high input impedance and low input bias and offset currents, applications for these devices include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices.

FEATURES

- Wide range of supply voltages (4 V To 16 V)
- True single supply operation
- Common-mode input voltage includes the negative rail
- Supply current range (150 μ A/Amp Typical)
- Slew-rate performance (0.6 V/µs Typical
- Extremely low input bias and offset currents Input bias current (1 pA Typical) Input offset current (1 pA Typical)
- Low input offset voltage (2 mV Maximum)
- Low noise-30 nV $\sqrt{\text{Hz}}$ Typical at f = 1 KHZ (High bias versions)

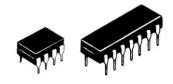
APPLICATIONS

- Transducer Interfacing
- **Analog Calculations**
- Amplifier Blocks
- Active Filters
- Signal Buffering

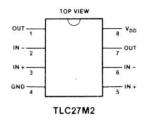
ABSOLUTE MAXIMUM RATINGS

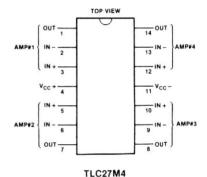
Supply Voltage (V _{DD}) (See Note 1)
Differential Input Voltage (See Note 2)
Input Voltage Range (Any Input)0.3 V To 18 V
Power Dissipation
Operating Temperature Range 0°C To 70°C
Storage Temperature Range65°C To +150°C
Duration of Short-Circuit at (Or Below) 25°C
Free-Air Temperature (See Note 3)
respective that the first than the contract of

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded

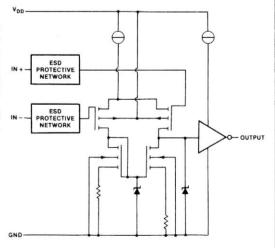


PIN CONNECTIONS



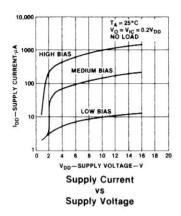


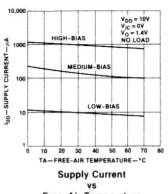
INTERNAL CIRCUIT (Each Amplifier)



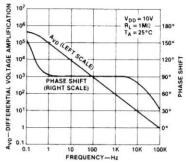
TLC27M2 276-1749 TLC274 276-1750

TYPICAL CHARACTERISTICS





Free-Air Temperature



Low-Bias Versions Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

TYPICAL APPLICATION INFORMATION

static protection

The inputs of this device are protected by series resistors and clamp diodes. As with any integrated circuit, ESD handling precautions should be used to avoid damage from strong electrostatic fields.

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, any input signals are applied.

output stage considerations

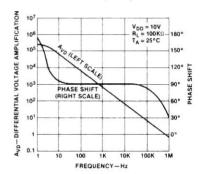
The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with high values of $V_{\rm DD}$ and reduced output loading. The low-level output voltage ($V_{\rm OL}$) decreases with reduced output current and high input common-mode voltage. With no load, Vol. is essentially equal to the GND pin potential.

supply configuration

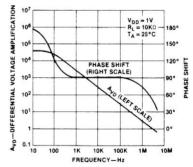
Even though this device is characterized for single-supply operation, it can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

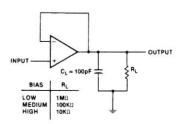
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.



Medium-Bias Versions Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency



High-Bias Versions Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency



Unity Gain Amplifier

TLC271 276-1748

PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIER

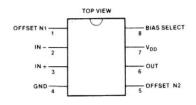


GENERAL DESCRIPTION

The TLC271 consists of low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike tradition metal-gate CMOS op amps, the device utilizes the silicon-gate LinCMOSTM process, giving it stable input offset voltages without sacrificing the advantages of metal-gate CMOS. The TLC271 can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this device is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels, from a high bias level (slew rate of 4.5 V/us, 10 V) to a low level (slew rate of 0.04 V/ μ s, dissipation of only 100 μ W at 10 volts) to suit the application.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC271 include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective us of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the lower penalties of traditional bipolar devices. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption.

PIN CONNECTION



FEATURES

- · Wide range of supply voltages
- · True single supply operation
- · Common-mode input voltage range includes the negative rail
- Selectable supply current Low = 100 μA typical Medium = 150 μA typical High = 1000 μA typical
- Extremely low input bias and offset currents
 I_{IB}—1 PA typical

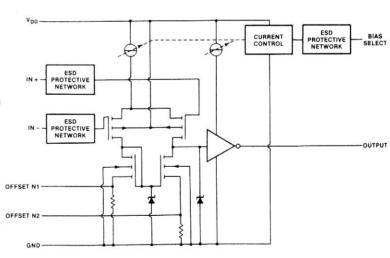
I_{IO}-1 PA typical

Low input offset voltage

Low noise—30 nV √ H z typical at 1 kHz (High Bias)

High slew rate
 High bias 4.5 V/μs typical
 Medius bias 0.6 V/μs typical
 Low bias 0.4 V/μs typical

INTERNAL CIRCUIT



APPLICATIONS

- · Transducer interfacing
- · Analog calculations
- Amplifier blocks
- Active filters
- · Signal buffering

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{DD}) (See Note 1)
Differential Input Voltage (See Note 2) ± 18 V
Input Voltage Range (Any Input)0.3 V To 18 V
Power Dissipation
Duration of Short-Circuit at (Or Below)
25°C Free Air Temperature (See Note 3)
Operating Temperature Range
Storage Temperature Range65°C To 150°C

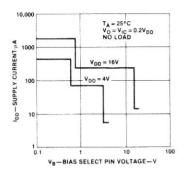
NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.

Differential voltages are at the noniverting input terminal with respect to the inverting input terminal.

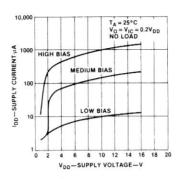
 The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

TLC271 276-1748

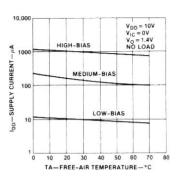
TYPICAL CHARACTERISTICS



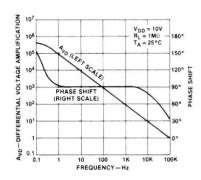
Supply Current vs Bias Select Pin Voltage



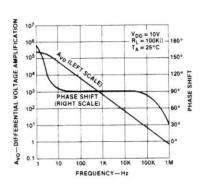
Supply Current vs Supply Voltage



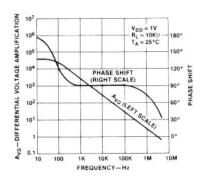
Supply Current vs Free-Air Temperature



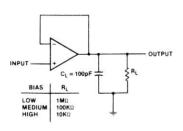
Low-Bias Versions
Large-Signal
Differential Voltage Amplification
and Phase Shift
vs
Frequency



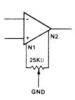
Medium-Bias Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency



High-Bias
Large-Signal
Differential Voltage Amplification
and Phase Shift
vs
Frequency



Unity-Gain Amplifier



Input Offset Voltage Null Circuit

TLC555 276-1718

TIMER



GENERAL DESCRIPTION

The TLC555 is a monolithic timing circuit fabricated using the Lin CMOST process. Due to its high-impedance inputs (typically $10^{12}\Omega$), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors. The TLC555 achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The Lin CMOST process allows the TLC555 to operate at frequencies up to 2 MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 1 mW at $V_{\rm DD} = 5V$) over a wide range of supply voltages ranging from 2 volts to 18 volts.

Threshold and trigger levels are normally two-thirds and one-third respectively of $V_{\rm DD}$. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

While the complementary CMOS OUTPUT is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply current spikes during output transitions.

FEATURES

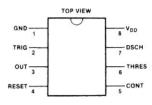
- Very low power consumption (1 mW typical at $V_{DD} = 5 \text{ V}$)
- · Capable of very high-speed operation (2 mHz in a stable operation)
- · Complementary CMOS output capable of swinging rail to rail
- High output-current capability (sink 100 mA typical) (soucre 10 mA typical)
- · Output fully CMOS, TTL, and MOS-compatible
- Low supply current reduces spikes during output transitions
- High impedance input 10¹²Ω typical)
- Single supply operation from 2 to 18 volts

ABSOLUTE MAXIMUM RATINGS

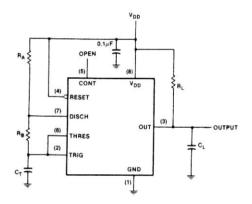
Supply Voltage (V_{DD}) (See Note 1)
Input Voltage Range (Any Input)
Power Dissipation (mW) 600mV
Operating Temperature Range
Storage Temperature Range65°C To 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.

PIN CONNECTION

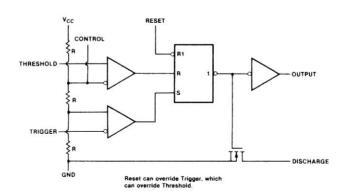


TYPICAL APPLICATION



Circuit for Astable Operation

BLOCK DIAGRAM





5.8W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TA7205AP is a monolithic audio power amplifier with a built in thermal shut-down circuit designed for car radio and stereo applications.

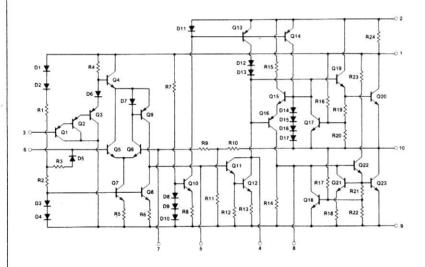
FEATURES

- Low distortion
- THD=0.15% (Typ.) (@ P_{OUT}=1W, G_V=55dB) THD=0.07% (Typ.) (@ P_{OUT}=1W, G_V=44dB) Operating supply voltage range: V_{CC}=9~18V
- 'PCT' process to insure low noise characteristic
- Current limiting for short-circuit protection
 Built in thermal shut-down circuit
- Built in surge voltage protection circuit

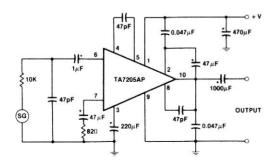
ABSOLUTE MAXIMUM RATINGS

Operating Supply Voltage(V_{CC})
Quiescent Supply Voltage (V _{CCQ})
Output Peak Current (I _O)
Quiescent Current (I _{CCO})80mA
Operating Temperature
Storage Temperature55 to +150°C

INTERNAL CIRCUIT

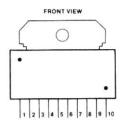


TYPICAL APPLICATION



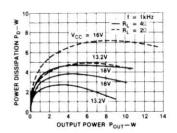
5 Watt Audio Amplifier

PIN CONNECTION

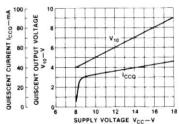


PIN	FUNCTION
1	V +
2	BOOTSTRAP
3	DECOUPLING
4	PHASE COMPENSATION
5	PHASE COMPENSATION
6	INPUT
7	NEGATIVE FEEDBACK
8	PHASE COMPENSATION
9	GROUND
10	OUTPUT

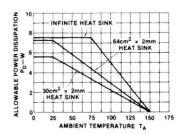
TYPICAL CHARACTERISTICS



Power Dissipation vs Output Power



Quiescent Current and Output Voltage vs Supply Voltage



Allowable Power Dissipation vs Ambient Temperature

SN76495 276-1764

COMPLEX SOUND GENERATOR



GENERAL DESCRIPTION

The SN76495 complex sound generator is a monolithic chip combining both analog (bipolar) and digital (I2L) circuitry. It includes a noise generator, a voltage-controlled oscillator (VCO), and a super-low-frequency oscillator (SLF) together with a noise filter, mixer, audio amplifier, and control circuitry to provide noise, tone, or low-frequency sounds and any combinations of these. Programming is accomplished via control inputs and user-defined external components, which allows a wide variety of sound to be created and tailored for particular applications. This device may be used in a variety of applications requiring audio feedback to the operator.

Operation is from a 7.5 volts to 10.5 volt supply applied to a built-in regulator through the $V_{\rm CC}$ terminal, in which case a regulated five volts is available from the Vreg terminal to power a small amount of external circuitry, or to provide a high-logic-level voltage to logic inputs.

FEATURES

- Generates noise, tone, or low frequency based sounds, or combinations of these
- · Sounds are defined by user via external components
- · Allows custom sounds to be created easily
- Low power requirements
- · Allows multiple sound system
- · Compatible with microprocessor systems
- On board 125 mW audio amplifier

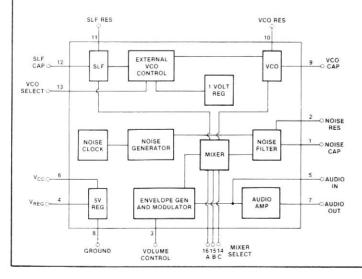
APPLICATIONS

- Arcade Games
- Video Games
- Pinball Games
- Toys
- Timers
- Alarms

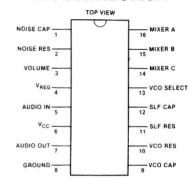
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC}
Input Voltage: Logic Input
Capacitor Input 5.0 V
Resistor Input
Operating Temperature Range
Storage Temperature Range65°C To +150°C
NOTE 1: All voltage values are with respect to package ground terminal.

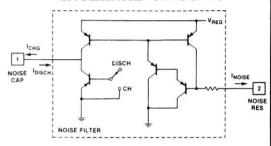
BLOCK DIAGRAM

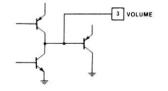


PIN CONNECTION

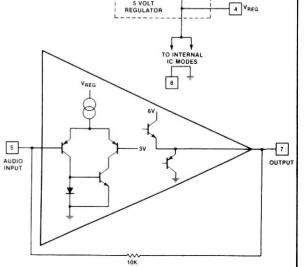


INTERNAL CIRCUITS





6 Vcc



SN76495 276-1764

OPERATION

Super Low Frequency Oscillator (SLF)

The SLF is normally operated in the range of 0.1 Hz to 30 hertz, but will operate up to 20 kHz. The frequency is determined by two external components, the SLF control resistor (Rslf) at pin 11 at ground and the SLF control capacitor (Cslf) at pin 12 at ground according to the following equation:

Equation 1: SLF Frequency (Hz) = .66/(9Kohm+Rslf)xCslf at Vreg=5V

The SLF supplies two signals to other parts of the device. It feeds a 50% duty cycle square wave to the mixer, and it feeds a triangular wave to the external VCO of SLF select logic, where, if VCO select (pin 13) is at a low logic level, it is fed through to the VCO to modulate the frequency of that oscillator.

Voltage Controlled Oscillator (VCO)

The VCO produces a tone output whose frequency is dependent upon the voltage at the input of the VCO. This controlling voltage may be either the SLF output described above, an internal voltage producing a constant tone, or externally by placing a voltage on the SLF capacitor pin. The higher the voltage applied to the VCO, the lower the frequency of the VCO output.

The first mode, VCO controlled by SLF, is selected by placing the VCO select pin low and supplying both the VCO capacitor (CVCO) at pin 9 at ground the the VCO resistor (RVCO) at pin 10 at ground. Minimum frequency of the VCO is determined by the following equation:

Equation 2: Minimum VCO Frequency (Hz) = 0.60/(9Kohm+RVCO) × CVCO

The frequency range of the VCO is internally determined at an approximate ratio of 10:1, so that maximum frequency of the VCO will be approximately ten times the minimum frequency determined by the external components RVCO and CVCO.

The second method of supplying a control voltage for the VCO is to use an internal voltage preset at 1 volt. This mode is selected by taking VCO select to a high level. In this mode, the VCO puts out a constant tone determined by CVCO and RVCO in this relationship:

Equation 3: fVCO = 1.45/(RVCO + 9Kohn) × CVCO × 0.9V) Hz

A third method of controlling the voltage to the VCO is to apply the controlling voltage (Vext) to the SLF capacitor pin. This voltage level (0 to 2.30 volts) will determine the output frequency of the VCO. Output frequency in this mode is determined by this relationship:

Equation 4: fVCO = 1.45/(RVCO + 9Kohn) × CVCO × (Vext - .1V) Hz

Mixer

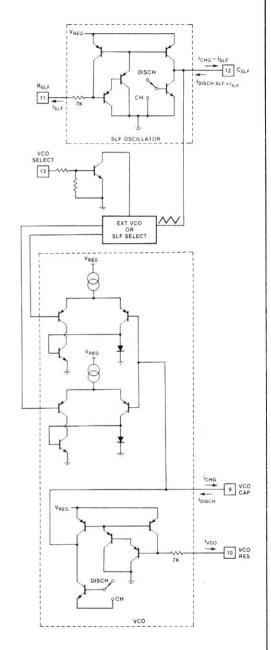
The mixer logic selects one or a combination of the inputs from the generators and feeds the output to the amplifier. The mixer performs a logical AND function on these sounds; therefore, the output of the mixer is not a combination of simultaneous sounds. The output of the mixer is determined by the logic levels at the mixer select inputs as shown in Table 1.

TABLE 1

MIXER SELECTS INPUTS			ER SELECTS INPUTS	
A (PIN 16)	B (PIN 15)	C (PIN 14)	MIXER OUTPUT	
L	L	L	VCO	
Н	L	L	SLF	
L	Н	L	NOISE	
Н	Н	L	VCO/NOISE	
L	L	Н	SLF/NOISE	
Н	L	Н	SLF/VCO/NOISE	
L	Н	Н	SLF/VCO	
H	Н	Н	INHIBIT	

H = HIGH LEVEL L = LOW LEVEL OR OPEN

INTERNAL CIRCUITS (Cont'd)



SN76495 276-1764

Mixer (Cont'd)

Figure 1 is an example of how two signals would be combined by the mixer according to the logical AND function with the mixer select times set for SLF/noise (C input high, A and B inputs low).

To obtain two sounds occurring simultaneously (e.g., car engine and siren or steam engine and whistle), multiplexing is required. The multiplexing is accomplished by switching the mixer select lines at a sufficiently rapid rate that the two sounds seem to occur at the same time. The frequency of the multiplexing should be above the human hearing range. A multiplexing drive signal with a 50% duty cycle is required to provide equal amplitudes for both sound functions.

Volume

Output volume from the SN76495 can be controlled by varying a voltage level on pin 3. This voltage level should range from 3.5 volts, for maximum volume, to .4 volts or below for no output. Under no circumstances should this pin be taken above 5 volts or below 0 volts. Voltages outside of this range could damage the unit.

Noise Generator/Filter

The noise generator produces pseudo-random white noise that passes through the noise filter before being applied to the mixer. The variable-bandwidth low-pass filter has its cutoff point defined by the noise filter control resister (Rnf) at pin 2 and the noise filter control capacitor (Cnf) at pin 1 according to the following equation:

Equation 5: fCutoff (Hz) $\approx .43/(9$ Kohm + Rnf) \times Cnf

Output Amplifier

The output amplifier is contained entirely on chip. The amplifier operates in a transimpedance mode and has a push-pull output capable of delivering 125 mA into a capacitively coupled 8 ohm load. This produces a two volt peak to peak output signal. The amplifier input (pin 5) can be used to sum several external current signals. If the signals are composed of a varying voltage they must first be converted to current signals. This can be accomplished by using a resistor in series between the external source and the input (pin 5). The relationship of this resistor value (R series) to the external signal voltage (V max) is given by the following equation:

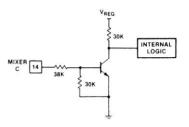
Equation 6: 100
$$\mu$$
A < Vmax - 3V/Rseries < 100 μ A

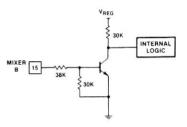
Gain of the amplifier can be controlled by adding a resistor in parallel to the internal 10 Kohm feedback resistor. This will decrease gain and allow a larger input current.

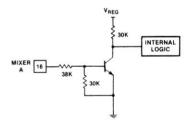
Regulator

The circuit will operate from a singe supply (pin 6). An internal 5 volt regulator allows the use of a 7.5 volt to 10.5 volt unregulated supply applied to $V_{\rm CC}$ (pin 6) and in addition to supplying power for the chip, the internal regulator will provide a 5 volt regulated supply of up to 5 mA from Vreg (pin 4) for use outside the integrated circuit.

INTERNAL CIRCUITS (Cont'd)







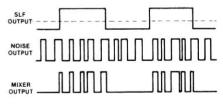


Figure 1



AUDIO POWER AMPLIFIER

380 276-706

GENERAL DESCRIPTION

The 380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

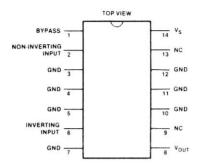
FEATURES

- · Wide supply voltage range
- · Low quiescent power drain
- · High peak current capability
- · Input referenced to GND
- · High input impedance
- · Low distortion
- Quiescent output voltage is at one-half of the supply voltage

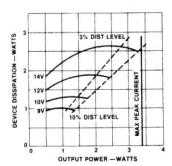
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	22 V
Peak Current	1.3 A
Package Dissipation 14-Pin DIP	10 W
Input Voltage	±0.5 V
Storage Temperature65 t	o + 150°C
Operating Temperature	to + 70°C
Junction Temperature	+ 150°C
Lead Temperature (Soldering, 10 sec)	+ 300°
Lead Temperature (Soldering, 10 sec)	

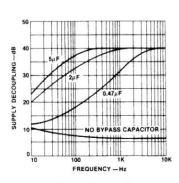
PIN CONNECTION



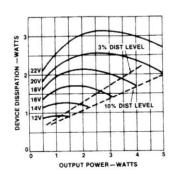
TYPICAL CHARACTERISTICS



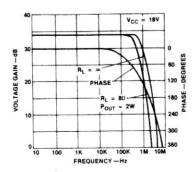
Device Dissipation vs Output Power — 4Ω Load



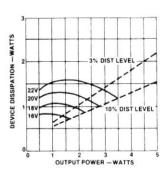
Supply Decoupling vs Frequency



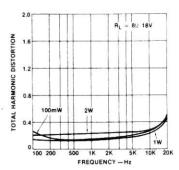
Device Dissipation vs Output Power — 8Ω Load



Output Voltage Gain and Phase vs Frequency



Device Dissipation vs Output Power — 16Ω Load

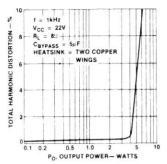


Total Harmonic Distortion vs Frequency

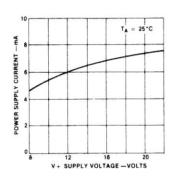
LINEAR (AUDIO)

380 276-706

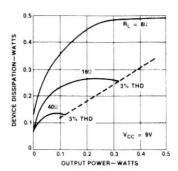
TYPICAL CHARACTERISTICS (Cont'd)



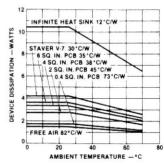
Total Harmonic Distortion vs Output Power



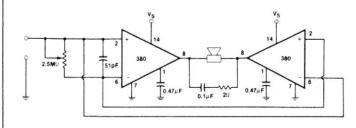
Power Supply Current vs Supply Voltage



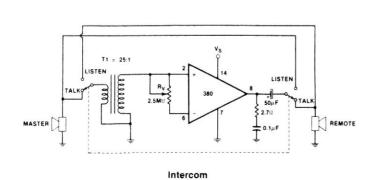
Device Dissipation vs Output Power



Device Dissipation vs Ambient Temperature



Bridge Amplifier

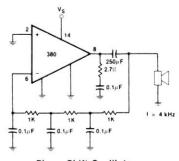


CRYSTAL CARTRIDGE

CONTROL

CO

Phono Amplifier



Phase Shift Oscillator



8 WATT AUDIO POWER AMPLIFIER

383 276-703

GENERAL DESCRIPTION

The 383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The 383 is current limited and thermally protected. The 383 comes in a 5-pin TO-220 package.

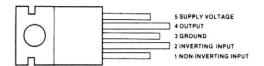
FEATURES

- High peak current capability (3.5A)
- · Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V-20V)
- · Few external parts required
- Pin for pin compatible with TDA2002

• Low distortion

- High input impedance
- No turn-on transients
- Low noise
- Short circuit protected

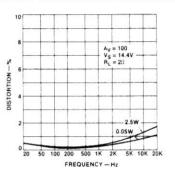
PIN CONNECTION



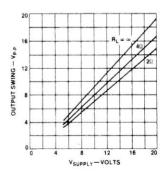
ABSOLUTE MAXIMUM RATINGS

Peak Supply Voltage (50 ms)25V
Operating Supply Voltage
Output Current
Repetitive
Non-repetitive
Input Voltage
Power Dissipation
Operating Temperature
Storage Temperature
Lead Temperature (Soldering, 10 seconds)

TYPICAL CHARACTERISTICS

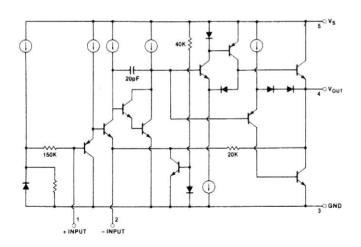


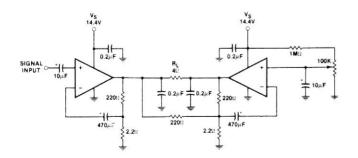
Distortion vs Frequency



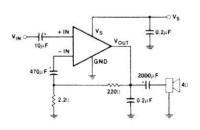
Output Swing vs Supply Voltage

INTERNAL CIRCUIT





16W Bridge Amplifier



Basic Audio Amp

386

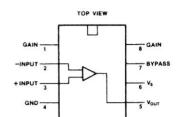
LOW VOLTAGE AUDIO POWER AMPLIFIER



GENERAL DESCRIPTION

The 386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 18 milli-watts when operating from a 6 volt supply, making the 386 ideal for battery operation.



PIN CONNECTION

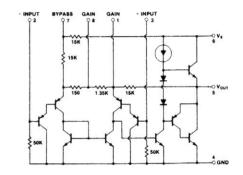
FEATURES

- · Battery operation
- Minimum external parts
- Wide supply voltage range 4-12 volts
- Low quiescent current drain 3 mA
- Voltage gains from 20 to 200

- Portable tape player amplifiers

- · Ground referenced input
- Self-centering output quiescent
- Low distortion
- · Eight pin dual-in-line package

INTERNAL CIRCUIT



APPLICATIONS

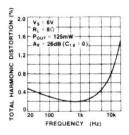
- AM-FM radio amplifiers
- Intercoms
- TV sound systems

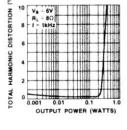
- Line drivers
- Ultrasonic drivers
- · Small servo drivers
- · Power converters

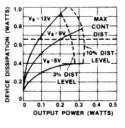
ABSOLUTE MAXIMUM RATINGS

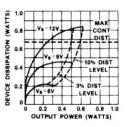
Supply Voltage
Package Dissipation 8 Pin DIP
Input Voltage
Junction Temperature
Operating Temperature 0 to +70°C
Storage Temperature65 to +150°C
Lead Temperature (Soldering. 10 seconds)+300°C

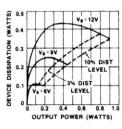
TYPICAL CHARACTERISTICS











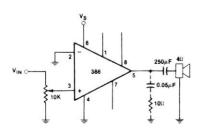
Distortion vs Frequency

Distortion vs **Output Power**

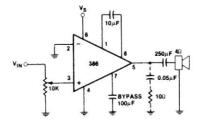
Device Dissipation vs Output Power -4Ω Load **Device Dissipation vs**

Device Dissipation vs Output Power – 8 Ω Load Output Power – 16 Ω Load

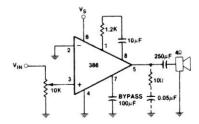
TYPICAL APPLICATIONS



Amplifier with Gain = 20 (Minimum Parts)



Amplifier with Gain = 50



Amplifier with Gain = 200



LOW NOISE DUAL PREAMPLIFIER

276-1737

8 + INPUT(2)

- INPUT(2)

5 OUTPUT(2)

PIN CONNECTION

TOP VIEW

+ INPUT(1)

OUTPUT(1)

GND -3

GENERAL DESCRIPTION

The 387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (104 dB), large output voltage swing (V_{CC} – 2 V) P.P. and wide power band width (75 kHz, 20 VP.P). The 387 operates from a single supply across the wide range of 9 to 30 V.

FEATURES

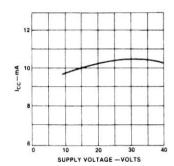
- Low noise 0.8 μV total input noise
 High gain 104 dB open loop
 Wide supply range 9 to 30 V

- Power supply rejection 110 dB
- Large output voltage swing (V_{CC} 2 V) P-P
- Wide band width 15 MHz unity gain
- Power band width 75 kHz, 20 VP-P
- · Internally compensated
- · Short circuit protected

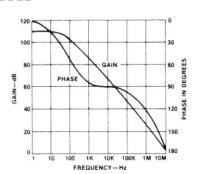
ABSOLUTE MAXIMUM RATINGS

Supply Voltage + 30 V
Operating Temperature Range
Storage Temperature Range – 65 to + 150°C
Lead Temperature (Soldering, 10 seconds)

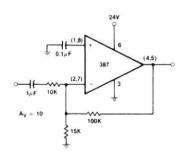
TYPICAL CHARACTERISTICS



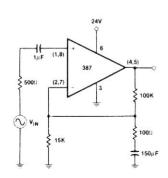
Supply Current vs Supply Voltage



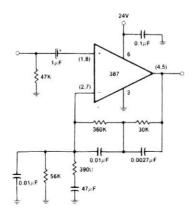
Gain and Phase Response vs Frequency



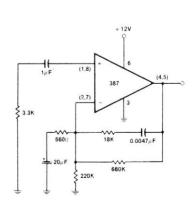
Ultra-Low Distortion Inverting Amplifier



Flat Gain Circuit $(A_V = 1000)$



Magnetic Phono Preamplifier



NAB Tape Circuit

3914 276-1707 3915 276-1708

DOT/BAR DISPLAY DRIVER



GENERAL DESCRIPTION

The 3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating resistors. This feature allows operation of the system from less then 3V. Controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many 3914s can be "chained" to form displays of segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

Individual DC regulated currents provide flexibility and various effects can be achieved by modulating these currents. Outputs can drive a transistor and a LED so controller functions including "staging" control can be performed.

The 3915 Bar/Graph Display Driver is different by a - 3db per segment logarithmic scaling compared to the linear scaling of the 3914.

The 3915 can be used with AC or DC signals. With AC (audio) inputs, the display will be quite eye-catching and informative, especially in the Dot mode. Connecting an audio signal to the signal input direct is all that is required.

FEATURES

- Bar or dot display mode externally selectable by user
- Expandable to displays of 20 steps (3915)
- Expandable to displays of 100 steps (3914)
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 to 3 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
 LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic. The internal 10step divider is floating and can be reference to a wide range of voltages

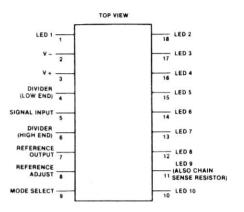
APPLICATIONS

- "Slow"—fade bar or dot display (doubles resolution)
- 20 step meter with single pot brightness control
- 10-step (nor multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Exclamation point display for power savings
- Power Meters in stereo systems
- VU Meters in tape recorders
- S meters in Ham and CB radios
- Direction and rate indicator (to add to DVMs)

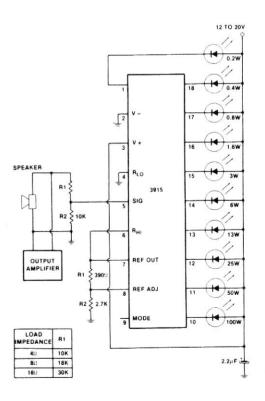
ABSOLUTE MAXIMUM RATINGS

112002012111111111111111111111111111111
Power Dissipation
V + Voltage
LED Collector Output Voltage25V
Input Signal Overvoltage
Voltage on Resistor String
Reference Load Current
Signal Input Current (With Overvoltage Applied) ±3 mA

PIN CONNECTION



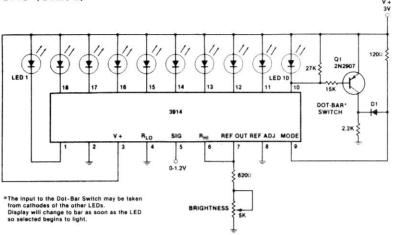
TYPICAL APPLICATIONS



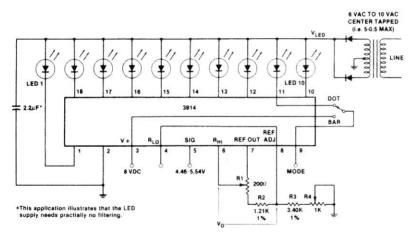
Audio Power Meter

3914 276-1707 3915 276-1708

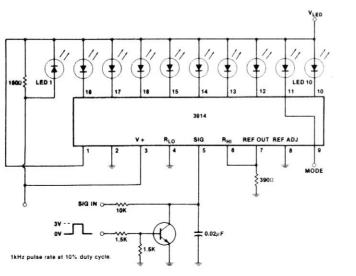
TYPICAL APPLICATIONS (Cont'd)



Indicator and Alarm



Expanded Scale Meter, Dot or Bar

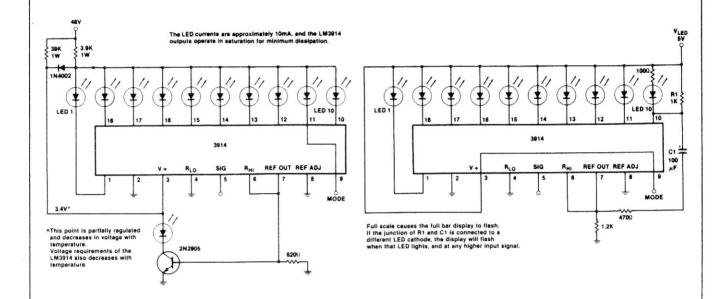


Exclamation Point Display

LINEAR (DRIVER)

3914 276-1707 3915 276-1708

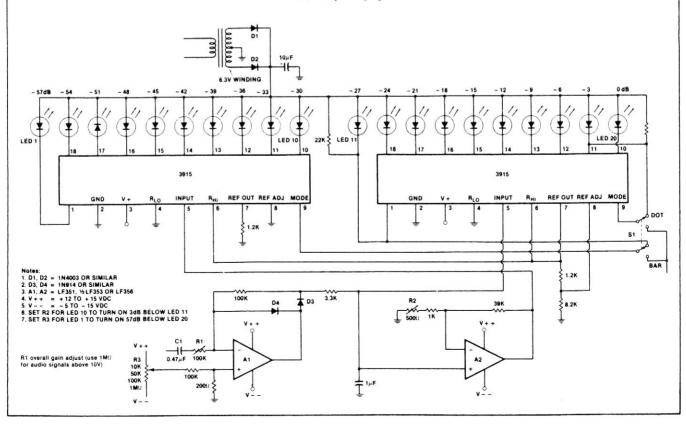
TYPICAL APPLICATIONS (Cont'd)



Operating with a High Voltage Supply

Bar Display with Alarm Flasher

Bar Graph Display





DOT/BAR DISPLAY DRIVER

276-1709

GENERAL DESCRIPTION

The 3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The 3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

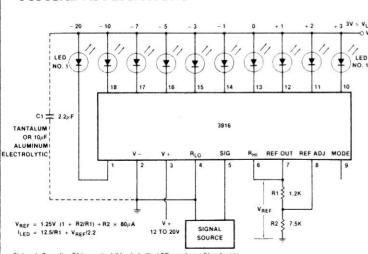
FEATURES

- · Fast responding electronic VU meter
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- · Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	3 to 25 V
Input Signal Over Voltage	± 35 V
Storage Temperature	

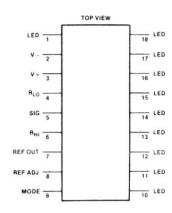
TYPICAL APPLICATIONS

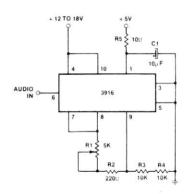


. Capacitor C1 is required if leads to the LED supply are 6" or longer.
Circuit as shown is wired for dot anode. For bar mode, connect pin 9 to pin 3.
L_{LED} must be kept below 'Y or dropping resistor should be used 10 limit IC power dissipation.

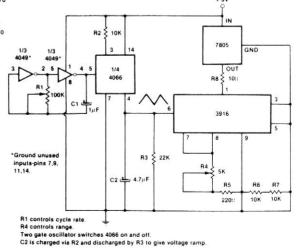
0V to 10V VU Meter

PIN CONNECTION





VU Bar Graph Display



Back and Forth Flasher

TL084CN 276-1714

QUAD BI-FET OPERATIONAL AMPLIFIER



GENERAL DESCRIPTION

The TL084 JFET-input operational amplifier is designed to offer better performance than any previously developed quad-operational amplifier. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

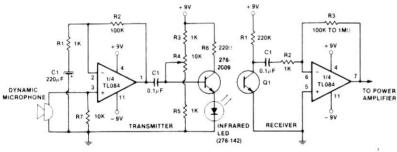
FEATURES

- Low power consumption
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- · Output short-circuit protection
- High input impedance—IFET-input stage
- Internal frequency compensation
- · Latch-up-free operation
- High slew rate 13 V/μs Typ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage. V _{CC} +
Supply Voltage, V _{CC} 18V
Differential Input Voltage
Input Voltage
Duration of Output Short Circuit
Continuous Total Dissipation at (or Below)
25°C Free-Air Temperature
Operating Free-Air Temperature Range
Storage Temperature Range65 to +150°C
Lead Temperature 1/16 inch from Case for 10 Seconds

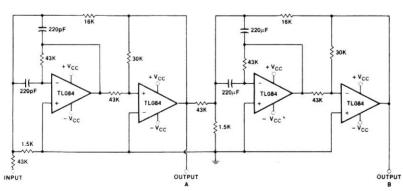
TYPICAL APPLICATIONS



Point the led at Q1 and adjust R4 until best voice quality is obtained. (R4 applies prebias to LED.) R6 limits maximum led current to a safe 40mA

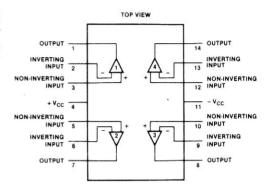
Use RADIO SHACK 276-130 phototransistor for Q1. Maximum range: Hundreds of feet at night with lenses at Q1 and LED. Power amp: See LM386

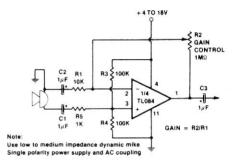
Infrared Voice Communicator



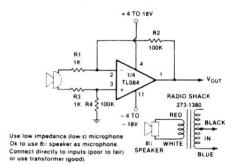
Positive-Feedback Bandpass Filter

PIN CONNECTION

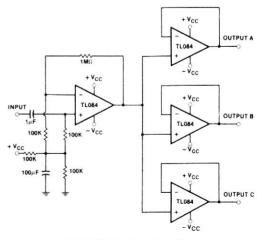




Microphone Preamplifier



Low-Z Preamplifier



Audio Distribution Amplifier



QUAD OP AMP

OUTPUT 1-

INPUT 1-

INPUT 2-

PIN CONNECTION

TOP VIEW

324 276-1711

14 OUTPUT 4

13 INPUT 4-

12 INPUT 4+

10 INPUT 3+

- INPUT 3-

OUTPUT 3

11 GND

GENERAL DESCRIPTION

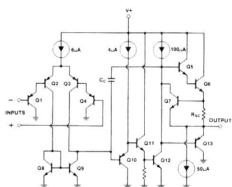
The 324 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the 324 series can be directly operated off of the standard $\pm 5~V_{DC}$ power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15~V_{DC}$ power supplies.

FEATURES

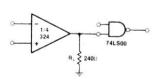
- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range: Single supply 3 V_{DC} to 30 V_{DC} or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800 μA)—essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V⁺ − 1.5 V_{DC}

INTERNAL CIRCUIT (Each Amplifier)

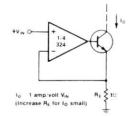


ABSOLUTE MAXIMUM RATINGS

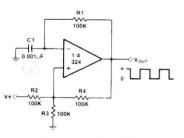
Supply Voltage, V+
Differential Input Voltage
Input Voltage. -0.3 V_{DC} to $+32 \text{ V}_{DC}$
Power Dissipation
Molded DIP
Cavity DIP900 nW
Output Short-Circuit to GND (One Amplifier)
$V^* \leq 15 \text{ V}_{DC} \text{ and } T_A = 25^{\circ}\text{C}$
Input Current $(V_{IN} \le -0.3 V_{OL})$
Operating Temperature Range
Storage Temperature Range
Lead Temperature (Soldering, 10 seconds)



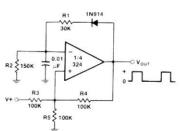
Driving TTL



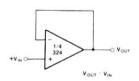
High Compliance Current Sink



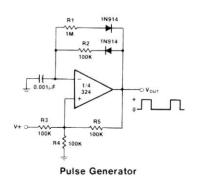
Squarewave Oscillator



Pulse Generator



Voltage Follower



353 276-1715

WIDE BANDWIDTH DUAL JEET INPUT OPERATIONAL AMPLIFIER



GENERAL DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II^m) technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents.

These amplifers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

FEATURES

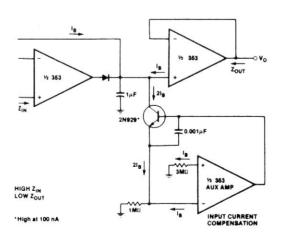
- Internally trimmed offset voltage = 2 mV
- Low input bias current = 50pA

- Wide gain bandwidth = 4 MHz
- High slew rate = 13 V/μs
- Low supply current = 3.6 mA
- High input impedance = $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$,
- $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20kHz = < 0.02%
- Low 1/f noise corner = 50 Hz
- fast settling time to $0.0\% = 2\mu s$

ABSOLUTE MAXIMUM RATINGS

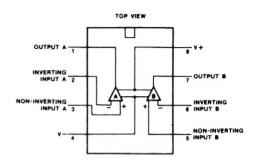
Supply Voltage
Power Dissipation
Differnetial Input Voltage±30V
Input Voltage Range
Output Short Circuit Duration
T _{i(MAX)}
Operating Temperature Range
Storage Temperature Range65 to +150°C
Lead Temperature (Soldering, 10 seconds)300°C

TYPICAL APPLICATIONS

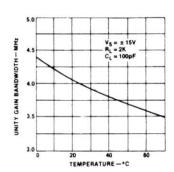


Low Drift Peak Detector

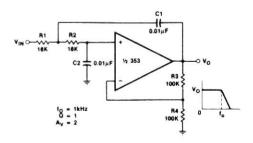
PIN CONNECTION



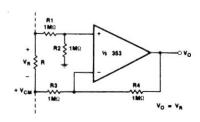
TYPICAL CHARACTERISTICS



Unity Gain Bandwidth vs Temperature



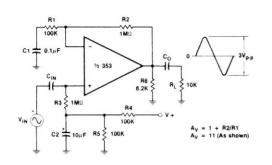
DC Coupled Low-Pass RC Active Filter

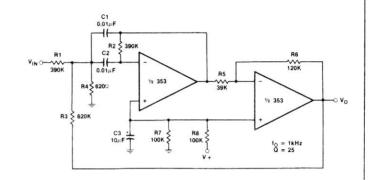


Ground Referencing A Differential Input Signal

353 276-1715

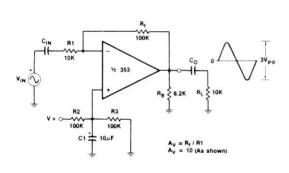
TYPICAL APPLICATIONS (Cont'd)

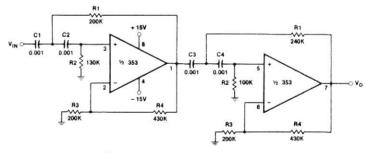




AC Coupled Non-Inverting Amplifier

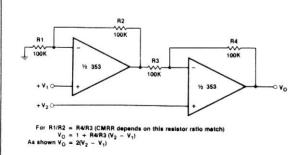
Bandpass Active Filter

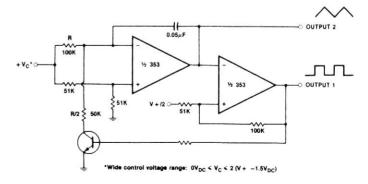




AC Coupled Inverting Amplifier

Fourth Order High Pass Butterworth Filter





High Input Z, DC Differential Amplifier

Voltage Controlled Oscillator (VCO)

741 276-007

OPERATIONAL AMPLIFIER



GENERAL DESCRIPTION

The 741 series are general purpose operational amplifiers which feature im-

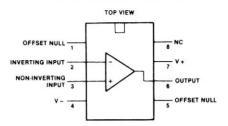
proved performance over industry standards.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded. as well as freedom from oscillations.

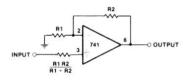
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V
Power Dissipation	V
Differential Input Voltage	V
Input Voltage	V
Output Short Circuit Duration	e
Operating Temperature Range	\mathbb{C}
Storage Temperature Range65 to +150°C	3
Lead Temperature (Soldering, 10 seconds)	3

PIN CONNECTION

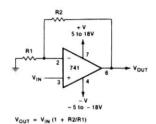


TYPICAL APPLICATIONS

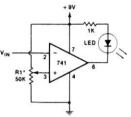


GAIN	R1	R2	вw	RIN
10	18	9К	100kHz	400M:
100	100:	9.9K	10kHz	280M:
1000	100:	99.9K	1kHz	80M:

Non-Inverting Amplifier



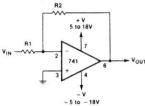
Non-Inverting Amplifier



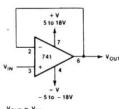
Level Detector

*R1 sets the voltage detection threshold (up to +9V).

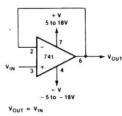
When V_{IN} exceeds the threshold (reference), the LED glo

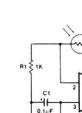


Inverting Amplifier



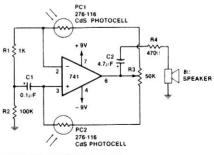
Unity Gain Follower





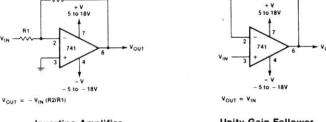


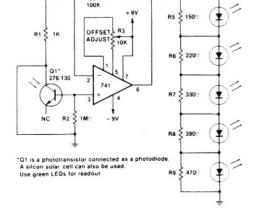
*Adjust R3 to just below oscillation point. Adjust R2 and R3 for sounds such as bell, drum, tinkling, etc.



Bargraph Light Meter

Audible Light Sensor







DUAL OPERATIONAL AMPLIFIER

1458 276-038

GENERAL DESCRIPTION

The 1458 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

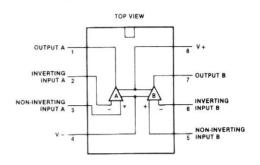
FEATURES

- · No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- No latch up when input common mode range is exceeded

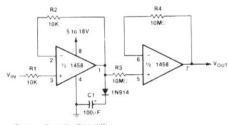
ABSOLUTE MAXIMUM RATINGS

Supply Voltage.	±16V
Power Dissipation	400 mW
Differential Input Voltage	±30V
Input Voltage	±15V
Output Short-Circuit Duration.	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range65	to +150°C
Storage Temperature Range	300°C
Lead Temperature (Soldering, 10 sec)	300 C

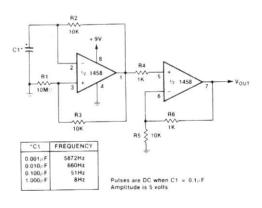
PIN CONNECTION



TYPICAL APPLICATIONS

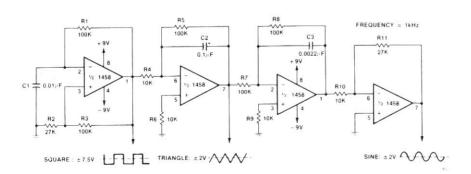


C1 stores the peak voltage at $\mathbf{V}_{\text{IN}}.$



Peak Detector

Pulse Generator



Function Generator

3900 276-1713

QUAD OPERATIONAL NORTON AMPLIFIER



GENERAL DESCRIPTION

The 3900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers. RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed. high voltage digital logic gates.

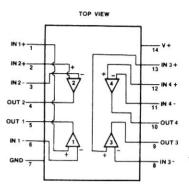
FEATURES

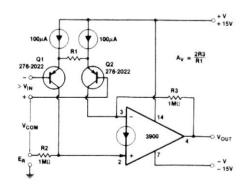
- ullet Wide single supply voltage 4 V_{DC} to 36 V_{DC} range or dual supplies $\pm 2~V_{DC}$ to
- Supply current drain independent of supply voltage
- Low input biasing current 30 nA
- High open-loop gain 70 dB
- Wide bandwidth 2.5 MHz (Unity Gain)
- Large output voltage swing (V+ -1) V_{p-p}
 Internally frequency compensated for unity gain
- Output short-circuit protection

ABSOLUTE MAXIMUM RATINGS

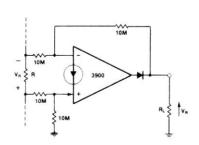
Supply Voltage (Wide Range, Single Supply)
Supply Voltage (Wide Range, Dual Supply)
Power Dissipation ($T_A = 25^{\circ}C$)
Flat Pack
Input Currents, I _{IN} + or I _{IN}
Output Short-Circuit Duration—One Amplifier
$T_A = 25$ °C (See Application Hints)
Operating Temperature Range
Storage Temperature Range
Lead Temperature (Soldering, 10 seconds)

PIN CONNECTION

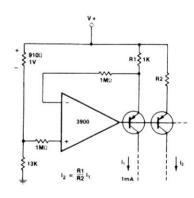




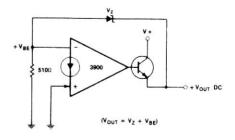
Basic Instrumentation Amplifier



Ground-Referencing a Differential Input Signal



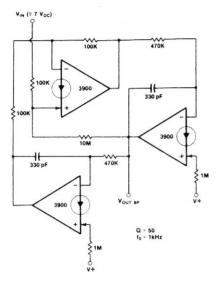
Fixed Current Sources



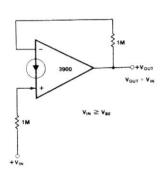
Voltage Regulator

3900 276-1713

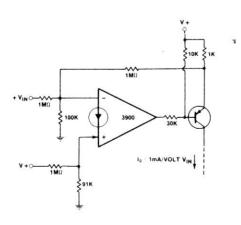
TYPICAL APPLICATIONS (Con't)



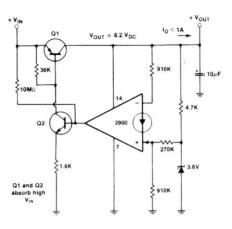
Bi-Quad Active Filter (2nd Degree State-Variable Network)



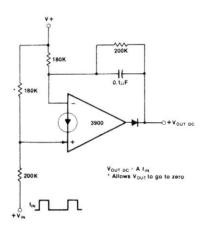
Buffer Amplifier



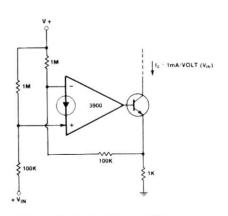
Voltage Controlled Current Source (Transconductance Amplifier)



High V_{IN} , Low $(V_{IN} - V_{OUT})$ Self Regulator



Tachometer



Voltage-Controlled Current Sink (Transconductance Amplifier)

555 276-1723

TIMER



GENERAL DESCRIPTION

The 555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

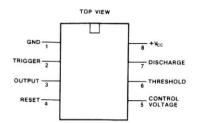
FEATURES

- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- · Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

APPLICATIONS

- Precision timing • Pulse generation
- Time delay generation
- · Pulse width Sequential timing
 - modulation
- Pulse position
- modulation
- Linear ramp generator

PIN CONNECTION



TRUTH TABLE

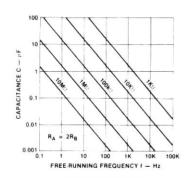
PIN 2 TRIGGER	PIN 6 THRESHOLD	PIN 4 RESET	PIN 3 OUTPUT
Н	X	Н	L
L	X	Н	Н
Н	L	Н	L
X	X	L	L

X = Don't Care L = Low Level H = High Level

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 16V
Power Dissipation	600 mW
Operating Temperature Range	
Storage Temperature Range65	
Lead Temperature (Soldering, 10 seconds)	300°C

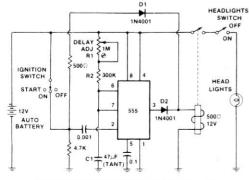
TYPICAL CHARACTERISTICS



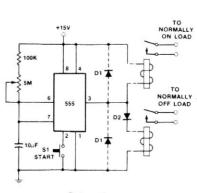
The charge time (output high) is given by: $t_1=0.693~(R_A+R_B)~C$ The discharge time (output low) is given by: $t_2=0.693~(R_B)~C$ Thus the total period is: $T=t_1+t_2=0.693~(R_A+2R_B)~C$ The frequency of oscillation is: $f=i/T=1.44~\ell(R_A+2R_B)~C$

Capacitance vs Free-Running Frequency

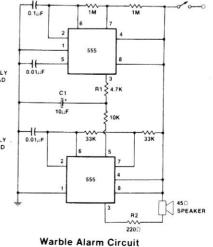
TYPICAL APPLICATIONS



Automatic Headlight Turn-Off Circuit



Relay Timer





GENERAL DESCRIPTION

The 556 dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only $V_{\rm CC}$ and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

FEATURES

- · Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

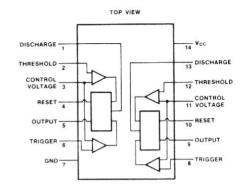
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation

DUAL TIMER

556 276-1728

PIN CONNECTION



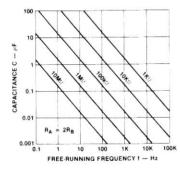
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+16V
Power Dissipation) mW
Operating Temperature Range 0 to	-70°C
Storage Temperature Range65 to +	150°C
Lead Temperature (Soldering, 10 seconds)	

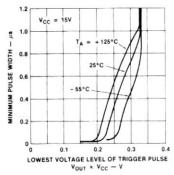
• Pulse width modulation Pulse position modulation

Linear ramp generator

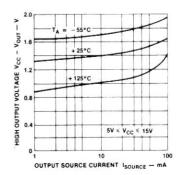
TYPICAL CHARACTERISTICS



The charge time (output high) is given by: $t_1=0.893\,(R_A+R_B)\,C$ The discharge time (output low) is given by: $t_2=0.893\,(R_B)\,C$ Thus the total period is: $T=t_1+t_2=0.693\,(R_A+2R_B)\,C$ The trequency of oscillation is: $t=1/T=1.44\,/\,(R_A+2R_B)\,C$

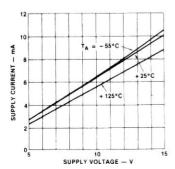


Minimum Pulse Width vs Lowest Voltage Level of Trigger Pulse



High Output Voltage vs **Output Source Current**

Capacitance vs Free-Running Frequency



Supply Current vs Supply Voltage

MC1330 276-1757

LOW-LEVEL VIDEO DETECTOR



GENERAL DESCRIPTION

This is an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band. > 8.0 MHz. with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

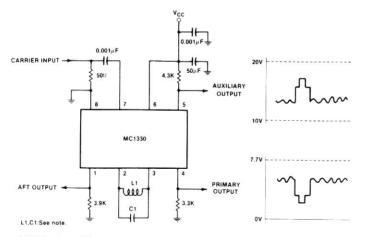
FEATURES

- Conversion gain 33 dB typical
- Excellent differential phase and gain
- · High rejection of IF carrier feedthrough
- High video output-8.0 V p-p
- Fully balanced detector.
- Output temperature compensated

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
DC Video Output Current5mAdc
DC AFT Output Current
Zero Signal dc Output Voltage (V_{cc} =+20 Vdc, Q=40, f_c =45.75 MHz)
MC1330A1P8.2 Vdc
MC1330A2P9.0 Vdc
Supply Current
Maximum Signal dc Output Voltage (Pin 4)
Conversion Gain for 1Vp-p Output (30% Modulation)
AFT Buffer Output at Carrier Frequency
Junction Temperature
Operating Temperature Range (Ambient)
Storage Temperature Range65 to +150°C

TYPICAL APPLICATIONS



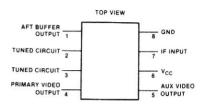
NOTE: The choice of Q for the funed circuit of pins 2 and 3 is not critical.

The higher the Q, the better the rejection of 920 kHz products but the more critical the funing accuracy required. See Figure 3.

Values of Q from 20 to 50 recommended. (Note the internal resistance.)

Test Fixture Circuit

PIN CONNECTION



TYPICAL CHARACTERISTICS $(V_{cc} = +20 \text{ Vdc})$

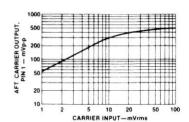


Figure 1

AFT Carrier Output
vs Carrier Input

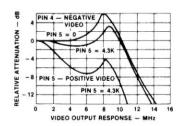
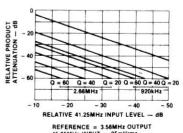


Figure 2
Relative Attenuation vs
Video Output Response



REFERENCE = 3.58MHz OUTPUT 45.75MHz INPUT = 25mVrms 42.17MHz INPUT = 12.5mVrms 41.25MHz INPUT — RELATIVE TO 45.75 MHz INPUT = 4.5MHz

Figure 3
Relative Product Attenuation vs
Relative 41.25 MHz Input Level

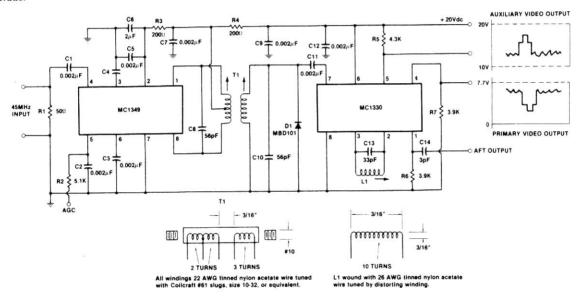
MC1330 276-1757

TYPICAL APPLICATIONS (Cont'd)

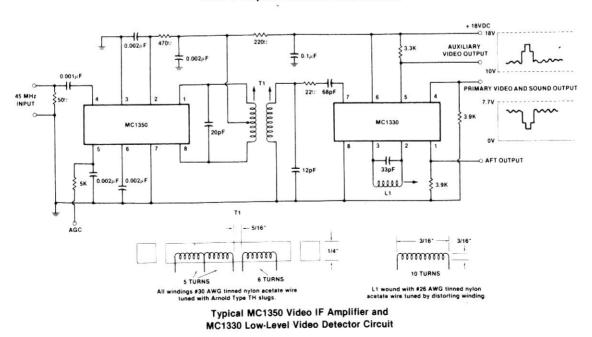
Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude.



Video IF Amplifier and Low-Level Detector





IF AMPLIFIER



GENERAL DESCRIPTION

This monolithic IF amplifier is an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV.

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FEATURES

- Power gain 50 dB typ at 45 MHz.
 - 48 dB typ at 58 MHz
- AGC range 60 dB min. dc to 45 MHz
- Nearly constant input and output admittance over the entire AGC range
- y₂₁ constant (-3.0 dB) to 90 MHz
- Low reverse transfer admittance << 1.0 μmho typ
- 12-volt operation, single-polarity-power supply

ABSOLUTE MAXIMUM RATINGS

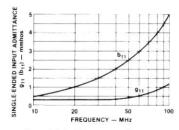
Power Supply Voltage	.8Vdc
Power Dissipation	5mW
Operating Temperature Range	

ELECTRICAL CHARACTERISTICS

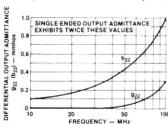
 $(V + = +12 \text{ Vdc}; T_A = +25^{\circ}\text{C unless otherwise noted})$

Power Gain (Pin 5 grounded via a 5.1k resistor)	
f = 58 MHz. BW = 4.5 MHz	18dB
f = 45 MHz. BW = 4.5 MHz	50dB
f = 10.7 MHz, BW = 350 kHz	58dB
f = 455 kHz, BW = 20 kHz	32dB
Power Dissipation	mW

TYPICAL CHARACTERISTICS (V+=12V, T_A =+25°C)

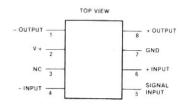


Input Admittance vs Frequency

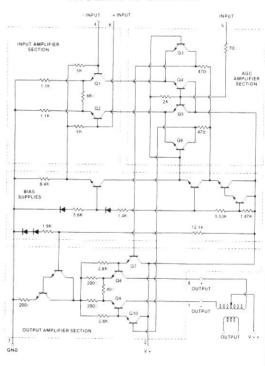


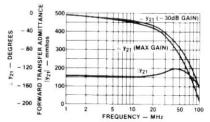
Differential Output Admittance vs Frequency

PIN CONNECTION

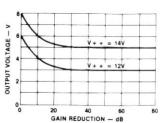


INTERNAL CIRCUIT





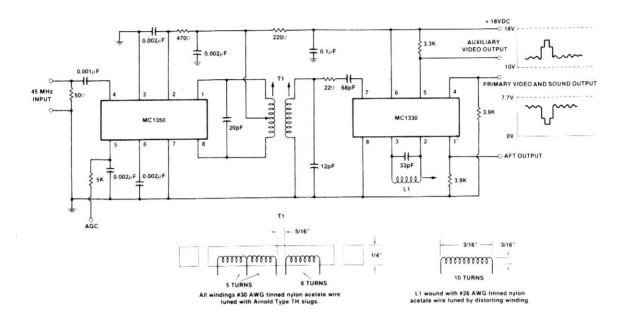
Forward Transfer Admittance and Phase vs Frequency



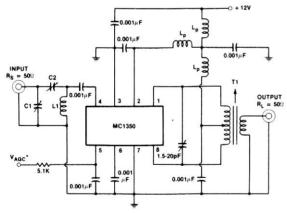
Differential Output Voltage vs Gain Reduction

MC1350 276-1758

TYPICAL APPLICATIONS



Typical MC1350 Video IF Amplifier and MC1330 Low-Level Video Detector Circuit



*Connect to ground for maximum power gain test.

All power-supply chokes (L_p), are self-resonate at input frequency. L_p ≥ 20K
Li @ 45 MHz = 7½ turns on a ½" coil form.
@ 55 MHz = 6 turns on a ½" coil form.
Ti primary winding = 18 turns on a ½" coil form, center-tapped.
secondary winding = 2 turns can abra coil form, center-tapped.
= 1 turn @ 58MHz

Core = Arnold TH material ½" long.

- [45MHz		MHz 58M	
L1	0.4μΗ	Q ≥ 100	0.3μΗ	Q ≥ 100
T1	1.3-3.4µH	Q ≥ 100 @ 2µH	1.2·3.8µH	Q ≥ 100 @ 2µH
C1	50-160pF		8-	-60pF
C2	8-60pF		3-	35pF

Power Gain, AGC, and Noise Figure Test Circuit (45 MHz and 58 MHz)

INPUT R _S = 50Ω L1 C	:3 📮		Ţ	C4 7	0 12V
C1 # C2#	4 3	2 1		Tangan Land	F OUTPUT R _L = 500
V _{AGC} *	5 6	7 8	≠ c5	(SEE NOTES)	
	TI	<u></u>	-		

Note 1. Primary = 120µH, center-tapped.

O_u = 140 at 455kHz.

Primary: Secondary turns ratio = 13

2. Primary = 6,0µH

Primary winding = 24 turns #36 AWG, close wound on ¼* diameter form.

Secondary winding = 1½ turns #36 AWG, ¼* diameter, wound over center-tap.

Core = Arnold type TH, or equivalent.

	FREQUENCY		
COMPONENT	455kHz	10.7MHz	
C1	_	80-450pF	
C2	-	5-80pF	
C3	0.05µF	0.001µF	
C4	0.05µF	0.05µF	
C5	0.001µF	36pF	
C6	0.05µF	0.05µF	
C7	0.05µF	0.05µF	
L1	-	4.6µH	
T1	NOTE 1	NOTE 2	

Power Gain and AGC Test Circuit (455 kHz and 10.7 MHz)



IF AMPLIFIER, LIMITER, FM DETECTOR AUDIO DRIVER, ELECTRONIC ATTENUATOR



GENERAL DESCRIPTION

This TV sound IF amplifier is a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

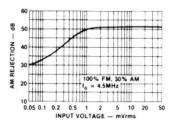
FEATURES

- Differential peak detector requiring a single tuned circuit
- Electronic attenuator replaces conventional ac volume control Range > 60 dB
- Excellent AM rejection at 4.5 and 5.5 MHz
- · High stability
- Low harmonic distortion
- Audio drive capability 6.0 mAp-p
- Minimum undesirable output signal @ maximum attenuation

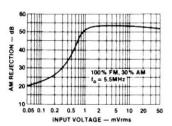
ABSOLUTE MAXIMUM RATINGS

Input Signal Voltage (Pins 1 and 2)	±3.0Vdc
Power Supply Current	50mA
Power Dissipation	625mW
Operating Temperature Range (Ambient)	-20 to +75°C
Storage Temperature Range	-65 to +150°C

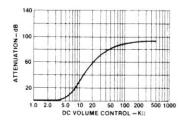
TYPICAL CHARACTERISTICS



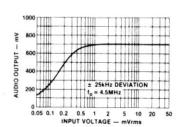
AM Rejection vs Input Voltage



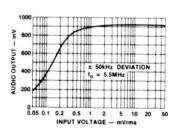
AM Rejection vs Input Voltage



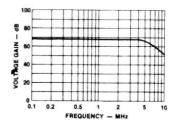
Attenuation vs DC Volume Control



Audio Output vs Input Voltage

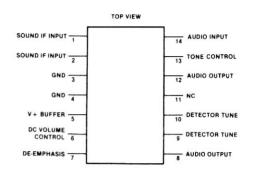


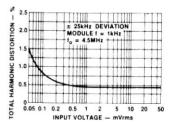
Audio Output vs Input Voltage



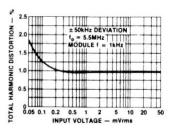
Voltage Gain vs IF Frequency

PIN CONNECTION

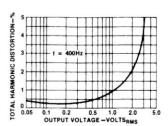




Total Harmonic Distortion vs Input Voltage



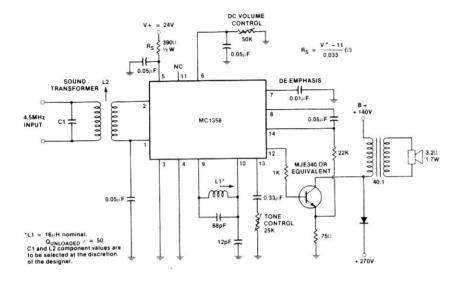
Total Harmonic Distortion vs Input Voltage



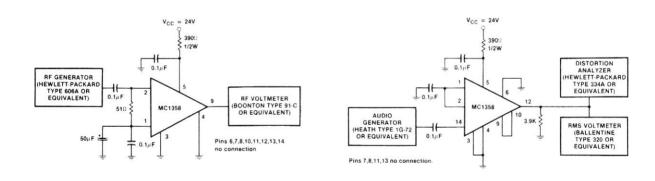
Total Harmonic Distortion vs Output Voltage

MC1358 276-1759

TYPICAL APPLICATIONS

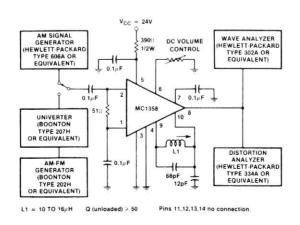


TV Application



IF Frequency Response Test Circuit

Audio Voltage Gain, Audio THD Test Circuit



AM Rejection, Detected Audio, THD, Attenuation Test Circuit

317T 276-1778

3-TERMINAL ADJUSTABLE POSITIVE REGULATOR

GENERAL DESCRIPTION

The 317T is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 1.5 A over a 1.2 V to 37 V output range. This device is exceptionally easy to use and requires only two external resistors to set the output voltage.

In addition to higher performance than fixed regulators, the 317T offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the 317T is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

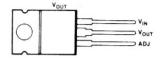
It will also serve as a simple adjustable switching regulator, programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the 317T can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2 V where most loads draw little current.

FEATURES

- Adjustable output down to 1.2V
- Guaranteed 1.5A outpput current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

PIN CONNECTIONS

FRONT VIEW



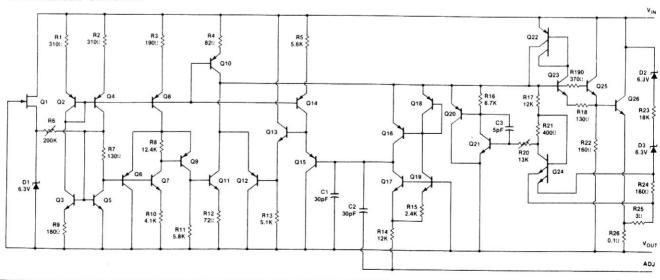


317T

ABSOLUTE MAXIMUM RATINGS

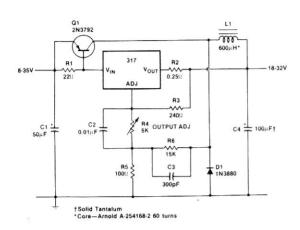
Power Dissipation	y limited
Input-Output Voltage Differential	
Operating Junction Temperature Range	+125°C
Storage Temperature65 to	+150°C
Lead Temperature (Soldering 10 seconds)	300°C

INTERNAL CIRCUIT

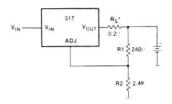


317T 276-1778

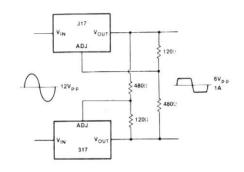
TYPICAL APPLICATIONS



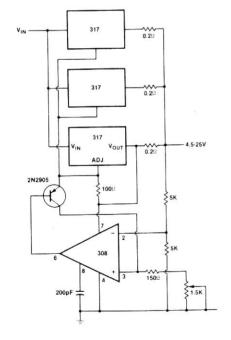
Low Cost 3A Switching Regulator



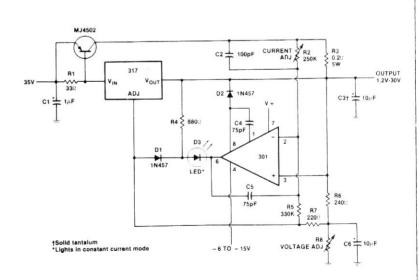
12V Battery Charger



AC Voltage Regulator



Adjustable 4A Regulator



5A Constant Voltage/Constant Current Regulator

723 276-1740

ADJUSTABLE VOLTAGE REGULATOR



GENERAL DESCRIPTION

The 723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA: but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

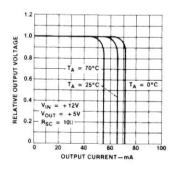
FEATURES

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

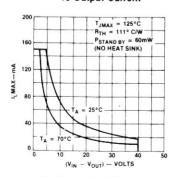
The 723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

ABSOLUTE MAXIMUM RATINGS

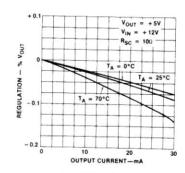
TYPICAL CHARACTERISTICS



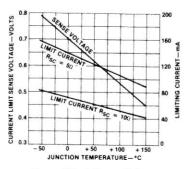
Relative Output Voltage vs Output Current



Maximum Load Current vs Input-Output Voltage Differential

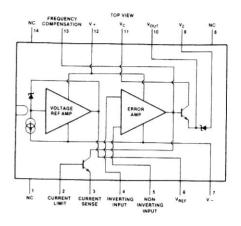


Load Regulation vs Output Current

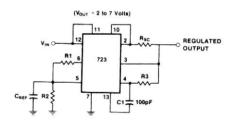


Current Limit Sense Voltage vs Junction Temperature

PIN CONNECTION

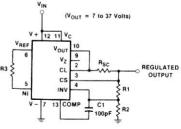


TYPICAL APPLICATIONS



Note: R3 = R1 R2 for minimum temperature drift

Basic Low Voltage Regulator



TYPICAL PERFORMANCE Regulated Output Voltage 15V Line Regulation (Δ V_{IN} = 3V) 1.5mV Load Regulation (Δ I_L = 50mA) 4.5mV

Note: R3 = $\frac{R1R2}{R1 + R2}$ for minimum temperature drift

Basic High Voltage Regulator

5V VOLTAGE REGULATOR 12V VOLTAGE REGULATOR 15V VOLTAGE REGULATOR

GENERAL DESCRIPTION

This series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation. HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

This series will allow over 1.5A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

FEATURES

•	Internal their	rmal overload protection
	No external	components required

- · Output transistor safe area protection
- · Internal short circuit current limit

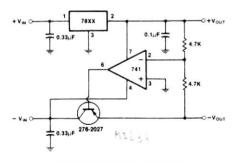
VOLTAGE RANGE

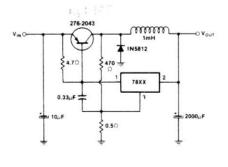
7805	٠		•			ė	•	8	٠		8		. 5V
7812	٠								•				12V
7815													

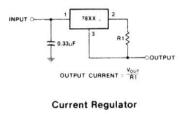
ABSOLUTE MAXIMUM RATINGS

Input Voltage
(Output Voltage Options 5V through 18V)
(Output Voltage Option 24V)
Internal Power Dissipation Internally Limited
Maximum Junction Temperature
Operating Temperature Range 0 to +70°C
Storage Temperature Range
Lead Temperature (Soldering, 10 seconds)

TYPICAL APPLICATIONS

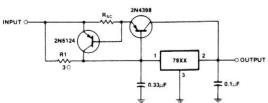




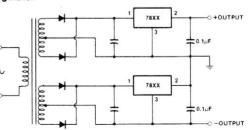


±Tracking Voltage Regulator

Switching Regulator



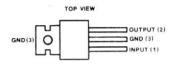




High Output Current, Short Circuit Protected

Positive and Negative Regulator

PIN CONNECTION





3-TERMINAL NEGATIVE REGULATOR

GENERAL DESCRIPTION

This regulator employs internal current limiting, safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the 7905 allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of this device ensures good regulation in the voltage boosted mode.

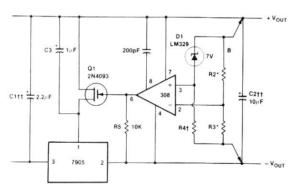
FEATURES

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

ABSOLUTE MAXIMUM RATINGS

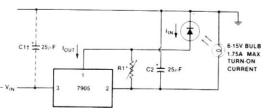
Input Voltage $(V_0 = 5V)$	-35 V
Input/Output Differential ($V_0 = 5V$)	25 V
Power Dissipation Internally I	Limited
Operating Temperature Range 0 to	+125°C
Storage Temperature Range65 to	+150°C
Lead Temperature (Soldering. 10 seconds)	. 230°C

TYPICAL APPLICATIONS



- Load and line regulation <0.01%, temperature stability $\leqslant0.2\%$
- tt Solid tantalum
- *Select resistors to set output voltage. 2ppm/°C tracking suggested

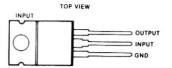
High Stability 1 Amp Regulator

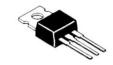


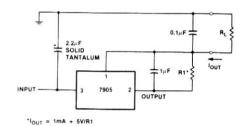
*Lamp brightness increases until I_{1N} = I_{QUT} (= 1mA) + 5V/R1. † Necessary only if raw supply filter capacitor is more than 2° from LM790SCT

Light Controller Using a Silicon Photo Cell

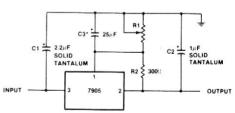
PIN CONNECTION





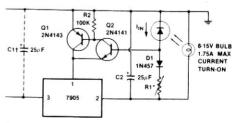


Current Source



- *Improves transient response and ripple rejection. Do not increase beyond 50μ F. $V_{OUT} = V_{SET}(\frac{R1+R2}{R2})$

Variable Output



amp brightness increases until $I_{IN} = 5V/R1$ (I_{IN} can be set as low as $1\mu A$). † Necessary only if raw supply filter capacitor is more than 2" from LM7905CT.

Light Controller Using a Silicon Photo Cell

3-TERMINAL NEGATIVE REGULATOR

7912 276-1774

GENERAL DESCRIPTION

This negative 12 V regulator employs current limiting, thermal shutdown, and safe-area compensation—making it remarkably rugged under most operating conditions with adequate heat-sinking it can deliver output currents in excess of 1.0 ampere.

FEATURES

- · No external components required
- Internal thermal overload protection
- Internal short-circuit current limiting
- Output transistor safe-area compensation

ABSOLUTE MAXIMUM RATINGS

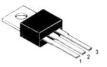
Input Voltage ($V_0 = -12 \text{ V}$)40	V
Input-Output Differential ($V_O = -12 \text{ V}$)	V
Dropout Voltage (T ₁ = 25°C, I _{out} = 1A	
Output Voltage ($T_1 = 25$ °C)12.5	V
Line Regulation Voltage	
Quiescent Current ($T_1 = 25$ °C)3 m	A
Power Dissipation Internally Limite	ed
Operating Temperature Range0°C To +125°	C
Storage Temperature Range65°C To +150°	C

DESIGN CONSIDERATIONS

This device is designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitator should be selected to provide good high-frequence characteristics to insure stable operation under all load conditions. A 0.33 uF or larger tantalum, mylar or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators inputs terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

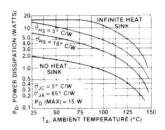
PIN CONNECTION

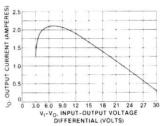


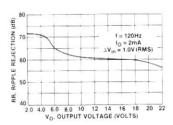
(Heat sink surface connected to Pin 2)

N 1. Ground 2. Input 3. Output

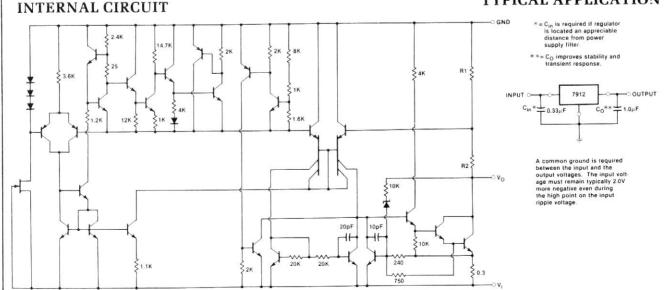
TYPICAL CHARACTERISTICS







TYPICAL APPLICATION





PRECISION WAVEFORM GENERATOR/ VOLTAGE CONTROLLED OSCILLATOR

GENERAL DESCRIPTION

The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations.

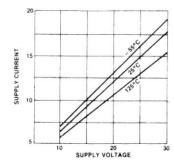
FEATURES

- Low frequency drift with temperature 50ppm/°C
- · Simultaneous sine, square, and triangle wave outputs
- Low distortion 1% (sine wave output)
- High linearity 0.1% (triangle wave output)
- Wide operating frequency range 0.001Hz to 0.3MHz
- Variable duty cycle 2% to 98%
- High level outputs TTL to 28 V
- Easy to use just a handful of external components required

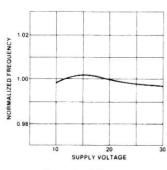
ABSOLUTE MAXIMUM RATINGS

Supply Voltage
Power Dissipation
Input Voltage (any pin) Not To Exceed Supply Voltages
Input Current (Pins 4 and 5)
Output Sink Current (Pins 3 and 9)25 mA
Storage Temperature Range
Lead Temperature (Soldering, 10 sec.)

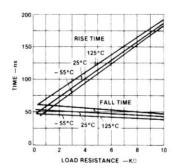
TYPICAL CHARACTERISTICS



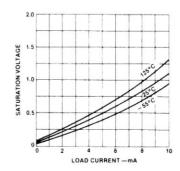
Supply Current vs Supply Voltage



Normalized Frequency vs Supply Voltage



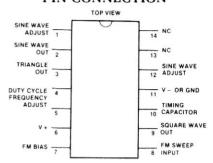
Time vs Load Resistance

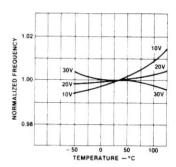


Saturation Voltage vs Load Current

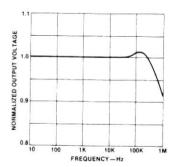
Performance of the Square-Wave Output

PIN CONNECTION

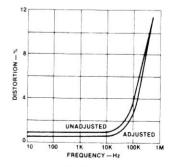




Normalized Frequency vs Temperature



Normalized Output Voltage vs Frequency



Distortion vs Frequency Performance of the Sine-Wave Output

ICL8038 276-2334

TEST CIRCUIT

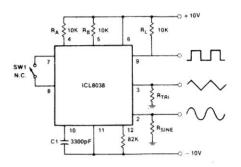
Selecting RA, RB AND C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than $1\mu A$ are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of $10\mu A$ to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R1 \times V_{SUPPLY}}{(R1 + R2)} \times \frac{1}{R_A} = \frac{V_{SUPPLY}}{5R_A}$$

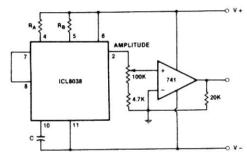
A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

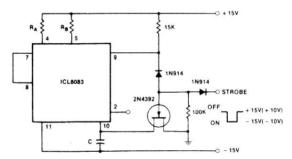


Test Circuit

TYPICAL APPLICATIONS



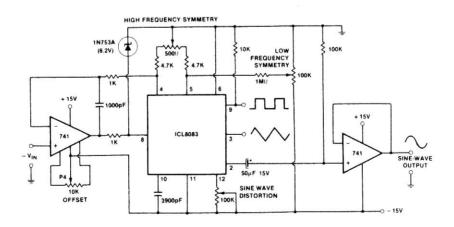
The sine wave output has a relatively high output impedance (1kt) typical). This circuit provides buffering, gain and amplitude adjustment. A simple op amp



With a dual supply voltage the external capacitor on pin 10 can be shorted to ground to halt the 8083 oscillation. This application uses a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the

Sine Wave Output Buffer Amplifier

Strobe-Tone Burst Generator



Linear Voltage Controlled Oscillator

XR-2206 276-2336

MONOLITHIC FUNCTION GENERATOR



GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1MHz.

The XR-2206 is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000: 1 frequency range with an external control voltage with very little affect on distortion.

The monolithic circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog multiplier and sine-shaper, a unity gain buffer amplifier; and a set of current switches. The internal current switches transfer the oscillator current to any one of the two external timing resistors to produce two discrete frequencies selected by the logic level at the FSK input terminal (pin 9).

FEATURES

- Low Sinewave Distortion (THD .5%—insensitive to signal sweep
- Excellent Stability (20 ppm/°C, typ)
- Wide Sweep Range (2000:1, typ)
- Low Supply Sensitivity (0.01%/V, typ)
- Linear Amplitude Modulation
- Adjustable Duty-Cycle (1% to 99T)
- TTL Compatible FSK Controls
- Wide Supply Range (10V To 26V)

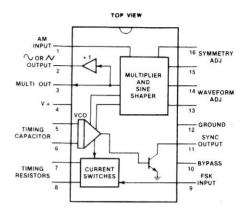
APPLICATIONS

- Waveform Generation Sine, Square, Triangle, Ramp
- Sweep Generation
- AM/FM Generation
- FSK and PSK Generation
- Voltage-to-Frequency Conversion
- Tone Generation
- · Phase-Locked Loops

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Single Supply	6 V
Split Supply±1	3 V
Supply Current $(R_1 \ge 10K\Omega)$	mA
Power Dissipation	mW
Operating Temperature Range	5°C
Storage Temperature Range65°C To + 150)°C

PIN CONNECTION



TEST CIRCUIT

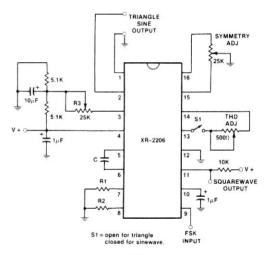


Figure 1

TYPICAL CHARACTERISTICS

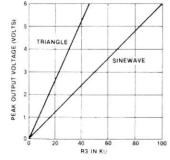


Figure 2—Output Amplitude as a Function of Resistor R3 at Pin 3.

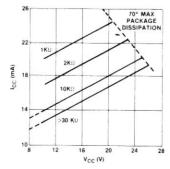


Figure 3—Supply Current vs Supply Voltage, Timing R

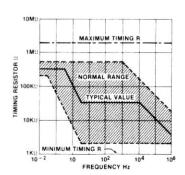


Figure 4-R vs Oscillation Frequency

XR-2206 276-2336

TYPICAL CHARACTERISTICS (Cont'd)

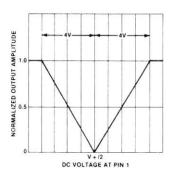


Figure 5—Normalized Output Amplitude vs DC Bias at AM Input (Pin 1).

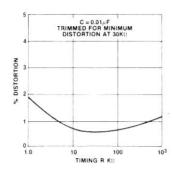


Figure 6—Trimmed Distortion vs Timing Resistor

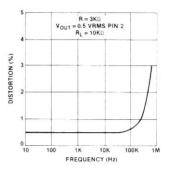


Figure 7—Signwave Distortion vs Operating Frequency With Timing Capacitors Varied

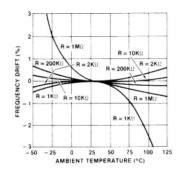


Figure 8—Frequency Drift vs Temperature

TYPICAL APPLICATIONS

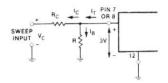


Figure 9—Circuit Connection for Frequency Sweep

DESCRIPTION OF CIRCUIT CONTROLS FREQUENCY OF OPERATION

The frequency of oscillation, f_o , is determined by the external timing capacitor C across pins 5 and 6, and by the timing resistor R connected to either pin 7 or pin 8. The frequency is given as:

$$f_O = \frac{1}{RC} Hz$$

and can be adjusted by varying either R or C. The recommended values of R for a given frequency range are shown in Figure 4. Temperature-stability is optimum for $4K\Omega < R < 200~K\Omega.$ Recommended values of C are from 1000 pF to 100 $\mu F.$

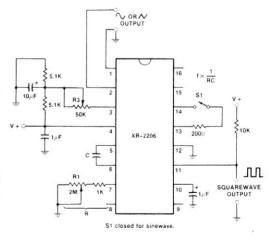


Figure 10—Circuit for Sinewave Generation Without External Adjustment (See Fig. 2 for choice of R3)

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FREQUENCY SWEEP AND MODULATION

Frequency of oscillation is proportional to the total timing current I_T drawn from pin 7 or 8

$$f = \frac{320I_T (mA)}{C (\mu F)} Hz$$

Timing terminals (pins 7 or 8) are low impedance points and are internally biased at +3V, with respect to pin 12. Frequency varies linearly with I_T over a wide range of current values, from 1 μ A to 3mA. The frequency can be controlled by applying a control voltage, V_C , to the activated timing pin as shown in Figure 9. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC} \left[1 + \frac{R}{RC} \left(1 - \frac{V_C}{3} \right) \right] Hz$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f/\partial V_C = -\frac{0.32}{R_C C} Hz/V$$

NOTE: For safe operation of the circuit, I_T should be limited to <3 mA.

TYPICAL APPLICATIONS (Cont'd)

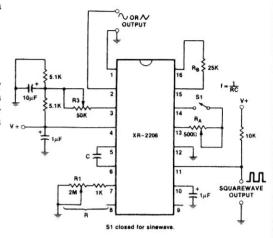


Figure 11—Circuit for Sinewave General With Minimum Harmonic Distortion (R3 Determines Output Swing—See Fig. 2)

OUTPUT CHARACTERISTICS

Output Amplitude

Maximum output amplitude is directly proportional to external resistor R_3 connected to pin 3 (See Fig. 2). For sinewave output, amplitude is approximately 60 mV peak per $K\Omega$ of R_3 . For triangle, the peak amplitude is approximately 160 mV peak per $K\Omega$ of R_3 . Thus, for example, R_3 = 50 $K\Omega$ would produce approximately $\pm 3V$ sinusoidal output amplitude.

Amplitude Modulation

Output amplitude can be modulated by applying a dc bias and a modulating signal to pin 1. The internal impedance at pin 1 is approximately 100 k Ω . Output amplitude varies linearly with the applied voltage at pin 1, for values of dc bias at this pin, within ± 4 volts of V⁺/2, as shown in Fig. 5. As this bias level approaches V⁺/2, the phase of the output signal is reversed; and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

NOTE: AM control must be used in conjunction with a well-regulated supply since the output amplitude now becomes a function of V⁺.

FREQUENCY-SHIFT KEYING

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2 , connected to the timing pins 7 and 8, respectively, as shown in Figure 12. Depending on the polarity of the logic signal at pin 9, either one or the other of these timing resistors is activated. If pin 9 is open-circuited or connected to a bias voltage $\geq 2V$, only R_1 is active. Similarly, if the voltage level at pin 9 is $\leq 1V$, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2 as:

$$f_1 = 1/R_1C$$
 and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at pin 9 is referenced to V-.

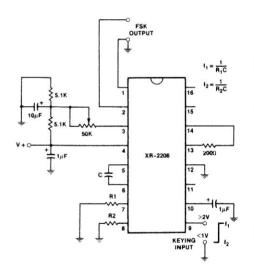


Figure 12-Sinusoidal FSK Generator

XR-2206 276-2336

OUTPUT DC LEVEL CONTROL

The dc level at the output (pin 2) is approximately the same as the dc bias at pin 3. In figures 10, 11 and 12, pin 3 is biased mid-way between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

SINEWAVE GENERATION

A) Without External Adjustment

Figure 10 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer R_1 at pin 7 provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$ and the typical distortion (THD) is < 2.5%. If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 10 can be converted to split supply operation simply by replacing all ground connections with V^- . For split supply operation, R_3 can be directly connected to ground.

B) With External Adjustment

The harmonic content of sinusoidal output can be reduced to $\approx 0.5\%$ by additional adjustments as shown in Figure 11. The potentiometer R_A adjusts the sine-shaping resistor; and R_B provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

- 1. Set R_B at mid-point and adjust R_A for minimum distortion.
- 2. With RA set as above, adjust RB to further reduce distortion.

TRIANGLE WAVE GENERATION

The circuits of Figures 10 and 11 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sinewave output.

FSK GENERATION

Figure 12 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors R_1 and R_2 ; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^- .

PULSE AND RAMP GENERATION

Figure 13 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2 . The values of R_1 and R_2 sould be in the range of 1 K Ω to 2 M Ω .

TYPICAL APPLICATIONS (Cont'd)

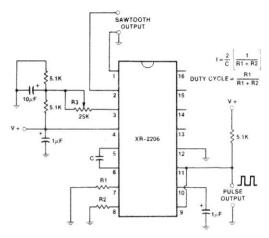


Figure 13—Circuit for Pulse and Ramp Generation



FSK DEMODULATOR/TONE DECODER



GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band. It also has a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

FEATURES

- Wide Frequency Range (0.01 Hz To 300 kHz)
- Wide Supply Voltage Range (4.5 V To 20 V)
- DTL/TTL/ECL Logic Compatibility
- FSK Demodulation, with Carrier-Detection
- Wide Dynamic Range (2 mV To 3 Vrms)
- Adjustable Tracking Range (±1% To ±80%)
- Excellent Temp. Stability (20ppm/°C, typ.)

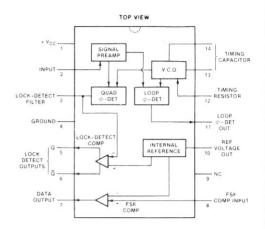
APPLICATIONS

- · FSK Demodulation
- · Data Synchronization
- · Tone Decoding
- · FM Detection
- Carrier Detection

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V
Supply current ($R_0 \ge 10 \text{ K}\Omega$ See Figure 4)	A
Input Signal Level	IS
Power Dissipation	V
Operating Temperature Range 0 °C To 75 °C	C

PIN CONNECTION



BLOCK DIAGRAMS

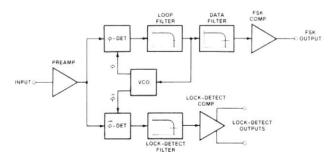


Figure 1—Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

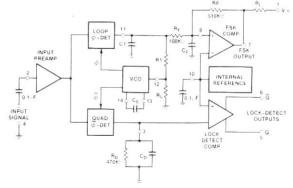
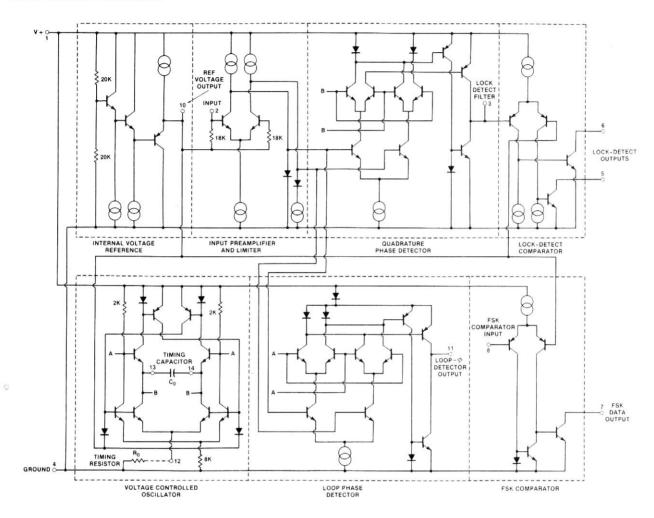


Figure 2—Generalized Circuit Connection for FSK and Tone Detection

INTERNAL CIRCUIT



TYPICAL CHARACTERISTICS

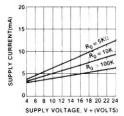


Figure 4—Typical Supply Current vs V + (Logic Outputs Open Circuited)

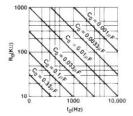


Figure 5—VCO Frequency vs Timing Resistor

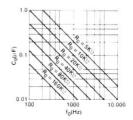


Figure 6—VCO Frequency vs Timing Capacitor

TYPICAL CHARACTERISTICS (Cont'd)

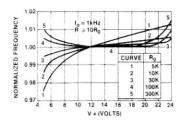


Figure 7—Typical f₀ vs Power Supply Characteristics

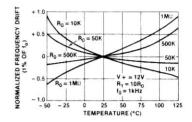


Figure 8—Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2)

Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 $k\Omega.$ Recommended input signal level is in the range of 10 mVrms to 3 Vrms.

Quadrature Phase Detector Output (Pin 3)

This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (See Fig. 2) to eliminate the chatter at lock-detect outputs. If the tone-detect section is not used, Pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5)

The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor, R_L , to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

Lock-Detect Complement, Q (Pin 6)

The output at Pin 6 is the logic complement of the lock-detect output at Pin 5. This output is also an open-collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7)

This output is an open-collector logic stage which requires a pull-up resistor, $R_{\rm L}$, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency; and at "low" or on state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8)

This is the high-impedance input to the FSK voltage comparator. Normally, and FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (Pin 11). This data filter is formed by $R_{\rm F}$ and $C_{\rm F}$ of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, $V_{\rm R}$, available at Pin 10.

Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R : $V_R = V + /2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

Loop Phase Detector Output (Pin 11)

This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (See Fig. 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 11 is very nearly equal to $V_R.$ The peak voltage swing available at the phase detector output is equal to $\pm V_R.$

VCO Control Input (Pin 12)

VCO free-running frequency is determined by external timing resistor, $R_{\rm O}$, connected from this terminal to ground. The VCO free-running frequency, $f_{\rm O}$, is:

$$f_{\rm O} = \frac{1}{R_{\rm O}C_{\rm O}}\,{\rm Hz}$$

where C_O is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_O must be in the range of 10 K Ω to 100 K Ω (See Fig. 8).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R . The maximum timing current drawn from Pin 12 must be limited to ≤ 3 mA for proper operating of the circuit.

VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C_O , connected across these terminals (See Fig. 5). C_O must be non-polar, and in the range of 200 pF to 10 μ F.

VCO Frequency Adjustment

VCO can be fine-tuned by connecting a potentiometer, $R_{\rm X}$, in series with $R_{\rm O}$ at Pin 12 (See Fig. 9).

VCO Free-Running Frequency, fo

XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with C_D disconnected), with no input and with Pin 2 shorted to Pin 10.

APPLICATIONS INFORMATION

FSK DECODING

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: $R_{\rm O}$ and $C_{\rm O}$ set the PLL center frequency, $R_{\rm 1}$ sets the system bandwidth, and $C_{\rm 1}$ sets the loop filter time constant and the loop damping factor. $C_{\rm F}$ and $R_{\rm F}$ form a one-pole post-detection filter for the FSK data output. The resistor $R_{\rm B}$ (= 510 K Ω) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table I.

ADJUSTMENT PROCEDURE

With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that $f_{\rm O}$ can be monitored:

- 1. Short pin 2 to pin 10 and measure fo at pin 3 with CD disconnected;
- 2. Open R₁ and monitor pin 13 or 14 with a high-impedance probe; or
- Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

NOTE: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

TYPICAL APPLICATIONS

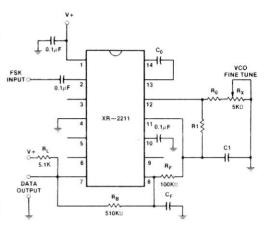


Figure 9—Circuit Connection for FSK Decoding

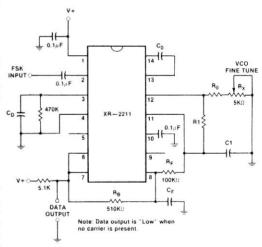


Figure 10—External Connectors for ESK Demodulation with Carrier-Detect Capability

TABLE I

FSK BAND	COMPONENT	VALUES
300 Baud $f_1 = 1070 \text{ Hz}$ $f_2 = 1270 \text{ Hz}$	$C_{\rm O} = 0.039 \mu{\rm F}$ $C_{\rm 1} = 0.01 \mu{\rm F}$ $R_{\rm 1} = 100 {\rm K}\Omega$	$C_F = 0.005 \mu\text{F}$ $R_O = 18 \text{K}\Omega$
300 Baud $f_1 = 2025 \text{ Hz}$ $f_1 = 2225 \text{ Hz}$	$C_{\rm O} = 0.022 \mu{\rm F}$ $C_{\rm 1} = 0.0047 \mu{\rm F}$ $R_{\rm 1} = 200 {\rm K}\Omega$	$C_F = 0.005 \mu\text{F}$ $R_O = 18 \text{K}\Omega$
1200 Baud $f_1 = 1200 \text{ Hz}$ $f_2 = 2200 \text{ Hz}$	$C_{\rm O} = 0.027 \ \mu { m F}$ $C_{\rm I} = 0.01 \ \mu { m F}$ $R_{\rm I} = 30 \ { m K}\Omega$	$C_F = 0.0022 \mu F$ $R_O = 18 K\Omega$

Recommended Component Values for Commonly Used FSK Bands (See Circuit of Fig. 9).

FSK DECODING WITH CARRIER-DETECT

The lock-detect section of XR-2211 can be used as a carrier-detect option, for FSK decoding. The recommended circuit connection for this application is shown in Fig. 10. The open-collector lock-detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PPL, and the pin 6 output goes "high", to enable the data output.

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $+\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1 .For most applications, $\Delta f_c > \Delta f/2$. For $R_D = 470~K\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \ge 16/\text{capture range in Hz}.$$

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of C_D will slow the response time of the lock-detect output.

TONE DETECTION

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and \overline{Q} at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} , as shown in Fig. 11.

With reference to Figs. 2 and 11, the functions of the external circuit components can be explained as follows: R_O and C_O set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and \overline{Q} logic outputs.

LINEAR FM DETECTION

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Fig. 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of $R_{\rm F}$ and $C_{\rm F}$, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Fig. 12.

TYPICAL APPLICATION (Cont'd)

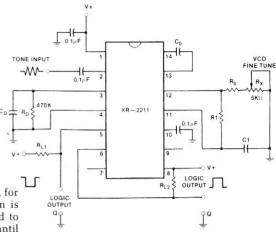


Figure 11—Circuit Connection for Tone Detection

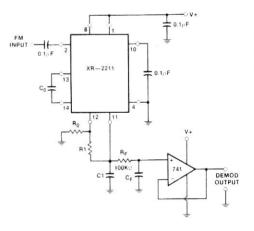


Figure 12—Linear FM Detector Using XR—2211 and an External Op. Amp.



QUAD COMPARATOR

276-1712

GENERAL DESCRIPTION

The 339 series consists of four independent voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

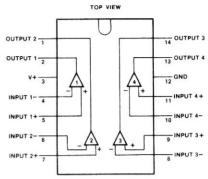
FEATURES

- Wide single supply:
- Voltage range 2 V_{DC} to 32 V_{DC} or dual supplies ± 1 V_{DC} to ± 16 V_{DC} Very low supply current drain (0.8 mA)—independent of supply voltage (1 mW/comparator at +5 V_{DC})
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5 µA: saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL (fanout of 2). DTL. ECL. MOS and CMOS logic systems

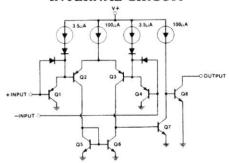
ABSOLUTE MAXIMUM RATINGS

Supply Voltage. V+
Differential Input Voltage
Input Voltage0.3 V _{DC} to +36 V _{DC}
Power Dissipation
Molded DIP 570 mW
Cavity DIP
Output Short-Circuit to GND
Input Current (V _{IN} < -0.3 V _{DC})
Operating Temperature Range 0 to +70°C
Storage Temperature Range65 to +150°C
Lead Temperature (Soldering, 10 seconds)

PIN CONNECTION

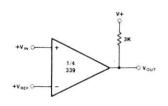


INTERNAL CIRCUIT

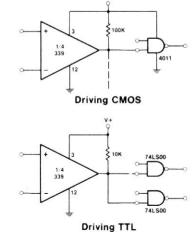


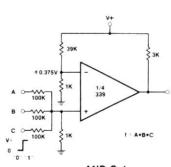
TYPICAL APPLICATIONS

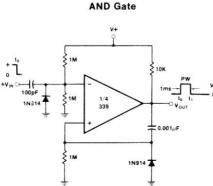
5 VOLT GROUP



Basic Comparator

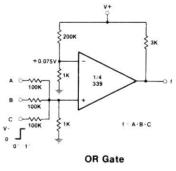


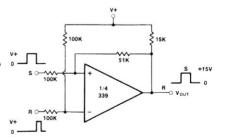




One-Shot Multivibrator

15V GROUP





Bi-Stable Multivibrator

565 276-1720

PHASE LOCKED LOOP



PIN CONNECTION

TOP VIEW

GENERAL DESCRIPTION

The 565 phase-locked loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- Highly stable center frequency (200ppm/°C typ.)
- Wide operating voltage range (±6 to ±12 volts)
- Highly linear demodulated output (0.2% typ.)
- Center frequency programming by means of a resistor or capacitor, voltage or
- TTL and LS compatible square-wave output; loop can be opened to insert digital frequency divider.
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from < ±1% to > ±60%
- Frequency adjustable over 10 to 1 range with same capacitor

APPLICATIONS

- · Frequency shift keying
- Modems
- Telemetry receivers
- Tone decoders
- SCA receivers

- · Wideband FM discriminators
- Data synchronizers
- · Tracking filters
- Signal restoration

• Frequency multiplication & division

VCO OUTPUT -

REFERENCE OUTPUT 6

PHASE COMPARATOR VCO INPUT

DEMODULATED

INDIIT

(FREQUENCY MODULATED SIGNAL)	OUTPUT C	Î	6 v	
<u>=</u> 600⊞ 2	4 5	9	10	
	565		R3	S R _O
10µF	6 7 0.001 15K 15K 10.05μF	9.09K 47	499K	7,5K J 10µF 499K 7 108 4 30pF
				(V ₇ -V ₈) DEMODULATED OUTPUT

Test Circuit

TEST CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Maximum operating voltage	V
Input voltage	p
Power dissipation300mV	٧
Operating temperature range 0 to +70°	C
Storage temperature65 to +150°	C

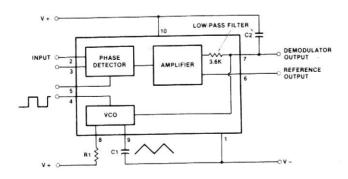
DESIGN FORMULAS (See Figure 1, Page 100)

Free-running frequency of VCO: $f_0 = \frac{1.2}{4R1C1}$ in Hz

$$\begin{aligned} & \text{Lock-range } f_L = \pm \frac{8 f_o}{V_{CC}} \; \; \text{in Hz} \\ & \text{Capture-range: } f_C \; \cong \; \pm \; \frac{1}{2\pi} \sqrt{\frac{2 \, \pi \, f_L}{\tau}} \end{aligned}$$

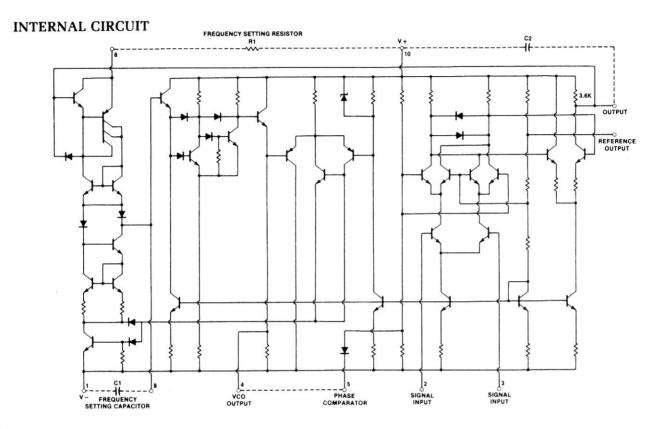
where $\tau = (3.6 \text{ X} 10^3) \text{ X} \text{ C}_2$

BLOCK DIAGRAM

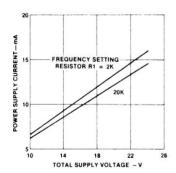




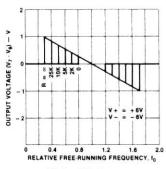
565 276-1720



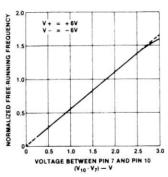
TYPICAL CHARACTERISTICS



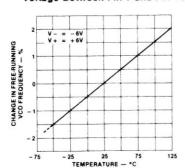
Power Supply Current vs Total Supply Voltage



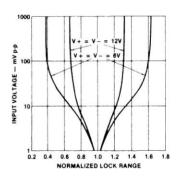
Output Voltage vs Relative Free Running Frequency



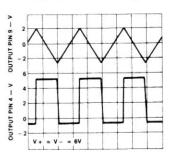
Normalized Free Running Frequency vs Voltage Between Pin 7 and Pin 10



Change in Free-Running VCO Frequency vs Temperature



Input Voltage vs Normalized Lock Range



VCO Output Waveform

565 276-1720

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide brandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_o = \frac{1.2}{4R1C1}$$

and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20.000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from $\pm 60\%$ of $f_{\rm o}$ to approximately $\pm 20\%$ of $f_{\rm o}$ (at $\pm 6V$).

A small capacitor (typically 0.001 μ F) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the 565 Phase Locked Loop without the use of any resonant circuits.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer, only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

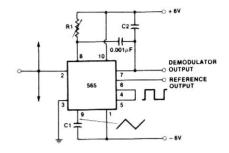


Figure 1 - FM Demodulation

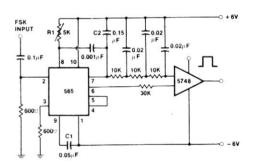


Figure 2 - Frequency Shift Keying (FSK)

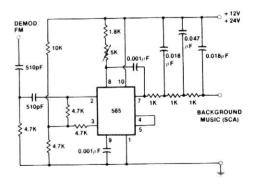


Figure 3 - SCA Decoder



TONE DECODER

567 276-1721

GENERAL DESCRIPTION

The 567 is a general purpose tone decoder designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

FEATURES

- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

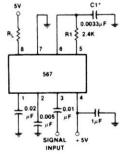
APPLICATIONS

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

ABSOLUTE MAXIMUM RATINGS

Supply Voltage9V
Power Dissipation
V ₈ (Output Voltage)
V ₃ (-Voltage at Input)10V
V_3 (+Voltage at Input) V_8 +0.5V
Operating Temperature 0 to +70°C
Storage Temperature Range65 to +150°C

TYPICAL APPLICATIONS



ncy of the VCO. This is given by $f_0 \equiv 1/R1C1$ The band width of the filter may

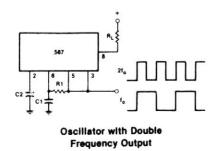
 V_{IN} = Input voltage (volts rms), $V_{IN} \le 200 \text{mV}$.

C2 = Capacitance at pin 2 in μ F.

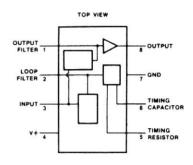
Adjust for to = 100kHz

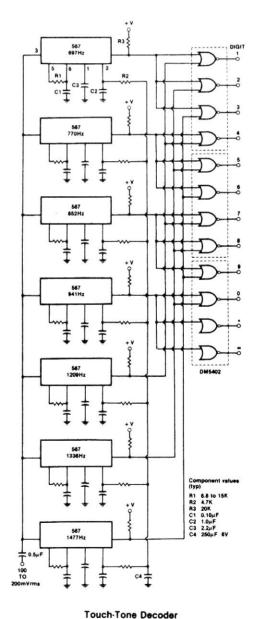
f; = 100kHz +5V

AC Test Circuit



PIN CONNECTION





3909 276-1705

LED FLASHER/OSCILLATOR



GENERAL DESCRIPTION

The 3909 is a monolithic oscillator specifically designed to flash light emitting diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as a LED flasher.

It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example -20% to +100%.

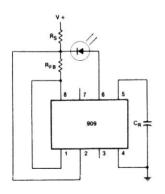
FEATURES

- Operation over one year from one C size flashlight cell
- · Bright, high current LED pulse
- · Minimum external parts
- Low voltage operation. from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful: as an oscillator directly drives an 8Ω speaker

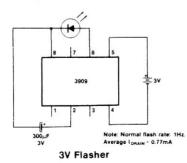
ABSOLUTE MAXIMUM RATINGS

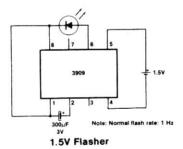
nW
4V
ms
nΑ
nΑ
Hz
Hz
0°C

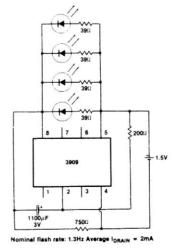
TYPICAL APPLICATIONS



Warning Flasher High Voltage Powered

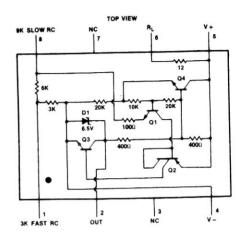




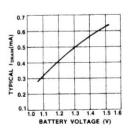


Parallel LED's

PIN CONNECTION



TYPICAL CHARACTERISTICS



Drain Current vs Battery Voltage

ESTIMATED BATTERY LIFE (CONTINUOUS 1.5V FLASHER OPERATION)

	TYPE		
SIZE CELL	STANDARD	ALKALINE	
AA	3 MONTHS	6 MONTHS	
С	7 MONTHS	15 MONTHS	
D	1.3 YEARS	2.6 YEARS	

Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended tor any application of the months or more. Nickel Cadmium cells are not recommended

TYPICAL OPERATING CONDITIONS

٧+	NORMAL FLASH Hz	$C_{\mathtt{T}}$	R _s 1W	RFB	V+RANGE
6V	2	400µF	1K	1.5K	5-25V
15V	2	180µF	3.9K	1K	13-50V
100V	1.7	180µF	43K	1K	85-200V



TUNES SYNTHESIZER

AY-3-1350 276-1782

GENERAL DESCRIPTION

The AY-3-1350 is an N-channel MOS microcomputer based synthesizer of pre-programmed tunes for applications in toys, musical boxes, and doorchimes. The standard device has a set of 25 different popular and classical tunes chosen for their international acceptance. In addition there are 3 chimes making a total of 28 tunes.

The chip is mask-programmable during manufacture enabling the quantity user to select his own music. Up to 28 tunes of varying length can be chosen.

The device has multi-mode operation making it suitable for a wide variety of applications.

FEATURES

- 25 different tunes plus 3 chimes
- Mask programmable with customer specified tunes for toys, musical boxes, etc.
- Minimal external components
- Automatic switch-off signal at end of tune for power savings
- Envelope control to give organ or piano quality
- Sequential tune mode
- 4 door capability when used as doorchime
- Operation with tunes in external PROM if required
- Single supply (+5V) operation

TUNES

The standard AY-3-1350 contains the following tunes:

A0	Toreador	A3	U Sole Mio
Bo	William Tell	B3	Santa Lucia
Co	Hallelujah Chorus	C3	The End
D ₀	Star Spangled Banner	D3	Blue Danube
E0	Yankee Doodle	E3	Brahms' Lullaby
A1	John Brown's Body	A4	Hell's Bells
B1	Clementine	B4	Jingle Bells
C1	God Save the Queen	C4	La Vie en Rose
D1	Colonel Bogey	D4	Star Wars
E1	Marseillaise	E4	Beethoven's 9th
A2	America, America		
B2	Deutschland Leid		
C2	Wedding March	Chi	me X Westminster Chime
D ₂	Beethoven's 5th	Chime Y Simple Chime	
E2	Augustine	Chi	me Z Descending Octave Chime

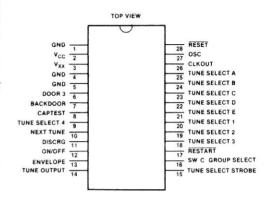
ABSOLUTE MAXIMUM RATINGS

Primary Supply Voltage, V _{DD} 7V
Output Buffer Supply Voltage, VXX9V
Primary Supply Current (No Load), IDO55mA
Output Buffer Supply Current (No Load), IXX5mA
Logic Input Low Voltage, V _{IL}
Logic Input High Voltage (Note 2), V _{IH1} V _{DD} V
(Except RESET and OSC when driven externally)
Logic Input High Voltage, V _{IH2} V _{DD} V
(RESET and OSC)
Logic Output High Voltage (Note 2), $V_{OH}(I_{OH} = 100\mu A)$
Logic Output Low Voltage, V_{OL} ($I_{OL} = 1.6\mu A$, $V_{XX} = 4.5V$)
$(I_{OL} = 5mA, V_{XX} = 9V) \dots 0.90V$
$(I_{OL} = 5mA, V_{XX} = 9V) \dots 0.50V$
$(I_{OL} = 10 \text{mA}, V_{XX} = 9 \text{V}) \text{ (Note 1)}$
Operating Temperature 0 to 70°C

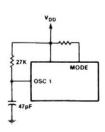
Notes: 1. Total I_{OL} for all registers must be less than 150mA under any conditions.

2. Except following pins which have open drain outputs/inputs: 6, 7, 8, 12 and 13.

PIN CONNECTION



TEST CIRCUIT



Test Circuit

AY-3-1350 276-1782

TYPICAL APPLICATIONS

Implementation

There are many ways to connect the standard device depending on the exact application. Figure 1 shows just one implementation of the device in a doorchime. This circuit gives access to all 25 tunes from switch A and one of 5 tunes from switch C as well as the descending active chime from switch B. The tune selected for switch B follows the tunes list according to the setting of the two, tune select switches (A-E and 0-4). The tune selected from switch C in Figure 1 is one of the five tunes A0 through E0 depending on the setting of the letter switch. For example, with the letter switch set at E and the number switch set at 4, the tunes available will be:

Switch A: Beethoven's 9th (E4) Switch C: Yankee Doodle (EO)

Switch B: Descending Octave Chime (Chime Z)

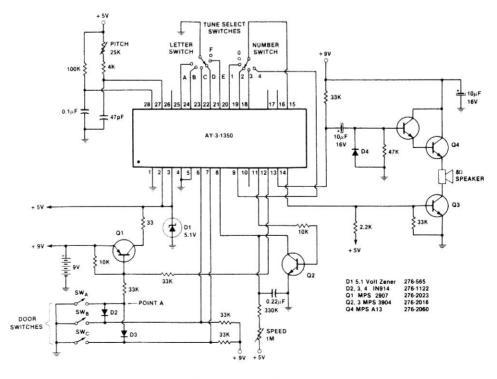
When the letter switch is in position F there will be chimes on all doors independent of the number switch setting as follows:

Switch A: Westminster Chime Switch C: Simple Chime

Switch B: Descending Octave Chime

There is virtually no power consumption in the standby condition (external transistor leakages only). When any door switch is activated the circuit powers up, plays a tune, and then automatically powers down again to conserve the battery, even if the operator keeps his finger on the switch to the end of the tune. He must release it and re-press to play again with the circuit in Figure 1. Activating any of the door switches will pull point A to ground turning on the PNP transistor in the power supply line. This causes +5V to be applied to the AY-3-1350 and the first operation of the chip is to put ON/OFF (pin 12) to logic 0. This maintains the power through the PNP, even after the switch is released. The device can turn off its own power at the end of a tune by raising ON/OFF to logic 1.

Figure 1 shows only a typical one-chip implementation. Further options come from use of different switching and/or from use of the next tune facilities built into the chip. These will now be considered in turn.



AY-3-1350 276-1782

TYPICAL APPLICATIONS (Cont'd)

Switching Options

In Figure 1 the Switch C Group Select pin (16) is not connected, and one of the five tunes (A0 through E0) will play if switch C is activated. Other number groups can be chosen by connecting the Switch C Group Select pin as follows:

Switch C Group Select pin (16) is connected to:	Switch C Tunes
no other pin	A0-E0
Tune Select 1 (pin 20)	A1-E1
Tune Select 2 (pin 19)	A2-E2
Tune Select 3 (pin 18)	A3-E3
Tune Select 4 (pin 9)	A4-E4

Which of the five possible switch C tunes will be played depends on the current setting of the LETTER SWITCH A-E.

Switch C selection can be made by hard-wire connection for a permanent selection or a third switch can be added for an additional group selection feature.

LED Direct Drive

 V_{XX} drives the gate of the output buffer, allowing adjustment of drive capability:

V _{xx}	V _{OUT}	I _{SINK} (typ.)
5V	0.4V	2.5mA
5V	0.7V	4.2mA
10V	0.4V	5.8mA
10V	0.7V	10.0mA
10V	1.0V	14.1mA

Using the power-up circuit of Figure 1, the AY-3-1350 will have +5V applied and be latched within a few microseconds (dependant upon external components) from any bell-push closing. The device starts to operate when the RESET pin reaches logic 1 (about 10ms with components shown) but in fact the tune select switches are not interrogated until approximately 6 ms later. The total is sufficient for most bell-pushes to complete any bounce period and for a firm selection of tunes to be made.

Next Tune Facilities

At the end of tune play the circuit of Figure 1 powers down because ON/OFF (pin 12) is raised to a logic 1. This simplified flow diagram in Figure 3 shows that before the power down there is a test for connection between NEXT TUNE (pin 10) then RESTART (pin 17) with TUNESELECT 4 (pin 9). At this time NEXT TUNE (pin 10) then RESTART (pin 17), which is normally at logic 1, output a logic 0. This is looked for at input TUNESELECT 4 (pin 9). If neither is found the power down system is reached as in Figure 1.

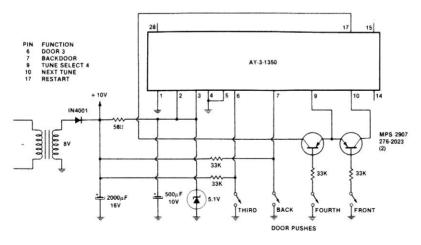


Figure 2

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TYPICAL APPLICATIONS (Cont'd)

A NEXT TUNE (pin 10)—TUNE SELECT 4 (pin 9) connection at the moment of test causes the next tune in the list to be played after a short pause (equal to a musical breve—the actual time depends on the setting of the tune speed control). The order of the tunes is A0 to E4 as given in the listing of standard AY-3-1350 tunes. If the last tune (E4) was played then the circuit will go on to play the first tune A0 (and then successive ones). The chimes are not included in the cycling sequence.

A RESTART (pin 17)—TUNESELECT 4 (pin 9) connection at the moment of test at the end of a tune causes the same selected tune to be played again. Figure 3 shows that in this case the tune sensing mechanism is passed through once more so the tune would be different the second time if the switches were altered while the first tune was playing.

The connections referred to cannot be permanent because otherwise the circuit would never stop playing tunes. Figure 2 shows how transistors are used to make the connection in a practical application.

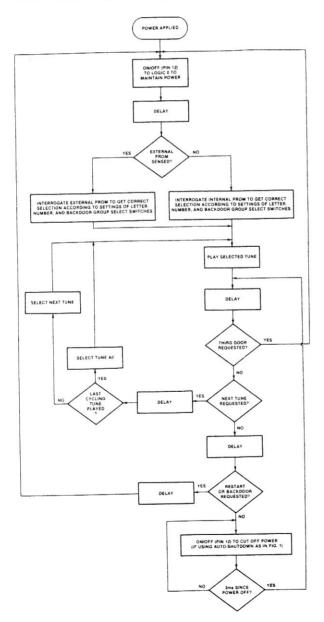


Figure 3—Flow Diagram



SPEECH PROCESSOR

SP0256 276-1784

GENERAL DESCRIPTION

The SPO256 (Speech Processor) is a single chip N-Channel MOS LSI device that is able, using its stored program to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5KHz, a dynamic range of 42dB, and a signal to noise ratio of approximately 35 dB.

The SPO256 incorporates four basic functions:

- A. A software programable digital filter that can be made to model a VOCAL TRACT.
- B. A 16K ROM which stores both data and instructions (THE PROGRAM).
- C. A MICROCONTROLLER which controls the data flow from the ROM to the digital filter, the assembly of the "word settings" necessary for linking speech elements together, and the amplitude and pitch information to excite the digital filter.
- D. A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

FEATURES

- · Natural Speech
- Wide Operating Voltage
- Simple Interface to Most Microcomputers or Microprocessors
- Supports L.P.C. Synthesis: Formant Synthesis: Allophone Synthesis

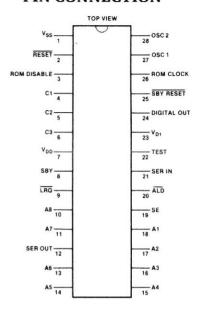
ABSOLUTE MAXIMUM RATINGS

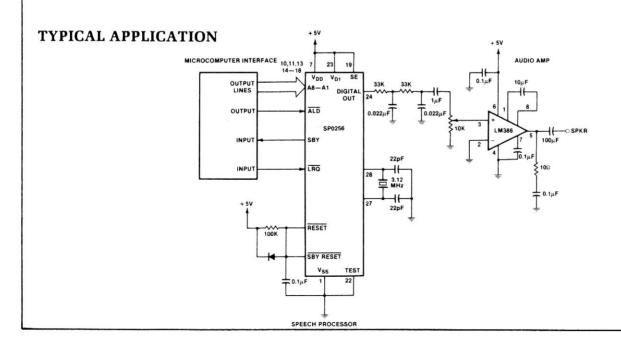
Supply Voltage (V $_{DD}$)
(V_{D1}) 7 V
All Pins With Respect to V_{SS})
Supply Current (I_{DD}) $(V_{D1}, V_{DD} = 7V)$
(Reset and SBY Reset High) 90 mA
Supply Current (I_{D1} (V_{D1} , V_{DD} =7V)
(Reset and SBY Reset High) 21 mA
Storage Temperature Range25°C To 125°C
Operating Temperature Range 0 °C To 70 °C

STANDARD CONDITIONS

Clock-Crystal Frequency 3.120 MHz

PIN CONNECTION





ALLOPHONE USAGE WITH A MICROPROCESSOR

The SPO256 requires the use of a processor to concatenate the speech sounds to form words.

The SPO256 is controlled using the address pins (A1-A8), ALD (Address Load), and SE (Strobe Enable). The object for controlling the chip is to load an address into it which contains the desired allophone. The speech data for the allophone set is contained within the internal 16 K ROM of the SPO256.

This particular application (Allophone Set) requires only six address pins (A1-A6) to address all the 59 allophones plus five pauses, a total of 64 locations. For simplicity, since only six address pins are needed to address the 64 locations, pins A7 and A8 can be tied low (to ground) and now any further references to the address bus will include A1-A6 and A7=A8=0.

There are two modes available for loading an address into the chip. SE (Strobe Enable) controls the mode that will be used.

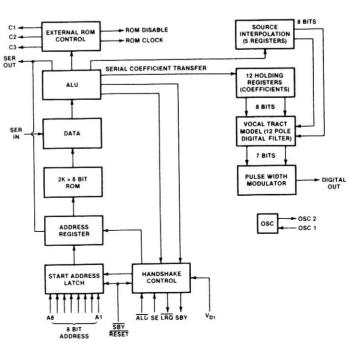
Mode 0. (SE=0) will latch in an address when any one or more of the address pins makes a low to high transition. For example, to load the address one (1), A2 to A6=0 and A1 is pulsed high. To load the address twelve (12 octal), A1=A3=A5=A6=0, A2 and A4 are pulsed high simultaneously. (Note that an address of zero cannot be loaded using this mode).

Mode 1 (SE=1) will latch in an address using the ALD pin. First, setup the desired address on the address bus (A1=A6) and then pulse ALD low. Any address can be loaded using this mode, but certain setup and hold times are required.

Two microprocessor interface pins are available for quick loading of addresses. They are LRQ and SBY LRQ (Load Request) tells the processor when the input buffer is full. SBY (Stand By) tells the processor that the chip has stopped talking and no new address has been loaded. Either interface pin can be used when concatenating allophones. LRQ is an active low signal, when LRQ goes low it is time to load a new address to the chip. If LRQ is high, then simply wait for it to go low before loading the address. SBY will stay high until an address is loaded, then it will go low and stay low until all the internal instructions (Speech Code) from that one address are completed. Once this signal goes high, it is time to load a new address. Since speech does not require very fast address loading, it would be acceptable to use SBY to interface to the processor.

To end a word using allophones it is necessary to load a pause to complete the word. For example, the word "TWO" can be implemented using the following allophones, TT2-VW2-PA1. PA1 is actually not an allophone but a pause which is needed to end the word.

BLOCK DIAGRAM



ALLOPHONE BASED SPEECH PROCESSOR—SP0256-AL2

PIN FUNCTIONS

PIN NUMBER	NAME	FUNCTION
1	V_{SS}	Ground
2	RESET	A logic 0 resets that portion of the SP powered by V_{DD} . Must be returned to a logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM, a logic 1 disables the external ROM.
4, 5, 6	C1, C2, C3	Output control lines for use with an external serial speech ROM.
7	V_{DD}	Power supply for all portions of the SP except the microprocessor interface logic.
8	SBY	STANDBY. A logic 1 output indicates that the SP is inactive and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9	ĪRQ	LOAD REQUEST. LRQ is a logic 1 output whenever the input buffer is full. When LRQ goes to a logic 0, the input port may be loaded by placing the 8 address bits on A1-A8 and pulsing the ALD output.
10, 11, 13, 14, 15, 16, 17, 18,	A8, A7, A6, A5, A4, A3, A2, A1	8 bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, $\overline{\text{ALD}}$ is disabled and the SP will automatically latch in the address on the input bus approximately $1\mu\text{s}$ after detecting a logic 1 on any address line.
20	ALD	ADDRESS LOAD. A negative pulse on this input loads the 8 address bits into the input port. The negative edge of this pulse causes LRQ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22	TEST	This pin should be grounded for normal operation.
23	VD1	Power supply for the microprocessor interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5KHz low pass filter and amplified, will drive a loudspeaker.
25	SBY RESET	STANDBY RESET. A logic 0 resets the microprocessor interface logic and the address latches. Must be returned to a logic 1 for normal operation.
26	ROM CLOCK	This is a 1.56MHz clock output used to drive an external serial speech ROM.
27	OSC1	XTAL IN. Input connection for a 3.12MHz crystal.
28	OSC2	XTAL OUT. Output connection for a 3.12MHz crystal

ALLOPHONE SPEECH SYNTHESIS

INTRODUCTION

The allophone speech synthesis technique provides the user with the ability to synthesize an unlimited vocabulary at a very low bit rate. Fifty-nine discrete speech sounds (called allophones) and five pauses are stored at different addresses in the SPO256 internal ROM. Each speech sound was excised from a word and analyzed using linear predictive coding (LPC). Any English word or phrase can be created by addressing the appropriate combination of allophones and pauses. Since there is a total of 64 address locations each requires a 6 bit address. Assuming that speech contains 10 to 12 sounds per second, allophone synthesis requires addressing less than 100 bits per second.

LINGUISTICS

A few basic linguistic concepts will help you start your own library of "allophone words". (See Table 1 for Allophone Dictionary). First, there is no one-to-one correspondence between written letters and speech sounds; secondly, speech sounds are acoustically different depending upon their position within

LINGUISTICS (Continued)

a word; and lastly, the human ear may perceive the same acoustic signal differently in the context of different sounds.

The first point compares to the problem that a child encounters when learning to read. Each sound in a language may be represented by more than one letter and, conversely each letter may represent more than one sound. (See the examples in Table 2.) Because of these spelling irregularities, it is necessary to think in terms of sounds, not letters, when using allophones.

The second, and equally important, point to understand, is that the acoustic signal of a speech sound may differ depending upon its position within a word. For example, the initial K sound in coop will be acoustically different from the K's in keep and speak. The K's in coop and keep differ due to the influence of the vowels which follow them, and the final K in speak is usually not as loud as initial K's.

Finally, a listener may identify the same acoustic signal differently depending on the context in which it is perceived. Don't be surprised, therefore, if an allophone word sounds slightly different when used in various phrases.

PHONEMES OF ENGLISH

The sounds of a language are called phonemes, and each language has a set which is slightly different from that of other languages. Table 3 contains a chart of all the consonant phonemes of English, table 4 all the vowel phonemes.

Consonants are produced by creating an occlusion or constriction in the vocal tract which produces an aperiodic sound source. If the vocal cords are vibrating at the same time, as in the case of the voiced fricatives VV, DH, ZZ, and ZH, (See Table 5) there are two sound sources: one which is aperiodic and one which is periodic.

Vowels are usually produced with a relatively open vocal tract and a periodic sound source provided by the vibrating vocal cords. They are classified according to whether the front or back of the tongue is high or low (See Table 4) whether they are long or short, and whether the lips are rounded or unrounded. In English all rounded vowels are produced in or near the back of the mouth (UW, UH, OW, AO, OR, AW).

Speech sounds which have features in common behave in similar ways. For example, the voiceless stop consonants PP, TT and KK (See Table 3) should be preceded by 50-80 msec of silence, and the voiced stop consonants BB, DD, and GG by 10-30 msec of silence.

ALLOPHONES

Phoneme is the name given to a group of similar sounds in a language. Recall that a phoneme is acoustically different depending upon its position within a word. Each of these positional variants is an allophone of the same phoneme. An allophone, therefore, is the manifestation of a phoneme in the speech signal. It is for this reason that our inventory of English speech sounds is called an allophone set.

HOW TO USE THE ALLOPHONE SET

(See Table 1 for instructions on how to create all the sample words mentioned in this section.) The allophone set (Refer to Table 5) contains two or three versions of some phonemes. It may be necessary to use one allophone of a particular phoneme for word-or-syllable-final position. A detailed set of guidelines for using the allophones is given in Table 5. Note that these are suggestions, not rules.

For example, DD2 sounds good in initial position and DD1 sounds good in final position, as a "daughter" and "collide". One of the differences between the initial and final versions of a consonant is that an initial version may be longer than the final version. Therefore, to create an initial SS, you can use two SSs instead of the usual single SS at the end of a word or syllable, as in "sister". Note that this can be done with TH and FF, and the inherently short vowels (to be discussed below), but with no other consonants. You will want to experiment with some consonants such as str, cl) to discover which versions works best in the cluster. For example, KK1 sounds good before LL as in "clown", and KK2 sounds good before WW as in "square". One allophone of a particular phoneme may sound better before or after back vowels and another

HOW TO USE THE ALLOPHONE SET (Continued)

before or after front vowels. KK3 sounds good before UH and KK1 sounds good before IY, as in "cookie". Some sounds (PP, BB, TT, DD, KK, GG, CH, and JH) require a brief duration of silence before them. For most of these, the silence has already been added but you may decide you want to add more. Therefore, there are several pauses included in the allophone set varying from 10-200 msec. To create the final sounds in the words "letter" and "little" use the allophone ER and EL.

Remember that you must always think about how a word sounds, not how it is spelled. For example, the NG sound is represented by the letter N in "uncle". And remember that some sounds may not even be represented in words by any letters, as the YY in "computer".

As mentioned earlier there are some vowels which can be doubled to make longer versions for stressed syllables. These are the inherently short vowels IH, EH, EA, EX, AA, and UH. For example, in the word "extent" use one EH in the first syllable, which is unstressed and two EHs in the second syllable which is stressed. Of the inherently long vowels there is one, UW, which has a long and shot version. The short one UW1, sounds good after YY in computer. The long version, UW2, sounds good in monosyllabic worlds like "two". Included in the vowel set is a group called R-colored vowels. These are vowel + R combinations. For example, the AR in "alarm" and the OR in "score". Of the R-colored vowels there is one, ER, which has a long and short version. The short version is good for polysyllabic words with final ER sounds like "letter", and the long versions is good for monosyllablic words like "fir". One final suggestion is that you may want to add a pause of 30-50 msec between words, when creating sentences, and a pause of 100-200 msec between clauses.

Note: Every utterance must be followed by a pause in order to make the chip stop talking the last allo-

TABLE 1: THE ALLOPHONE DICTIONARY

ZZ YR OW

NUMBERS

zero

one, won	WW SX ZX NN1
two, to, too	TT2 UW2
three	TH RR1 IY
four, for, fore	FF FF OR
five	FF FF AY VV
six	SS SS IH IH PA3 KK2 SS
seven	SS SS EH EH VV IH NN1
eight, ate	EY PA3 TT2
nine	NN1 AA AY NN1
ten	TT2 EH EH NN1
eleven	IH LL EH EH VV IH NN1
twelve	TT2 WH EH EH LL VV
thirteen	TH ER1 PA2 PA3 TT2 IY NN1
fourteen	FF OR PA2 PA3 TT2 IY NN1
fifteen	FF IH FF PA2 PA3 TT2 IY NN1
sixteen	SS SS IH PA3 KK2 SS PA2 PA3 TT2
	IY NN1
seventeen	SS SS EH VV TH NN1 PA2 PA3 TT2
	IY NN1
eighteen	EY PA2 PA3 TT2 IY NN1
nineteen	NN1 AY NN1 PA2 PA3 TT2 IY NN1
twenty	TT2 WH EH EH NN1 PA2 PA3 TT2
200	IY
thirty	TH ER2 PA2 PA3 TT2 IY
forty	FF OR PA3 TT2 IY
fifty	FF FF IH FF FF PA2 PA3 TT2 IY
sixty	SS SS IH PA3 KK2 SS PA2 PA3 TT2
	IY
seventy	SS SS EH VV IH NN1 PA2 PA3 TT2
	IY
eighty	EY PA3 TT2 IY
ninety	NN1 AY NN1 PA3 TT2 IY
hundred	HH2 AX AX NN1 PA2 DD2 RR2 IH

IH PA1 DD1

housand	TH AA AW ZZ TH PA1 PA1 NN1
	DD1
nillian	MAN III III I VVA AV NINIA

nillion MM IH IH LL YY1 AX NN1

DAY OF THE WEEK:

Sunday	SS SS AX AX NN1 PA2 DD2 EY
Monday	MM AX AX NN1 PA2 DD2 EY
Tuesday	TT2 UW2 ZZ PA2 DD2 EY
Wednesday	WW EH EH NN1 ZZ PA2 DD2 EY
Thursday	TH ER2 ZZ PA2 DD2 EY
Friday	FF RR2 AY PA2 DD2 EY
Saturday	SS SS AE PA3 TT2 PA2 DD2 EY

MONTHS:

January	JH AE AE NN1 YY2 XR IY
February	FF EH EH PA2 BR RR2 UW2 XR IY
March	MM AR PA3 CH
April	EY PA3 PP RR2 IH IH LL
May	MM EY
June	JH UW2 NN1
July	JH UW1 LL AY
August	AO AO PA2 GG2 AX SS PA3 TT1
September	SS SS EH PA3 PP PA3 TT2 EH EH
	PA1 BB2 ER1
October	AA PA2 KK2 PA3 TT2 OW PA1 BB2
	ER1
November	NN2 OW VV EH EH MM PA1 BB2
	ER1
December	DD2 IY SS SS EH EH MM PA1 BB2
	ER1

ALLOPHONE DICTIONARY (Continued)

The second secon	DICTIONARY (Continued)		
LETTERS:			
A	EY	emotional	IY MM OW SH AX NN1 AX EL
В	BB2 IY	engage	EH EH PA1 NN1 GG1 EY PA2 JH
С	SS SS IY	engagement	EH EH PA1 NN1 GG1 EY PA2 JH
D	DD2 IY		MM EH EH NN1 PA2 PA3 TT2
E	IY	engages	EH EH PA1 NN1 GG1 EY PA2 JH IH
F	EH EH FF FF	144	ZZ
G	JH IY	engaging	EH EH PA1 NN1 GG1 EY PA2 JH IH
Н	EY PA2 PA3 CH		NG
I	AA AY	enrage	EH NN1 RR1 EY PA2 JH
Ţ	JH EH EY	enraged	EH NN1 RR1 EY PA2 JH PA2 DD1
K	KK1 EH EY	enrages enraging	EH NN1 RR1 EY PA2 JH JH ZZ
L	EH EH EL	enraging	EH NN1 RR1 EY PA2 JH IH NG EH SS SS PA3 KK1 PA2 PA3 PP
M N	EH EH EM EH EH NN1	escape	EH SS SS PA3 KK1 PA2 PA3 PP PA2
O	OW	escaped	TT2
P	PP IY	escapes	EH SS SS PA3 KK1 PA2 PA3 PP SS
0	KK1 YY1 UW2	escaping	EH SS SS PA3 KK1 PA2 PA3 PP IH
Q R	AR		NG
S	EH EH SS SS	equal	IY PA2 PA3 KK3 WH AX EL
T	TT2 IY	equals	IH PA2 PA3 KK3 WH AX EL ZZ
U	YY1 UW2	error	EH XR OR
V	VV IY	extent	EH KK1 SS TT2 EH EH NN1 TT2
W	DD2 AX PA2 BB2 YY1 UW2	fir	FF ER2
X	EH EH PA3 KK2 SS SS	freeze	FF FF RR1 IY ZZ
Y	WW AY	freezer	FF FF RR1 IY ZZ ER1
Z	ZZ IY	freezers	FF FF RR1 IY ZZ ER1 ZZ
		freezing	FF FF RR1 IY ZZ IH NG
DICTIONARY		frozen	FF FF RR1 OW ZZ EH NN1
alarm	AX LL AR MM	gauge	GG1 EY PA2 JH
bathe	BB2 EH DH2	gauged	GG1 EY PA2 JH PA2 DD1
bather	BB2 EY DH2 ER1	gauges gauging	GG1 EY PA2 JH IH ZZ GG1 EY PA2 JH IH NG
bathing	BB2 EY DH2 IH NG	hello	HH EH LL AX OW
beer	BB2 YR	hour	AW ER1
bread	BB1 RR2 EH EH PA1 DD1	infinitive	IH NN1 FF FF IH IH NN1 IH PA2
by	BB2 AA AY		PA3 TT2 IH VV
calendar	KK1 AE AE LL EH NN1 PA2 DD2	intrigue	IH NN1 PA3 TT2 RR2 IY PA1 GG3
	ER1	intrigued	IH NN1 PA3 TT2 RR2 IY PA1 GG3
clock	KK1 LL AA AA PA3 KK2	0.0000000000000000000000000000000000000	PA2 DD1
clown	KK1 LL AW NN1	intrigues	IH NN1 PA3 TT2 RR2 IY PA1 GG3
check	CH EH EH PA3 KK2		ZZ
checked	CH EH EH PA3 KK2 PA2 TT2	intriguing	IH NN1 PA3 TT2 RR2 IY PA1 GG3
checker	CH EH EH PA3 KK1 ER1 CH EH EH PA3 KK1 ER1 ZZ		IH NG
checkers	CH EH EH PA3 KK1 IH NG	investigate	IH IH NN1 VV EH EH SS PA2 PA3
checking checks	CH EH EH PA3 KKI IN NG		TT2 IH PA1 GG1 EY PA2 TT2
cognitive	KK3 AA AA GG3 NN1 IH PA3 TT2	investigated	IH IH NN1 VV EH EH SS PA2 PA3
cognitive	IH VV		TT2 IH PA1 GG1 EY PA2 TT2 IH
collide	KK3 AX LL AY DD1	investigator	PA2 DD1 IH IH NN1 VV EH EH SS PA2 PA3
computer	KK1 AX MM PP1 YY1 UW1 TT2 ER	investigater	TT2 IH PA1 GG1 EY PA2 TT2 ER1
cookie	KK3 UH KK1 IY	investigaters	IH IH NN1 VV EH EH SS PA2 PA3
coop	KK3 UW2 PA3 PP	investigaters	TT2 IH PA1 GG1 EY PA2 TT2 ER1
correct	KK1 ER2 EH EH PA2 KK2 PA2 TT1		ZZ
corrected	KK1 ER2 EH EH PA2 KK2 PA2 TT2	investigates	IH IH NN1 VV EH EH SS PA2 PA3
	IH PA2 DD1		TT2 IH PA1 GG1 EY PA2 TT1 SS
correcting	KK1 ER2 EH EH PA2 KK2 PA2 TT2	investigating	EH EH NN1 VV EH EH SS PA2 PA3
	IH NG		TT2 IH PA1 GG1 EY PA2 TT2 IH NG
corrects	KK1 ER2 EH EH PA2 KK2 PA2 TT1	key	KK1 IY
	SS	legislate	LL EH EH PA2 JH JH SS SS LL EY
crown	KK1 RR2 AW NN1	2 8 2 66	PA2 PA3 TT2
date	DD2 EY PA3 TT2	legislated	LL EH EH PA2 JH JH SS SS LL EY
daughter	DD2 AO TT2 ER1	1	PA2 PA3 TT2 IH DD1
day	DD2 EH EY	legislates	LL EH EH PA2 JH JH SS SS LL EY
divided	DD2 IH VV AY PA2 DD2 IH PA2		PA2 PA3 TT1 SS
1	DD1		

ALLOPHONE DICTIONARY DICTIONARY (Continued)

legislating LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 TT 2 IH NG legislature LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 CH ER1 letter LL EH EH PA3 TT2 ER1 litter LL IH IH PA3 TT2 ER1 little LL IH IH PA3 TT2 EL memory MM EH EH MM ER2 IY memories MM EH EH MM ER2 IY ZZ minute MM 1H NN1 IH PA3 TT2 month MM AX NN1 TH nip NN1 IH IH PA2 PA3 PP nipped NN2 IH IH PA2 PA3 PP PA3 TT2 nipping NN1 IH IH PA2 PA3 PP IH NG nips NN1 IH IH PA2 PA3 PP SS NN2 AX OW no physical FF FF IH ZZ IH PA3 KK1 AX EL pin PP IH IH NN1 pinned PP IH IH NN1 PA2 DD1 pinning PP IH IH NN1 IH NG1 pins PP IH IH NN1 ZZ pledge PP LL EH FH PA3 JH pledged PP LL EH EH PA3 IH PA2 DD1 pledges PP LL EH EH PA3 JH IH ZZ pledging PP LL EH EH PA3 IH IH NG plus PP LL AX AX SS SS ray RR1 EH EY ravs RR1 EH EY ZZ ready RR1 EH EH PA1 DD2 IY red RR1 EH FH PA1 DD1 robot RR1 OW PA2 BB2 AA PA3 TT2 robots RR1 OW PA2 BB2 AA PA3 TT1 SS score SS SS PA3 KK3 OR second SS SS EH PA3 KK1 IH NN1 PA2 DD1 sensitive SS SS EH EH NN1 SS SS IH PA2 PA3 TT2 IH VV sensitivity SS SS EH EH NN1 SS SS IH PA2 PA3 TT2 IH VV IH PA2 PA3 TT2 IY SS SS IH IH NN1 SS SS YR sincere sincerely SS SS IH IH NN1 SS SS YR LL IY sincerity SS SS IH IH NN1 SS SS EH EH RR1 IH PA2 PA3 TT2 IY sister SS SS IH IH SS PA3 TT2 ER1 speak SS SS PA3 IY PA3 KK2 spell SS SS PA3 PP EH EH EL spelled SS SS PA3 PP EH EH EL PA3 DD1 SS SS PA3 PP EH EH EL ER2 speller spellers SS SS PA3 PP EH EH EL ER2 ZZ spelling SS SS PA3 PP EH EH EL IH NG spells SS SS PA3 PP EH EH EL ZZ start SS SS PA3 TT2 AR PA3 TT2 started SS SS PA3 TT2 AR PA3 TT2 IH PA1 DD2 starter SS SS PA3 TT2 AR PA3 TT2 ER1 starting SS SS PP3 TT2 AR PA3 TT2 IH NG starts SS SS PP3 TT2 AR PA3 TT1 SS stop SS SS PA3 TT1 AA AA PA3 PP stopped SS SS PA3 TT1 AA AA PA3 PP PA3 TT2 stopper SS SS PA3 TT1 AA AA PA3 PP ER1

SS SS PA3 TT1 AA AA PA3 PP IH

SS SS AX AX PA2 BB1 PA2 JH EH

SS SS AX PA2 BB1 PA2 JH EH EH

SS SS PA3 TT1 AA AA PA3 PP SS

PA3 KK2 PA3 TT2

PA3 KK2 PA3 TT2

NG

stopping

subject (noun)

subject (verb)

SS SS WW EH EH PA3 TT2 sweat SS SS WW EH EH PA3 TT2 IH PA3 sweated DD1 sweater SS SS WW EH EH PA3 TT2 ER1 sweaters SS SS WW EH EH PA3 TT2 ER1 ZZ sweating SS SS WW EH EH PA3 TT2 IH NG sweats SS SS WW EH EH PA3 TT2 SS switch SS SS WH IH IH PA3 CH switched SS SS WH IH IH PA3 CH PA3 TT2 switches SS SS WH IH IH PA3 CH IH ZZ2 switching SS SS WH IH IH PA3 CH IH NG2 system SS SS IH IH SS SS PA3 TT2 EH MM systems SS SS IH IH SS SS PA3 TT2 EH MM talk TT2 AO AO PA2 KK2 talked TT2 AO AO PA3 KK2 PA3 TT2 talker TT2 AO AO PA3 KK1 ER1 talkers TT2 AO AO PA3 KK1 ER1 ZZ talking TT2 AO AO PA3 KK1 IH NG talks TT2 AO AO PA2 KK2 SS thread TH RR1 EH EH PA2 DD1 threaded TH RR1 EH EH PA2 DD2 IH PA2 threader TH RR1 EH EH PA2 DD2 ER1 threaders TH RR1 EH EH PA2 DD2 ER1 ZZ threading TH RR1 EH EH PA2 DD2 IH NG threads TH RR1 EH EH PA2 DD2 ZZ then DH1 EH EH NN1 time TT2 AA AY MM times TT2 AA AY MM ZZ uncle AX NG PA3 KK3 EL whale WW EY EL whaler WW EY LL ER1 WW EY LL ER1 ZZ whalers whales WW EY EL ZZ whaling WW EY LL TH NG vear YY2 YR yes YYS EH EH SS SS

N-CHANNEL MOS (AUDIO)

SP0256 276-1784

TABLE 2—EXAMPLES OF SPELLING IRREGULARITIES

	Same sound represented by different letters	Different sounds represented by the same letters
Vowels	mEAt fEEt pEte pEOple pennY	vEIn forElgn dEIsm dEIcer gEIsha
Consonants	SHip tenSIon preCIous naTIon	althouGH GHastly couGH hiccouGH

TABLE 3—CONSONANT PHONEMES OF ENGLISH

		LABIAL	LABIO- DENTAL	INTER- DENTAL	ALVEO- LAR	PALATAL	VELAR	GLOTTAL
Stops:	Voiceless Voiced	PP BB			TT DD		KK GG	
Fricatives:	Voiceless Voiced	WH	FF VV	TH DH	SS ZZ	SH ZH*		нн
Affricates:	Voiceless Voiced					CH JH		
Nasals	Voiced	MM			NN		NG*	
Resonants	Voiced	ww			RR,LL	YY		

These do not occur in word-initial position in English.

Upper and Lower Lips Touch or Approximate

Labio-Dental: Upper Teeth and Lower Lip Touch

Inter-Dental: Tongue Between Teeth

Tip of Tongue Touches or Approximates Alveolar Ridge (just behind upper teeth) Alveolar:

Palatal:

Body of Tongue Approximates Palate (roof of mouth)
Body of Tongue Touches Velum (posterior portion of roof of Velar:

mouth)

Glottis (opening between vocal cords) Glottal:

TABLE 4-VOWEL PHONEMES OF ENGLISH

	FRONT	CENTRAL	BACK
High	YR IY IH*		UW# UH*#
Mid	EY EH* XR	ER AX*	OW# OY#
Low	AE*	AW# AY AR AA*	AO*# OR#

*SHORT VOWELS #ROUNDED VOWELS

TABLE 5—GUIDELINES FOR USING THE ALLOPHONES

Silence				
Silence			Voiced Stops	
	10 ms)	-before BB, DD, GG and JH	/BB1/	-final position: rib; between vowels:
,	30 ms)	-before BB, DD, GG, and JH		fibber;
PA3 (5	50 ms)	-before PP, TT, KK, and CH, and be-	/ppa/	-in clusters: bleed, brown
DA4 (1	100 ()	tween words	/BB2/ /DD1/	—initial position before a vowel: <u>b</u> east —final position: played, end
	100 ms) 200 ms)	 between clauses and sentences between clauses and sentences 	/DD2/	—initial position: down; clusters: drain
FA3 (2	200 1115)	—between clauses and sentences	/GG1/	-before high front vowels: YR, IY, IH,
Short V	owels		, 001,	EY, EH, XR
*/IH/		-sitting, stranded	/GG2/	-before high back vowels: UW, UH, OW,
*/EH/		extent, gentlemen		OY, AX; and
*/AE/		-extract, acting		—clusters; green, glue
*/UH/		—c <u>oo</u> kie, f <u>u</u> ll	/GG3/	-before low vowels: AE, AW, AY, AR,
*/AO/		—talking, song		AA, AO, OR, ER; and
*/AX/		—lapel, instruct		-medial clusters: anger; and final posi-
*/AA/		—pottery, cotton		tion: peg
Long Vo	owels		Voiceless Stops	
/IY/		-treat, people, penny	/PP/	—pleasure, ample, trip
/EY/		great, statment, tray	/TT1/	—final clusters before SS: tests, its
/AY/		-Kite, sky, mighty	/TT2/	-all other positions: test, street
/OY/		-noise, toy, voice	/KK1/	-before front vowels: YR, IY, IH, EY, EH,
/UW1/		-after clusters with YY; computer		XR, AY, AE, ER, AX;
/UW2/		—in monosyllabic words: two, food	2500000000	—initial clusters: cute, clown, scream
/OW/		-zone, close, snow	/KK2/	-final position: speak; final clusters: task
/AW/		-sound, mouse, down	/KK3/	-before back vowels: UW, UH, OW, OY,
/EL/		—litt <u>le,</u> ang <u>le</u> , gent <u>le</u> men		OR, AR, AQ; —initial clusters: crane, quick, clown,
R-Color	red Vov	vels		scream
		—letter, furniture, interrupt	Affricates	<u> </u>
<pre>/ER1/ /ER2/</pre>		-monosyllables: bird, fern, burn	/CH/	-church, feature
/OR/		-fortune, adorn, store	/JH/	— <u>indge</u> , injure
/AR/		-farm, alarm, garment	Nasal	_լաս <u>գ</u> ս, ուլաւս
/YR/		-hear, earring, irresponsible	/MM/	—milk, alarm, ample
/XR/		-hair, declare, stare	/NN/	before front and central vowels: YR, IY,
Resonan	, to			IH, EY, EH, XR, AE, ER, AX, AW, AY,
	115			UW; final clusters: earn
/WW/		—we, warrant, linguist	/NN2/	-before back vowels: UH, OW, OY, CR,
/RR1/		-initial position: read, write, x-ray		AR, AA
/RR2/ /LL/		—initial clusters: brown, crane, grease —like, hello, steel	/NG/	—stri <u>ng,</u> a <u>ng</u> er
/YY1/		-clusters: cute, beauty, yarn, yo-yo	*These allophone	s can be doubled.
/YY2/		-initial position: yes, yarn, yo-yo		
Voiced I	Fricative			
/VV/	LICALIVE			
/VV/ /DH1/		vest, prove, evenword-initial position: this, then, they		
/DH2/		-word-final and between vowels: bathe,		
		bathing		
/ZZ/		—zoo, phase		
/ZH/		—beige, pleasure		
Voiceles	s Fricat	ives		
*/FF/		-) These may be doubled for initial posi-		
21.00.00.00		tion and used singly in final position		
*/TH/		—)		
*/SS/		—)		
/SH/		— <u>sh</u> irt, lea <u>sh</u> , na <u>ti</u> on		
/HH1/		-before front vowels, RY, IY, IH EY, EH,		
17.17.7.0.1		XR, AE		
/HH2/		-before back vowels: UW, UH, OW, OY,		
/WH/		AO, OR, AR —white, whim, twenty		
/ ***11/		winte, within, twomy		

TABLE 6-ALLOPHONE ADDRESS TABLE

	TABLE 6—ALLOPHONE ADDRESS TABLE					
		DDRESS ALLOPHONE	SAMPLE WORD	DURATION		
				10MS		
	000	PA1	PAUSE PAUSE	30MS		
	001	PA2	PAUSE	50MS		
	002 003	PA3 PA4	PAUSE	100MS		
	003	PA5	PAUSE	200MS		
	004	/OY/	Boy	420MS		
	006	/AY/	Sky	260MS		
	007	/EH/	End	70Ms		
	010	/KK3/	Comb	120MS		
	011	/PP/	Pow	210MS		
	012	/IH/	Dodge	140MS		
	013	/NN1/	Thin	140MS		
	014	/IH/	Sit	70MS		
	015	/TT2/	to	140MS		
	016	/RR1/	Rural	170MS		
	017	/AX/	Succeed	70MS		
	020	/MM/	Milk	180MS		
	021	/TT1/	Part	100MS		
	022	/DH1/	They	290MS		
	023	/IY/	See	250MS		
	024	/EY/	Beige	280MS		
	025	/DD1/	Could	70MS		
	026	/UW1/	To	100MS		
	027	/AO/	Aught Hot	100MS 100MS		
	030	/AA/	Yes	180MS		
	031	/YY2/ /AE/	Hat	120MS		
	032	/HH1/	He	130MS		
	033 034	/BB1	Business	80MS		
	035	/TH/	Thin	180MS		
	036	/UH/	Book	100MS		
	037	/UW2/	Food	260MS		
١	040	/AW/	Out	370MS		
	041	/DD2/	Do	160MS		
١	042	/GG3/	Wig	140MS		
١	043	/VV/	Vest	190MS		
	044	/GG1/	Got	80MS		
l	045	/SH/	Ship	160MS		
١	046	/ZH/	Azure	190MS		
l	047	/RR2/	Brain	120MS		
l	050	/FF/	Food	150MS		
١	051	/KK2/	Sky	190MS		
١	052	/KK1/	Can't	160MS		
١	053	ZZ	Zoo Anchor	210MS 220MS		
	054	/NG/ /LL/	Anchor Lake	110MS		
	055	/LL/ /WW/	Wool	180MS		
	056	/ VV VV / / X R/	Repair	360MS		
١	057 060	/XK/ /WH/	Whig	200MS		
l	061	/YY1/	ves	130MS		
١	062	/CH/	Church	190MS		
١	063	/ER1/	Fir	160MS		
١	064	/ER2/	Fir	300MS		
١	065	/OW/	Beau	240MS		
١	066	/DH2/	They	240MS		
١	067	ISSI	Vest	90MS		
1	070	/NN2/	No	190MS		
1	071	/HH2/	Hoe	180MS		
	072	/OR/	Store	330MS		
1	073	/AR/	Alarm	290MS		
	074	/YR/	Clear	350MS		
	075	/GG2/	Guest	40MS 190MS		
	076	/EL/	Saddle Business	190MS 50MS		
1	077	/BB2/	Dusiness	201010		
١						

RADIO CONTROL ELECTRONIC KIT 277-1012

GENERAL DESCRIPTION

This module was designed for radio control of cars, racers and boats. It can be operated in forward, forward with right turn, forward with left turn and backward. The carrier frequency is 27 MHz. The control commands are transmitted by tone pulse.

Forward-without carrier.

Forward W/right turn—carrier with 3000 Hz pulse modulation.

Forward W/left turn-carrier with 500 Hz pulse modulation.

Backward-carrier only.

There are some wires & external components that you need.

Please see External Component Requirements.

EXTERNAL COMPONENT REQUIREMENTS

	Transmitter	Recommendations			
Ant	Transmitting antenna	0.5 meter (20 inch) length telescope antenna or steel wire.			
S1	Functional switch for driving	Two poles, two throw switch (DPDT) (275-663)			
S2 Functional switch for steering		Two poles, two throw switch with center (DPDT) (275-664)			
Battery snap		For 006P 9V battery (270-325)			
Receiver		Recommendations			
Ant.	Receiving antenna	0.3 meter (12 inch) length steel wire			
M1	Steering motor	3V motor (Mabuchi motor RN-140-14180)			
M2	Driving motor	3V motor (Mabuchi motor RE-280-2865)			
S1	ON/OFF switch	2 poles, 2 throw slide switch (DPDT) (275-607)			
	Battery snap	For 006P 9V battery (270-325)			
	Battery holder	For two D cells 1.5V (270-386)			

CONTROL INSTRUCTIONS

The receiver will respond to commands as follows:

Action	Command
Forward	ON/OFF switch of receiver is switched ON.
Forward and Right	Poles of functional switch S2 are at the "R" position
Forward and Left	Poles of functional switch S2 are at the "L" position
Backward	Poles of functional switch S1 are at the "B" position

Note: There are no steering functions while the car is being driven backward. If the system is out of command, please read the trouble shooting.

SIMPLE ADJUSTMENTS

- 1. Adjust L1 for best response to 27.145 MHz signal from a standard signal generator. Insert a 5 pF capacitor in series between the signal generator and receiver's antenna input.
- 2. Adjust L3 for maximum transmitter output power as indicated on a field strength meter.
- 3. Adjust L4 for proper transmitter oscillation as indicated by maximum reading on a field strength meter.

TROUBLESHOOTING

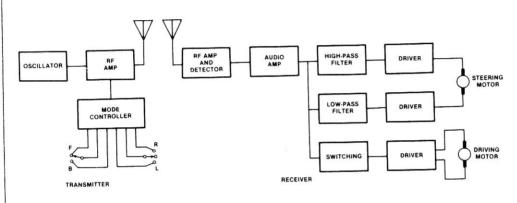
Trouble	Possible Cause	Solution
No function	Low battery voltage	Replace batteries
	Poor soldering	Checked soldering
	Wrong connection	Checked connection
	Corroded functional switch and ON/OFF switch.	Replace functional switch and ON/OFF switch
Insufficient control distance	Low battery voltage	Replace batteries
	Poor soldering for antenna	Checked soldering for antenna
	Length of antennas are not suitable	Replace with suitable antenna.

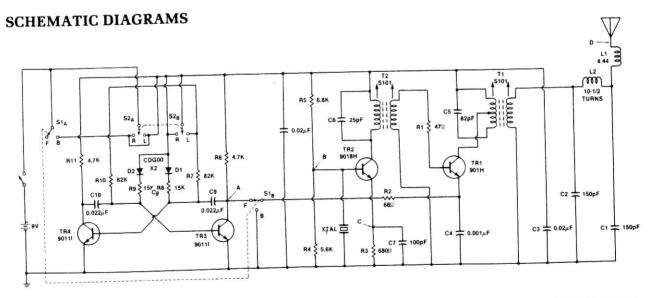
277-1012

ABSOLUTE MAXIMUM RATINGS

Transmitter	
E 27.145 M	IHZ
Current	
O P. Waltana	. 0 4
Battery Life	,1113
Receiver	/H2
Frequency	mA
Current	.9V
Operating Voltage	

BLOCK DIAGRAM

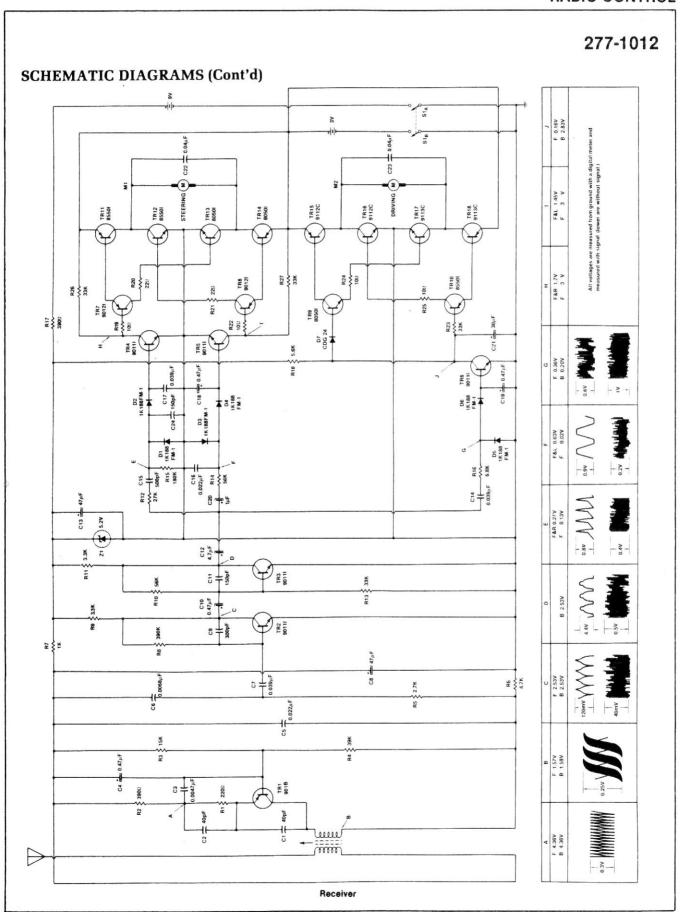




			С		D	
A	2.3V	2.2V	4.0V	B = CARRIER	F&L = 500Hz	F&R = 3000Hz
VOLTAGE 2.9V	sv MM					

Note:All voltages are measured from ground with digital meter

Transmitter



UM1285-8 277-221

VHF MODULATOR

GENERAL DESCRIPTION

The UM1285-8 is a high performance intercarrier vestigial sideband modulator which is primarily intended for use in color TV games, home computer, graphics, teletext and view data adapters. The modulator has a very linear transfer characteristic which ensures good chroma levels and freedom from sync compression and associated frame and line jitter problems, good subcarrier inter modulation performance minimizes the on screen bar pattern due to chroma and sound subcarrier beats.

FEATURES

- · Compact & low profile
- · Rugged & stable
- Good modulation linearity
- · Low chroma/sound beat product (55 dB typ)
- Pretuned vision carriers Ch 3, Ch 4
- Pretuned sound subcarrier 4.5 MHz
- · Pretuned vestigial sideband filter
- Built-in voltage regulator
- · Negative transfer characteristic
- For color application
- · 75 ohm output from a standard phono socket

ABSOLUTE MAXIMUM RATINGS

Voltage between Pin 1, 3, 4, and Case Ground 3.0	o + 15 V
Voltage between Pin 3 and V _{CC} 3.0 t	o + 8.0 V
(Refer to table for high voltage application.)	
Operating Temperature Range	o + 45 °C
Storage Temperature Range	o + 70°C

ELECTRICAL CHARACTERISTICS
V _{CC}
(Refer to table for higher supply voltage application.)
RF Output Load
Channel 3 Video Carrier
Channel 4 Video Carrier
Sound Carrier
Video Carrier output (Vmod = 2.2 V)
Video Carrier output (Vmod = 2.8 V)
Sound Carrier output
Spurious/Harmonic
Voltage Standing Wave Ratio (CH 3 and CH 4)
ΔF for Change in Temperature
ΔF for Change in Temperature
ΔF for 1 Volt Change in V _{CC} ±30 kHz/V
ΔF for 1 Volt Change in V _{CC}
RF Output Impedance
- 3DB Bandwidth (RF)
CH 3
CH 4
Supply Current
Frequency modulating
Sensitivity Chroma/Sound Beat Level

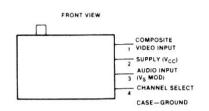
TABLE

Supply Voltage V _{CC}	Volt	6.0	7.5	9.0	12.0	15.0
Series Resistor R _S	Ohm	0	47	100	180	270

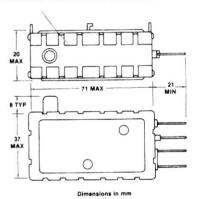
Series resistor with respect to supply voltage



PIN CONNECTION



DIMENSIONAL DIAGRAM



RF OUTPUT SOCKET



Phono Socket

Typical Phono Plug

UM1285-5 277-221

TYPICAL CHARACTERISTICS

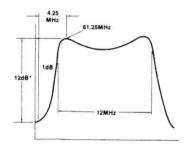
The UM1285-8 is designed to work over a wide range of supply voltage from 6 to 15 V (V_{CC}). A built-in 5.0 V (V_{DD}) voltage regulator is provided to achieve excellent stability against voltage change. A series resistor is recommended in putting between power source and modulator supply input for purpose of current limiting.

Modulation occurs when a positive going voltage is applied to the modulation input (video) pin. The transfer characteristic is negative, that means a positive input causes the RF output to decrease. Peak RF output is specified when the video input is at $2.2~\rm V$.

RF channel frequency of Ch 3 or Ch 4 can be selected by connecting channel select pin to ground level (0V) to have Ch 3, or open connection to have Ch 4.

FCC APPROVABLE

The UM1285-8 is FCC approvable due to its very low radiation, stabilized carrier oscillators and vestigial side bank filter which ensures all side band components outside FCC limits are greater than 30 dB down.



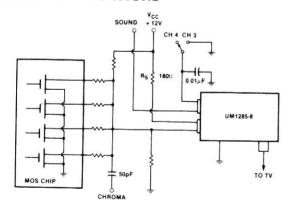
*Note: Subcarriers are > 18dB down wrt carrier at Input to bandpass
filter giving maximum out of band level of < 20dB wrt posters

1.0 0.8 - 0.8 - 0.8 - 0.4 0.4 0.4 0.0 0.01 mA VIDEO MODULATING SIGNAL AT VIDEO INPUT

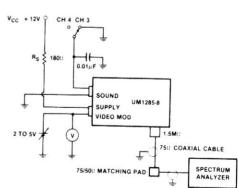
Typical Transfer Characteristic

Typical Bandpass Filter Response

TYPICAL APPLICATIONS



Typical Application

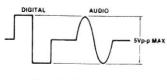


Note: 1. In case of testing with 50t: 1/P spectrum analyzer, matching pad 75/50t: (attenuation 10dB) shound be employed.

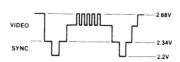
2. Standard RF coaxial cable should be 1.5 meters long and 75ti characteristic impedance.

Test Circuit

TYPICAL INPUT WAVEFORMS

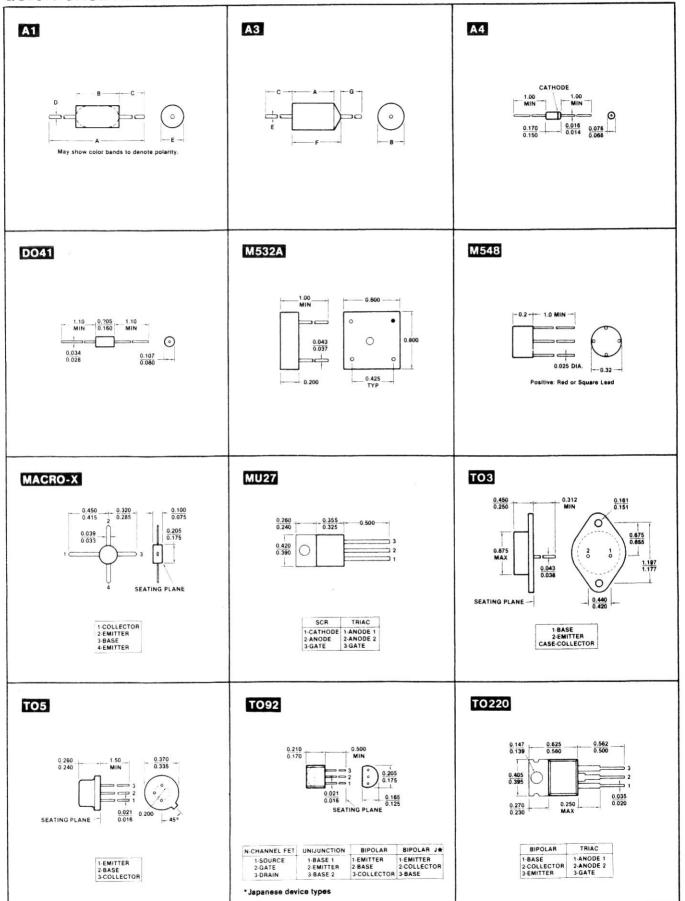


Sound I/P Setup

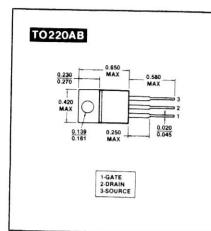


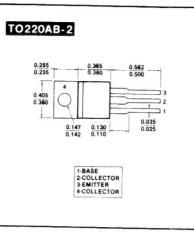
Modulated Input Voltage Setup

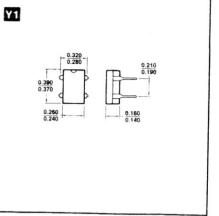
QUICK CASE REFERENCE



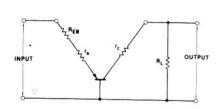
QUICK CASE REFERENCE

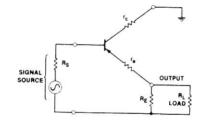


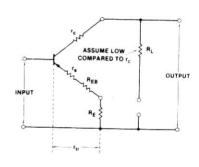




USEFUL INFORMATION







Parameters of Common-Base Circuit

Input Impedance Zin

$$Z_{in} = r_{tr}$$

Load Impedance

 $Z_L = R_L$ in parallel with input impedance of following stage.

Current Gain

$$A_i = \alpha = \frac{\beta}{1 + \beta}$$

(In practice, α is 0.95 to

0.995, or approximately 1.)

Voltage Gain

$$A_{v} \approx \frac{Z_{L}}{r_{tr}} = g_{m}Z_{L}$$

Parameters of Common-Collector Circuit

Input Impedance

$$Z_{in} = (\beta + 1)Z_{L}$$

where

Z_L is R_L in parallel with R_E.

Output Impedance

$$Z_{\text{out}} = \frac{R_s}{\beta + 1}$$

where.

R_s is the output imped

ance of the signal source

Current Amplification

Voltage Amplification $A_v = Less than unity$

Parameters of Common-Emitter Circuit

Input Impedance

$$Z_{in} = h_{fe}r_{tr}$$

Load Impedance

 $Z_L = R_L$ in parallel with input impedance of next stage.

Current Gain

$$A_i = \frac{\Delta I_C}{\Delta I_B} = h_{fe}$$

where

$$h_{fe} = \beta = \frac{l_c}{l_b} = \frac{\alpha}{1 - \alpha}$$

Voltage Gain

$$A_{v} = \frac{\Delta V_{C}}{\Delta V_{B}} = \frac{Z_{L}}{r_{tr}} = g_{m}Z_{L}$$

Power Gain

$$A_{p} = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \beta \frac{Z_{L}}{r_{tr}}$$

IMPORTANT SUGGESTIONS ON THE USE AND REPLACEMENT OF TRANSISTORS

You can use various styles and sizes of transistors in any given circuit application, as long as the electrical characteristics of the device are within the required range of operation. Thus, a tab-type device can be used to replace a TO-3 or TO-66 case device; or a small epoxy-type device can be used in place of TO-5 or other size transistor.

Generally speaking, you must observe the following maximum characteristics of a transistor when contemplating substitution or selection:

Power dissipation

Maximum collector current

Maximum collector-to-emitter voltage

Maximum collector-to-base voltage

Maximum emitter-to-base voltage

Also, it is useful to consider the following characteristics for actual circuit operation:

Gain

Frequency limitations

Caution: It may be necessary in some cases to adjust bias values to achieve required operation. With tuned circuits, it is a good practice to check alignment after replacing any transistor.

When replacing power transistors, always check driver devices to be sure they are OK. Also, check other circuit components to be sure they were not shorted (or otherwise defective) when the original device failed. If you fail to correct such problems before applying power to the circuit once again, the replacement transistor could easily be permanently damaged. Be sure to use proper heat-sink precautions and use silicon grease to reduce the thermal resistance between the case of the transistor and the heat-sink.

Always observe temperature limitations as specified with transistor ratings.

It almost goes without saying, but let us remind you anyway—

Always observe voltage polarity with all semiconductor devices.

CROSS-REFERENCE/SUBSTITUTION LISTING

Most users of semiconductors realize that it is almost impossible to guarantee absolute equivalents (as in the case of tubes). Thus, the only way to create replacement or cross-reference listings is by carefully evaluating each characteristic of both devices (original transistor and the possible alternate). This is how the Technical Staff of Radio Shack went about preparing the following cross-reference/replacement lists.

IMPORTANT NOTE

We caution you that in many cases the listed cross reference ARCHER device may be different in appearance, size or mounting style. Thus, before beginning replacement or installation procedures, check to be sure you have enough room for proper mounting.

Also, when making substitutions or replacements in radio or high frequency circuitry, it may be necessary to realign tunable circuit elements. This is true even when making **exact** replacements (junction capacitances normally vary between devices even from the same production run).

Information contained in this guide is based on the latest available data and is believed to be accurate. Every care has been taken to assure technical accuracy. However, Radio Shack does not assume responsibility for any contingencies of the use of this information. Nor does Radio Shack assume any responsibility for any infringements of patents or other rights of third parties which may result from its use.

When you are looking for a specific number and it does not show up in the following listing—refer to the technical data provided for our line of ARCHER devices. With this information you probably will be able to make a suitable substitution.

MAJOR SEMICONDUCTOR COMPONENTS

NAME OF DEVICE	CIRCUIT SYMBOL	COMMONLY USED JUNCTION SCHEMATIC	ELECTRICAL (CHARACTERISTICS	MAX RATINGS AVAILABLE	MAJOR APPLICATIONS	ROUGHLY ANALOGOUS TO:
Diode or Rectifier	ANODE	ANODE	VANODE (-)	Conducts easily in one direction, blocks in the other	1500 Amps 3000 Volts	Rectification Blocking Detecting Steering	Check valve Diode tube Gas diode
Avalanche (Zener) Diode	ANODE	ANODE P n CATHODE	Vanode (-)	Constant voltage characteristic in negative quadrant E(+)	22 Volts 1 Watt	Regulation Reference Clipping	V-R tube
Integrated Voltage Regulator (IVR)	3 IVR 2	3 n n p n n n n n n n n n n n n n n n n	R ₃₁ 1 .7 .5	Programmed to desired V ₂₁ by two resistors 92	40 Volts 100 mA 0.4 Watts	Shunt voltage regulator Reference element Error modifier Level sensing Level shifting	Avalanche Diode
Tunnel Diode	POSITIVE ELECTRODE NEGATIVE ELECTRODE	POSITIVE ELECTRODE P NEGATIVE ELECTRODE	Vanode (-)	Displays negative resistance when current exceeds peak point current lp	Peak point current = 100 mA Resistive cutoff freq. = 40 Gc	UHF converter Logic circuits Microwave circuits Level sensing	None
Back Diode	ANODE	ANODE n p CATHODE	Vanode (-)	Similar characteristics to conventional diode except very low forward voltage drop	5 mA 400 mV	Microwave mixers and low power oscillators	None
Thyrector	*	P n	VOLTAGE	Rapidly increasing current above rated voltage in either direction	70 A peak pulse (2" Sq. cell)	Transient voltage suppression and arc suppression	Thyrite Two avalanche diodes in inverse-series connection
n-p-n Transistor	COLLECTOR BASE EMITTER	BASE P EMITTER	Ic IB5 IB5 IB3 IB3 IB2 IB1 I	Constant collector current for given base drive	300 Volts 25 Watts	Amplification Switching Oscillation	Pentode Tube
p-n-p Transistor	COLLECTOR BASE IS EMITTER	BASE P EMITTER	VCOLLECTOR (-) 0 B	Complement to n-p-n transistor	75 Volts 25 Watts	Amplification Switching Oscillation	None
Photo Transistor	COLLECTOR BASE IB EMITTER	COLLECTOR n p n EMITTER	H4 H3 H2 H1 V _{CE}	Incident light acts as base current of the photo transistor	0.25 Amps 0.6 Watts	Tape readers Card readers Position sensor Tachometers	None
Unijunction Transistor (UJT)	BASE 2	BASE 1	WILLIAM O EMITTER I'S	Unijunction emitter blocks until its voltage reaches V_p ; then conducts	0.450 Watts (nterval timing Oscillation Sevel Detector SCR Trigger	None

MAJOR SEMICONDUCTOR COMPONENTS

AME OF		MAJOR SER	ELECTRICAL CHAR		MAX RATINGS AVAILABLE	MAJOR APPLICATIONS	ROUGHLY ANALOGOUS TO:
mple- entary hijunction ansistor UJT)	BASE 1	SCHEMATIC	V _E	Functional complement to UJT	0.30 Watts	igh stability N timers Oscillators and level detectors	lone
ogram- able nijunction ansistor UT)	ANODE GATE	ANODE P GATE	VALLEY POINT PEAK	Programmed by two resistors for V _p , I _p , I _v . Function equivalent to normal UJT.	0.30 Watts 0.15 Amps	ow cost timers and oscillators ong period timers SCR trigger Level detector	Τμυ
ilicon ontrolled ectifier GCR)	ANODE GATE CATHODE	ANODE P P n P n IGATE	ANODE (-) VANODE (-)	With anode voltage (+), SCR can be triggered by Ig. remaining in conduction until anode I is reduced to zero	1800 Volts	Power switching Phase control Invertets Choppers	Gas thyratron or ignitron
comple- nentary filicon Controlled Rectifier CSCR)	ANODE	ANODE GATE	VAC (-)	Polarity comple- ment to SCR	00	Ring counters Low speed logic Lamp driver	None
Light Activated SCR* (LASCR)	ANODE GATE CATHODE	ANODE P n P n GATE	V _{ANODE} (-)	Operates similar to SCR, except can also be triggered into conduction by light falling on junctions	1.6 Amps 200 Volts	Relay Replace- ment Position controls Photoelectric applications Slave flashes	None
Silicon Controlled Switch* (SCS)	CATHODE GATE		Vanode (-)	Operates similar to SCR except can also be triggered on by a negative signal on anode-gate. Also several other specialized modes of operation	100 Volts 200 mA	Logic applications Counters Nixie drivers Lamp drivers	transistor pair
Silicon Unilateral Switch (SUS)	ANODE GATE CATHODE	ANODE GATE P n P P CATHODE	VANODE (*)	Similar to SCS by zener added to ano gate to trigger devi into conduction at ~ 8 volts. Can also triggered by negati pulse at gate lead.	de 0.200 Amps ice 10 Volts	Switching Circuits Counters SCR Trigger Oscillator	Shockley or 4-layer diode
Silicon Bilateral Switch (SBS)	GATE ANODE 1	GATE ANODE	RB VANODE 2(Symmetrical bilateral version of the SUS. Breaks down in both directions as SUS does in forward.		Switching Circuits Counters TRIAC Phase Control	Schockley diodes
Triac	ANODE 2 GATE ANODE 1	n P	VANODE 2(-)	Operates similar to SCR except car be triggered into conduction in eith direction by (+) o (-) gate signal	ner	AC switching Phase control Relay replacemen	
Diac Trigger		GATE ANODE		When voltage reaches trigger level (about 35 volts), abruptly switches down about 10 volts.	40 Volts 2 Amps pea	Triac and k SCR trigger Oscillator	Neon lamp

GLOSSARY OF WORDS, SYMBOLS AND ABBREVIATIONS

The following letter symbols and abbreviations are recommended by the Joint Electron Device Engineering Council (JEDEC) of the Electronic Industries Association (EIA) and the National Electrical Manufacturers Association (NEMA) for use in semiconductor device data sheets and specifications.

- A, a —Anode
- B, b −Base
- \mathbf{b}_{fs} —Common-source small-signal forward transfer susceptance
- **b**_{is} —Common-source small-signal input susceptance
- **b**_{os} —Common-source small-signal output susceptance
- \mathbf{b}_{rs} —Common-source small-signal reverse transfer susceptance
- C, c -Collector
- \mathbf{C}_{cb} —Collector-base interterminal capacitance
- Cce -Collector-emitter interterminal capacitance
- C_{ds} —Drain-source capacitance
- Cdu -Drain-substrate capacitance
- \mathbf{C}_{eb} —Emitter-base interterminal capacitance
- $\mathbf{C}_{\mathrm{ibo}}$ —Common-base open-circuit input capacitance
- C_{ibs} —Common-base short-circuit input capacitance
- Cieo —Common-emitter open-circuit input capacitance
- Cies -Common-emitter short-circuit input capacitance
- $\mathbf{C}_{\mathrm{iss}}$ —Common-source short-circuit input capacitance
- $\mathbf{C}_{\mathrm{obo}}$ —Common-base open-circuit output capacitance
- $\mathbf{C}_{\mathrm{obs}}$ —Common-base short-circuit output capacitance
- Common-emitter open-circuit output capaci-
- $\mathbf{C}_{\mathrm{oes}}$ —Common-emitter short-circuit output capaci-
- Coss —Common-source short-circuit output capacitance
- C_{rbs} —Common-base short-circuit reverse transfer
- **C**_{res} —Common-collector short-circuit reverse transfer capacitance
- C_{res} —Common-emitter short-circuit reverse transfer capacitance
- C_{rss} —Common-source short-circuit reverse transfer capacitance
- Ctc -Collector depletion-layer capacitance
- Cte -Emitter depletion-layer capacitance
- D, d -Drain
- E, e -Emitter
- η -Intrinsic standoff ratio
- **f**_{hfb} —Common-base small-signal short-circuit forward current transfer ratio cutoff frequency
- f_{hfc} —Common-collector small-signal short-circuit forward current transfer ratio cutoff frequency
- fhie —Common-emitter small-signal short-circuit forward current transfer ratio cutoff frequency
- f_{max} —Maximum frequency of oscillation
- FT —Transition frequency (frequency at which common-emitter small-signal forward current transfer ratio extrapolates to unity)
- G, g -Gate
- gis —Common-source small-signal forward transfer conductance
- gis -Common-source small-signal input conductance
- **g**_{MB} —Common-base static transconductance
- **g**MC —Common-collector static transconductance
- gme -Common-emitter static transconductance
- **g**_{os} —Common-source small-signal output conductance
- GPB -Common-base large-signal insertion power gain
- **G**_{pb} —Common-base small-signal insertion power gain
- **G**_{PC} —Common-collector large-signal insertion power gain

- \mathbf{G}_{pc} —Common-collector small-signal insertion power
- **G**PE —Common-emitter large-signal insertion power gain
- G_{pe} —Common-emitter small-signal insertion power gain
- **G**_{pg} —Common-gate small-signal insertion power gain
- \mathbf{G}_{ps} —Common-source small-signal insertion power gain
- grs —Common-source small-signal reverse transfer conductance
- G_{TB} —Common-base large-signal transducer power gain
- \mathbf{G}_{tb} —Common-base small-signal transducer power gain
- **G**_{TC} —Common-collector large-signal transducer power gain
- G_{tc} —Common-collector small-signal transducer power gain
- GTE —Common-emitter large-signal transducer power gain
- **G**_{te} —Common-emitter small-signal transducer power
- \mathbf{G}_{tg} —Common-gate small-signal transducer power
- G_{ts} —Common-source small-signal transducer power gain
- **h**_{FB} —Common-base static forward current transfer ratio
- h_{fb} —Common-base small-signal short-circuit forward current transfer ratio
- **h**_{FC} —Common-collector static forward current transfer ratio
- **h**_{fc} —Common-collector small-signal short-circuit forward current transfer ratio
- **h**_{FE} —Common-emitter static forward current transfer ratio
- **h**_{fe} —Common-emitter small-signal short-circuit forward current transfer ratio
- \mathbf{h}_{FEL} —Inherent large-signal forward current transfer ratio
- h_{IB} —Common-base static input resistance
- \mathbf{h}_{ib} —Common-base small-signal short-circuit input impedance
- h_{IC} —Common-collector static input resistance
- **h**_{ic} —Common-collector small-signal short-circuit input impedance
- h_{IE} —Common-emitter static input resistance
- $\begin{array}{ll} \boldsymbol{h}_{ie} & -Common-emitter\ small-signal\ short-circuit\ input\\ impedance \end{array}$
- $\mathbf{h}_{\text{ie}(\text{imag})}$ —Imaginary part of common-emitter small-signal short-circuit input impedance
- h_{ie[real]} —Real part of common-emitter small-signal shortcircuit input impedance
- \mathbf{h}_{ob} —Common-base small-signal open-circuit output admittance
- h_{oc} —Common-collector small-signal open-circuit output admittance
- \mathbf{h}_{oe} —Common-emitter small-signal open-circuit output admittance
- h_{oe(imag)}—Imaginary part of common-emitter small-signal open-circuit output admittance

hoe(real) -Real part of common-emitter small-signal opencircuit output admittance

Common-base small-signal open-circuit reverse \mathbf{h}_{rh} voltage transfer ratio

-Common-collector small-signal open-circuit re- \mathbf{h}_{rc} verse voltage transfer ratio

 \mathbf{h}_{re} -Common-emitter small-signal open-circuit reverse voltage transfer ratio

-Base-terminal dc current IB

-Alternating component (rms value) of base-ter-I b minal current

 Instantaneous total value of base-terminal current iΒ

IBEV -Base cutoff current, dc

I_{B2(mod)} - Interbase modulated current -Collector-terminal dc current Ic

Ic -Alternating component (rms value) of collectorterminal current

 Instantaneous total value of collector-terminal $i_{\rm C}$ current

ICBO -Collector cutoff current (dc), emitter open

ICEO -Collector cutoff current (dc), base open

-Collector cutoff current (dc), specified resistance between base and emitter

-Collector cutoff current (dc), base shorted to ICES emitter

ICEV -Collector cutoff current (dc), specified voltage between base and emitter

ICEX -Collector cutoff current (dc), specified circuit between base and emitter

-Drain current, dc I_D

ID[off] -Drain cutoff current

I_{D(on)} —On-state drain current

IDSS -Zero-gate-voltage drain current

-Emitter-terminal dc current IE

Le -Alternating component (rms value) of emitterterminal current

ie. Instantaneous total value of emitter-terminal current

IEBO -Emitter cutoff current (dc), collector open

IEB20 -Emitter reverse current

I_{EC(ofs)} -Emitter-collector offset current

-Emitter cutoff current (dc), base short-circuited to collector

I_{E1E2(off)}—Emitter cutoff current

-For voltage-regulator and voltage-reference diodes: dc forward current. For signal diodes and rectifier diodes: dc forward current (no alternating component)

I -Alternating component of forward current (rms value)

iF -Instantaneous total forward current

I_{F(AV)} — Forward current, dc (with alternating component)

I_{FM} —Maximum (peak) total forward current

I_{F(OV)} —Forward current, overload

IFRM -Maximum (peak) forward current, repetitive

I_{F(RMS)} —Total rms forward current

I_{FSM} -Maximum (peak) forward current, surge

-Gate current, dc

-Forward gate current I_{GF}

 I_{GR} -Reverse gate current

IGSS -Reverse gate current, drain short-circuited to source

I_{GSSF} —Forward gate current, drain short-circuited to source

IGSSR -Reverse gate current, drain short-circuited to source

I -Inflection-point current Im(hie)—Imaginary part of common-emitter small-signal short-circuit input impedance

Im(hoe)-Imaginary part of common-emitter small-signal open-circuit output admittance

-Average forward current, 180° conduction angle, I_{O} 60-Hz half sine wave

IP -Peak-point current

-For voltage-regulator and voltage-reference di-IR odes: dc reverse current. For signal diodes and rectifier diodes: dc reverse current (no alternating component)

-Alternating component of reverse current (rms I

Instantaneous total reverse current

I_{R(AV)}—Reverse current, dc (with alternating component)

I_{RM} -Maximum (peak) total reverse current

I_{RRM} -Maximum (peak) reverse current, repetitive

IRIRMS - Total rms reverse current

-Maximum (peak) surge reverse current IRSM

-Source current, dc I_S

I_{SDS} —Zero-gate-voltage source current

Isloff -Source cutoff current

Iv —Valley-point current

 I_Z -Regulator current, reference current (dc)

-Regulator current, reference current (dc near I_{ZK} breakdown knee)

-Regulator current, reference current (dc maxi- I_{ZM} mum rated current)

K, k -Cathode

—Conversion loss L

M -Figure of merit

NF_o -Overall noise figure

NR_o -Output noise ratio

-Power input (dc) to base, common emitter \mathbf{P}_{BE}

-Instantaneous total power input to base, com-PRE mon emitter

 P_{CB} -Power input (dc) to collector, common base

-Instantaneous total power input to collector, **P**CB common base

 \mathbf{P}_{CE} -Power input (dc) to collector, common emitter

-Instantaneous total power input to collector, PCE common emitter

 \mathbf{P}_{EB} -Power input (dc) to emitter, common base

-Instantaneous total power input to emitter, com-PEB mon base

 \mathbf{P}_{F} -Forward power dissipation, dc (no alternating component)

-Instantaneous total forward power dissipation

P_{F(AV)}—Forward power dissipation, dc (with alternating component)

 P_{FM} -Maximum (peak) total forward power dissipation

 \mathbf{P}_{IB} Common-base large-signal input power

-Common-base small-signal input power Dib

-Common-collector large-signal input power \mathbf{P}_{IC}

-Common-collector small-signal input power \mathbf{p}_{ic}

 \mathbf{P}_{IE} -Common-emitter large-signal input power

-Common-emitter small-signal input power

Pie

 P_{OB} -Common-base large-signal output power

-Common-base small-signal output power $\boldsymbol{p}_{\mathrm{ob}}$

 P_{OC} -Common-collector large-signal output power

-Common-collector small-signal output power \mathbf{p}_{oc}

POE -Common-emitter large-signal output power

-Common-emitter small-signal output power \mathbf{p}_{oe}

 \mathbf{P}_{R} -Reverse power dissipation, dc (no alternating component)

-Instantaneous total reverse power dissipation

 $\mathbf{P}_{\mathsf{R}(\mathsf{AV})}$ —Reverse power dissipation, dc (with alternating component)

P_{RM} —Maximum (peak) total reverse power dissipation \mathbf{P}_{T}

-Total nonreactive power input to all terminals -Nonreactive power input, instantaneous total, to DT all terminals

 \mathbf{Q}_{S} -Stored charge

-Interbase resistance \mathbf{r}_{BB}

 $r_b'C_c$ —Collector-base time constant

r_{CE(sat)} -Saturation resistance, collector-to-emitter

r_{DS(on)} -Static drain-source on-state resistance

r_{ds(on)} -Small-signal drain-source on-state resistance

Re(hie) - Real part of common-emitter small-signal shortcircuit input impedance

Re(hoe) — Real part of common-emitter small-signal opencircuit output admittance

r_{e1e2(on)} -Small-signal emitter-emitter on-state resistance

r -Dynamic resistance at inflection point

 $\boldsymbol{R}_{\boldsymbol{\theta}}$ -Thermal resistance

Reca -Thermal resistance, case to ambient

 $\mathbf{R}_{\Theta | A}$ —Thermal resistance, junction to ambient

Rolc -Thermal resistance, junction to case

S, s -Source

 T_A -Ambient temperature or free-air temperature

 $T_{\rm C}$ -Case temperature

-Delay time t_d

td(off) -Turn-off delay time

td(on) -Turn-on delay time

-Fall time tr

tfr -Forward recovery time

T -Junction temperature -Turn-off time toff

-Turn-on time ton

-Pulse time t_p

t, -Rise time

trr -Reverse recovery time

t. -Storage time

TSS -Tangential signal sensitivity

 $\mathbf{T}_{\mathrm{stg}}$ -Storage temperature

Pulse average time

U, u -Bulk (substrate)

V_{BB} —Base supply voltage (dc)

 \mathbf{V}_{BC} -Average or dc voltage, base to collector

-Instantaneous value of alternating component \mathbf{V}_{bc} of base-collector voltage

 \mathbf{V}_{BE} -Average or dc voltage, base to emitter

-Instantaneous value of alternating component of base-emitter voltage

V_(BR) -Breakdown voltage (dc)

v_(BR) —Breakdown voltage (instantaneous total)

V_{(BR)CBO} —Collector-base breakdown voltage, emitter open

V_{|BR|CEO} —Collector-emitter breakdown voltage, base open $\mathbf{V}_{\mathsf{IBR}|\mathsf{CER}}$ —Collector-emitter breakown voltage, resistance

between base and emitter $\mathbf{V}_{(\mathsf{BR})\mathsf{CES}}$ —Collector-emitter breakdown voltage, base

shorted to emitter

 $\mathbf{V}_{ ext{(BR)CEV}}$ —Collector-emitter breakdown voltage, specified voltage between base and emitter

V_{[BR]CEX} —Collector-emitter breakdown voltage, specified circuit between base and emitter

 $\mathbf{V}_{(BR)EBO}$ – -Emitter-base breakdown voltage, collector open

 $\mathbf{V}_{(\mathsf{BR})\mathsf{ECO}}$ —Emitter-collector breakdown voltage, base

 $\mathbf{V}_{(\mathsf{BR})\mathsf{E}_1\mathsf{E}_2}$ —Emitter-emitter breakdown voltage

 $\mathbf{V}_{(\mathsf{BR})\mathsf{GSS}}$ —Gate-source breakdown voltage

 $\mathbf{V}_{|\mathsf{BR}|\mathsf{GSSF}}\mathbf{-}\mathsf{Forward}$ gate-source breakdown voltage

 $\mathbf{V}_{(\mathsf{BR})\mathsf{GSSR}}$ —Reverse gate-source breakdown voltage

V_{B2B1} —Interbase voltage

 $\mathbf{V}_{ extsf{CB}}$ —Average or dc voltage, collector to base

-Instantaneous value of alternating component of collector-base voltage

 $\mathbf{V}_{ ext{CB(ff)}}$ —Collector-base dc open-circuit voltage (floating potential)

VCBO -Collector-base voltage, dc, emitter open

V_{CC} -Collector supply voltage (dc)

 $\mathbf{V}_{ extsf{CE}}$ —Average or dc voltage, collector to emitter

-Instantaneous value of alternating component of collector-emitter voltage

V_{CE(ff)}—Collector-emitter dc open-circuit voltage (floating potential)

 $\mathbf{V}_{ ext{CEO}}$ —Collector-emitter voltage (dc), base open

V_{CE(ofs)} -Collector-emitter offset voltage

V_{CER} -Collector-emitter voltage (dc), resistance between base and emitter

 \mathbf{V}_{CES} —Collector-emitter voltage (dc), base shorted to emitter

 $\mathbf{V}_{ ext{CE(sat)}}$ —Collector-emitter dc saturation voltage

 $\mathbf{V}_{ ext{CEV}}$ —Collector-emitter voltage (dc), specified voltage between base and emitter

 $\mathbf{V}_{ ext{CEX}}$ —Collector-emitter voltage (dc), specified circuit between base and emitter

V_{DD} —Drain supply voltage (dc)

VDG -Drain-gate voltage

V_{DS} —Drain-source voltage

 $\mathbf{V}_{ extsf{DS(on)}}$ —Drain-source on-state voltage

V_{DU} -Drain-substrate voltage

VEB —Average or dc voltage, emitter to base

 \mathbf{v}_{eb} —Instantaneous value of alternating component of emitter-base voltage

 $\mathbf{V}_{\mathrm{EB(fl)}}$ —Emitter-base dc open-circuit voltage (floating potential)

 $\mathbf{V}_{\mathsf{EBO}}$ —Emitter-base voltage (dc), collector open

V_{EB1(sat)}—Emitter saturation voltage

V_{EC} —Average or dc voltage, emitter to collector

-Instantaneous value of alternating component of emitter-collector voltage

 $\mathbf{V}_{ ext{EC(fl)}}$ —Emitter-collector dc open-circuit voltage (floating potential)

 $\mathbf{V}_{\mathrm{EC}(\mathrm{ofs})}$ -- Emitter-collector offset voltage

 $egin{array}{lll} \mathbf{V}_{\text{EE}} & -\text{Emitter supply voltage (dc)} \\ \mathbf{V}_{\text{F}} & -\text{For voltage-regulator and voltage-reference di-} \end{array}$ odes: dc forward voltage. For signal diodes and rectifier diodes: dc forward voltage (no alternating component)

-Alternating component of forward voltage (rms

Instantaneous total forward voltage

 $\mathbf{V}_{\mathsf{F}(\mathsf{AV})}$ —Forward voltage, dc (with alternating component)

V_{FM} —Maximum (peak) total forward voltage

V_{F(RMS)} - Total rms forward voltage V_{GG} —Gate supply voltage (dc)

VGS -Gate-source voltage

V_{GSF} -Forward gate-source voltage

V_{GS[off]} —Gate-source cutoff voltage

V_{GSR} -Reverse gate-source voltage

VGS[th] -Gate-source threshold voltage

V_{GU} -Gate-substrate voltage

 \mathbf{V}_1 -Inflection-point voltage

VOB1 -Base-1 peak voltage

 \mathbf{V}_{P} -Peak-point voltage

VPP -Projected peak-point voltage

-For voltage-regulator and voltage-reference diiodes: dc reverse voltage. For signal diodes and rectifier diodes: dc reverse voltage (no alternating component)

-Alternating component of reverse voltage (rms

v_R —Instantaneous total reverse voltage

V_{R(AV)} —Reverse voltage, dc (with alternating component)

V_{RM} -Maximum (peak) total reverse voltage

V_{RRM} -Repetitive peak reverse voltage

V_{R(RMS)}—Total rms reverse voltage

V_{RSM} -Nonrepetitive peak reverse voltage

VRT -Reach-through voltage

V_{RWM}-Working peak reverse voltage

V_{SS} —Source supply voltage (dc)

VSU -Source-substrate voltage

V(TO) -Threshold voltage

 \mathbf{V}_{V} -Valley-point voltage

 \mathbf{V}_{Z} -Regulator voltage, reference voltage (dc)

V_{ZM} -Regulator voltage, reference voltage (dc at maximum rated current)

-Common-base small-signal short-circuit forward Vib transfer admittance

-Common-collector small-signal short-circuit for-**V**fc ward transfer admittance

-Common-emitter small-signal short-circuit forward transfer admittance

-Common-source small-signal short-circuit forward transfer admittance

y_{fs(imag)}—Common-source small-signal forward transfer susceptance

y_{fs(real)} -Common-source small-signal forward transfer conductance

-Common-base small-signal short-circuit input Vib admittance

-Common-collector small-signal short-circuit input admittance

-Common-emitter small-signal short-circuit input admittance

yie(imag) - Imaginary part of small-signal short-circuit input admittance (common-emitter)

yie(real) -Real part of small-signal short-circuit input admittance (common-emitter)

-Common-source small-signal short-circuit input admittance

y_{is(imag)} —Common-source small-signal input susceptance y is(real) - Common-source small-signal input conduc-

tance

MANUEL COLUDED

-Common-base small-signal short-circuit out**y**ob put admittance

-Common-collector small-signal short-circuit Voc output admittance

-Common-emitter small-signal short-circuit output admittance

yoe(imag) - Imaginary part of small-signal short-circuit output admittance (common-emitter)

yoe(real) - Real part of small-signal short-circuit output admittance (common-emitter)

-Common-source small-signal short-circuit output admittance

yos(imag)—Common-source small-signal output susceptance

y_{os(real)} —Common-source small-signal output conductance

-Common-base small-signal short-circuit reverse transfer admittance

-Common-collector small-signal short-circuit reverse transfer admittance

-Common-emitter small-signal short-circuit re-Vre. verse transfer admittance

-Common-source small-signal short-circuit reverse transfer admittance

y_{rs[imag]}—Common-source small-signal reverse transfer susceptance

y_{rs(real)} -Common-source small-signal reverse transfer conductance

-Intermediate-frequency impedance Zif

-Modulator-frequency load impedance \mathbf{z}_{m}

-Radio-frequency impedance

 $\mathbf{Z}_{\theta|A(t)}$ —Junction-to-ambient transient thermal impedance

 $\begin{array}{l} \mathbf{Z}_{\theta|C(t)} - \text{Junction-to-case transient thermal impedance} \\ \mathbf{Z}_{\theta(t)} - \text{Transient thermal impedance} \end{array}$

-Video impedance

-Regulator impedance, reference impedance Z, (small-signal at I2)

-Regulator impedance, reference impedance (small-signal at IZK)

 \mathbf{Z}_{7m} -Regulator impedance, reference impedance (small-signal at I_{ZM})

PREFIX AND MANUFACTURER IDENTIFICATION

PREFIX	MANUFACTURER	PREFIX	MANUFACTURER	PREFIX	MANUFACTURER
BA	Rohm	MOC	Motorola	SLP	Sanyo
CEX	Control Electronics	MPS	Motorola	SN	Texas Instrument
DAC	National Semiconductor	MRF	Motorola	TA	Toshiba
FND	Fairchild	MU	Motorola	TIL	Texas Instrument
FRL	Litronix	MV	General Instrument	TIP	Motorola
ICM	Intersil	NE	Signetics	TLO	Texas Instrument
LF	National Semiconductor	NSM	National Semiconductor	TL	Texas Instrument
LM	National Semiconductor	PCIM	PC International	TLG	Toshiba
MA	National Semiconductor	S	American Micro Systems	TLR	Toshiba
MC	Motorola	SAD	Reticon	VN	Siliconix
MJ	Motorola	SE	Signetics	XC	Xciton
MM	National Semiconductor.	SEL	Sanken		
	Motorola or Teledyne	SCS	Spectronics		

GENERIC PART NUMBER PREFIX CODE

AD AH AM CD	Analog To Digital Analog Hybrid Analog Monolithic	DA DM LF	Digital To Analog Digital Monolithic Linear FET	LM MM TBA	Linear Monolithic MOS Monolithic Linear Monolithic
CD	CMOS Digital	LH	Linear Hybrid		

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DRIVER (Bidfet)	
FSK DEMODULATOR/TONE DECODER	
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MONOLITHIC FUNCTION GEN	
OPERATIONAL AMP (LinCMOS)	
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