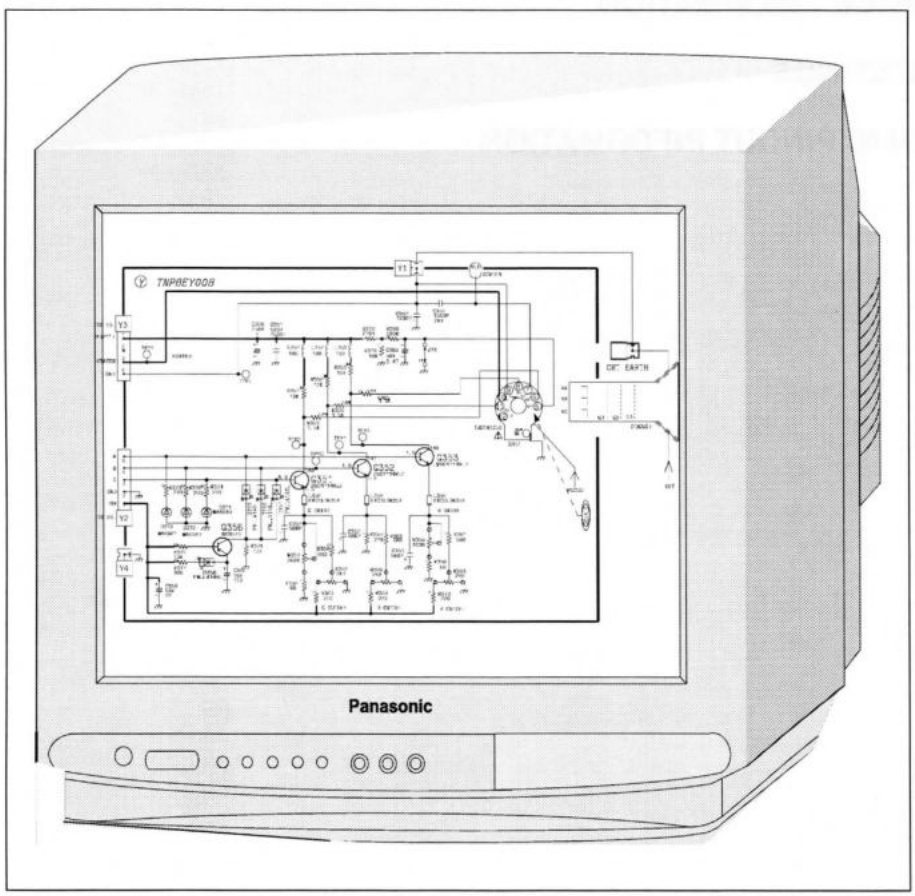
Technical Guide

Colour Television

Z5 Chassis

Circuit Explanation



Panasonic

Panasonic

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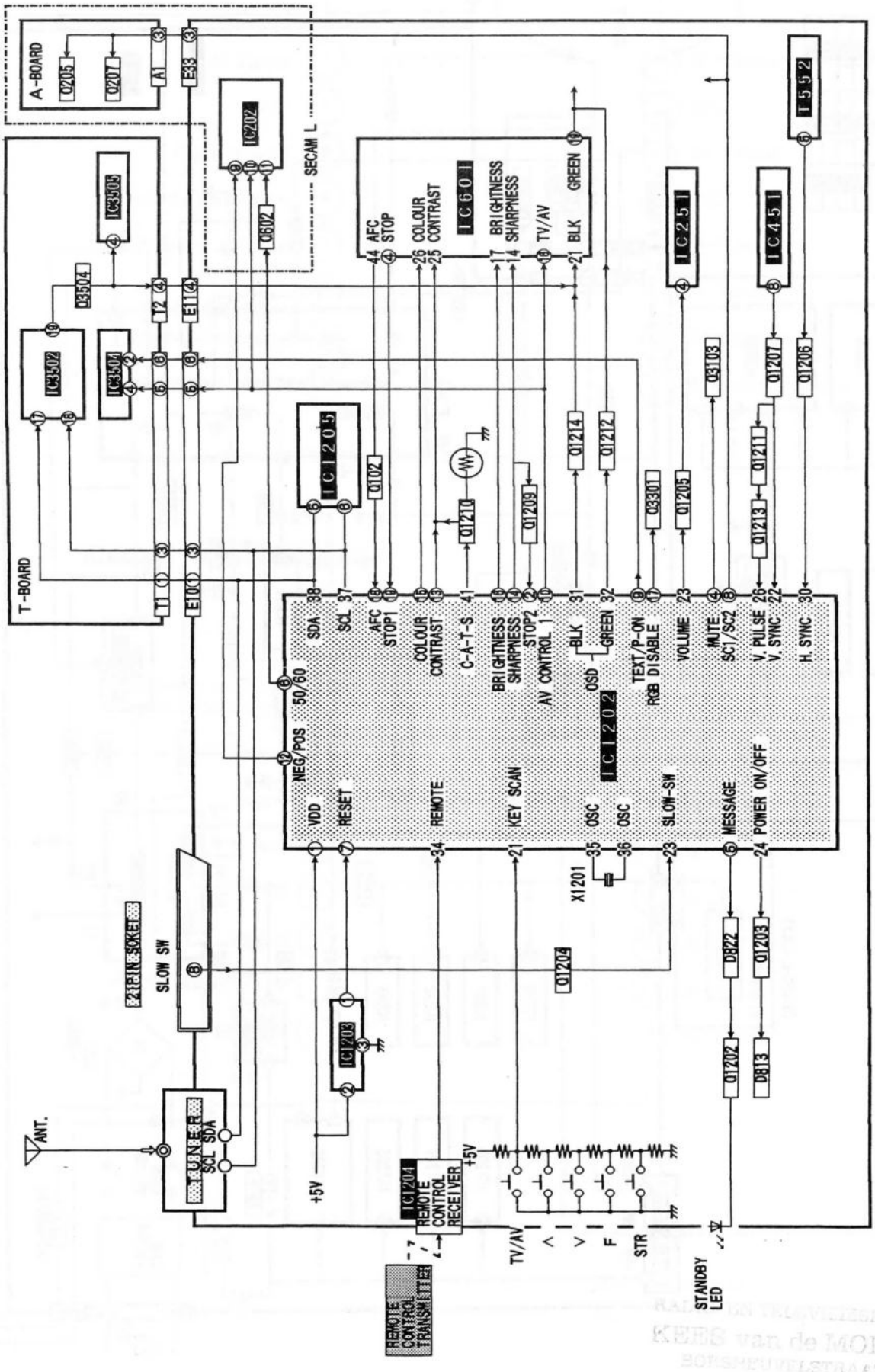

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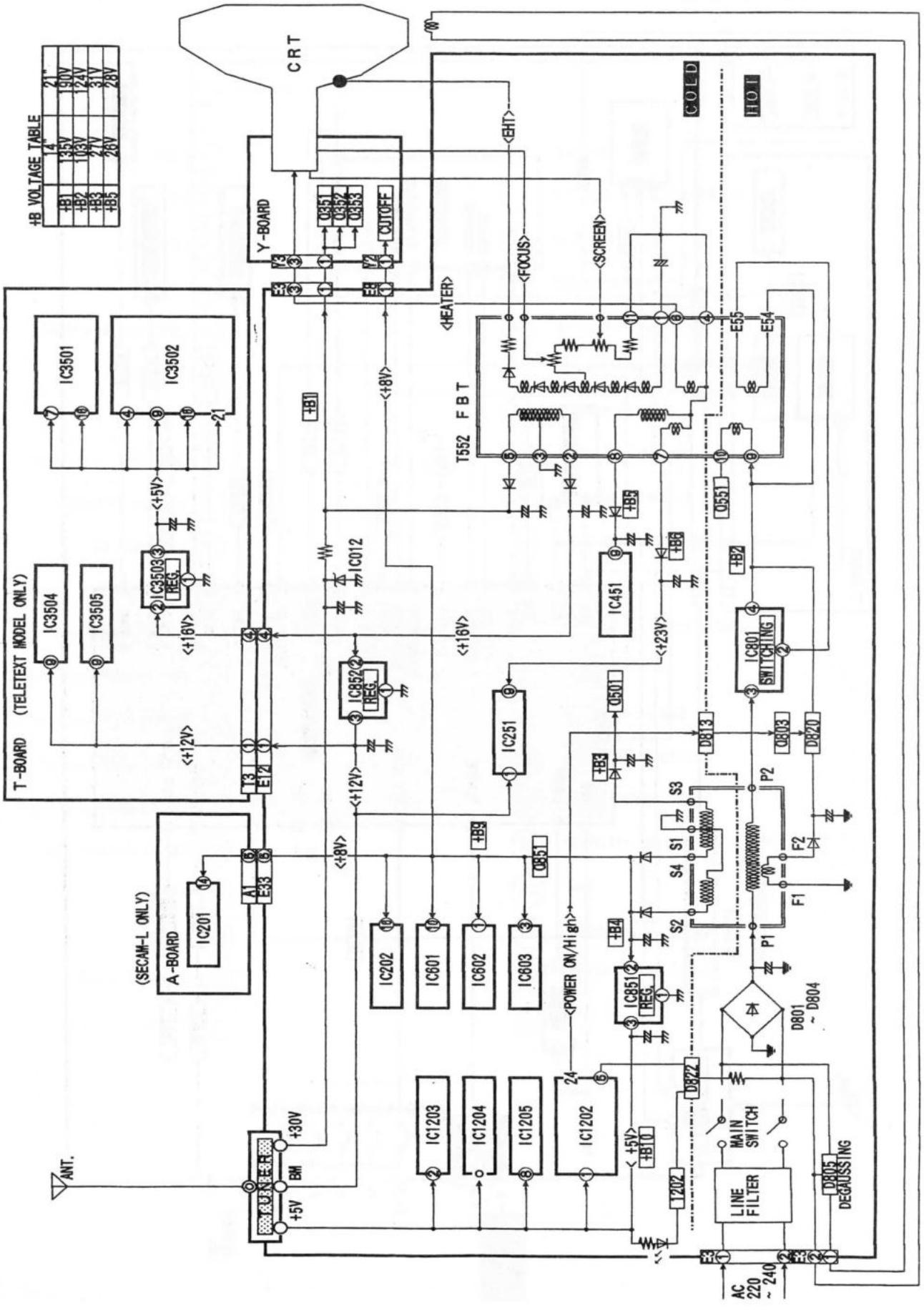

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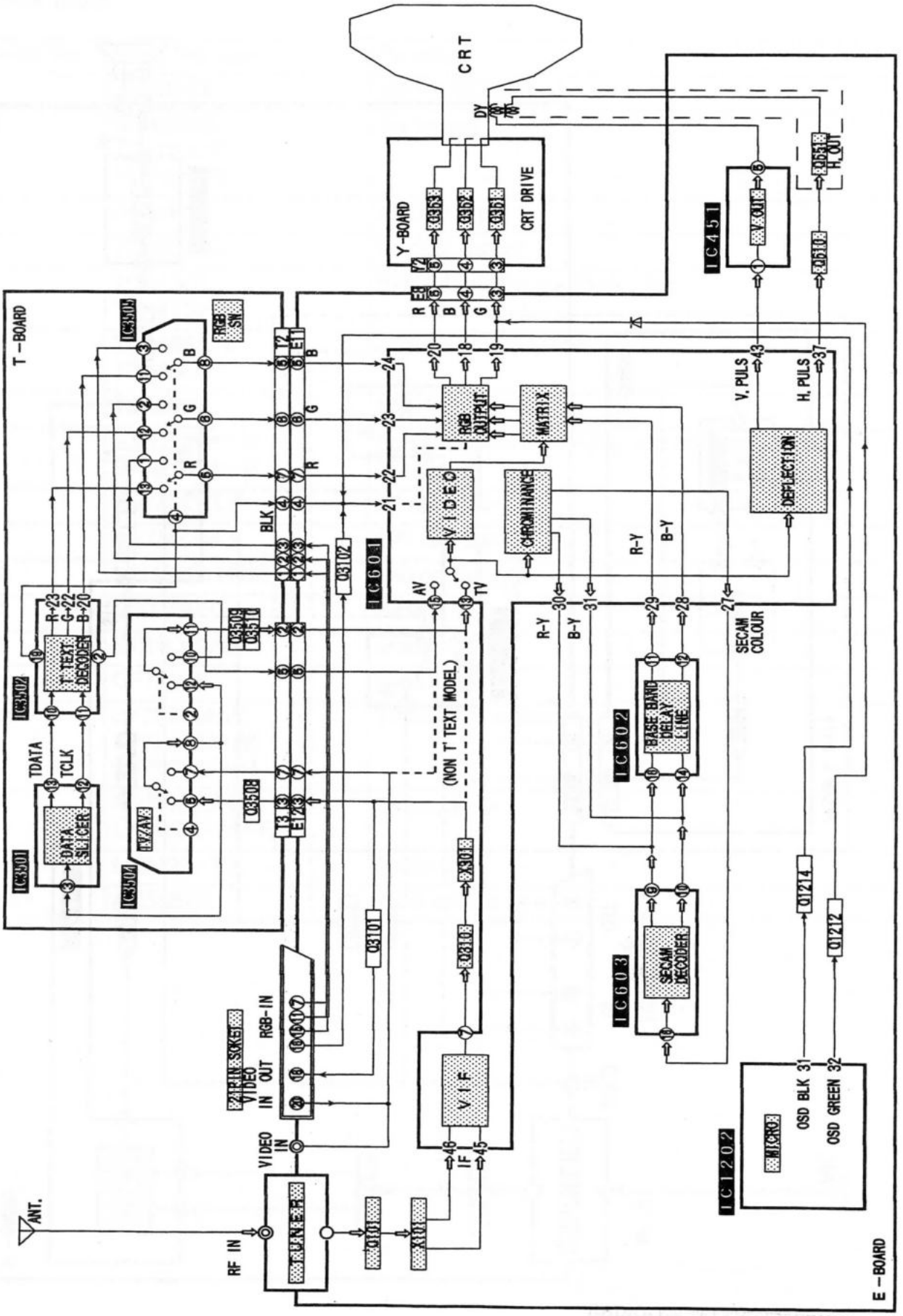

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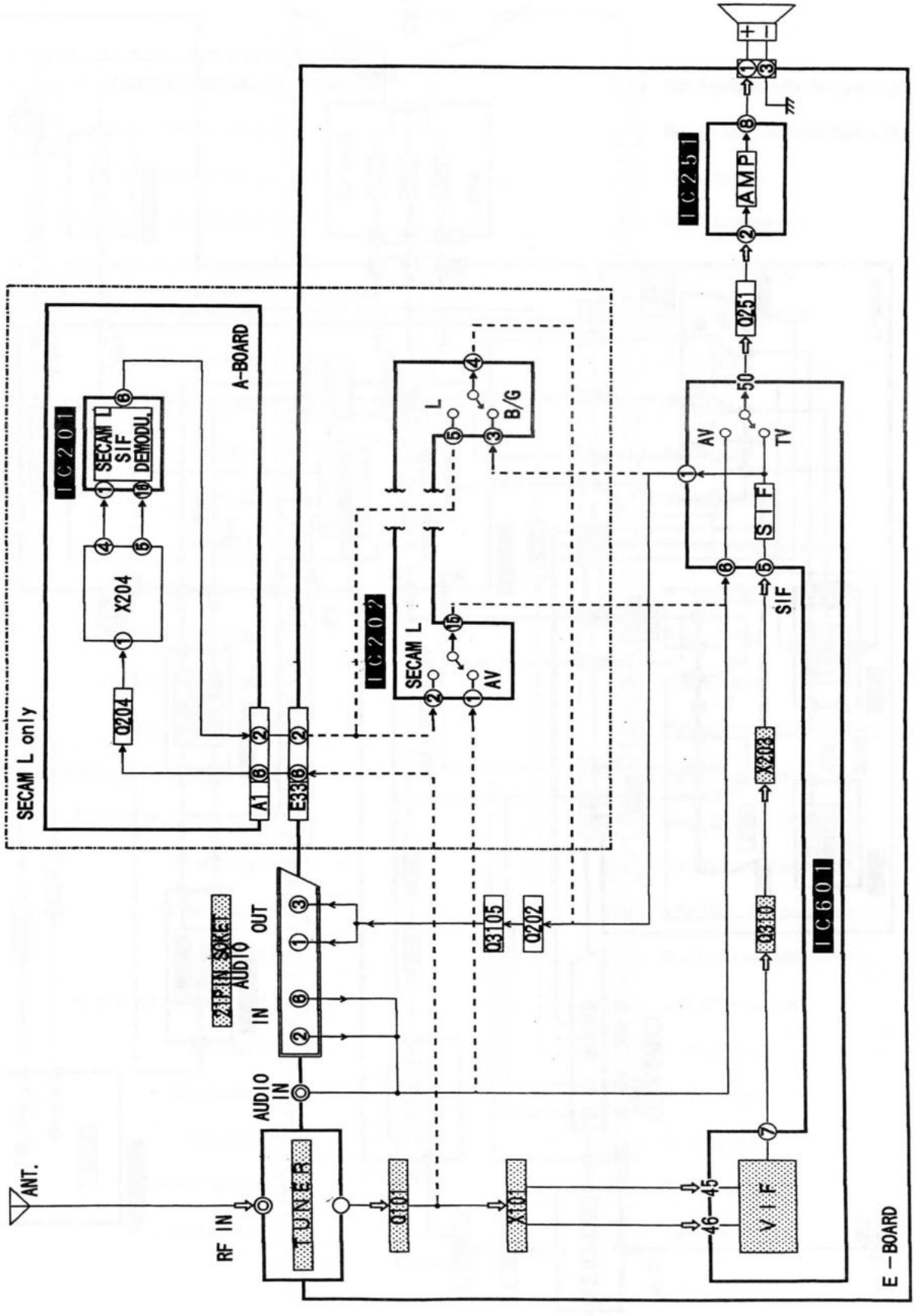
SECAM L only
A-BOARD
IC201
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X204
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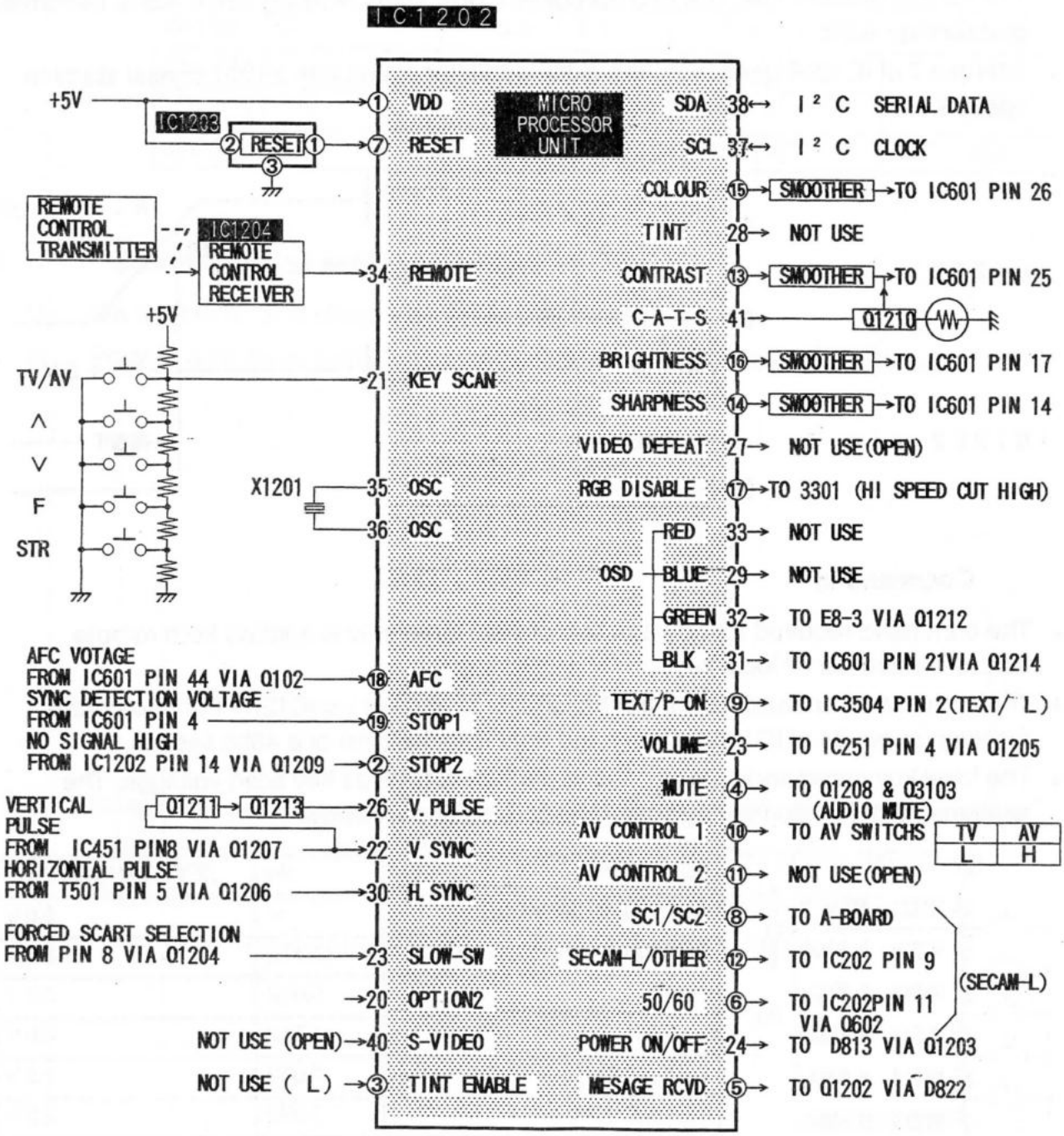
1. MICROPROCESSOR PROCESSOR AND CONTROL

OUTLINE

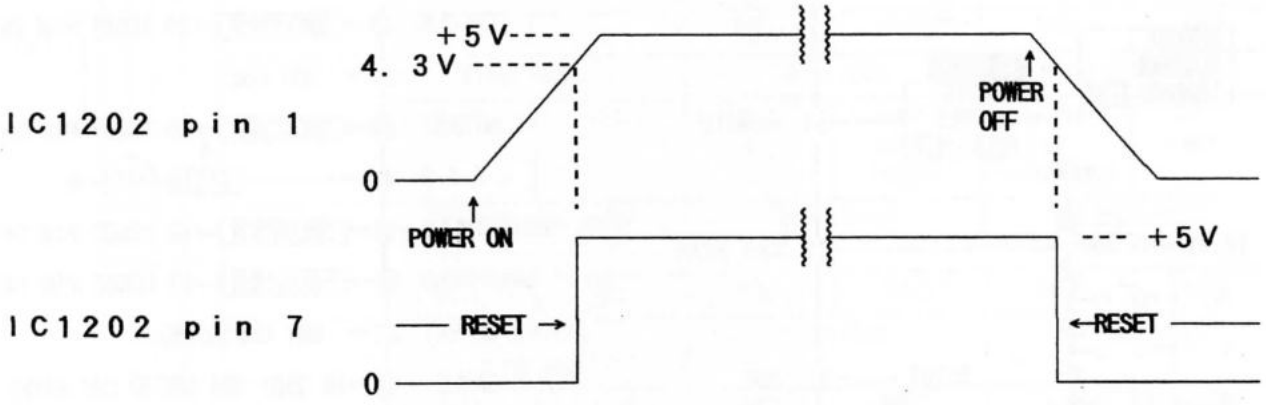
The microprocessor processor unit IC1202 is a 8K x 8bit device which provides all the control and on−screen display functions for the TV receiver. Memory storage is provided by IC1205.

Microprocessor unit



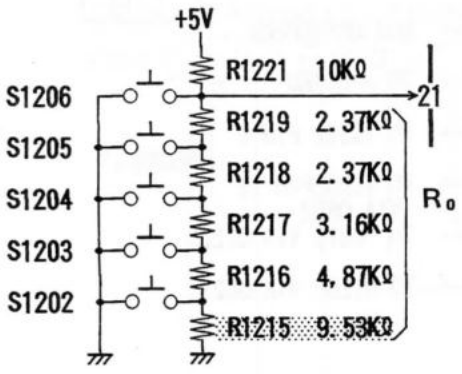
1. Reset

- During the power ON/OFF operation, or during a momentary fall in the +B line voltage, sufficient voltage may not be supplied to the microprocessor (IC1202) and there is a possibility that the microprocessor operation may be incorrect.
- Accordingly, in order to prevent this incorrect operation, the reset circuit activates, keeping the microprocessor in a reset condition, until the voltage level feeding the reset IC (IC1203) returns to normal.
- When the power switch is turned on, the +B10 is less than 4.3V and the voltage at pin 1 of IC1203 remains low. The microprocessor only starts working when +B10 becomes greater than 4.3V.
- After pin 7 of IC1202 goes high, the clock oscillator circuit with X1201 crystal starts to operate.



2. Command in

- The command required for any function of the TV receiver is applied from remote control transmitter or local keys.
- The command from remote control transmitter is applied via IC1204 (remote control receiver) to pin 34 of IC1202. Command data is in the form of a 48bit system.
- The local key commands are applied to pin 7 of IC1202 as key scan voltages. The relationship of function to key scan voltage is as shown below.



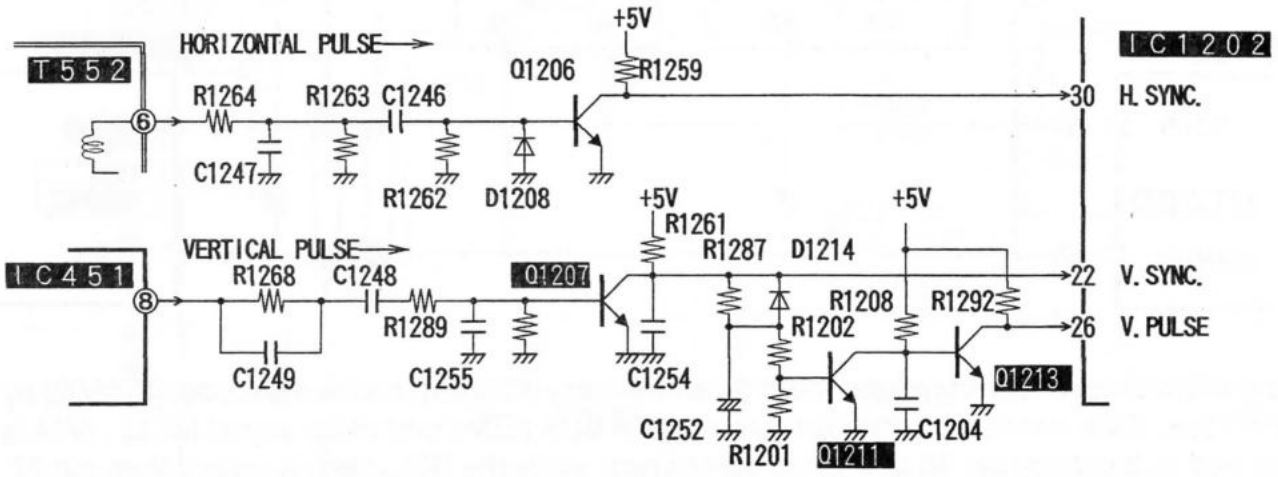
FUNCTION	Ro	KEY SCAN VOLTAGE
NORMAL (TEXT MODEL)	∞	5.0 V
NORMAL (NON-TEXT MODEL	22.30Ω	3.4 V
TV/AV	0.00Ω	0.0 V
Λ (UP)	4.74Ω	0.9 V
V (DOWN)	0.00Ω	1.6 V
F (FUNCTION)	7.90Ω	2.2 V
STR (STORE)	12.77Ω	2.8 V

* R1215 is used for text models only.

3. Input information

To control all operations in the TV set, the microprocessor receives information concerning the condition of TV set. This information is as follows.

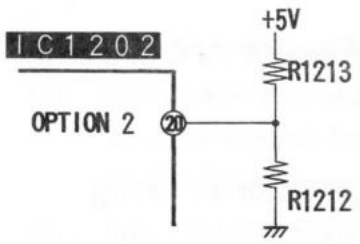
- AFC voltage
  This is an analogue DC voltage which is applied to pin 18 from the VIF AFC circuit, to control AFC operation.
- Stop 1 (Sync. detection voltage)
  High (+5V) or Low (0V) is applied to pin 19 from the VIF sync detector for tuning control.
- Stop 2 (Sync. detection voltage)
  High (+5V) or Low (0V) is applied to pin 2 from the sharpness control via Q1209 and provides a control for sleep timer operation.



- Horizontal sync.
  A Horizontal pulse is applied to pin 30 and is used for synchronization of microprocessor clock and horizontal sync. signal.
- Vertical sync.
  A vertical pulse is applied to pin 22 and is used for synchronization of microprocessor clock and vertical sync. signal.
- Vertical pulse
  A Vertical pulse is applied to pin 26 to be used for 50Hz/60Hz detection.
- Tint enable
  If pin 3 is set to high, then tint control for NTSC is possible. However Z–5 chassis can receive PAL/SECAM signals only so this pin should always be in a low condition.
- S–Video
  If pin 40 is set to high, the microprocessor can control a S–video input signal. However Z–5 chassis is not ready for S–video signal so this pin should always be in a low condition.
- Slow–SW
  If the voltage at pin 39 goes low and the AV–control line 1 goes high. Then the 21 pin input signal is displayed automatically.

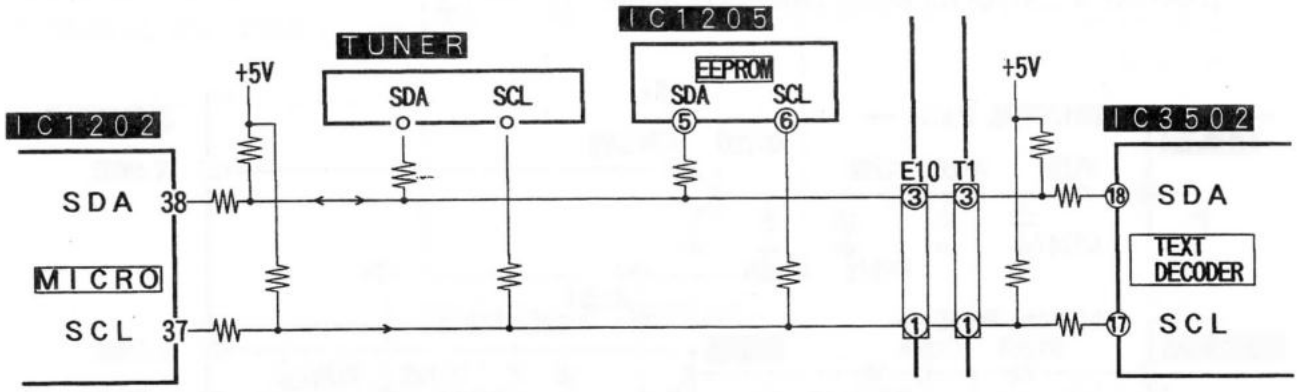
- Option 2

Model version is set by voltage at pin 20.



VERSION	C & CP	FRENCH	UK
VOLTAGE	0.85V	2.7V	5.0V
R1213	33KΩ	6.8KΩ	47KΩ
R1212	39KΩ	33KΩ	OPEN

4. I²C bus



The microprocessor communicates with tuner, memory (IC1205), and text decoder (IC3502) by the I²C bus. Data on this bus line consists of serial data (SDA) and clock signal (SCL) . SDA is input and output from pin 38 of the microprocessor, while the SCL clock is output from pin 37.

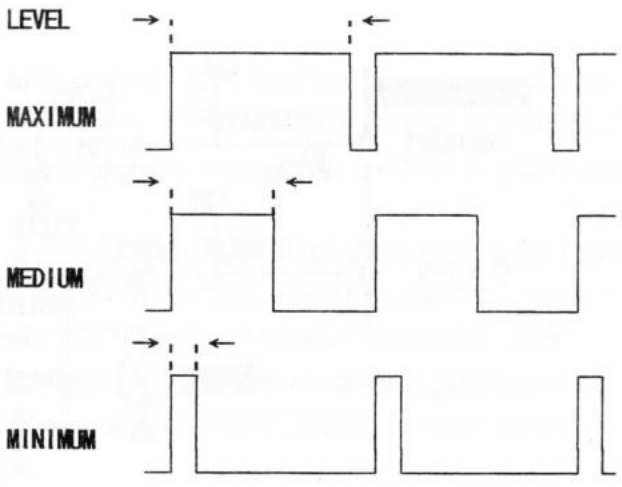
5. Memory (EEPROM)

The memory IC is interfaced with the microprocessor by the I²C bus. The following data are memorised by the memory IC.

- Tuning data for 50 programme positions
  - Channel number
  - Offset data
  - SIF data SC1/SC2
  - Colour system (SECAM L or PAL B/G/I)
- Last memory information
  - Power on/off condition
  - Programme position
  - Volume level
  - Colour level
  - Contrast level
  - Brightness level
  - Sharpness level
  - C–A–T–S mode

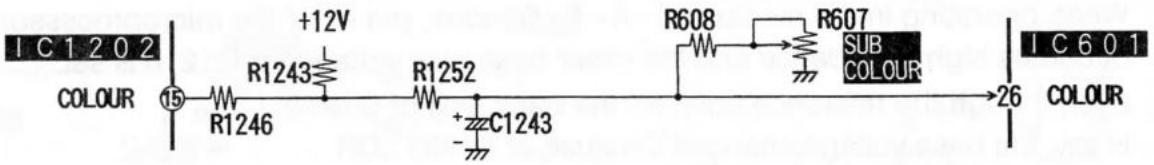
6. PWM control

PWM (Pulse width modulation) pulse
The microprocessor can output only digital signals, however most of manual controls for the TV are carried out by analogue DC voltages.
To achieve this, the microprocessor outputs PWM pulses and these pulses are converted to DC voltages by smoothing circuits.
Z−5 chassis uses PWM pulses for colour, contrast, brightness, sharpness and volume control and these are generated as 6 bit/64 steps PWM pulse trains.



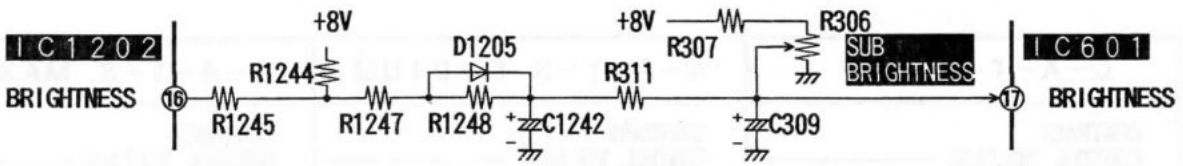
PWM (Pulse width modulation)

- Colour



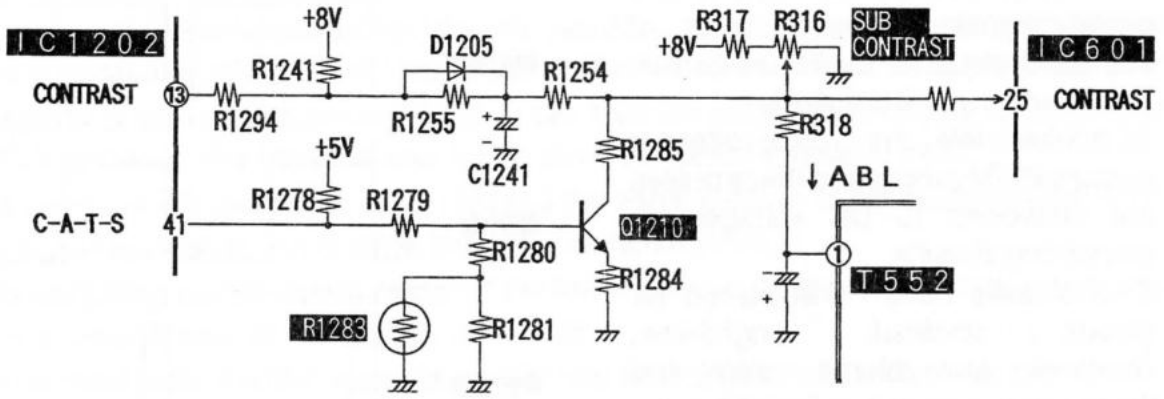
Colour control PWM is output from pin 15 and smoothed by C1243 and provides control voltage in the range of 0 to 12V DC which is supplied to pin 26 of IC601.
When a video signal is applied into the circuitry, the level of control from the colour PWM is 4.5Vp−p (peak to peak) however if a video signal is not present this level decreases to 4.0Vp−p to reduce colour noise on the screen.

- Brightness



Brightness control PWM (4.5Vp−p) is output from pin 16 and smoothed by C1242. This provides a control voltage in the range of 0 to 8V DC which is supplied to pin 17 of IC601.

- Contrast
  Contrast control PWM (2.0Vp−p) is output from pin 13 and smoothed by C1241. This provides a DC control voltage which is supplied to pin 25 of IC601.
  However contrast control DC voltage is controlled by C−A−T−S (Contrast Automatic Tracking System)) and ABL (Automatic Beam Limiter) .



C–A–T–S

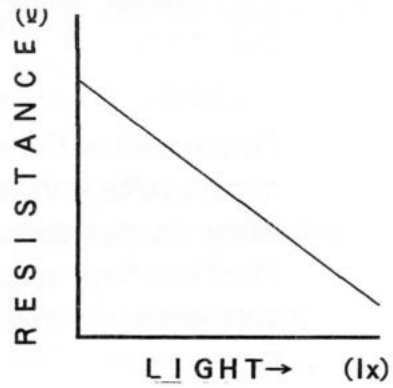
When C–A–T–S is off, pin 41 of the microprocessor goes low (ground) and Q1210 becomes cut off because the base bias voltage is no longer supplied.

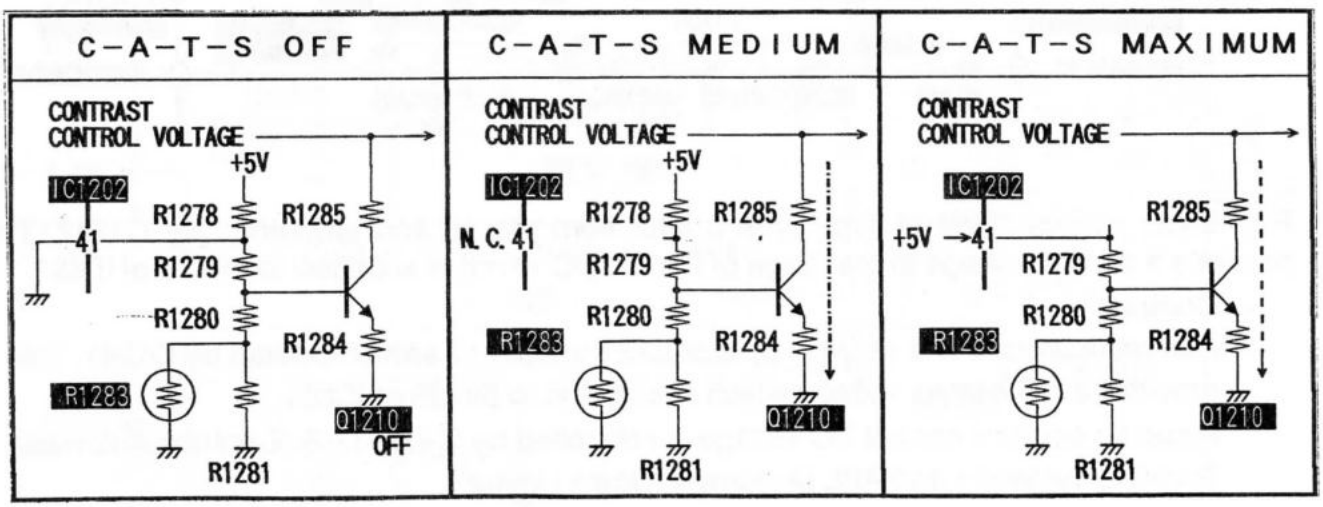
When maximum C–A–T–S mode is selected, +5V is output from pin 41 of the microprocessor and the highest reference base bias voltage for Q1210 is set.

When operating in the medium C–A–T–S mode, pin 41 of the microprocessor becomes high impedance and the lower base bias voltage for Q1210 is set.

Even though the reference point for the base bias of Q1210 is set, the base voltage changes because of R1283 LDR (Light Dependent Resistor) due to its resistance being changed by incidental light. This allows the conduction of Q1210 collector – emitter to be controlled by the condition of the external light surrounding the TV..

The result of this is to ensure that the contrast control voltage is controlled.

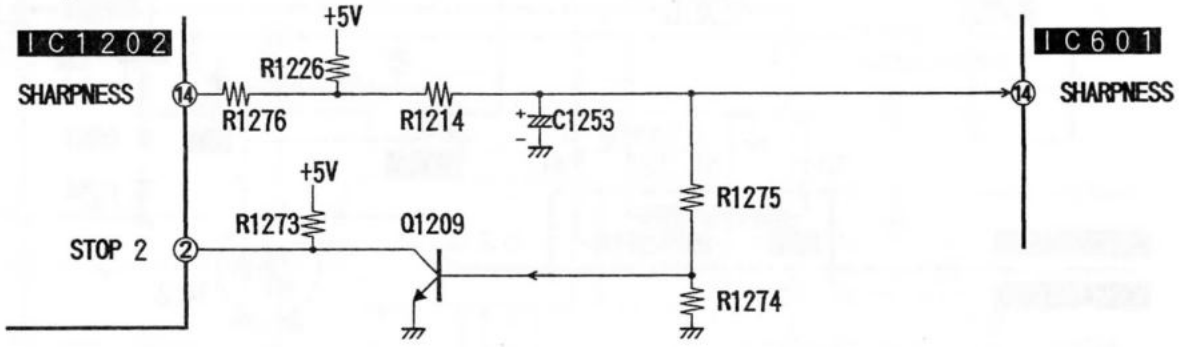




- ABL

  If CRT beam current is increased then pin 1 of T552 falls. When the voltage at pin 1 of T552 goes negative, some of the contrast control current flows to pin 1 via R318. When maximum beam current is reached. the ABL operating point is set by R318.

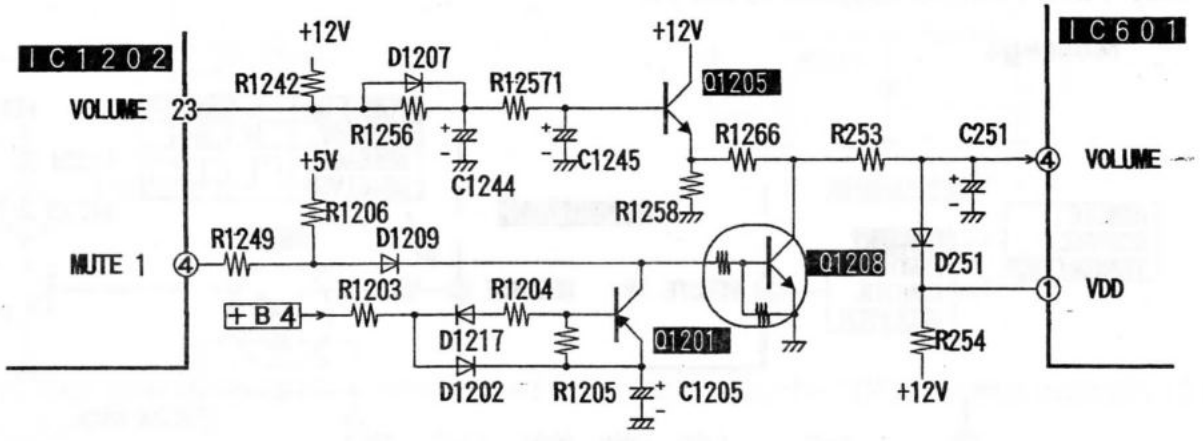
- Sharpness



Sharpness control PWM (4.5Vp−p) is output from pin 16 and smoothed by C1242. This provides a 0 to 4V DC control voltage which is supplied to pin 14 of IC601. However to reduce visible snow noise during no video signal condition, the sharpness PWM level is reduced to 3Vp−p.

Q1209 detects sharpness level changes and is passed to pin 2 of IC1202 as stop 2 information.

- Volume

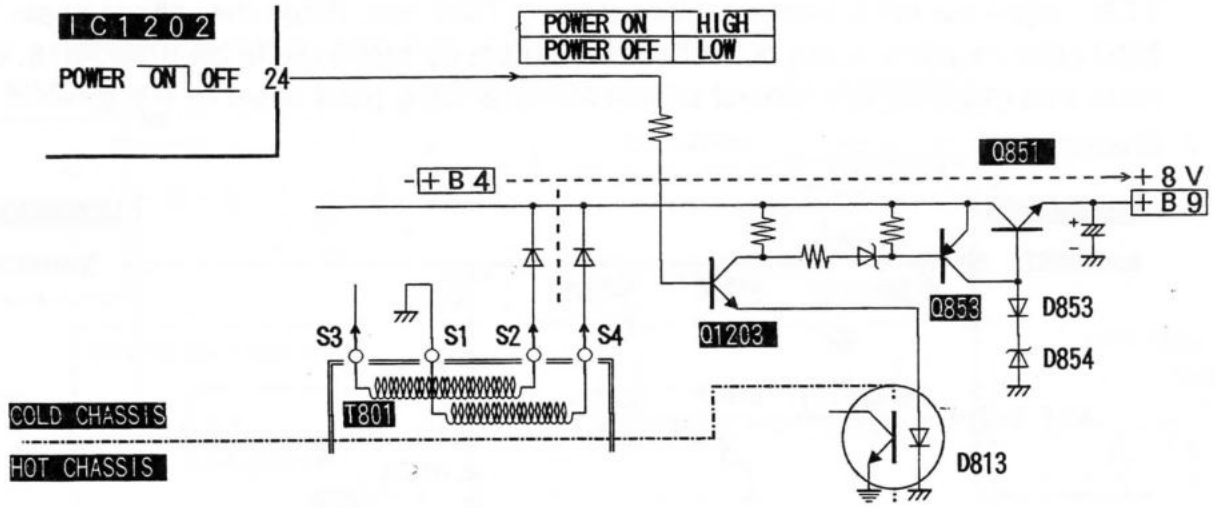


Volume control PWM (12Vp−p) is output from pin 23 and smoothed by C1244 and C1245. This DC control voltage is supplied to pin 4 of IC601 via Q1205 (Buffer) .

The mute function is carried out by Q1208 which is controlled by the mute 1 signal from pin 4 of IC1202.

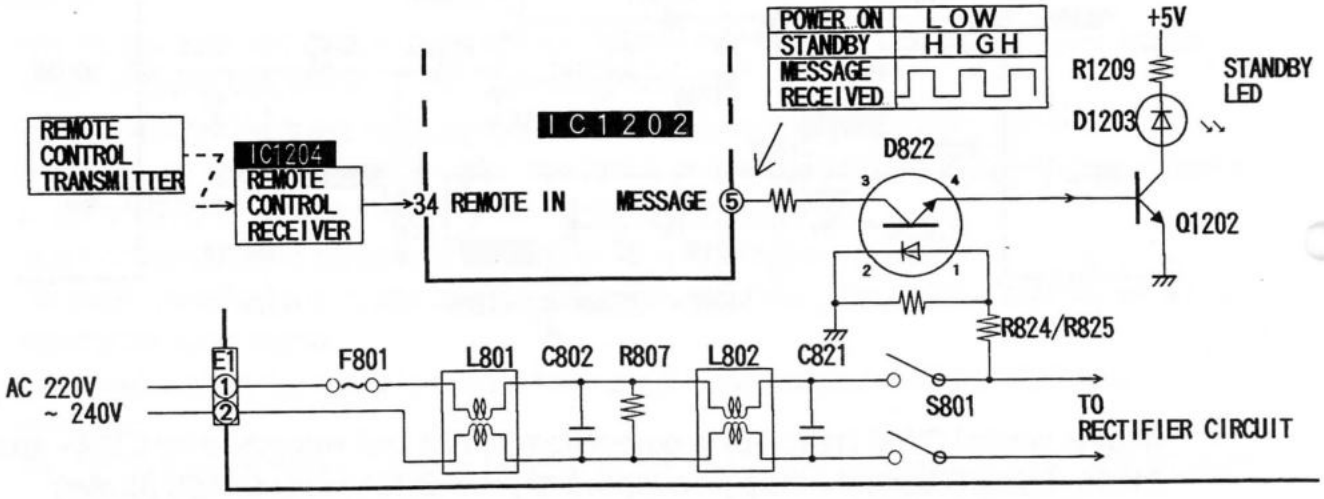
Volume control voltage is also removed to eliminate any 'pop' noise during power on, off or channel change operation.

7. Power on/off control



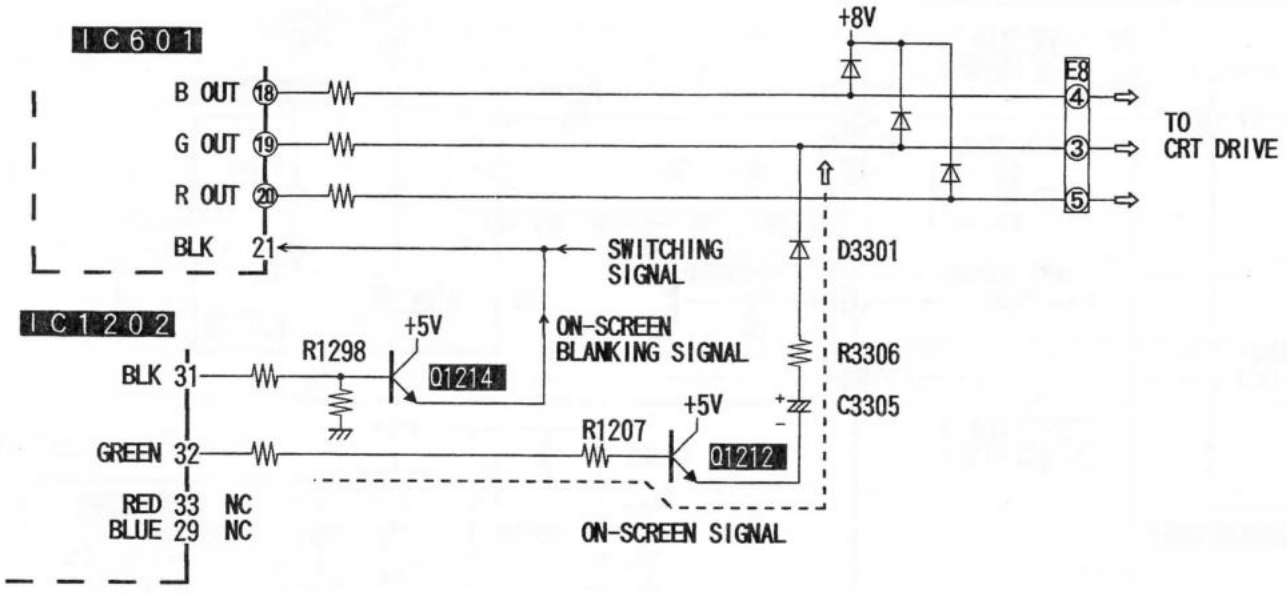
- Pin 24 of IC1202 is the power on/off control terminal.
- When power on is selected, pin 24 becomes high (+5V).
  Q1203 and the photo−transistor D813 turns on. This allows the power circuit to operate as a switching regulator and all supply voltages are generated. In addition to this, when Q853 and Q851 turn on then +B9 (+8V) is supplied to the TV circuitry.
- When standby mode is selected by the remote control, pin 24 goes low (0V) and Q1203 and photo−transistor of D813 are turned off.
  The power circuit operates as amplifier and only the +B4 voltage is generated. So that only +B10 (+5V) is supplied to the TV.

8. Message

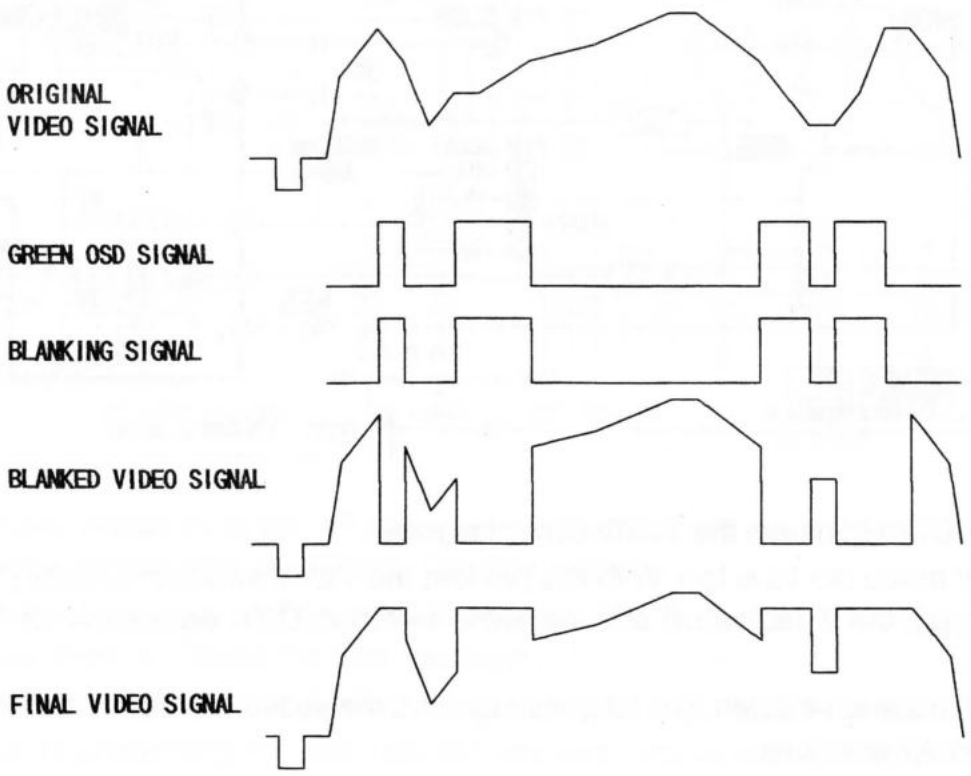


- During standby mode the standby LED is lit. This is because when pin 5 of IC1202 goes high then Q1202 turns on.
- When any button of the remote control transmitter is pressed, the standby LED flashes. because the pulse output from pin 5 of the microprocessor causes Q1202 to turn on and off rapidly.
- When S801 is off, the standby LED does not turn off immediately because the microprocessor still operates for a short time. To prevent this, D822 is used to cut off the base control signal of Q1202.

9. On–Screen Display (OSD)

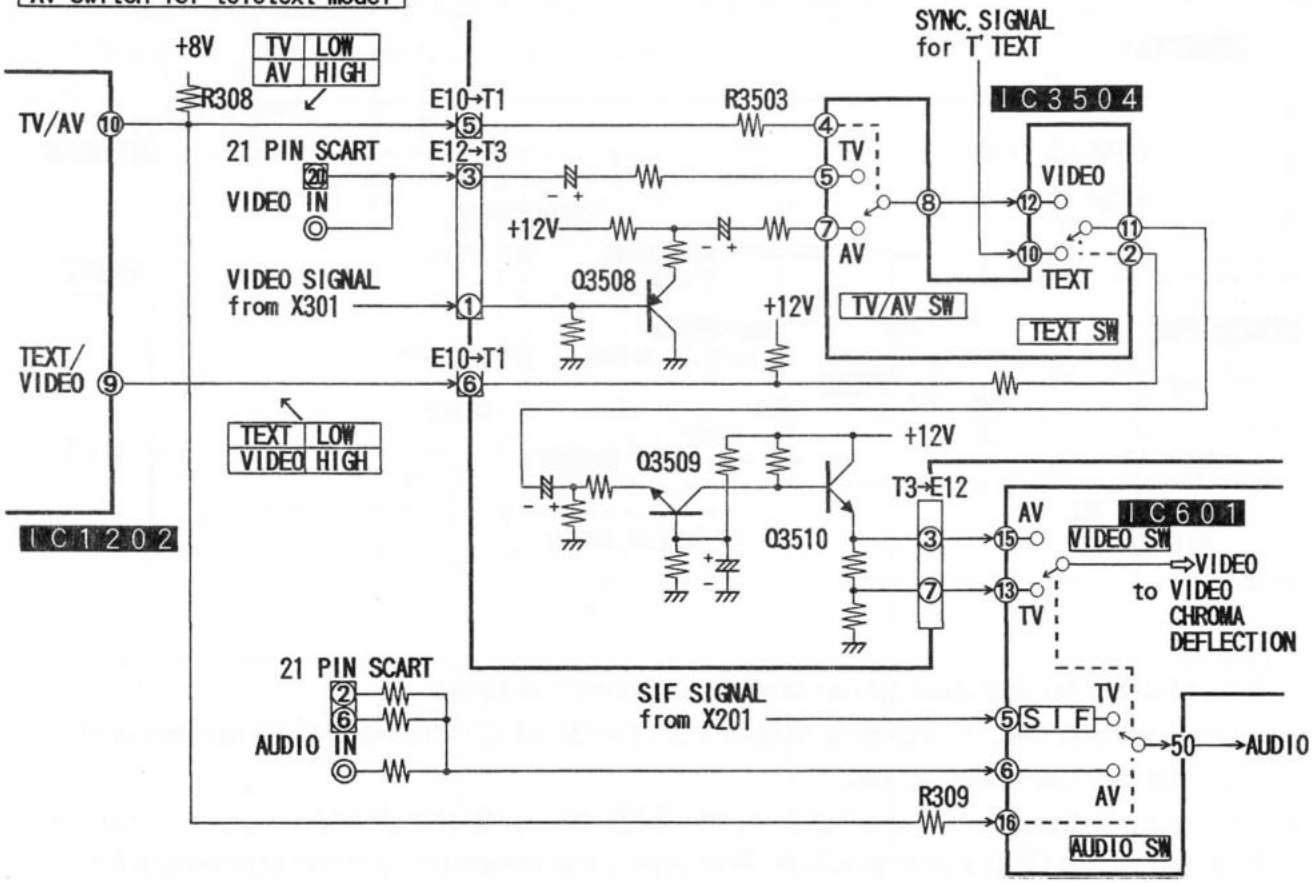


- This chassis design uses green only for on screen display.
- The on screen display signal is output from pin 32 of IC1202 via Q1212 (buffer) and inserted into the green signal.
- To ensure a clear area is available for the OSD, the R, G and B video picture signals are blanked at the OSD insert position. This give clear green on–screen characters for viewing.

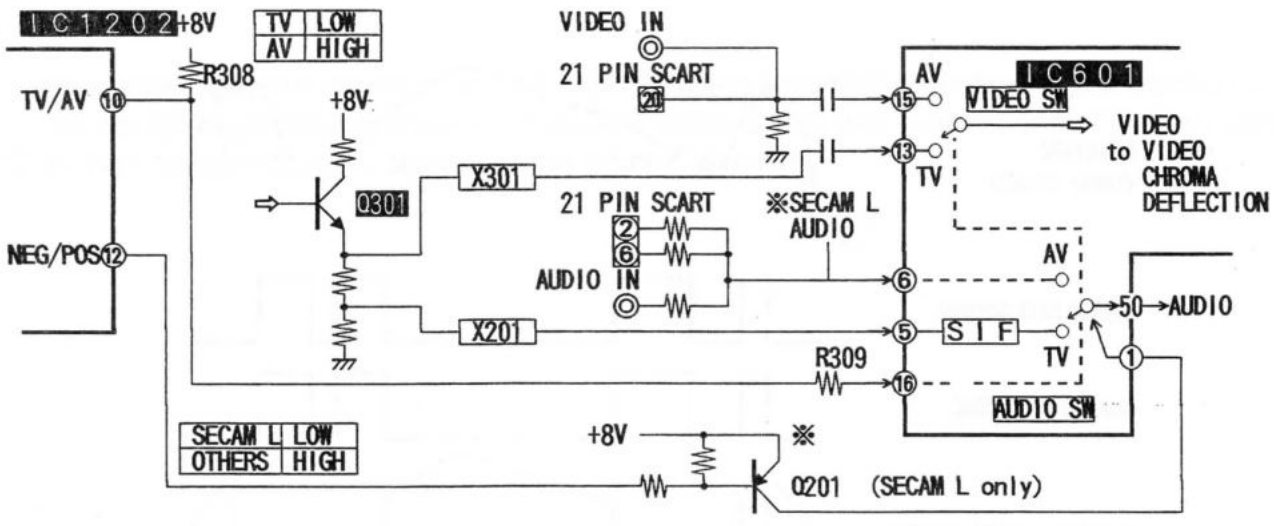


10. AV switch

AV switch for teletext model



AV switch for non-teletext model



- Pin 10 of IC1202 outputs the TV/AV control signal.
- During TV mode pin 10 is low. With this pin low, the TV/AV switch in IC3504 (Teletext models only), the Video switch and the Audio switch in IC601 are set to their TV positions.
- When AV mode is selected, pin 10 goes high and the above mentioned switches are set to their AV positions.

* When a SECAM L signal is received Q201 switches on and +8V is supplied to pin 1 of IC601. This forces the audio switch to lock to AV position.

AV switch connection

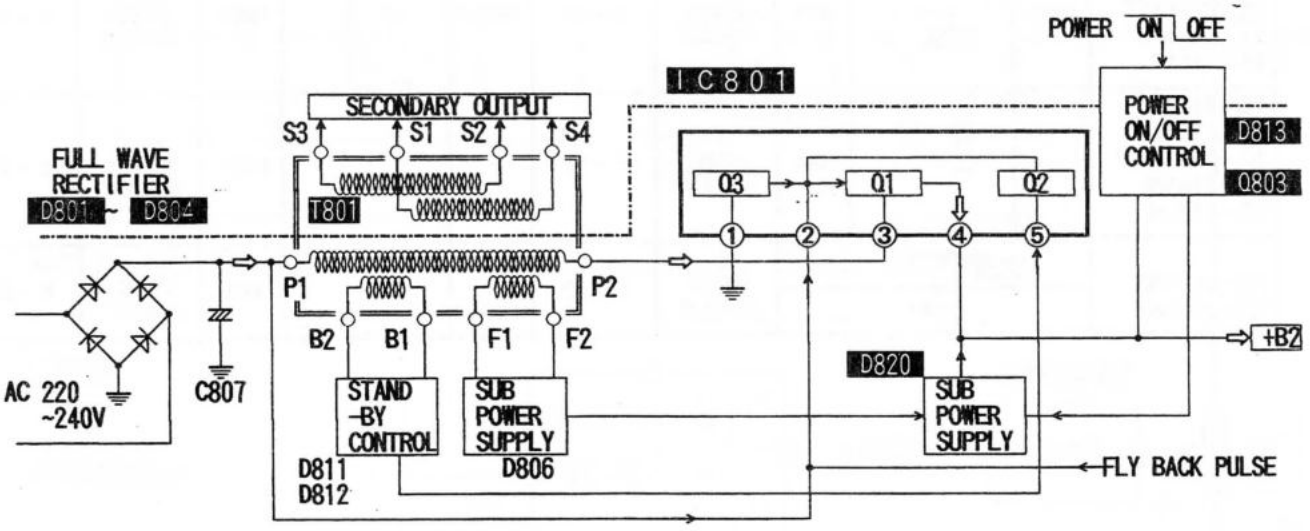
MODE SWITCH / MODEL	TV MODE					AV MODE				
	IC3504		IC601			IC3504		IC601		
	PIN 4	CONNECTION	PIN 16	CONNECTION		PIN 4	CONNECTION	PIN 16	CONNECTION	
				VIDEO	AUDIO				VIDEO	AUDIO
TX–21S1T TX–21S1TC TX–21S1TCP TX–21S1TL TX–14S1T	LOW	5–8	LOW	13 – VIDEO CIRCUIT	5 – 50	HIGH	7 – 8	HIGH	15 – VIDEO CIRCUIT	6 – 50
TC–21S1R TC–21S1RC TC–21S1RCP TC–21S1RL TC–14S1R	–	–	LOW	13 – VIDEO CIRCUIT	5 – 50	–	–	HIGH	15 – VIDEO CIRCUIT	6 – 50
TC–21S1RF TC–14S1RF	IC601 PIN 1 HIGH			13 – VIDEO CIRCUIT	6 – 50	–	–	HIGH	15 – VIDEO CIRCUIT	6 – 50

2. POWER SUPPLY CIRCUIT

1. Outline

Low power consumption (Use of small size power transformer) circuit. Both main power and remote power are provided by one circuit.

2. Construction



- The power supply circuit consist of :–

A) Full wave rectifier (D801, D802, D803, D804 and C807)

B) Switching transformer (T801)

C) Control IC (IC801)

D) Power ON/OFF control circuit (D813 and Q803)

E) Standby control circuit (D811, D812, C813, D817 and Q807)

F) Sub power supply circuit (D820, D806 and C818)

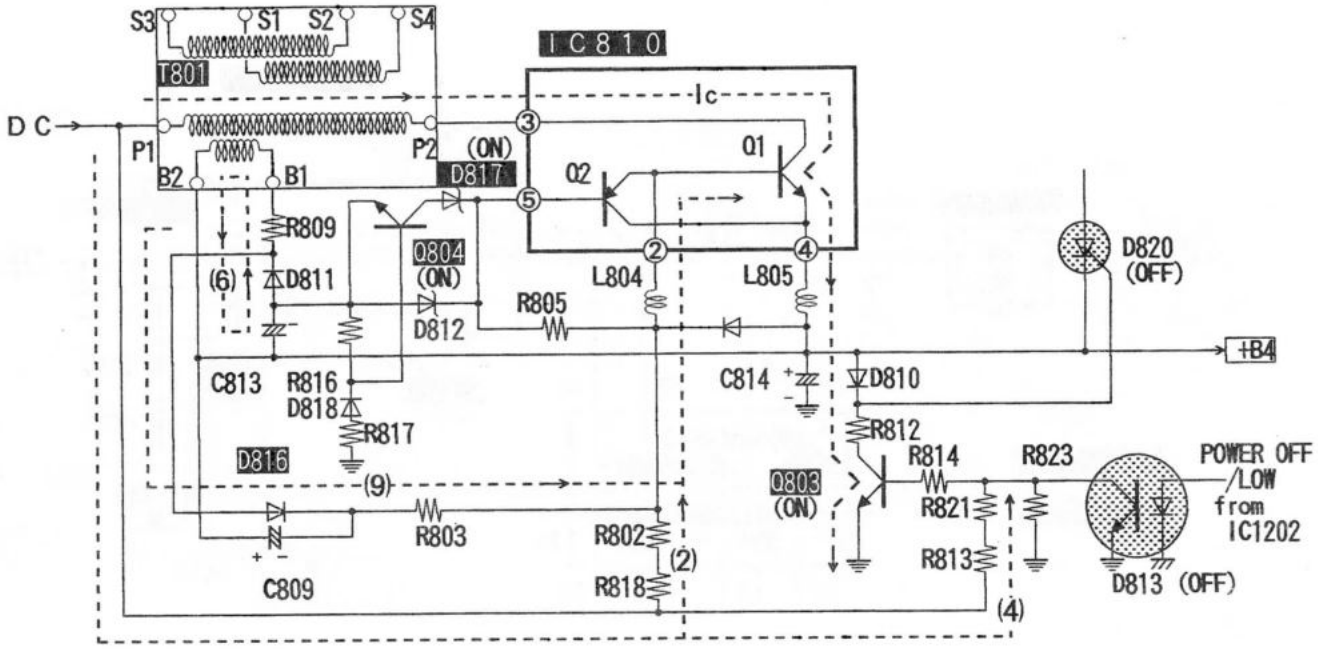
3. Operation

Standby

(1) AC voltage is passed to the bridge rectifier D801, D802,D803 and D804 where it is full wave rectified and smoothed by C807.

(2) The DC voltage produced by this (approx.300V) is passed to pin 3 of IC801 through the primary windings of T801 (P1 ~ P2) .

(3) The startup supply current is fed via R818, R802, L804 to pin 2 of IC801,the internal circuit of the I.C. shows that this will cause Q1 to switch on and collector current (Ic) will flow.



(4) DC voltage is also applied to base of Q803 via R813 and R821 and causes Q803 to switch on. This is because during standby mode the power ON/OFF voltage from the microprocessor (IC1202) is low and photo−transistor in D813 is off.

(5) With Q803 turned on Ic flows to ground via D810 and R812 so that voltage at pin 4 of IC801 (+B4) becomes approx.+1V. (Q1 operates as an A class amplifier and the level of Ic is very small.)

(6) The rising Ic through the primary windings P1−P2 of T801 will induce a feedback voltage via windings B1−B2. This negative feedback voltage charges C813 via D811 and R809. However, because the positive pin of C813 is connected to the +B2 line (approx.1 volt) the voltage of the negative pin falls to approx. −2V.

(7) Following this Q804 turns on and the voltage between the anode and cathode of D817 becomes 3V causing D817 to turn on (Anode : −2V, Cathode +1V).

(8) D817 and Q2 inside IC801 control the base current of Q2 to prevent Q2 having full drive applied. Therefore the the voltage at pin 4 of IC801 is kept to a constant level of approx. 2V.

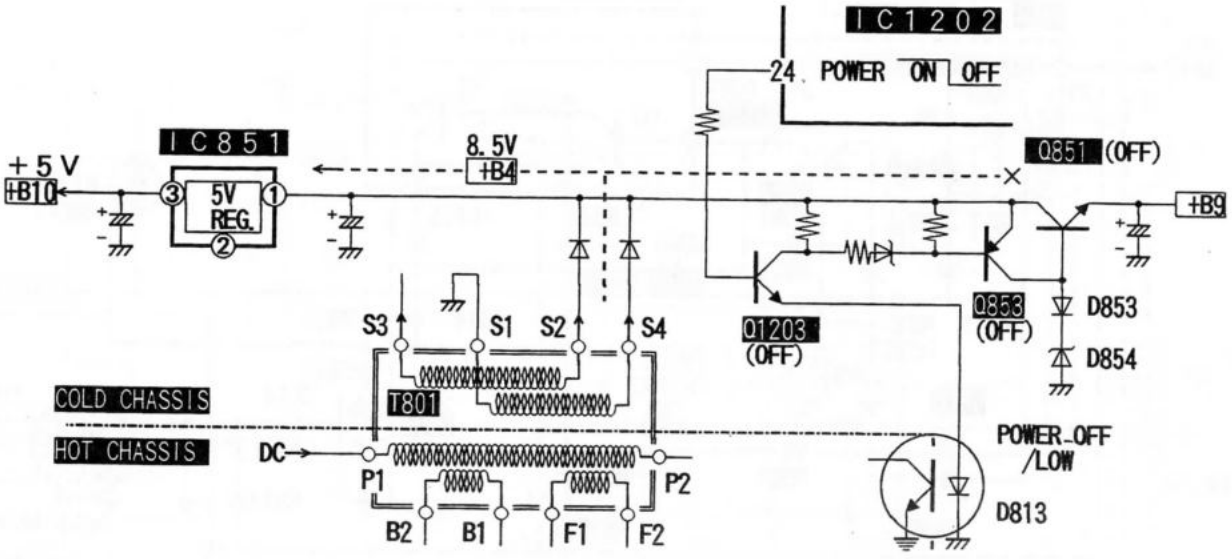
(9) In addition to this, the voltage induced at winding B1−B2 of T801 is also applied to the base of Q1 as a trigger via D816, R803, L804 and pin 2 of IC801.

(10) Q1 amplifies this trigger voltage and outputs from its collector a phase inverted signal. Because of this amplification, the Ic changes and so the induced voltage at the secondary windings will also change. This change is fed to the base of Q1.

(11) Therefore this circuits operate as a oscillator.

−Note−

Q2 in IC801 does not operate during standby mode.

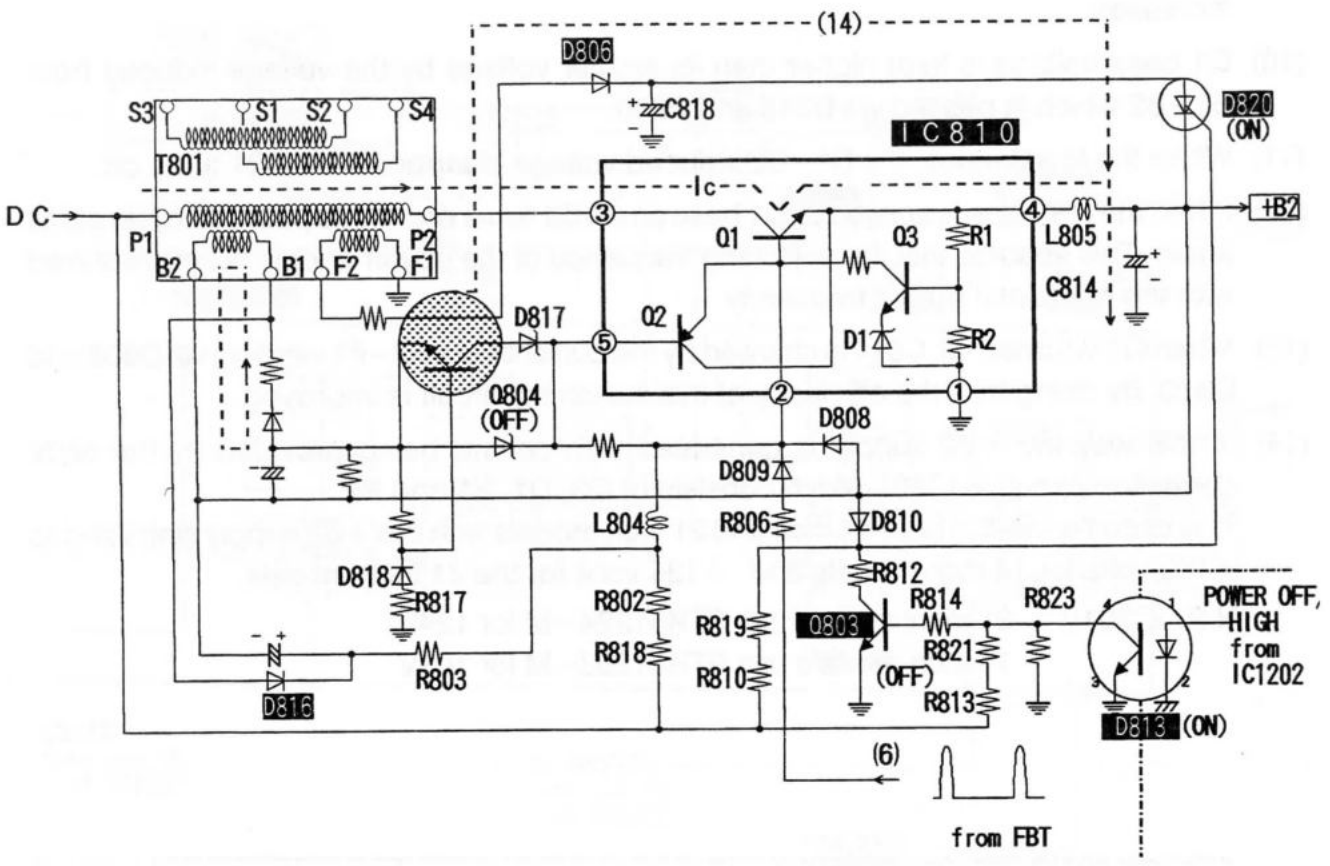


(12) The induced voltages at S2, S4−S1 of T801 are rectified by D851 and D856 and the +B4 supply (approx. 8.5V) is created.

(13) +B4 is passed to IC851 and this creates the +B10 (5V) line which is used to supply the microprocessor (IC1202) and its peripheral circuitry.

(14))However, with the power ON/OFF output from pin 24 of IC1202 low, then Q1203, Q853 and Q851 are turned off. and the +B9 supply line is not available.

4. Power On



(1) When power is on, pin 24 of IC1202 goes high. This high is applied to pin 1 of D813 via buffer transistor Q1203.

(2) With Q1203 on then pin 4 of D813 (the opto isolator) goes low, and Q803 is turned off.

(3) The voltage at the gate of D820 becomes high (because Q803 is cut off) and D820 turns on.

(4) With Q803 turned off the voltage supplied from R810 and R819 passes via R811 and charges C814 and the +B2 voltage increases.

(5) C818 is charged during standby mode to approximately 90 volts and this is supplied to +B2 line via D820.
At the same time, the+B9 (+8V) also appears because Q851 is turned on by the power on high from pin 24 of the microprocessor which is applied to the base of Q851 via Q1203 and Q853..

(6) With these supply lines available, IC601 and the horizontal output circuits operate. With the horizontal output stage operating, a horizontal pulse (H−pulse) is fed from pin E54 of fly back transformer (FBT) via R806 and D809 to pin 2 of IC801.

(7) This pulse causes Q804 to turn off because the +B2 line rises to a voltage higher than the voltage potential of C813, and the voltage at the negative pin of C813 becomes positive. Because of this positive voltage, the emitter voltage of Q804 becomes higher than base voltage and Q2 in IC801 is also turned off.

(8) However Q1 base voltage is kept below 0.6V of its emitter voltage by D808. This means Q1 turns off.

(9) When the H−pulse from the FBT enters the base of Q1 then Q1 turns on fully and Ic increases.

(10) Q1 base voltage is kept higher than its emitter voltage by the voltage induced from B1−B2 which is passed via D816 and R803.

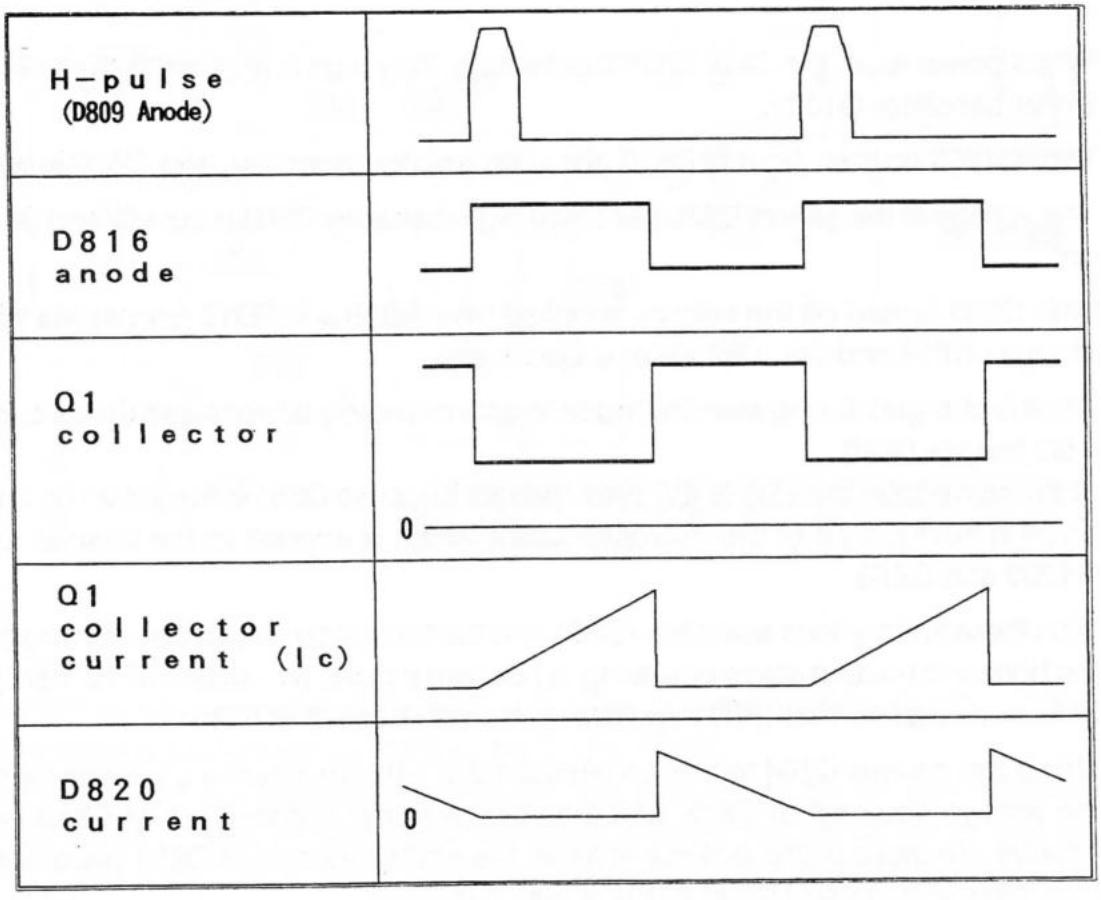
(11) When the Ic saturates, the B1−B2 induced voltage disappears and Q1 turns off.

(12) When the H−pulse is applied to Q1 base again Q1 turns on. At this point the cycle starts again. This ensures that the switching frequency of the power supply is synchronized with the horizontal output frequency.

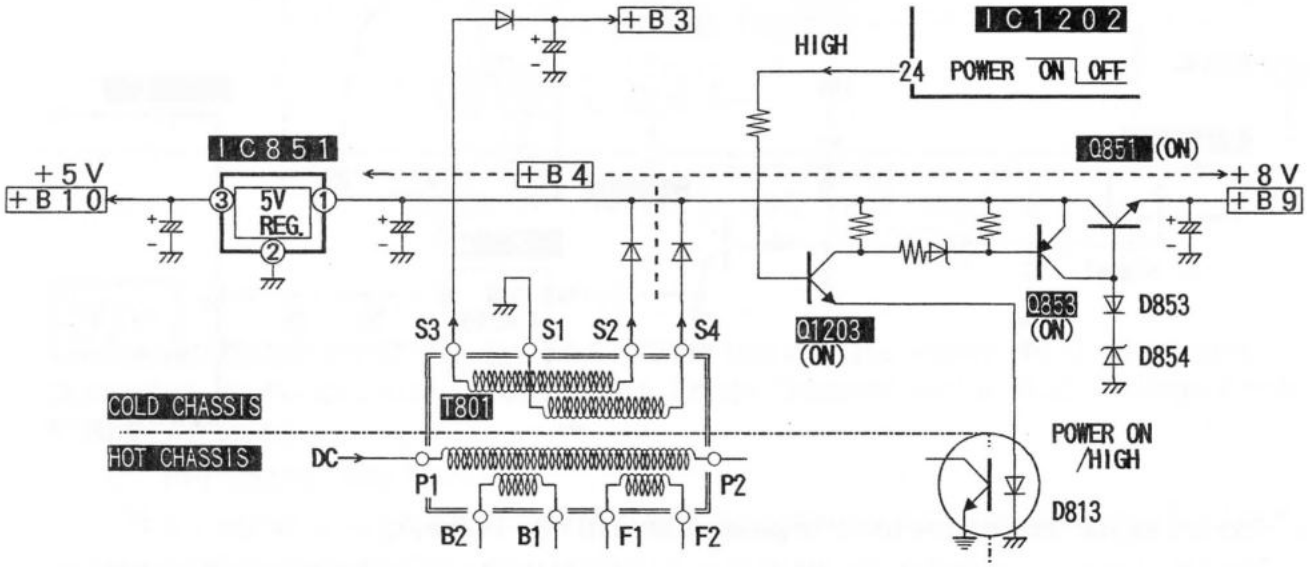
(13) When Q1 is turned off, C814 is charged by the current from F2−F1 winding via D806 and D820. By doing this, the efficiency of this switching circuit is improved.

(14) In this way the +B2 supply is generated with control being provided by the error correction circuit in IC801 which consists of Q3, D1, R1 and R2.
This circuit is used in both 14 inch and 21 inch models with the +B2 supply stabilized to +103 volts for 14 inch models and +124 volts for the 21 inch models.

N.B. IC801 : 21 inch models use STR51224−M for 124V
14 inch models use STR51203−M for 103V



Supply lines



By the switching of IC801, induced voltage is output from T801 secondary windings. These voltages are rectified and supplied to the load circuits. Other supply lines are made available by the flyback pulses generated at secondary winding of the FBT which are rectified.

The following table shows each supply line with an indication of their respective voltages and the main components which provide them.

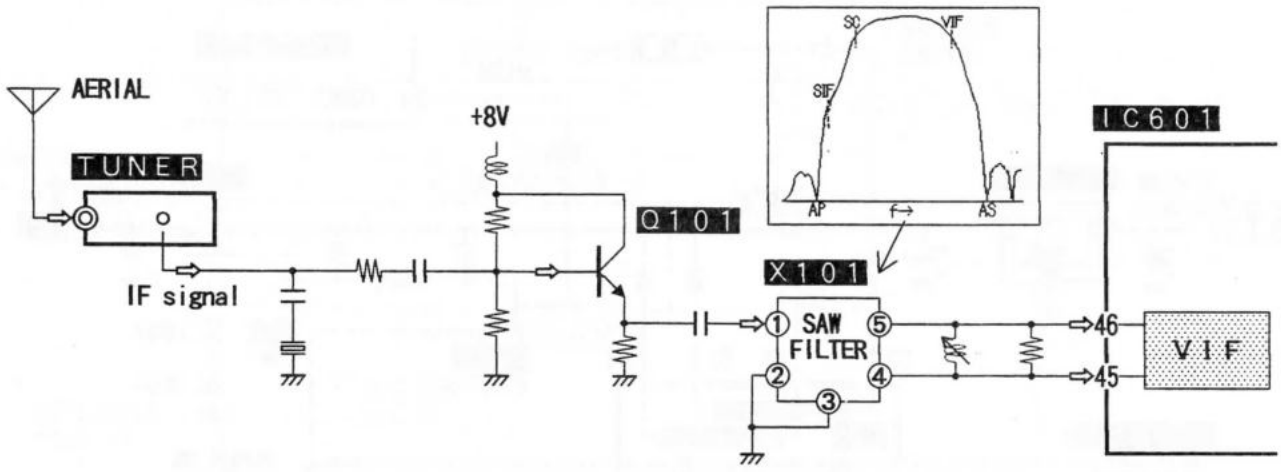
TABLE 1

NAME	OUTPUT PIN	RECTIFIER	SMOOTHER	21"		14"		REMARK
				POWER ON	STANDBY	POWER ON	STANDBY	
+B1	FBT 5	D561	C562	135V	0	190V	0	CRT DRIVE
+B2	T801 P1	IC801 4	C814	103V	1V	124V	1V	HORIZONTAL OUT
+B3	T801 S3	D852	C856	27V	0	31V	0	HORIZONTAL DRIVE
+B4	T801 S2,S4	D851,D856	C852	11V	8V	11V	8V	+B9 & +B10
+B5	FBT 8	D565	C568	27V	0	28V	0V	VERTICAL OUT
+B6	FBT 7	D564	C569	23V	0	23V	0	AUDIO OUT
+B7	FBT 2	D562	C564	16V	0	16V	0	+B8 & IC3503
+B8	+B7	IC852	C859	12V	0	12V	0	MAIN 12V
+B9	+B4	Q851	C857	8V	0	8V	0	MAIN 8V
+B10	+B4	IC851	C854	5V	5V	5V	5V	MAIN 5V
+BT	+B9	IC012	C022	30V	0	30V	0	TUNING VOLTAGE
T'TEXT	+B7	IC3503	C3521	5V	0	5V	0	TELETEXT 5V

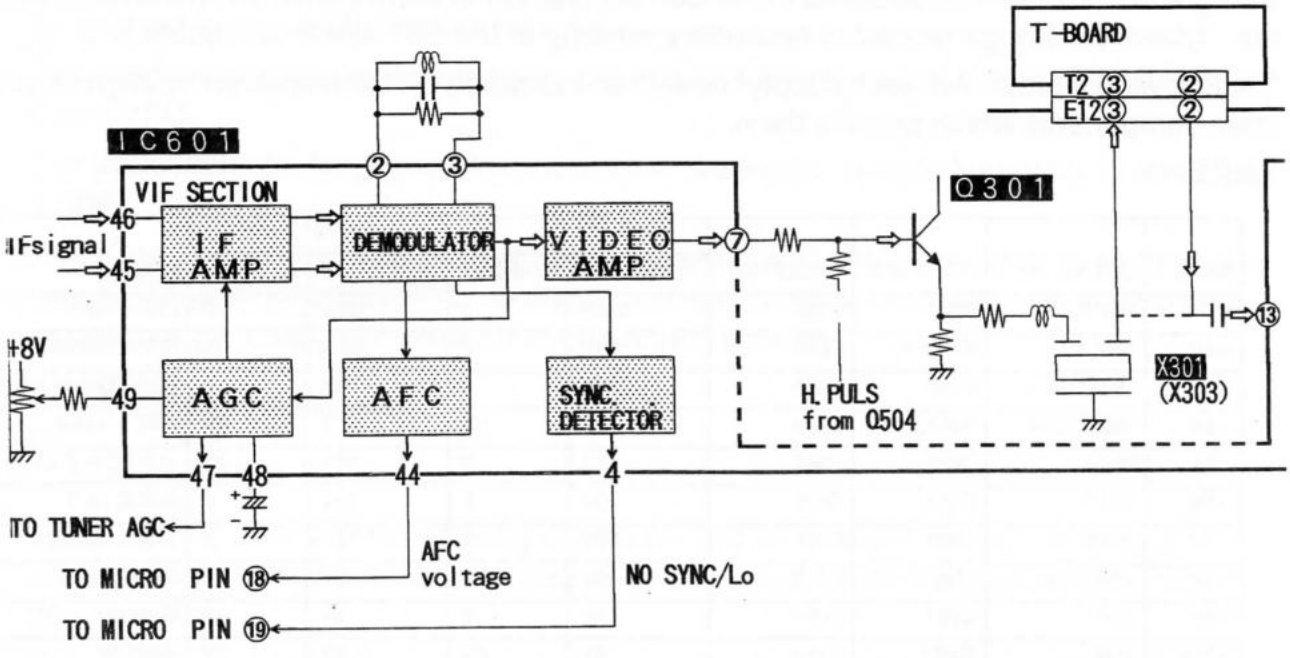
N.B. The +B9 (8V) is generated from the +B4 line and supplied only during power on mode. This line is switched by Q851 which is controlled by the power on/off switching control from pin 24 of IC1202.

3. VIF CIRCUIT

1. Video signal path

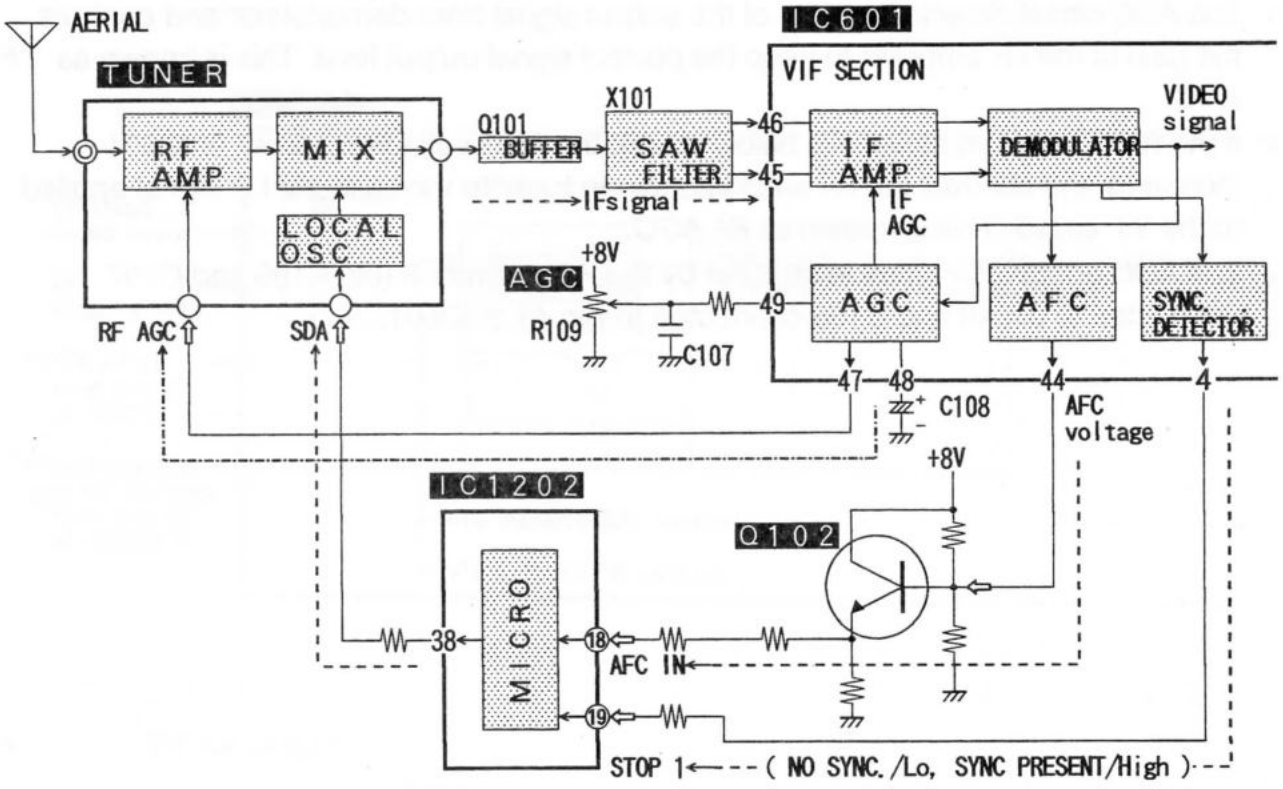


- The I.F. signal leaving the tuner is passed to Q101 for buffering .
- The I.F. signal is applied to the SAW filter X101 which provides the required bandpass shaping for the signal.
- From X101 the signal is applied to pins 45 and 46 of IC601.



- The signal is applied to VIF amplifier in IC601. After amplification the signal is passed to Demodulator (video detector), AGC circuit, AFC circuit and the Sync. signal detector.
- After detection the signal by demodulator is passed to Video amplifier and output from pin 7 of IC601.
- The signal is passed to Q301, filtered by X301 (X303) to remove the remaining SIF component and re-enters pin 13 of IC601. (The signal for teletext models is passed through the T-board. Pin 3 of E12- T3 connectors is the output for the E-board and pin 2 of T3-E12 is the input .)

2. Tuning & AFC (Automatic Frequency Control)

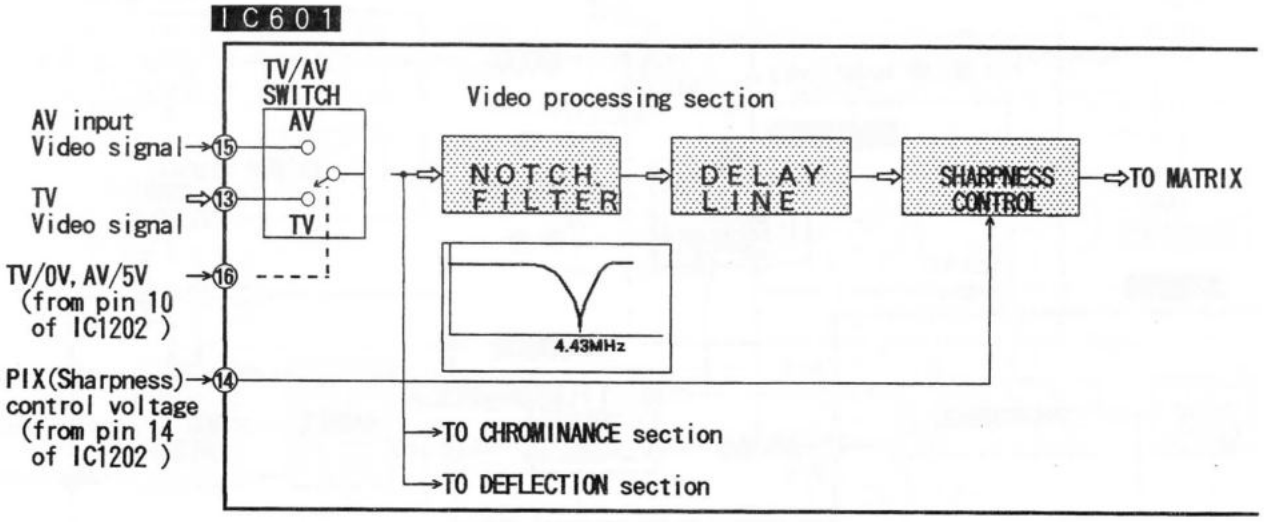


- When a channel is selected, the tuner local oscillation frequency is set the SDA data stream output from pin 38 of IC1202 and desired channel's I.F. signal (VIF 38.9MHz,{SECAM−L : 34.2MHz}) is output from tuner I.F. pin.
- If no signal is available on the selected channel frequency then the I.F. signal is not output, The sync. detector output (Called Stop 1) goes to a low voltage level (Lo=0V) at pin 4 of IC601. This Stop 1 signal is applied to pin 19 of IC 1202 the microprocessor.
- The microprocessor outputs control data to enable a high speed search operation to control the Local oscillator in the tuner.
- When the I.F. signal appears due to the high speed search, the sync. detector identifies the sync. pulse in the video signal from demodulator and the Stop1 voltage at pin 4 of IC601 goes high.
- If the Stop1 voltage goes high, the microprocessor changes the tuning control data to slow speed search operation.
- The AFC circuit detects and monitors the I.F. signal frequency. When the I.F. frequency is below 38.9MHz, the AFC voltage rises and causes the I.F. frequency to rise. When the I.F. frequency is higher than 38.9MHz the AFC voltage reduces and the I.F. frequency falls.
- During slow speed search mode, the microprocessor detects the AFC voltage applied from pin 44 of IC601 through Q102. When the AFC voltage becomes mid level between the highest and lowest points of its swing, the microprocessor stops the search operation and maintains the data.
- During normal signal reception, the microprocessor monitors the AFC voltage and controls the tuner local oscillator to maintain the I.F. signal frequency at 38.9MHz.

3. AGC (Automatic Gain Control)

- The AGC circuit detects the level of the output signal from demodulator and controls the gain of the I.F. amplifier to keep the correct signal output level. This is known as I.F. AGC.
- If the RF signal from aerial falls below 60 dB, the AGC voltage at pin 47 of IC601 increases and controls the RF amplifier gain in tuner to increase the I.F. signal applied to the VIF circuit. This is known as RF AGC.
- The AGC operating control level is set by the RC network R108, R109 and C107 connected to pin 49 and C108 connected to pin 48 of IC601.

4. VIDEO PROCESSING



1. TV/AV switch

- Video signals from the VIF circuit and the AV terminal (Through the T−board on teletext model) are applied to pins 13 and 15 of IC601 which are input terminals of the TV/AV switch.
- This switch is controlled by AV−cont1 from pin 10 of IC1202. When the AV−cont1 voltage is low (approx 0V) the TV video signal is selected and when the AV−cont1 voltage is high (approx 5V) the AV input video signal is selected.
- The video signal output from the TV/AV switch is applied to the Video processing, Chrominance processing and Deflection circuits.

2. Notch filter

- A notch filter removes the chrominance signal from the composite video signal and only the luminance (Y) signal is output to delay line.

3. Luminance Delay line

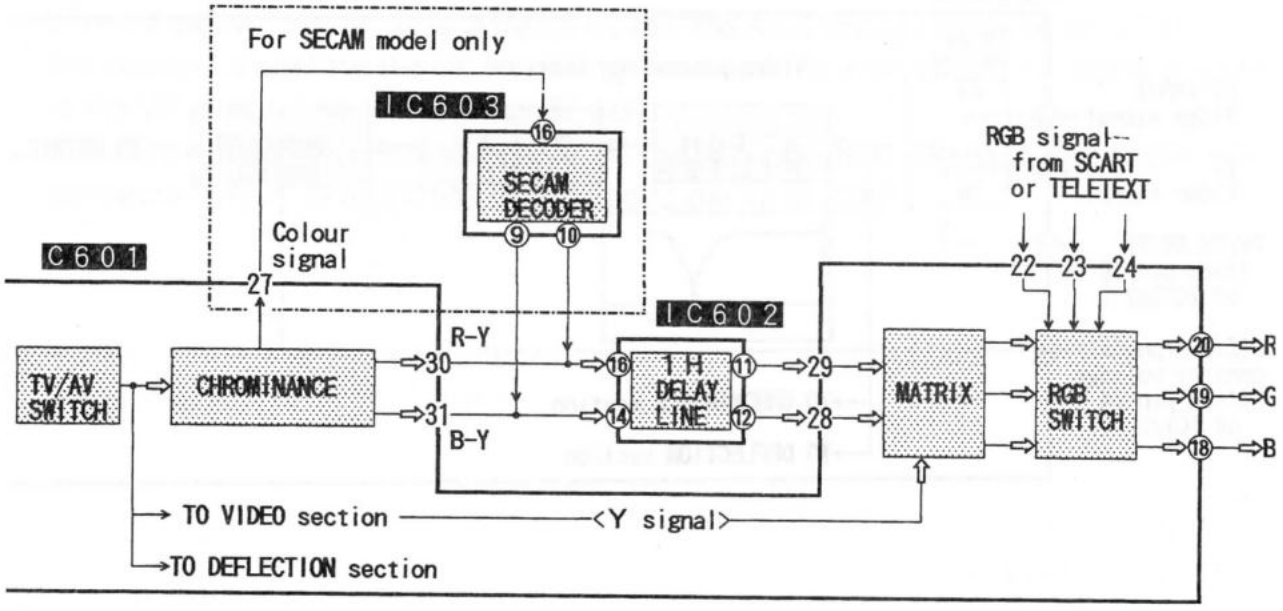
- The luminance delay line delays the luminance signal to match the timing of the chrominance signal which is delayed due to different frequency band of the signal and the chrominance delay line..

4. Sharpness control

- The sharpness control circuit adjusts the peaking level of luminance signal. The adjustment level is controlled by the PIX. voltage output from pin 14 of IC1202 and applied to pin 14 of IC601.
- The luminance signal is then applied to the RGB matrix circuit.

5. COLOUR PROCESSING

1. Colour signal path



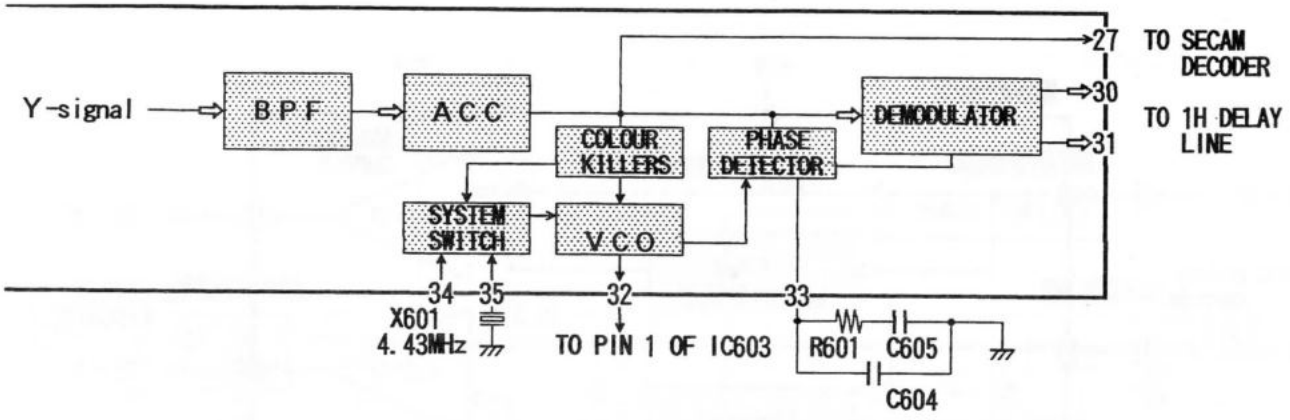
For PAL

- The video signal from the TV/AV switch is applied to the chrominance circuit.
- The chrominance circuit demodulates and outputs R−Y and B−Y colour−difference signals from pins 30 and 31 of IC601.
- These colour difference signals are applied to pins 16 and 14 of IC602 (the chrominance delay line) .
- the delay line operate as a comb filter so that the Y−signal component is removed and pure colour difference signals are output from pins 11 and 12 and applied to pins 28 and 29 of IC601.
- From here the colour signals pass to the matrix circuit where R, G and B signals are produced from the colour difference signals and the Y−signal.
- The R, G, B signals are output from pins 18, 19 and 20 of IC601 and pass through the RGB switch.

For SECAM

- The colour signal is output from pin 27 of IC601 and applied to pin 16 of IC603.
- IC603 demodulates and outputs colour difference signals from pin 9 and 10.
- These colour difference signals are applied to 1H delay line (pins 16 and 14 of IC602) and then follow the same path as the PAL signals.

2. Chrominance circuit



The chrominance circuit consist of the BPF (Band Pass Filter), ACC (Automatic Colour Controller), Multi−decoder, Colour Killers, Phase Detector and a VCO (Voltage Controlled crystal Oscillator) .

(1) BPF (Band Pass Filter)

- The Y signal is removed by the BPF and the colour signal is applied to ACC circuit..

(2) ACC (Automatic Colour Control)

- To keep a constant level of colour saturation, the ACC circuit controls the amplification of colour signal dependant on the intensity of the colour burst signal.
- The colour signal is supplied to multi−decoder.
- The colour signal is output from pin 27 of IC601 to pin 16 of IC603 for SECAM decoding.

(3) Colour killers

- The colour killer discriminates between the black and white or colour broadcasting signal by checking for the presence of the colour burst signal, and provides an ON/OFF operation for the succeeding colour processing circuits.

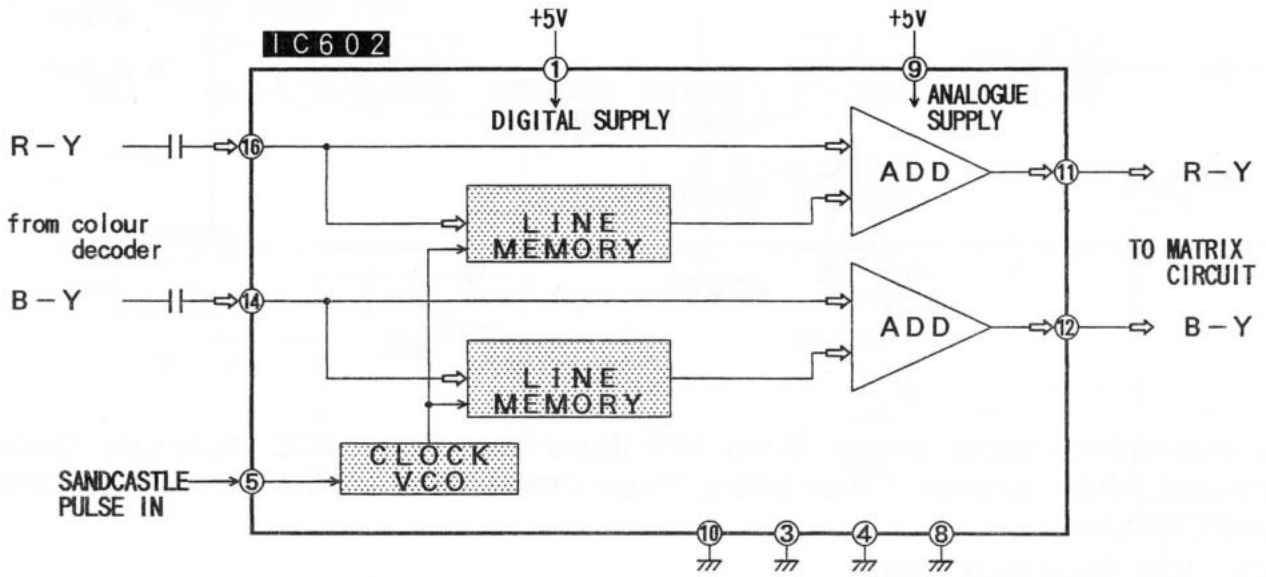
(4) VCO (Voltage Controlled crystal Oscillator) and Phase detector

- The VCO oscillates at 4.43MHz and provides a reference frequency signal whose base oscillation is set by X601 (4.43MHz crystal). This reference signal is applied to the colour phase detector.
- In the phase detector, the phase difference between the VCO reference signal and the colour burst signal is detected and output as a DC voltage.
- This DC voltage controls the reference signal which applied to the demodulator.
- The reference signal is also output from pin 32 of IC601 and passed to pin 1 of IC603 for the SECAM decoder. Pin 32 of IC601 also outputs the SECAM ident signal. When no PAL signal has been identified the DC voltage of pin 32 goes High.
- R601,C605 and C604 connected to pin 33 are the phase detection filter components.

(5) Multi−decoder

- The multi−decoder separates the colour difference signals from the colour signal. (The multi−decoder can demodulate PAL and NTSC colour signals. However this chassis only uses the PAL demodulator section of the decoder.)
- Colour difference signals are output from pins 30 (R−Y) and 31 (B−Y) of IC601 and applied to pins 16 and 14 of IC602.

3. 1H delay line



- The colour difference signals enter pins 16 and 14 of IC602
- Each signal is passed to a delayed and non–delayed path.
- The non–delayed signal is passed directly to the input of the adder, while the signal to be delayed is passed to the line memory.
- The line memory is synchronised with the horizontal sync. signal by the clock from the Clock VCO.
- The adder corrects for phase errors and provides signal outputs from pins 11 and 12 of IC602.
- This IC is consists of digital circuitry (Line memory) and analogue circuitry, so there are two +5V supply terminals. Pin 1 is supply voltage terminal for the digital circuitry and pin 9 is supply voltage terminal for the analogue circuitry.

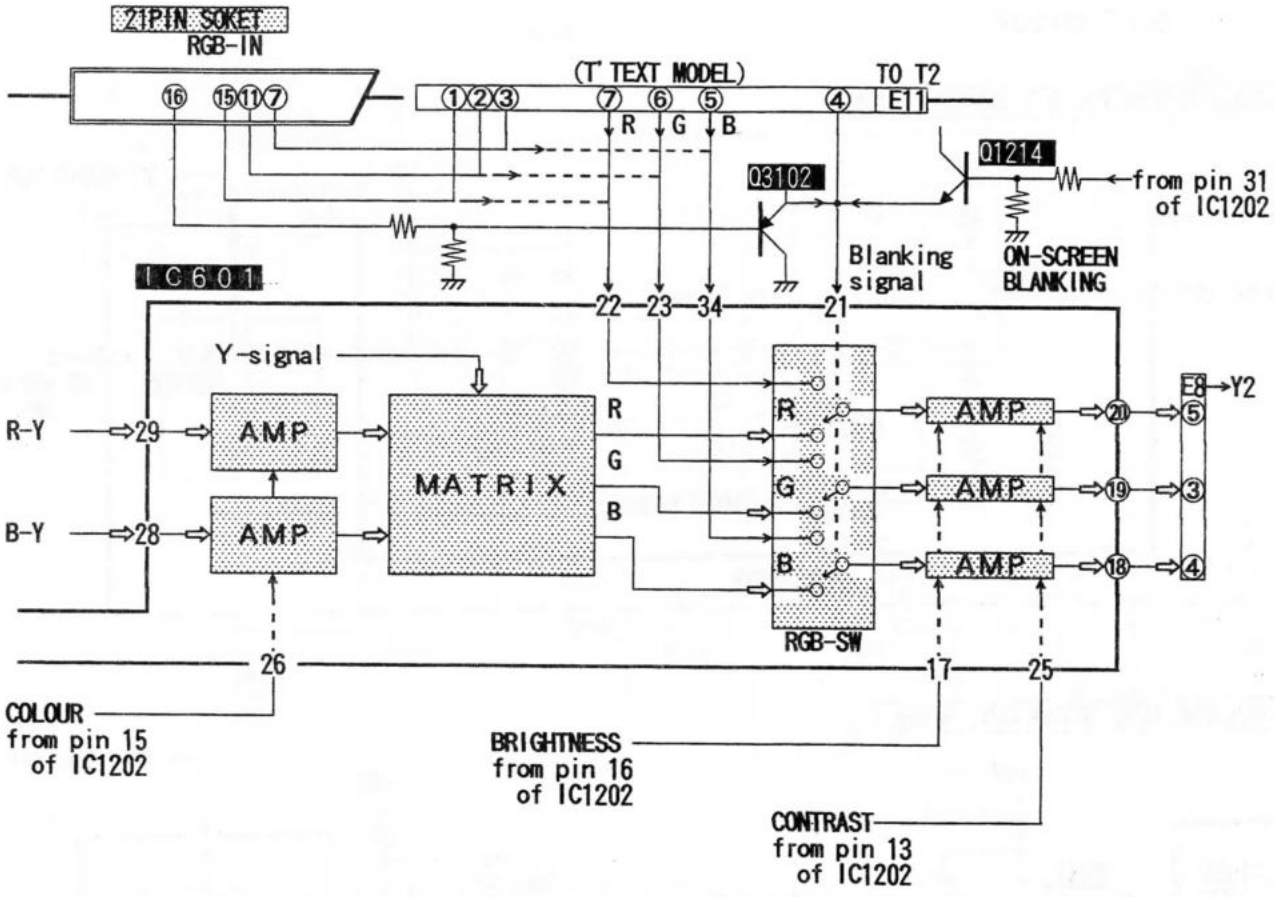
4. Matrix and RGB switch

(1) AMP (Amplifier)

- The R–Y and B–Y signals entering at pins 29 and 28 of IC601 are passed to gain controlled amplifiers which are controlled by the colour control voltage applied to pin 26.
- This control is supplied from two sources, one the colour DAC output of IC1202 pin 15 allowing customer control, and the other from the resistor network R607, R608 for sub colour control.

(2) Matrix

- After applying colour control the R–Y and B–Y signals are passed to the colour matrix circuit which produces the R–Y, B–Y and G–Y at it outputs.
- From here RGB signals are produced by matrixing the R–Y, B–Y and G–Y with the Y signal. The luminance signal is received from Video section of IC601.



(3) RGB switching

- The R,G,B signals from the matrix circuit are then applied to the RGB switching circuits.
- The RGB switching circuit switches between the RGB signals from the matrix circuit and RGB signals input at pins 22,23 and 24 of IC601.
- RGB switching control is performed by pin 21 of IC601, a High on this pin will allow the RGB signals available at pins 22, 23 and 24 to be processed.
- The switching of this pin is determined by one of three sources.
  - a.) Pin 16 of 21 pin AV terminal.
  - b.) Blanking control from pin 31 of IC1202 through Q1214.
  - c.) Teletext RGB blanking from pin 4 of connector E11.

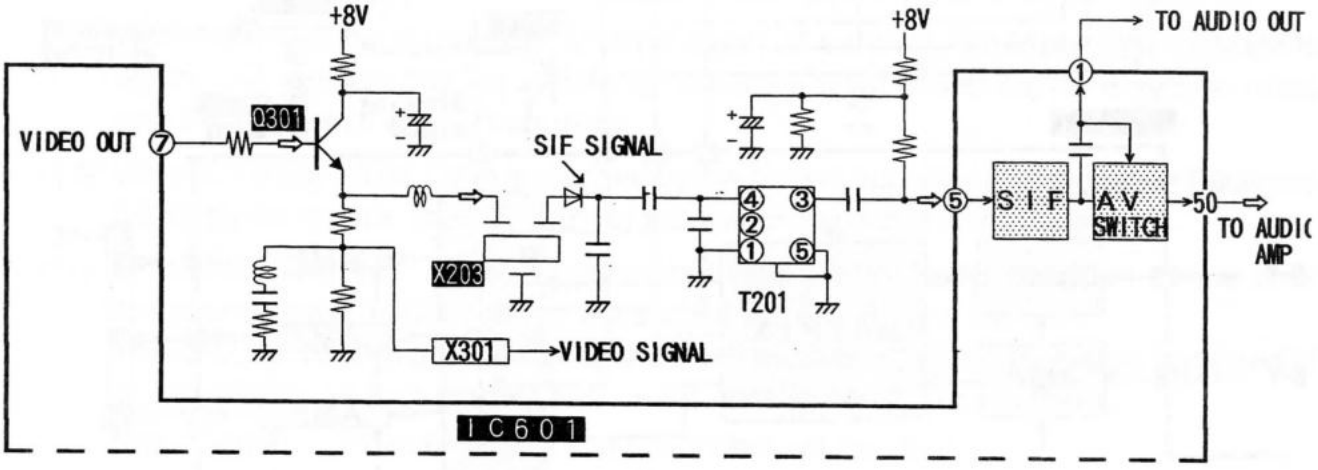
(4) Brightness/Contrast control

- The RGB signals are passed through the brightness & contrast control amplifiers.
- The brightness control voltage is applied at pin 17 of IC601.
- The contrast control voltage is applied at pin 25 of IC601.
- After brightness and contrast control, the RGB signals are output from pins 18,19 and 20, of IC601 and supplied to the CRT drive circuits via connectors E8 – Y2.

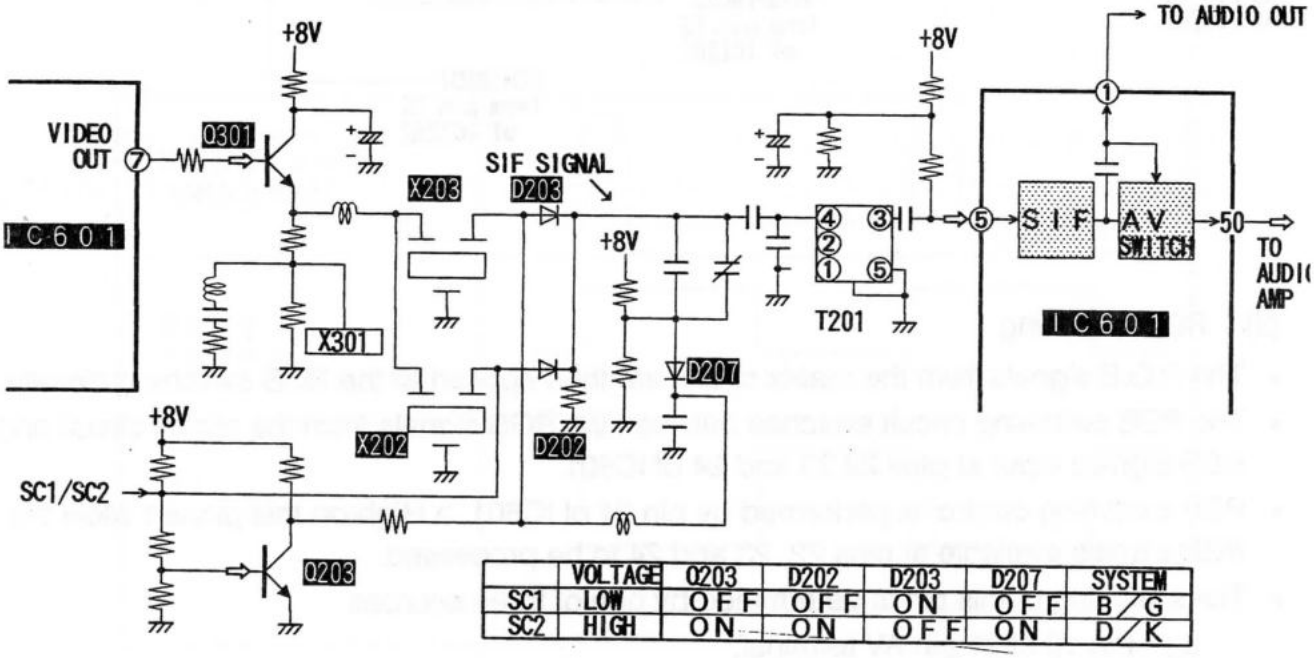
6. AUDIO CIRCUIT

1. S.I.F. circuit

SIGLE SYSTEM(PAL B/G OR PAL I) MODEL



DUAL(PAL B/G, SECAM D/K) MODEL

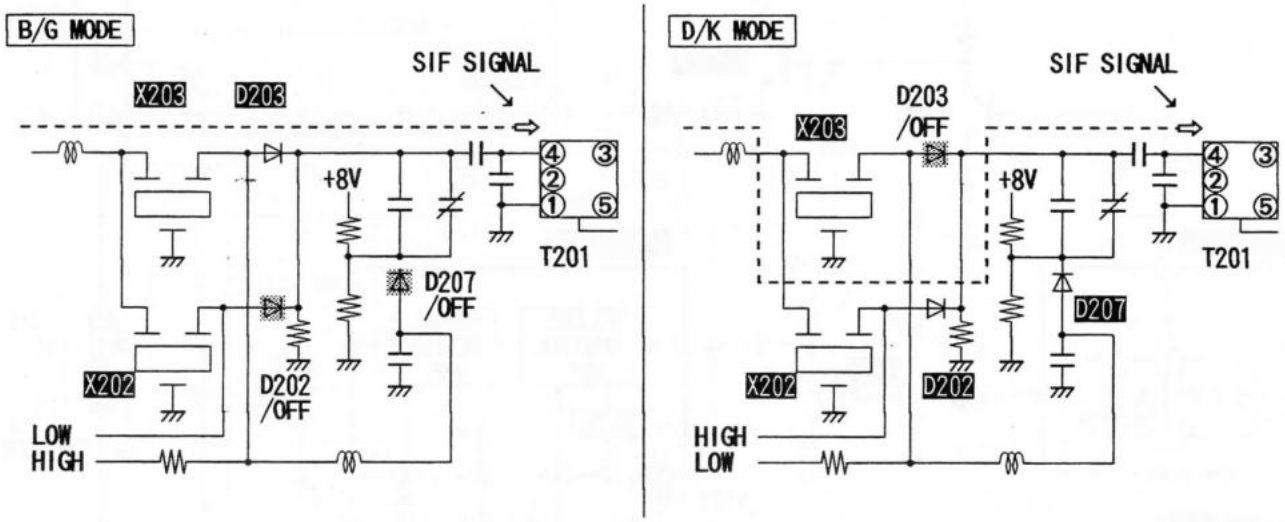


	VOLTAGE	Q203	D202	D203	D207	SYSTEM
SC1	LOW	OFF	OFF	ON	OFF	B/G
SC2	HIGH	ON	ON	OFF	ON	D/K

(1) Demodulation

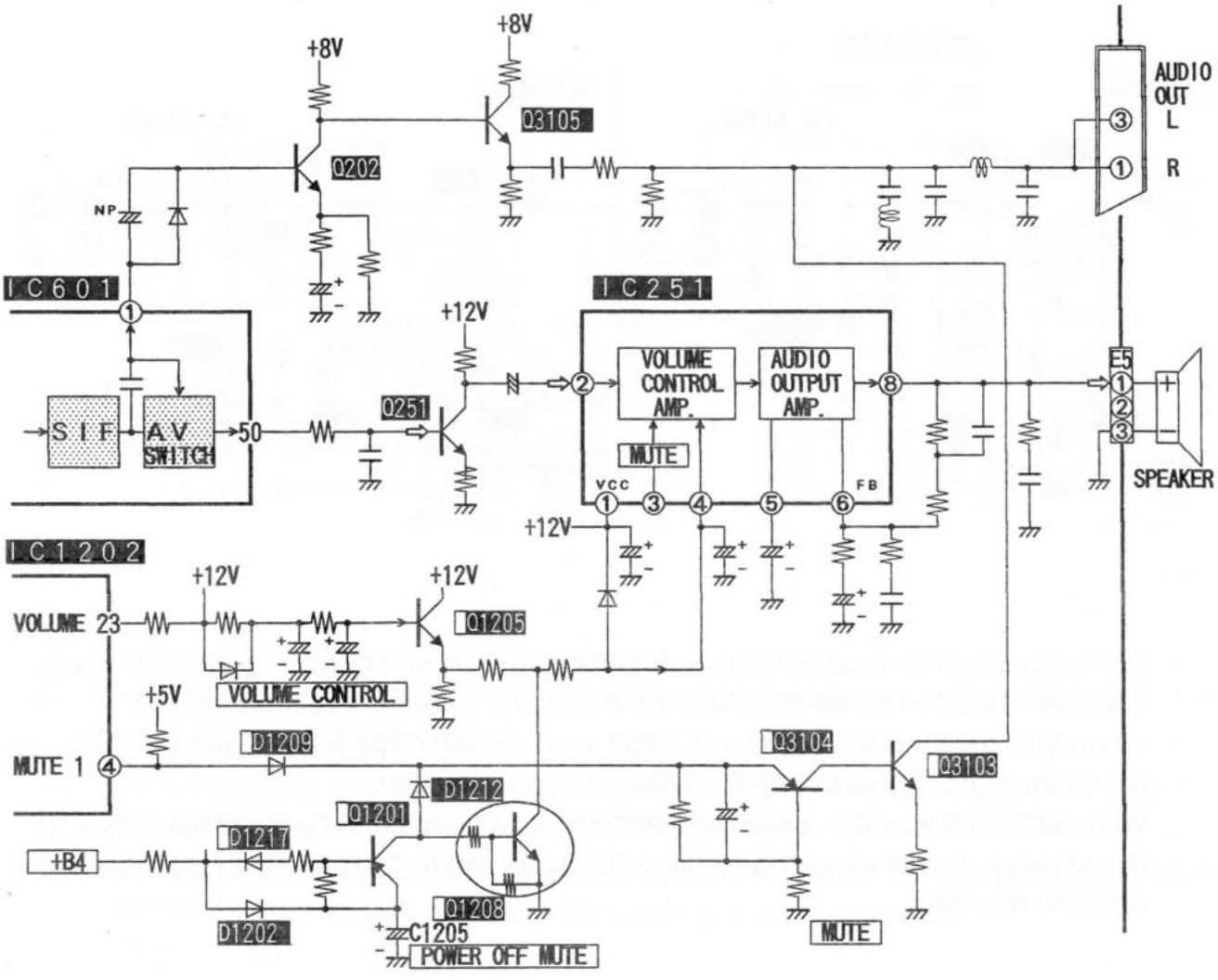
- The SIF signal is separated from the video signal at the emitter of Q301. This separation is performed by X202 or X203 (SIF filters).
- This separated signal is passed through T201 and enters the SIF demodulator inside IC601 at pin 6. After demodulation the signal is output via an AV switch and appears at pins 1 and 60 of IC601. From pin 60 the audio signal is passed to the audio output circuit (IC251).
- At the same time the audio signal from pin 1 is used to feed "audio out" signal to the 21 pin scart terminal

(2) SIF Filter selection (Dual sound system models only).



- Dual sound system models have both 5.5Mhz. (X203) and 6.5Mhz. (X202) SIF filters. These are selected by the SC1/SC2 control signal output from pin 8 of IC1202.
- When SC1 (B/G mode) is selected, D203 turns on and D202 & D207 turn off. This allows the signal filtered by X203 (5.5Mhz.) to pass to T201.
- When SC2 (D/K mode) is selected, D202 and D207 turn on while D203 turns OFF. In this situation the SIF signal filtered by X202 is passed to T201 and the response of the SIF path changed.

2. Audio Output



Speaker out

- The audio signal output from pin 55 of IC601 is applied to pin 2 of IC251 via Q251.
- The amplitude of the signal is controlled by the volume control voltage which is supplied from pin 23 of IC1202 via Q1205. The signal is then amplified at the audio output amplifier and output from pin 8 to speaker.

Audio out

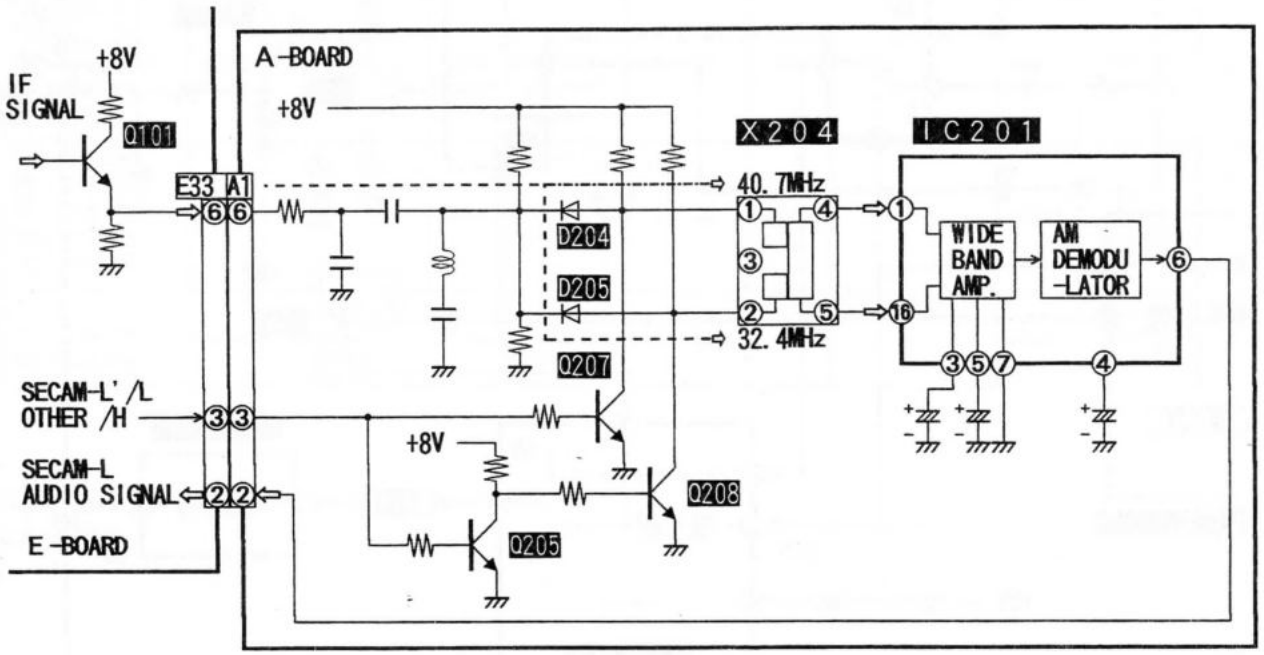
- The audio signal output from pin 1 of IC601 is applied to pins 1 and 3 of the 21 pin scart socket via Q202 and Q3105.

Power off mute

- When the power to the TV is switched off, the audio amplifier circuit creates a "pop" noise due to the electric charge in the circuitry.
- To prevent this noise Q1201 and Q1208 operate. During normal operation the +B4 voltage charges C1205 via D1202.When the power is switched off, the emitter voltage of Q1201 is held at the +B4 level by C1205. Because of this, Q1201 and Q1208 turn on and the volume control voltage is grounded. As the result the "pop" noise is prevented.
- However after the +B4 supply is discharged from C1205 via D1217, Q1201 and Q1208 will turn off. (Volume control and mute circuit are explained in the microprocessor and control section.).

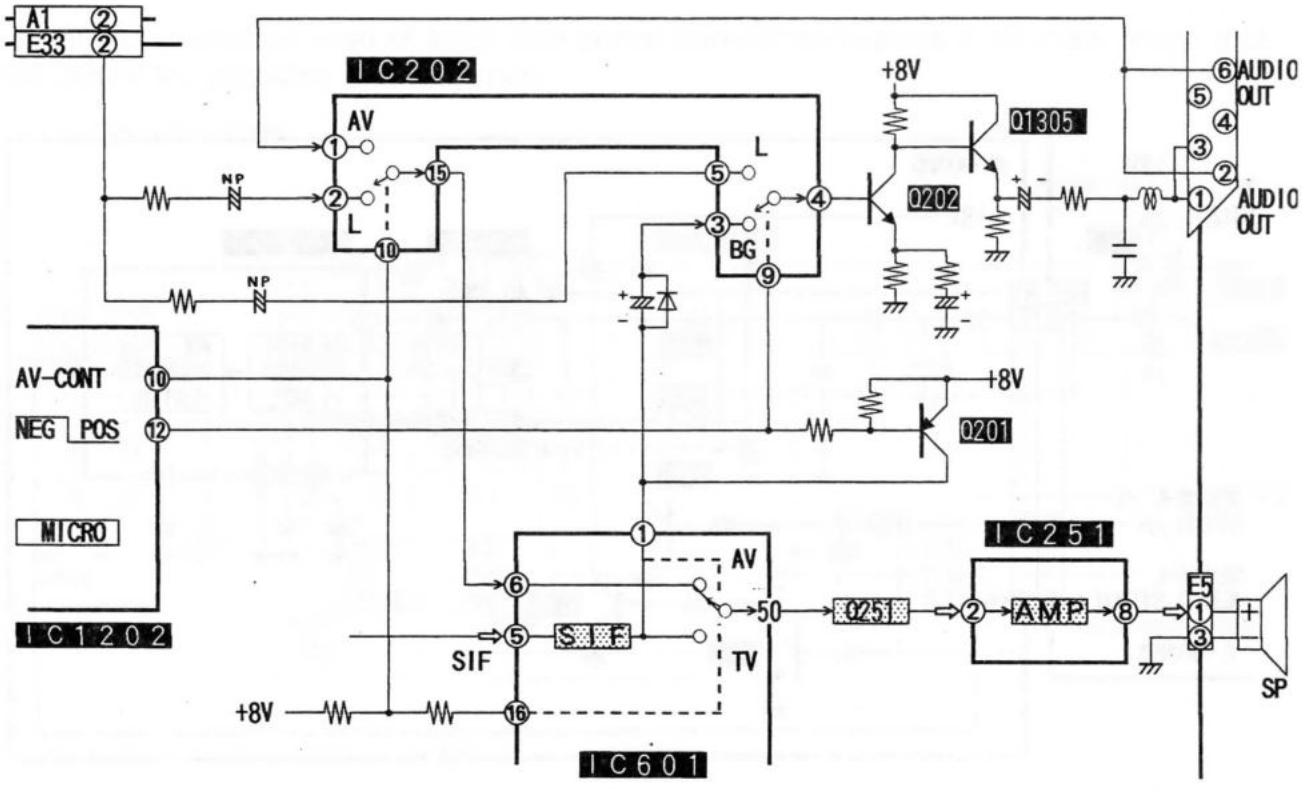
3. SECAM L audio circuit

SIF circuit



BAND	A1 PIN 3 SECAM−L'/OTHERS	Q205	C	Q207	C	Q208	C	D204	D205	SIF
VIF−L	L	OFF	H	OFF	H	ON	L	OFF	ON	40.7MHz
VHF−H/UHF	H	ON	L	ON	L	OFF	H	ON	OFF	32.4MHz

- I.F. signal from Q101 emitter is applied to the cathode of D204 and D205 through pin 6 of connectors E33 and A1.
- The SIF filter X204 has two inputs, one at with a filter centred at 32.4MHz and the other centred at 40.7MHz.
- Depending on the "SECAM−L/OTHERS" signal output from IC1202, the diodes D204 or D205 switch on or off (via transistors Q205 and Q207) and the required filter input is selected.
- This ensures that the correct SIF signal is supplied to IC201(Wide band amplifier and AM demodulator).
- The audio signal is amplified and demodulated inside the IC201 and output from pin 6.



- When the SECAM–L signal is received, pin 12 of IC1202 goes low ($\overline{\text{NEG}}$|POS). Then the audio AV switch in IC601 becomes set to AV mode.(If pin 1 is high, the audio AV switch in IC601 is set to AV mode.)
- IC202 operates as the audio AV switch and the audio out select switch.

7. TELETEXT

The Z–5 chassis uses a EUROTEXT device which provides Europe–wide text decoder, 4 page memory and automatic FLOF & TOP decoder. Only Russian and Hebrew versions generate the need for a single language device.

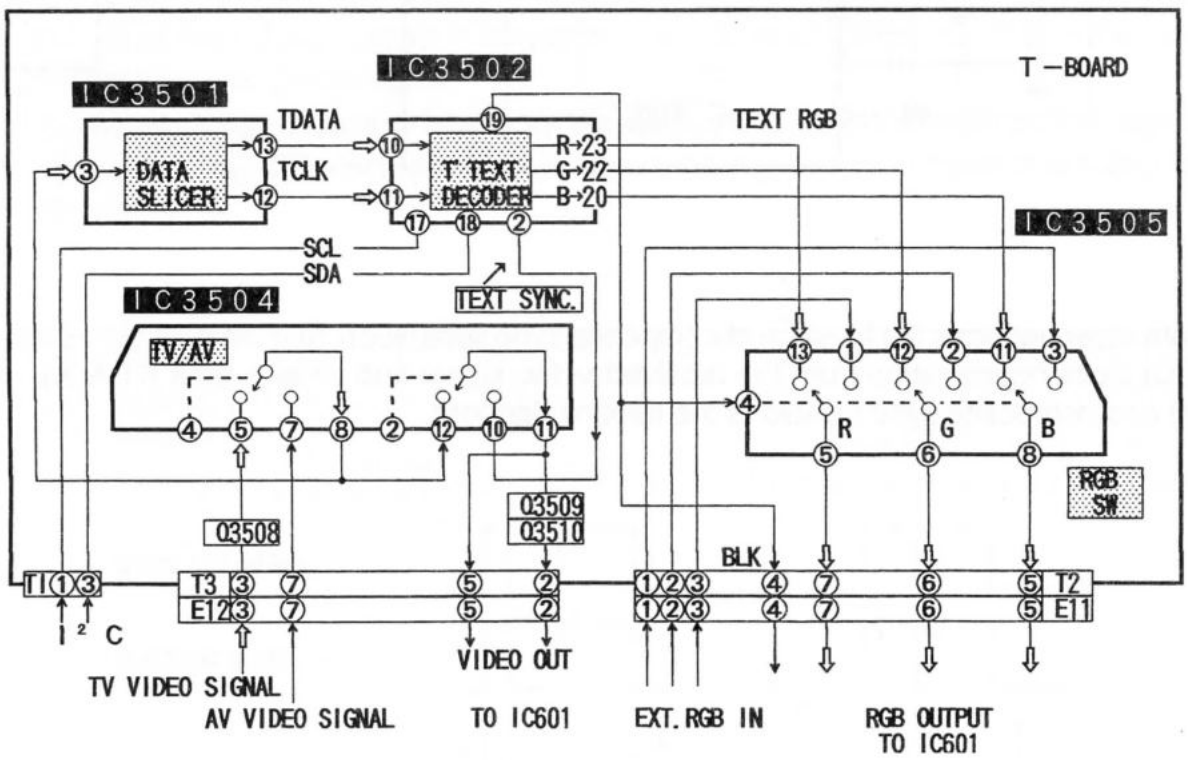
EURO–WIDE

PARTS No.	LANGUAGE	
CF70205ANW CF70205BNW	SELECTABLE BY SOFTWARE	ENGLISH, GERMAN, FRENCH, ITALIAN, SPANISH, SWEDISH, FINNISH TURKISH ,HUNGARIAN
CF70204NW		GERMAN, ITALIAN, FRENCH, FINNISH, POLISH, CZECH, CROATIAN, SLOVENIAN

SINGLE VERSION

CF70209NW	RUSSIAN
CF70210NW	HEBREW

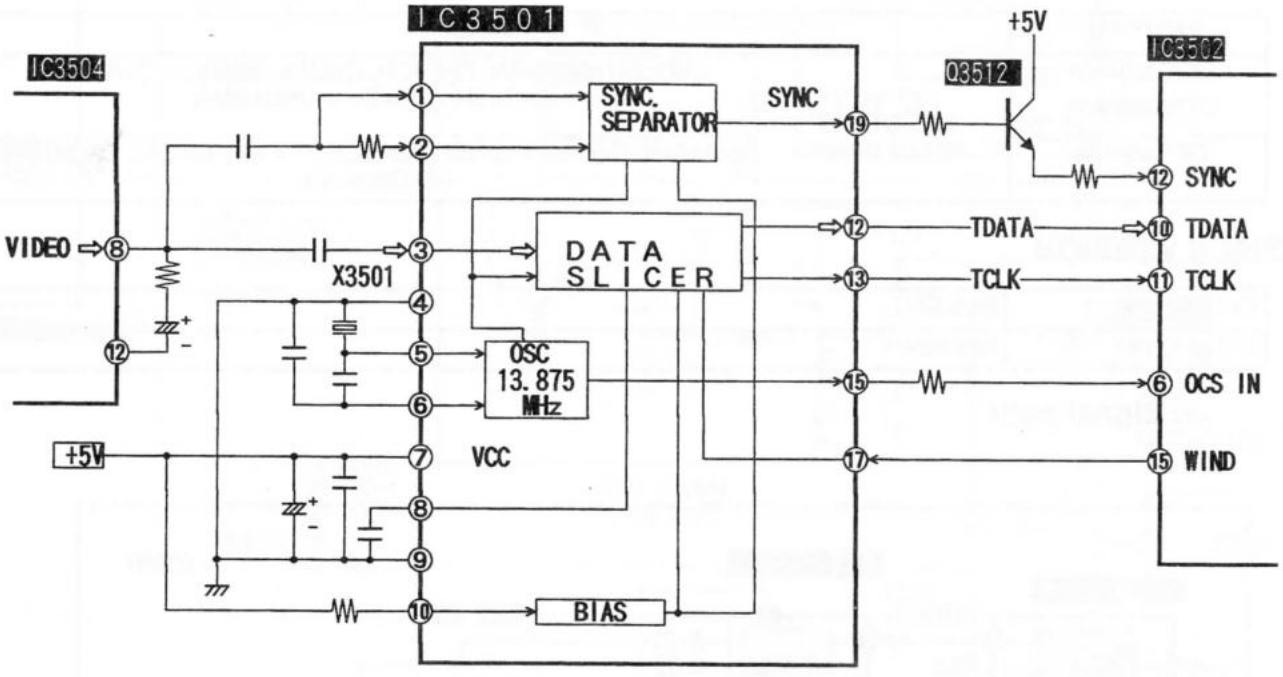
1. Signal path



- The video signals from the VIF circuit and AV terminal are selected by IC3504 the TV/AV switch and sent to IC3501 the data slicer .
- The Data slicer picks up Text data (TDATA) and the Text clock (TCLK) signals and supplies them to IC3502 the Text decoder.
- The Text decoder process the Text data and outputs R, G, B signals.
- As well as processing the Text data, the text sync. signal is output from IC3502 to IC3504. When text mode is selected the text sync. signal is passed to IC601 for use by the deflection circuit.

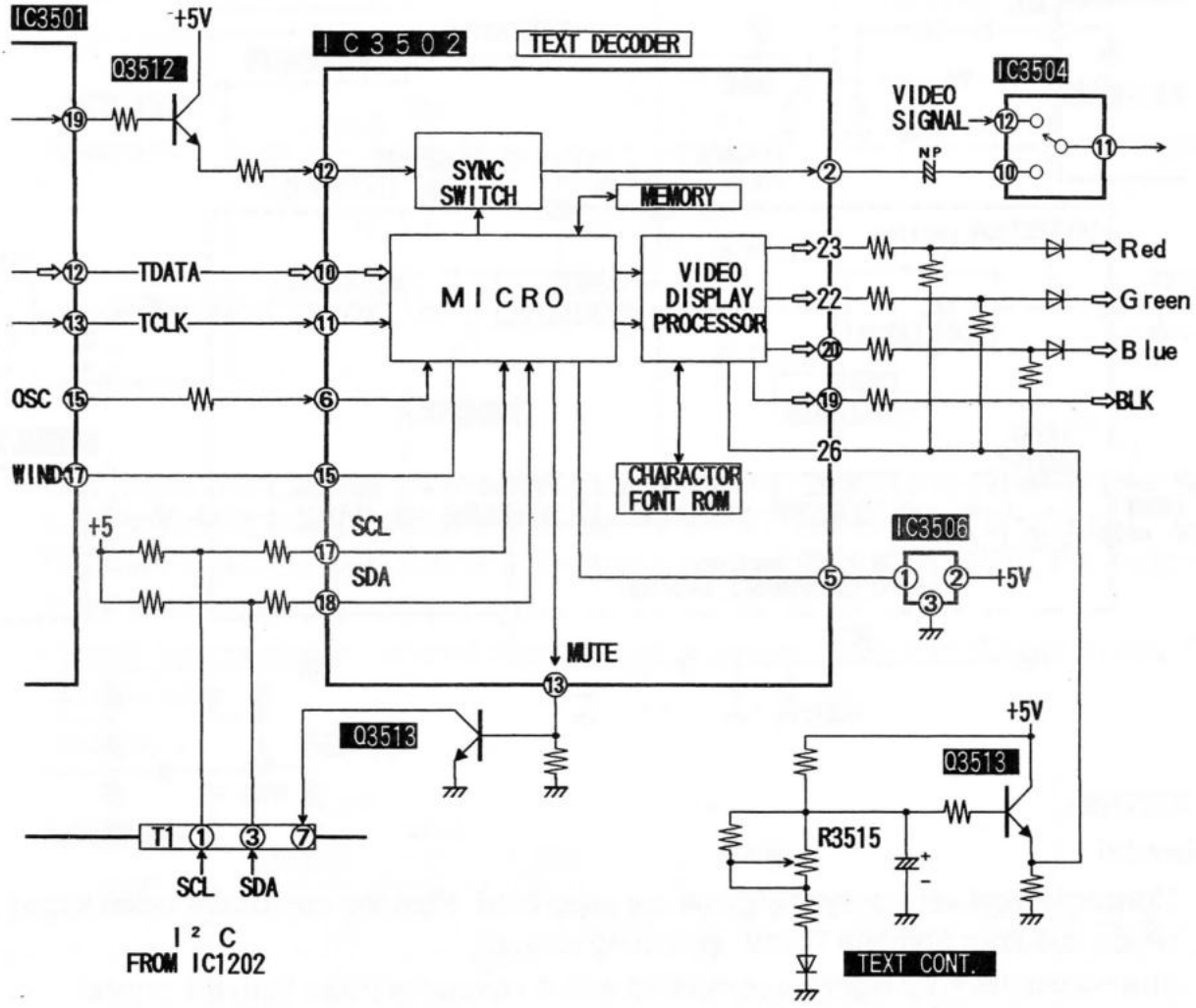
- The text RGB signals and the external RGB signals from the Scart socket are switched by IC3505 the RGB switch. The RGB switch in IC3505 is controlled by the blanking (BLK) signal from the text decoder.

2. Data slicer



The data slicer performs the function of composite sync separation, teletext data extraction and text data clock regeneration from the received video signal and passes data (TDATA), clock (TCLK) and composite sync signals to the teletext decoder.

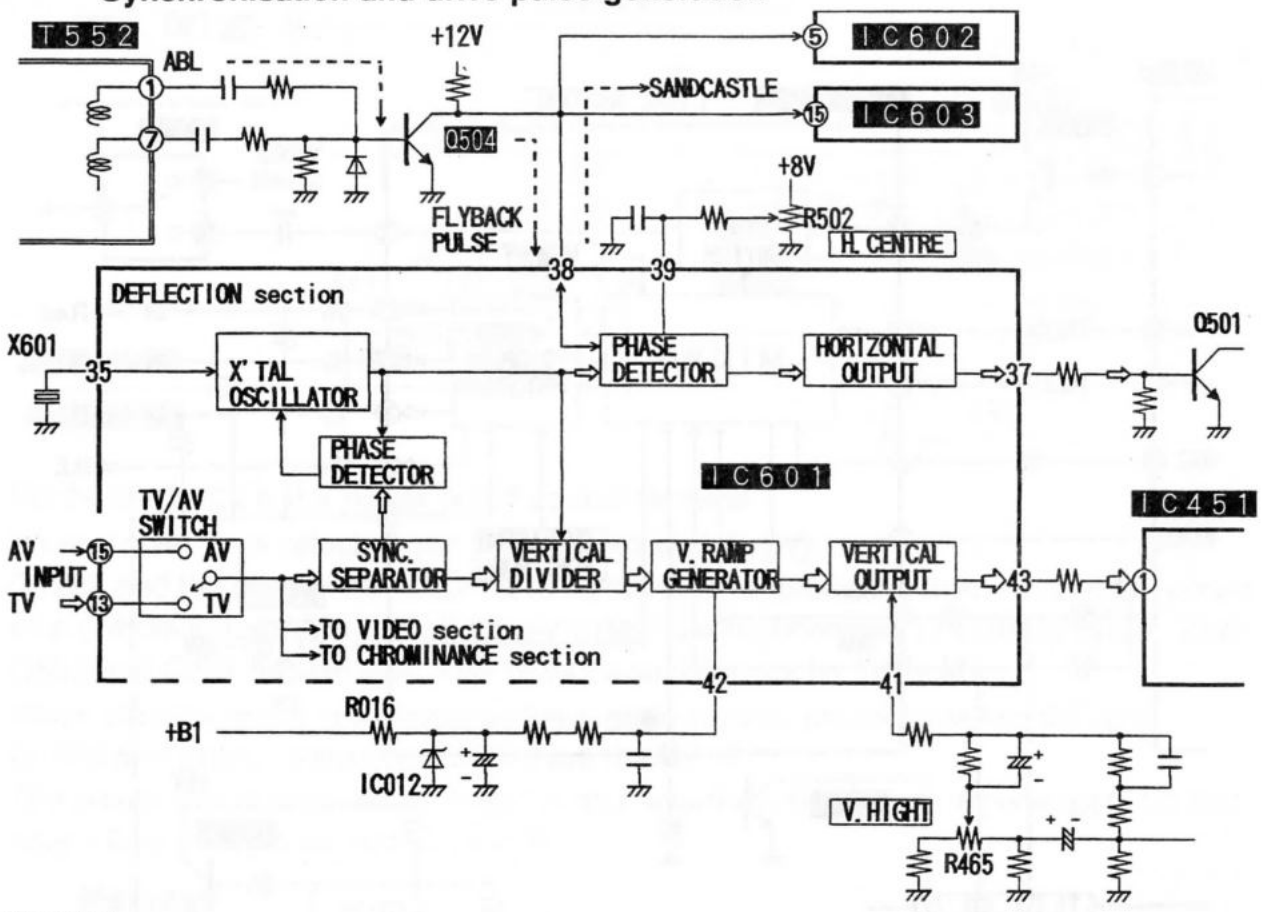
3. Teletext decoder



- IC3502 (text decoder) is synchronized with IC3501 by the "OSC" signal from pin 15 of IC3501.
- The microprocessor chooses a maximum of 4 pages of text data which are selected by I^2C information and memorised by the internal memory element.
- The video display processor creates red, green, and blue characters as well as text blanking signals according to the text data from the microprocessor.
- The sync signal is applied to pin 12 and input to sync switch. When text mode is selected, the microprocessor controls the sync switch and outputs sync signals from pin 2.
- The microprocessor outputs window pulses from pin 15 which is high during lines 2 to 22 of the video signal. This allows for text data acquisition.
- The microprocessor outputs a mute signal from pin 13 which is low when text is displayed on the screen and a bad incoming video signal is detected. It is used for connection to the TV audio mute circuit (IC601) via Q3513.

8. DEFLECTION

1. Synchronisation and drive pulse generation



Horizontal

- Horizontal and vertical sync signals are separated from the composite video signal which is output from the TV/AV switching circuit.
- The horizontal sync signal is compared with a horizontal pulse from the crystal oscillator by a phase detector and the result of this controls the horizontal drive pulse to allow synchronization with the horizontal sync signal.
- The horizontal drive pulse is also compared with a flyback pulse from T552(F.B.T./ Flyback Transformer) to ensure that the horizontal deflection is synchronised with the horizontal sync signal.
- The horizontal drive pulse is output from pin 37 and applied to Q501 (line drive transistor).
- Pin 38 has two functions, one is flyback pulse input and the other is SCP (Sand Castle pulse) output.

Vertical

- A vertical divider counts horizontal pulses from the crystal oscillator used for the line drive circuits. When the divider receives a vertical sync signal from the sync separator, it outputs vertical drive pulse. The vertical drive pulse is also synchronized with the vertical sync signal. If a vertical sync signal is not applied to the divider, the divider outputs a reset pulse after counting approx. 350H .(Free run condition)
- The vertical drive pulse (Reset pulse) is converted to a ramp signal and output from pin 43 of IC601 via the vertical output circuit.

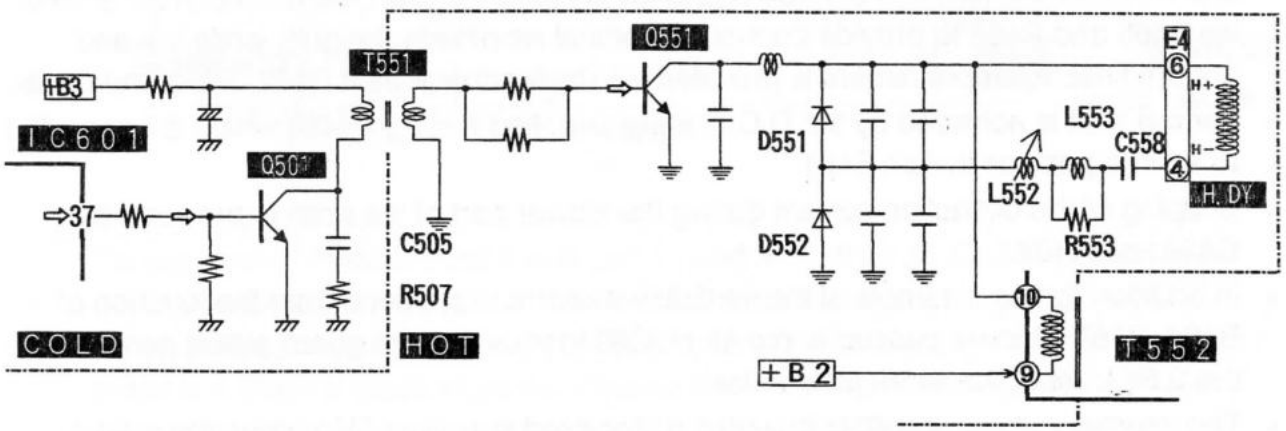
2. Horizontal output

OUTLINE

Horizontal drive signal is provided from IC601 and passed to a horizontal drive transistor for amplification and impedance matching before passing to the horizontal output transistor.

The horizontal output stage provides deflection current for the scan coils, EHT for the CRT and a number of supply lines for peripheral circuits.

- The line drive signal from pin 37 of IC601 is fed to the horizontal drive transistor Q501. This transistor has a transformer T551 in its collector circuit, which is used to provide A.C. coupling and impedance matching with the horizontal output transistor Q551.
- To ensure that the transistor Q501 is not damaged by excessive spikes generated by the back E.M.F. in the drive transformer, a filter network R507, C505, is connected across the emitter collector of the transistor.
- The horizontal output transistor Q551 is used to drive the horizontal deflection coils and flyback transformer.
- S – correction is achieved by C558 and its associated circuitry.
- Linearity is achieved by L553 and R553 while the diode modulator circuit is formed by D551 and D552.

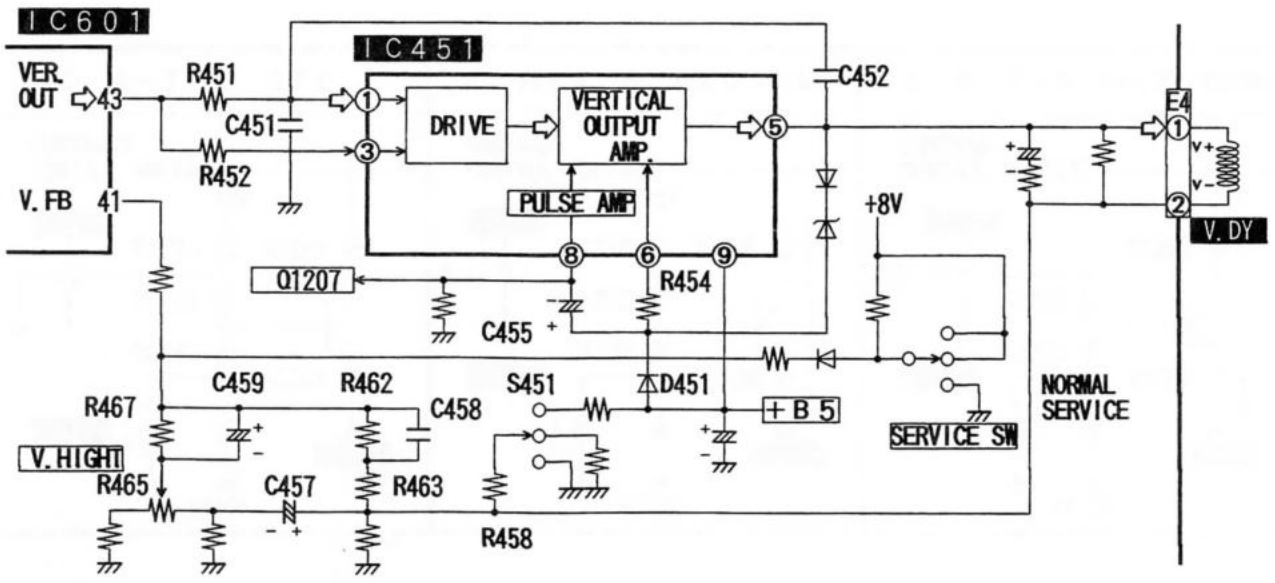


3. Vertical output

OUTLINE

The vertical timebase functions are provided in two parts,. IC601 produces the synchronisation and vertical oscillation while the vertical drive for the deflection coils is provided by a IC451.

- The vertical drive signal enters IC451 at pin 1 via an integration network consisting of R451and C451. The signal is also fed to pin 3 via external resistor R452.
- The signal which is input at pin 1 is fed to the vertical driver of the output stage, while the signal applied to pin 3 is the input to a switching circuit.
- This switching circuit rapidly turns off the lower output stage when flyback starts, which allows a quick start of the flyback generator.
- The vertical output which appears at pin 5 is also applied as feedback to pin 1.
- During scan pin 6 is connected to ground via pin 4 and the capacitor C455 is charged rapidly via D451. During flyback, pin 6 is connected to pin 9. This in conjunction with D451 and C455 provide twice the supply voltage to the vertical output stage at flyback time, this ensures a linear ramp for the vertical waveform.
- The vertical deflection waveform appearing at pin 5 of IC451 is then passed through the deflection coils to achieve scan.
- The return path of the deflection coils is through C457 (which provides A.C. coupling) and R464. At the junction of R464 and C457 a sample of the deflection current is taken via R465 and R456 to provide control for vertical amplitude (height), while top and bottom linearity improvement is provided via the feedback path R462, R463 and C458.
- Vertical shift is achieved by the D.C. current supplied through R458 which is connected to a three position switch S451.
- Shaping of the deflection current during the slower part of the scan is provided by C459 and R467.
- In addition to this a sample of the vertical waveform is provided from the junction of R462, R467 which is passed to pin 41 of IC601 for use by the guard circuit generating the 2.5V level of the sandcastle pulse.
- The internal voltage stabilizer provides a stabilised supply of 6V to drive the output stage, so the drive current is not affected by supply voltage variations.



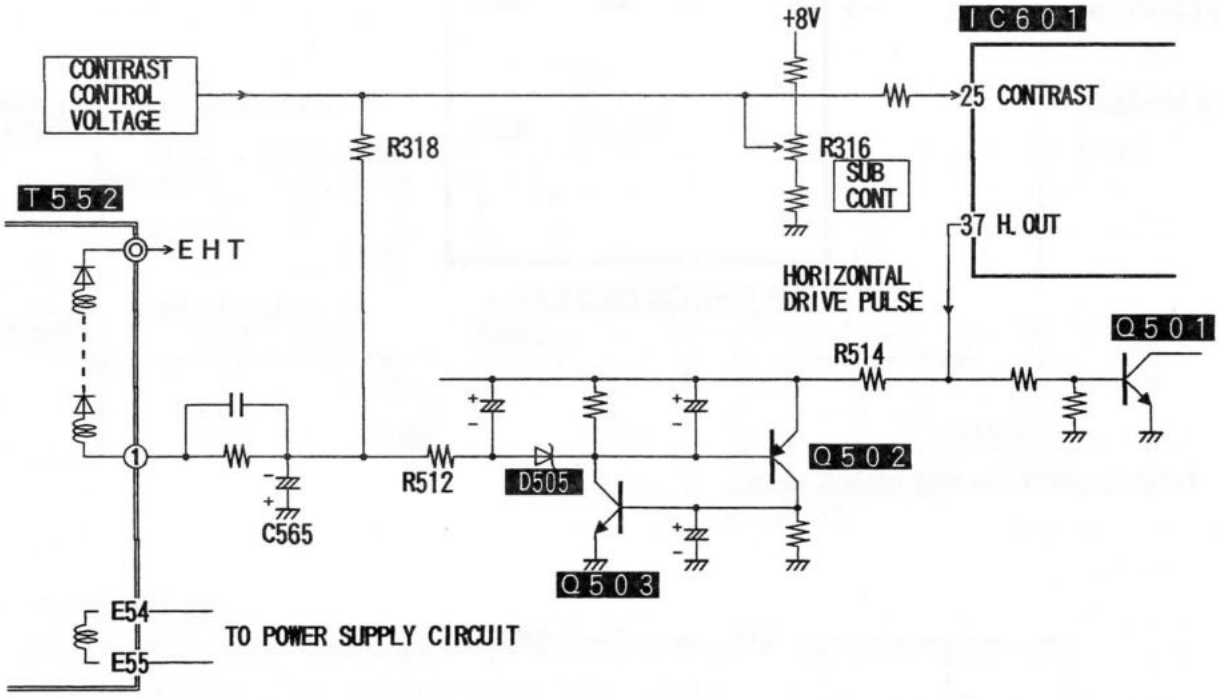
BEAM CURRENT LIMITING (A.B.L)

The C.R.T. beam current is monitored from pin 1 of the flyback transformer. As the beam current increases, an increasingly negative charge is developed across C565.

This is passed to the contrast control of IC601 to limit the beam current.

As the negative charge increases across C565 this is passed to resistor R318. This has the effect of reducing the positive voltage being applied to the contrast control of IC601 pin 25, which in turn reduces the beam current.

If however the beam current continues to increase to a point where it reaches approx 1.1mA, the maximum control range of pin 1 of the F.B.T. will be reached. At this point D505 will conduct causing Q502 to conduct. This will provide base current for Q503 causing it to conduct so forming a latch. With both transistors conducting base drive will be removed from the horizontal drive transistor Q501 and the horizontal output stage will shutdown.



9. SERVICE INFORMATION

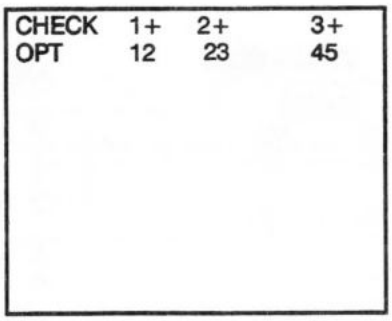
1. SELF CHECK AND SOFTWARE OPTION SETTING

This chassis provides self check function which is included option setting check.

(1) Self check procedure
Simultaneously press the off timer button on the remote control unit and the V (−) button on the TV set.

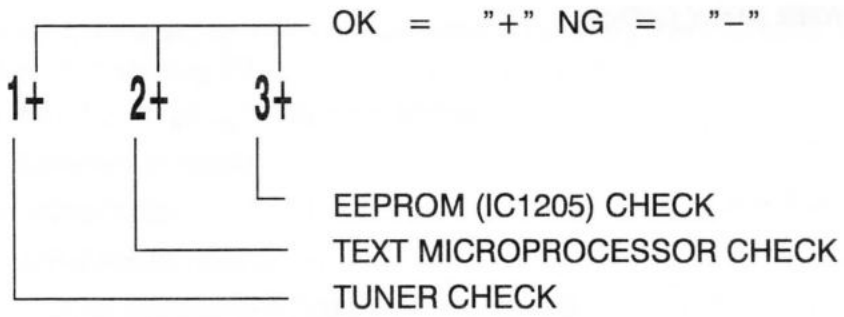
(2) The TV set enters the self check mode and the result are displayed on the screen.

Self check data →
Option setting data →



−SELF CHECK DISPLAY−

- How to read the self check data



None text model should display " 2− "

(3) Press any key to clear the self check mode and return to the normal mode.

*It is possible to change options as follows.

Option 1

By the resistor R1215.

With resistor	None text model
Without resistor	Teletext model

Option 2

By voltage change at pin 20 of IC1202 using resistor combination R1212 and R1213

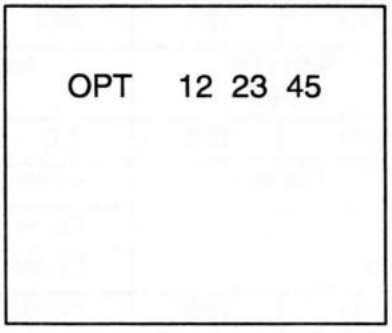
Voltage	0.5 ~ 1.1	2.4 ~ 2.9	4.3 ~ 5.0
SECAM L	NO	YES	NO
TUNER TYPE	V+U+H	V+U+H	UHF
UNITEX	YES	NO	NO

Option 3 ~ 6

2. Software option setting procedure

(1) Set the colour and sharpness level to minimum

(2) Press the Off timer button on remote control and the F key on the TV set.



ON–SCREEN

(3) Select the desired option by the program up/down button on the remote control.

(4) Select the decimal option bits by using the 0 ~ 7 buttons on the remote control.

(5) Press the STR button on the TV set to store the new option settings.

(6) Press the F button to return the TV to normal operating mode.

3. Option setting check

The feature and function(System,market mode) are set by 6 option bytes on this chassis. There are two types of option byte setting methods.
One is hardware setting which is set by changing the resistor value.
The other one is software setting which is set by EEPROM data.

OPT 1 2 2 3 4 5Each number is decimal equivelent of the option bit settings.

Option number	BIT 2		BIT 1		BIT 0	
	0	1	0	1	0	1
1	NOT USE (Fixed to 0)		Tint control		Teletext	
		–	NO	YES	NO	YES
2	SECAM L		Tuner type		Type of teletext	
	NO	YES	UHF only	VHF UHF Hyper	None or Euro–text	Uni–text
3	English character		Fine tuning		SIF(SC1/SC2) selection	
	NO	YES	NO	YES	NO	YES
4	Top–text inhibition		Auto Flof		Text language	
	NO	YES	NO	YES	EAST	WEST
5	Cats eye		AV mode		BIT1	BIT0
			TV/AV		0	0
			TV/AV1/AV2		0	1
	NO	YES	TV/AV1/AV2/AV3		1	1
6	Tuner		Market setting			
	NO (Monitor)	YES (Receiver)	Others	UK	France	Others

How to read the option settings

Example : Values for Model TX–21S1TC

OPT (1 2) (2 3) (4 5)

Binary	
1 0 1 (5)	Receiver Not UK and France
1 0 0 (4)	Cats eye TV/AV
0 1 1 (3)	TOP text Auto FLOF West European language
0 1 0 (2)	With fine tuning
0 1 0 (2)	EUROTEXT VHF/UHF/Hyper tuner
0 0 1 (1)	With text

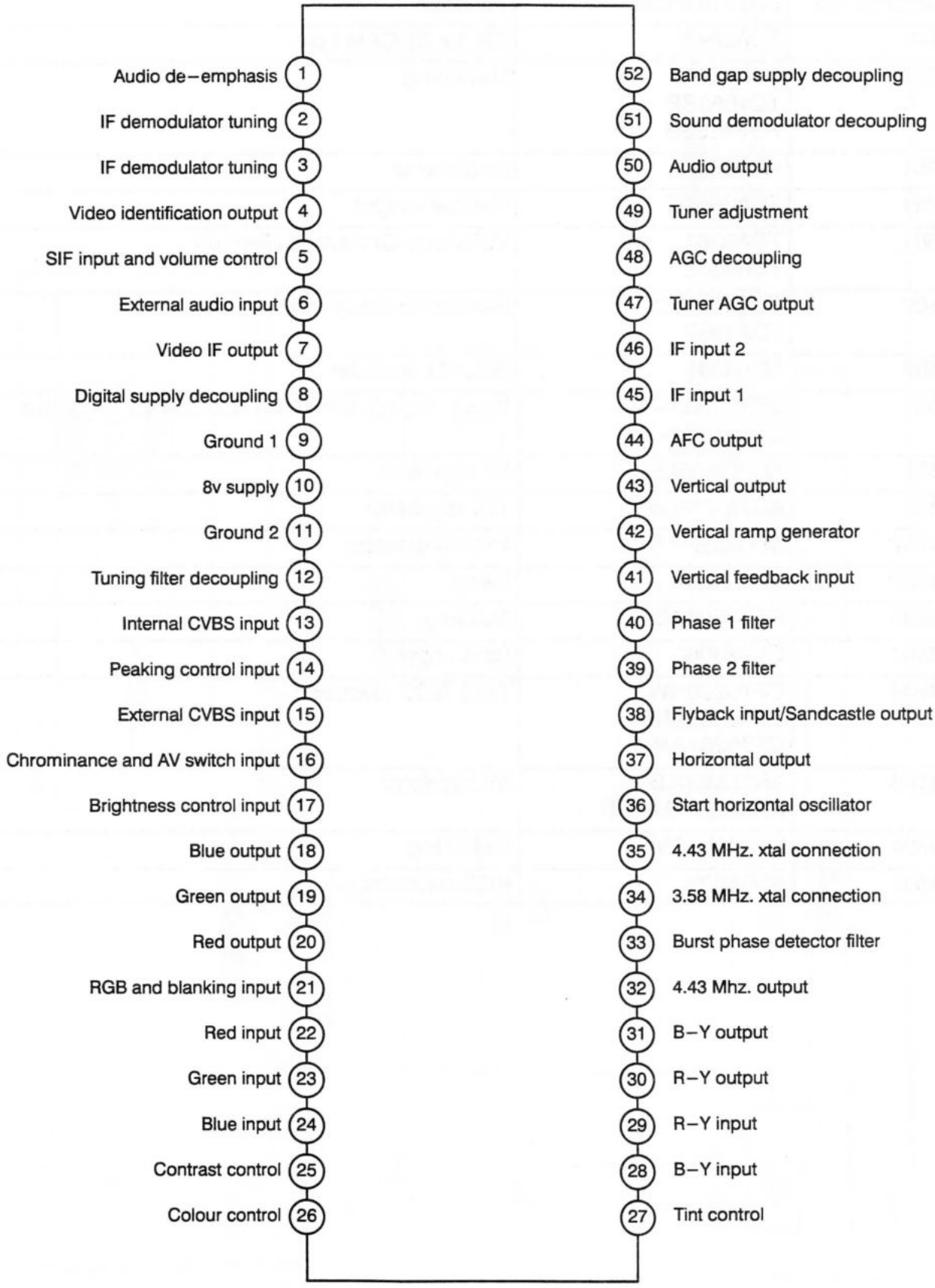
10. I.C LISTINGS

Reference Table

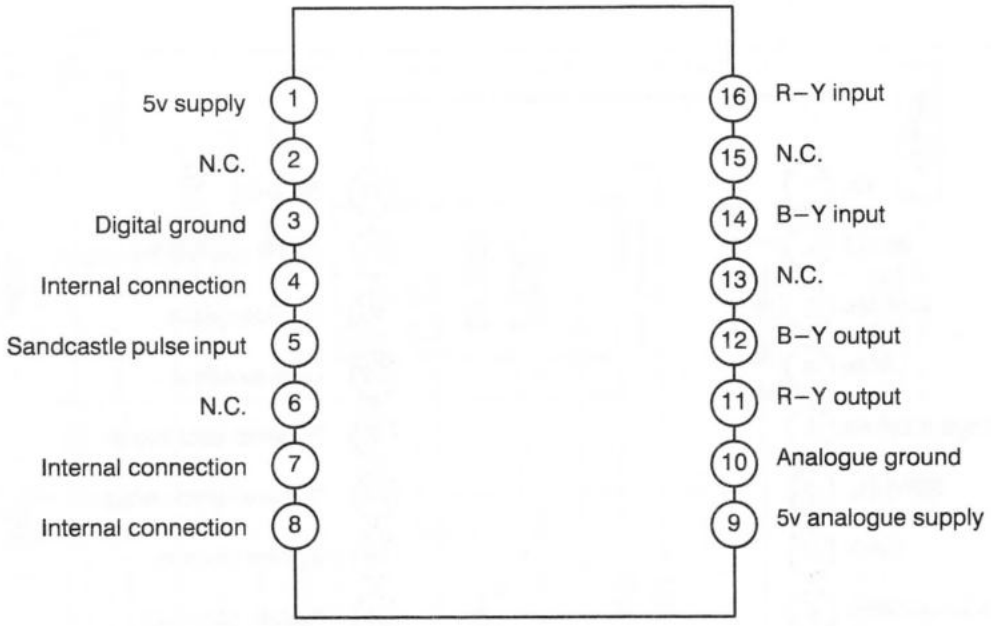
Reference No.	Parts Number	Function
IC201	TDA3843	SIF for SECAM I & L'
IC202	MN4053B TC4053BP HEF4053B	Switching
IC251	AN5265	Audio amp
IC451	TDA3653C	Vertical output
IC601	TDA8361 TDA8362	VIF/Video/Chroma/Deflection
IC602	TDA4661V2 TDA4662	Baseband delay line
IC603	TDA8395	SECAM decoder
IC801	STR51203−M STR51224−M	Power supply switching and control regulator
IC851	AN78M05LB	5V regulator
IC852	AN78M12LB	12V regulator
IC1202	MN152811TBS	Microprocessor
IC1203	MN1280R	Reset
IC1205	ST24C02AB1	Memory
IC3501	CF72306	Data slicer
IC3502	CF70200NW CF70095ANM CF70204ANM	TELETEXT decoder
IC3503	AN78M05LB L78MO5−M−RB	5V regulator
IC3504	LA7222−TV	Switching
IC3505	AN5862K	RGB switching

11. MAIN IC PINOUT INFORMATION

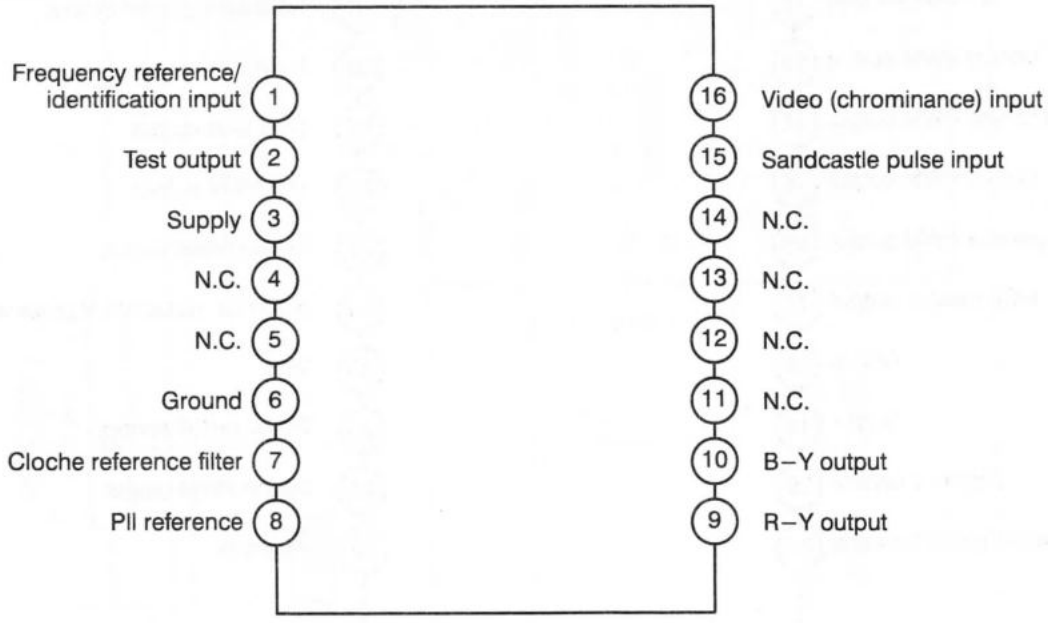
1. IC601 VIF/Video/Chroma/Deflection



2. IC602 Baseband delay line



3. IC603 SECAM decoder



4. IC1202 Microprocessor