DIGITAL VOLTMETERS

A210, A111, A212 AND A213

AND

FANOUT UNIT A214

PROVISIONAL
TECHNICAL
MANUAL

The information contained in this manual is provisional; a full Technical Manual will be sent to all registered users immediately it becomes available.

Part No: A2100194 **Date of Issue: May 1972**

CONTENTS

FAN OUT ACCESSORIES

	Solartron Part No.
Plug 50 Way BICC 1 off MS50 RN - BR118	354002340
Pins (Male) BICC 50 off RM20M - 12 - D29	354001610

NOTE

FAN OUT UNIT A214

In the Provisional Manual, the Fan Out Unit does not appear as a separate diagram.

Parts of the Unit (comprising Boards 27 and 28) appear in the following diagrams:-

13. Clock Oscillator and Reset (Part of Board 28).

14. Ramp Up/Ramp Down Control (Part of Board 28).

15. Counter and Reading Display (Part of Board 27).

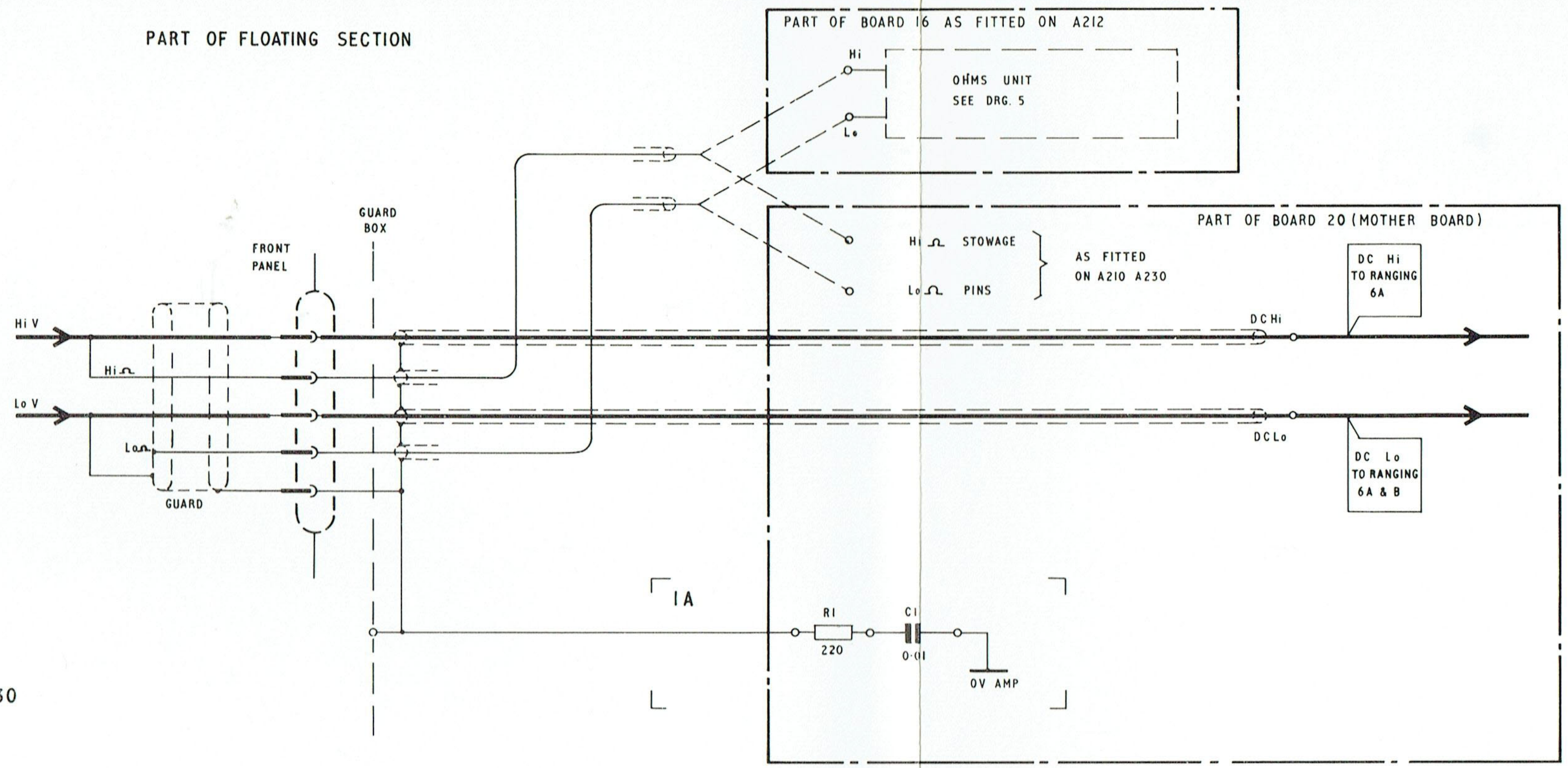
16. Range, Mode, Response & Rate Commands (Part of Boards 27 and 28).

17. Range & Mode Serialiser, Store & Display (Part of Board 27).

18. Sample and Auto Range Control (Part of Boards 27 and 28).

SECTION 7 Circuit Description

PART OF FLOATING SECTION



INPUT

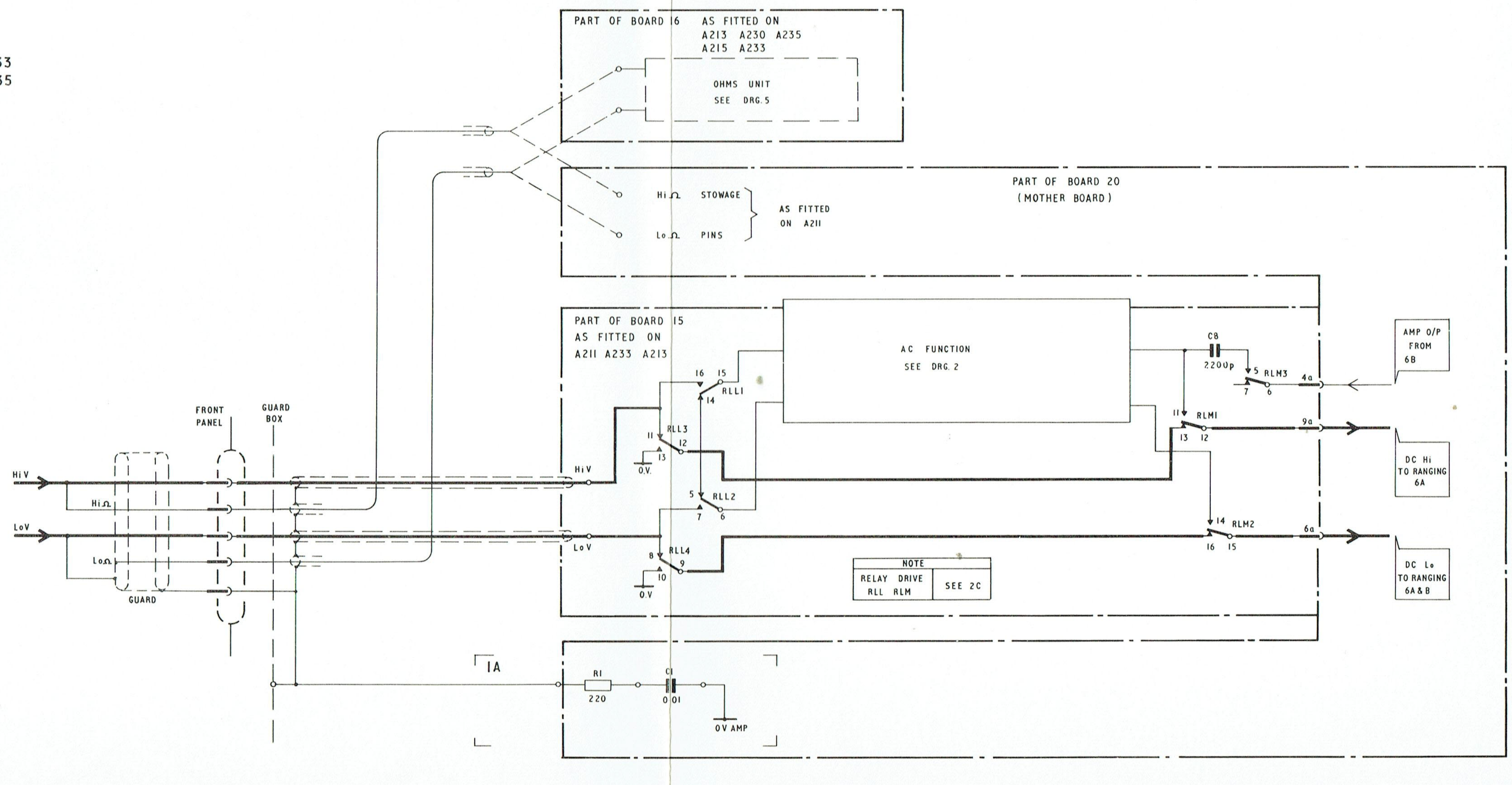
DC A210 A230

DC & ⊓ A212

INPUT

DC & AC A211

DC, AC & ⊓ A213 A233
A215 A235



DC INPUT 1

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1. DC INPUT

TOP

DC	A210, A230
DC and Ω	A212

BOTTOM

DC and AC	A211
DC, AC and Ω	A213, A215, A233, A235

	MODE	
Relay	**AC**	**DC & Ω**
RLL	ON	OFF
RLM	OFF	ON

The RELAYS are shown in the DC and Ω MODE.

1A

R1, C1 is a filter for inverter signal pick up on the GUARD BOX.

2. AC INPUT MEAN SENSING (A211, A213, A233)

Mode relays RLL and RLM are shown set to AC.

2A AC RANGE ATTENUATOR

1000V Range

R1, R4 and R5 is a 1000/1 attenuator, selected by RLG (OFF), RLH (OFF) and set by RV2. C16 is the h.f. response trimmer.

100V Range

R1, R3 and R2 is a 100/1 attenuator, selected by RLG (OFF), RLH (ON), RLR (OFF) and set by RV1. LINKS 1, 2 and 3 are set for correct h.f. response on 100V range, with C17 as fine trimmer.

10V

R1, R10 and R11 is a 10/1 attenuator, selected by RLG (OFF), RLH (ON), RLR (ON) and set by RV3. C23 is the h.f. response trimmer.

1V and 100mV Ranges

No attenuation. RLG is ON.

2B RLL AND RLM DRIVE

Mode	RLL	RLM
AC	ON	OFF
DC & Ω	OFF	ON

2C AC RANGE LOGIC

Mode	OUTPUTS		
	A	B	C
DC & Ω	Hi	Hi	Lo
AC	See 2D		

2D AC MODE

	RELAYS						
AC	AC				DC		
Range	G	H	R	J	A	B	C
1000V	OFF	OFF	OFF*	OFF	ON	OFF	ON
100V	OFF	ON	OFF	OFF	ON	OFF	ON
10V	OFF	ON	ON	OFF	ON	OFF	ON
1V	ON	ON*	ON*	OFF	ON	OFF	ON
100mV	ON	OFF*	OFF*	ON	ON	OFF	ON

*Not effective

2E AC CONVERTER (SEE DRG. 3 - AC CONVERTER MEAN SENSING)

The differential output is 1.2V DC (at f.s.d.) for nominal input on each range.

AC Range	RLJ	Gain
1V	OFF	X1
100mV	ON	X10

2F AC FILTER

Response	RLK	Time to 0.1% fsd
FAST	OFF	< 1 sec
SLOW	ON	< 4 secs

The differential input is filtered by R6, R7, R8, R9 and C4, C5, C10,C11 which make a low pass filter of 60dB at 50Hz.

With RLK on, attenuation is increased to 90dB at 50Hz with the addition of C3, C6, C9 and C19.

2G AC FILTER DRIVE

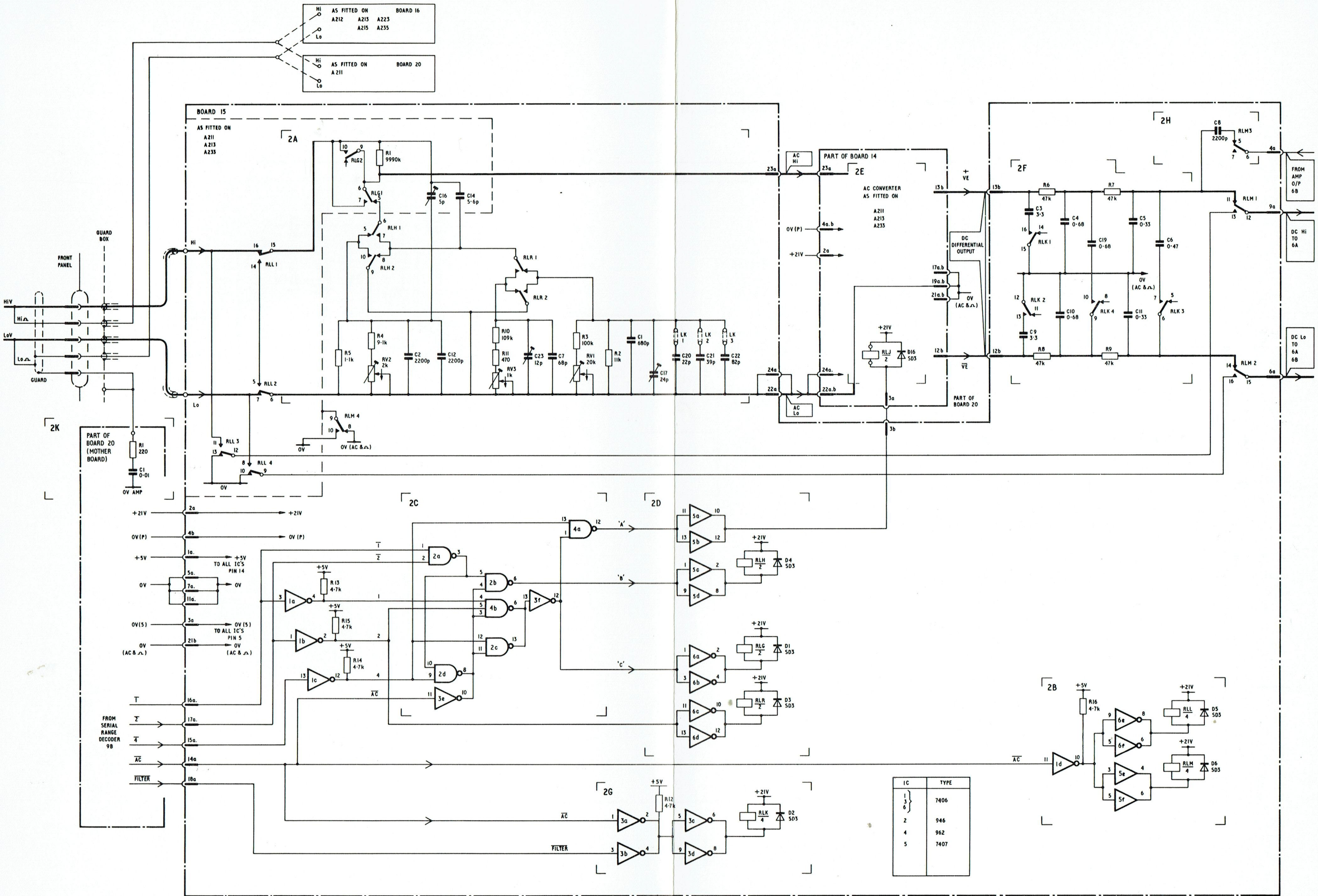
RLK is disabled unless AC Mode is selected.

2H

On AC Mode, C8 is coupled between INPUT AMPLIFIER (Drg. 7) output and DC Hi from 2F. This compensates the amplifier response on low frequency ac inputs.

2K

R1, C1 is a filter for inverter pick up on the GUARD BOX.



IC	TYPE
1, 3, 6	7406
2	946
4	962
5	7407

AC INPUT (MEAN SENSING) 2

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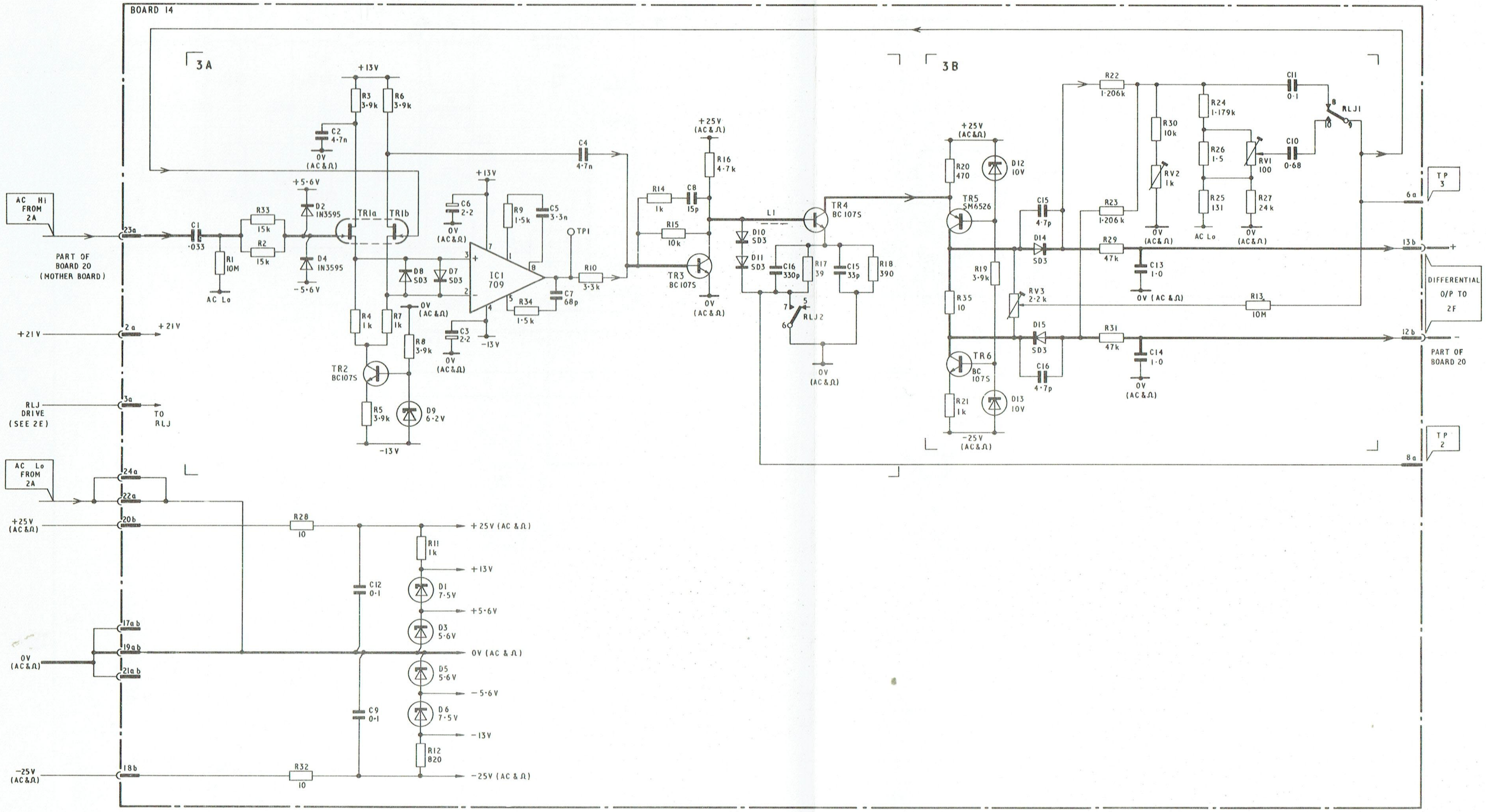
PART OF FLOATING SECTION



3. AC CONVERTER, MEAN SENSING (A211, A213, A233)

3A INPUT AMPLIFIER

The function comprises a differential amplifier, with a frequency shaping stage, TR3, and a driver stage, TR4. The gain of TR4 is increased by a factor 10 when RLJ is energised.

D2 and D4 are for overload protection.

TR2, R5, R8 and D9 is a constant current source for TR1a and TR1b of 1.5ma.

C4 is an ac bypass channel to maintain gain at high frequencies.

3B AC CONVERTER MEAN SENSING

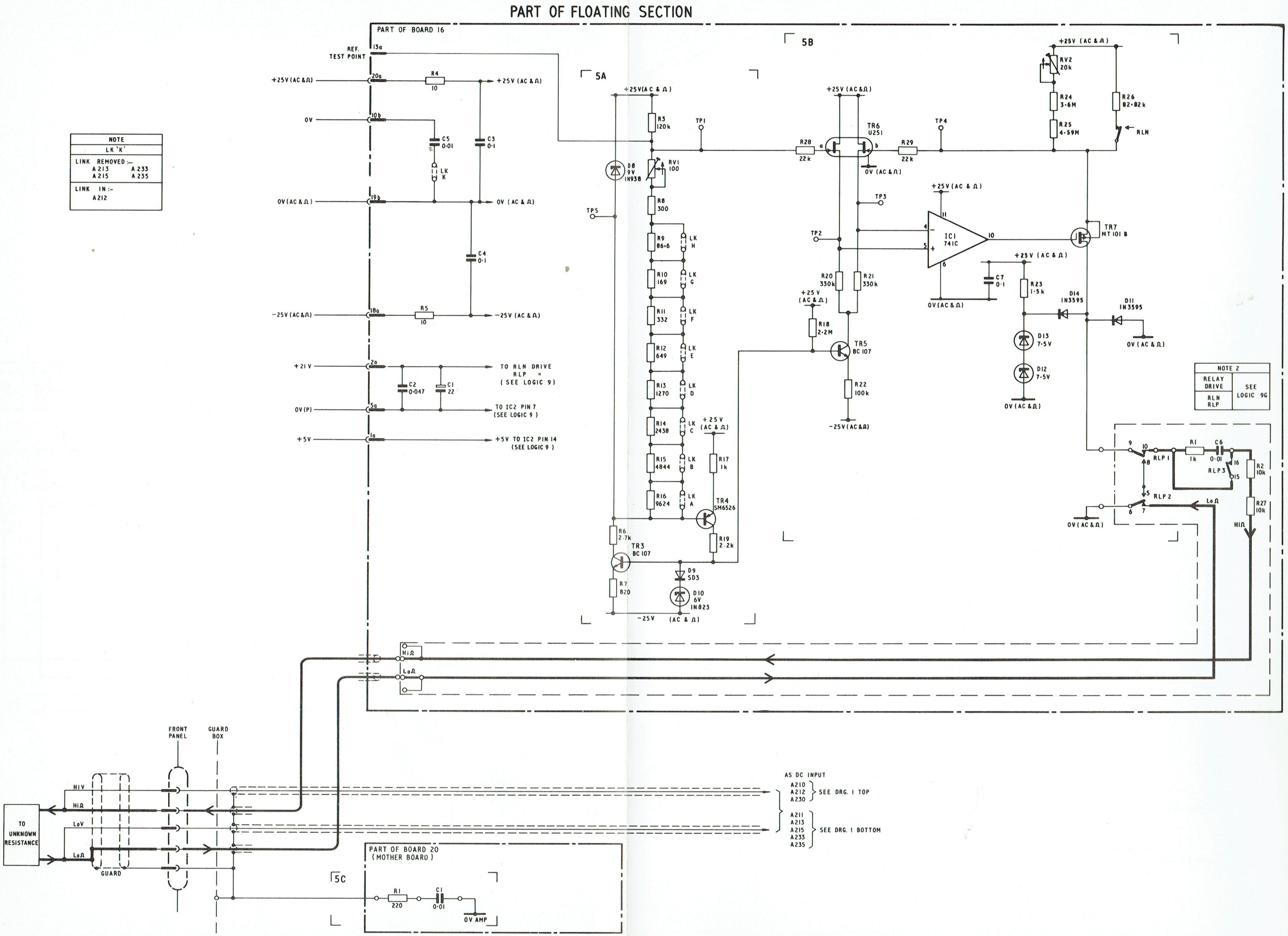
TR5 and TR6 is a current output stage, with D14 and D15 the rectifiers. R29/C13 and R31/C14 are low pass filters for the positive and negative half cycles respectively.

The output is differential and proportional to the mean value of the ac input.

RLJ1 selects two potential divider settings, through C10 and C11, supplying ac feedback to TR1b. The feedback is scaled to give the RMS value of a sine wave input with overall gain of X1 or X10. RV1 and RV2 set the scaling on X10 and X1 gain respectively.

AC Range	RLJ	Adjust
1V	OFF	RV2
100mV	ON	RV1

RV3 sets dc feedback via R13 to TR16 and is set for best linearity.



Ω INPUT

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5

5. Ω INPUT (A212, A213, A215, A233, A235)

Link K	
Made	A212
Removed	A213, A215, A233 and A235

5A VOLTAGE REFERENCE

D9, D10, TR3 and TR4 determine a constant current for zener diode D8. Potential divider R3, RV1, R9 to R16 sets a voltage reference at TR6a gate. LINKS A to H form the primary control for the reference (measuring) current selected* during test, and RV1 is the fine control (100μA).

* LINKS A to H may require resetting. Reference may be made to "A210 Range Tables".

5B CONSTANT CURRENT SOURCE

TR6 and IC1 together make a high input impedance differential amplifier.

This compares the reference voltage with the voltage across the reference resistors RV2, R24, R25 and R26, and sets TR7 gate to pass a reference current so that these voltages are always equal. This is the reference (measuring) current through the unknown resistor.

RV1 sets the reference current to 100μA on the 1kΩ, 10kΩ and 100kΩ Ranges.

RV2 sets the reference current to 1μA.

R18, TR5 and R22 form a constant current source of 60μA, limiting the total current through TR6 to 60μA, with 30μA through each half.

Reference Current

Range	DC Range	Reference Current	RLN
10M	10V	1μA	OFF
1M	1V	1μA	OFF
100k	10V	100μA	ON
10k	1V	100μA	ON
1k	100μV	100μA	ON

D14 and D11are to protect TR7 against voltages on the input leads to max. 15V and min. 0V when the DVM is in the Ω mode.

5C

R1, C1 is a filter for inverter signal pick up on the GUARD BOX.

6. RANGE AND DC FILTER

DRG. 6 shows RELAYS set for DC, 10/SEC, 1kV RANGE, FAST RESPONSE

TABLES

		R	E	L	A Y	S
DC Ranges	**Setting**	**A**	**B**	**C**	**Q(SLOW)**	**Q(FAST)**
1kV	RV1	OFF	OFF	OFF	ON	OFF
100V		OFF	OFF	ON	OFF	OFF
10V	RV5	ON	OFF	OFF	ON	OFF
1V	RV2	ON	OFF	ON	OFF	OFF
100mV	RV3	ON	ON	OFF	ON	OFF
10mV*	RV4	ON	ON	ON	OFF	OFF

RLF: OFF for FAST Response, ON for SLOW Response.

*10mV DC only available for 25/SEC and 100/SEC RATES.

		R	E	L	A Y	S
AC Ranges	**Setting**	**A**	**B**	**C**	**Q(SLOW)**	**Q(FAST)**
All Ranges	See DRG 2	ON	OFF	ON	OFF	OFF

NOTE: RELAYS A, B and C are set for 1V DC.

RLF: OFF for FAST Response, ON for SLOW Response.

		R	E	L	A Y	S
Ω Range	**Setting**	**A**	**B**	**C**	**Q(SLOW)**	**Q(FAST)**
10M Ω		ON	OFF	OFF	ON	OFF
1M Ω	See	ON	OFF	ON	OFF	OFF
100k Ω	DRG 5	ON	OFF	OFF	ON	OFF
10k Ω		ON	OFF	ON	OFF	OFF
1k Ω		ON	ON	OFF	ON	OFF

RLF: OFF for FAST Response, ON for SLOW Response.

6A INPUT ATTENUATOR

R1, R2, R3, R4, R5 and R7 comprise a 100/1 attenuator (with RLA OFF), RV1 setting the 100V and 1000V Ranges; R33, R34 and C5 form an arc suppression circuit for RLA contacts.

6B INPUT AMPLIFIER (See DRG 7)

Input Lo goes to the inverting input, and the output is the same polarity as Input Hi.

6C GAIN

The amplifier gain is set by the resistor network selected by relays RLB 2, RLC 1 and RLC 2.

Gain	RLB 2	RLC 1 and RLC 2
X1	OFF	OFF
X10	OFF	ON
X100	ON	OFF
X1000	ON	ON

6D SCALING

This network determines the 10V Range of the DVM.

LINKS A to J form the primary setting for the 10V Range on all reading rates, and are selected* during test.

RLD	Rate	10V Range Fine Control
OFF	10 and 100/SEC	RV5
ON	25/SEC	RV6

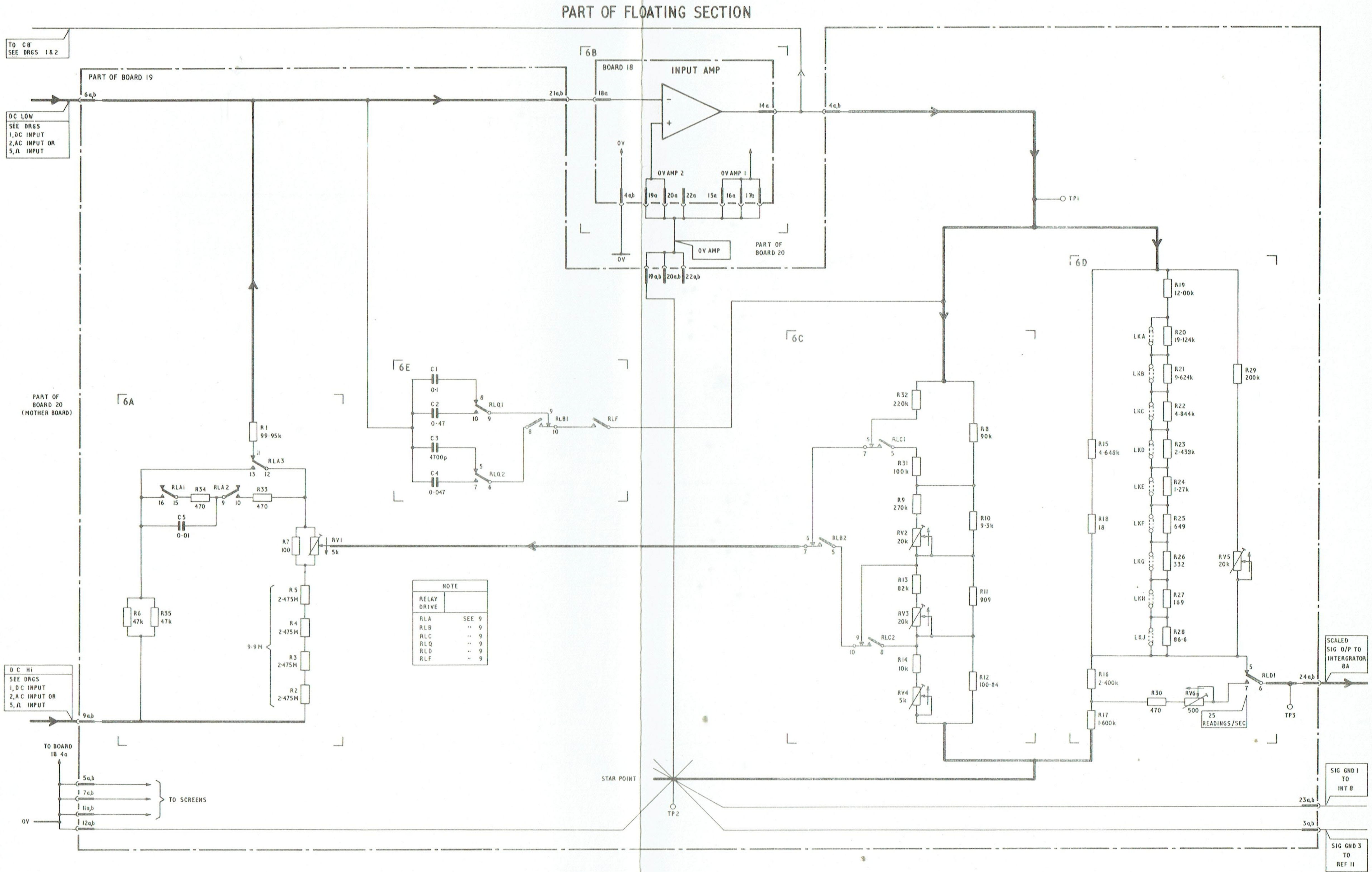
*LINKS A to J may require setting.

Reference may be made to "A210 Range Tables".

6E

RLF is OFF for FAST Response and ON for SLOW Response. RLQ and RLB1 set the appropriate filter capacitors (C1 to C4) as indicated in the Tables.

RLQ is always OFF when RLF is OFF (i.e. FAST Response).



RANGE AND
DC FILTER
6
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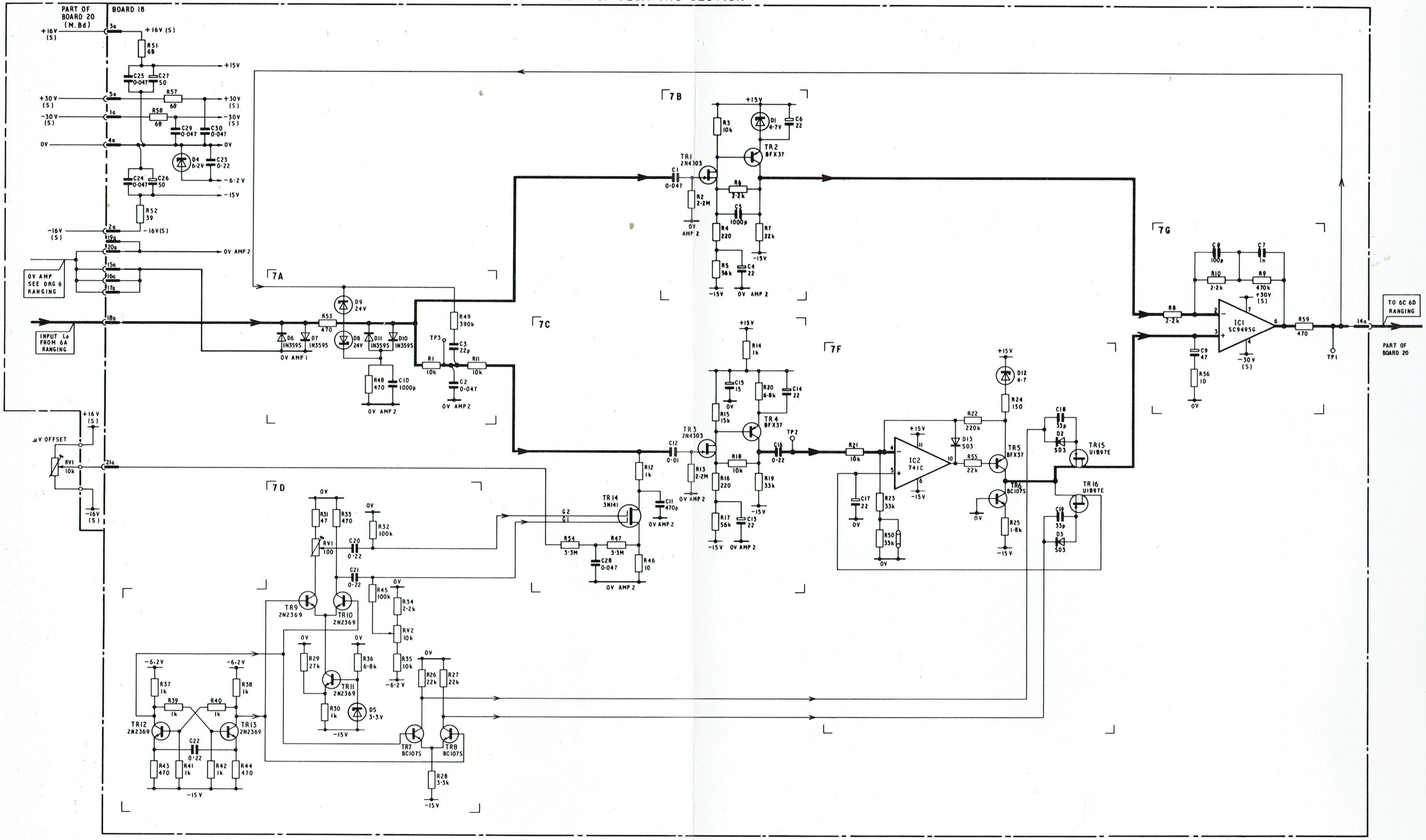
PART OF FLOATING SECTION



INPUT AMPLIFI

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7. INPUT AMPLIFIER

7A

D6, D7 are for overload protection, and D8, D9, D10 and D11 limit amplifier output to $\pm$ 25V (7G).

R1, R11 and C2 form a filter for 2.5kHz (the chopper drive frequency).

7B AC PRE AMPLIFIER

This has a gain of 10 at AC up to 70kHz governed by the impedance of R6, R4 and C5.

7C CHOPPER and DC PRE AMPLIFIER

Chopper drive (from 7D on G1 of TR14 switches it from OFF to ON, shorting chopper input to 0V AMP 2 at 2.5kHz.

Anti-phase Chopper drive to G2 minimises chopper spikes at the input.

The resulting square wave at TR3 gate is amplified by 40, as set by R16, R18 of the DC PRE-AMPLIFIER TR3 and TR4.

7D CHOPPER DRIVE

TR12, TR13 is an emitter coupled multivibrator at 2.5kHz driving differential amplifier TR9, TR10 (for CHOPPER DRIVE) and TR7, TR8 (for DEMODULATOR DRIVE)'

RV2 sets the dc bias on G1 of TR14 and is set for maximum amplitude chopped waveform (approx. 2V peak to peak).

RV1, CHOPPER DRIVE, sets the amplitude of antiphase CHOPPER DRIVE signals at G2 of Chopper TR14 and is set for minimum input current.

7E μV OFFSET.

Front Panel Control.

7F CHOPPER AMPLIFIER AND DEMODULATOR

IC2, TR5 and TR6 is a differential amplifier which compares the voltage on C17 with the output of the DC PRE-AMPLIFIER 7C.

When the chopper is not conducting, TR5 and TR6 output is connected by TR16 to C17, which then charges to the output voltage of the DC PRE-AMPLIFIER.

When the chopper conducts, TR5 and TR6 output defines a current proportional to the voltage of C17 and is connected to the OUTPUT AMPLIFIER (7G) by TR15. During this period, C9 (7G OUTPUT AMPLIFIER) changes at a rate proportional to the DC or low frequency voltage at the input to 7A during the preceeding period of chopper not conducting.

7G OUTPUT AMPLIFIER

C9 stores Demodulator output.

Voltage at 7A input, includes the difference between voltage on C9 and DC offset due to AC PRE-AMPLIFIER and IC1, fed back via the Hi input (See Drg. 6), and DVM input.

8. INTEGRATOR

INPUT SWITCHING. Only one FET switch function can be on at a time.

8A RAMP UP SWITCH

Command is +ve level. TR1 switches on the Scaled Input is fed to the Integrator (8D) for the Ramp Up period.

Ramp Up Time	Rate
40ms	10 /sec
20ms	25 /sec
4ms	100 /sec

8B WAIT SWITCH

Command is a +ve level, TR4 switches on the the Integrator input is grounded to 0V SIG 1.

8C RAMP DOWN SWITCHES

TR1 or TR2, depending on input polarity, are switched on by a +ve level at the end of WAIT, applying the internal reference or external reference (Ratio)* to the Integrator.

DVM Input	Reference	Switch ON
–ve	+ve	TR2
+ve	–ve	TR3

RV9 (Board 11) sets equal +ve and –ve Internal Reference Inputs
RV8 (Board 11) sets equal +ve and –ve External Reference (Ratio)*

*As fitted on A230, A233 and A235.

Ramp Down Time	Rate
0 - 40ms	10 /sec
0 - 8ms	25 /sec
0 - 4ms	100 /sec

8D INTEGRATOR

Integrates the Scaled Input and the Reference. C10 is the integrator capacitor and R10 the input resistor.

TR9, TR11 and IC1 make a low noise, low input current, high gain differential amplifier.

TR10 is a constant current source for TR9.

TR9a is the inverting input and TR9b the non-inverting input from 8J (Drift Correct).

8E

This stage is a X10 inverting amplifier. The gain is set by R23 and R29.

D7, D8, D9 and D10 limit the output swing to 8F and 8J.

8F COMPARATOR

IC3 is a high speed, high gain amplifier.

1. Signal polarity is detected at the output of IC2 (referred to Signal Ground), during the WAIT period.

2. End of Ramp Down is detected when IC2 output equals the +ve or −ve applied offset.

An adjustable dc offset (set by RV1, 8G) is also applied to the non inverting input to IC3. This balances initial amplifier offsets. RV1 is set (with 0V input to the DVM) to give equal + and − polarity decisions.

8G OFFSET

TR16 switches the +ve Reference (-ve DVM inputs) and TR17 switches the -ve Reference (+ve DVM inputs) to potential dividers, which apply a small offset (approx. 30 digits on the display) to the Comparator input, allowing the Integrator output to go beyond zero before end of Ramp Down is detected.

RV1 sets COMPARATOR offset (Zero on 10V Range DC).
RV6 sets +Internal Ref. offset on −ve inputs (DC).
RV7 sets −Internal Ref. offset on +ve inputs (DC).
RV4 sets + External Ref. offset on −ve inputs } RATIO*
RV5 sets −External Ref. offset on +ve inputs }

*As fitted on A230, A233 and A235.

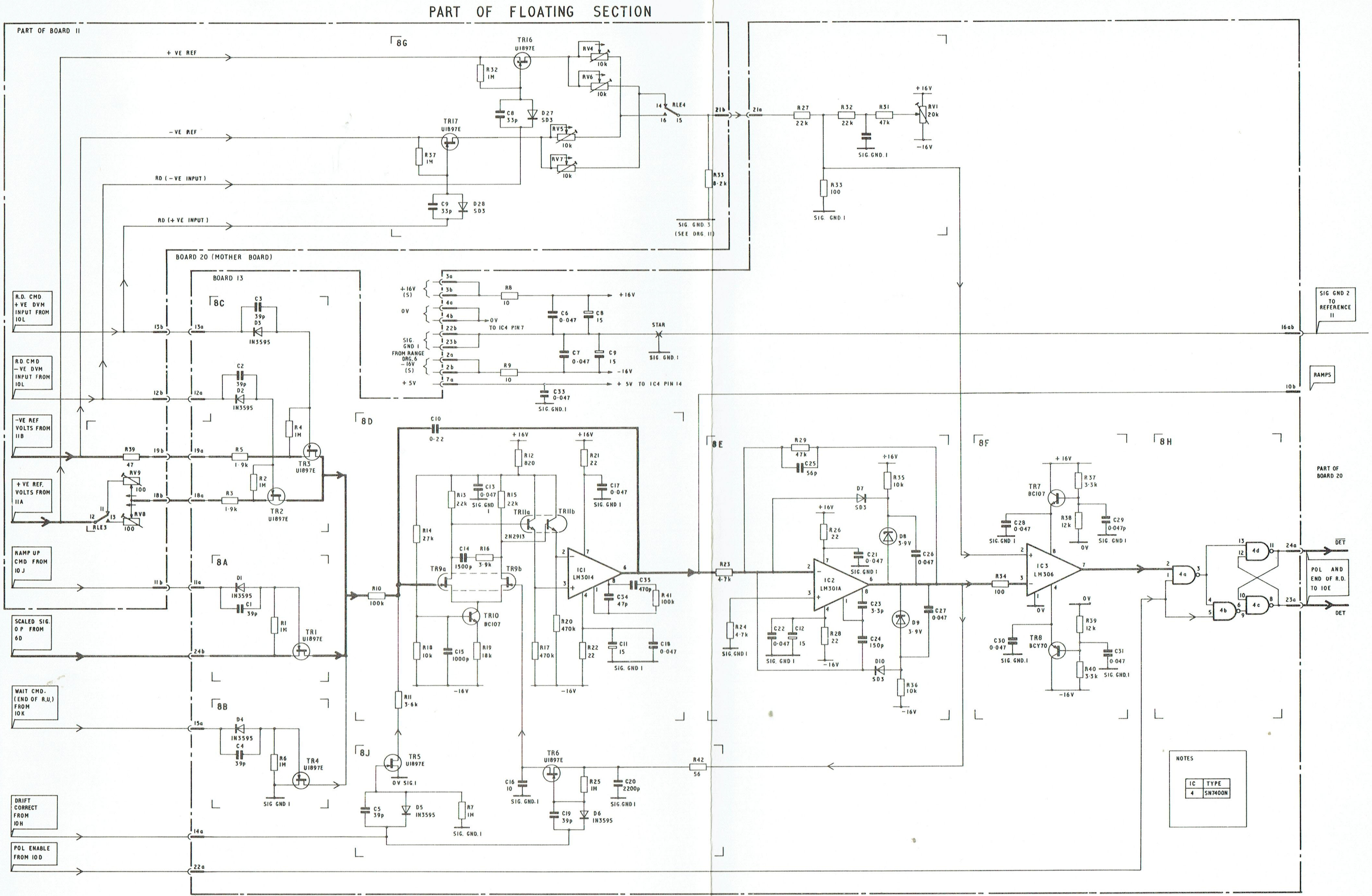
8H

Polarity and End of Ramp Down are detected by the COMPARATOR (8F) and buffered by IC4. Polarity decision is made at the end of t1 (see 10D and POLARITY ENABLE waveform).

DVM Input	IC4a	DET	$\overline{\text{DET}}$
+ve	Hi Lo pulse at end RD	Hi Lo at end RD	Lo Hi at end RD
	IC4b		
−ve	Hi Lo pulse at end RD	Lo Hi at end RD	Hi Lo at end RD

8J DRIFT CORRECT

At end of Ramp Down until start of Ramp Up, TR9a is connected to 0V SIG 1, TR5 being on; TR6 is also on for this period and connects the X10 AMPLIFIER (8E) output to C16, which charges to the offset error of the Integrator and X10 AMPLIFIER and is applied to the Integrator at TR9b as a correction during Ramp Up and Ramp Down.



INTEGRATOR 8

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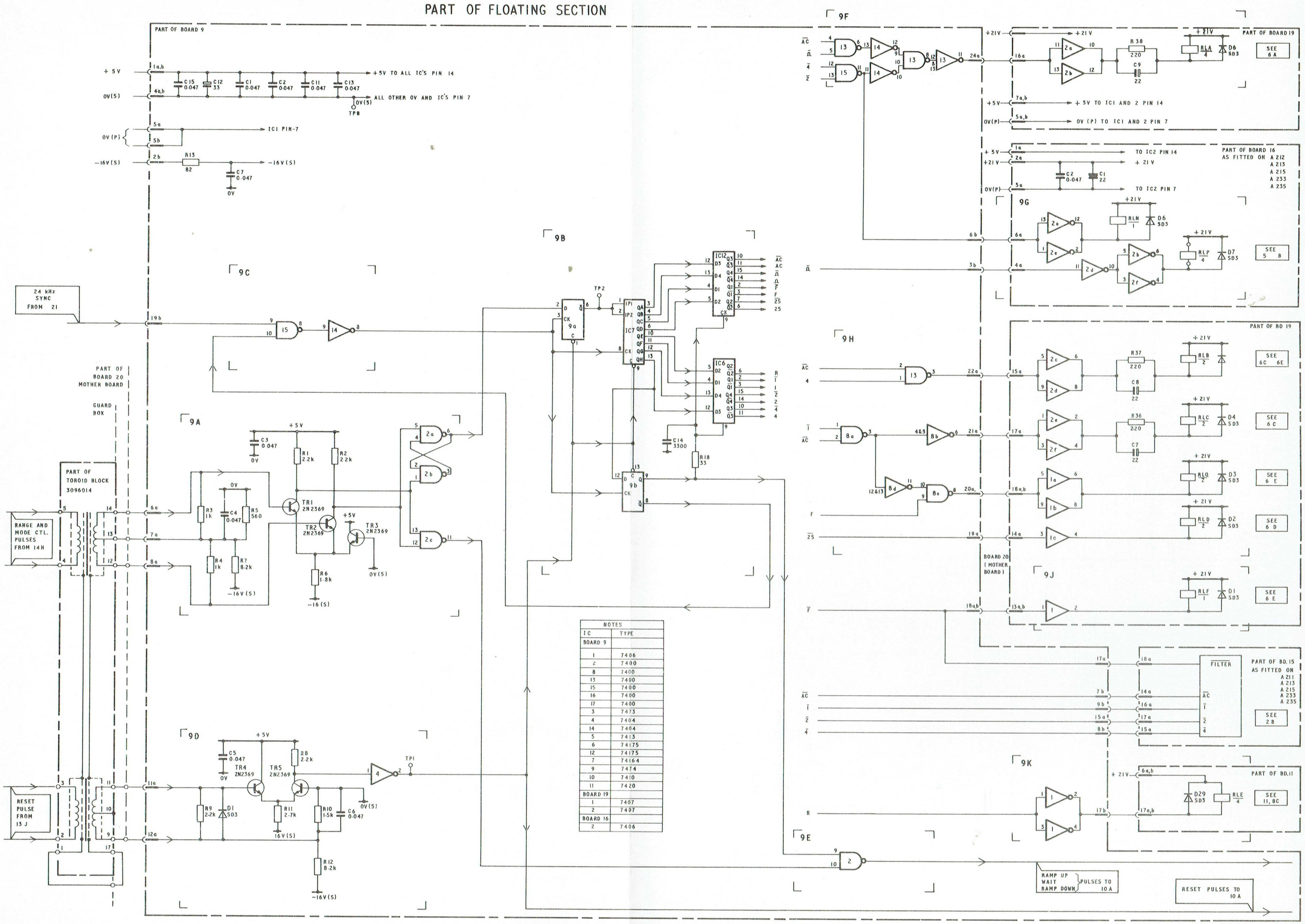


NOTES

IC	TYPE
BOARD 9	
1	7406
2	7400
8	7400
13	7400
15	7400
16	7400
17	7400
3	7473
4	7404
14	7404
5	7413
6	74175
12	74175
7	74164
9	7474
10	7410
11	7420
BOARD 19	
1	7407
2	7407
BOARD 16	
2	7406

CONTROL RECE
RANGE & MOD

A2107009 01

9. CONTROL RECEIVER, RANGE & MODE DECODE

9A CONTROL RECEIVER

Information is received as +ve and -ve (100ns) pulses, via the toroid transformer, from the Earthy Section. This is converted to logic levels by TR1, TR2, TR3 and IC2. A +ve going pulse at TR1 base results in the latch (2a/2b being set to Lo at 2a. A +ve going pulse at TR2 base results in the latch being set Hi at 2a. Range and mode data, received during the RESET period is fed to 9B, 9E being inhibited during RESET.

Ramp Up, Wait, Ramp Down and Drift Correct signals are fed to 9E. 9B input is inhibited after RESET.

9B RANGE AND MODE REGISTER

Range and Mode data at IC9a is clocked by the 24kHz SYNC to the Range and Mode register, IC7, through 9a $\overline{Q}$ during RESET.

The 9th clock edge transfers the Hi at 9b from D to Q, and via delay R18/C14 to IC6 and IC12, when the Range and Mode data is staticised as outputs to the relay drive logic (9F, 9G, 9H, 9J, 9K and 2B); this remains unchanged until range and mode are changed.

At this time, IC15 gate (9c) inhibits the 24kHz SYNC from reaching the range and mode register and IC2 gate (9E) passes control pulses (Ramp Up, Wait, Ramp Down) to Control Counter (See 10A).

9C SYNC GATE

	IC15 Pin 10)
OPEN (during RESET)	Hi
CLOSED (from start Ramp Up to start RESET)	Lo

9D RESET

A +ve going pulse (100ns) switches TR4 ON. TR5 collector goes Hi, IC4 pin 2 is set Lo resetting the Range and Mode registers IC9, IC7 to Lo.

The Lo output to Control Counter (10A) sets Q1 and Q2 Lo, if this setting has not already occurred.

9E

The Hi from 9B opens the gate (9th SYNC edge, end of RESET) and the output from 9A (IC2c) is fed to 10A, which starts the measuring cycle (Ramp Up to the start of Reset).

9F to 9K and 2A

See Range and Mode Table.

RANGE AND MODE TABLE

Relays	DC Ranges			Rate	Ratio	Filters			
	A	B	C	D	E	F		Q	
						FAST	SLOW	FAST	SLOW
DC									
1000V	OFF	OFF	OFF			OFF	ON	OFF	ON
100V	OFF	OFF	ON			OFF	ON	OFF	OFF
10V	ON	OFF	OFF			OFF	ON	OFF	ON
1V	ON	OFF	ON			OFF	ON	OFF	OFF
100mV	ON	ON	OFF			OFF	ON	OFF	ON
10mV	ON	ON	ON			OFF	ON	OFF	OFF
AC									
1000V	ON	OFF	ON			OFF	ON	OFF	OFF
100V	ON	OFF	ON			OFF	ON	OFF	OFF
10V	ON	OFF	ON			OFF	ON	OFF	OFF
1V	ON	OFF	ON			OFF	ON	OFF	OFF
100mV	ON	OFF	ON			OFF	ON	OFF	OFF
Ω									
10M	ON	OFF	OFF			OFF	ON	OFF	ON
1M	ON	OFF	ON			OFF	ON	OFF	OFF
100k	ON	OFF	OFF			OFF	ON	OFF	ON
10k	ON	OFF	ON			OFF	ON	OFF	OFF
1k	ON	ON	OFF			OFF	ON	OFF	ON
RATE									
10 & 100/SEC				OFF					
25/SEC				ON					
RATIO*									
RATIO					ON				
$\overline{\text{RATIO}}$					OFF				

*Not on 100/SEC

Relays	AC Ranges				AC Filter		AC/DC Mode		Ω Range	Ω Mode	
	G	H	R	J	K		L	M	N	P	S^{+}
					FAST	SLOW					
DC											
1000V	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	
100V	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	
10V	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	
1V	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	
100mV	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	
10mV	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	
AC											
1000V	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	
100V	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	
10V	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	
1V	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	
100mV	ON	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	
Ω											
10M	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	
1M	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	
100k	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	
10k	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	
1k	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	
RATE											
10 & 100/SEC											
25/SEC											
RATIO*											
RATIO											OPERATING
$\overline{\text{RATIO}}$											OFF

+See Drg. 12 (RATIO as fitted on A230, A233, A235).

*Not on 100/SEC

10. INTEGRATOR CONTROL LOGIC

10A CONTROL COUNTER

Times the Q1, Q2 outputs which control the measuring cycle.

Period	FET Drive	Q1	Q2
Drift Correct & Reset	10H	0	0
Ramp Up	10J	1	0
Wait	10K	0	1
Ramp Down			
+VE Input	10L	1	1
-VE Input		1	1

10B WAIT

Generates a delay, t1 (Lo pulse of approx. 16μs) at end of Ramp Up, during which DVM Input Polarity is detected (8H).

Time constant of R15 and C9 delays Q2 (set Hi at End of Ramp Up) reaching IC5a resulting in a Lo pulse, t1 at IC5a output to 10D and 10E.

TP4 is Hi during the Wait Period after t1 and during Drift Correct and Reset.

Total Wait period is approx. 40μs.

10C RAMP DOWN DELAY

Generates a delay, t2 (Lo pulse of approx. 6μs) at the start of Ramp Down Command to INTEGRATOR (8C). Time constant R14 and C8 delays Q1 (set Hi to start Ramp Down) reaching IC5b, resulting in IC5b output remaining Hi for duration t2 and then Lo until Drift Correct and Reset.

IC10 output is a Lo during Ramp Down, after t2.
Output at TP3 is a Hi pulse during t2.
Output at TP5 is a Hi during Ramp Down.

10D POLARITY ENABLE GATE

The output for the measurement cycle is:

Ramp Up	Lo
Wait during t1	Hi (polarity decision)
Wait after t1	Lo
Ramp Down during t2	Lo
Ramp Down after t2	Hi
Drift Correct & Reset	Lo

10E POLARITY STORE

t1 delay pulse is inverted at 14a to Hi, enabling 16a and 16b. During t1, 16c and 16d store the polarity on the D and $\overline{D}$ lines.

Stored output to 10F and 10L

DVM Input	16c($\overline{D}$)	16d(D)
+ve	0	1
-ve	1	0

Detected polarity, inverted by 14b and 14c is an output to 10F.

10F

Both outputs are Hi until End of Ramp Down. Either IC10a or 10b output is a Lo pulse until start of Drift correct, when TP5 goes Lo.

DVM Input	10a O/P	10b O/P
+ve	0	1
- ve	1	0

10G POLARITY, START AND END RAMP DOWN TO EARTHY SECTION

1. Polarity. 17b, 17c are enabled (TP4 output from 10c) during Wait after t1.

DVM Input	1a O/P	1b O/P
+ve	0	1
-ve	1	0

2. Ramp Down Starts. 17a, 17b enabled (during t2)

DVM Input	1a O/P	1b O/P
+ve	1	0
- ve	0	1

3. End of Ramp Down. Lo Pulse from 10a (+ve DVM Input) or 10b (-ve DVM Input).

DVM input	1a O/P	1b O/P
+ve	0	1
- ve	1	0

10H 10J 10K 10L

Each function is a current mode FET level switch. When all inputs to each pair (or group of three) diode gates are Hi, the output to the relevant FET gate is also Hi.

10H DRIFT CORRECT

$\overline{Q1}$	$\overline{Q2}$	TP1
1	1	1
When any one input Lo		0

10J RAMP UP

Q1	$\overline{Q2}$	TP2
1	1	1
When any one input Lo		0

10K WAIT

$\overline{Q1}$	Q2	TP3
1	1	1
When any one input Lo		0

10L RAMP DOWN

-ve DVM Input

Q1	Q2	$\overline{D}$	TP4
1	1	1	1
When any one input Lo			0

+ve DVM Input

Q1	Q2	D	TP5
1	1	1	1
When any one input Lo			0

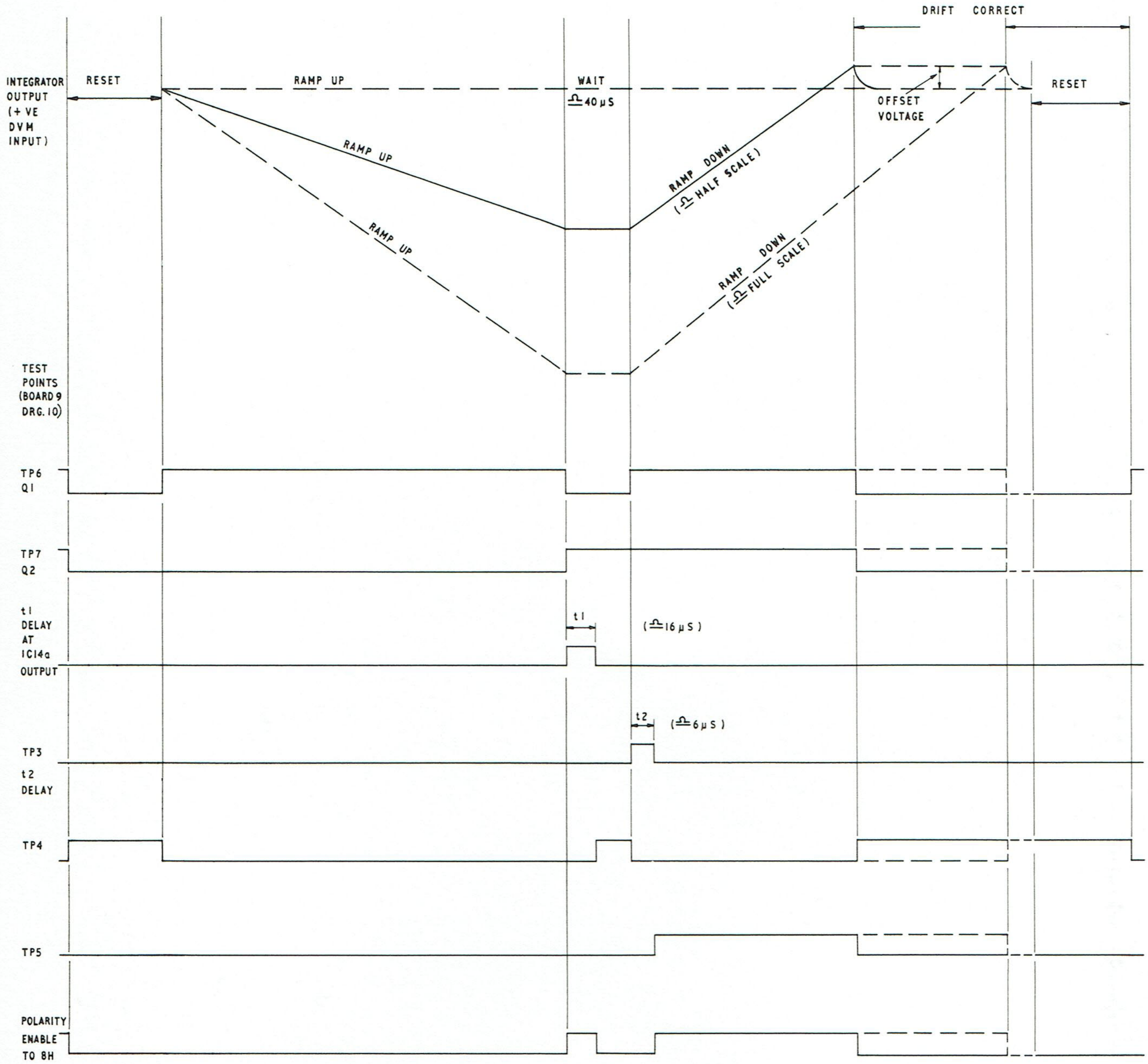
10M

'X', +12V

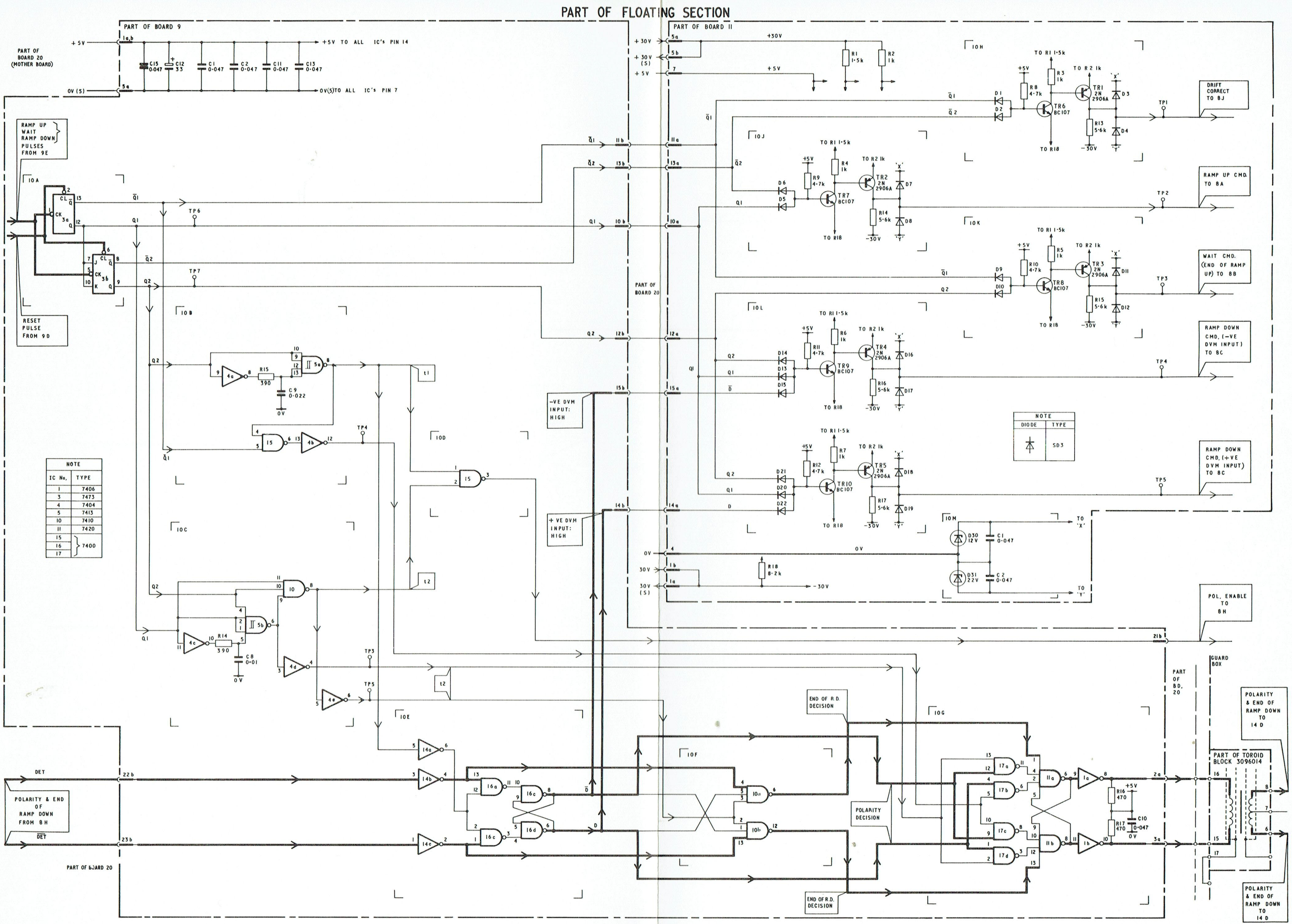
'Y', −22V

This limits the voltage level applied to the FET gates (DRG 8).

INTEGRATOR CONTROL TIMING



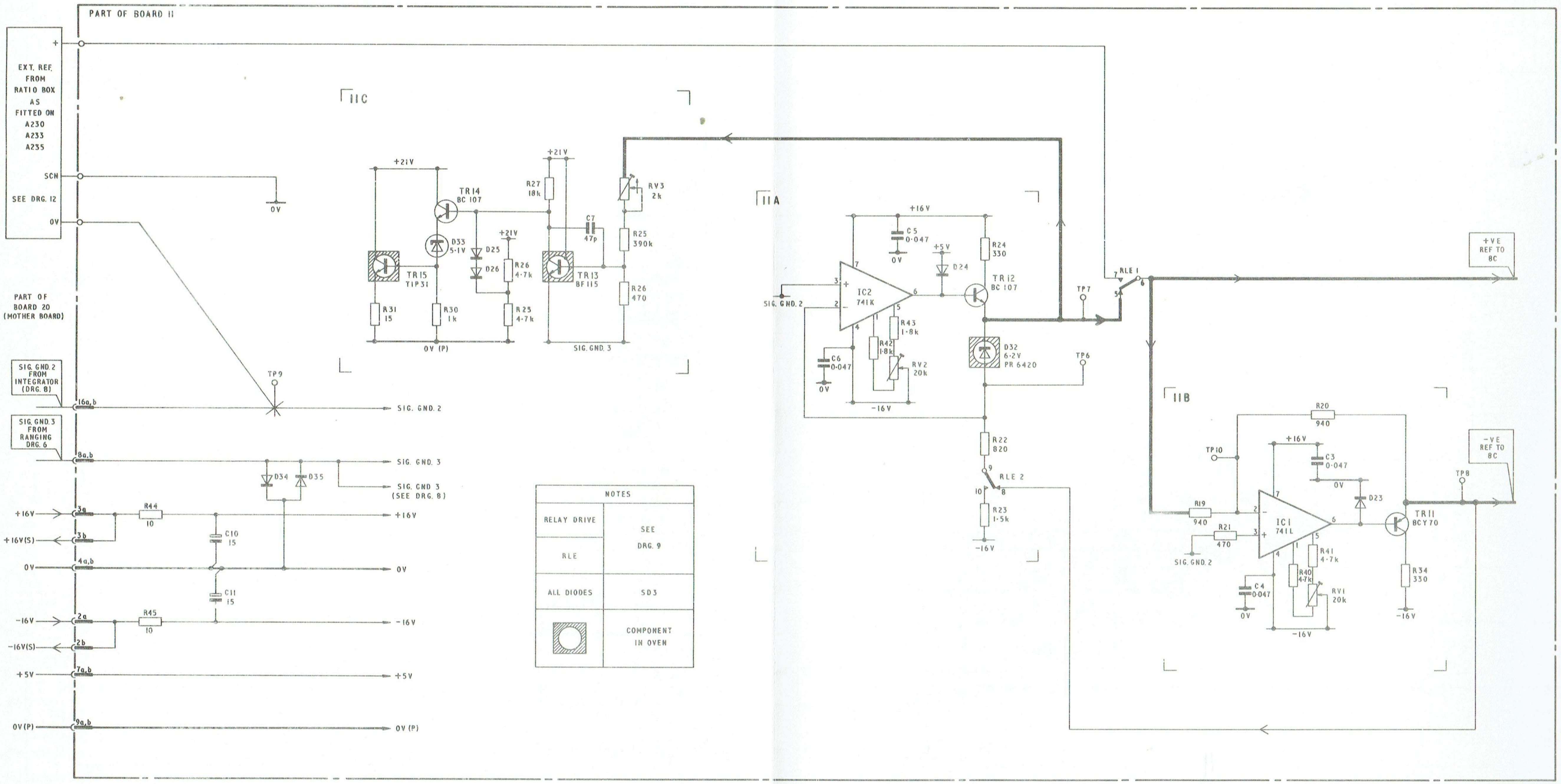
NOT TO SCALE



INTEGRATOR CONTROL LOGIC **10**

A2107010 01

PART OF FLOATING SECTION



11. REFERENCE

11A REFERENCE SOURCE (INTERNAL)

D32 is the reference zener which, with IC2 and TR12 provide a reference output of +6.2Volts. The –ve Reference Voltage from 11B (IC1) across R22 defines the zener current.

RV2 sets the zero output level of IC2 and is adjusted for minimum reading at TP6.

D32 has been aged for more than 600 hours by the manufacturer, at the operating current of 7.5mA.

11B

IC1 has unity gain and inverts the +ve Reference input to provide the -6.2 Volts Reference output. This also provides the feedback to 11A (IC2).

RV1 sets the zero output level of IC2 and is adjusted for minimum reading at TP10.

11C TEMPERATURE CONTROLLED OVEN

TR13, TR15 and D32 are in the same oven enclosure.

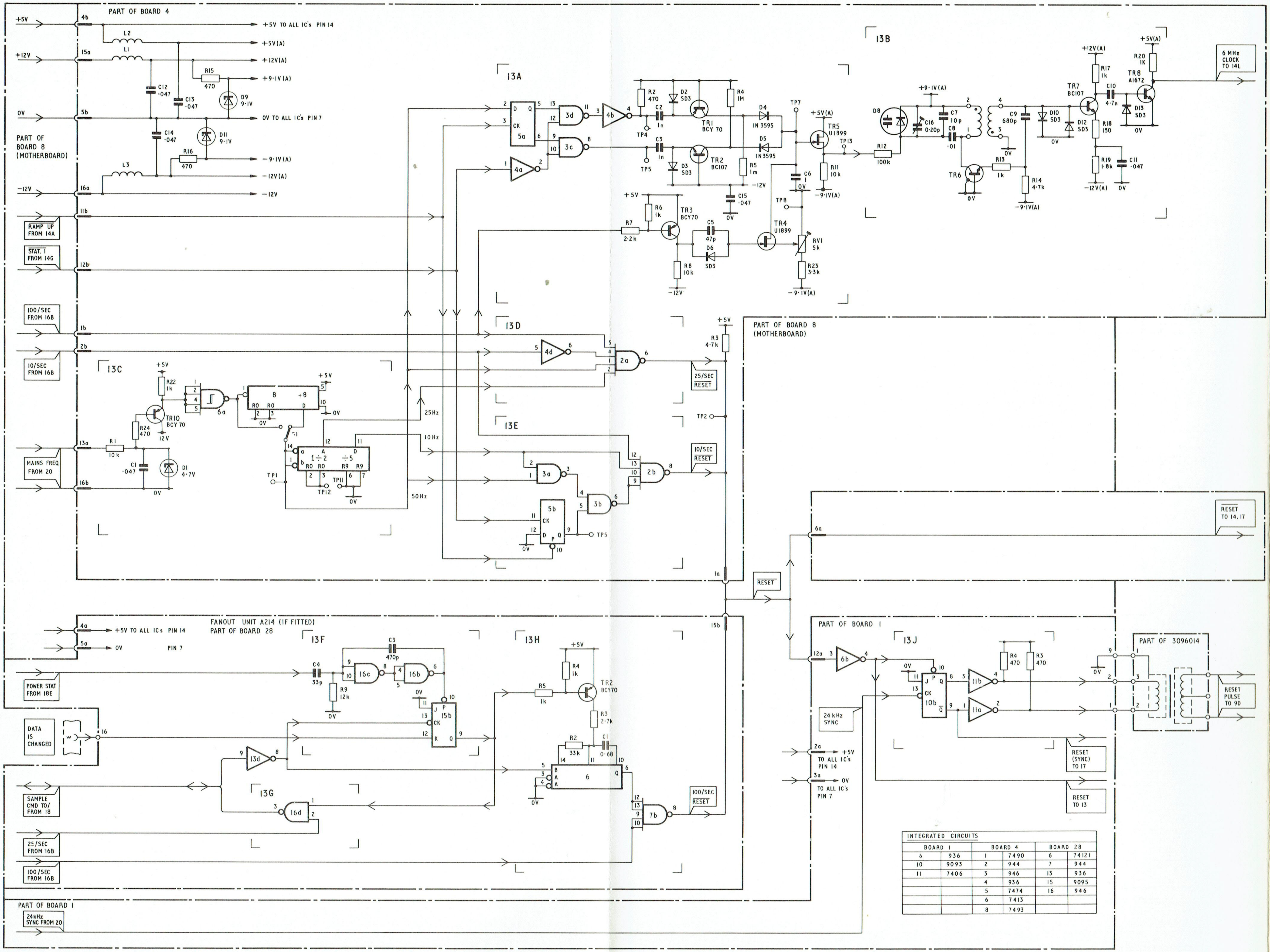
RV3 sets the oven temperature ($80^{o}C \pm 1^{o}C$).

The potential divider RV3, R25 and R26 defines a control voltage to the base of TR13, which acts as a temperature sensor and error amplifier.

Thus at switch on, TR13 collector current is zero, TR14 and TR15 (the oven heater) are ON. As the oven temperature rises TR13 conducts, TR14 base voltage goes low and TR15 heating current falls until the control setting is reached.

RLE	
OFF	Internal Reference
ON	External Reference (Ratio*)

*As fitted on A230, A233 and A235.



INTEGRATED CIRCUITS					
BOARD 1		BOARD 4		BOARD 28	
6	936	1	7490	6	74121
10	9093	2	944	7	944
11	7406	3	946	13	936
		4	936	15	9095
		5	7474	16	946
		6	7413		
		8	7493		

CLOCK OSCILLA AND RESET

A2107013 01

13. CLOCK OSCILLATOR AND RESET

13A CLOCK FREQUENCY CONTROL

At the end of Ramp Up $\overline{\text{RAMP UP}}$ goes high clocking IC5a and the level on the 50Hz input will be stored. If the clock frequency is high end of Ramp Up will occur before the 50Hz input goes low and the Q output will go high. For a low clock frequency the $\overline{\text{Q}}$ output will go high.

The $\overline{\text{STAT 1}}$ pulse at the end of Ramp Down enables IC3d and IC3a and for a high clock frequency TP4 pulses low, and for a low clock frequency TP3 pulses high. These pulses are differentiated by C2 or C3 to add or subtract a small charge to/from C6. Thus the voltage on C6, buffered by TR5 will increase for high clock frequencies and decrease for low clock frequencies.

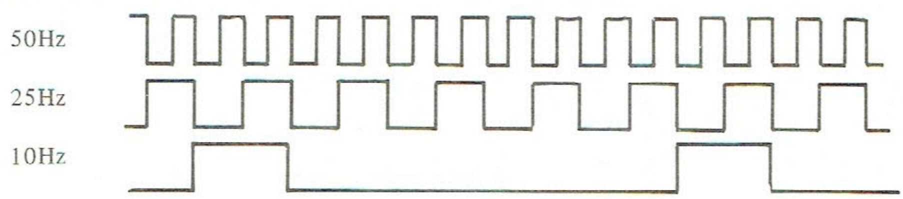
During 100/SEC operating the clock frequency is not mains locked. TR4 is turned on, and the voltage on C6 (and the clock frequency) is set by RV1.

13B CLOCK OSCILLATOR

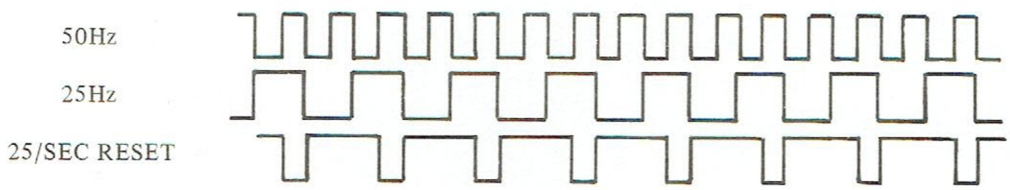
The output of 13A controls the frequency of the 6MHz oscillator TR6 via varactor diode D8. The output is buffered by TR7 and TR8.

13C

The MAINS FREQ. input is squared by TR10 and IC6a. S1 is set to give a 50Hz input to IC1 (50Hz of 400Hz operation). IC1 outputs are at 25Hz and 10Hz.



13D 25/SEC RESET



13E 10/SEC RESET

During normal operation the 10Hz input is inverted. To ensure that the instrument starts in the right state at switch-on IC5b inhibits RESET if STAT 1 does not occur until the output of 3a is gated on as a $\overline{\text{RESET}}$.

13F

If DATA IS CHANGED is high (Data Changed), the trailing edge of the low $\overline{\text{SAMPLE CMD}}$ pulse clocks 13F output high. The output is reset low by the trailing edge of POWER STAT.

13G

During 25/SEC operation, if DATA IS CHANGED $\overline{\text{SAMPLE CMD}}$ is held low until POWER STAT (for the previous reading) occurs.

13H 100/SEC RESET

100/SEC operation reset is initiated by $\overline{\text{SAMPLE CMD}}$, which triggers monostable IC6. If DATA is not CHANGED the Reset period is approximately 1ms.

If DATA is CHANGED the Reset period is approximately 15ms.

13J

IC10 synchronises the start of RESET PULSE sent to the Floating Section with the 24kHz SYNC signal. The first low going edge of 24kHz SYNC clocks IC11b output high. At the end of the Reset period IC11b output is reset low.

14. RAMP UP/RAMP DOWN CONTROL

14A

Output is low during Reset and when 119999 is detected (end of Ramp Up and Overload).

14B

At the end of Reset IC1a C input is released and IC10a output will be high. The next 3MHz input clocks $\overline{\text{RAMP UP}}$ low, sending a start Ramp Up signal to the Floating Section via 14H. When 119999 is detected (end of Ramp Up) $\overline{\text{RAMP UP}}$ is set high until the end of the next Reset. IC10c output is high during Reset and Ramp Up.

14C

40μs Wait period monostable IC11 is triggered by end of Ramp Up. The leading edge of low pulse $\overline{\text{WAIT}}$ ends Ramp Up via 14H.

14D

Polarity and end of Ramp Down receiver.

14E

At the end of Reset IC16a output will be high, RAMP DOWN CMD will be low and $\overline{\text{RAMP DOWN}}$ will be high. At the end of the low $\overline{\text{WAIT}}$ pulse IC16a output and RAMP DOWN CMD will be low. The next 3MHz input clocks RAMP DOWN CMD high giving a Ramp Down command to the floating section via 14F and 14H. Then a Ramp Down has started signal (polarity information) from 14D clocks $\overline{\text{RAMP DOWN}}$ low and IC16a output high.

The next 3MHz input clock RAMP DOWN CMD low, and when end of Ramp Down is received from 14D $\overline{\text{RAMP DOWN}}$ is clocked high. If an overload occurs $\overline{\text{RAMP DOWN}}$ is set high when 119999 is detected. IC8d output goes low between Ramp Down has started and when RAMP DOWN CMD goes low.

14F

Gates via 14H start Ramp Up to the Floating Section and ensures that the Floating Section is reset if Ramp Down does not occur.

14G

At the end of Ramp Down $\overline{\text{RAMP DOWN}}$ goes high, gating one low 24kHz SYNC. pulse to the output of IC13d ($\overline{\text{STAT 1}}$). This is a start Drift Correct command to the Floating section.

14H

Transmits the serial Range and Mode information (during the reset period) and Ramp Up/Ramp Down commands to the Floating Section.

	IC14f Output goes to:	IC14e Output goes to:
Start Ramp Up	Lo	High
End Ramp Up	High	Lo
Start Ramp Down	Lo	High
Start Drift Correct	High	Lo
Reset Period	Range and Mode Information.	

14J

$\overline{\text{RAMP DOWN CMD}}$ reset IC7a and 7b $\overline{Q}$ low. The output of IC16b in 14E sets $\overline{\text{OFFSET}}$ low. $\overline{\text{RAMP DOWN}}$ going low enables the clock to the MAIN COUNTER on DRG. 15 via 14M and the COUNTER OUTPUT 8_0 clocks 14J. The third 8_0 pulse (30 bits) takes $\overline{\text{OFFSET}}$ high and releases COUNTER RESET 2 via 14K.

14K

COUNTER RESET 1 is high (Reset):

i) During the Reset period,
ii) From the start of the wait period until RAMP DOWN goes low (Ramp Down has started).

COUNTER RESET 2 is high (Reset):

i) During the Reset period
ii) From the start of the Wait period to the end of Offset.

14L

Divides the 6MHz CLOCK by 2 to provide pulses to operate the control logic.

14M

The 3MHz output occurs:

i) During Ramp Up
ii) From the receipt of Ramp Down has started until end of Ramp Down is received (or an overload is detected).

14N

During 25/SEC operation, the 25/SEC CLOCK is

i) 600kHz during Ramp Up
ii) 1.5MHz from the end of the Offset period until end of Ramp Down is received (or an overload is detected).

14P

During Ramp Down, after the Offset period, the GATED CLOCK output is

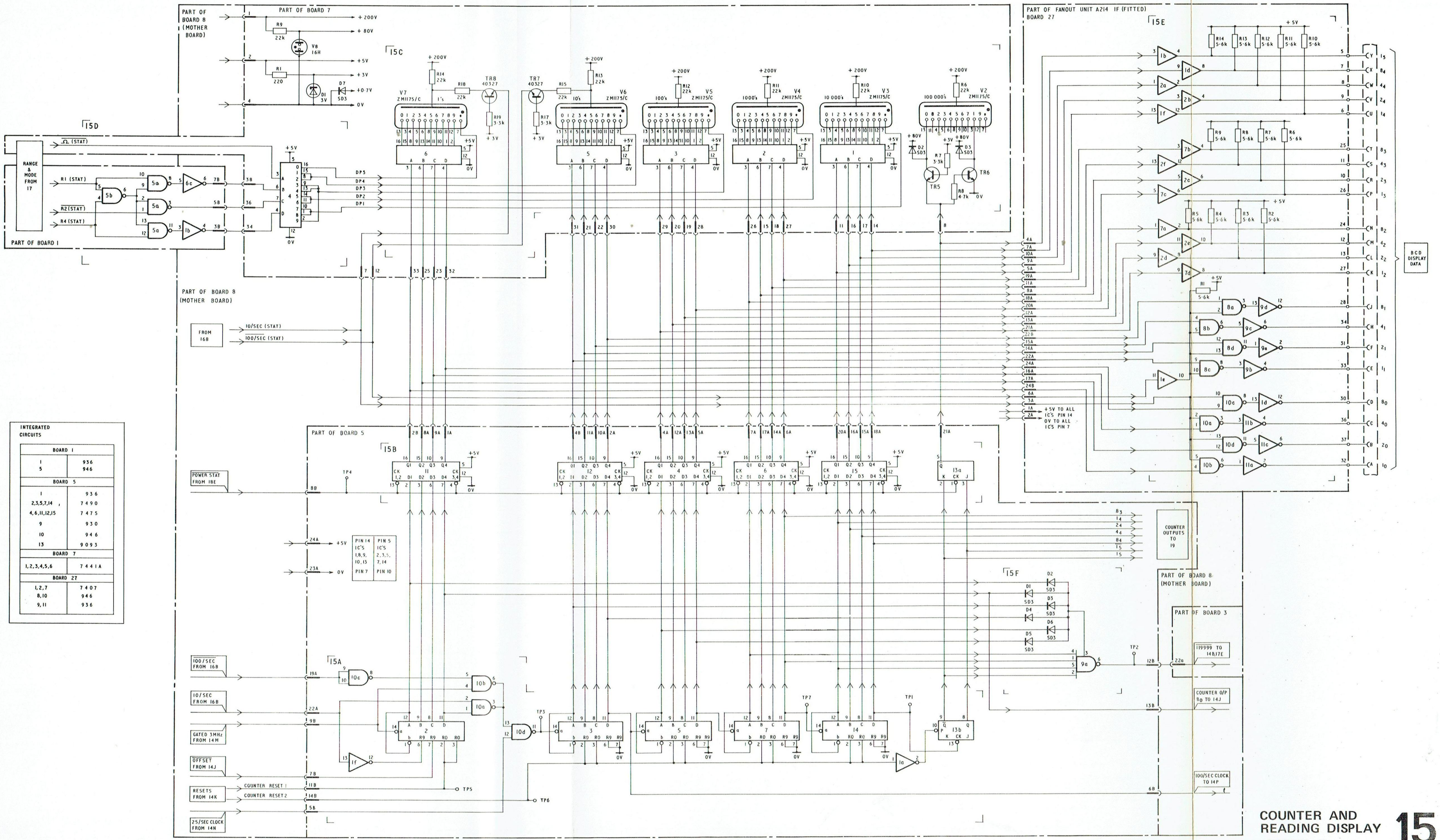
10/SEC	3MHz
25/SEC	1.5MHz
100/SEC	300kHz

INTEGRATED CIRCUITS

BOARD 1		BOARD 3		BOARD 4		BOARD 28	
13	930	1,15	7473	4	936	7	944
14	7406	2,10	7400	7	7473	5,13	936
		3	7404			11	962
		7,12,13,14	9093			12	7490
		8,13	946			14	946

RAMP UP/RAMP DOWN CONTROL **14**

A2107014 01



BOARD 1	
1	936
5	946
BOARD 5	
1	936
2,3,5,7,14	7490
4,6,11,12,15	7475
9	930
10	946
13	9093
BOARD 7	
1,2,3,4,5,6	7441A
BOARD 27	
1,2,7	7407
8,10	946
9,11	936

COUNTER AND READING DISPLAY **15**

A2107015 01

15. COUNTER AND READING DISPLAY

15A MAIN COUNTER

i) 10/SEC Operation

a) Ramp Up: GATED 3MHz pulses are accumulated until all the counter outputs go high and 119999 is detected.

b) Ramp Down: COUNTER RESET 1 resets IC2 from end of Ramp Up until Ramp Down has started.

COUNTER RESET 2 resets IC1, 3, 5, 7, 14 and 13b during the 10μs Offset period. At the start of the Offset period the GATED 3MHz pulses appear, and when COUNTER OUTPUT 8_0 goes low for the 3rd time (30 pulses counted) COUNTER RESET 2 is released, enabling the rest of the counter.

ii) 25/SEC Operation

a) Ramp Up: $\overline{\text{OFFSET}}$ is high and therefore IC2 is reset to BCD9 output. The 25/SEC 600kHz Ramp Up CLOCK pulses are accumulated until all the counter outputs go high and 119999 is detected (11999 pulses).

b) Ramp Down: COUNTER RESET 1 resets IC2 from the end of Ramp Up until Ramp Down has started.

COUNTER RESET 2 resets IC3, 5, 7, 14 and 13b during the 10μs Offset period, which is ended as in 10/SEC operation. At the end of the Offset period IC2 is reset to BCD9 output, and the rest of the Counter accumulates the 25/SEC 1.5MHz Ramp Down CLOCK pulses.

iii) 100/SEC Operation

a) Ramp Up: $\overline{\text{OFFSET}}$ is high and therefore IC2 is reset to BCD9 output. The GATED 3MHz pulses via IC10b are accumulated in the rest of the counter until 119999 is detected (11999 pulses).

b) Ramp Down: COUNTER RESET 1 resets IC2 from the end of Ramp Up until Ramp Down has started.

COUNTER RESET 2 resets IC3, 5, 6, 14 and 13b during the Offset period, which is ended as in 10/SEC operation. At the end of the 10μs Offset period IC2 is reset to BCD9 output, and the rest of the counter accumulates the GATED 3MHz pulses via IC10b.

15B MAIN STATICISOR

Counter outputs are staticised by POWER STAT at the end of Ramp Down if a reading is required.

15C READING DISPLAY

V7 is disabled during 25/SEC and 100/SEC operation

V6 is disabled during 100/SEC operation

15D DECIMAL POINT DECODE

Range	DP1	DP2	DP3	DP4	DP5
1000V				0	
100V			0		
10V		0			
1V	0				
100mV			0		
10mV		0			

Range	DP1	DP2	DP3	DP4	DP5
10M					0
1M				0	
100k			0		
10k		0			
1k	0				

15E DISPLAY DATA BUFFERS

1's outputs are low for 25/SEC and 100/SEC operation.
10's outputs are low for 100/SEC operation.

15F 119999 DETECTOR

Output goes low when 119999 is detected for the end of lamp Up or if an overload occurs for Ramp Down.

16. RANGE, MODE, RESPONSE AND RATE COMMANDS

16A CONTROL

Front Panel	$\overline{\text{CMD REMOTE}}$	REM	$\overline{\text{REM}}$
Local	1	0	1
Remote	1	1	0
Disabled	0	1	0

16B RATE

CMD RATE				
$\overline{\text{25/SEC}}$ (Pin EE)	$\overline{\text{100/SEC}}$ (Pin FF)	10/SEC	25/SEC	100/SEC
1	1	1	0	0
0	1	0	1	0
1	0	0	0	1
Non-Standard				
0	0	1	0	0

ICs 4a and 4b staticise the rate command

i) For fixed range operation at the end of Ramp Up

ii) For auto range operation at the end of Ramp Down

16C MODE

i) When Remote is not selected or commanded $\overline{\text{REM}}$ is high and the mode lines are controlled by SB. During remote operation they are controlled by the CMD MODE lines

CMD MODE		Select Mode	$\overline{\text{DC}}$	$\overline{\text{AC}}$	$\overline{\Omega}$
$\overline{\text{AC}}$ (Pin AA)	$\overline{\Omega}$ (Pin BB)				
1	1	DC	0	1	1
0	1	AC	1	0	1
1	0	Ω	1	1	0
Non-Standard					
0	0	DC	0	1	1

16D COMMAND AUTO RANGE

Auto range operation is inhibited during 100/SEC operation.

16E RANGE

SA commands the range if REMOTE and AUTO RANGE have not been selected or commanded.

The CMD RANGE lines command the range if REMOTE and not AUTO RANGE have been selected or commanded.

The Auto Ranging commands the range if AUTO RANGE has been commanded or selected.

			CMD RANGES			16F Input		
Voltage Range	Resistance Range	Range	1	2	4	$\overline{1}$	$\overline{2}$	$\overline{4}$
1000V	10M	0	0	0	0	1	1	1
100V	1M	1	1	0	0	0	1	1
10V	100k	2	0	1	0	1	0	1
1V	10k	3	1	1	0	0	0	1
100mV	1k	4	0	0	1	1	1	0
(10mV)		5	1	0	1	0	1	0

16F RANGE CHECK

The output RANGE lines $(\overline{4}\ \overline{2}\ \overline{1})$ all go high (1000V or 10MΩ range) if

i) 10mV DC range (5) is commanded for 10/SEC operation.

ii) Range 5 is commanded for AC and resistance measurement.

The $\overline{\text{DOWN RANGE INHIBIT}}$ line goes low inhibiting 19C (Auto Range Counter) during 25/SEC and 100/SEC operation if

i) 10mV DC range (5) is commanded

ii) Range 4 is commanded for AC and resistance measurement.

16G RESPONSE

FILTER cannot be commanded for Auto Ranged AC measurements or 100/SEC operation.

16H RATIO

RATIO cannot be commanded for 100/SEC operation.

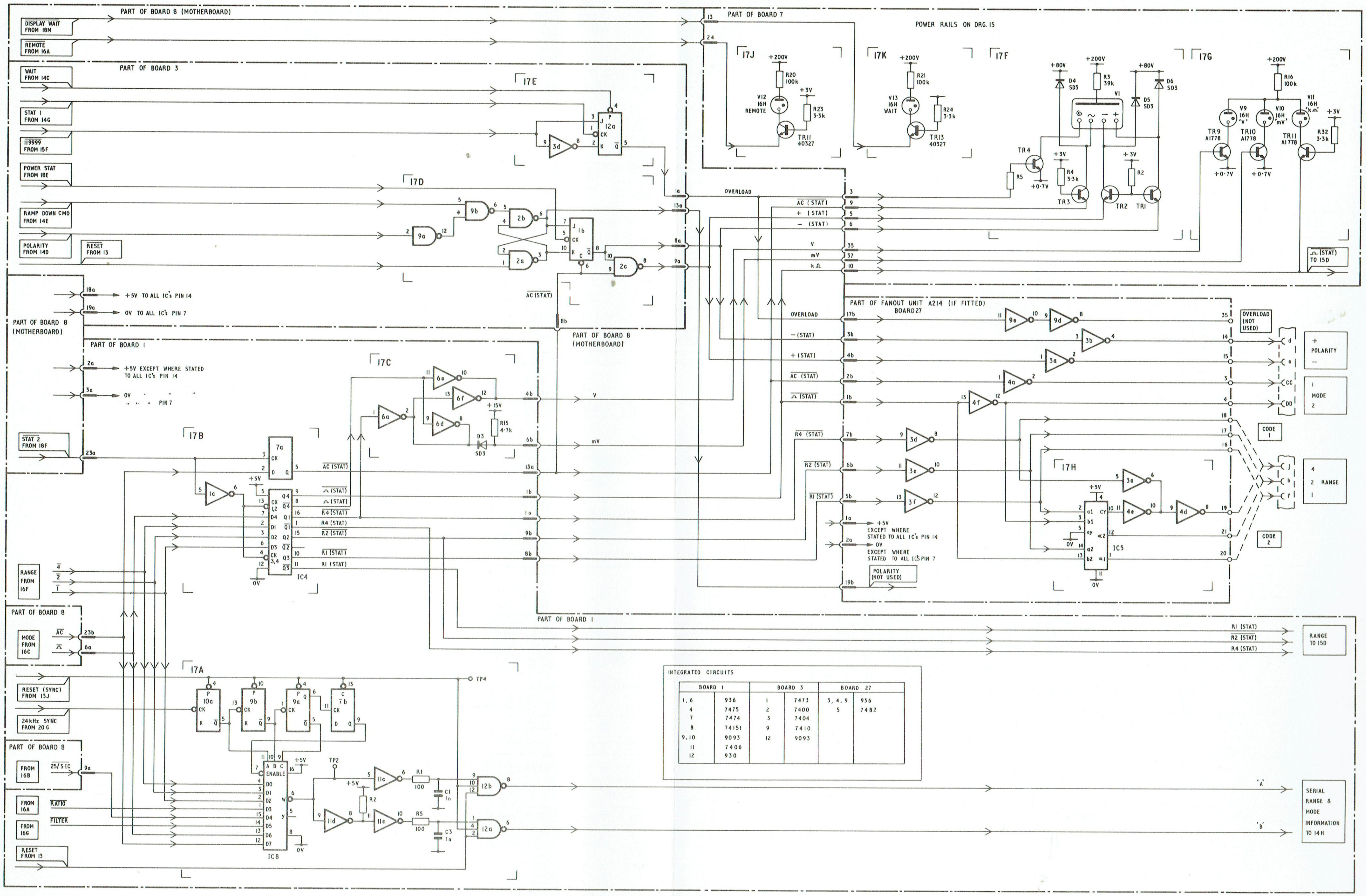
INTEGRATED CIRCUITS

BOARD 1		BOARD 27		BOARD 28		BOARD 29	
1	936	4, 9, 11	936	1, 3	962	1, 2	7406
2	962	6	962	8, 10			
3	946			2, 5, 13	936		
				4	7474		
				9	7486		
				14	946		

RANGE, MODE, RESPONSE & RATE COMMANDS

16

A2107016 01



INTEGRATED CIRCUITS

BOARD 1		BOARD 3		BOARD 27	
1, 6	936	1	7473	3, 4, 9	936
4	7475	2	7400	5	7482
7	7474	3	7404		
8	74151	9	7410		
9, 10	9093	12	9093		
11	7406				
12	930				

RANGE & MODE
STORE & DISPL

A2107017 01

17. RANGE AND MODE SERIALISER, STORE AND DISPLAY

17A SERIALISER

At the start of the Reset Period RESET (SYNC) goes high, releasing the reset on the counter IC10a, 9b, 9a and 7b. IC7b Q output will be low, enabling serialiser IC8. The 24kHz SYNC pulses are counted and a BCD address appears at the A, B & C inputs of IC8. This address transfers the Range, Ratio command, Rate command, Filter command and Mode command in serial form to the floating section via 14H. The 8th. 24kHz SYNC pulse after the start of Reset takes IC8 ENABLE high disabling the serialiser.

17B RANGE AND MODE STORE

Range and Mode information is staticised by $\overline{\text{STAT 2}}$.

i) For fixed range operation at the end of Ramp Up

ii) For auto range operation at the end of Ramp Down, when the correct range is found.

17C V AND mV DECODE

Resistance Ranges:	V and mV lines are low.
Voltage Ranges:	A high gives indication.

17D POLARITY STORE

The polarity input to the latch IC2b/IC2a is enabled when RAMP DOWN CMD is high, and the latch is cleared by $\overline{\text{RESET}}$ at the start of the Reset period. The polarity information is transferred to IC1b at the end of Ramp Down by POWER STAT. During ac measurement +(STAT) and –(STAT) are both high.

17E OVERLOAD

Overload is clocked high by STAT 1 at the end of Ramp Down if 119999 is detected during Ramp Down, and is reset low at the end of the next Ramp Up by $\overline{\text{WAIT}}$.

17F, 17G, 17J & 17K

These are displays.

17H Part of Fan-Out

If CODE 2 is selected for voltage measurements 2 is added to the BCD range and for resistance measurements 1 is added to the BCD range.

18. SAMPLE AND AUTO RANGE CONTROL

18A

When Remote is not externally commanded IC1a output is low and the 10/SEC (Repetative) and MANUAL (Single Sample) buttons are enabled.

18B

A Contact Sample or Pulse Sample command takes SINGLE SAMPLE low.

18C

i) **Repetative:** SAMPLE CMD is held low

ii) **Single Sample:** When a Single Sample is commanded SAMPLE CMD pulses low. If DATA IS CHANGED for 25/SEC operation (see 13G) SAMPLE CMD is held low until the next POWER STAT occurs. This makes the DVM skip a sample.

18D

i) **Repetative:** IC14a Q output is held high. SAMPLE is clocked high at the start of Reset.

ii) **Single Sample:** IC14a Q output is set high by SAMPLE CMD, and SAMPLE is clocked high at the start of Reset. If STAT INHIBIT then goes low (inhibit) SAMPLE is held high until the inhibit is removed. Otherwise the start of the next Reset sets SAMPLE low, provided another sample is not required. IC9c output goes low during the Reset period after a Single Sample is commanded.

18E

STAT 1 is gated as POWER STAT if SAMPLE and STAT INHIBIT (not inhibit) are high.

18F

i) **Fixed Range:** The high WAIT pulse at the end of Ramp Up is inverted to become STAT 2 if SAMPLE and STAT INHIBIT (not inhibit) are high.

ii) **Auto Range:** The high STAT 1 pulse at the end of Ramp Down is inverted to become STAT 2 if SAMPLE and STAT INHIBIT (not inhibit) are high.

18G

i) **Repetative:** PRINT COMMAND (LEVEL) is held low by SAMPLE CMD

ii) **Single Sample:** PRINT COMMAND LEVEL is clocked low by POWER STAT and is reset high by SAMPLE CMD.

18H

i) **Repetative:** DATA CAN CHANGE is held high by SAMPLE CMD

ii) **Single Sample:** DATA CAN CHANGE is set high by SAMPLE CMD and reset low by STAT 2

18J

Stores Auto Range command/selection.

18K STAT DELAY

1.5s monostable is triggered at the start of the Reset period, if a single sample is required, by the 18D output during 10/SEC or 25/SEC operation if AC or SLOW (Filter) is commanded or selected. It is retriggered during Auto Ranging by the CHANGE RANGE pulses. This gives extra settling time before a measurement is staticised.

18L STAT SKIP

During 25/SEC Auto range operation 2 samples are made before a range change or POWER STAT occurs. IC1a divides the STAT 1 pulses by 2 until $\overline{\text{CORRECT RANGE}}$ goes low (range correct).

18M DISPLAY WAIT

$\overline{\text{DISPLAY WAIT}}$ is set low ('WAIT' indicated) by 18K or 18L output and is clocked high at the start of Ramp Up.

18N

STAT 1 is inverted to CHANGE RANGE if Auto Range is selected or commanded, $\overline{\text{CORRECT RANGE}}$ is high (range incorrect and $\overline{\text{DISPLAY WAIT}}$ is high (no STAT DELAY or STAT SKIP)

18P

Stores CHANGE RANGE when the Main Counter is Reset and the Auto Range decision (RANGE CORRECT) is invalid.

18Q

$\overline{\text{STAT INHIBIT}}$ goes low (inhibits) when SAMPLE is high if

i) DISPLAY WAIT is high (during STAT DELAY (18K) or STAT SKIP (18L))

or

ii) During Auto Ranging is 18P output is high (range incorrect).

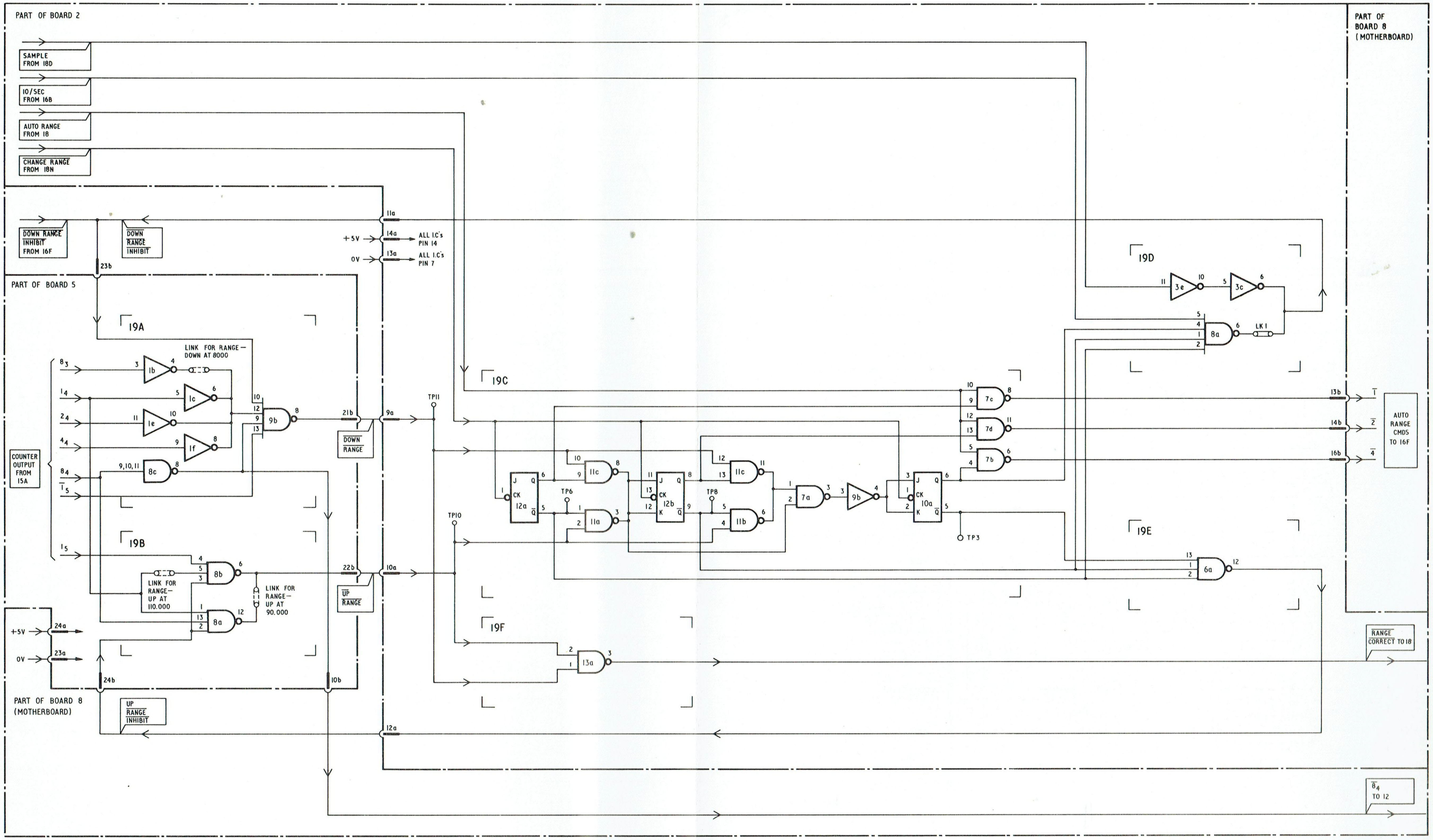
INTEGRATED CIRCUITS

BOARD 2		BOARD 3		BOARD 28		BOARD 29	
1,10	9093	4	7474	14	946	1	7406
2,13	946	5	930	15	9093		
3,9	936	6	932				
4	74121	9	7410				
5	930	14	9093				
6	962						

SAMPLE AND AUTO RANGE CONTROL

18

A2107018 01



AUTO RANGING

A2107019 01

19 AUTO RANGING

19A

When DOWN RANGE INHIBIT is high (no inhibit):

i) 8000 Link made

DOWN RANGE is low for Counter Outputs or less than 8000

ii) Link not made

DOWN RANGE is low for Counter Outputs of less than 10000

19B

When UP RANGE INHIBIT is high (no inhibit):

i) 110000 Link made

UP RANGE is low for Counter Outputs or greater than 109999

ii) 90000 Link made

UP RANGE is low for Counter Outputs or greater than 89999

19C AUTO RANGE COUNTER

On receipt of a low CHANGE RANGE pulse, it counts up to a more sensitive range if DOWN RANGE is low and counts down to a less sensitive range if UP RANGE is low.

19D

During 10/SEC operation, inhibits 19C via 19A when range 4 (100mV, 1kΩ) is reached.

SAMPLE from 18D inhibits ranging down to a more sensitive range during single sample operation, when a sample has not been ammended.

19E

Inhibits 19C via 19B when range 0 (1000V, 10MΩ) is reached.

19F

RANGE CORRECT is low when a correct range is detected by 19A and 19B.

20. POWER SUPPLIES

20A POWER INPUT

SK connects the primaries of T1 in series or parallel. SJ selects the taps on the primaries.

20B +20 VOLT SUPPLY

RV1 adjusts the +20V rail. R8 and D14 stabilise the current through D1, the starting current being through R4.

TR3 limits the overload current to 2A.

20C INVERTER OSCILLATOR

Either TR6 or TR7 is turned on by the unstabilised supply through R10 when the DVM is switched ON.

When the inverter starts, the +12V rail voltage rises and TR8 (emitter and collector functions reversed) turns on. T1 secondary centre tap goes to 0V and the drive is removed to TR6 and TR7 from the unstabilised supply.

20D

Bridge rectifier and filters for 200V rail.

20E

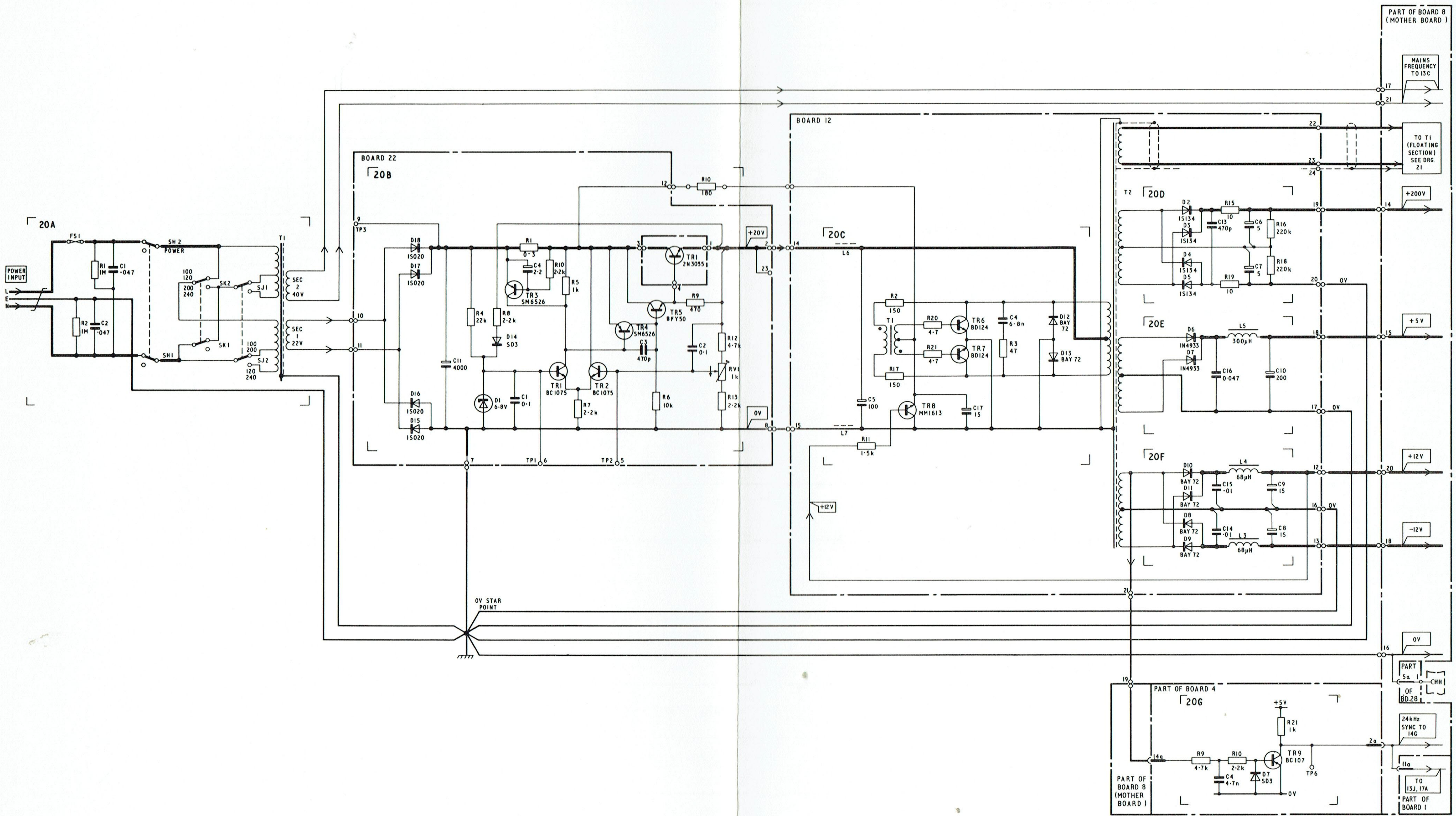
Full wave rectifier and filter for +5V.

20F

Full wave rectifiers and filters for + and −12 volts.

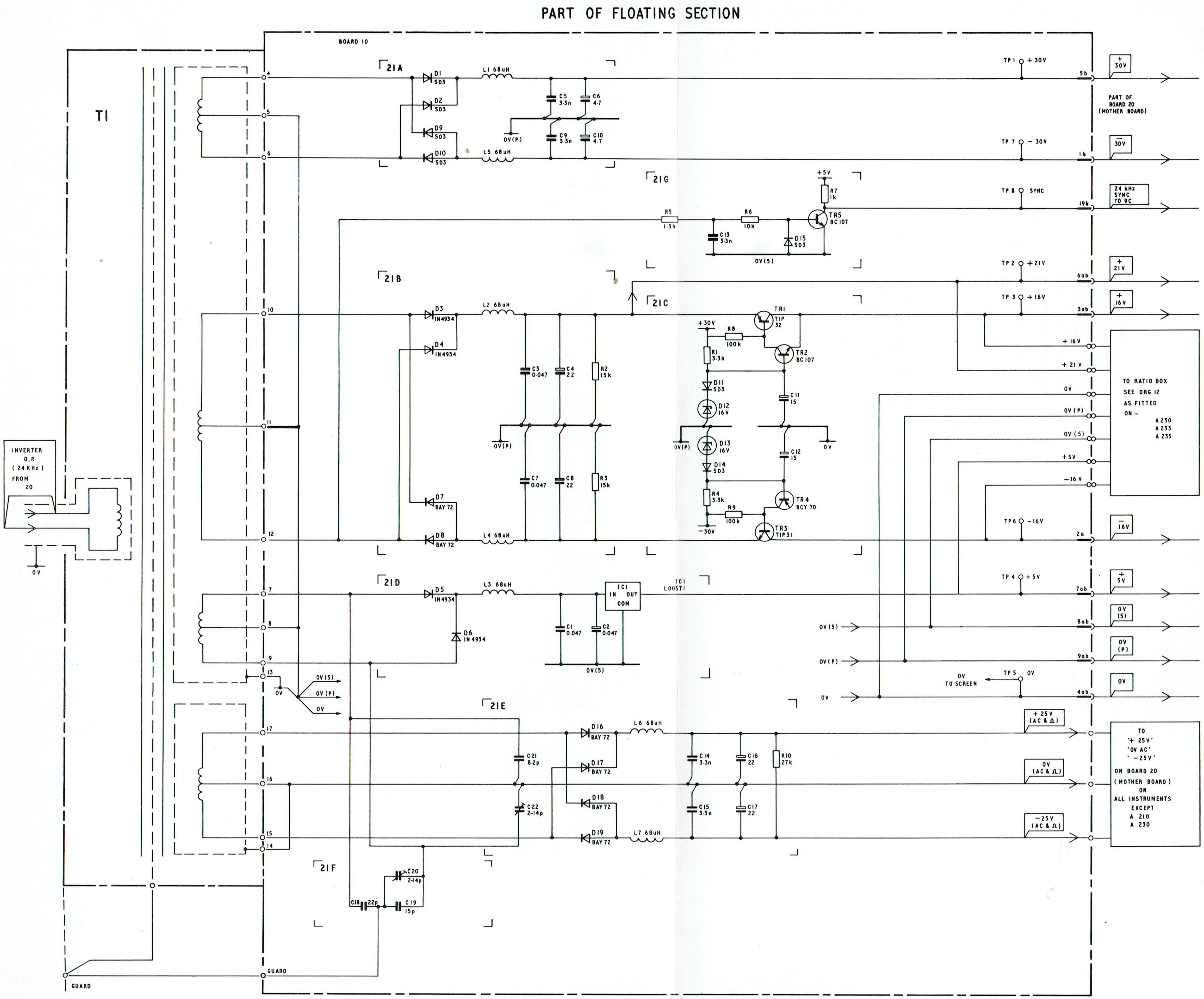
20G

Squarer for 24kHz SYNC to 14G, 13J and 17A.



POWER SUPPLIES **20**

A2107020 01



FLOATING POW SUPPLIES

A2107021 01

21. FLOATING POWER SUPPLIES

ISOLATION TRANSFORMER (T1)

This isolates the Floating Power supplies from the earthed section.

21A

Fullwave rectifiers and filters for + and −30V rails .

21B

Fullwave rectifiers and filters for +21V rail. Supply for rails for + and −16V stabilised supply.

21C

Stabilising network for + and −16V rails.

21D

Fullwave rectifier, filter and stabiliser for the +5V rail.

21E

Fullwave rectifiers and filters for the + and −25V (AC and Ω) rails and the 0V (AC and Ω).

C21 and C22 form a bridge for cancelling inverter pick up on the 0V (AC and Ω), C22 being adjusted on AC mode.

21F

Capacitive bridge for cancelling inverter pick up on the Guard Box. C20 is adjusted for minimum inverter frequency at TP1 Board 18 (see Drg. 7).

21G

Squarer for 24kHz SYNC to 9C.

SECTION 8 Test Specification

CONTENTS

TEST EQUIPMENT

Variac

Multimeter e.g. AVO model 8.

Sub-standard Multimeter, e.g. EIL44A.

Oscilloscope with a Y amplifier bandwidth of approximately 20kHz.

e.g. Tektronix 545A with 1A7A Module,

or Solartron CD1400 with CX1441, CX1442 and CX1443 Modules.

Thermocouple Thermometer, e.g. Comark Thermometer.

DC Calibrator, e.g. COHU 351, DC Voltage Standard.

DC Digital Voltmeter of at least 0.05% accuracy, and 10μV resolution, e.g. Solartron A220.

Kelvin Varley Divider, e.g. ES1 Dekavider RV622A (10kΩ).

For A212, A213, A215, A233, A235

Decade Resistance Standard (to 1.11MΩ) e.g. ES1 RS624.

Resistance Standard, 10MΩ, of known value to an uncertainty of 0.025% e.g. ES1 SR1.

Resistance Standard, 5MΩ, of known value to an uncertainty of 0.01% e.g. ES1 SR1.

Resistance Standard, 1MΩ, of known value to an uncertainty of 0.003% e.g. ES1 SR1.

Resistance Standard, 100MΩ of known value to an uncertainty of 0.003% e.g. ES1 SR1.

For A211, A213, A215, A233, A235

AC Calibrator e.g. Hewlett Packard AC Calibrator 745A
with a Hewlett Packard 1000V Amplifier 746A.

PRECAUTIONS

Check for short circuits on all rails.

Check the connection of the rails from the Inverter (pcb 12, Drg. 20) to the Earthy Mother Board (pcb 8, Drg. 20).

A INITIAL CALIBRATION (Earthy Section)

1. POWER SUPPLIES (EARTHY)

1.1 Switch OFF.

Set the Main Selector to 220 - 255V, and check that a 250mA fuse is fitted.

Connect the DVM to the mains via a Variac.

Set the Variac to 0V, and switch DVM and Variac ON.

Using the test equipment DVM on the 200V range, increase the Variac to 240V and check the 20V rail stabilises at this value (pin 2, pcb 22).

1.2 Adjust RV1, pcb 22 for a reading of +20V ± 0.1V.

Set Variac to 0V.

1.3 Check out each of the four mains settings, as indicated on each of the four mains selector plates, checking that the +20V rail remains stabilised over the mains variation in the table.

Ensure the correct fuse is fitted.

Mains Selector	Selector Switches	Mains Supply	Fuse
195 - 230V	Upper LEFT Lower RIGHT	200 - 230V	250mA
220 - 255V	Upper LEFT Lower LEFT	220 - 250V	250mA
98 - 115V	Upper RIGHT Lower RIGHT	98 - 115V	500mA
110- 128V	Upper RIGHT Lower LEFT	110 - 130V	500mA

1.4 Rail Volts

Check the rails for voltage and ripple limits in the table:

Rail	Pin No. (pcb 22)	Voltage Limits	Ripple Limits
+5V	18	5V ± 0.5V	≯150mV p-p
+12V	13	12.5V ± 0.5V	≯150mV p-p
-12V	12	12.5V ± 0.5V	≯350mV p-p
+200V	19	210V ± 20V	≯2V p-p

2. CLOCK OSCILLATOR

2.1 Measure the voltage between TP3 and TP8, pcb 4, and adjust C16 for a minimum reading, < ± 0.2V.

2.2 Command 100/SEC rate remotely [with TG1022/7 connected to FAN OUT, or pin FF connected to pin HH] and adjust RV1 pcb 4 for a minimum reading < ± 0.2V.

3. **INVERTER PHASING**

3.1 Monitor the waveform, at TP3 pcb 1 and TP8 pcb 10 (use both displays of the oscilloscope). Both waveforms should be almost in phase. If not, reverse primary inverter leads (Pins 22 and 23, pcb 12).

INITIAL CALIBRATION (Floating Section)

4. **POWER SUPPLIES (FLOATING)**

4.1 Check the following rails for voltage and ripple:

	Rail	PCB	Pin	Reference	Voltage	Ripple
	+5V	10	TP4	TP5 (0V)	5V ± 0.25V	≯10mV p-p
	+16V	10	TP3	TP5 (0V)	16.5V ± 2V	≯10mV p-p
	-16V	10	TP6	TP5 (0V)	16.5V ± 2V	≯10mV p-p
	+21V	10	TP2	TP5 (0V)	20V ± 2V	≯250mV p-p
	+30V	10	TP1	TP5 (0V)	20V ± 2V	≯150mV p-p
	-30V	10	TP7	TP5 (0V)	29V ± 2V	≯150mV p-p
A212	+25V (AC&Ω)	20	+25V	0V AC	24V ± 1V	≯150mV p-p
A212	-25V (AC&Ω)	20	-25V	0V AC	24V ± 1V	≯150mV p-p
A211 A213 A215 A233 A235	+25V (AC&Ω)	20	+25V	0V AC	23V ± 1V	≯150mV p-p
A211 A213 A215 A233 A235	-25V (AC&Ω)	20	-25V	0V AC	23V ± 1V	≯150mV p-p

5. **INPUT AMPLIFIER**

All Adjustments and test points are on pcb 18.

5.1 Select LOCAL, DC, 10/SEC, 10V Range, SLOW, and fit an INPUT lead to the DVM. Use the oscilloscope with a bandwidth of approximately 20kHz (e.g. Solartron CD1400, with an CX1442 Y amplifier, or Tektronix 545A with 1A7 Y amplifier).

5.2 Apply approximately +100mV from the COHU 351 (or other low impedance source) to TP3, adjusting RV2, for maximum amplitude waveform at TP2. This should be approximately 2V p-p.

Remove the applied voltage.

5.3 Check the spike amplitude at TP1.

Adjust RV1 for ≯2mV p-p.

5.4 Check the volts across C9. If >1.8V, remove the link across R50.

5.5 Select FAST. Check the waveform at TP1.

Adjust C20, pcb 10, for minimum amplitude of inverter frequency (24kHz).

6. OVEN AND REFERENCE AMPLIFIER

The DVM should have been ON for at least 1 hour. All functions are on pcb 11.

6.1 If pcb 11 has not been pre-tested, RV4, RV5, RV6, and RV7 should be set fully clockwise.

Check the oven space around D32 is filled with heatsink compound.

6.2 Measure the oven temperature with the thermocouple probe (test equipment thermometer) in the oven test aperture.

Adjust RV3 to set the oven temperature to $80^{o}C \pm 1^{o}C$.

6.3 Using the test equipment dvm on $10\mu V$ resolution, measure the voltage between TP6 and TP9 (0V) and adjust RV2 for a minimum reading.

Measure the voltage between TP10 and TP9, adjusting RV1 for a minimum reading.

7. INTEGRATOR OFFSET

7.1 Select LOCAL, DC, 10/SEC, 10V RANGE, FAST.

7.2 Short INPUT Hi and Lo. Adjust RV1 for + and - signs displayed alternately.

8. OFFSET AND REFERENCE SUPPLIES

8.1 Using the COHU 351, DC Voltage Standard, carry out the following adjustment on pcb 11.

Apply +1mV to the Input. Adjust RV7 for a reading of +10 digits.

Apply -1mV to the Input. Adjust RV6 for a reading of -10 digits.

Repeat 1. and 2. and 7.2. tests until all points are correct.

Apply +10.0000V to the Input. Note the reading.

Apply -10.0000V to the Input. Adjust RV9 for the same reading.

9. 10V RANGE CALIBRATION

RV5 and RV6 are on pcb 19.

Select LOCAL, DC, 10/SEC, 10V RANGE, FAST.

9.1 Apply +10.0000V to the Input and note the reading.

9.2 Adjust RV5 for a reading of exactly +10.0000V.

If the range of RV5 is inadequate, LINKS H or J will require alteration.

9.3 In case of difficulty in selecting the correct link pattern, reference may be made to "A210 Range Tables" proceeding as follows:

(a) Set RV5 fully clockwise, and connect TP3 to TP4.

(b) Apply +10.0000V to the INPUT and note the reading.

(c) Set the LINKS A to J as indicated in the Range Tables for this reading.

(d) Remove TP3 and TP4 connection and adjust RV5 for exactly +10.0000V, finally altering LINKS H or J if the range of RV5 is inadequate.

9.4 Command 25/SEC remotely.

[TG1022/7 connected to fan out socket, or pin EE connected to HH].

Adjust RV6 for a reading of +10.000V.

10. INPUT CURRENT AND ZERO CHECKS

10.1 Select LOCAL, DC, 10/SEC, 100mV RANGE, SLOW.

Ensure the Floating Box screen is fitted.

10.2 Connect a 1MΩ resistor across Input Hi and Lo. Adjust RV1 pcb 18 for a minimum reading.

10.3 Connect the input lead. Short Input Hi to Lo. Select FAST and adjust "μV OFFSET" (RV1, front panel) for a reading of about +5μV. Check the noise on the display. The scatter should be ≯ 4 digits.

Adjust "μV OFFSET" for minimum reading.

10.4 Recheck 8. **OFFSET AND REFERENCE SUPPLIES** making final adjustments where necessary.

10.5 Short circuit Input Hi to Lo and check the reading on 1V to 1000V Ranges is zero ± 1 digit.

10.6 Select SLOW and check the reading on all ranges is zero ± 1 digit.

11. INPUT RESISTANCE

11.1 Select DC, 10/SEC, SLOW.

Check the input resistance on the ranges in the following table, on both polarities, using the COHU 351 (or similar low impedance source).

Connect a 1MΩ 1% resistor between Input Hi and voltage source. Note the change in reading with Input Hi connected direct to voltage source.

DC Range	Input Voltage	Change in Reading
10V	10.0000V	± 10 digits
1V	1.00000V	± 30 digits
100V	100.000V	± 100 digits

12. LINEARITY

12.1 Select LOCAL, DC, 10/SEC, 10V RANGE, FAST.

Using the COHU 351, apply voltage increments to the DVM via the Kelvin Varley divider RV622A (10kΩ) checking that the DVM reads the applied voltage within the limits detailed in the table.

Input Positive and Negative	Limits
100μV to 1mV in 100μV steps	± 1 digit
100mV to 900mV in 100mV steps	± 1 digit
1V to 11V in 1V steps	± 1 digit
Check with 11.9000V	± 1 digit

13. RANGE CALIBRATION

CAUTION: Observe OVERLOAD limits (see Operating Instructions). On A210, A212, A230 if "AC" MODE (normally masked by the front panel) is selected, the DVM is in the 1V, DC range.

13.1 Select SLOW.

13.2 Apply the voltages shown in the tables, using the COHU 351, and the RV622A for voltages below 10V, adjusting the potentiometers appropriate to each range for the correct reading.

Check that correct polarity, mV, V and decimal point are displayed.

Rate	Range	Input	Adjustment pcb 19	Reading
10/SEC	1V	+1.00000V	RV2	+1.00000V
10/SEC	100mV	+100.000mV	RV3	+100.000mV
25/SEC	10mV*	+10.0000mV	RV4	+10.000 mV

*10mV RANGE

Command 25/SEC

[or connect pin EE (Command RATE) to pin HH].

Note the last DVM decade is not displayed.

Command 10mV Range

[or command 10mV Range as in Range Logic, see Operating Instructions].

Repeat the above table until readings are correct.

Command 10/SEC

[or disconnect pin EE from pin HH].

Rate	Range	Input	Adjustment	Reading
10/SEC	100V	+100.000	RV1	+100.000V
10/SEC	1000V	+1000.00V		+1000.00V
				± 2 digits

13.3 Repeat 13.2 on -ve polarity. The difference between the two polarities for each reading should not exceed 2 digits.

13.4 Select FAST.

The difference in readings on either polarity at full scale, 100mV to 100V Ranges, should not exceed ± 2 digits of the readings on SLOW.

14. Ω MODE (A212, A213, A215, A233, A235)

Remove top screening cover of the floating box assembly and check that pcb 16 is correctly fitted.

14.1 Select Ω. Check that **mV**, **V** and ~ signs are not displayed, and "kΩ" and the correct decimal point for each range are displayed.

14.2 Measuring Current Set Up.

Select 10/SEC, LOCAL, 100kΩ RANGE.

Connect the 100kΩ Precision Resistor across Input Hi and Lo.

Adjust RV1, pcb 16, until the display reads the value of the precision resistor.

If the range of RV1 is inadequate, LINKS G or H will require alteration.

In case of difficulty, reference may be made to "A210 Range Tables", proceeding as follows:

(a) Select 10k on the RS624, and connect this to the Input Hi and Lo. Select 10kΩ RANGE.

(b) Connect TP1 to TP5 pcb 16.

(c) Note the DVM reading and set the LINKS A to H as indicated in the Range Tables for this reading.

(d) Remove TP1 and TP5 connection, and adjust RV1 until the display reads the value of the 10kΩ setting.

Select 1000kΩ RANGE.

Connect the 1MΩ precision resitor across Input Hi and Lo.

Adjust RV2 pcb 16 until the display reads the value of the precision resistor.

Repeat the RV1 and RV2 adjustments until both are correct.

14.3 Zener Stability

Select 100kΩ RANGE.

With the 100kΩ between Input Hi and Lo change the 20V rail on pcb 22 (RV1) by + or - 0.5V checking that the reading on the display does not change by more than + or - 10 digits. Reset the rail to 20V ± 0.1V.

14.4 Zero Checks

Fit a 4 terminal lead* to the DVM input.

Short Inputs Hi to Inputs Lo.

Select 100mV DC and check the setting of the 10μV OFFSET is zero.

Select Ω and each Ω RANGE in turn.

Readings should be zero ± 1 digit.

*Only necessary on 1kΩ Range.

14.5 Overload Checks

(a) Select 1000kΩ.

(b) Monitor the volts across D11 pcb 16 with an isolated voltmeter (e.g. AVO8).

(c) Apply a 200V input to the DVM (+ve to INPUT Hi). Voltage across D11 should be ≏16V.

(d) Reverse the INPUT leads to the 200V supply. Voltage across D16 should be ≏1V.

14.6 Range, Accuracy and Linearity.

Using the Decade Resistance Standard (0.01% Grade e.g. RS624), checked to an uncertainty of ± 0.003% at 20°C, the precision resistor 10MΩ (of known value, ± 0.025%) and precision resistor 5MΩ (of known value, ± 0.01%), check the DVM reading is within the limits given for the resistance standard connected to the input.

Resistance Standard	**DVM Range**	**Limits**
***use 4 terminal input**		
1k	1k*	± 10 digits
0.8k		± 8 digits
0.6k		± 6 digits
0.4k		± 4 digits
0.2k		± 2 digits

Resistance Standard *use 4 terminal input	DVM Range	Limits
10k	10k	± 10 digits
8k		± 8 digits
6k		± 6 digits
4k		± 4 digits
2k		± 2 digits
100k	100k	± 10 digits
80k		± 8 digits
60k		± 6 digits
40k		± 4 digits
20k		± 2 digits
1000k	1000k	± 10 digits
800k		± 8 digits
600k		± 6 digits
400k		± 4 digits
200k		± 2 digits
10M	10 000k	± 50 digits
5M		± 25 digits
1M		± 5 digits

15. FUNCTIONAL CHECKS

15.1 Select MANUAL, DC.

Apply a variable dc input within the Range selected. Check that the reading does not change until MANUAL button is pressed.

15.2 AC Display. On A210, A212 and A230, although AC option is not fitted, the display may be checked by removing the control part of the front panel so as to expose the AC Mode selector. Select AC (press the central MODE selector) and check the correct decimal point, **mV, V and ~** are displayed on all ac ranges.

Select DC and replace the front panel.

15.3 Ω Display. On A210, A211 and A230, although the Ω option is not fitted, the display may be checked by removing the control part of the front panel so as to expose the Mode selector.

Select Ω (press the right hand MODE selector) and check the correct decimal point and "kΩ" are displayed on all ohms ranges, the **mV, V** and ~ being extinguished.

Select DC and replace the front panel.

15.4 Select MANUAL and SLOW.

Check that "WAIT" is displayed for approximately 1 sec. when the MANUAL button is pressed.

15.5 Select REMOTE.

Check that REMOTE is displayed.

15.6 Select 10/SEC, DC, 1V RANGE.

Apply a dc input so that "1.19999" is displayed. Check that the Overload symbol is also displayed.

16. AUTO RANGE

16.1 Select LOCAL, DC, AUTO, 10/SEC, FAST.

Using a variable DC source, check the instrument selects a higher range when the reading exceeds 110 000 digits, and a lower range when the reading falls below 10 000 digits.

16.2 Apply the voltages detailed in the following table and check the DVM selects the correct range.

INPUT VOLTAGE	90mV	900mV	9V	90V	900V	0V
DC RANGE	100mV	1V	10V	100V	1 000V	100mV

16.3 Select MANUAL.

Apply 900V and check that the range relays are heard to operate.

Press MANUAL button and check the display is updated.

Apply zero input, and press MANUAL button.

Check that the range relays are heard to operate, selecting the 100mV range, and the display reads zero $\pm$ 20μV.

16.4 Select SLOW and repeat 16.3. 100mV range should read zero $\pm$ 20μV.

16.5 Fit an A214 (Fan Out option) to the fan out socket or connect TG1022/7 to the fan out socket. Select REMOTE on the DVM.

Command 25/SEC

[or connect pin EE to pin HH].

Repeat 16.3. 10mV range should be selected on 0V input and the display should read zero $\pm$ 20μV.

Command 10/SEC

[or remove pin EE from pin HH].

17. FAN OUT

17.1 Plug in an A214 Fan Out Unit.

17.2 Select REMOTE and check REMOTE is displayed.

17.3 Check the DVM will not operate on any of the front panel controls except MANUAL and 10/SEC.

17.4 Connect TG 1022/7 (if available) to the fan out socket.

Check the DVM samples when SAMPLE button is pressed [or connect pin s (Contact Sample) to pin HH (0V)].

17.5 Select REMOTE on TG 1022/7

[or connect pin r (Command CONTROL to pin HH].

Check that this disables all front panel controls except POWER.

Operate PULSE SAMPLE on TG 1022/7 (or apply a pulse $>$+3V and $<$+8V and $>$10μs duration to pin t (Pulse Sample)].

Check that the DVM samples.

17.6 Rate, 100/SEC.

Command 100/SEC on TG 1022/7 (or connect pin FF to pin HH, 0V).

Check the last two DVM decades are not displayed.

Command 10mV Range, DC on TG 1022/7

[or command 10mV Range, DC as in the Operating Instructions].

Apply +10mV dc to the DVM and check the DVM display reads correctly when SAMPLE is pressed or when PULSE SAMPLE is operated on TG 1022/7

[or when Contact Sample or Pulse Sample are applied as in 17.4 and 17.5].

Repeat on each range, applying a full scale DVM input.

17.7 Rate, 25/SEC.

Command 25/SEC on TG 1022/7 (or disconnect pin FF and connect pin EE to pin HH).

Check that the last DVM decade is not displayed. Cancel REMOTE on the TG 1022/7.

[or disconnect pin r from pin HH, 0V].

Command 10mV Range, DC on TG 1022/7

[or command the 10mV DC range as per the Operating Manual].

Apply a variable dc input up to 10mV and check the DVM displays the input continuously (i.e. readings are repetitive).

17.8 Auto Ranging.

Command AUTO on TG 1022/7

[or connect pin y (Command AUTO Range) to pin HH].

Increase the DC input for a reading exceeding 11.000mV and check the DVM selects the 100mV Range.

Reduce the input for a reading below 10.000mV and check the DVM selects the 100mV Range.

Command AC on TG 1022/7

[or connect pin AA to pin HH].

Check that ~ (AC MODE), is displayed.

Command each range in turn on TG 1022/7

[or command each range as in the Operating Instructions] and check each range is correctly displayed.

Command Ω on TG 1022/7
[or disconnect pin AA and connect pin BB to pin HH].

Check that "kΩ" is displayed, and **mV**, **V** and ~ are not displayed.

Command each range in turn on TG 1022/7

[or command each range as in the Operating Instructions] and check each range in turn is correctly displayed.

Command DC

[or disconnect pin BB from pin HH].

Cancel AUTO RANGING.

[or disconnect pin y from pin HH].

Select LOCAL on the DVM.

18. SERIES MODE REJECTION

18.1 Select LOCAL, DC, 10/SEC, SLOW.

Connect the test equipment as shown in **Fig. 8.1.**

Apply the series mode mains frequency inputs to the DVM on the ranges shown in the following table; check the change in reading is ⊁ ± 1 digit.

Mode	Range	Series Mode Input
10/SEC	10V	7V rms
10/SEC	1V	700mV rms
10/SEC	100mV	70mV rms

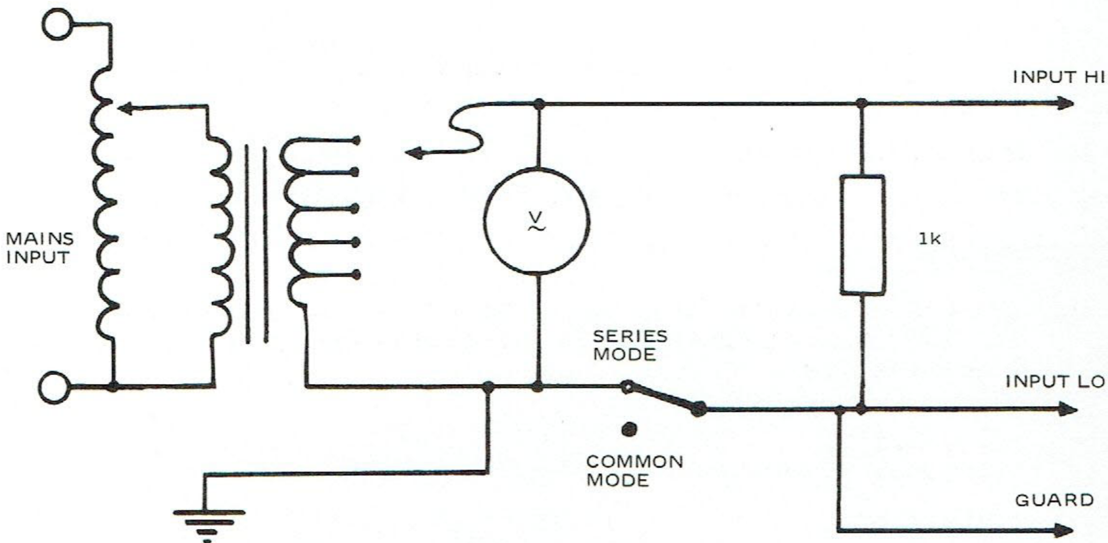


Fig. 8.1 AC Series and Common Mode Rejection

19. AC COMMON MODE REJECTION

19.1 Refer to **Fig. 8.1.**

19.2 Select FAST, 100mV RANGE.

Apply 7V rms at mains frequency to the DVM, checking the change in reading is ⊁ ± 1 digit.

19.2 Select FAST, 100V RANGE.

Apply 70V rms at mains frequnecy to the DVM, checking that the change in reading is ⊁ ± 1 digit.

20. DC COMMON MODE REJECTION

20.1 Select DC, 10/SEC, 100mV RANGE, SLOW.

20.2 Refer to **Fig. 8.2** and apply 500V DC common mode voltage.
The DVM reading should be $\ngtr$ 10mV.

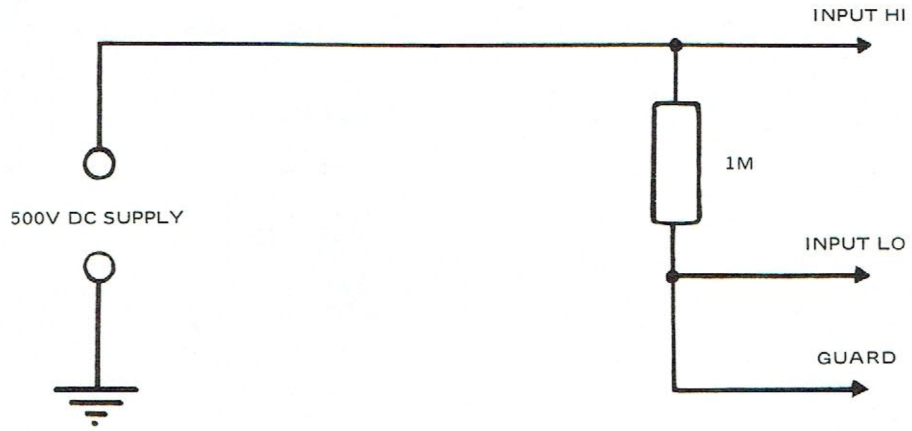


Fig. 8.2 DC Common Mode Rejection

21. TEMPERATURE CHECKS

Switch ON and allow the DVM to stabilise for 2 hours at room ambient.

21.1 Select LOCAL, DC, 10/SEC, SLOW.

21.2 Using the COHU 351 DC Voltage Standard, the H.P. 745A/746A AC Voltage Standard, a 1MΩ Grade 1 Resistor, the RS624 and the 10MΩ resistance standard, carry out the following Range and Mode checks;

(a) At a known room ambient, recording the temperature.

(b) At an oven temperature of 45°C after 2 hours stabilisation in the oven.

DVM Mode	Range	Input Conditions	(a) Ambient Check	(b) Oven Check	(c) Reading Change
	100mV	S/C Input	Note Reading		$\pm$ 0.3 V/°C
	100mV	1MΩ GR1	Note Reading		100μV total
ALL	10V Ranges	Input $\pm$ 1mV	Note Reading		$\pm$ 0.1 digits/°C
A210 DC A230	100mV	-100.000mV	Note Reading		$\pm$ 1 digit/°C
	1V	-1.00000V	Note Reading		$\pm$ 1 digit/°C
SERIES	10V	$\pm$ 10.0000V	Note Reading		$\pm$ 1 digit/°C
	100V	-100.000V	Note Reading		$\pm$ 1.5 digits/°C
	1000V	-1000.00V	Note Reading		$\pm$ 1.5 digits/°C

DVM Mode		Range	Input Conditions	(a) Ambient Check	(b) Oven Check	(c) Reading Change
A211		All Ranges	S/C Input	Note Reading		
A213	AC	100mV	100.000mV	Note Reading		$\pm$ 5 digits/^{o}C
A215	at	1V	1.00000V	Note Reading		$\pm$ 5 digits/^{o}C
A233	400Hz	100V	100.000V	Note Reading		$\pm$ 15 digits/^{o}C
A235		1000V	1000.00V	Note Reading		$\pm$ 15 digits/^{o}C
A212		All Ranges	S/C Input	Note Reading		
A213						
A215	Ω	10kΩ	10kΩ	Note Reading		$\pm$ 4 digits/^{o}C
A233		10 000kΩ	10 000kΩ	Note Reading		$\pm$ 4 digits/^{o}C
A235						

Record the readings at each temperature and check these against the limits in column (c).

21.2 Repeat the readings at a known room ambient temperature, after 2 hours stabilisation.

B. DC FINAL CALIBRATION

TEST EQUIPMENT

DC Potentiometer, 0.001%	e.g. Cambridge Type 44248
Temperature Controlled Standard Cell Bank	e.g. Guildline 9152T/4
Volts Ratio Box	e.g. Sullivan T2100
DC Voltage Standard, 0.003%	e.g. COHU 351

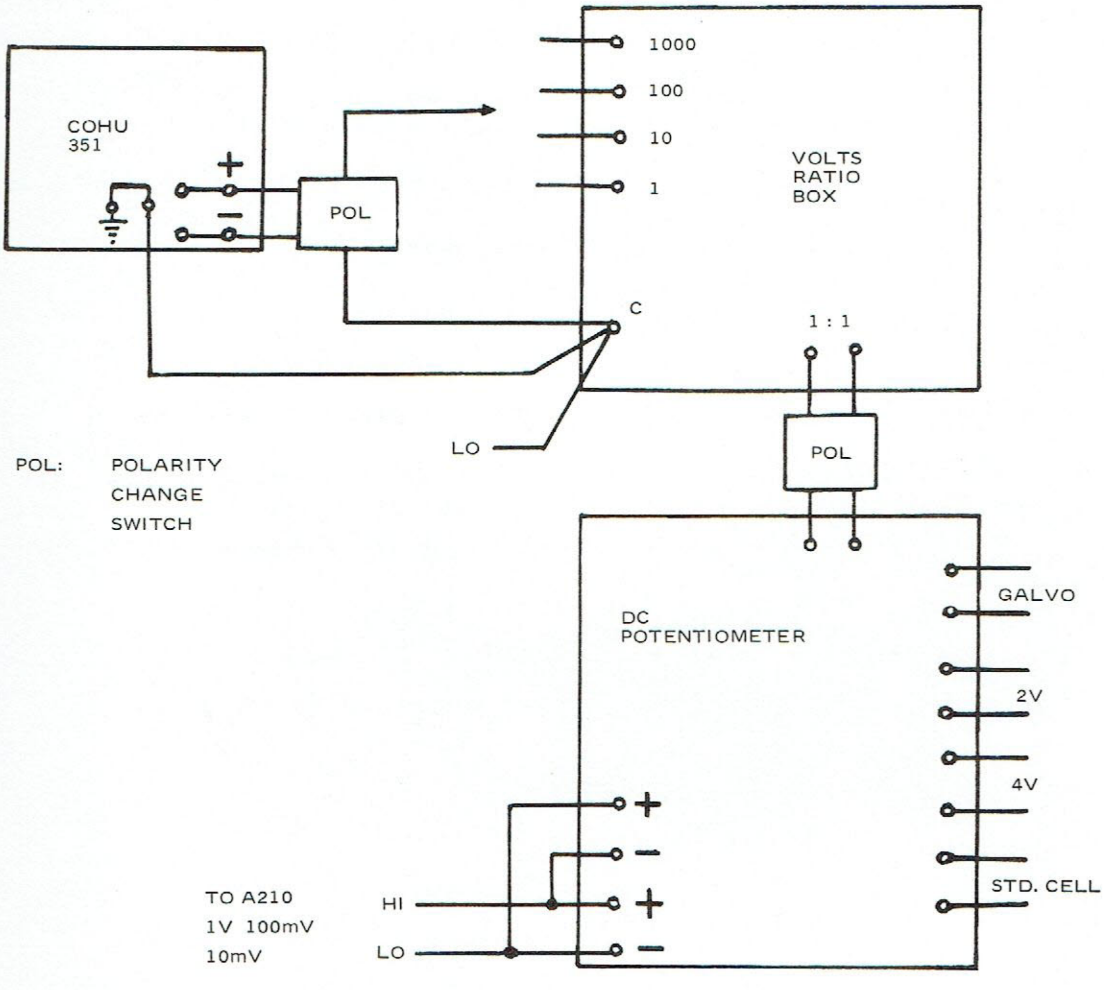


Fig. 8.3 DC Final Calibration

The test equipment interconnection is shown in **Fig. 8.3.**

The equipment must be thoroughly stabilised at $20^{\circ}C \pm 1^{\circ}C$ and must be operated, maintained and records kept in accordance with Standards Room Procedures.

The Volts Ratio Box and Standard Cell Bank should have valid certificates of calibration and values traceable to a National Calibration Authority.

The instrument should have been switched on for at least two hours in a $20^{\circ}C$ ($\pm$ $1^{\circ}C$) ambient, stable to $0.5^{\circ}C$.

1.1 Select LOCAL, DC, 10/SEC, 100mV, SLOW.

Connect a screened 1MΩ resistor across Input Hi and Lo. Adjust RV1 pcb 18 for minimum reading.

NOTE: If the input lead is connected to the DVM and an unscreened 1MΩ resistor used, locate the lead for minimum pick up and allow time for the reading to settle.

1.2 Connect the input lead. Short Input Hi to Lo and adjust "μV OFFSET" (front panel) for zero reading or 0 to 1 flicker.

Select 10V Range. Check the display for zero reading with + and - signs alternatively displayed.

Adjust RV1 pcb 13 for this display.

Apply +1mV. Adjust RV7 pcb 11 for a reading of +10 digits.

Apply -1mV. Adjust RV6 pcb 11 for a reading of -10 digits.

Apply +10.0000V. Adjust RV5 pcb 19 for a reading of +10.0000V.

Apply -10.0000V. Adjust RV9 pcb 11 for a reading of -10.0000V.

Select 1V Range.

Apply +1.00000V. Adjust RV2 pcb 19 for a reading of +1.00000V.

Select 100mV Range, SLOW.

Check the reading is zero with zero input.

Apply +100.000mV. Adjust RV3 pcb 19 for a reading of +100.000mV.

Repeat 10V, 1V and 100mV adjustments until all readings are correct.

1.3 Select 100V RANGE.

Apply +100V. Adjust RV1 pcb 19 for a reading of +100.000V.

With Inputs applied and response set, as shown in the following Table, check that the readings are within the specified limits.

Response	DC Range	Input	Reading Limits
FAST	10V	+10.0000V	± 2 bits
		+5.0000 V	± 2 bits
		-5.0000V	± 2 bits
		-10.0000V	± 2 bits
FAST	1V	+1.00000V	± 2 bits
		+0.50000V	± 2 bits
		-0.50000V	± 2 bits
		- 1.00000V	± 2 bits
SLOW	100mV	+100.000mV	± 2 bits
		+50.000mV	± 2 bits
		-50.000mV	± 2 bits
		-100.000mV	± 2 bits

Response	DC Range	Input	Reading Limits
FAST	100V	+100.000V	± 2 bits
		+50.000V	± 2 bits
		-50.000V	± 2 bits
		-100.000V	± 2 bits
FAST	1000V	+1000.00V	± 2 bits
		+500.00V	± 2 bits
		-500.00V	± 2 bits
		-1000.00V	± 2 bits

C. Ω FINAL CALIBRATION

TEST EQUIPMENT

The resistance standards detailed in Section A must be thoroughly stabilised at $20^{\circ}C \pm 1^{\circ}C$. The DVM should have been switched on for at least 2 hours in a $20^{\circ}C$ ($\pm$ $1^{\circ}C$) ambient and the DC FINAL CALIBRATION (Section B) completed.

1.1 Recheck "μV OFFSET" as in Section B 1.2.

1.2 Select Ω, 100kΩ RANGE.

Connect the 100kΩ resistance standard between Input Hi and Lo. Adjust RV1 pcb 16 until the display reads the resistance value.

Select 1000kΩ RANGE.

Connect the 1MΩ resistance standard between Input Hi and Lo and adjust RV2 pcb 16 until the display reads the resistance value. Repeat 100kΩ and 1000kΩ RANGE calibration until both readings are correct.

1.3 Check the ranges in the following table, with the appropriate resistance standards connected, for correct DVM readings within the specified limits.

Filter	Range	Resistor	Reading
FAST	1kΩ	1kΩ	Resistor Value ± 8 digits
FAST	10kΩ	10kΩ	Resistor Value ± 8 digits
FAST	10MΩ	10MΩ	Resistor Value ± 30 digits

D. AC CALIBRATION (A211, A213, A233)

The following tests 1 to 8 should be carried out after completing **14.Ω MODE** of the A210 Test Specification and before commencing **15. FUNCTIONAL CHECKS**. Remove the top screening cover from the Floating Box assembly and check the two pcbs 14 and 15 are fitted and correctly wired to the input socket. Set RV3 pcb 14 to its mid position.

A voltage standard HP745A/746A should be used for all calibration checks. The 745A voltage standard and instrument should have been switched on for a period of at least 1 hour.

1. AC MODE

Select: AC, LOCAL, 100mV RANGE, FAST.

1.1 Inverter Rejection

Connect input high to low and adjust C22 pcb 10 for a minimum reading on the display.

Recheck paragraph 5.3 of Section A. INITIAL CALIBRATION.

1.2 Linearity
Select: AC, 1V RANGE, FAST.

Feed in 1V at 400Hz and adjust RV2 pcb 14 for a reading of 1.00000V ± 10 digits.

Reduce the input to 0.1V and adjust RV3 pcb 14 for a reading of 0.10000 ± 2 digits.

Repeat the above until both readings are correct. Refit the top cover to the floating box.

1.3 Zero Checks

Connect input high to low and check the readings on the 1V, 100V and 1000V ranges do not exceed 5 digits.
Check the readings on the 100mV and 10V ranges do not exceed 15 digits.

In all cases allow some short time for the reading to run down to its final minimum value.

1.4 Basic Range Calibration and Frequency Check

Feed in 0.1V at 400Hz on the 100mV range and adjust RV1 pcb 14 for a reading of 100.000mV ± 10 digits.

Change the frequency to 20kHz when the reading should be 100.000mV ± 50 digits.

Change the frequency to 100kHz when the reading should be 100.000mV ± 300 digits.
Select SLOW. Change the frequency to 40Hz when the reading should be 100.00mV ± 60 digits.

1.5 100V Range Calibration
Select: SLOW

Feed in 100V at 400Hz on the 100V range and adjust RV1 pcb 15 for a reading of 100.000V ± 10 digits.

Change the frequency to 20kHz and adjust C17 pcb 15 for a reading of 100.000V ± 10 digits.
N.B It may be necessary to short links A, B or C to bring this range into calibration if the initial range of C17 is inadequate.

Repeat the above until both readings are correct.

1.6 10V Range Calibration
Select: SLOW

Feed in 10V at 400Hz on the 10V range when the reading should be 10.000V ± 15 digits.

Change the frequency to 20kHz and adjust C23 pcb 15 for a reading of 10.0000V ± 10 digits. It may be necessary to modify link D to obtain the correct range of C23.

Change the frequency to 10kHz when the reading should be 10.0000V ± 40 digits.

Repeat the above until both readings are correct.

1.7 1000V Range Calibration
Select: SLOW

Feed in 500V at 400Hz on the 1000V range and adjust RV2 pcb 15 for a reading of 500.00V ± 20 digits.

Change the frequency to 20kHz and adjust C16 pcb 15 for a reading of 500.00V ± 20 digits.

1.8 Auto Range Checks
Select: AC and AUTO

Feed in the voltages as shown in the table below at 400Hz checking the voltmeter lies on the correct range.

INPUT	90mV	900mV	9V	90V	500V
RANGE	100mV	1V	10V	100V	1000V

2. AC FINAL CALIBRATION

The following calibration should be carried out with the instrument in an ambient temperature of 20°C after it has received the final dc calibration. Recheck the μV zero setting on the 100mV dc range with input high connected to low.

2.1 Voltage Linearity Check
Select: AC, SLOW, 1V RANGE

Feed in 1V at 400Hz and adjust RV2 pcb 14 for a reading of 1.00000V ± 5 digits.

Reduce the input to 0.1V and adjust RV3 pcb 14 for a reading of 0.10005V ± 2 digits.

Repeat the above until both points are correct.

Check out linearity on the 1V range as indicated in the table below.

AC INPUT	0.80000V	0.60000V	0.40000V	0.20000V
READING LIMITS	0.80000V ± 5 digits	0.60000V ± 5 digits	0.40000V ± 5 digits	0.20000V ± 4 digits

2.2 Final Adjustments on all Ranges
Select: AC, SLOW

Carry out the adjustments in the table below in sequency. *N.B. The application of 500V on the 1000V range results in a power dissipation in the 1MΩ input attenuator of 0.25W. The temperature coefficient of the resistor is such that the heating effect of the input power will result in the instrument calibration changing slightly as the resistor temperature increases.

Thus after applying the 500V input allow about 5 minutes for the instrument reading to stabilise at a final value.

Similarly when returning to the 10V or 100V ranges it will be necessary to allow a similar resettling time.

SEQUENCE	RANGE	INPUT	FREQUENCY	ADJUSTMENT	LIMITS
a)	100mV	0.10000V	400Hz	RV1 pcb 14	± 5 digits
b)	100V	100.000V	400Hz	RV1 pcb 15	± 10 digits
c)	100V	100.000V	20kHz	C17 pcb 15	± 10 digits
d)				repeat b) and c)	
e)	10V	10.0000V	400Hz	-	± 15 digits
f)	10V	10.0000V	20kHz	C23 pcb 15	± 10 digits
g)				Repeat e) and f)	
h)	1000V	500.00V*	400Hz	RV2 pcb 15	± 20 digits
j)	1000V	500.00V*	20kHz	C16 pcb 15	± 20 digits
k)				Repeat c) and f)	

2.3 Frequency Response Checks on all Ranges
Select: SLOW

Feed in the following voltages at the frequencies indicated checking the readings are within the limits shown.

AC RANGE	AC INPUT	FREQUENCY	LIMITS
	0.1V	40Hz	± 70 digits
	0.1V	2.5kHz	± 20 digits
	0.1V	10kHz	± 30 digits
100mV	0.1V	20kHz	± 60 digits
	0.1V	50kHz	± 200 digits
	0.1V	100kHz	± 400 digits
	0.01V	100kHz	± 100 digits
	0.01V	20kHz	± 12 digits
	1V	40Hz	± 60 digits
	1V	2.5kHz	± 20 digits
	1V	5kHz	± 30 digits
1V	1V	20kHz	± 60 digits
	1V	50kHz	± 200 digits
	1V	100kHz	± 400 digits
	0.1V	100kHz	± 100 digits
	0.1V	20kHz	± 12 digits
	10V	40Hz	± 70 digits
	10V	2.5kHz	± 50 digits
	10V	5kHz	± 50 digits
10V	10V	20kHz	± 60 digits
	10V	50kHz	± 200 digits
	10V	100kHz	± 400 digits
	1V	100kHz	± 100 digits
	1V	20kHz	± 12 digits

AC RANGE	AC INPUT	FREQUENCY	LIMITS
	100V	2.5kHz	± 50 digits
	100V	10kHz	± 50 digits
100V	100V	20kHz	± 60 digits
	100V	50kHz	± 200 digits
	100V	100kHz	± 400 digits
	10V	100kHz	± 100 digits
	10V	20kHz	± 15 digits
	100V	20kHz	± 12 digits
	100V	100kHz	± 100 digits
	500V	50kHz	± 100 digits
1000V	500V	40kHz	± 100 digits
	500V	20kHz	± 30 digits
	500V	10kHz	± 25 digits
	500V	2.5kHz	± 20 digits