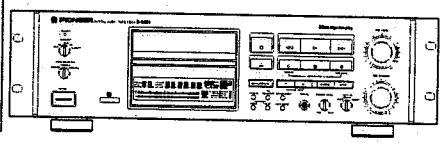
PIONEER®
The Art of Entertainment

Service Manual



ORDER NO.
RRV1350

DIGITAL AUDIO TAPE DECK
D-9601

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model	Power Requirement	The voltage can be converted by the following method.
	D-9601		
IUEW	○	AC100V/120V/230V	With the voltage selector

● **For the "DAT FORMAT" technical information, refer to the service guide ARP2338 for D-500.**

CONTENTS

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T-DFG JULY 1995 Printed in Japan

1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).
When servicing or handling circuit boards and other components which contain lead in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols (fast operating fuse) and/or (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible (fusible de type rapide) et/ou (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

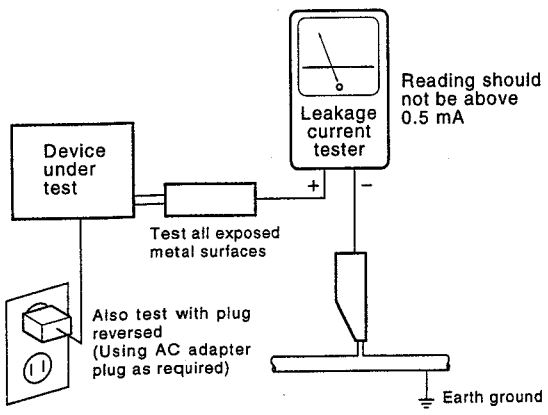
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60 Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5 mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage , etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

2. SPECIFICATIONS

Type ..... Rotating-head type digital audio recorder
Tape speed. ..... Only 4.075 mm/s (LP) playback
8.15mm/s (SP)
16.3mm/s (HS)
Recording time (using a standard 120-min. tape)
..... SP: Maximum 120 minutes
HS: Maximum 60 minutes
Number of channels ..... 2-channel stereo
Number of quantum bits ..... 16-bit linear
Sampling frequency ..... 48kHz (Record/Playback)
44.1kHz (Record/Playback)
32kHz (Playback)
96kHz (Record/Playback)
88.2kHz (Record/Playback)
Error correction method ..... Double-encoded Reed-Solomon code
Modulation method ..... 8 – 10 conversion
Emphasis ..... Analog recording: OFF fixed
Playback: Auto-select
Head ..... AT-construction sendust head
Recording frequency characteristics .. HS (fs = 96kHz): 20 – 44kHz
HS (fs = 88.2kHz): 20 – 40kHz
SP (fs = 48kHz): 20 – 22kHz(±0.5dB)
SP (fs = 44.1kHz): 20 – 20kHz(±0.5dB)
SN ratio ..... 90dB or more
Dynamic range ..... 90dB or more
Total harmonic distortion ..... 0.006% or less
Wow and flutter ... Within measurement limit (±0.001% W. PEAK)

■ Analog Input/Output Terminals

Line input terminal ..... XLR-3 type;
standard input level: +4dBu
(Recoording level: –12dB)
(Input impedance: 10kΩ)
Line output terminal ..... XLR-3 type;
standard output level: +4dBu
(Recording level: –12dB,playback)
(Output impedance: 100Ω or less)
Headphone output terminal ..... Stereo standard jack 6mmϕ
(Maximum 40mW, load impedance: 32Ω)

■ Digital Input/Output Terminals (AES/EBU Type) (format: EIAJ CP-1201 TYPE Ⅰ)

Input terminal ..... XLR-3 type
(Input impedance: 110Ω,with transformer)
Output terminal ..... XLR-3 type
(Output impedance: 110Ω or less,with transfgormer)

■ Digital Input/Output Terminals (IEC958Type) (format : EIAJ CP-1201 TYPE Ⅱ)

Input terminal ..... RCA; 0.5V p-p (Input impedance: 75Ω)
Output terminal ..... RCA; 0.5V p-p (Output impedance: 75Ω)

■ Remote Control Terminal

Parallel remote terminal ..... 8-pin DIN connector
Serial remote terminal
..... 9-pin D-Subconnector x 2 (input/output use)
(Corresponding to RS-422A)

■ Power Source / Others

Power source ..... AC100V/120V/230V (selection), 50/60Hz
Power consumption 44W
External dimensions ..... 483(W) x 137(H) x 377(D)mm
19(W) x 5-3/8(H) x 14-7/8(D)in.
Weight 7.6kg (16lb 12oz)

■ Accessories

Power cable for the US (color: gray) 1
Power cable for Japan (color: black) 1
Operating Instructions 1
Wireless remote control unit 1

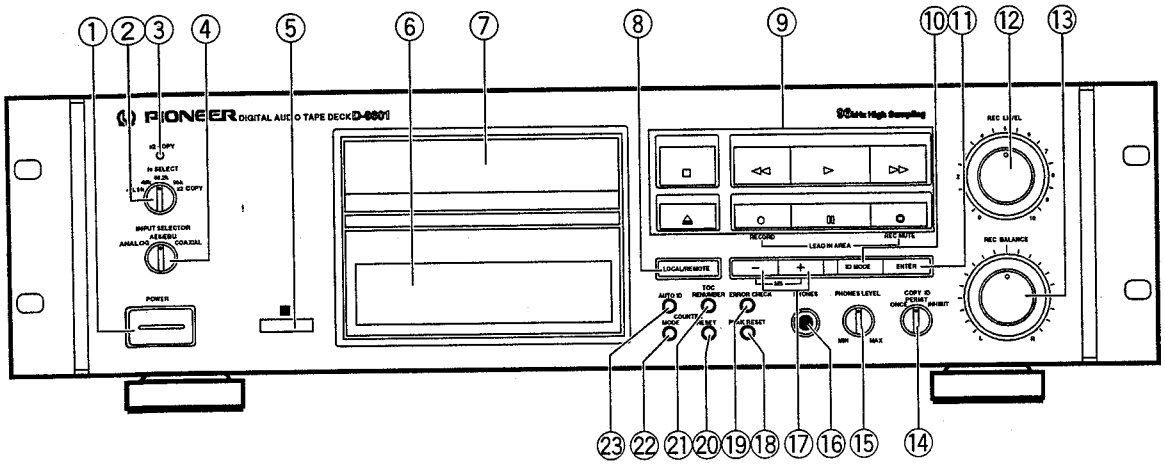
NOTE:

- *The accessory power cables can only be used on the continent of North America and in Japan. In Europe, do not use the accessory power cables. Consult with a company sales representative. Use Only Safety-Licensed Power Cables.*
- *The batteries for the remote control are not included. Please prepare two AAA (R03) batteries.*

- *Specifications and design are subject to possible modifications without notice, due to improvements.*

3. PANEL FACILITIES

FRONT PANEL



① Power Switch (POWER)

Operation starts about 4 seconds after the power has been turned ON.

② fs Select Switch (fs SELECT)

44.1k: Records in Standard Mode of 44.1kHz sampling frequency when an analog signal is being input.

48k: Records in Standard Mode of 48kHz sampling frequency when an analog signal is being input.

88.2k: Records in High Sampling Mode of 88.2kHz sampling frequency when an analog signal is being input.

96k: Records in High Sampling Mode of 96Hz sampling frequency when an analog signal is being input.
High Sampling recording (88.2k or 96k) in a wide range above 40kHz is possible, but the recording time is reduced to half that of Standard Mode.

x2 COPY: This position is selected when a digital copy of a tape with a sampling frequency of 44.1kHz or 48kHz is made at double speed.

③ Double-Speed Digital Copy Mode Indicator (x2 COPY)

Lights up when Double-Speed Copy Mode is selected.

④ Input Selector Switch (INPUT SELECTOR)

Selects the recording source input terminal.

ANALOG: When recording from a unit connected to a line input terminal;

AES/EBU: When recording from a unit connected to a Canon-type digital input terminal (XLR-3 type).

COAXIAL: When recording from a unit connected to a coaxial digital input terminal (IEC958, RCA terminal).

⑤ Remote Control Light-Receiving Part

Receives light from the Wireless Remote Control.

⑥ Display

(Refer to Page 6.)

⑦ Cassette Tray

The cassette tray slides in and out of the unit according to the operation of the OPEN/CLOSE button (⏏).

⑧ LOCAL/REMOTE Selector Button (LOCAL/REMOTE)

LOCAL Mode: Accepts operations performed with the buttons on the unit, with a parallel remote control, and with the Wireless Remote Control.

REMOTE Mode: Accepts commands only from the RS-422. At this time, the key lock indicator (▮▮▮▮▮▮▮▮) will light.

- When switching from REMOTE Mode to LOCAL Mode, keep the button depressed until the key lock indicator (▮▮▮▮▮▮▮▮) goes out(about 2 seconds).
- The mode prior to turning the power OFF will be stored in memory even after the power has been turned OFF.
- With operation of unit buttons, parallel remote control, or wireless remote control at the time of REMOTE mode, flashing display of "REMOTE" will be made at the counter display part to indicate that the operation will not be accepted.

⑨ Operation Buttons

⏏ **: OPEN/CLOSE button**
Used to eject or insert a tape.

■ **: STOP button**
Stops movement of the tape.

◀◀ **: REWIND button**
Rewinds the tape. When pressed during Playback, REVIEW operation is engaged.

▶▶ **: FAST FORWARD button**
Fast-forwards the tape. When pressed during Playback, CUE operation is engaged.

▶ **: PLAY button**
Used to play back a tape or start recording (after the RECORD button has been operated).

●: RECORD button

When pressed, Record Mode (Record Standby status) is engaged, and the REC indicator and PAUSE (II) indicator are illuminated.

To start recording, press either the PLAY (►) button or PAUSE (II) button.

II: PAUSE button

Temporarily stops tape operation during Record or Playback. When pressed again, operation is resumed. The tape cannot be paused during FAST FORWARD or REWIND operation.

O: REC MUTE button

Creates and records a blank portion on the tape.

⑩ ID MODE button (ID MODE)

Used for Subcode editing. Selects the desired ID Mode.

⑪ ENTER button (ENTER)

Used for Subcode editing. When pressed, enables storage/deletion of a Subcode selected with the ID MODE button.

⑫ Recording Level knob (REC LEVEL)

Sets the recording level during analog recording.

⑬ Recording Level Balance knob (REC BALANCE)

Adjusts the recording level left-right balance during analog signal input.

⑭ COPY - ID switch (COPY ID)

Sets the SCMS status bit (ID 6) while recording is in progress.

ONCE: Only a first-generation digital copy to a public-use DAT can be made.

PERMIT: Digital copy to a public-use DAT can be performed any number of times.

INHIBIT: Digital copy to a public-use DAT is prohibited.

⑮ Headphone Level knob (PHONES LEVEL)

⑯ Headphone Jack (PHONES)

⑰ Music Search button (MS +, –)

Used for music Search and other operations.

⑱ PEAK RESET button (PEAK RESET)

Resets the holder of the peak margin display. When pressed continuously, the peak margin display changes to real time display.

⑲ ERROR CHECK button

When this button is pressed during Playback, error correction status is displayed in the Counter display part as "E A2 B3", "A" indicates error correction of A head and "B" indicates error correction of B head. (Refer to Page 9.) Return to the original counter display will be made when this button is pressed again or when the COUNTER MODE button is pressed.

⑳ Counter RESET button (Counter RESET)

When the Counter Mode is set to TIME Counter and the RESET button is pressed, the Counter is reset to "0 00 00."

㉑ RENUMBER button (TOC RENUMBER)

Used when re-recording (rearranging) song numbers or recording TOC (Table of Contents) data.

㉒ COUNTER MODE button (COUNTER MODE)

Used when selecting Counter display.

㉓ AUTO ID button (AUTO ID)

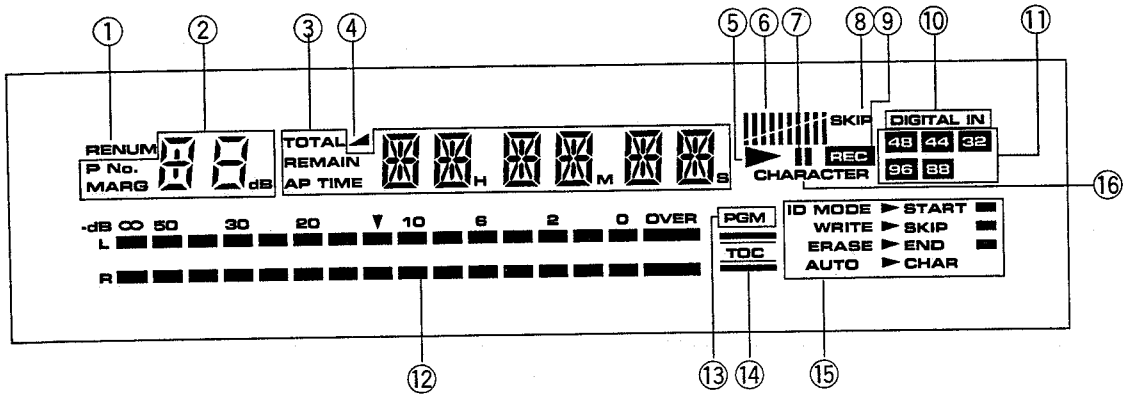
During Record: Used when AUTO ID is recorded automatically.

During Playback: Used when skipping portions you do not want to listen to. (Skips from the SKIP ID to the subsequent START ID.)

Also, when a character pack has been read during playback, this is used to switch the scroll display of the counter display part on and off.

- The input mode prior to turning the power OFF will be stored in memory even after the power has been turned OFF.

DISPLAY



① Renumber Indicator (RENUM)

② Peak Margin (MARG)/Program Number (P.No.) Indicator

③ Counter Indicator

Displays tape running time data such as absolute time (A-TIME), program time (P-TIME), and remaining time (REMAIN), and character data such as the Character Pack, operation display, etc.

④ Character Data Remaining Indicator

Indicates that undisplayed character data are on the left side in Character Input Mode.

⑤ Play Indicator (►)

⑥ Key Lock Indicator

Indicates that button operation is not possible (when REMOTE is selected with the LOCAL/REMOTE button). Only RS-422 operations are possible.

⑦ Pause Indicator (II)

⑧ SKIP Indicator (SKIP)

Indicates that SKIP Play is ON.

⑨ Record Indicator (REC)

⑩ Digital Input Indicator (DIGITAL IN)

Indicates that digital input (COAXIAL or AES/EBU) has been selected.

⑪ Sampling Frequency Indicator

This indicates the present sampling frequency. When the signal is interrupted during digital input recording, repeated flashing indication will be made in the sequence of 48→44→96→88.

⑫ Record/Play Level Indicator

OVER: Lights up when the input level is too high. At this time the Peak Margin display flashes 00dB (during analog signal input).

⑬ PGM Indicator

Indicates that a one-point memory has been recorded (flashing indication).

⑭ TOC Indicator

Indicates that TOC data have been read from the tape. Flashes when TOC data are being written or read.

⑮ ID Indicator

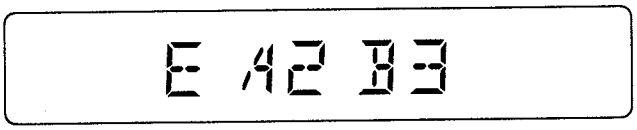
ID MODE	: Indicates type of ID Mode.
►	: Indicates selected ID Mode.
■	: Indicates detected ID.
WRITE	: Indicates that ID Write Mode is engaged.
ERASE	: Indicates that ID Erase Mode is engaged.
AUTO	: Indicates that Auto ID Write is ON during Record.

⑯ Character Indicator (CHARACTER)

Indicates that Character data from the tape have been read.

Error Check Indicator

When the ERROR CHECK button is pressed during Playback, error correction status is displayed in the Counter display part.

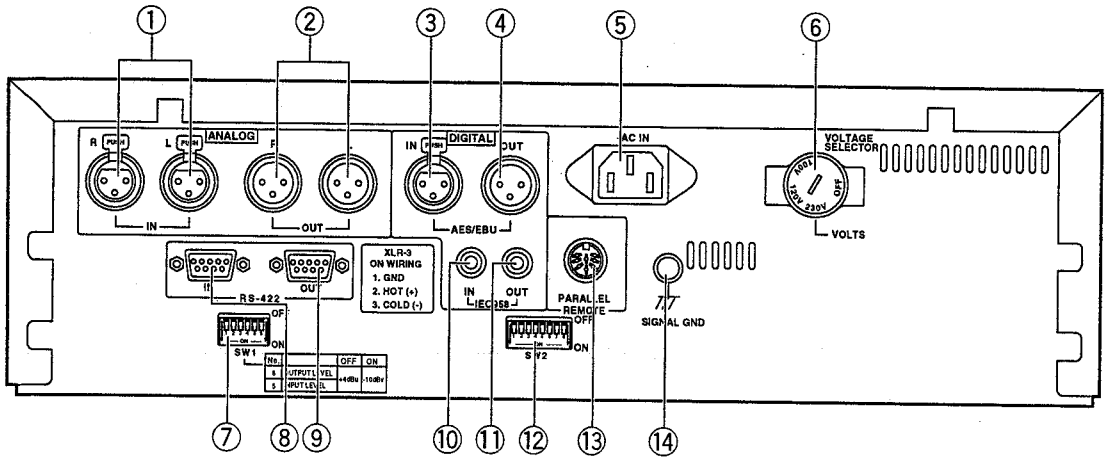


Both Head A and Head B are displayed, accompanied by a number from 0 – 9. Error correction is 10% of the number displayed; "9" indicates an error that is practically uncorrectable. In this case the head may be dirty, so use of a head cleaner is recommended.

NOTE:

• 9 will be displayed when an unrecorded tape is played back.

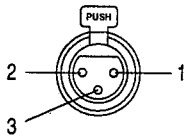
REAR PANEL



Always switch off the power switch before connecting equipment or changing connections.

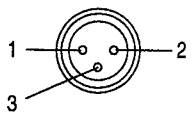
① Analog Input Terminal (ANALOG IN L/R)

Analog audio signal (L/R) input terminal. It is a Canon-type (XLR-3-31) terminal with balanced input. The terminal polarity is: No. 1 pin: GND; No. 2 pin: HOT (+); No. 3 pin: COLD (–).



② Analog Output Terminal (ANALOG OUT L/R)

Analog audio signal (L/R) output terminal. It is a Canon-type (XLR-3-32) terminal with balanced output. The terminal polarity is: No. 1 pin: GND; No. 2 pin: HOT (+); No. 3 pin: COLD (–).



③ AES/EBU Digital Input Terminal (DIGITAL AES/EBU IN)

Input terminal for digital audio signal in AES/EBU format (pro format).

- Use the cable for the digital signal.

④ AES/EBU Digital Output Terminal (DIGITAL AES/EBU OUT)

Output terminal for digital audio signal in AES/EBU format (pro format).

- Use the cable for the digital signal.

⑤ Power Cable Connector (AC IN)

Use an accessory power cable for the US (color:gray) and connect it to a grounded outlet.

NOTE:

The accessory power cables can only be used on the continent of North America and in Japan. In Europe, do not use the accessory power cables. Consult with a company sales representative. Use Only Safety-Licensed Power Cables.

⑥ Voltage Selector Switch (VOLTAGE SELECTOR)

Before using the unit, set the power source and voltage within the service range of the unit. (Refer to the front cover.)

- The factory setting is 120V.

⑦ DIP Switch (SW1)

Use for the following settings:

1. Down converter
2. Test Mode (Keep in OFF position.)
3. Test Mode (Keep in OFF position.)
4. Wireless Remote Control ON/OFF selection
5. Output level selection
6. Input level selection

⑧ RS-422 Input Terminal (RS-422 IN)

Input terminal for controlling unit in this unit with a 9-pin serial interface.

- Since this is a 9-pin D-SUB connector, make sure you use this type of cable.

⑨ RS-422 Output Terminal (RS-422 OUT)

Output terminal for control of several units, including this unit, with a 9-pin serial interface.

- Since this is a 9-pin D-SUB connector, make sure you use this type of cable.

⑩ IEC 958 Coaxial Digital Input Terminal (DIGITAL IEC 958 IN)

RCA pin-type input terminal for digital audio signal in a public-use format.

4. DISASSEMBLY

■ DAT MECHANISM ASSEMBLY

1. Remove the bonnet.
2. Remove the flexible P. C. boards CN3, CN4, and CN5 of the MAIN unit, the connectors CN6, CN7, and CN8, and CN2 of the RF unit.
3. Remove the five screws ①, and remove the loading mechanism while raising the rear part of the DAT mechanism assembly. (Refer to Fig. 1.)
4. Remove the two flexible P. C. boards and the connector wiring material from the groove of part Ⓐ. (Refer to Fig. 2.)
5. Remove the four screws ② and the four mechanism mounting springs, and then remove the DAT mechanism assembly from the cassette installation unit. (Refer to Fig. 2.)

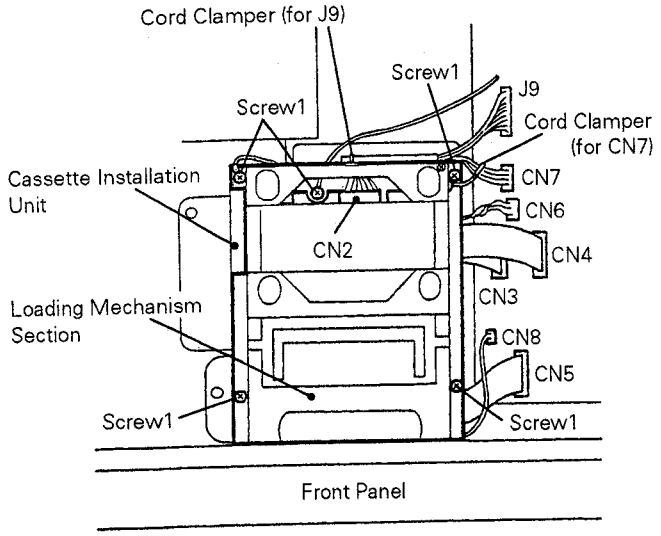


Fig. 1

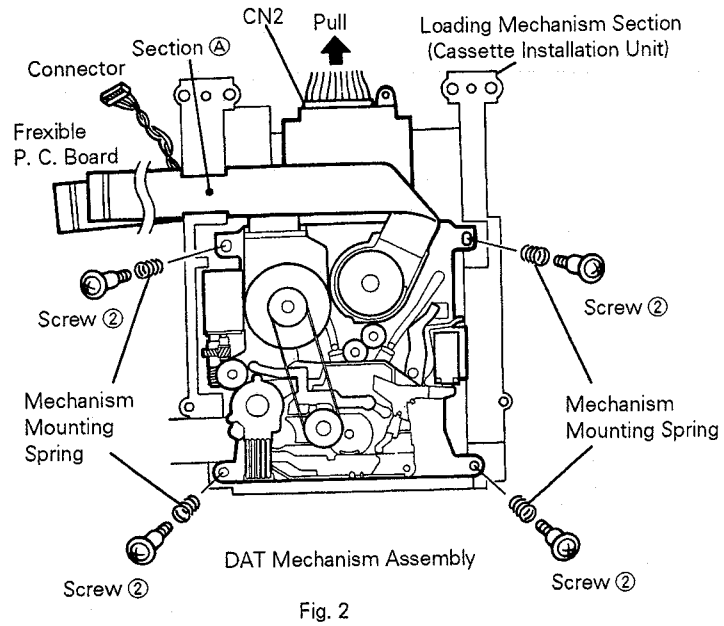


Fig. 2

Preparations before adjustment (at the time of pull guide adjustment)

1. Remove the cassette installation unit and the wiring material of the DAT mechanism assembly from the MAIN unit.
2. Remove the DAT mechanism assembly from the cassette installation unit.
3. Place the DAT mechanism assembly so onto the mechanism stay that the motor pulley at the lower surface does not come into contact with other parts, and then fix the shield case of the DAT mechanism assembly with screws. (Refer to Fig. 3.)
4. Insert the DAT mechanism assembly and the wiring material of the installation unit into the MAIN unit. (Adjustment of the DAT mechanism assembly is executed in this condition.)

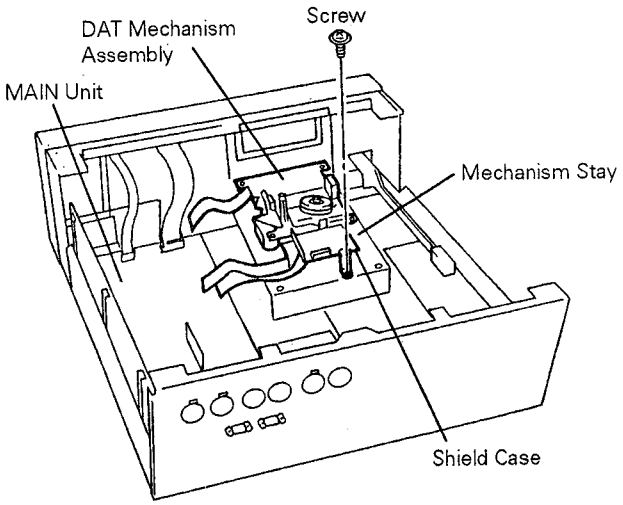


Fig. 3

5. REPLACING MAIN PARTS IN THE MECHANICAL SECTION

5.1 REPLACING THE DRUM

< Removing >

1. Cut the wire clamp and disconnect connector CN1.
2. Remove three screws ① and screw ② to remove the rotating drum assembly.

Note: Do not touch the outer surface of the drum.

< Re-installing >

1. Use the removal procedure in the reverse sequence. However, be sure to tighten three screws ① counterclockwise starting from position Ⓐ with torque of 1kgcm as shown in Fig. 5–1.

Note: After replacement, be sure to perform the tape pass adjustment, TACH adjustment, and record current adjustment.

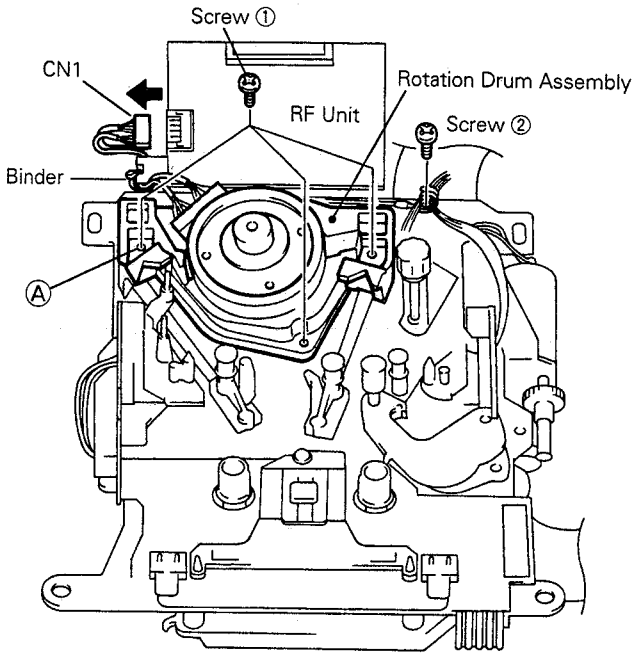


Fig. 5–1

5.2 REPLACING THE CAPSTAN DD MOTOR UNIT

< Removing >

1. Remove rubber belt ①.
2. Remove three screws ② to remove the capstan DD motor unit.

< Re-installing >

1. Use the removal procedure in the reverse sequence.

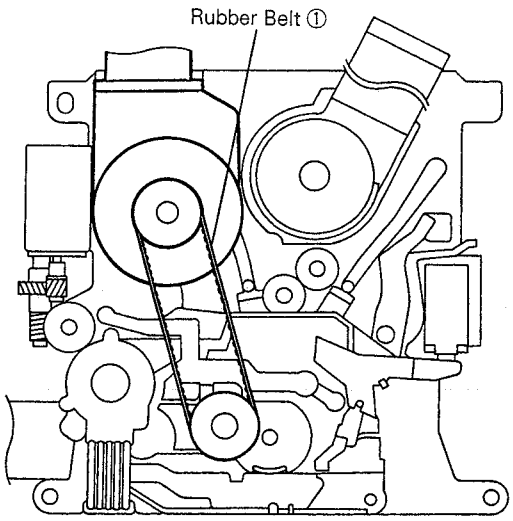


Fig. 5–2

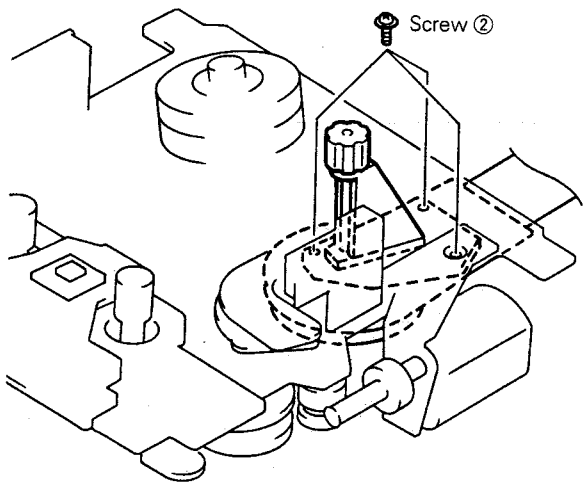


Fig. 5–3

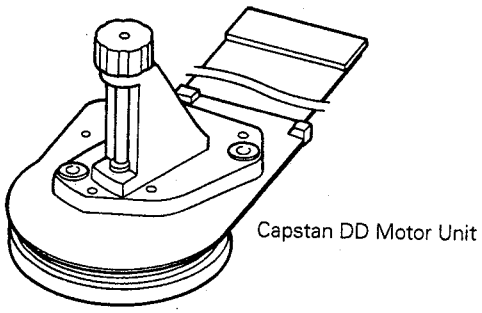


Fig. 5–4

5.3 REPLACING THE PINCH ROLLER

< Removing >

1. Remove the poly-slider washer at the upper section of the pinch roller using the edge of a precision screwdriver.

Note : Care must be taken to prevent deforming the pinch arm assembly.

< Re-installing >

1. Insert the pinch roller on the pinch arm assembly and press-fit the poly-slider washer to the pinch roller.

Note : Pay attention to prevent dust (especially, magnetic powder) from adhering to the pinch roller. Use a new poly-slider washer after replacing the pinch roller.

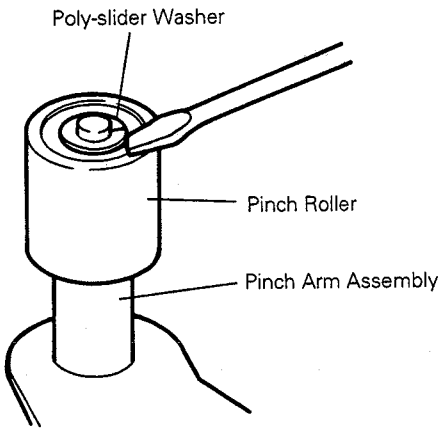


Fig. 5–5

5.4 REPLACING THE POWER MOTOR

< Removing >

1. Loosen the clamp to remove the wiring.
2. Remove one screw ① to remove the motor bracket from the chassis.
3. Remove poly-slider washer ② using a screwdriver and extract the worm gear.
4. Remove two screws ③ to remove the power motor.

< Re-installing >

1. Use the removal procedure in the reverse sequence.

Note : After replacing the motor, be sure to press-fit a new motor gear. Do not change the clamp screw direction.

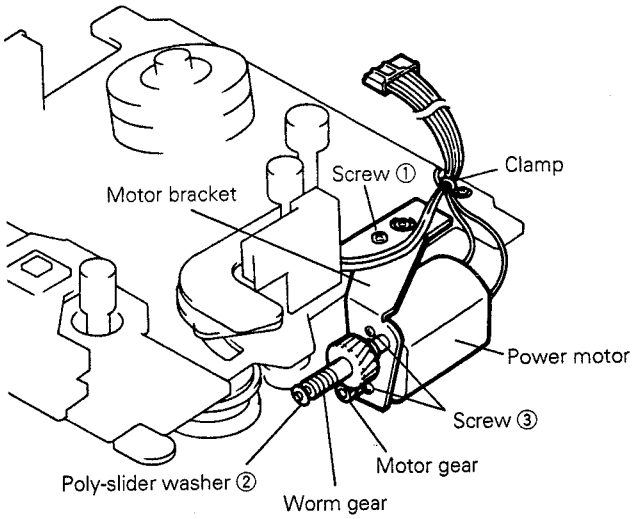


Fig. 5–6

5.5 REPLACING THE PLUNGER SOLENOID

< Removing >

1. Melt and remove solder Ⓐ connecting the end sensor PCB and reel PCB.
2. Remove one screw ① to remove the end sensor PCB. Melt and remove the solder connecting the solenoid lead wire to the end sensor PCB, and remove the wire from the end sensor PCB.
3. Remove two screws ② to remove the plunger solenoid.

< Re-installing >

1. Use the removal procedure in the reverse sequence.

Note : After re-installation, press-fit the solenoid to the hook section of the end sensor bracket.

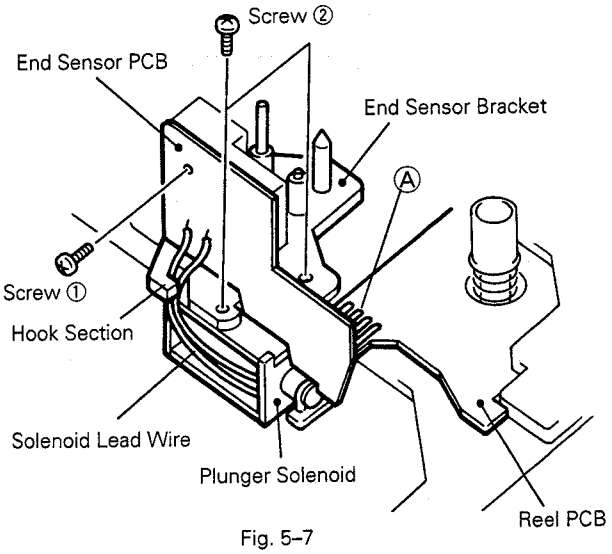


Fig. 5–7

5.6 REMOVING/RE-INSTALLING THE REEL BASE ASSEMBLY

< Removing >

1. Set the mode to unthreading.
2. Remove the rubber belt.
3. Remove one screw ① fixing the encoder.
4. Remove four screws ② to remove the reel base assembly.

< Re-installing >

1. Use the removal procedure in the reverse sequence.

Notes :

- *When re-installing the reel base assembly in the chassis, move the mode plate to the leftmost side viewed from the rear side.*
- *When re-installing the encoder, match the convex of the encoder shaft to the concave. (See page 12.)*

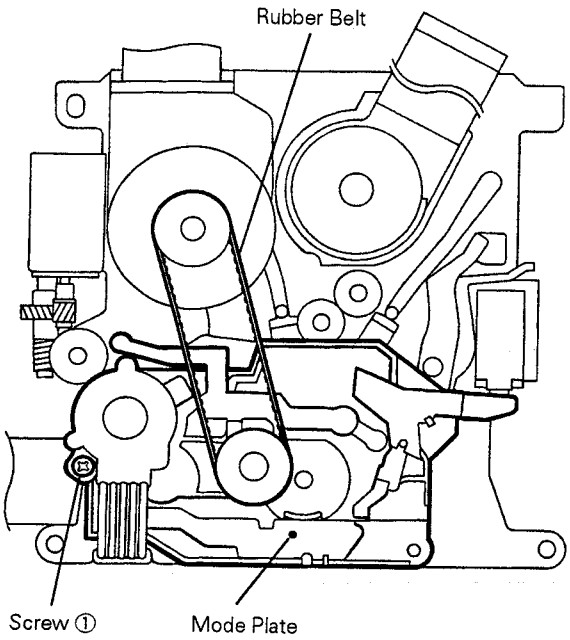


Fig. 5–8

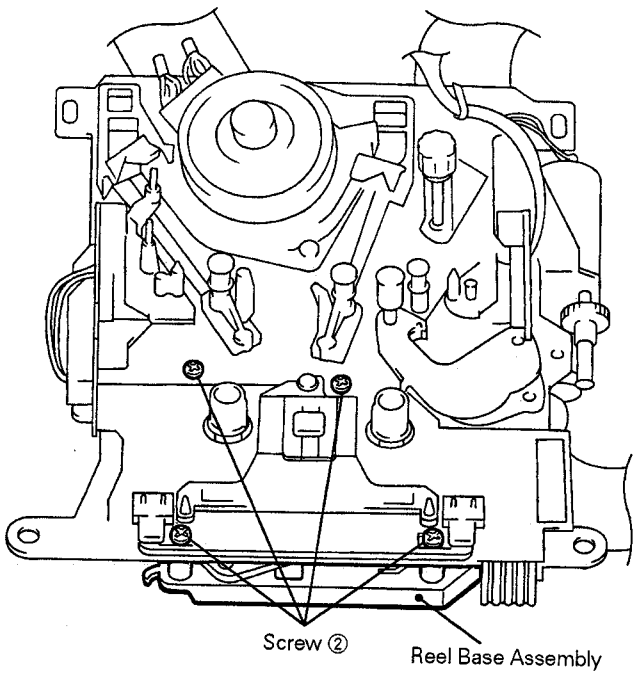


Fig. 5–9

5.7 ALIGNING THE GEARS

1. Align the gears with care using the mark position on each gear.

Note : Set the unthreading mode before gear alignment.

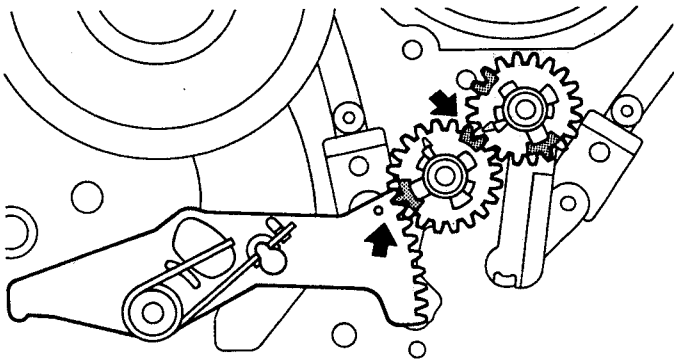


Fig. 5–10

Aligning the Interval Gear

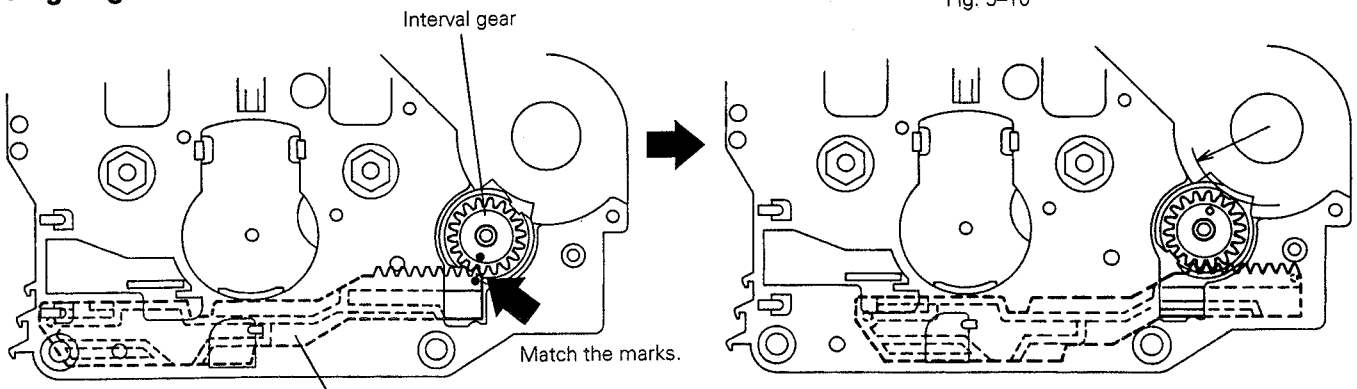


Fig. 5–11

5.8 NOTE

When tightening the switch screw, care must be taken to prevent giving torque exceeding 1 kg · cm.

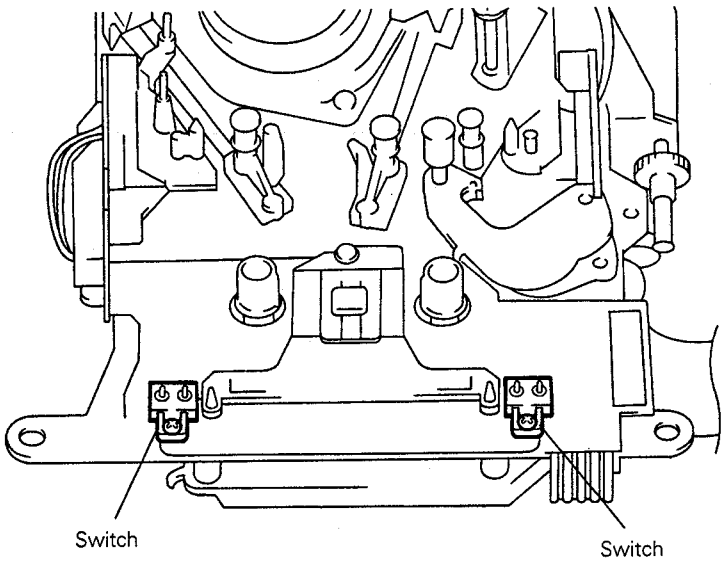


Fig. 5–12

6. EXPLODED VIEWS, PACKING AND PARTS LIST

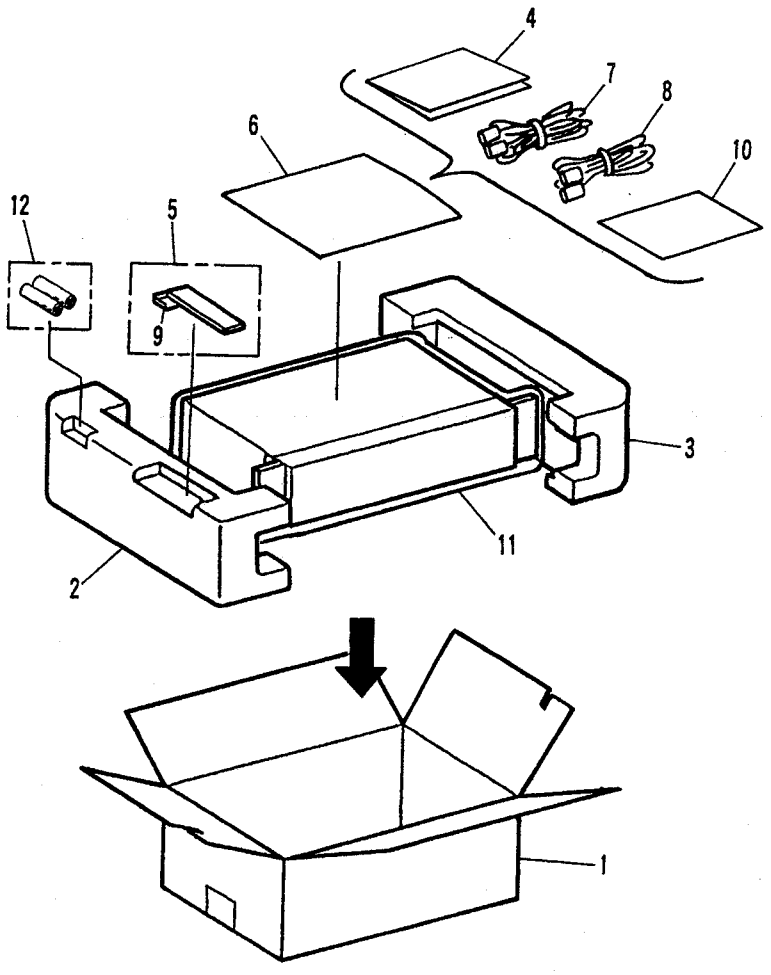
NOTES :

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

6.1 PACKING

Parts List

Mark	No.	Description	Parts No.
	1	PACKING CASE	RHG1682
	2	PAD (L)	RHA1182
	3	PAD (R)	RHA1183
	4	OPERATING INSTRUCTIONS (English)	RRB1165
	5	REMOTE CONTROL UNIT	RPX1075
	6	POLY. BAG	Z21–040
⚠	7	AC POWER CORD (with PLUG)	DDG1028
⚠	8	AC POWER CORD	ODG1003
	9	BATTERY COVER	PZN1010
	10	LABEL	RRN1008
	11	MIRROR MAT	DHL1006
NSP	12	BATTERY (R03, AAA)	VEM–022

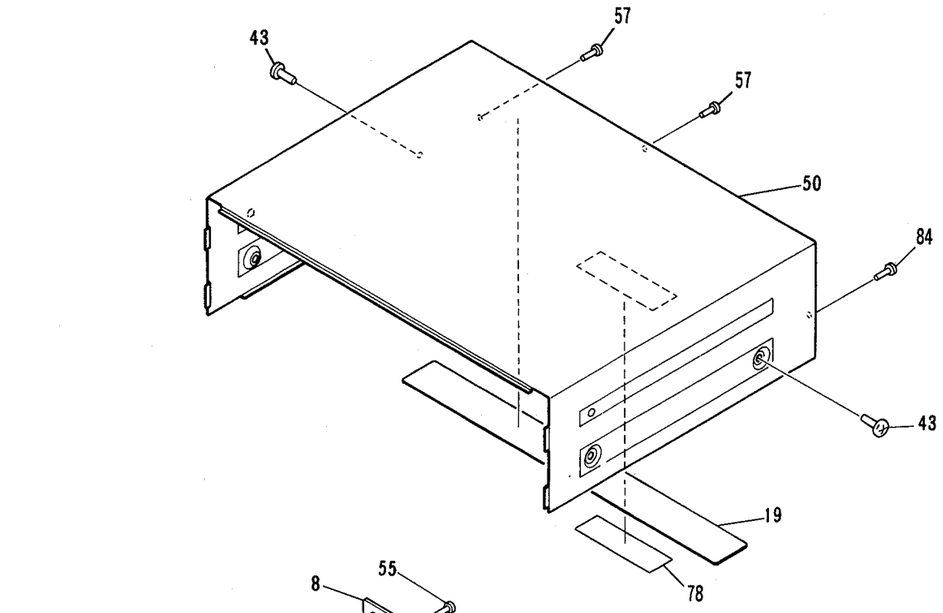


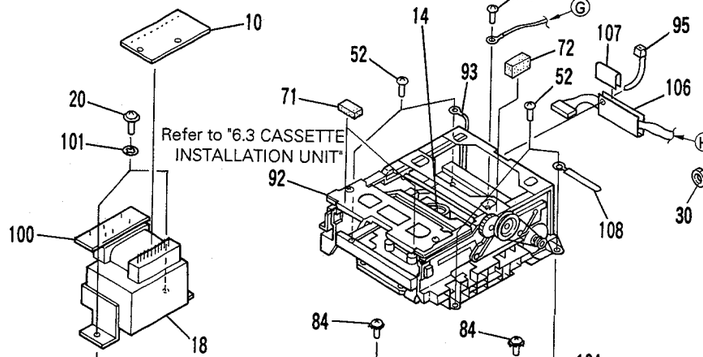
6.2 EXTERIOR

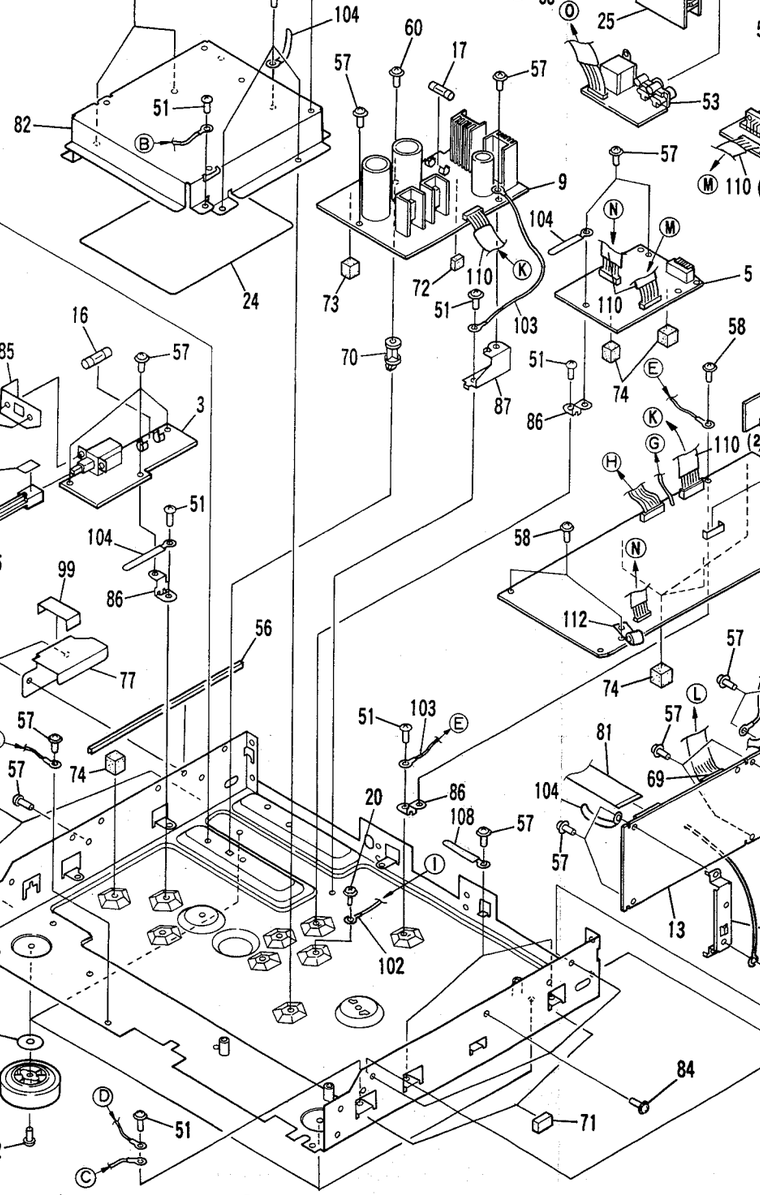
Parts List

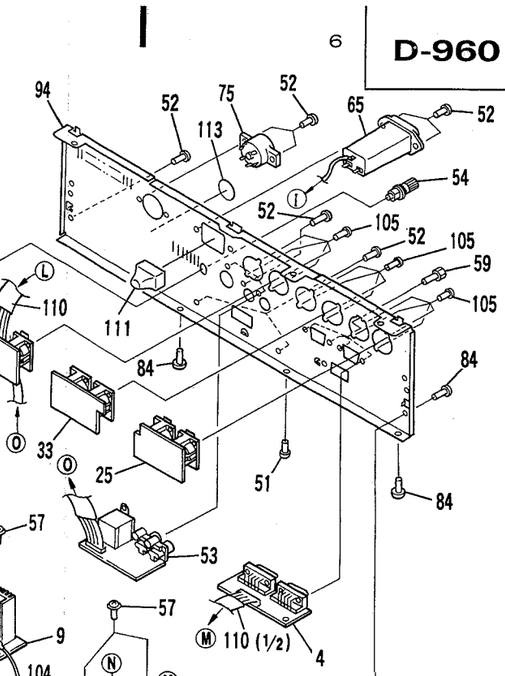
Mark	No.	Description	Parts No.
	1	MAIN UNIT	RWZ3471
	2	HEADPHONE UNIT	RWZ3478
⚠	3	POWER SW UNIT	RWZ3479
NSP	4	D-SUB UNIT	RWZ3609
	5	RS422 CONTROL UNIT	RWZ3608
NSP	6	VR UNIT	RWZ3485
	7	DISPLAY UNIT	RWZ3484
NSP	8	SW UNIT	RWZ3482
	9	POWER UNIT	RWZ3481
	10	TRANS B UNIT	RWZ3486
NSP	11	COPY ID UNIT	RWZ3483
NSP	12	LED UNIT	RWZ3487
	13	INTERFACE UNIT	RWZ3475
	14	DAT MECHA ASSY	EXK9003
	15	RF ENV UNIT	RWZ3472
⚠	16	FUSE (T1.6A, FU2)	REK1100
⚠	17	FUSE (T3.15AH250V, FU1)	AEK1059
⚠	18	POWER TRANSFORMER (T1)	RTT1290
	19	DAMPER PLATE B	PNB1109
	20	SCREW (FE)	RBA1099
	21	ARM SPRING	RBH1143
	22	GEAR SPRING	RBH1191
	23	BONNET CUSHION	REB1193
	24	DAMPER PLATE C	RNC1070
	25	BALANCE IN UNIT	RWZ3473
	26	GEAR	RNK1289
	27	ARM	RNK1290
	28	SCREW	BBT30P100FZK
	29	DOOR HOLDER ASSY	RXA1383
	30	NUT	NK70FUC
	31	INSULATOR ASSY	DXA1490
	32	LED LENS	AMR1160
	33	BALANCE OUT UNIT	RWZ3474
	34	AES-EBU UNIT	RWZ3476
	35	POWER BUTTON	RAC2008
	36	FUNCTION KNOB	RAC2005
	37	SUB FUNCTION KNOB	RAC2006
	38	BALANCE KNOB	RAC2007
NSP	39	RACK MOUNT ANGLE	RNE1879
	40	FL FILTER (PVC)	RAH2125
	41	DOOR PANEL	RAH2614
	42	FL LENS	RAH2127
	43	SCREW (FE)	RBA1117
	44	DOOR STABILIZER	REB1177
	45	DOOR MOLD	RNK2147
NSP	46	CAUTION SEAL	RRW1079
	47	VR KNOB ASSY A	RXA1688
	48	SENSOR ACRYLIC	VNK1566
NSP	49	PCB ANGLE	RNE1834
	50	BONNET	REA1199
	51	SCREW	BBT30P060FCC
	52	SCREW	BBT30P080FCC
	53	DIGITAL I/O UNIT	RWZ3477
	54	EARTH TERMINAL	AKE-039
	55	SCREW	BBZ26P080FZK
NSP	56	EDGING T	PEC1028
	57	SCREW	IBZ30P060FCC
	58	SCREW	IBZ30P080FCC
	59	BOLT #4-40/M2.6	DBA1078
	60	SCREW	IBZ30P150FCC
	61	SCREW	PMA30P060FCU
	62	NUT	RBN-006
	63	WASHER	WT21D050D050
	64	WASHER	WT21D070D050
⚠	65	NOISE FILTER (INLET TYPE)	DTX1002
⚠	66	CONNECTOR ASSY 8P	RKP1736
⚠	67	CONNECTOR ASSY 6P	RKP1741
	68	TAPE	PNM-044
⚠	69	CONNECTOR ASSY 11P	RKP1742
NSP	70	PCB SPACER	PNY-404
	71	RUBBER SPACER (A)	REB1057
	72	FL SPACER	REB1171
	73	RUBBER SPACER	REB1293
	74	SPACER	REB1179
⚠	75	VOLTAGE SELECTOR	RSB1013
NSP	76	VR SHIELD PLATE (PVC)	REC1162
NSP	77	COVER (PVC)	REC1163
	78	65 LABEL	ORW1069
NSP	79	MAIN CHASSIS ASSY	RXA1692
	80	SCREW	BBZ40P180FZK
	81	24P F•F•C/30V	PDD1161
NSP	82	MECHA STAY (FE)	RNC1076
	83	SCREW	ABA1208
	84	SCREW	ABA1207
NSP	85	PS HOLDER	RNE1850
NSP	86	PCB BASE	RNE1849
NSP	87	PCB HOLDER	RNE1848
NSP	88	DOOR STOPPER	RNK1855
NSP	89	EARTH PLATE	RNE1717
NSP	90	PANEL STAY	RNT1223
NSP	91	EARTH PLATE	VNE1164
NSP	92	CASSETTE INSTALLATION UNIT	RXA1470
NSP	93	EARTH LEAD UNIT	XDF-506
	94	REAR PANEL (FE)	RNA1921
	95	BINDER	ZCA-SKB90BK
	96	NAME PLATE (AL)	VAM1032
	97	FRONT PANEL (AL)	RAH2613
NSP	98	SPACER (1)	PNM1056
NSP	99	TAPE (F)	REH1008
NSP	100	TRANS A UNIT	RWZ3480
	101	WASHER	WH40FUC
NSP	102	EARTH LEAD UNIT	RDF1151
NSP	103	EARTH LEAD UNIT	PDF1150
NSP	104	CORD HOLDER BRACKET	RNH1005
	105	SCREW	PMZ26P040FMC
NSP	106	SHIELD PLATE A	PNM1162
NSP	107	TAPE (L)	REH1014
	108	CORD CLAMPER	RNH-184
NSP	109	CABLE CLIP	REC1259
	110	SHIELD (AL) 210L	PDM1006
NSP	111	LAPPING COVER	REB1069
⚠NSP	112	FERRITE CLAMP	DTH1159
	113	GROUND LABEL	DRW1518

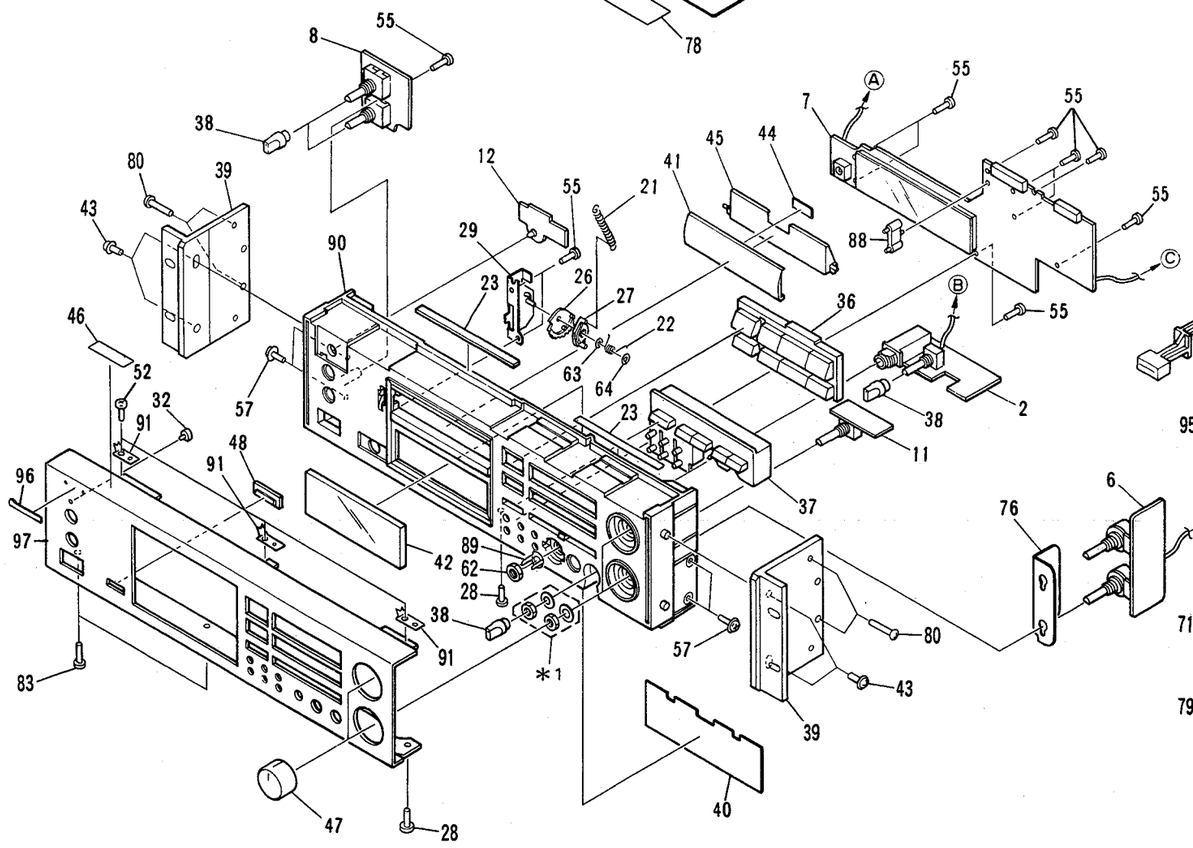
● Exterior









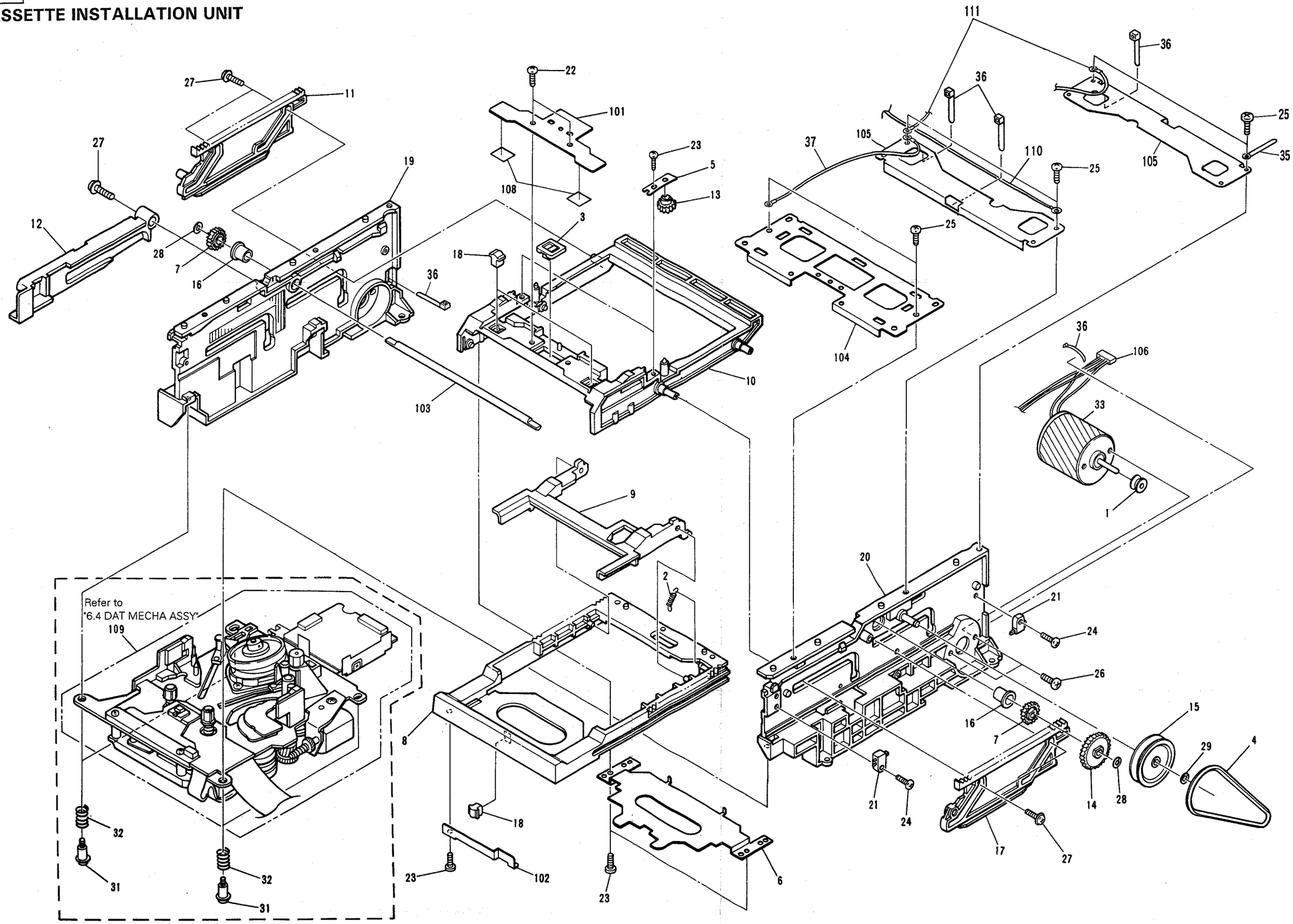


NOTE : Screws adjacent to ▼ mark on the product are used for disassembly.

*1: These washers and nuts are accessories for the SEL SW volume used for the COPY ID UNIT and the VR UNIT.

Note : Three shrink shields No.110 are used.
Ⓚ and Ⓜ are used cut in half.

6.3 CASSETTE INSTALLATION UNIT



Note : Parts encircled with [---] are not included in the Cassette installation unit.

Parts List

Mark	No.	Description	Parts No.
	1	MOTOR PULLEY	PNW1634
	2	SPRING	RBH1279
	3	HALF DAMPER	REB1033
	4	BELT	REB1140
	5	GEAR STOPPER	RNE1394
	6	CONTAINER PLATE	RNE1395
	7	GEAR	RNK1272
	8	TRAY	RNK1876
	9	FLAP	RNK1649
	10	CONTAINER	RNK1650
	11	MAIN RACK PLATE L	RNK1653
	12	LEVER	RNK1657
	13	GEAR	RNK1658
	14	GEAR A	RNK1659
	15	PULLEY GEAR	RNK1660
	16	COLLAR	RNK1661
	17	MAIN RACK PLATE R	RNK1664
	18	HALF HOLDER	RNK1711
	19	SIDE PLATE L ASSY	RXA1356
	20	SIDE PLATE R ASSY	RXA1357
	21	PUSH SWITCH (S2001, S2002)	RSF1008
	22	SCREW	BBZ20P040FMC
	23	SCREW	BBZ20P060FZK
	24	SCREW	BBZ20P080FMC
	25	SCREW	BBZ26P060FMC
	26	SCREW	BMZ30P040FMC
	27	SCREW	PBA1035
	28	WASHER	WT21D050D025
	29	WASHER	WT26D047D050
	30	.....	
	31	SCREW	PBA1002
	32	SPRING	RBH1125
	33	LOADING MOTOR	VXM1034
	34	.....	
	35	CORD CLAMPER	RNH-184
	36	BINDER	Z09-056
	37	EARTH LEAD UNIT	XDF-502

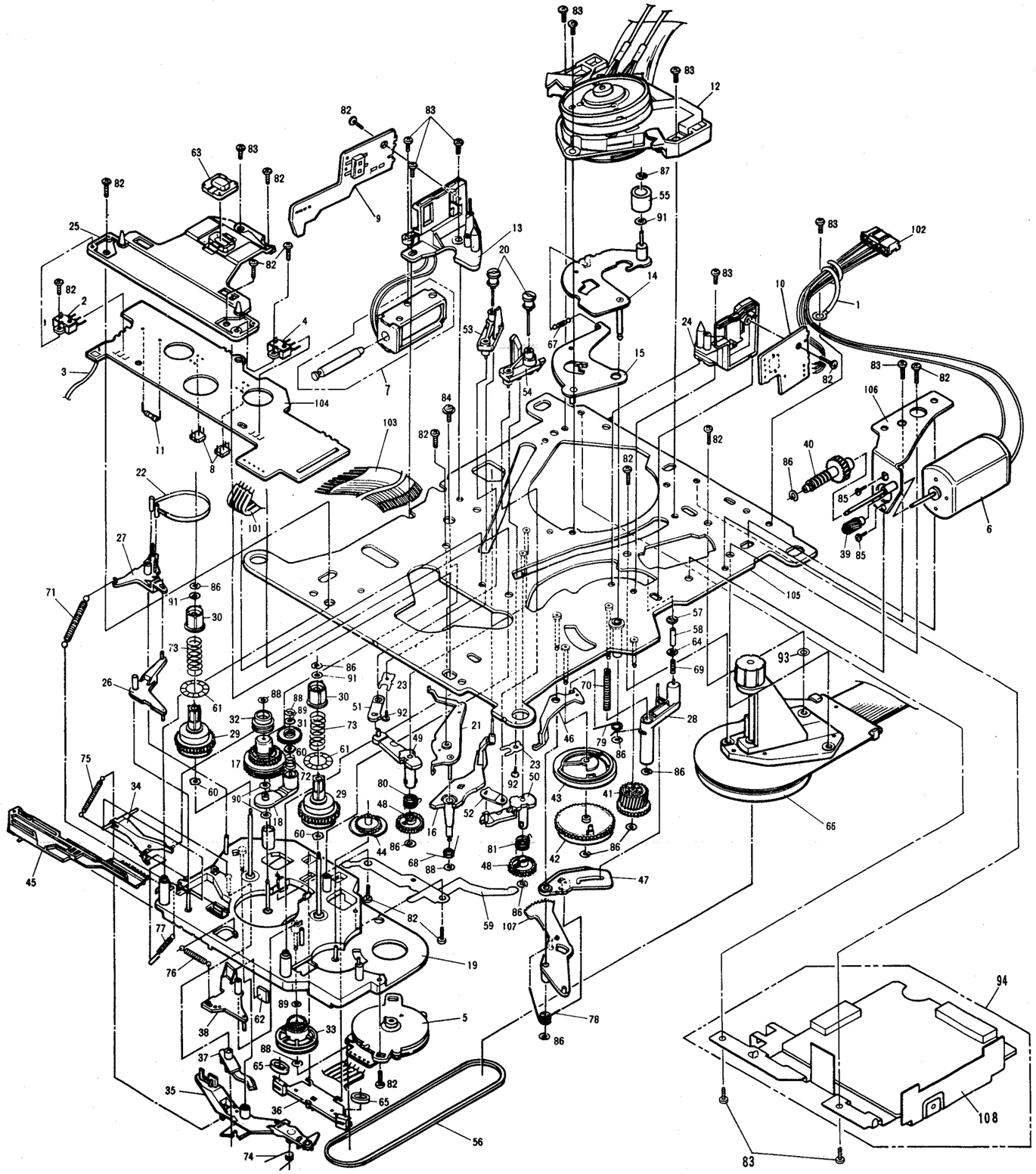
Mark	No.	Description	Parts No.
NSP	101	SPRING	RBK1035
NSP	102	SPRING (TRAY)	RBK1036
	103	SHAFT	RLA1152
NSP	104	TOP PLATE	RNE1396
NSP	105	REAR STAY	RNE1397
NSP	106	CONNECTOR ASSY 6P	RKP1433
	107	.....	
NSP	108	TAPE	PNM1017
	109	DAT MECHA ASSY	EXK9003
NSP	110	EARTH LEAD UNIT	XDF-506
NSP	111	EARTH LEAD UNIT	XDF-501

6.4 DAT MECHA ASSY (EXK9003)

Parts List

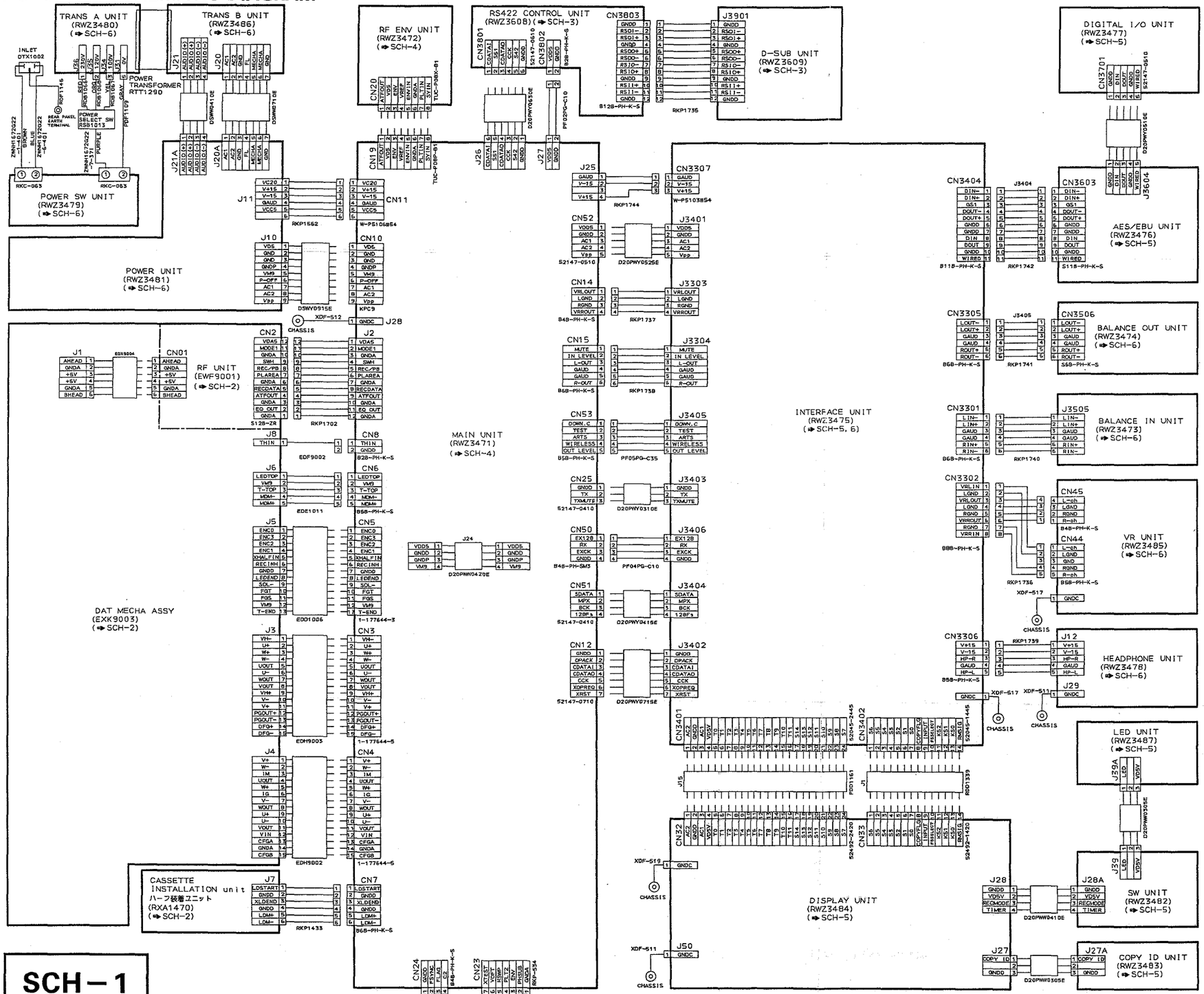
Mark	No.	Description	Parts No.
	1	CLAMPER	HEF-102
	2	SWITCH (S102)	ESG9001
NSP	3	CONNECTOR (J8)	EDF9002
	4	SWITCH 2P (S101)	ESG1001
	5	ENCODER ASSY	ESX1001
	6	POWER MOTOR	CXM1020
	7	SOLENOID	EXP1007
	8	PHOTO REFLECTOR (Q101, Q102) (REEL SENSOR)	GP2S24C
	9	PHOTO REFLECTOR ASSY (Q103) (END SENSOR)	EXX1023
	10	PHOTO REFLECTOR ASSY (Q104) (TOP SENSOR)	EXX1022
	11	RESISTOR (R101)	RD1/4PM431J
	12	DRUM ASSY	EXH9011
	13	BRACKET L ASSY	EXA1117
	14	PINCH ARM ASSY	EXA1118
	15	PINCH DRIVE ARM ASSY	EXA1119
	16	TR ARM ASSY	EXA1122
	17	DRIVE GEAR ASSY	EXA1123
	18	SWING ARM ASSY	EXA1124
	19	REEL BASE ASSY	EXA1125
	20	ROLLER GUIDE	EXA1129
	21	TR ARM BRACKET ASSY	EXA1184
	22	TR BAND ASSY	EXA1185
	23	SLIDER PLATE	ENE1006
	24	SENSOR BRACKET R	ENV1236
	25	STABILIZER	ENV1192
	26	TR LEVER	ENV1194
	27	TR BRAKE	ENV1195
	28	PULL ARM	ENV1197
	29	REEL GEAR	ENV1251
	30	REEL HUB	ENV1252
	31	IDLER GEAR	ENV1253
	32	CLUTCH DRUM	ENV1254
	33	PULLEY GEAR	ENV1255
	34	CHANGE ARM	ENV1256
	35	BRAKE LEVER	ENV1257
	36	BRAKE PLATE	ENV1258
	37	CHANGE LEVER	ENV1259
	38	REV BRAKE	ENV1260
	39	MOTOR GEAR	ENV1231
	40	WORM GEAR	ENV1232
	41	WORM WHEEL	ENV1233
	42	DRIVE GEAR	ENV1234
	43	CAM	ENV1235
	44	INTERVAL GEAR	ENV1238
	45	MODE PLATE	ENV1239
	46	HARD BRAKE	ENV1240
	47	DRIVE ARM	ENV1241
	48	THREADING GEAR	ENV1242
	49	THREADING ARM L	ENV1243
	50	THREADING ARM R	ENV1244
	51	THREADING LINK L	ENV1245
	52	THREADING LINK R	ENV1246
	53	SLIDER L	ENV1247
	54	SLIDER R	ENV1248
	55	PINCH ROLLER	ENT1016
	56	BELT	ENT1017
	57	PULL GUIDE FLANGE	ELA2025
	58	TAPE GUIDE	ELA2022
	59	EARTH SPRING	EBL1004
	60	REEL WASHER	EBF1014
	61	SENSOR SHEET	EEF1001
	62	BRAKE FELT	ENM1019
	63	DAMPER	ENT1021
	64	TAPE GUIDE	ENV1282
	65	BRAKE SHOE	ENT1022
	66	CAPSTAN DD UNIT	EXH9002
	67	PINCH-ARM SPRING	EBH9005
	68	TR ARM SPRING	EBH1237
	69	PULL-GUIDE SPRING	EBH1222
	70	SPRING	EBH1223
	71	TR BRAKE SPRING	EBH1224
	72	IDLER GEAR SPRING	EBH1226
	73	REEL HUB SPRING	EBH1227
	74	BRAKE PLATE SPRING	EBH1228
	75	BRAKE LEVER SPRING	EBH1229
	76	REV BRAKE SPRING	EBH9006
	77	CHANGE ARM SPRING	EBH1231
	78	DRIVE ARM SPRING	EBH1232
	79	HARD BRAKE SPRING	EBH1233
	80	THREADING ARM SPRING (L)	EBH1238
	81	THREADING ARM SPRING (R)	EBH1239
	82	SCREW	BBZ20P060FZK
	83	SCREW	BMZ20P040FMC
	84	SCREW	PMS20P025FMC
	85	SCREW	JGZ20P030FMC
	86	WASHER	WT16D040D050
	87	WASHER	WT16D032D025
	88	WASHER	WT10D035D025
	89	WASHER	WA16D032D025
	90	WASHER	WA16D032D013
	91	WASHER	WA20D040D050
	92	WASHER	EBA1025
	93	WASHER	EBE1002
	94	RF UNIT	EWF9001
NSP	101	JUMPER WIRE 5P (J101)	EDD1004
NSP	102	CONNECTOR ASSY 5P (J6)	EDE1011
NSP	103	LEAD CARD 13P (J5)	EDD1006
NSP	104	REEL SENSOR BOARD	ENP1027
NSP	105	CHASSIS ASSY	EXA1183
NSP	106	MOTOR BRACKET ASSY	EXA1130
	107	DRIVE LEVER	ENR1014
NSP	108	SHIELD CASE	RNE1566

● DAT Mecha Assy



7. SCHEMATIC AND PCB CONNECTION DIAGRAMS

7.1 OVERALL SCHEMATIC DIAGRAM



SCH-1

NOTE FOR SCHEMATIC DIAGRAMS (Type 6A)

1. **When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".**
2. **Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.**
3. **RESISTORS:**
   Unit: k:kΩ, M:MΩ, or Ω unless otherwise noted.
   Rated power: 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
   Tolerance: (F): ±1%, (G): ±2%, (K): ±10%, (M): ±20% or ±5% unless otherwise noted.
4. **CAPACITORS:**
   Unit: p:pF or µF unless otherwise noted.
   Ratings: capacitor (µF)/ voltage (V) unless otherwise noted.
   Rated voltage: 50V except for electrolytic capacitors.
5. **COILS:**
   Unit: m:mH or µH unless otherwise noted.
6. **VOLTAGE AND CURRENT:**
   ▭ or ← V :
   DC voltage (V) in STOP mode unless otherwise noted.
   ⇦ mA or ← mA :
   DC current in STOP mode unless otherwise noted.
7. **OTHERS:**
   - ⊘ or ⊘ : Adjusting point.
   - ⊸ : Measurement point.
   - The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.
8. **SCH-□ ON THE SCHEMATIC DIAGRAM:**
   - *SCH-□ indicates the drawing number of the schematic diagram.* (SCH stands for schematic diagram.)
9. **SWITCHES** (Underline indicates switch position):

MAIN unit
S902:DIP SWITCH(SW1)

POWER SW unit
S1201:POWER

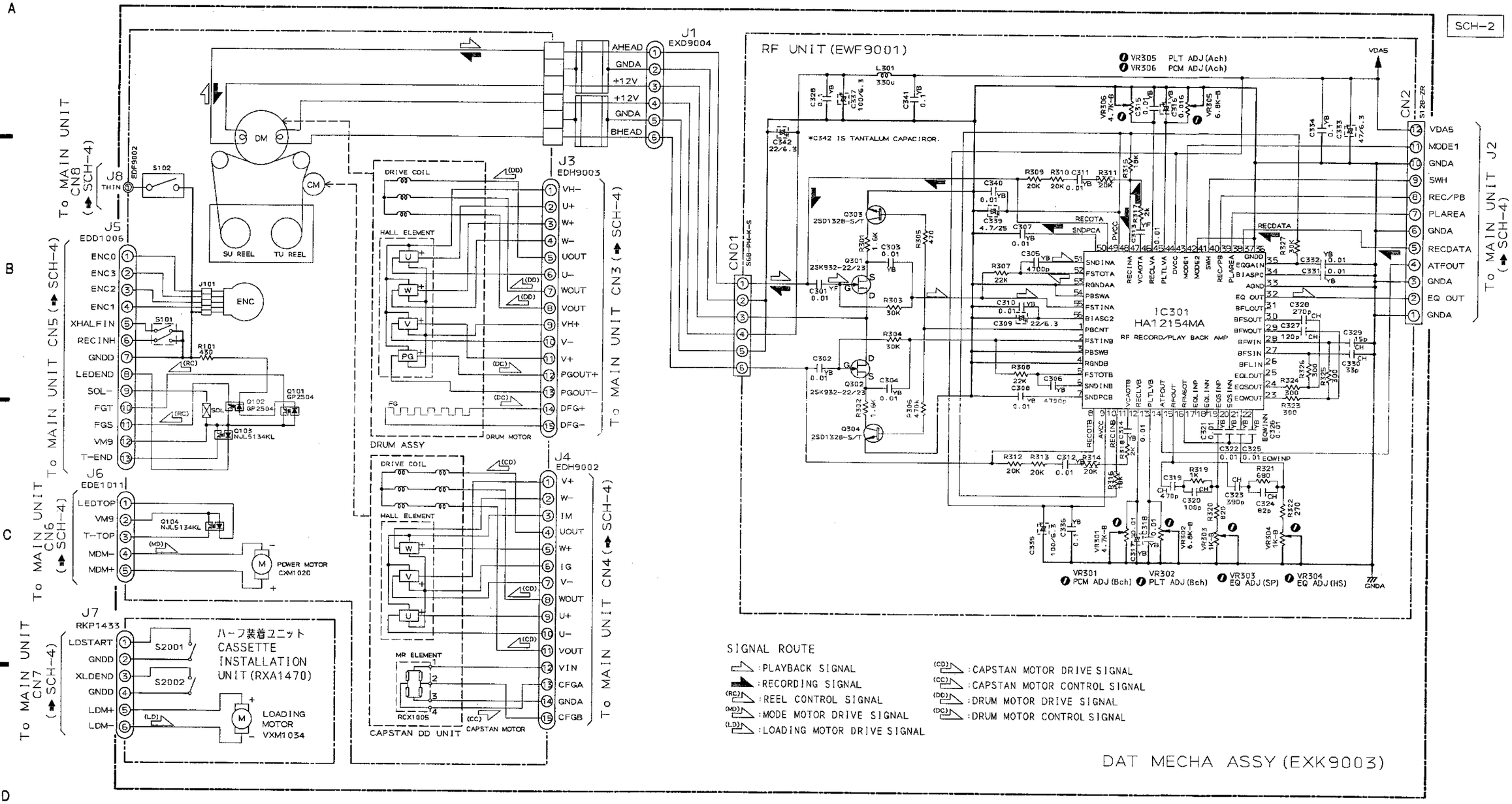
DISPLAY unit
S1601:⏻
S1602:ENTER
S1603:ID MODE
S1604:▶▶
S1605:▶
S1606:⏸
S1607:MS +
S1608:MS −
S1609:ERROR CHECK
S1610:LOCAL/REMOTE
S1611:◀◀
S1612:●
S1613:TOC RENUMBER
S1614:PEAK RESET
S1615:COUNTER RESET
S1616:COUNTER MODE
S1617:AUTO ID
S1618:■
S1619:⏏

SW unit
S1701:fs SELECT
44.1k-48k-88.2k-96k
S1702:INPUT SELECTOR
ANALOG-AES/EBU-COAXAL

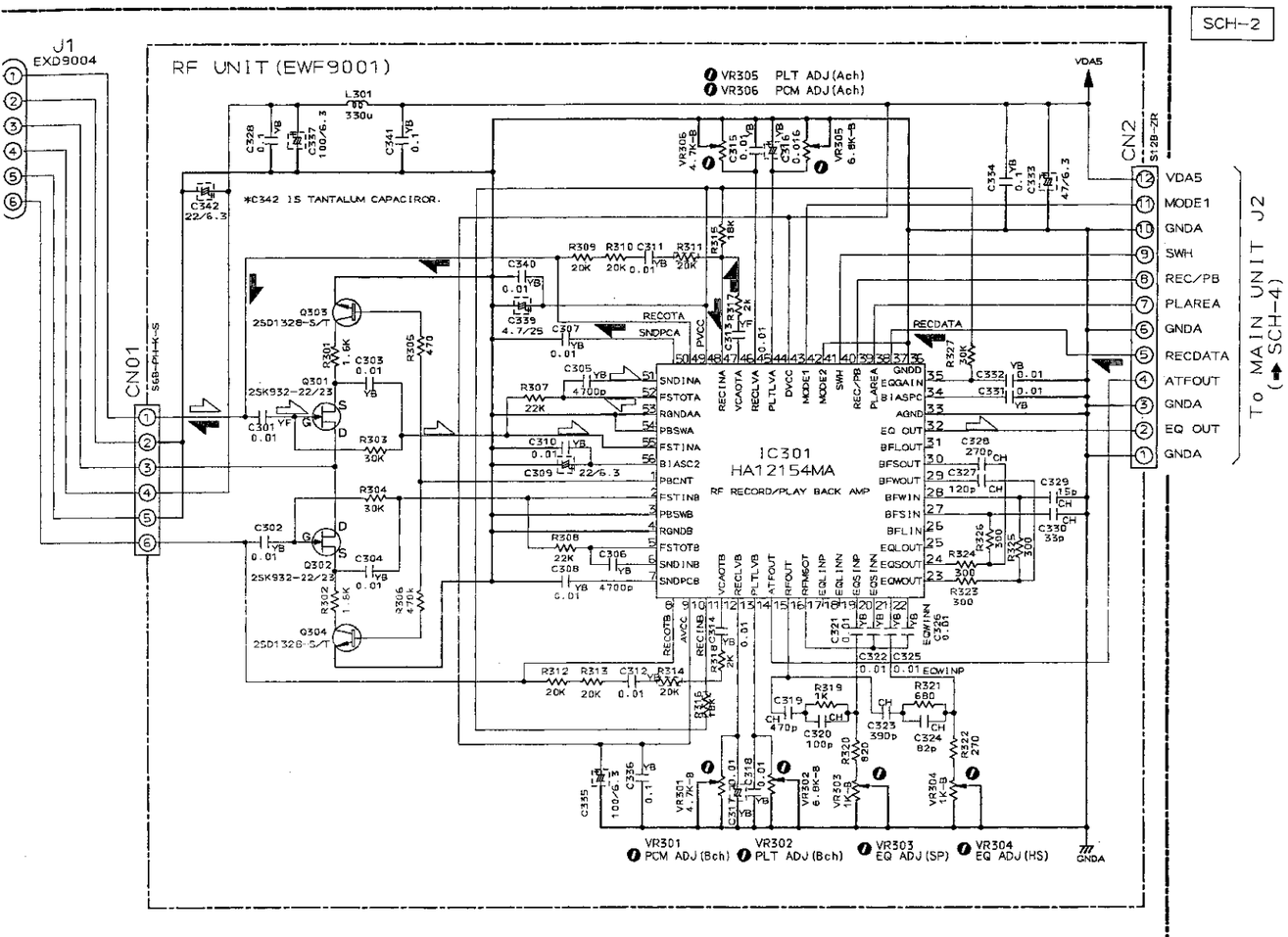
COPY ID unit
S1801:COPY ID
ONCE-PERMIT-INHIBIT

RS422 CONTROL unit
S3801:DIP SWITCH(S2)

7.2 DAT MECHA ASSY AND RF UNIT



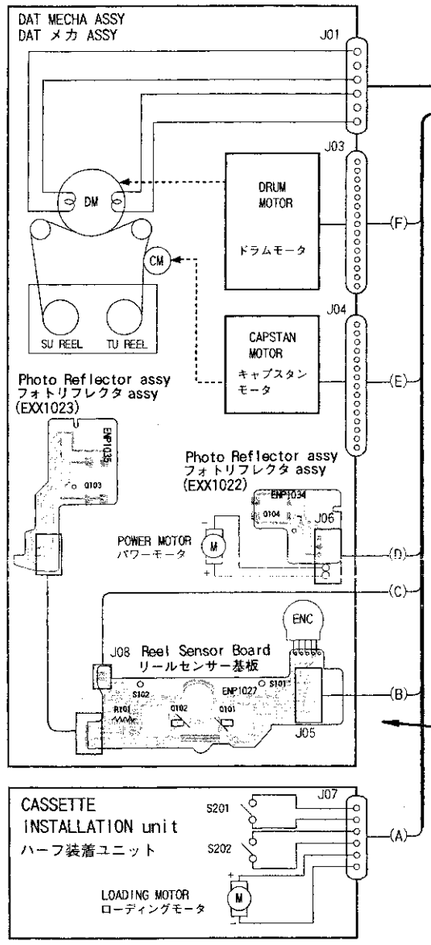
SCH-2



SIGNAL ROUTE

- : PLAYBACK SIGNAL
- : RECORDING SIGNAL
- (RC) : REEL CONTROL SIGNAL
- (MD) : MODE MOTOR DRIVE SIGNAL
- (LD) : LOADING MOTOR DRIVE SIGNAL
- (CD) : CAPSTAN MOTOR DRIVE SIGNAL
- (CC) : CAPSTAN MOTOR CONTROL SIGNAL
- (DD) : DRUM MOTOR DRIVE SIGNAL
- (DC) : DRUM MOTOR CONTROL SIGNAL

DAT MECHA ASSY (EXK9003)



NOTE FOR PCB DIAGRAMS:

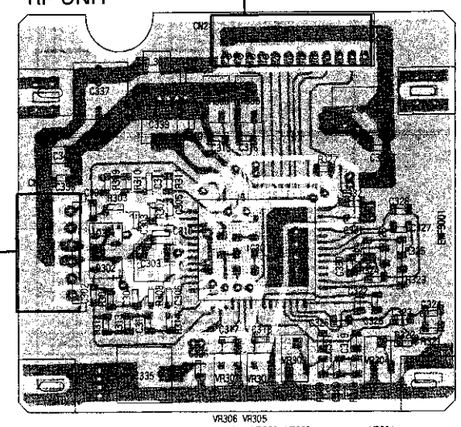
1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3- terminal regulator

(A) CN7
(B) CN5
(C) CN8
(D) CN6
(E) CN4
(F) CN3
— To MAIN unit

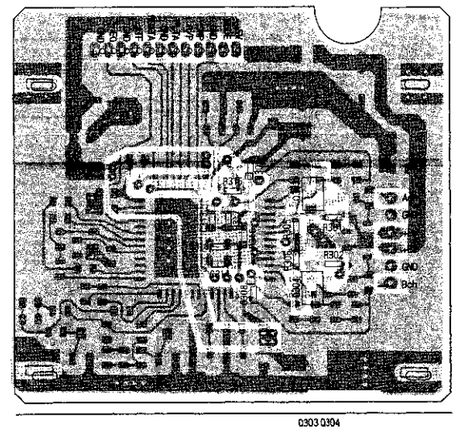
To MAIN unit J2

RF UNIT



- This diagram is viewed from the pink colored foil side.
- This is a multi-layer PCB.
  But information for both sides is shown.

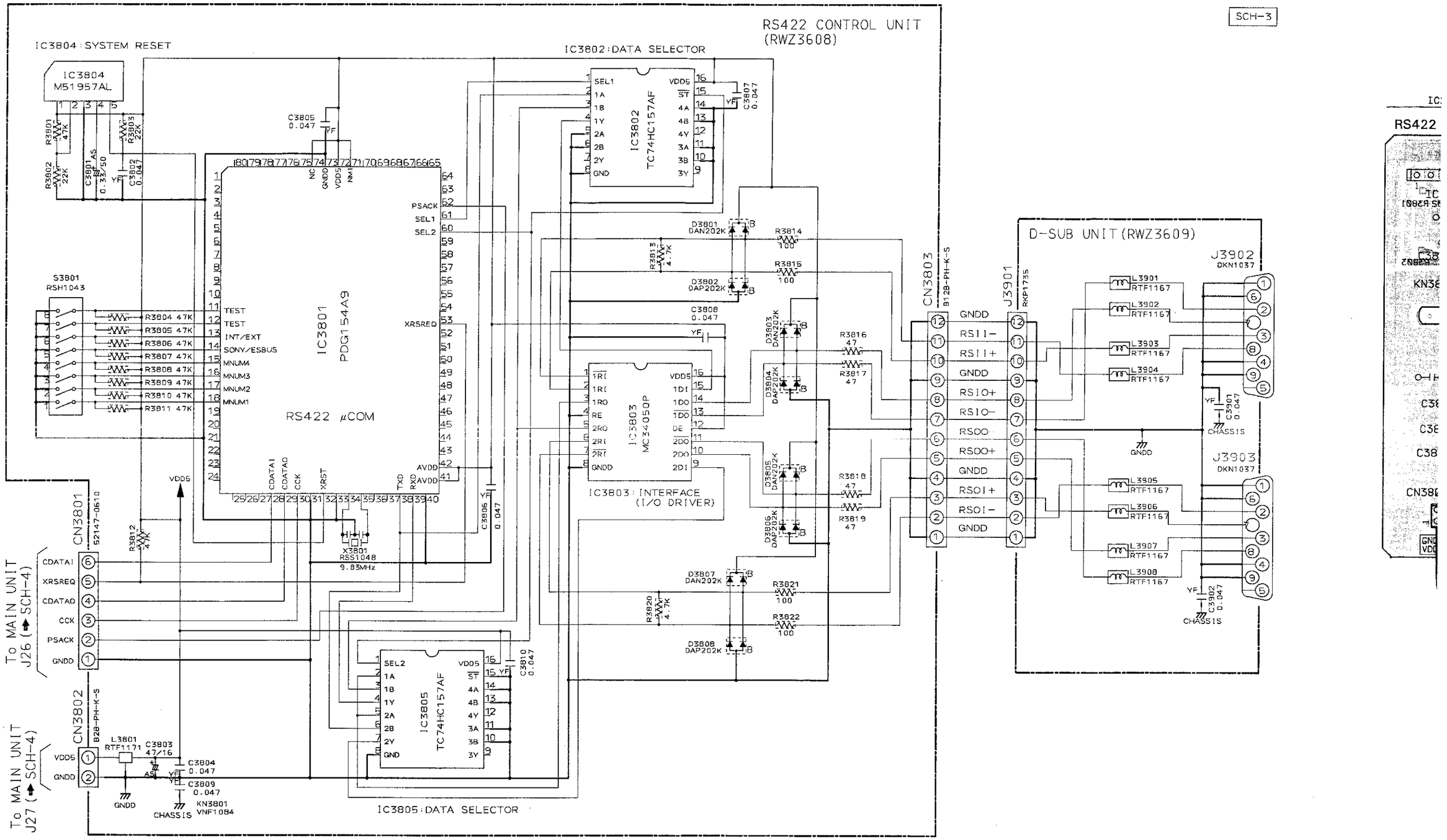
- This diagram is viewed from the mounted parts side.



- This diagram is viewed from the gray colored foil side.
- This is a multi-layer PCB.
  But information for both sides is shown.

DAT MECHA ASSY, RF UNIT — SCH-2

7.3 RS422 CONTROL UNIT AND D-SUB UNIT

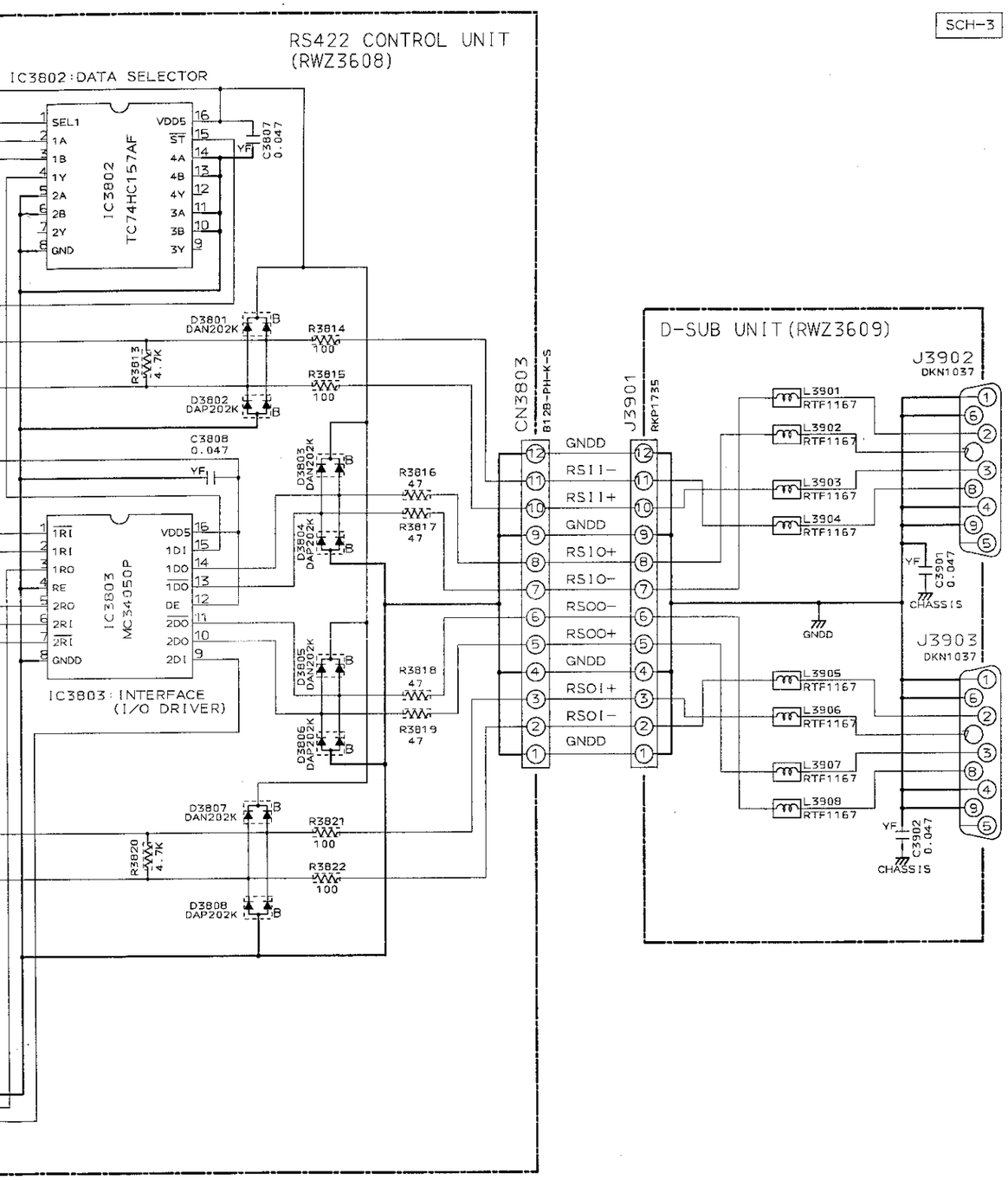


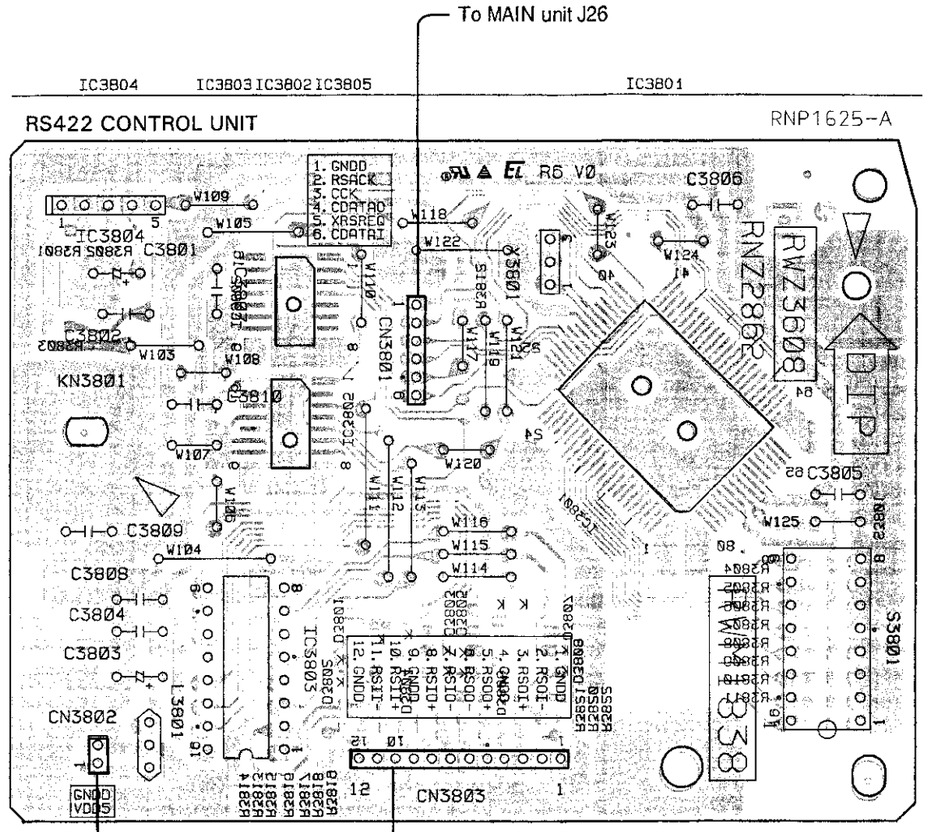
SCH−3 RS422 CONTROL UNIT, D-SUB UNIT

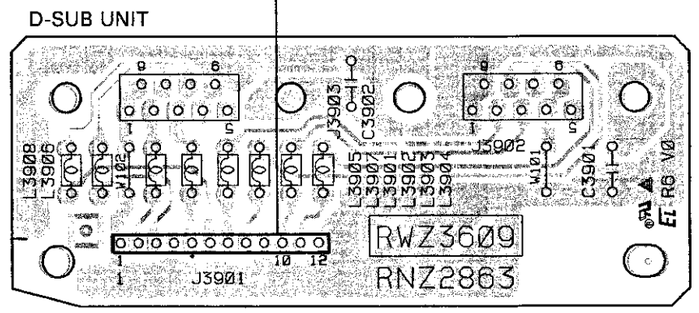
SCH-3

PCB-2

- This diagram is viewed from the mounted parts side.





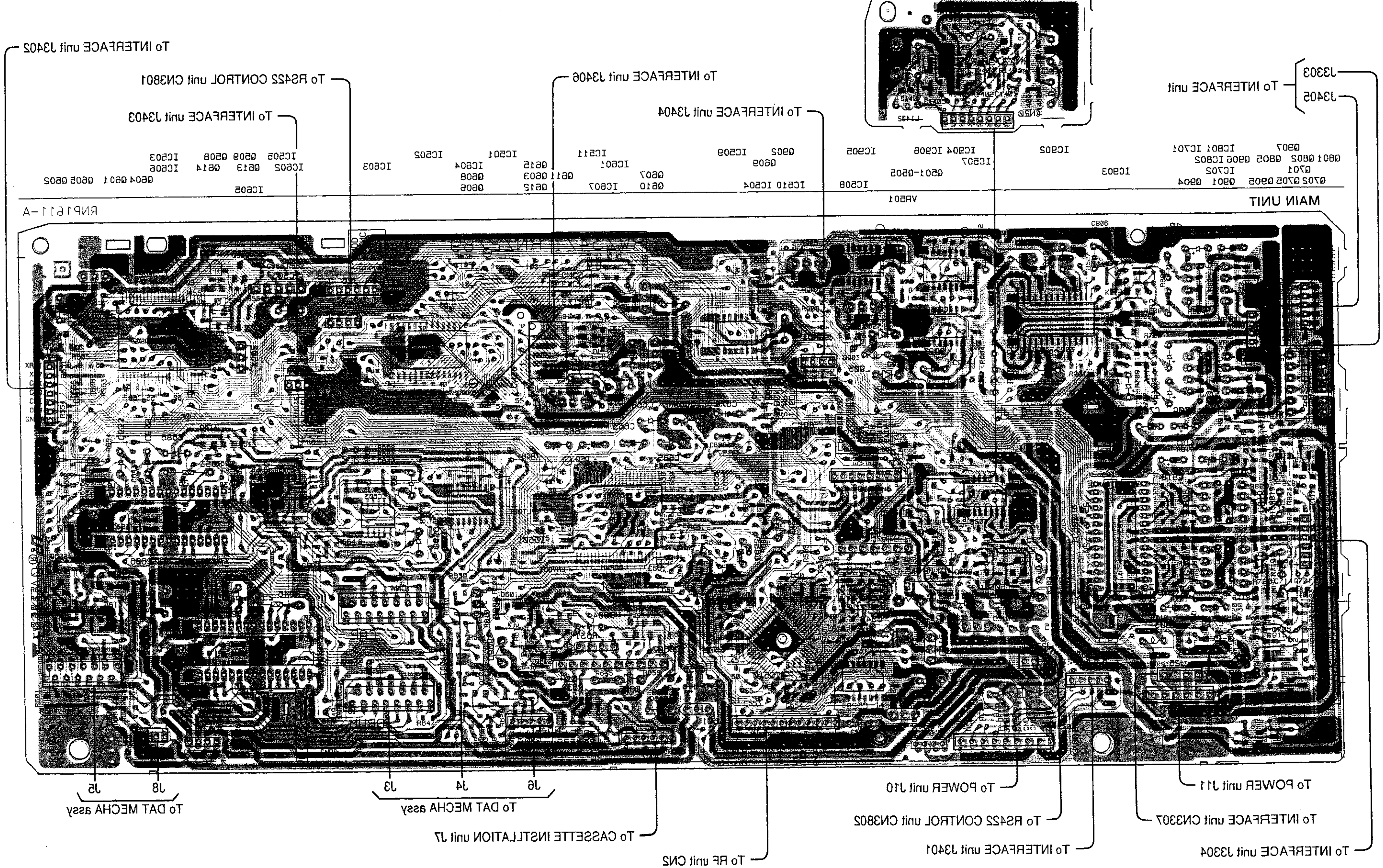


SCH-3

RS422 CONTROL UNIT, D-SUB UNIT

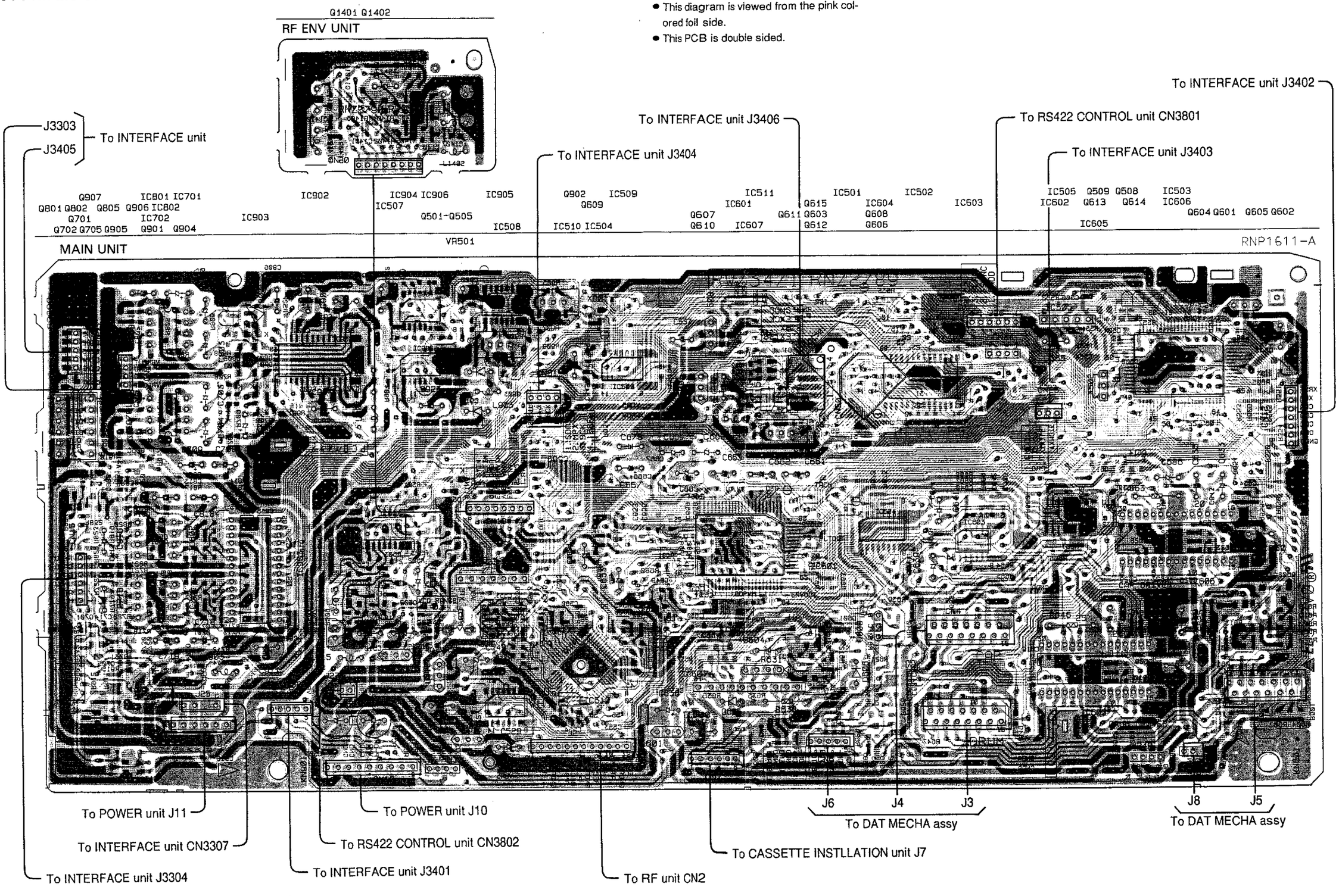
PCB-3

- This diagram is viewed from the gray colored foil side.
- This PCB is double sided.



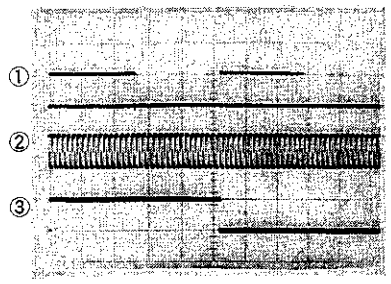
7.4 MAIN UNIT AND RF ENV UNIT

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.



Waveforms

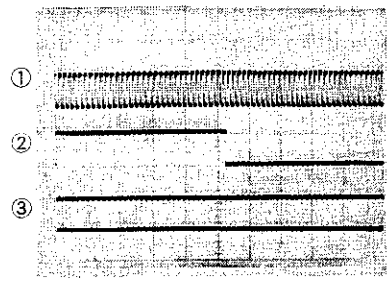
A1 : ADC



Mode: SP (REC)
Input: 1kHz, 0dB
5Vdiv., 2μS/div.

① SDATA
(IC902－Pin16)
② SCLK
(IC902－Pin15)
③ L/$\overline{R}$
(IC902－Pin14)

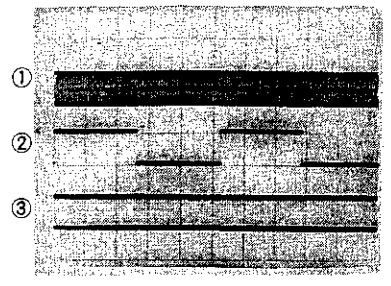
A2 : DAC



Mode: SP (REC)
Input: 1kHz, 0dB
5Vdiv., 2μS/div.

① BCK
(IC903－Pin26)
② LRCK
(IC903－Pin27)
③ DATA
(IC903－Pin25)

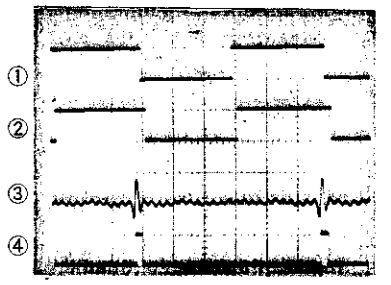
A4 : DAC



Mode: WSP (REC)
Input: 1kHz, 0dB
5Vdiv., 2μS/div.

① BCK
(IC903－Pin26)
② LRCK
(IC903－Pin27)
③ DATA
(IC903－Pin25)

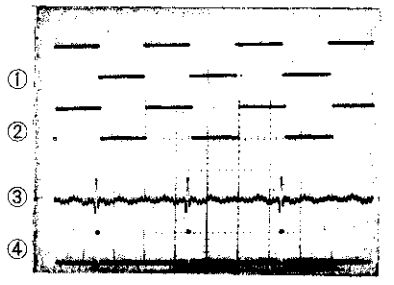
D1



Mode: SP (PLAY)
5Vdiv., 5mS/div.
(DPG: 0.5V/div.)

① SWH
(IC601－Pin70)
② SREF
(IC601－Pin71)
③ DPG
(IC603－Pin1)
④ TACH
(IC601－Pin7)

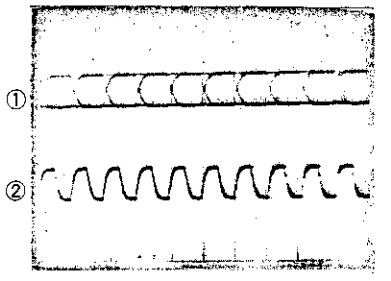
D3



Mode: WSP (PLAY)
5Vdiv., 5mS/div.
(DPG: 0.5V/div.)

① SWH
(IC601－Pin70)
② SREF
(IC601－Pin71)
③ DPG
(IC603－Pin1)
④ TACH
(IC601－Pin7)

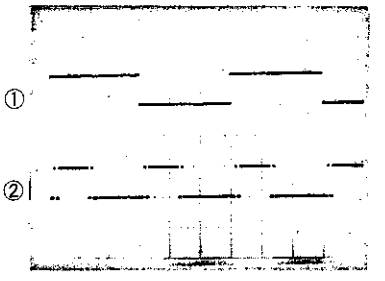
D4



Mode: SP (PLAY)
5Vdiv., 0.1μS/div.

① PDATA
(IC504－Pin52)
② PDCK
(IC504－Pin51)

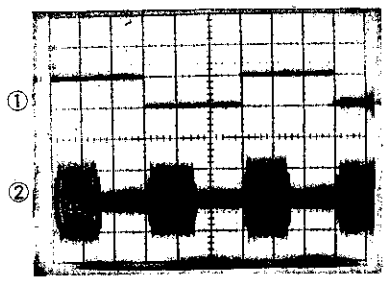
D5



Mode: SP (PLAY)
5Vdiv., 5mS/div.

① SWH
(IC601－Pin70)
② PARITY
(IC601－Pin67)

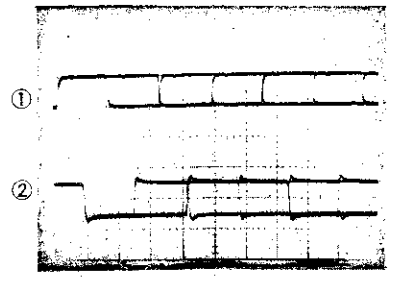
D6



Mode: SP (PLAY)

① HSWP
(CN23－Pin5)
5V/div., 5mS/div.
② EQ OUT
(J02－Pin11)
0.2V/div., 5mS/div.

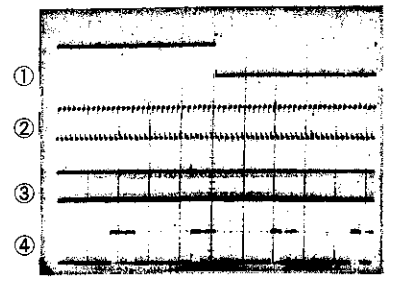
D8



Mode: D－IN (REC)

① TX
(IC501－Pin80)
5V/div., 0.1μS/div.
② COAX OUT
(JA504)
1V/div., 0.1μS/div.

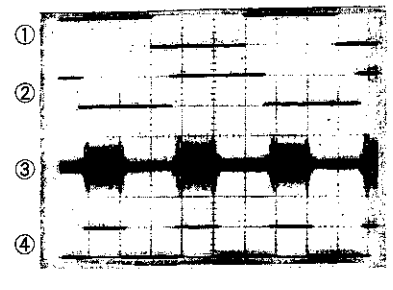
D9



Mode: SP (REC)
Input: No input
5Vdiv., 2μS/div.

① MPX
(IC501－Pin73)
② BCK
(IC501－Pin72)
③ FS256
(IC501－Pin70)
④ SOUT
(IC501－Pin71)

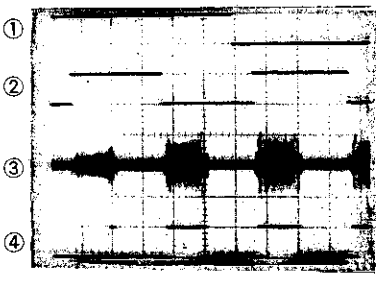
D10



Mode: SP (PLAY)
5Vdiv., 5mS/div.
(ENVIN: 0.5V/div.)

① FSYNC
(CN24－Pin2)
② HSWP
(CN23－Pin5)
③ ENV
(CN23－Pin3)
④ ENVOUT
(IC601－Pin64)

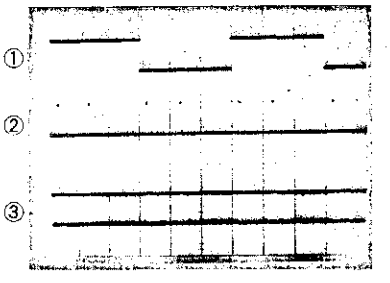
D11



Mode: LP (PLAY)
5Vdiv., 5mS/div.
(ENVIN: 0.5V/div.)

① FSYNC
(CN24－Pin2)
② HSWP
(CN23－Pin5)
③ ENV
(CN23－Pin3)
④ ENVOUT
(IC601－Pin64)

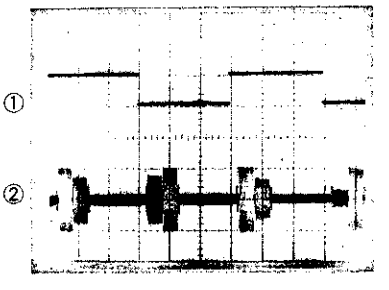
D12



Mode: SP (REC)
5Vdiv., 5mS/div.

① HSWP
(CN23－Pin5)
② PLAREA
(J02－Pin6)
③ RECDATA
(J02－Pin8)

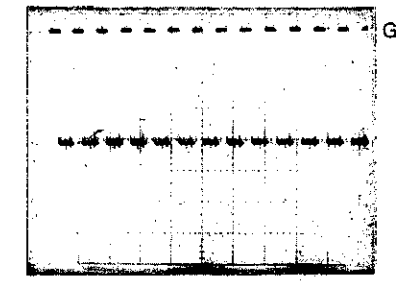
D13



Mode: SP (PLAY)
Test Tape: TY7111

① HSWP
(CN23－Pin5)
5Vdiv., 5mS/div.
② PLT2
(CN23－Pin4)
0.1Vdiv., 5mS/div.

D14



Mode: STOP
10V/div., 2mS/div.

SO (Segment)
(IC1601－Pin50)

SCH-4

MAIN UNIT, RF ENV UNIT

IC701 (2/2) : BUFFER AMP

IC902
A/D CONVERTER

IC902
AK5340A-VS
IC902:1bit ADC

CLOCK GENERATE CIRCUIT

DSP

IC501
HD49226AFS

RECORD/PLAYBACK SIGNAL
PROCESSING LSI

IC502
MS6225GCLL-10FC
RAM

IC504
HD49229
DATA STROBE

RF ENV UNIT
(RWZ3472)

To INTERFACE UNIT(2/2) J3303 (➡SCH-6)
To POWER UNIT J11 (➡SCH-6)
To INTERFACE UNIT(2/2) CN3307 (➡SCH-6)
To POWER UNIT J10 (➡SCH-6)
To INTERFACE UNIT(1/2) J3401 (➡SCH-5)
To INTERFACE UNIT(1/2) J3403 (➡SCH-5)
To INTERFACE UNIT(1/2) J3406 (➡SCH-5)
To INTERFACE UNIT(1/2) J3404 (➡SCH-5)
To RF UNIT CN2 (➡SCH-2)

NOTE)
S:STOP
P:PLAY
R:REC

SCH-4

MAIN UNIT (RWZ3471)

IC903 PD2029A(S)

IC903:1bit D/A CONVERTER

IC503 PDG152B9 SYSTEM CONTROLLER

IC505: SYSTEM RESET

IC601 HD49228FS SERVO CONTROL

IC607: MOTOR DRIVE

IC607 TA7288P

IC605: DRUM MOTOR DRIVE

IC606: CAPSTAN MOTOR DRIVE

Q606: T-TOP, END DETECT LED DRIVER

Q608: SOLENOID ON/OFF

MODE MOTOR & LOADING MOTOR DRIVE

Q601, Q602: REEL FG AMP

To INTERFACE UNIT (2/2) J3304 (→SCH-6)

To INTERFACE UNIT (1/2) J3405 (→SCH-5)

To CASSETTE INSTALATION UNIT J7 (→SCH-2)

To DAT MECHA ASSY J8 (→SCH-2)

To DAT MECHA ASSY J6 (→SCH-2)

To DAT MECHA ASSY J5 (→SCH-2)

To INTERFACE UNIT (1/2) J3402 (→SCH-5)

To RS422 CONTROL UNIT CN3801 (→SCH-3)

To RS422 CONTROL UNIT CN3802 (→SCH-3)

To DAT MECHA ASSY J3 (→SCH-2)

To DAT MECHA ASSY J4 (→SCH-2)

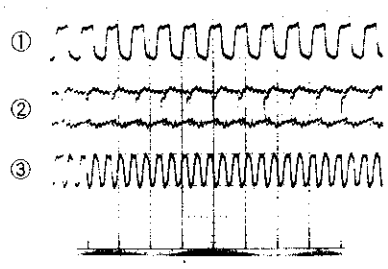
DAT MECHA ASSY J8 (→SCH-2)

SIGNAL ROUTE

- :PLAYBACK SIGNAL (ANALOG)
- :RECORDING SIGNAL (ANALOG)
- :PLAYBACK SIGNAL (DIGITAL)
- :RECORDING SIGNAL (DIGITAL)
- :CAPSTAN MOTOR DRIVE SIGNAL
- :CAPSTAN MOTOR CONTROL SIGNAL
- :DRUM MOTOR DRIVE SIGNAL
- :DRUM MOTOR CONTROL SIGNAL
- :REEL CONTROL SIGNAL
- :LOADING MOTOR DRIVE SIGNAL
- :MODE MOTOR DRIVE SIGNAL

7.5 AES/EBU UNIT, DIGITAL I/O UNIT, LED UNIT, SW UNIT, COPY ID UNIT, DISPLAY UNIT AND INTERFACE UNIT (1/2)

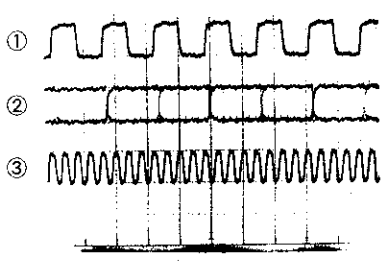
1



Mode: DIGITAL REC
[Input fs: 96kHz (HS)]
5Vdiv., 0.1μS/div.

① EX128 (J3406 – Pin1)
② RX (J3406 – Pin2)
③ EXCK (J3406 – Pin3)

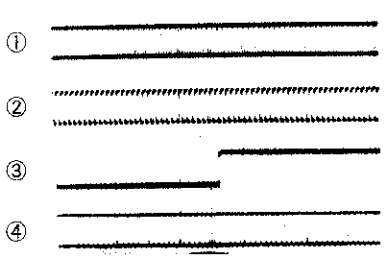
2



Mode: DIGITAL REC
[Input fs: 48kHz (SP)]
5Vdiv., 0.1μS/div.

① EX128 (J3406 – Pin1)
② RX (J3406 – Pin2)
③ EXCK (J3406 – Pin3)

3



Mode: HS (WSP) 96kHz PLAY
5Vdiv., 1μS/div.

① 128 fs (IC3406 – Pin5)
② BCK (IC3406 – Pin6)
③ MPX (IC3406 – Pin7)
④ SDATA (IC3406 – Pin8)

SIGNAL ROUTE
(D) : PLAYBACK SIGNAL (DIGITAL)
(D) : RECORDING SIGNAL (DIGITAL)

INTERFACE UNIT (1/2) (RWZ3475)

AES/EBU UNIT (RWZ3476)

DIGITAL I/O UNIT (RWZ3477)

IC3402 PDC019A(S) CDR ENCODER DECODER (DIGITAL IN PLL)

DIGITAL IN PLL CIRCUIT

X3403 : VOLTAGE CONTROL OSCILLATOR

IC3403 (1/6 to 3/6) TC74HC04AF

IC3403 (4/6 to 6/6) TC74HC00F

IC3404 TC9246F VCO

IC3405 : AES/EBU I/O DRIVER

IC3406 : DIGITAL INTERFACE

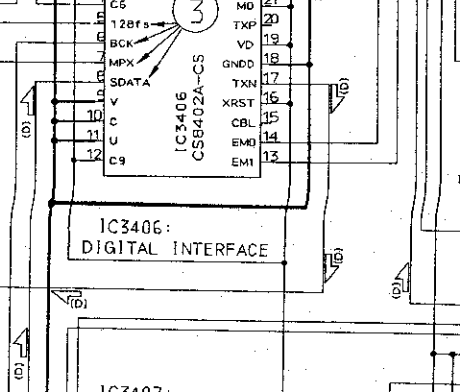
IC3407 : AES/EBU OUT SIGNAL

IC3419 : INPUT SELECTOR (COAX/AES)

IC3701 (1/6 to 3/6) COAXIAL INPUT CIRCUIT

IC3701 (4/6 to 6/6) DIGITAL OUTPUT CIRCUIT

● V1601 (RAW1117): FL TUBE

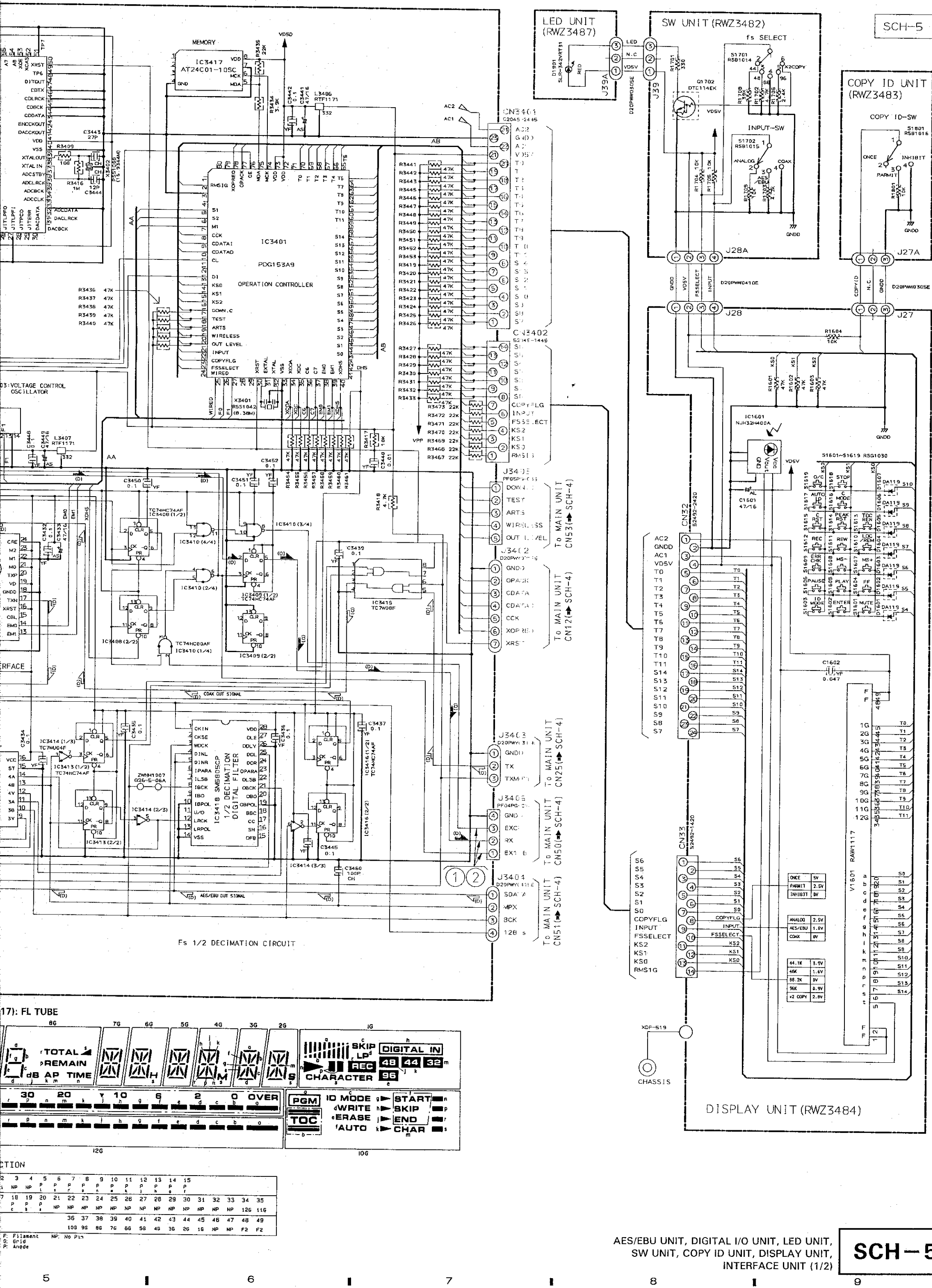


TERMINAL CONNECTION

TERMINAL NO.	1	2	3	4	5	6	7	8	9
ELECTRODE	F1	F1	NP	NP	P l	P g	P c	P b	P h
TERMINAL NO.	16	17	18	19	20	21	22	23	24
ELECTRODE	P e	P d	P c	P b	P a	NP	NP	NP	NP
TERMINAL NO.							35	37	38
ELECTRODE							10G	9G	8G

Notes F: Filament NP: No Pin
G: Grid
P: Anode

SCH – 5 AES/EBU UNIT, DIGITAL I/O UNIT, LED UNIT, SW UNIT, COPY ID UNIT, DISPLAY UNIT, INTERFACE UNIT (1/2)



CTION

2	3	4	5	6	7	8	9	10	11	12	13	14	15					
	NP	NP	P l	P k	P r	P p	P n	P m	P k	P j	P h	P e	P f					
7	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	P c	P b	P a	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	12G	11G
					36	37	38	39	40	41	42	43	44	45	46	47	48	49
					10G	9G	8G	7G	6G	5G	4G	3G	2G	1G	NP	NP	F2	F2

F: Filament NP: No Pin
G: Grid
P: Anode

AES/EBU UNIT, DIGITAL I/O UNIT, LED UNIT, SW UNIT, COPY ID UNIT, DISPLAY UNIT, INTERFACE UNIT (1/2)

SCH-5

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.

To BALANCE IN unit J3505

To VR unit CN45 and CN44

CN14
J25
To MAIN unit

To BALANCE OUT unit CN3506

INTERFACE UNIT

DIGITAL I/O U

Q3701–Q3708

CN53
CN12
To MAIN unit

IC3201 Q3108 Q3107 Q3109 Q3110 Q3208 Q3216 Q3207 Q3210 Q3209
Q3112 Q3111 Q3101 Q3114 Q3113 Q3102 Q3201 Q3212 Q3211
IC3101 IC3102 IC3103 IC3203 IC3202 Q3214 Q3213 Q3202

To MAIN unit CN15

To HEADPHONE unit J12

IC3405 IC3419 IC3403 IC3408 IC3409
IC3410 IC3404
IC3402 IC3406 IC3413 IC3414 IC3417 IC3401
Q3401 IC3415 IC3407 IC3418 IC3416

CN52 CN51 CN50 CN25
To MAIN unit

- This diagram is viewed from the mounted parts side.

LED UNIT

RWZ3487 D1901 J30A
RNZ2806
CMK-P3X

SW UNIT

Q1701 Q1702

RNP1612-A

DISPLAY UNIT

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.

CE OUT unit CN3506

DIGITAL I/O UNIT

Q3701–Q3708 IC3701

AES/EBU UNIT

CN53
CN12
To MAIN unit

Q3207 Q3210 Q3209
2Q3211
202 Q3214 Q3213 Q3202

IC3405 IC3419 IC3403 IC3408 IC3409 IC3410 IC3404 IC3406 IC3413 IC3414 IC3417 IC3401 IC3407 IC3418 IC3416 IC3402 Q3401 IC3415

CN52 CN51 CN50 CN25
To MAIN unit

ADPHONE unit J12

- This diagram is viewed from the mounted parts side.

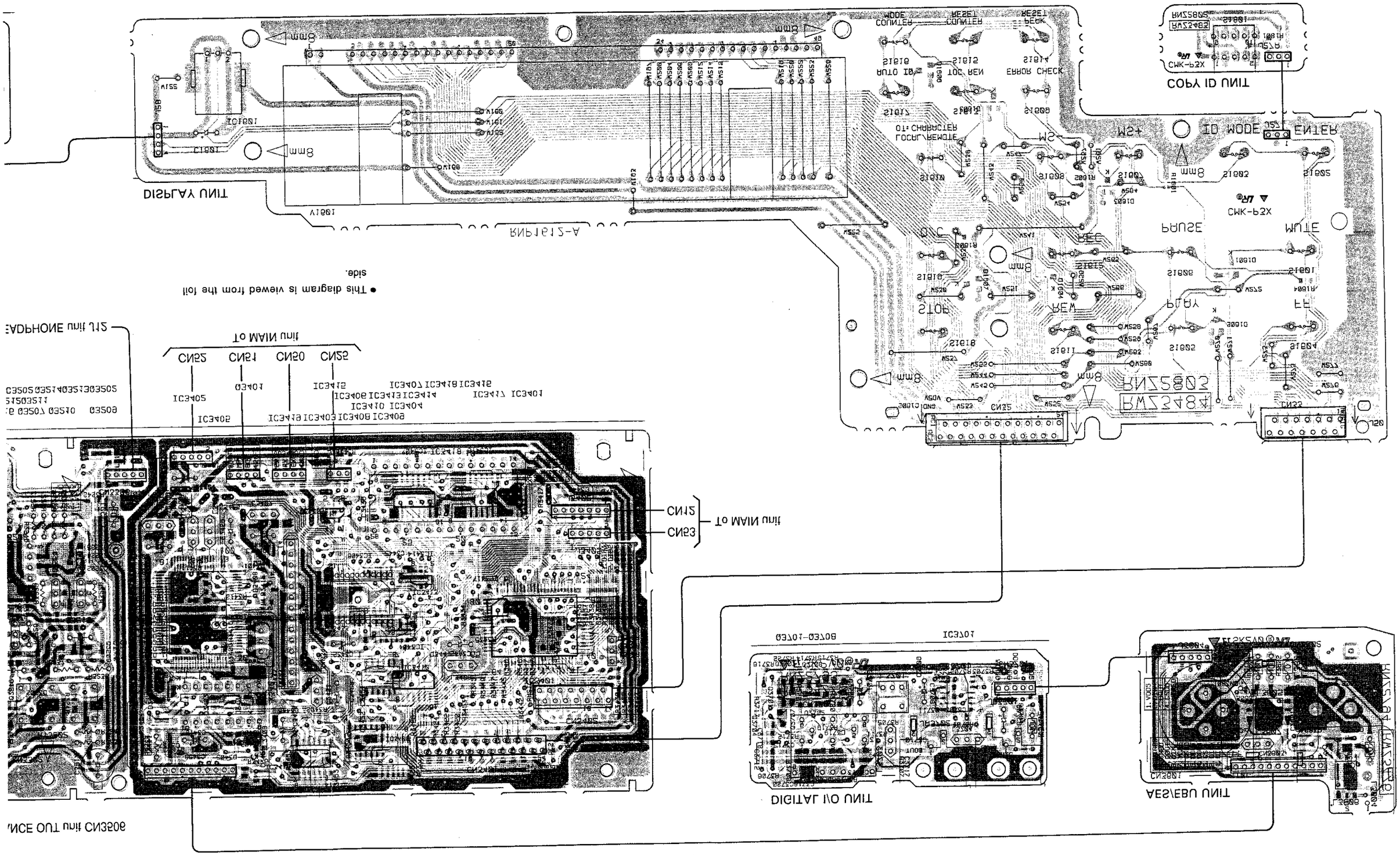
RNP1612-A

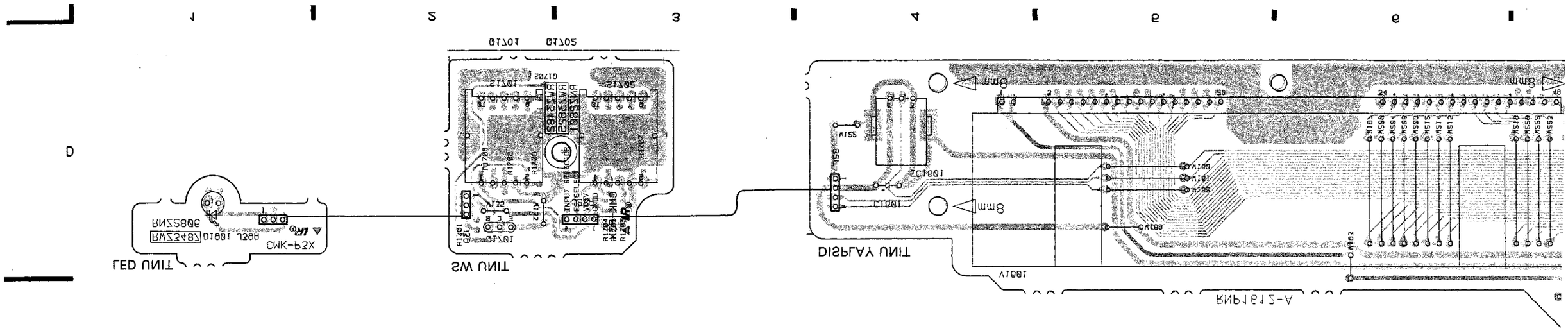
DISPLAY UNIT

RWZ3484
RNZ2803

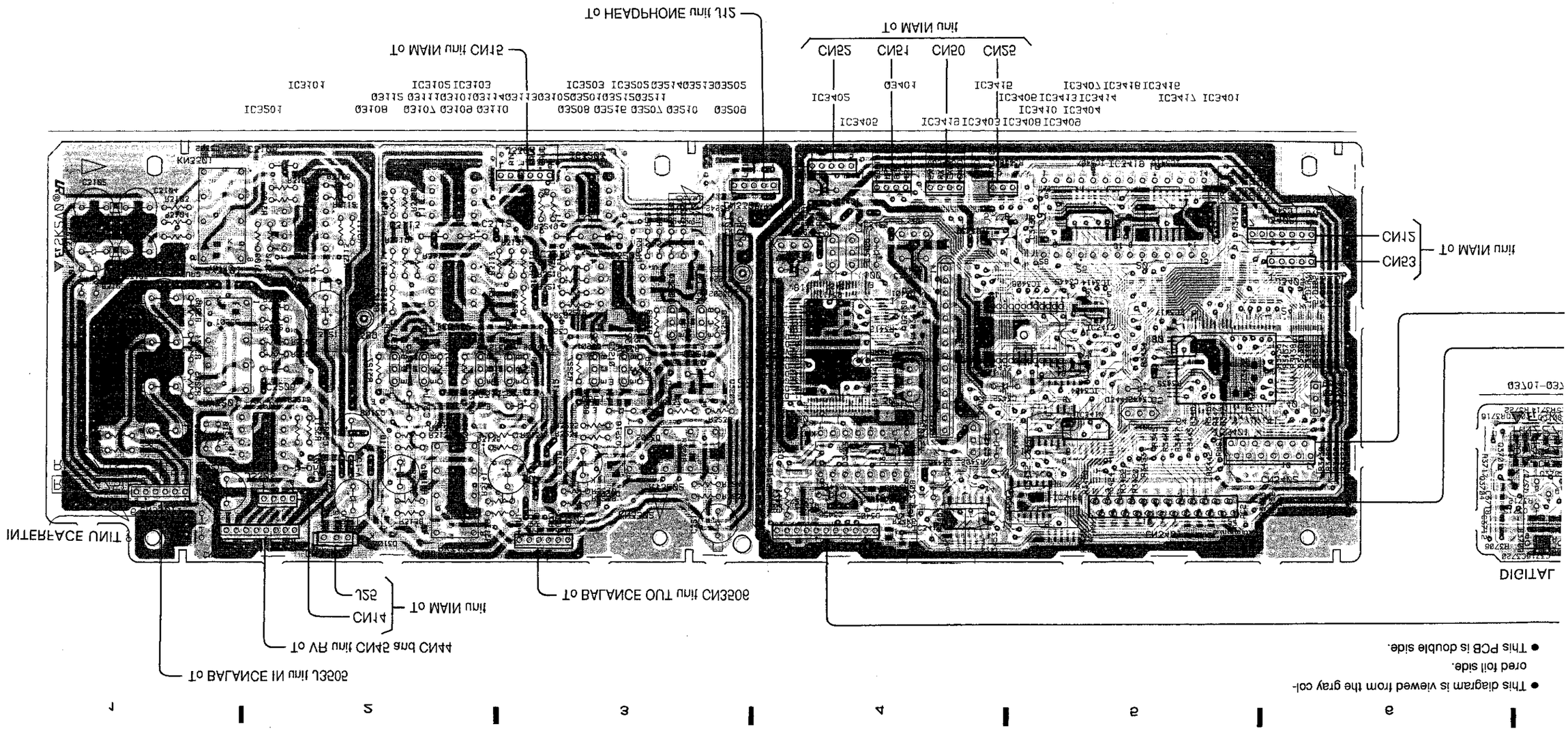
STOP REW PLAY FF
REC PAUSE MUTE
CMK-P3X
LOCAL/REMOTE
CHARACTER
AUTO IS
TOC REN
ERROR CHECK
COUNTER MODE
COUNTER RESET
PEAK RESET
MS- MS+ ID MODE ENTER

COPY ID UNIT

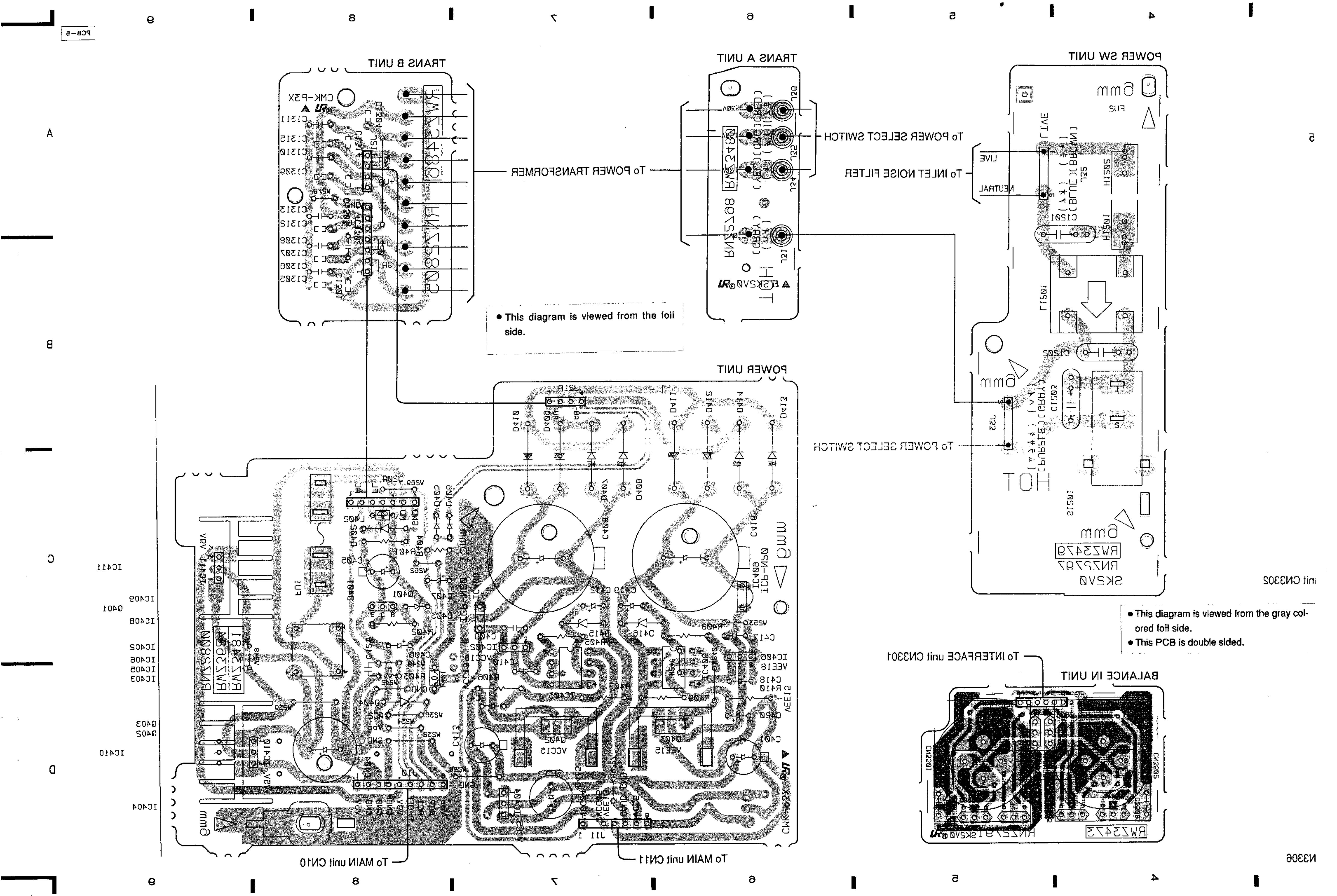

DISPLAY UNIT
COPY ID UNIT
ID MODE
ENTER
PAUSE
WAIT
REC
PLAY
STOP
DIGITAL I/O UNIT
AES/EBU UNIT
TO MAIN UNIT
CN15
CN23
CN25
CN27
CN20
CN22
TO MAIN UNIT
HEADPHONE UNIT
SERVICE OUT UNIT CN3208
• This diagram is viewed from the foil side.
• This diagram is viewed from the gray colored foil side.
• This PCB is double side.
PCB-A
D-3601

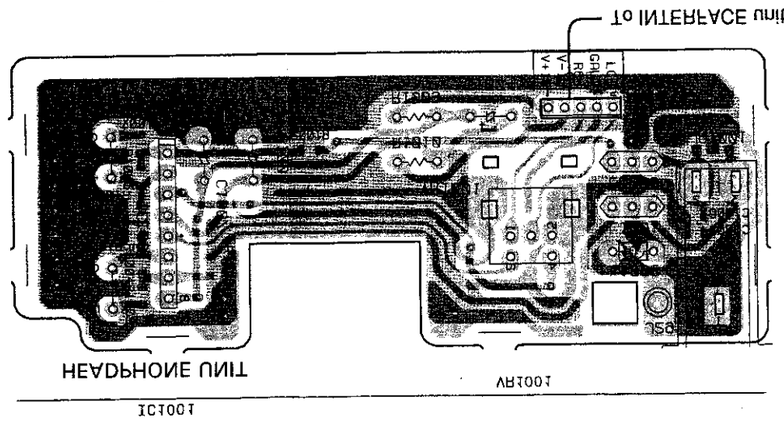


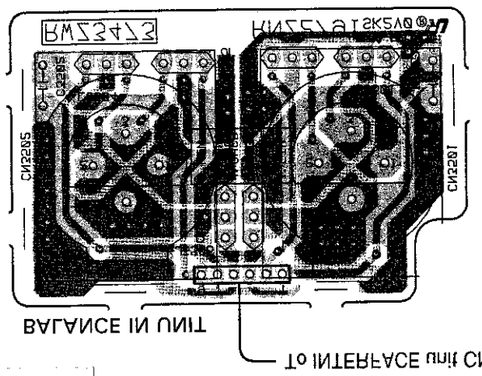
● This diagram is viewed from the foil side.



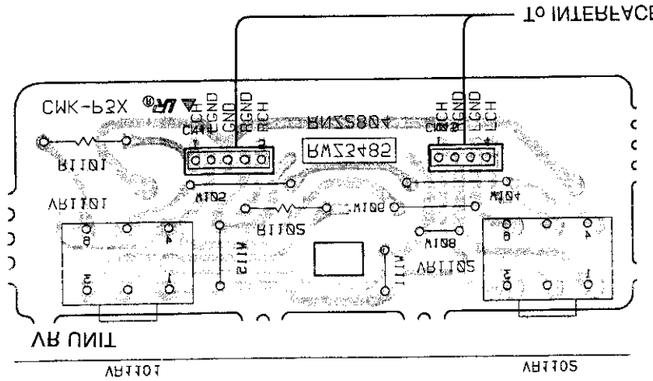
● This diagram is viewed from the gray colored foil side.
● This PCB is double side.

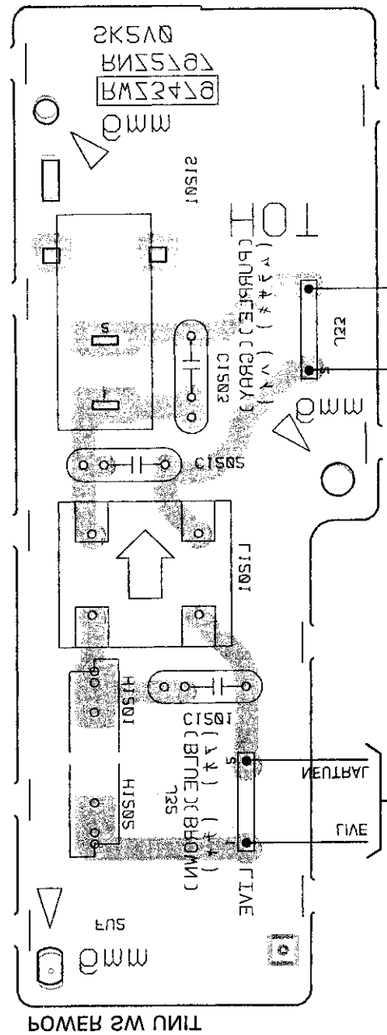

PCB-5
TRANS B UNIT
TRANS A UNIT
POWER SW UNIT
To POWER TRANSFORMER
To POWER SELECT SWITCH
To INLET NOISE FILTER
LIVE
NEUTRAL
This diagram is viewed from the foil side.
POWER UNIT
To POWER SELECT SWITCH
This diagram is viewed from the gray colored foil side.
This PCB is double sided.
To INTERFACE unit CN3301
BALANCE IN UNIT
To MAIN unit CN10
To MAIN unit CN11

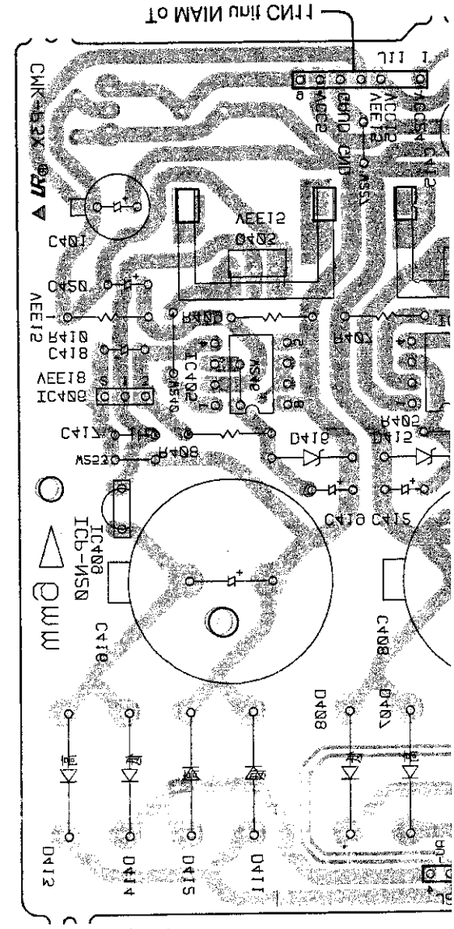


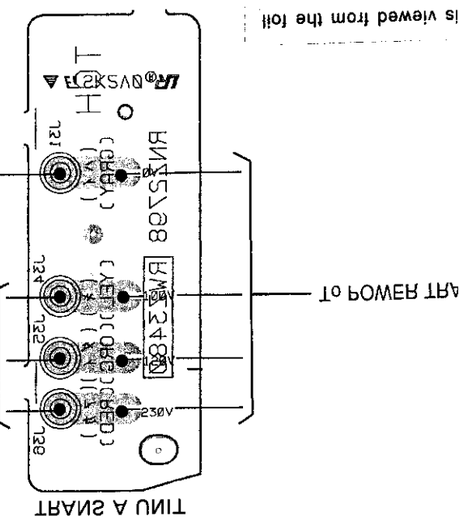


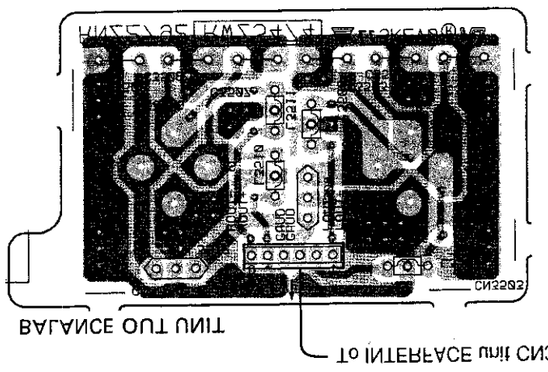
- This diagram is viewed from the gray color foil side.
- This PCB is double sided.



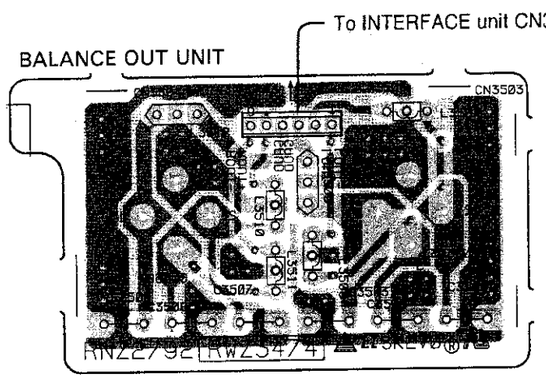


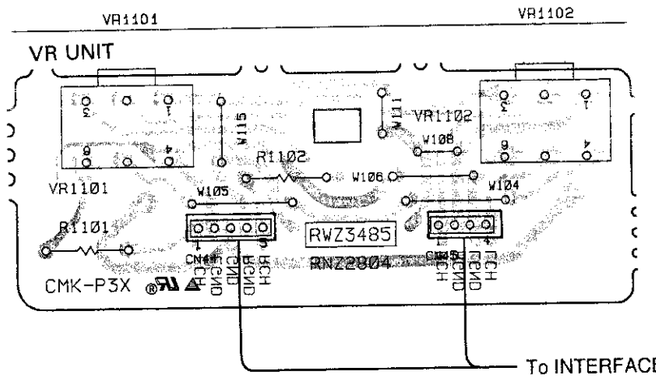


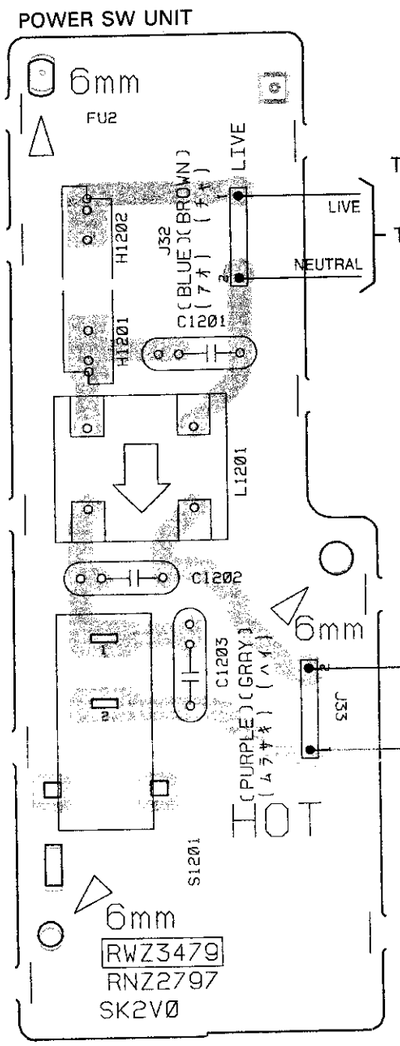


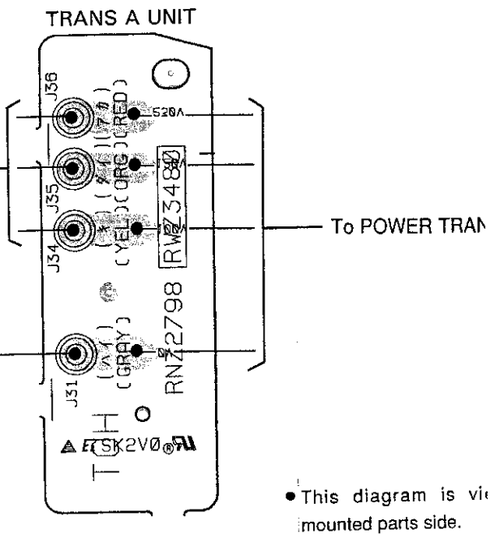


7.6 BALANCE IN UNIT, BALANCE OUT UNIT, VR UNIT, HEADPHONE UNIT, POWER UNIT, TRANS A UNIT, TRANS B UNIT, POWER SW UNIT AND INTERFACE UNIT (2/2)

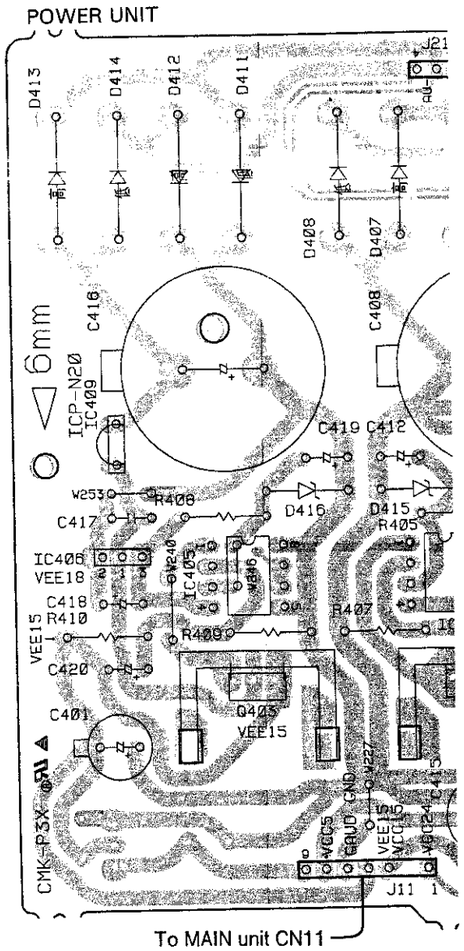




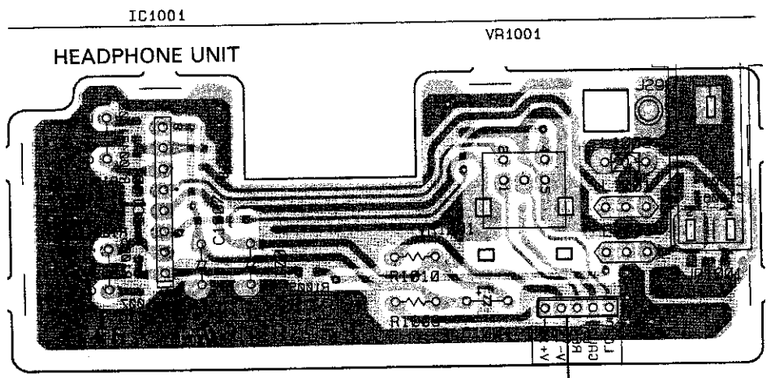


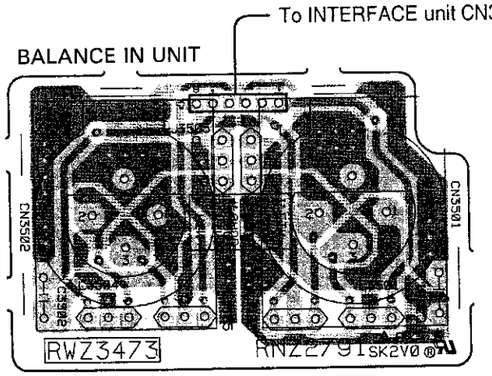


- This diagram is vie
mounted parts side.



- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.





POWER SW UNIT

TRANS A UNIT

TRANS B UNIT

To POWER SELECT SWITCH

To INLET NOISE FILTER

To POWER TRANSFORMER

To POWER SELECT SWITCH

- This diagram is viewed from the mounted parts side.

POWER UNIT

: CN3302

- This diagram is viewed from the pink colored foil side.
- This PCB is double sided.

To INTERFACE unit CN3301

BALANCE IN UNIT

J3306

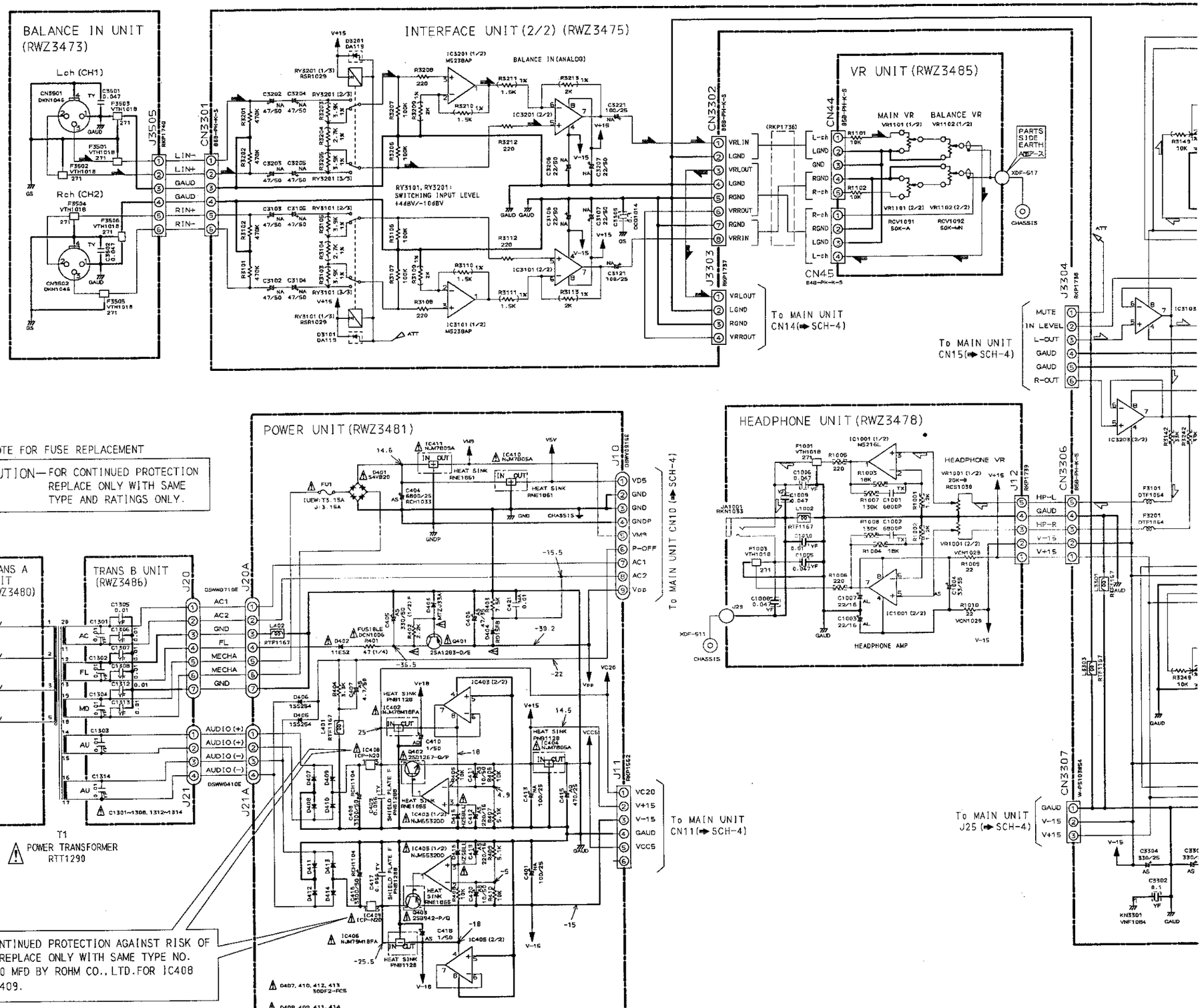
To MAIN unit CN11

To MAIN unit CN10

SIGNAL ROUTE

: PLAYBACK SIGNAL (ANALOG)

: RECORDING SIGNAL (ANALOG)



● NOTE FOR FUSE REPLACEMENT

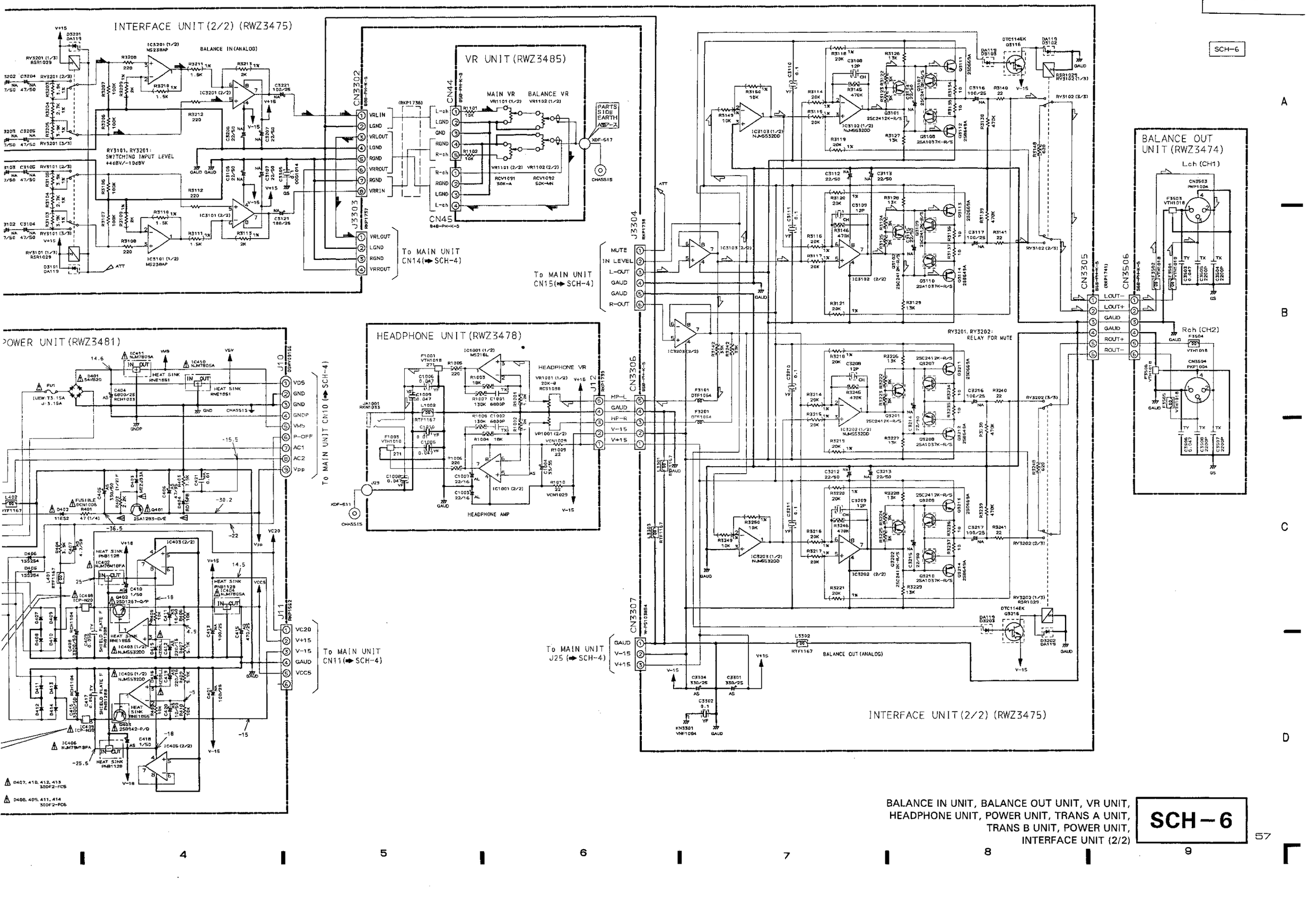
CAUTION—FOR CONTINUED PROTECTION REPLACE ONLY WITH SAME TYPE AND RATINGS ONLY.

CAUTION: FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. ICP-N20 MFD BY ROHM CO., LTD. FOR IC408 AND IC409.

SCH—6

BALANCE IN UNIT, BALANCE OUT UNIT, VR UNIT, HEADPHONE UNIT, POWER UNIT, TRANS A UNIT, TRANS B UNIT, POWER UNIT, INTERFACE UNIT (2/2)

SCH-6



BALANCE IN UNIT, BALANCE OUT UNIT, VR UNIT,
HEADPHONE UNIT, POWER UNIT, TRANS A UNIT,
TRANS B UNIT, POWER UNIT,
INTERFACE UNIT (2/2)

SCH−6

8. PCB PARTS LIST

NOTES :

- *Parts marked by " NSP " are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by " ◉ " are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560 Ω → 56 x 10¹ = 561 ..... RD1/8PM 5 6 1 J
47k Ω → 47 x 10³ = 473 ..... RD1/4PS 4 7 3 J
0.5 Ω → 0R5 ..... RN2H 0 R 5 K
1 Ω → 010 ..... RS1P 0 1 0 K

Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62k Ω → 562 x 10¹ = 5621 ..... RM1/4PC 5 6 2 1 F

Mark	No.	Description	Parts No.
LIST OF ASSEMBLIES			
NSP	MOTHER UNIT		RWM1797
	├ MAIN UNIT		RWZ3471
	├ RF ENV UNIT		RWZ3472
	├ BALANCE IN UNIT		RWZ3473
	├ BALANCE OUT UNIT		RWZ3474
	├ INTERFACE UNIT		RWZ3475
	├ AES/EBU UNIT		RWZ3476
	├ DIGITAL I/O UNIT		RWZ3477
	├ HEADPHONE UNIT		RWZ3478
	├ POWER SW UNIT		RWZ3479
	└ TRANS A UNIT		RWZ3480
NSP	SUB UNIT		RWM1803
	├ POWER UNIT		RWZ3481
NSP	├ SW UNIT		RWZ3482
NSP	├ COPY ID UNIT		RWZ3483
	├ DISPLAY UNIT		RWZ3484
NSP	├ VR UNIT		RWZ3485
	├ TRANS B UNIT		RWZ3486
NSP	└ LED UNIT		RWZ3487
NSP	RS422 UNIT		RWM1838
	├ RS422 CONTROL UNIT		RWZ3608
NSP	└ D-SUB UNIT		RWZ3609
	DAT MECHA ASSY		EXK9003
	└ RF UNIT		EWF9001
MAIN UNIT			
SEMICONDUCTORS			
	IC902		AK5340A-VS
	IC501		HD49226AFS
	IC601		HD49228FS
	IC504		HD49229
	IC605, IC606		LB1687
	IC505		M51957AL
	IC502		MS62256CLL-10FC
	IC603		NJM2902M
	IC602		NJM2904M
	IC701, IC801		NJM4565D-D
	IC702, IC802		NJM5532DD
	IC903		PD2029A (S)
	IC503		PDG152B9
	IC607		TA7288P
	IC604		TC4053BF
	IC508		TC74HC08AF
	IC904		TC74HC10AF
	IC906		TC74HC74AF
	IC507, IC509, IC905		TC74HCU04AF
	IC510		TC7W00F
	IC511		TC7WU04F
	Q607		2SA1037K
	Q603-Q606, Q609, Q612		2SC2412K
	Q608		2SC3246
	Q701, Q702, Q705, Q801, Q802		2SC3326
	Q805, Q907		2SC3326
	Q508, Q509, Q601, Q602, Q904		DTA114EK
	Q906		DTA114EK
	Q610, Q611, Q613-Q615		DTC114EK
	Q901-Q903, Q905		DTC114EK
	D605, D606, D901, D902		1SR35-100AVL
	D601, D603		DA119
	D701, D801		DAN202K
	D503-D505, D702, D802		DAP202K
	D604		MTZJ2.0AX
COILS AND FILTERS			
	F517-F519		DTF1064
	F516		DTF1068
	L901-L903, L905		LFA010J
	L510		LFA3R3J
	L505, L507-L509, L512, L514		RTF1171
	L601		RTF1171
SWITCHES AND RELAYS			
	S902		RSH1044
CAPACITORS			
	C560		CCSQCH030C50
	C712, C713, C812, C813, C925		CCSQCH050C50
	C557		CCSQCH060D50
	C556		CCSQCH080D50
	C543, C550, C926		CCSQCH100D50
	C541		CCSQCH101J50
	C702, C802		CCSQCH121J50
	C927		CCSQCH150J50
	C928		CCSQCH200J50
	C542		CCSQCH220J50

Mark	No.	Description	Parts No.
	C634		CCSQCH221J50
	C711, C811		CCSQCH390J50
	C569, C604, C605		CCSQCH470J50
	C715, C815		CCSQSL561J50
	C654		CEANP010M50
	C639		CEANP3R3M50
	C653		CEANP4R7M50
	C661-C663, C665, C668		CEAS010M50
	C641		CEAS100M50
	C502, C503		CEAS331M16
	C524, C529, C533, C537, C539		CEAS470M16
	C549, C561, C608, C617, C621		CEAS470M16
	C625, C630, C633, C635, C636		CEAS470M16
	C669		CEAS470M16
	C657		CEAS4R7M50
	C565		CEASR33M50
	C686		CEASR47M50
	C707, C807, C904, C908		CENA100M50
	C911		CENA101M25
	C703, C704, C708, C709, C716		CENA220M50
	C718, C719, C803, C804		CENA220M50
	C808, C809, C816, C818, C819		CENA220M50
	C906		CENA4R7M50
	C544, C919, C921, C923		CEYA470M25
	C678		CFTXA332J50
	C640, C660, C667		CKSQYB102K50
	C652		CKSQYB123K50
	C646		CKSQYB153K50
	C551, C620, C656, C659		CKSQYB222K50
	C559		CKSQYB223K50
	C552, C642, C651, C714, C814		CKSQYB472K50
	C655, C720, C820		CKSQYB683K25
	C705, C805		CKSQYB821K50
	C535, C536, C553, C555, C558		CKSQYF103Z50
	C601, C606, C614-C616, C619		CKSQYF103Z50
	C627-C629, C632, C643, C664		CKSQYF103Z50
	C666, C903, C920, C922, C924		CKSQYF103Z50
	C930-C934		CKSQYF103Z50
	C501, C512, C546, C554, C563		CKSQYF104Z25
	C647, C706, C710, C806, C810		CKSQYF104Z25
	C905, C907, C909, C910		CKSQYF104Z25
	C912, C913, C915-C917, C929		CKSQYF104Z25
	C918		CKSQYF104Z50
	C525, C528, C532, C538, C540		CKSQYF473Z50
	C545, C547, C548, C562, C564		CKSQYF473Z50
	C566-C568, C602, C603, C607		CKSQYF473Z50
	C609-C611, C618, C622-C624		CKSQYF473Z50
	C631, C637, C638, C644, C645		CKSQYF473Z50
	C648-C650, C658, C731, C732		CKSQYF473Z50
	C831, C832		CKSQYF473Z50
RESISTORS			
	VR501 (47kΩ)		RCP1047
	R638 (1Ω, 1/2W)		RCN1059
	R631 (10kΩ)		RCX1048
	R716, R717, R816, R817		RN1/10SE104D
	R646, R653		RS1/2LMFR47J
	Other Resistors		RS1/10S□□□J
OTHERS			
	CN5	13P FFC CONNECTOR	1-177644-3
	CN3, CN4	15P FFC CONNECTOR	1-177644-5
	CN25	3P JUMPER CONNECTOR	52147-0310
	CN51	4P JUMPER CONNECTOR	52147-0410
	CN52	5P JUMPER CONNECTOR	52147-0510

Mark	No.	Description	Parts No.
	CN12	7P JUMPER CONNECTOR	52147-0710
	CN8	KR CONNECTOR	B2B-PH-K-S
	CN14, CN24	KR CONNECTOR	B4B-PH-K-S
	CN50	PH CONNECTOR	B4B-PH-SM3
	CN53, CN6	KR CONNECTOR	B5B-PH-K-S
	CN15, CN7	KR CONNECTOR	B6B-PH-K-S
	CN10	9P JUMPER CONNECTOR	KPC9
	J25	CONNECTOR ASSY 3P	RKP1744
	X501 (37.632MHz)		RSS1041
	X502 (8.389MHz)		RSS1042
	X902 (22.5792MHz)		RSS1046
	X901 (24.5760MHz)		RSS1047
	CN19	CONNECTOR (8P)	TUC-P08P-B1
		PCB BINDER	VEF1040
	KN601, KN901	EARTH PLATE	VNF1084
RF ENV UNIT			
SEMICONDUCTORS			
	Q1401, Q1402		2SC2412K
COILS AND FILTERS			
	L1404, L1405		LFA331J
	L1401, L1403		LFA471J
	L1402		LFA680J
CAPACITORS			
	C1406, C1408		CCSQCH560J50
	C1407		CCSQSL331J50
	C1401, C1405		CCSQSL471J50
	C1410, C1412		CCSQSL561J50
	C1404		CEAS4R7M50
	C1403		CKSQYB102K50
	C1402, C1409, C1411		CKSQYB222K50
RESISTORS			
	All Resistors		RS1/10S□□□J
OTHERS			
	CN20	CONNECTOR (8P)	TUC-P08X-B1
BALANCE IN UNIT			
COILS AND FILTERS			
	F3501-F3506		VTH1018
CAPACITORS			
	C3501, C3502		CFTYA473J50
OTHERS			
	CN3501, CN3502	CANON CONNECTOR	DKN1046
	J3505	CONNECTOR ASSY 6P	RKP1740
BALANCE OUT UNIT			
COILS AND FILTERS			
	L3507, L3508, L3510, L3511		RTF1167
	L3509, L3512		RTF1171
CAPACITORS			
	C3504, C3505, C3507, C3508		CFTXA222J50
	C3503, C3506		CFTYA473J50
OTHERS			
	CN3503, CN3504	3P RECEPTACLE	PKP1004
	CN3506	KR CONNECTOR	S6B-PH-K-S

Mark	No.
INTERFACE UI	
SEMICONDUCTC	
	IC3417
	IC3406
	IC3101, IC3
	IC3405
	IC3102, IC3
	IC3402
	IC3401
	IC3418
	IC3410, IC3
	IC3407
	IC3408, IC3
	IC3403
	IC3415
	IC3414
	IC3404
	Q3108, Q3
	Q3112, Q3
	Q3101, Q3
	Q3201, Q3
	Q3111, Q3
	Q3116, Q3
	D3101-D3
	D3405-D3
	D3401, D3
	D3402, D3
COILS AND FILTE	
	F3101, F32
	F3408
	L3301-L33
	L3402-L34
SWITCHES AND	
	RY3101, RY
CAPACITORS	
	C3460
	C3108, C31
	C3459
	C3443
	C3411, C34
	C3447
	C3301, C33
	C3401, C34
	C3433, C34
	C3116, C31
	C3221
	C3106, C31
	C3206, C32
	C3102-C31
	C3454
	C3427
	C3429
	C3440, C34
	C3302, C34
	C3426, C34
	C3439, C34
	C3450-C34
	C3110, C31
	C3305
RESISTORS	
	R3134-R31
	R3106, R31

replacing,

ailable.

y J = 5%,

No.

C08AF
C10AF
C74AF
CU04AF
)0F

J04F
37K
12K
46
26

26
4EK
4EK

-100AVL

2K
2K
0AX

34
38
U
3J
'1

'1

44

H030C50
H050C50
H060D50
H080D50
H100D50

H101J50
H121J50
H150J50
H200J50
H220J50

Mark	No.	Description	Parts No.
	C634		CCSQCH221J50
	C711, C811		CCSQCH390J50
	C569, C604, C605		CCSQCH470J50
	C715, C815		CCSQSL561J50
	C654		CEANP010M50
	C639		CEANP3R3M50
	C653		CEANP4R7M50
	C661–C663, C665, C668		CEAS010M50
	C641		CEAS100M50
	C502, C503		CEAS331M16
	C524, C529, C533, C537, C539		CEAS470M16
	C549, C561, C608, C617, C621		CEAS470M16
	C625, C630, C633, C635, C636		CEAS470M16
	C669		CEAS470M16
	C657		CEAS4R7M50
	C565		CEASR33M50
	C686		CEASR47M50
	C707, C807, C904, C908		CENA100M50
	C911		CENA101M25
	C703, C704, C708, C709, C716		CENA220M50
	C718, C719, C803, C804		CENA220M50
	C808, C809, C816, C818, C819		CENA220M50
	C906		CENA4R7M50
	C544, C919, C921, C923		CEYA470M25
	C678		CFTXA332J50
	C640, C660, C667		CKSQYB102K50
	C652		CKSQYB123K50
	C646		CKSQYB153K50
	C551, C620, C656, C659		CKSQYB222K50
	C559		CKSQYB223K50
	C552, C642, C651, C714, C814		CKSQYB472K50
	C655, C720, C820		CKSQYB683K25
	C705, C805		CKSQYB821K50
	C535, C536, C553, C555, C558		CKSQYF103Z50
	C601, C606, C614–C616, C619		CKSQYF103Z50
	C627–C629, C632, C643, C664		CKSQYF103Z50
	C666, C903, C920, C922, C924		CKSQYF103Z50
	C930–C934		CKSQYF103Z50
	C501, C512, C546, C554, C563		CKSQYF104Z25
	C647, C706, C710, C806, C810		CKSQYF104Z25
	C905, C907, C909, C910		CKSQYF104Z25
	C912, C913, C915–C917, C929		CKSQYF104Z25
	C918		CKSQYF104Z50
	C525, C528, C532, C538, C540		CKSQYF473Z50
	C545, C547, C548, C562, C564		CKSQYF473Z50
	C566–C568, C602, C603, C607		CKSQYF473Z50
	C609–C611, C618, C622–C624		CKSQYF473Z50
	C631, C637, C638, C644, C645		CKSQYF473Z50
	C648–C650, C658, C731, C732		CKSQYF473Z50
	C831, C832		CKSQYF473Z50
	RESISTORS		
	VR501 (47kΩ)		RCP1047
	R638 (1Ω, 1/2W)		RCN1059
	R631 (10kΩ)		RCX1048
	R716, R717, R816, R817		RN1/10SE104D
	R646, R653		RS1/2LMFR47J
	Other Resistors		RS1/10S□□□J
	OTHERS		
	CN5	13P FFC CONNECTOR	1–177644–3
	CN3, CN4	15P FFC CONNECTOR	1–177644–5
	CN25	3P JUMPER CONNECTOR	52147–0310
	CN51	4P JUMPER CONNECTOR	52147–0410
	CN52	5P JUMPER CONNECTOR	52147–0510

Mark	No.	Description	Parts No.
	CN12	7P JUMPER CONNECTOR	52147–0710
	CN8	KR CONNECTOR	B2B–PH–K–S
	CN14, CN24	KR CONNECTOR	B4B–PH–K–S
	CN50	PH CONNECTOR	B4B–PH–SM3
	CN53, CN6	KR CONNECTOR	B5B–PH–K–S
	CN15, CN7	KR CONNECTOR	B6B–PH–K–S
	CN10	9P JUMPER CONNECTOR	KPC9
	J25	CONNECTOR ASSY 3P	RKP1744
	X501 (37.632MHz)		RSS1041
	X502 (8.389MHz)		RSS1042
	X902 (22.5792MHz)		RSS1046
	X901 (24.5760MHz)		RSS1047
	CN19	CONNECTOR (8P)	TUC–P08P–B1
		PCB BINDER	VEF1040
	KN601, KN901	EARTH PLATE	VNF1084
	RF ENV UNIT		
	SEMICONDUCTORS		
	Q1401, Q1402		2SC2412K
	COILS AND FILTERS		
	L1404, L1405		LFA331J
	L1401, L1403		LFA471J
	L1402		LFA680J
	CAPACITORS		
	C1406, C1408		CCSQCH560J50
	C1407		CCSQSL331J50
	C1401, C1405		CCSQSL471J50
	C1410, C1412		CCSQSL561J50
	C1404		CEAS4R7M50
	C1403		CKSQYB102K50
	C1402, C1409, C1411		CKSQYB222K50
	RESISTORS		
	All Resistors		RS1/10S□□□J
	OTHERS		
	CN20	CONNECTOR (8P)	TUC–P08X–B1
	BALANCE IN UNIT		
	COILS AND FILTERS		
	F3501–F3506		VTH1018
	CAPACITORS		
	C3501, C3502		CFTYA473J50
	OTHERS		
	CN3501, CN3502	CANON CONNECTOR	DKN1046
	J3505	CONNECTOR ASSY 6P	RKP1740
	BALANCE OUT UNIT		
	COILS AND FILTERS		
	L3507, L3508, L3510, L3511		RTF1167
	L3509, L3512		RTF1171
	CAPACITORS		
	C3504, C3505, C3507, C3508		CFTXA222J50
	C3503, C3506		CFTYA473J50
	OTHERS		
	CN3503, CN3504	3P RECEPTACLE	PKP1004
	CN3506	KR CONNECTOR	S6B–PH–K–S

Mark	No.	Description	Parts No.
	INTERFACE UNIT		
	SEMICONDUCTORS		
	IC3417		AT24C01–10SC
	IC3406		CS8402A–CS
	IC3101, IC3201		M5238AP
	IC3405		MC34050P
	IC3102, IC3103, IC3202, IC3203		NJM5532DD
	IC3402		PDC019A (S)
	IC3401		PDG153A9
	IC3418		SM5805CP
	IC3410, IC3419		TC74HC00AF
	IC3407		TC74HC157AF
	IC3408, IC3409, IC3413, IC3416		TC74HC74AF
	IC3403		TC74HCU04AF
	IC3415		TC7W08F
	IC3414		TC7WU04F
	IC3404		TC9246F
	Q3108, Q3110, Q3208, Q3210		2SA1037K
	Q3112, Q3114, Q3212, Q3214		2SB649A
	Q3101, Q3102, Q3107, Q3109		2SC2412K
	Q3201, Q3202, Q3207, Q3209		2SC2412K
	Q3111, Q3113, Q3211, Q3213		2SD669A
	Q3116, Q3216		DTC114EK
	D3101–D3103, D3201–D3203		DA119
	D3405–D3408		DA119
	D3401, D3403		DAN202K
	D3402, D3404		DAP202K
	COILS AND FILTERS		
	F3101, F3201		DTF1064
	F3408		DTF1067
	L3301–L3303		RTF1167
	L3402–L3407		RTF1171
	SWITCHES AND RELAYS		
	RY3101, RY3102, RY3201, RY3202		RSR1029
	CAPACITORS		
	C3460		CCSQCH101J50
	C3108, C3109, C3208, C3209, C3444		CCSQCH120J50
	C3459		CCSQCH220J50
	C3443		CCSQCH270J50
	C3411, C3412, C3456, C3457		CCSQCH470J50
	C3447		CCSQSL471J50
	C3301, C3304		CEAS331M25
	C3401, C3405, C3419, C3420, C3425		CEAS470M16
	C3433, C3441, C3449		CEAS470M16
	C3116, C3117, C3121, C3216, C3217		CENA101M25
	C3221		CENA101M25
	C3106, C3107, C3112–C3115		CENA220M50
	C3206, C3207, C3212–C3215		CENA220M50
	C3102–C3105, C3202–C3205		CENA470M50
	C3454		CFTXA472J50
	C3427		CKSQYB102K50
	C3429		CKSQYB103K50
	C3440, C3455, C3458		CKSQYF103Z50
	C3302, C3402, C3406, C3418, C3421		CKSQYF104Z25
	C3426, C3428, C3432, C3434–C3437		CKSQYF104Z25
	C3439, C3442, C3445, C3448		CKSQYF104Z25
	C3450–C3453		CKSQYF104Z25
	C3110, C3111, C3210, C3211		CKSQYF104Z50
	C3305		OCG1014
	RESISTORS		
	R3134–R3137, R3234–R3237		RD1/6PM100J
	R3106, R3107, R3206, R3207		RD1/6PM104J

Mark	No.	Description	Parts No.
	R3474		RD1/6PM111J
	R3126–R3129, R3226–R3229		RD1/6PM133J
	R3140, R3141, R3240, R3241		RD1/6PM220J
	R3108, R3112, R3208, R3212		RD1/6PM221J
	R3101, R3102, R3138, R3139		RD1/6PM474J
	R3201, R3202, R3238, R3239		RD1/6PM474J
	R3149, R3150, R3249, R3250		RN1/6PQ1002F
	R3110, R3111, R3210, R3211		RN1/6PQ1501F
	R3109, R3113, R3209, R3213		RN1/6PQ2001F
	R3114–R3121, R3214–R3221		RN1/6PQ2002F
	R3104, R3204		RN1/6PQ2701F
	R3103, R3105, R3203, R3205		RN1/6PQ3901F
	Other Resistors		RS1/10S□□□J
	OTHERS		
	CN3402	14P FFC CONNECTOR	52045–1445
	CN3401	24P FFC CONNECTOR	52045–2445
	CN3306	KR CONNECTOR	B5B–PH–K–S
	CN3301, CN3305	KR CONNECTOR	B6B–PH–K–S
	J3405	CONNECTOR	PF05PG–C35
	X3402 (16.9344MHz)		PSS1008
	J3303	CONNECTOR ASSY 4P	RKP1737
	J3304	CONNECTOR ASSY 6P	RKP1738
	X3401 (8.389MHz)		RSS1042
	X3403 (24.56MHz)		RSS1049
	KN3301	EARTH PLATE	VNF1084
	AES/EBU UNIT		
	COILS AND FILTERS		
	L3603, L3604		PTH1016
	L3607		RTF1171
	L3605, L3606		RTL1002
	CAPACITORS		
	C3601–C3603		CKSQYF104Z50
	OTHERS		
	CN3601	CANON CONNECTOR	DKN1046
	CN3602	3P RECEPTACLE	PKP1004
	RESISTORS		
	R3601, R3602		RS1/10S000J
	DIGITAL I/O UNIT		
	SEMICONDUCTORS		
	IC3701		TC74HCU04AF
	Q3701–Q3708		DTA114EK
	COILS AND FILTERS		
	L3701		PTL1003
	L3703		RTF1164
	L3704		RTF1171
	CAPACITORS		
	C3721		CCSQCH220J50
	C3703		CCSQCH470J50
	C3702, C3706		CEAS330M35
	C3709		CEAS470M16
	C3701, C3705, C3712–C3719		CKSQYF103Z50
	C3707, C3708, C3710, C3711, C3720		CKSQYF104Z50
	C3722 (0.1μF)		OCG1014
	RESISTORS		
	All Resistors		RS1/10S□□□J

Mark	No.	Description	Parts No.
	OTHERS		
	CN3701	5P JUMPER CONNECTOR	52147-0510
	JA3702	1P PIN JACK	RKB1021
	JA3701	1P PIN JACK with shield	RKB1027
	CN3702	8P DIN SOCKET	RKN1030

HEADPHONE UNIT

	SEMICONDUCTORS		
	IC1001		M5216L
	COILS AND FILTERS		
	L1002		RTF1167
	F1001, F1003		VTH1018
	CAPACITORS		
	C1003, C1007		CEAL220M16
	C1004		CEAS330M35
	C1001, C1002		CFTXA682J50
	C1005, C1006, C1008, C1009		CKSQYF473Z50
	C1010		CKSQYF103Z50
	RESISTORS		
	VR1001 (20KΩ-B)		RCS1038
	R1009, R1010 (22Ω, 1/6W)		VCN1029
	Other Resistors		RS1/10S□□□J
	OTHERS		
	JA1001	HEADPHONE JACK	RKN1033
	J12	CONNECTOR ASSY 5P	RKP1739
	J29	EARTH LEAD UNIT	XDF-511

POWER SW UNIT

	COILS AND FILTERS		
⚠	L1201		VTL-262
	SWITCHES AND RELAYS		
⚠	S1201		RSA-063
	CAPACITORS		
⚠	C1201-C1203 (0.01μF/400V)		VCG-048
	OTHERS		
		CAPACITOR COVER	REC-150
	H1201, H1202	FUSE HOLDER	RKR1002

TRANS A UNIT

TRANS A unit has no service part.

POWER UNIT

	SEMICONDUCTORS		
⚠	IC408, IC409		ICP-N20
⚠	IC403, IC405		NJM5532DD
⚠	IC404, IC410		NJM7805A
⚠	IC411		NJM7809A
⚠	IC402		NJM78M18FA
⚠	IC406		NJM79M18FA
⚠	Q401		2SA1283
⚠	Q403		2SB942
⚠	Q402		2SD1267
⚠	D402		11ES2
	D405, D406		1SS254
⚠	D407, D410, D412, D413		30DF2-FC5
⚠	D408, D409, D411, D414		30DF2-FC6
⚠	D415, D416		HZ5BLL
⚠	D403		MTZJ33A
⚠	D404		RD15FB
⚠	D401		S4VB20F
	COILS AND FILTERS		
	L401, L402		RTF1167
	CAPACITORS		
	C418		CEAS010M50
	C411, C420		CEAS100M50
	C412, C419		CEAS221M16
	C407		CEAS4R7M50
	C405		CEAS331M50
	C406		CEAS470M35
	C410		CEHAQ010M50
	C415		CEHAQ471M25
	C401, C413		CENA101M25
	C409, C417		CFTYA563J50
	C421		CQMA103J50
	C404 (6800μF/25V)		RCH1033
	C408, C416 (4700μF/50V)		RCH1104
	RESISTORS		
⚠	R401 (47Ω)		DCN1006
⚠	R402		RD1/2PMF222J
	R405, R406, R408, R410		RDR1/4PM103J
	R407, R409		RDR1/4PM512J
	Other Resistors		RD1/6PM□□□J
	OTHERS		
		EARTH PLATE	VNF-091

SW UNIT

	SEMICONDUCTORS		
	Q1702		DTC114EK
	SWITCHES AND RELAYS		
	S1701		RSB1014
	S1702		RSB1015
	RESISTORS		
	All Resistors		RS1/10S□□□J
	OTHERS		
	J39	3P JUMPER WIRE	D20PWW0305E

COPY ID UNIT

	SWITCHES AND RELAYS		
	S1801		RSB1016
	RESISTORS		
	All Resistors		RS1/10S□□□J
	OTHERS		
	J27	3P JUMPER WIRE	D20PWW0305E

DISPLAY UNIT

	SEMICONDUCTORS		
	D1601-D1607		DA119
	SWITCHES AND RELAYS		
	S1601-S1619		RSG1030

Mark	No.	Description	Parts No.
CAPACITORS			
	C1601		CEAL470M16
	C1602		CKSQYF473Z50
RESISTORS			
	All Resistors		RS1/10S□□□J
OTHERS			
	CN33	FFC BOTTOM CONNECTOR 14P	52492-1420
	CN32	FFC BOTTOM CONNECTOR 24P	52492-2420
		REMOTE SENSOR	NJH32H400A
	V1601	FL TUBE	RAW1117
	J50	EARTH LEAD UNIT	XDF-511

VR UNIT

RESISTORS			
	VR1101	(50kΩ-A)	RCV1091
	VR1102	(50kΩ-MN)	RCV1092
	R1101, R1102		RDR1/4PM103J
OTHERS			
	CN45	KR CONNECTOR	B4B-PH-K-S
	CN44	KR CONNECTOR	B5B-PH-K-S

TRANS B UNIT

CAPACITORS			
⚠	C1302, C1303, C1308, C1313, C1314		CKCYF103Z50
⚠	C1301, C1304-C1307, C1312		CKPUYF103Z25

LED UNIT

SEMICONDUCTORS			
	D1901		SLR-342VRT31

RS422 CONTROL UNIT

SEMICONDUCTORS			
	IC3804		M51957AL
	IC3803		MC34050P
	IC3801		PDG154B9
	IC3802, IC3805		TC74HC157AF
	D3801, D3803, D3805, D3807		DAN202K
	D3802, D3804, D3806, D3808		DAP202K
COILS AND FILTERS			
	L3801		RTF1171
CAPACITORS			
	C3803		CEAS470M16
	C3801		CEASR33M50
	C3802, C3804-C3810		CKCYF473Z50
RESISTORS			
	All Resistors		RS1/10S□□□J
OTHERS			
	CN3801	6P JUMPER CONNECTOR	52147-0610
	CN3802	KR CONNECTOR	B2B-PH-K-S
	S3801	DIP SW	RSH1043
	X3801	(9.83MHz)	RSS1048
	KN3801	EARTH PLATE	VNF1084

Mark	No.	Description	Parts No.

D-SUB UNIT

COILS AND FILTERS			
	L3901-L3908		RTF1167
CAPACITORS			
	C3901, C3902		CKCYF473Z50
OTHERS			
	J3902, J3903	9P D-SUB SOCKET	DKN1037

RF UNIT

SEMICONDUCTORS			
	IC301		HA12154MA
	Q303, Q304		2SD1328
	Q301, Q302		2SK932
COILS AND FILTERS			
	L301		ETF9001
CAPACITORS			
	C320		CCSQCH101J50
	C327		CCSQCH121J50
	C329		CCSQCH150J50
	C328		CCSQCH271J50
	C330		CCSQCH330J50
	C323		CCSQCH391J50
	C319		CCSQCH471J50
	C324		CCSQCH820J50
	C335, C337		CEV101M6
	C309		CEV220M6
	C333		CEV470M6
	C339		CEV4R7M25
	C301-C304, C307, C308		CKSQYB103K50
	C310-C318, C321, C322		CKSQYB103K50
	C325, C326, C331, C332, C340		CKSQYB103K50
	C334, C336, C338, C341		CKSQYB104K25
	C305, C306		CKSQYB472K50
	C342 (22 μ F)		ECX9001
RESISTORS			
	VR303, VR304	(1kΩ)	ECP9001
	VR301, VR306	(4.7kΩ)	ECP9002
	VR302, VR305	(6.8kΩ)	ECP9003
	Other Resistors		RS1/10S□□□J
OTHERS			
	CN1	KR CONNECTOR	EKS9001
	CN2	ZH CONNECTOR	EKS9002

9. ADJUSTMENTS

■ Adjustment Conditions

1. Clean the head and tape transit surfaces (tape guide, drum, capstan shaft, and pinch roller).
2. Before making adjustments, warm up the set for a few minutes.
3. Use an oscilloscope with a 10 : 1 probe.

● Test Tapes

Tracking tape	: SDA-101 (TY-7251)
Level tape	: SDA-102 (TY-7111)
Torque meter FWD	: SDA-104 (TY-7131)
Blank tape	: SDA-301
	SDA-302 (TY-30B)
Error-rate adjustment tape	: SDA-111 (SP)
	SDA-112 (HS)

■ Adjustment Items

Mechanical system Adjustment

1. Confirmation and Adjustment of Various Torque Values
2. Tape Pass Confirmation
3. Tape Pass Adjustment

Electrical system Adjustment

1. PLL Adjustment
2. TACH Adjustment
3. ATF Recording Current Adjustment
4. Error Rate Adjustment

■ SETTING THE TEST MODE

● 1.5 TP Test Mode

1. Short-circuit the connectors CN23-7 (XTEST) and CN23-1 (GNDA) of the MAIN unit (refer to Fig. 2-2 on page 65). At this time, "PGM" on the FL tube flashes.
2. Press the counter reset key (C-RESET). At this time, confirm that the counter display part of the FL tube becomes "TACH". (TACH adjustment mode)

● Test mode cancellation

Open the XTEST terminal to cancel this test mode.

● 2-3 waveform setting method

1. Enter into 1.5TP test mode.
2. Connect a stabilized power supply between CN23-6 (VOFT) and CN23-1 (GNDA) and apply +2.5 V.
3. Play back the tracking tape (SDA-101) and execute fine adjustment of the stabilized power supply (around +2.0V) so that the level close to the center of the RF waveform (Ach) becomes a maximum.
4. Execute fine adjustment of the stabilized power supply voltage so that the level close to the center of the RF waveform (Ach) becomes about 2-3 of the level in item 3. (Around +1.5V).

● Test Mode for Recording Current Adjustment

1. Short-circuit the connectors CN23-7 (XTEST) and CN23-1 (GNDA) of the MAIN unit. At this time, "PGM" on the FL tube flashes.
2. Press the counter mode key (C-MODE). At this time, confirm that the P-NO display part of the FL tube becomes "db".

● Test mode cancellation

Open the XTEST terminal to cancel this test mode.

Note: At the time of exchange of the memory IC (INTERFACE UNIT, IC3417), adjustment must be executed after initialization of the memory IC in initialization mode.

● Initialization mode

1. Short-circuit the connectors CN23-7 (XTEST) and CN23-1 (GNDA) of the MAIN unit. At this time, "PGM" on the FL tube flashes.
2. Press the ID mode key (ID-MODE) while holding the mute key (MUTE) pressed. At this time, confirm that the letters "INIT" are flashing on the counter display part of the FL tube.
3. Open the X TEST terminal.

Note: Please note that the last memory functions (following items) all will be initialized when the memory IC is initialized.

* AUDIO ID ON/OFF → ON
* LOCAL/REMOTE switching → LOCAL
* Detection level between tracks → -60 dB
* Drum rotation time cleared
* Error history cleared

■ MECHANICAL SYSTEM ADJUSTMENT

1. Confirmation and Adjustment of Various Torque Values

● Purpose: Checking that the tape is being wound correctly.
● Symptoms of Improper Adjustment :
Large winding torque: The tape run becomes unstable.
Small winding torque: The tape is not wound and auto stop occurs or the cassette is ejected with tape hanging out from the cassette.
Large back-tension torque: Tape damage, head damage.
Small back-tension: The tape run becomes unstable.

Measuring Device/jig	DAT Status	Standard		Adjustment Place and Related Parts
● Torque meter : SDA-104 (TW-7131) ● Cassette weight: R-2606	PLAY mode	Take-up torque	13 ± 4 g · cm	No. 17 drive gear assembly (EXA1123)
		Back tension torque	8 ± 1.5 g · cm	Adjust the position of the spring setting. (Fig. 1–1, Fig. 1–2)
	REVIEW mode	Take-up torque	13 ± 4 g · cm	No. 17 drive gear assembly (EXA1123)
		Back tension torque	10 ± 2 g · cm	Adjust the position of the spring setting. (Fig. 1–3)

Adjustment Procedure

Preparation

● Install the torque meter (SDA-104). (At this time, set the cassette weight, so that the tape does not float up.)
● Press the PLAY key and confirm the above torque values at the time of play mode.
● After the PLAY key has been pressed, press the REW key and confirm the above torque values at the time of REVIEW mode.
● When the standard values are not met, execute adjustment as described above or exchange the parts.

Adjustment Diagram

● PLAY Back Tension Torque

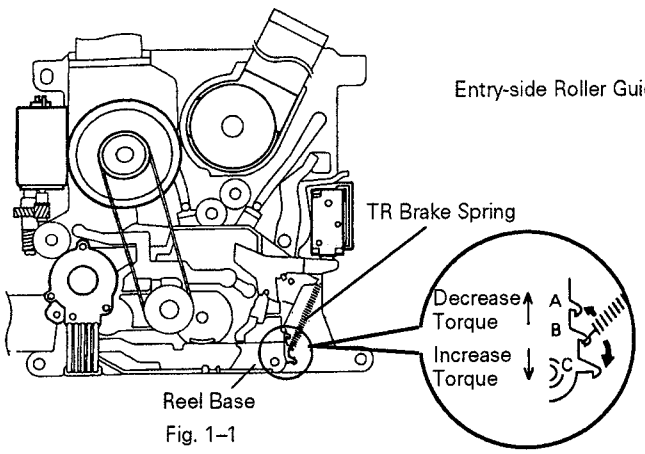


Fig. 1–1

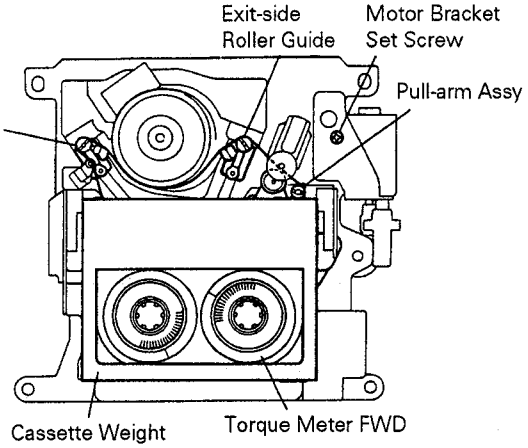


Fig. 1–2

● REVIEW Back Tension Torque

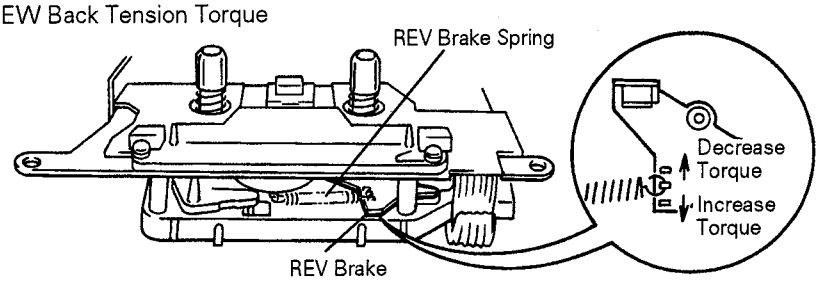


Fig. 1–3

2. Tape Pass Confirmation

● Purpose : To confirm that the tape is correctly aligned with the drum assembly lead. (Tape transit adjustment)
● Symptoms of Improper Adjustment : Sound is interrupted, noise is generated, or sound quality is poor.

Measuring Device/Jig	Measuring Device Connection	DAT State	Part to be Adjusted
● Oscilloscope ● Test Tape : Tracking/ SDA–101 (TY–7251) ● Cassette weight : R2606	● Oscilloscope MAIN unit interior : CH1: Between ENV (CN23–3) and GND A (CN23–1) CH2: Between HSWP (CN23–5) and GND A (CN23–1)	●PLAY mode (Test mode)	●Waveform check

Adjustment Procedure

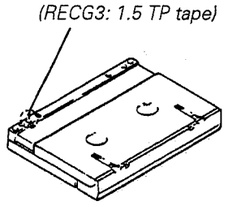
Preparation

● Mount the tracking tape (SDA–101). (At this time, place the cassette weight on the tape.)
● After setting the 1.5 TP test mode, produce the 2–3 waveform and play the tape. (Refer to Page 63.)
1. Check the waveform at this time on the oscilloscope and make sure that the degree of flatness is at least 75%. (At this time, play the tape after confirming that the RECG3 hole of the test tape is open.)
2. If the degree of flatness is less than 75%, perform the procedures described in "3. Tape Pass Adjustment" on Page 67.

● Degree of flatness = B/A x 100 [%]
(refer to Photo 1–1 to photo 1–3)

Adjustment Diagram

Note: Confirm that the hole is open. (RECG3: 1.5 TP tape)



Cassette Rear View

Fig. 2–1

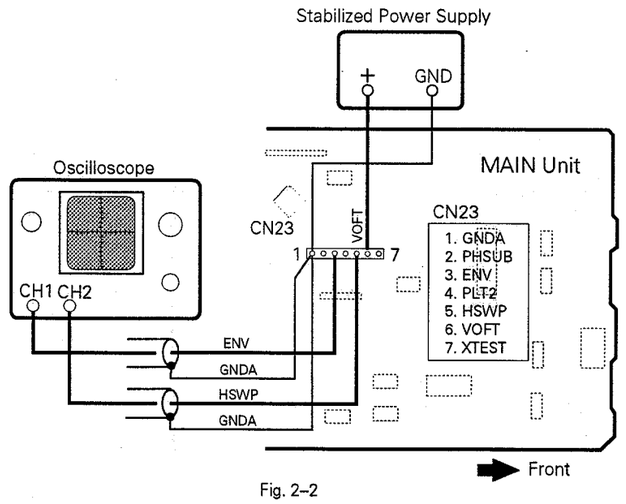


Fig. 2–2

Waveform

● Oscilloscope Range: 50mV/div., 1ms/div.

Normal

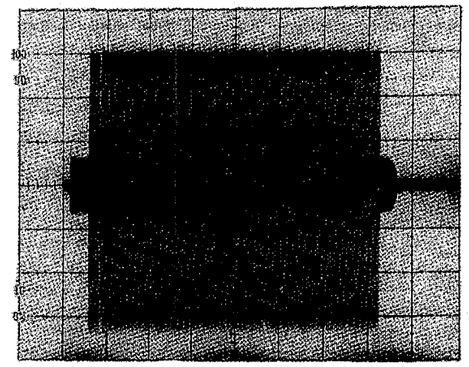


Photo 1–1

Fault on the Entry Side B

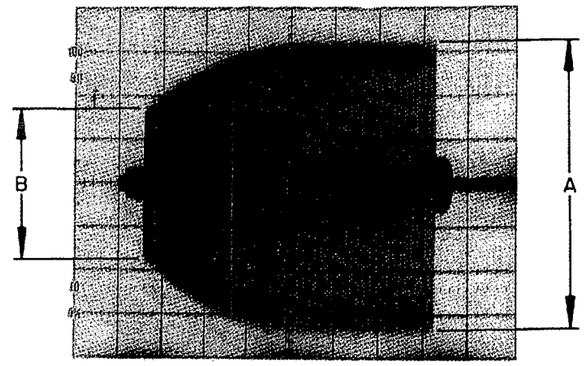


Photo 1–2

Fault on the Exit Side A

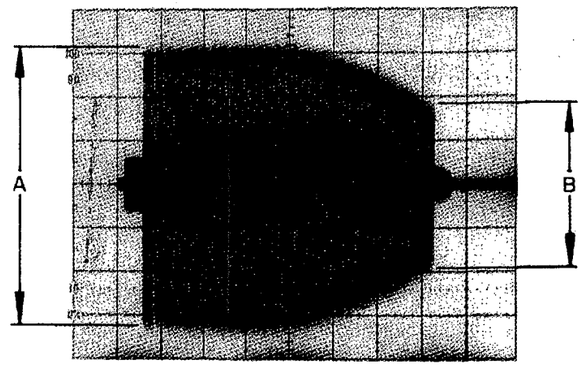


Photo 1–3

3. Tape Pass Adjustment

● Purpose : To confirm that the tape is correctly aligned with the drum assembly lead. (Tape transit adjustment)
● Symptoms of Improper Adjustment : Sound is interrupted, noise is generated, or sound quality is poor.

Measuring Device/Jig	Measuring Device Connection	DAT State	Part to be Adjusted
● Oscilloscope ● Test Tape : Tracking/ SDA–101 (TY–7251) ● Pin–face Screwdriver : R–1784 ● 0–bit Phillips Screwdriver ● Cassette Weight : R–2606	● Oscilloscope MAIN unit interior: CH1 : Between ENV (CN23–3) and GND A (CN23–1) CH2 : Between HSWP (CN23–5) and GND A (CN23–1)	● PLAY mode (Test mode)	● Roller guide (entry and exit sides) ● Pull guide

Adjustment Procedure

3–1. Rough adjustment of guides

1. Turn the entry–side – exit–side roller guides clockwise using the pin–face screwdriver (R–1784) until they lightly touch the end, and then turn them back about one rotation.
2. Turn the guide flange on the pull–arm assy until the top surface of the flange is aligned with the top of the pull–arm shaft. (Refer to Fig. 3–1.)

3–2. Fine adjustment of roller guide height

Preparation

● Mount the tracking tape (SDA–101). (At this time, place the cassette weight on the tape.)
● After setting the 1.5 TP test mode, produce the 2/3 waveform and play the tape. (Refer to Page 63.)
● Confirm that the RECG3 hole of the test tape is open. (Refer to Fig. 3–2.)

[Exit–Side Adjustment]

1. Inspect the RF waveform. If it resembles the waveform shown in Photo 2–4, tighten the exit–side roller guide (about 1–8 rotation). If it resembles the waveform shown in Photo 2–6, loosen the exit–side roller guide (about 1–8 rotation).

[Entry–Side Adjustment]

2. Inspect the RF waveform. If it resembles the waveform shown in Photo 2–3, tighten the entry–side roller guide (about 1–4 rotation). If it resembles the waveform shown in Photo 2–5, loosen the entry–side roller guide (about 1/4 rotation).
3. Observe the RF waveform and repeat Steps 1 and 2 above until the waveform looks like the one shown in Photo 2–2.
4. Press the OPEN/CLOSE key, and once the tape has been ejected, repeat the procedures described in "2. Tape Pass Confirmation". (Refer to Page 65.)

Adjustment Diagram

● The oscilloscope connections and other connections are as indicated in "2. Tape Pass Confirmation" (Page 65).

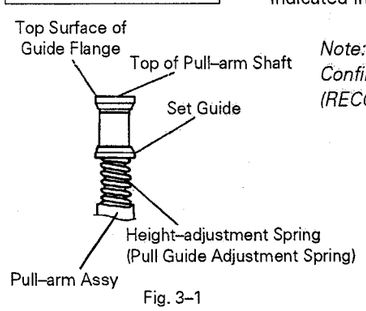
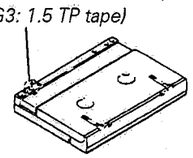


Fig. 3–1

Note:
Confirm that the hole is open.
(RECG3: 1.5 TP tape)



Cassette Rear View

Fig. 3–2

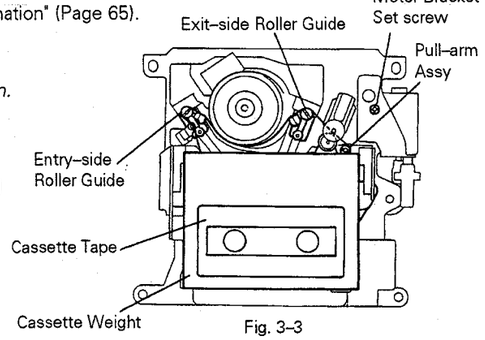


Fig. 3–3

Waveform

● Oscilloscope Range : 50mV/div., 1ms/div.

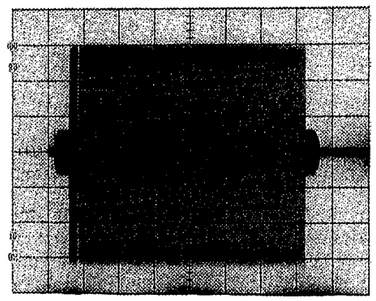


Photo 2–1
Maximum RF Output Level

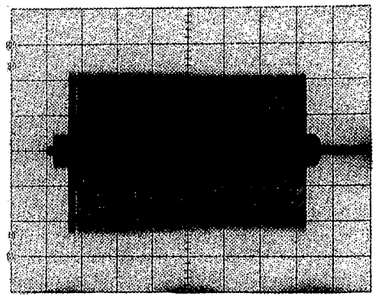


Photo 2–2
2–3 RF Output Level

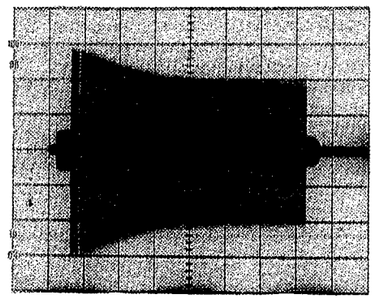


Photo 2–3
Entry–Side Guide Roller Too High

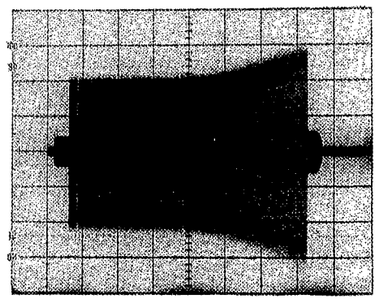


Photo 2–4
Exit–Side Guide Roller Too High

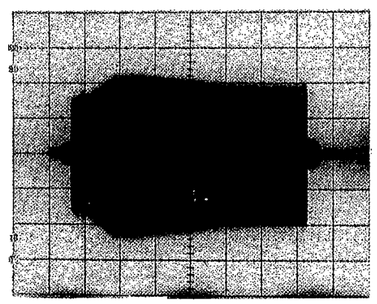


Photo 2–5
Entry–Side Guide Roller Too Low

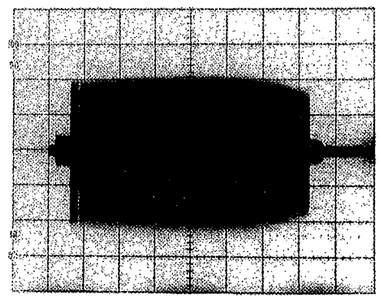


Photo 2–6
Exit–Side Guide Roller Too Low

3–3. Fine Adjustment of Pull Guide

Preparation

- Refer to pages 8 and remove the DAT mechanism assembly from the cassette installation unit.
- Place the cassette weight onto a commercial 120 min. tape and set it into the mechanism.

Adjustment

1. Play the tape and set the CUE mode by holding down the FF/CUE key when the tape starts winding. Check for twisting of the tape between the pinch roller and the pull guide by observing the image of the motor bracket setscrew head reflected on the magnetic surface of the tape. The relationship between the reflected image of the screw head and the height of the pull–guide flange is shown in Fig. 3–4.
2. Slowly tighten the pull–guide flange, turning it 180 degrees from its rough–adjusted position, and confirm that the appearance of the reflected image continuously changes from (c) to (a) during this process.
3. Then, while loosening the pull–guide flange 180 degrees, confirm that the appearance of the reflected image continuously changes from (a) to (c).
4. Tighten the pull–guide flange until the top edge of the tape curls slightly and the screw image resembles the shape shown in (b), and then loosen the flange 90 degrees.
5. Set the REW mode by pressing and holding down the REW/REV key. Confirm that the tape does not curl at Points A and B in Fig. 3–5.
6. After confirming that the tape is not twisted at Point C in Fig. 3–6, check the tape for twisting or bulging at Point D. (Normal bulge : no more than 0.5mm)
7. Press the OPEN/CLOSE key and eject the tape. Replay the tape, and keeping the FF/CUE key pressed down, observe the reflected image of the screw head and confirm that it has the same appearance as that shown in (c).
8. Press and hold down the REW/REV key and confirm that curling and twisting at Points A to D are the same.
9. Apply a locking adhesive to the screw on top of the pull–guide flange and lock the screw.

Adjustment Diagram

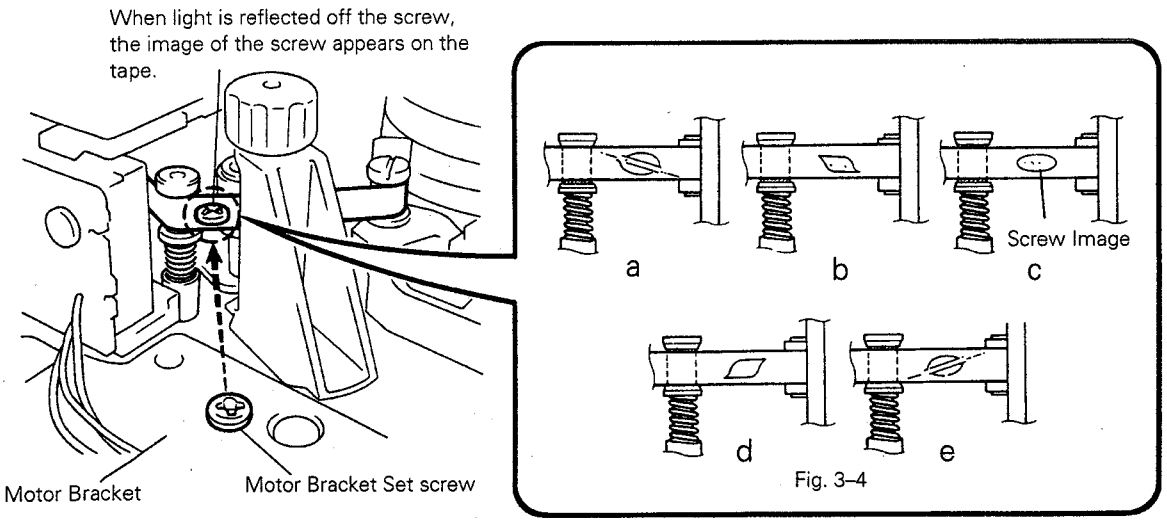


Fig. 3–4

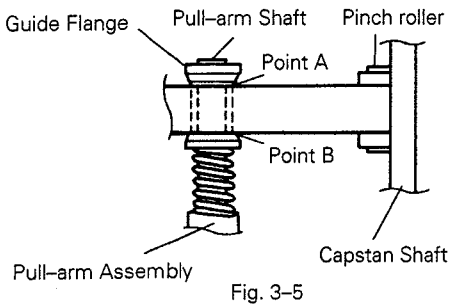


Fig. 3–5

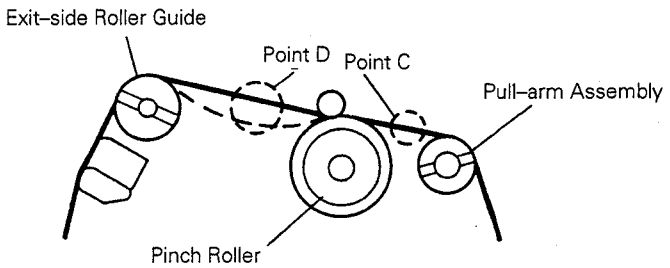


Fig. 3–6

■ ELECTRICAL SYSTEM ADJUSTMENT

1. PLL Adjustment

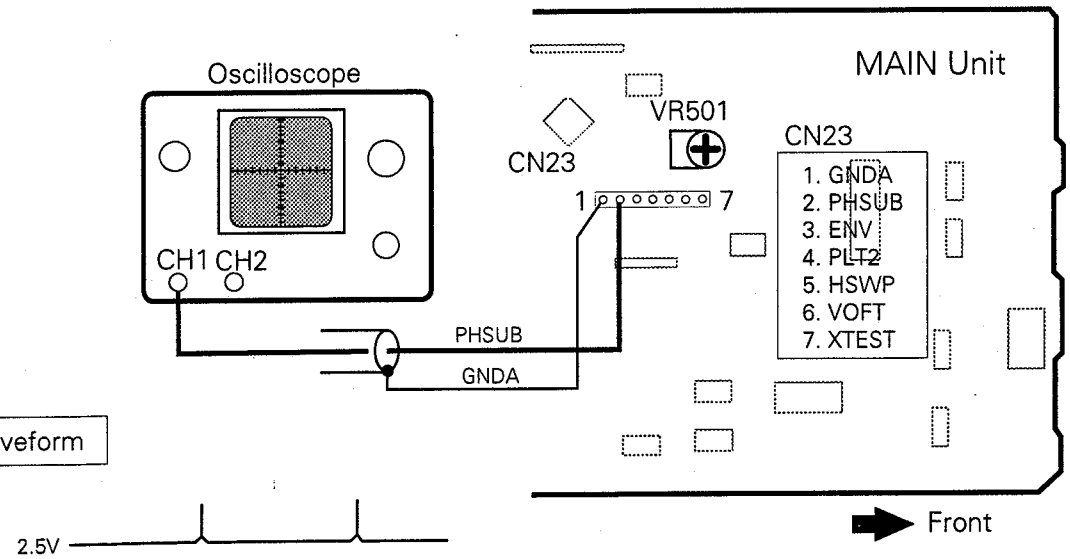
● Purpose : To correctly access digital signals stored in the tape.
● Symptoms of Improper Adjustment : Sound is intermittent, unit does not playback, noise is generated, or meter fails to oscillate.

Measuring Device/Jig	Measuring Device Connection	DAT State	Part to be Adjusted
● Oscilloscope ● Test Tape Blank Tape : SDA-301	● Oscilloscope MAIN unit interior : CH1 : Between PHSUB (CN23-2) and GND A (CN23-1)	● STOP mode	● MAIN unit VR501 (VCO RANGE ADJ.)

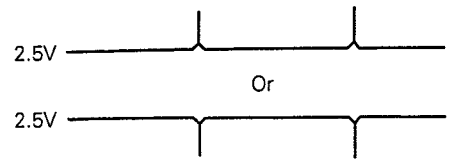
Adjustment Procedure

1. Insert the test tape.
2. Adjust the output voltage of the CN23-2 (PHSUB) to 2.5V. (At this time, if the beard-shaped pulses in the waveform are just slightly visible or disappear completely, adjust the voltage above or below 2.5V.)

Adjustment Diagram



Waveform



● If the beard-shaped pulses in the waveform are just slightly visible or disappear completely, adjust the voltage above or below 2.5V.

Fig. 4

2. TACH Adjustment

● Purpose : To match the recording position with the tape format.
● Symptoms of Improper Adjustment : Tapes recorded on other machines have intermittent sound or noise increases and the MUTE comes on. (Tapes recorded on this unit perform without problems.)

Measuring Device/Jig	Measuring Device Connection	DAT State	Part to be Adjusted
● Oscilloscope ● Test tape Tracking : SDA-101 (TY-7251)	● Oscilloscope MAIN unit interior : CH1 : Between ENV (CN23-3) and GND A (CN23-1) CH2 : Between HSWP (CN23-5) and GND A (CN23-1)	● PLAY mode (Test mode)	● MS key "+", "–"

Adjustment Procedure

Preparation

● Set the 1.5 TP test mode. (Refer to Page 63.)
1. Press the MS keys "+" or "–" to adjust so that the RF waveform marker position becomes 800 μs ± 20 μs from the drop of the HSWP waveform.

Note

The TACH adjustment is adjustment by means of the microcomputer, where the adjustment data are stored in the memory, and as the adjusted data are stored in the memory at the time of test mode cancellation, do not switch off the power supply while in test mode.

Waveform

● Oscilloscope Range :
CH1 : AC 500mV/div., 200 μs/div.
CH2 : DC 2V/div. (Trigger)

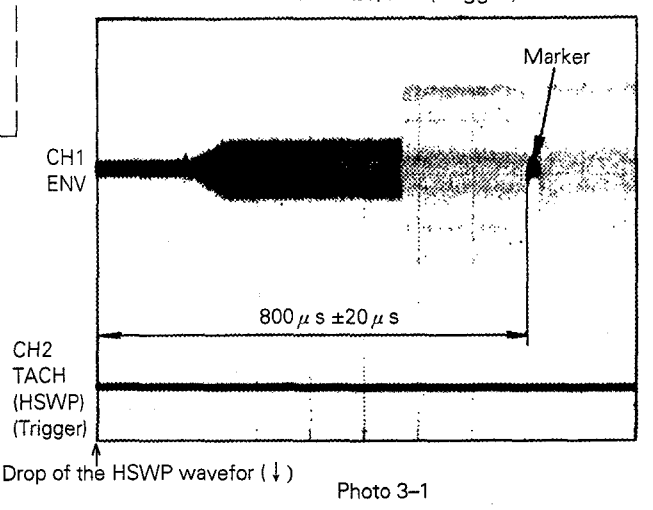


Photo 3–1

Adjustment Diagram

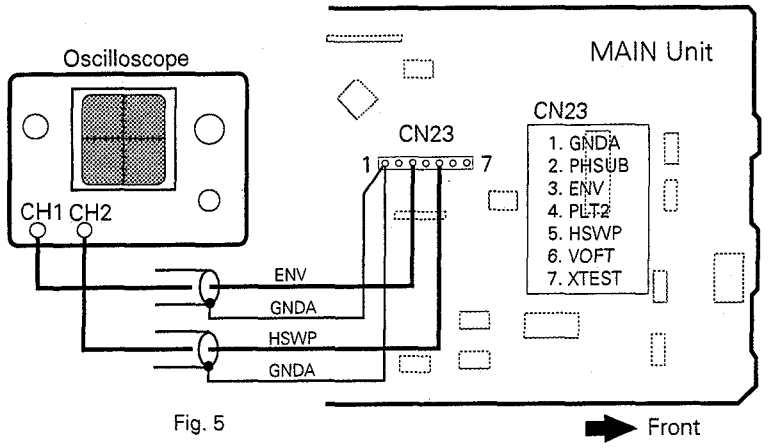


Fig. 5

3. ATF Recording Current Adjustment

● Purpose : To obtain the ideal recording current value.
● Symptoms of Improper Adjustment : Sound is intermittent (tracking cannot be obtained) or noise is generated.

Measuring Device/Jig	Measuring Device Connection	DAT State	Part to be Adjusted
● Oscilloscope ● Test Tape Level : SDA–102 (TY–7111) Blank : SDA–302 (TY–30B) *NOTE :* *Use an unused portion of tape where RF signals have not been recorded.*	● Oscilloscope MAIN Unit interior : CH1 : Between PLT2 (CN23–4) and GND A (CN23–1) CH2 : Between HSWP (CN23–5) and GND A (CN23–1)	● PLAY and REC modes	● RF unit VR305 (A head) VR302 (B head)

Adjustment Procedure

Preparation

● Set the test mode for adjustment of recording current. (Refer to Page 63.)

1. Play the level–use test tape (SDA–102) and record the voltage value at Points (a) and (b) on the waveform. (Refer to Photo 4–1.)
2. Confirm that the blank tape has not been used or has an unused portion. Press the REC key and then the PAUSE key. Record the signal from the unit's built–in transmitter on the tape for 30 to 60 seconds.
3. Stop the recording and rewind the recorded portion of the tape. Confirm that the levels of the reproduced waveform are within $\pm \frac{25}{20}$ % of levels (a) and (b) recorded according to the procedure described in Step 1. (Refer to Photo 4–2.)
4. When the values are outside the standard, slightly turn VR305 for A head or VR302 for B head, and record the signal again on an unused portion of tape. Confirm the levels as described in Step 3.
5. Repeat Steps 3 and 4 and make adjustments until the values are within the standard.

Adjustment Diagram

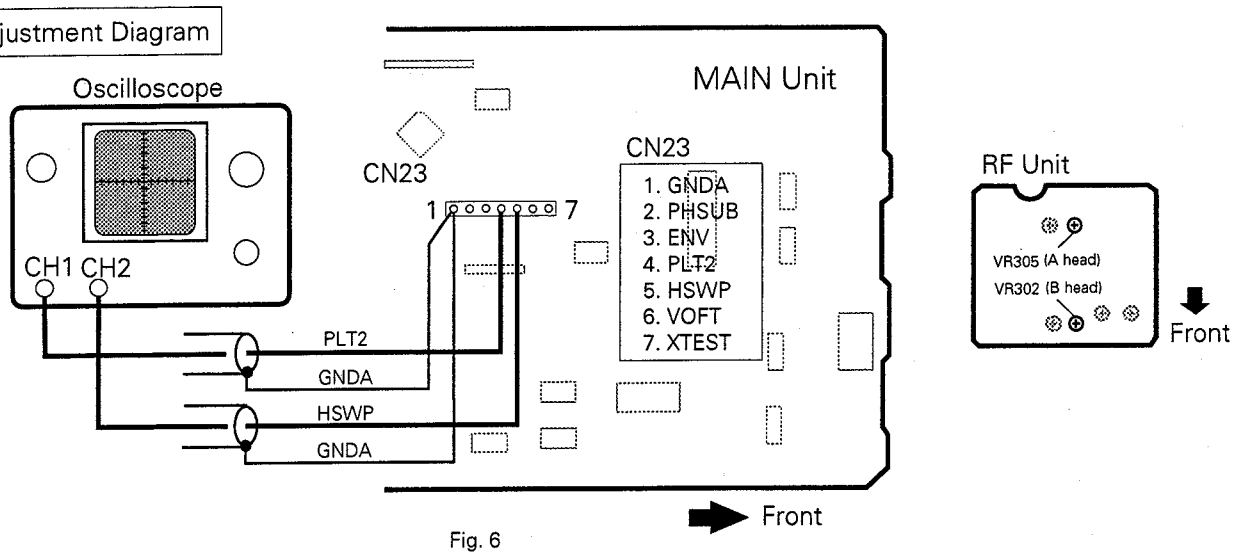


Fig. 6

Waveform [ ] : Reference

During Playback of Level Tape (SDA–102)

● Oscilloscope Range CH1 : 0.5V/div., 2.5ms/div.
CH2 : 5V/div.

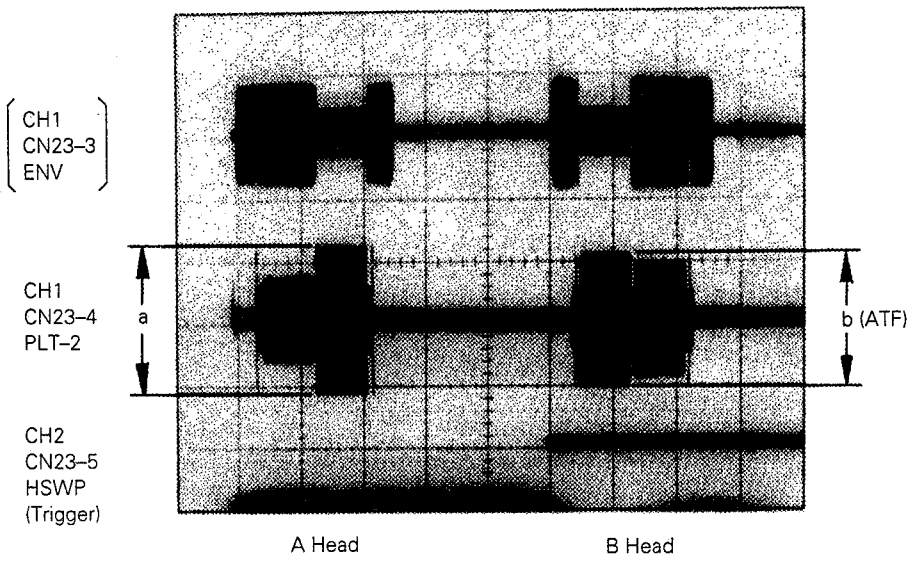


Photo 4–1

During Playback of Self–recorded Blank Tape

● Oscilloscope Range CH1 : 0.5V/div., 3ms/div. (PCM)
[CH1 : 100mV/div., 3ms/div] (ATF)
CH2 : 5V/div.

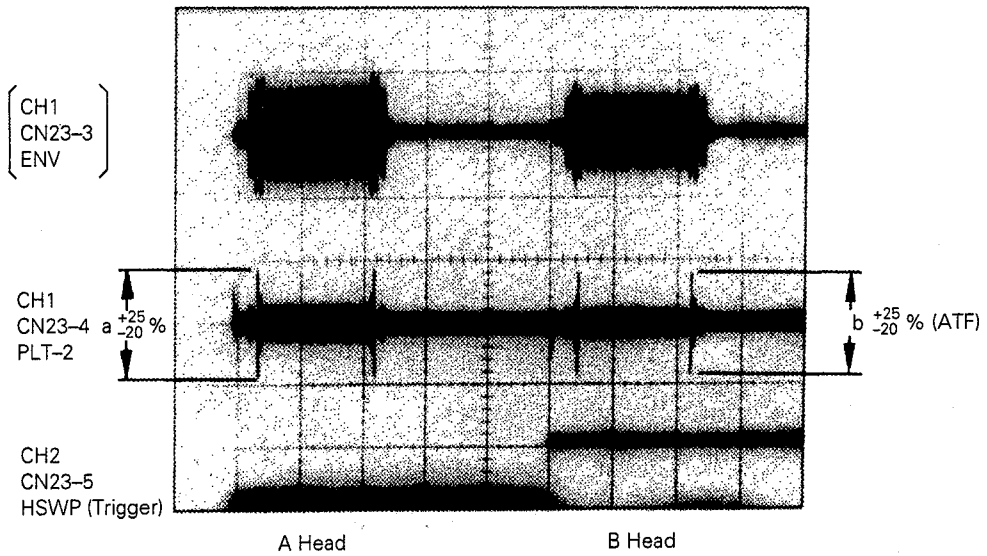


Photo 4–2

4. Error Rate Adjustment

● Purpose : To reproduce the correct data.
● Symptoms of Improper Adjustment : Units skips during playback, noise is generated, or meter does not oscillate.

Measuring Device/Jig	Measuring Device Connection	DAT State	Part to be Adjusted
● Test Tape Error Rate Adjustment Tape : SDA-111 (SP) : SDA-112 (WSP) ● Error Rate Counter [● Oscilloscope]	● Error rate counter MAIN unit interior Connector : CN24 ● Oscilloscope MAIN Unit interior : CH1 : Between FLAG (CN24-3) and GND D (CN24-1)	●PLAY mode	● RF unit VR303 (SP) VR304 (HS)

Adjustment Procedure

Preparation

● Connect the error rate counter connector to CN24 inside the signal processing unit and set the error rate counter timer at 10sec.

1. Play the error rate adjustment tapes (SDA-111 and SDA-112) and make adjustments so that the error rate is as small as possible.

[If the error rate counter is not used]

1. Play the error rate adjustment tapes (SDA-111 and SDA-112) and make adjustments so that the oscilloscope waveform error flag is the same as that shown in Photo 5. (Adjust until the error rate is as small as possible.)

Adjustment Diagram

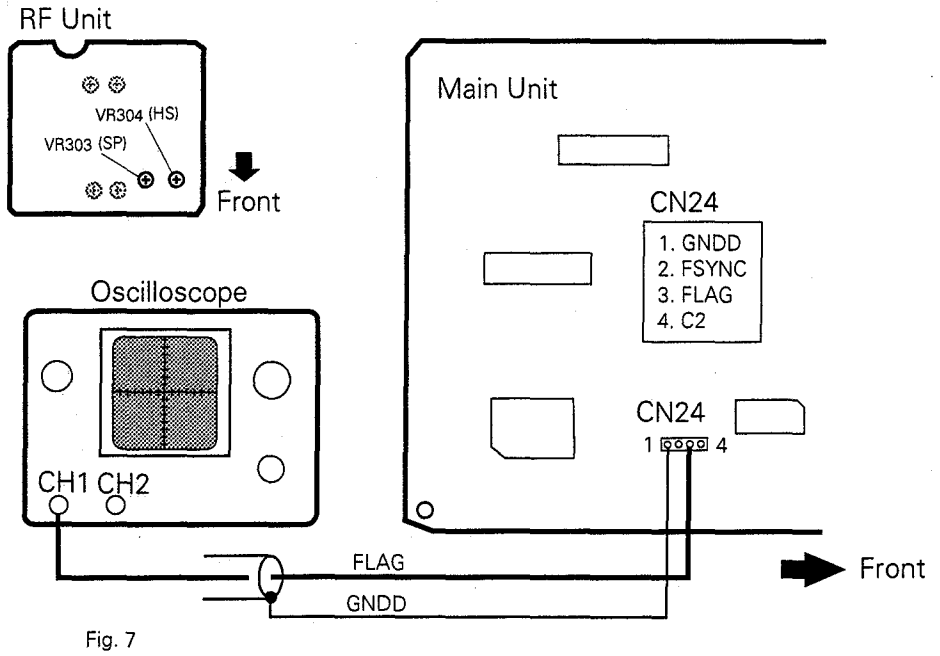


Fig. 7

Waveform

● Oscilloscope Range CH1 : 2 V/div., 5 ms/div.
[During SP]

When error rate is 1×10^{-1}

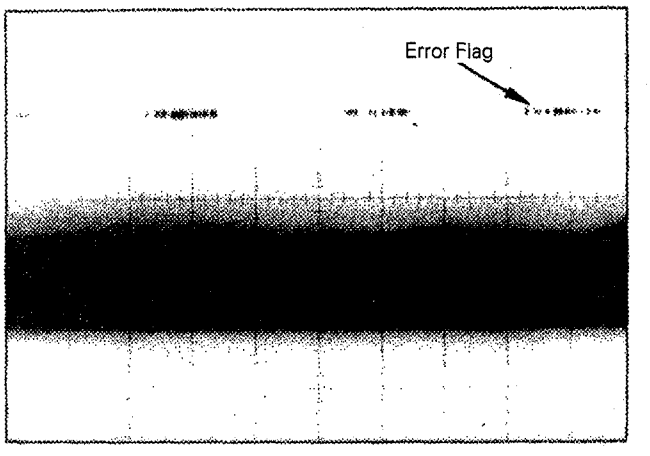


Photo 5–1

When error rate is 2×10^{-2}

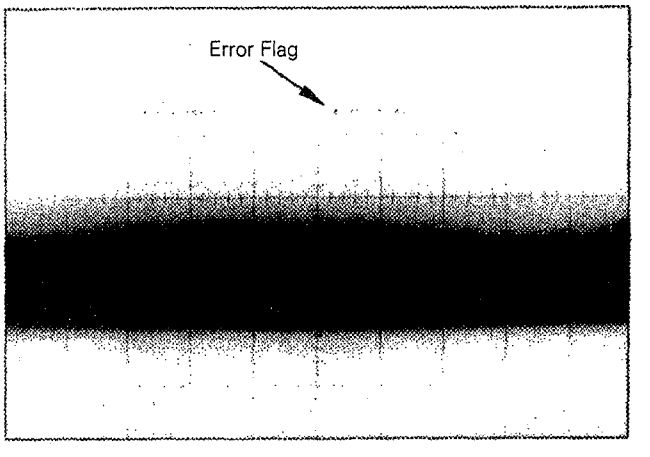


Photo 5–2

When error rate is 5×10^{-4}

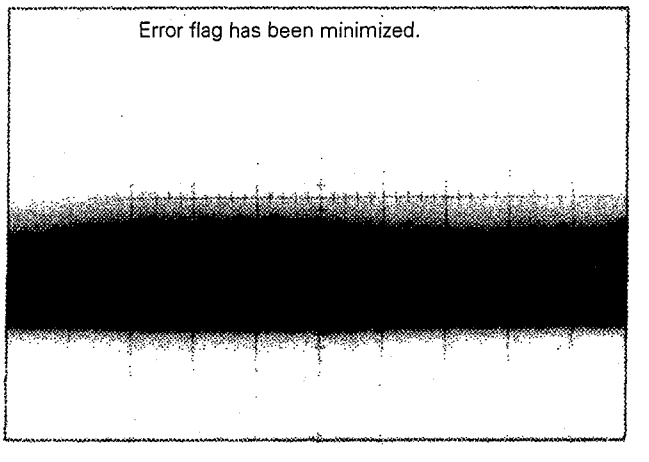


Photo 5–3

10. IC INFORMATION

● *The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.*

■ PDC019A (IC3402: INTERFACE UNIT)

● EFM Encoder IC

● Pin Function

No.	Name	I/O	Description
1	DIN1	I	Optical module correspondence data input terminal
2	DIN2		
3	DIN3	I	Coaxial input terminal
4	DIN4	I	AES/EBU input terminal
5	DIRRC1	I	RC oscillator input terminal
6	DIRRC2	O	RC oscillator output terminal
7	AVDD	–	Analog current terminal
8	DIRRS	I	VCO oscillation band adjustment input terminal
9	AGND	–	Analog ground terminal
10	DIRVCO	I	VCO free–running oscillation setting input terminal
11	DIRLPF	O	PLL low–pass filter terminal
12	Vss	–	Ground terminal
13	VDD	–	+5 V power supply terminal
14	DIRCK	O	System clock output terminal for DIR
15	DIRBCK	O	Bit clock output terminal for DIR
16	DIRLRCK	O	LR clock output terminal for DIR
17	DIRDATA	O	DIR demodulation data output terminal
18	DIRWDCK	O	Word clock output terminal for DIR
19	DIRU	O	U bit output terminal
20	DIRERR	O	Data error or lock status monitor output terminal
21	OPTSW	O	Optical module current–OFF signal output terminal
22	CJSDATA	I	Clock jitter suppressor data input terminal
23	CJSBCK	I	Clock jitter suppressor bit clock input terminal
24	CJSLRCK	I	Clock jitter suppressor LR clock input terminal
25	JITVCOIN	I	VCO input terminal
26	JITLPFO	O	LPF output terminal
27	JITLPFI	I	LPF input terminal

No.	Name	I/O	Description
28	JITPCO	O	Phase comparator output terminal
29	JITERR	O	Lock status monitor signal output terminal
30	DACDATA	O	DAC data output terminal
31	DACBCK	O	DAC bit clock output terminal
32	DACLRCK	O	DAC LR clock output terminal
33	ADCDATA	I	ADC recording data input terminal
34	ADCCLK	O	ADC clock output terminal
35	ADCBCK	O	ADC bit clock output terminal
36	ADCLRCK	O	ADC LR clock output terminal
37	ADCSTBY	O	ADC standby signal output terminal
38	XTALIN	I	System clock input terminal
39	XTALOUT	O	System clock output terminal
40	Vss	–	Ground terminal
41	VDD	–	+5 V power supply terminal
42	DACCKOUT	O	DAC system clock output terminal
43	ENCCKOUT	O	CD decoder system clock output terminal
44	CDDATA	I	CD decoder data input terminal
45	CDBCK	I	CD decoder bit clock input terminal
46	CDLRCK	I	CD decoder LR clock input terminal
47	CDTX	I	Input terminal from the CD decoder output
48	DITOUT	O	Biphase modulation output terminal
49	TP6	I	For test use
50	$\overline{\text{RESET}}$	I	System reset input terminal
51	TP7	I	For test use
52	$\overline{\text{CAS}}$	O	DRAM column address strobe signal output signal
53	$\overline{\text{OE}}$	O	DRAM output enable signal output signal
54 I 60	A8 I A2	O	DRAM address output terminal
61	VDD	–	+5 V power supply terminal
62	Vss	–	Ground terminal
63	A1		DRAM address output terminal
64	A0	O	
65	A9		

No.	Name	I/O	Description
66	$\overline{RAS}$	O	DRAM row address strobe signal output terminal
67	$\overline{WR}$	O	DRAM read/write signal output signal
68	DQ2	I/O	DRAM data I/O terminal
69	DQ1	I/O	
70	DQ4	I/O	
71	DQ3	I/O	
72 | 74	TP0 | TP2	I	For test use
75	TP3	O	For test use
76	ENCVCOIN	I	Encoder circuit clock input terminal
77	ENCLPFO	O	LPF output terminal
78	ENCLPFI	I	LPF input terminal
79	ENCPCO	O	Phase comparator output terminal
80	ENCERR	O	Clock status monitor signal output terminal
81	TP4	O	For test use
82	TP5	I	
83	RFDET	I	RF signal input terminal
84	$\overline{RECEN}$	I	Recording permission signal input terminal
85	XSAMPLE	O	Sample servo sample pulse signal output terminal
86	DET4T	O	4T detection signal output terminal
87	DET3T	O	3T detection signal output terminal
88	EFM	O	EFM signal output terminal
89	VDD	–	+5 V power supply terminal
90	Vss	–	Ground terminal
91	ENCCK	O	Encoding clock output terminal
92	EXTACK	O	ATIP sync notification signal output terminal
93	$\overline{EXTSYNC}$	I	ATIP sync permission signal input terminal
94	ATIPSYNC	I	ATIP sync signal input terminal
95	SUBSYNC	O	Subcode sync signal output terminal
96	CCB	I	CPU interface method switching signal input terminal
97	CE	I	CPU interface chip enable signal input terminal
98	CL	I	CPU interface data transmission clock input terminal
99	DI	I	CPU interface data input terminal
100	DO	O	CPU interface data output terminal

■ PDG152B9 (IC503: MAIN UNIT)

● System Controller IC

● Pin Function

No.	Name	I/O	Description	CPU Name
1	ENC3	I	Mechanism encoder output BIT3 input terminal	PF3
2	ENC0	I	Mechanism encoder output BIT0 input terminal	PF4
3	x256	O	256/384 Fs clock selection control output terminal Becomes "H" at the time of Fs = 32 (kHz) recording/playback (when ID2 of PCM–ID is "10"). (Also becomes "H" at the time of Fs = 64 (kHz) WSP/WLP mode.)	PF5
4	x44PB	O	Master clock selection control output terminal Selection and oscillation of the master clock at the time of Fs = 44.1 (kHz)recording/playback. Clock oscillation with "L". (Also becomes "H" at the time of Fs = 88.2 (kHz) WSP mode.)	PF6
5	x4832PB	O	Master clock selection control output terminal Selection and oscillation of the master clock at the time of Fs = 48/32 (kHz) recording/playback. Clock oscillation with "L". (Also becomes "H" at the time of Fs = 96/64 (kHz) WSP/WLP mode.)	PF7
6	D IN	O	Digital input recording mode monitor output terminal Becomes "H" in digital input recording mode. Used for mute processing at the time of RX–PLL unlocked.	PD0
7	GNDD	I	Connected to GND level.	PD1
8	xDARST	O	Audio block reset output terminal Becomes "L" at the time of power ON, Fs, REC/PB switching and resets the audio block (A/D converter, D/A converter).	PD2
9	MLE	O	D/A converter mode set latch output terminal Connected to the LATCH terminal (pin 20) of PD2029. The transmission data from the microcomputer are latched by the rising edge (↑).	PD3
10	WSMODE	O	Audio block double speed mode switching output A/D, D/A block switching is executed according to the operation mode. Becomes "H" at the time of WSP and WLP mode.	PD4
11	PBMUTE	O	Playback mute control output terminal Connected to the MUTE terminal (pin 1) of the signal processing LSI IC 501 (HD49226AFS). Execution of muting (digital muting) ON/OFF control for the playback output signal. Muting ON with "H".	PD5
12	LVDATA	I	Level meter data input terminal Connected to the LVDATA terminal (pin 97) of the signal processing LSI IC 501 (HD49226AFS).	PD6
13	LVCK	O	Level meter data clock output terminal Connected to the LVCK terminal (pin 96) of the signal processing LSI IC 501 (HD49226AFS). The shift clock for level data reading every half frame is generated for 8 pulses each in the sequence of L (ch) and R (ch) (for one frame each in WSP mode).	PD7
14	QDATA	I	CD Q data input terminal Connected to the QDATA terminal (pin 68) of the signal processing LSI IC 501 (HD49226AFS).	PC0
15	QDCK	O	CD Q data shift clock output terminal Connected to the QDCK terminal (pin 67) of the signal processing LSI IC 501 (HD49226AFS). Generation of the shift clock for CD Q data reading by 8 pulses each in the sequence of TNO and INDEX.	PC1

No.	Name	I/O	Description	CPU Name
16	LPMODE	O	LP mode selection output terminal Connected to the LP terminal (pin 60) of the signal processing LSI IC 501 (HD49226AFS). Selection of the signal processing LSI operation mode at the time of LP playback mode. "H" at the time of WLP mode. (WLP mode is the mode for half-speed LP playback.) Becomes "L" in the other LP, SP, and WSP modes. (LP is the mode for double scan LP playback, and in SP and WSP mode, the status of this terminal has no influence onto the operation.)	PC2
17	PLTL	I	PILOT level status monitor input terminal	PC3
18	RF	I	RF signal YES/NO monitor input terminal	PC4
19	CRLOCK	I	Capstan reel lock monitor input terminal	PC5
20	DLOCK	I	Drum lock monitor input terminal	PC6
21	PLLLOCK	I	Input terminal for DPLOCK monitor at the time of play and for PLLLOCK monitor at the time of high-speed search	PC7
22		I		PH0
23	xINLEV	I	Rear panel input sensitivity DIP switch ON/OFF status input terminal	PH1
24	xSRVRST	O	Servo LSI reset output terminal Connected to the RESET terminal (pin 61) of the servo LSI IC 601 (HD49228FS). The servo LSI is reset at the time of power ON/OFF and when switching from search mode to another mode.	PH2
25	BRAKE	I	Drum brake control monitor input terminal	PH3
26	RFMODE	O	RF amplifier operation switching output terminal Connected to the MODE1 terminal (pin 42) of the RF amplifier IC 301 (HA12154MA). Becomes "H" at the time of WSP mode. Executes control of the second amplifier of the RF amplifier and the equalizer.	PH4
27	TEST	O	Data strobe LSI test mode control output terminal Connected to the TEST terminal (pin 54) of the data strobe LSI IC 504 (HD49229). Becomes "H" at the time of VCO free-running adjustment mode (at the time of test mode). At this time, the xSER terminal must be "H".	PH5
28	xSER	O	Data strobe LSI search mode control output terminal Connected to the SEARCH terminal (pin 1) of the data strobe LSI IC504 (HD49229). Becomes "L" at the time of search run modes like FF, REW, etc. At this time, the TEST terminal must be "L".	PH6
29	RP	O	RF amplifier recording/playback mode switching output terminal Connected to the RECPB terminal (pin 39) of the amplifier IC 301 (HA12154MA) as AND output with the output from the RECPB terminal (pin 24) of the signal processing LSI IC 501 (HD49226AFS). Executes control of recording/playback mode switching for the RF amplifier IC. The output from this microcomputer is for protection.	PH7
30	xRST	I/O	System reset terminal "L" level active. Connected to the output terminal (pin 5) of the reset IC 505 (M51957AL).	$\overline{\text{RST}}$
31	EXTAL	I	System clock oscillation ceramic clock connection terminal (input) An 8.38 (MHz) ceramic oscillator is connected between this pin and pin 40.	EXTAL
32	XTAL	O	System clock oscillation ceramic clock connection terminal (output)	XTAL
33	Vss	–	GND terminal. Connected to ground.	Vss
34	NC	O	Not used terminal	TX
35				TEX

No.	Name	I/O	Description	CPU Name
36	AVss	–	A/D converter GND terminal Connected to ground.	AVss
37	AVREF	–	A/D converter reference voltage input terminal Connected to the 5 (V) line.	AVREF
38	LMUTE	O	Line muting control output terminal Executes line muting (analog muting) ON/OFF control. Muting ON with "H".	PA0/AN0
39	xOPRST	O	Operation control reset terminal The operation control IC 3401 (PDG153A9) is reset with "L". "L" is put out at the time of power ON. "L" also is put out when the communication between operation control (IC 3401) and system control (IC 503) (PDG152A9) is interrupted.	PA1/AN1
40	xOPREQ	O	Output terminal for communication requests to the operation control The operation control starts communication with the system control at the dropping edge (↓) of xOPREQ. "L" state exists during the communication with the operation control.	PA2/AN2
41	LPRUN	O	LP run mode monitor output terminal Becomes "H" at the time of LP run mode (tape speed = 4.075 mm). ("L" at the time of SP, WSP, and WLP run mode.)	PA3/AN3
42	RSACK	I	Input terminal for communication permission from the RS422 control The system control starts communication with the RS422 control at the edge of RSACK. Reversion is executed on completion of each byte of communication.	PA4/AN4
43	xADJ	O	TACH adjustment mode output terminal Output of "L" at the time of adjustment mode.	PA5/AN5
44	TTOP	I	Input terminal for the tape top sensor output Used as AN6 (analog input).	PA6/AN6
45	TEND	I	Input terminal for the tape end sensor output Used as AN7 (analog input).	PA7/AN7
46	FGS	I	Supply–side reel FG input terminal Used as interrupt terminal (CINT).	PB0/CINT
47	CTRL	O	Microcomputer data transfer mode input control signal–Microcomputer command control signal output terminal Connected to the CTRL terminal (pin 2) of the signal processing LSI IC 501 (HD9226AFS) and the CTRL terminal (pin 3) of the servo LSI IC 601 (HD49228FS).	PB1/$\overline{CS0}$
48	CCK	O	Serial data transfer clock output terminal Used as the SCK0 terminal. Connected to the shift clock input terminal of the device (signal processing LSI, servo LSI, operation control, D/A converter, RS422 control) controlled from the microcomputer by serial communication. The serial clock period is 1.95 (μ s) for signal processing LSI, servo LSI, and operation control, and it is 3.8 (μ s) for the D/A converter. The interval clock period is 30.5 (μ s) for signal processing LSI, servo LSI, and operation control, and it is 61 (μ s) for the D/A converter. (fex: @ 8.38 MHz)	PB2/$\overline{SCK0}$
49	CDATAO	I	Serial data input terminal (matched to the terminal name on the side of the signal processing LSI. The data I/O direction is opposite to the terminal name.) Used as SI0 terminal. Connected to the serial data output terminal of the device (signal processing LSI, operation control, RS422 control) controlled from the microcomputer by serial communication.	PB3/SI0
50	CDATAI	O	Serial data output terminal (matched to the terminal name on the side of the signal processing LSI. The data I/O direction is opposite to the terminal name.) Used as SO0 terminal. Connected to the serial data input terminal of the device (signal processing LSI, servo LSI, operation control, D/A converter, RS422 control) controlled from the microcomputer by serial communication.	PB4/SO0

No.	Name	I/O	Description	CPU Name
51	xRSREQ	O	Output terminal for communication requests to the RS422 control The RS422 control starts communication with the system control at the dropping edge (↓) of SREQ. The level is "L" during communication with the RS422 control.	PB5/$\overline{SCK1}$
52	HUNT	O	Encoder hunting prevention output terminal xOR output for LDM_ON and MDM_ON.	PB6/SI1
53	xDMUTE	O	Double speed digital output control output terminal Digital output prohibition with "L".	PB7/SO1
54	FSYNC	I	Frame sync signal input Connected to the FSYNC terminal (pin 94) of the signal processing LSI IC 501 (HD49226AFS). A pulse signal with a duty of 50 (%) and a period of 30 (ms) at the time of SP mode, 60 (ms) at the time of LP mode, and 15 (ms) at the time of WSP mode.	PE0/$\overline{EC0}$
55	POFF	I	Power OFF signal input terminal This drops from "H" to "L" at the time of power OFF. The drop is monitored by timer interrupt processing every 1.95 (ms), and the power OFF routine is started.	PE1/$\overline{EC1}$
56	OPACK	I	Input terminal for communication permission from the operation control The system control starts communication with the operation control at the edge of OPACK. Reversion is made after completion of each byte of communication.	PE2/RMC
57	xTEST	I	Test mode input terminal Test mode with "L".	PE3/$\overline{NMI}$
58	PADJ	O	TACH adjustment voltage output terminal Used as PWM output terminal.	PE4/$\overline{PWM}$
59	xEMP	O	De-emphasis control output terminal De-emphasis ON with "L".	PE5/T0
60	NC	O	Not used terminal	PI0/INT0
61	CFG	I	Capstan FG input terminal The rise edge is monitored by timer interrupt processing every 1.95 (ms), and this is used to check for capstan emergencies.	PI1/INT1
62	HSWP	I	Head switching pulse input terminal Used as interrupt terminal (INT2).	PI2/INT2
63	FGT	I	Take-up side reel FG input terminal Used as interrupt terminal (INT3).	PI3/INT3
64	LDMON	O	Cassette compartment loading motor control output terminal ON/OFF control for the cassette compartment loading motor. Loading motor ON with "H".	PI4
65	MLMCW	O	Mode motor, cassette compartment loading motor rotation direction control output terminal Control of the rotation direction for the mode motor of the D_4 mechanism and the cassette compartment loading motor. Rotation in clockwise direction at the time of "H".	PI5
66	MDMON	O	Mode motor control output terminal ON/OFF control for the mode motor of the D_4 mechanism. Mode motor ON with "H".	PI6
67	LDSTART	I	Cassette compartment loading start detection switch input terminal Loading start with "H".	PI7
68	xLDEND	I	Cassette compartment loading end detection switch input terminal Loading completion with "L".	PG0
69	TLED	O	Tape top/end sensor LED control output terminal ON/OFF control for the tape top/end sensor LED of the D_4 mechanism. Flashing at the period of 3.9 (ms).	PG1

No.	Name	I/O	Description	CPU Name
70	SOLON	O	Brake solenoid control output terminal ON/OFF control for the brake solenoid of the D_4 mechanism. Brake ON with "H".	PG2
71	xDMON	O	Drum motor control output terminal ON/OFF control for the drum motor of the D_4 mechanism. Drum motor ON with "L".	PG3
72	VDD	–	Positive power supply terminal Connected to the 5 (V) line.	VDD
73	NC	O	Not used terminal	NC
74	xCMON	O	Capstan motor control output terminal ON/OFF control for the capstan motor of the D_4 mechanism. Capstan motor ON with "L".	PG4
75	CMCW	O	Capstan motor rotation direction control output terminal Rotation direction control for the capstan motor of the D_4 mechanism. Clockwise (forward) rotation with "H".	PG5
76	THIN	I	Thin tape (9 μ m) detection switch input terminal Connected to the tape thickness recognition hole detection switch of the D_4 mechanism. Becomes "H" at the time of thick tape (hole open).	PG6
77	RECINH	I	Recording prohibition recognition hole detection switch input terminal Recording prohibition with "H".	PG7
78	xHALFIN	I	Cassette half detection switch input terminal Cassette half present with "L".	PF0
79	ENC1	I	Mechanism encoder output BIT1 input terminal	PF1
80	ENC2	I	Mechanism encoder output BIT2 input terminal	PF2

■ PDG153A9 (IC3401: INTERFACE UNIT)

● Mode Controller IC

● Pin Function

No.	Name	I/O	Description	CPU Name
1			————	PE3/INT3
2	RMSIG	I	Remote control signal input terminal Used as RMC terminal.	PE4/RMC
3			Connected to GND.	PE5
4			————	PE6
5	S1	O	TC9246F (IC 3404) control serial data output terminal	PE7/TO
6	S2	O	TC9246F (IC 3404) control serial clock output terminal	PB0/CINT
7	M1	O	TC9246F (IC 3404) clear signal output terminal	PB1/CSO
8	CCK	I	Serial data transfer clock input terminal Used as SC terminal. Connected to the shift clock output terminal of the system control. The serial clock period is 1.9 (μ s), and the interval clock period is 30.5 (μ s).	PB2/SCK0
9	CDATAI	I	Serial data input terminal Used as SI terminal. Connected to the serial data output terminal of the system control.	PB3/SI0
10	CDATAO	O	Serial data output terminal Used as SO terminal. Connected to the serial data input terminal of the system control.	PB4/SO0
11	CL	O	PDC019A (IC3402) control serial clock output terminal	PB5/SCK1
12			————	PB6/SI1
13	DI	O	PDC019A (IC3402) control serial data output terminal	PB7/SO1
14	KS0	I	Key scan data input terminal 0	PC0/KR0
15	KS1	I	Key scan data input terminal 1	PC1/KR1
16	KS2	I	Key scan data input terminal 2	PC2/KR2
17	DOWN. C	I	Down-conversion ON/OFF selection switch input terminal H = Down-conversion OFF L = Down-conversion ON	PC3/KR3
18	TEST	I	Test terminal	PC4/KR4
19			————	PC5/KR5
20	WIRELESS	I	Wireless remote control prohibition selection switch input terminal H = Wireless remote control operation possible L = Wireless remote control operation not possible	PC6/KR6
21	OUT LEVEL	I	Output level selection switch input terminal H = +4 dBV L = −10 dBV	PC7/KR7
22	INPUT	I	Recording input switching switch position input terminal Used as AN0 (analog input). Set to COAX input with 0 to 0.8 (V), AES/EBU input with 0.8 to 2.0 (V), analog input with 2.0 to 3.75 (V), and to intermediate position with 3.75 to 5 (V). [The respective voltages are the standard values at the time of VDD 5 (V).]	PA0/AN0
23	COPYFLG	I	COPY-ID setting switch position input terminal Used as AN1 (analog input). Set to PROH (prohibition) with 0 to 1.25 (V), PERMIT (permission) with 1.25 to 3.75 (V), and ONCE (permission only once) with 3.75 to 5 (V). [The respective voltages are the standard values at the time of VDD 5 (V).]	PA1/AN1

No.	Name	I/O	Description	CPU Name
24	FSSELECT	I	Recording mode switching switch position input terminal Used as AN2 (analog input). Set to 88 kHz with 0 to 0.5 (V), 96kHz with 0.5 to1.3 (V), 48 kHz with 1.3 to 2.5 (V), X2 copy with 2.5 to 3.65 (V), 44 kHz with 3.65 to 4.5 (V), and intermediate position with 4.5 to 5 (V). [The respective voltages are the standard values at the time of VDD 5 (V).]	PA2/AN2
25	WIRED	I	Wired remote control input terminal Used as AN3 (analog input). Becomes OFF with 0 to 1.25 (V), REC with 1.25 to 1.75 (V), MS+ with 1.75 to 2.25 (V), PAUSE with 2.25 to 2.75 (V), FF with 2.75 to 3.25 (V), REW with 3.25 to 3.75 (V), MS– with 3.75 to 4.25 (V), PLAY with 4.25 to 4.75 (V), and STOP with 4.75 to 5 (V). [The respective voltages are the standard values at the time of VDD 5 (V).]	PA3/AN3
26	F0	O	VCO control output terminal 0 H = Oscillation stop L = Oscillation	PA4/AN4
27	F1	O	VCO control output terminal 1 H = 24 MHz oscillation L = 22 MHz oscillation	PA5/AN5
28			————	PA6/AN6
29			————	PA7/AN7
30	xRST	I/O	System reset terminal "L" level active.	$\overline{\text{RST}}$
31	EXTAL	I	System clock oscillation ceramic oscillator connection terminal (input) An 8.38 (MHz) ceramic oscillator is connected between this pin and pin 32.	EXTAL
32	XTAL	O	System clock oscillation ceramic oscillator connection terminal (output)	XTAL
33	Vss	–	GND terminal Connected to GND.	Vss
34	XCOA	O	Digital input terminal switching output terminal H = AES/EBU input L = COAX input	PD0/S0
35	XDC	O	Down–conversion control output terminal H = Down–conversion OFF L = Down–conversion ON	PD1/S1
36	C6	O	CS8402A-CS(IC3406) control output terminal H = 48 kHz L = 44.1 kHz, 32 kHz	PD2/S2
37	C7	O	CS8402A-CS(IC3406) control output terminal H = 44.1 kHz L = 48 kHz, 32 kHz	PD3/S3
38	EM0	O	CS8402A-CS(IC3406) control output terminal H = Emphasis L = No emphasis	PD4/S4
39	EM1	O	CS8402A-CS(IC3406) control output terminal H = No emphasis L = Emphasis	PD5/S5
40	XDHS	O	Double speed interface control output terminal H = Normal speed L = Double speed	PD6/S6
41	DHS	O	Double speed interface control output terminal Pin 40 reversion output	PD7/S7
42			————	PF0/S8
43 | 49	S0 | S6	O	FL segment signal output terminal 0 | FL segment signal output terminal 6	PF1/S9 | PF7/S15

No.	Name	I/O	Description	CPU Name
50 | 54	S7 | S11	O	FL segment signal output terminal 7 | FL segment signal output terminal 11	S16 | S20
55 | 57	S12 | S14	O	FL segment signal output terminal 12 | FL segment signal output terminal 14	T15/S21 | T13/S23
58			————	T12/S24
59 | 62	T11 | T8	O	FL timing signal output terminal 11 | FL timing signal output terminal 8	T11/S25 | T8/S28
63 | 70	T7 | T0	O	FL timing signal output terminal 7 | FL timing signal output terminal 0	T7 | T0
71			————	VREF
72	VDD	–	Positive power supply terminal Connected to the 5 (V) line.	VDD
73	NC	–	Connected to the 5 (V) line.	NC
74	MCK	O	Shift clock output terminal for memory communication	PG0
75	MDA	I/O	Data I/O terminal for memory communication	PG1
76	CE	O	PDC019A (IC3402) control serial communication enable output terminal	PG2
77	OPACK	O	Output terminal for communication permission signal to the system control	PG3
78	xOPREQ	I	Input terminal for communication request signal from the system control Used as interrupt terminal (INT3).	$\overline{\text{PE0}}$/EC0/INT0
79			————	$\overline{\text{PE1}}$/EC1/INT1
80			————	PE2/INT2

■ PDG154B9 (IC3801: RS422 CONTROL UNIT)

● RS422 Micro-computer

● Pin Function

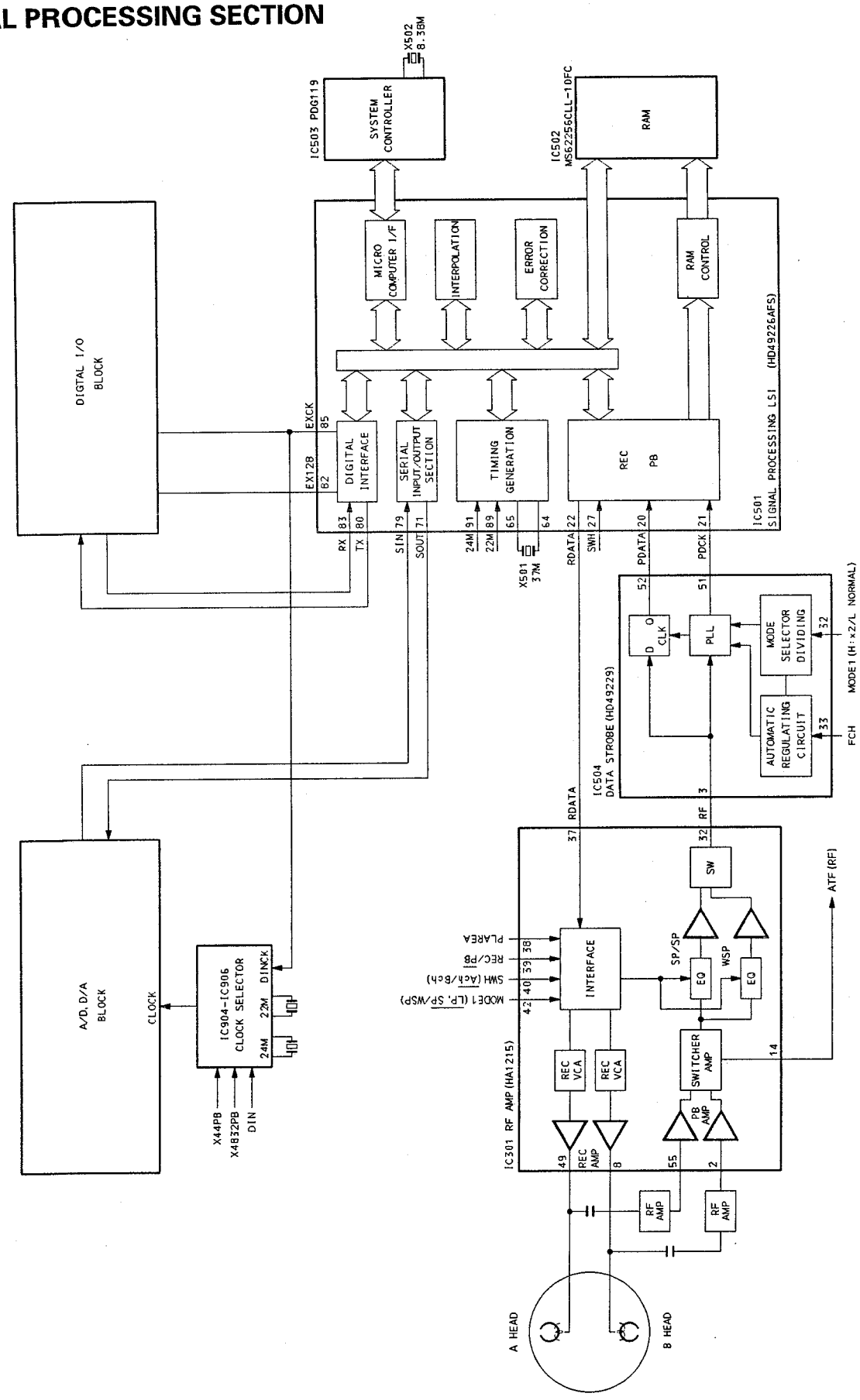
No.	Name	I/O	Description	CPU Name
1	——		——	PA1/A9
2	——		——	PA0/A8
3	——		——	PB7/A7
4	——		——	PB6/A6
5	——		——	PB5/A5
6	——		——	PB4/A4
7	——		——	PB3/A3
8	——		——	PB2/A2
9	——		——	PB1/A1
10	——		——	PB0/A0
11	TEST	I	Test terminal	PC7/D7
12	TEST	I	Test terminal	PC6/D6
13	INT/EXT	I	RS422 return line selection switch input terminal Selection of output of the return message of this unit or the return message of another connected unit. H = INTERNAL (this unit) L = EXTERNAL (other unit)	PC5/D5
14	SONY/ESBUS	I	RS422 protocol selection switch input terminal H = SONY protocol L = ES-bus	PC4/D4
15	MNUM4	I	Machine number selection switch input terminal 4	PC3/D3
16	MNUM3	I	Machine number selection switch input terminal 3	PC2/D2
17	MNUM2	I	Machine number selection switch input terminal 2	PC1/D1
18	MNUM1	I	Machine number selection switch input terminal 1	PC0/D0
19	——		——	PD7/$\overline{\text{HALT}}$
20	——		——	PD6/$\overline{\text{BRQ}}$
21	——		——	PD5/$\overline{\text{BAK}}$
22	——		——	PD4/$\overline{\text{SYNC}}$
23	——		——	PD3/C
24	——		——	PD2/$\overline{\text{EDS}}$
25	——		——	PD1/$\overline{\text{WR}}$
26	——		——	PD0/$\overline{\text{RD}}$
27	——		——	PH7
28	CDATAI	I	Serial data input terminal Used as SI terminal. Connected to the system control serial data output terminal.	PH6/SI

No.	Name	I/O	Description	CPU Name
29	CDATAO	O	Serial data output terminal Used as SO terminal. Connected to the system control serial data input terminal.	PH5/SO
30	CCK	I	Serial data transmission clock input terminal Used as SC terminal. Connected to the system control shift clock output terminal. The serial clock frequency is 1.9 (μ s), and the interval clock frequency is 30.5 (μ s).	PH4/SC
31		–	Connected to ground.	MP
32	xRST	I/O	System reset terminal "L" level active.	$\overline{\text{RST}}$
33	Vss	–	GND terminal Connected to ground.	Vss
34	XTAL	O	System clock oscillation ceramic oscillator connection terminal (output)	XTAL
35	EXTAL	I	System clock oscillation ceramic oscillator connection terminal (input) Connect a ceramic oscillator of 9.83 (MHz) between this pin and pin 34.	EXTAL
36	———		———	PH3/PWM1
37	———		———	PH2/PWM0
38	TXD	O	RS422 transmission terminal Transmission of a start–stop sync type serial bit signal (baud rate = 38.4 kb/s).	PH1/TXD
39	RXD	I	RS422 reception terminal Reception of a start–stop sync type serial bit signal (baud rate = 38.4 kb/s).	PH0/RXD
40	AVss	–	A/D converter GND terminal Connected to ground.	AVss
41	AVREF	–	A/D converter reference voltage input terminal Connected to the 5 (V) line.	AVREF
42	AVDD	–	A/D converter positive power supply terminal Connected to the 5 (V) line.	AVDD
43	———		———	PF7/AN7
44	———		———	PF6/AN6
45	———		———	PF5/AN5
46	———		———	PF4/AN4
47	———		———	PF3/AN3
48	———		———	PF2/AN2
49	———		———	PF1/AN1
50	———		———	PF0/AN0
51	———		———	PI3/CINT1/INT1
52	———		———	PI2/EC1
53	xRSREQ		Input terminal for communication request signal input from the system control Interrupt terminal	PI1/CINT0/INT0
54	———		———	PI0/$\overline{\text{EC0}}$
55	———		———	PG7
56	———		———	PG6

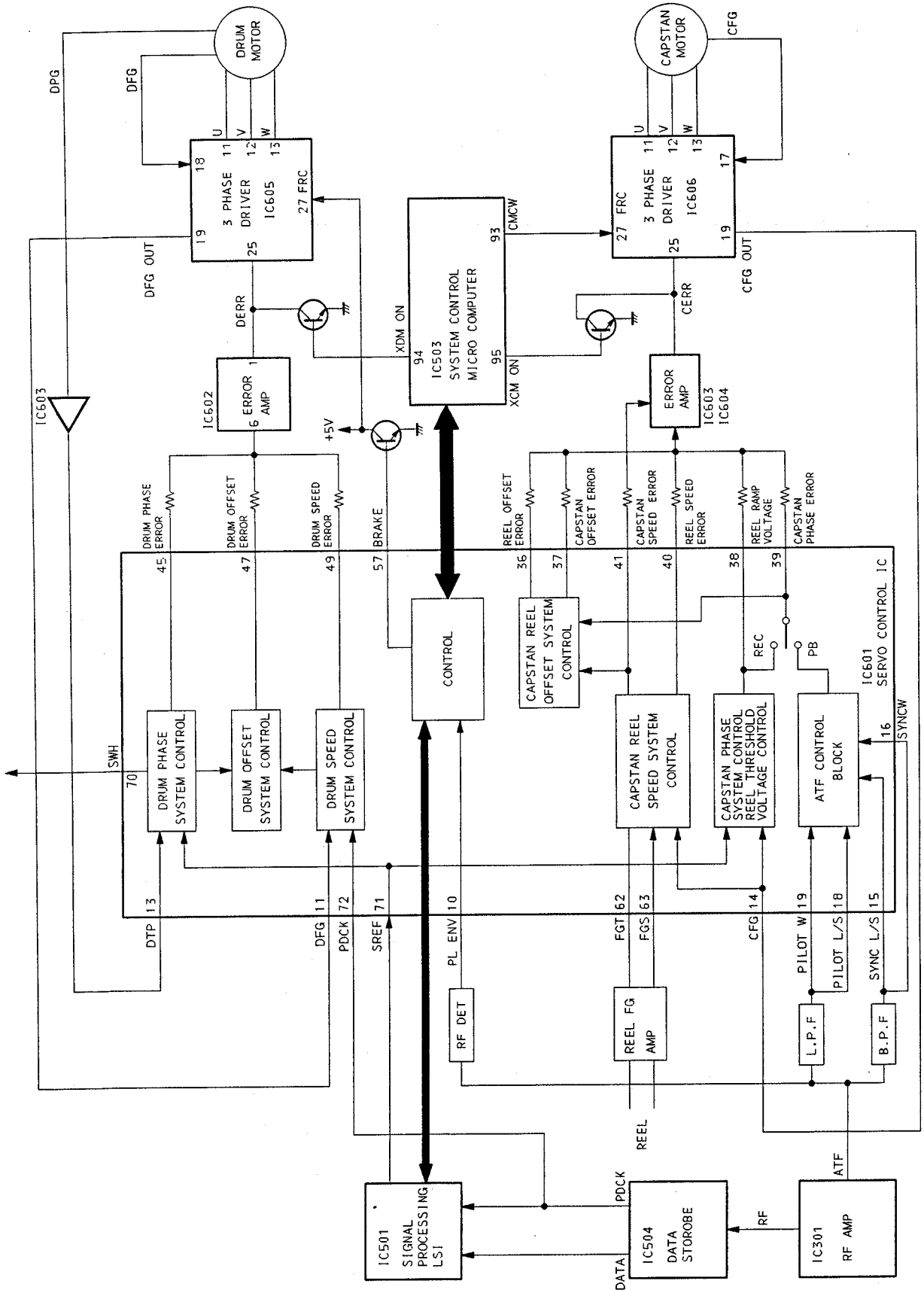
No.	Name	I/O	Description	CPU Name
57	———		———	PG5/TO1
58	———		———	PG4/TO0
59	———		———	PG3/EC3
60	SEL2	O	RS422 transmission circuit switching output terminal Fixed to "L".	PG2/EC2
61	SEL1	O	RS422 return line circuit switching output terminal H = EXTERNAL L = INTERNAL	PG1
62	RSACK	O	Output terminal for a communication permission signal to the system control	PG0
63	———		———	PE7/Yd
64	———		———	PE6/Yc
65	———		———	PE5/Yb
66	———		———	PE4/Ya
67	———		———	PE3/Xd
68	———		———	PE2/Xc
69	———		———	PE1/Xb
70	———		———	PE0/Xa
71	NMI	I	Connected to the 5 (V) line.	/NMI
72	VDD	–	Positive power supply terminal Connected to the 5 (V) line.	VDD
73	Vss	–	GND terminal Connected to ground.	Vss
74	NC	–	Connected to the 5 (V) line.	NC
75	———		———	PA7/A15
76	———		———	PA6/A14
77	———		———	PA5/A13
78	———		———	PA4/A12
79	———		———	PA3/A11
80	———		———	PA2/A10

11. BLOCK DIAGRAM

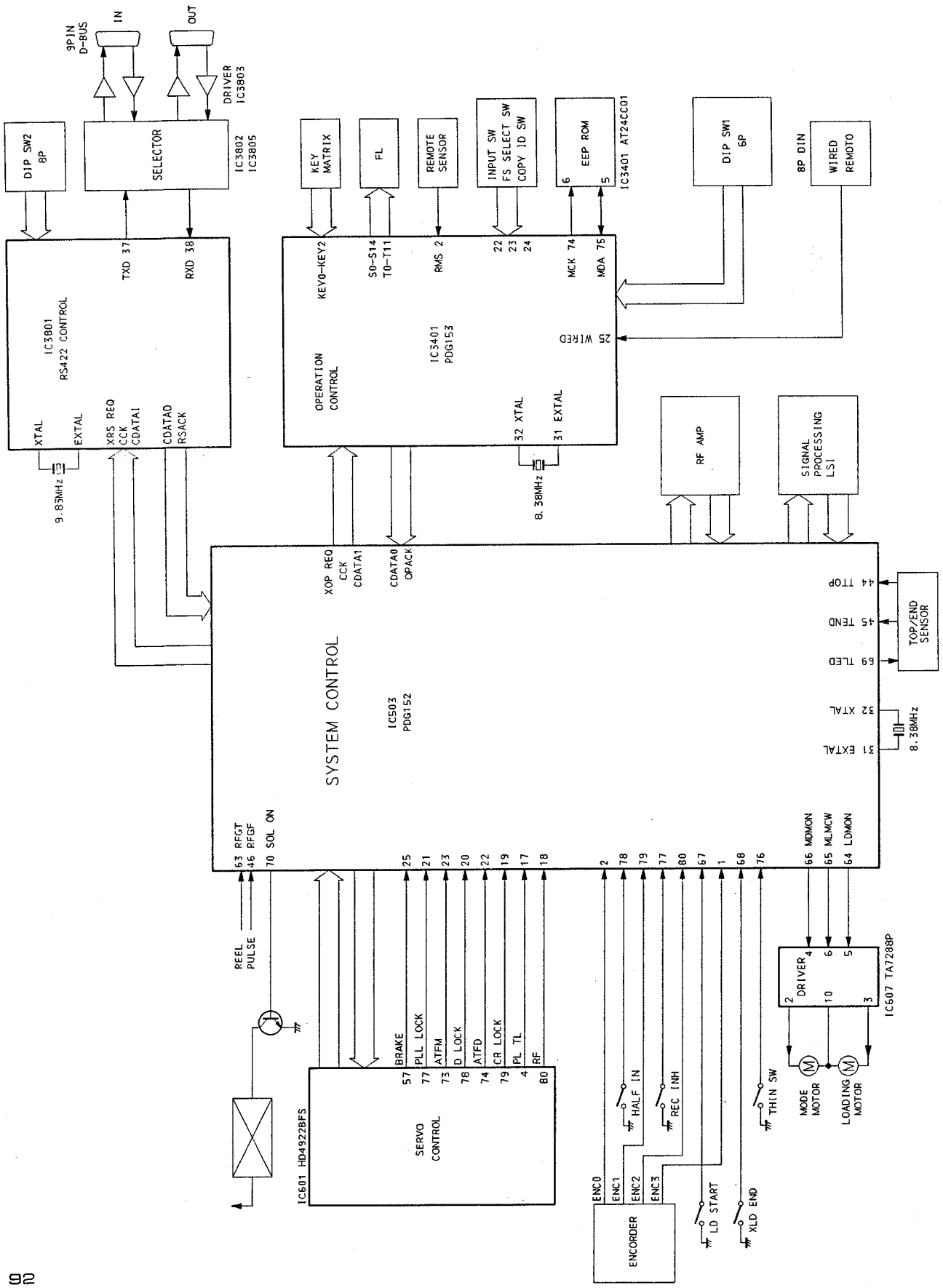
■ SIGNAL PROCESSING SECTION



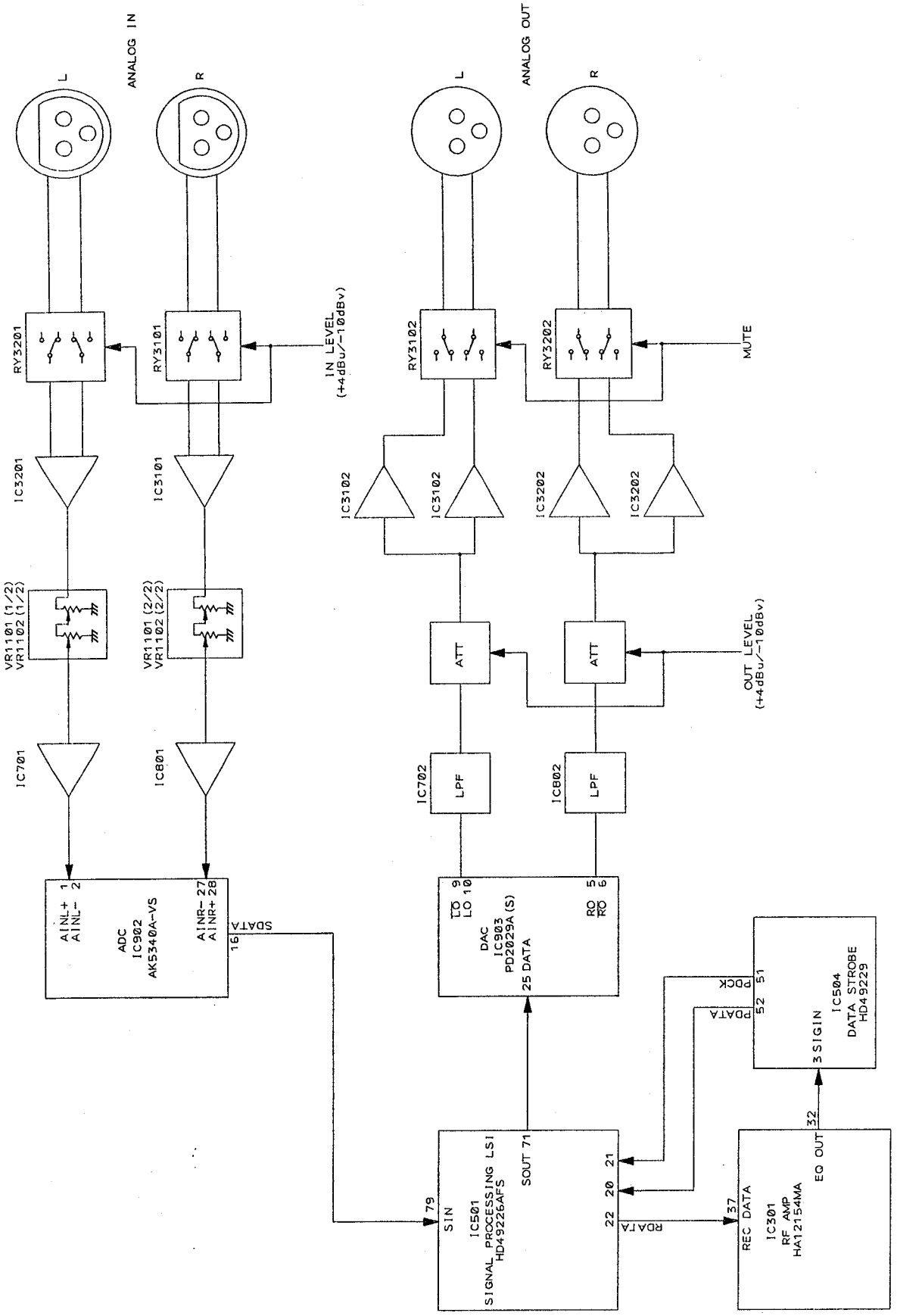
■ SERVO SECTION



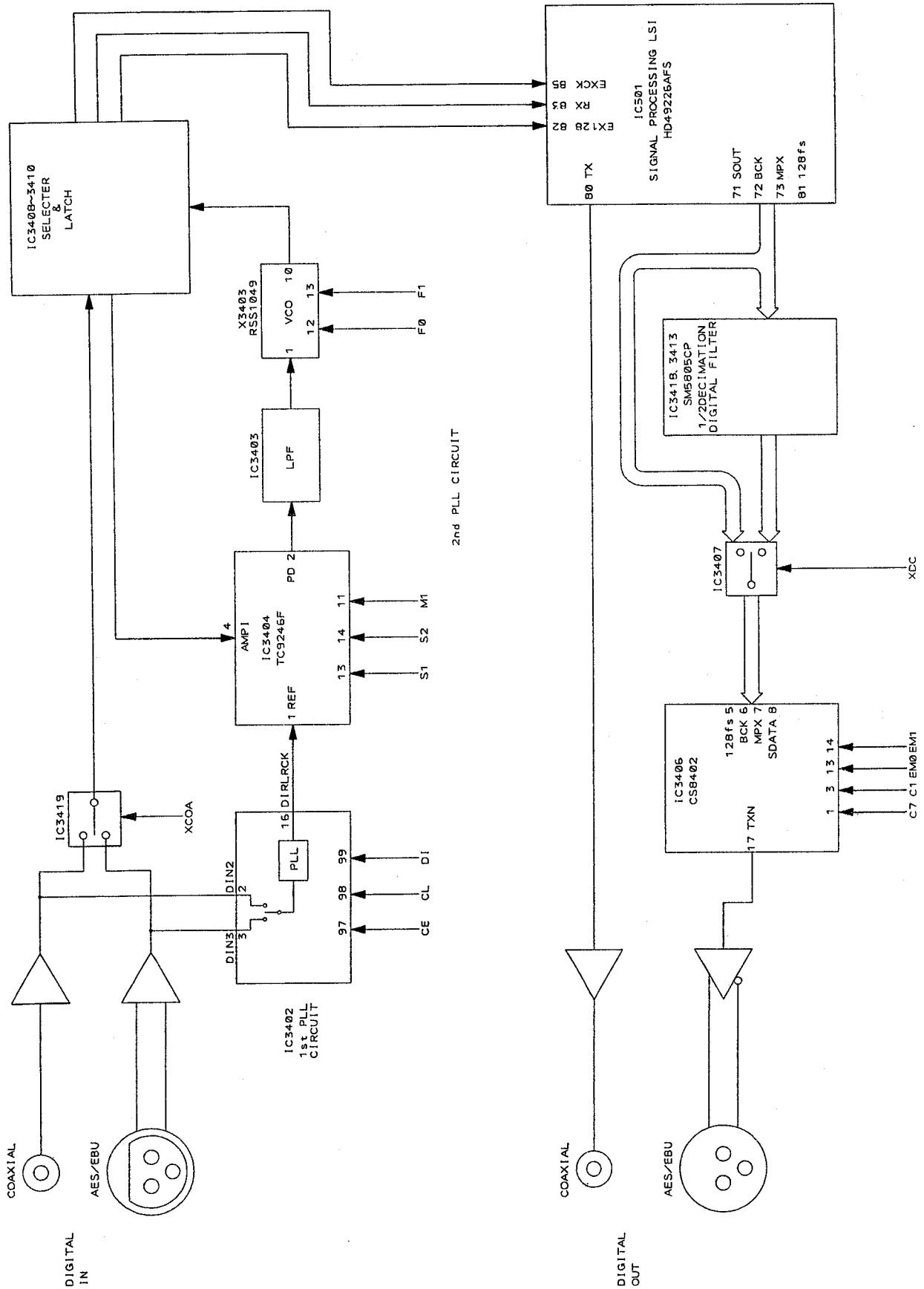
■ SYSTEM CONTROL SECTION



■ A/D, D/A SECTION

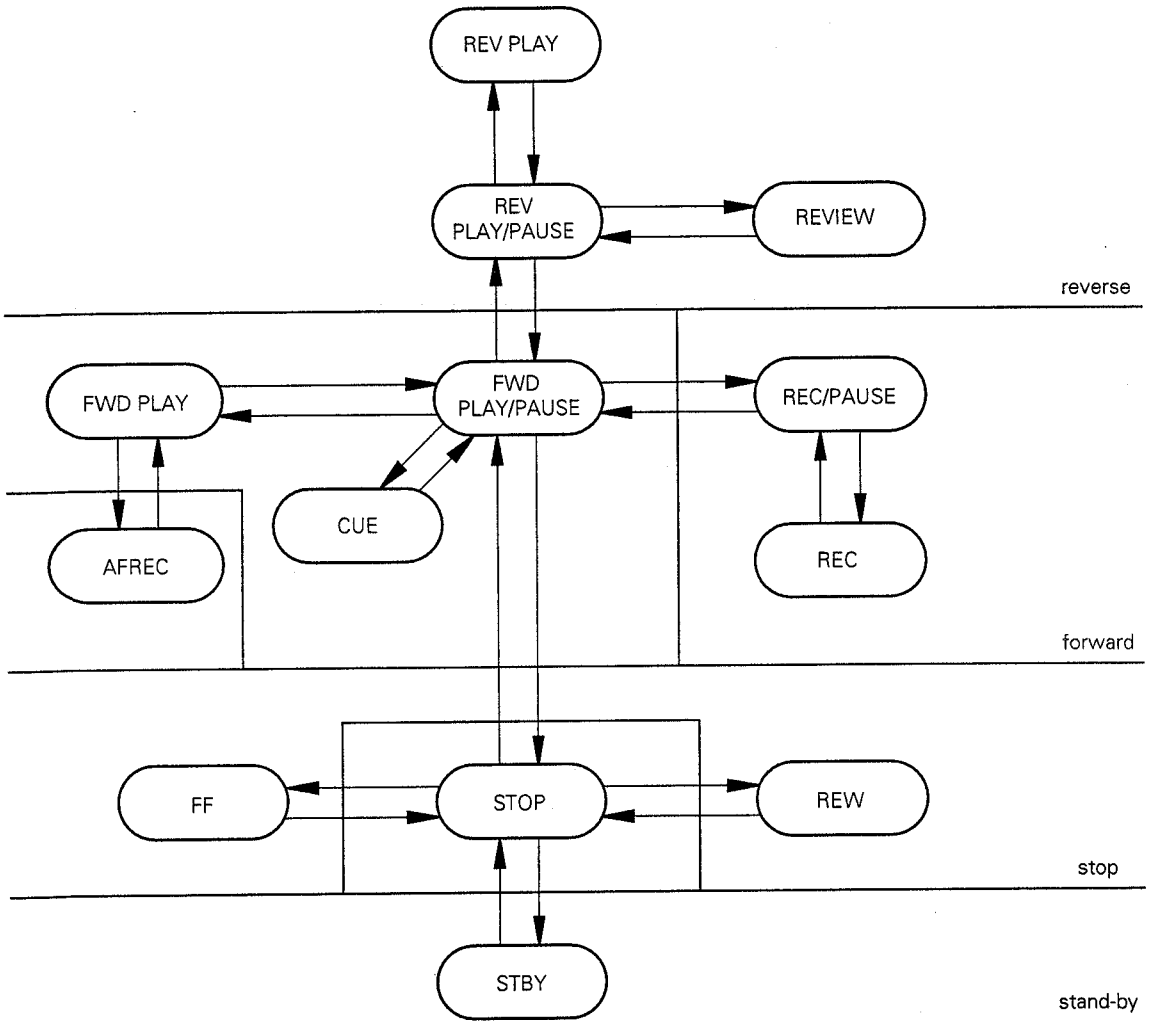


■ DIGITAL I/O SECTION



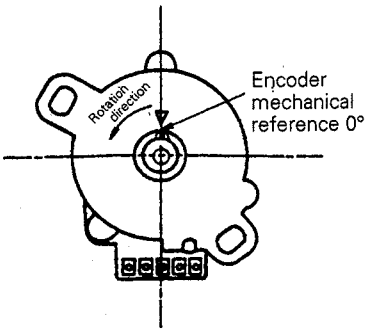
12. FLOW CHART

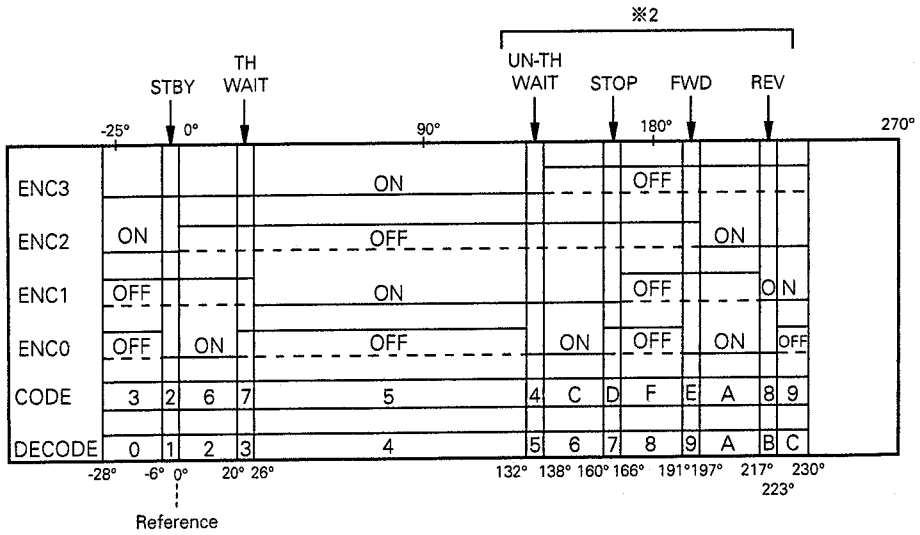
12.1 MECHANICAL MODE TRANSITION DIAGRAM



12.2 ENCODER PATTERN

● **STBY → TH WAIT (Threading Wait) → UN TH WAIT (Unthreading Wait) → STOP → FWD → REV**

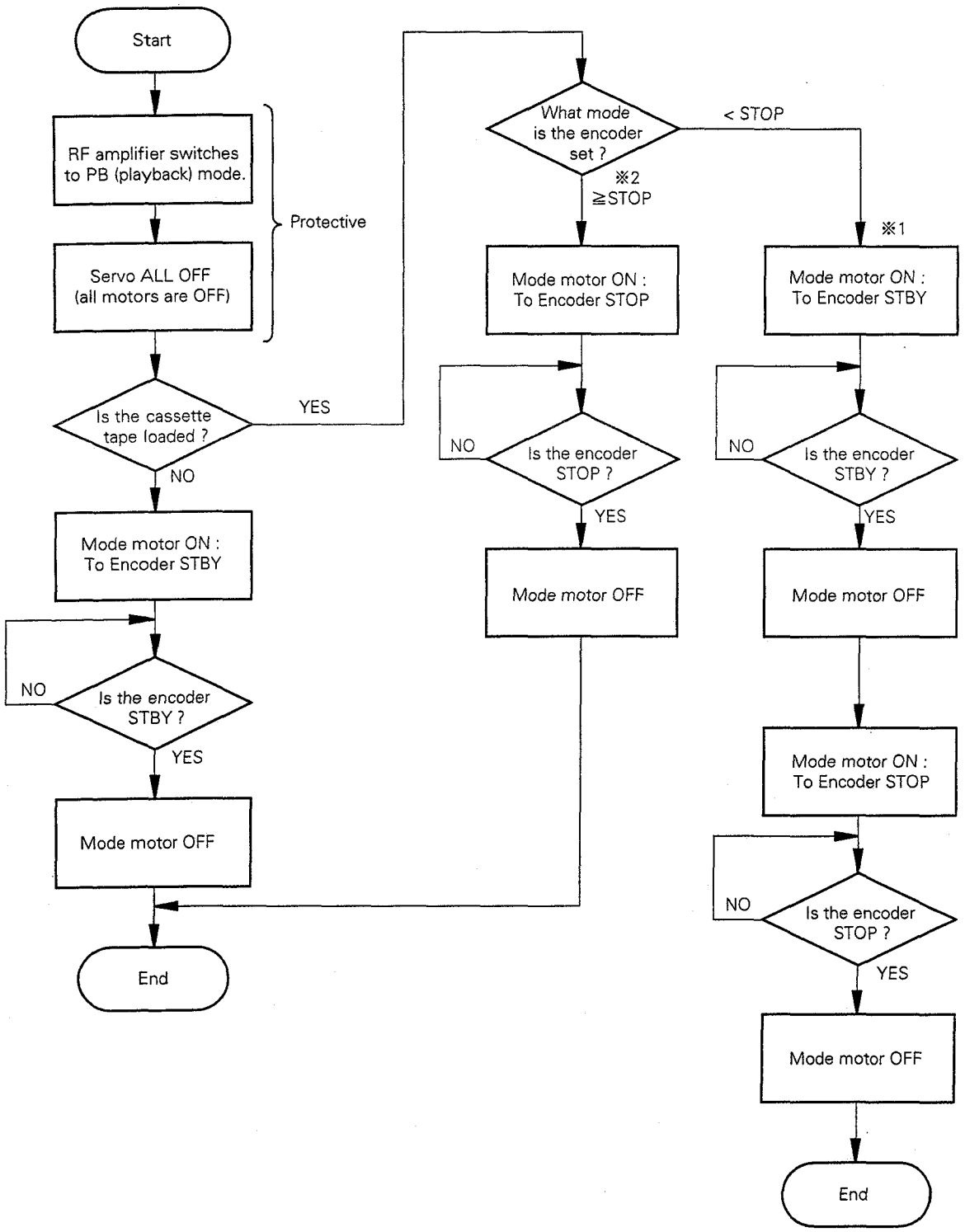




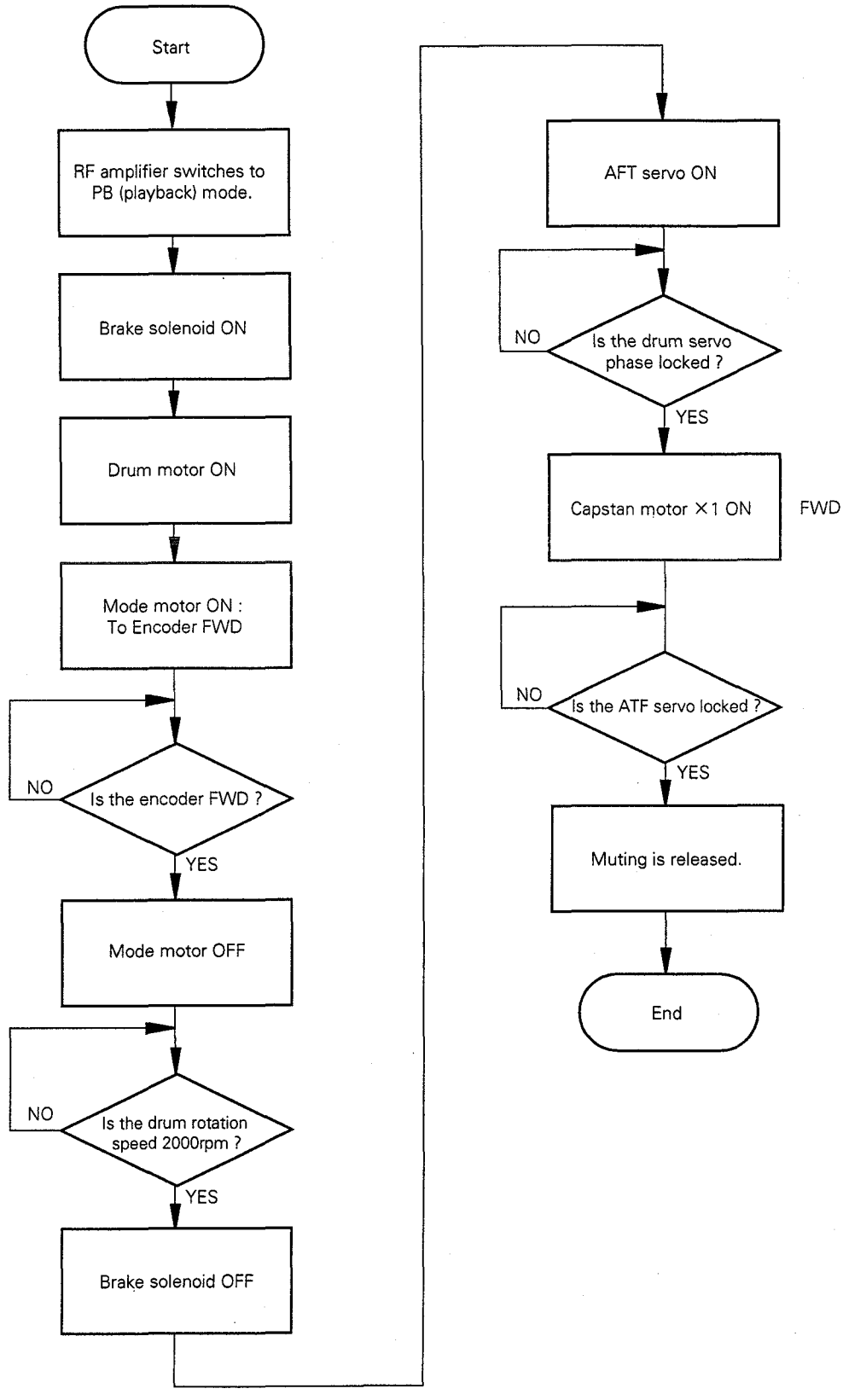
12.3 POWER ON

Cassette Tape Loaded → STOP
Cassette Tape Unloaded → STBY (standby, unthreading)

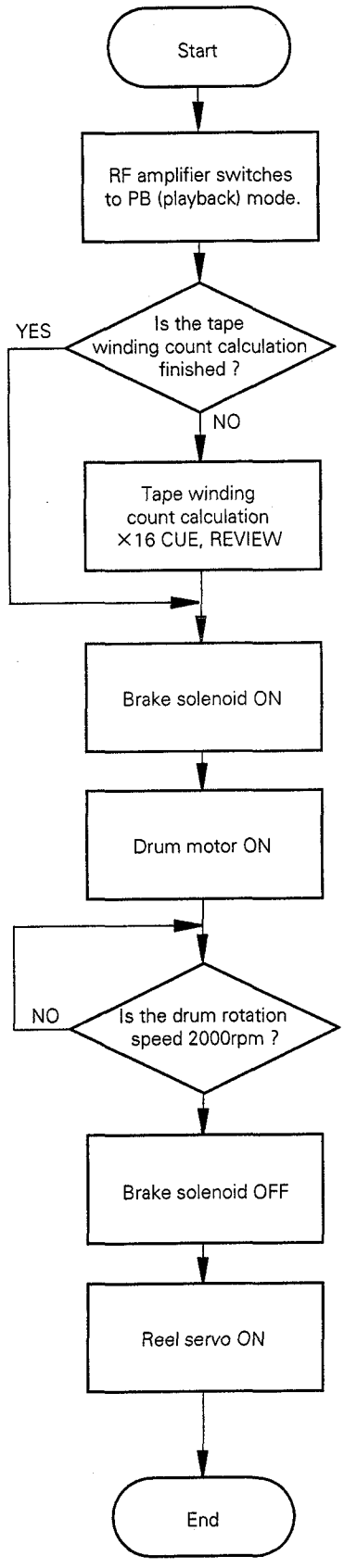
※1 Set the STBY mode, then STOP mode.
※2 ≧ STOP indicates the range of ※2 on page 95.



12.4 STOP → PLAY



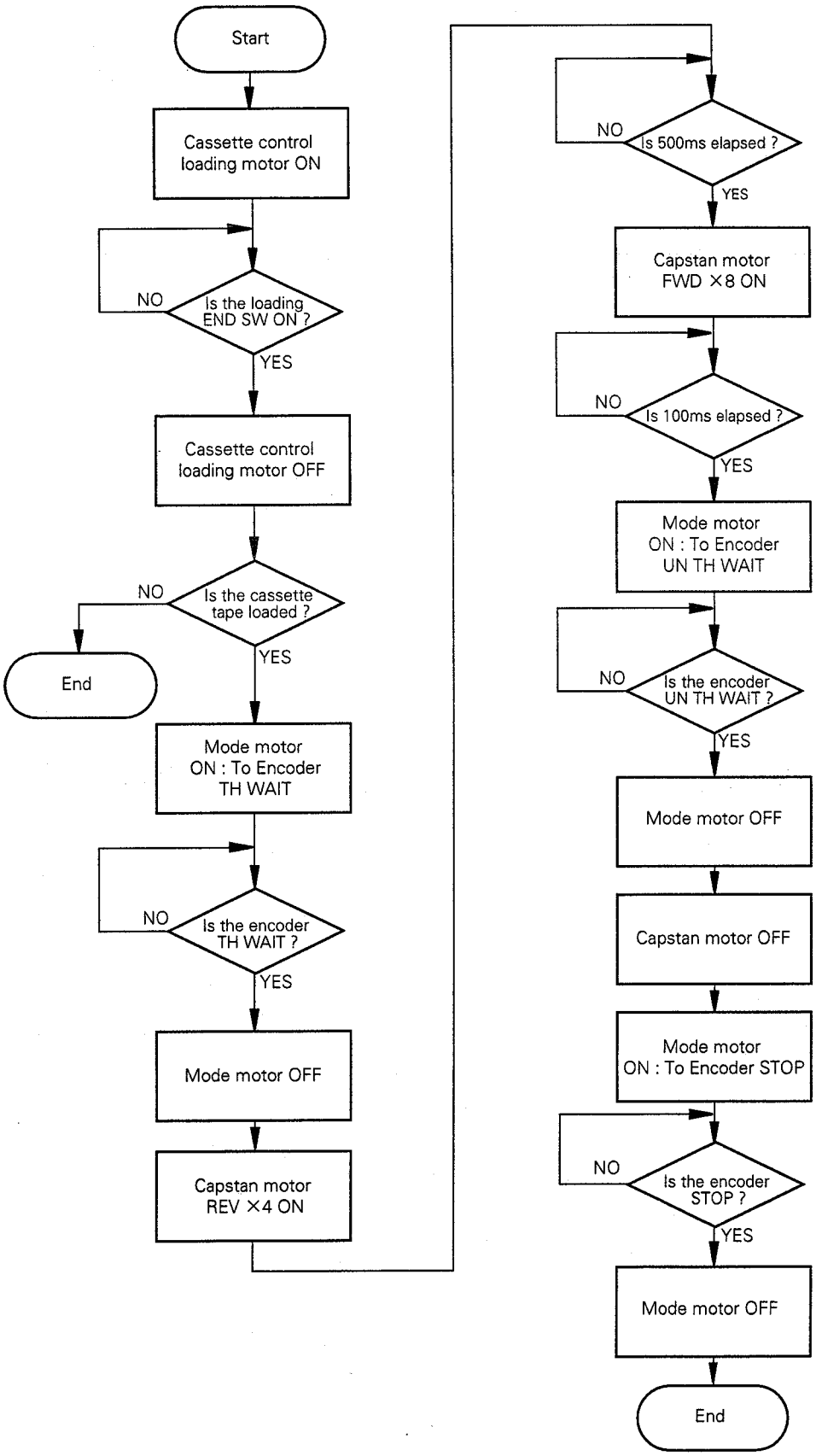
12.5 STOP → FF, REW



STOP
↓
CUE, REVIEW
↓
STOP and Mechanical mode transition

The encoder position remains at STOP.

12.6 OPEN → CLOSE → STOP



13. DAT CASSETTE TAPE OPERATION DESCRIPTION

When the cassette tape placed on the tray is slid into the main body, the protrusion at portion Ⓐ on the plate contacts portion Ⓑ of the tape. As shown in Fig. 13–1, the claw of portion Ⓑ is pushed up while the tape passes the protrusion on the plate. The protrusion on the plate then contacts the notch of the slider, and the slider gradually opens as shown in Fig. 13–1 as the tape enters the main body. At this point, when the claw of the tape moves down into the Hall in portion Ⓒ of the slider, the slider is retained open. Then, when the container moves down to mount the tape, the tape lid contacts the sensor bracket of the mechanical unit, pushing the lid up. At this time, portion Ⓓ of the lid contacts portion Ⓔ of the brake lever to remove the brake lever from the reel, so that the tape will be free.

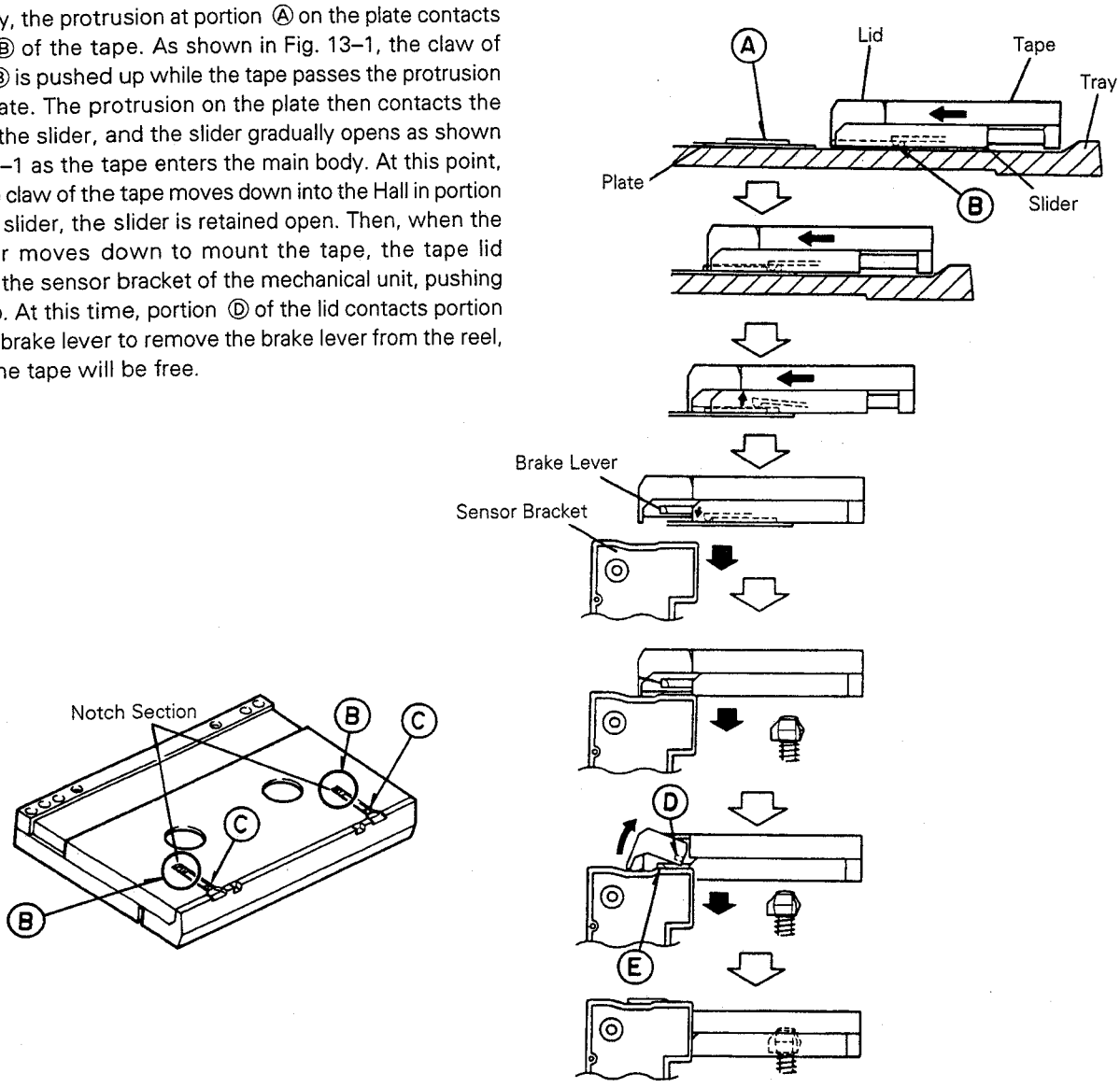


Fig. 13–1 Tape Motion

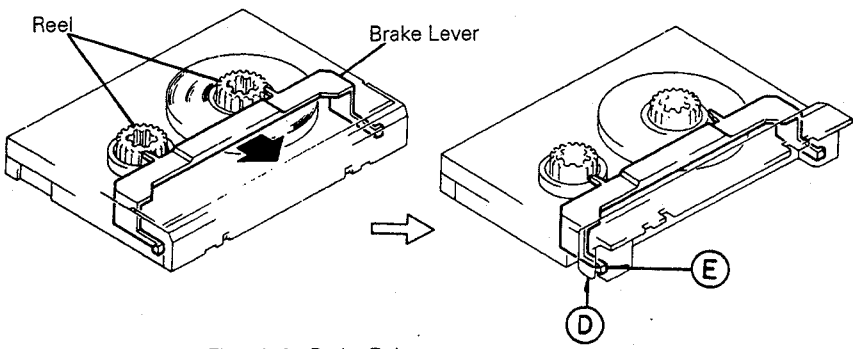


Fig. 13–2 Brake Release

14. DAT MECHANICAL UNIT OPERATION DESCRIPTION

14.1 OUTLINE OF MECHANICAL SECTION

The mechanical section of this machine consists of driving DD motors each for the drum and the capstan, mode switch DC motor, plunger for reel brake ON/OFF. The mechanical status is detected by a 4-bit rotary encoder to control the mode change motor. (Fig. 14-1)

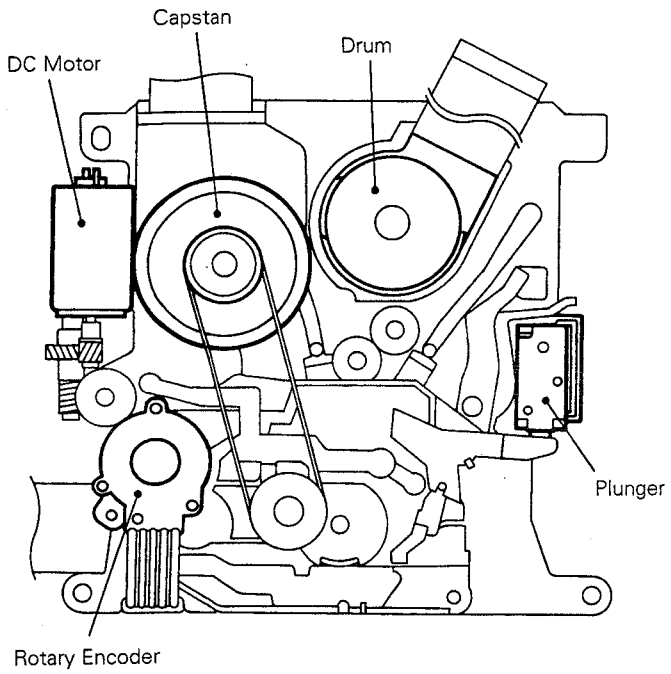


Fig. 14-1

14.2 BASIC MECHANICAL UNIT MODE

The mechanical unit uses the following four basic modes:

① Unthreading mode (Fig. 14-2)
② STOP mode (Fig. 14-3)
③ PLAY mode (Fig. 14-4)
④ FF/REW mode (Fig. 14-3)

[Although the mechanical operating state is the same as in the STOP mode, the reel is rotated by the capstan motor during brake OFF (plunger OFF) in the FF/REW mode.]

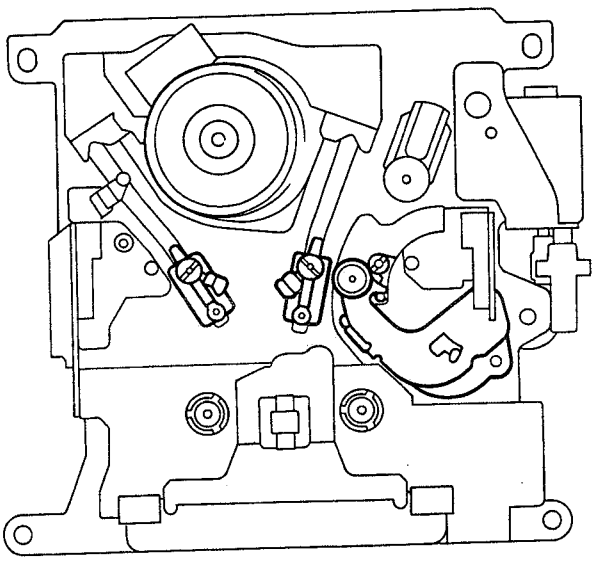


Fig. 14-2 Unthreading Mode

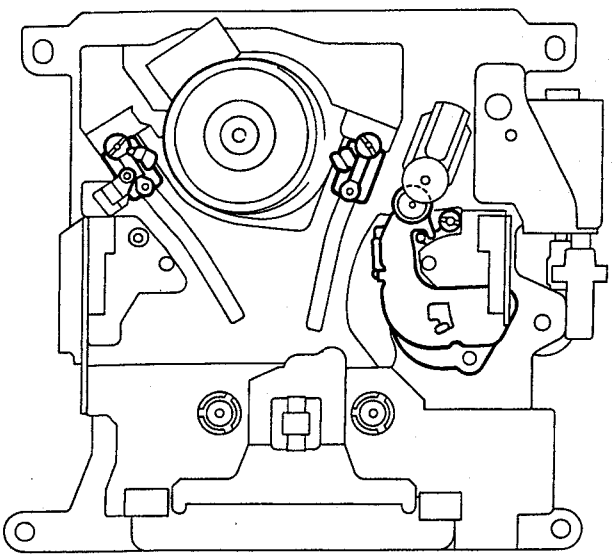


Fig. 14-3 STOP or FF/REW Mode

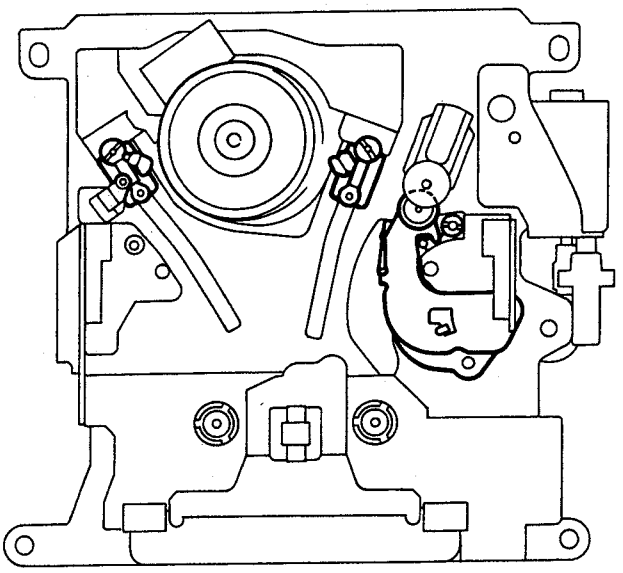


Fig. 14-4 PLAY Mode

14.3 MODE CHANGE

The mechanical mode is changed as follows. The driving power transmission path of the power motor assembly (mode change motor) is shown in Fig. 14–5.

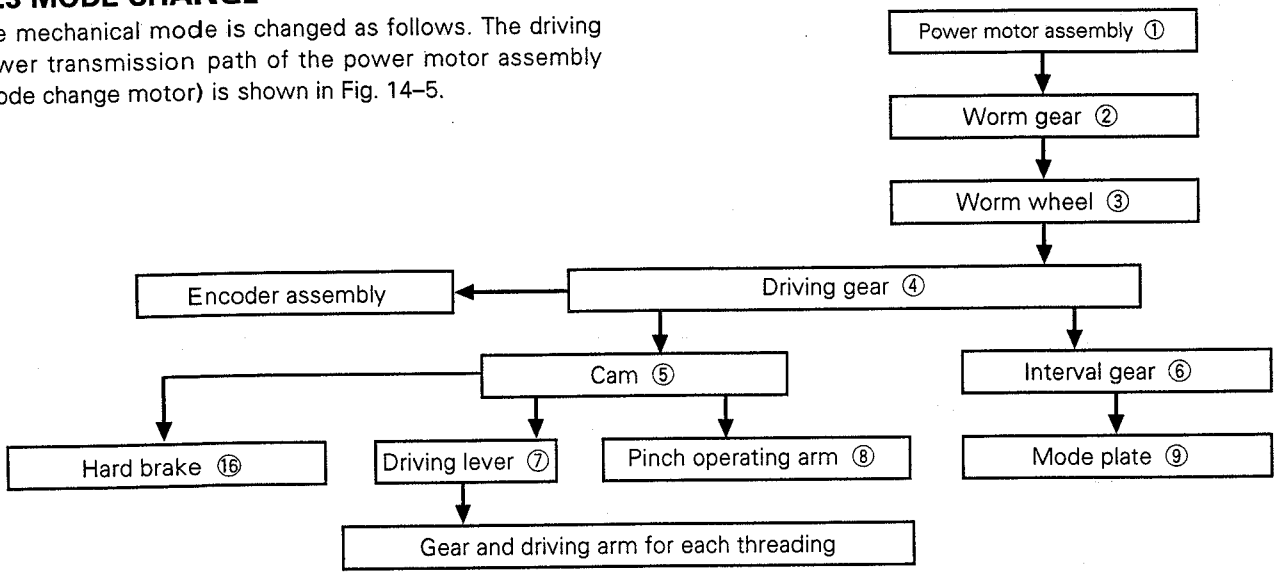
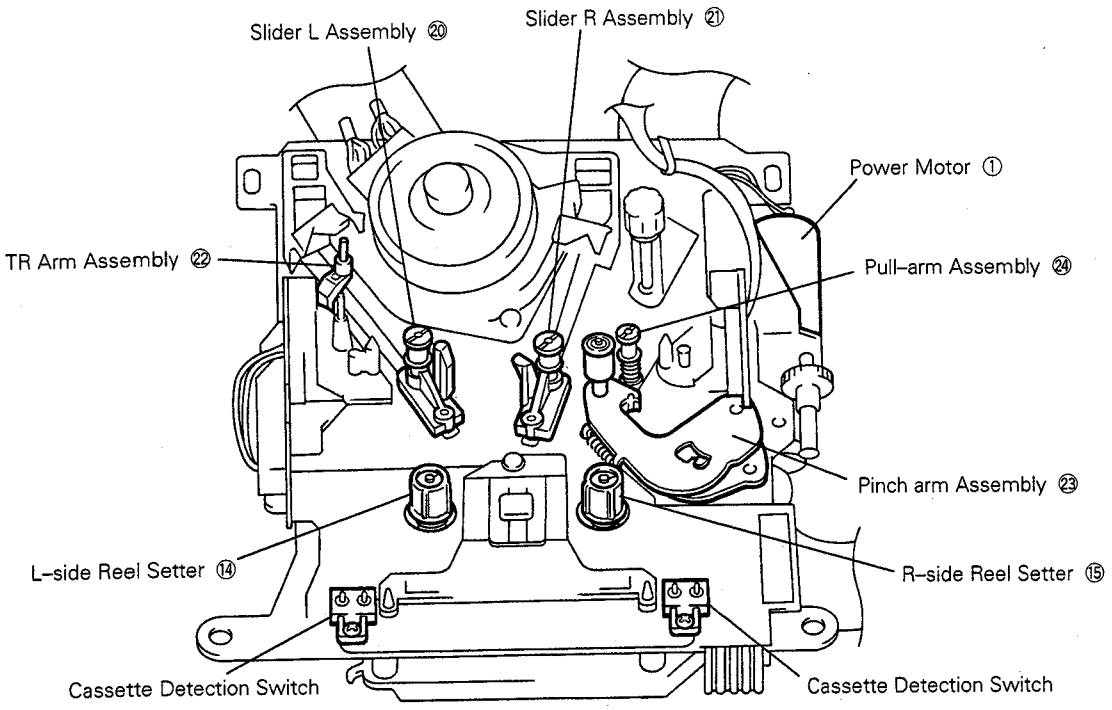


Fig. 14–5 Power Transmission Path Block Diagram

14.3.1 Unthreading Mode → STOP Mode (threading mode)

1. In the unthreading mode, the mechanical section is in the state shown in Fig. 14–6, in which the slider L assembly ⑳, R assembly ㉑, pinch arm assembly ㉓, and pull–arm assembly ㉔ are located on the front side.
2. When the cassette tape is loaded, the cassette detection switch is turned ON. Then, power motor ① starts rotating, and hard brake ⑯ fixes R–side reel setter ⑮. (See Fig. 14–9.)



NOTE: View from the top : hereinafter indicated Top

Fig. 14–6 Unthreading Mode

3. Power motor ① rotates counterclockwise as shown in Fig. 14–7. The power is transmitted to worm gear ②, worm wheel ③, and driving gear ④ under the reel base assembly in that order.

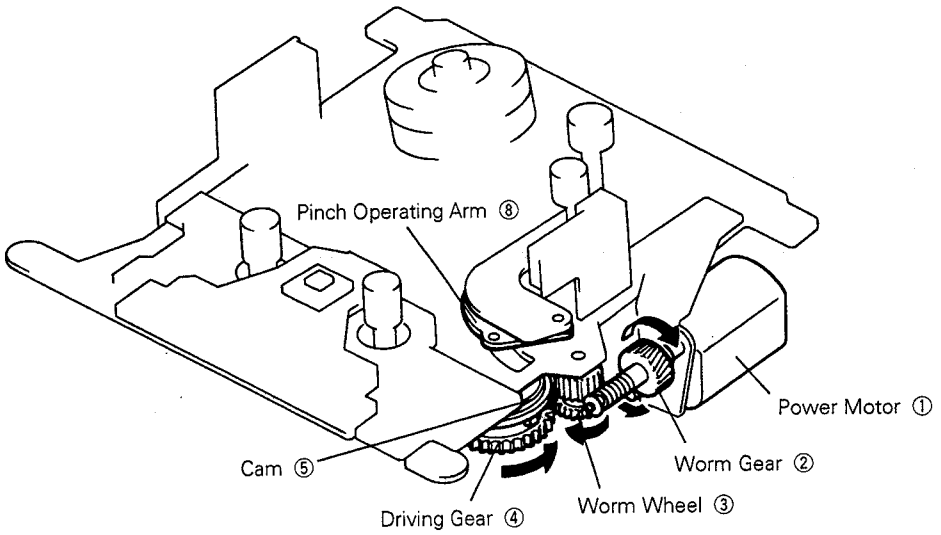
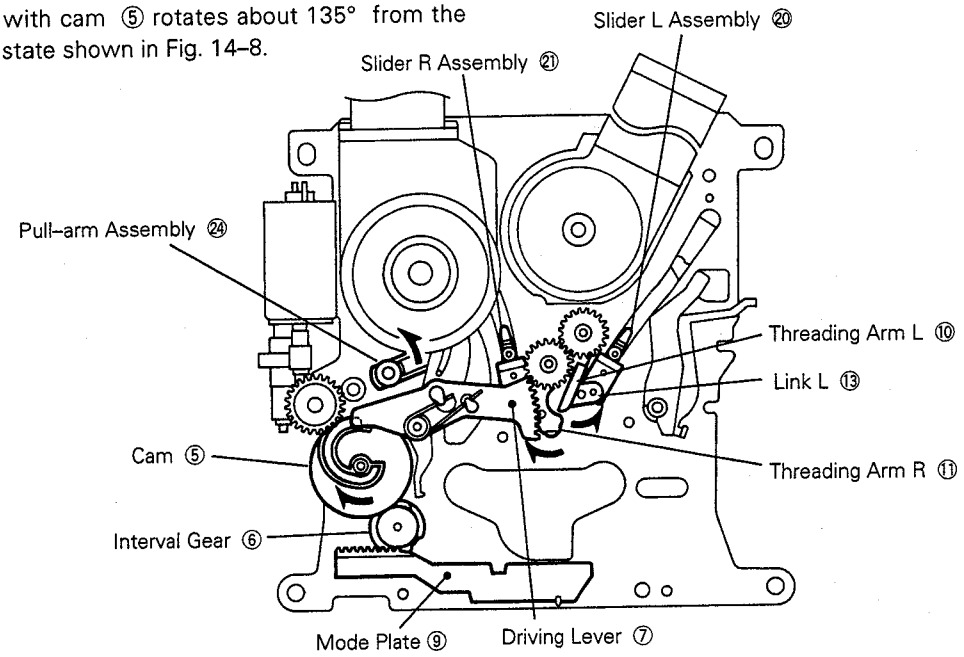


Fig. 14–7 (Top)

4. In the this power transmission method, driving gear ④ rotates in the direction indicated by the arrow shown in Fig. 14–7. (See Fig. 14–8 for the following.) Cam ⑤ rotating synchronously with driving gear ④ is directly connected to the upper side of driving gear ④ and also rotates in the arrow direction. The driving power of driving gear ④ is output to two systems of interval gear ⑥ and cam ⑤. Interval gear ⑥ performs the intermittent operation and is stopped until the STOP mode is set. Driving lever ⑦ interlocking with cam ⑤ rotates about 135° from the unthreading state shown in Fig. 14–8.

According to this motion, the power is transmitted to the arm driving gears. Pull–arm assembly ㉔ and threading arm L ⑩ rotate counterclockwise and threading arm R ⑪ rotates clockwise to start threading. Threading arm L ⑩ and slider L assembly ⑳ are linked via link L ⑭; the rotational power of threading arm L ⑩ generates the linear motion of slider L assembly ⑳. Threading arm R ⑪ also produces the same results.



NOTE: View from the bottom side: hereinafter indicated Bottom

Fig. 14–8

5. As threading arm L ⑩ and R ⑪ rotate, both slider L assembly ⑳ and R assembly ㉑ move along the groove of the mechanical chassis. As pull-arm assembly ㉔ rotates, pinch arm assembly ㉓ is pulled and starts rotating (see Figs. 14–10 and 14–11). (At this time the tape is extracted from L-side reel setter ⑭ by sliders L ⑳, R ㉑, and pull-arm assembly ㉔.)

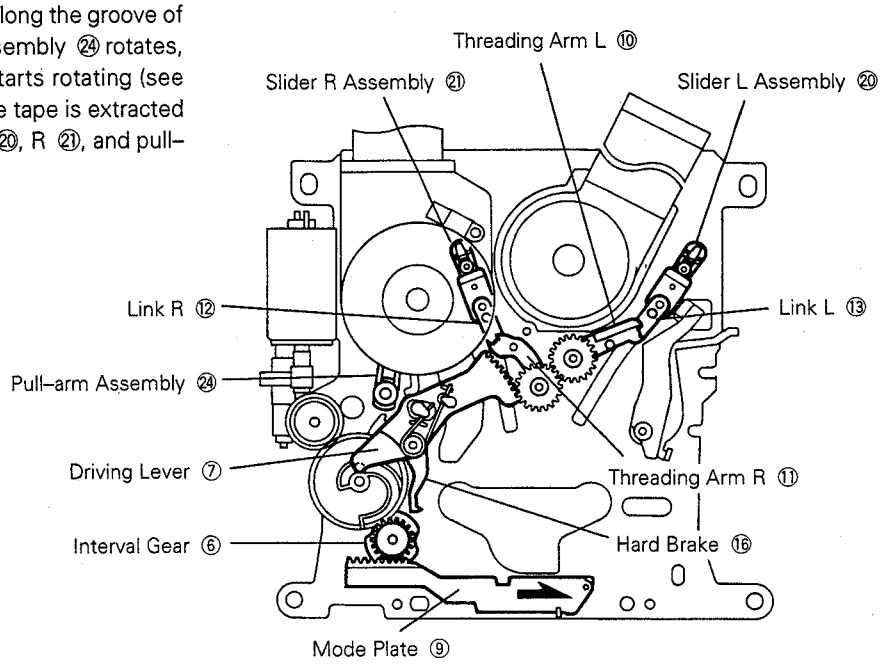


Fig. 14–9 (Bottom)

6. As driving gear ④ rotates, sliders L ⑳ and R ㉑ are press-fit into the groove of drum base ㉕; pull-arm assembly ㉔ is press-fit into sensor bracket R ㉖. At this time, if sliders L ⑳, R ㉑, and pull-arm assembly ㉔ stop, driving gear ④ continues rotating because it provides the specified press-fit force by the force of the spring in each gear.

Then, hard brake ⑯ stopping R-side reel setter ⑮ goes OFF to rotate the drum, completing the threading operation.

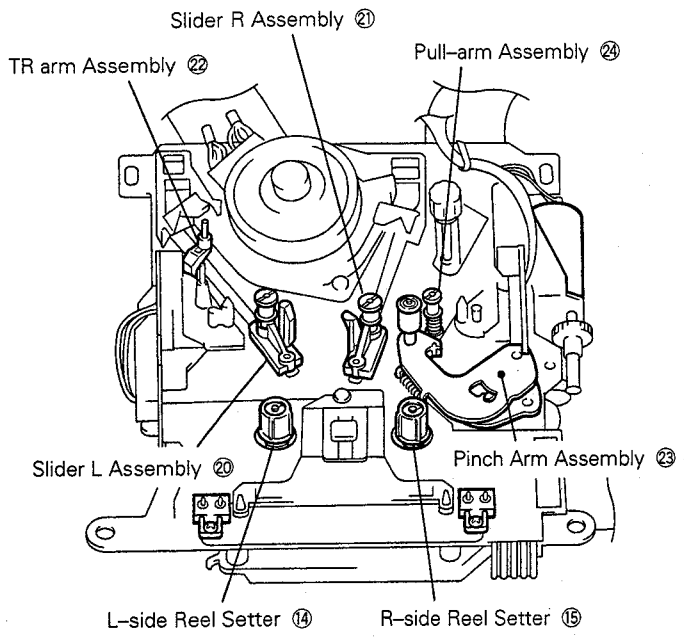


Fig. 14–10 Unthreading State (Top)

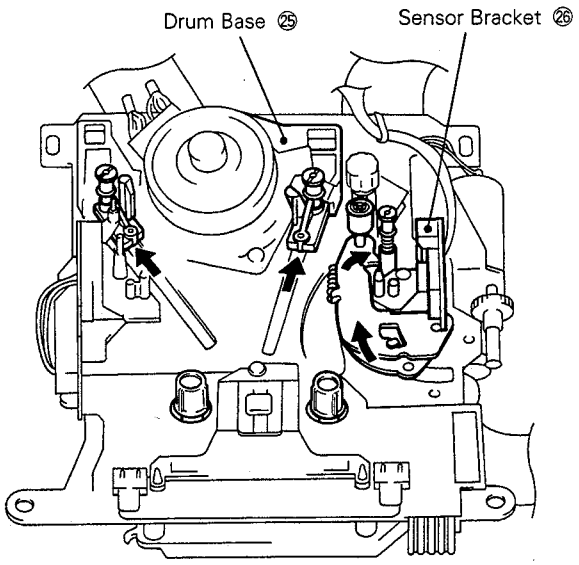


Fig. 14–11 STOP State (Top)

14.3.2 STOP, PLAY, REV, FF–REW Operations

1. When the STOP state shown in Fig. 14–11 is set, the gear mode is as shown in Fig. 14–9. At this time, driving lever ⑦ is stopped and interval gear ⑥ can be rotated. Rotation of interval gear 6 moves mode plate ⑨ to the left and right. This motion of mode plate ⑨ determines the mode. Rotation of driving gear ④ causes interval gear ⑥ to rotate so that mode plate ⑨ will move to the left side viewed from the top, in Fig. 14–12. The motion of mode plate ⑨ is classified into four points as shown in Fig. 14–12 viewed from the bottom. As mode plate ⑨ moves, clutch drum ⑲ shown in Fig. 14–13 moves up and down to rotate REV brake ⑰ and TR lever ⑱ (Fig. 14–14).

However, for the pinch roller press–fit, the power is transmitted by cam ⑤ coaxial and synchronous with driving gear ④ from the bottom side to the top side of the mechanical chassis; cam ⑤ → pinch operating arm ⑧ (linked with pinch arm assembly and pinch press–fit spring ⑮ → pinch arm assembly ㉓ shown in Fig.s 14–15 and 14–16. When cam ⑤ rotates in the direction indicated by the arrow, pinch arm assembly ㉓ rotates in the press–fit direction.

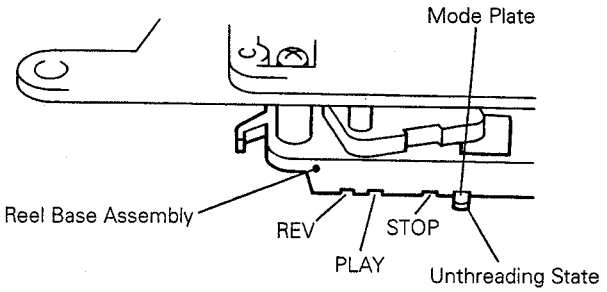


Fig. 14–12

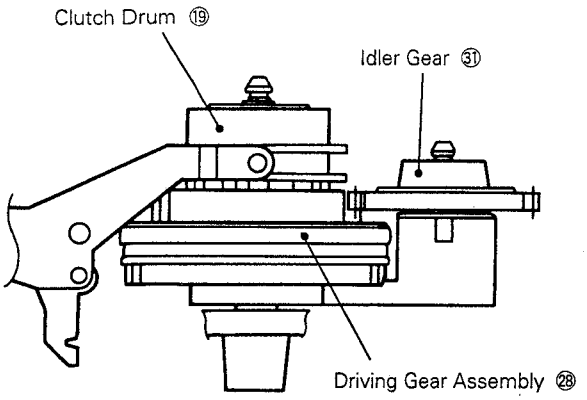


Fig. 14–13

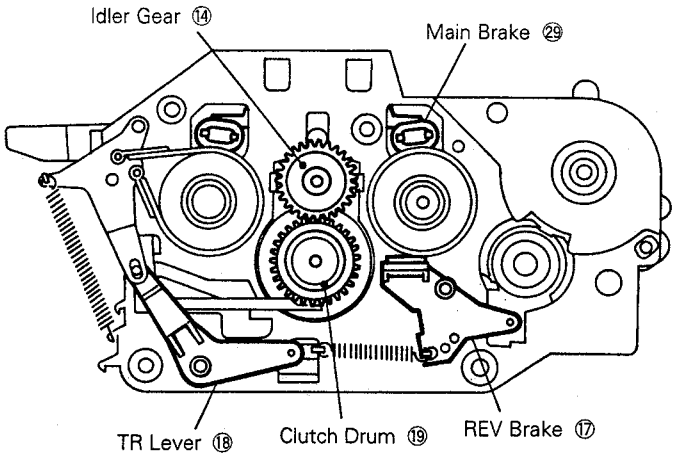


Fig. 14–14

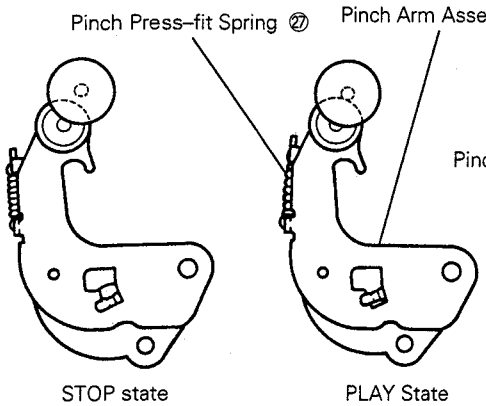


Fig. 14–15

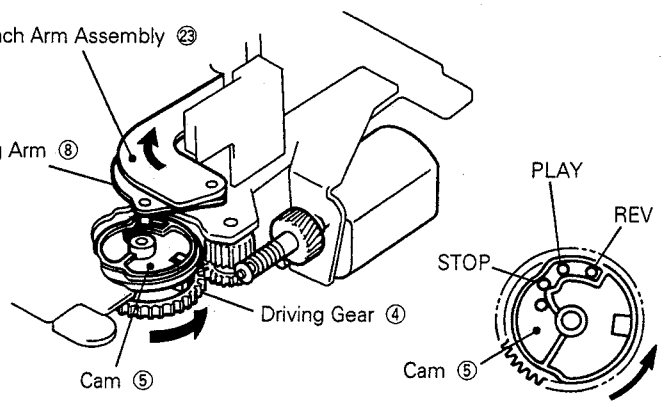


Fig. 14–16

2. Although clutch drum ⑲ moves up/down depending on the motion of mode plate ⑨, driving gear assembly ㉘ is limited in torque as shown in Fig. 14–13 (page Å~) by the mechanism of the felt clutch placed between upper and lower gears. Downward motion of clutch drum ⑲ causes the upper and lower gears to be directly connected, activating FF/REW.
3. Main brake ㉙ works only when plunger ㉚ is ON. When the plunger is ON, clutch drum ⑲ is freed via change lever ㊲. Idler gear ㉛ oscillates to the left and right by the power transmitted from capstan ㉝ by belt ㉞ and transmits the power to the reel set. (See Figs. 14–14 and 14–17.)
4. The following shows the operations in each mode: (See Table 1.)

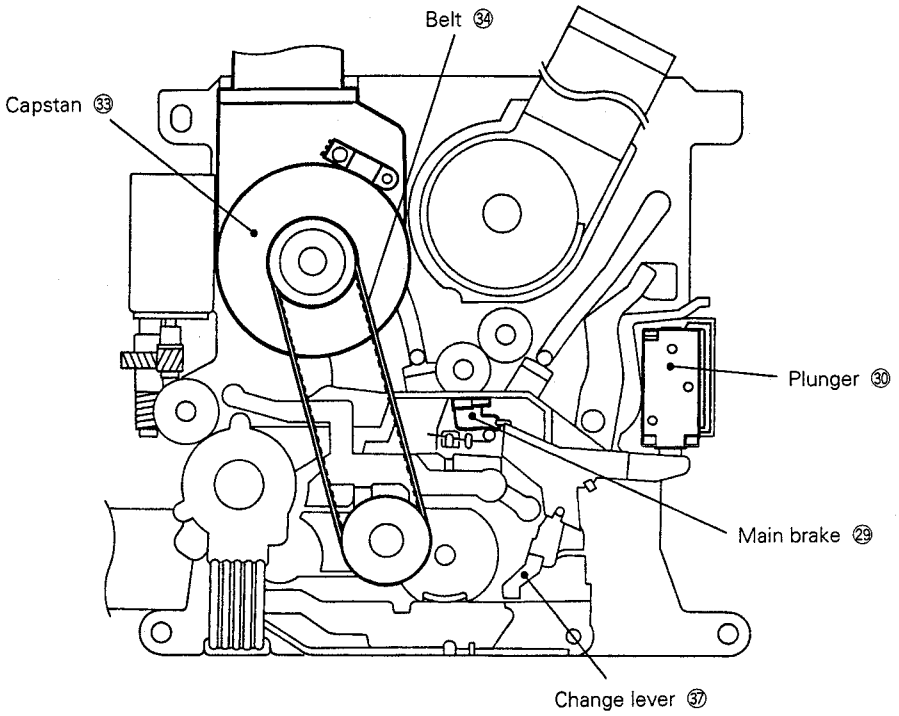


Fig. 14–17 (Bottom)

	Pinch Roller Press–fit	Clutch Drum	REV Brake	TR Lever
STOP	OFF	Down (locked)	OFF	STOP state
FF. REW (search mode)	OFF	Down (locked)	OFF	STOP state
PLAY. REC CUE. PAUSE	ON	Up (free)	OFF	PLAY state
REVIEW	ON	Up (free)	ON	STOP state

Table 1 Operation Matrix

14.3.3 STOP Mode → Unthreading Mode

The basic operation is the reverse operation from the unthreading mode to the STOP mode. The main difference is to wind the tape into the cassette case.

1. Power motor ① rotates for a short time and fixes R-side reel setter ⑮ by hard brake ⑯.
2. Power motor ① rotates to start moving slider L and R assemblies ⑳ and ㉑, pull-arm assembly ㉔, and pinch arm assembly ㉓ (trying to return by the spring force) forward to the unthreading position along the groove, and simultaneously to rotate capstan ㉝, so that power is transmitted to L-side reel setter ⑭ via idler gear ㉛. Thus, guides move from the STOP position to the unthreading position while L-side reel setter ⑭ winds the tape.
3. When all the guides are housed in the cassette tape case, power motor ① stops. For a while after the motor stops, L-side reel setter ⑭ is rotated to completely wind the tape, then the capstan motor is stopped to stop L-side reel setter ⑭.
4. Power motor ① is rotated to release hard brake ⑯ locking R-side reel setter ⑮, and power motor ① is stopped to terminate the operation.

14.3.4 Tape Pass

The following diagram shows the path as the tape is wound from L-side reel setter ⑭ to R-side reel setter ⑮ in PLAY mode. The tape is shown by the thick line in the diagram.

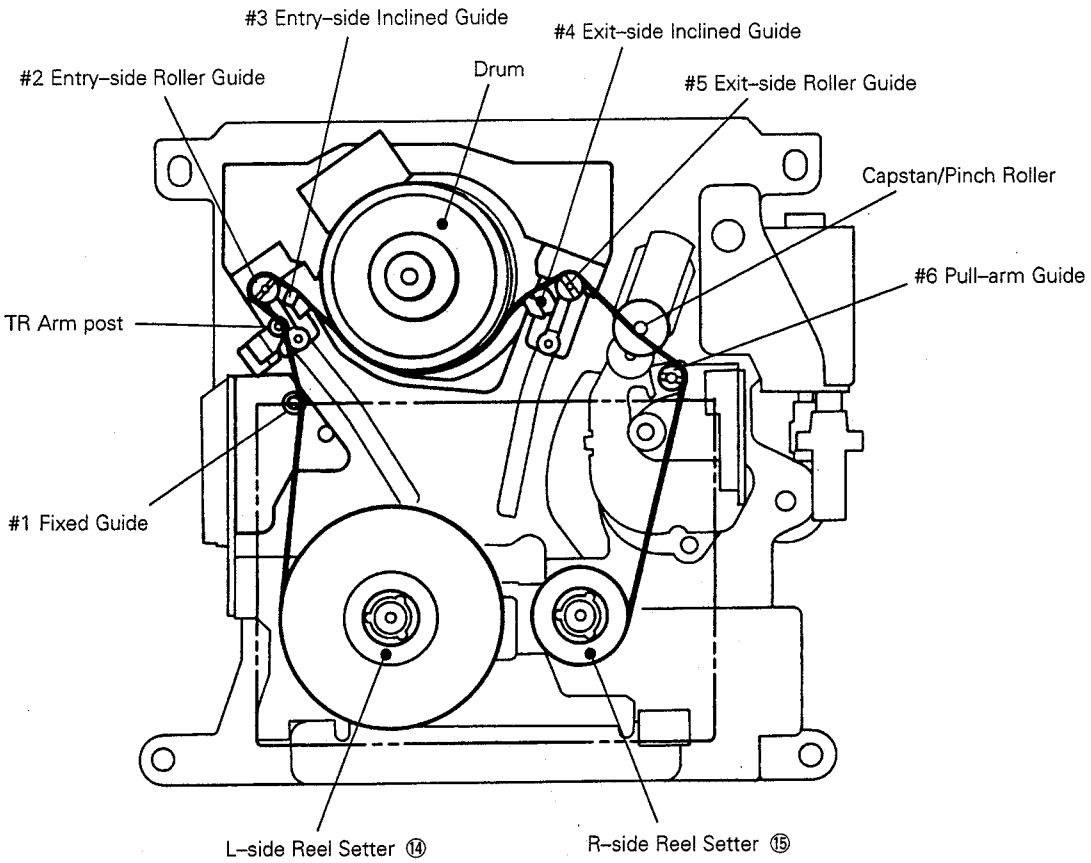


Fig. 14-18 (Top)

15. DIAGNOSIS METHOD

15.1 IN REGARD TO THE DIAGNOSIS METHOD FOR PCB ASSY

■ Diagnosis preparations for main unit and interface unit

1. Remove the bonnet.
2. Remove the rear panel. (Remove the four screws marked ◄ at the side of the rear panel and the three screws at the bottom.)

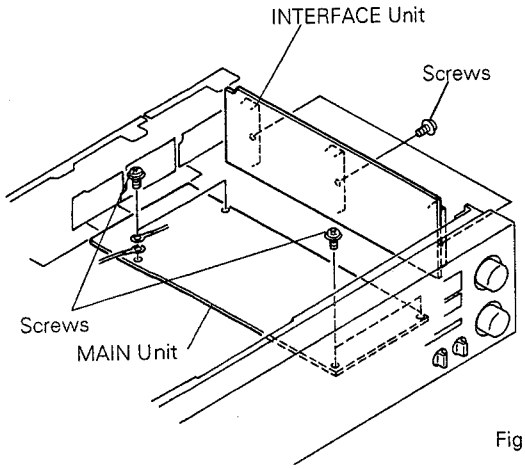


Fig.1

5. Remove the INTERFACE unit connectors CN3301 (ANALOG IN), CN3305 (ANALOG OUT), CN3302 (connector from the VR unit), and CN3306 (connector from the HEADPHONE unit).
6. Cut the binders (4 places).

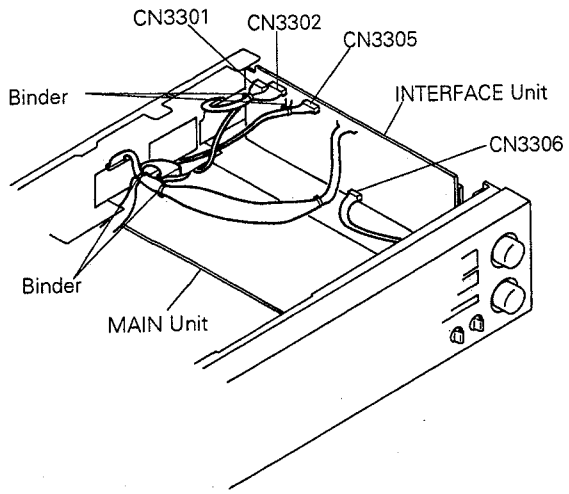


Fig.2

7. Raise the MAIN unit. (Fig. 3)
   Use the clip on the rear panel side of the INTERFACE unit to connect the INTERFACE unit and the MAIN unit.
8. Stand the unit against the rib of the panel stay.
   Please be careful, as the three rubber spacers at the rear of the MAIN unit may come off when the MAIN unit is raised.

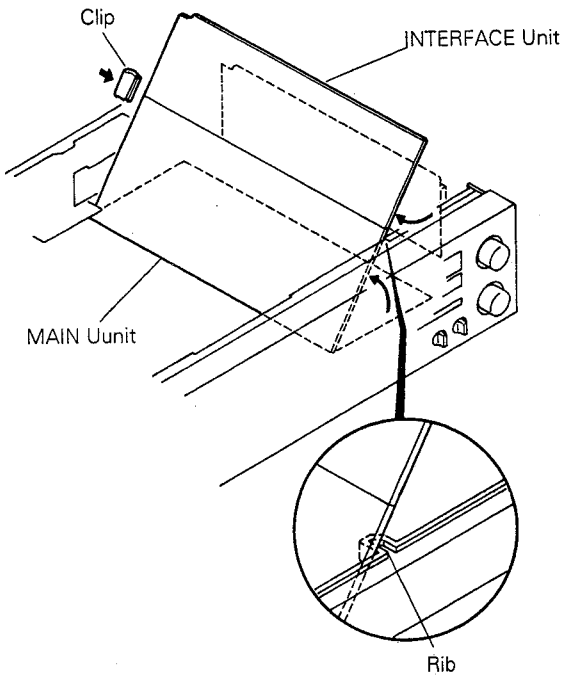
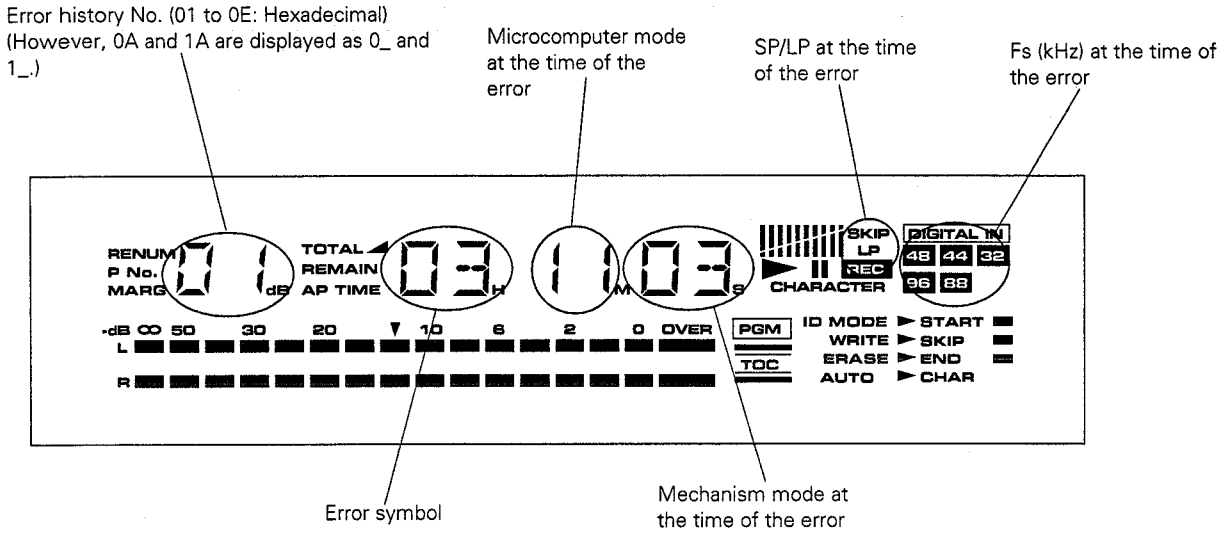


Fig.3

15.2 IN REGARD TO THE SELF-DIAGNOSIS/ERROR HISTORY DISPLAY FUNCTION

The self-diagnosis function is the function for display of the error symbol on the PNo display part of the front panel when the PEAK RESET key is pressed at the time of error-occurrence.
As the error data are stored in the memory, the error symbols again can be displayed by executing the following operations even when the power cable has been disconnected from the power outlet (error history display function).

1. Enter test mode by bringing pin 7 (xTEST) of the MAIN unit connector CN23 to L level (ground). At this time, [PGM] will be displayed flashing.
2. Enter error history display mode by pressing the CHECK key on the remote control.
   In error history display mode, display on the FL is made as shown in the following figure.



* When the error history contains no data (when not even a single error has occurred), "NOERR" will be displayed flashing for 3 sec and the unit will not enter into error history display mode.
* On entry into error history display mode, the most recent error will be displayed.
* Please refer to the following tables for error symbols, mechanism mode, and microcomputer mode.

3. The MS+/– key can be used to follow the error history in both directions. The error history No. "1" is the oldest error, ad the error with the highest number is the most recent error. The error history can memorize a maximum of 30 errors.
4. When the ID MODE key is pressed while the MUTE key is being pressed, the error history will be cleared (all error history data will be erased).
5. The error history display is ended when the xTEST terminal is brought to H level (5 V) or by switching to a different test mode (TACH adjustment etc.).

• In regard to the mechanism mode

Mechanism Mode	Contents
01	Standby
02	STOP
03	Forward PLAY
04	Reverse PLAY
05	CUE
06	REVIEW
07	Forward PLAY/PAUSE
08	Reverse PLAY/PAUSE
09	FF
0_	REW
0B	REC
0C	REC/PAUSE
0D	AFREC
0E	Emergency
0F	Reset

• In regard to the error symbols

Error symbol	Contents	Occurrence condition	Estimated cause
1	Abnormal drum rotation error	The HSWP signal has not been generated for 2 sec at the time of drum rotation start-up.	The drum does not rotate. • Tape sticking at the time of dewing etc. • Defective contact of CN3, tape entanglement • Defective motor drive • Entry of foreign matter, defective drum motor • Defective drum FG amplifier circuit
2		The HSWP signal has not been generated for 0.48 sec at the time of FF/REW (< 125 rmp).	Abnormal drop of the drum speed • Large tape load
3		The drum servo lock has been unlocked for 0.12 sec at the time of constant drum speed.	Drum servo deviation • Large tape load • Tape sticking • Noise in the drum FG
4	Abnormal reel rotation error	At the time of PLAY/REC/CUE/REVIEW (< x16), either reel pulse has not been generated for 5 sec.	The reel base is not rotating. • Defective mechanism, tape is being spit out. • Defective reel pulse generation circuit
5		At the time of x16 CUE/REVIEW, either reel pulse has not been generated for 1.25 sec.	
6		At the time of FF/REW, either reel pulse has not been generated for 15 sec.	
7	Abnormal capstan error	At the time of PLAY, the capstan FG pulse has not been generated for 2 sec.	The capstan motor does not rotate. • Defective contact of CN4 • Defective motor driver • Entry of foreign matter, defective drum motor • Defective capstan FG amplifier circuit

• In regard to the microcomputer mode

Microcomputer mode	Processing contents	Microcomputer mode	Processing contents	Microcomputer mode	Processing contents
10	STOP processing	20	+MS processing	40	Start ID post recording
11	PLAY processing	21	–MS processing	41	Skip ID post recording
12	Reverse PLAY processing	22	Track number search processing	42	Start, skip erasing
13	CUE processing	23	ATIME search processing	43	End ID erasing
14	REVIEW processing	24	Numerical input at the time of STOP	44	End ID recording
15	FF processing	25	PLAY/PAUSE numerical input	45	Post recording mode transition
16	REW processing	26	Program check processing	80	Recording processing
17	PAUSE processing	27	End search	81	REC MUTE processing
18	Tape end processing	28	STOP → REC pause	82	REC/PAUSE processing
19	Tape top processing	29	Start ID post recording	83	Start ID post recording
1_	Tray close processing	2_	Skip ID post recording	84	Skip ID post recording
1B	Tray open processing	2B	Start, skip erasing	85	End ID erasing
1C	Cassette loading processing	2C	End ID erasing	86	STOP → REC pause
1D	Cassette eject processing	2D	End ID recording	87	REC monitor processing
1E	Tape threading processing	2E	PB mode transition	88	REC mode transition
1F	Power ON initialization processing	2F	Emergency		

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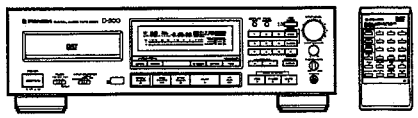
Service Manual



SERVICE GUIDE
ORDER NO.
ARP2338

DIGITAL AUDIO TAPE DECK

D-500

- **Refer to the service manual ARP2336, D – 500/HEM type.**

CONTENTS

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DG SEPT. 1991 Printed in Japan

1. DAT FORMAT

The standard mechanical system of DAT (digital audio tape deck) is a helical scan system that winds tape over a 30-millimeter diameter drum at a 90-degree angle. Two heads on the drum have azimuth angles of ±20 degrees. Therefore, these heads are aligned obliquely (6 degrees 22 minutes) versus the track on the tape without a guard band as shown in Fig. 2.

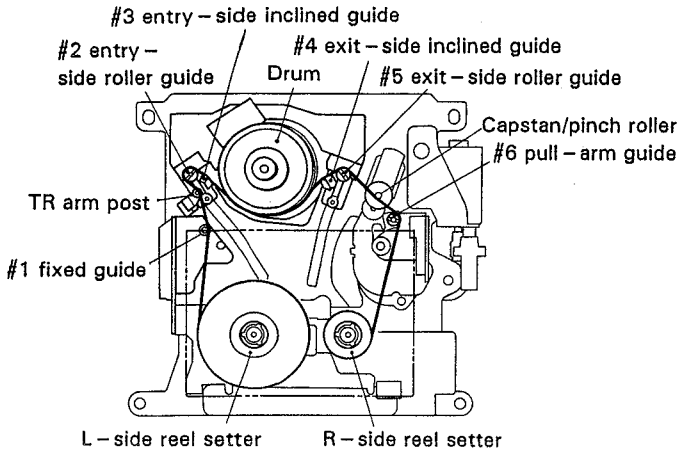


Fig. 1 DAT Tape Motion Diagram

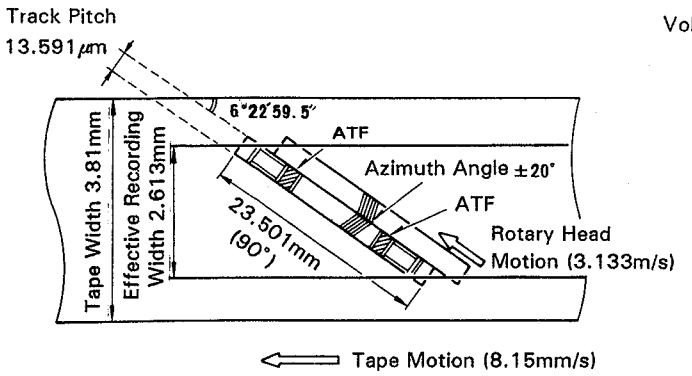


Fig. 2 DAT Tape Format

DAT employ the following new features which household videotape recorders lack.

(1) Tape wrap angle of 90 degrees.
(2) Tracking servo during playback is ATF (ATF pilot signal exists only before and after tracks).
(3) The erasing head records a completely new signal and erases the old signal.

A wrap angle of 90 degrees versus the drum means that the two heads only make contact with the tape at 90-degree intervals during one rotation of the drum. Therefore, the playback RF waveform is not continuous like the waveform of a VTR and becomes intermittent (see Fig. 3).

Consequently, RAM is used as a data processor because compression of the time base is necessary during recording, while expansion of the time base is required during playback. DAT has four modes that can record and playback. The standard mode has a sampling frequency of 48kHz, quantization law coding of 16 bits, and a tape speed of 8.15 millimeters per second. Additionally, there are two playback modes dedicated to the playback of prerecorded tapes. The difference in these two modes lies in the track pitch. The normal track mode has the same width as the record and playback modes, while the wide track mode has 1.5 times the width of normal track mode.

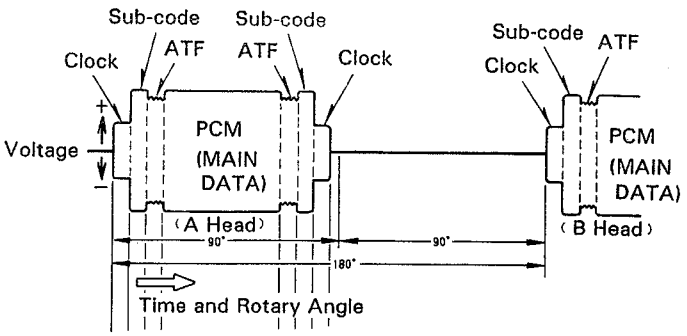


Fig. 3 RF Signal (Play Back)

1.1 SAMPLING FREQUENCIES

The sampling frequencies included are 48kHz, 44.1kHz, and 32kHz. The standard sampling frequency is 48kHz, and 44.1kHz is used for soft tapes and CD digital recordings.
A sampling frequency of 32kHz is used for options, and there are three modes. Option 1 only changes the sampling frequency from 48kHz to 32kHz, and is generally used for satellite broadcasts. Option 2 uses 12-bit nonlinear quantization to achieve a transmission rate that is half that of the standard mode. The recording time is doubled because the tape feed rate is halved. Option 3 allows 4-channel recording with a sampling frequency of 32kHz (see Fig. 1-1).

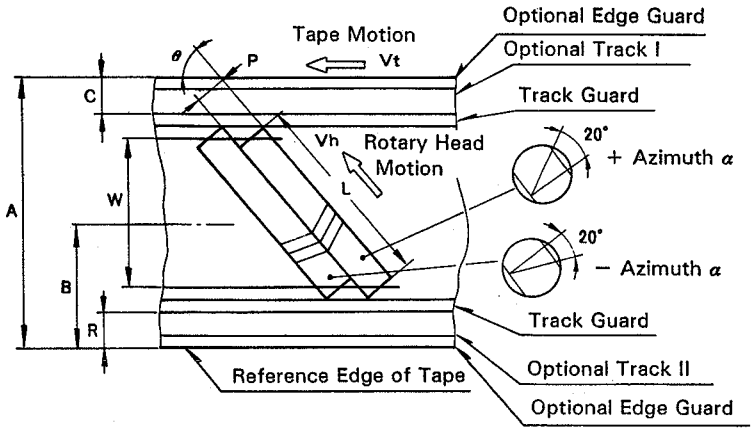
1.2 TAPE FORMAT

The tracks of digital audio tape are closely aligned without any space between tracks. This arrangement is known as "guard band-less" recording. Short tape naturally allows recording of many signals. Additionally, cross talk will occur if this problem is not addressed because neighboring tracks are traced, and noise adulterates the tracks.

The "azimuth system" is used as a method to prevent noise from contaminating the signal when cross talk occurs. Conventional audio recorders also drop the high frequency signals during playback if the azimuth angle is distorted, and the high tones are lost.
Digital audio tape uses this principle in reverse to eliminate cross talk from neighboring tracks. The A head is installed at + azimuth α from the track perpendicular, while the B head is installed at − azimuth α from the track perpendicular. Therefore, signals that have a slope of $\pm\alpha$ versus the tracks on the tape are recorded alternately as shown in Fig. 1-2-1. The A head traces the recorded track during playback, and the tape is correctly played back including the high frequency range when the azimuth error is zero. However, a slope of 2α results between the recording pattern and the playback head if part of the A head is caught by track B. Therefore, the high frequency signal is cancelled and cross talk does not occur. The data format that performs the above functions is indicated in Fig. 1-2-1 and Fig. 1-2-2.

MODE / ITEMS	Normal Track					Wide Track
	Mandatory	Option-1	Option-2	Option-3	Start Tapes & Digital Rec. only	Start Track
Number of channels (CH)	2	2	2	4	2	2
Sampling Frequency (kHz)	48	32	32	32	44.1	
Quantization Law Coding (bit)	16 (Linear)	16 (Linear)	12 (Non Linear)	12 (Non Linear)	16 (Linear)	16 (Linear)
Linear Recording Density (KBPI)	61.0	61.0			61.0	61.0
Packing Density (MBPI²)	114	114			114	76
Transmission Rate (MBPS)	2.46	2.46	1.23	2.46	2.46	
Sub-coding (Capacity)(KBPS)	273.1	273.1	136.5	273.1	273.1	
Modulation Scheme	8-10					
Error Correction Code	Doubly encoded RSC					
Tracking Method	Area divided ATF					
Cassette Size (mm)	73 × 54 × 10.5					
Maximum Recording Time (Tape thickness 13μm)(MIN)	120	120	240	120	120	80

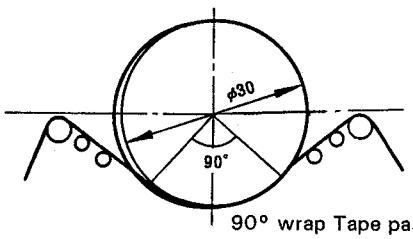
Fig. 1-1 Basic Parameters of R-DAT Format



Track Configuration and Dimensions
(View on magnetic sensitive side)

ITEMS \ MODE	Mandatory	Option-1	Option-2	Option-3	PRE-RECORDED TAPE	
					Normal Track	Wide Track
(A) Tape width [mm]	3.81 (+0, −0.02)				3.81 (+0, −0.02)	
(W) Effective recording width [mm]	2.613				2.613	
(Vt) Tape speed [mm/sec]	8.15	8.15	4.075	8.15	8.15	12.225
	±0.5%					
(L) Track length [mm]	23.501				23.501	23.171
(P) Track pitch [μm]	13.591				13.591	20.41
(θ) Track angle (Tape runs) [deg]	6° 22′ 59.5″				6° 22′ 59.5″	6° 23′ 29.4″
(a) Head gap azimuth angle [deg]	±20				±20	
(B) Center of track [mm]	1.905				1.905	
(C) Optional track I [mm] (Including optional edge guard (0.1))	0.5				0.5	
(R) Optional track II [mm] (Including optional edge guard (0.1))	0.5				0.5	

Fig. 1−2−1 Tape Format (1)



90° wrap Tape pass

Rotary Head system Tape pass

Recommended Cylinder Specifications \ MODE	Mandatory	Option-1	Option-2	Option-3	PRE-RECORDED TAPE	
					Normal Track	Wide Track
(φ) Drum diameter [mm]	30.0				30.0	
(H) Drum revolution speed [mm]	2000		1000	2000	2000	
(Vh) Writing speed [m/S]	3.133		1.567	3.133	3.133	3.129
(φ) Wrap angle [deg]	90.0				90.0	
(θ) Track angle [deg]	6° 22′				6° 22′	

Fig. 1−2−2 Tape Format (2)

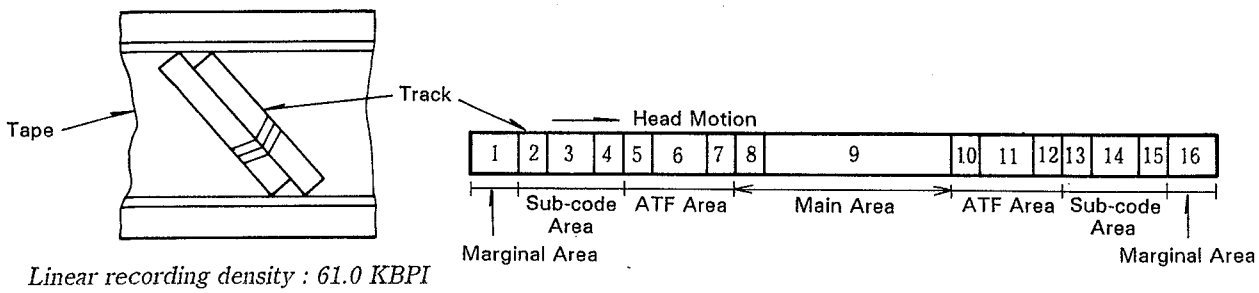
1.3 TRACK FORMAT

The following three major areas are included on one track.

(1) Main area for recording the Main audio data and parities for error correction
(2) ATF servo area for the head to correctly trace the track during playback
(3) Sub-code area for index, program no., and other sub-code recording

One track can be divided into 196 blocks. The necessary block count is assigned to separate the above three areas.

The track format is shown in Fig. 1-3-1. The Main data is sandwiched between two ATF (Automatic Track Finding) areas provided for tracking. Additionally, sub-code areas that can record the recorded tune order, time code, and other data are included on both sides. A margin of approximately 5 percent is provided on both edges of the track to make the total wrap angle of the drum 90 degrees. The ATF areas on wide tracks are slightly wider. The wider ATF areas are suited to the tracking of wide tracks and are interchangeable with normal tracks during operation. Inter Block Gaps (IBG) are provided between signals, and each area can be changed independently by overwriting.



Linear recording density : 61.0 KBPI
fch : 9.408 MHz
Track format : Drum 30φ, Wrap angle 90°
Drum revolution speed 2000 rpm

No.	Block name	Signal	Normal track (For DAT and Pre-Recorded Tape)			Wide trak (For Pre-Recorded Tape)		
			Angle (deg)	Number of blocks	Period (μS)	Angle (deg)	Number of blocks	Period (μS)
1	MARGIN	1/2fch	5.051	11	420.9	5.051	11	420.9
2	PLL (SUB)	1/2fch	0.918	2	76.5	0.918	2	76.5
3	SUB-1		3.673	8	306.1	3.673	8	306.1
4	POST AMBLE	1/2fch	0.459	1	38.3	0.459	1	38.3
5	IBG	1/6fch	1.378	3	114.8	0.918	2	76.5
6	ATF		2.296	5	191.3	3.444	7.5	287.0
7	IBG	1/6fch	1.378	3	114.8	0.689	1.5	57.4
8	PLL (MAIN)	1/2fch	0.918	2	76.5	0.918	2	76.5
9	PCM		58.776	128	4898.0	58.776	128	4898.0
10	IBG	1/6fch	1.378	3	114.8	0.918	2	76.5
11	ATF		2.296	5	191.3	3.444	7.5	287.0
12	IBG	1/6fch	1.378	3	114.8	0.689	1.5	57.4
13	PLL (SUB)	1/2fch	0.918	2	76.5	0.918	2	76.5
14	SUB-2		3.673	8	306.1	3.673	8	306.1
15	POST AMBLE	1/2fch	0.459	1	38.3	0.459	1	38.3
16	MARGIN	1/2fch	5.051	11	420.9	5.051	11	420.9
Total			90	196	7500	90	196	7500

Fig. 1-3-1 Track Format

1.4 BLOCK FORMAT

One track consists of 196 blocks of signals, including 128 blocks for Main data. A block has the structure of the the Main block format shown in Fig. 1-4-1. One block corresponds to 1 frame (588 channel bits) of a CD (compact disc). The following data is included in the one block of Main area.

(1) SYNC (8 bits)

4T-4T indicates the beginning of the block (11T-11T in a CD).

(2) ID Code (8 bits)

The ID code indicates the characteristics of the Main data in the block.

(3) Block Address (8 bits)

Because there are 128 blocks of Main data on one track, a binary address (0000000 through 1111111) is added to each of the 128 (2^7) blocks.

(4) Parity (8 bits)

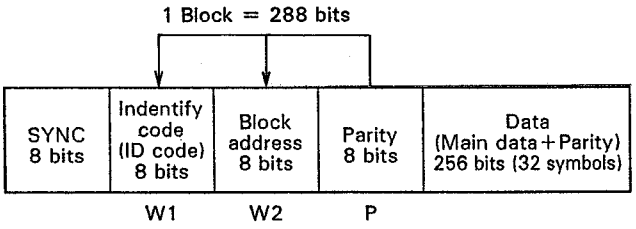
The parity bit for items (2) and (3) above, exclusive OR for items (2) and (3).

(5) Main data (256 bits)

32-symbol Main data and parity

Refer to "Sub-codes" on page 13 for details concerning items (2) and (3) above. The 32,768 (32 symbols × 128 = 4,096 symbols = 32,768 bits) bits of data in the Main area of a track has the capacity to record parity. This capacity is equivalent to 4 KB of RAM. In addition to the Main data, an ID code (IDENTIFY CODE : W1) and block address (W2) are provided, and a control signal for the Main signal is recorded.

The sub-code blocks are the eight blocks before and after the Main area. The structure of a sub-code block is the same as a block of the Main area, and only the contents of W1 and W2 are different. For example, there are four bits from 0000 to 1111 because there are total of only 16 sub-code blocks on one track. Additionally, the most significant bit (MSB) of W2 is "0" in the Main area and "1" in the sub-code area, and that block contains the identifying bit for Main and sub-code areas (refer to page 13 for details).



Parity : P = W1 ⊕ W2 (⊕ : MOD2)

Block address : Block address for main data block.
The MSB is identify bits for sub-code block or main data block.
MSB "0" = PCM data.
MSB "1" = SUB code data.

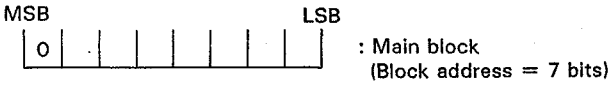
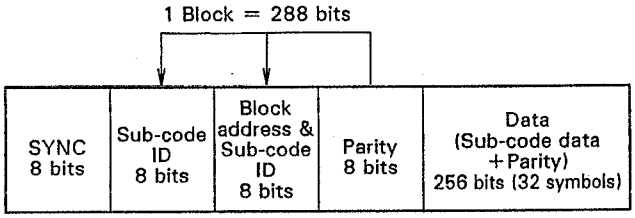
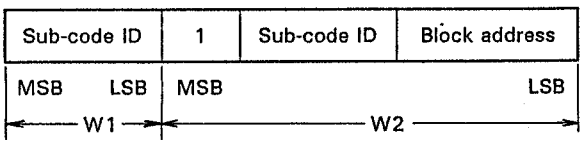


Fig. 1-4-1 Main Block Format



Parity : P = W1 ⊕ W2 (⊕ : MOD2)



Block address : Block address for sub-code block

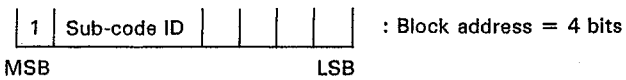


Fig. 1-4-2 Sub-code Block Format

1.5 INTERLEAVE

Frequency sampling of 48kHz and 16-bit quantization are standard in the DAT operating mode. The 16 bits of data are divided into upper and lower areas of 8 bits each, and each bit is processed as one symbol. Compact discs employ the CIRC (Cross Interleave Reed-Solomon Code) error correction code, which is a combination of interleave and error correction. However, digital audio tape cannot use the same system as a compact disc because the time base must be compressed and expanded. Additionally, signal processing must position the lowest track for processing. Naturally, the lowest track must be synchronized with the head position (drum rotation position) at that time. The data capacity for processing contained in one track (half a rotation of the drum) is as follows because the drum revolution speed is 2,000rpm for 48kHz sampling frequency and the 16-bit quantization mode.

15 ms × 48kHz = 720 (number of sampling occurrences in half a rotation of the drum)

One sampling occurrence has two symbols each in the left and right channels. Therefore, the total number of symbols is 2,880 (720 × 2 × 2). Because one track has a capacity of 4,096 symbols, the remaining capacity can be used to record error correction codes. Additionally, the data capacity of this track is the equivalent of 4 KB of RAM. The DAT interleave consists of one separator for data that encompasses two tracks (one rotation of the drum). Refer to Fig. 1-5-1 Interleave Scheme for details.

The data capacity for one channel for one rotation of the drum (30 ms) is 1,440 words (2,880 symbols). Therefore, the data numbers range from 0 to 1439, and are divided into two tracks using the even and odd numbers for the left and right channels. One track (azimuth angle of +20 degrees) consists of the even numbers of the left channel and the odd numbers of the right channel. The next track (azimuth angle of −20 degrees) consists of the odd numbers of the right channel and the even numbers of the left channel. Next, data is arranged in one Main area divided into 8 upper bits and 8 lower bits as shown in Fig. 1-6-1 (a). Fig. 1-6-1 (a) shows a Main block (1 block = 32 symbols), and the block address within a track is shown in Fig. 1-6-1 (b). One data number corresponds to one location in Fig. 1-6-1 (a). Therefore, if this is mapped with the address of RAM, interleave can be accomplished by recording data input from a sequential analog-to-digital converter to the required RAM address. This is similar to the processing in the interleave of an 8-mm videotape recorder (VTR).
The A head (+ azimuth) and B head (− azimuth) are positioned as shown in Fig. 1-5-2 (a) so that a complete span is achieved. The even samplings of the L channel are recorded on the first half of the A head, and the odd samplings of the R channel are recorded on the latter half of the A head. The even samplings of the R channel are recorded on the first half of the B head, and the odd samplings of the L channel are recorded on the latter half of the B head. This allows correction of an entire erroneous track or dropouts up to 2,664 symbols by blinding the head.

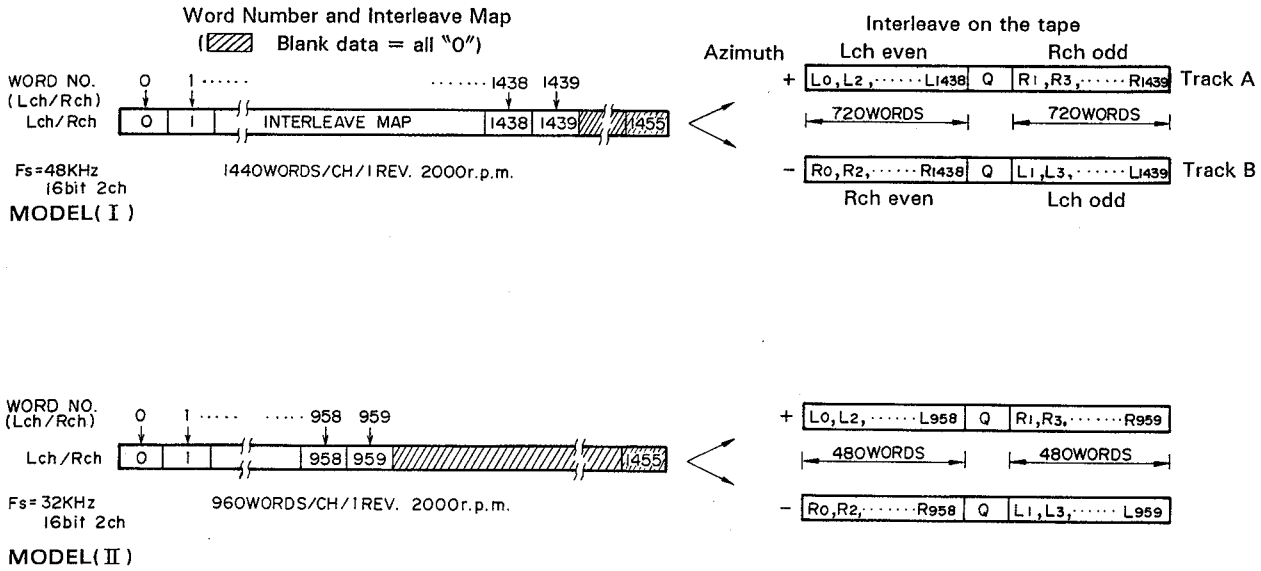
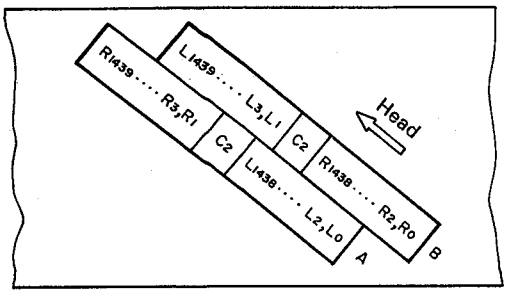
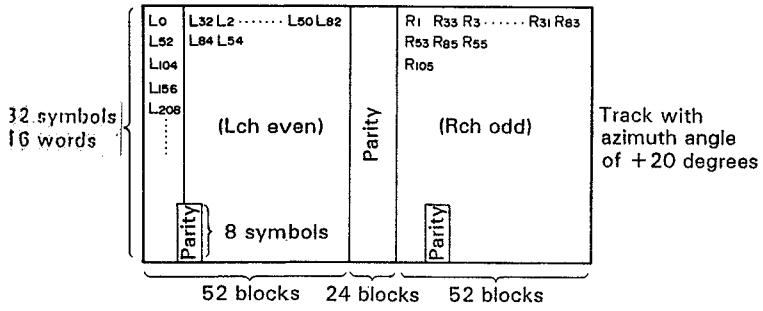
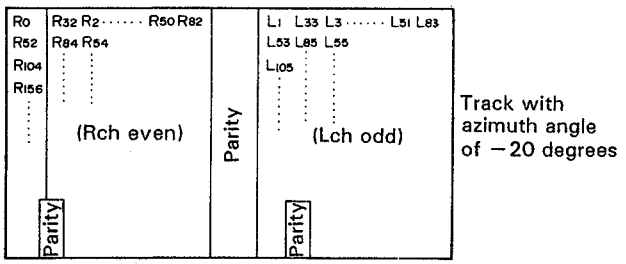


Fig. 1-5-1 Interleave Scheme (Modes I and II)



(a)



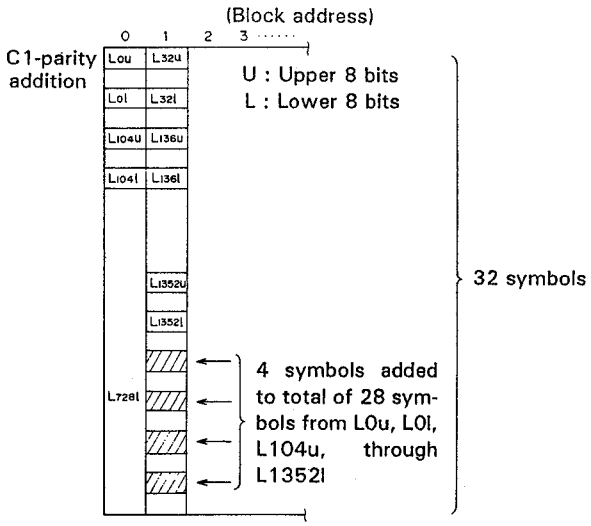


(b)

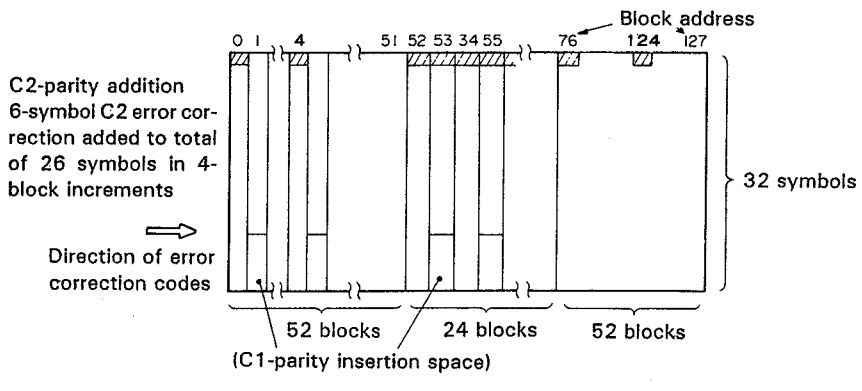
Fig. 1−5−2 Interleave Format

1.6 ERROR CORRECTION CODE

An error correction code is added to data for which interleave has been completed (Fig. 1−6−1). First, a 4-symbol C1-parity is added to each of the 28 symbols of data from L0u, L0l, L104u, through L13521, as shown in Fig. 1−6−1 (a). Then, four symbols are added below the 28 symbols from L0u, L0l, L104u, through L13521. A C1-parity spans two blocks, and the C1-parity within two blocks comprises eight symbols. Next, a 6-symbol C2-parity is added to a total of 26 symbols in 4-block increments from block 0, block 4, through block 124. The C2-parity is sandwiched into a position in the Main data. One track (total number of error correction codes in one Main area) contains a total of 1,184 symbols (C1 4 × 128 = 512, C2 32 × 12 + 24 × 12 = 672). Because the data capacity of one track is 4,096 symbols, the data capacity for non-parity information is 2,912 symbols (4,096 − 1,184). However, 32 symbols are leftover because the data capacity of this interval is 2,880 symbols. These 32 symbols are filled with zeroes. This portion of the block corresponds to word numbers 1440 through 1455 shown in Fig. 1−5−1.



(a)



(b)

Fig. 1−6−1 Addition of Error Correction Codes

1.7 8 – 10 MODULATION

The 8 bits of data that allows easy control and demodulation of the frequency band of a signal recorded on the disc of a CD was changed to 14 bits in order to perform EFM modulation. EFM is a type of modulation that selects a 256-bit (2^8) pattern [factor of 4,096 (2^{14})] and handles 8-bit data so that the minimum inversion space (Tmin) is 3 bits and the maximum inversion space (Tmax) is 11 bits. DAT 8 – 10 modulation handles 8-bit data so that Tmax is 4 bits (factor of 1,024) and Tmin is 1 bit. DAT 8 – 10 modulation also handles a 10-bit pattern. Additionally, items having a DC component within ±2 are selected for this 10-bit pattern. As seen from the conversion table, there are two 10-bit patterns for one 8-bit data item. If the DC component of the 10-bit pattern is 0, the two patterns are the same. If the DC component is ±2, the most significant bit (MSB) is changed to 0 or 1 and the remaining nine bits of the pattern are the same. The Q in the table represents the characteristics of the code. If Q equals 1, the next code will be selected from the pattern of the Q' = 1 column corresponding to the data. If Q equals −1, the pattern in the Q' = −1 column on the left will be selected. DC is 0 or −2 in the Q' = 1 column, and DC is 0 or +2 in the Q' = −1 column. If DC equals 0, the 10-bit codes are the same regardless of the value of Q'. However, the value of Q differs for the Q' = 1 column and the Q' = −1 column. The 8-bit data repeated the same value when the data was 80 (assume Q' = 1).

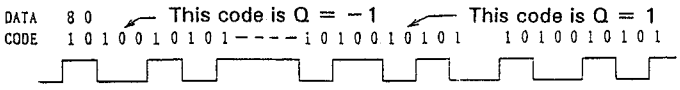


Fig. 1 – 7 – 1

As shown in the above diagram, the polarity is inverted and recorded on the tape even though the code is the same. Next, if DC equals 2 or −2, the 10-bit code is different, but the value of Q is the same. Use Q' = 1 if it is assumed that the data repeated the same value like the above diagram.

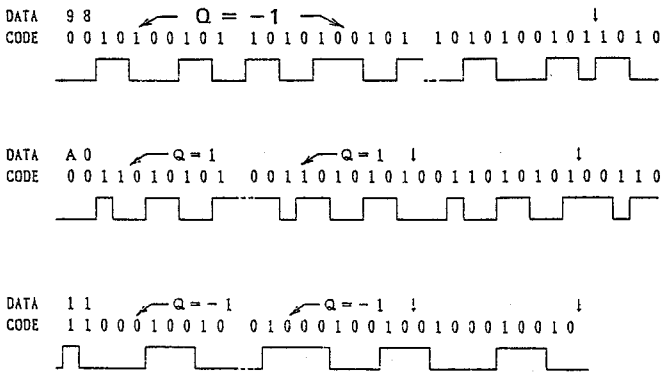


Fig. 1 – 7 – 2

As shown in the above diagram, the DC component alternates repeatedly between + and − to invert the polarity and cause recording, and the D.S.V. (Digital Sum Value) of the recording signal approaches zero. In DAT, the interleave cannot be accomplished during playback unless the data from the two tracks is united because the Main data is interleaved on two tracks. The data capacity of these two tracks is 8,192 symbols (4,096 × 2) or 65,536 bits. This is the equivalent of 8 KB of RAM. During playback, data must be output to a digital-to-analog converter while unraveling the interleave, and the data for playback must be written to RAM. The reverse of this process occurs during recording. The data to be recorded must be transferred to the head while being interleaved. Therefore, there must be at least two 8-KB blocks available as RAM for repeated alternating processing.

Data : Main (pulse code modulation) data
Code : Selects encoder code of NRZI modulator and Q' (Q data obtained from previous code)
Coding direction : Left to right (from most significant bit to least significant bit)
Q' : DC data of previous code
Q : DC data of current code

		Q' = − 1			Q' = 1		
	DATA (MSB···LSB)	CODE (MSB···LSB)	DC	Q	CODE (MSB···LSB)	DC	Q
00	0 0 0 0 0 0 0 0	0 1 0 1 0 1 0 1 0 1	0	1	0 1 0 1 0 1 0 1 0 1	0	− 1
01	0 0 0 0 0 0 0 1	0 1 0 1 0 1 0 1 1 1	0	− 1	0 1 0 1 0 1 0 1 1 1	0	1
02	0 0 0 0 0 0 1 0	0 1 0 1 0 1 1 1 0 1	0	− 1	0 1 0 1 0 1 1 1 0 1	0	1
03	0 0 0 0 0 0 1 1	0 1 0 1 0 1 1 1 1 1	0	1	0 1 0 1 0 1 1 1 1 1	0	− 1
04	0 0 0 0 0 1 0 0	0 1 0 1 0 0 1 0 0 1	0	− 1	0 1 0 1 0 0 1 0 0 1	0	1
05	0 0 0 0 0 1 0 1	0 1 0 1 0 0 1 0 1 1	0	1	0 1 0 1 0 0 1 0 1 1	0	− 1
06	0 0 0 0 0 1 1 0	0 1 0 1 0 0 1 1 1 0	0	1	0 1 0 1 0 0 1 1 1 0	0	− 1
07	0 0 0 0 0 1 1 1	0 1 0 1 0 1 1 0 1 0	0	1	0 1 0 1 0 1 1 0 1 0	0	− 1
08	0 0 0 0 1 0 0 0	0 1 0 1 1 1 0 1 0 1	0	− 1	0 1 0 1 1 1 0 1 0 1	0	1
09	0 0 0 0 1 0 0 1	0 1 0 1 1 1 0 1 1 1	0	1	0 1 0 1 1 1 0 1 1 1	0	− 1
0A	0 0 0 0 1 0 1 0	0 1 0 1 1 1 1 1 0 1	0	1	0 1 0 1 1 1 1 1 0 1	0	− 1
0B	0 0 0 0 1 0 1 1	0 1 0 1 1 1 1 1 1 1	0	− 1	0 1 0 1 1 1 1 1 1 1	0	1
0C	0 0 0 0 1 1 0 0	0 1 0 1 1 0 1 0 0 1	0	1	0 1 0 1 1 0 1 0 0 1	0	− 1
0D	0 0 0 0 1 1 0 1	0 1 0 1 1 0 1 0 1 1	0	− 1	0 1 0 1 1 0 1 0 1 1	0	1
0E	0 0 0 0 1 1 1 0	0 1 0 1 1 0 1 1 1 0	0	− 1	0 1 0 1 1 0 1 1 1 0	0	1
0F	0 0 0 0 1 1 1 1	0 1 0 1 1 1 1 0 1 0	0	− 1	0 1 0 1 1 1 1 0 1 0	0	1
10	0 0 0 1 0 0 0 0	1 1 0 1 0 1 0 0 1 0	0	1	1 1 0 1 0 1 0 0 1 0	0	− 1
11	0 0 0 1 0 0 0 1	0 1 0 0 0 1 0 0 1 0	2	− 1	1 1 0 0 0 1 0 0 1 0	− 2	− 1
12	0 0 0 1 0 0 1 0	0 1 0 1 0 1 0 0 1 0	0	− 1	0 1 0 1 0 1 0 0 1 0	0	1
13	0 0 0 1 0 0 1 1	0 1 0 1 1 1 0 0 1 0	0	1	0 1 0 1 1 1 0 0 1 0	0	− 1
14	0 0 0 1 0 1 0 0	1 1 0 1 1 1 0 0 0 1	2	1	0 1 0 1 1 1 0 0 0 1	− 2	1
15	0 0 0 1 0 1 0 1	1 1 0 1 1 1 0 0 1 1	2	− 1	0 1 0 1 1 1 0 0 1 1	− 2	− 1
16	0 0 0 1 0 1 1 0	1 1 0 1 1 1 0 1 1 0	2	− 1	0 1 0 1 1 1 0 1 1 0	− 2	− 1
17	0 0 0 1 0 1 1 1	1 1 0 1 1 1 0 0 1 0	0	− 1	1 1 0 1 1 1 0 0 1 0	0	1
18	0 0 0 1 1 0 0 0	0 1 0 1 1 0 0 1 0 1	2	− 1	1 1 0 1 1 0 0 1 0 1	− 2	− 1
19	0 0 0 1 1 0 0 1	0 1 0 1 1 0 0 1 1 1	2	1	1 1 0 1 1 0 0 1 1 1	− 2	1
1A	0 0 0 1 1 0 1 0	0 1 0 1 1 0 1 1 0 1	2	1	1 1 0 1 1 0 1 1 0 1	− 2	1
1B	0 0 0 1 1 0 1 1	0 1 0 1 1 0 1 1 1 1	2	− 1	1 1 0 1 1 0 1 1 1 1	− 2	− 1
1C	0 0 0 1 1 1 0 0	0 1 0 1 1 1 1 0 0 1	2	1	1 1 0 1 1 1 1 0 0 1	− 2	1
1D	0 0 0 1 1 1 0 1	0 1 0 1 1 1 1 0 1 1	2	− 1	1 1 0 1 1 1 1 0 1 1	− 2	− 1
1E	0 0 0 1 1 1 1 0	0 1 0 1 1 1 1 1 1 0	2	− 1	1 1 0 1 1 1 1 1 1 0	− 2	− 1
1F	0 0 0 1 1 1 1 1	0 1 0 1 1 0 1 0 1 0	2	− 1	1 1 0 1 1 0 1 0 1 0	− 2	− 1

Fig. 1 − 7 − 3 8 − 10 Conversion Table

1.8 AUTOMATIC TRACK FINDING (ATF)

Automatic Track Finding (ATF) is a tracking control system that ensures that heads accurately trace over narrow 13μm tracks. The principle is to control the servo system so that the cross talk values of the ATF signals for the tracks to the left and right of the track being traced are equalized and the data speed is regulated. The signal sequence and length are fixed for DAT for recording on one track. The three major elements are SUB, ATF, and Main, and each of these is divided into finer detail. One track consists of 196 blocks.

The ATF track pattern is shown in Fig. 1-8-2.

The signals are broadly divided and arranged on a track in the order of ATF signals first, followed by data signal ATF signals. ATF signals consist of a combination of frequencies f_1, f_2, f_3, and f_4. The frequencies are respectively 130.67kHz, 522.67kHz, 784.00kHz, and 1.568MHz.

Detailed examination of an ATF signal block shows that there is a margin space called an Inter Block Gaps (IBG) on both sides. This space is for absorbing signal position errors during overwriting. Writing a 1.568MHz signal has the function of erasing the previous recording.

The principal frequency of ATF is 130kHz (f_1). f_2 and f_3 are synchronization signals that are used to create sampling pulses. Observe ATF (1) of the second track (A head even frame) from the left in Fig. 1-8-2.

IBG are passed over when the A head traces this track. The IBG signal (f_4 = 1.5MHz) is not detected because the band-pass filter is passed at point Ⓑ in Fig. 1-8-1. A major 130kHz signal is detected at point Ⓑ when the head passes f_1. Then, when the head passes f_4, f_2, and f_4, the f_1 of the neighboring track on the right and the f_1 of the neighboring track on the left are detected as cross talk of adjoining tracks.

The cross talk values are proportionate to whether the head traces from the track center to the right or traces from the left. The f_1 detection values for the tracks adjoining on the left and right should be equal when the head is tracing properly. Stated differently, tracking control is effected so that both f_1 detection values become equal. This control method is the basic principle of ATF for digital audio tape. Generally, the head width is designed in consideration of track curvature and is fabricated to be approximately 1.5 times the track pitch. Therefore, playback from adjacent tracks is possible.

The actual circuit is represented in Fig. 1-8-1. Signals that have passed the band-bypass filter (point Ⓑ) are subjected to envelope detection and fed to S/H1 and S/H2.

The RF signal is converted to a digital signal by the comparator and input to the controller, and sampling pulses Ⓒ and Ⓓ are created.

The sampling pulse outputs Ⓒ if a synchronizing signal is detected. That causes the previous track level to be held in S/H1, and outputs Ⓓ after a delay of two blocks. A difference in adjacent levels is held in S/H2, and the two different output signals are fetched as tracking error output. Tracking is performed by feedback of this error signal to the capstan motor.

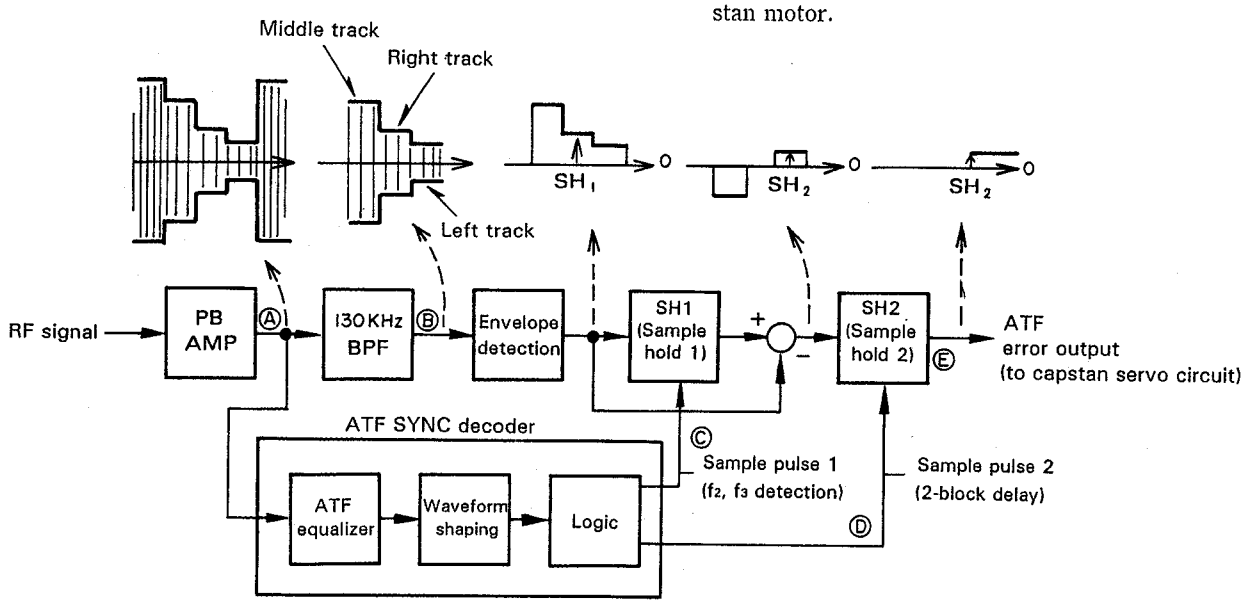


Fig. 1-8-1 ATF Block Diagram

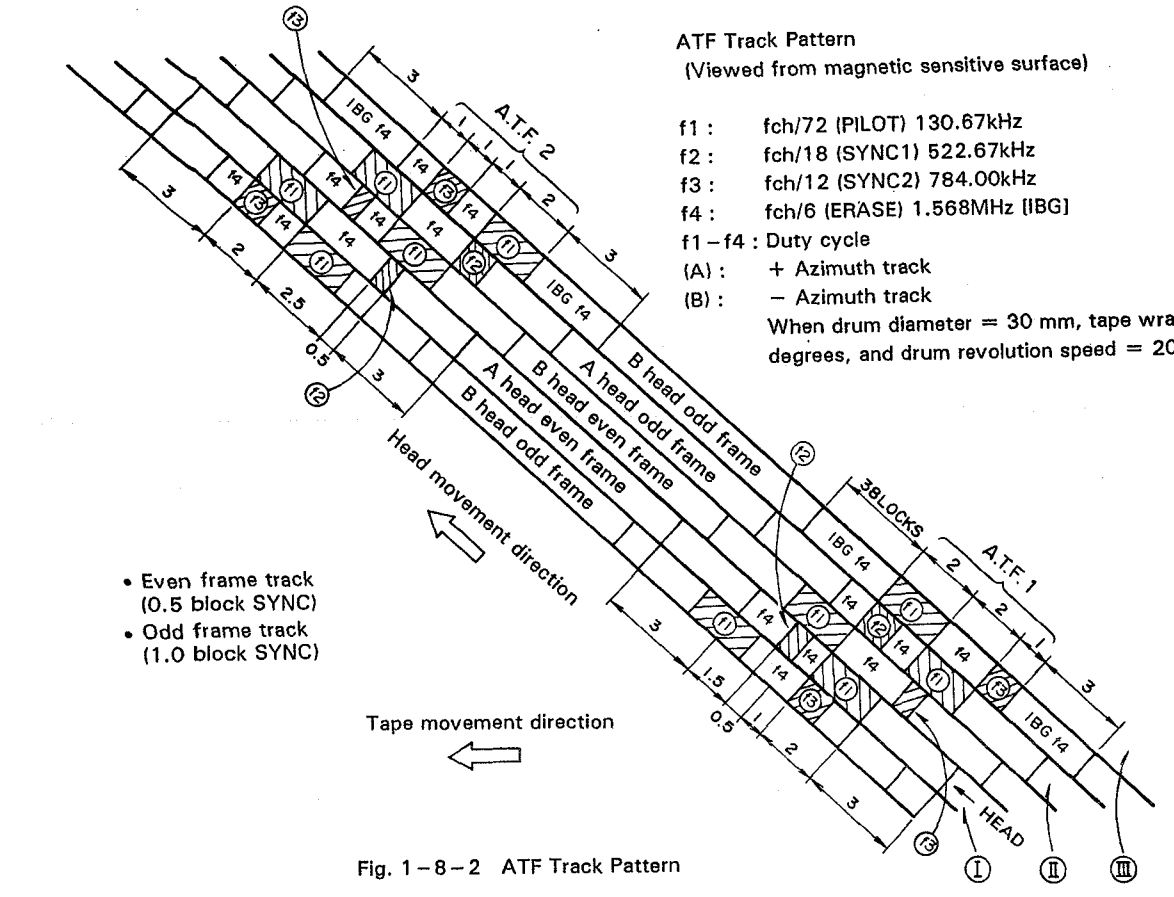


Fig. 1 – 8 – 2 ATF Track Pattern

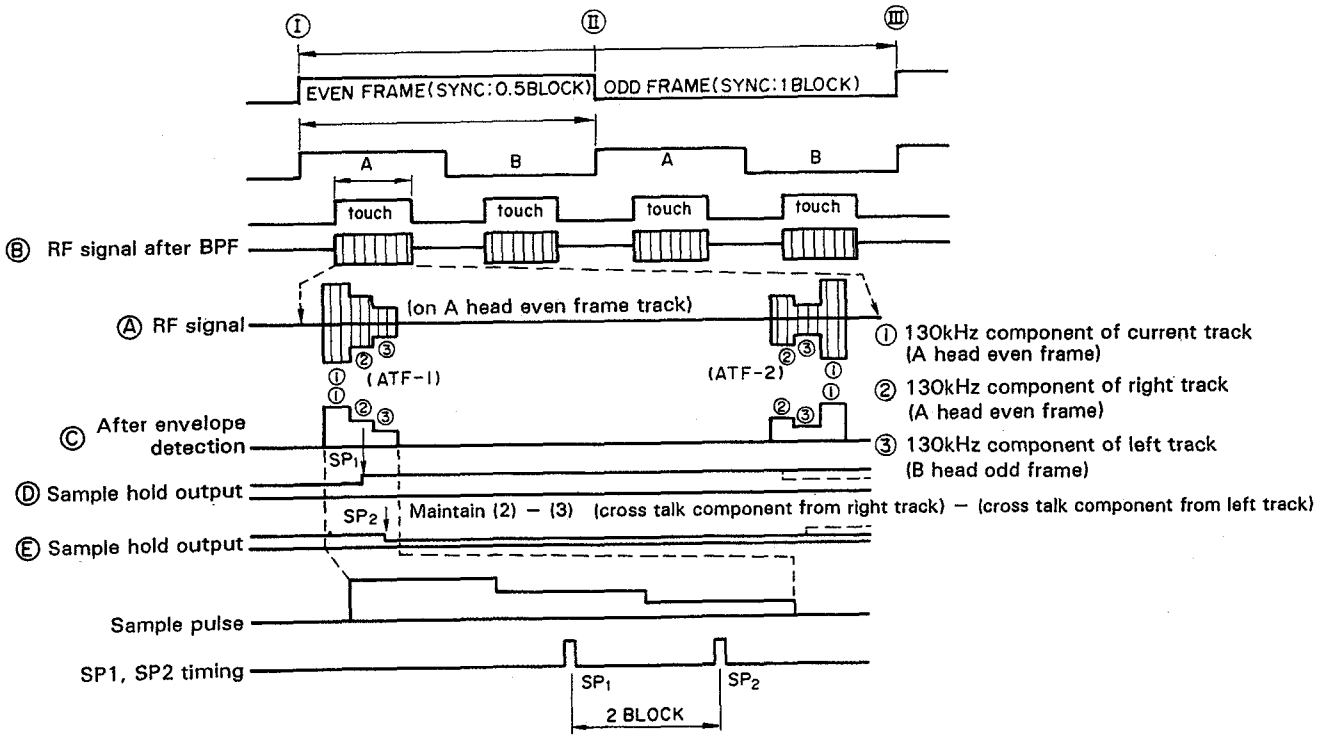
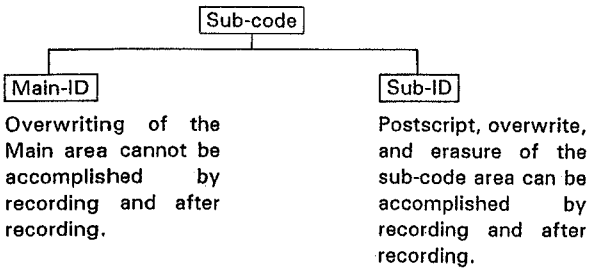


Fig. 1 – 8 – 3 Timing Chart

1.9 SUB-CODES

A major feature of digital audio tape lies in its ability to realize many functions through the use of sub-codes. There are essentially two types of sub-codes. There are sub-codes that are recorded in Main areas that record music signals, and sub-codes that are recorded in sub-code areas. Signals that are recorded in Main areas are control signals required for playback of Main signals, and they are simultaneously recorded along with music. Items recorded in a fixed sub-code area are recorded in a location separate from music signals and independently from the recording of music. This means that this portion can be recorded again or different control signals can be recorded or erased after music is recorded. Tune order and the beginning position of the tune can be recorded, and programmed play, direct selection, and many other functions can be incorporated. Additionally, program time, absolute time, running time (time code), TOC (program table of contents), calendars, catalogue numbers, and other information can be recorded. The capacity of this area is fairly large (4.6 times a compact disc) and there are many possibilities for adding new functions in the future.



● Status ID's

Generally, the codes shown below are recorded in the sub-ID. This sub-ID has the capacity to be overwritten and erased by after recording.

TOC-ID :

Indicates whether the program is registered in TOC.

START-ID :

A 9-second interval from the beginning of the tune is recorded, and it is used for finding the beginning of a tune during high-speed search. Unrecorded portions are automatically detected during recording and a flag can be set. However, a pianissimo passage in classical music may be judged as an unrecorded portion and the flag will be set within a tune.

Shortening ID :

Generally, the Shortening ID is called the skip ID. Control skips from the location where this ID is encountered and jumps to the next START-ID.

Priority ID :

The Priority ID determines whether a signal exists in the PNO-ID (program number) of the sub-code area. If a signal exists, the Priority ID gives the PNO-ID a priority code higher than the tune number of the Main area.

PNO-ID (program number) :

The PNO-ID is a code that indicates the recorded tune order. Generally, the PNO-ID and START-ID are recorded as a pair. The recorded order of tunes is lost if a new START-ID is created or an unnecessary ID is erased by after recording. The recorded order of tunes can be maintained using a renumbering function.

PNO-OEE :

PNO-OEE is a flag set at the end of a recorded portion that is used for end search. It is one element of PNO-ID.

● Sub-codes

The DAT format can record and playback information other than Main data as a sub-code (after recording).

● Main area

The Main-ID consists of ID1 through ID7, and it is recorded in the W1 area of the block format.
ID1 : Emphasis
ID2 : Sampling frequency
ID3 : Number of channels
ID4 : Number of quantization bits
ID5 : Track pitch
ID6 : Copy prohibit
ID7 : PACK data (see page 16)

Each of these codes consists of two bits, and they are recorded in the four bits of the W1 area of every other block (in even block address frames) as shown in Fig. 1-9-1. Therefore, the Main-ID is repeated and recorded 16 times in one track (128 blocks) because the same data is repeated once every eight blocks.

● Sub-code area

Sub-ID (the following four types exist)
① Control ID (4 bits)
② Data ID (4 bits)
③ Pack ID (3 bits)
④ Program number ID

Sub-code data
Different types of data can be recorded as a 64-bit (8 symbols) PACK.

[Main-ID]

ID-1 Emphasis
ID-2 Sampling Frequency
ID-3 Number of Channel
ID-4 Quantization
ID-5 Track Pitch
ID-6 Digital Copy
ID-7 Pack

[Control ID's within the sub-code ID]

TOC-ID	TOC recording (Y/N)
Start-ID	Tune start, tune end
Shortening-ID	Fast forwards to next START-ID when this ID is present
Priority-ID	Recorded tune order after recording (Y/N)

● Main-ID (W1/ID code in Main area) Contents

W1			W2 (Block address) 8 bits		
(2 bits)	(2 bits)	(4 bits)			
Format ID	Emphasis	※ Frame address	0	× × × ×	000
00 : For audio use 01 : For data use	00 : OFF 01 : ON (50/15μS)				
Reserved			0	× × × ×	001
Sampling frequency (Hz)	Number of channel	※ Frame address	0	× × × ×	010
00 : 48 kHz 01 : 44.1 kHz 10 : 32 kHz	00 : 2 CH 01 : 4 CH				
Reserved			0	× × × ×	011
Quantization	Track pitch	※ Frame address	0	× × × ×	100
00 : 16 bits uniform 01 : 12 bits non-uniform	00 : Normal track mode 01 : Wide track mode				
Reserved			0	× × × ×	011
Digital copy	Pack data	※ Frame address	0	× × × ×	110
00 : Permitted 10 : Prohibited 11 : Special	Pack contents				
Reserved			0	× × × ×	111

※Frame address (0000~1111, Factor of 16)
The two tracks of one interleave pair have the same frame address.

The Main-ID is repeated and the same data is recorded 16 times on one track because one group consists of a total of eight symbols.

[128 blocks (0000000~1111111) are included on one track]

Main area : 0
Sub-code area : 1

Fig. 1 – 9 – 1 Main-ID

● Sub-code ID

<table>
<tr><td colspan="4">Sub-code ID (W1)</td><td rowspan="2">4 bits</td><td colspan="3">W2</td></tr>
<tr><td colspan="4">4 bits</td><td>MSB</td><td>Sub-code ID (3 bits)</td><td>Block address (4 bits)</td></tr>
<tr><td colspan="4">Control ID</td><td>Data ID</td><td>MSB</td><td>Pack ID</td><td>×××0</td></tr>
<tr><td>Priority ID</td><td>Start ID</td><td>Shortening ID</td><td>TOC ID</td><td rowspan="2">0000</td><td rowspan="2">1</td><td rowspan="2">These three bits indicate the number of PACK's within two blocks.</td><td rowspan="2">The address is also 0000~1111 because there are 16 blocks in one track.</td></tr>
<tr><td>1 : Priority
0 : No priority</td><td>1 : Program start (9 seconds)
0 : Within the tune</td><td>1 : Skip
0 : OFF</td><td>1 : TOC
0 : OFF</td></tr>
<tr><td colspan="4">Program No. 2</td><td>Program No. 3</td><td>1</td><td>Program No. 1</td><td>×××1</td></tr>
</table>

Fig. 1-9-5 Sub-code ID

There are eight sub-code blocks before and after the ATF areas on one track. Like the Main block, 32 symbols of data and the parity are included in one block. One PACK consists of 64 bits (eight symbols) (see PACK FORMAT). Therefore, four PACK's are included in one sub-code block, and two blocks have a total of eight PACK's. Seven data items are included as a PACK because one block within a PACK is for the C1 error correction code. The PACK ID shows the number of PACK's actually recorded in the two blocks and the position.

Example :

P-ID = 001
(Pack ID)

<table>
<tr><td></td><td colspan="2">W1</td><td colspan="3">W2</td><td>Parity</td><td colspan="2">Data</td></tr>
<tr><td>SYNC</td><td>CONTROL ID</td><td>0000</td><td>1</td><td>001 (Pack ID)</td><td>×××0</td><td>Parity (8bits)</td><td>Pack-1</td><td>All "0"</td></tr>
<tr><td>SYNC</td><td></td><td></td><td>1</td><td></td><td>×××1</td><td>P</td><td colspan="2">All "0" / C1</td></tr>
</table>

P-ID = 110
(Pack ID)

<table>
<tr><td></td><td colspan="2">W1</td><td colspan="3">W2</td><td>Parity</td><td colspan="4">Data</td></tr>
<tr><td>SYNC</td><td>CONTROL ID</td><td>0000</td><td>1</td><td>110 (Pack ID)</td><td>×××0</td><td>P</td><td>Pack-1</td><td>Pack-3</td><td>Pack-5</td><td>All "0"</td></tr>
<tr><td>SYNC</td><td></td><td></td><td>1</td><td></td><td>×××1</td><td>P</td><td>Pack-2</td><td>Pack-4</td><td>Pack-6</td><td>C1</td></tr>
</table>

Fig. 1-9-6 Pack-ID

● PACK Format

A PACK consists of a total of eight symbols.

* ITEM (indicates contents of information included in a PACK)

Pack item	Contents	Remarks
0000	Reserved	
0001	Program time	Program number, index number and continuous time code within a program
0010	Absolute time	Program number, index number and continuous time code on a tape
0011	Running time	PC1, B3 = 0 : specified in this sub-clause for consumer use PC1, B3 = 1 : for professional use
0100	TOC	Table of contents
0101	Date	Year, month, day, the day of the week, hour, minute, second
0110	Catalog number	Catalog number of the cassette
0111	ISRC	The international Standard Recording Code
1000	Pro binary	For professional use
1001	Character	Character information
1010	Reserved	
1011	Reserved	
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	To be defined by pre-recorded tape manufactuturers

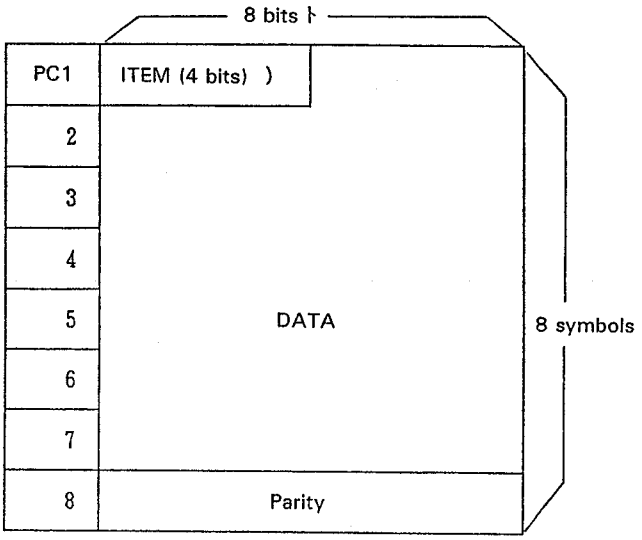


Fig. 1-9-7

● PACK in Main area

ID-7 (2 bits) of the Main-ID is PACK DATA, and the configuration of one PACK is shown below.

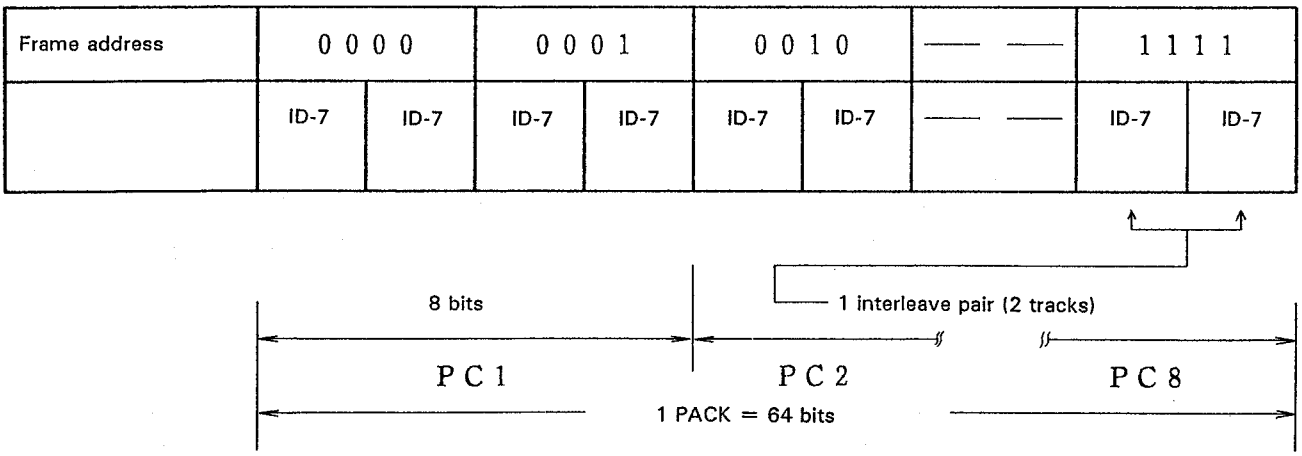


Fig. 1-9-8 PACK Format

The data of one PACK is recorded across 32 tracks in sections corresponding to frame addresses 0000 through 1111. ID-7 is recorded at block address 0 × × × × 110 (6 + 8n (n = 0 to 15)).

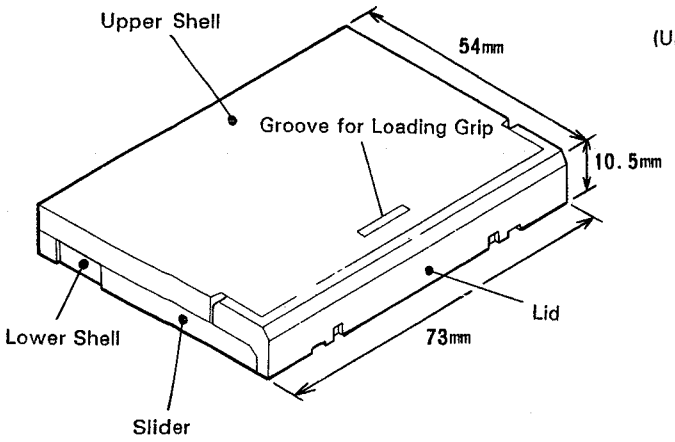
Stated differently, there are 16 occurrences of ID-8 on one track (block addresses 0 through 127). Therefore, 16 PACK's are formed by frame addresses 0000 through 1111 on 32 tracks.

The data for one PACK must be recorded in a minimum of two locations. Therefore, the data for block address 6 + 8n (n = 0 to 7) is also recorded at block address 6 + 8n (n = 8 to 15).

1.10 DAT CASSETTE STRUCTURE

The appearance of the cassette is shown in Fig. 1-10-1. The cassette dimensions are 73 mm (L), 54 mm (W), and 10.5 mm (H), which makes it considerably smaller than conventional compact cassettes.

Top View



Bottom View

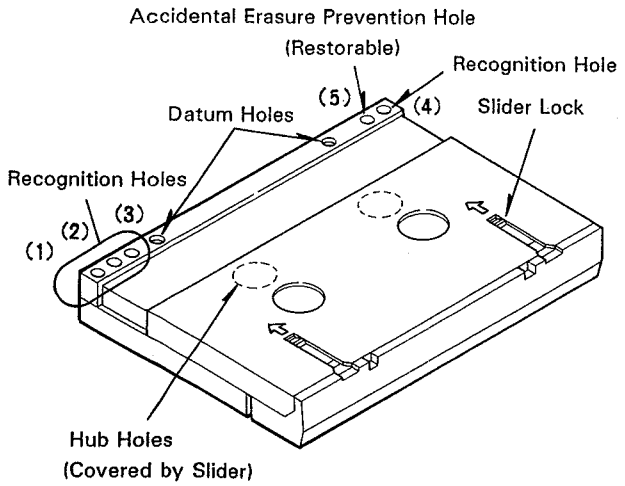


Fig. 1-10-1 Outside View of DAT Cassette

The DAT cassette has a lid to protect the tape. The lid and slider are shown in Fig. 1-10-1. The lid and slider are ordinarily closed to prevent dust and fingerprints on the surface of the tape. Additionally, the cassette is engineered so that the brake does not make contact with the reel and slackness in winding does not occur when the lid and slider are closed. The quality of the metal tape is higher than the metal tape of audio cassettes and magnetic materials are employed to allow high density recording.

The dimensions of DAT cassettes and other types of cassettes are compared in Fig. 1-10-2.

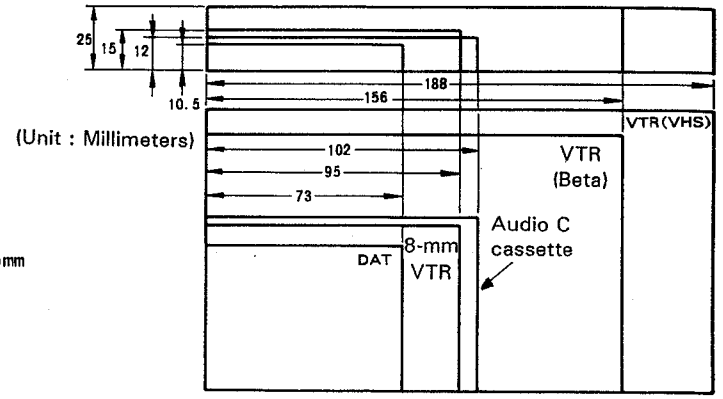


Fig. 1-10-2 Comparison of Dimensions for DAT Cassettes and other Cassettes

A prism is integrated into the DAT tape cassette. As shown in Fig. 1-10-3, light from an external LED strikes the prism integrated into the cassette. In the transparent portion of the leader tape, the reflected light from the prism is radiated onto a phototransistor and the beginning or end of the tape can be detected. Tape end detection is performed to prevent the tape from breaking when winding at high speed, and the brake is immediately applied when the tape end is detected. Additionally, chrome tape, barium ferrite, and other materials with excellent properties are being investigated even though their coercive force is limited in prerecorded tapes due to contact printing.

There are five types of recognition holes in a DAT cassette as shown in Fig. 1-10-1. Recognition holes to prevent recording work the same way as those of conventional cassettes. However, the DAT cassette also has other types of exclusive recognition holes (see Fig. 1-10-4). Recognition hole (5) indicates whether or not recording is possible.

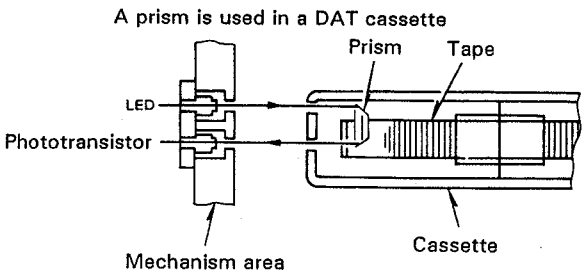


Fig. 1-10-3 Tape Beginning and End Detection Method for Digital Audio Tape

"1" : Open "0" : Closed

Recognition Hole (1)	Recognition Hole (2)	Recognition Hole (3)	
0	0	0	Metal tape or equivalent product/tape thickness 13μm
0	1	0	Metal tape or equivalent product/thin tape
0	0	1	Track pitch 1.5×/tape thickness 13μm
0	1	1	Track pitch 1.5×/thin tape
1	×	×	(Reserved)

Recognition Hole (4)	
1	Prerecorded tape
0	Non-prerecorded tape (Conventional tape for recording and playback)

Recognition Hole (5)	Original condition can be restored by opening or closing the slider
1	Recording impossible
0	Recording possible

Fig. 1-10-4

Conventional audio cassettes allow prevention of accidental erasures by breaking off a tab on the back of the cassette. However, this is not convenient because the original condition cannot be restored once the tab is broken. The DAT cassette has improved this system by allowing and preventing recording by opening and closing a control on the back of the cassette (see Fig. 1-10-5).

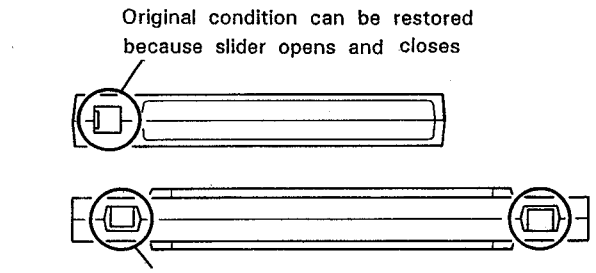


Fig. 1-10-5 Accidental Erasure Prevention Holes of C Cassette and DAT Cassette

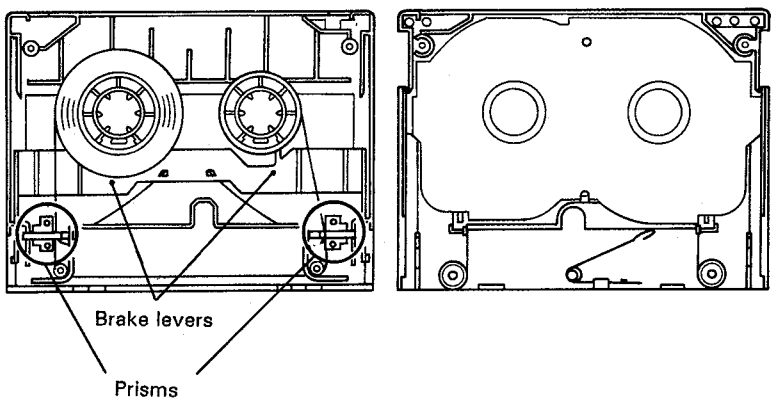


Fig. 1-10-6 DAT Cassette Interior

2. CIRCUIT DESCRIPTION

●Serial Copy Management System (SCMS) Overview

The new system, which is called the Serial Copy Management System, digitally controls serial copy. DAT's equipped with this system have the following features :

- Digital copy can be accomplished regardless of the copy prohibit code and sampling frequency (32, 44.1, and 48kHz).
- Digital copy can be accomplished from CD's, DAT music tapes, and other digital sources that are copyrighted. However, it is not possible to make another digital copy from a copied tape (see Fig. 1–a).
- Broadcast satellite (BS), digital microphone, and other digital signals not having copy prohibit codes have no particular limitations. Therefore, digital copy can be freely accomplished (see Fig. 1–b).
- Copy prohibit codes do not exist in analog signals. Therefore, copy is possible. Regardless of its contents, a copied tape can be used as a DAT music tape that has a copy prohibit code. Because there is no identification system for determining the existence or nonexistence of a copyright, digitally recorded tapes of analog signals can be used again to make more digital copies. However, those tapes cannot be copied to again. This means that once signals that have passed through an analog-to-digital converter have been recorded on digital audio tape, the recorded tape becomes a DAT music tape with a copy prohibit code (see Fig. 1–d).
- Separate analog-to-digital converters and other general category products can accomplish digital copy up to two times from original digital sources, like the above copy from analog signals. Digital copy cannot be accomplished more than twice due to the limitations imposed by the specifications (see Fig. 1–c).

● Digital Source

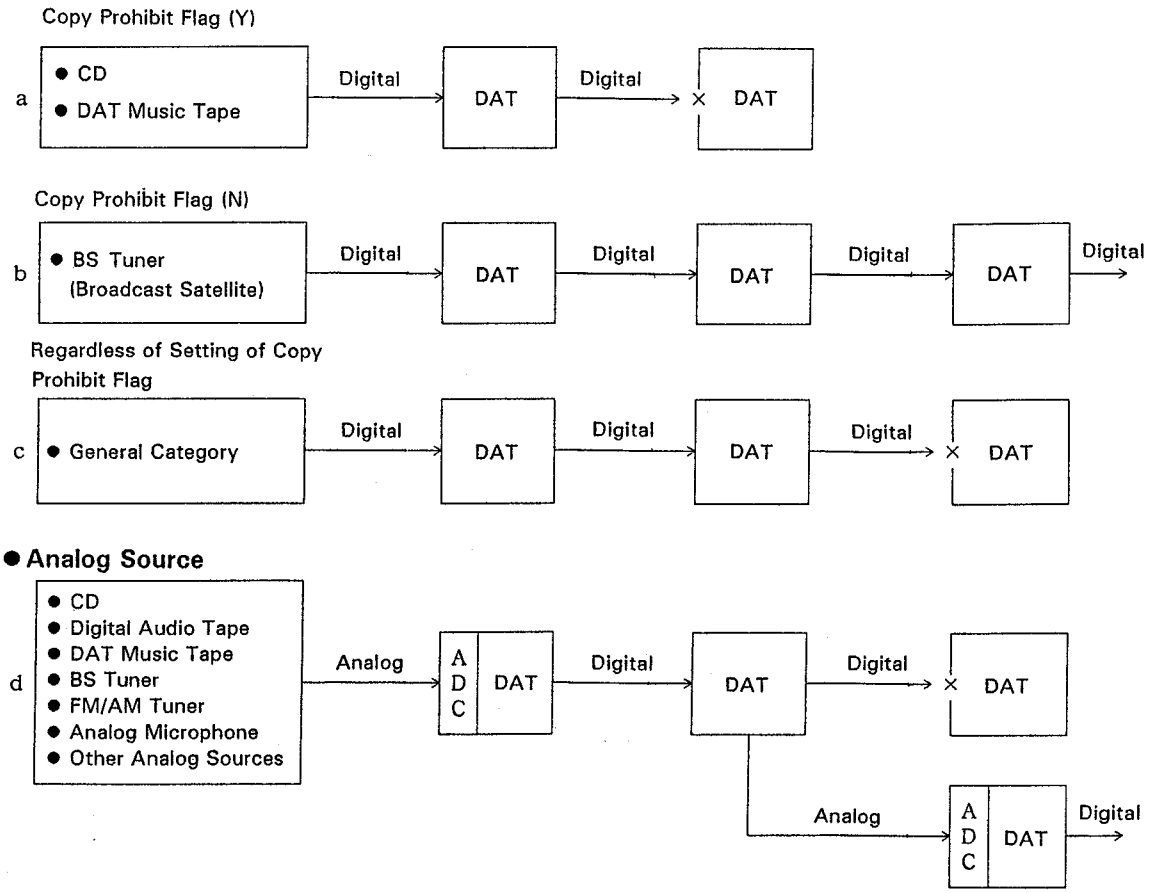


Fig. 1 Serial Copy Management System
(Handles fs = 32kHz, 44.1kHz, and 48kHz)

●SCMS Details

The determination of whether or not copy can be accomplished using SCMS is performed by the 2-bit copy prohibit code recorded on the digital audio tape and the copy prohibit bit and category code defined by the digital I/O interface. The copy prohibit code within the DAT format uses the two bits of ID6 of MAIN ID. In the past, the two choices of "copy permitted" (00) and "copy prohibited" (10) were defined. The choice of "special copy" (11) has been newly added, and digital copy from tapes recorded with this code can be accomplished for one generation only (see Fig. 2).

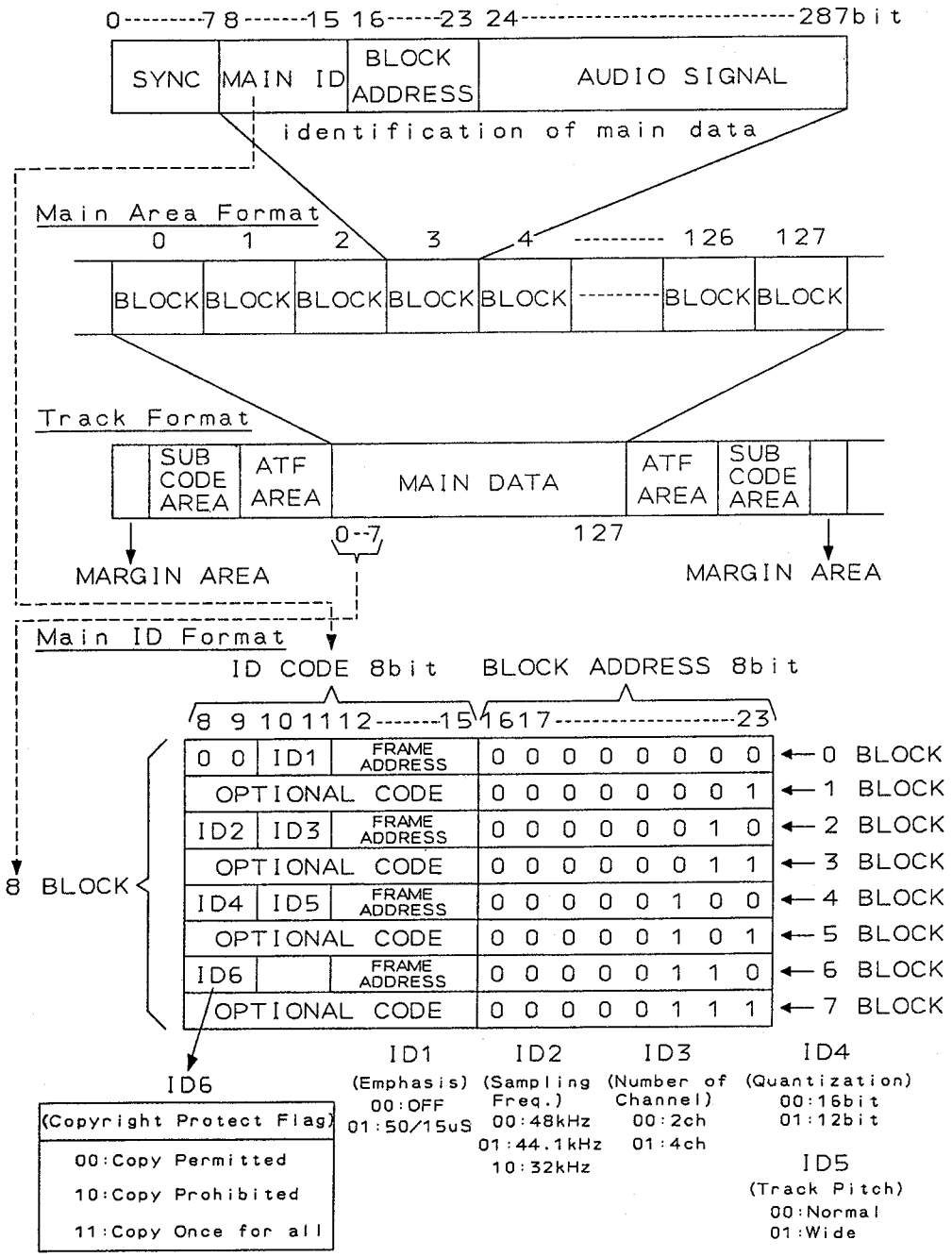


Fig. 2 DAT Recording Format

The copy prohibit bit within the subframe format of the digital I/O format assumes the setting (copy prohibited "0" and copy permitted "1") within the channel status. The category code defines General (00000000), Main Processor (01000000), CD Player (10000000), DAT (11000000), or the new DAT-P (11000001). Accordingly, digital audio tapes without copyrights and DAT music tapes have been separated (see Fig. 3).

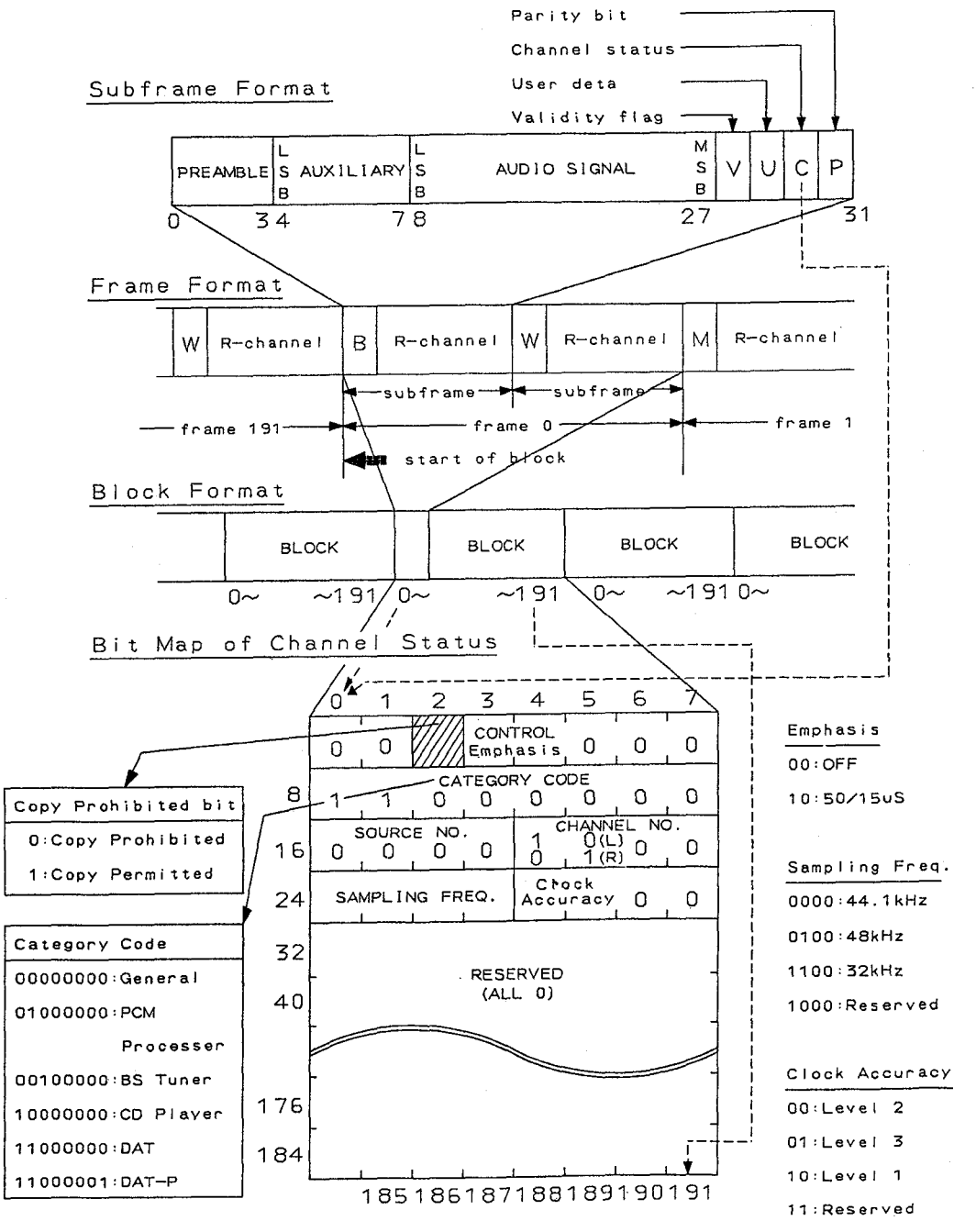


Fig. 3 Digital-Audio Interface

Using a compact disc (CD) as an example, the copy prohibit bit of the CD digital output signal is "0" (copy prohibit). "10000000" is output because the category code is "CD Player", and this code is input to the DAT.
Copy is prohibited at this time because the copy prohibit bit is "0", but recording is possible because the category code is "CD". The copy prohibit code of "10" is recorded on the tape in ID6 when the DAT records this code. Then, the copy prohibit bit of the DAT's digital output is "0", and the category code changes to "11000000". Attempts to record this tape to another DAT will fail because the copy prohibit bit is "0" and the category code is "DAT". The copy prohibit bit is generally "1" for broadcast satellite (BS) tuners and the copy prohibit code of the DAT is "00". Therefore, digital copy is possible any number of times, regardless of the category code. The copy prohibit bit is "0" for DAT music tapes and the category code is "11000001" (DAT-P). Therefore, digital copy can be accomplished only once like CD's.

The products which output the general category have copy prohibit bits of "0" and "1" and the category code is "00000000". Therefore, "11" is recorded on the digital audio tape and digital copy is possible twice. When there are analog input signals, "11" is recorded on the digital audio tape. Therefore, digital copy from an analog source is possible twice (see Fig. 4).

Product Item		CD	DAT Music Tape	BS Tuner	General Category	Analog Input (CD, DAT, BS Tuner)	Number of Times
Digital Input	Copy Prohibit Bit	0	0	1	0 or 1	———	
	Category Code	10000000	11000001	00100000	00000000	———	
		⇩	⇩	⇩	⇩	⇩	
When Recording	Copy Prohibit Code (ID6)	10	10	00	11	11	1st Time
		⇩	⇩	⇩	⇩	⇩	
Digital Output	Copy Prohibit Bit	0	0	1	0	0	
	Category Code	11000000	11000000	11000000	11000001	11000001	
		⇩	⇩	⇩	⇩	⇩	
When Recording	Copy Prohibit Code	Copy Impossible	Copy Impossible	00	10	10	2nd Time
				⇩	⇩	⇩	
Digital I/O	Copy Prohibit Bit	———	———	1	0	0	
	Category Code	———	———	11000000	11000000	11000000	
				⇩	⇩	⇩	
When Recording	Copy Prohibit Code	———	———	00 (possible any number of times)	Copy Impossible	Copy Impossible	3rd Time

Fig. 4 Code Transition Table by Product Item

3. TROUBLESHOOTING

Symptom	Cause	Remedy
1. Power is not turned ON.	① Fuse FU1 has blown. ② Fusible resistor R500 has blown. ③ CN13 is disconnected.	
2. Power is turned ON, but the FL display has a failure.	① CN13 is disconnected. ② Crystal resonator X502 (49MHz) is not oscillating. ③ IC503 is not reset during power ON. ④ IC1201 is not operating.	→ Check the signal is input to IC501 pin64. → Check IC503 pin32 ("L" during power ON).
3. Cassette tray is not open/closed.	① Cassette installation unit does not correctly engage with the door section. ② Motor is not rotating. ③ Motor is rotating reverse. ④ IC508 is faulty.	→ Check CN07. → ● Check IC508. ● Check SW2001 and SW2002 of the cassette installation unit. → Check IC508.
4. Tape is not loaded.	① Cassette tape is not detected. ② END sensor is faulty. ③ Check for dust in the mechanical arm section. ④ Motor is not rotating. ⑤ IC508 is faulty.	→ ● Check CN05. ● Check S101 in the mechanical system section. → Check CN19 – 5 is 1.6Vp – p or less while the cassette tape is loaded. → Check CN06 → Check IC508
5. Drum cannot be controlled.	① Connectors are disconnected. ② IC503 is not operating. ③ IC506 is faulty.	→ Check CN03. → ● Check IC503 is reset during power ON (pin32). ● Check the clock signal (9.4MHz) is input to pins 35 and 61. → Check IC506.
6. Tape stops with error indication.	① Tape is caught due to condensation. 《Error during playback》 ① Capstan rotates, but the reel does not. ② IC503 does not detect the reel FG (RFGT – pin55). ③ Drum FG (D – FG) has a failure. 《Error in the tape top section》 ① Tape top sensor is faulty. 《Other》 ① Mechanical system section has a failure.	→ Mechanical system section has a failure. → ● Check CN05. ● Check the RFGS and RFGT amplifier circuit sections. → Check the D – FG generating circuit sections, IC509 and IC510. → Check CN19 – 4 is 1.7Vp – p or more in the tape top section. → Replace the mechanical system section.

Symptom	Cause	Remedy
7. Playback cannot be performed.	《Neither level meter nor A-Time are displayed or sound is interrupted.》 ① Head cannot read correctly. Check the RF waveform. ② ATF is not activated. ③ Drum servo is not locked. 《Only fs = 44.1kHz is not reproduced.》 ① Crystal resonator X901 (22MHz) is not oscillating. 《Level meter is active, but no sound is generated.》 ① IC904 and IC907 are faulty.	 → Clean the head with the head cleaning tape. → ● Check CN08. ● Check the D-FG and C-FG. → ● Check IC503 pin60 DREF inputs the signal. ● Check D-PG. ● Check X501 (18MHz) is oscillating.
8. Data can be reproduced, but cannot be recorded.	《Analog recording》 ① Connectors are disconnected. ② IC903 is faulty 《Digital recording》 ① Check data is input to IC501. ② PLL is not operating.	 → Check CN15 and CN16. → Check IC903. → Check data is input to IC501 pin52 Rx. → Check the clock signal is input to IC501 pin48 PLCo. Check for oscillation output on IC517 pin12.
9. Other failure or failure by unknown cause.	① Check the waveform of each section listed in the service manual. ② Adjust the waveform.	