





ORDER NO. CRT1055

COMPONENT CAR STEREO COMPACT DISC PLAYER





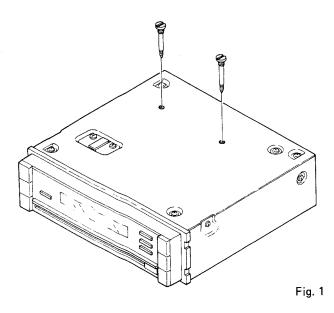
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• CD Player Service Precautions

1. Since this screw protects the mechanism during transport, be sure to affix it when it is transported for repair, etc.



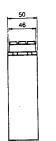
- 2. For pickup unit (CGY1001) handling, please refer to "Disassembly" (Fig. 13). During replacement, handling precautions shall be taken to prevent an electrostatic discharge (protection by a short pin).
- 3. During disassembly, be sure to turn the power off since an internal IC might be destroyed when a connector is plugged or unplugged.

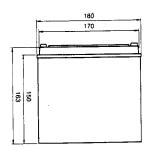
1. SPECIFICATIONS

General
System Motor vehicle compact disc digital audio system
Disc Diameter: 120 mm
Thickness: 1.2 mm
Maximum playing time: Over 60 minutes (stereo)
Linear velocity: 1.2 - 1.4 m/sec.
Rotation direction: Counterclockwise
Signal format Sampling frequency: 44.1 kHz
Number of quantization bits: 16; linear
Transmission bit rate: 4.3218 Mbit/sec.
Modulation system: EFM
Error correction system: CIRC
Pre-emphasis: 50/15 μsec.
Laser
Power requirements14.4 V DC (10.8 – 15.6 V possible)
Power consumption
Maximum power consumption 16 W
Weight
Dimensions

Αι	ıdi	C

Frequency characteristics $5 - 20,000 \text{ Hz}$ (±1 dB)
Signal-to-noise ratio 90 dB (1 kHz) (IEC-A network)
Dynamic range
Wow and flutter Below measurement range
Distortion factor 0.005% (1 kHz, 0 dB)
Output voltage
Number of channels





Note:

Specifications and the design are subject to possible modification without notice due to improvements.



2. SAFETY INFORMATION

- 1. Safety Precautions for those who Service this Unit.
- Follow the adjustment steps (see pages 78 through 85) in the service manual when servicing this unit. Whe checking or adjusting the emitting power of the laser diode exercise caution in order to get safe, reliable results.

Caution:

- 1. During repair or tests, minimum distance of 13cm from the focus lens must be kept.
- 2. During repair or tests, do not view laser beam for 10 seconds or longer.
- 2. A "CLASS 1 LASER PRODUCT" label is affixed to the bottom of the player. (Fig. 2)
- Two screws are affixed to the bottom of the unit to secure the mechanism during transport. Be sure to remove these screws before installation of the player. (Fig. 2)

3. The triangular label is attached to the mechanism unit plate unit (Fig. 3)

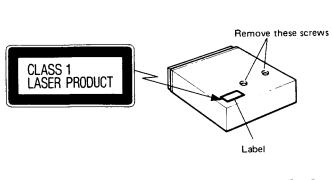


Fig. 2

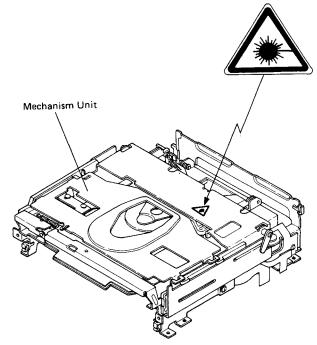


Fig. 3

4. Specifications of Laser Diode

Specifications of laser radiation fields to which human access is possible during service.

Wavelength

780 nanometers

Radiant power

55.3 microwatts

(Through a circular aperture stop having a diameter of 80 millime-

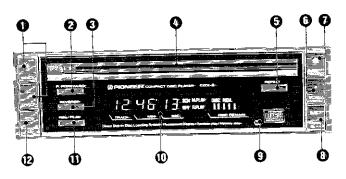
ters)

0.44 microwatts

(Through a circular aperture stop having a diameter of 7 millimeters)



3. NAME OF PARTS AND THEIR FUNCTIONS



Track Number Search Button

Press to search for a specific selection (track number). Each press of the (+) side increases the displayed track number, while pressing the (-) side decreases the number. Holding down either side of this button causes the displayed number to successively change at high speed.

2 Fast Forward Button

Press to advance the present selection at high speed. Play resumes when the next selection (track number) is reached. Holding down the button causes fast forward to continue even after the next selection is reached.

Reverse Button

Press to reverse the present selection at high speed. Play resumes when the beginning of the present selection (track number) is reached. Holding down the button causes reverse to continue even after the beginning of the present selection is reached.

Disc Insert Slot

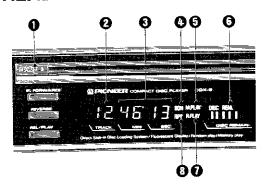
Discs are loaded into the unit with the label on the disc facing up. Once a disc is inserted into the disc insert slot, it is automatically set and play begins.

 Turn the cassette deck power switch or the tuner power switch to the OFF position.

6 Music Repeat Button

Press to repeat the current selection a number of times. Either the release button or the music repeat button can be used to cancel the music repeat operation once it is activated. All selections on a disc are continuously played when the music repeat function is not activated.

4. READING THE DISPLAY



1 Disc Set Display

Lights when a disc is set in the unit.

Track Display

Indicates the track number of the selection being played. Also shows the total number of tracks included on a disc for approximately five seconds after the disc is loaded into the unit.

Play Time Display

Indicates the elapsed play time of the selection being played. Also shows the total play time for a discs for approximately five seconds after the disc is loaded into the unit.

6 Track Scan/Memory Button

Press once to play the beginning (approximately 10 seconds) of each selection from the current selection (track scan). Pressing again during track scan records the number of the current selection in memory (scan memory) for playback during memory play.

Track Scan

Press to play the beginning (approximately 10 seconds) of each selection in order. Pressing the release button when the desired selection is found releases track scan and returns to normal play. Track scan is automatically released and normal play resumes when the selection during which track scan was originally selected is reached again.

Scan Memory

Press during play of the beginning (approximately 10 seconds) of a selection to record the selection in memory. Up to eight selections can be stored in memory.

 Up to eight selections can be stored in memory. A beep is heard when the memory button is pressed to indicate a full memory. Storing a selection in memory automatically deletes any selection previously stored.

Eject/Reload Button

Press to eject a disc from the unit. Pressing again reloads the disc into the unit.

Memory Play Button

Press to play the selections stored in the scan memory.

Clear Button

Press with a thin pointed object when the effects of noise on the built-in micro computer make it impossible to turn the power of the unit ON, cause other buttons to become inoperative or results in an abnormal display.

Display

Release/Play Button

Press to cancel track scan, music repeat, fast forward, and reverse. Also suspends operation during random play, memory play, and play. Pressing again resumes play from the spot where it was originally suspended.

1 Random Play Button

Press to cause random selection and play from among the track numbers stored in the micro computer.

4 Track Scan Display

Lights when the track scan/memory button is pressed and remains lit while the track scan/memory functions are in operation.

6 Memory Play Display

Lights when the memory play button is pressed and remains lit while the memory play function is in operation. This indicator will not light and memory play will be impossible when there is nothing stored in memory.

6 Disc Remain Display

Indicates the total play time remaining on the disc being played.

Random Play Display

Lights when the random play button is pressed and remains lit while the random play function is in operation.

8 Music Repeat Display

Lights when the music repeat button is pressed and remains lit while the music repeat function is in operation.

- A built-in function protects the semiconductor laser from damage by automatically suspending play when the ambient temperature of the unit exceeds a certain level. This condition is indicated by ∃∃∃ ∃∃being shown on displays ② and ③. The disc should be ejected and the unit should not be used until the ambient temperature is reduced.
- When a space of a few seconds exists between the selections of the disc being used, ③ will show - □□□□□□ when the spaces are passed.



5. OPERATION

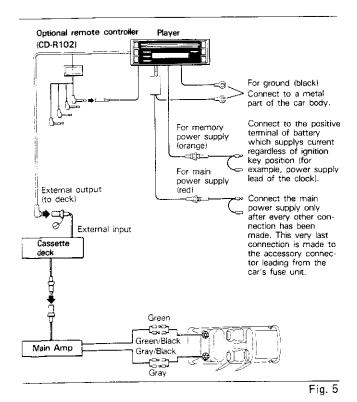


- Turn the cassette deck power switch or the tuner power switch to the OFF position.
- 1. Load a disc into the disc insert slot 10 with the label on the disc facing up. Once a disc is inserted into the unit, it is automatically set and play begins. (The total number of selections on the disc and total disc play time will appear on the display for approximately five seconds.)
- 2. Set the volume, balance, bass and treble to the desired level using the cassette deck controls.

6. CONNECTION

- · Before making final connections, make temporary connections then operate the unit to check for any connecting cord problems.
- Refer to the instruction manual for details on connecting the various cords of the deck and main amp then make connections correctly.
- Be sure to correctly connect the memory power supply lead (orange) and main power supply lead (red) as specified. If the connections are made incorrectly or forgotten, this unit will not work at all.
- Don't pass the memory power supply lead through a hole into the engine compartment to connect to the battery. This will damage the lead insulation and cause a very dangerous short.
- If you should encounter more than two lead wires of the same color, when wiring connections, it will be convenient to wire them together, as shown in the following diagram.

Example wiring with component car stereo cassette deck.

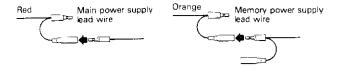


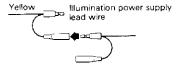
· A short period of time will pass from when the disc is loaded to the point at which play begins. This "setting" time is required to allow the unit to begin reading the digital signals on the disc. The cassette tape deck and tuner can be used while a disc is in the set position. DISC SET 4 is illuminated on the display while a disc is set. Note that attempting to load another disc while one is already set can damage

3. Press the release/play button 2 to stop play without ejecting the disc.

Pressing the release/play button again will resume play from the point at which it was stopped. Press the eject/reload button 3 to stop play and eject the disc. Pressing the eject/reload button while the disc is still in the ejected position will reload the disc and resume play from

the discs and cause malfunction. Never attempt to load two discs at the same time. This can cause serious malfunction of the unit.





the first selection.

Fig. 4

Example wiring with CENTRATE component car stereo cassette deck.

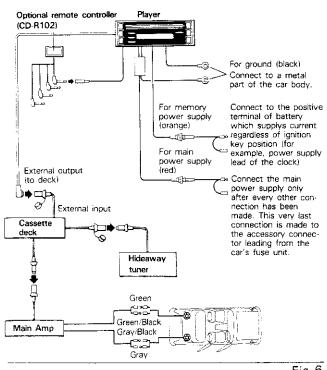


Fig. 6



7. PARTS LOCATION

NOTE:

- For your parts Stock Control, the fast moving items are indicated with the marks $\star\star$ and \star .
 - * *: GENERALLY MOVES FASTER THAN *.

This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

 Parts marked by "

" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.



Fig. 7

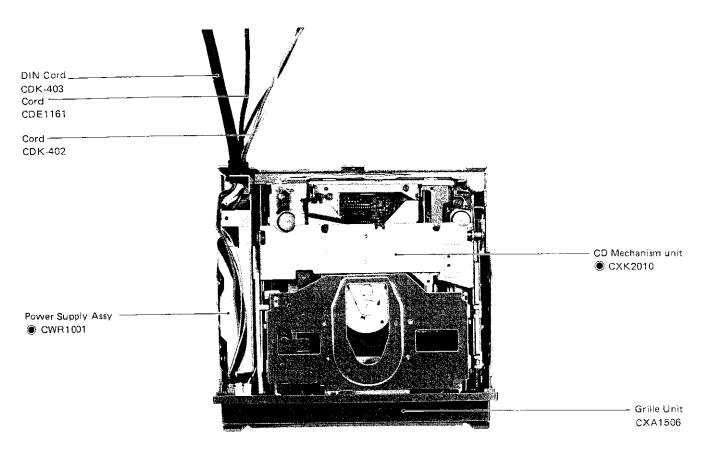


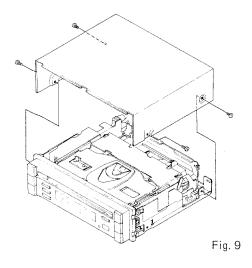
Fig. 8



8. DISASSEMBLY

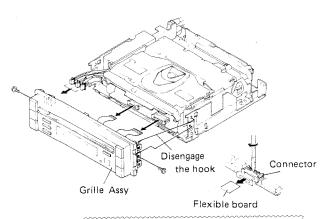
• Case Removal (Fig. 9)

1. Remove 4 screws, then remove the case.



• Grille Assy Removal (Fig. 10)

- 1. Remove 2 screws and release 4 catches, then remove the grille assembly.
- 2. Remove 5 connectors.



Insert a (-) screwdriver and turn it in the arrow direction, then two connector catches come off and the flexible circuit board can be removed.

Fig. 10

• Display Unit Removal (Fig. 11)

- 1. Crush the holder (Fig. 11) by using pliers to allow the circuit board to be lifted.
- 2. Remove 6 screws, then remove the display unit.

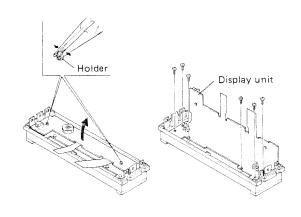


Fig. 11

• Chassis Removal (Fig. 12)

- 1. Turn the set the other way.
- 2. Remove 8 screws, then remove the chassis.

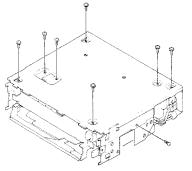


Fig. 12



• Mechanism Unit Removal (Fig. 13)

- 1. Remove 4 screws.
- 2. Remove 5 connectors.

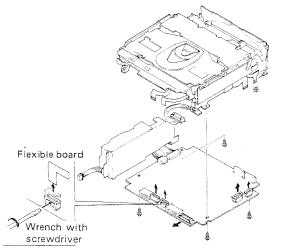
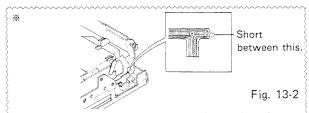


Fig. 13-1

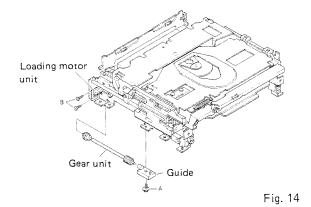


When this connector (CN2, wiring to the semi conducter laser) is removed because the mechanism has to be removed, be sure to apply a shorting pin or short between the patterns with a jumper before removal.

When it is reconnected, connect it to the connecter, then remove the shorting pin or jumper.

• Loading Motor Unit Removal (Fig. 14)

- 1. Remove the screw (M2.6 x 4) at A, then remove the guide and gear unit.
- 2. Remove 2 screws (M2 x 2.5) at B, then remove the loading motor unit.



• Clamper Plate Unit Removal (Fig. 15)

- 1. Remove 1 screw (M2 x 4) at P, then remove the flexible circuit board (to prevent circuit board cutting).
 - * To tighten the screw at P, use a screw tightener.
- 2. Remove 2 screws (M2.6 x 4) at C, then remove a bracket.
- 3. Remove 1 screw (M2.6 x 4) at D, then remove a bracket (for a switch).
- 4. Remove the clamper plate unit toward the back as shown by an arrow while avoiding arm E and plate Q.

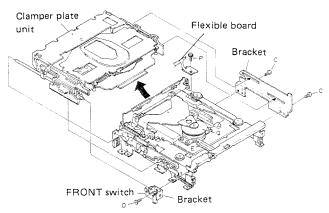
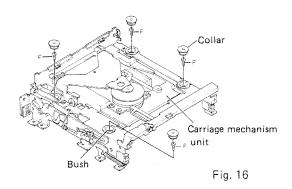


Fig. 15



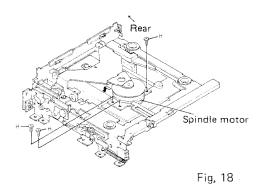
Vibration Proof Rubber (Bush) Removal (Fig. 16)

- 1. Remove the collar, then remove 4 screws (M2.6 x 5) at F
 - * Use a tightener to tighten the screw at F.
- 2. Remove the carriage mechanism unit.
- 3. Remove the bushing toward the bottom.



Spindle Motor Removal (Fig. 18)

- Lower the pickup unit toward the back. (It can be shifted manually if shaft deviation is performed as shown in Fig. 19.)
- 2. Remove 3 screws (M2.6 x 4) at H, then remove the spindle motor as shown by an arrow.



• Carriage Mechanism Unit Removal (Fig. 17)

- 1. Turn the mechanism the other way.
- 2. Remove 2 screws (M2.6 x 5) at G, then remove the carriage mechanism unit as shown by an arrow.
 - * Use a tightener to tighten the screws at G.

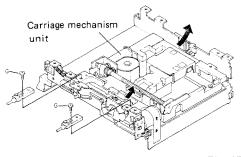
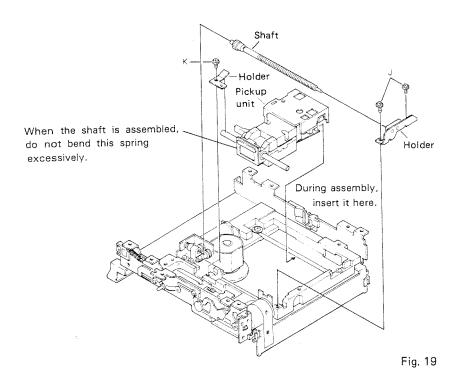


Fig. 17



• Pickup Unit Removal (Fig. 19)

- 1. Turn the mechanism the other way.
- 2. Remove 2 screws (M2 x 4) at J, then remove the holder shaft
- 3. Remove 1 screw (M2 x 4) at K, then remove the holder.
- 4. Remove the pickup unit.



• Carriage Motor Unit Removal (Fig. 20)

1. Remove 2 screws (M2 x 4) at L and 1 screw (M2 x 4) at M, then remove the carriage motor unit.

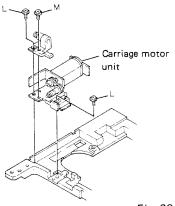
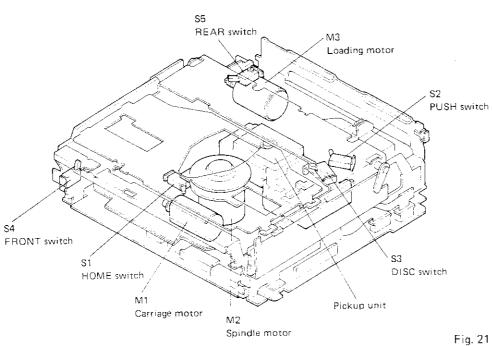


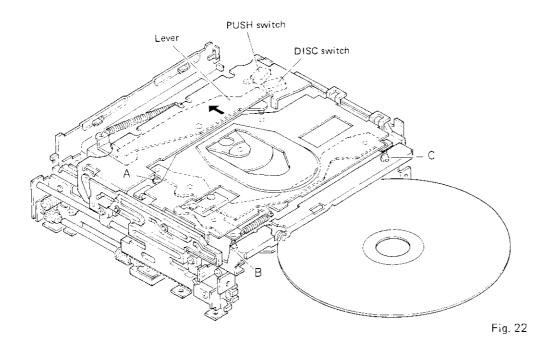
Fig. 20



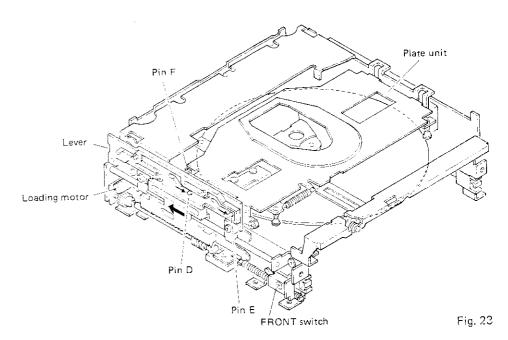
9. MECHANISM DESCRIPTION



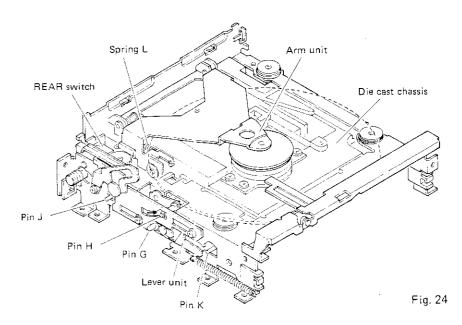
- When a disc is inserted, it is supported at point A, B and C. At the same time, a lever moves toward the arrow direction and the DISC switch is opened (Fig. 22).
- When the disc is pushed further, a PUSH switch is turned on and the loading motor rotates to start loading (Fig. 22).



- 3. A lever and plate unit are shifted toward the arrow direction, then the FRONT switch is opened (Fig. 23).
- 4. When the center of the disc comes to the spindle motor, plate unit movement toward the back is terminated and it is then shifted down by the pins of D and E (Fig. 23).
- 5. A lever moves further toward the back which widens point A, B and C (Fig. 22) using pin F and frees the disc (Fig. 23).



6. A lever unit is moved toward the back by pin G the same as the lever. An arm unit presses the spindle motor shaft with spring L because pin H moves in the arrow direction, then a magnet holds the disc. After this, pin J and K become free and the die cast chassis becomes vibration proof. Also, the REAR switch is turned on and the loading motor stops to complete the loading operation (Fig. 24).





10. CIRCUIT DESCRIPTION

Block Diagram

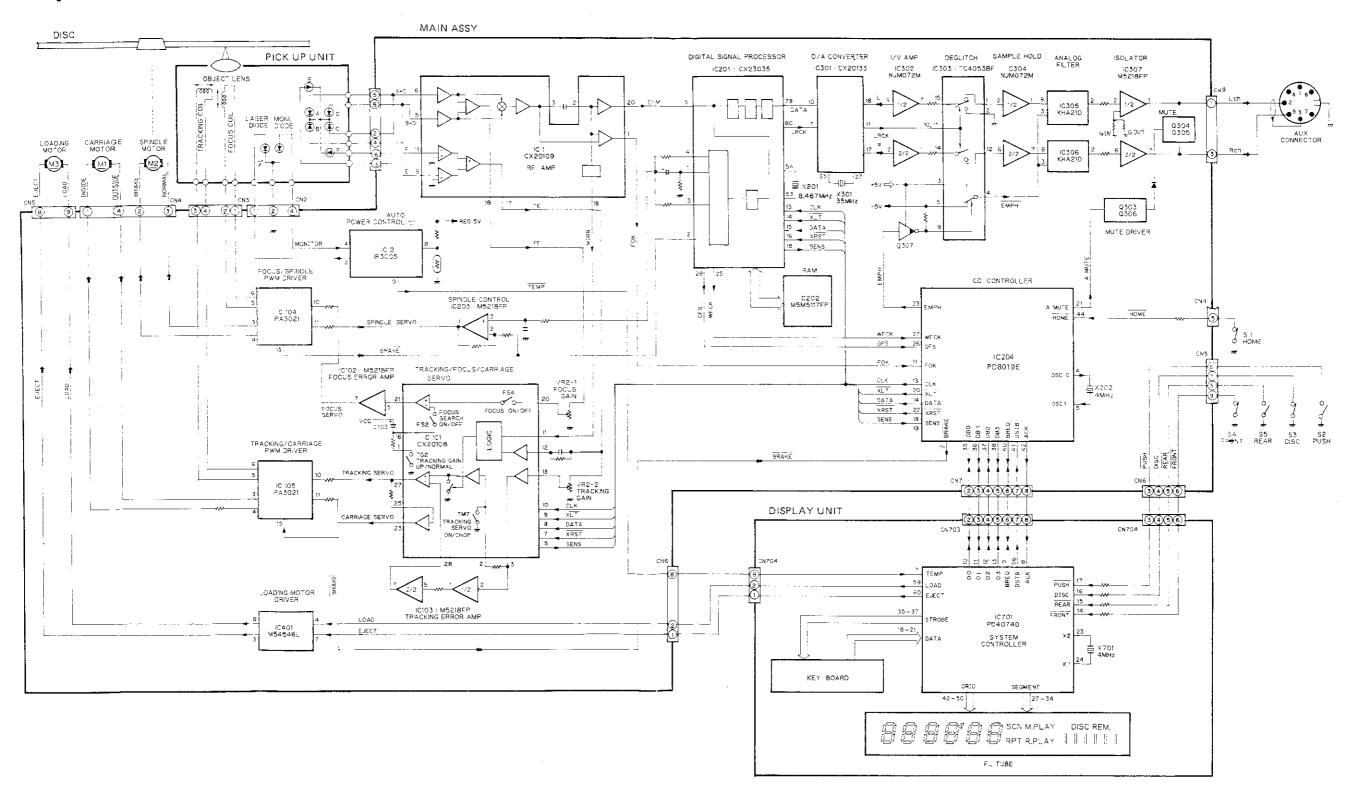
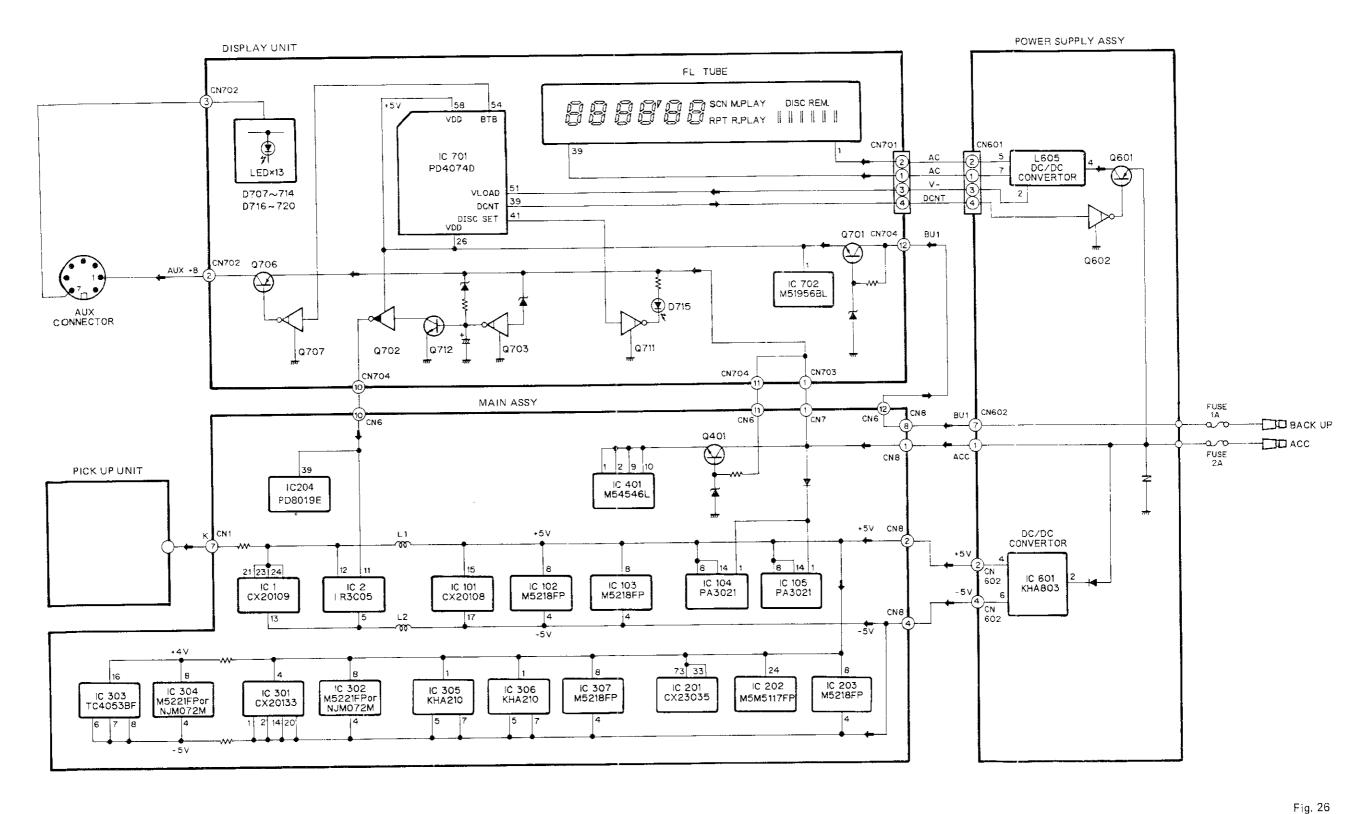


Fig. 25

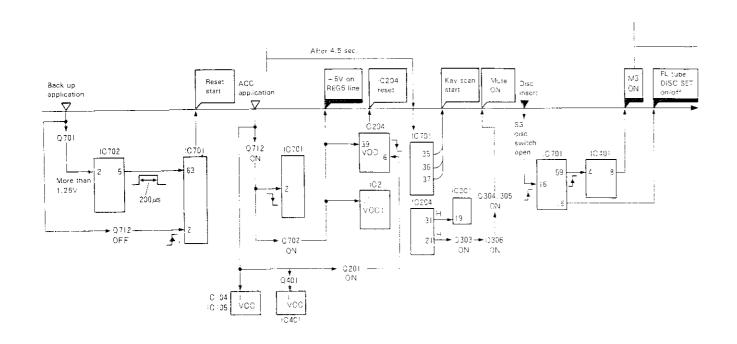


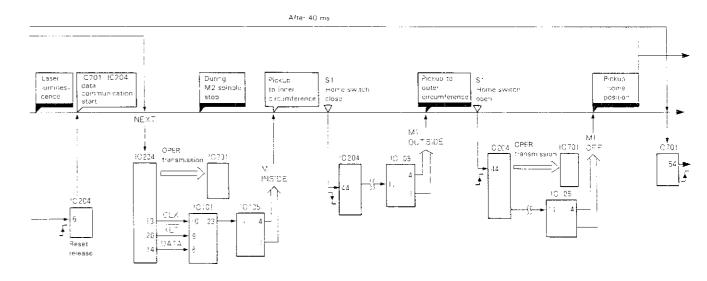
• +B Block Diagram

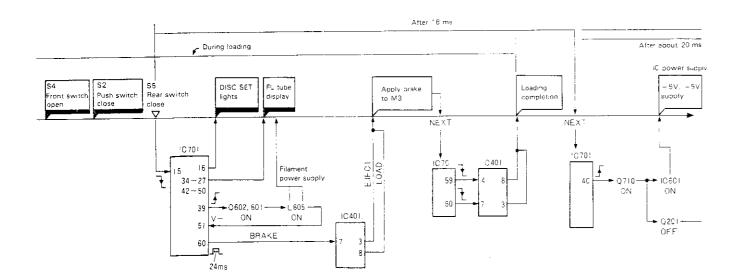


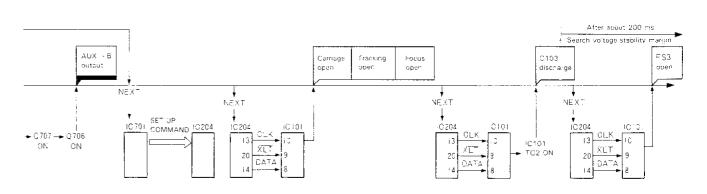


Power Supply Application ⇒ PLAY

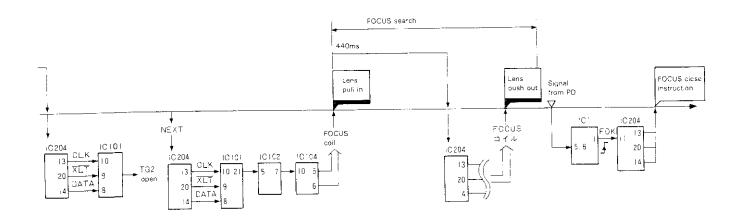


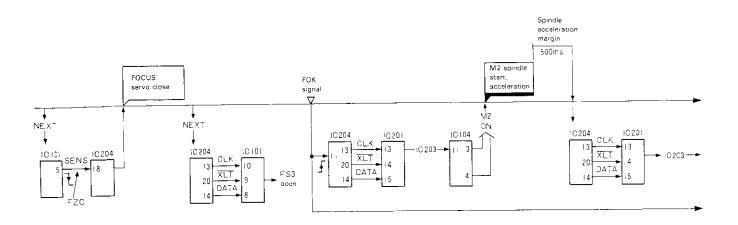




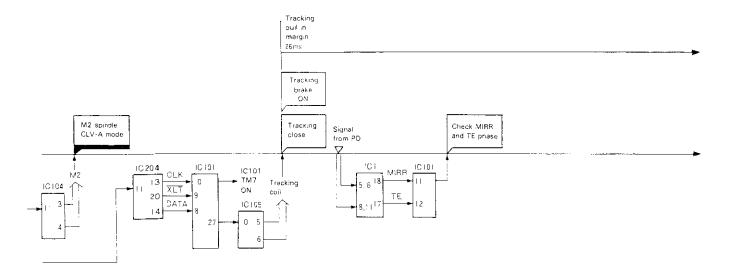


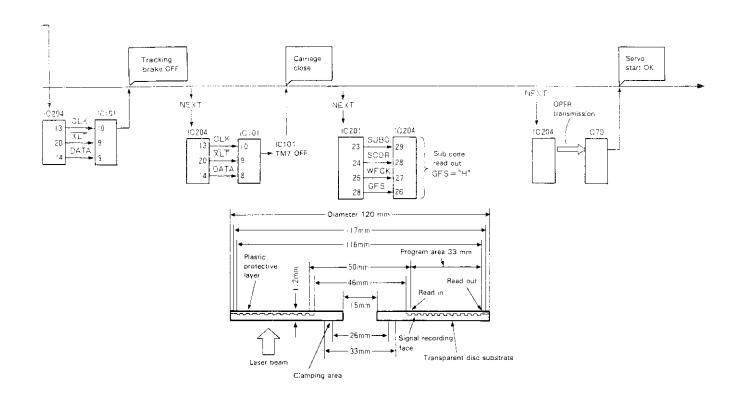












TOC read TOC read Since all servo system rise is performed at the HOME position, the pick up is located in the disc program area where a signal is readable. Then the sub-code absolute address is read and the number of tracks up to recorded TOC (read-in partiage computed by the pickup shift distance to start TOC read

*TOC (Table of Contents)
Data concerning the music No. and musical performance time period which is recorded at the disc inner circumference.

Since the TOC is recorded at Play Program search — Play IC701, the TOC is transferred from IC204 to IC701.



System Outline

Unit control is performed by a system controller (IC701: PD4074D).

The system controller in the display unit controls the CD controller (IC204: PD8019E) by using a communication line. The CD controller performs all CD player operations such as focus servo, tracking servo, basic play operations, and sequence control for the signal processing LSI group (CX20108, CX23035, etc.) related to search operations.

Normally the system controller provides CD player system external interface as indicated below.

- · Key matrix sense and beep control
- Display control
- · Loading system mechanism control
- Power supply line monitoring and control such as for ACC, back up, etc.
- High temperature sense and protective operation control
- CENTRATE, LC II interface management

Also, the system controller takes care of CD player functions (search, random play, scan, etc.). For example, in regard to the scan function,

A command is sent to IC204 to search for the music of the present track No. (TNO).

IC204 responds to a search termination command (indicates pickup was moved to subject track).

A "Play command" is sent to IC204 for mute release and play operation entry.

(During play operation, IC204 sends sequential time data.)

IC701 monitors the sent time data.

When 10 seconds are detected after play start, a search command is sent again to IC204 for the next TNO.

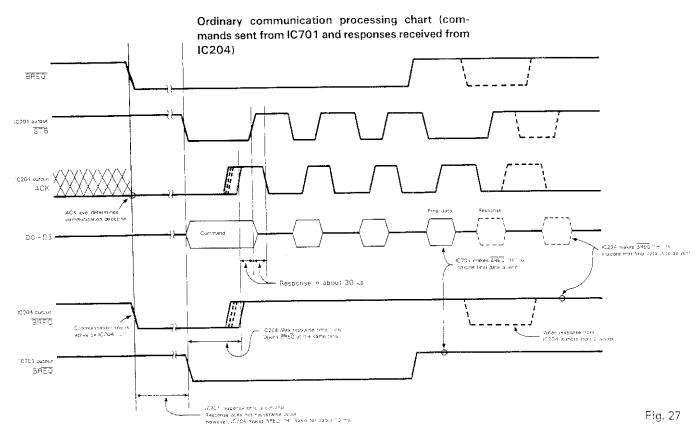
IC701 provides sequential control for IC204 that only performs basic operations as mentioned above. Therefore, this unit is roughly divided into:

- IC701 that controls the entire CD player.
- IC204 that controls the pickup system servo.

Communication Bus

The following provides an explanation of the dedicated communication bus that facilitates data exchange between the system controller (IC701) and the CD controller (IC204). This communication bus consists of 7 lines which are 4 data lines (D0-D3), ACK, STB handshake lines and a bus request (BREQ) line. Data exchange is parallel 4-bit bi directional. ACK, STB handshaking is provided so that data transfer is confirmed. Also, the BREQ line is used to control the timing for data string (play command, search command, etc.) output. Generally, IC204 output is "L" periodic with a 26 ms cycle (Fig. 27).





1) Data format

Data is sent by DO-D3 data lines. The instructions and request data sent by the system controller are called commands and response data sent by the CD controller is called a response.

Command, response code allocation

Command	D3	Co D2		DΟ	Response	Contents
?	0	0	0	0	?	Resend request
	0	0	0	1		
	0	0	1	0	NACK	Not acknowledged
	0	0	1	1		
STAT	0	1	0	0	STAT	Mechanism status
	0	1	0	1	OPER	Operation satus change, When operation is normal.
	0	1	1	0	INT	Operation status change. When operation is abnormal.
PARAM	. 0	1	1	1	ACK	Parameter set
STOP	1	0	0	0	ACK	Stop operation instruction
SET UP	1	0	0	1	ACK	Set up operation instruction
PLAY	1	0	1	0	ACK	Play operation instruction
SEARCH	1	0	1	1	ACK	Search operation instruction
FF	1	1	0	0	ACK	High speed forward operation instruction
REV	1	1	0	1	ACK	High speed reverse operation instruction
	1	1	1	0		
	1	1	1	1		

ACK: Response signal that indicates acceptance.

Representaive examples of each command and response format are provided as follows. (Also, communication can be performed with other formats.)

[Operation instruction command]([Operation parameter]) ↔ [Command response] [Asynchronous response] [Operation status data]

This format is used when the system controller provides a certain operation instruction for the CD controller. When the CD controller receives a command, it immediately returns a command response depending on the controller status, and starts mechanism operation at the same time. Although communication is suspended once, the CD controller sends an asynchronous response to the system controller depending on a change in the mechanism operation status, then it sends operation change data. Since operation change data is sent for an operation instruction command, that for an operation instruction command just sent is sent until a new operation instruction command is sent. The operation parameter that succeds the operation command depends on a different operation command. When it is omitted, operation is prescribed by a previously determined default value or a value set by a parameter set command.

[Status request command] ←→ [Synchronous response] [Mechanism status data]



When the system controller sends a status request command, the CD controller provides a direct synchronous response instead of a command response and a command response is omitted. In this case, mechanism status data is sent after a synchronous response.

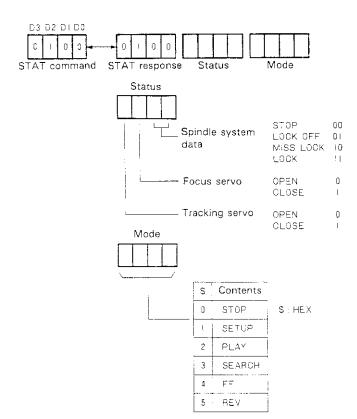
 $[Parameter\ set\ command][Parameter\ data] \longleftrightarrow [Command\ response]$

Format when CD controller parameter is set.

When this command is received, the CD controller returns "ACK" unconditionally as a command response, and at the same time rewrites the internal CD controller parameter.

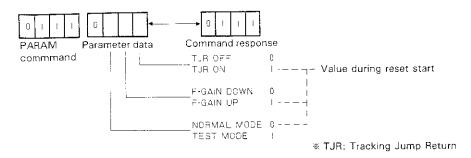
• STAT command

STAT is a command sent by the system controller as a status send request. The CD controller responds with a synchronous STAT response and sends the following data.

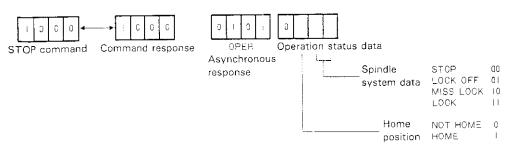


PARAM command

PARAM, a parameter set comand, sets the following data.



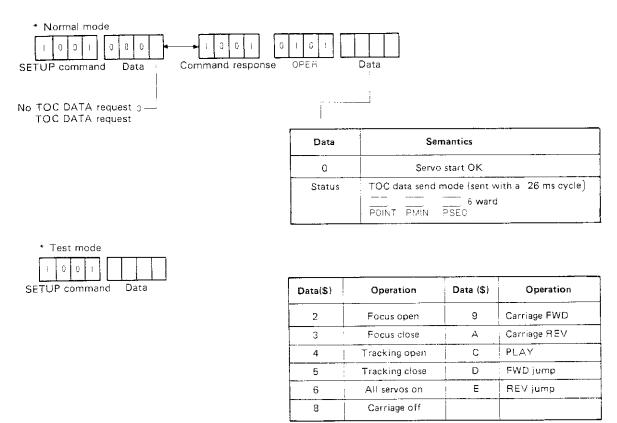
STOP command





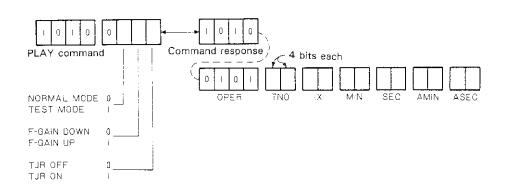
SETUP command

The SETUP command format depends on the mode set by PARAM.



^{*}As a response format, one equivalent to the STAT response is sent when servo operation has been terminated.

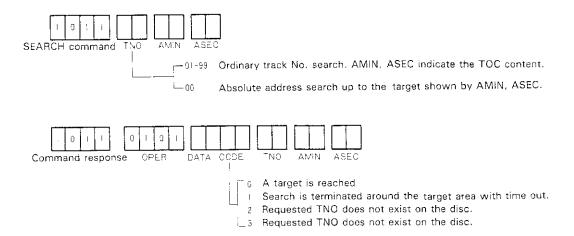
PLAY command



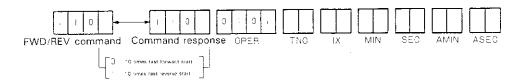
As a response, 12 woad sub-code data is sent continuously to OPER. Also, the response is sent every second because it is sent only with a second change. However, it is sent immediately when the parameter is changed, or in other words when the music or index is changed.



SEARCH command



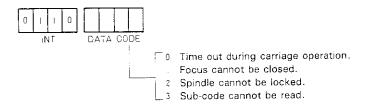
• FWD/REV command



A response is sent after OPER when it changes every 26 ms. When a parameter (TNO, IX, etc.) change occurs, it is sent immediately.

• INT response

An INT response can be accepted with any system controller operation status as an asynchronous response to notify the system controller that the CD controller has entered the STOP mode.





• CD Controller (IC204)

The servo IC CX2O108 (IC101) and digital processing IC CX23035 (IC201) are controlled by DATA, CLK, XLT, XRST outputted by the CD controller PD8019E (IC204) in which a SENS signal that matches the data content is outputted to IC204. The timing for DATA, CLK, XLT is shown in Fig. 28.

DATA transfer is by 8 bit serial data. This data is latched by the XLT signal which executes the instruction. The XRST signal clears the IC shift register during ACC ON.

The content of data to IC101, 201 is as shown in the table below.

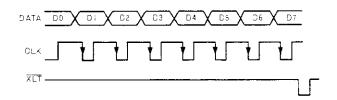


Fig. 28

Communicate to	Kinds (command) -	Address		Ta	sk	1	CENC Assessing I	
Communicate to	Kilius (comittanu)	D7 D4	D3	D2	D1	D0	SENS terminal	
	Focus control	0000	: FS4 Focus on	FS3 F gain down	FS2 F search ON	FS1 F search	FZC	
IC101 CX20108	Tracking control	0001	Anti shock	Brake on	TG 2	TG 1	AS	
					Gain set			
	Tracking mode	0010	Trackin	g mode	Sled r	mode	TZC	
	Sync protection, attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z	
	Counter set, lower 4 bits	1011	Tc3	Tc2	Tc1	TcO	COMPLETE	
IC201 CX23035	Counter set, upper 4 bits	1100	Tc7	Tc6	Tc5	Tc4	COUNT	
	CLV control	1101	DiV	TB	TP	GAIN	Z	
	CLV mode	1110		CLV	mode mode	1	PW <u>≥</u> 64	

FZC: Focus zero cross, AS: Anti shock, TZC: Tracking zero cross, Z: High impedance

1) Focus control command

Provides the focus search voltage in order to search for the zero cross point by moving the lens up and down. Outputs the FZC signal (H to L) from the IC101 SENS terminal at the zero cross point to fetch the focus lock timing.

2) Tracking control command

This command controls the tracking gain and brake circuit.

The tracking gain is increased when TG1 = TG2 = 1.

TG1 changes the high pass compensation time constant by turning the phase compensation selection switch on. TG2 switches the high pass gain. When a large impact is detected in the anti shock circuit, a sound skip is prevented by increasing the tracking gain. Also, during track jump, spot return is prevented by increasing the gain to realize a track jump.

The anti shock circuit consists of a window comparator (in IC101) for checking the tracking error signal magnitude by input from IC101 terminal (19). When the entry of an error signal larger than the window occurs, player mechanical impact is detected and the servo gain is increased to keep the beam on the track. The anti-shock circuit functions

when D3 = 1. During this command, SENS output expresses AS (Anti Shock). If tracking error input exceeds the window size (large impact), AS = 1 occurs.

If 100 track jump or 10 track jump occurs during access, the brake circuit turns the tracking servo circuit on and off to stop the beam at a desired position quickly. The brake functions when D2=1.



3) Tracking mode command

This command is used to cause a jump pulse and fast forward pulse during access, and tracking servo and carriage servo ON/OFF.

	Trackin	ng mode	O-anation	Carriage mode		
Operation	D3	D2	Operation	D1	D0	
Servo off	0	0	Servo off	0	0	
Servo on	0	1	Servo on	0	1	
FWD jump	1	0	Fast FWD	1	0	
REV jump	1	1	Fast REV	1	1	

Command Code

4) Sync protection, attenuator control command

D3	D2		D1		D0		
GSEM	GSEL	Number of interpolated frames		Window width (clock)	ATTM	MUTG terminal (pin 19)	Attenuation (dB)
0	0	2	0	±3	0	0	0
0	1	4	1	±7	0	1	
1	0	8			1	0	-12
1	1	13			1	1	-12

Command Code

• Sync protection (D3-D1)

Although a data pattern (3T – 11T) the same as a frame sync signal (24T) does not exist during recording, sometimes the same pattern is detected in data due to the influence of dropout and jitter. Also, on the other hand, since an original frame sync signal is not detected sometimes, protection and interpolation as well as detection are necessary.

Only the edge of the EFM signal latched by PLCK is input as "1" and the other part is input to the 23 bit shift register after conversion to "0" to detect a frame sync signal.

A window is provided to protect a frame sync signal, and the same pattern outside the window is eliminated. When a frame sync signal does not exist in the window, interpolation is performed by a signal generated by the 588 octal counter (4.3218 MHz / 588 = 7.35 kHz). A 4 bit counter is provided that counts the number of interpolated frames. When this value reaches the number of frames selected by GSEL, GSEM, the window is ignored and the 4 bit counter is reset when the next frame sync signal occurs during which GTOP (pin 27) becomes "H". Also, the GFS terminal (pin 28) becomes "H" while the frame sync signal generated

by the 588 octal counter for interpolation is synchronized with the frame sync signal from the disc.

The write request signal (WREQ) and timing such as the write frame clock (WFCK) are generated based on the protected and iterpolated frame sync signal.

Attenuator (D0)

A signal appears at the MUTG terminal (pin 19) from IC204 (CD controller). Muting or -12dB attenuation is executed by a 2 bit signal.



5) Counter set (lower bit, upper 4 bits)

During access, a track count pulse enters the CNIN terminal (pin 17) from the IC101 CSET terminal (pin 6). This command presets the counter preset value that counts the pulse.

6) CLV control command and CLV mode command

DiV	D3	1	RFCK/4 and WFCK/4 RFCK/8 and WFCK/8	Phase comparison frequency during CLV-P mode
ТВ	D2	1	RFCK/32 RFCK/16	Bottom hold cycle during CLV-S, CLV-H mode.
TP	D1	0	RFCK/4 RFCK/2	Peak hold cycle during CLV-S mode,
GAIN	DO	0	-12dB 0dB	MDP terminal (pin 3) gain during CLV-S, CLV-H mode.

CLV Control Command

Mode	D3 - D0	MDP (pin 3)	MDS (pin4)	 FSW (pin 1) 	MON(pin 2)
STOP	0000	L	Z	L	L
Kick	1000	Н	Z	L	н
BRAKE	1010	L	Z	L	Н
CLV-S	1110	CLV-S	Z	L	Н
CLV-H	1100	CLV-H	Z	L	Н
CLV-P	1111	CLV-P	CLV-P	Z	Н
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	LorZ	Н

CLV Mode Command

Z: High impedance

These signal are commands that concern the CLV servo. IC204 (CD Controller) selects each CLV mode and sends a command to IC201. IC201 controls spindle motor rotation by the following output. IC201 output is by the MDP terminal that controls the speed and phase synchronization, the MDS terminal that controls speed synchronization, the FSW terminal that performs filter constant switching, and the MON terminal that controls motor on/off. A signal that matches each motor is applied to the spindle control circuit for these terminals.

Usually each control signal outputted from IC201 during play has a modulated pulse width. These signals are applied to the spindle servo circuit (IC203) before application to the PWM driver (IC104) to stabilize operation. The spindle servo circuit consists of a low pass filter with IC203, R206, 207, C205, 204 which converts a signal (pulse) to DC. D201-203 are connected to IC203 output through R210. This circuit is a limiter that prevents excessive motor current flow when a signal becomes abnormally large and is set so that the PWM driver (IC104) output duty range does not become 100%. When IC203 output becomes a large positive value,

D202, 203 are turned on and are fixed at +2.5 to 2.7V. When it becomes a large negative value, D201 is turned on and is fixed at -0.5 to -0.7V.

STOP mode

During this mode, the \pm 5V D/D convertor (IC601) operates and the spindle motor does not rotate (during EJECT, etc.). In regard to each IC201 output, MDP = ''L'', MDS = ''Z'', FSW = ''L'', and MON = ''L''. IC203 pin 1 output is OV (SPDD). Also, the MON pin is connected to IC104 pin 15. When this terminal becomes ''H'', the spindle driver operates. When it is ''L'', no output occurs (to prevent driver operation by the IC203 offset voltage).



KłCK mode

In this mode, when the spindle motor shifts from a stop status to an operation status, it is forced to operated (forward rotation) so that PLL pull in can be easily performed. Pin 1 (SPDD) of IC203 becomes ± 4 or ± 5 V which is applied to IC104. Since MON = "H", IC104 operates.

BRAKE mode

In this mode, when motor stop is required during spindle motor forward rotation, a voltage reverse to the forward rotation is applied to the motor to reduce motor rotation rapidly to stop the motor quickly. IC203 pin 1 (SPDD) becomes -3 or -4V. After low speed motor rotation is detected by the signal from IC201 pin 18 SENS terminal, IC204 stops sending the BRAKE command.

• CLV-S mode (S:SPEED)

Rough servo mode used when EFM-PLL circuit lock is released during rotation start, track jump, etc.

CLV-H mode

Used when the RF signal has an intermittent status such as during high speed search.

CLV-P mode

Ordinary play mode used during PLL lock.

CLV-A mode

When the CLV-P mode becomes unstable due to vibration and disc scratches, or when track jump (several tracks) occurs, a switch is made to the CLV-S mode, then an automatic switch is made to the CLV-P mode when disc rotation and PLL are stabilized.

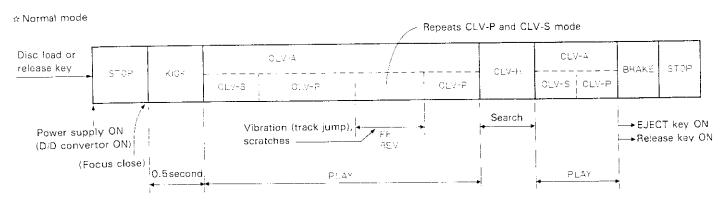


Fig. 29

Fig. 29 Spindle motor control mode selection

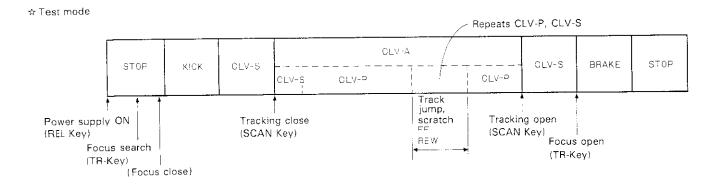


Fig. 30 Spindle motor, control mode switching



• RF Amplifier (IC1:CX20109)

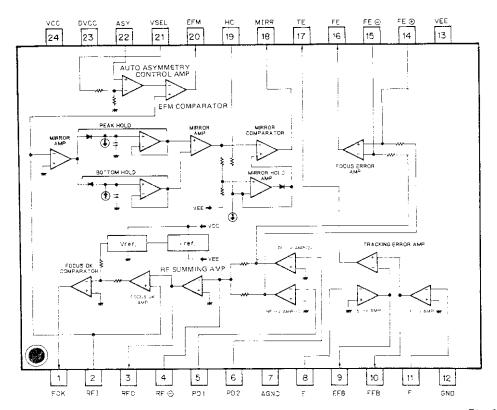


Fig. 31

A circuit that processes the 3 spot pickup output signal and provides a signal to the next step, servo section, demodulator section and servo controller.

1) RF amplifier

Photo diode current input to pin 5, 6 is converted to I-V by the RF I-V amplifier. Also, summation by the RF summing amplifier (A+B+C+D) is output to pin 3.

2) EFM comparator

The RF binary signal input by pin 2 is output to pin 20 as an EFM signal. Since asymmetry that occurs due to uneven disc manufacture cannot be removed just by AC coupling, the 50% probability of a 1, 0 binary EFM signal is used to control the reference voltage of the EFM comparator.

3) Focus error amplifier

The RFI-V amplifier (1) output (A+C) and RFI-V amplifier (2) output (B+D) difference is provided as focus error signal (A+C-B-D) output from pin 16.

4) Tracking error amplifier

Side spot photo diode current input to pin 8, 11 is converted to I-V by the E, F I-V amplifier. Also, the E, F I-V amplifier difference used by the tracking error amplifier is provided as tracking error signal (E-F) output from pin 17.

5) Focus OK circuit

This circuit provides the timing window which turns the focus servo on from a focus search status. In regard to the Focus OK signal (an RF comporator signal), when pin 3 becomes more than 0.4V, pin 1 becomes "H".

6) Mirror circuit

Peak and bottom hold occurs after the pin 2 RFI signal is amplified. A DC reproduced envelope signal is obtained by differential amplification of the peak/bottom hold signals. This signal is compared to a signal in which 2/3 of the peak value is peak held with a large time constant to obtain mirror output. Since the mirror signal becomes "L" on a disc track and "H" between tracks (mirror part), the track difference is detected when the pickup crosses a track. Also, "H" output occurs during defect detection.



D/A Convertor (IC301) and Integrator (IC302)

IC301 is used to convert 16 bit data to a current signal. IC301 receives each signal (DATA, LRCK, WDCK, BCLK) from IC201 to extract data. Current (I OUT L, R) output occurs from count start until the count becomes zero. In regard to IC302 operation, current output from IC301 charges condensor C310, 311 connected between the (-) input terminal (pin 6, 2) and the output terminal (pin 7, 1). Then voltage that matches this is outputted from IC302 (pin 7, 1) as current conversion to voltage.

When current from IC301 stops, IC302 output holds the voltage.

However, since new data entry is continuous, the hold voltage must return to OV. Therefore, C310, 311 are discharged by Q301, 302 before new data is extracted. In regard to discharge timing, it is provided as DCL, DCR output by IC301. The output of IC302 varys between OV and 4V (Fig. 32).

It is as shown in Fig. 32 during non-signal ($-\infty dB$) reproduction. Audio signal operation is with a 2V offset.





Fig. 33

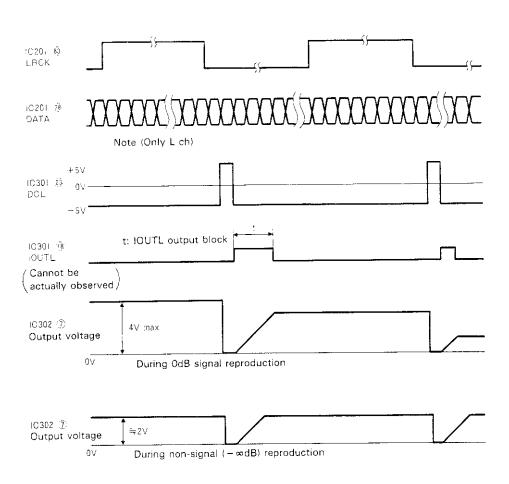


Fig. 34



Deglitch (IC303) and Sample Hold (IC304) Circuit the Following Gives Description for L-ch Only.

IC302 signal output is connected to the IC304 (-) input terminal through R306 and the IC303 switch. In regard to the IC303 switch, pin 15 and 1 are turned on by the LRCK "H" section output from IC201. Pin 15 and 2 are turned on by the "L" section, the signal from R306 drops to GND and the IC304 (-) input terminal is opened.

An approximate circuit when IC303 pin 15 and 1 are turned on is as shown in Fig. 35. At that time, the circuit functions as an ordinary amplifier.

1C302 output voltage is increased by this amplifier gain to become IC304 output (180° phase deviation).

Next, the IC303 switch becomes as shown in Fig. 35 when pin 15 and 2 become on.

IC302 is separated from IC304. However, since C318 is charged by the previous output voltage, the voltage is held between this.

Also, IC302 output is offset \pm 2V, negative voltage is applied by R308, R310 and C314 so that the offset is cancelled. IC304 functions as an adder with OV output. There is a \pm /- audio signal shift centered on OV.

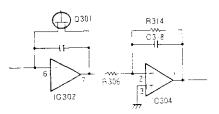


Fig. 35

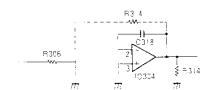


Fig. 36

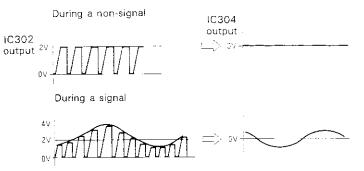
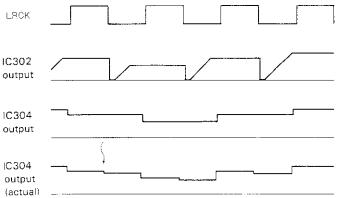


Fig. 37



There is a difference between the hold voltage and previous voltage influenced by a slight discharge of C318 and the IC offset voltage.

Fig. 38



• Low Pass Filter (IC305, 306) (LPF)

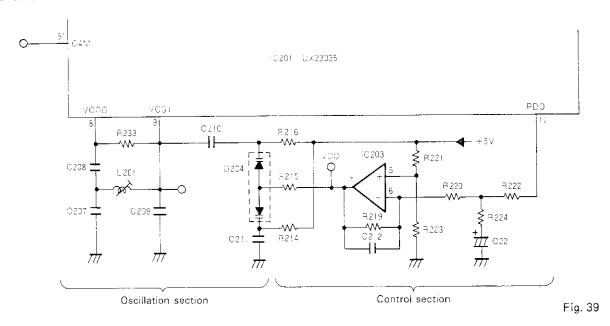
Since there is excessive spectral density in IC304 output, the frequency component in areas other than the audible zone is eliminated by an LPF provided with 6dB gain as well as an internal deemphasis circuit so that deemphasis ON/OFF can be controlled by applying $\pm 5V$ or $\pm 5V$ to pin 3. In regard to deemphasis ON/OFF, lead-out is performed by a disc sub-code, and signal output is by IC204 (CD controller). However, since IC204 output is OV and OV0V, the IC303 switch is controlled through Q307, then the switch selected voltage is applied to pin 3 of IC305. (Since IC305 pin 3 requires current, the Q307 collector cannot be directly connected.)

Isolator (IC307) and Mute Circuit

The isolator is used to cancel noise that occurs on the GND line of the connection cable when it is connected to a cassette deck. GIN is the unit ground and GOUT is connected so that it drops to the GND level of the cassette deck.

When a CDX-2 audio signal is checked, this is performed by shorting GIN and GOUT or by shorting DIN cord pin 3 and the external side (wire mesh).

• PLL Circuit



This circuit is used to extract the EFM signal reproduction clock. The phase of the signal produced by the oscillation section and that of the EFM signal are compared, then the IC201 (PDO) pin 11 output result is amplified for application to the varicap (D204) anode. IC203 output is usually set for -0.5V during play. (Measured by a tester and millivolt meter. When it is measured by an oscilloscope, the voltage is seldom set because of overlapping high pass noise.)

When oscillation circuit frequency is high, the output is high $(-0.5V \rightarrow 0V \rightarrow \pm 2V)$ and when it is low, the output is low $(-0.5V \rightarrow -3V)$. The oscillation frequency is usual-

ly 8.643 MHz during play. However, if a measuring instrument is directly connected to the oscillation section, the circuit becomes unstable. Therefore precautions should be taken.

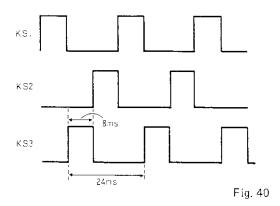
Also, PLL circuit lock or non-lock can be confirmed by IC201 pin 28 (GFS). When it is "H", a lock status occurs and when it is "L", a non-lock status occurs. When PLL lock does not occur, IC203 output is in a range from 0 to -1V.



Key Scan

Positive pulse sequential output occurs from IC701 (PD4074D) pin 35-37 (KS1-KS3) with the timing shown in Fig. 40 when ''L'' voltage is applied to IC701 pin 2 (VSENSE)

Data is read from IC701 pin 18-21 (KD0-KD3) with "H" key scan timing which identifies a key that was pressed. When no key is pressed, usually pins 18-21 are all "L".



Display

The FL driver is built into IC701, which provides a direct FL display.

IC701 output is provided by the 9 grid output timing of pins 42-50 and the 8 segment output timing of pins 27-34. Also, since V-(-30V) is applied to pin 51, and pins 42-50 and 27-34 are pulled down to -30V, an output swing from -30V to $\pm5V$ can be obtained, and FL is lit with grid and "H" segment timing. Also, -22.5V biased with 1.8Vrms AC is applied to the FL filament.

· AUX control circuit

When voltage (12V) is applied to the external control input DIS Bline, Q704 is turned on and IC701 pin 6 becomes "L" which stops all operations until Q704 is turned off and

pin 6 becomes ''H'' again. At that time, IC701 pin 54 becomes ''L'', Q707, 706 become off and the AUX \pm B output becomes ''L''.

AUX ÷ B output indicates unit operation. When the player is operational, it is on together with Q706, 707 which provide ACC + B output. However, when independent player operation stops by an external operation stop command or by disc eject, "L" output occurs from IC701 pin 54, and Q706, 707 become off which stops AUX - B output.

The iLL line is a control line that lights night illumination by synchronizing with external units which are directly connected to the illumination circuit. When illumination is lit by the ILL line, IC701 pin 5 becomes "H" which reduces the display scan duty and performs dimmer operation.

Search Mode

In regard to the search sequence, three steps (cross count search, step search, cueing step) are performed by a combination that depends on the situation.

· Cross count search (Fig. 41)

Computation of the shift direction and number of tracks is based on the present address and subject address to be searched.

When a command is sent to IC101 for tracking open, spindle CLV-H mode entry and the carriage voltage shifts toward a desired direction, carriage feed is by IC105 (carriage driver). Cross pulse output occurs from IC101 CNT (pin 6) every time one track is crossed and is sent to IC201. Next 1/256 frequency divided pulse output occurs from SENS (pin 18) of IC201 which is counted by IC204 (CD controller). When a prescribed track is crossed, reverse carriage drive occurs to apply a brake and to stop the pickup. (Since

cross count search feed is with 256 track units, the fraction is shifted by a 128 track jump and multi jump.)

After braking is terminated, tracking close and tracking brake on occur and the spindle motor is changed to the CLV-A mode. Next, after 100ms, tracking brake off and carriage close occur and the present address is read in again. The number of tracks that are sent is computed again based on this address and the subject address. This operation is repeated until a subject address is reached. When a subject address is reached, shift to the final cueing step occurs. (In the last address search, a cueing step is not performed which terminates the search.)

The cross count search mentioned above can only be used when a subject address is known which is restricted to TOC data use and during search to the last address memory location. For a case other than that mentioned above, a step search (mentioned below) is performed.



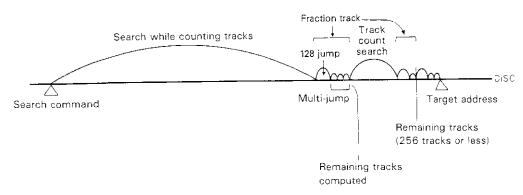


Fig. 41 Cross count search (When the target address is known)

• Step search (Fig. 42)

The basic pickup shift method and brake output method are the same as that for cross count search. Step search is performed when a subject address is unknown. Since the number of tracks up to the subject address cannot be computed, a certain value is set and the target is reached step by step.

First, the number of tracks is set as 768 (256 x 3) to shift the pickup, then the address is checked. The pickup is shifted by 768 tracks each time by repeating this until the target is passed. When the target is passed, the pickup shift is reduced to 1/2 that of the original shift, then the pickup is shifted again by reversing the shift direction. This procedure is repeated by reducing the shift to 1/2 that of the previous shift every time the target is passed and by reversing the shift direction. After this, a shift is made to the cueing step.

· Cueing step

The spindle motor quartz servo is out of sync because the pickup was rapidly shifted in a radial disc direction due to cross count search and step search. Therefore it is necessary to terminate the search operation before the original subject address and shift to the play mode because a quartz servo pull in margin must be obtained and mute release timing must be checked.

Also, in regard to cross count search, since the reliability precision of data recorded on TOC is only 1 second even if pickup shift precision is improved, it is necessary to perform a fine adjustment of the pickup position when it shifts to the play mode. Therefore, when a subject address is reached, a 3-track jump back is performed during play. If INDEX = 0 exists, MUTE is released 1 second before the subject address to shift to play, and if INDEX = 0 does not exist, MUTE is released at the subject address.

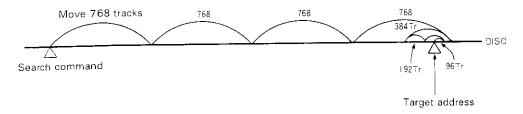


Fig. 42 Step search (When distance to target address is unknown)



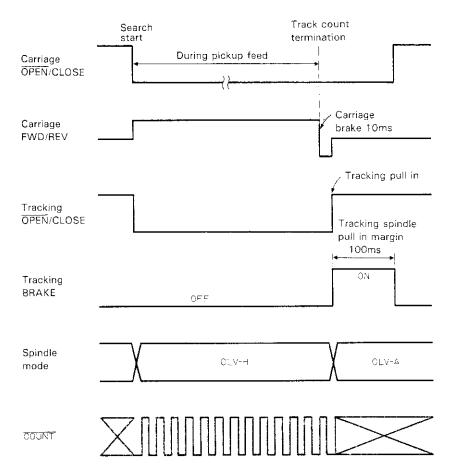


Fig. 43 Track, count sequence

· Protective operation during search

If the pickup jumps to the mirror face of the disc while it is being shifted, erroneous operation might occur. Therefore, it is necessary to provide quick pickup return to the inner circumference area where data is recorded. To accomplish this with IC204, the MIRR signal is checked with 1ms intervals while pickup shift occurs. When MIRR = "H" continues for 15ms, the projection of the pickup onto the mirror face is judged, the pickup shift direction is reversed, and a 100 track cross pulse count occurs to confirm that it has returned to the data face. Next, pickup shift stops, address read in occurs and and search continues. When the count is not terminated after 1 second has passed, it shifts to the STOP mode by judging that the servo system is abnormal, then it shifts to the set up mode again.

Also, when search cannot be performed after 10 seconds have passed due to an abnormality, stop occurs and the disc is ejected.



Play Mode

The mode used for ordinary music playback. When no abnormality exists, active operation is not performed but monitoring of each part is performed in which the representative pin status is as follows.

IC204 Pin 21 AMUTE "L" Pin 22 XRST "H" Pin 31 MUTG "L" Pin 2 CBRAKE "H"

in regard to monitoring, the address of the reproduced location obtained by the FOK signal, GFS signal and the sub code is monitored once every 26ms. Also, carriage servo OPEN/CLOSE and emphasis ON/OFF switching is performed. The FOK signal indicates focus or out of focus to detect an abnormal focus servo system. If the FOK signal is "L" for 100ms, it is judged that the focus servo system is abnormal, then it shifts to the STOP mode.

The GFS signal indicates spindle PLL circuit lock or no lock to detect an abnormal spindle system. If the GFS signal is "L" for more than 2 seconds, it is judged that the spindle system is abnormal, then it shifts to the STOP mode.

When a sound jump occurs during play reproduction due to a sudden shock, the pickup can be returned to an address that continues to the address just before the sound jump occured so that reproduction can continue and abnormal

music reproduction can be performed. In regard to reproduction address monitoring, the reference address to be read out next is internally computed based on the reproduction position address that was read during play. When the address is read out next, the internally generated address is compared to the address that was actually read out. As a result, if a difference of more than 1 second exists 5 times continuously, it is judged that sound jump occurred due to some reason, and the reference address is searched as a target address.

To operate the function for sound jump return by monitoring the address of the reproduction location, it is necessary for the sub-code to be read correctly. Therefore, the sub-code is checked during play to see if it can be read or not. When it cannot be read 16 times continuously, a shift is made to the STOP mode.

The purpose of carriage servo OPEN/CLOSE selection is to conserve power. When the pickup lens is near the center, servo open occurs and when it deviates from the center, servo close occurs which moves the carriage to move the lens relatively toward the center against the pickup.

Emphasis ON/OFF selection is performed to change the frequency characteristics of the reproduction system by matching the music emphasis ON/OFF during reproduction which is switched according to sub code data that was read in

· Address read out by a sub code

In regard to sub code Q-channel demodulation, SCOR, WFCK, SUBQ signal output by the signal processing IC (IC201) is read out by IC204 to perform a CRC check.

SCOR is a synchronous 98 bit 1-frame sub code signal while WFCK is a serial clock for the 98 bit sub code, and SUBQ is sub code Q channel control data. Fig. 44 shows the timing for these signals.

As evident in this figure, SCOR = H wait occurs and SUBQ data is read in with 96 bits at the WFCK rising edge at the frame sync point, then a CRC check is performed and the sub code is fetched. Since 1 cycle of WFCK is 136 μ s, and the sub code consists of 98 bit data including the SCOR sync pattern, about 13.3 ms is necessary for a one time fetch of the sub code.

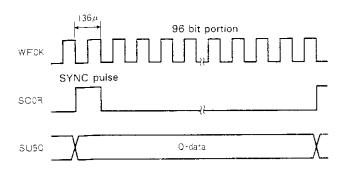


Fig. 44 Sub code read out timing

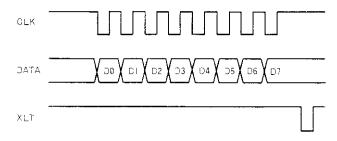


Fig. 45 Serial data output timing



• FF, REV Mode

A fast feed mode. In the FF mode, "sub code read once as a 2—7 track jump" is repeated toward the outer circumference, and in the REV mode, it is repeated toward the inner circumference. In regard to the number of tracks, 7 tracks are provided on the inner circumference and 2 tracks are provided on the extreme outer circumference so that the fast feed speed becomes constant at both the outer and inner circumference. When the FF mode exists at the extreme outer circumference, it shifts to the Play mode by a return to the extreme inner surface even if the REV mode exists. Also, when TR and index changes occur in the FF, REV mode, a shift to the Play mode occurs at this point.

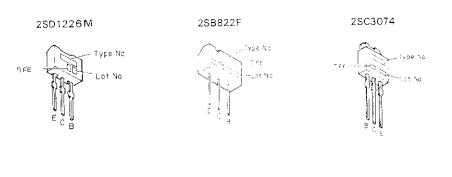
Protective Operation

- 1) When a disc is pulled out during loading and the disc switch is closed, the eject operation occurs.
- 2) When the REAR switch is not closed 6 seconds after loading has started, the eject operation occurs.
- When the servo system has trouble and does not recover after 15 seconds have passed, the eject operation occurs.
- 4) When an operation does not terminate within 7.5 seconds after the eject (loading) operation has started, the loading (eject) operation occurs.
- 5) When section 4 operation occurs 4 times continuously, the mechanism enters a stop status. If the eject key is pressed during this status, the eject operation starts.
- 6) When loading is performed by inserting a new disc to enter the set up mode, if servo close has not occurred, focus cannot be performed or tracking cannot be closed, it shifts to the eject operation after finding that the back of the disc is being read. Since disc reload is not accepted in this case, when loading is performed again, it must be performed after removing the disc once.

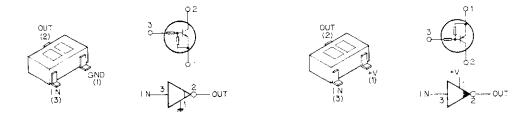
- 7) When the focus shifts and the servo system has trouble such as spindle miss lock, if the servo system does not recover to a normal status after 15 seconds have passed, the disc is ejected by a judgement that continuous vibration is applied to the set.
- 8) If the status does not change after 10 seconds have passed when a carriage shift is attempted such as when the carriage mechanism does not move or search does not occur, the disc is ejected by a judgement that the carriage mechanism has trouble.
- 9) When data cannot be exchanged continuously 3 times during communication, the disc is ejected by a judgement that a communication error has occurred.
- 10) When the temperature detection circuit detects a high temperature and makes IC701 pin 7 (TEMP) low, "HH HHHH" is displayed in a high temperature detection protective operation which turns the DC/DC converter (IC601) off to enter a release status. When TEMP returns to a HIGH status, play is reopened at the address just before release.



●ICs and Transistors



UN2211 UN2111



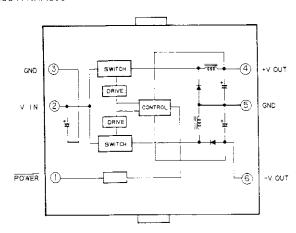
Chip Transistor

Part No.	1	Indication (Type No., hFE)
2SD1048-X6	X6) PEE
2SD1048-X7	X7	Type No.
2SD1048-X8	X8	
2SD601-YQ	YQ	L'n
2SD601-YR	YR	3
2SC2712-LG	LG	Tyoe No USS
2SC2712-LY	LY	64: 8
2SK508-K52	K52	
2SK508-K53	K53	Service of the servic



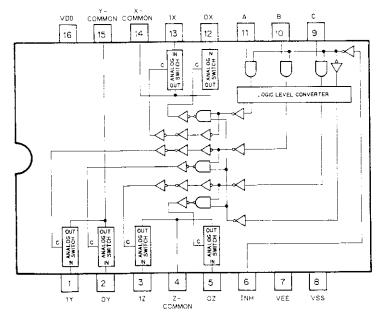
• Power Supply Assy

IC601: KHA803



Main Assy

IC303: TC4053BF

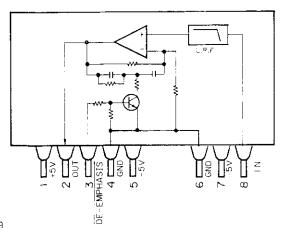


TC4053BF is a 2 channel x 3 multiplexer that enables an analog signal, digital signal selection and combination. The corresponding switch of each channel is turned on by a control terminal digital signal.

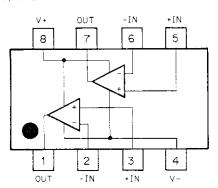
Truth Table for TC4053 BF

	Contro	linput		"ON" channel
INH	С	В	Α	ON channel
L	L	L	L	0X, 0Y, 0Z
L	L,	L	Н	1X, 0Y, 0Z
L	L	Н	L	0X, 1Y, 0Z
L	L	Н	Н	1X, 1Y, 0Z
L	Н	L	L	0X, 0Y, 1Z
L	Н	. L	Н	1X, 0Y, 1Z
L	Н	, н	L	0X, 1Y, 1Z
L	Н	j H	Н	1X, 1Y, 1Z

IC305, 306: KHA210A

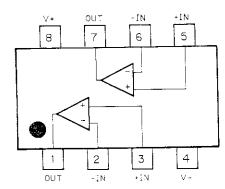


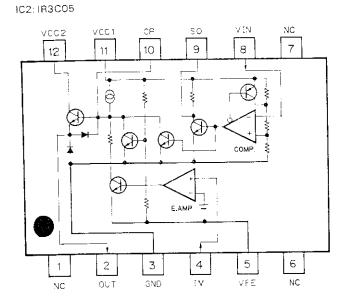
IC102, 103, 203, 307: M5218FP



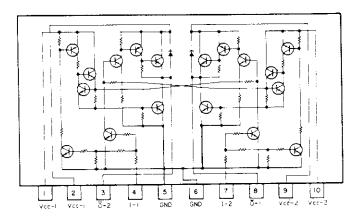


IC302, 304: M5221FP(NJM072M)





IC401: M54546L

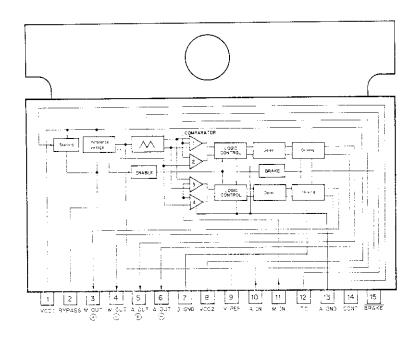


IR3C05 Terminal Function

Laser diode constant light output drive IC

Pin No.	Pin name	I/O	Function and operation
1	NC		
2	OUT	Output	Output
3	GND		Ground
4	IM	Input	Monitor input
5	VEE		(-) power supply
6	NC		
7	NC		
8	VIN	Input	Control input (ON/OFF), thermal shutoff
9	\$O	Output	Operation signal output. "H" during operation, "L" during stop.
10	СР	!	Phase compensation
11	VCC1		Control (+) power supply
12	VCC2		Output (+) power supply

IC104, 105; PA3021A





PA3021A Terminal Functions

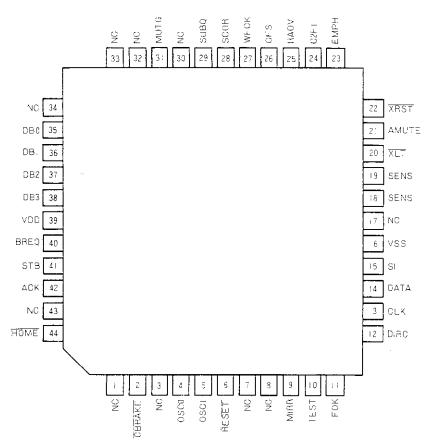
PWM driver

Pin No.	Pin name	1/0	Function and operation
1	VCC1		ACC power supply
2	BYPASS		IC reference voltage ripple filter condensor connection terminal
3	MOUT+	Output	Motor driver positive output terminal
4	MOUT-	Output	Motor driver negative output terminal
5	AOUT+	Output	Actuator driver positive output terminal
6	AOUT-	Output	Actuator driver negative output terminal
7	DGND		Power step GND terminal
8	VCC2		+5V power supply
9	Vref	Qutput	IC stabilizing supply output terminal
10	AIN	Input	Actuator system analog signal input terminal
11	MIN	Input	Motor system analog signat input terminal
12	TC		Chopping waveform condensor connection terminal
13	AGND		Small signal system GND terminal
14	CONT	Input	Circuit operation status, standby status selection terminal. Active "H".
15	BRAKE	Input	Motor system operation, non-operation (STOP) selection terminal. Active "L"

*10204 : PD8019E

IC's marked by * are MOS type.

Be careful in handling them because they are very liable to be damaged by electrostatic induction.





PD8019E Terminal Function

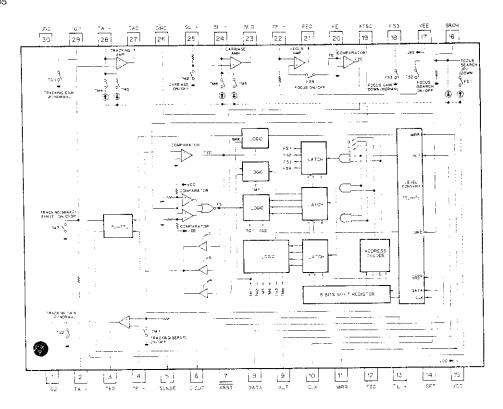
CD controller

Pin No.	Pin name	1/0	Function and operation
1	NC		
2	CBRAKE	Output	Carriage motor brake terminal. N-ch open drain with pull up. "L": Brake ON.
3	NC		
4	OSC0	Input	Clock oscillation terminal. 4MHz
5	OSC1	Output	Clock oscillation terminal
6	RESET	Input	ICreset terminal. N-ch open drain with pull up. "L": Reset ON, "H" = Reset OF
7	NC		
8	NC		
9	MIRR	Input	Mirror signal input terminal. Input port with latch, "H": Mirror face, between tracks.
10	TEST	Input	Normal mode/chip check mode selection terminal. Input port with latch.
11	FOK	Input	FOCUS OK signal input termianl, Input port with latch, "H": Focus OK
12	DIRC	Output	Single jump control terminal. N-ch open drain with pull up.
13	CLK	Output	Serial data transmission clock output. N-ch open drain with pull up.
14	DATA	Output	Serial data output. N-ch open drain with pull up. Controls CX20108 and CX2303
15	SI	Input	Chip checking command input terminal. N-ch open drain with pull up.
16	VSS		GND
17	NC		
18	SENS	Input	Sense signal input terminal, N-ch open drain with pull up.
19	SENS	Input	Sense signal input terminal. N-ch open drain with pull up.
20	XLT	Output	Serial data latch pulse, N-ch open drain with pull up,
21	AMUTE	Output	Audio signal mute, N-ch open drain with pull up.
22	XRST	Output	Reset terminal. N-ch open drain with pull up. Resets the shift registers, CX2010 CX23035.
23	EMPH	Output	Emphasis ON/OFF selection terminal. N-ch open drain with pull up. "H": Emphasis ON.
24	C2FL	Input	Error correction NG monitor input terminal, N-ch open drain with pull up,
25	RAOV	Input	Jitter extraction RAM overflow. N-ch open drain with pull up.
26	GFS	Input	Spindle lock detection, N-ch open drain with pull up, "H' during spindle lock,
27	WFCK	Input	Sub code read out clock. N-ch open drain with pull up.
28	SCOR	Input	Sub code sync. N-ch open drain with pull up.
29	SUBQ	Input	Sub code data, N-ch open drain with pull up,
30	NC		
31	MUTG	Output	Signal processing mute. N-ch open drain with pull up.
32 – 34	NC		
35 — 38	DB0 - DB3	1/0	Communication data bus, N-ch open drain with pull up.
39	VDD		Power supply terminal, +5V



Pin No.	Pin name	1/0	Function and operation
40	BREQ	Input/Output	Communication control line. N-ch open drain with pull up. Data link control. Communication bus is enabled by "L" status entry from an "H" status. At the same time, the communication mode is determined by the ACK output level. ACK
41	STB	Input	Communication control line • Handshake control. N-ch open drain with pull up. Communication direction (PD4074D → PD8019E) Indicates that PD4074D data output at the rise of this signal is effective. Communication direction (PD8019E → PD4074D) Indicates that data output at the rise of this signal was accepted by PD4074D.
42	ACK	Output	Communication control line. N-ch open drain with pull up. Data link control The communication mode is determined by the level of this signal. Handshake control Communication direction (PD4074D → PD8019E) Outputs "H" which indicates that data output by PD4074D was accepted. Communication direction (PD8019E → PD4074D) Outputs "L" which indicates that data output for PD4074D is effective.
43	NC		
44	НОМЕ	Input	HOME switch detection terminal. N-ch open drain with pull up. Terminal that determines the pickup home position. Home position: Location where this terminal changes from "L" to "H".

* IC101: CX20108



CX20108 Terminal Functions

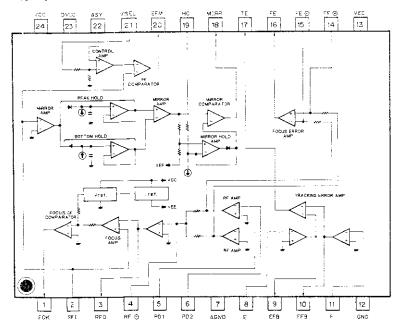
Focus, tracking, carriage servo IC

Pin No.	Pin name	1/0	Function and operation
1	TG2	Output	Tracking amplifier gain selection terminal. Becomes open or GND level.
2	TA+	Input	Amp 2 (tracking amp) non-inverted input, Tracking error signal input,
3	TE0	Output	Amp 4 (tracking amp) output, Tracking error signal output.
4	TE-	Input	Amp 4 (tracking amp) inverted input.
5	SENSE	Output	Outputs an IC status that corresponds to the DATA address. (Changes with address content of internal serial resgister.)
6	C OUT	Output	Track number counting signal output during high speed access.
7	XRST	j Input	Clears all internal registers when "L".
8	DATA	Input	Serial data input from CD controller (IC204). Inputted by LSB, D0-D7.
9	XLT	Input	DATA latch (The content of the internal serial shift register is transferred to a latch that was address-decoded.) Transferred with "L". Since it is not an edge trigger, it is necessary to return it to H after execution.
10	CLK	Input	DATA transfer clock. Data transferred at the trailing edge.
11	MIRR	Input	Mirror signal input from RF amplifier.
12	TZC	Input	Tracking zero cross. Tracking error signal is inputted with a C coupler. Although the time constant is determined by the 1 track jump situation, it is usually abou 2 kHz.
13	TE+	Input	Tracking error signal input.
14	ISET		Current value setting that determines the focus search voltage, tracking jump voltage and the carriage feed voltage.
15	VCC		Power supply terminal. Usually +5V.
16	SRCH		Connects a condensor that determines the focus search charge and discharge waveform time constant.



Pin No.	Pin name	1/0	Function and operation
17	Vee		Power supply terminal. –5V
18	FS3	Input	Focus amplifier gain selection terminal, OPEN or GND level,
19	ATSC	Input	Terminal that inputs data that indicates mechanical shock was applied to the player. Tracking error input through BPF.
20	FE	Input	Focus error signal input.
21	FEO	Output	Amp 1 output. Focus error signal output.
22	FE-	Input	Amp 1 invert input,
23	SLO	Output	Amp 3 output. Carriage servo signal output.
24	SL-	Input	Amp 3 invert input.
25	SL+	Input	Amp 3 non-invert input. Carriage servo signal input.
26	DIRC	Input	Utilized during 1 track jump, Usually "H", WHen "L" reverses the track jump pulse direction. Set to a normal tracking mode by "H". When TZC rise and fall detection occurs, it is "L" for a certain period of time.
27	TAO	Output	Amp 2 output, Tracking error signal output.
28	TA-	Input	Amp 2 invert input. Tracking error signal input.
29	TG1		Tracking amp gain selection terminal. Becomes OPEN or GND level.
30	GND		GND terminal

* IC1: CX20109



CX20109 Terminal Functions

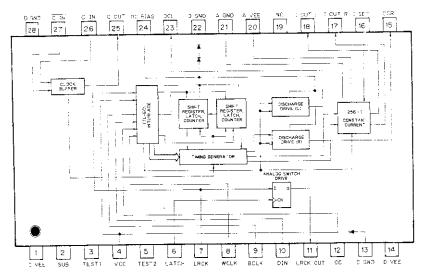
RF amplifier

Pin No.	Pin name	I/O	Function and operation
1	FOK	Output	Allows focus servo output. Active "H", PNP open collecter,
2	RFI	Input	RF summing amp output is C coupled for input,
3	RFO	Output	; RF summing amp output. Eye pattern test point,
4	RF-	Input	RF summing amp invert input, CR return connection to (3) $=$ (4).
5	PD1	Input	: RF I-V amp (1) invert input, Connects to PIN diode B+D for current input.



Pin No.	Pin name	1/0	Function and operation
6	PD2	Input	RF I-V amp (2) invert input, Connects to PIN diode A+C for current input.
7	AGND		Small signal analog system GND.
8	E	Input	E I-V amp invert input. Connects to PIN diode E for current input.
9	EF8	Output	E I-V amp output, CR return connection to (8) — (9).
10	FFB	Output	F I-V amp output. CR return connection to (10) - (11).
11	F	Input	F I-V amp invert input. Connects to PIN diode F for current input.
12	GND		
13	VEE		Negative power supply. –5V.
14	FE+	Input	Focus error amp non-invert input. Low pass CR connection,
15	FE-	Input	Focus error amp invert input.
16	FE	Output	Focus error amp output, CR return connection to (15) — (16).
17	ΤE	Output	Tracking error amp output.
18	MIRR	Output	Mirror output, Active "H". PNP open collector.
19	HC	Input	Mirror hold condensor connection terminal.
20	EFM	Output	EFM output comparator output.
21	VSEL	Input	Auto, asymmetry control amp reference input level selection terminal. Connects to +5V.
22	ASY	Input	Auto, asymmetry control input. Slice the RF signal to generate a square wave.
23	DVcc		EFM comparator system positive power supply. Connects to +5V,
24	Vcc		Positive power supply. Connects to +5V.

*1C301: CX20133



CX20133 Terminal Functions

16 bit D/A converter

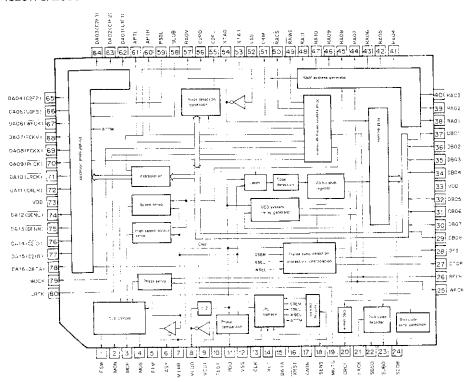
Pin No.	Pin name	1/0	Function and operation
1 ;	DVEE		- power supply terminal, -5V.
2	SUB		5∨
3	TEST1	İ	Not used
4	VCC		+ power supply terminal, +5V.
5	TEST2		Not used.
6	LATCH	Input	Clock input. When PAM waveform jitter exists, a conversion error occurs. D type flip flop clock for this jitter.



Pin No.	Pin name	1/0	Function and operation
7	LRCK	Input	44.1 kHz strobe signal input. Data assignment during the stereo mode. LRCK = "L" R ch data call. LRCK = "H" L ch data cali.
8	WCLK	Input	88.2 kHz strobe signal input. Word clock. Changes WCLK from "H" to "L" at 17th BCLK break, then 16 bit data is transferred from the shift register to the latch by this break signal.
9	BCLK	Input	Bit clock input. Data is sent to the IC sequentially from MSB by synchronization with the rise of this clock. (Data change is by BCLK break.)
10	DIN	Input	16 bit serial data input.
11	LRCKOUT	Output	TC4053BF (CMOS analog switch) drive output.
12	CC	Input	Conversion command. Changes CC to "H" and enters 3 clocks or more from CIN to reset all internal timing circuits. After reset, CC becomes "L" and enters a clock from CIN, then the internal timing circuit starts operating.
13	DGND		GND
14	DVEE		-5V
15	DCR	Output	Discharge signal Controlled by LRCK LRCK = "H" Output from DCR. LRCK = "L" Output from DCL
16	ISET	Input	Integrating current determination terminal. Integrating current is determined by a constant current value that flows from this terminal.
17	IOUTR	Output	Integrating current output terminal LRCK = "L" — — Output from IOUTL LRCK = "H" — — Output from IOUTR
18	IOUTL	Output	
19	NC		
20	AVEE		-5V
21	AGND		GND
22	DGND		GND
23	DCL	Output	Discharge signal Controlled by LRCK, LRCK = "L" Output from DCL. LRCK = "H" Output from DCR,
24	DCBIAS		Bias terminal Bias circuit for the discharge signal output circuit.
25	COUT	Output	Clock terminal, 35 MHz.
26	CIN	Input	Clock terminal, 35 MHz.
27	CIN	Input	Clock terminal, 35 MHz.
28	DGND		GND



*IC201: CX23035



CX23035 Terminal Functions

Digital signal processor

Pin No.	Pin name	1/0	Function and operation
1	FSW	Output	Spindle motor output filter time constant selection output.
2	MON	Output	Spindle motor ON/OFF control output.
3	MDP	Output	Spindle motor drive output. Rough control during CLV-S mode and phase control during CLV-P mode.
4	MDS	Output	Spindle motor drive output. Speed control during CLV-P mode.
5	EFM	Input	EFM signal input from RF amp.
6	ASY	Output	Output for EFM signal slice level control.
7	MIRR	Input	MIRROR input from RF amplifier. Connects to GND.
8	VC00	Output	VCO output. When EFM signal lock occurs, f=8,6436 MHz.
9	VCOI	Input	VCO input
10	TEST	Input	GND
11	PDO	Output	Phase comparison output of EFM signal and VCO/2.
12	VSS		GND
13	CLK	Input	PD8019E serial data transmission clock input. Latches data at the clock rise edge.
14	XLT	Input	PD8019E latch input. Latches 8 bit shift register data (serial data from PD8019E) to each register.
15	DATA	Input	PD8019E serial data input.
16	XRST	Input	System reset input. Reset with "L".
17	CNIN	Input	Tracking pulse input.
18	SENS	Output	Outputs internal status by address correspondence,
19	MUTG	Input	Muting input, When internal register ATTM is "L", MUTG is "L" which is a normal status, When "H", a silent status occurs.
20	CRCF	Output	Outputs the SUB-Q CRC result. (Not used)



Pin No.	Pin name	1/0	Function and operation
21	EXCK	Input	Clock input for SUB-Q serial output. (Not used)
22	\$BSO	Output	SUB-Q serial output, (Not used)
23	SUBQ	Output	SUB-Q output.
24	SCOR	Output	SUB-Q S0+S1 output.
25	WFCK	Output	Write Frame Clock output. When frame sync lock occurs, f = 7.35 kHz.
26	RFCK	Output	Read frame clock output, X'tal system 7.35 kHz.
27	GTOP	Output	Frame sync protective status display output. (Not used)
28	GFS	Output	Frame sync lock status display output.
29	DB08	1/0	External RAM data terminal, DATA 8 (MSB)
30	DB07	1/0	External RAM data terminal, DATA 7
31	DB06	1/0	External RAM data terminal, DATA 6
32	DB05	1/0	External RAM data terminal, DATA 5
33			Power supply terminal. +5V
34	DB04	1/0	External RAM data terminal, DATA 4
35	DB03	1/0	External RAM data terminal, DATA 3
36	DB02	1/0	. External RAM data terminal, DATA 2
37	DB01	1/0	External RAM data terminal, DATA 1 (LSB)
38	RA01	Output	External RAM address output, ADDR01 (LSB)
39	RA02	Output	External RAM address output, ADDR02
40	RA03	Output	External RAM address output, ADDR03
41	RA04	Output	External RAM address output, ADDR04
42	RA05	Output	External RAM address output, ADDR05
43	RA06	Output	External RAM address output, ADDR06
44	RA07	Output	External RAM address output. ADDR07
45	RA08	Output	External RAM address output, ADDR08
46	RA09	Ouptu	External RAM address output, ADDR09
47	RA10	Output	External RAM address output, ADDR10
48	RA11	Output	External RAM address output, ADDR11 (MSB)
49	RAWE	Output	Write enable signal output to external RAM. Active "L".
50	RACS	Ouput	Chip select signal output to external RAM, Active "L".
51	C4M	Output	X'tal 1/2 frequency division output, f = 4.2336 MHz.
52	VSS	Острат	GND
53	XTAL	Input	X'tal oscillation circuit input. f = 8.4672 MHz.
54	XTAO	Output	X'tal oscillation circuit output, f = 8,4672 MHz.
55	C2FL	Output	Correction status output. When C2 system correction attempt is not successful, "H" occurs.
56	C2PO	Outout	C2 pointer display output. Synchronized to audio data output. (Not used.)
57	RAOV	Output	= 4 frame jitter extraction RAM overflow and underflow display output.
58	SLOB	Input	Audio data output code selection input. With "L", 2's complement output. With "H", offset binary output,
59	PSSL	Input	Audio data output mode selection input. With "L", serial output, With "H", parallel output. (This unit uses "L".)
60	APTR	Output	Aperture compensation control output, "H" during R ch. (Not used.)
61	APTL	Output	Aperture compensation control output, "H" during L ch. (Not used.)
62	DA01	Output	When PSSL = "H", DA01 (parallel audio data LSB) output. When PSSL = "L", CIF1 output.

Pin No.	Pin name	1/0	Function and operation	
63	DA02	Output	When PSSL = "H", DA02 output.	
			When PSSL = "L", C1F2 output.	
64	DA03	Output	When PSSL = "H", DA03 output. When PSSL = "L", C2F1 output. (Not used.)	
65	DA04	Output	When PSSL = "H", DA04 output. When PSSL = "L", C2F2 output. (Not used.)	
66	DA05	Output	When PSSL = "H", DA05 output, When PSSL = "L", UFGS output, (Not used.)	
67	DA06	Output	When PSSL = "H", DA06 output. When PSSL = "L", WFCK output. (Not used.)	
68	DA07	Output	When PSSL = "H", DA07 output. When PSSL = "L", FCKV output. (Not used.)	
69	DA08	Output	When PSSL = "H", DA08 output, When PSSL="L", FCKX output, (Not used.)	
70	DA09	Output	When PSSL = "H", DA09 output, When PSSL = "L", PLCK output, (Not used.)	
71 ,	DA10	Output	When PSSL = "H", DA10 output, When PSSL = "L", TRCK output, (Not used.)	
72	DA11	Output	When PSSL = "H", DA11 output. When PSSL = "L" C4LR output. (Not used.)	
73	VDD		Power supply terminal5V	
74	DA12	Output	When PSSL = "H", DA12 output. When PSSL = "L", DENL output. (Not used.)	
75	DA13	Output	When PSSL = "H", DA13 output. When PSSL = "L", DENR outut. (Not used.)	
76	DA14	Output	When PSSL = "H", DA14 output, When PSSL = "L", C210 output.	
77	DA15	Output	When PSSL = "H", DA15 output. When PSSL = "L", C210 output. (Not used.)	
78	DA16	Output	When PSSL = "H", DA16 (parrallel audio MSB) output.	
			When PSSL = "L", DATA output.	
79	WDCK	Output	88.2 kHz strobe signal output	
80	LRCK	Output	44.1 kHz strobe signal output	

C1F1: C1 decode error correction status monitor output. C1F2:

C2F1:

C2 decode error correction status monitor output. C2F2:

UGFS: Unprotected frame sync pattern output. WFCK: WFCK invert output.

FCKV: WFCK/4 or WFCK/8 output. FCKX: RFCK/4 or RFCK/8 output.

 \overline{PLCK} : VCO/2 output. When locked to EFM signal, f = 4.3218 MHz.

C4LR: 176.4 kHz strobe signal

DENL: L-ch serial data enable signal.

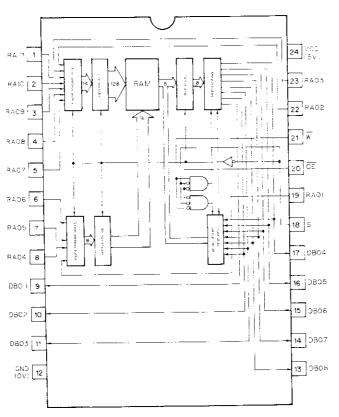
DENR: R-ch serial data enable signal.

C210: C210 invert output.

C210: Bit clock output. f = 2.1168 MHz.

DATA: Audio signal serial data output.

* 1C202: M5M5117FP



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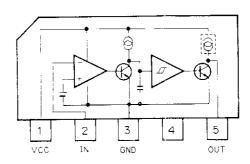
M5M5117FP Terminal Functions

RAM

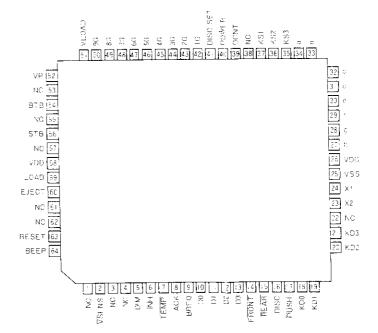
Pin No.	Pin name	1/0	Function and operation	
1 – 8	RA11 – RA04	Input	Address input	
9 – 11	DB01 - DB03	1/0	Data I/O	
12	GND		0V	
13 17	DB08 - DB04	1/0	Data I/O	
18	S	Input	Chip select input, "L" during write-in and read out.	
19	A10	Input	Address input	
20	ŌĒ	Input	Output enable input, "L" during read out.	
21	W	Input	Write control input. "L" during wite-in, "H" during read out.	
22, 23	RA02, RA03	Input	Address input.	
24	Vcc	-	+5V	

• Display Unit

IC702: M51956BL



* IC701: PD4074D



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PD4074D Terminal Functions

System controller

Pin No.	Pin name	1/0	Function and operation	
1	NC	í		
2	VSENS	Input	ACC voltage detection circuit signal input terminal. CMOS input, ACC ON: "L" ACC OFF: "H"	
3	NC		i	
4	NC			
5	DIM	Input	Dimmer control input terminal, CMOS input, Changes FL tube dynamic drive duty to perform, "H": Dimmer ON "L": Dimmer OFF	
6 .	ĪNĦ	Input	+B disable detection terminal. CMOS input, Operation stops with "L" to wait until "H" occurs.	
7	TEMP	Input	High temperature detection terminal, CMOS input. With "L", a high temperature judgement is made to stop system operation.	
8	ACK	Input	Communication control line ■ Data link control Communication mode is determined by the level of this signal. ■ Handshake control Communication direction (PD4074D → PD8019E) Indicates that outputted data was accepted by PD8019E when this signal rises. Communication direction (PD8019E → PD4074D) Indicates that data outputted by PD8019E is effective when this signal breaks.	
9	BREQ	1/0	Communication control line, CMOS I/O. • Data link control When "L" occurs by PD8019E, the communication mode is determined by the ACK level outputted by PD8019E.	
İ		: 	ACK Communication mode	
			"L" Command send enable status for PD8019E. When a command to be sent exists, a communication status occurs with STB "L".	
i			"H" Data send request status from PD8019E. PD4074D must immediately accept the request with STB"L"	
			 Handshake control When a data string is sent, "L" output occurs when the first data is sent and termination of the last data string is indicated by "H" when the last data is sent 	
10 - 13	D0 - D3	I/O	Communication data bus, For CMOS I/O.	
14	FRONT	Input	FRONT switch detection terminal, CMOS input. Terminal that detects if the plate unit (mechanism part) is at the front or not. (If it is at the front, it is "L"). Indicates eject completion.	
15	REAR	Input	REAR switch detection terminal, CMOS input. Terminal that detects if the plate unit is at the back or not, ("L" if at the back Indicates loading completed.	
16	DISC	Input	DISC switch detection terminal, CMOS input. Terminal that detects if a disc is inserted or not, "H" if a disc is present.	
17	PUSH	Input	PUSH switch detection terminal, CMOS input, Terminal that detects if an inserted disc is pressed ro not, "L" if pressed,	
18	KD0	Input	KEY input terminal by matrix with KS3—KS1. CMOS input.	
19	KD1	Input	KS3 KS2 KS1	
20	KD2	Input	KDD LJECT FF SOAN	
21	KD3	Input	KD1 REL/PLAY REV V-PLAY	



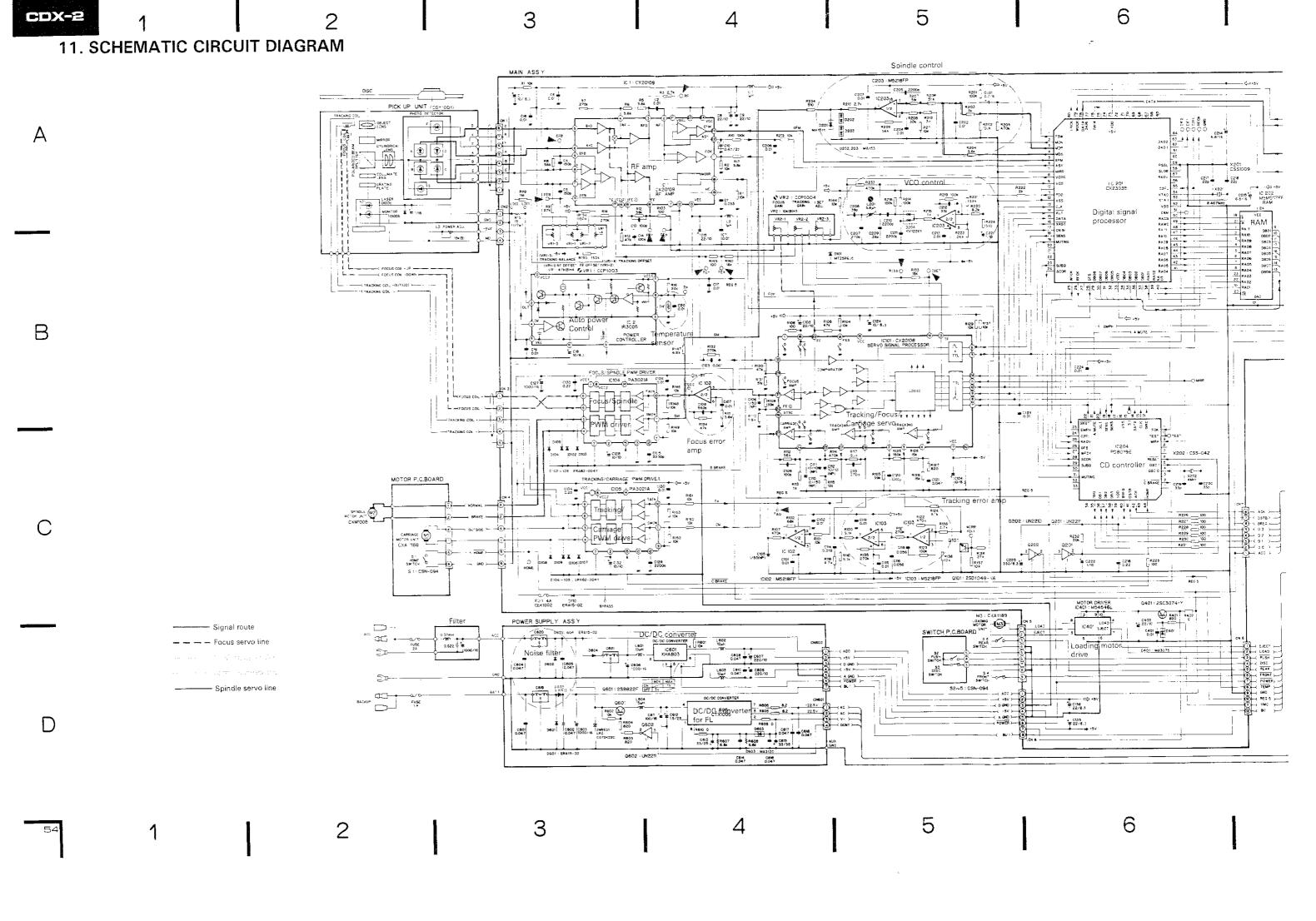
Pin No.	Pin name	1/0	Function and operation	
22	NC		GND	
23	X2		Clock oscillation terminal, 4 MHz	
24	X1		Clock oscillation terminal,	
25	Vss	:	GND	
26	VDD	-	Power supply terminal, ÷5V	
27	h	Output		
28	9	Output	1	
29	f	Output	1	
30	e	Output		
31	d	Output	FL anode output, P-ch open drain with pull down.	
32	c	Output	: -	
33		-	1	
	b	Output	_	
34	8	Output		
3E :	KS3	Output		
36	KS2	Output	Strobe output for key scan.	
37	KS1	Output	P-ch open drain no pull down.	
38	NC		10° No.	
38	DCNT	Output	FL display DC/DC converter control terminal. P-ch open drain no pull down. Power is supplied to the DC/DC converter with "H".	
40	POWER	Output	Servo system DC/DC converter control terminal. P-ch open drain no pull down. With "H", PD8019D reset start, DC/DC converter ON.	
41	DISC SET	Output	LED (DISC SET) control terminal During disc loading: FIGURE Disc set: "H"	
42 – 50	1G – 9G	Output	FL grid output, P-ch open drain with pull down,	
51 .	VLOAD	Input	FL driver power supply. –30V	
52 .	VP	Input	FL driver power supply. Connects to GND.	
53	NC			
54	ВТВ	Output	AUX B output terminal, CMOS output. With "H", +B output from AUX connecter.	
55	NC		The supplied of the supplied o	
56	STB	Output	Communication control line. CMOS output. • Data link control Outputs "H" for a data send request from PD8019E to notify data send request acceptance. • Handshake control Communication direction (PD4074D → PD8019E) Outputs "L" to indicate that output data is effective for PD8019E. Communication direction (PD8019E → PD4074D) Outputs "H" to indicate that data output from PD8019E was accepted.	
57	NC	İ	GND	
58	VDD	—i	Power supply terminal, +5V	
59	LOAD	Output	Disc load control terminal, CMOS output, LOAD with "H".	
60	EJECT	Output	Disc Eject control terminal, CMOS output. EJECT with "H".	
61	NC		,,	
62	NC		<u>i</u>	
63	RESET	Input	Reset terminal, CMOS input,	
			"H": Reset ON" "L": Reset OFF	

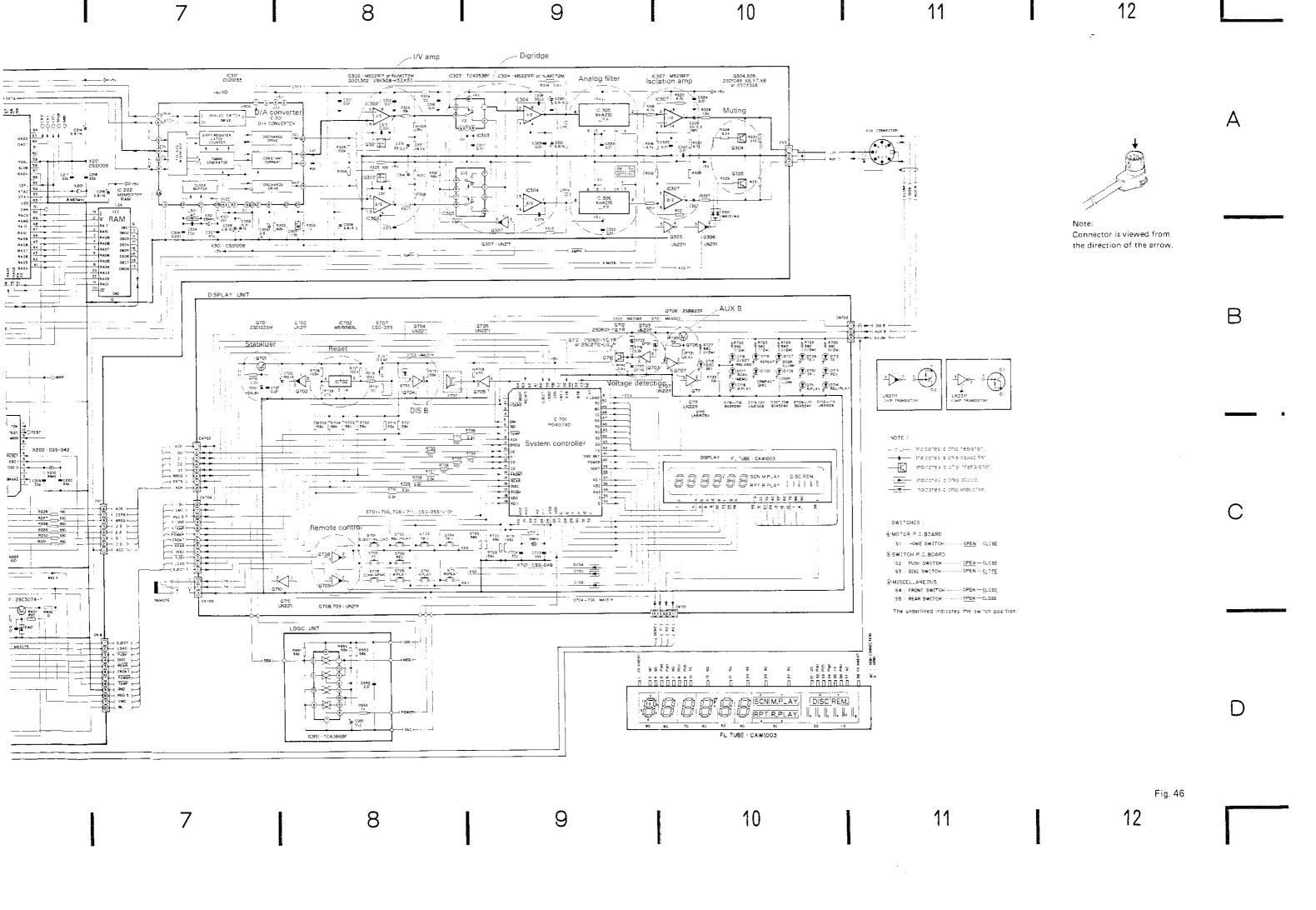
52

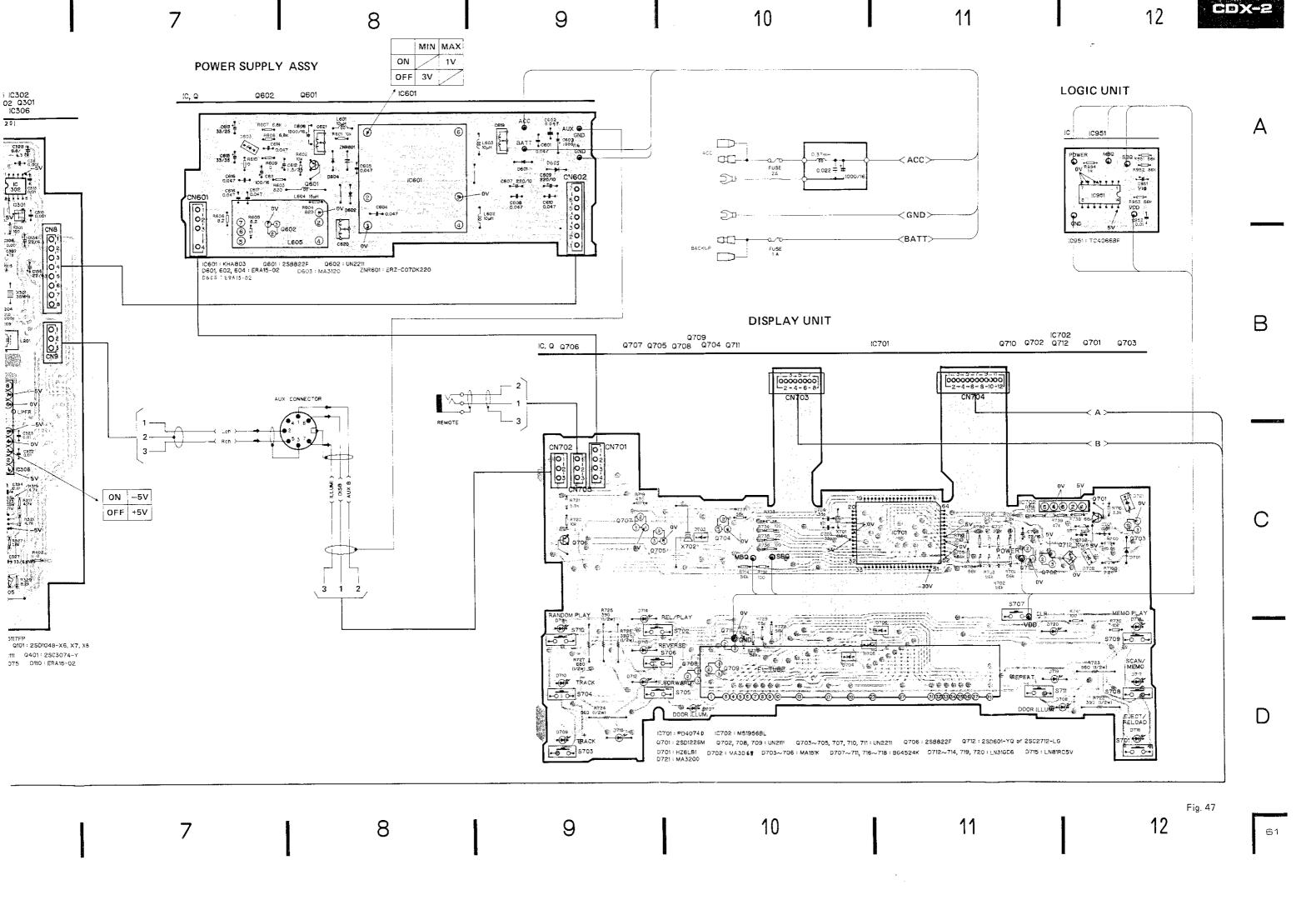
53

D

В





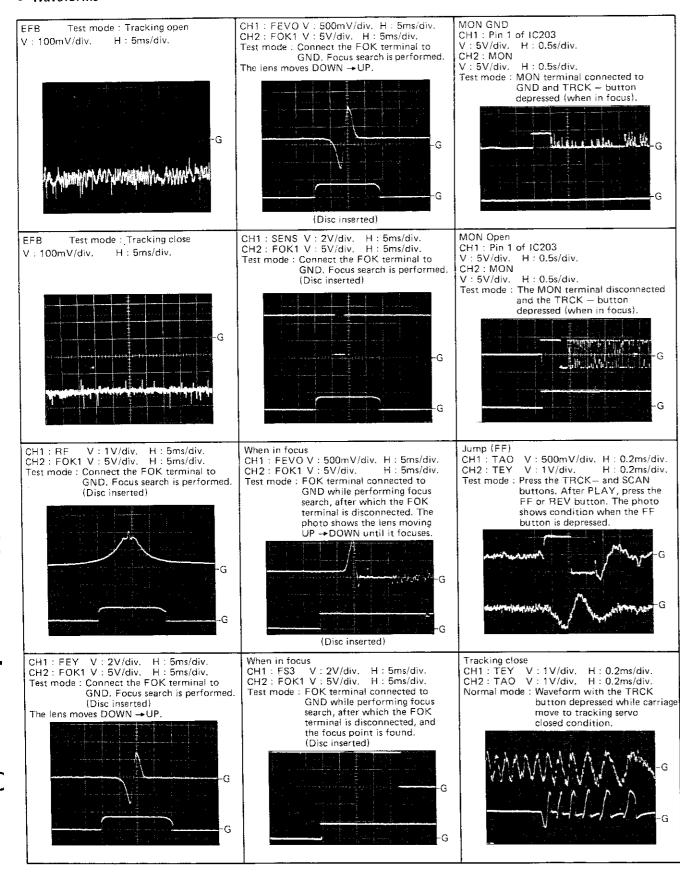


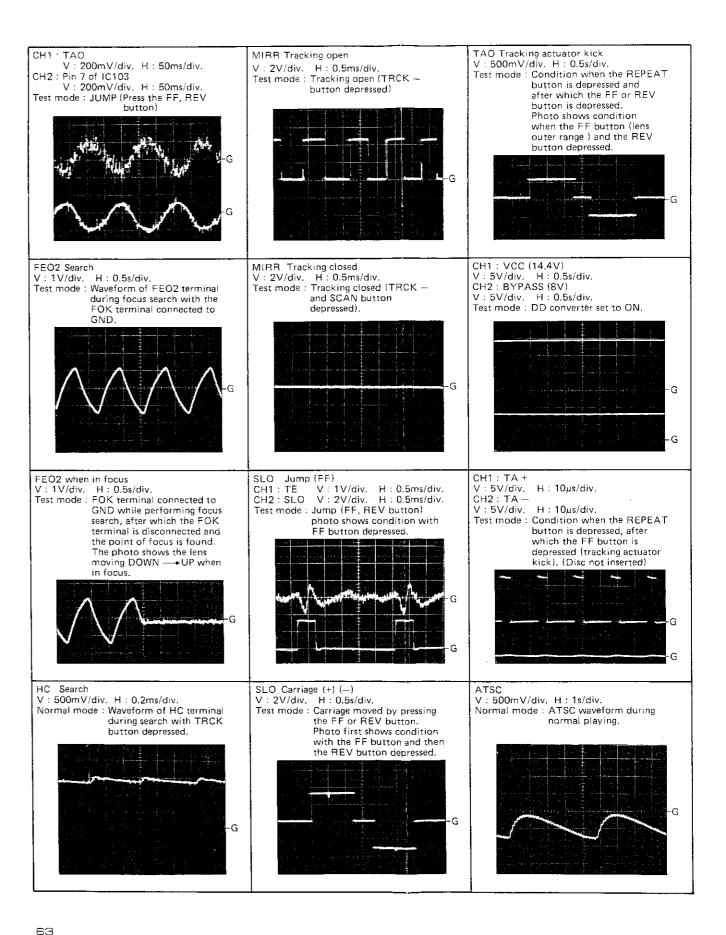


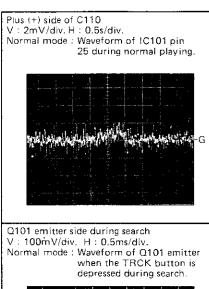
Waveforms

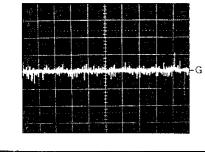
В

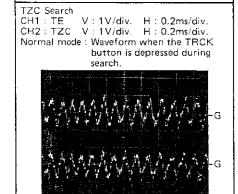
62











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13. CHASSIS EXPLODED VIEW

NOTE:

- For your parts Stock Control, the fast moving items are indicated with the marks ★ ★ and ★.
 - **: GENERALLY MOVES FASTER THAN *.

This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

- Parts whose parts numbers are omitted are subject to being not supplied.
- Parts marked by "•" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.

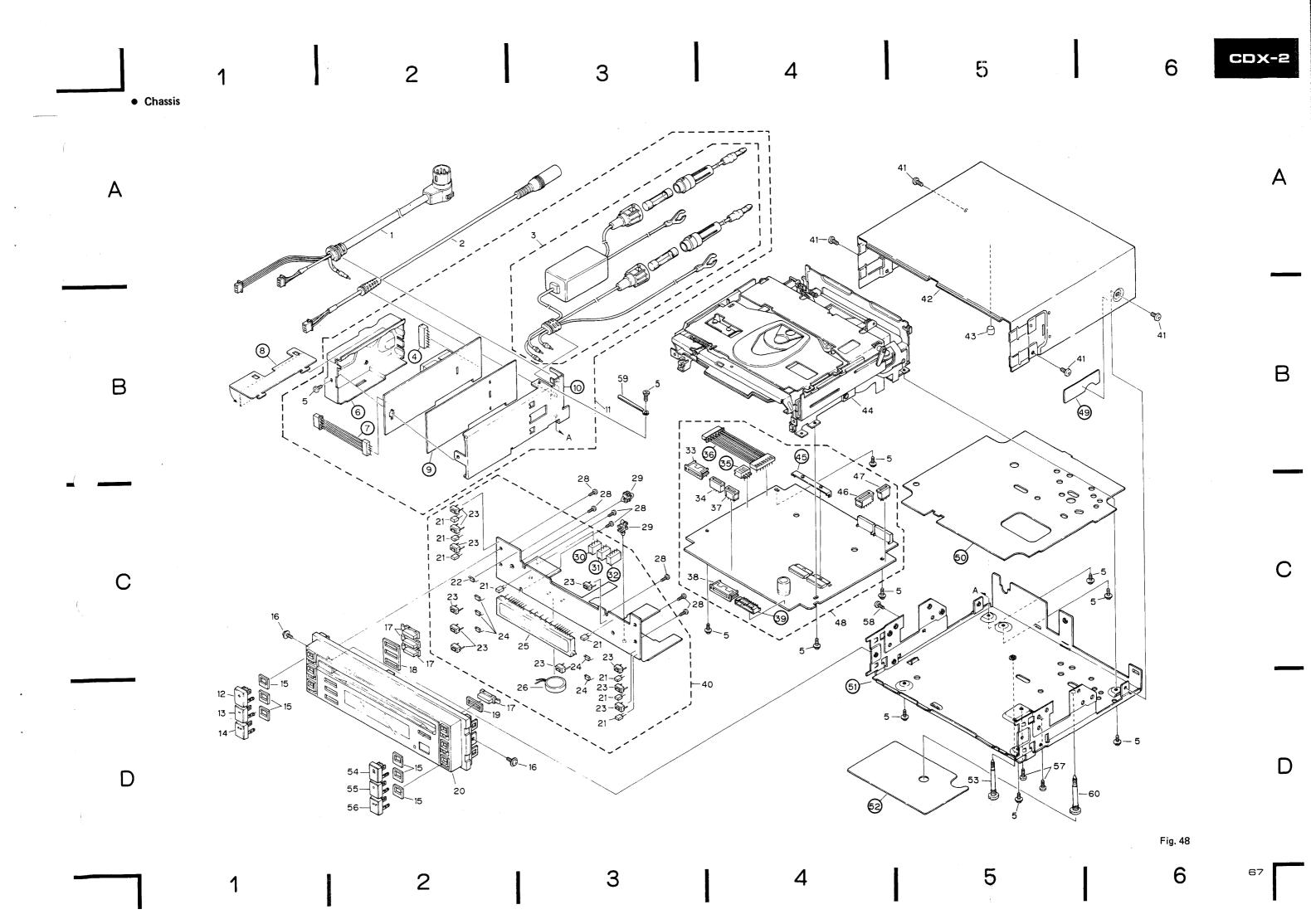
• Parts List

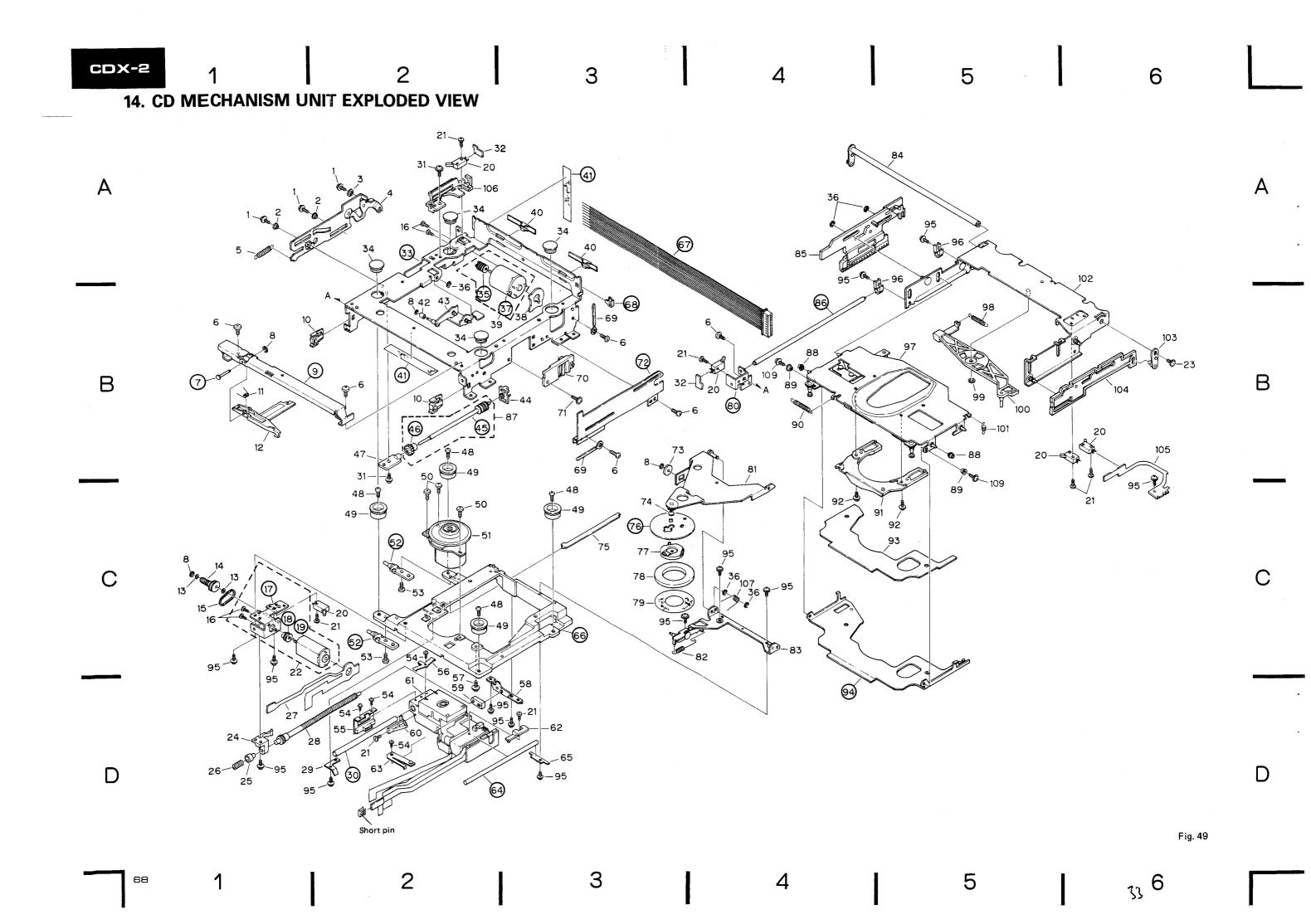
Mark	No.	Part No.	Description	Mark	No.	Part No.	Description
	1.	CDK-403	DIN Cord		31.		Plug
	2.	CDE1161	Cord		32.		Plug
	3.	CDK-402	Cord		33.	CKS1063	Connector
	4.		Plug		34.	CKS-721	Connector
	5.	PMS26P040FMC	Screw		35.		Plug
	6.		Shield Case		36.		Connector
	7.		Connector		37.	CKS-720	Connector
	8.		Clamper		38.	CKS1122	Connector
	9.		Insulator		39.		Plug
	10.		Shield Case	•	40.	CWX1020	Display Unit
•	11.	CWR1001	Power Supply Assy		41.	CBA-178	Screw
*		CAE-246	Button (TR+)		42.	CNB1049	Case
*		CAE-247	Button (TR-)		43.	CNM1166	Cushion
*		CAE-248	Button (R·PLAY)	•	44.	CXK2010	CD Mechanism Unit
	15.	CNM1100	Cushion		45.		Bracket
	16.	PMS30P050FMC	Screw		46.	CK\$1070	Connector
*	17.	CAC1081	Button		47.	CKS-719	Connector
	18.	CNM1101	Cushion	•	48.	CWX1019	Main Assy
	19.	CNM1102	Cushion		49.		Insulator
	20.	CXA1506	Grille Unit		50.		Insulator
*		BG4524K	LED		51.		Chassis
*		LN81RC5V	LED		52.		Seal
	23.	CSG-255	Switch		53.	CBA1019	Screw
*	24.	LN31GC6	LED		★ 54.	CAE-243	Button (EJECT)
	25.	CAW1003	FL Tube		★ 55.	CAE-244	Button (SCAN)
	26.	CPV 1005	Buzzer		★ 56.	CAE-245	Button (M·PLAY)
	27.	VACANT			57.	BMZ26P060FMC	Screw
	28.	BPZ20P060FMC	Screw		58.	CMZ26P040FMC	Screw
	29.	CNV1154	Holder		59.	CEF-007	Clamper
	30.		Plug		60.	CBA1049	Screw

Note:

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^{*}Two screws labeled 53 and 60 are attached to the back of the set to protect it in transit. If the set is shipped (i.e., for repairs), be sure to protect your set by re-attaching these screws.







rk	1. 2. 3. 4. 5.	PMS20P040FMC CLA1102 CLA1037	Description Screw		56. 57.	CBL1003 CBA1052	Spring Screw
	1. 2. 3. 4.	CLA1102			57.	CBA1052	Screw
	2. 3. 4.	CLA1102					
	3. 4.		0 - 11 - 11		58.	CNC1068	Holder
	4.	CLA1037	Collar		59.	CNV1055	Holder
	4.		Collar		60.	CNV1059	Spacer
		CXA1057	Lever Unit		00.	01111000	
	٥.	CBH1024	Spring		61	CCV1001	Pickup Unit
		0502			61.	CGY1001	•
		BMZ26P040FMC	Screw		62.	CNV1060	Guide
	6.	BIVIZZOFU4UFIVIC			63.	CNV1064	Spacer
	7.		Shaft		64.		Shaft
	8.	YE12FUC	Washer		65.	CNC1069	Holder
	9.		Bracket				
	10.	CNV1080	Clamper		66.		Chassis
					67.		Connector
	11.	CBH1025	Spring		68.		Clamper
	12.	CNV1130	Arm			UEE 102	Clamper
	13.	HBF-117	Washer		69.	HEF-102	,
			Gear		70.	CNV1081	Clamper
	14.	CNV1205					
**	15.	CNT-114	Belt		71.	PMS26P040FUC	Screw
			_		72.		Bracket
	16.	HBA-175	Screw		73.	CLA1093	Roller
	17.		Bracket Unit		74.	CNM1056	Washer
	18.		Pulley		75.	CNM1118	Spacer
	19.		Motor		70.	CHIMICITO	5,000
	20.	CSN-094	Switch				Dist
**	20.	C314-03-4	Owner.		76.		Plate
			0		77.	CNV1061	Guide
	21.	CBA1025	Screw		78.	CNR1009	Magnet
**	22.	CXA1188	Motor Unit (Carriage)		79.	CNM1055	Feit
	23.	PMS20P040FMC	Screw		80.		Bracket
	24.	CNV1054	Holder				
	25.	CNV1058	Spacer		81.	CXA1052	Arm Unit
		_	·				
	26.	CBH1008	Spring		82.	CBH1010	Spring
			P.C. Board		83.	CXA1167	Bracket Unit
	27.	CNP1201			84.	CXA1062	Arm Unit
	28.	CXA1056	Gear Unit		85.	CNV1072	Lever
	29.	CNC1067	Holder				
	30.		Shaft		86.		Shaft
					87.	CXA1455	Gear Unit
	31.	PMS26P040FUC	Screw		88.	CLA1067	Roller
	32.	CNP1200	P.C. Board				Collar
	33.	0.11. 12.00	Chassis		89.	CLA1102	
		ONIV/1100	Spacer		90.	CBH1014	Spring
	34.	CNV1199	·				
	35.		Gear		91.	CNV1077	Cover
					92.	PMS20P025FMC	Screw
	36.	YE15FUC	Washer		93.	CNM1379	Sheet
	37.		Motor		94.		Tray
	38.		P.C. Board		95.	CBA1026	Screw
	k 39.		Motor Unit (Loading)		30,	00/10/20	U U. U. I
^ ′	40.		Clamper		00	CNIV/4 074	Guida
	₩.	G111 1200	erenge"		96.	CNV1071	Guide
			Cover		97.	CXA1064	Plate Unit
	41.		Cover		98.	CBH1012	Spring
	42.		Roller		99.	YE20FUC	Washer
	43.		Arm Unit		100	. CNV1074	Arm
	44.	CNV1070	Guide				
	45.		Shaft		101	. CBH1013	Spring
						. CXA1060	Plate Unit
	46.		Gear				
			Guide			. CXA1063	Arm Unit
	47.					. CNV1073	Lever
	48.		Screw		105	. CNP1202	P.C. Board
	49.		Bush				
	50.	CBA1013	Screw		106	. CNV1129	Guide
					107		Spring
	★ 51.	CXM1005	Motor Unit (Spindle)				Op: mg
*			Shaft			. VACANT	_
	52.				109	. BMZ20P040FMC	Screw
	53.		Screw				
	54	. НВА-161	Screw				
	55	. CNV 1063	Rack				



15. ELECTRICAL PARTS LIST

NOTE:

When ordering resistors, first convert resistance values into code form as shown in the following examples.

- Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%). 56×10^{1} 561 RD1/4PS 5 6 1 J 560Ω $47k\Omega$
 - 47×10^{3} 473..... RD1/4PS 4 7 3 J OR5 RN2H 0 R 5 K 0.5Ω 1Ω 010 RS1P @ 1 0 K
- Ex. 2 When there are 3 effective digits (such as in high precision metal film resis-
- For your parts Stock Control, the fast moving items are indicated with the marks $\star \star$ and \star .
 - * *: GENERALLY MOVES FASTER THAN *.

This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

- Parts whose parts numbers are omitted are subject to being not supplied.
- The part numbers shown below indicate chip components. Chip Resistor

 $RS1/8S \square \square \square J$

Chip Capacitor (except for COS)

CKS...., CCS.....

Main Assy

MISCELLANEOUS

rk	Symbol & Description	Part No.	Mark	Symbol & I	Description	Part No.
**	IC1	CX20109	*	D202, 203	Chip Diode	MA153
**		IR3C05	*	D204		KV1226Y
	10101	CX20108	*	D301	Chip Diode	MA151WA
	IC102, 103, 203, 307	M5218FP	*	D401	Chip Diode	MA3075
	IC104, 105	PA3021A		L1, 2	Ferri-Inductor	CTF1007
	10201	CX23035		L201	Coil	CTA1001
	IC201	M5M5117FP		L301	Inductor	CTF1006
	10202	PD8019E	*	TH1	Thermister	CCX-021
	IC204	CX20133	**	VR1	Semi-fixed, 47kΩ (B)x4	CCP1003
	IC301			VR2	Semi-fixed, 10kΩ (B)x3	CCP1004
**	10302, 304	M5221FP			•	
		(NJM072M)		X201	X'tal 8.467MHz	CSS1009
		T04050D5		X202	Ceramic Resonator	CSS-042
	10303	TC4053BF		X301	X'tal 35MHz	CSS1008
	10305, 306	KHA210A	**	FU1	Fuse, 4A	CEK 1002
* *		M54546L			. 255,	021(1002
**		UN2211	RESIST	ORS		
* *		UN221D		-		
**	Q301, 302 Chip Transistor	2SK508-K52 or	Mark	Symbol &	Description	Part No.
		2\$K508-K53		R15		RS1/2P150JL
* *	Q304, 305 Chip Transistor	2SD1048-X6 or		R156		RS1P220JL
		2SD1048-X7 or		R316-323	1760	
		2SD1048-X8 or				CCN-140
		2SC3326		Other Nesi	stors (Chip Resistors)	RS1/10S□□□J
**	Q306, 307 Chip Transistor	UN2111				
**	Q401	2\$C3074-Y				
*	D101	MTZ5R6JC				
*	D102 — 109	ERA82-004Y				
*	D110	ERA15-02				
*	D201 Chip Diode	MA151K				



CAPACITORS

Power Supply Assy MISCELLANEOUS

rk	Symbol & Description	Part No.	MISCEL	LANEOUS	j	
	C1, 18	CSYA100M6R3OS	Mark	Symbol & D	Description	Part No.
	C2, 6, 7, 16, 17, 19, 20, 101, 102,	CKSYB103K50L	**	IC601	Converter	KHA803
	107, 115, 119, 126, 130, 202 – 204,		**	Q601		2SB822F
	206, 213			Q602	Chip Transistor	UN2211
	C4, 5	CCSSL151J50L		D601, 602,	· ·	ERA 15-02
	01, 0				Chip Diode	MA3120
	C8, 9, 15, 402	CEA220M10LS	*	D603	Chip blode	WA3120
	C10 Chip Capacitor	CSZSR47M20		L601, 602	Coil	CTH-035
	C11	CKSYB333K25			Coil	CTH1006
	C13, 14, 109	CCSSL101J50L		L603		
		CSZS220M10		L604	Ferri-Inductor	CTF-078
	C103 Chip Capacitor	C020220W10		L605	Transformer	CTX 1005
	0404 424	CEA100M6R3LS	*	ZNR601	Surge Absorber	ERZ-C07DK220
	C104, 124					
	C105, 106	CEA010M50NPLL	RESIST	ORS		
	C108	CCSSL561J50L	Manula	Cumbal 9	Description	Part No.
	C110	CEAORIM50NPLL	Mark	Symbol &	Description	1 01 (110.
	C111, 112	CEA100M10NPLL		R601 - 61	0	RS1/8S□□□J
	0113 207	CCSCH271J50L				
	C113, 207 C114	CKSYB183K25L	CAPAC	ITORS		
	C114 C116, 118	CKSYB563K25	Mark	Symbol &	Description	Part No.
	C120	CCSSL152J50L			004 005 000 010 014	CKSYF473Z50
	C121	CKSYB473K25			, 604, 605, 608, 610, 614,	CK31F473250
	C121	0.10101701120		616 – 6		00114000
		CCCCI 102 IEOI		C603, 606	1000μF/16V	CCH1003
	C123, 306, 310, 311	CCSSL102J50L		C607, 609		CEAUH221M10
	C125, 129, 205, 210, 211	CKSYB222K50L		C611		CEA101M16LL
	C127 1000µF/16V	CCH1003				
	C128, 132	CEA100M10LS		C612		CSYA1R5M250
	C133, 134, 218	CKSYF224Z25		C613		CEA330M25LL
				C615		CEA330M35LL
	C135, 136	CSYA220M6R3OS			Files	CCG1001
		CKSYB103K50L		C619, 621	Filter	
	C139, 224	CSZS2R2M6R3		C620		CCG-104
	C201 Chip Capacitor					
	C208, 209	CCSCH390J50L				
	C212, 219, 220	CCSCH330J50L	Displa	y Unit	·	
			MISCE	LLANEOU	JS	
	C214, 215, 302, 309	CSZA6R8M16L				
	C214, 215, 302, 309	CSZA6R8M16L CCSCH220J50L	Mark	Symbol &	Description	Part No.
	C216, 217	CCSCH220J50L	Mark		Description	
	C216, 217 C221, 222, 303 Chip Capacitor	CCSCH220J50L CSZS010M10		Symbol & IC701	Description	Part No. PD4074D
	C216, 217 C221, 222, 303 Chip Capacitor C225	CCSCH220J50L CSZS010M10 CEA331M6R3L2	**		Description	
	C216, 217 C221, 222, 303 Chip Capacitor	CCSCH220J50L CSZS010M10 CEA331M6R3L2	**	IC701	Description	PD4074D
	C216, 217 C221, 222, 303 Chip Capacitor C225	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L	**	IC701 IC702 Q701		PD4074D M51956BL 2SD1226M
	C216, 217 C221, 222, 303 Chip Capacitor C225	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L	**	IC701 IC702 Q701 Q702, 70	3, 709 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 – 325, 329	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L	**	IC701 IC702 Q701 Q702, 70	8, 709 Chip Transistor 05, 707, 710, 711	PD4074D M51956BL 2SD1226M
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 – 325, 329	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L	**	IC701 IC702 Q701 Q702, 70	3, 709 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 – 325, 329 C304 C307 C308, 320, 321, 328	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L	* 1 * 1 * 1 * 1	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711	PD4074D M51956BL 2SD1226M UN2111 UN2211
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS	* 1 * 1 * 1 * 1	IC701 IC702 Q701 Q702, 70	8, 709 Chip Transistor 05, 707, 710, 711	PD4074D M51956BL 2SD1226M UN2111 UN2211
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 – 325, 329 C304 C307 C308, 320, 321, 328	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50	***	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711	PD4074D M51956BL 2SD1226M UN2111 UN2211
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 – 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS	***	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS	***	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS	***	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C 1C701 C 1C702 C Q701 C Q702, 70 C Q703 — 7	8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C701 C702 C701 C702 C701 C702, 70 C703 - 7 C706 C702 8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or	
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C701 C702 C701 C702, 70 C703 - 7 C706 C701 C702 C701 8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1 MA3068	
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C701 C702 C701 C702 C701 C702 C703 C703 C703 C704 C705 8, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor Chip Transistor	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1	
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C 10701 C 10702 C 10701 C 10702, 70 C 10703 – 7 C 10706 C 10706 C 10701 C 10702 C 10703 – 7 C 10707 – 7	20, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor Chip Transistor Chip Diode Chip Diode Chip Diode Chip Diode Chip Diode Chip Diode Chip Diode	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1 MA3068 MA151K BG4524K
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C 10701 C 10702 C 10701 C 10702, 70 C 10703 – 7 C 10706 C 10706 C 10701 C 10702 C 10703 – 7 C 10707 – 7	20, 709 Chip Transistor 205, 707, 710, 711 Chip Transistor Chip Transistor Chip Diode 206 Chip Diode 211, 716 — 718 LED	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1 MA3068 MA151K BG4524K LN31GC6
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C 10701 C 10702 C 10701 C 10702, 70 C 10703 – 7 C 10706 C 10706 C 10701 C 10702 C 10703 – 7 C 10707 – 7	20, 709 Chip Transistor 05, 707, 710, 711 Chip Transistor Chip Transistor Chip Diode Chip Diode Chip Diode Chip Diode Chip Diode Chip Diode Chip Diode	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1 MA3068 MA151K BG4524K LN31GC6 LN81RC5V
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C701	20, 709 Chip Transistor 205, 707, 710, 711 Chip Transistor Chip Transistor Chip Diode 206 Chip Diode 211, 716 — 718 LED	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1 MA3068 MA151K BG4524K LN31GC6
	C216, 217 C221, 222, 303 Chip Capacitor C225 C301, 313, 316, 317, 322 — 325, 329 C304 C307 C308, 320, 321, 328 C312 C314, 315 C318, 319 C326, 327 33µF/6.3V	CCSCH220J50L CSZS010M10 CEA331M6R3L2 CKSYB103K50L CCSCH330J50L CCSCH470J50L CSYA6R8M6R3OS CKSYB103K50 CEA220M6R3LS CCSSL391J50L GGF-809	***	C701 C702 C701 C702 C701 C702 C703 C706 C704 C705 20, 709 Chip Transistor 205, 707, 710, 711 Chip Transistor Chip Transistor Chip Diode 206 Chip Diode 211, 716 — 718 LED 214, 719, 720 LED LED	PD4074D M51956BL 2SD1226M UN2111 UN2211 2SB822F 2SD601-YQ or 2SD601-YR or 2SC2712-LG or 2SC2712-LL HZ6LB1 MA3068 MA151K BG4524K LN31GC6 LN81RC5V	

CSG-255

CAW1003

★★ \$701 - 711 Switch

FL Tube

:DX-2

RESISTORS

Mark	Symbol & Description	Part No.	
	R722 - 727	RS1/2P□□□JL	
	Other Resistors	R\$1/8\$□□□J	

CAPACITORS

Mark	Symbol & Description	Part No.
	C701	CKSYB103K50
	C702	CEA101M6R3LS
	C703, 704	CCSCH330J50
	C705	CEA220M16LS

Switch P.C. Board

Mark	Symbol &	Description	Part No.
**	S2, 3	Switch (Push, Disc)	CSN-094

Motor P. C. Board

Mark	Symbol &	Description	Part No.
**	M1	Motor Unit (Carriage)	CXA1188
**	S1	Switch (Home)	CSN-094

Logic Unit

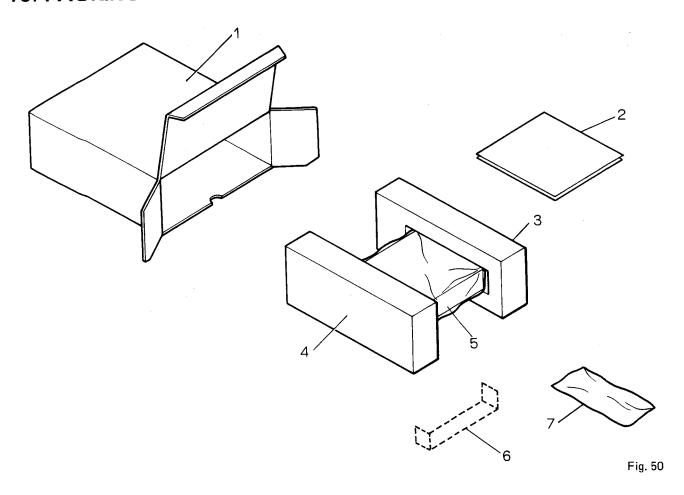
Mark	Symbol & Des	cription	Part No.	
**	IC951		TC4066BF	
	R951 - 954	Chip Resistor	RS1/10S□□□J	
	C951 Ch	ip Capacitor	CSZS010M10TL	
	C952		CKSQYB103K50	

Miscellaneous Parts List

Mark	Symbol	& Description	Part No.	
	Pickup U	Jnit	CGY1001	
**	M2	Motor Unit (Spindle)	CXM1005	
**	M3	Motor Unit (Loading)	CXA1189	
**	S4. 5	Switch (Front, Rear)	CSN-094	



16. PACKING METHOD

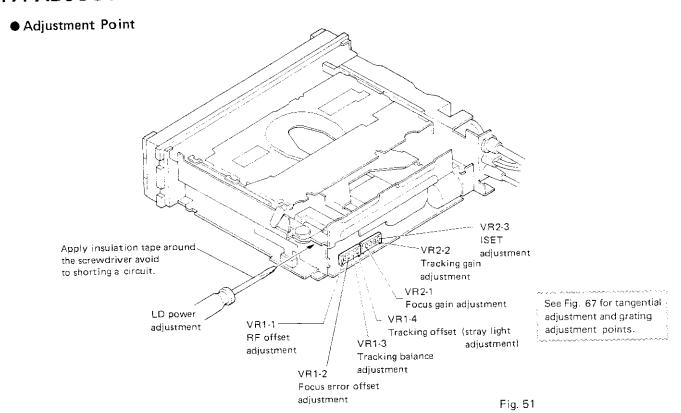


• Parts List

Mark	No.	Part No.	Description
	1.	CHG1077	Carton
	2.	CRD1041	Owner's Manual
			(English, French, German, Spanish)
		CRD1042	Owner's Manual
			(Swedish, Norwegian, Dutch, Italian
			Card
	3.	CHP1036	Styrofoam (L)
	4.	CHP1037	Styrofoam (R)
	5.	CEG-114	Cover
		CRP1004	Caution Card
	6.	CNB-723	Mounting Bracket
	7.	CEA1108	Accessory Kit
	7-1.	CNF-111	Strap
	7-2.	CNN-058	Spacer
	7-3.		Screw Kit
	7-3-1.	CBA-102	Screw
	7-3-2.	HMF40P080FZK	Screw
	7-3-3.	NF50FMC	Nut



17. ADJUSTMENT



Test Point

MAIN ASSY

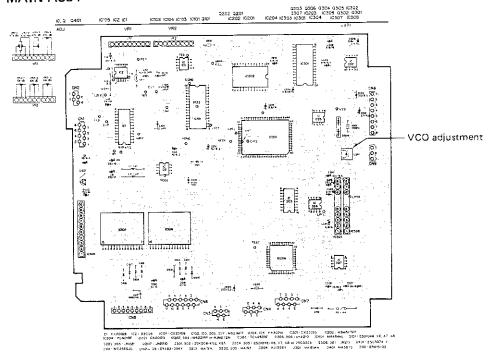


Fig. 52



• Test Mode

1) Starting Starts by simultaneously pressing $\overline{TR}+\overline{TR}-\overline{Clear}$ to light all displays.

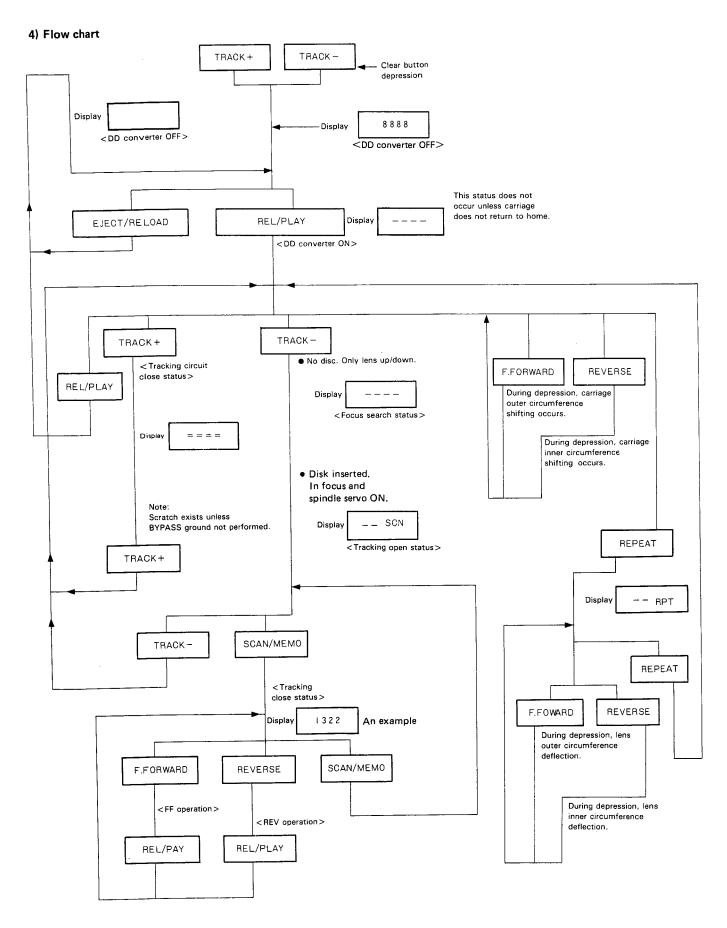
2) Functions

Button name	Operation
EJÉCT/RELOAD	Disc load, eject.
REL/PLAY	DD converter ON, OFF. However, during continuous jump, play occurs with jump release.
F-FORWARD REVERSE	* In case DD converter is ON, Focus tracking OFF. • Repeat display OFF Carriage FWD/REV • Repeat display ON Tracking actuator FWD/REV *In case DD converter is ON, Focus tracking ON. • FWD/REV continuous jump
TRACK+	Carriage, tracking loop switch individual ON-OFF. (IC101 CX20108 system adjustment function)
TRACK-	Focus search ON-OFF
SCAN/MEMO	Tracking servo ON-OFF
REPEAT	* In case DD converter is OFF All display segments ON-OFF. * In case DD converter is ON. REPEAT display ON-OFF (FWD/REV function selection).

3) Display

Display	Status	
	Indicates DD converter OFF. However, all lighting enabled by REPEAT.	
	Indicates DD converter ON.	
scn	Indicates DD converter ON. Focus closed.	
8.12.345	Indicates tracking close.	
	Indicates tracking close, non-drive.	

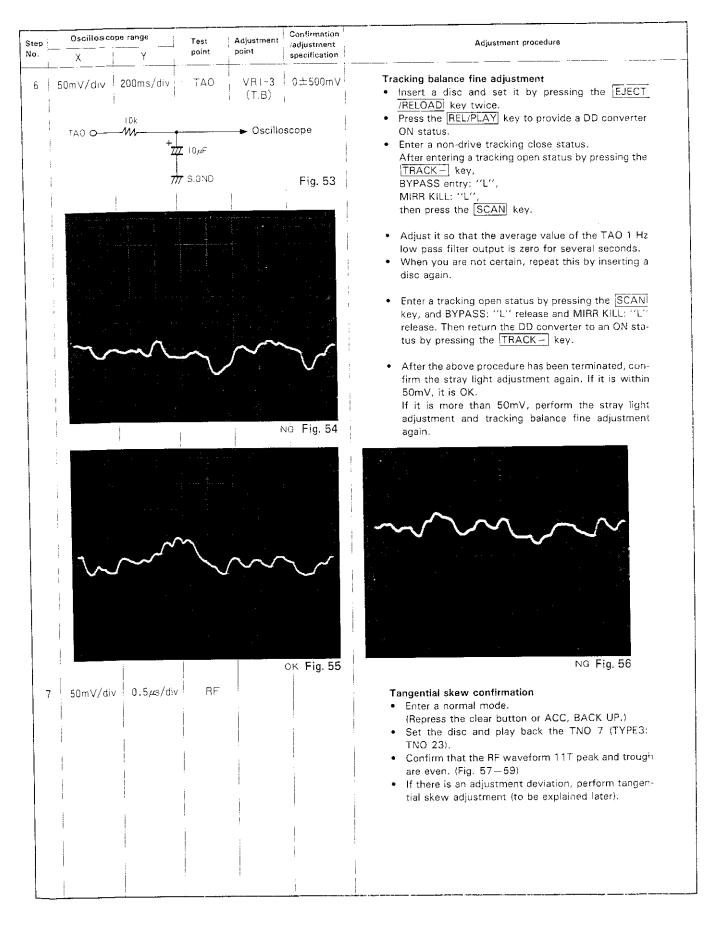




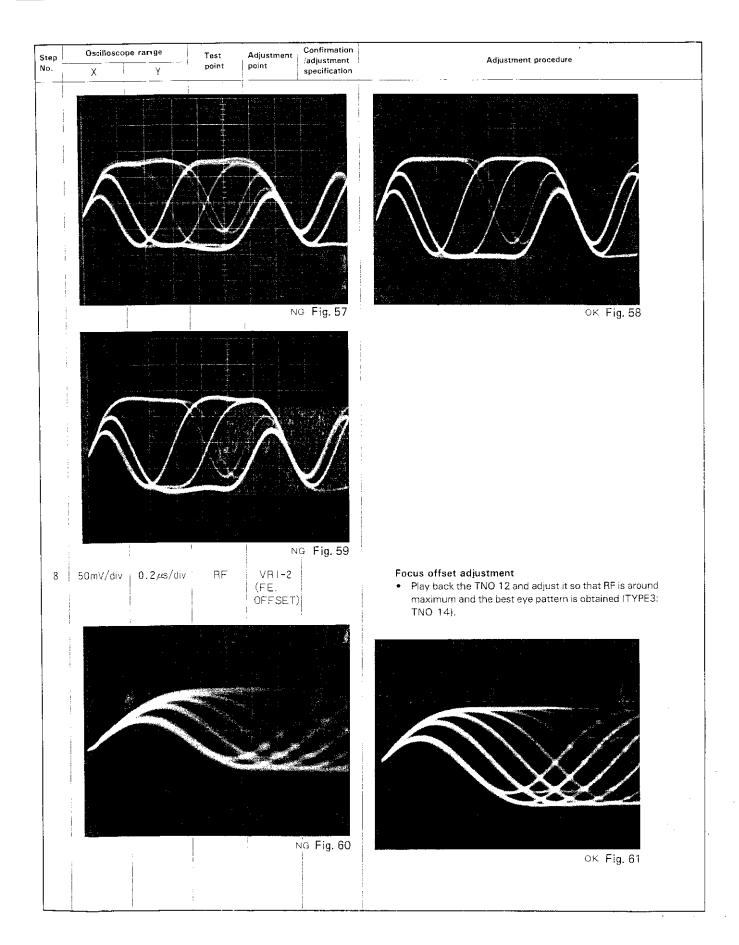
Sten	Step Oscilloscope range		Test Adjustment		Confirmation /adjustment	Adjustment procedure	
No.	X	Y	point	point	specification		
						Measuring instrument and jig used Two-channel oscilloscope with delayed sweep. Optical power meter (LEADER: LPM8000) Test disc (SONY TEST CD TYPE 4 YEDS-18) (TYPE 3 YEDS-7 is usable.) Two needle voltmeter DC power supply (More than 5A) Gain adjustment filter CR oscillator Extension connector	
						Precautions Oscilloscope used must have a 10:1 probe as a rule. Waveform photos are taken by using a 100 MHz oscilloscope. When the laser is on, do not look into the object lens.	
						Preparation • Remove the case top and chassis.	
						Test mode entry Press the clear button while simultaneously pressing TRACK+ TRACK- (or turn ACC, BACK UP on instead of pressing the clear button). BBBBBB is displayed.	
						Turn the DD converter on. Press the REL/PLAY key. ———————————————————————————————————	
i	I					Actuator, motor operation confirmation Carriage motor Confirm that the pickup shifts toward the outer circumference by pressing the F. FORWARD key and toward the inner circumference by pressing the REVERSE key. Then shift it to the extreme outer circumference.	
						 Focus actuator When the TRACK key is pressed, it is shifted downward first. After this, it shifts smoothly up and down about 1mm. When TRACK is pressed again, lens up and down movement stops and the DD converter returns to an ON status. is displayed. 	
						Tracking actuator Press the REPEAT key.	

Step Oscilloso		scilloscope range		Advistment	Confirmation	Adjustment procedure
No.	Х	Y	Test point	point	/adjustment specification	Adjustment procedure
						Confirm that the lens shifts toward the outer circumference when the F. FORWARD key is pressed and toward the inner circumference when the REVERSE key is pressed. Lens shift is about 0.2mm. Press the REPEAT key to return the DD converter to an ON status. ————— is displayed.
2				VR in the pickup.	250±20,AW	 LD power confirmation and adjustment Place a power sensor on the pickup object lens. If it is outside the proper range, quickly adjust VR in the pickup so that it is within the proper range. (Increased by clockwise movement). Turn it slow so that the meter index swing is not excessive.
3			RF	VRI-I (RF)	0.1±0.1V	RF offset adjustment DD converter - ON. Perform this without a disc.
4			EFB FFB	VRI-3 (T.B)	0±0.5dB	 Tracking balance rough adjustment Insert a disc and set it by pressing the EJECT /RELOAD key twice. Turn the DD converter ON by pressing the REL/PLAY key. Obtain focus by pressing the TRACK key to enter a tracking open status. Adjust the AC component level of sub beam output EFB, FFB by using a two needle voltmeter so that the level difference is a standard value.
5		(While the (Tracking act			0±50mV N status.) → non-drive) →	Stray light adjustment After ejecting a disc by pressing the EJECT //RELOAD key, remove the disc. Provide the DD converter with an ON status by pressing the REL/PLAY key. Provide the non-drive tracking circuit with a close status. MIRR KILL: "L" Grounded to S. GND BYPASS: "L" Grounded to S. GND If this is not performed, the actuator might be damaged by fire. Press the TRACK+ key. MIRR KILL: "L" can be preset. BYPASS: "L" shall occur after DD converter ON. ====== is displayed. Adjust it so that it is within the range. After adjustment, return the DD converter to an ON status by pressing the TRACK+ key.

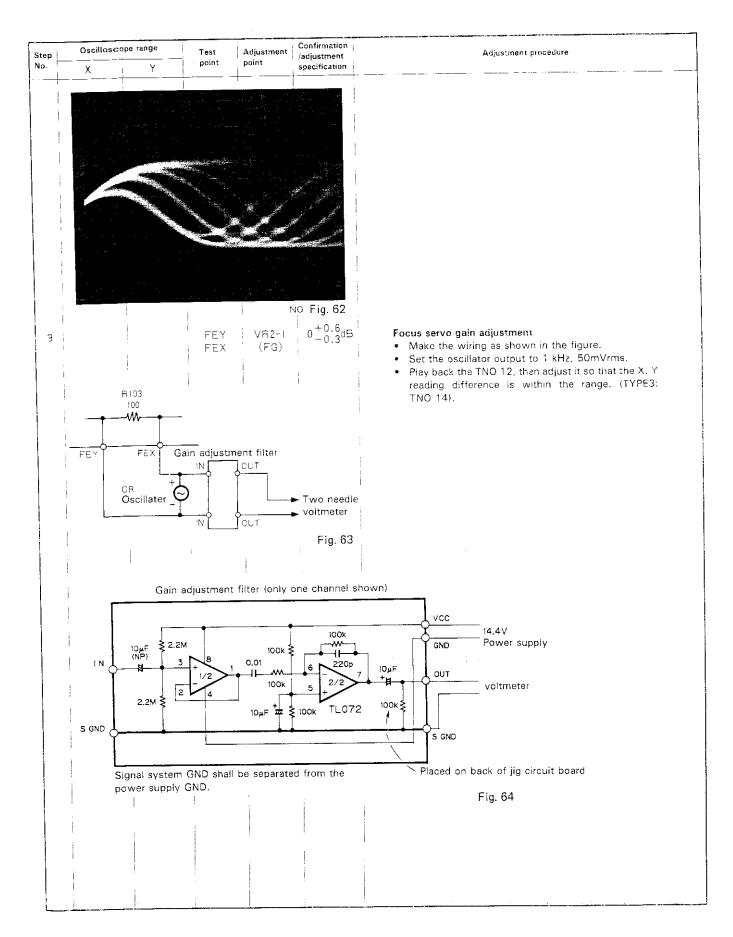




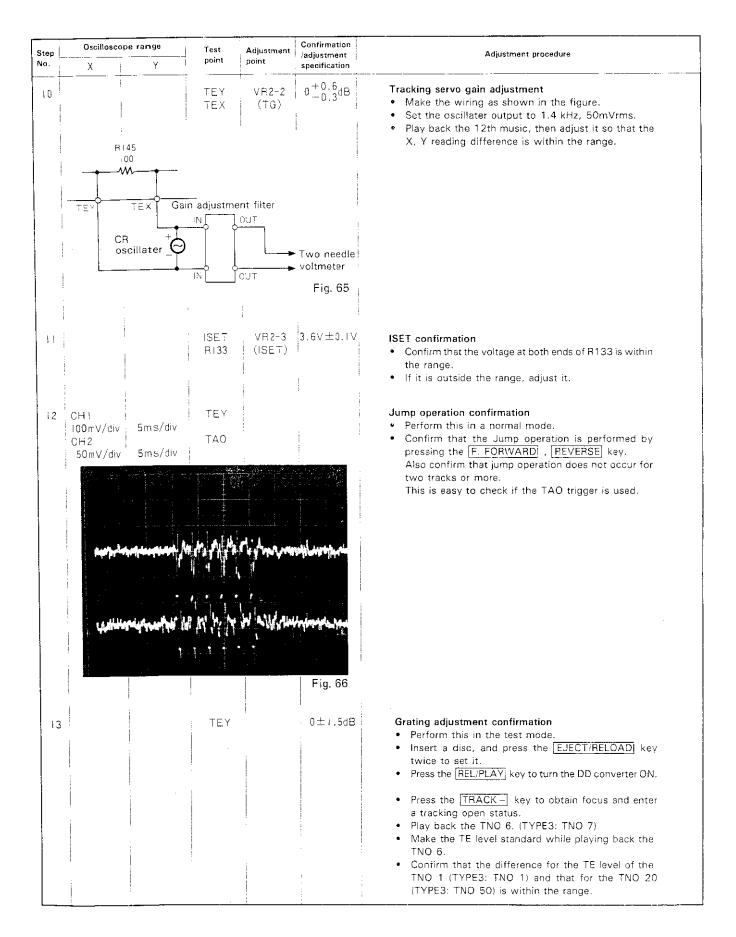




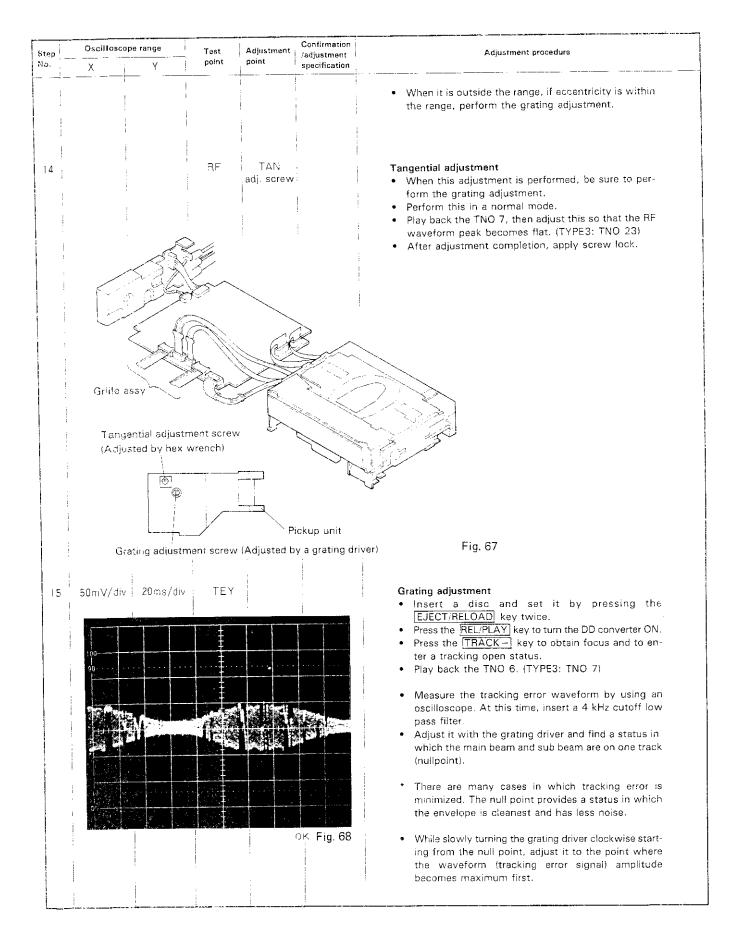














Step	Oscillo	scope	range	Test	Adjustment	Confirmation /adjustment	Adjustment procedure
No.	X		Υ	point	point	specification	
	109						* If the driver is pressed too strongly, the pickup main- frame is lifted. Therefore, precautions shall be taken concerning this.
16						G Fig. 69	 Grating fine adjustment Adjust the TE level during tracking open so that the level for the TNO 1, 6, 20 becomes within 1.5 dB. (TYPE3: TNO 1, 7, 50)
!7				V00	L201	-0.5V	 VCO adjustment Play back music in a normal mode. Measure the voltage at IC201 pin 28 (GFS) with a millivolt meter and confirm if PLL lock has occurred or not. Lock H level about 5V Unlock L level about -0.5V Adjust L201 so that the VCO voltage becomes -0.5V during PLL lock.