PIONEER®
The future of sound and vision.

Service Manual

ORDER NO.
ARP2072

CD CDV LD PLAYER

CLD-92 KU/CA

- **Refer to the service manual ARP1853, CLD-91/KU/CA.**
- **This manual is applicable to the CLD-92/KU/CA type.**

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).
When servicing or handling circuit boards and other components which contain lead in in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS SERVICE INC. P.O. Box 1760, Long Beach, California 90801 U.S.A.
PIONEER ELECTRONICS OF CANADA, INC. 505 Cochrane Drive, Markham, Ontario L3R 8E3 Canada
PIONEER ELECTRONIC [EUROPE] N.V. Keetberglaan 1, 2740 Beveren, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia TEL: [03] 580-9911

FV JULY 1990 Printed in Japan

1. SAFETY INFORMATION

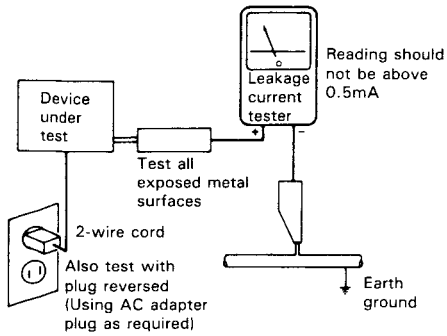
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

2. CONTRAST OF MISCELLANEOUS PARTS

NOTES:

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

CLD-92/KU/CA type is the same as CLD-91/KU/CA type with the exception of following sections.

Mark	Symbol & Description	Part No.		Remarks
		CLD-91/KU/CA type	CLD-92/KU/CA type	
	AC Cord spacer	....	ANG1153	
⚠	AC Power cord	VDG1026	VDG1042	
	Packing case	VHG1060	VHG1107	For packing
	FL Panel	VNK1227	VNK1493	
	Operating instructions (English)	VRB1020	VRB1035	
	Front door assembly-S	VXX1271	VXX1433	
	Front panel assembly-S	VXX1331	VXX1457	
◉	STTB assembly	Non supply	VWG1110	
	YCSB assembly	Non supply	....	
	YCSB2 assembly	....	Non supply	
◉	8FSB assembly	VWV1077	VWV1147	
	DLSB assembly	....	Non supply	2 boards are used.

3. ELECTRICAL PARTS LIST

NOTES:

- *Parts without part number cannot be supplied.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560Ω	*56 × 10¹*	*561*	*RD1/4PS 5 6 1 J*
47kΩ	*47 × 10³*	*473*	*RD1/4PS 4 7 3 J*
0.5Ω	*0R5*		*RN2H 0 R 5 K*
1Ω	*010*		*RS1P 0 1 0 K*

Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62kΩ	*562 × 10¹*	*5621*	*RN1/4SR 5 6 2 1 F*

◉ 8FSB Assembly(VWV1147)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC202,IC203	AD1862N
	IC106	BU4551B
	IC101	CXD1135Q
	IC103	CXK5816M-12L
	IC201	HD74HC153P
	IC401	M5F78M12L
	IC402	M5F79M12L
	IC104,IC107	NJM082D
	IC502,IC503	NJM5532DD
	IC204,IC205	NJM5532SD
	IC301	PA0034A
	IC102	PDE024
	IC108	PD0036
	IC105	TC40H004P
	IC501	TC74HCU04AP
	Q301,Q403	UN4112
	Q302,Q404	UN4212
	Q401	2SA886
	Q201,Q204	2SA933S
	Q1 - Q10	2SC1740S
	Q402	2SC1847
	Q202,Q203	2SD1302
	Q501 - Q504	2SD1468S
	D102	FC54M
	D101	KV1225YBR
	D1,D2,D103,D104,D201, D301,D302,D405,D406	1SS254
	D401 - D404	31DF2-FE

RELAY

Mark	Symbol & Description	Part No.
	RY501 Relay	VSR-005

COILS AND FILTERS

Mark	Symbol & Description	Part No.
	L3 Axial inductor	LAU101J
	L1,L2 Axial inductor	LAU620J
	L4 Coil (3.9MH)	VTL-170
	VL101 Variable coil	VTL-275
	F301 2.3MHz B.P.F	VTF1002
	F302 2.8MHz B.P.F	VTF1003
	F1 1.75MHz L.P.F	VTF1021

CAPACITORS

Mark	Symbol & Description	Part No.
	C1,C3,C23,C132	CCCCH220J50
	C113,C125 - C128,C201,C231, C232	CCCCH330J50
	C309,C325	CCCCH560J50
	C2,C7,C9	CCCCH820J50
	C20	CCCSL121J50
	C114	CCCSL221J50
	C324	CCCSL271J50
	C307	CCCSL301J50
	C111	CCCSL331J50
	C8,C123	CCCSL471J50
	C133	CCPUSL330J50
	C118	CEALNP2R2M35
	C108	CEALO10M50
	C109,C110	CEAL100M16
	C130,C131,C134	CEAL101M6R3
	C107	CEAL470M6R3
	C333	CEANLR47K50
	C319,C334	CEANP100M16
	C310,C314,C327,C330,C508, C510	CEANP220M10
	C18,C27	CEANP3R3M50
	C315	CEANP330M16
	C4	CEAS010M50
	C19,C119,C120,C124,C203, C318,C503	CEAS100M50
	C22,C306,C323,C501	CEAS101M10
	C305,C316,C320,C322	CEAS221M10
	C303	CEAS221M10
	C332	CEAS4R7M50
	C15	CEAS470M10

Mark	Symbol & Description	Part No.
	C512,C514	CEAS470M25
	C218,C225	CENA470M25
	C206,C209,C212,C215,C217, C224	CENA470M50
	C210,C216	CEYANP010M50
	C207,C213	CEYANP100M50
	C129	CEYA101M25
	C403,C404	CEYA221M50
	C205,C208,C211,C214	CEYA470M25
	C401,C402	CEZA222M35
	C115,C317	CFTXA104J50
	C504 - C507	CFTXA471J50
	C117,C121	CFTXA474J50
	C220,C227	CFTXA683J50
	C103,C136,C408	CGCYX473M25
	C10	CKCYB472K50
	C5,C6,C11,C12,C16,C17, C26,C101,C502	CKCYF103Z50
	C301,C302,C304,C321	CKCYF223Z50
	C112,C137	CKPUYF223Z25
	C102,C104,C135,C513,C515	CKPUYY103N16
	C105,C106	CQMA102J50
	C308,C326	CQMA152J50
	C14	CQMA183J50
	C116	CQMA273J50
	C313,C331	CQMA393J50
	C311,C312,C328,C329	CQMA472J50
	C122	CQMA473J50
	C219,C226	CQMA562J50
	C221,C228	CQMA822J50
	C233,C234	CQSF101J125
	C222,C229	CQSF471J125
	C21	CQSH471J50
	C13	CQSH821J50
	C223,C230,C516,C517 (22μF/50V NP)	VCH1038
	C509,C511,C518,C519 (47μF/80V)	VCH1071

RESISTORS

Mark	Symbol & Description	Part No.
	R403	RD1/2PM□□□J
	R402	RD1/4PM□□□J
	R503,R504,R506, R516 - R520	RDR1/4PM□□□J
	R116,R118,R119,R121, R129,R130	RN1/6PQ□□□□F
	VR103,VR104 Semi-fixed(100k)	VRTB6VS104
	VR101,VR102 Semi-fixed(22k)	VRTB6VS223
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	JA1 Optical transmission module	TOTX172
	JA2 Pin jack (4P)	VKB1014
	X101 Crystal resonator (16MHz)	VSS1022

◉STTB Assembly (VWG1110)

OTHERS

Mark	Symbol & Description	Part No.
	DIN socket (4P.mini)	VKN1078

DLSB Assembly

FILTERS

Mark	Symbol & Description	Part No.
	F1 COMB Filter	VTF1032

YCSB2 Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC2,IC3	MC1496P
	IC1	TA7302P
	Q1,Q6	2SA933S
	Q2 - Q5, Q7 - Q15	2SC1740S
	D1	1SS254

COILS

Mark	Symbol & Description	Part No.
	L5 Axial inductor	LAU100J
	L2 Axial inductor	LAU120J
	L4 Axial inductor	LAU150J
	L1,L3,L6 Axial inductor	LAU470J

CAPACITORS

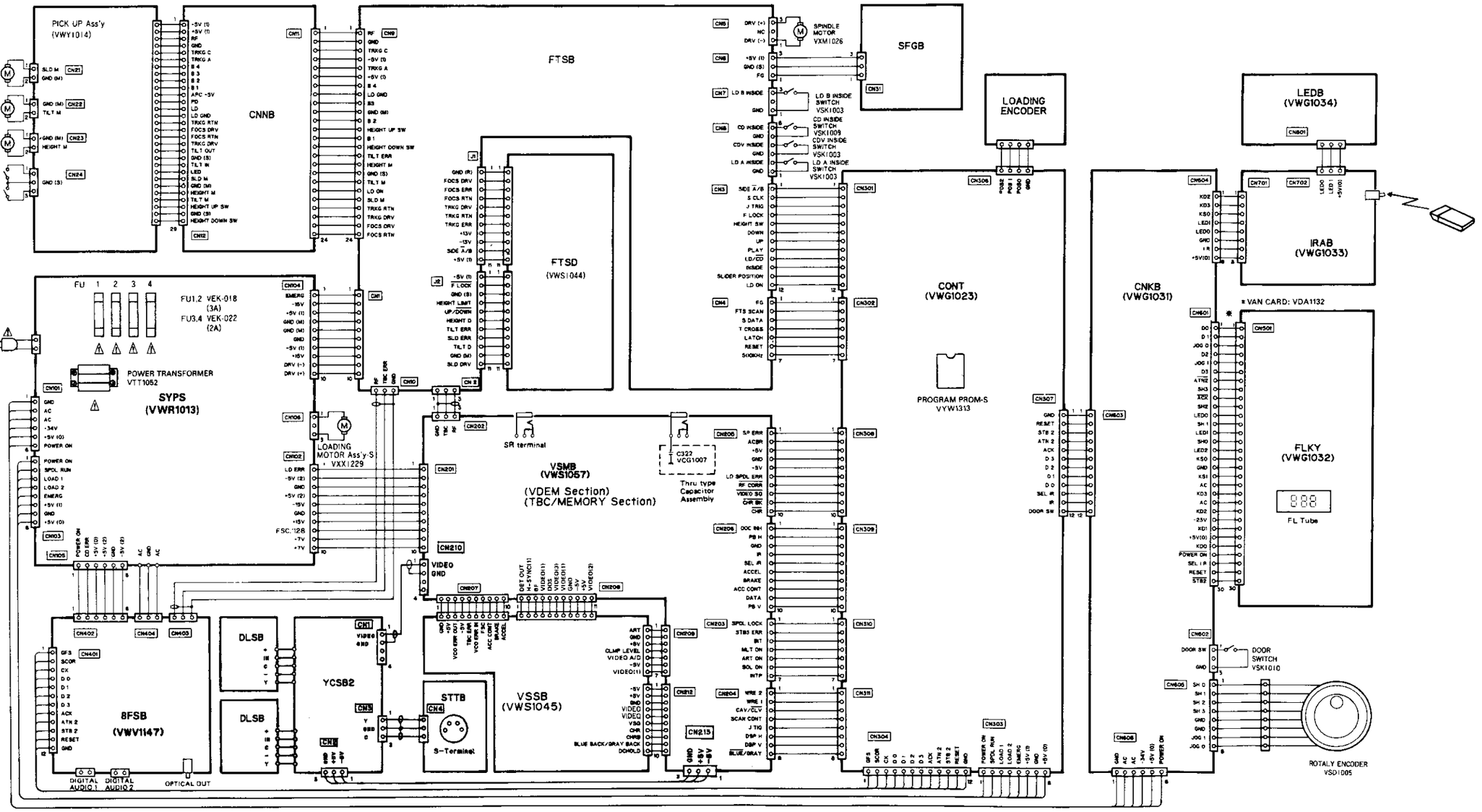
Mark	Symbol & Description	Part No.
	C34	CCCCH390J50
	C31,C39	CCPUCH150J50
	C35	CCPUSL270J50
	C38,C40,C41	CCPUSL470J50
	C36	CCPUSL680J50
	C7	CEAS101M10
	C3	CEAS101M16
	C2	CEAS220M16
	C5,C6	CEAS471M16
	C43	CGDYX473M25
	C33,C42	CKPUYB151K50
	C32,C37	CKPUYB181K50
	C8,C9,C12 - C29	CKPUYY103N16

RESISTORS

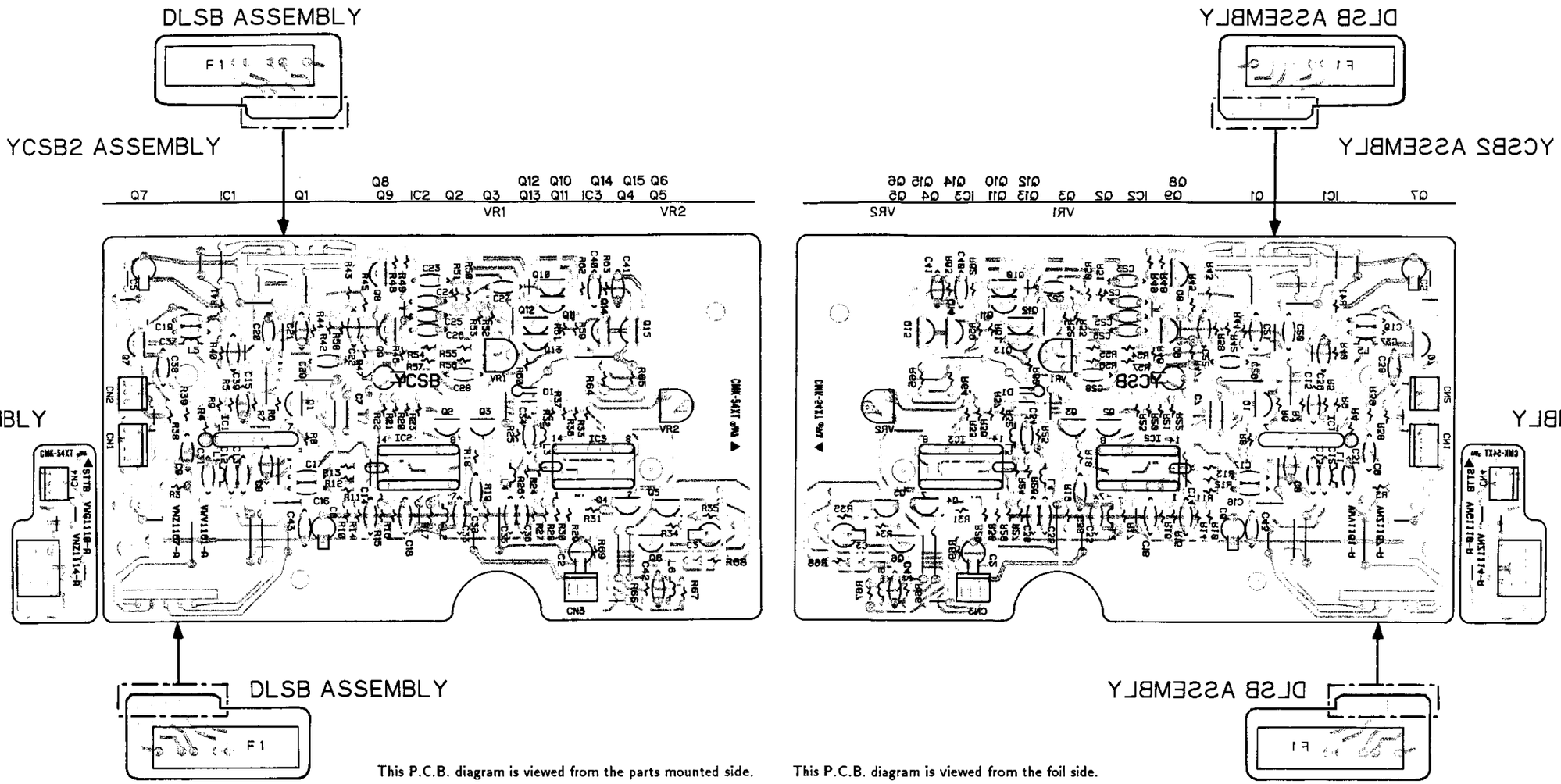
Mark	Symbol & Description	Part No.
	VR1 Semi-fixed(2.2k)	VRTB6VS222
	VR2 Semi-fixed(470)	VRTB6VS471
	Other resistors	RD1/6PM□□□J

4. SCHEMATIC DIAGRAMS AND P.C. BOARDS PATTERNS

4.1 OVERALL CONNECTION DIAGRAM



4.2 YCSB2 AND STTB ASSEMBLY



This P.C.B. diagram is viewed from the parts mounted side.

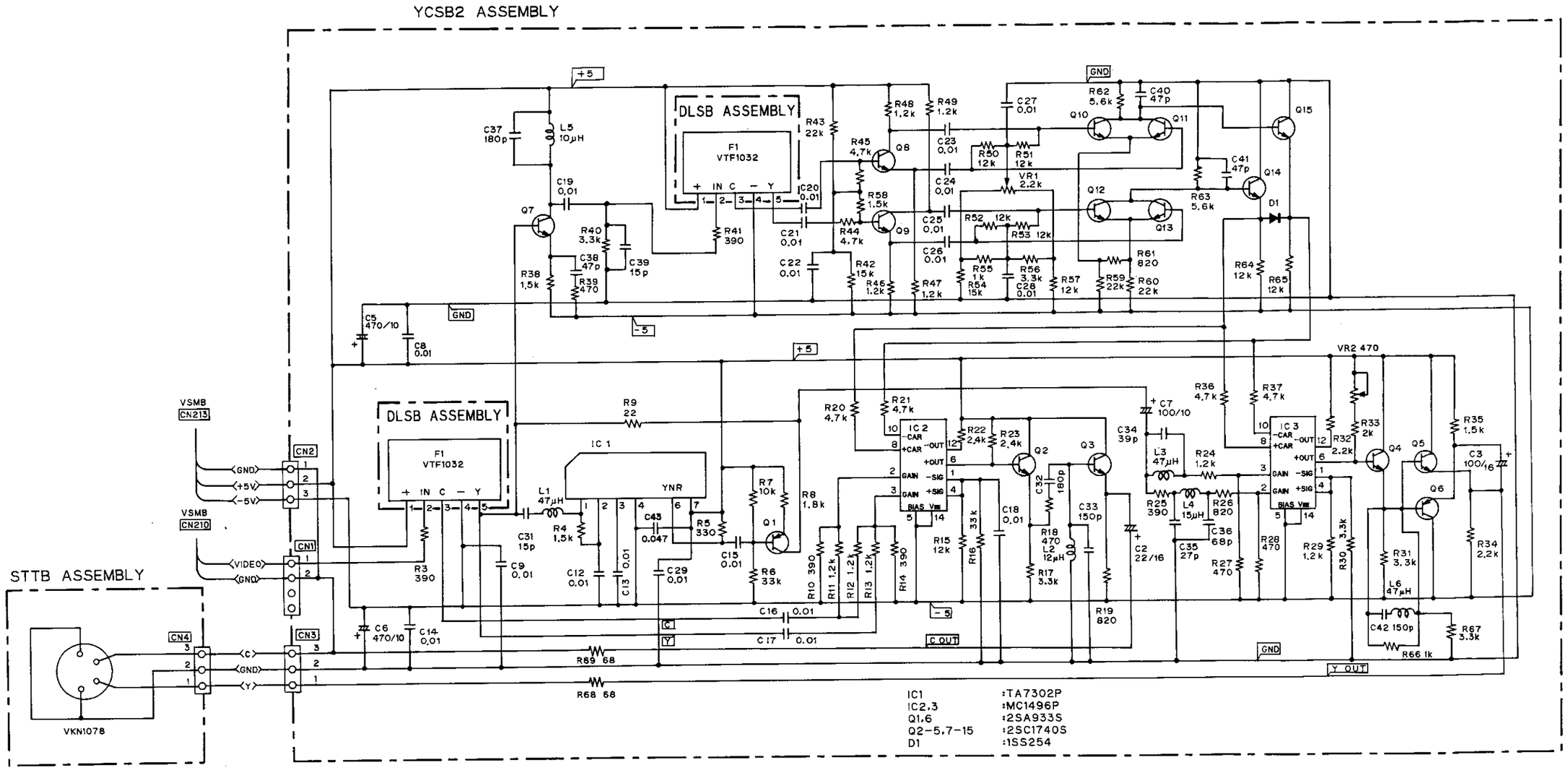
P.C.B. pattern diagram indication	Corresponding part symbol	Part name	P.C.B. pattern diagram indication	Corresponding part symbol	Part name
		Transistor			Ceramic capacitor
		FET			Mylar capacitor
		Diode	SA		Styrol capacitor
			NP		Electrolytic capacitor (Non polarized)
			NL		Electrolytic capacitor (Noiseless)
		Zenner diode			Electrolytic capacitor (Polarized)
					Electrolytic capacitor (Polarized)
		LED			Power capacitor

This P.C.B. diagram is viewed from the foil side.

		Varactor			Semi-fixed resistor
		Tact switch			Resistor array
					Resistor
		Inductor			
		Coil			Resonator
		Transformer			Thermistor
		Filter			

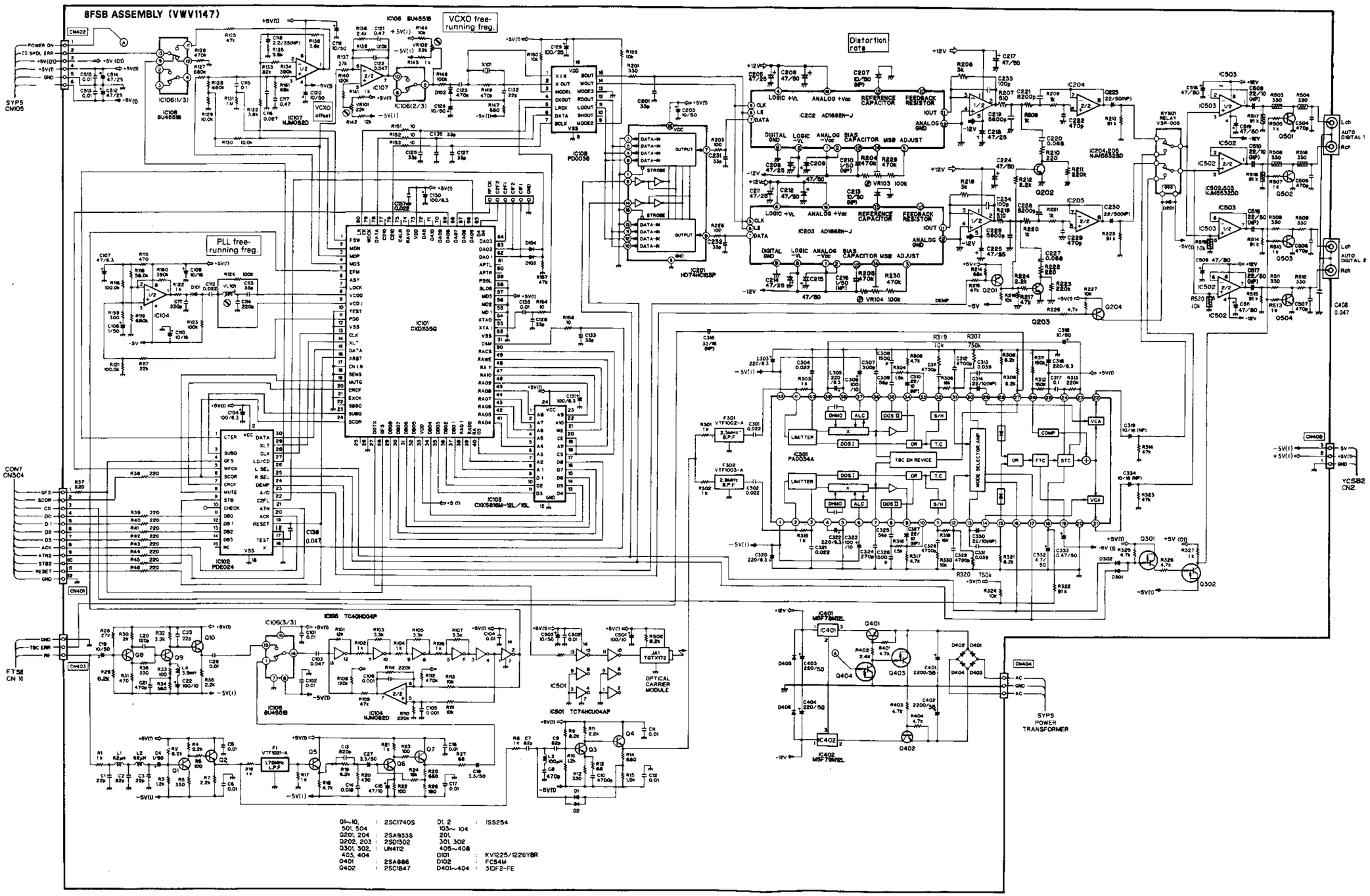
1. The parts which have been mounted on the board can be replaced with those shown with the corresponding wiring symbols listed in the above Table.
2. The capacitor terminal marked with ▭ shows negative terminal.
3. The diode marked with ○ shows cathode side.
4. The transistor terminal marked with ▭ shows emitter.

YCSB2 ASSEMBLY



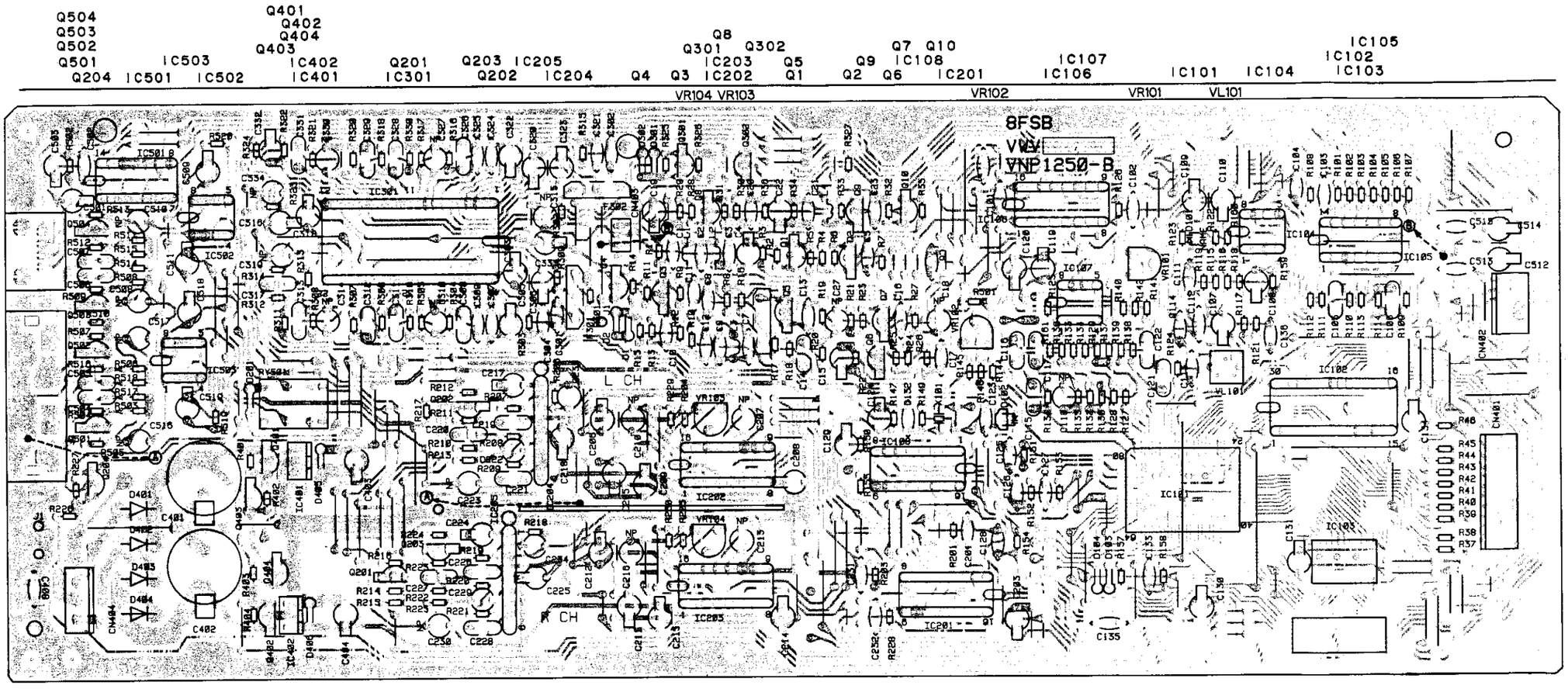
IC1 :TA7302P
IC2,3 :MC1496P
Q1,6 :2SA933S
Q2-5,7-15 :2SC1740S
D1 :1SS254

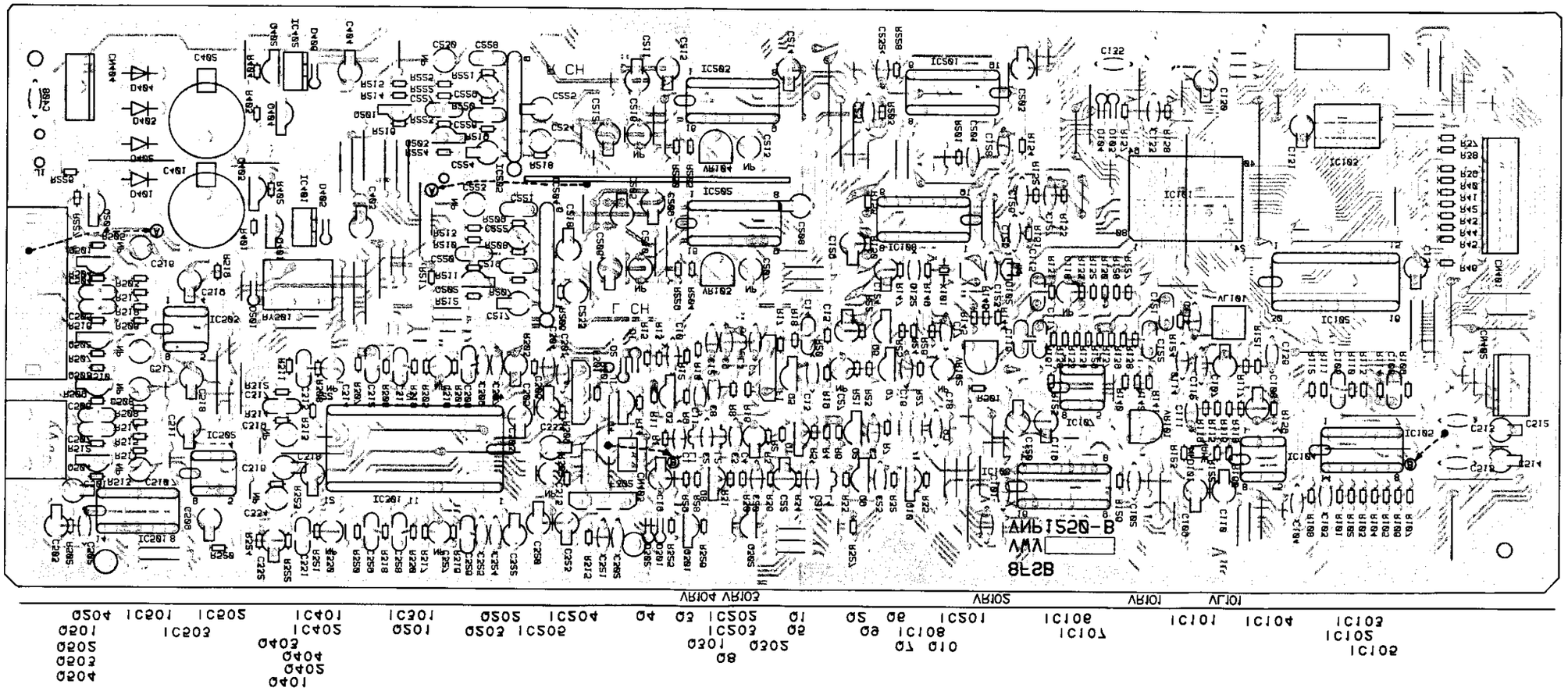
4.3 8FSB ASSEMBLY



8FSB ASSEMBLY (VWV1147)

This P.C.B. diagram is viewed from the parts mounted side.





This P.C.B. diagram is viewed from the foil side.

CT-S18 ASSEMBLY (FOIL VIEW)

5. ADJUSTMENTS

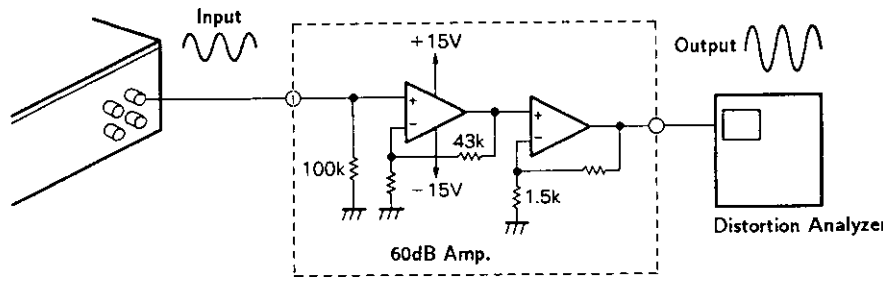
5.1 8FSB ASSEMBLY ADJUSTMENT

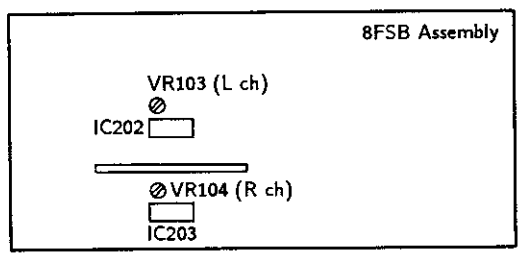
1. Distortion Rate Adjustment (Reference)

- Purpose : To minimize digital sound distortion.
- When not properly adjusted : Digital sound is distorted.

• Measuring instruments and jigs :	• Distortion analyzer • 60dB Amp.
• Measuring position :	• Digital audio output terminal.
• Test disc and player mode :	• M1 test disc chapter 20 (1kHz, 60dB)
• Position to be adjusted :	• 8FSB Assembly VR103, VR104

Connection diagram





Adjusting procedure

1. Connect the 60dB amplifier between the digital audio output terminal and the distortion analyzer.
2. Play the M1 test disc Chapter 20 (1kHz, -60dB) in distortion mode. (20kHz L.P.F. ON)
3. Adjust the VR103 (L ch) and the VR104 (R ch) respectively to minimize the distortion rate.

Note : Adjustments of VR101,VR102 and VL101 on 8FSB assembly are the same as CLD-91 adjustments. (Refer to CLD-91/KU/CA service manual (ARP1853))

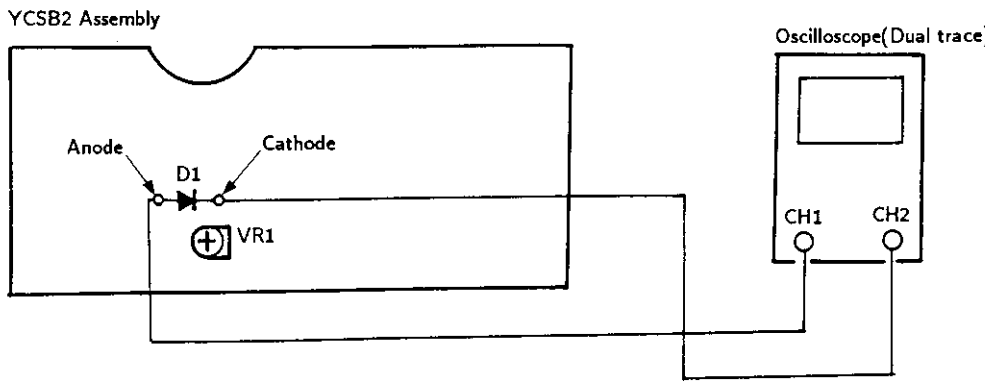
5.2 YCSB2 ASSEMBLY ADJUSTMENT

1. Y/C Level Adjustment

- Purpose : To minimize the dot interference
- When not properly adjusted : An increase in image dot interference. If there is a level slip off on the reverse side, the image resolution will grow worse.

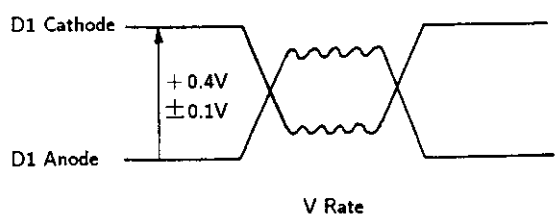
• Measuring instruments and jigs :	• Oscilloscope(Dual trace)
• Measuring position :	• YCSB2 Assembly, Cathode and Anode of D1
• Test disc and player mode :	• LD test disc GGV1002 ····· #5401 STILL
• Position to be adjusted :	• VR1

Connection diagram



Adjusting procedure

1. Connect an oscilloscope (Dual trace) to the anode and cathode of D1.
2. Set the LD test disc #5401 in the still mode and observe the DC potential difference between the anode and the cathode with the oscilloscope set to the V rate.
3. Adjust the VR1 so that the DC potential difference between the anode and the cathode becomes + 0.4 V ±0.1 V.

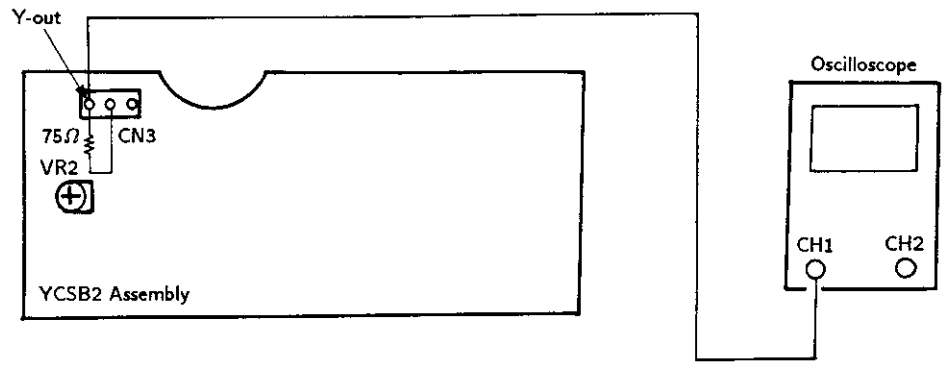


2. Y Level Adjustment

- Purpose : To obtain proper brightness and contrast
- When not properly adjusted : V-synchronization flows on the white screen and the black screen.

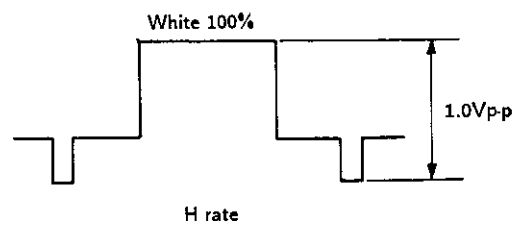
• Measuring instruments and jigs :	• Oscilloscope (Dual trace)
• Measuring position :	• CN3 Y-out terminal (Terminated in 75 Ω)
• Test disc and player mode :	• LD test disc GGV1002·····#1801 (STILL or PLAY)
• Position to be adjusted :	• VR2

Connection diagram



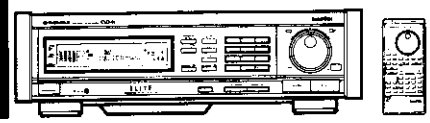
Adjusting procedure

1. Connect an oscilloscope to the Y-out terminal of CN3.(Terminated in 75 Ω)
2. Set LD test disc GGV1002 #1801 in the still or play mode and observe the white 100% waveform with an oscilloscope set to the H rate.
3. Adjust the VR2 so that the Y-out terminal output waveform of the CN3 becomes 1.0 Vp-p.



PIONEER®
The future of sound and vision.

Service Manual



ORDER NO.
ARP 1853

CD CDV LD PLAYER

CLD-91

- **This manual is applicable to the KU/CA type.**
- **As to the circuit and mechanism descriptions, please refer to the CLD-3070 service guide (ARP1702).**

CONTENTS

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS SERVICE INC. P.O. Box 1760, Long Beach, California 90801 U.S.A.
PIONEER ELECTRONICS OF CANADA, INC. 505 Cochrane Drive, Markham, Ontario L3R 8E3 Canada
PIONEER ELECTRONIC [EUROPE] N.V. Keetberglaan 1, 2740 Beveren, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia TEL: [03] 580-9911

FJ JULY 1989 Printed in Japan

1. SAFETY INFORMATION

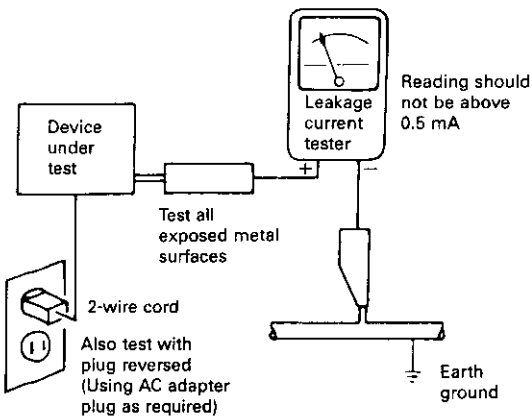
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120 V AC 60 Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5 mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

(FOR EUROPEAN MODEL ONLY)

VAROITUS!
LAITE SISÄLTÄÄ LASERDIODIN, JOKA LÄHETTÄÄ NÄKYMÄTÖNTÄ, SILMILLE VAARALLISTA INFRAPUNASÄTEILYÄ LAITTEEN SISÄLLÄ ON LASERDIODIN LÄHEISYYDESSÄ KUVAN 1. MUKAINEN VAROITUSMERKKI.

LASER
Kuva 1
Lasersateilyn varoitusmerkki

WARNING!
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

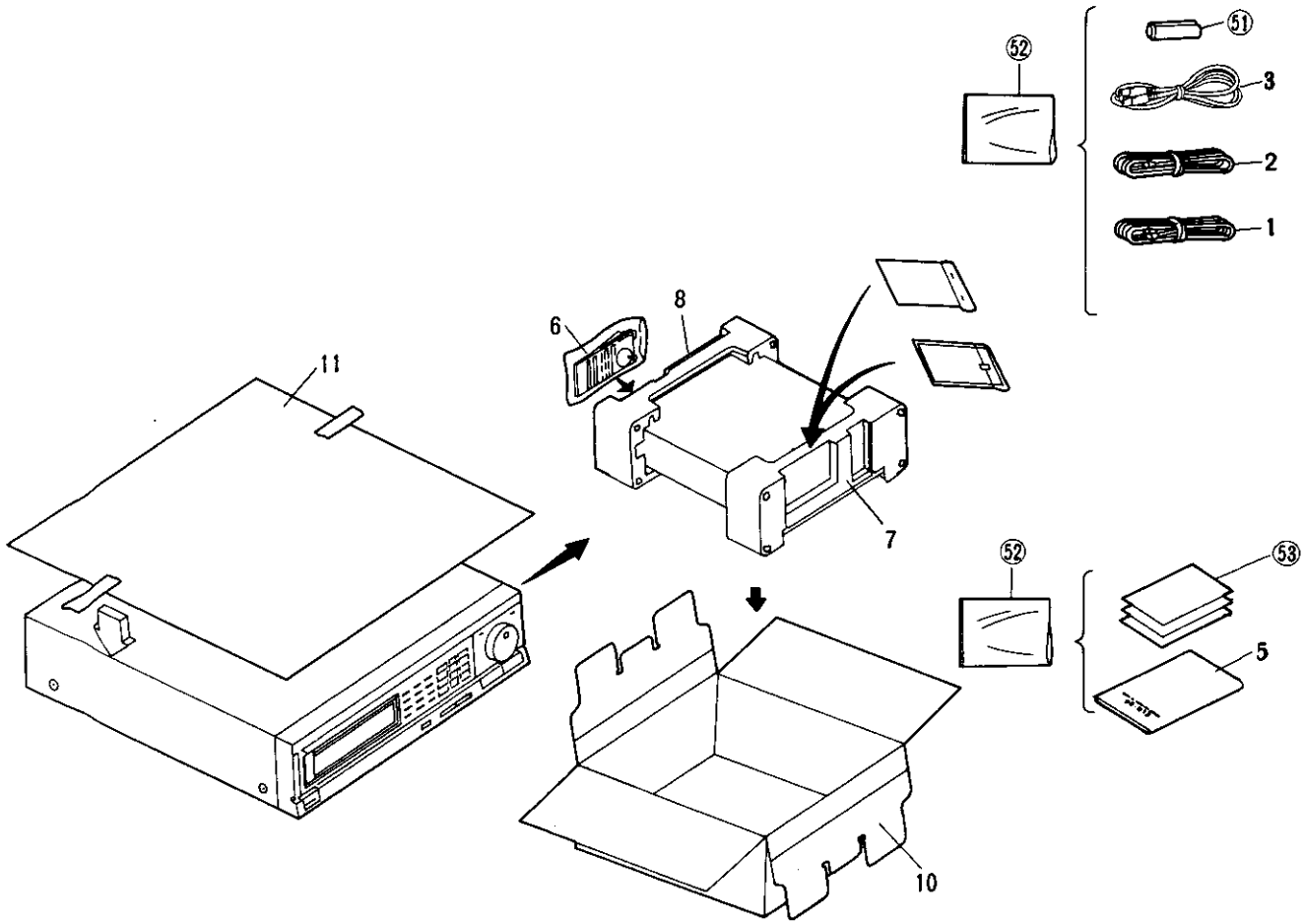
LASER
Picture 1
Warning sign for laser radiation

ADVERSEL:
USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSAETTELSE FOR STRÅLING.

IMPORTANT
THIS PIONEER APPARATUS CONTAINS LASER OF HIGHER CLASS THAN 1. SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

VIKTIGT
APARATEN INNEHÅLLER LASER AV HÖGRE KLASS ÄN 1. INGREPP I APPARATEN BÖR GÖRAS AV SPECIELLT UTBILDAD PERSONAL.

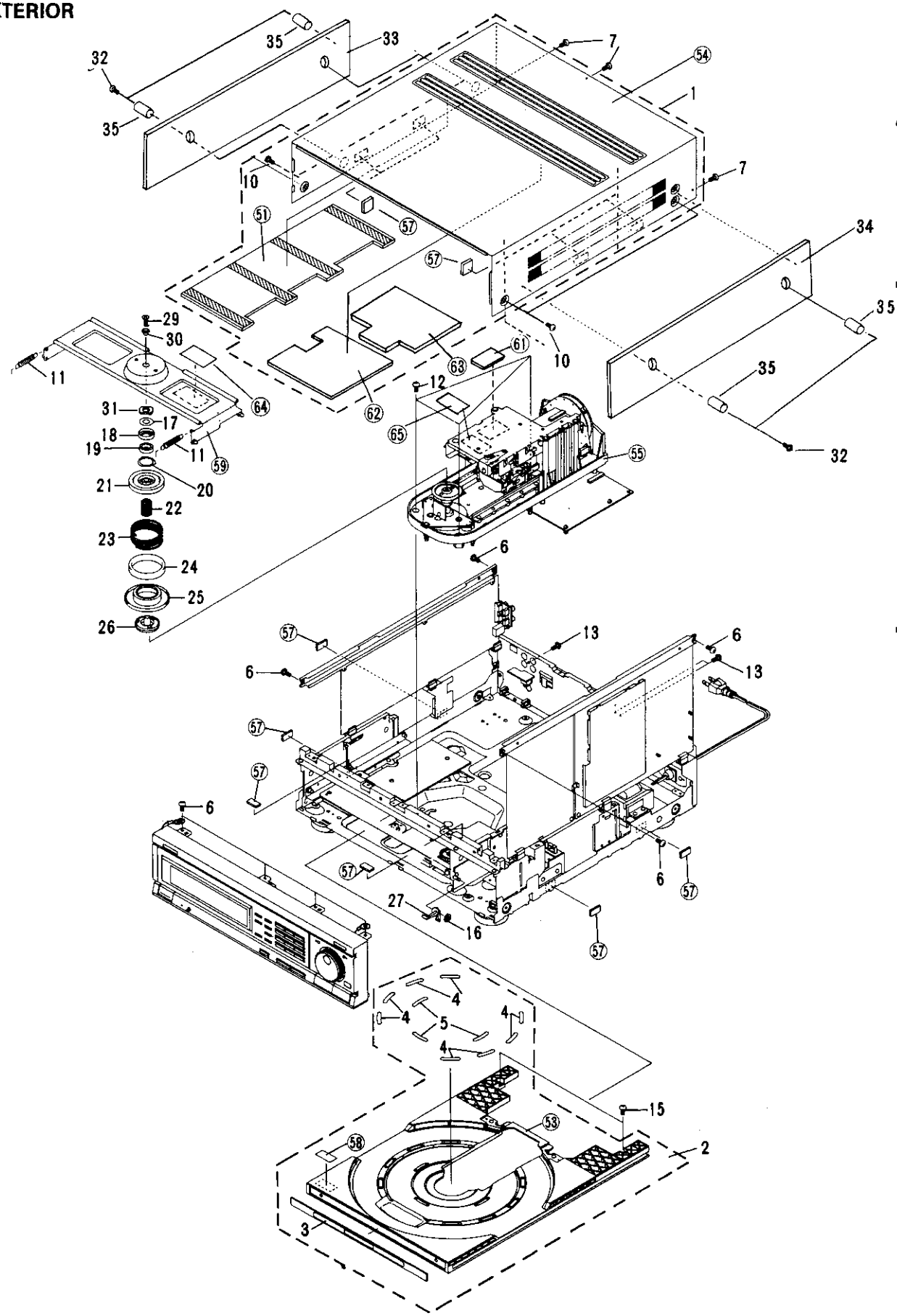
2. PACKING



Mark	No.	Part No.	Description
	1.	PDE1003	Connection cord with pin plug
	2.	VDE1003	Video cable
	3.	VDE1013	S-Video cable
	4.	. . .	. . .
	5.	VRB1020	Operating instructions
	6.	VXX1268	Remote control unit
	7.	VHA1041	Pad (F)
	8.	VHA1042	Pad (R)
	9.	. . .	. . .
	10.	VHG1060	Packing case
	11.	VHL1012	Mirror mat
	51.		Battery (SUM-3)
	52.		Vynil bag
	53.		Caution card

3. EXPLODED VIEWS AND PARTS LIST

3. 1 EXTERIOR

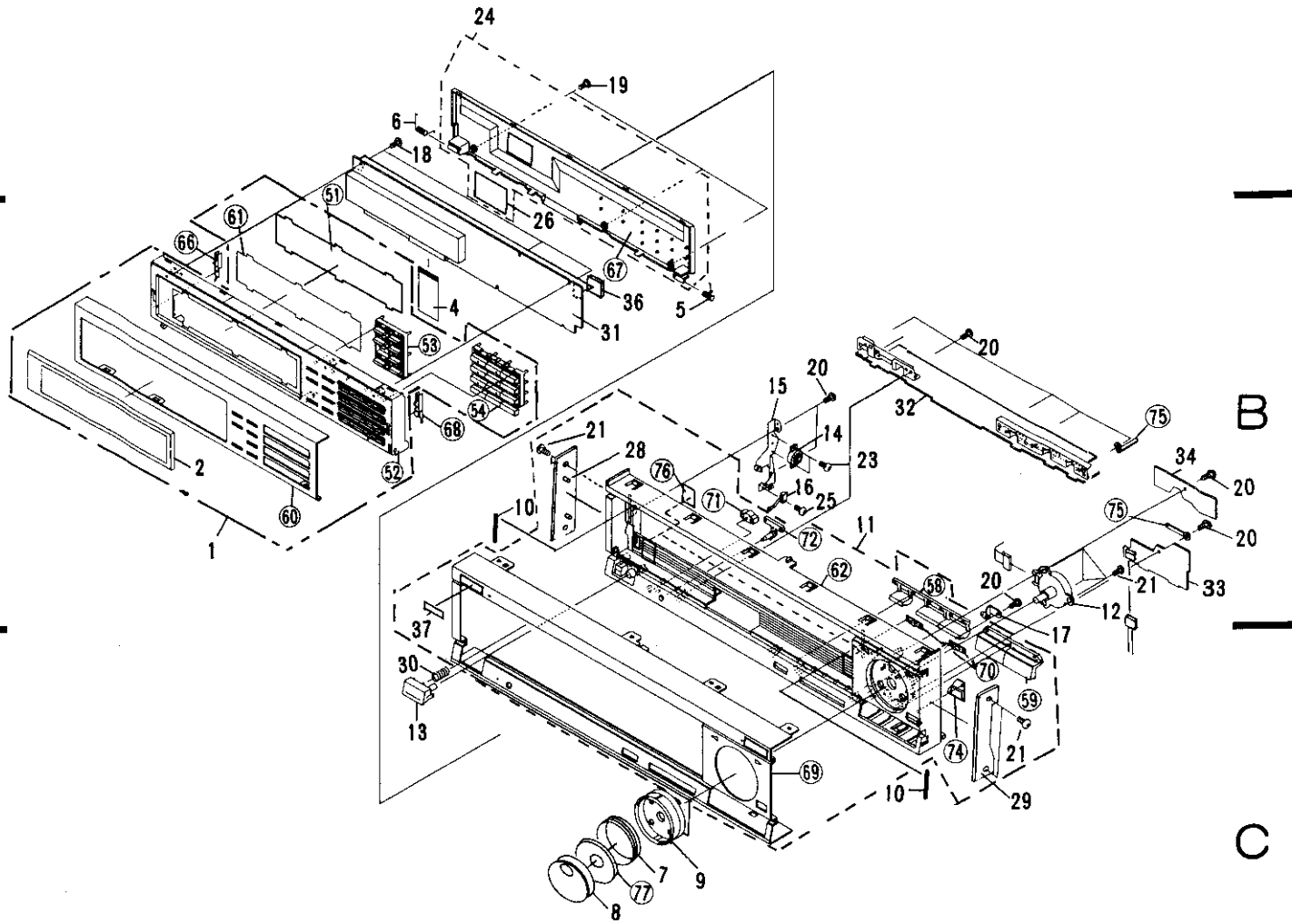


NOTES:

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

Mark	No.	Part No.	Description
	1.	VXX1270	Bonnet assembly-S
	2.	VXX1259	Caddy assembly-S
	3.	VEB1060	Caddy rubber
	4.	VEC1191	Disc pad (L)
	5.	VEC1192	Disc pad (S)
	6.	BBZ30P060FCC	Screw
	7.	BBT30P040FZK	Screw
	8.	BBZ40P060FZK	Screw
	9.	BPZ30P060FCU	Screw
	10.	BCZ40P060FZK	Screw
	11.	VBH1070	Dump spring
	12.	BBZ40P100FCC	Screw
	13.	BPZ30P080FBR	Screw
	14.	IBZ30P060FCC	Screw
	15.	BPZ30P120FZK	Screw
	16.	WT34D060D050	Washer
	17.	VNE1300	SUS sheet
	18.	VNL1176	Spacer
	19.	VNX1001	Radial bearing
	20.	VEC1189	Sheet
	21.	VNL1150	Clamper base
	22.	VBH1055	Cetering spring
	23.	VBH1071	Clamp spring
	24.	VEC1197	Cushion
	25.	VNL1149	Disc clamper
	26.	VNT1014	Centering hab (B)
	27.	VNL1145	Door lever
	28.	. . .	. . .
	29.	CPZ26P100FZK	Screw
	30.	VLL1171	Color
	31.	VEB1073	Dump rubber
	32.	VBA1009	Decorative screw
	33.	VAP1003	Side wood (L)
	34.	VAP1004	Side wood (R)
	35.	PNW1238	Wood color
	51.		Bonnet cushion (A)
	52.		. . .
	53.		Caddy assembly
	54.		Bonnet
	55.		Mechanism assembly
	56.		. .
	57.		Cushion
	58.		Caddy label
	59.		Clamper holder assembly
	60.		. . .
	61.		Mechanism chassis cushion
	62.		Bonent cushion (C)
	63.		Bonnet cushion (D)
	64.		Fuse Caution Label
	65.		Caution Label

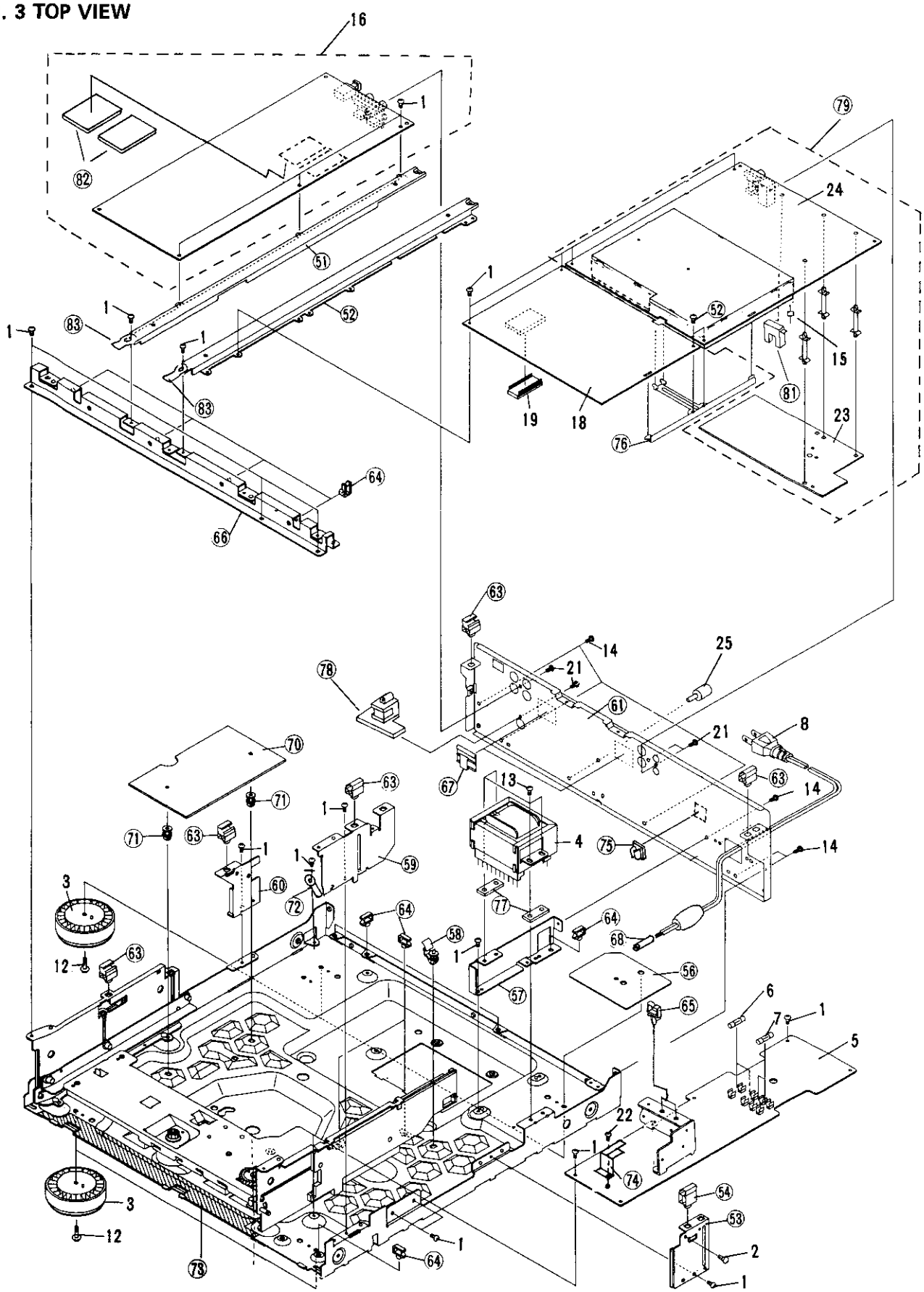
3. 2 FRONT PANEL SECTION



Mark	No.	Part No.	Description
	1.	VXX1271	Front door assembly-S
	2.	VNK1227	FL panel
	3.	. . .	. . .
	4.	VDA1132	Van card
	5.	VBH1052	Door spring (R)
	6.	VBH1051	Door spring (L)
	7.	VEB1070	Shatle rubber
	8.	VNK1239	Jog dial
	9.	VNK1240	Shatle ring
	10.	VEB1058	Front rubber
	11.	VXX1331	Front panel assembly-S
	12.	VSD1005	Rotary encoder
	13.	VNK1231	Power button
	14.	VXA1153	Dumper assembly
	15.	VXA1264	Dumper plate assembly
	16.	VSK1010	Slide switch (DOOR)
	17.	VXA1226	Hinge assembly
	18.	BPZ26P060FCU	Screw
	19.	CPZ26P100FZK	Screw
	20.	BPZ30P060FCU	Screw
	21.	BPZ30P080FCU	Screw
	22.	BPZ30P060FZK	Screw
	23.	PMZ20P040FCU	Screw
	24.	VXX1285	Door cover assembly-S
	25.	PMZ20P060FMC	Screw
	26.	VEC1203	Cover spacer
	27.	. . .	. . .
	28.	VAH1089	Gold Panel L
	29.	VAH1090	Gold Panel R
	30.	VBH1066	Power button spring
◉	31.	VWG1032	FLKY assembly
◉	32.	VWG1031	CNKB assembly
◉	33.	VWG1033	IRAB assembly
◉	34.	VWG1034	LEDB assembly
	35.	VNK1258	Door cover
	36.	VNL1176	Spacer
	37.	AAM1001	Name Plate

Mark	No.	Part No.	Description
	51.		FL smoke plate
	52.		Front door
	53.		Program key
	54.		Numerical key
	55.		. . .
	56.		. . .
	57.		. . .
	58.		Skip button
	59.		Play button
	60.		Door aluminum
	61.		FL filter
	62.		Front panel
	63.		. . .
	64.		. . .
	65.		. . .
	66.		GND plate L
	67.		. . .
	68.		GND plate
	69.		Aluminum panel assembly
	70.		LED lens
	71.		LED lens (B)
	72.		Button base assembly
	73.		. . .
	74.		IR window
	75.		Cord holder
	76.		Dump sheet
	77.		Jog plate

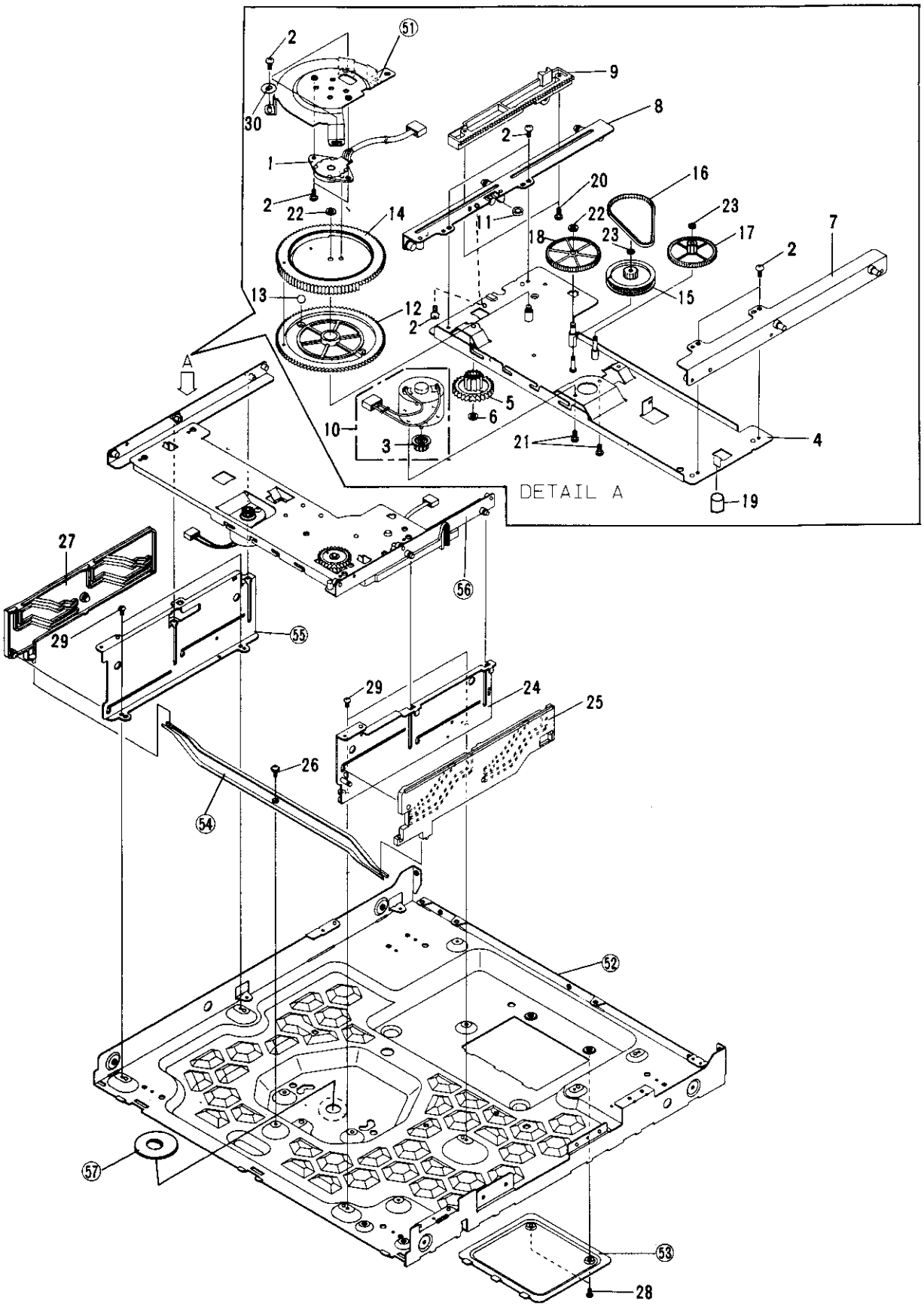
3. 3 TOP VIEW


16
1
82
51
52
83
64
66
79
24
15
81
19
18
23
76
63
14
25
21
61
78
8
67
13
4
75
70
71
59
60
72
58
68
56
57
65
6
7
5
22
74
54
53
2
12
3

Mark	No.	Part No.	Description
	1.	BBZ30P060FCC	Screw
	2.	VEC-143	Plastic rivet
	3.	VXA1301	Insulator assembly
⚠	4.	VTT1052	Power transformer
◉	5.	VWR1013	SYPS assembly
⚠	6.	VEK-018	Fuse (3A) (FU1, FU2)
⚠	7.	VEK-022	Fuse (2A) (FU3, FU4)
⚠	8.	VDG1026	AC power cord
	9.	. . .	. . .
	10.	. . .	. . .
	11.	. . .	. . .
	12.	BBZ30P140FCC	Screw
	13.	BCZ40P080FZK	Screw
	14.	BBZ30P060FZK	Screw
	15.	VCG1007	Thru. type Capacitor (C322)
◉	16.	VWV1077	8FSB assembly
	17.	. . .	. . .
◉	18.	VWG1023	CONT assembly
	19.	VYW1313	Program PROM-S
	20.	. . .	. . .
	21.	BPZ30P080FBR	Screw
	22.	BBZ30P070FCC	Screw
◉	23.	VWS1045	VSSB assembly
◉	24.	VWS1057	VSMB assembly
	25.	VLL1180	Transit screw

Mark	No.	Part No.	Description
	51.		Bridge (B)
	52.		Bridge (C)
	53.		PCB holder (C)
	54.		PCB hinge
	55.		. . .
	56.		Insulation sheet
	57.		Transformer plate
	58.		PC support 7
	59.		PCB holder (A)
	60.		PCB holder (D)
	61.		Rear panel
	62.		. . .
	63.		PCB hinge
	64.		Wire clip
	65.		Wire clip (H)
	66.		Bridge (F)
	67.		Wire clip (R)
	68.		Vynil tube
	69.		. . .
	70.		YCSB assembly
	71.		PCB spacer
	72.		Binder
	73.		Under sheet
	74.		IC heat sink
	75.		Wire clamp (A)
	76.		PCB holder (E)
	77.		Transformer rubber
	78.		STTB assembly
	79.		VSOP assembly (VSSB assembly + VSMB assembly)
	80.		Insulator Pad
	81.		Thru. type capacitor assembly
	82.		DACB assembly
	83.		Earth plate

3. 4 LOADING ASSEMBLY



Mark	No.	Part No.	Description
	1.	VSD1004	Loading encoder
	2.	BBZ30P050FCC	Screw
	3.	VNL1148	Motor pulley
	4.	VXA1260	Motor base assembly
	5.	VNL1144	Gear (E)
	6.	WT41D064D050	Washer
	7.	VXA1268	Roller plate (L) assembly
	8.	VXA1267	Roller plate (R) assembly
	9.	VNL1181	Rack
	10.	VXX1229	Loading motor assembly-S
	11.	VNL1147	Roller
	12.	VNL1143	Gear (C)
	13.	VNX1002	Steel ball (6)
	14.	VNL1142	Gear (B)
	15.	VXA1263	Timing pulley assembly
	16.	VEB1069	Synchro belt
	17.	VNL1106	Gear (D)
	18.	VNL1141	Gear (A)
	19.	VEB1087	Rubber tube
	20.	IPZ30P080FCU	Screw
	21.	PMB26P040FCU	Screw
	22.	WT34D070D050	Washer
	23.	WT26D047D050	Washer
	24.	VXA1236	Clamp base (R) assembly
	25.	VNL1185	Guide (R)
	26.	VBA1005	Screw
	27.	VNL1177	Guide (L)
	28.	BBZ30P040FCC	Screw
	29.	BBZ30P060FCC	Screw
	30.	WB30FMC	Washer

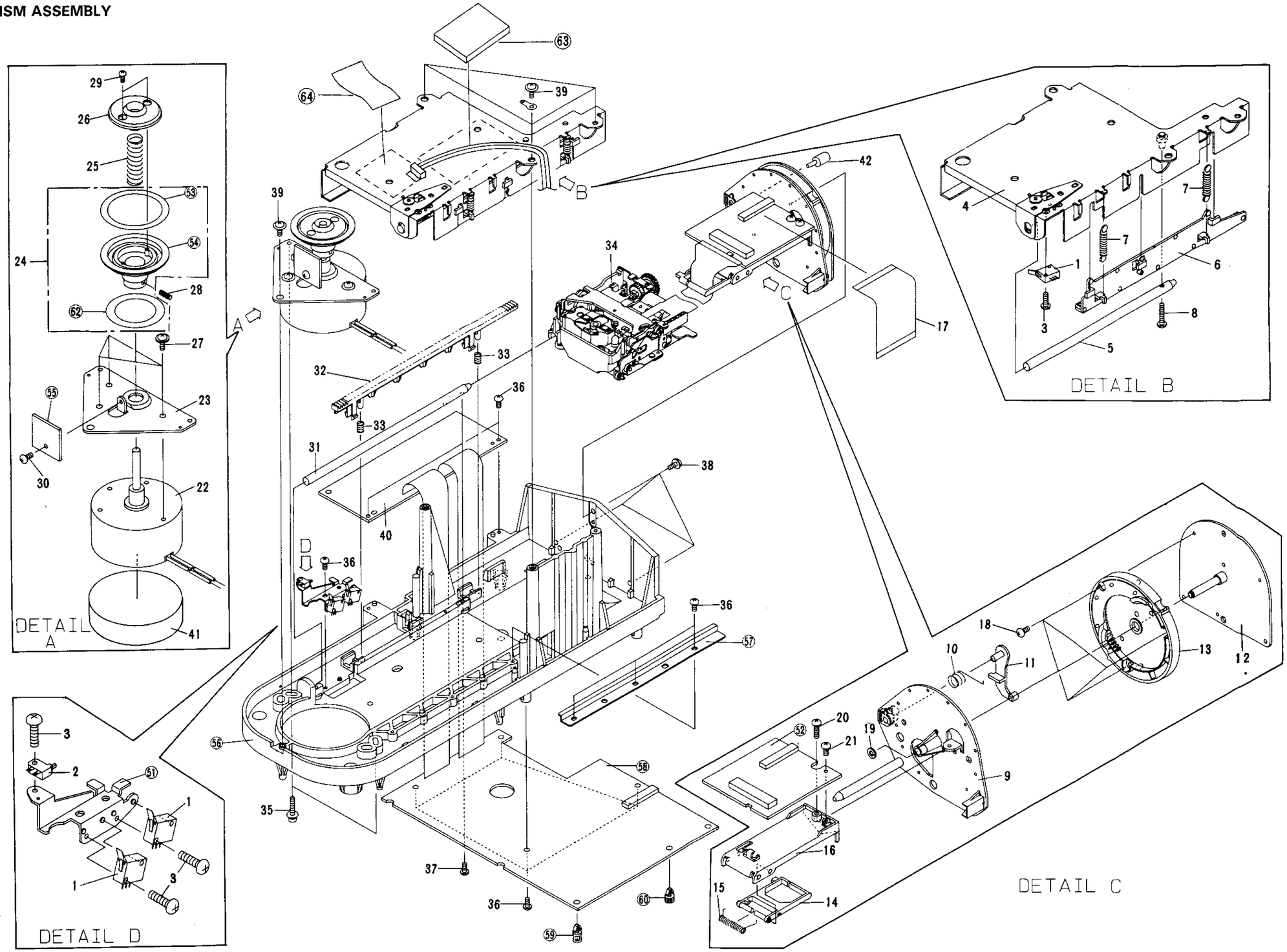
Mark	No.	Part No.	Description
	51.		Gear holder assembly
	52.		Under base
	53.		Under cover
	54.		Joint plate
	55.		Clamp base (L)
	56.		Loading assembly
	57.		Motor cushion

• Parts List of Mechanism Assembly

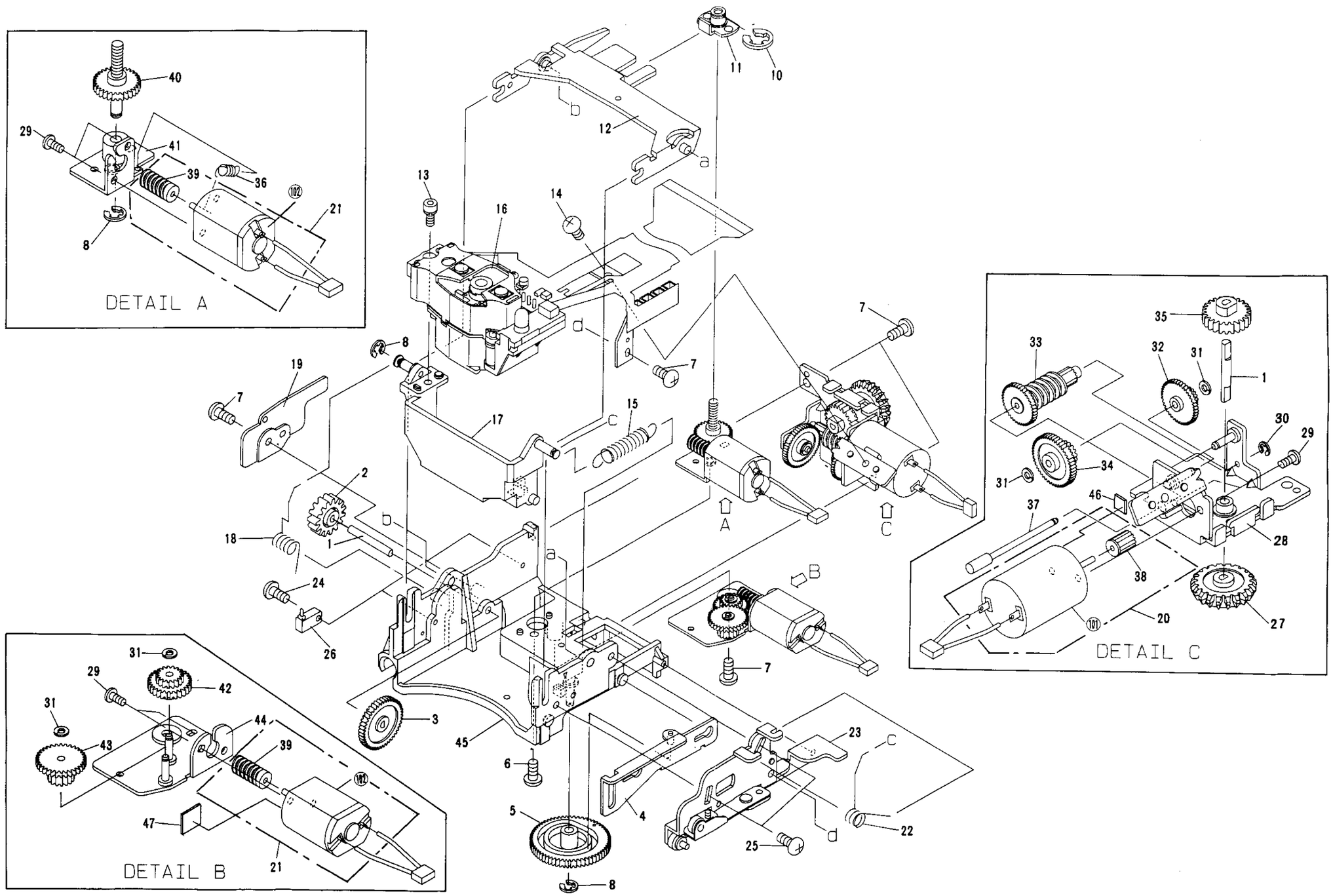
Mark	No.	Part No.	Description
	1.	VSK1003	Slide switch
	2.	VSK1009	Slide switch (CD inside)
	3.	PMZ20P080FMC	Screw
	4.	VXA1250	Mechanism chassis (top) assembly
	5.	VLL1146	Carriage shaft (top)
	6.	VNL1153	Rack gear (top)
	7.	VBH1058	Rack spring (top)
	8.	PMZ20P160FMC	Screw
	9.	VXA1223	R plate assembly
	10.	VBH1072	Lever spring
	11.	VNL1169	Lock lever
	12.	VXA1277	G plate assembly
	13.	VXA1222	Internal gear assembly
	14.	VNL1156	Harness guide (B)
	15.	VBH1059	Guide spring
	16.	VNL1155	Harness guide (A)
	17.	VDA1116	FFC
	18.	BBZ26P060FCC	Screw
	19.	WT36D072D050	Washer
	20.	BBZ30P080FCC	Screw
	21.	BPZ30P060FCU	Screw
	22.	VXM1026	Spindle motor
	23.	VNE1288	Motor holder
	24.	VXX1228	Turntable assembly-S
	25.	VBH1064	Centering spring (A)
	26.	VNL1133	Centering hab (A)
	27.	PMB30P050FCU	Screw
	28.	ZMD30H060FBT	Screw
	29.	IBZ20P040FCC	Screw
	30.	BBZ30P060FCC	Screw
	31.	VLL1145	Carriage shaft (bottom)
	32.	VNL1151	Rack gear (bottom)
	33.	VBH1057	Rack spring (bottom)
◉	34.	VWT1042	Carriage assembly
	35.	VLL1065	Bolt 3 × 18
	36.	BPZ30P100FCU	Screw
	37.	PMZ26P120FMC	Screw
	38.	BBZ30P080FZK	Screw
	39.	IPZ30P100FCU	Screw
◉	40.	VWS1044	FTSD assembly
	41.	VEB1074	Motor cover
	42.	VLL1180	Transit screw

Mark	No.	Part No.	Description
	51.		Switch holder
	52.		CNNB assembly
	53.		Rubber sheet
	54.		Turntable
	55.		SFGB assembly
	56.		Mechanism chassis (bottom)
	57.		Roller clamper
	58.		FTSB assembly
	59.		PC support B
	60.		PC support
	61.		. . .
	62.		Insulator sheet
	63.		Mechanism chassis cushion
	64.		Caution label

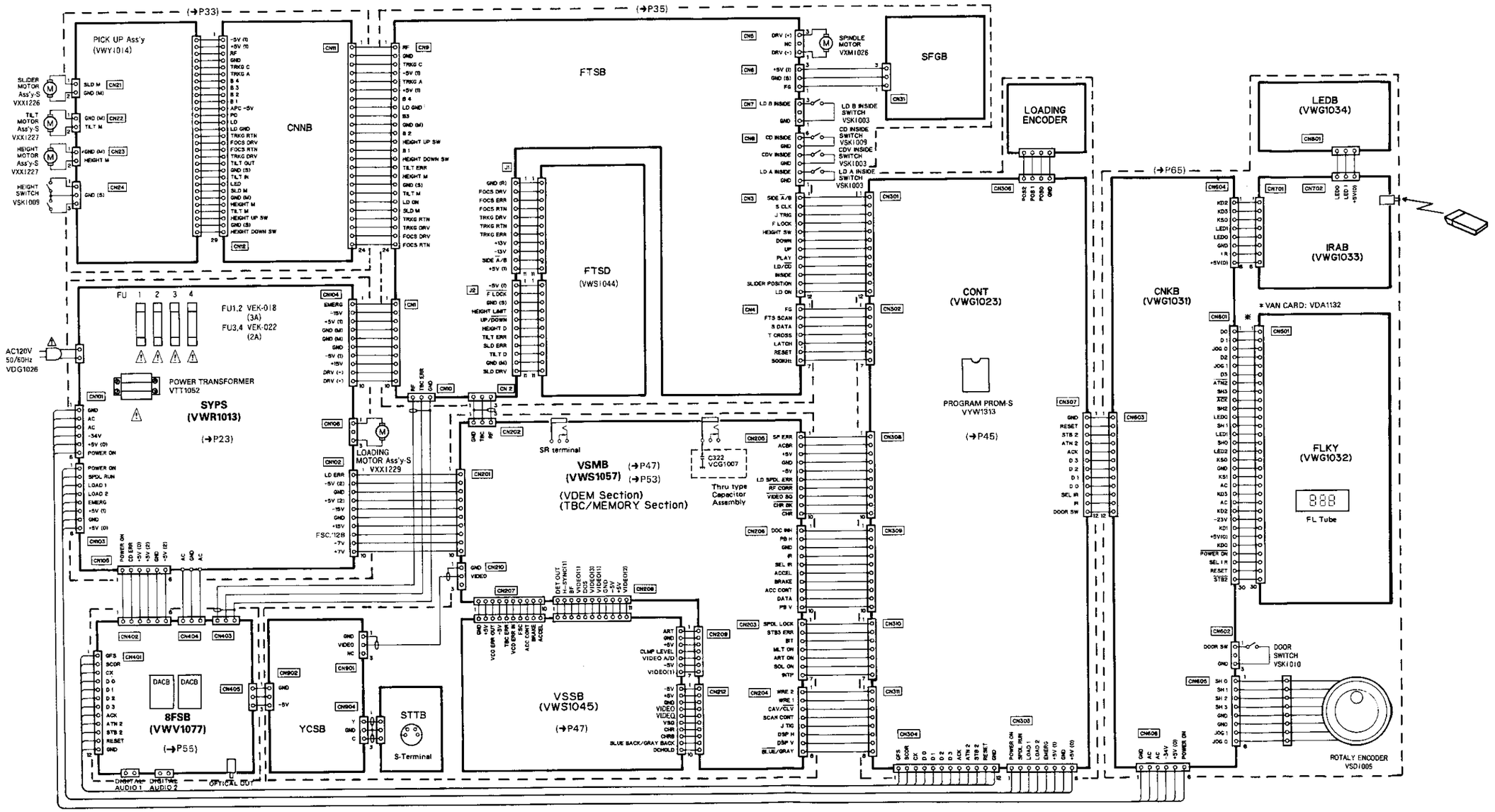
3.5 MECHANISM ASSEMBLY



3.6 CARRIAGE ASSEMBLY

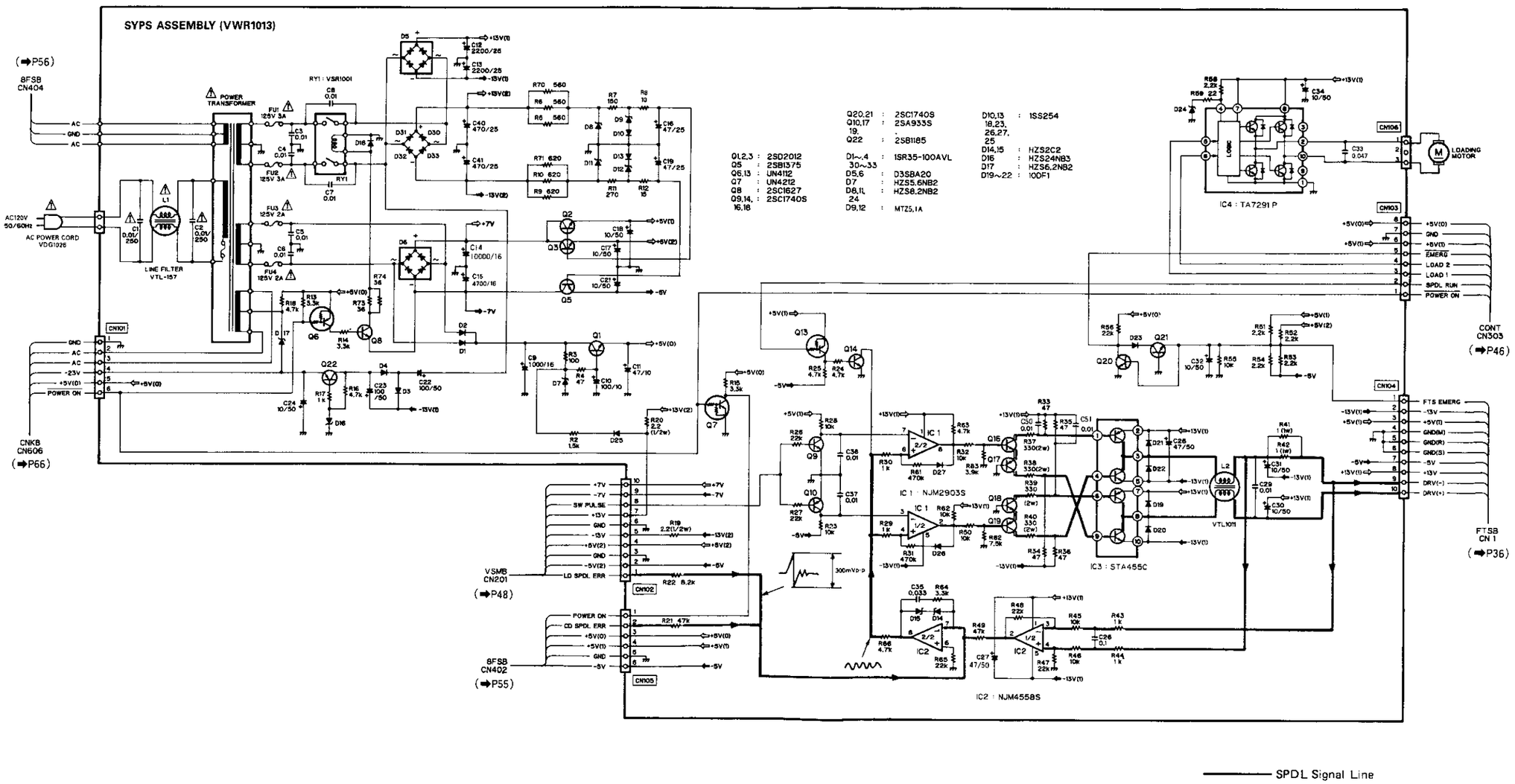


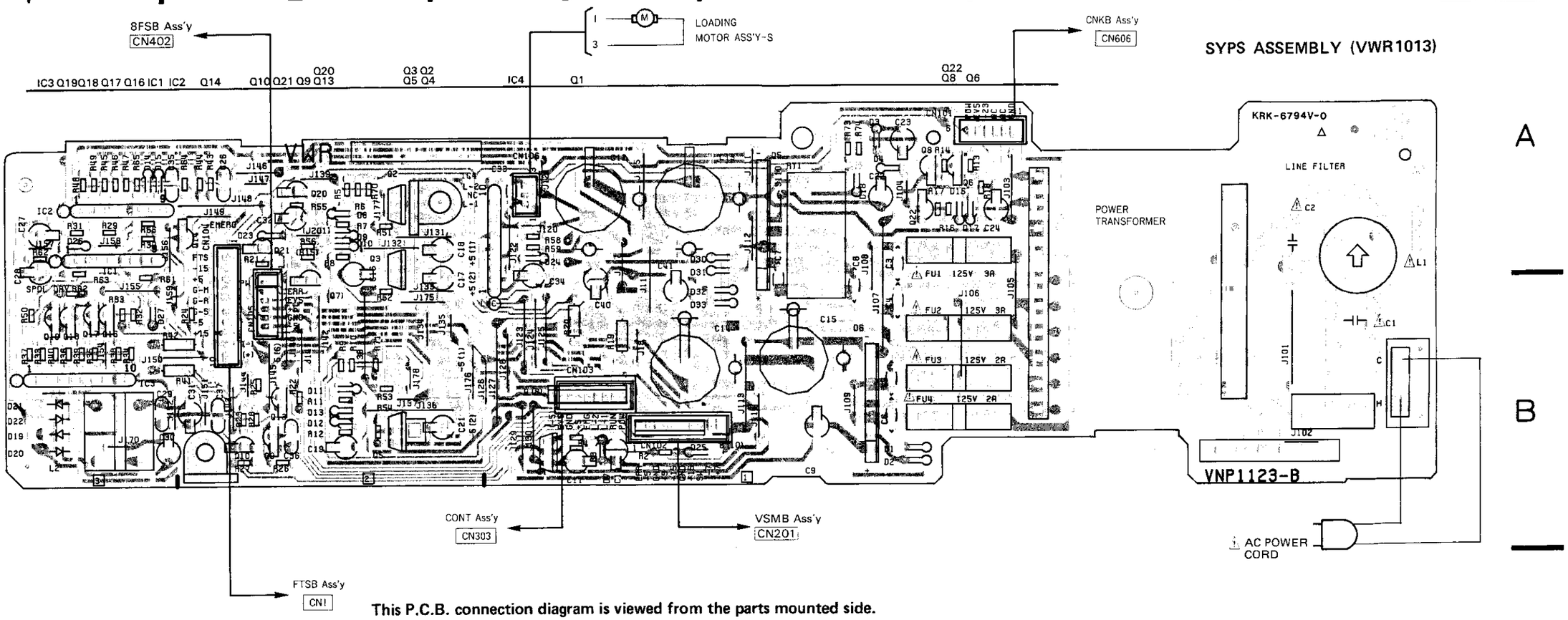
5. CONNECTION DIAGRAM



6. SCHEMATIC DIAGRAM AND P.C. BOARD PATTERNS

6. 1 SYPS ASSEMBLY





This P.C.B. connection diagram is viewed from the parts mounted side.

P.C.B. pattern diagram indication	Corresponding part symbol	Part name	P.C.B. pattern diagram indication	Corresponding part symbol	Part name
		Transistor			Ceramic capacitor
		FET			Mylar capacitor
			SA		Styrol capacitor
		Diode	NP		Electrolytic capacitor (Non polarized)
			NL		Electrolytic capacitor (Noiseless)
		Zenner diode		+	Electrolytic capacitor (Polarized)
					Electrolytic capacitor (Polarized)
		LED			Power capacitor

		Varactor			Semi-fixed resistor
		Tact switch			Resistor array
					Resistor
		Inductor			
		Coil			Resonator
		Transformer			Thermistor
		Filter			

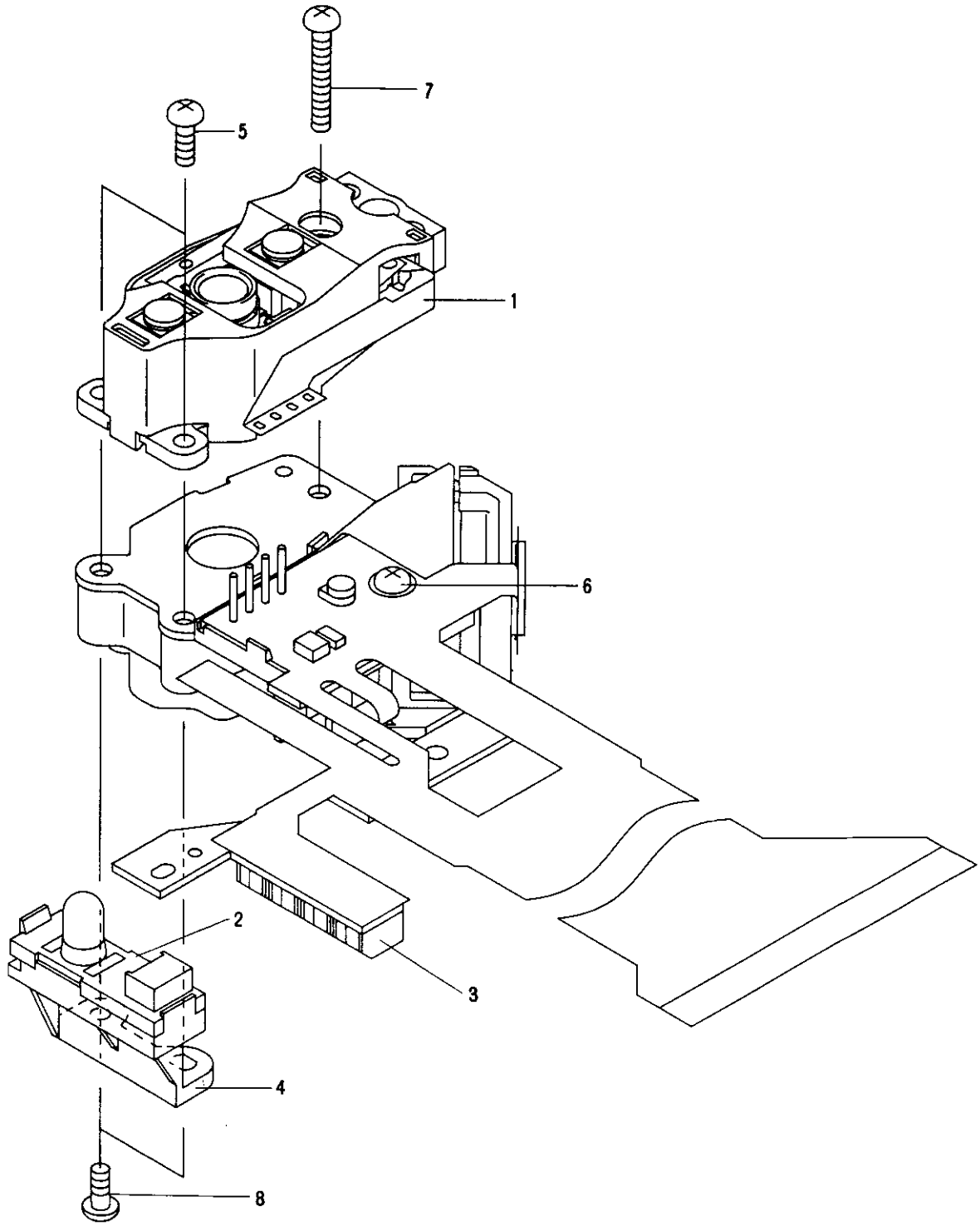
1. This P.C.B. connection diagram is viewed from the parts mounted side.
2. The parts which have been mounted on the board can be replaced with those shown with the corresponding wiring symbols listed in the above Table.
3. The capacitor terminal marked with ▭ shows negative terminal.
4. The diode marked with O shows cathode side.
5. The transistor terminal marked with ▭ shows emitter.

• Parts List of Carriage Assembly

Mark	No.	Part No.	Description
	1.	VLL1152	SL shaft (B)
	2.	VNL1158	SL gear (F)
	3.	VNL1253	SL gear (E)
	4.	VXA1243	Slide plate assembly
	5.	VNL1166	TL cam gear
	6.	PMA26P050FMC	Screw
	7.	BBZ26P050FCC	Screw
	8.	YE20FUC	E ring
	9.	PBZ26P050FCC	Screw
	10.	YE40FUC	Washer
	11.	VXA1259	AF plate assembly
	12.	VXA1246	AF arm assembly
	13.	VLL1107	Bolt 2.6 x 6
	14.	PBZ26P040FCC	Screw
	15.	VBH1063	Tilt spring
	16.	VWY1014	Pick-up assembly
	17.	VXA1220	PU holder assembly
	18.	VBH1061	AF spring (L)
	19.	VNE1284	AF stopper
	20.	VXX1226	Slider motor assembly-S
	21.	VXX1227	Tilt (height) motor assembly-S
	22.	VBH1088	AF spring (R)
	23.	VXA1240	TAN base assembly
	24.	PBZ20P070FCC	Screw
	25.	PMB26P050FCU	Screw
	26.	VSK1009	Slide switch
	27.	VNL1163	SL gear (H)
	28.	VXA1241	SL base assembly
	29.	JGZ20P022FMC	Screw
	30.	YE12FUC	Washer
	31.	WT17D034D050	Washer
	32.	VNL1251	SL gear (B)
	33.	VNL1137	SL gear (C)
	34.	VNL1252	SL gear (D)
	35.	VNL1159	SL gear (G)
	36.	VBH1069	M spring
	37.	VLL1151	SL shaft (A)
	38.	VNL1250	SL gear (A)
	39.	VNL1138	AF worm
	40.	VXA1244	AF gear assembly
	41.	VXA1245	AF holder assembly
	42.	VNL1164	TL gear (A)
	43.	VNL1165	TL gear (B)
	44.	VXA1242	TL base assembly
	45.	VXA1219	Carriage assembly
	46.	VEB1108	Rubber
	47.	VEC1193	Sheet

Mark	No.	Part No.	Description
	101.		Slider motor
	102.		Tilt motor

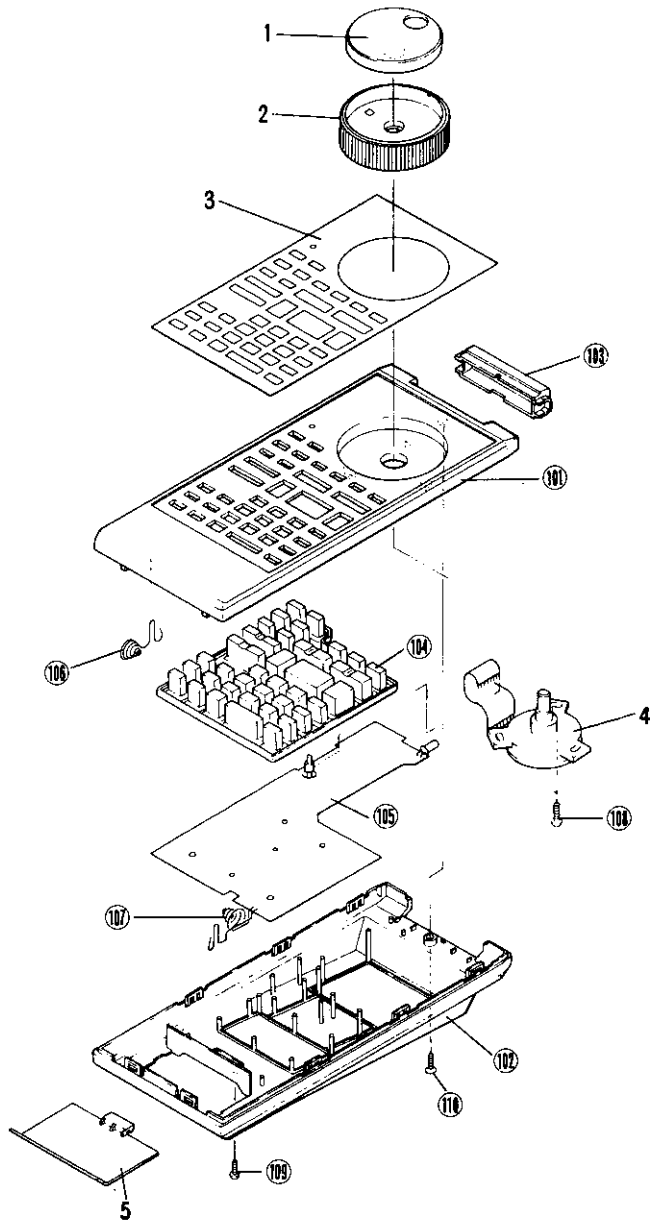
3.7 PICK-UP ASSEMBLY (VWY1014)



• Parts List of Pick-up Assembly

Mark	No.	Part No.	Description	Mark	No.	Part No.	Description
	1.	VXX1241	Actuator assembly		6.	PMA20P080FMC	Screw
	2.	VEX1018	Sensor assembly		7.	PMA20P140FMC	Screw
	3.	VXX1211	Pre pick-up assembly		8.	PMB20P050FMC	Screw
	4.	VNH1020	Sensor stay				
	5.	PMA20P060FMC	Screw				

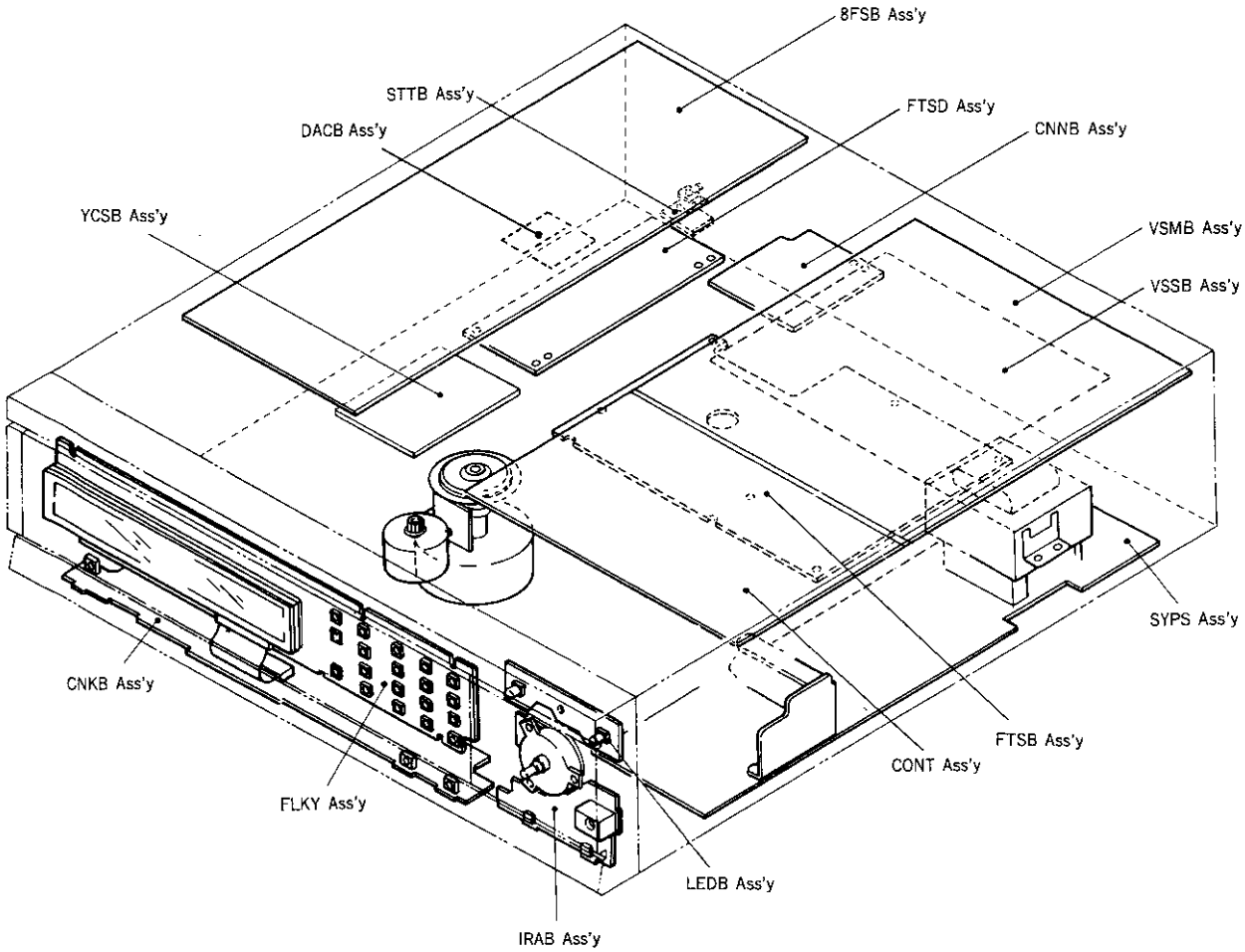
3.8 REMOTE CONTROL UNIT (VXX1268)



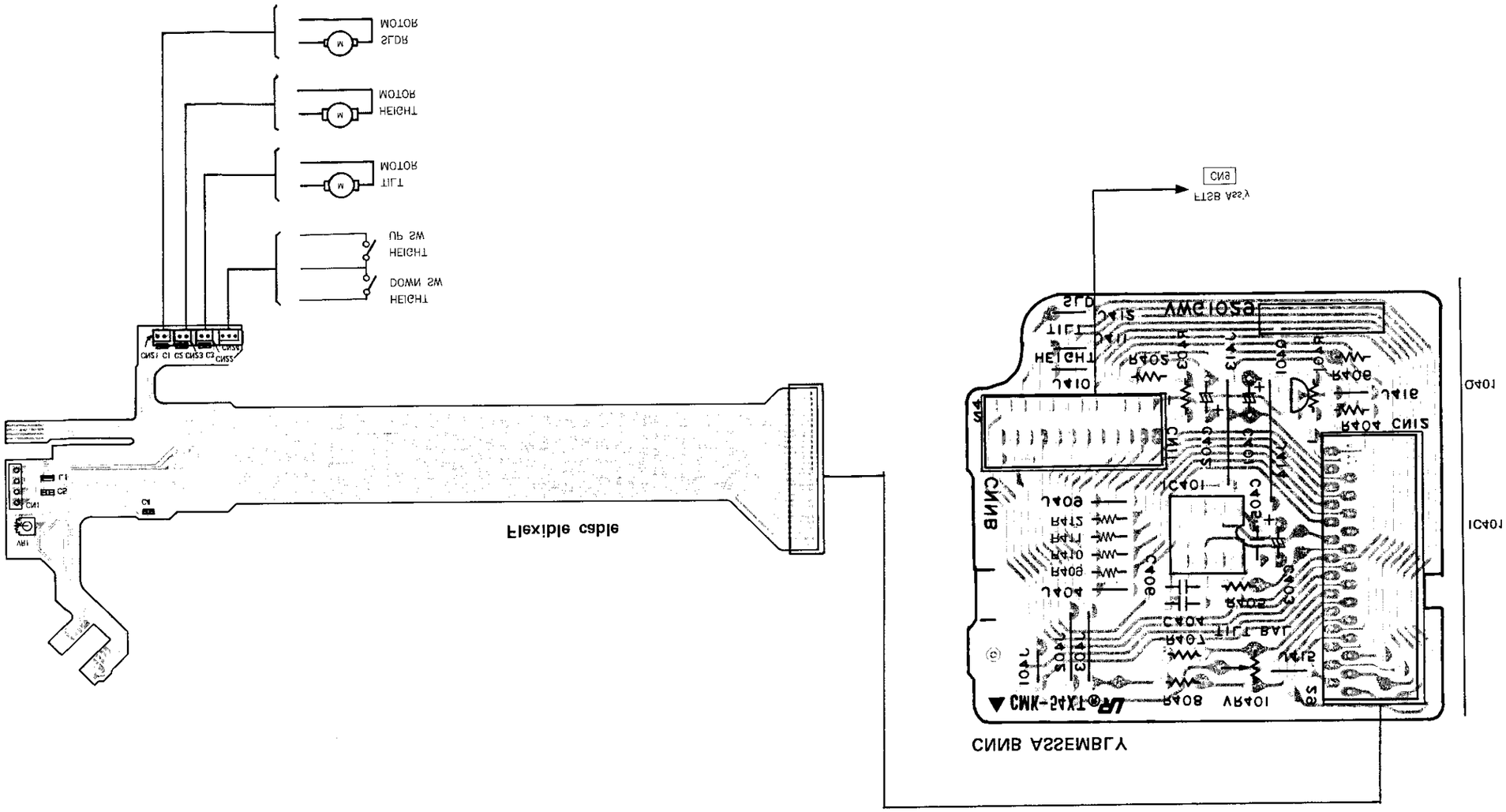
Mark	No.	Part No.	Description
	1.	VNK1114	Jog dial (Y)
	2.	VNK1108	Shatle ring
	3.	VAH1094	Aluminum plate
	4.	VSD1003	Rotary encoder
	5.	VNK1133	Battery cover

Mark	No.	Part No.	Description
	101.		Case (A)
	102.		Case (B)
	103.		Filter
	104.		Rubber attachment
	105.		Remote control transmission assembly
	106.		Terminal (A)
	107.		Terminal (B)
	108.		Screw
	109.		Screw
	110.		Screw

4. P.C. BOARD LOCATIONS

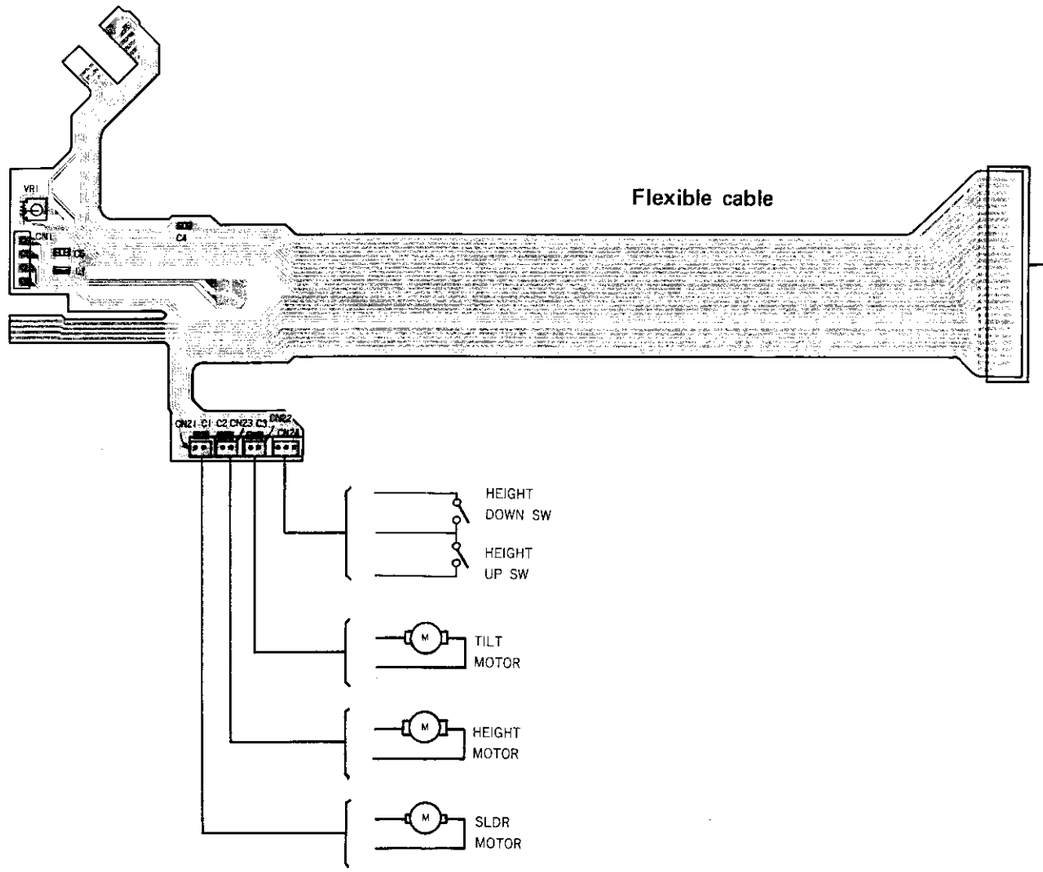


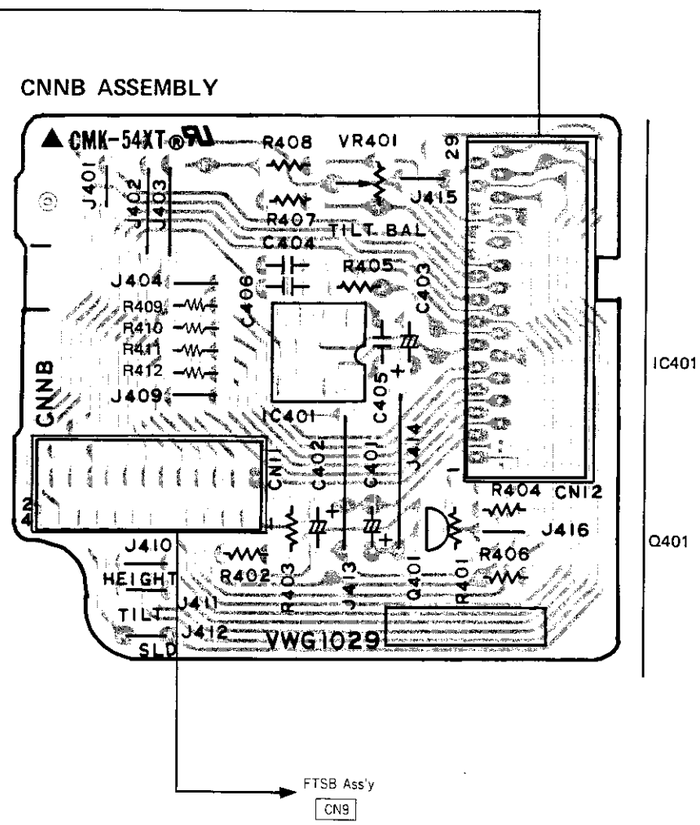
8FSB Ass'y VWV1077 (8FS Board) *Include DACB Assembly
FTSB Ass'y (Focus Tracking Slider Board)
FTSD Ass'y VWS1044 (Focus Tracking Slider Drive)
CNNB Ass'y (CoNNector Board)
VSMB Ass'y VWS1057 (Video System Main Board) *Include Thru. type capacitor Assembly
(VSMB Assemdly consists of Memory, VDEM and TBC sections.)
VSSB Ass'y VWS1045 (Video System Sub Board)
CONT Ass'y VWG1023 (CONTroller Board)
SYPS Ass'y VWR1013 (SYstem Power Supply)
LEDB Ass'y VWR1034 (LED Board)
IRAB Ass'y VWG1033 (InfraRed Amplifier Board)
FLKY Ass'y VWG1032 (FLorescent and KeYboard)
CNKY Ass'y VWG1031 (ConNector and KeYboard)
YCSB Ass'y (Y/C Separate Board)
STTB Ass'y (S terminal)
Note: VSOP Ass'y = VSSB Ass'y + VSMB Ass'y



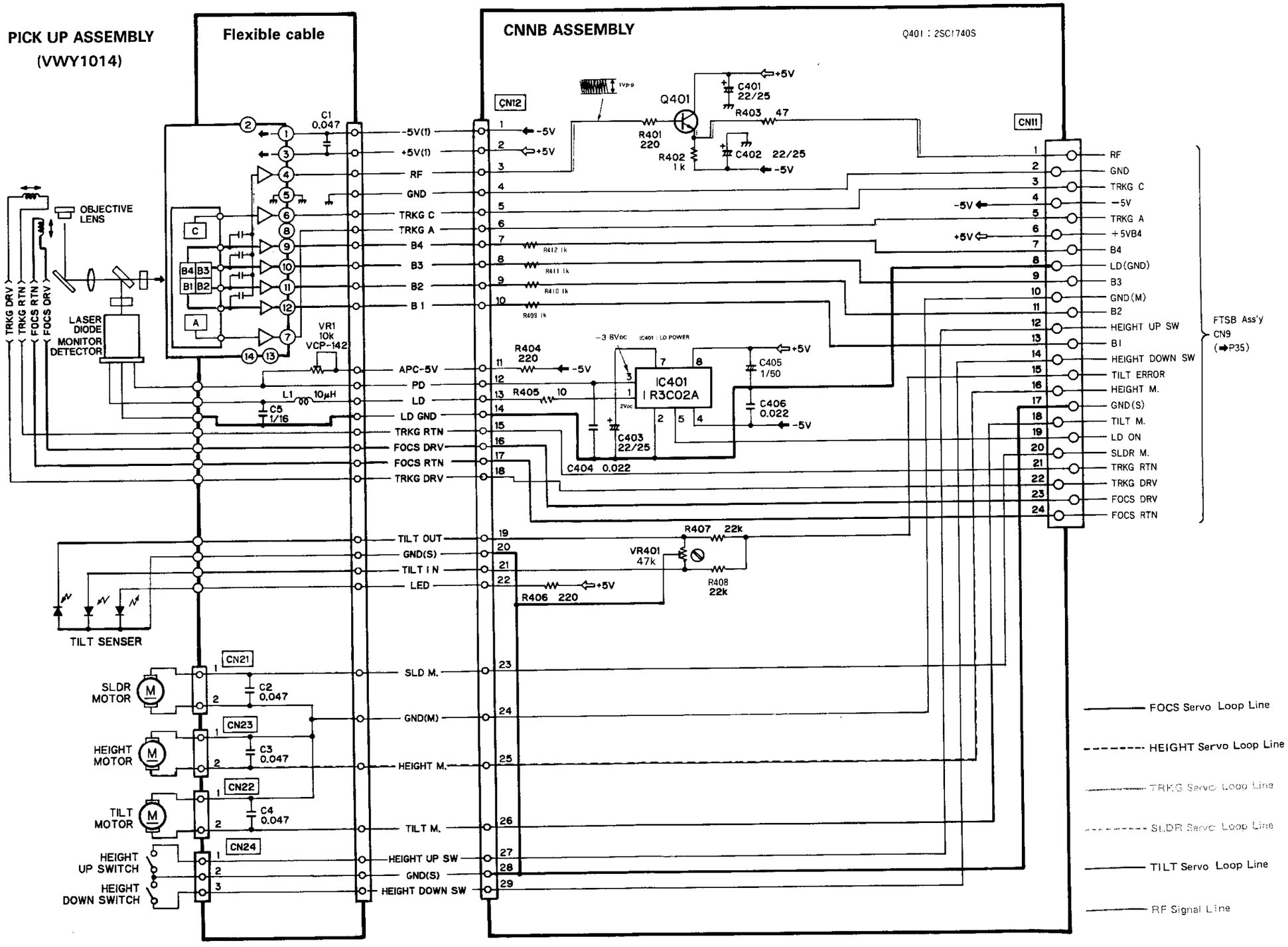
This P.C.B. connection diagram is viewed from the foil side.

This P.C.B. connection diagram is viewed from the parts mounted side.

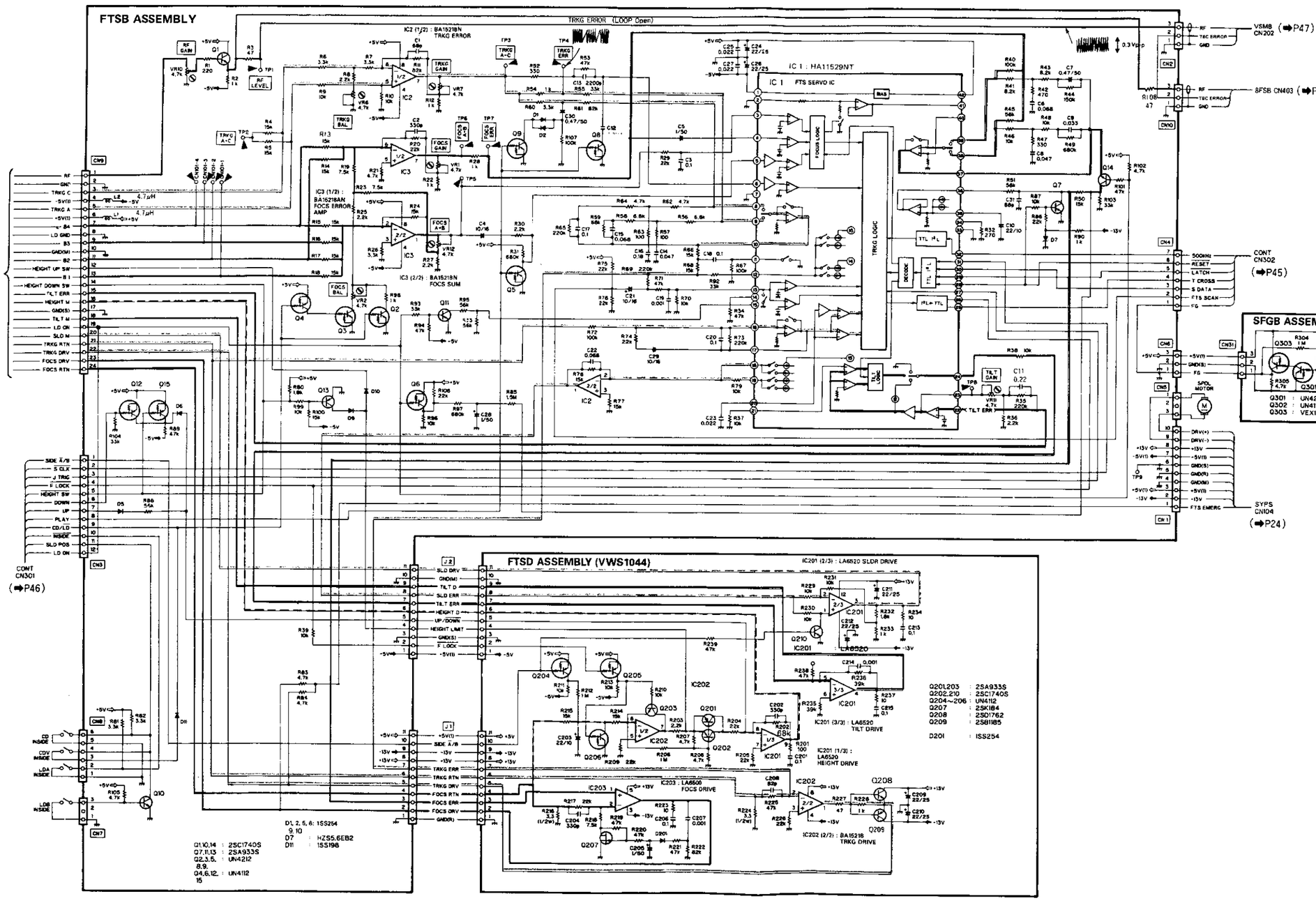




6. 2 PICK-UP AND CNNB ASSEMBLY

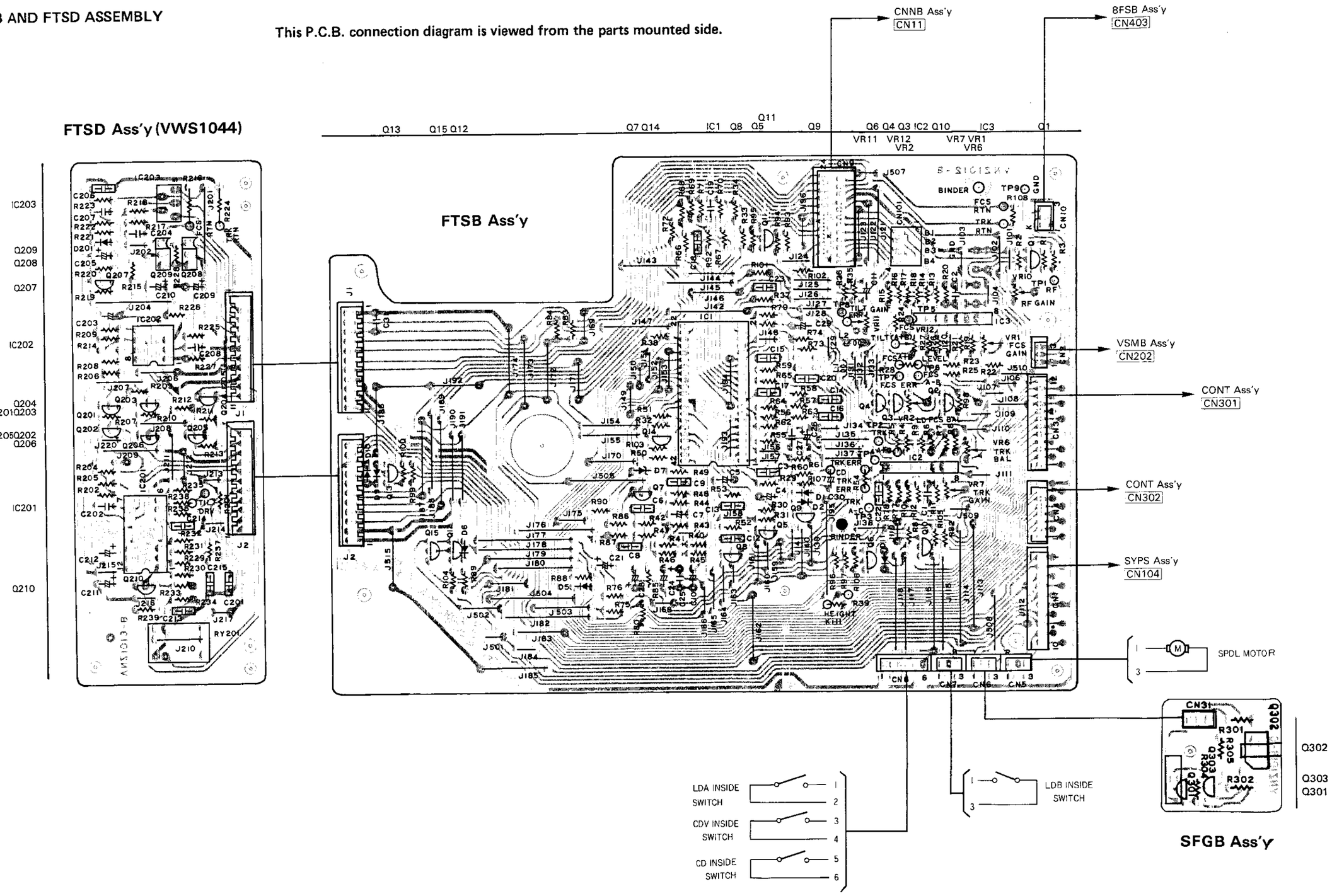


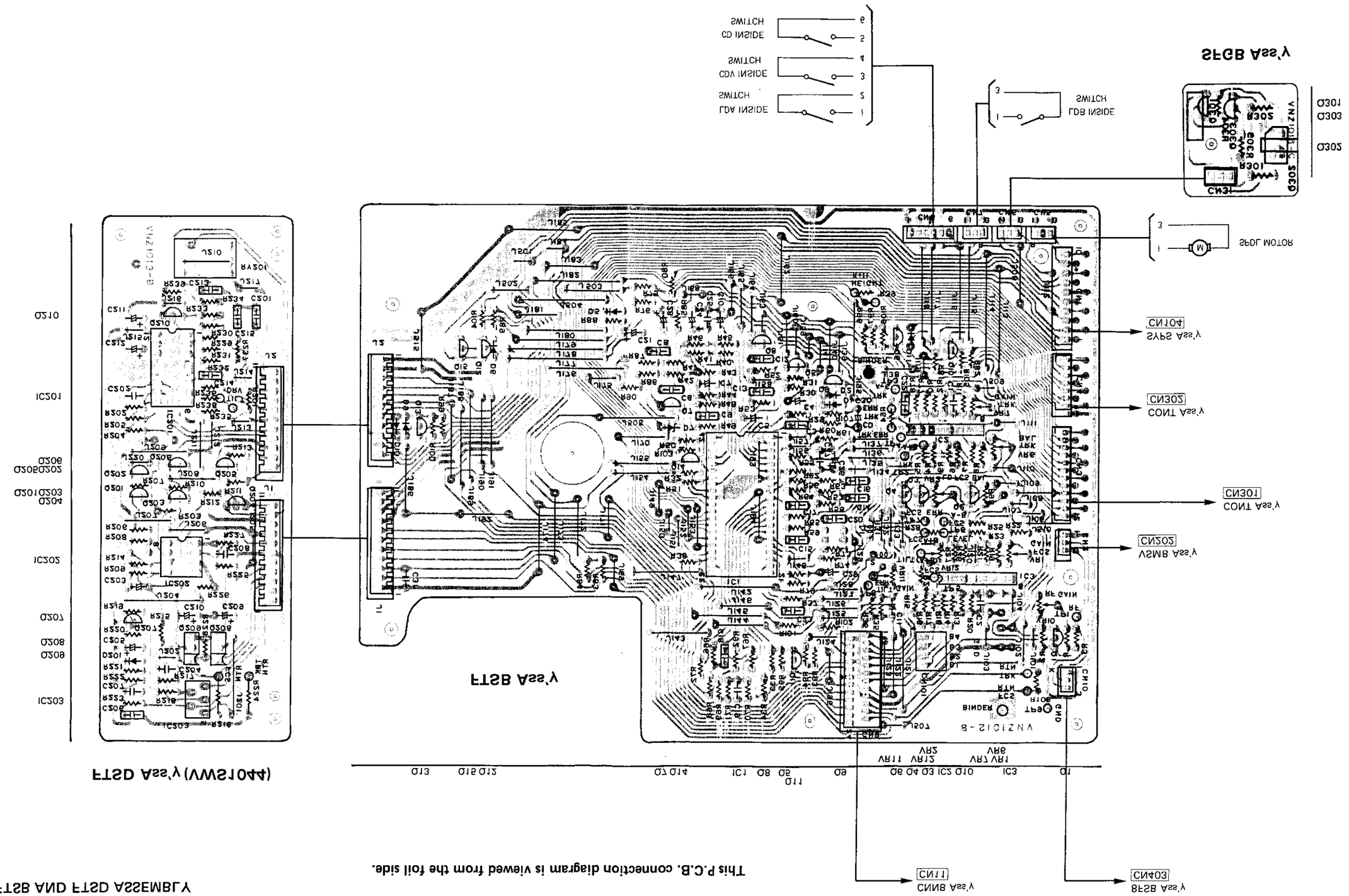
6. 3 FTSB, FTSD AND SFGB ASSEMBLY



FTSB AND FTSD ASSEMBLY

This P.C.B. connection diagram is viewed from the parts mounted side.

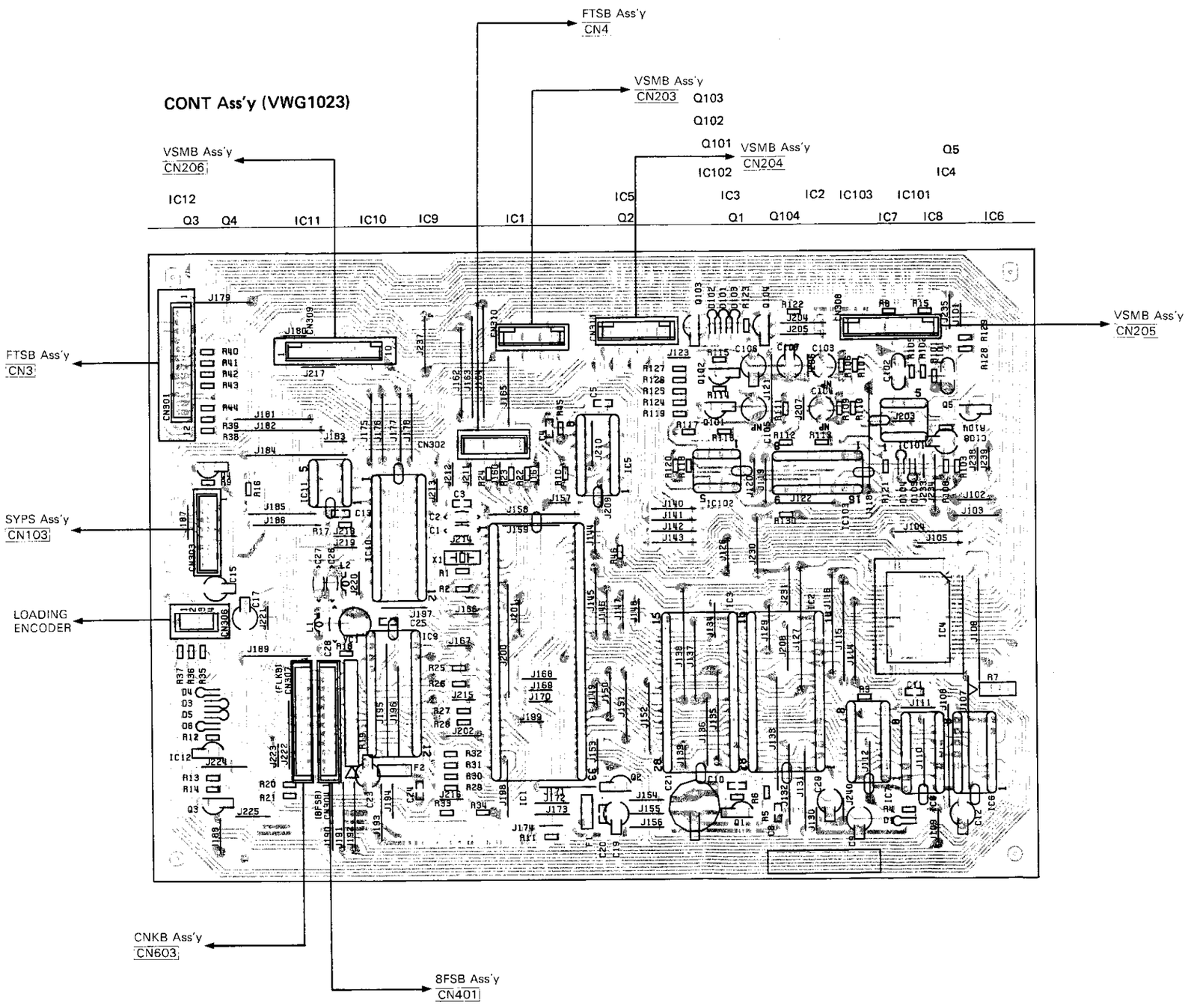


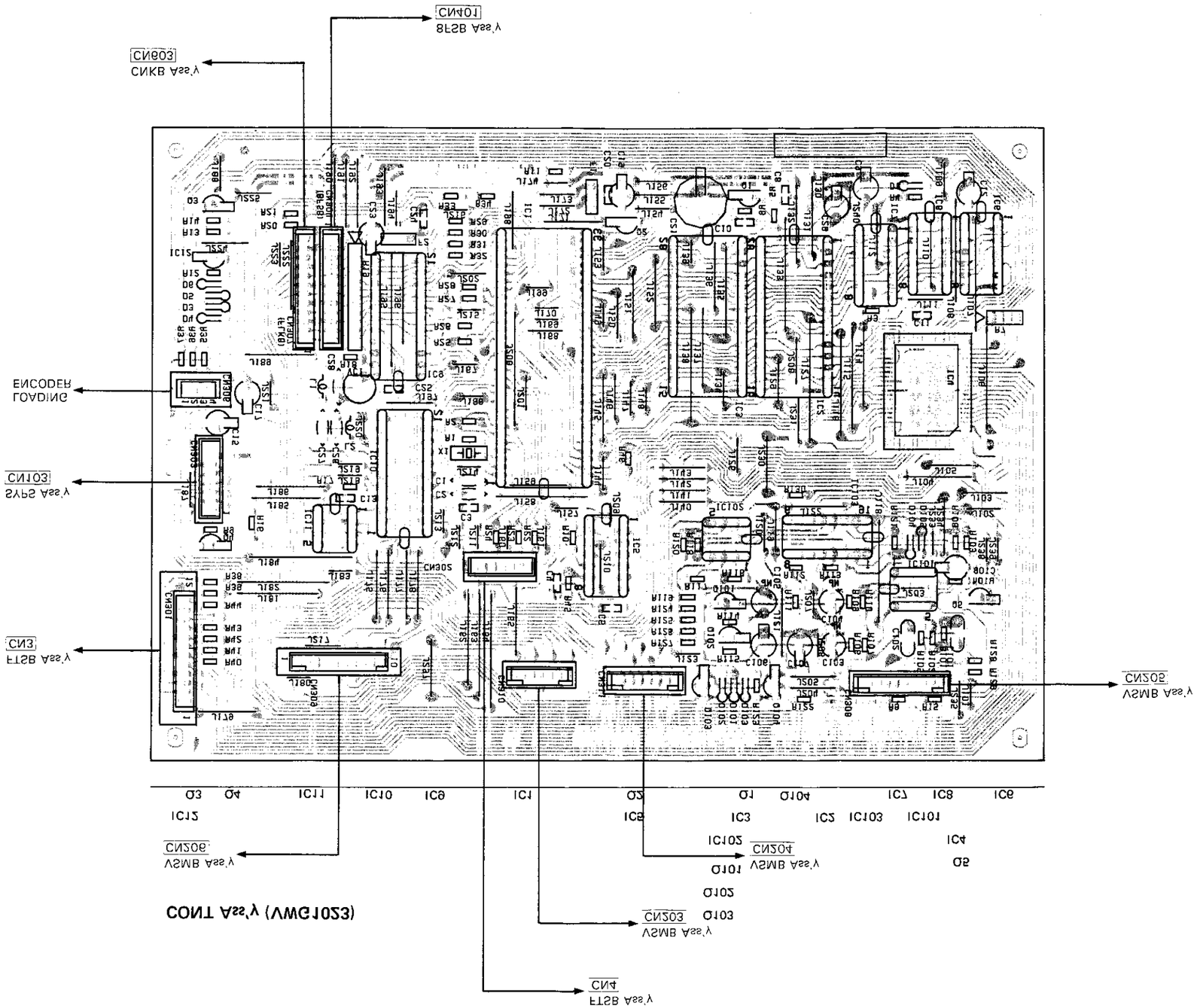


FTSB AND FTSD ASSEMBLY

This P.C.B. connection diagram is viewed from the parts mounted side.

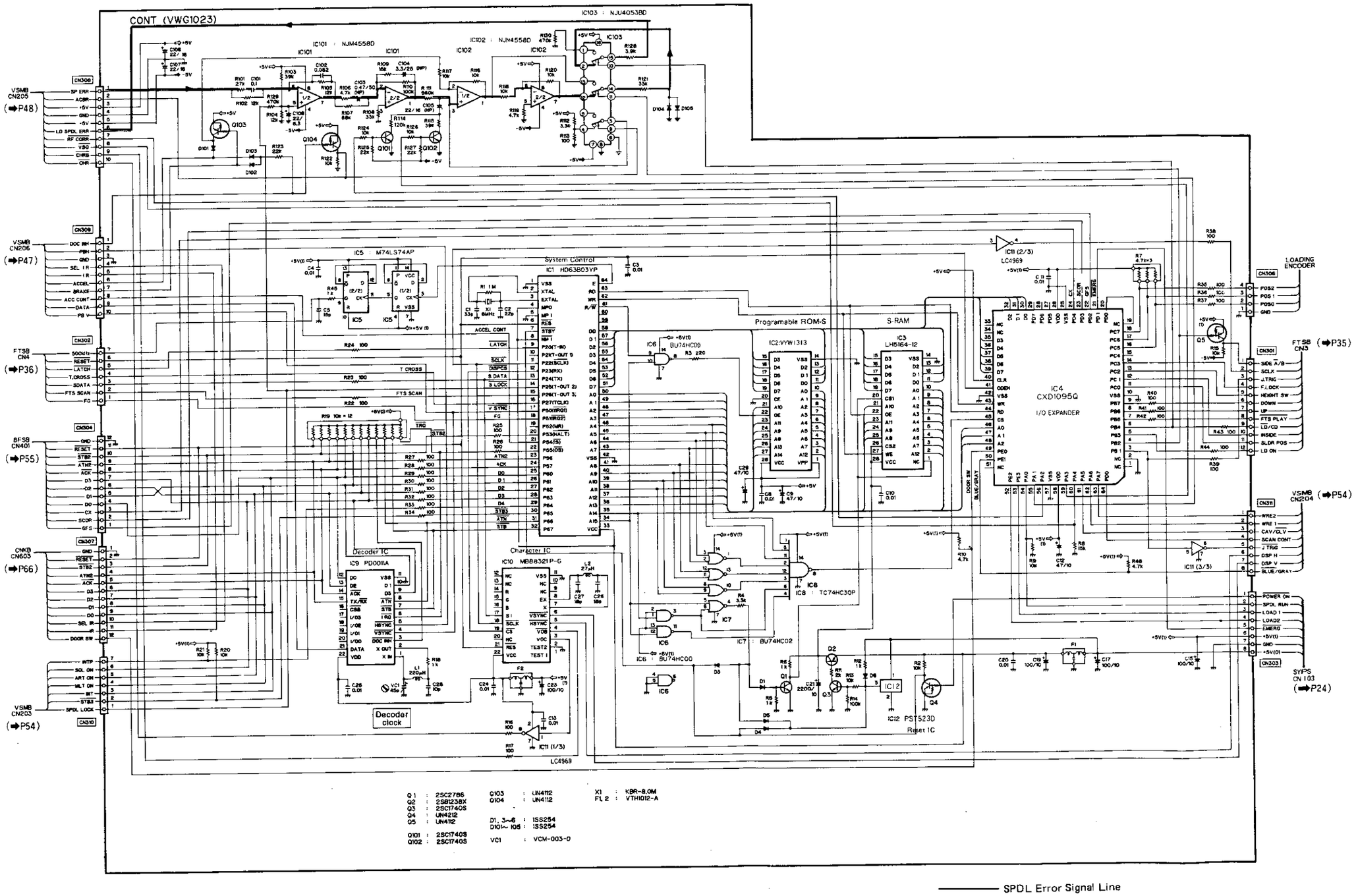
CONT Ass'y (VWG1023)



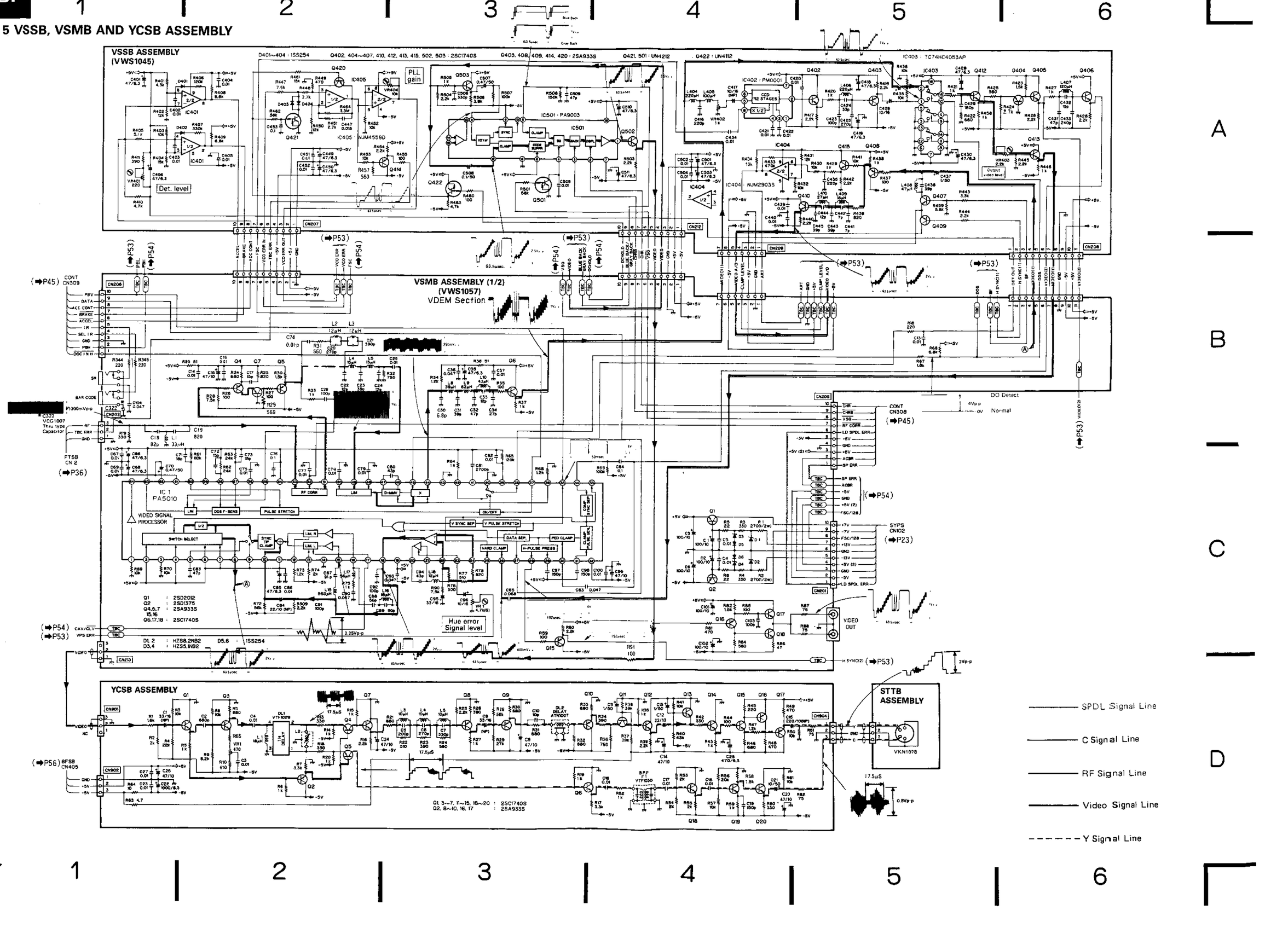


This P.C.B. connection diagram is viewed from the foil side.

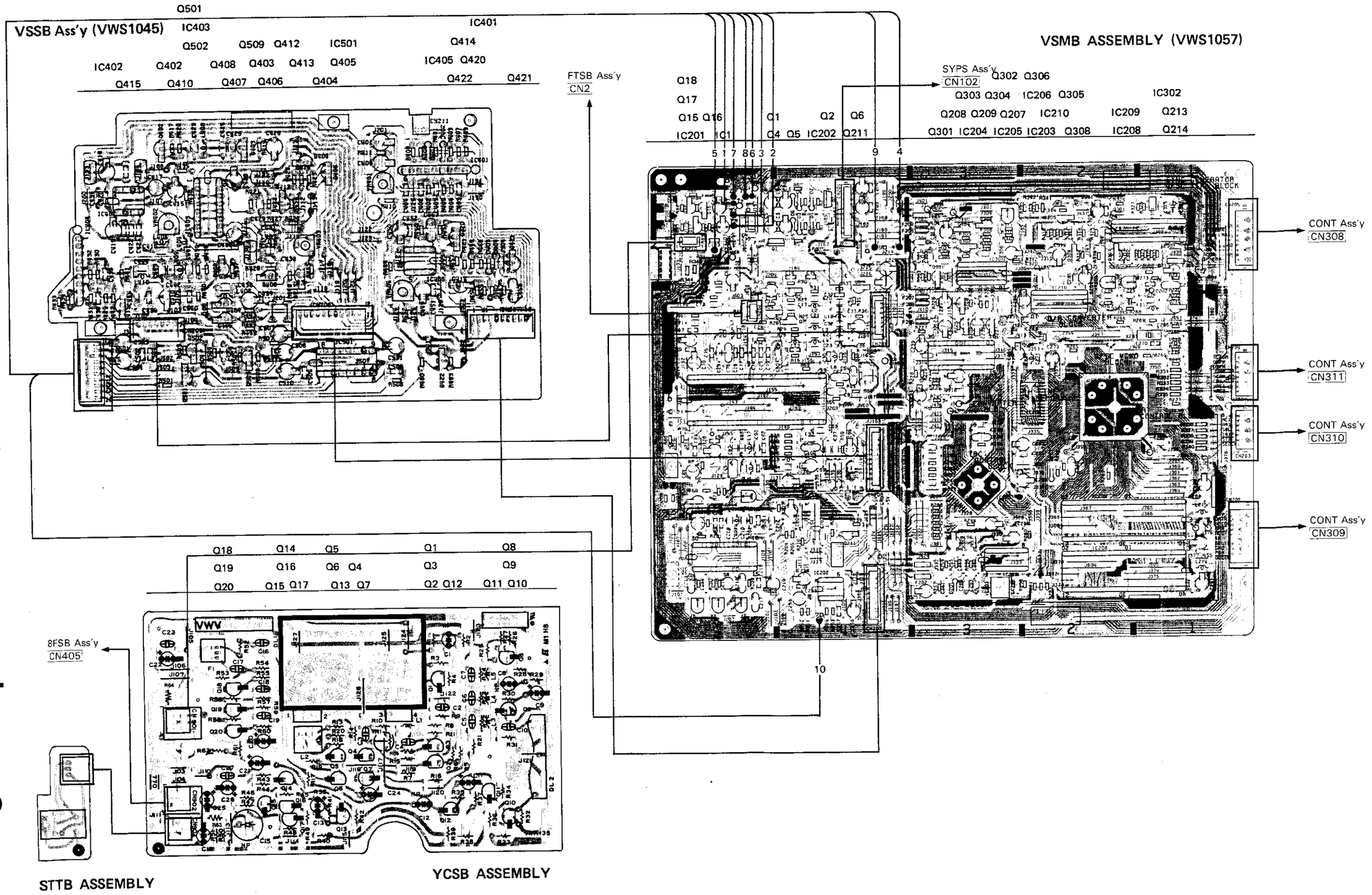
6. 4 CONT ASSEMBLY

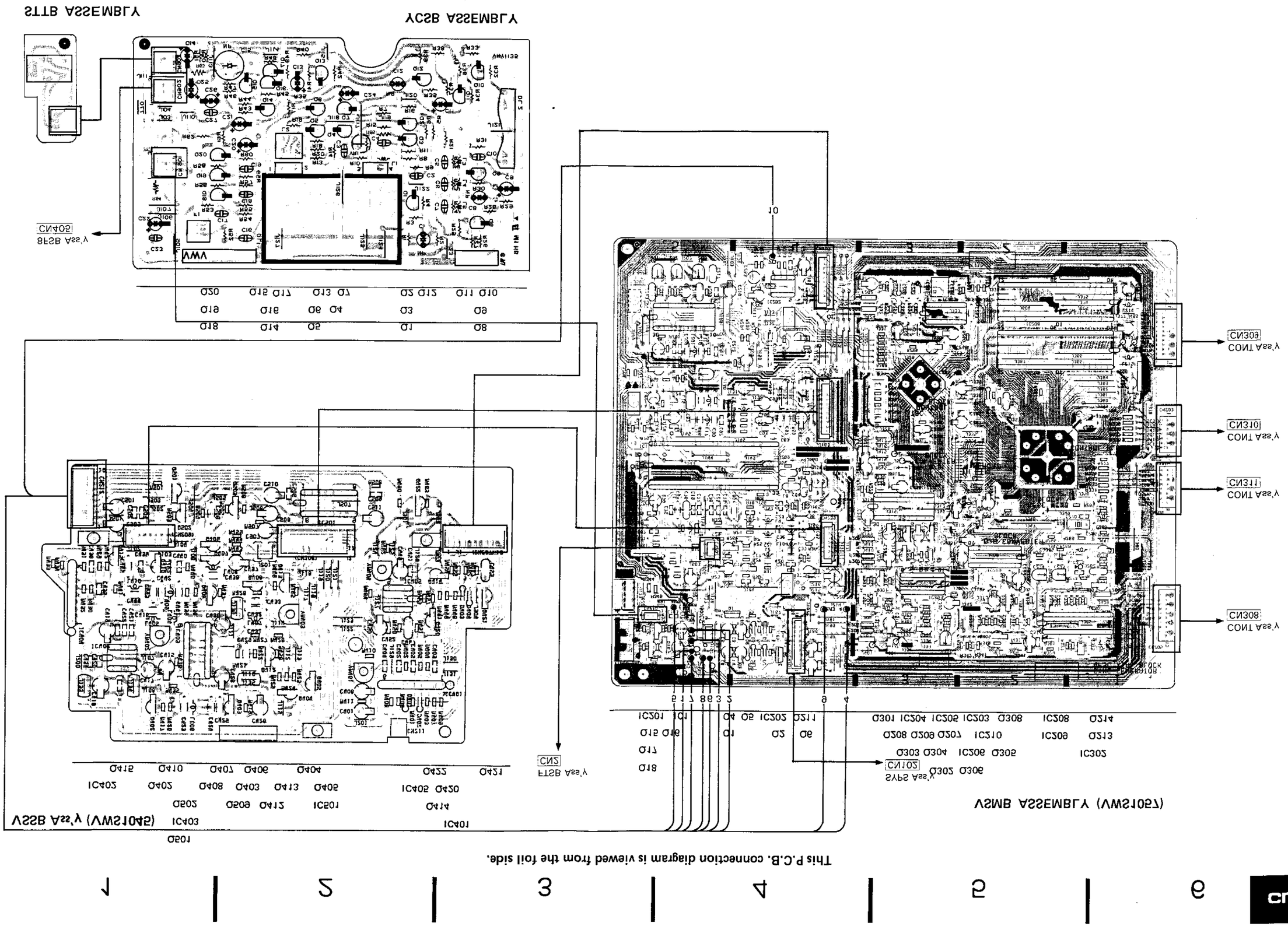


6. 5 VSSB, VSMB AND YCSB ASSEMBLY



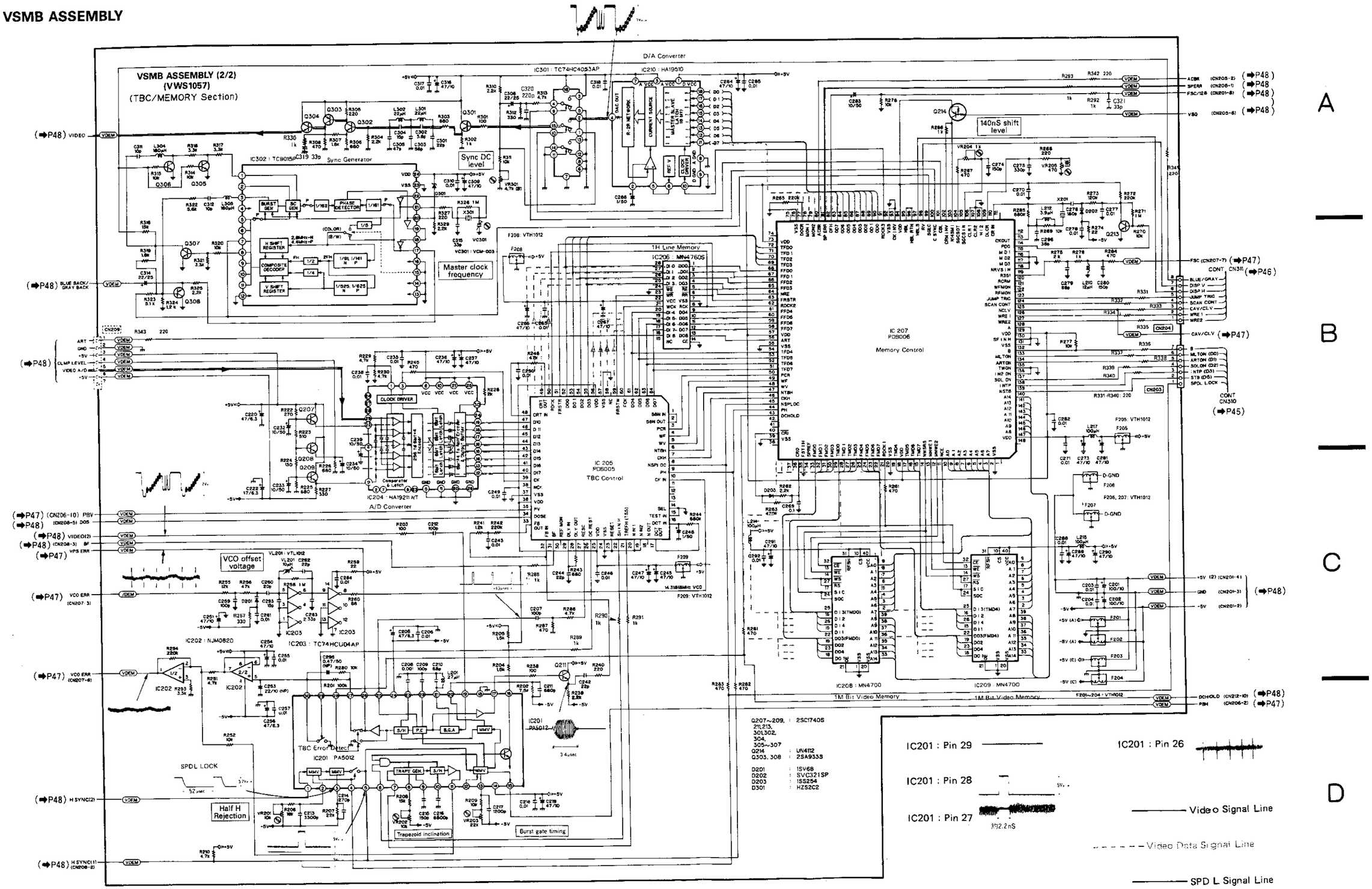
This P.C.B. connection diagram is viewed from the parts mounted side.



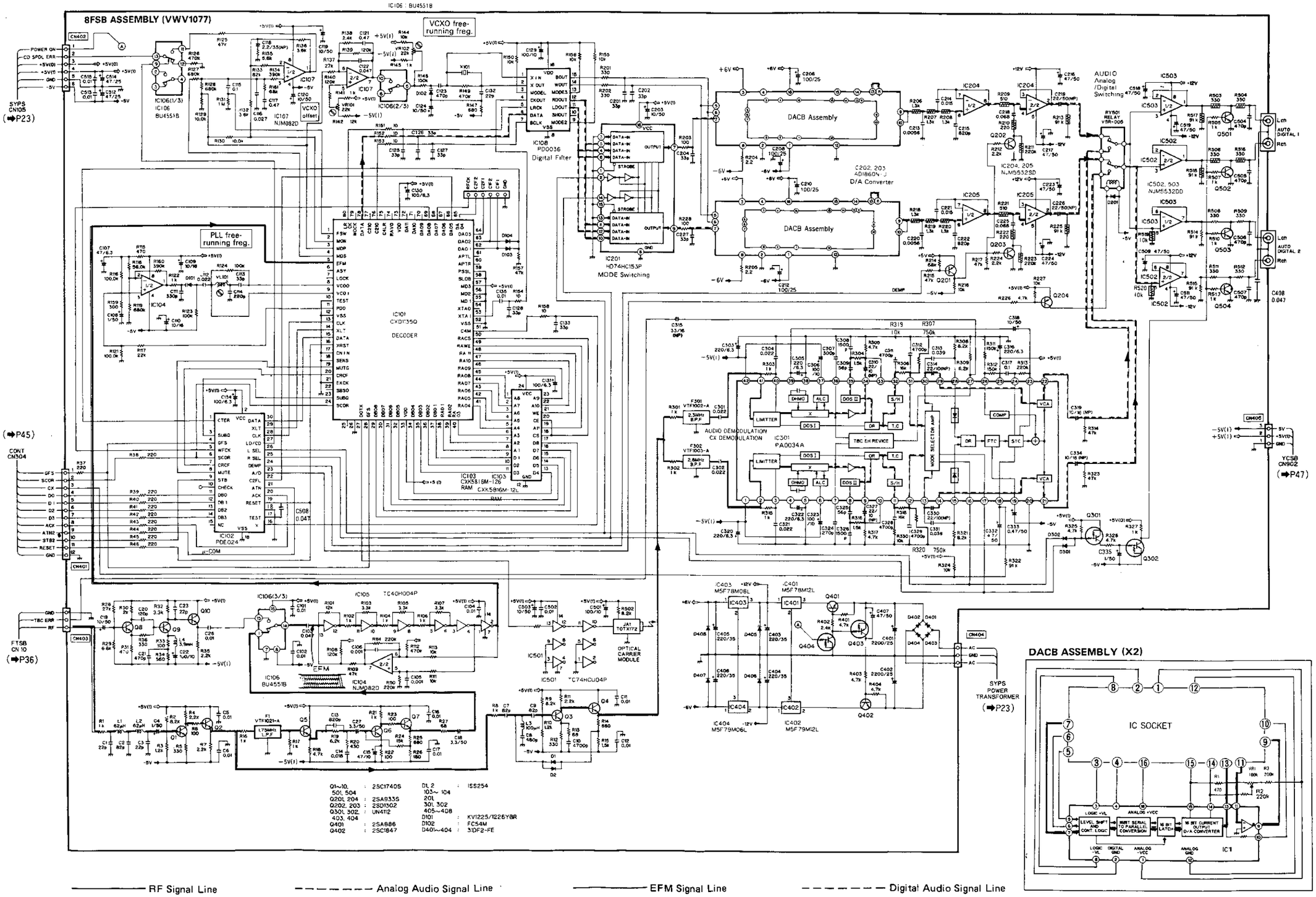


This P.C.B. connection diagram is viewed from the foil side.

6. 6 VSMB ASSEMBLY

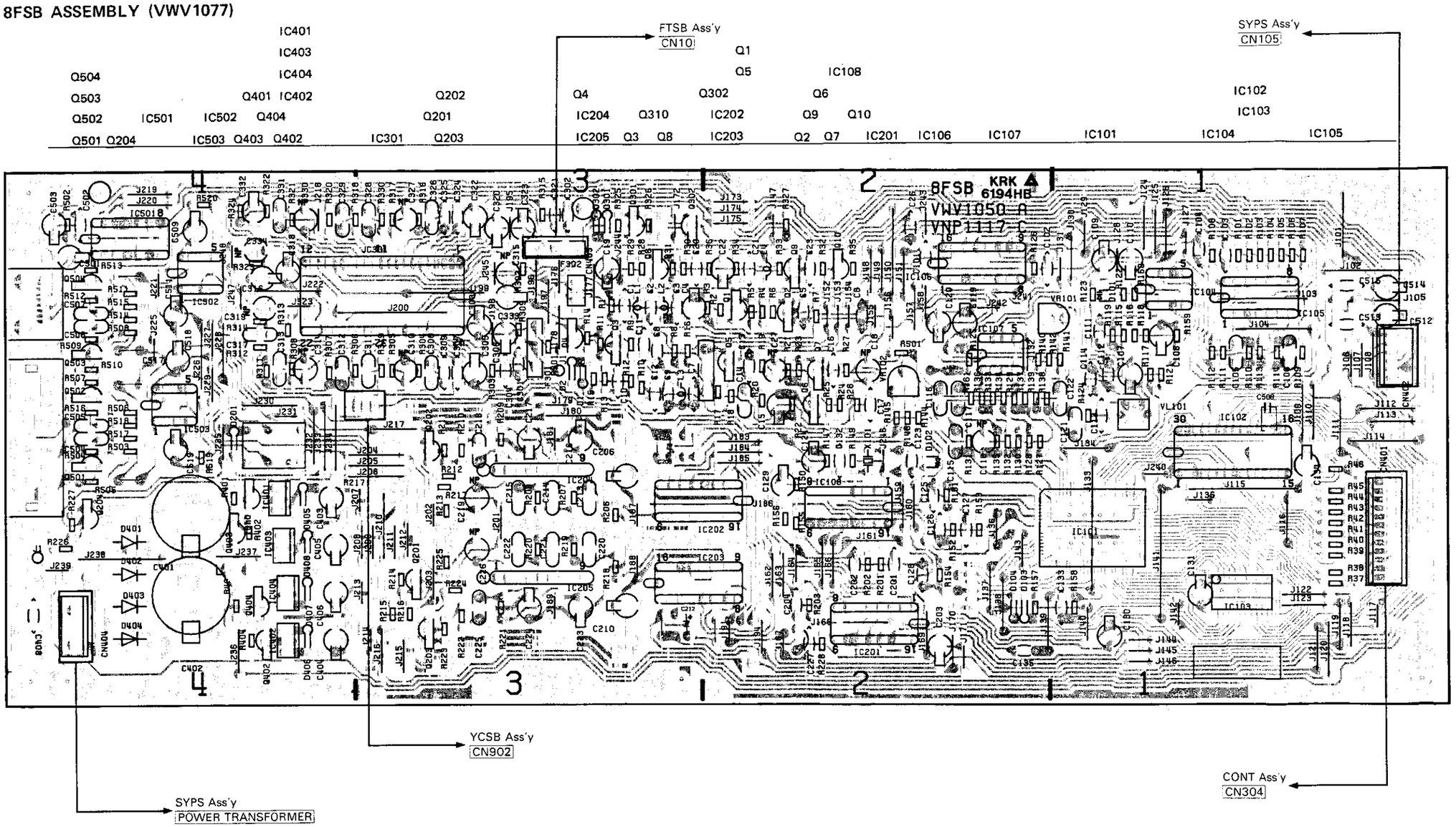


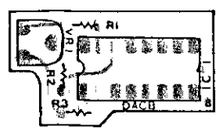
6. 7 8FSB ASSEMBLY



This P.C.B. connection diagram is viewed from the parts mounted side.

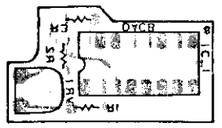
8FSB ASSEMBLY (VWV1077)

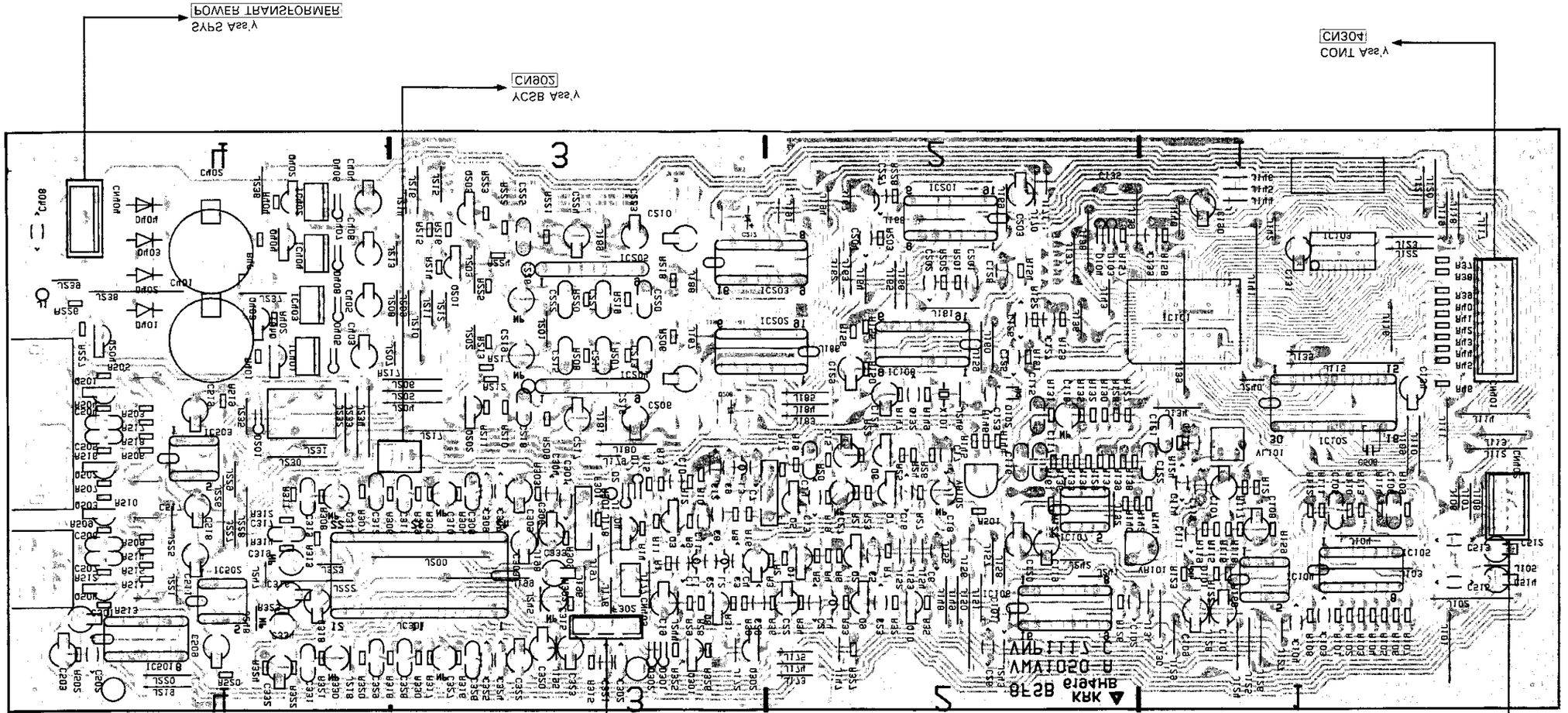




DACB ASSEMBLY

DACB ASSEMBLY



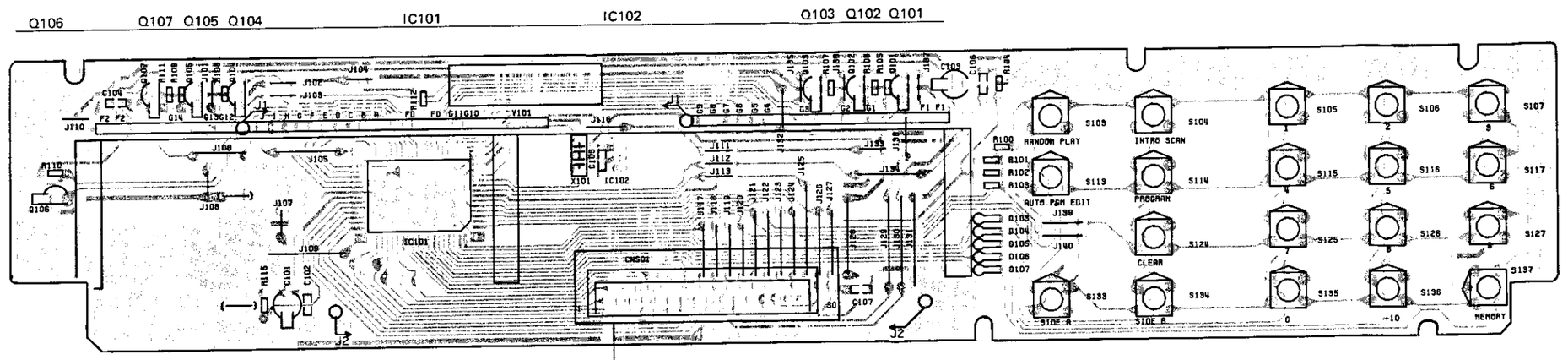


8F2B ASSEMBLY (VWV1777)

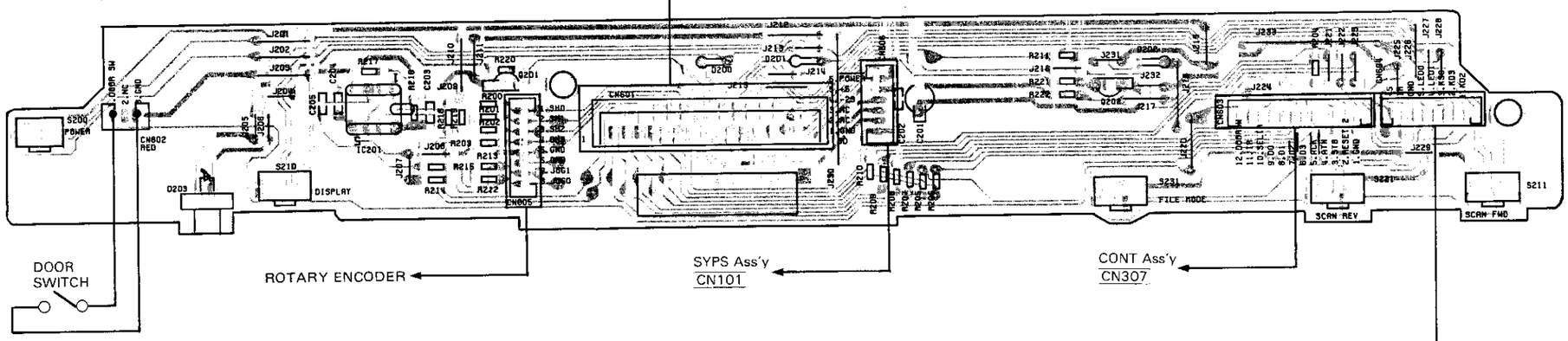
This P.C.B. connection diagram is viewed from the foil side.

This P.C.B. connection diagram is viewed from the parts mounted side.

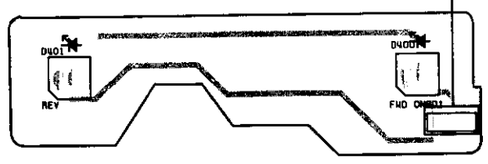
FLKY Ass'y (VWG1032)

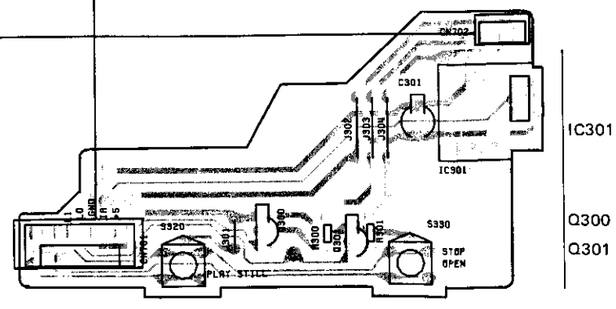


CNKB Ass'y (VWG1031)



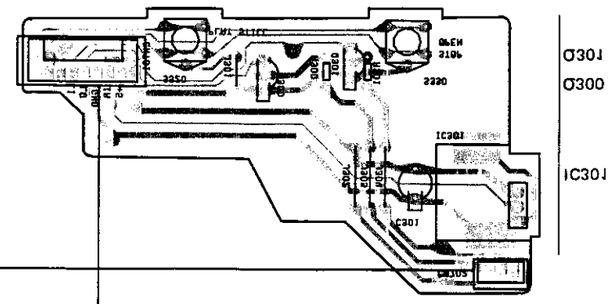
LEDB Ass'y (VWG1034)





IRAB Ass'y (VWG1033)

IRAB Ass'y (AWG1033)



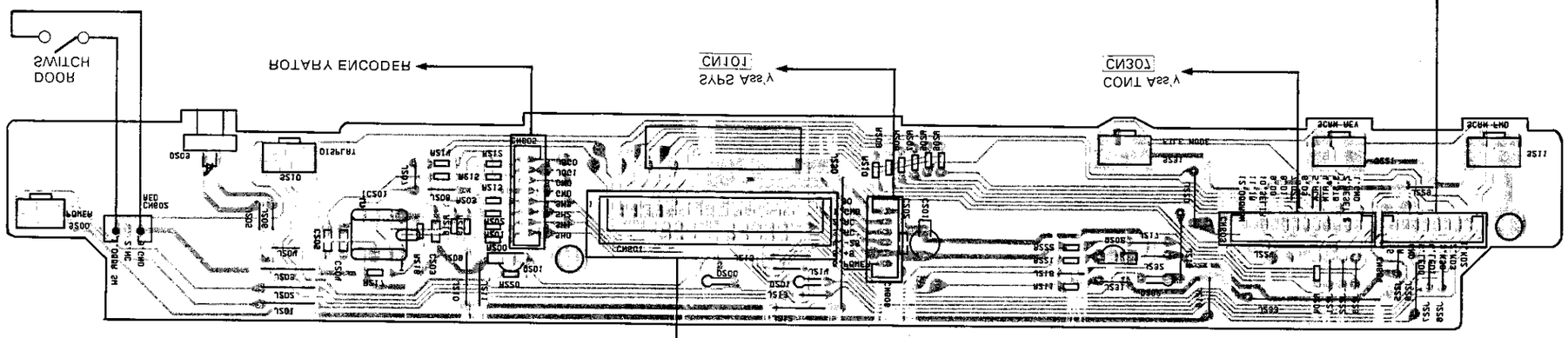
LEDB Ass'y (AWG1034)

SWITCH
DOOR

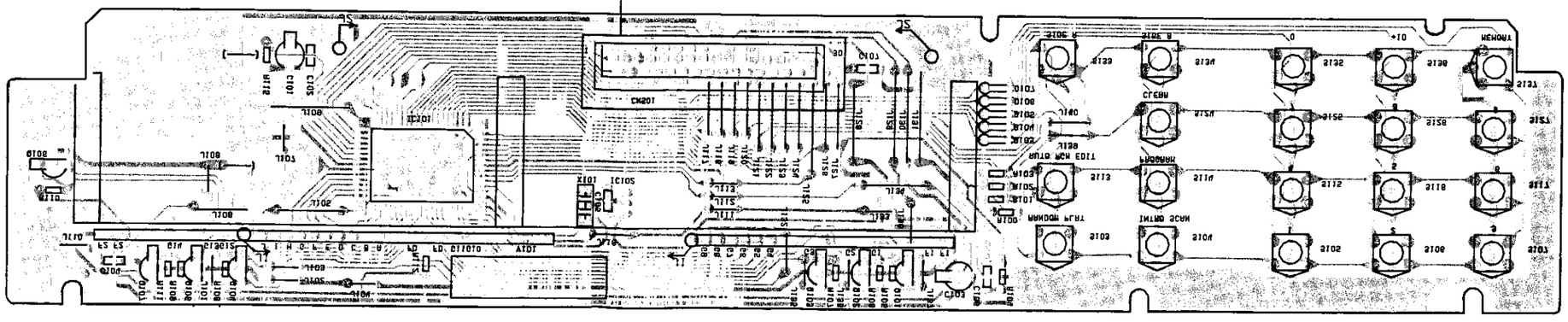
ROTARY ENCODER

SYS2 Ass'y

CONT Ass'y



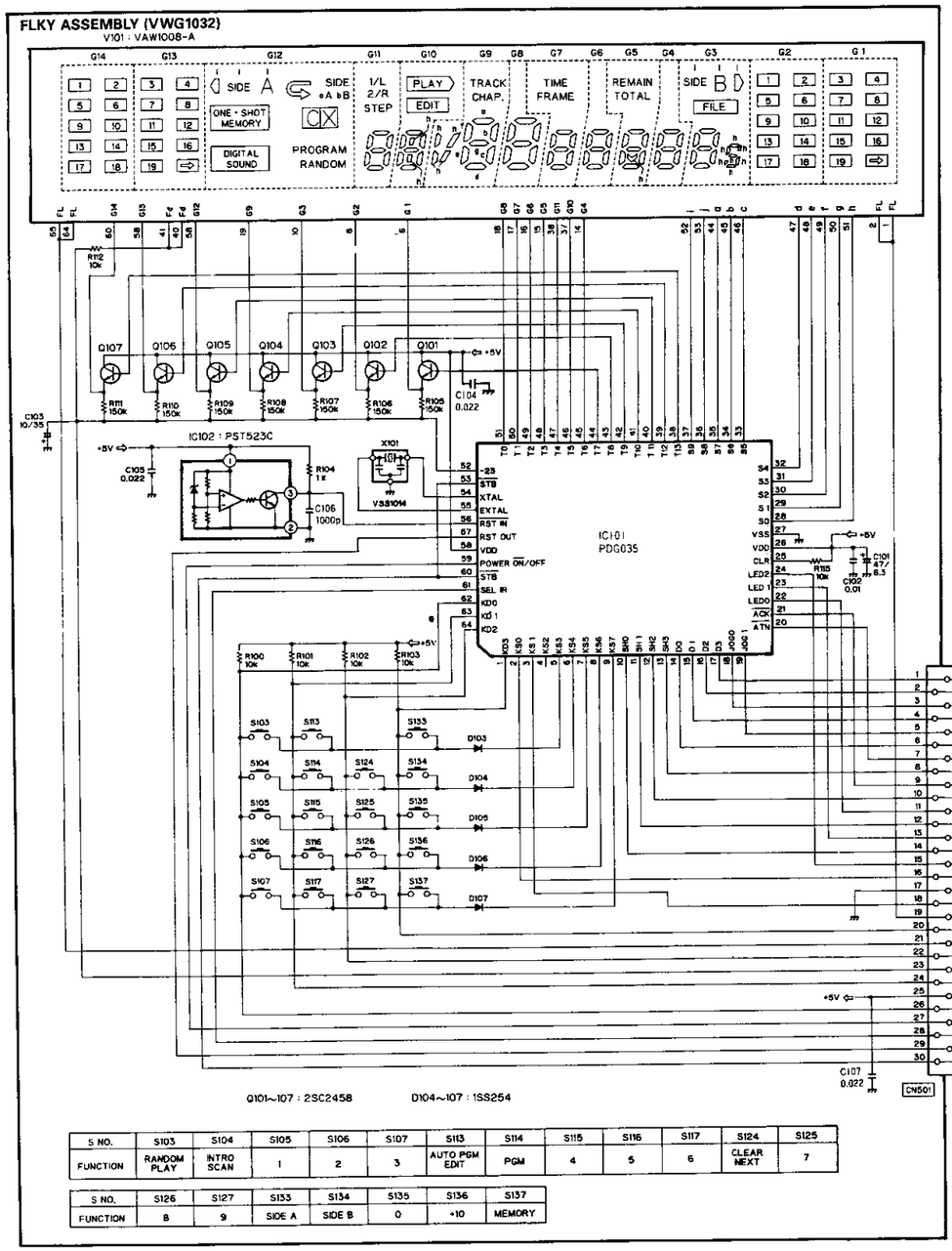
CNKB Ass'y (AWG1031)



This P.C.B. connection diagram is viewed from the foil side.

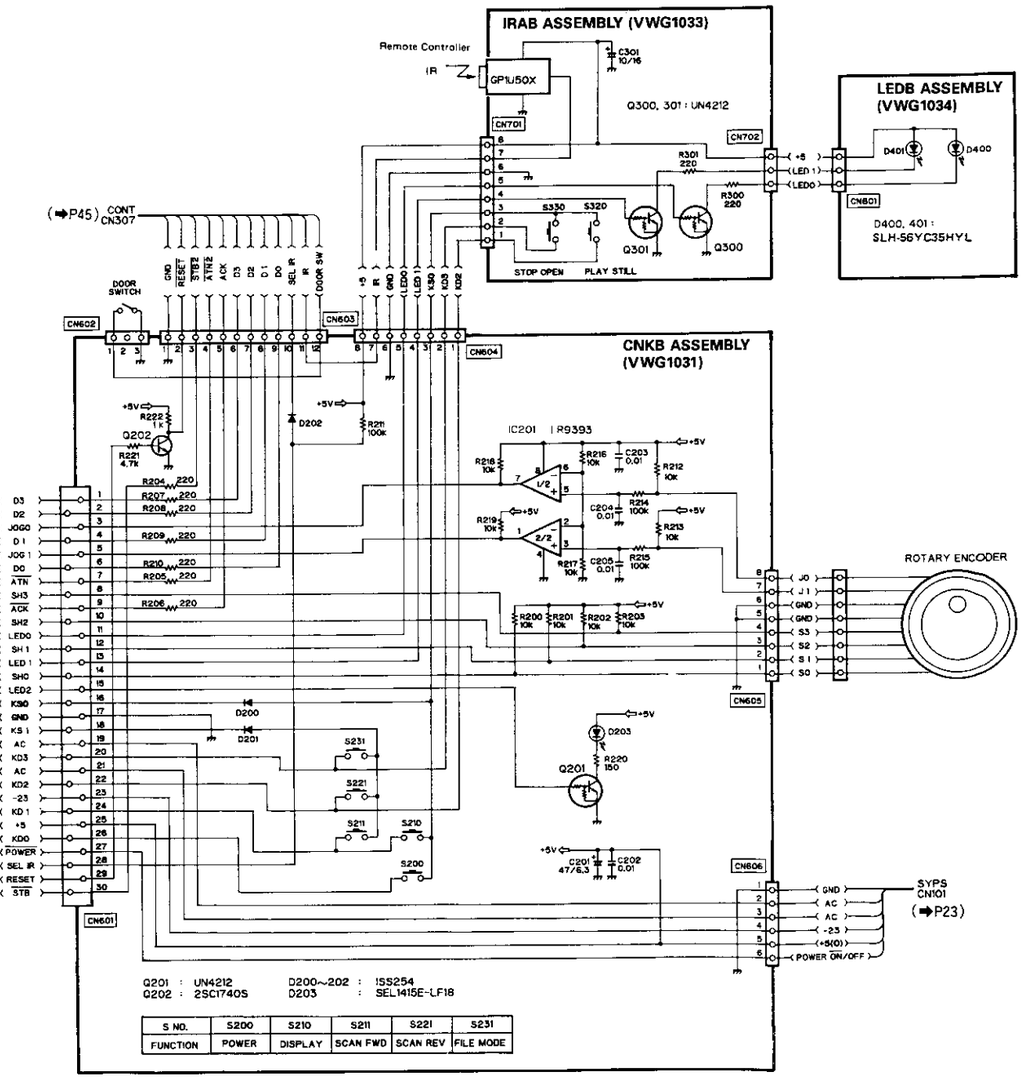
LEKY Ass'y (AWG1035)

6. 8 FLKY, CNKB, IRAB AND LEDB ASSEMBLY



S NO.	S103	S104	S105	S106	S107	S113	S114	S115	S116	S117	S124	S125
FUNCTION	RANDOM PLAY	INTRO SCAN	1	2	3	AUTO PGM EDIT	PGM	4	5	6	CLEAR NEXT	7

S NO.	S126	S127	S133	S134	S135	S136	S137
FUNCTION	8	9	SIDE A	SIDE B	0	+10	MEMORY



S NO.	S200	S210	S211	S221	S231
FUNCTION	POWER	DISPLAY	SCAN FWD	SCAN REV	FILE MODE

7. ELECTRICAL PARTS LIST

NOTES:

- *Parts without part number cannot be supplied.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560Ω	*56 × 10¹*	*561*	*RD1/4PS 5 6 1 J*
47kΩ	*47 × 10³*	*473*	*RD1/4PS 4 7 3 J*
0.5Ω	*0R5*		*RN2H 0 R 5 K*
1Ω	*010*		*RS1P 0 1 0 K*

Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62kΩ	*562 × 10¹*	*5621*	*RN1/4SR 5 6 2 1 F*

Miscellaneous

P.C. BOARD ASSEMBLIES

Mark	Symbol & Description	Part No.
◉	CONT assembly	VWG1023
◉	VSMB assembly	VWS1057
◉	VSSB assembly	VWS1045
◉	8FSB assembly	VWV1077
◉	SYPS assembly	VWR1013
	YCSB assembly	
◉	FLKY assembly	VWG1032
◉	CNKB assembly	VWG1031
◉	IRAB assembly	VWG1033
◉	LEDB assembly	VWG1034
	CNNB assembly	
	SFGB assembly	
	FTSB assembly	
◉	FTSD assembly	VWS1044
	STTB assembly	
	DACB assembly	

OTHERS

Mark	Symbol & Description	Part No.
	Van card	VDA1132
⚠	AC power cord	VDG1026
⚠	Fuse (FU1, FU2) (3A)	VEK-018
⚠	Fuse (FU3, FU4) (2A)	VEK-022
	Rotary encoder	VSD1005
	Slide switch	VSK1010
⚠	Power transformer (T1)	VTT1052
	Program PROM-S (CONT assembly, IC2)	VYW1313
	FFC	VDA1116
	Slide switch (CDV/LD-A, LD-B)	VSK1003
	Slide switch (CD Inside)	VSK1009
	Spindle motor	VXM1026
	Encoder	VSD1004
	Loading motor assembly-S	VXX1229
	Carriage assembly	VWT1042
	Pick-up assembly	VWY1014
	Slider motor assembly-S	VXX1226
	Tilt (Height) motor assembly-S	VXX1227
	Thru. type capacitor assembly	
	Thru. type capacitor	VCG1007

◉ CONT Assembly (VWG1023)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC6	BU74HC00
	IC7	BU74HC02
	IC4	CXD1095Q
	IC1	HD63B03YP
	IC5	M74LS74AP
	IC11	LC4969
	IC9	PD0011A
	IC12	PST523D
	IC8	TC74HC30AP
	IC3	LH5164-12
	IC10	MB88321P-G
	IC101, IC102	NJM4558D
	IC103	NJU4053BD
	Q5, Q103, Q104	UN4112
	Q4	UN4212
	Q1	2SC2786
	Q2	2SB1238X
	Q3, Q101, Q102	2SC1740S
	D1, D3 – D6, D101 – D105	1SS254

COILS AND FITLERS

Mark	Symbol & Description		Part No.
	L1	Axial inductor	LAU221J
	L2	Axial inductor	LAU270J
	F1, F2	EMI filter	VTH1012

CAPACITORS

Mark	Symbol & Description	Part No.
	C28	CCCCH200J50
	C26, C27	CCCCH180J50
	C2	CCCCH220J50
	C1	CCCCH330J50
	C5	CCPUSL150J50
	C103	CEALNPR47M50
	C105	CEALNP220M16
	C104	CEALNP3R3M25
	C106, C107	CEAL220M16
	C108	CEAL220M6R3
	C15, C17, C19, C23	CEAS101M10
	C21	CEAS222M10
	C9, C12, C29	CEAS470M10
	C101	CFTXA104J50
	C102	CFTXA823J50
	C3, C4, C8. C10, C11, C13, C20, C24, C25	CKPUYY103N16
	VC1 Ceramic trimmer	VCM-003

RESISTORS

Mark	Symbol & Description	Part No.
	R7 Resistor array (4.7k x 3)	VCN1016
	R19 Resistor array (10k x 12)	VCN1017
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	IC socket (28P)	VKH1001
	X1 Ceramic resonator	KBR-8.0M

◉ VSMB Assembly(VWS1057)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC204	HA19211NT
	IC210	HA19510
	IC208, IC209	MN4700
	IC206	MN4760S
	IC202	NJM082D
	IC1	PA5010
	IC201	PA5012
	IC205	PDB005
	IC207	PDB006
	IC203	TC74HCU04AP
	IC301	TC74HC4053AP
	IC302	TC9015P
	Q214	UN4112
	Q4, Q5, Q7, Q15, Q16, Q303, Q308	2SA933S
	Q2	2SB1375
	Q6, Q17, Q18, Q207 – Q209, Q211, Q213, Q301, Q302, Q304 – Q307	2SC1740S
	Q1	2SD2012
	D301	HZS2C2
	D3, D4	HZS5.1NB1
	D1, D2	HZS8.2NB2
	D202	SVC321SP
	D5, D6, D203	1SS254
	D201	1SV68

COILS AND FILTERS

Mark	Symbol & Description		Part No.
	L2, L3, L4, L5, L18, L210 Axial inductor		LAU120J
	L16	Axial inductor	LAU180J
	L304, L305	Axial inductor	LAU181J
	L301, L302	Axial inductor	LAU220J
	L201	Axial inductor	LAU270J
	L212	Axial inductor	LAU3R9J
	L8	Axial inductor	LAU390J
	L10	Axial inductor	LAU430J
	L1, L17	Axial inductor	LAU560J
	L9	Axial inductor	LAU620J
	L15	Radial inductor	LRA561K
	L214, L215, L217 Coil (100μH)		VTL-035
	VL201	Variable coil	VTL1012
	F201 – F209 EMI filter		VTH1012

CAPACITORS

Mark	Symbol & Description	Part No.
	C311, C312	CCCCH100D50
	C29, C207, C209, C212, C259	CCCCH101J50
	C89	CCCCH111J50
	C24	CCCCH120J50
	C72, C73, C304	CCCCCH150J50
	C97, C98, C274, C280	CCCCH151J50
	C71	CCCCH180J50
	C260	CCCCH200J50
	C242, C244, C301	CCCCH220J50
	C22, C34	CCCCH270J50
	C263, C315, C319, C321	CCCCH330J50
	C296	CCCCH360J50
	C23, C31	CCCCH390J50
	C94	CCCCH430J50
	C32, C305	CCCCH470J50
	C88, C303	CCCCH560J50
	C210, C279	CCCCH680J50
	C87	CCCCH910J50
	C20, C214	CCCSL271J50
	C275	CCCSL331J50
	C276	CCCUJ181J50
	C262	CCCUJ220J50
	C21	CCCSL391J50
	C320	CCDSL221J50
	C33	CCPUCH120J50
	C17, C293	CCPUCH150J50
	C302	CCPUCH5R6K50
	C30	CCPUCH6R8K50
	C80	CCPUSL430J50
	C18, C83	CCPUSL470J50
	C295	CEALNPR47M50
	C70	CEALR47M50
	C96	CEAL100M16
	C35, C66, C68, C85, C205, C220, C222, C256	CEAL470M6R3
	C84	CEANP220M10

Mark	Symbol & Description		Part No.
	C248, C286		CEAS010M50
	C232 – C234, C239, C283		CEAS100M50
	C6, C101, C102, C201, C202		CEAS101M10
	C306, C314		CEAS220M25
	C95		CEAS330M16
	C15, C99, C219, C236, C237, C245, C247, C251, C254, C266, C267, C273, C281, C284, C289, C290, C291, C309, C316		CEAS470M10
	C1, C2, C5		CEHAQ101M10
	C253		CEJANP220M10
	C64, C76, C269		CFTXA104J50
	C65		CFTXA683J50
	C36, C63, C90, C93		CGCYX473M25
	C250		CFTXA183J50
	C92, C103		CKPUYB101K50
	C208		CKPUYB102K50
	C211		CKPUY681K50
	C3, C4, C13, C14, C16, C25, C37, C67, C69, C74, C75, C77 – C79, C86, C100, C203, C204, C206, C218, C235, C238, C243, C246, C249, C255, C257, C261, C264, C265, C270, C271, C278, C282, C285, C288, C292, C310, C317, C318		CKPUYY103N16
	C19		CKPUYB151K50
	C82, C277		CQMA103J50
	C217		CQMA122J50
	C81		CQMA272J50
	C213		CQMA332J50
	C216		CQMA682J50
	C215		CQSA151J50
	VC301	Ceramic trimmer	VCM-003

RESISTORS

Mark	Symbol & Description		Part No.
	VR1	Semi-fixed (4.7k)	VRTG6VS472
	VR301	Semi-fixed (4.7k)	VRTB6VS472
	VR205	Semi-fixed (470)	VRTB6VS471
	VR203	Semi-fixed (22k)	VRTB6VS223
	VR201, VR202	Semi-fixed (10k)	VRTB6VS103
	VR204	Semi-fixed (1k)	VRTB6VS102
	R61 – R63, R65, R68		RN1/6PQ□□□□□F
	R1, R2		RD1/2PM271J
		Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
		Pin jack (2P)	VKB1009
		Mini jack (2P)	VKN-183
	X301	Crystal resonator	VSS1005
	X201	Crystal resonator	VSS1021

◉ VSSB Assembly (VWS1045)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC401, IC404	NJM2903S
	IC405	NJM4558D
	IC501	PA9003
	IC402	PM0001
	IC403	TC74HC4053AP
	Q422	UN4112
	Q421, Q501	UN4212
	Q403, Q408. Q409, Q414,. Q420	2SA933S
	Q402, Q404 – Q407, Q410, Q412, Q413, Q415, Q502, Q503	2SC1740S
	D401 – D404	1SS254

COILS

Mark	Symbol & Description		Part No.
	L405	Axial inductor	LAU101J
	L407	Axial inductor	LAU121J
	L409	Axial inductor	LAU180J
	L404, L406	Axial inductor	LAU221J
	L410	Axial inductor	LAU270J
	L408	Axial inductor	LAU470J

CAPACITORS

Mark	Symbol & Description	Part No.
	C441, C442	CCCCH070D50
	C423	CCCCH101J50
	C444	CCCCH120J50
	C432	CCCCH150J50
	C424	CCCCH330J50
	C438, C443, C445	CCCCH390J50
	C431	CCCCH470J50
	C429	CCCCSL181J50
	C416	CCCCSL221J50
	C433	CCCCSL241J50
	C425	CCCCSL271J50
	C506	CCCCSL331J50
	C509	CCPUSL470J50
	C417	CEALNP100M16
	C508	CEALR10M50
	C507	CEALR47M50
	C437	CEAL010M50
	C415, C426	CEAL100M16
	C401, C406, C418, C419, C428, C430, C449, C450, C501, C503, C510, C511	CEAL470M6R3
	C453	CFTXA104J50
	C435	CKPUYB221K50
	C402 – C405, C420 – C422, C434, C436, C439, C440, C451, C452, C502, C504, C505	CKPUYY103N16
	C447	CQMA153J50

RESISTORS

Mark	Symbol & Description		Part No.
	VR403	Semi-fixed (2.2k)	VRTB6VS222
	VR401	Semi-fixed (220)	VRTB6VS221
	VR404	Semi-fixed (10k)	VRTB6VS103
	VR402	Semi-fixed (1k)	VRTB6VS102
	R401 – R404, R431, R450, R461		RN1/6PQ□□□□□F
		Other resistors	RD1/6PM□□□J

◉ 8FSB Assembly (VWV1077)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC201	HD74HC153P
	IC106	BU4551B
	IC501	TC74HCU04AP
	IC101	CXD1135Q
	IC103	CXK5816M-12L
	IC403	M5F78M06L
	IC104, IC107	NJM082D
	IC502, IC503	NJM5532DD
	IC301	PA0034A
	IC102	PDE024
	IC108	PD0036
	IC204, IC205	NJM5532SD
	IC105	TC40H004P
	IC401	M5F78M12L
	IC404	M5F79M06L
	IC402	M5F79M12L
	Q201, Q204	2SA933S
	Q1 – Q10	2SC1740S
	Q301, Q403	UN4112
	Q302, Q404	UN4212
	Q401	2SA886
	Q501 – Q504	2SD1468S
	Q402	2SC1847
	Q202, Q203	2SD1302
	D102	FC54M
	D101	KV1225YBR
	D1, D2, D103, D104, D201, D301, D302, D405 – D408	1SS254
	D401 – D404	31DF2-FE

RELAY

Mark	Symbol & Description		Part No.
	RY501	Relay	VSR-005

COILS AND FILTERS

Mark	Symbol & Description		Part No.
	L3	Axial inductor	LAU101J
	L1, L2	Axial inductor	LAU620J
	L4	Coil (3.9mH)	VTL-170
	VL101	Variable coil	VTL-275
	F301	2.3MHz B.P.F	VTF1002
	F302	2.8MHz B.P.F.	VTF1003
	F1	1.75MHz L.P.F.	VTF1021

CAPACITORS

Mark	Symbol & Description	Part No.
	C1, C3, C23, C132	CCCCH220J50
	C113, C125 – C128, C201, C204, C202, C227	CCCCH330J50
	C309, C325	CCCCH560J50
	C2, C7, C9	CCCCH820J50
	C20	CCCSL121J50
	C114	CCCSL221J50
	C324	CCCSL271J50
	C307	CCCSL301J50
	C111	CCCSL331J50
	C8, C123	CCCSL471J50
	C133	CCPUSL330J50
	C118	CEALNP2R2M35
	C108	CEAL010M50
	C109, C110	CEAL100M16
	C130, C131, C134	CEAL101M6R3
	C107	CEAL470M6R3
	C333	CEANLR47K50
	C310, C314, C327, C330	CEANP220M10
	C319, C334	CEANP100M16
	C18, C27	CEANP3R3M50
	C315	CEANP330M16
	C4	CEAS010M50
	C19, C119, C120, C124, C203, C318, C503	CEAS100M50
	C22, C129, C306, C323, C501	CEAS101M10
	C303, C305, C316, C320, C322	CEAS221M10
	C332	CEAS4R7M50
	C15	CEAS470M10
	C512, C514	CEAS470M25
	C403 – C406	CENA221M35
	C210, C212, C206, C208	CEAS101M25
	C216, C217, C223, C224	CEYA101M25
	C115, C317	CFTXA104J50
	C504 – C507	CFTXA471J50
	C117, C121	CFTXA474J50
	C103, C408, C508	CGCYX473M25
	C10	CKCYB472K50
	C5, C6, C11, C12, C16, C17, C26, C101, C502	CKCYF103Z50
	C301, C302, C304, C321	CKCYF223Z50
	C112	CKPUYF223Z25
	C102, C104, C135, C513, C515	CKPUYY103N1 €
	C105, C106	CQMA102J50
	C308, C326	CQMA152J50
	C14	CQMA183J50
	C116	CQMA273J50
	C313, C331	CQMA393J50

Mark	Symbol & Description	Part No.
	C311, C312, C328, C329	CQMA472J50
	C122	CQMA473J50
	C21	CQSH471J50
	C13	CQSH821J50
	C213, C220 (5600p)	VCE1008
	C214, C221 (1500p)	VCE1009
	C215, C222 (820p)	VCE1010
	C218, C225 (68000p)	VCE1011
	C509, C511, C518, C519 (47/50)	VCH1023
	C219, C226 (22/50NP)	VCH1038
	C401, C402 (2200/25)	VCH1043

RESISTORS

Mark	Symbol & Description	Part No.
	VR101, VR102 Semi-fixed (22k)	VRTB6VS223
	R116, R118, R119, R121, R129, R130	RN1/6PQ□□□□F
	R206 – R211, R213, R218 – R223, R225, R503, R504, R506, R516 – R520	RDR1/4PM□□□J
	R403	RD1/2PM472J
	R402	RD1/4PM242J
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	JA1 Optical transmission module	TOTX172
	Pin jack (4P)	VKB1014
	X101 Crystal resonator (16MHz)	VSS1022
	DACB Assembly (D/A converter PCB of 8FSB)	

◉ SYPS Assembly (VWR1013)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1	NJM2903S
	IC2	NJM4558S
	IC3	STA455C
	IC4	TA7291P
	Q6, Q13	UN4112
	Q10, Q17, Q19	2SA933S
	Q22	2SB1185
	Q5	2SB1375
	Q8	2SC1627
	Q9, Q14, Q16, Q18, Q20, Q21	2SC1740S
	Q1 – Q3	2SD2012
	Q7	UN4212
	D5, D6	D3SBA20
	D14, D15	HZS2C2
	D16	HZS24NB3
	D9, D12	MTZJ5.1A
	D7	HZS5.6NB2
	D17	HZS6.2NB2
	D8, D11, D24	HZS8.2NB2
	D1 – D4, D30 – D33	1SR35-100AVL
	D10, D13, D18, D23, D25 – D27	1SS254
	D19 – D22	10DF1

RELAY

Mark	Symbol & Description	Part No.
	RY1 Relay	VSR1001

FILTERS

Mark	Symbol & Description	Part No.
⚠	L1 Line filter	VTL-157
	L2 Line filter	VTL1011

CAPACITORS

Mark	Symbol & Description	Part No.
	C17, C18, C21, C24, C30 – C32, C34	CEAS100M50
	C10	CEAS101M10
	C22, C23	CEAS101M50
	C9,	CEAS102M16
	C14 (10000/16)	VCH1049
	C12, C13	CEAS222M25
	C11	CEAS470M10
	C16, C19	CEAS470M25
	C27, C28	CEAS470M50
	C40, C41	CEAS471M25
	C15	CEAS472M16
	C29, C36, C37	CFTXA103J50
	C26	CFTXA104J50
	C35	CFTXA333J50
	C33	CGCYX473M25
	C3, C4, C7, C8	CKCYF103Z50
⚠	C1, C2	RCG-009
	C50, C51	CKDYF103Z50
	C5, C6	CKPUYF103Z25

RESISTORS

Mark	Symbol & Description	Part No.
	R41, R42	RS1LMF010J
	R37 – R40 (2W)	RS2PMF331J
	R63	RD1/2PM□□□J
	R3	RD1/4VM101J
	R43 – R48	RN1/6PQ□□□□F
	R19, R20	RD1/2PMF2R2J
	Other resistors	RD1/6PM□□□J

YCSB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	Q2, Q8 – Q10, Q16, Q17	2SA933S
	Q1, Q3 – Q7, Q11 – Q15, Q18 – Q20	2SC1740S

COILS AND FILTER

Mark	Symbol & Description	Part No.
	L2 Tuning coil	ATG1006
	L3 – L5 Axial inductor	LAU100J
	L1 Axial inductor	LAU180J
	F1 Band pass filter	VTF1030

CAPACITORS

Mark	Symbol & Description	Part No.
	C10	CCCCH100D50
	C19	CCCCH151J50
	C5	CCCSL201J50
	C6	CCCSL271J50
	C7	CCCSL331J50
	C2	CCCSL681J50
	C12	CEAS220M10
	C15	CEANP221M10
	C1, C8	CEANP330M16
	C11, C13	CEAS010M50
	C21	CEAS100M50
	C22	CEAS102M6R3
	C9, C14, C20, C24, C26	CEAS470M10
	C3, C4, C16 – C18, C23, C27	CKPUYF103Z25
	C25	CEAS471M6R3

RESISTORS

Mark	Symbol & Description	Part No.
	VR1 Semi-fixed (470Ω)	VRTB6VS471
	R14, R15	RN1/6PQ1001F
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	DL2 Delay element	ATN1007
	DL1 Glass delay line	VTF1029

◉ FLKY Assembly (VWG1032)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC101	PDG035
	IC102	PST523C
	Q101 – Q107	2SC2458
	D103 – D107	1SS254

SWITCHES

Mark	Symbol & Description	Part No.
	S103 – S107, S113 – S117, S124 – S127, S133 – S137 Tact switch (RANDOM PLAY, INTRO SCAN, AUTO PGM EDM, 0-9, +10, PGM, CLEAR, SIDE A/B, MEMORY)	VSC-010

CAPACITORS

Mark	Symbol & Description	Part No.
	C103	CEJA100M35
	C101	CEJA470M6R3
	C106	CKPUYB102K50
	C102	CKPUYY103N16
	C105, C104, C107	CKPUYF223Z25

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	CN501 Connector (30p)	VKN1047
	V101 Fluorescent tube	VAW1008
	X101 Ceramic resonator	VSS1014

◉ CNKB Assembly (VWG1031)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC201	IR9393
	Q202	2SC1740S
	Q201	UN4212
	D200 – D202	1SS254
	D203	SEL1415E

SWITCHES

Mark	Symbol & Description	Part No.
	S200, S210, S211, S221, S231 Tact switch (POWER, DISPLAY, FWD/REV, FILE MODE)	VSC1001

CAPACITORS

Mark	Symbol & Description	Part No.
	C201	CEJA470M6R3
	C202 – C205	CKPUYY103N16

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

OTHER

Mark	Symbol & Description	Part No.
	CN601 Connector (30P)	VKN1071

◉ IRAB Assembly (VWG1033)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	Q300, Q301	UN4212

SWITCHES

Mark	Symbol & Description	Part No.
	S320, S330 Tact switch (STOP/OPEN, PLAY/STILL)	VSC-010

CAPACITORS

Mark	Symbol & Description	Part No.
	C301	CEJA100M16

RESISTORS

Mark	Symbol & Description	Part No.
	R300, R301	RD1/6PM221J

OTHER

Mark	Symbol & Description	Part No.
	IR sensor unit	GP1U50X

◉LEDB Assembly (VWG1034)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	D400, D401 LED indicator (YEL)	SLH-56YC35HYL

CNNB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC401	IR3C02A
	Q401	2SC1740S

CAPACITORS

Mark	Symbol & Description	Part No.
	C401 – C403	CEAS220M25
	C404, C406	CKPUYF223Z25
	C405	CEJA010M50

RESISTORS

Mark	Symbol & Description	Part No.
	VR401 Semi-fixed (47kΩ)	VRTB6VS473
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	CN12 Connector (29P)	VKN1025
	CN11 Connector (24P)	VKN1049

SFGB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	Q301	UN4212
	Q302 Photo reflector	VEX1019
	Q303	UN4112

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

FTSB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC2, IC3	BA15218N
	IC1	HA11529NT
	Q4, Q6, Q12, Q15	UN4112
	Q2, Q3, Q5, Q8, Q9	UN4212
	Q13, Q7, Q11	2SA933S
	Q1, Q10, Q14	2SC1740S
	D7	HZ5.6EB2
	D11	1SS198
	D1, D2, D5, D6, D9, D10	1SS254

COILS

Mark	Symbol & Description	Part No.
	L1, L2 Radial inductor	LRA470J

CAPACITORS

Mark	Symbol & Description	Part No.
	C1, C31	CCPUSL680J50
	C7, C30	CEJANPR47M50
	C5	CEJANP010M50
	C4, C29	CEJANP100M16
	C10	CEJANP220M10
	C28	CEJA010M50
	C21	CEJA100M16
	C24, C26	CEJA220M25
	C12	CQMA332J50
	C3, C17, C18, C20	CFTXA104J50
	C16	CFTXA184J50
	C13	CFTXA222J50
	C23	CFTXA223J50
	C9	CFTXA333J50
	C8, C14	CFTXA473J50
	C6, C15, C22	CFTXA683J50
	C19	CKPUYB102K50
	C2	CKPUYB331 K50
	C25, C27	CKPUYF223Z25
	C11	CFTXA224J50

RESISTORS

Mark	Symbol & Description	Part No.
	VR1, VR2, VR6, VR7, VR10 – VR12 Semi-fixed (4.7kΩ)	VRTB6V472
	Other resistors	RD1/6PM□□□J

OTHER

Mark	Symbol & Description	Part No.
	CN9 Connector (24P)	VNK1049

◉ FTSD Assembly (VWS1044)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC202	BA15218
	IC203	LA6500
	IC201	LA6520
	Q204 – Q206	UN4112
	Q201, Q203	2SA933S
	Q209	2SB1185
	Q202, Q210	2SC1740S
	Q208	2SD1762
	Q207	2SK184
	D201	1SS254

CAPACITORS

Mark	Symbol & Description	Part No.
	C208	CCCCH820J50
	C203	CEJANP220M10
	C205	CEJA010M50
	C209 – Q212	CEJA220M25
	C201, C206, C213, C215	CFTXA104J50
	C207, C214	CKPUYB102K50
	C202, C204	CKPUYB331K50

RESISTORS

Mark	Symbol & Description	Part No.
	R216, R224	RD1/2PMF3R3J
	Other resistors	RD1/6PM□□□J

STTB Assembly

OTHER

Mark	Symbol & Description	Part No.
	DIN socket (4P.mini)	VKN1078

DACB Assembly (DACB Assembly is included 8FSB Assembly.)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1 D/A CONVERTER	AD1860N-K

RESISTORS

Mark	Symbol & Description	Part No.
	R1 – R3	RD1/6PM□□□J
	VR1	VRTB6VS104

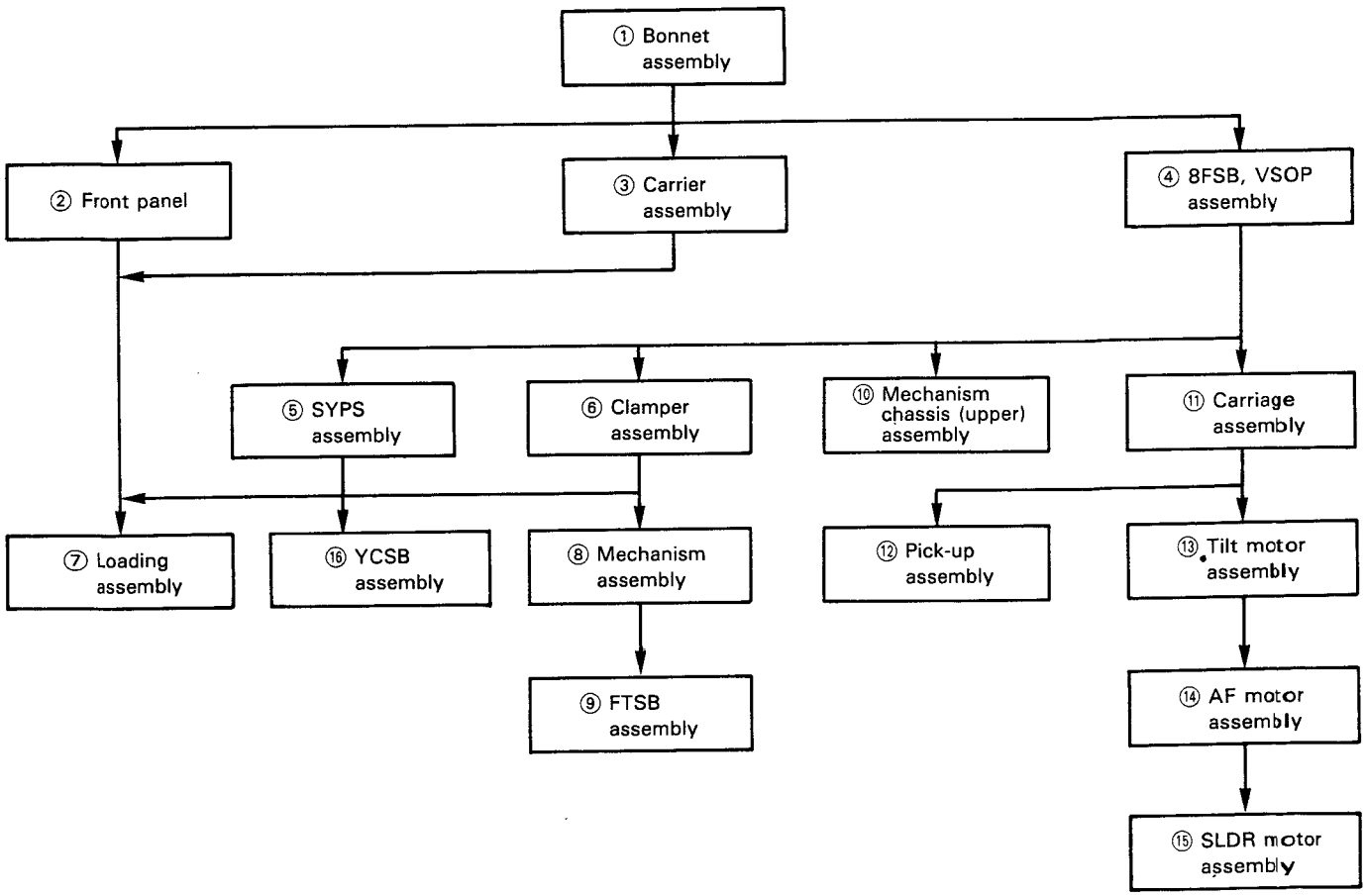
OTHERS

Mark	Symbol & Description	Part No.
	IC SOCKET (16P)	VKH1005

8. DISASSEMBLY

8.1 DISASSEMBLY FLOW CHART

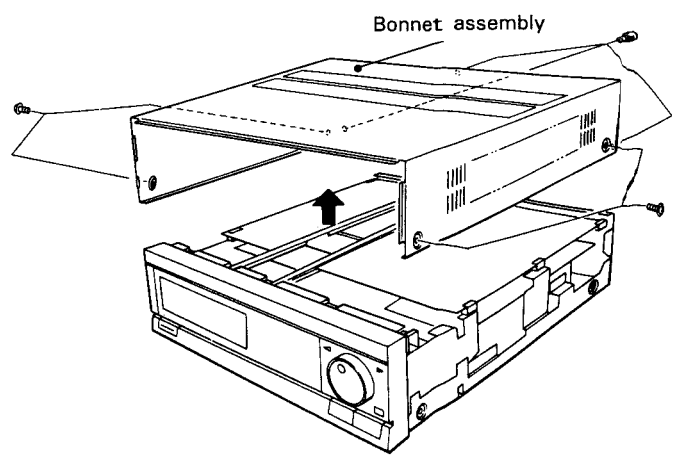
Note: The numbers in the flow chart correspond to the paragraph numbers in the explanatory text in Section 8.2.



8.2 EXPLANATION OF DISASSEMBLY PROCEDURES

1. Bonnet Assembly

Remove the two screws on each side of the unit (left and right) and then the three screws at the rear of the unit.



2. Front Panel

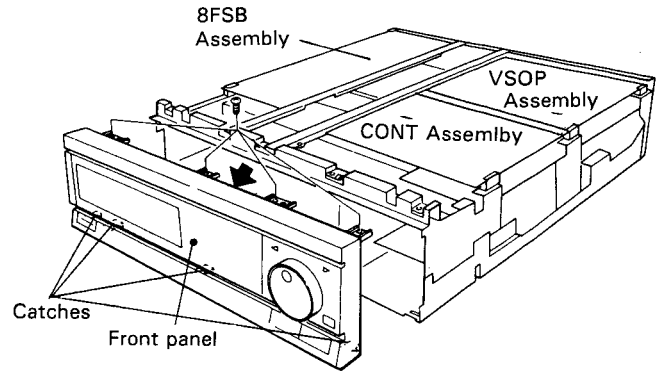
Note: The bonnet assembly should be removed first.

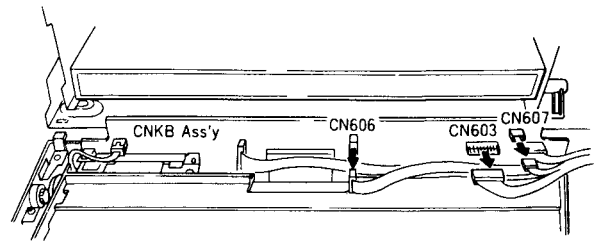
① Remove the four locking screws on the top of the front panel.

② Release the four catches on the bottom of the front panel.

③ Disconnect connectors CN603, CN606 and CN607 on the CNKB assembly.

Note: When reassembling the front panel, after connecting the CNKB connectors, engage the four catches under the front panel before tightening the screws.





3. Carrier Assembly

Note: The bonnet should be removed first.

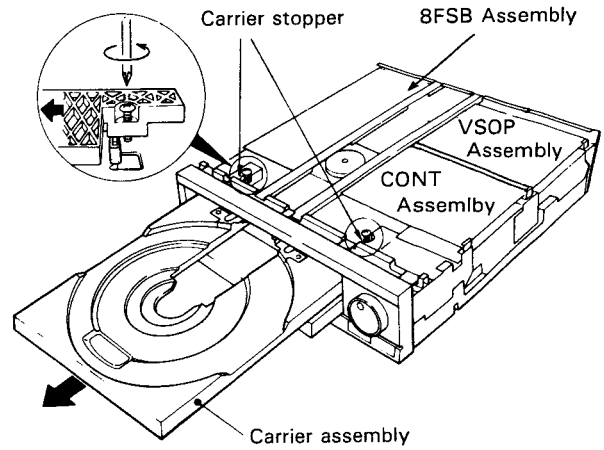
① Turn the power switch ON, and press the STOP (■)/OPEN (■/▲) key to open the carrier. (Carrier out operation)

② Disconnect the power cord.

Note: Only by turning the power switch OFF, the carrier will be closed by the backup power supply.

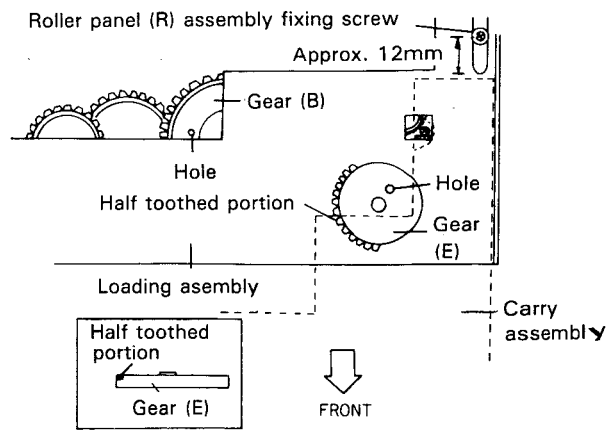
③ Loosen the two carrier locking screws without touching the screws to the notches of the loading base.

④ Pull out the carrier assembly toward you gently to remove it.



— Inserting the carry assembly —

To install the carry assembly, confirm that the positions of the hold in gears (B) and (E) as well as the roller panel (R) assembly fixing screw are as shown in the diagram. Align the meshing section of the carry assembly with the teeth of the half-toothed gear (E) and slowly insert the assembly.



Gear (E) viewed from the side

Diagram showing positions of holes in gears (B) and (E) and roler panel (R) assembly fixing screw

4. 8FSB · VSOP and CONT Assemblies

Note: The bonnet should be removed first.

— VSOP and CONT Assemblies —

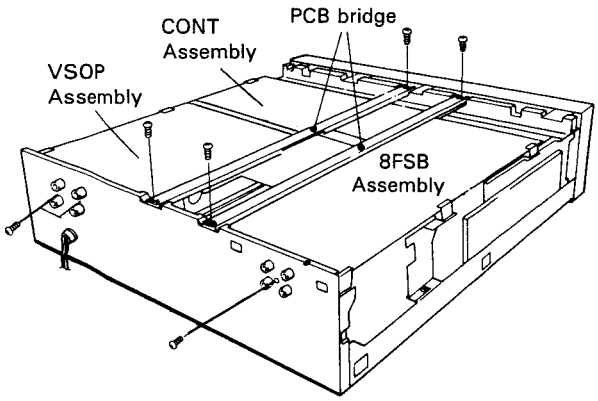
① Remove the two locking screws on the PCB bridge.

② Remove the two locking screws for VIDEO OUTPUT terminal and controller input terminal from the rear side.

— 8FSB Assembly —

① Remove the locking screws for AUDIO, output jacks.

② Remove the two locking screws on the PCB bridge.



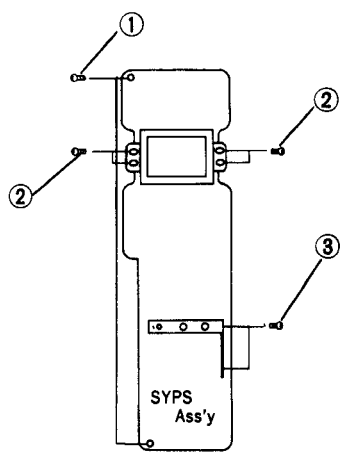
5. SYPS Assembly

Note: The VSOP assembly and the CONT assembly should be removed first.

① Remove the two screws holding the SYPS assembly.

② Remove the four screws holding the power transformer.

③ Remove the two screws holding the heat sink.

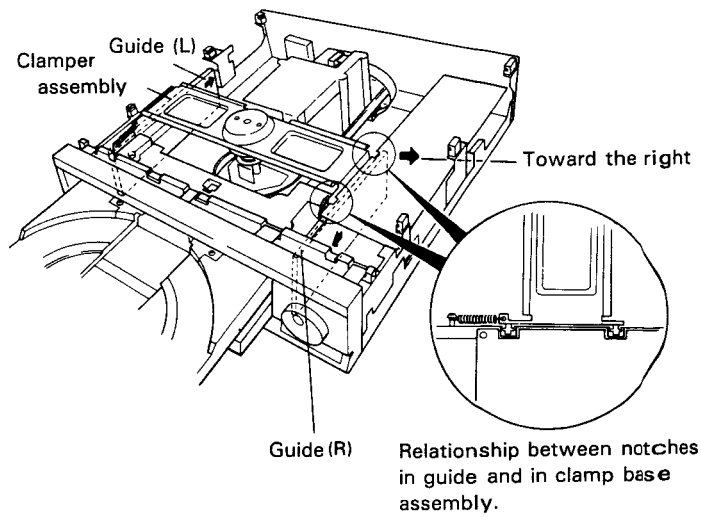


6. Clamper Assembly

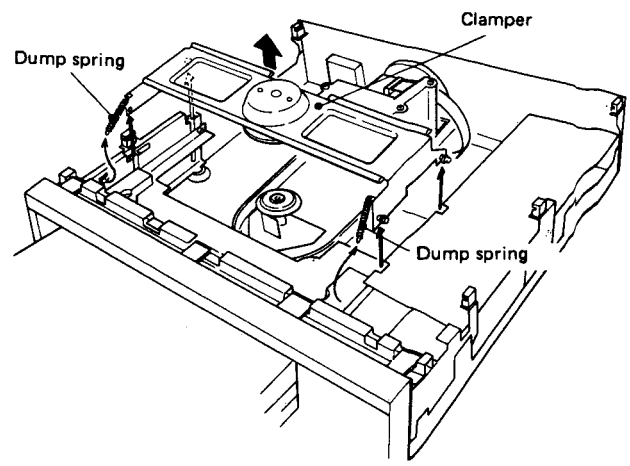
Note: The 8FSB, VSOP and CONT assemblies should be removed first.

① While pressing the catch of the guide (R) toward the right, pull the right guide toward you until the catch is released from the clamp base and inserted into the hole. (Refer to the "Note" in item 7. "Loading assembly".)

Note: Since the guide (L) and guide (R) are connected to each other by a joint plate, they move in opposite directions.
At this time, the relationship between the notches in the guide (R) and the clamp base assembly on the right should be as shown by the arrows in the diagram.



② Disengage the left and right dump springs from the clamp base and pull the clamper straight up.



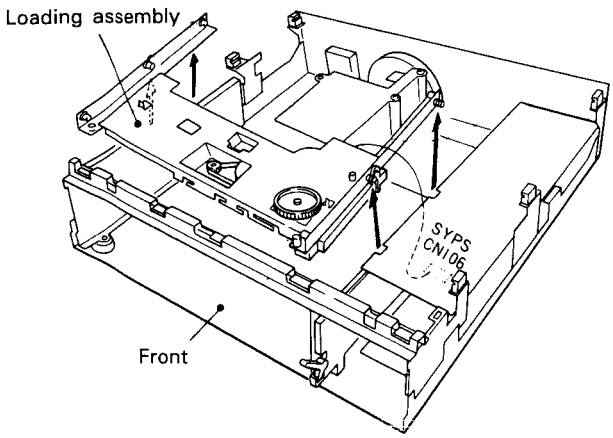
7. Loading Assembly

Note: The front panel, bonnet, carrier and clamper should be removed.

① Release the catch on the guide (R) from the clamp base hole, and set it in the middle position between the groove and the hole.

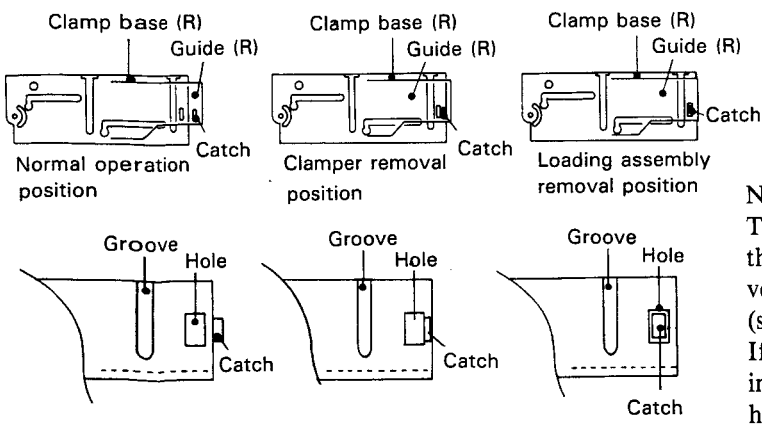
② Disconnect connector CN106 on the SYPS assembly and CN306 on the CONT assembly.

③ Lift the Loading assembly straight up.

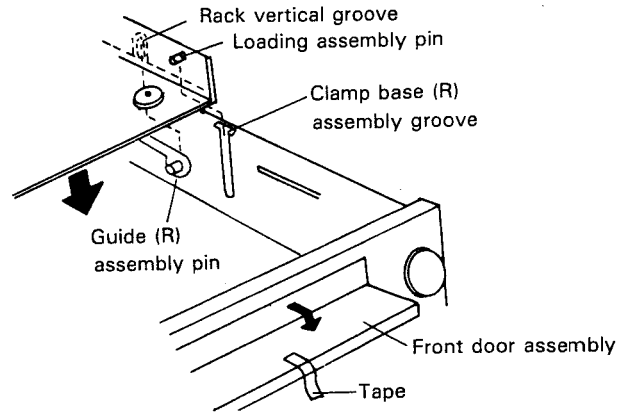


Note:
The catch of the guide (R) and the clamp base (R) should be positioned as follows in different operation modes.

- Catch is positioned at the edge in the clamp base (R)
  —Normal operation position
- Catch is in the hole in the clamp base (R)
  —When removing the clamper
- Catch is positioned in the middle between the groove and the clamp base (R)
  —When removing the loading assembly



— Installing the loading assembly —



① Open the front door assembly with your hand and tape it in place. (This is to keep the door lever in the proper position.)

② Align the vertical groove in the rack with the guide (R) pin and the loading assembly pin with the clamp base (R) assembly groove. Insert straight.

Note: The guide (R) has about 10mm of leeway in front and back.

③ Attach the clamp. After confirming that loading operates properly, remove the tape from the front door.

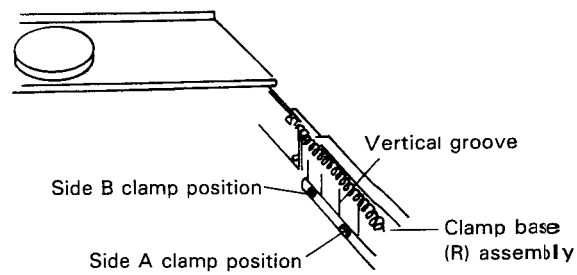


Diagram showing positions of side A and side B clamps and guide (R) pin

Note: Position of disc clamps
The positions of the disc clamps can be determined from the positions of the guide (R) assembly pin and the four vertical grooves engraved in the clamp base (R) assembly (see diagram).
If the positions of the clamps differ from those shown in the diagram, fine adjust the fixing position of the gear holder assembly (see page 10).

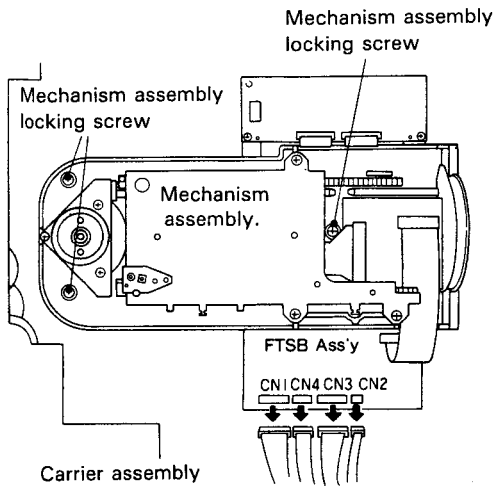
8. Mechanism Assembly

Note: The bonnet, VSOP, ADEM assembly and the clamper should be removed first.

① Move the carrier assembly to the "loading out" position.

② Disconnect connectors CN1 to CN4 on the FTSB assembly.

③ Remove the three locking screws on the mechanism assembly.

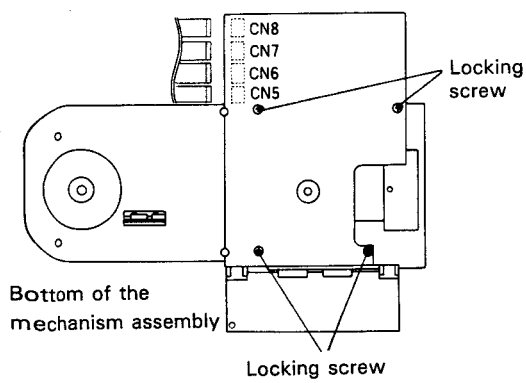


9. FTSB Assembly

Note: The mechanism assembly should be removed first.

① Remove connectors CN5 through CN8 on the FTSB assembly.

② Remove the four locking screws on the bottom of the mechanism assembly.

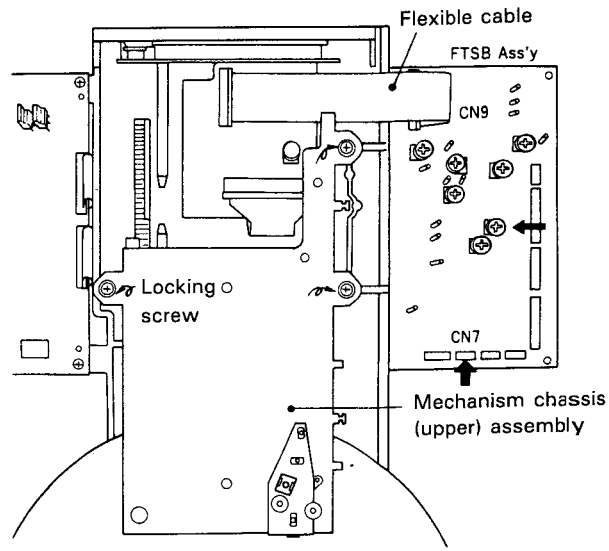


10. Upper Mechanism Chassis Assembly

Note: The bonnet, VSOP and ADEM assemblies should be removed first.

① Remove connector CN7 on the FTSB assembly.

② Remove the three locking screws.



11. Carriage Assembly

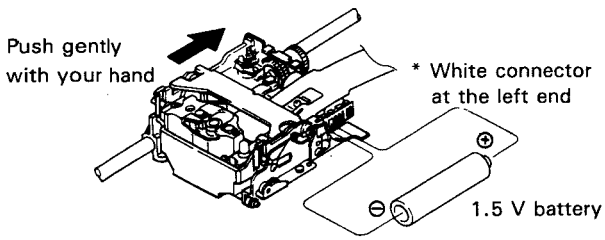
Note: The bonnet, 8FSB, CONT and VSOP assemblies should be removed first.

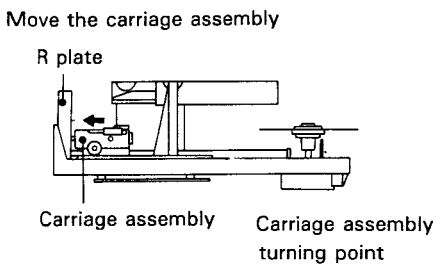
Note: In this section, the R plate, G plate and the internal gear assembly are together called the "turn plate".

① Move the carriage assembly to the position of the turn plate shaft.

— How to move the carriage assembly —

Move the carriage assembly by pushing the end of the slider shaft gently with your hand, or by connecting a 1.5 V battery to the slider motor connector.





② Disengage the flexible cable connecting the FTSB and CNNB assemblies from FTSB assembly CN9.

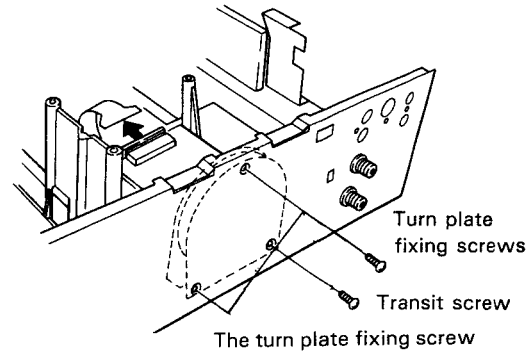
③ Disengage the flexible cable connecting the pickup and CNNB assemblies from the CNNB assembly.

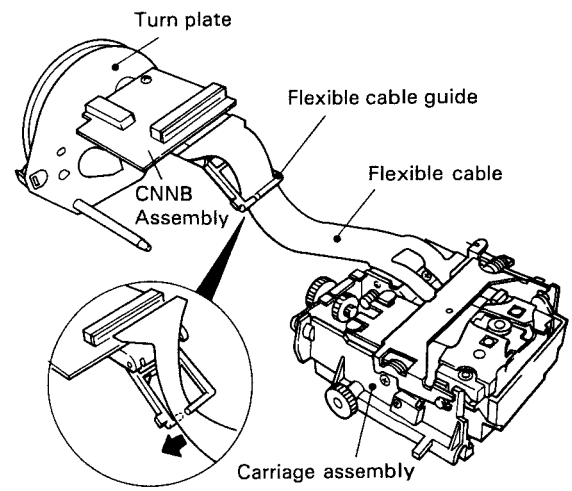
④ Insert a screwdriver into the hole in the rear panel and remove the turn plate fixing screws (3 screws).

⑤ Remove the carriage assembly together with the turn plate.

⑥ Disengage the carriage assembly from the turn plate.

⑦ Disengage the flexible cable from the flexible cable guide on the back of the CNNB assembly. Take care not to expose the unit to static electricity.





12. Pick-up Assembly

Note: The carriage assembly should be removed first.

① Check that a AF plate assembly is in the middle or bottom position of the shaft of the AF gear assembly. If not, connect the battery to the AF motor connectors to rotate the AF gear assembly shaft so that the AF plate assembly comes to the middle or bottom of the shaft.

② Remove the height springs on both sides.

③ Remove a AF stopper locking screw.

④ Remove the E-ring holding the pick-up holder assembly.

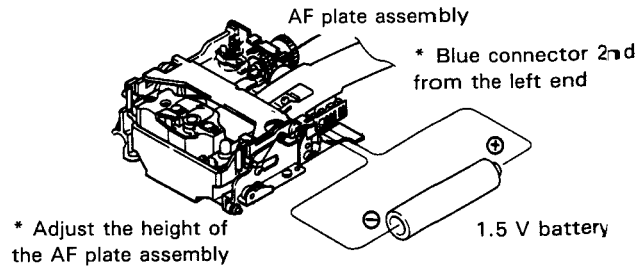
⑤ Remove the E-ring from the AF plate assembly.

⑥ While slightly lifting the AF arm on the AF gear assembly side, slide the AF arm to remove it.

⑦ Remove the two pick-up connector locking screws.

⑧ Remove all four connectors from the connector PC board on the flexible cable.

⑨ Remove a pick-up locking screw.



13. Tilt Motor

Note: The carriage assembly should be removed first.

① Remove the tilt motor connector.

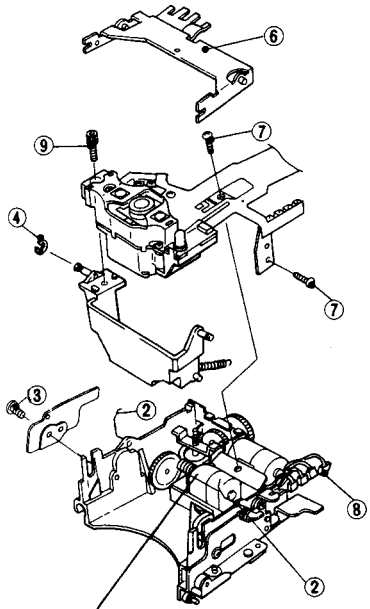
② Remove the screw holding the tilt motor assembly-S and the carriage assembly from the bottom of the carriage assembly.

14. AF Motor

Note: The pick-up assembly and the tilt motor assembly should be removed first.

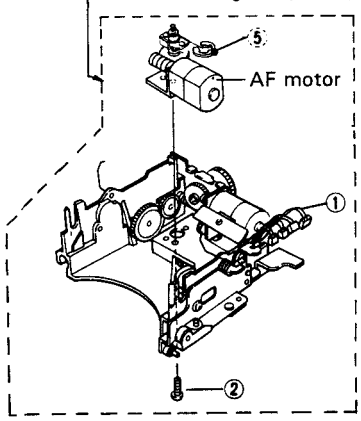
① Remove the AF motor connector.

② Remove the screw holding the AF motor assembly and the carriage assembly.

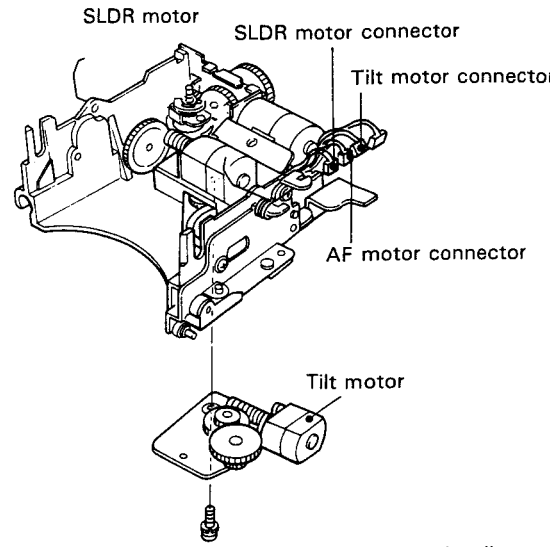


Note: The numbers in the diagram correspond to the numbers in the disassembly procedure.

12. Removing the pick-up assembly



14. Removing the AF motor



13. Removing the tilt motor
15. Removing the SLDR motor

15. SLDR Motor

Note: The pick-up assembly, AF motor assembly and the tilt motor assembly should be removed first.

① Remove the SLDR motor connector.

② Remove the wire harness wrapped around the slider base.

③ Remove the two screws fixing the SLDR motor.

9. ADJUSTMENT

9.1 JIGS AND INSTRUMENTS REQUIRED FOR ADJUSTMENT

- Small ⊖ screwdriver (about 7 cm long)
- Small Phillips head screwdriver (at least 15 cm long)
- Hexagonal wrenches (2.0 mm and 2.5 mm)
- L-shaped eccentric screwdriver (GGV-129)
- 1.5 V battery with lead wires
- Low-pass filter (100k ohms + 1 μF)
- Dual-trace oscilloscope (with delay)
- AF generator
- Frequency counter
- LD test disc (GGV1002 or 8-inch F2)
- LDD disc (buy locally)
- CD test disc (YEDS-7)
- Shorting clip
- Digital voltmeter

9.2 PREPARATIONS FOR ADJUSTMENT AND PRECAUTIONS

1.) When replacing the pick-up assembly, adjust in the following way:

— Carriage assembly in forward condition —

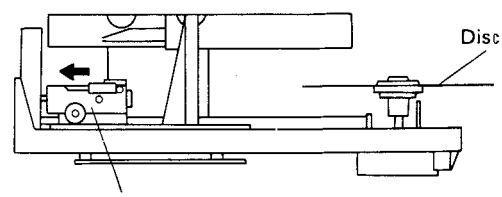
1. Coarse grating adjustment, tracking balance adjustment
2. Crosstalk adjustment
   1) Pick-up tangential direction angle adjustment and tilt servo balance adjustment
   2) LD focus error balance adjustment
3. Spindle motor centering check
4. Spindle motor centering adjustment
5. Fine grating adjustment
6. RF gain adjustment
7. Focus sum level adjustment
8. FOCS servo loop gain adjustment
9. TRKG servo loop gain adjustment

— Carriage assembly in reverse condition —

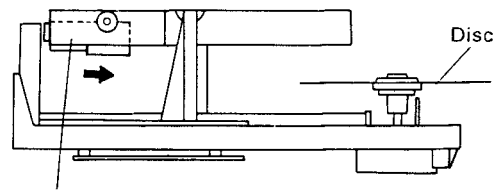
10. Centering adjustment for side B play
11. Pick-up tangential direction angle adjustment for side B play
12. Fine centering adjustment for side B play

Note: The forward status of carriage assembly is when the carriage assembly is in the position to play side A of the disc. The reverse status is when it is in the position to play side B of the disc.

Carriage assembly forward status

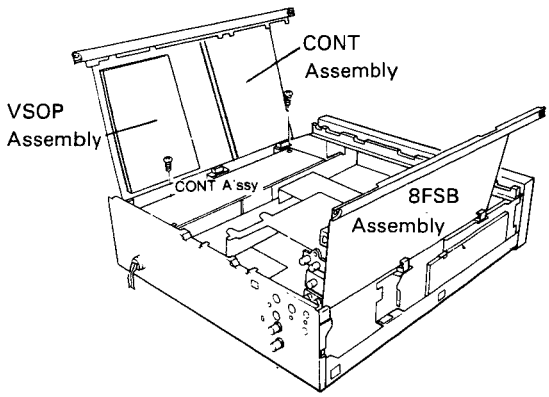


Carriage assembly reverse status

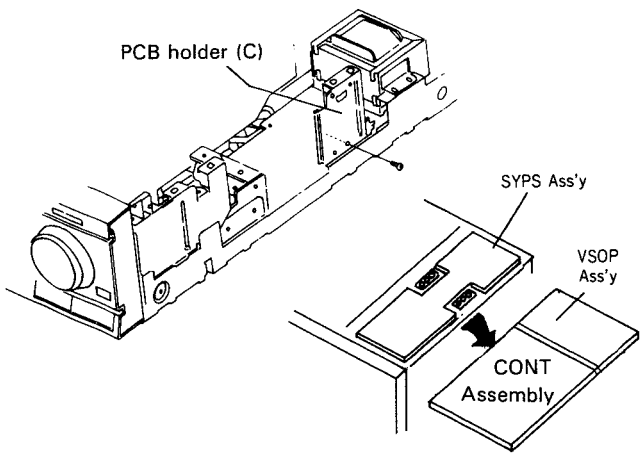


2.) Condition of the unit when adjusting

Mechanical adjustments are to be done with the bonnet and the carrier assembly removed, with the VSOP, CONT and 8FSB assemblies open.
Electrical adjustments are to be done with the corresponding circuit boards open.
When adjusting the SYPS assembly (power supply board), open the circuit boards by swining them up as shown in the figure (below), to measure voltages, etc.



- When turning the SYPS assembly upside down, with the carrier moved out, remove connectors CN1 and CN4 from the FTSB assembly, and set the SYPS assembly to its correct position, then re-connect the connectors. If the PCB holder (C) is removed, the CONT assembly will be stabilized. (For PCB holder (C), refer to page 8.)

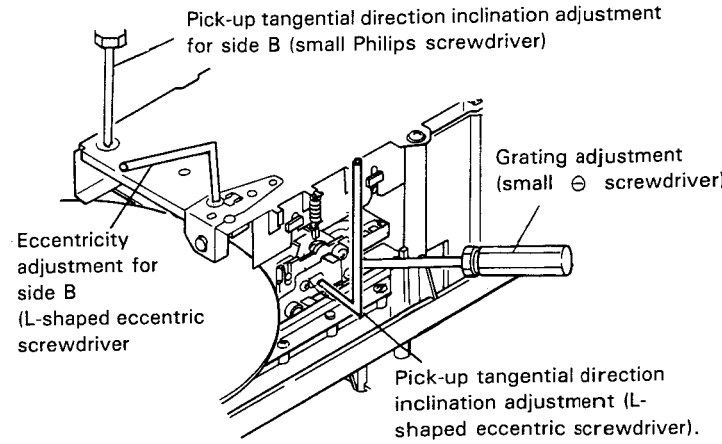


3.) Precautions when reversing the carriage assembly

- The carriage assembly cannot be reversed unless it is advanced by playing a disc.
- If the power switch is turned OFF with the carriage assembly reversed, the backup power supply functions to resume the forward status of the carriage assembly.

4.) Where to insert the screwdriver when adjusting the pick-up assembly

— Carriage assembly in forward condition —



5.) Test disc

The LD test disc used for mechanical adjustment and FTSB assembly adjustment may either be the GGV1002 or 8-inch F2. The frame numbers given in the text are for the GGV1002 while those enclosed in parentheses are for the F2.
The LD test disc used for electrical adjustments can be either N series or F series. The frame numbers given in the text are for the N series while those enclosed in parentheses are for the F series.

6.) Abbreviation in the text indicate the following

FOCS = Focus
TRKG = Tracking
SPDL = Spindle
SLDR = Slider
TAN = Tangential

7.) Replacement of IC10 program PROM-S (VYW1313) on the CONT assembly

In the test mode, pressing the key combination [CX] + [8] on the remote control clears the external RAM. (Refer to "Test Mode" on page 84.)

8.) Numbers given in connection diagram correspond to those in the text covering the adjustment procedure.

9.) Test Mode

This unit has a Test Mode function with which the tracking servo can be opened and closed easily while various switch setting conditions can be monitored on the TV screen.

— Test Mode —

1. Activating the Test Mode
   Test Mode can be activated in the following manner:
   1) Open the door and turn the power switch ON. (Except when the disc is in the player, the door is opened by the carrier during opening, ejecting and loading operations.)
2. Releasing the Test Mode
   There are two ways to release the Test Mode:
   1. Press the [CX] + [9] keys on the remote control unit.
   2. Turn the power switch OFF.

Notes:

① In the Test Mode, lifting the clamper or ejecting the disc is impossible as they would be dangerous. However, if there is no disc on the tray, ejecting is possible.
② Be careful of the clamper as it will rise up when changing the play mode from side B to side A.
③ In the Test Mode, the Emergency port (expansion I/O No. 21) cannot be observed.
④ In the Test Mode, the initial search function can be released with the Clear key.
⑤ When an LD disc is placed on the tray in the Test Mode, the power will be switched off about 20 seconds after the POWER button is pressed to OFF.

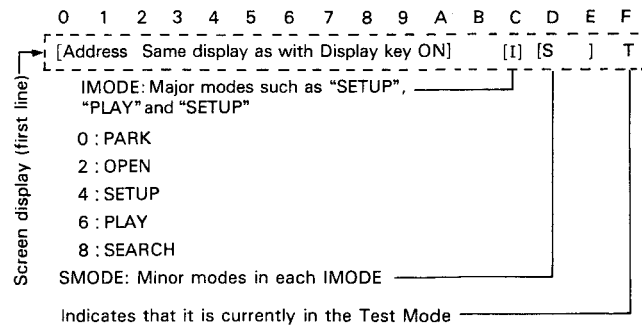
3. Functions
   After the Test Mode is activated, the following functions will be engaged by pressing a combination of the [CX] key and a numeric key.
   [CX] + [0] : The FL display and LEDs light up, and the ROM version will be displayed on the screen of the monitor TV.
   [CX] + [1] : Error rate measurement. Either an LD or CD will be measured for 15 seconds, then the result will be displayed on the screen of the monitor TV.
   [CX] + [2] : Alternately opens and closes the tracking servo. (Toggle switch)
   [CX] + [3] : Alternates the CX (noise reduction) circuit between CX default and default. (Toggle switch)
   [CX] + [4] : Turns the tilt OFF forcibly.
   [CX] + [5] : Sets the tilt to the normal position.
   [CX] + [6] :
   [CX] + [7] :
   [CX] + [8] : Clears the external RAM. (The RAM is not cleared when these keys are pressed, but the contents of the RAM will be cleared the next time the power is turned ON.)
   [CX] + [9] : Releases the Test Mode

   Note: Only the following two functions are directly connected to this Service Manual. The other items are listed for reference.
   [CX] + [2] : Tracking servo ON/OFF
   [CX] + [8] : External RAM clear

4. Display

In the Test Mode, the statuses of switches and other data are displayed on the screen of the monitor TV.

[1st line]

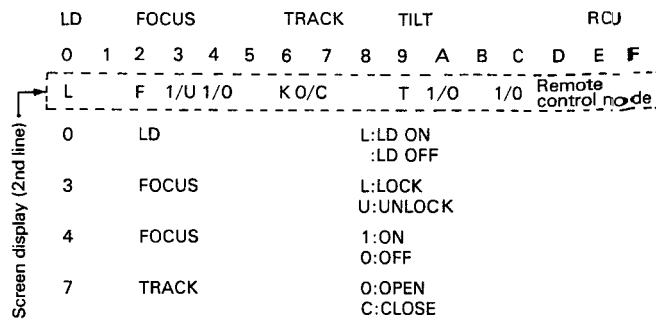


[2nd line]

Five indications are displayed on the second line, and the contents displayed will be changed according to the priority of each item.

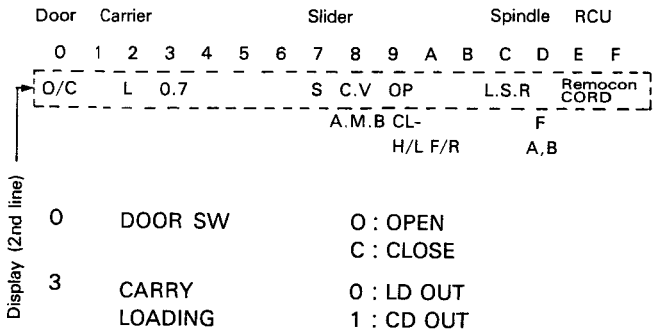
a. Searching object input mode (same as the normal search input mode)
b. Error rate indication (ERR _____ _____)
c. ROM version indication (VYW-_____ 88 _____)
d. Pick-up status indication (LD, FOCS, TRKG, TILT)
e. Mechanism status indication (Door SW, Carry, 8 steps of Loading position)

* When the Test Mode is activated from the remote control, the "d" indication will appear.
* When the Test Mode is activated while opening the door with the Power switch ON, the "c" indication will appear, in the same way when activated by pressing the [CX] + [0] keys.
* Indications of "d" and "e" can be changed by pressing the Display key.

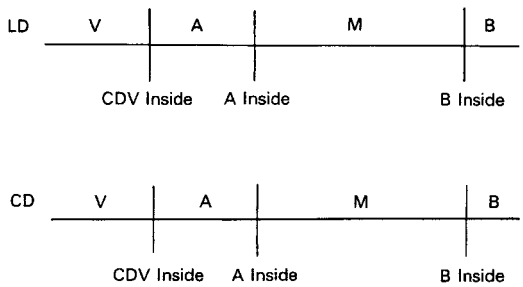


A	TILT	1 : ON 0 : OFF
B	HEIGHT MOTOR	U : UP D : DOWN S : STOP
C	HEIGHT SW	1 : ON 0 : OFF

E, F, Remote Control, Main Unit, Key Code



0	DOOR SW	O : OPEN C : CLOSE
3	CARRY LOADING POSITION	0 : LD OUT 1 : CD OUT 2 : 3 : PARK 4 : TURN 5 : 6 : A CLAMP 7 : B CLAMP
8	SLIDER POSITION	



9,A	SLIDER SPEED DIRECTION	OP : OPEN CL : CLOSE H : HIGH SCAN L : LOW SCAN F : FWD R : REW
C	SPINDLE (status)	L : LOCK R R : RUN S : STOP
D	SPINDLE (control)	F : FREE RUN A : ACCEL B : BRAKE

*SPINDLE display is for LD only.

Reference:

Code	Function	Code	Function
00	0	4B	(Audio 1/L)
01	1	4C	Program
02	2	4D	Side A
03	3	4E	Side B
04	4	4F	Not used
05	5	50	Step REV (reverse)
06	6	51	Not used
07	7	52	Chapter Skip FWD (forward)
08	8		
09	9	53	Chapter Skip REV (reverse)
0A	(A)		
0B	(B)	54	Step FWD (forward)
0C	Digital/Analog	55	Multi-Speed REV (reverse)
0D	Custom File		
0E	CX	56	Not used
0F	(TV/LVP)	57	Not used
10	Scan FWD (forward)	58	Multi-Speed FWD (forward)
11	Scan REV (reverse)		
12	Not used	59	Not used
13	Chapter/Frame	5A	Not used
14	Not used	5B	Still & Sound
15	(Side toggle)	5C	Not used
16	Stop/Open	5D	One-shot Memory
17	Play	5E	(LED Test)
18	Pause	5F	(ESC)
19	Not used		
1A	(Power ON)		
1B	(Power OFF)		
1C	Power toggle		
1D	Not used		
1E	Audio Monitor		
1F	+10		
40	(Chapter)		
41	(Frame)		
42	Search/Memory		
43	Display		
44	Repeat B		
45	Clear		
46	Speed DOWN		
47	Speed UP		
48	Repeat A		
49	(Audio 2R/R)		
4A	(Audio Stereo)		

Codes in brackets ( ) are not generated with the normal remote control keys or keys on the front panel, but they will be accepted. "Not used" codes will not be accepted.

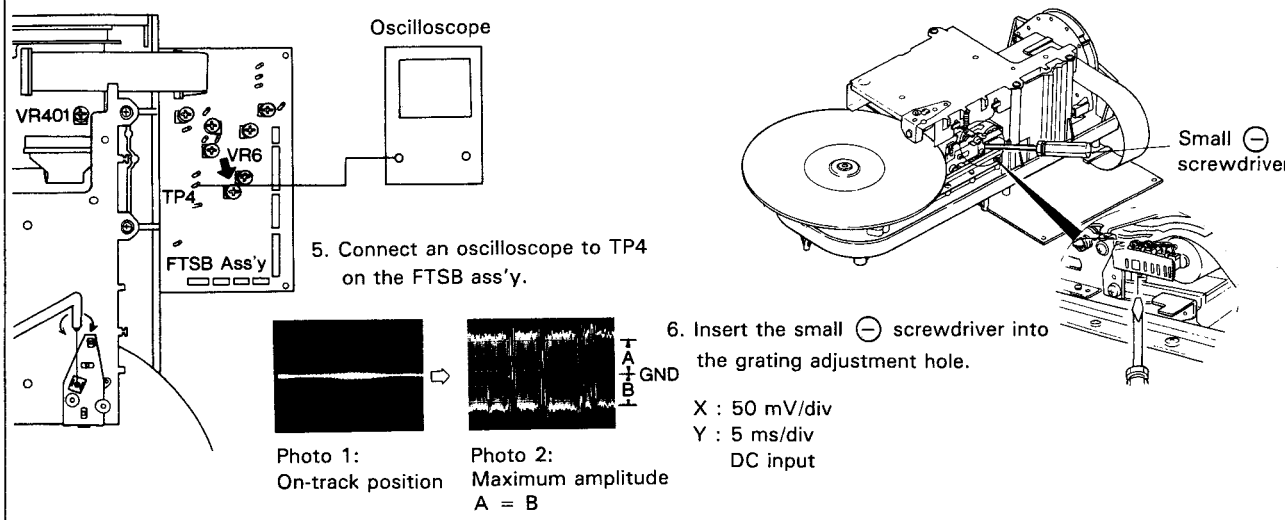
9.3 MECHANISM ADJUSTMENT

1. Coarse Grating and Tracking (TRKG) Balance Adjustment

- Purpose: To adjust the laser beam which is divided into three by the grating to the optimum position on the track. Set the TRKG servo offset voltage to 0 V.
- When not properly adjusted: Disc playback will be impossible. During play, tracks may be skipped.

• Measuring instruments and jigs:	• Small ⊖ screwdriver (flat blade) • Oscilloscope
• Measuring point:	• FTSB assembly TP4 (TRKG error)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #6,500, (#300) • Still mode • Test Mode (TRKG servo: Open) • The carriage assembly should be in the forward position.
• Positions to be adjusted	• Grating • FTSB assembly VR6 (TRKG balance)

Connection diagram



Adjustment Procedure

<Coarse Grating Adjustment>

1. Play the LD test disc.
2. Press the DISPLAY key to display the frame # (No.) on the TV screen.
3. Move the pick-up to frame #6,500 (#300) by scanning or searching.
4. Open the TRKG servo. (See p. 84.)
5. Connect an oscilloscope to TP4 of the FTSB assembly and observe the waveform.
6. Insert the small ⊖ screwdriver into the grating adjustment hole. Turning the grating will allow you to vary the amplitude of the TRKG error waveform. Find the position where the waveform amplitude becomes minimum with a smooth envelope. (Photo 1)
   (This indicates that the 3-way split laser beams are directed onto the track. This is called the "on-track" position.)
7. Slowly turn the grating counterclockwise from the on-track position until the waveform amplitude becomes maximum. (Photo 2)
8. Close the TRKG servo and check that a normal picture is displayed on the TV screen.

<TRKG Balance Adjustment>

1. Align the oscilloscope GND so that it comes to the center of the oscilloscope screen.
2. Adjust VR6 on the FTSB assembly so that the positive and negative amplitude of the TRKG error waveform become equal. (Photo 2)

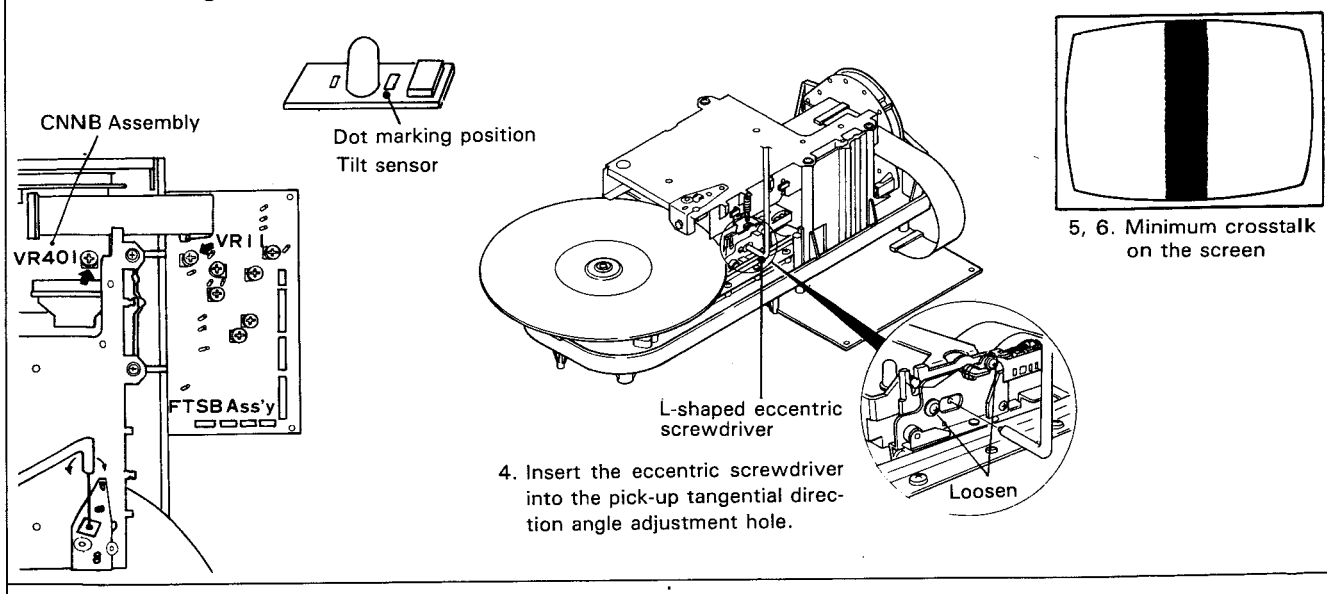
2. Crosstalk Adjustment

(1) Pick-up Tangential Direction Angle Adjustment and Tilt Servo Balance Adjustment (Pick-up TRKG direction angle adjustment)

- Purpose: To adjust the pick-up tangential direction angle so as to minimize crosstalk.
- If not properly adjusted: Noticeable crosstalk will appear.

• Measuring instruments and jigs:	• TV monitor • L-shaped eccentric screwdriver (GGV-129) • Oscilloscope
• Measuring point:	• Crosstalk on the screen
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #115 (#104) • Still mode • Test Mode (TRKG servo: Open/Close) • Carriage assembly must be in the forward position.
• Positions to be adjusted	• Pick-up tangential direction angle adjustment screw • FTSB assembly VR11 (TILT gain), CNNB assembly VR401 (TILT balance).

Connection diagram



Adjustment Procedure

1. Check the color of the dot marked on the top of the tilt sensor, at the side of the post.
   Some players have red and blue dots. According to the color of the dot, adjust the FTSB assembly VR11 as follows:
   Red dot : Turn VR11 fully clockwise.
   Blue dot: Turn VR11 fully counterclockwise.
   No dot : Set VR11 to the center position.

— Pick-up Tangential Direction Angle Adjustment —

2. Loosen the two locking screws shown in the figure.
3. Play the 8-inch LD test disc, and search frame #115 (#104).
4. Insert the eccentric screwdriver into the pick-up tangential direction angle adjustment hole.
5. While watching the TV monitor screen, adjust the pick-up tangential direction angle adjustment screw so that the crosstalk on the TV screen becomes minimum.

— Tilt Servo Balance Adjustment —
(Pick-up TRKG Direction Angle Adjustment)

6. In the condition in 5, adjust VR401 on the CNNB assembly so that the crosstalk on the TV screen becomes minimum or the left and right halves become equal. (Turn VR401 to alter the tilt of the pickup assembly TRKG direction.)
7. If there is still noticeable crosstalk on the TV screen, repeat adjustment steps 5 and 6.
8. After adjustment is complete, tighten the two locking screws.

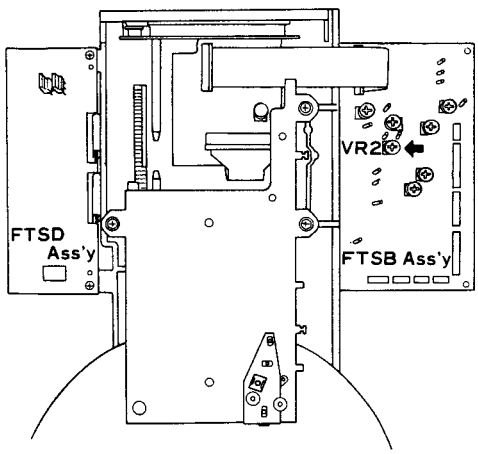
Note: When the pick-up tangential angle is changed in the side A play mode, be sure to perform "3. Spindle Motor Centering Check", "10. Centering Adjustment for Side B" and "11. Pick-up Tangential Direction Angle Adjustment for Side B".

(2) LD FOCS Error Balance Adjustment

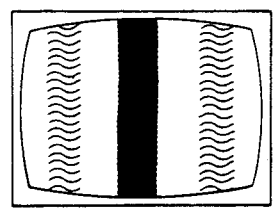
- Purpose: To ensure that the FOCS servo maintains the objective lens at the optimum distance from the disc surface.
- When not properly adjusted: Crosstalk will be generated.

• Measuring instruments and jigs: • Measuring point: • Test disc and player mode • Position to be adjusted	• TV monitor • Video signal output terminal • 8-inch LD test disc GGV1002 ... #115 (#104) • Still mode • Test Mode (TRKG servo: Open) • The carriage assembly should be in the forward position. • FTSB assembly VR2

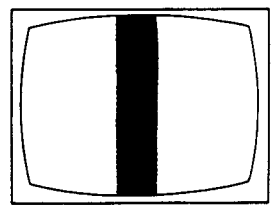
Connection diagram



2. Adjust VR2 on the FTSB assembly for minimum crosstalk.



Crosstalk generated on the screen



2. Adjust so that the crosstalk on the screen is minimum.

Adjustment Procedure

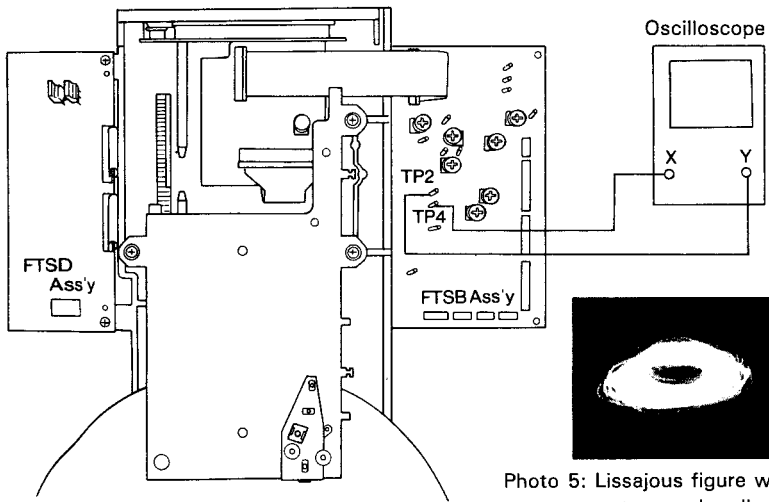
1. Play the LD test disc and search frame #115 (#104).
2. Adjust VR2 on the FTSB assembly so that the crosstalk on the left and right sides on the TV screen is minimized.
   If adjustment of VR2 fails to reduce crosstalk to an allowable level, perform "Pick-up Tangential Direction Angle Adjustment" and "Tilt Servo Balance Adjustment".

3. Spindle Motor Centering Check

- Purpose: To check that the center of the spindle motor is on the orbit of the laser beam.

• Measuring instruments and jigs:	• Oscilloscope
• Measuring point:	• FTSB assembly TP4 (TRKG error), TP2 (TRKG sum)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #100 and #22,000, (#100 and #22,000 with a commercially available "karaoke" LD disc) • Play mode • CD test disc (YEDS-7) • Test Mode (TRKG servo: Open) • The carriage assembly should be in the forward position.
• Position to be adjusted	• Check the Lissajous figure

Connection diagram



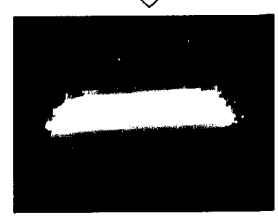
3. Connect TP4 and TP2 on the FTSB ass'y to the X, Y inputs of oscilloscope.

Photo 5: Lissajous figure when not properly adjusted

Lissajous figure of the inner track of the disc (CD)

Photo 3
Y
X: 20 mV/div, AC input
Y: 20 mV/div (1:1), AC input, X-Y mode

Check that Y = Y'



Lissajous figure of the outer track of the disc (CD)

Y'
Photo 4

5. The Y axis of the Lissajous figure should be the same for the inner and the outer tracks.

Note: LD test disc F2 is not suitable for this adjustment because the recorded portion with a track pitch of 1.52 μm is present only around inner tracks #1 to #500.

Checking Procedure

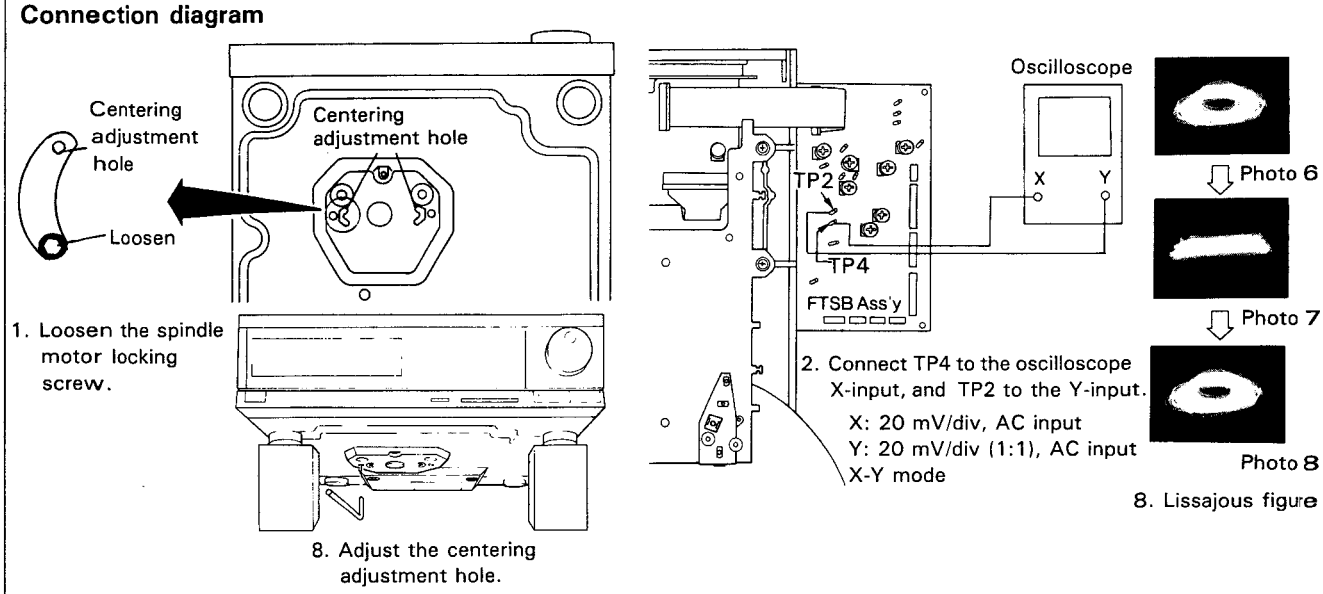
1. Play the 8-inch LD test disc.
2. Move the pick-up to frame #22,000 by scanning or searching, then open the TRKG servo.
3. Connect TP4 on the FTSB assembly to the X-input (CH-1) of the oscilloscope and TP2 to the Y-input (CH-2).
   Set the oscilloscope to the X-Y mode and observe the Lissajous figures of the TRKG error signal and the TRKG sum signal.
4. Write down the Y-axis amplitudes of the Lissajous figures. (Photo 3)
5. Close the TRKG servo and search frame #100, then open the TRKG servo again to observe the Lissajous figure.
   At this time, check that the Y-axis amplitude of the Lissajous figure is the same as that noted in step 4. (Photo 4)
6. Remove the 8-inch LD test disc from the player, then load the CD test disc and repeat the checking procedures steps 1 to 5. However, it is not necessary to specify the inner or outer track positions of the disc. If the Y-axis amplitude of the Lissajous figure is different for the inner and outer tracks, perform "4. Spindle Motor Centering Adjustment".

4. Spindle Motor Centering Adjustment

- Purpose: To adjust so that the center of the spindle motor is on the orbit of the laser beam.
- When not properly adjusted: Track skips, or searching takes too long.

• Measuring instruments and jigs:	• L-shaped eccentric screwdriver (GGV-129) • 2.5 mm Hexagonal wrench • Oscilloscope
• Measuring point:	• FTSB assembly TP4 (TRKG error), TP2 (TRKG sum)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #100 and #22,000, (or a commercially available "karaoke" LD disc) • Play mode • CD test disc (YEDS-7) • Test Mode (TRKG servo: Open/Close) • The carriage assembly should be in the forward position.
• Adjustment position	• Spindle motor centering adjustment hole

Connection diagram



Adjustment Procedure

Note: For the same reasons given in the "Note" in section 9.3.3, the LD test disc F2 is not suitable for this adjustment.

Note: There are two centering adjustment holes on the player. Either can be used.

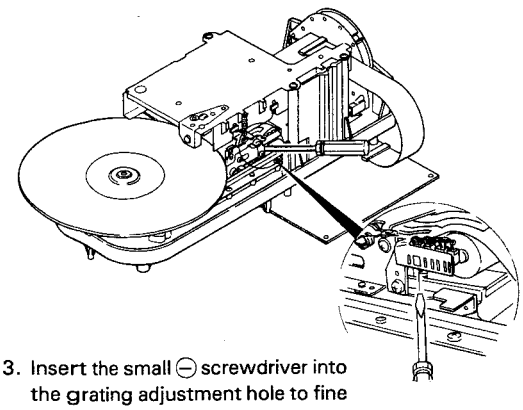
1. Loosen the two spindle motor locking screws using the hexagonal wrench.
2. Connect TP4 of the FTSB assembly to the X-input (CH-1) of the oscilloscope and TP2 to the Y-input (CH-2).
3. Play the 8-inch LD test disc and search frame #22,000.
4. Open the TRKG servo and observe the Lissajous figures of the TP4 (TRKG error signal) and the TP2 (TRKG sum signal).
5. Fine-adjust the grating so that the Y-axis amplitude of the Lissajous figure is minimized. (Photo 7)
6. Close the TRKG servo and search frame #100.
7. Open the TRKG servo again and observe the Lissajous figure and write the values down. (Photo 6)
8. Insert the L-shaped eccentric screwdriver into the adjusting hole from the left bottom of the player, and turn slowly so that the Y-axis amplitude of the Lissajous figure is reduced.
   After the Y-axis amplitude of the Lissajous figure is minimized, turn the adjusting screw further until the amplitude becomes the same shape as that observed in procedure 7. (Photos 6 - 8)
9. Close the TRKG servo, and move the pick-up assembly to the outer track of the disc (#22,000), then perform the adjustments in steps 4 to 6 again.
10. Re-open the TRKG servo and observe the Lissajous figure to check that the Y-axis amplitude is minimum. (Photo 7)
    If the Y-axis amplitude of the Lissajous figure is larger than specified, repeat the adjustment procedures from steps 5 to 7.
11. After adjustment is complete, perform the adjustment in "3. Spindle Motor Centering Check" item6.

5. Fine Grating Adjustment

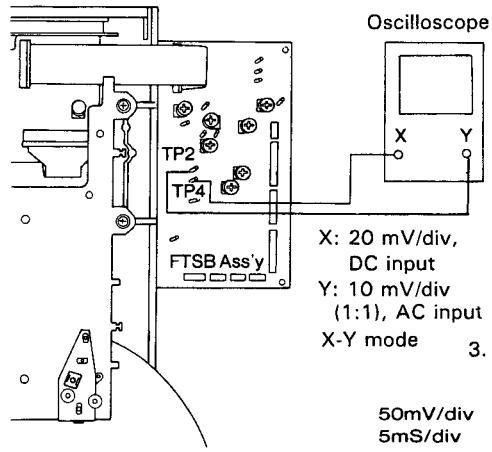
- Purpose: To fine adjust the grating so that the two tracking beams for the TRKG servo are projected in the optimum positions on the tracks being played.
  Set the TRKG servo loop offset voltage to 0 V.
- When not properly adjusted: During play, tracks may be skipped.

• Measuring instruments and jigs:	• Oscilloscope • Small ⊖ screwdriver (flat blade)
• Measuring point:	• FTSB assembly TP4 (TRKG error), TP2 (TRKG sum)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #6,500, (#300) • Still mode • The carriage assembly should be in the forward position. • Test Mode (TRKG servo: Open)
• Position to be adjusted	• Grating

Connection diagram

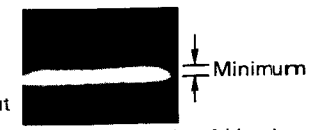


3. Insert the small ⊖ screwdriver into the grating adjustment hole to fine adjust it.



2. Connect FTSB ass'y TP4 and TP2 to the oscilloscope's X-input and Y-input.

Photo 9: Fine grating adjustment



3. Y-axis amplitude of Lissajous figure becomes minimum

50mV/div
5mS/div

Photo 10: TRKG balance adjustment

Adjustment Procedure

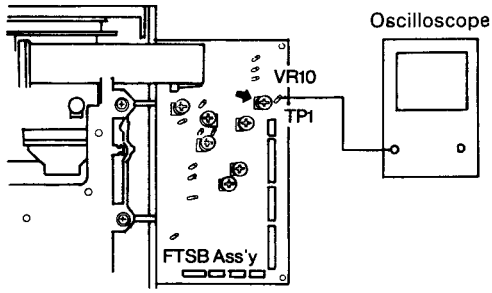
1. Play the LD test disc and search frame #6,500 (#300), then open the TRKG servo.
2. Connect the oscilloscope's X-input (CH-1) to FTSB assembly TP4, and the Y-input (CH-2) to TP2.
   Set the oscilloscope to the X-Y mode and observe the Lissajous figures of the TRKG error signal and the TRKG sum signal.
3. Insert the small ⊖ screwdriver into the grating adjustment hole, and fine-adjust the grating so that the Y-axis amplitude of the Lissajous figures is minimized. (Photo 9)
   If the grating is turned too much and the optimum position can no longer be found, repeat the "Coarse Grating Adjustment".
4. Select the oscilloscope's X-input (CH-1) and check that the positive and negative amplitudes of the TRKG error signal are equal. (Photo 10)
   If they are not, repeat the "Tracking Balance Adjustment".
5. Close the TRKG servo and check that the picture (image) on the TV screen is normal.

6. RF Gain Adjustment

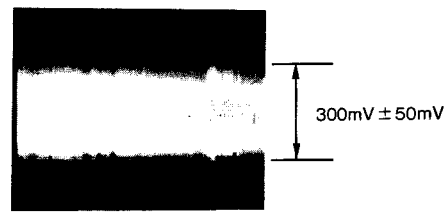
- Purpose: To adjust the RF signal amplitude to the optimum value.
- When not properly adjusted: Dropout occurs frequently.

• Measuring instruments and jigs:	• Oscilloscope
• Measuring point:	• FTSB assembly TP1 (RF signal)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #15,000 (#15,000) • Still mode • Test Mode (TRKG servo: Close) • The carriage assembly should be in the forward position.
• Position to be adjusted	• FTSB assembly VR10 (RF gain)

Connection diagram



2. Connect FTSB ass'y TP1 to an oscilloscope



3. RF signal

Photo 11

Adjustment Procedure

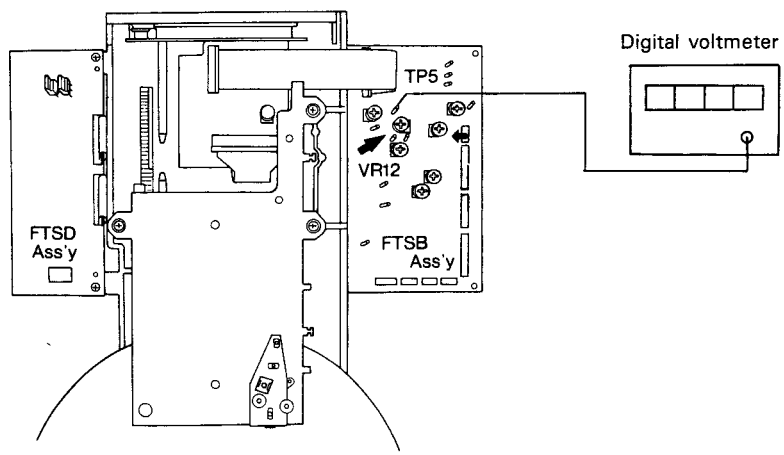
1. Play the LD test disc and search frame #15,000 (#15,000).
2. Connect an oscilloscope to FTSB assembly TP1 (RF signal) and observe the RF signal.
3. Adjust FTSB assembly VR10 so that the amplitude of the RF signal becomes 300 mV ± 50 mV. (Photo 11)

7. FOCS Sum Level Adjustment

- Purpose: To set the voltage of the FOCS (A + B) signal to the optimum value.
- When not properly adjusted: FOCS servo is not locked, and tracks may be skipped.

• Measuring instruments and jigs:	• Digital voltmeter
• Measuring point:	• FTSB assembly TP5 (FOCS (A + B))
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #15,000 (#15,000) • Play mode • The carriage assembly should be in the forward position.
• Position to be adjusted	• FTSB assembly VR12

Connection diagram



1. Connect FTSB ass'y TP5 to the digital volt meter.

Adjustment Procedure

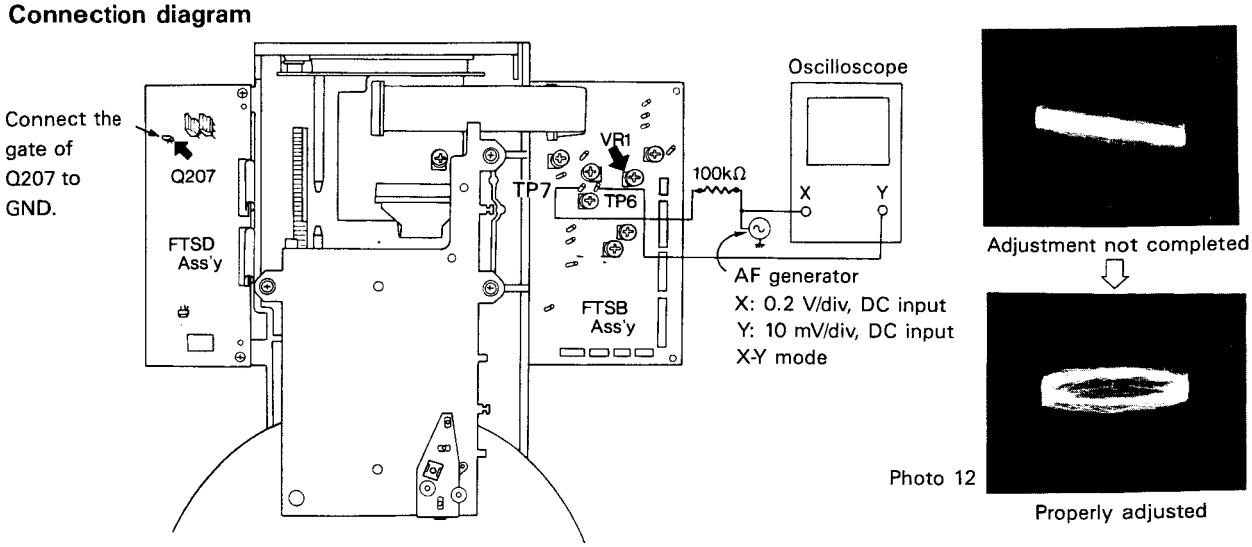
1. Connect FTSB assembly TP5 (FOCS A + B) to the digital voltmeter.
2. Play the 8-inch LD test disc and play frame #15,000.
3. Measure the voltage at TP5, and adjust FTSB assembly VR12 so that the voltage becomes 2.0 V DC.

8. FOCS Servo Loop Gain Adjustment

- Purpose: To set the loop gain of the FOCS servo to the optimum value.
- When not properly adjusted: Performance deteriorates.

• Measuring instruments and jigs:	• Oscilloscope • AF generator • Resistor (100k ohm)
• Measuring point:	• FTSB assembly TP7 (FOCS error), TP6 (FOCS gain)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #15,000 (#15,000) • Still mode • TRKG servo: Close • The FOCS motor protection circuit is disabled. • The carriage assembly should be in the forward position.
• Adjustment position	• FTSB assembly VR1

Connection diagram



1. Ground the gate of FTSD ass'y Q207.
2. Connect FTSB ass'y TP7, AF generator, resistor and the oscilloscope.
6. The X-axis and Y-axis of the Lissajous figure are symmetrical.

Adjustment Procedure

1. Connect the gate of the FTSD assembly Q207 to GND to inhibit the operation of the focus motor protection circuit.
2. Connect the resistor, AF generator and the oscilloscope to FTSB assembly TP7, as shown in the above diagram.
3. Set the AF generator output to 1.6 kHz/6 Vp-p for GGV1002, or 1.6 kHz/6 Vp-p for F2, according to the test disc used.
4. Play the 8-inch LD test disc and search frame #15,000 (#15,000).
5. Set the oscilloscope to the X-Y mode and observe the Lissajous figure.
6. Adjust VR1 on the FTSB assembly so that Lissajous figure is symmetrical on both the X- and Y-axes of the oscilloscope. (Photo 12)
7. Release the grounding from Q207 of the FTSD assembly.

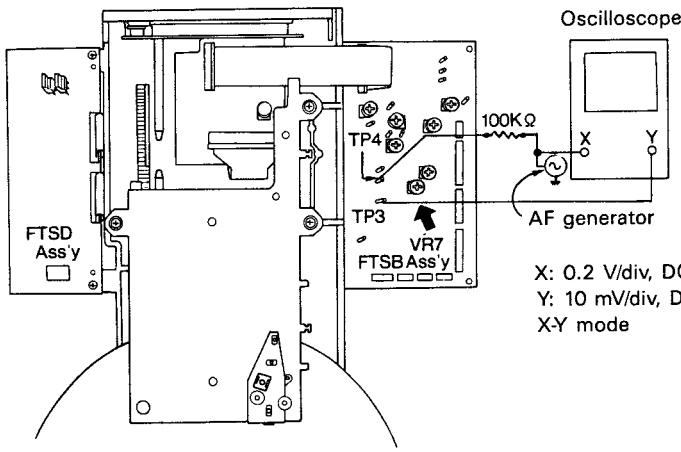
Note: If the AF generator output does not exceed 6 Vp-p, reduce the value of the resistor (100 kohm) in the above diagram, for easier observation of the Lissajous figure. (not below 33k ohms)

9. TRKG Servo Loop Gain Adjustment

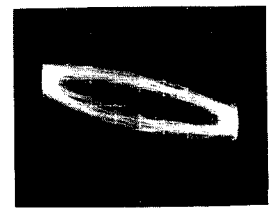
- Purpose: To set the loop gain of the TRKG servo to the optimum value.
- When not properly adjusted: Performance deteriorates.

• Measuring instruments and jigs:	• Oscilloscope • Resistor (100k ohm) • AF generator
• Measuring point:	• FTSB assembly TP4 (TRKG error), TP3 (TRKG gain)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #15,000 (#15,000) • Still mode • TRKG servo: Close
• Adjustment position	• The carriage assembly should be in the forward position. • FTSB assembly VR7

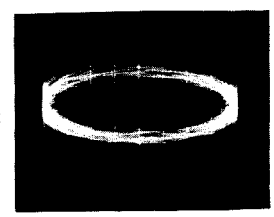
Connection diagram



2. Connect FTSB ass'y TP4, AF generator, resistor and the oscilloscope as shown.



⇩ Adjustment not completed



Properly adjusted

Photo 13

5. The X-axis and Y-axis of the Lissajous figure are symmetrical.

Adjustment Procedure

1. Play the LD test disc and search frame # 15,000 (#15,000).
2. Connect FTSB assembly TP4 to the oscilloscope's X-input via the resistor and AF generator, and TP3 to the Y-input, as shown in the above diagram.
3. Set the AF generator output to 3.4 kHz/6 Vp-p for GGV1002, or 3.5 kHz/6 Vp-p for F2, according to the test disc used.
4. Set the oscilloscope to the X-Y mode and observe the Lissajous figure.
5. Adjust VR7 on the FTSB assembly so that the Lissajous figure is symmetrical on both the X- and Y-axes of the oscilloscope. (Photo 13)

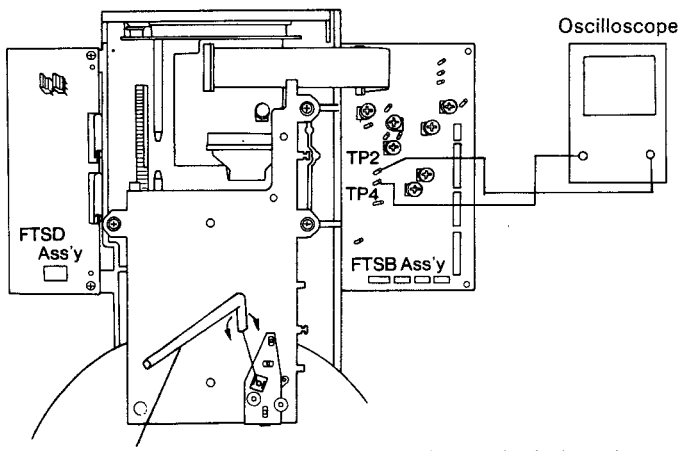
   Note: If the AF generator output does not exceed 6 Vp-p, reduce the value of the resistor (100k ohm) in the above diagram, for easier observation of the Lissajous figure. (not below 33k ohms)

10. Centering Adjustment for Side B Play

- Purpose: To set the center of the spindle motor on the path of the laser beam when playing the side B of the disc.
- When not properly adjusted: Tracks skipped, longer searching time or searching is impossible when playing side B of the disc.

• Measuring instruments and jigs:	• L-shaped eccentric screwdriver (GGV-129) • Oscilloscope
• Measuring points:	• FTSB assembly TP4 (TRKG error), TP2 (TRKG sum)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #100 (#300) • Play mode • The carriage assembly should be in the reverse position. • Test mode (TRKG servo: Open/Close)
• Position to be adjusted	• Centering adjustment hole for side B

Connection diagram

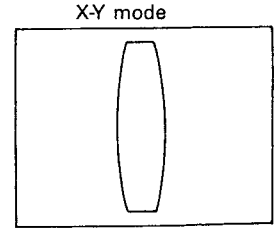


L-shaped eccentric screwdriver

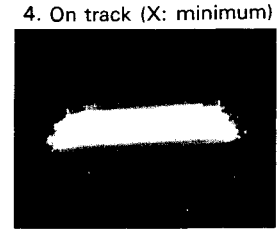
4. Centering adjustment for side B play

(Insert the L-shaped eccentric screwdriver with its grip on the spindle side.)

X: 20 mLV/div
Y: 20 mV/div
X-Y mode



4. On track (X: minimum)



4. Properly adjusted (X: maximum)

Photo 14

Adjustment Procedure

1. Turn the LD test disc upside-down (change from side A to side B).
2. Set the oscilloscope to the X-Y mode, and connect FTSB assembly TP4 (TRKG error) to the oscilloscope's X-input (CH-1) and TP2 (TRKG sum) to the Y-input (CH-2).
3. Play the LD test disc and search frame #100 (#300), then open the tracking servo.

Note: If the center is too eccentric on side B of the disc, since searching will be impossible on side B, open the TRKG servo when the carriage assembly moves to the side B play position and searches around frame #100.

4. While observing the Lissajous figure on the oscilloscope, insert the eccentric screwdriver into the centering adjustment hole for side B and adjust it so that the X-axis amplitude of the Lissajous figure is minimized (on-track position). Then turn the eccentric screwdriver clockwise further until the X-axis amplitude of the Lissajous figure becomes maximum. (Photo 14)

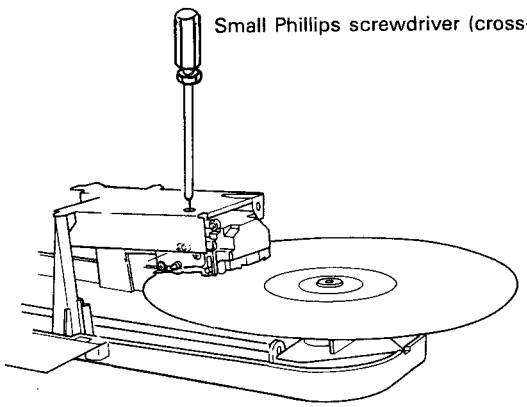
Note: When "2 (1) Tangential Direction Angle Adjustment" is performed with the pick-up in the forward direction, perform "11. Pick-up Tangential Direction Angle Adjustment for Side B Play" and "12. Fine Centering Adjustment for Side B play".

11. Pick-up Tangential Direction Angle Adjustment for Side B Play

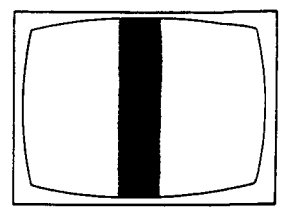
- Purpose: To adjust the crosstalk to become minimum in the tangential direction angle of the pick-up assembly when playing side B of the disc.
- When not properly adjusted: Crosstalk is significant.

• Measuring instruments and jigs:	• TV monitor • Small Phillips screwdriver (cross-bladed)
• Measuring point:	• Monitor screen
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #115 (#104) • Still mode • The carriage assembly should be in the reverse position.
• Position to be adjusted	• Pick-up tangential direction angle adjustment screw

Connection diagram



2. Pick-up tangential direction angle adjustment



2. Minimum crosstalk

Adjustment Procedure

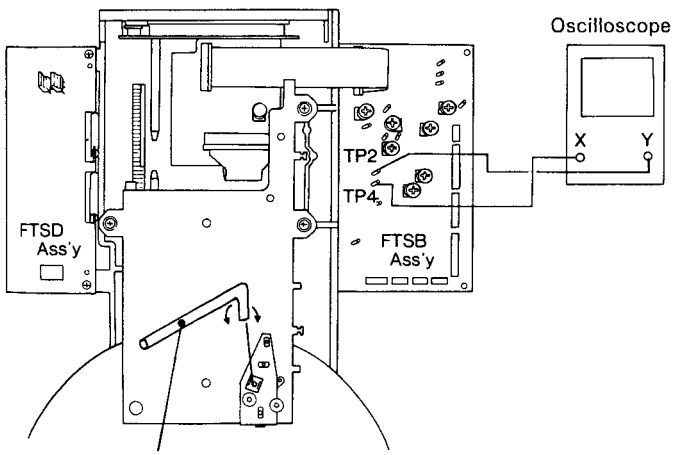
1. Play the LD test disc and search frame #115 (#104).
2. Check if crosstalk appears on the screen of the TV monitor, and adjust the pick-up tangential direction angle adjustment screw so that the crosstalk is minimized.
3. After steps 1 and 2 have been completed, perform "10. Centering Adjustment for Side B Play" again.
   Note: When the pick-up tangential direction angle for side B play is varied by this adjustment, the center of the disc for side B may be shifted slightly. As a countermeasure, perform the centering adjustment again.
   (→ 12. Fine Centering Adjustment for Side B Play)

12. Fine Centering Adjustment for Side B Play

- Purpose: To set the center of the spindle motor on the track of the laser beam when playing the side B of the disc.
- When not properly adjusted: Tracks skipped when playing side B of the disc.

• Measuring instruments and jigs:	• Oscilloscope • L - shaped eccentric screwdriver (GGV-129)
• Measuring points:	• FTSB assembly TP4 (TRKG error), TP2 (TRKG sum)
• Test disc and player mode	• 8-inch LD test disc GGV1002 ... #100 (#300) • Play mode • The carriage assembly should be in the reverse position. • Test mode (TRKG servo: Open)
• Adjustment position	• Centering adjustment hole for side B

Connection diagram



L-shaped eccentric screwdriver

4. Fine centering adjustment for side B play

(Insert the L-shaped eccentric screwdriver with its grip on the spindle side.)

X: 20m V/div
Y: 20 mV/div
X-Y mode

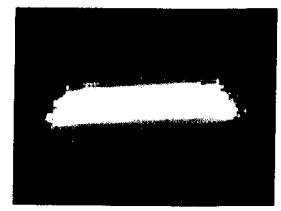


Photo 15

4. X-axis of Lissajous figure maximum

Adjustment Procedure

1. Set the oscilloscope to the X-Y mode, and connect FTSB assembly TP4 (TRKG error) to the oscilloscope's X-input (CH-1) and TP2 (TRKG sum) to the Y-input (CH-2).
2. Play the LD test disc and search frame #100 (#300).
3. Open the TRKG servo.
4. While observing the Lissajous figure on the oscilloscope, insert the eccentric screwdriver into the centering adjustment hole for side B and adjust it so that the X-axis amplitude of the Lissajous figure becomes maximum. (Photo 15)

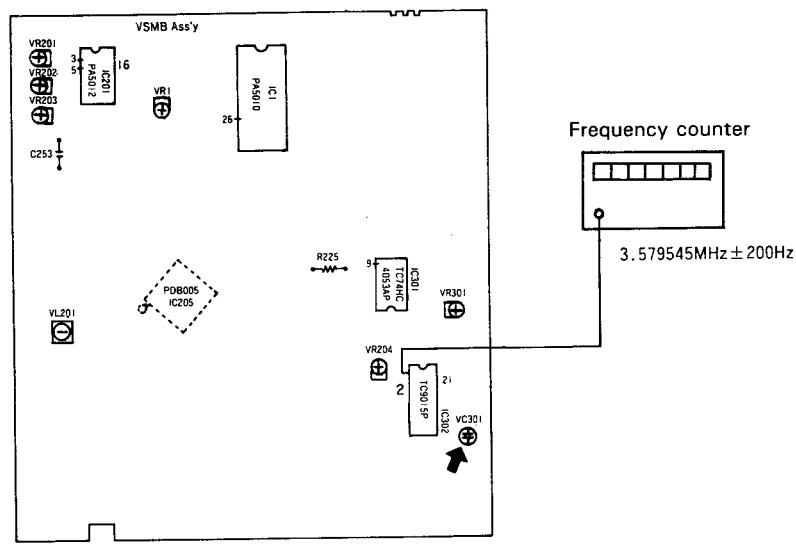
9.4 VSOP ASSEMBLY (VSMB ASSEMBLY AND VSSB ASSEMBLY) ADJUSTMENTS

1. Master Clock Frequency Adjustment

- Purpose: To set the VCXO input voltage to the optimum value.
- When not properly adjusted: Horizontal scanning frequency is incorrect, resulting in distorted picture.

• Measuring instruments and jigs:	• Frequency counter
• Measuring position:	• IC302 (TC9015P) pin 2 in the VSMB assembly (TBC, MEM sections)
• Test disc and player mode:	• Power ON (Stop mode)
• Position to be adjusted:	• VC301 in the VSMB assembly (TBC, MEM sections)

Connection diagram



Adjustment Procedure

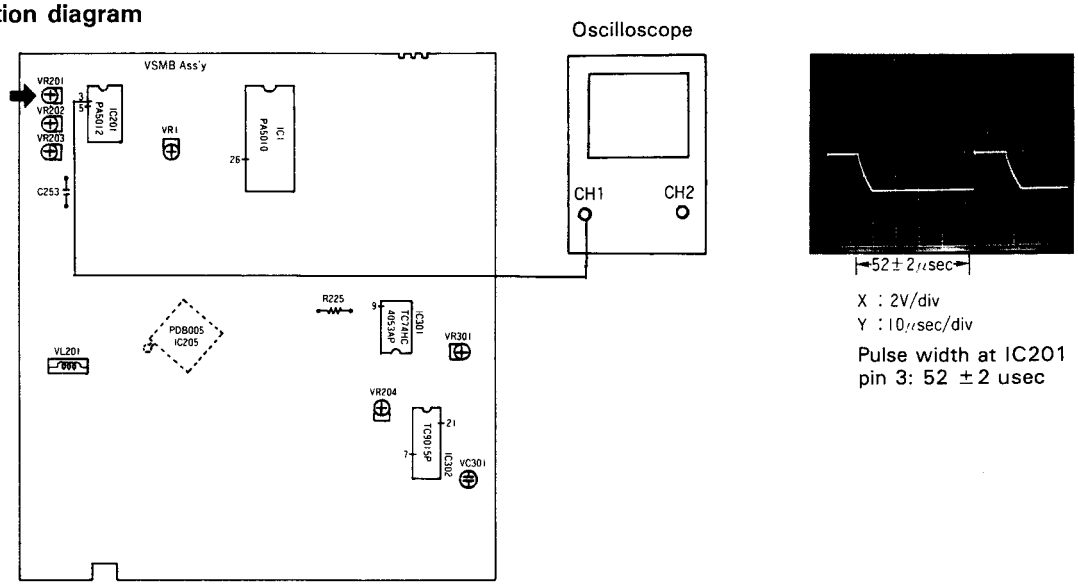
1. After switching the player's power ON, connect the frequency counter to pin 2 of IC302 in the VSMB assembly (TBC, MEM) to observe the frequency.
2. Adjust VC301 in the VSMB assembly so that the frequency at pin 2 becomes 3.57945 MHz ±200 Hz.

2. Half H Rejection Adjustment

- Purpose: To set the MMV output for half H rejection to the optimum value.
  (MMV: Monostable Multi Vibrator)
- When not properly adjusted: Longer search time. Picture not synchronized (SPDL lock does not function).

• Measuring instruments and jigs:	• Oscilloscope
• Measuring position:	• IC201 (PA5012) pin 3 in the VSMB assembly (TBC, MEM sections)
• Test disc and player mode:	• Play the LD test disc.
• Position to be adjusted:	• VR201 in the VSMB assembly (TBC, MEM)

Connection diagram



Adjustment Procedure

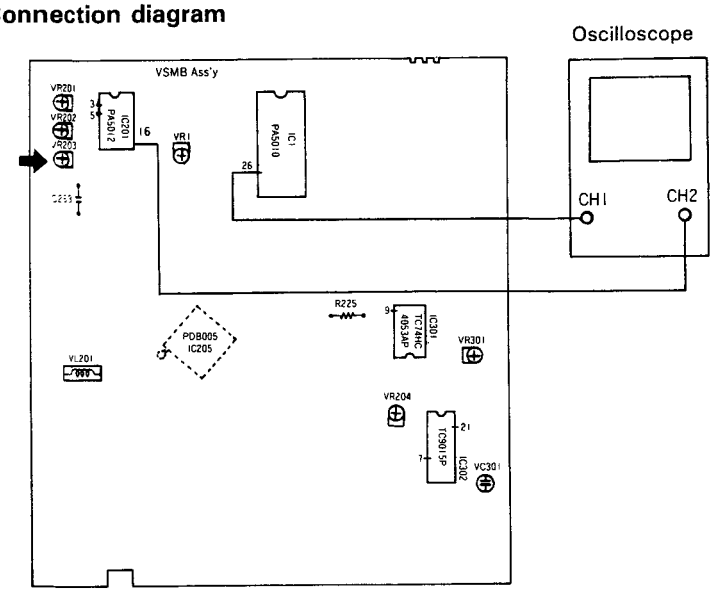
1. Play the LD test disc, and connect the oscilloscope to pin 3 of IC201 (PA5012) in the VSMB assembly (TBC, MEM) to observe the pulse waveform.
2. Adjust VR201 in the VSMB assembly so that the pulse width at pin 3 becomes 52 ±2 μsec.

3. Burst Gate Timing Adjustment

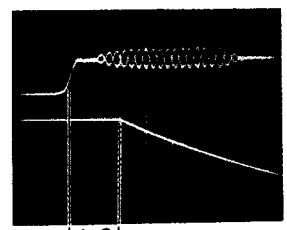
- Purpose: To set the burst gate to the optimum value.
- When not properly adjusted: Play back starts from the middle of the disc.
  No color or irregular color, or thin stripes are noticeable.

• Measuring instruments and jigs:	• Oscilloscope
• Measuring positions:	• VSMB assembly IC201 (PA5012) pin 16, IC1 (PA5010) pin 26
• Test disc and player mode:	• LD test disc • Play mode
• Position to be adjusted:	• VSMB assembly (TBC, MEM) VR203

Connection diagram



X: 20 mV/div, DC input
Y: 0.2V/div, DC input



Upper: (TBC VIDEO)

Lower:

Photo 17

Adjustment Procedure

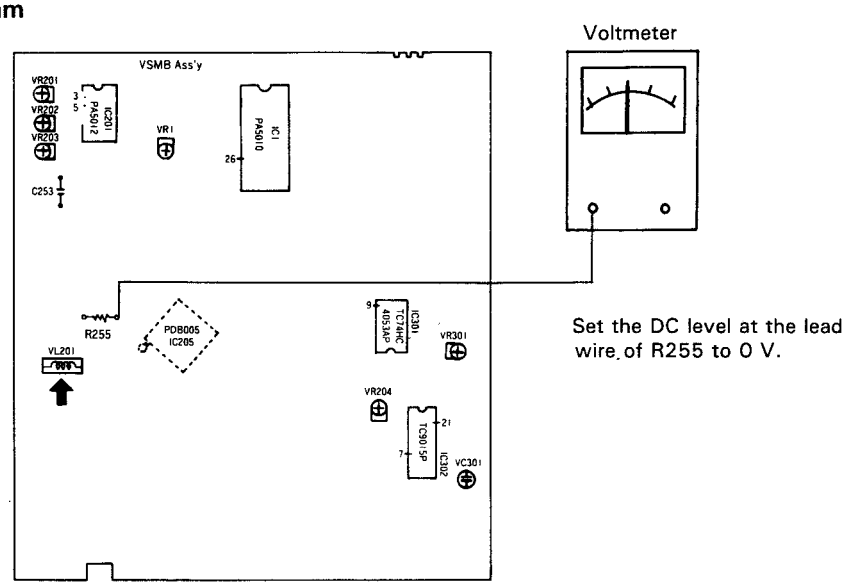
1. Play the LD test disc.
2. Connect the oscilloscope's X-input (CH-1) to the pin 26 of IC1 (PA5010) in the VSMB assembly and Y-input (CH-2) to pin 16 of the IC201 (PA5012).
3. Adjust VR203 in the VSMB assembly so that descending point of the MMV's output comes 1 μsec later than the rising edge of the video signal. (Photo 17)

4. VCO Offset Voltage Adjustment

- Purpose: To set the offset voltage of the 14.31818 MHz VCO to 0 V.
- When not properly adjusted: Picture is not synchronized when scanning with a CLV or CDV disc. No horizontal synchronization. No color.

• Measuring instruments and jigs:	• Voltmeter
• Measuring positions:	• Lead wire of R225 in the VSMB assembly (TBC, MEM sections)
• Test disc and player mode:	• Play the LD test disc. (PLL lock condition)
• Position to be adjusted:	• VL201 in the VSMB assembly (TBC, MEM sections)

Connection diagram



Adjustment Procedure

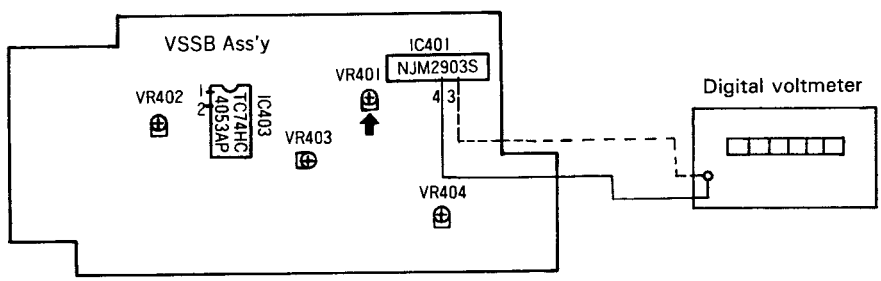
1. Play the LD test disc.
2. Connect the voltmeter to the lead wire from R255 in the VSMB assembly, and adjust VL201 so that the DC level becomes 0 V.
   Note: If this adjustment is too far from the standard value, it may be impossible to play a disc.

5. Detection Level Adjustment

- Purpose: To set the input voltage applied to the comparator for the detection of spindle motor overrunning
- When not properly adjusted: Spindle servo is not locked, and screen distorted.

• Measuring instruments and jigs:	• Digital voltmeter
• Measuring positions:	• VSSB assembly IC401 (NJM2903S) pin3, pin 4
• Test disc and player mode:	• N-series LD test disc ... #4,801 (F-series ... #5,401)
• Position to be adjusted:	• VSSB assembly VR401

Connection diagram



Adjustment Procedure

1. Play the LD test disc and search frame #4,801 (# 5,401).
2. Connect the digital voltmeter to pin 3 of IC401 (NJM2903S) in the VSSB assembly, and measure and write down the reference voltage of the detection comparator for the overrunning of the spindle motor.
3. Connect the digital voltmeter to IC401 pin 4 and measure the output voltage for speed detection. Adjust VR401 in the VSSB assembly so that the voltage at pin 4 is higher than the voltage at pin 3 by 330 mV ± 20mV.

6. Trapezoid Inclination Adjustment

- Purpose: To adjust the inclination of the trapezoidal (pulse) waveform used for SPDL/TBC error detection.
- When not properly adjusted: Flickering on the screen in the through or still mode with a CAV disc. Memory picture is displaced.

• Measuring instruments and jigs:	• Oscilloscope
• Measuring positions:	• Pin 5 of IC201 (PA5012) in the VSMB assembly (TBC, MEM sections). Land adjacent to pin 1.
• Test disc and player mode:	• Short-circuit both ends of C253 in the VSMB assembly (DC reset mode). • Play the LD test disc. (PLL lock condition)
• Position to be adjusted:	• VR202 in the VSMB assembly (TBC, MEM sections)

Connection diagram

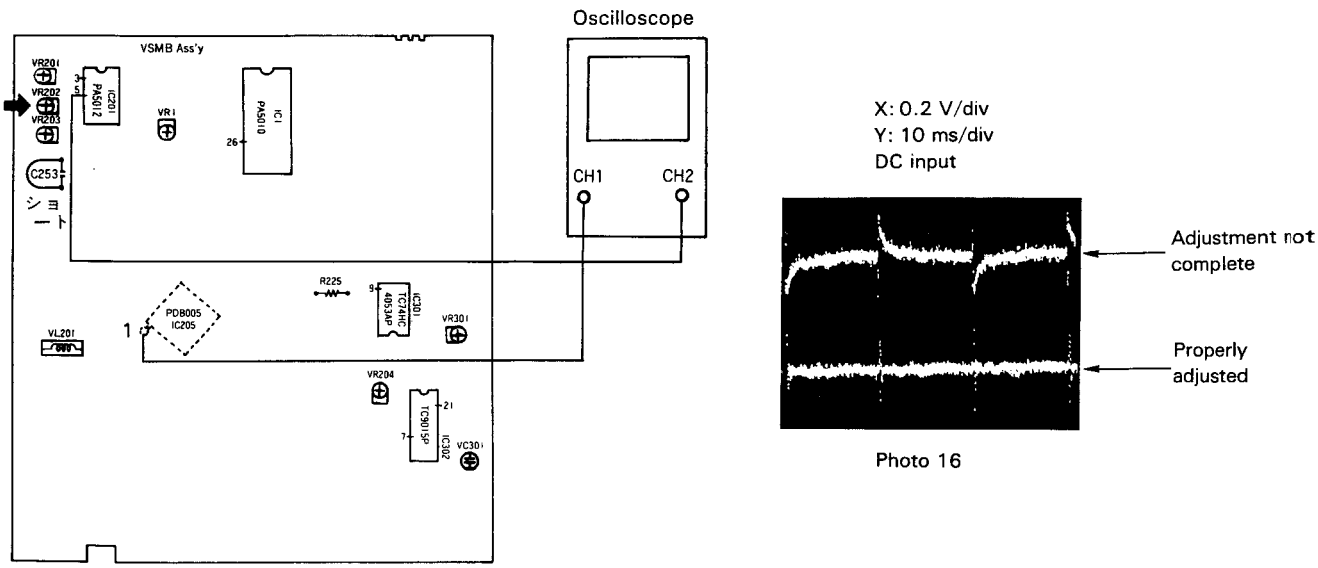


Photo 16

Adjustment Procedure

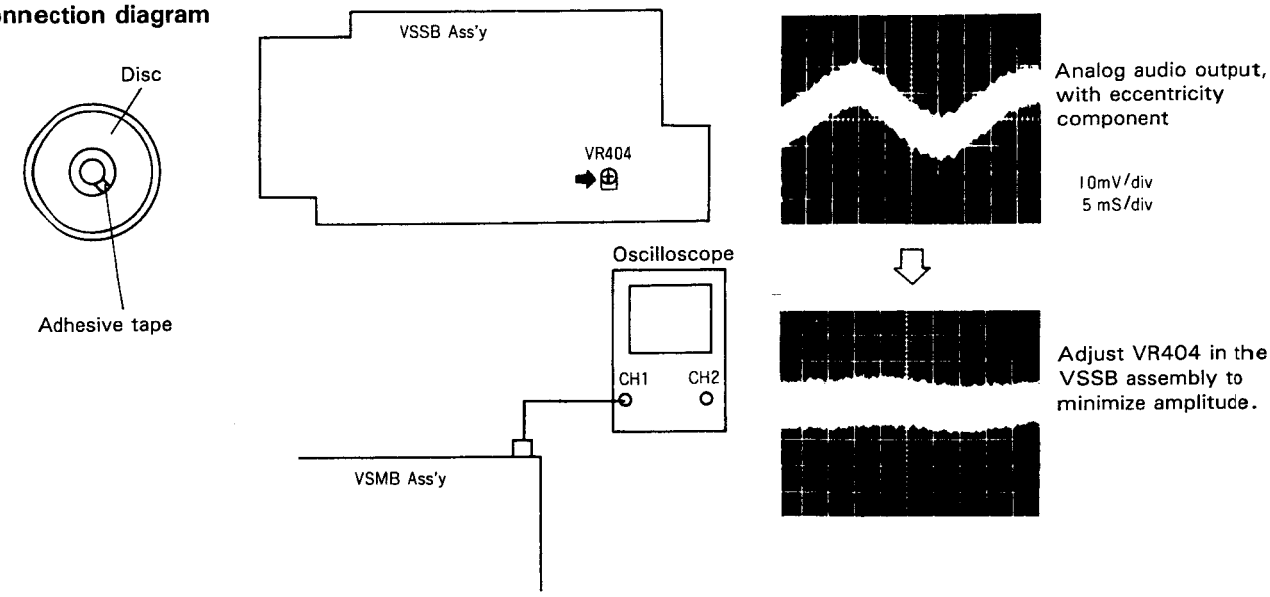
1. Short-circuit both ends of C253 in the VSMB assembly. (DC reset mode)
2. Connect the land adjacent to IC205 pin 1 (560 msec detection window) in the VSMB assembly to the CH-1 input of the oscilloscope, and connect pin 5 of IC201 (PBH) to the CH-2 input.
3. Adjust VR202 so that the falling point of the waveform at IC201 pin 5 comes at the center of "H" period of the waveform at pin 1.

7. PLL Gain Adjustment

- Purpose: To cancel the eccentricity components superimposed on the audio signal.
- When not properly adjusted: Poor audio S/N ratio. Shaded color on the screen when playing a CDV disc.

• Measuring instruments and jigs:	• Oscilloscope • Adhesive tape
• Measuring position:	• Audio output terminals L/R
• Test disc and player mode:	• LD test disc ... #2,701 (#2,701); (Stick adhesive tape at the center hole) • Check ... (CDV disc)
• Position to be adjusted:	• VR404 in the VSSB assembly

Connection diagram



Adjustment Procedure

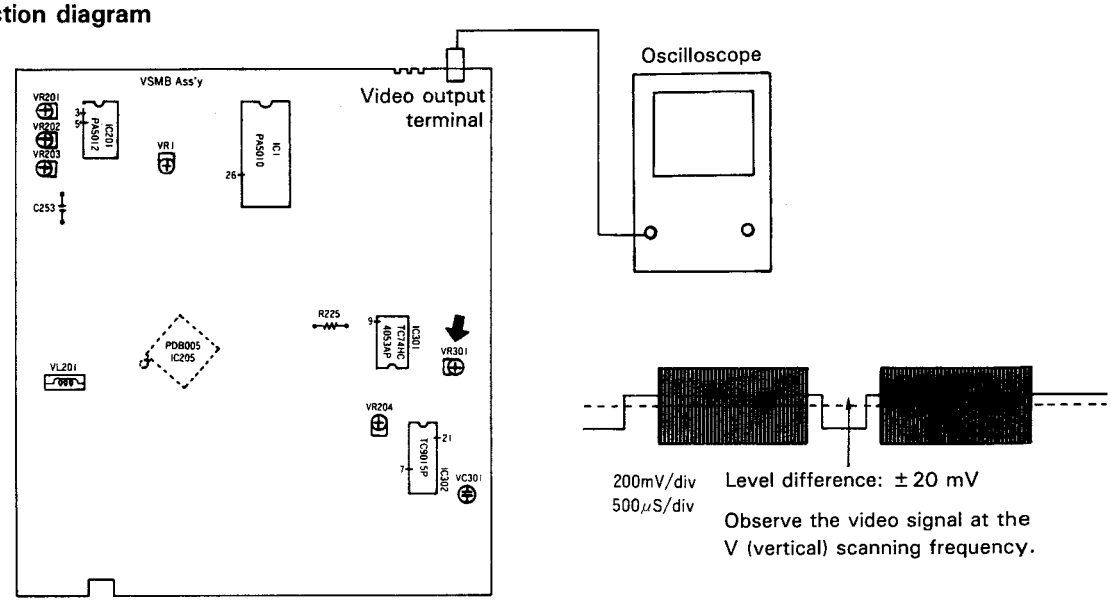
1. Stick adhesive tape at the center hole of the LD test disc to make it eccentric.
2. Connect the audio output terminal in the VSSB assembly to the oscilloscope.
3. Play the LD test disc around frame #2,701 (#2,701) and observe the waveform on the oscilloscope.
4. Adjust VR404 in the VSSB assembly so that the waveform amplitude becomes minimum and minimized the level difference between the L and R channels.
5. Play the CDV disc and check that a shaded color band does not appear on the screen.

8. Sync DC Level Adjustment

- Purpose: To set the pedestal level of the output video signal to an appropriate level.
- When not properly adjusted: Screen too dark or too bright.

• Measuring instruments and jigs:	• Oscilloscope
• Measuring position:	• Video output terminal
• Test disc and player mode:	• LD test disc: N series ... #2,701 (F series ... #2,701) • Play mode
• Position to be adjusted:	• VR301 in the VSMB assembly

Connection diagram



Adjustment Procedure

1. Connect the video output terminal in the VSMB assembly to the oscilloscope.
2. Play the LD test disc around the frame #2,701 (#2,701) and observe the video signal waveform on the oscilloscope set to the vertical rate.
3. Adjust VR301 in the VSMB assembly so that the difference of the pedestal level becomes 0 ±20 mV.

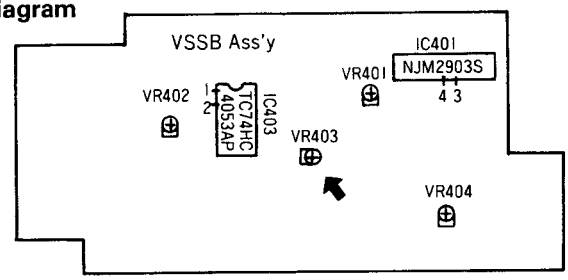
9. Output Video Level Adjustment

9.4 VSOP (VDEM) Assembly Adjustment

- Purpose: To set the output video signal amplitude (between the pedestal level and 100% white level) to 0.71 Vp-p.
- When not properly adjusted: Video data cannot be read out and play starts in the middle of the disc.
  Screen is too bright or too dark.

• Measuring instruments and jigs:	• Oscilloscope
• Measuring position:	• Video signal output terminal in the ADEM Assembly
• Test disc and player mode:	• N-series LD test disc ... #19,801 (F-series ... #19,801)
• Position to be adjusted:	• VSSB assembly VR403

Connection diagram



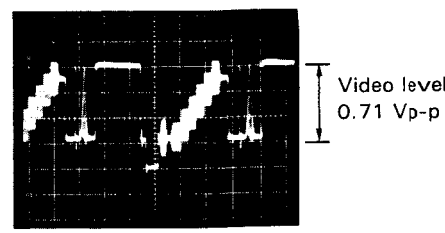
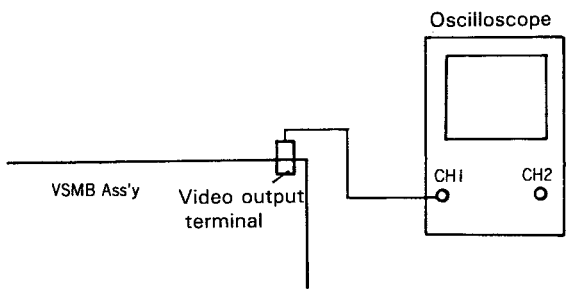


Photo 20



Adjustment Procedure

Note: The video output terminal should be terminated with 75 ohms by connecting to the video monitor. When a TV without a video input terminal is used, terminate the video output terminal using a 75-ohm resistor.

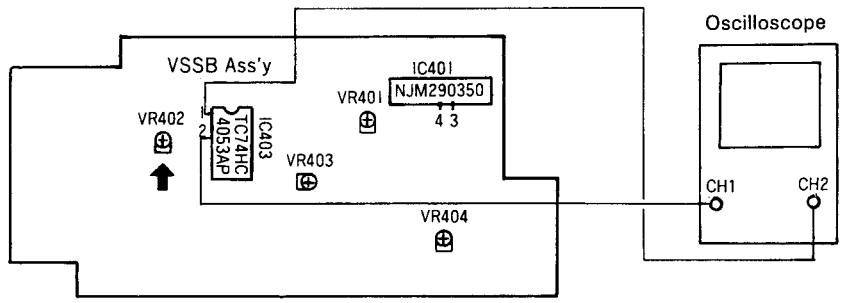
1. Play the LD test disc and search frame #19,801 (#19,801).
2. Connect the oscilloscope to the video output terminal and observe the playback video signal waveform.
3. Adjust VR403 in the VSSB assembly so that the amplitude between the pedestal level and the white level of the playback video signal waveform becomes 0.71 Vp-p ±0.5%. (Photo 20)

10. 1H Delay Video Level Adjustment

- Purpose: To adjust so that the amplitude of the video signal subject to 1H delay becomes the same as the amplitude of the main track video signal.
- When not properly adjusted: When 1H delay level is too high
  → White dropout becomes noticeable and horizontal sync is disordered (horizontal stripes appear on the screen)
  When 1H delay level is too low
  → Black dropout becomes noticeable

• Measuring instruments and jigs:	• Dual-trace oscilloscope
• Measuring positions:	• VSSB assembly IC403 (TC74HC4053AP) pin 1, pin 2
• Test disc and player mode:	• N-series LD test disc ... #19,801 (F-series ... #19,801)
• Position to be adjusted:	• VSSB assembly VR402

Connection diagram



Adjustment Procedure

1. Play the LD test disc and search frame #19,801 (#19,801).
2. Connect the oscilloscope's CH-1 to pin 2 of IC403 (TC74HC4053AP) in the VSSB assembly and CH-2 to pin 1 of IC403, to observe the main track video signal waveform and the 1H delay line video signal waveform at the same time.
3. Adjust VR402 in the VSSB assembly so that the amplitude from the sync tip to the white level of the 1H delay video signal (CH-2) becomes the same as that of main track video signal (CH-1). (Photo 18)

X: 50 mV/div, DC input
Y: 50 mV/div, DC input
10 μs/div

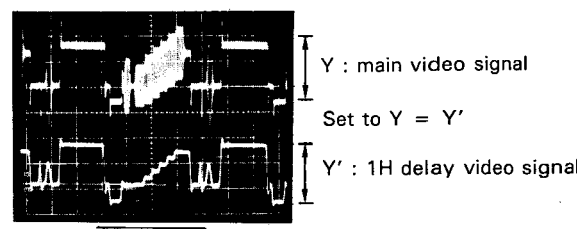


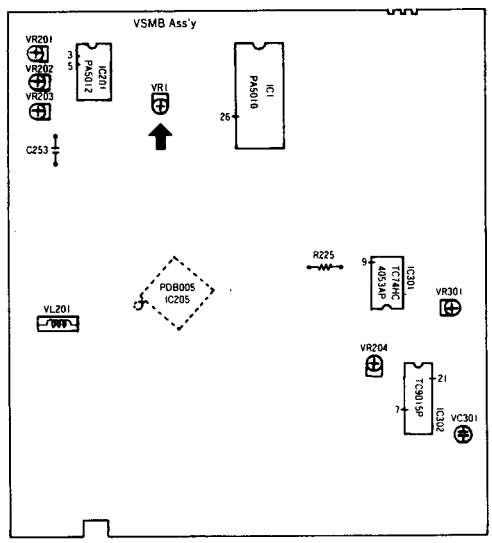
Photo 18

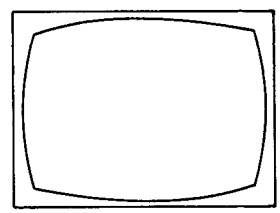
11. Hue Error Signal Level Adjustment

- Purpose: To set the amount of the hue error signal applied to the color hue compensator to the optimum value.
- When not properly adjusted: Irregular color significant

• Measuring instruments and jigs:	• TV monitor
• Measuring position:	• Adjust by watching the screen of the monitor
• Test disc and player mode:	• N-series LD test disc ... #7,201 (F-series . #26,101)
• Adjustment position:	• VSMB assembly VR1

Connection diagram





TV screen Minimize irregular color

Adjustment Procedure

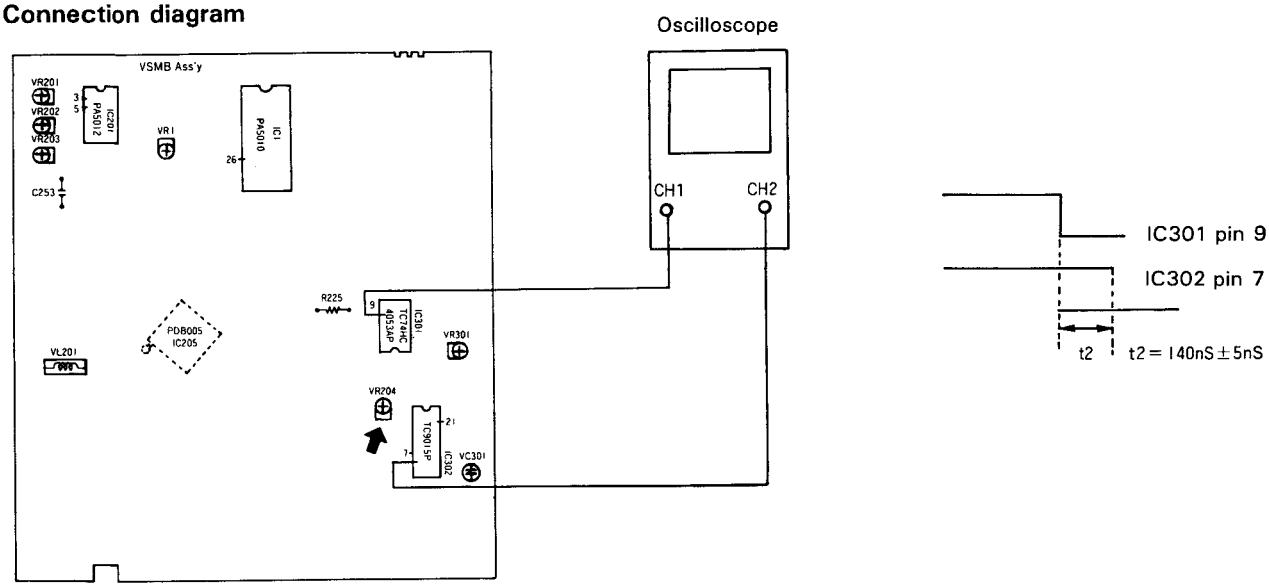
1. Play the LD test disc and search frame #7,201 (#26,101).
3. Adjust VR1 in the VSMB assembly so that irregularities of the magenta screen are minimized.

12. 140ns Shift Level Adjustment

- Purpose: To make the amplitudes of the chroma signal waveform of the video signal which is shifted by 140 ns and that of the video signal which is not shifted the same.
- When not properly adjusted: Flickering on the TV screen.

• Measuring instruments and jigs:	• Dual-trace oscilloscope
• Measuring position:	• IC301 (TC74HC4053AP) pin 9, IC302 (TC9015P) pin 7 in the VSMB assembly
• Test disc and player mode:	• LD test disc: N series ... #2,701 (F series ... #2,701) • Still mode
• Position to be adjusted:	• VR204 in the VSMB assembly (TBC, MEM)

Connection diagram



Adjustment Procedure

1. Connect IC301 pin 9 in the VSMB assembly to CH-1 of the oscilloscope and connect IC302 pin 7 to CH-2.
2. Play the LD test disc and search frame #2,701 (#6,301).
3. Trigger the oscilloscope at the falling edge of the output waveform at IC301 pin 9 (CH-1).
4. Adjust VR204 in the VSMB assembly so that the period "t2" shown in the "connection diagram" becomes 140 ns ±5 ns.

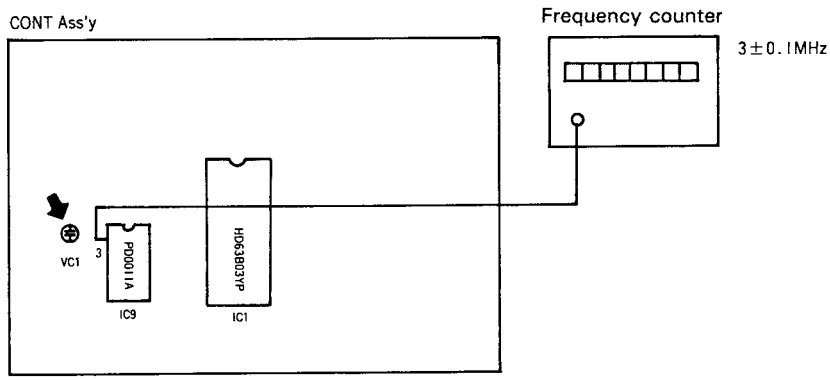
9.5 CONT ASSEMBLY ADJUSTMENTS

1. Decoder Clock Adjustment

- Purpose: To set the decoder clock frequency to an appropriate value.
- When not properly adjusted: Longer search time.

• Measuring instruments and jigs:	• Frequency counter
• Measuring posiiton	• IC9 (PD0011A) pin 3 in the CONT assembly
• Test disc and player mode:	• Set the player to the test mode (PD0011A oscillating mode) (Refer to "Test mode" on page 84.)
• Position to be adjusted:	• VC1 in the CONT assembly

Connection diagram



Adjustment Procedure

1. Open the front door and switch the player's power ON with no disc loaded. (Refer to "Test mode" on page 84.)
2. Press the [CX] and [6] buttons on the remote control simultaneously so that IC9 pin 3 enters the 3 MHz oscillating mode.
3. Connect the frequency counter to IC9 pin 3, and adjust VC1 so that the frequency becomes 3 MHz ± 100 kHz.
   Note: If no reading appears on the frequency counter, attach a 1-kohm resistor to IC9 pin 3 to pull the voltage up to +5 V.

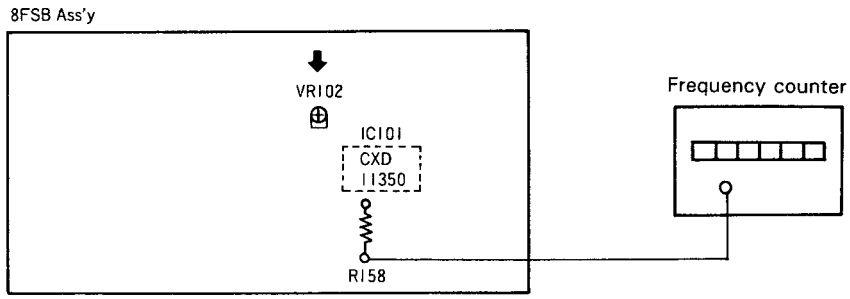
9.6 8FSB ASSEMBLY ADJUSTMENT

1. VCXO Freerunning Frequency Adjustment

- Purpose: To adjust the frequency of the crystal oscillator used by the EFM decoder to the optimum value.

• Measuring instruments and jigs:	• Frequency counter
• Measuring point:	• Lead wire of R158 in the 8FSB assembly
• Test disc and player mode:	• CD test disc • Play any track of the disc
• Position to be adjusted:	• 8FSB assembly VR102

Connection diagram



Adjustment Procedure

1. Play any track of the CD test disc.
2. Connect the frequency counter to the lead wire of R158 in the 8FSB assembly and observe the free-running frequency of VCXO.
3. Adjust VR102 in the 8FSB assembly so that the frequency becomes 4.2336MHz ±200Hz.
   VCXO: Voltage Controlled Crystal Oscillator

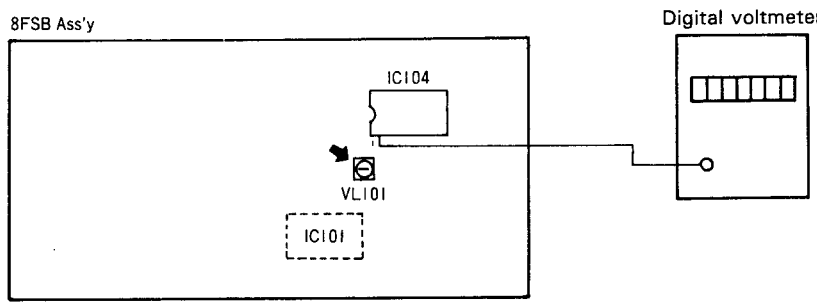
Note: With this adjustment, the VCXO will free run when playing CD and be locked when playing an LD.

2. PLL Freerunning Frequency Adjustment

- Purpose: To adjust the freerunning frequency of the PLL VCO used by the EFM decoder to the optimum value.
- When not properly adjusted: No sound is output, or sound is interrupted

• Measuring instruments and jigs:	• Digital voltmeter
• Measuring position:	• 8FSB assembly IC104 (NJM082S) pin 1
• Test disc and player mode:	• LD disc with digital audio (hereinafter, LDD) • Play an arbitrary frame
• Position to be adjusted:	• 8FSB assembly VL101

Connection diagram



Adjustment Procedure

1. Play any frame of the LDD disc.
2. Connect the digital voltmeter to pin 1 of IC104 in the 8FSB assembly and observe the DC voltage of the VCO control signal.
3. Adjust VL101 of the 8FSB assembly so that the DC voltage of the VCO control signal becomes +400 mV ± 100 mV.

PLL : Phase Locked Loop
VCO : Voltage Controlled Oscillator

Note: This adjustment should be performed with the PLL in the locked condition.

3. VCXO Offset Adjustment

- Purpose: To set the offset voltage of the VCXO PLL phase error signal to minimum.
- When not properly adjusted: Digital audio output is interrupted when playing an LDD disc. (Noise appears synchronously)

• Measuring instruments and jigs:	• Oscilloscope
• Measuring position:	• Lead wire of R128 (MDP) in the 8FSB assembly
• Test disc and player mode:	• LDD disc • Play any frame
• Position to be adjusted:	• 8FSB assembly VR101

Connection diagram

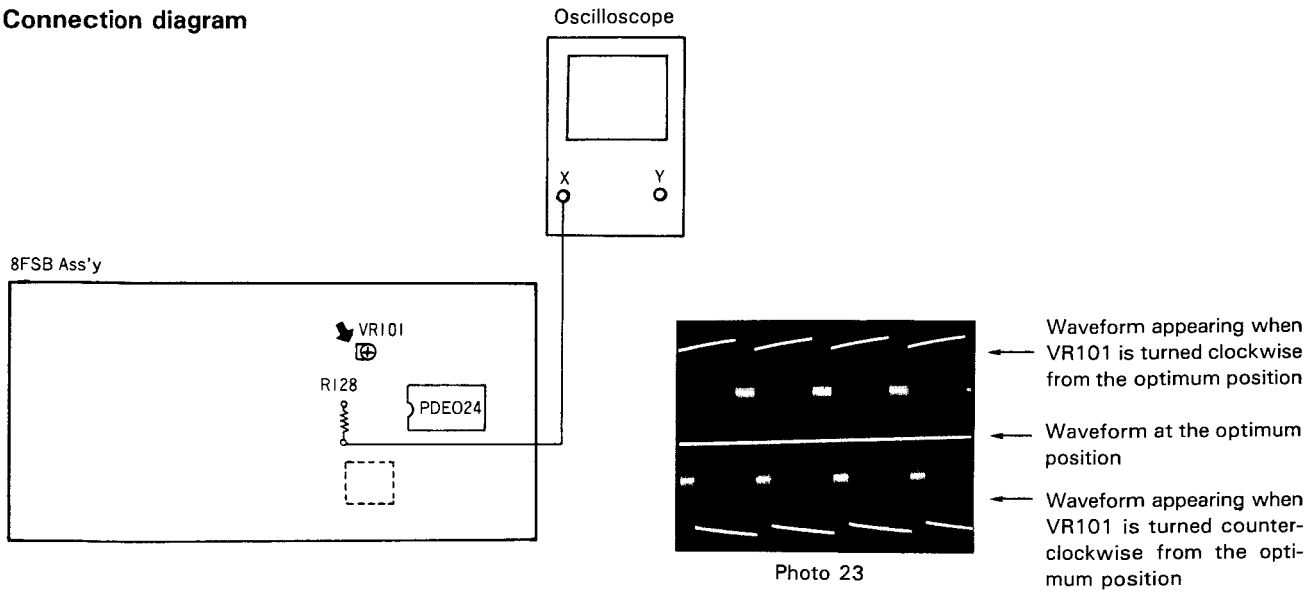


Photo 23

Waveform appearing when VR101 is turned clockwise from the optimum position

Waveform at the optimum position

Waveform appearing when VR101 is turned counter-clockwise from the optimum position

Adjustment Procedure

1. Play any frame of the LDD disc.
2. Connect the oscilloscope to the lead wire of R128 (MDP) in the 8FSB assembly and observe the PLL phase error output signal of the VCXO.
3. Adjust VR101 in the 8FSB assembly so that the width of the pulse appearing on the positive or negative side becomes minimum with continuous waveforms. (Photo 23, center)

VCXO : Voltage Controlled Crystal Oscillator
PLL : Phase Locked Loop

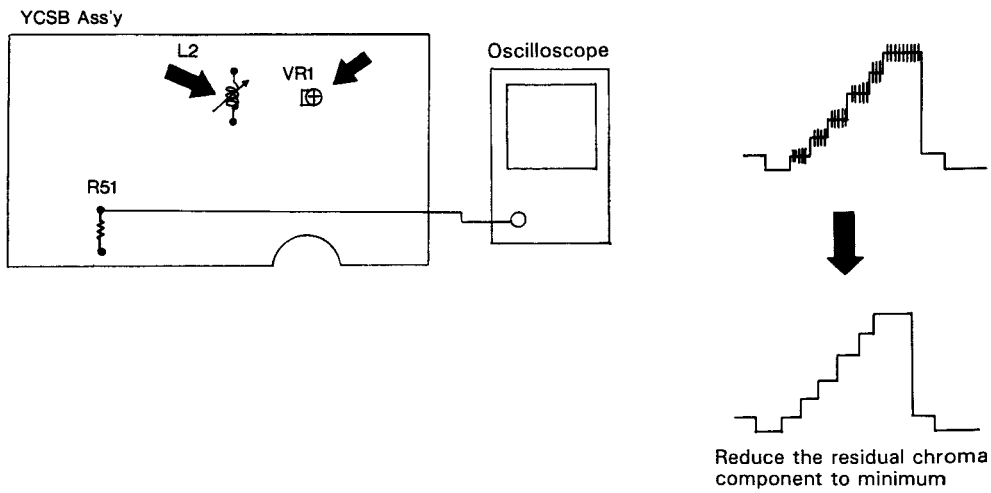
9.6 YCSB ASSEMBLY ADJUSTMENT

9.6 YCSB Assembly Adjustment

- Purpose: To set the chroma component included in the luminance signal to minimum.
- When not properly adjusted: Dot interference increases on the screen and the image becomes too glossy.

• Measuring instruments and jigs:	• Oscilloscope • LD test disc
• Measuring position:	• Lead wire of R51 in YCSB assembly
• Test disc and player mode:	• N-series LD test disc ... #19,801 (F-series ... #19,801)
• Positions to be adjusted:	• YCSB assembly VR1, L2

Connection diagram



Adjustment Procedure

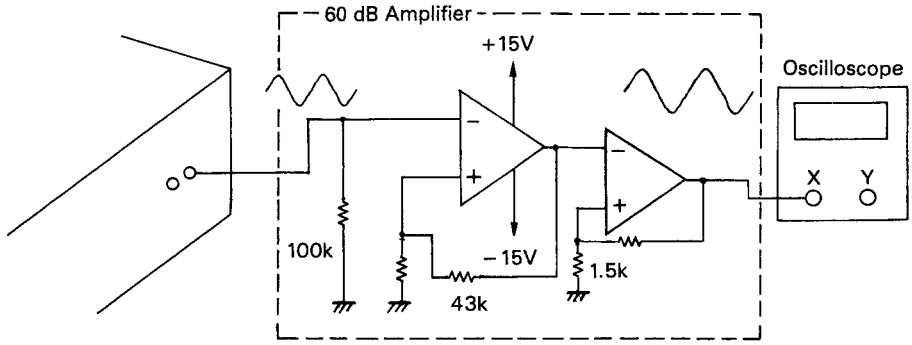
1. Connect an oscilloscope to the lead wire of R51 in the YCSB assembly.
2. Play frame #19,801 (#19,801) of the LD test disc.
3. Observe the luminance signal and turn VR1 to minimize the chroma component.
4. Turn L2 further so that the chroma component is minimized.
5. Repeat the procedures in steps 3 and 4.
6. Check that there is no abnormal color in the image on the TV screen.

MSB adjustmetn

- Minimize the distortion noise of audio signal.
-

• Measuring instruments and jigs:	• Oscilloscope • 60dB amplifier
• Measuring point:	• Audio output terminals (L and R)
• Test disc and player mode	• YEDS-7
• Position to be adjusted	• DACB Assembly VR1

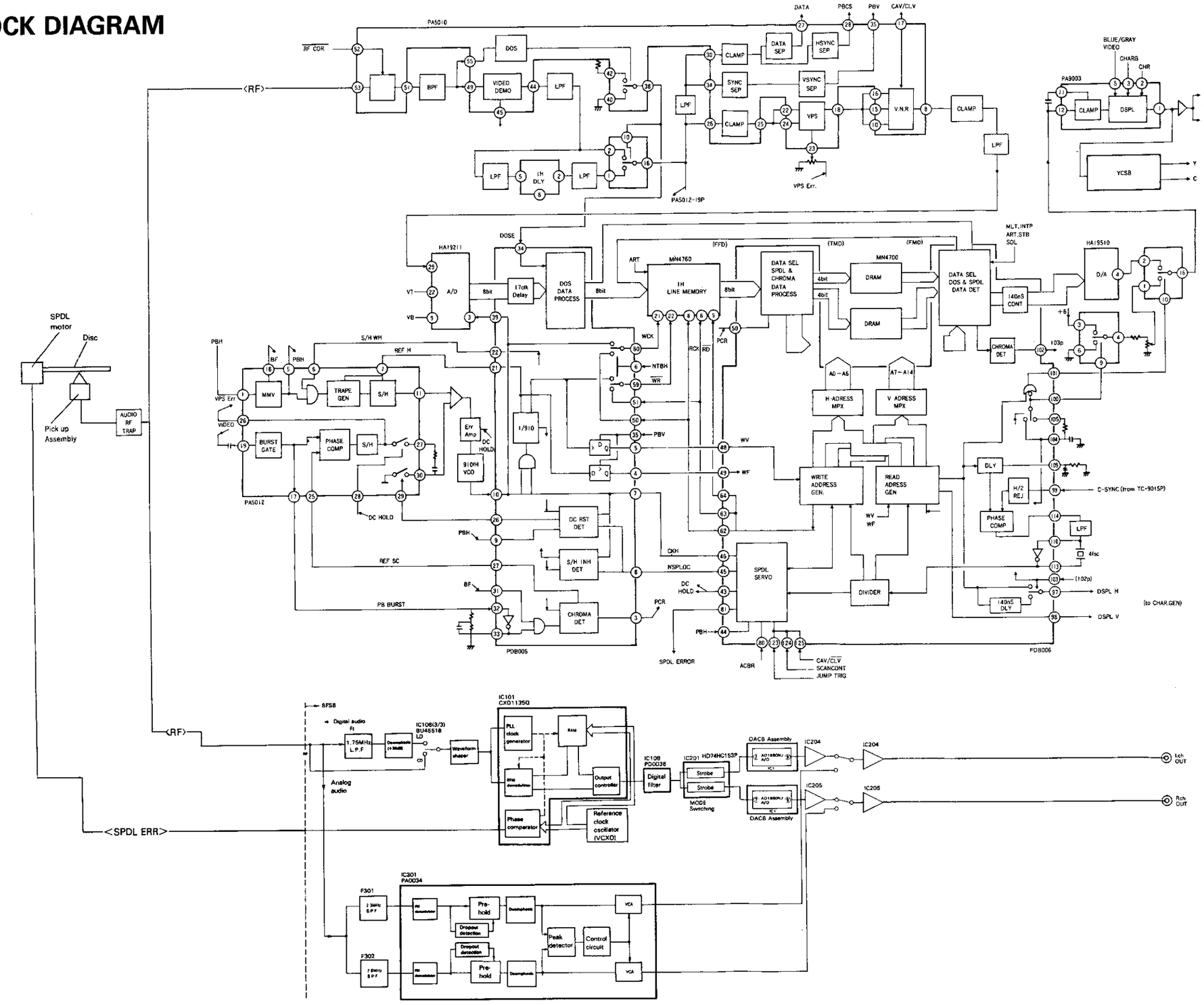
Connection diagram



Adjustment Procedure

1. Connect the 60dB amplifier between oscilloscope and Lch (Rch) of the audio out terminal. (Fig.)
2. Set the player to the normal play mode.
3. Play back the track 20 (−60dB 1kHz, Lch or Rch) of the test disc (YEDS-7).
4. Observe the audio output waveform.
5. Adjust VR1 of DACB assembly so that a smooth sine wave is obtained on the oscilloscope.

10. BLOCK DIAGRAM



11. DESCRIPTION OF BOTH-SIDES PLAYBACK MECHANISM (α-TURN SYSTEM)

11-1 OUTLINE

The both-sides playback mechanism is called "α-Turn System" and has the following features:

- The signal reading by the pickup assmbly from the disc surface is performed in the same way when playing both sides A and B.
- The relationship of the three beams (zero and first order beams) for signal read-out is the same when playing both sides A and B.
- The direction of rotation of the spindle motor is reversed when playing side B.

11-2 OUTLINE OF OPERATION

Fig. 11-1-1 shows the operating principles of the system.

The carriage assembly for side-A play moves toward the inner or outer edge of the disc guided by the carriage shaft (A). When the Carriage Assembly is inverted from Side A to Side B, the carriage assembly is moved toward the outer edge of the disc, through the carriage shaft (A) to the guide shaft at the inversion mechanism, and at the same time, the inversion mechanism starts rotating. At the position where the inversion mechanism is rotated by 180°, the carriage assembly is fed toward the inner edge of the disc, and passed by the guide of the guide shaft to the carriage shaft (B) then the carriage assembly is moved toward the inner edge of the disc to start playing side B.

Changing from sides B to A is performed in the opposite way.

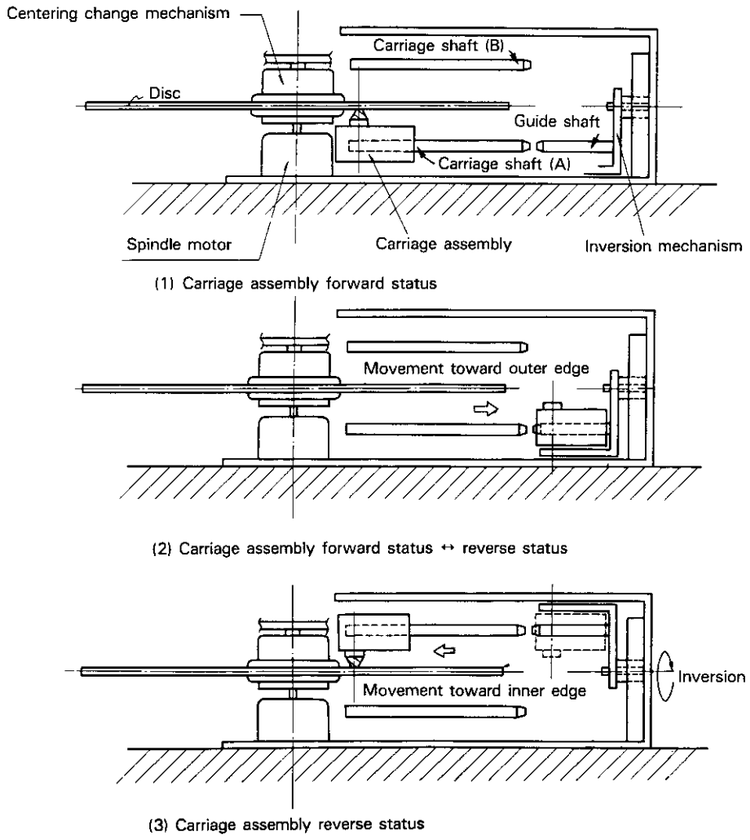


Fig. 11-1-1 Operating principle of "both-sides playback mechanism" (α-turn system)

Fig. 11-1-2 is a diagram showing the outline of the "α-turn" system both-sides playback mechanism. In this system, since the two carriage shafts (A) and (B) are securely fixed along the upper and lower surfaces of the disc, while the guide shaft in the inversion mechanism is located on the same axis with respect to each carriage shaft (A) and (B) when playing both sides A and B, the transition of the carriage assembly can be performed smoothly.

The pickup assembly is located inside the carriage assembly, in which the slider drive mechanism used for the movement of the pickup assembly (it is also used for driving the turn-gear to invert the carriage assembly), tilt drive mechanism and height drive mechanism (described below) are also incorporated.

The above inversion operation is started when the turn gear located at the rear of the carriage section is engaged with the internal gear (sun gear). Then the entire carriage section is turned by 180° by means of the rotation of the turn gear (planetary gear). In this system, the invertion mechanism itself does not have an exclusive drive section.

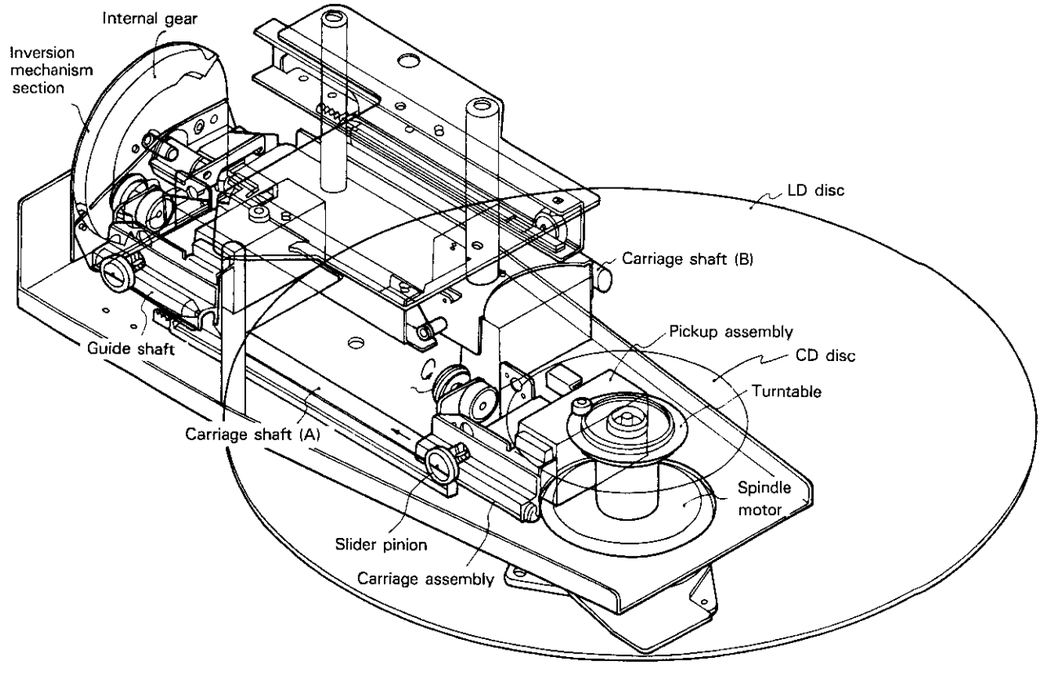


Fig. 11-1-2 Overall diagram of the "Alpha-Turn" both-sides playback mechanism

12. DESCRIPTION OF CLAMPER MECHANISM

12-1. OUTLINE

Eccentricity due to errors when the two sides of the disc are attached may increase time base errors and cause Color Band. Therefore, the centering ability of the clamper mechanism is especially important in a both-sides playback system.

Because of this, the CLD-91 is equipped with a clamper mechanism having an independent centering system for sides A and B and side B of the disc can be played back with the same stability as side A.

12-2 OUTLINE OF OPERATION

In the side A/B independent centering system, the centering hub (B) is pointed inside the disc clamper. Fig. 12-2-1 shows its structure and the operation. In status (2) when side A is clamped, in the same way as in the conventional system, the center of side A is adjusted to the center of the spindle motor by applying the tapered section of the centering hub (A) to the inside of the center hole on side A of the disc so that the disc is clamped to the turntable by the disc clamper.

When playing side B from this condition, the clamper holder which maintains the clamper mechanism is lowered to lower the centering hub (B) located inside the disc clamper. Then, while the centering hub (A) is lowered, the tapered section of the centering hub (B) comes into contact with the inner edge of the center hole on side B of the disc in which there is a displacement between sides A and B. When the clamper holder is further lowered, the centering hub (A) is completely released from the disc while the disc is pressed by the tapered section of centering hub (B). So that this is possible, the disc is held at the center of the spindle motor while it is shifted to the surface of the turntable, then the mechanism goes to status (3).

As described above, the side A/B independent centering mechanism is constructed simply by changing the upper/lower stroke of the clamper and provides the same centering accuracy as the conventional system.

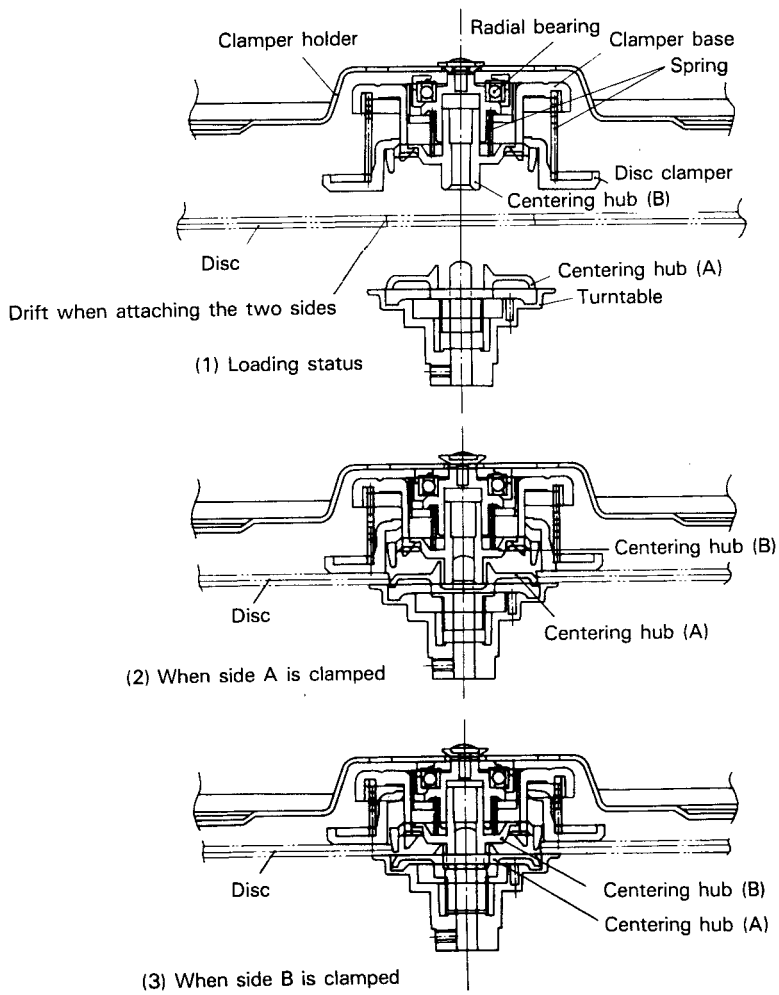


Fig. 12-2-1 Disc clamping mechanism with side A/B independent centering system

13. TILT & HEIGHT SERVO MECHANISM

13-1 OUTLINE OF OPERATION

Fig. 13-1-1 shows a comparison between the conventional tilt mechanism and the newly developed Tilt & Height Mechanism.

Fig. 13-1-2 shows the structure of the Tilt & Height Mechanism.

In this system, since the tilt fulcrum is located on the extension of the center line of the beam axis of the pickup, the light axis angle can be swung by the exclusive tilt drive mechanism. And since this tilt fulcrum is supported by the AF arm, it can also be moved up/down by swinging the AF arm with the exclusive height drive mechanism. The tilt servo is controlled by the output of the tilt sensor which detects the angle of the warpage of the disc so that the laser beam is always emitted at right angles to the disc. The height servo mechanism controls it so that the operating distance (the optimum distance for the focus servo) of the pickup above the disc is always kept at a fixed value.

With the above method, since the angle and displacement can be compensated independently, there will be no residual tilt error with uneven or warped discs while discs are played back with optimum focus servo. Therefore, the optimum pickup performance will be obtained and the playing ability will be greatly improved.

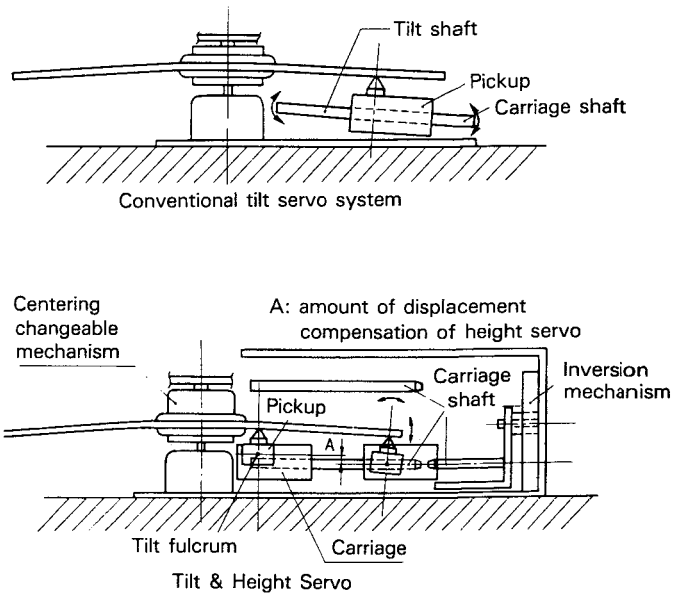


Fig. 13-1-1 Comparison between the conventional tilt servo and the "tilt & height servo"

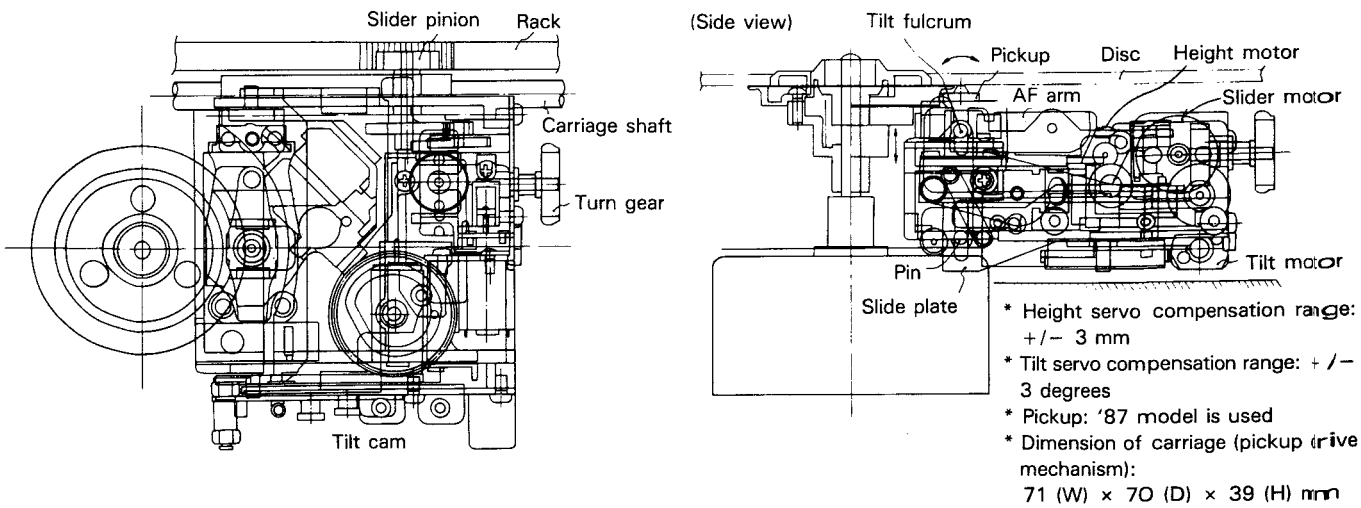


Fig. 13-1-2 Structure of pickup drive mechanism used in both-sides CLD player

13-2 DESCRIPTION OF HEIGHT SERVO

The focus lens focuses the laser beam on the bit surface of the disc to read out the recorded signal. If a warped disc is loaded, normally the lens is moved up and down slightly to position the fulcrum center of the stroke. When the inner area of the disc is being played back, and is moved much more due to the warping of the disc when the outer area is being played back. Therefore, the dynamic range of the lens may become uneven for the top and bottom sides.

To compensate for this, in the conventional system, the slidershaft is rotated while it is swung up and down using the point where the shaft is located as a supporting point to assure the dynamic range of the lens. (Fig. 13-2-1)

As opposed to this, in the Tilt & Height Servo Mechanism, the entire pickup assembly is moved up and down.

The DC component of the current flowing in the focus lens is proportional to the distance from the pickup body (l_2). To operate, this current is converted into voltage E_R by the resistor R_1 and this is used to move the entire pickup assembly up and down by rotating the motor when E_R exceeds a positive or negative fixed value (E_{TH}), so that the focus lens is used within its effective stroke. Fixed value E_{TH} is set at 1/4 of the stroke between the upper and lower limits, considering the operating sensitivity of the lens. (Fig 13-2-2)

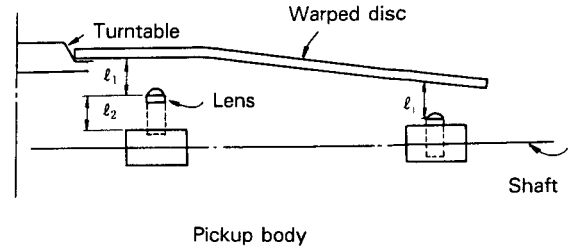


Fig. 13-2-1

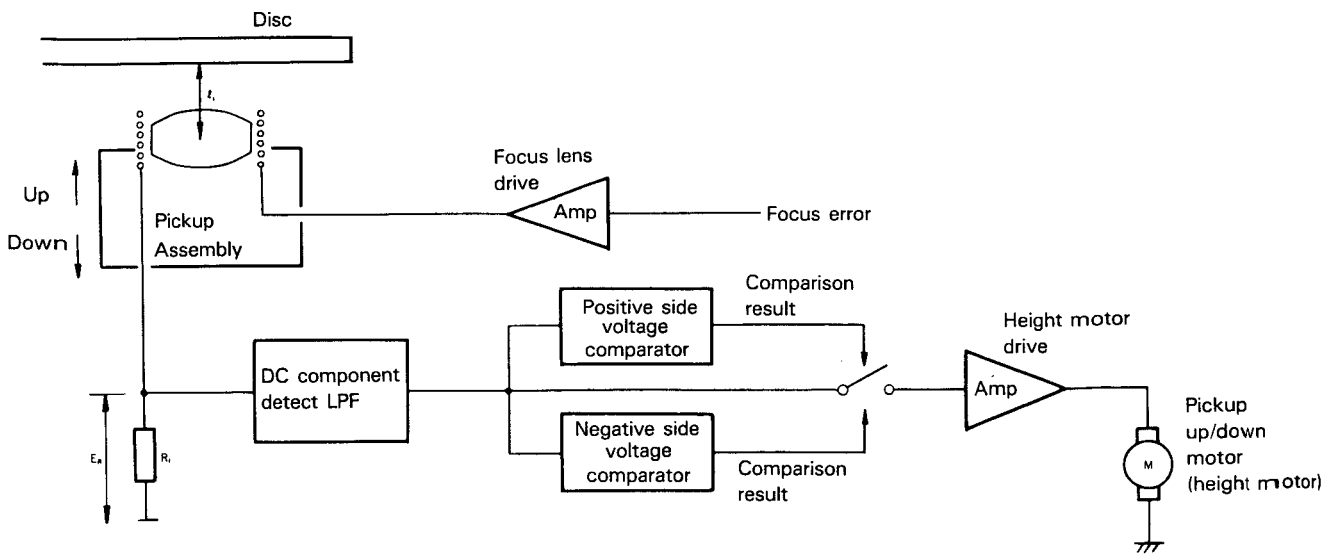
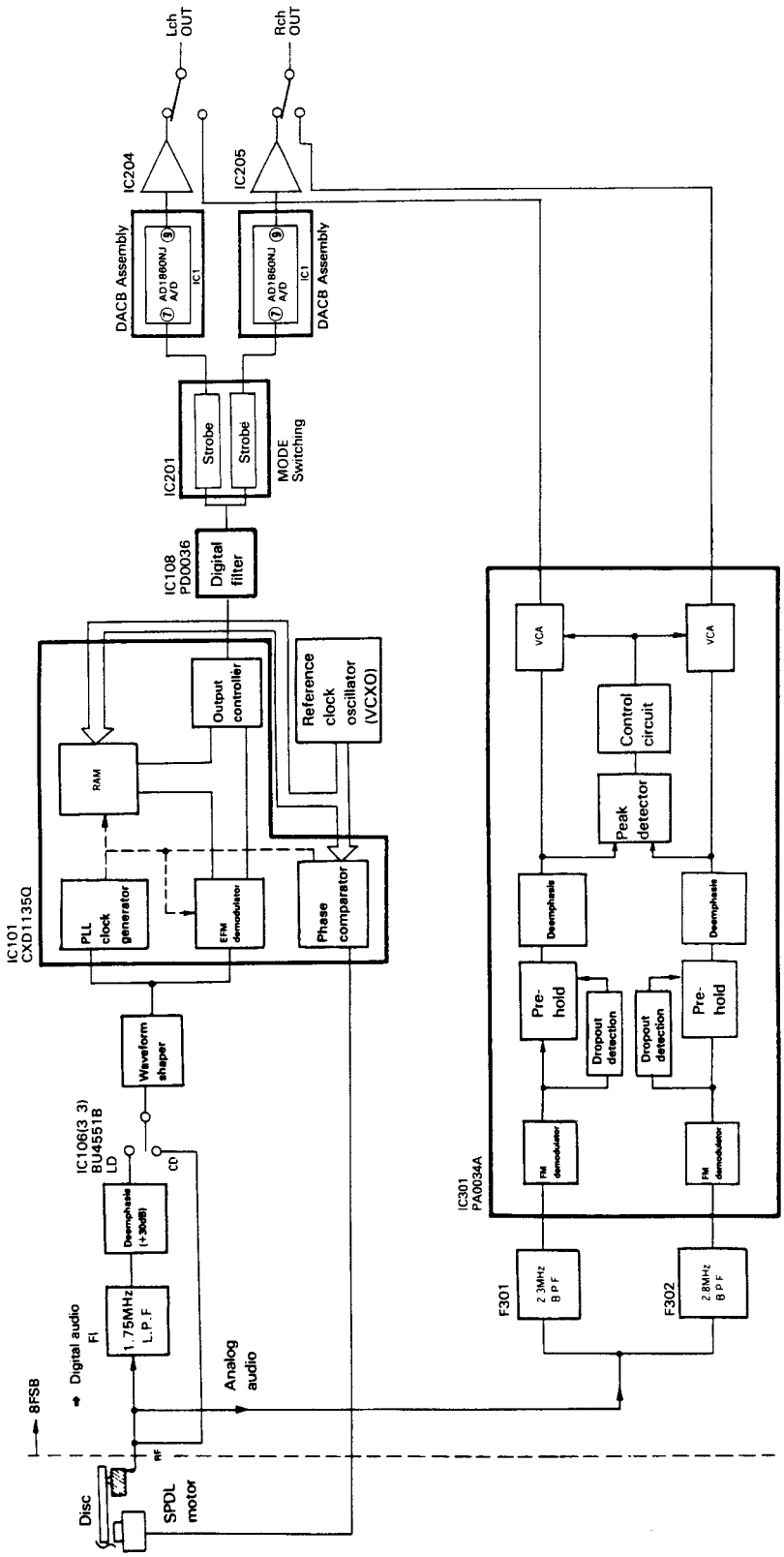


Fig. 13-2-2 Height servo block diagram

14. AUDIO SIGNAL PROCESSING CIRCUIT



Audio Signal Processing Circuit Block Diagram

14-1 OUTLINE

The 8FSB assembly accepts the RF signal from the VSOP assembly and performs the required audio signal processing. The main IC in the analog audio circuit is PA0034 (Audio Demodulation & CX Demodulation), while the main IC in the digital audio circuit is CXD1135Q.

14-2 DESCRIPTION OF PA0034A

After the FM audio signal from the band-pass filters (2.3 MHz for L-channel and 2.8 MHz for R-channel) is demodulated, the resultant signal is passed through the pre-hold circuit, deemphasis circuit and VCA (voltage controlled amplifier), and is then output as the analog audio signal.

If dropout occurs, it is detected by the dropout detector. When dropout is detected, the signal level is maintained at the value immediately before the dropout occurs by the pre-hold circuit, to prevent noise from occurring. Further, CX noise reduction is provided to improve the audio dynamic range as well as the signal-to-noise ratio.

PA0034A is a one-chip IC exclusively for LD audio, and performs the whole of the above signal processing. Fig. 14-2-1 shows the functions of each pin, while the internal block diagram is shown in FIg. 14-2-2.

14.3 DESCRIPTION OF CXD1135Q

CXD1135Q has the following function

1. Generation of the bit clock (PLCK: 4.3218M) by EFM-PLL
2. EFM signal demodulation, error correction and interpolation
3. Frame synch. signal detection, protection and interpolation
4. Subcode signal demodulation and error detection
5. SPDL servo (obligatory deceleration/acceleration, brake, speed servo, phase servo)
6. Zero cross counter for 8-bit tracking error (not found in these models)
7. Double oversampling digital filter (35-stage)
8. Digital audio interphase output

The pin connection diagram of CXD1135Q and its internal block diagram are shown in Fig. 14-3-1.

Item No.	Symbol	Function	Item No.	Symbol	Function
1	VEER	Power supply pin	22	LOUT	L-ch output
2	VINR	FM signal input	23	STC2	STC pin 2
3	BIASR	Input bias	24	STC1	STC pin 1
4	VREFR	Internal reference power supply	25	VCC	Power supply pin
5	GNDR	Ground pin	26	COMP	Compensator pin
6	ALCR	ALC capacitor pin	27	TBC	TBC error signal input pin
7	CSR	Carrier removal pin	28	CINL	CX control signal input
8	DOS2R	DOS2 input	29	CXINL	CX input
9	DEMOR	Demodulator output	30	SWOL	Mode select amp output
10	SINR	Dropout compensator switch input	31	SWINL	Mode select amp input
11	DOCR	Dropout compensator switch output	32	DOCL	Dropout compensator switch output
12	SWINR	Mode select amp input	33	SINL	Dropout compensator switch input
13	SWOR	Mode select amp output	34	DEMOL	Demodulator output
14	CXINR	CX input	35	DOS2L	DOS2 input
15	CINR	CX control signal input	36	CSL	Carrier removal pin
16	R	Mode select pin R	37	ALCL	ALC capacitor pin
17	L	Model select pin L	38	GNDL	Ground pin
18	CX	CX control	39	VREFL	Internal reference power supply
19	FTC	For connection of FTC capacitor	40	BIASL	Input bias
20	GNDCX	Ground pin	41	VINL	FM signal input
21	ROUT	R-ch output	42	VEEL	Power supply pin

Fig. 14-2-1 PA0034 pin functions

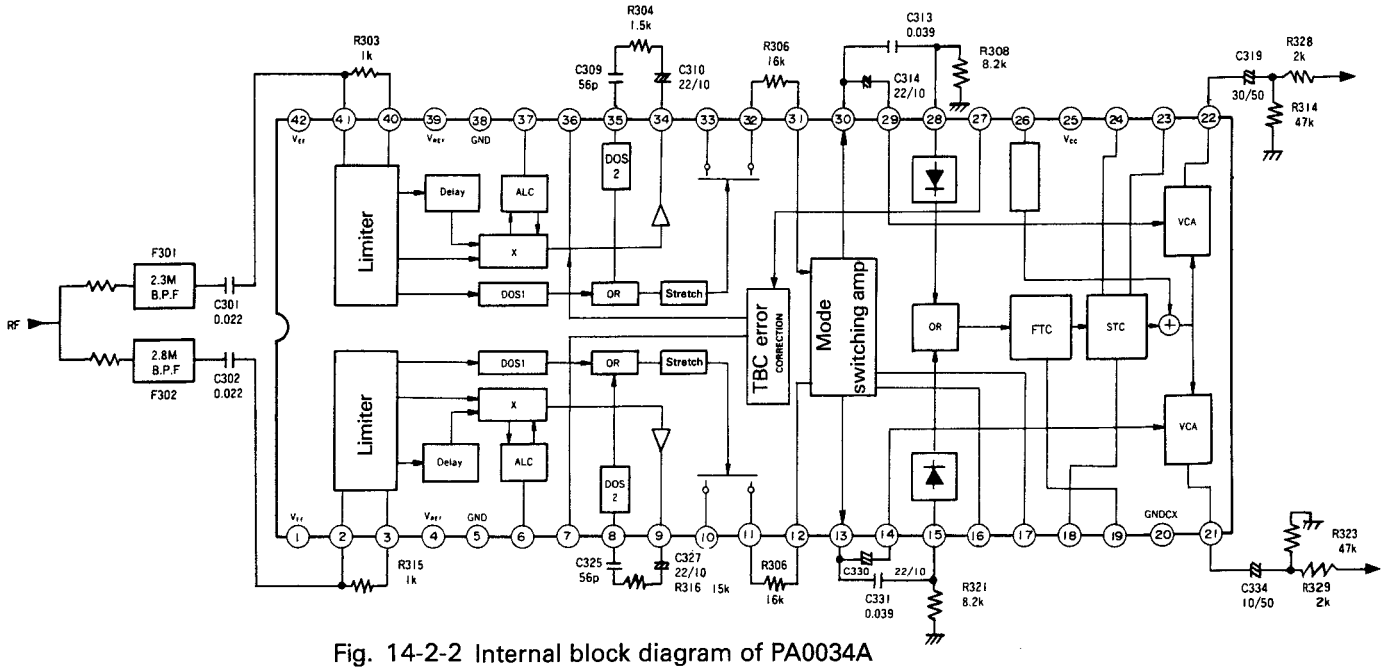


Fig. 14-2-2 Internal block diagram of PA0034A

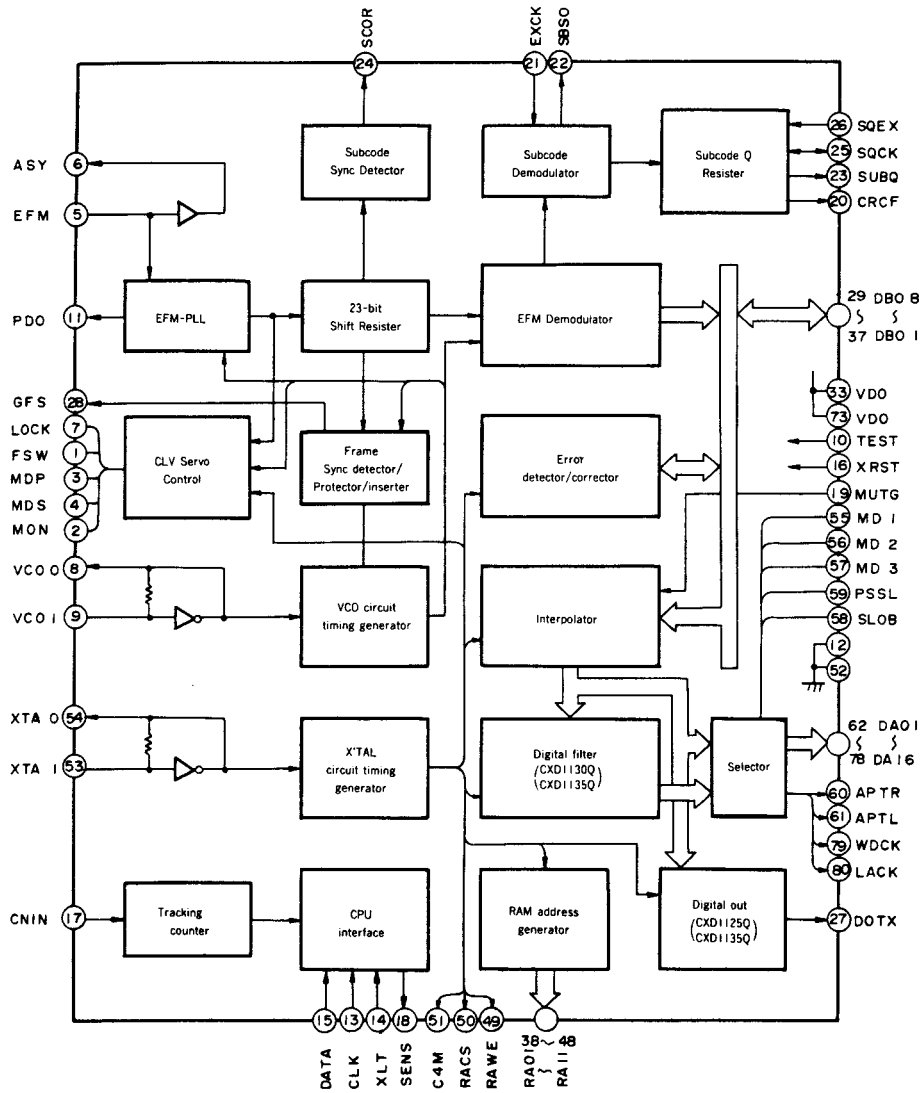


Fig. 14-3-1 Internal block diagram of CXD1135Q

14.4 CXD1135Q COMMAND CODE

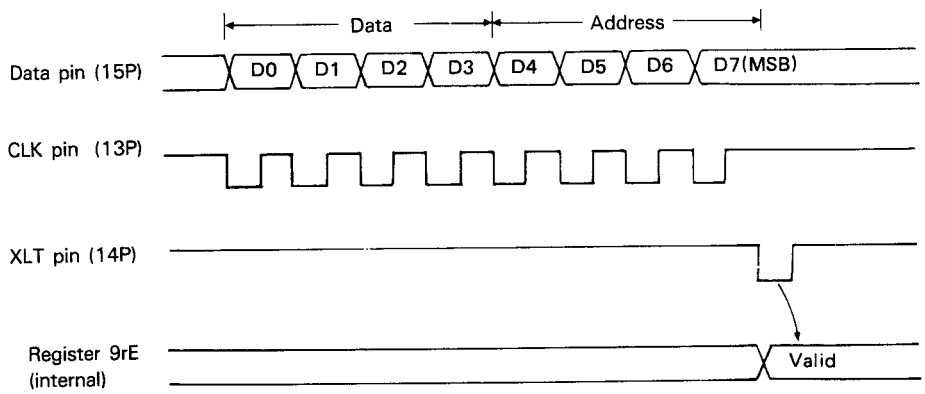
As the table below shows, CXD1135Q has a 4-bit register containing addresses 9 through E. Player operations can be performed by sending 8-bit data (command code) containing address and data (totalling 8-bits) to these addresses.

*Note: FOR STATUS
H: High Level
L: Low Level
High Z or Z: High impedance
P: Pin No. of IC

<Register Chart>

Register Name	Command	Addresses D7 – D4	Data				SENS pin (18P)
			D3	D2	D1	D0	
9	Control of new functions	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A	Synch protection, attenuation control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Lower 4-bits	1011	Tc3	Tc2	Tc1	Tc0	COMPLETE
C	Counter set, Upper 4-bits	1100	Tc7	Tc6	Tc5	Tc4	COUNT
D	CLV control	1101	DIV	Tz	Tp	GAIN	Z
E	CLV mode	1100		CLV mode			Pw ≧ 64

<Data Input Timing Chart>



*After 8-bit data input, the input commands are executed during the time period when XLT is L. Data input timing is the same as in the CXA1082A.

«Information about the Registers»

- **Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero cross MUTE OFF	Zero cross MUTE ON
HZPD	D2	The PDO pin is always active	The PDO pin is Z at the trailing edge of GFS
NCLV	D1	CLV-P servo supported by frame synch signal	CLV-P servo supported by base count
CRCQ	D0	CRCF is not superimposed on SUBQ	At the leading edge of SCOR, SUBQ = CRCF
		(Functions identical to those of the CX23035)	(New functions)

ZCMT: Turns zero cross MUTE ON/OFF.
HZPD: Switches PD output to Hi-Z (ON/OFF) from the trailing edge of the GFS pulse (GFS is H when SPDL LOCK is activated) to a maximum of 0.55nS. (PLCK and play EFM undergo phase comparison, and the PD output controls the VCO.)
NCLV: Switches the SPDL phase servo error detection method when PLL is locked.
CRCQ: Switches the output of CRCF data from the subcode data Qoutput pin, SUBQ, ON/OFF.

If the content of Register 9 is cancelled out by activating POWER ON RESET and none of its commands are active, the IC will function exactly like the CX23035.

• **Register A**

Controls the 4 signals: GSEM, GSEL, WSEL, ATTM.

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

When frame synch detection is not working properly, a dummy frame synch is interpolated, but the number of frames for which interpolation will be performed is fixed: during LD play, 8 frames; during CD play 8 frames; and during SCAN, 13 frames.

WSEL	Clock
0	±3
1	±7

To prevent errors during frame synch detection, a detection window of a certain width is set and synch patterns which fall outside the detection window are ignored.

The width of the detection window is set as follows: (set at ±7 clock)

ATTM	MUTG pin	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

In combination with the MUTG pin (19P), MUTE ON/OFF and the application of -12dB attenuation can be controlled.

In terms of actual command code, $AA is being input. Since A = 1010 and GSEL = 1, GSEL = 0, there are 8 interpolation frames with detection width parameter set at 7 clock.

• **Register D**

DIV	D3	0	RFCK/4 and WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 and WFCK/8	
TB	D2	0	RFCK/32	Bottom hold cycles in CLV-S, CLV-H modes
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold cycle in CLV-S mode
		0	RFCK/2	
GAIN	DO	0	−12dB	MDP pin gain in CLV-S, CLV-H modes
		1	0dB	

RFCK: Read Frame Clock (frequency divided from X'TAL, 7.35k)

WFCK: Write Frame Clock (Frame synch during play EFM)

CLV-P mode: Phase servo which operates when the PLL loop is locked

CLV-S mode: Speed servo which operates when the PLL loop is not locked

CLV-H mode: Speed servo during search (when pickup is moving)

In terms of actual command code, $D4 is being input. Since 4 = 0100, RFCK, WFCK are frequency divided by 4 for phase error, RFCK is frequency divided by 16 for bottom hold in the CLV-S mode, RFCK is frequency divided by 4 for peak hold and MDP pin gain is −12dB.

• **Register E**

		(3P)	(4P)	(1P)	(2P)
Mode	D3−D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	1000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	Z	L	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H
CLV-A'	0101	CLV-S' or CLV-P	Z or CLV-P	L or Z	H

This register sets the operating mode for the SPDL servo. In this mode, the SENS pin, 19P, registers L when the frame sync pulse amplitude detected at CLV-S is over 64T. This output, however, is not utilized.

From commands 0000 to 0110, the system is identical to that of the CX23035.

After the focus servo lock check, actual SPDL start is performed by $E8, i.e., command code 1000 puts the unit into KICK mode which force starts the SPDL. Next, $E6 puts the unit into CLV-A mode which closes the SPDL servo and PLL loop. The lock can be checked by verifying that GFS registers an H.

When stopping, $EA, command code 1010, applies the brake, and after SPDL stop detection at FG, $EO puts the unit into stop mode. Because the CLD-91 has a 8-times oversampling digital filter IC (PD0036), the digital filter in the CXD1135Q is not utilized.

As a digital OUT terminal, the toss link for optical fiber transmission is passed through a buffer and connected to 27P. However, since the function assigned to MODE 0 of the digital OUT IC, 27P is no longer needed for this purpose. Instead, modulated output for the digital audio interface format is obtained from 27P.

ON/OFF for digital filter and OUT functions can be fixed according to the H and L signals from MD1, 2 and 3 of 55, 56 and 57P. On the CLD-91 these are set at L, L, H corresponding to digital, OFF and digital OUT, ON.

14-5 SIGNAL PROCESSING AND CXD1135Q PERIPHERAL CIRCUITRY

The EFM signal passes through the ATC circuit made up of IC501 (TC74HCU04AP) and IC104 (2/2) (NJM082D) and is input to IC101 — 5P (CXD1135Q). The result of phase comparison between EFM and the VCO output of IC104 (1/2) is output from IC101 — 11P and controls the VCO these compose a PLL loop.

IC101 performs SPDL servo error detection from EFM and the output of 1 through 4P is utilized for the SPDL servo. The function of the pins is as follows:

FSW (1P): When the PLL loop is locked, it is High-impedance. At other times it is L level. IC104 (1/2) (NJM082D) is the phase and speed error mix filter, and is used to switch the cut-off frequency. (Hi-Z, 500Hz, L: 20Hz).

MON (2P): When the motor is stopped: L, when rotating: H.

MDP (3P): SPDL phase error when PLL is locked and otherwise, speed error

MDS (4P): Speed error when PLL is locked and, otherwise, Hi-Z

Internal detection of whether PLL is locked or not, is performed at the GFS pin, 28P, which registers H when PLL is locked.

During CD or the audio section of a CDV play, the error signal of IC104 — 8P is input as CD ERR to the absolute value amp for the SPDL servo section from IC106 — 5P (BU4551B) and drives the SPDL motor.

During LDD play or the video section of a CDV, error signal is output from IC106 — 5P to control IC104 VCXO. As a clock signal, VCXO output signal is input to IC101 — 8P. At IC101 the demodulated digital audio data is input as serial data to IC108 (PD0036) along with 80P LRCK (44.1k) and 76P C210 (2.1168M).

IC108 is a 8-times oversampling digital filter.

The CLD-91 utilizes a sub-CPU, IC102 (PDE024), to handle the transmission of 8-bit serial command data to IC101 (CXD1135Q) and the reception of sub-code data from IC101.

IC102 is connected to the main CPU by the 4-bit data bus and by the signal lines ATN, STB and ACK.

However, with the introduction of TOC (ADR = 4) in LDD discs, the reading of the TOC renders processing time too long and it is no longer practical for the main CPU to directly read the data.

For this reason, sub-code data from CXD1135Q is placed in a buffer at IC102 (PDE024) and, in response to a command from the main CPU, is transmitted by 4-bit bus. In addition, command code destined for CXD1135Q is input through IC102.

On the basis of data received from CXD1135Q and the main CPU, IC102 performs digital/analog switching, LD/CD switching and Emphasis ON/OFF.

Another function of IC102 is to output LSEL and RSEL signals used for switching Left/Right channels during LDD play:

	Both CH	RCH only	LCH only
LSEL	L	L	H
RSEL	L	H	L

14-6. DESCRIPTION OF PD0036 (8-TIMES OVERSAMPLING DIGITAL FILTER)

Fig. 14-6-1 shows the internal block diagram of PD0036 and Fig. 14-6-2 shows its pin functions.
Fig. 14-6-3 shows the concepts of each oversampling operation.

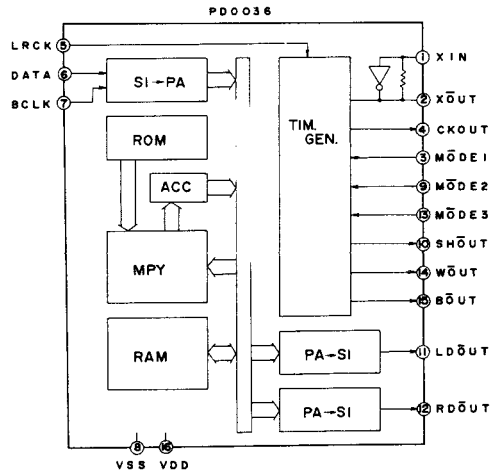


FIG. 14-6-1 PD0036 Internal Block Diagram

Pin No.	Symbol	Pin Name	I/O	Function
1	XIN	XIN	Input	Crystal oscillator input or external input
2	XOUT	XOUT	Output	Crystal oscillator output
3	MODE1	MODE1	Input	High: 16.9344 MHz, Low: 8.4672 MHz
4	CKOUT	CLOCK OUT	Output	MODE1 = High: 16.9344 MHz clock output MODE1 = Low: 8.4672 MHz clock output
5	LRCK	LR CLOCK	Input	L/R clock input
6	DATA	DATA	Input	Serial data input (2's complement, MSB first)
7	BCLK	BIT CLOCK	Input	Bit clock input for input data
8	VSS			GND pin
9	MODE2	MODE2	Input	MODE2 = High: Outputs 18-bit data MODE2 = Low: Outputs 16-bit data
10	SHOUT	SHOUT	Output	Sample & hold pulse output
11	LDOUT	Lch DATA OUT	Output	L-channel data output (2's complement, MSB first)
12	RDOUT	Rch DATA OUT	Output	R-channel data output (2's complement, MSB first)
13	MODE3	MODE3	Input	MODE3 = High: Outputs 16-bit or 19-bit data MODE3 = Low: Outputs 20-bit data
14	WOUT	WOUT CK OUT	Output	Word clock output
15	ROUT	BIT CK OUT	Output	Bit clock output for LDOUT, RDOUT
16	VDD			+5 V power supply pin

Fig. 14-6-2 PD0036 Pin Functions

14-7. DESCRIPTION OF AD1860NJ (18-BIT D/A CONVERTER)

Fig. 14-7-1 and Fig. 14-7-2 show pin functions and the internal block diagram.

Input		Data Input				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

FIG. 14-7-1 AD1860NJ Pin Functions

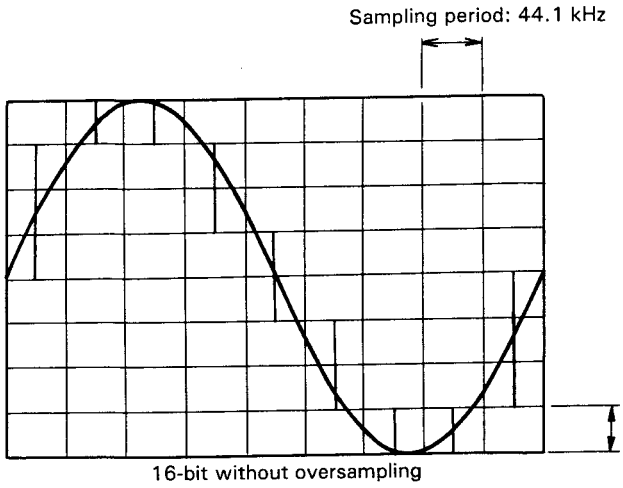


FIG. 14-6-3 Oversampling Concept

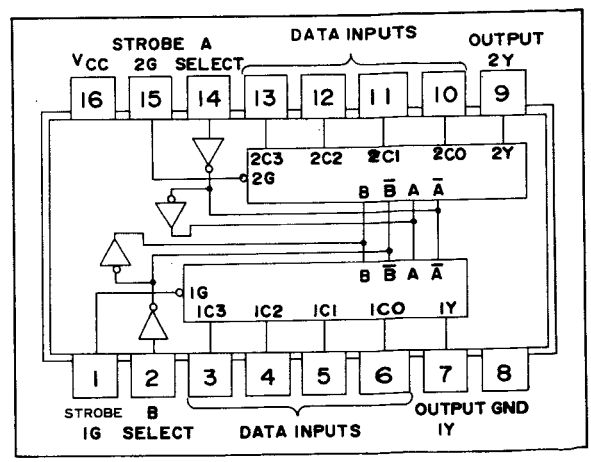
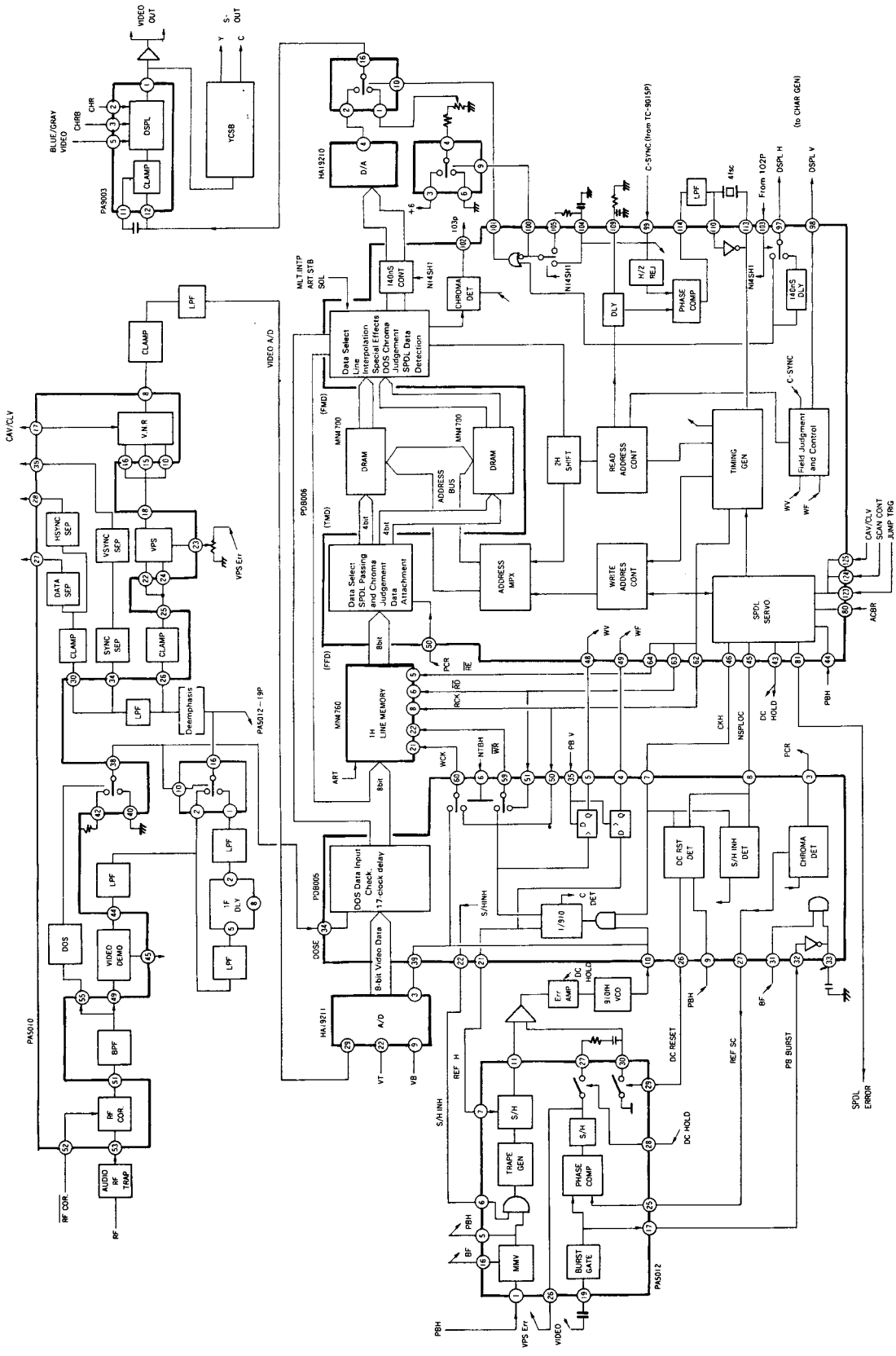


FIG. 14-7-2 AD1860NJ Internal Block Diagram

15. VIDEO SIGNAL PROCESSING SYSTEM



15.1. OUTLINE

The pickup of this model incorporates a unitized IC (PA0032) containing both photodetectors and head amp section. After gain adjustments have been made on the FTSB board, the RF output of PA0032 is input to the PA5010 (Video signal processor) of VSOP assembly and is processed.

15-2 DESCRIPTION OF PA5010 (VIDEO SIGNAL PROCESSOR)

PA5010 has the following functions.

- RF signal correction
- Video signal demodulation
- Dropout detection/Video correction SW
- EFM amp
- V-H synch and data separation
- VPS (Video Phase Shifter)
- VNR (Video Noise Reduction)
- Blue background SW and squelch
- Screen display
  (when video memory is OFF or when using blue background screen)

The pin connection diagram of PA5010 and its internal block diagram are shown in Fig. 15-2-1 and Fig. 15-2-2 respectively.

With video that passes through memory, unless the characters (screen display) are inserted before the 140nS (equivalent to one half the cycle of the sub-carrier) shift circuit that is used to maintain sub-carrier continuity between frames (every successive frame undergoes phase inversion). Because only the characters on screen will not be 140nS shifted.

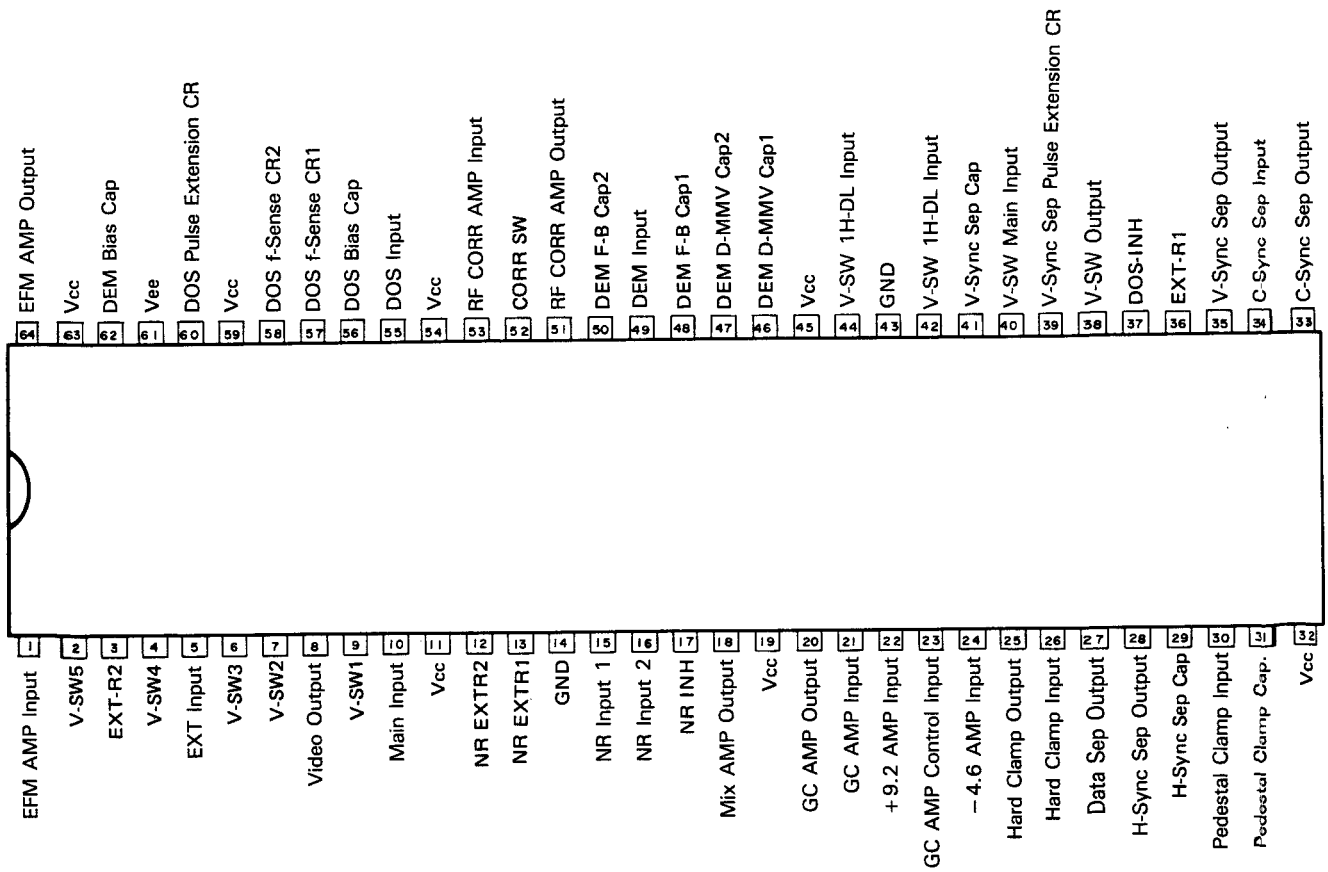


Fig. 15-2-1 PA5010 Pin Connections

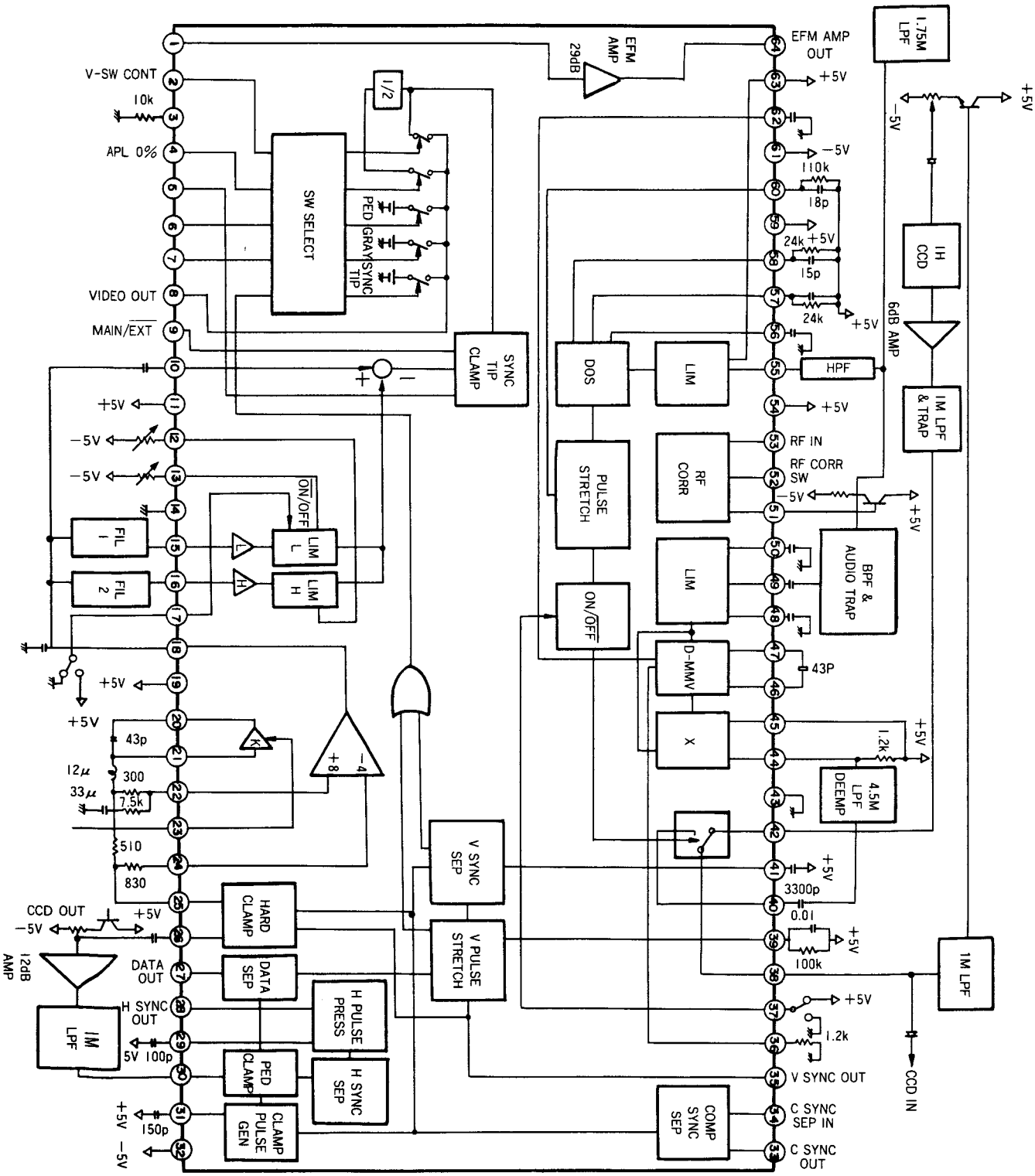


Fig. 15-2-2 PA5010 internal block diagram

15-3. DESCRIPTION OF VIDEO MEMORY SYSTEM

The signal reproduced by the pickup assembly is demodulated to a video signal by PA5010 in the VSMB assembly, then A/D-converted to 8-bit 4fc digital video data by HA19211NT.

While in digital form, the time base of the video data is corrected (digital TBC) by the line memory (MN4700), and sync-conversion is performed by writing to and reading from field memory (MN4700 x 2 = 2M bits) so that trick play is possible with CLV discs.

Writing to and reading from field memory (MN4700) is performed by PDB006.

The video signal the time base of which has been corrected and processed in various ways is converted a digital signal into an analog signal by HA19510 (D/A conversion), and after the H-sync (horizontal sync signal) is inserted, it is output as the player's video output signal from PA5010.

In the whole system, other than the digital video data processing mentioned above, writing clock for the digital TBC is generated by means of PDB005, PA5012 and VCO (Voltage-Controlled Oscillator), while the spindle error signal is generated by PDB006, etc.

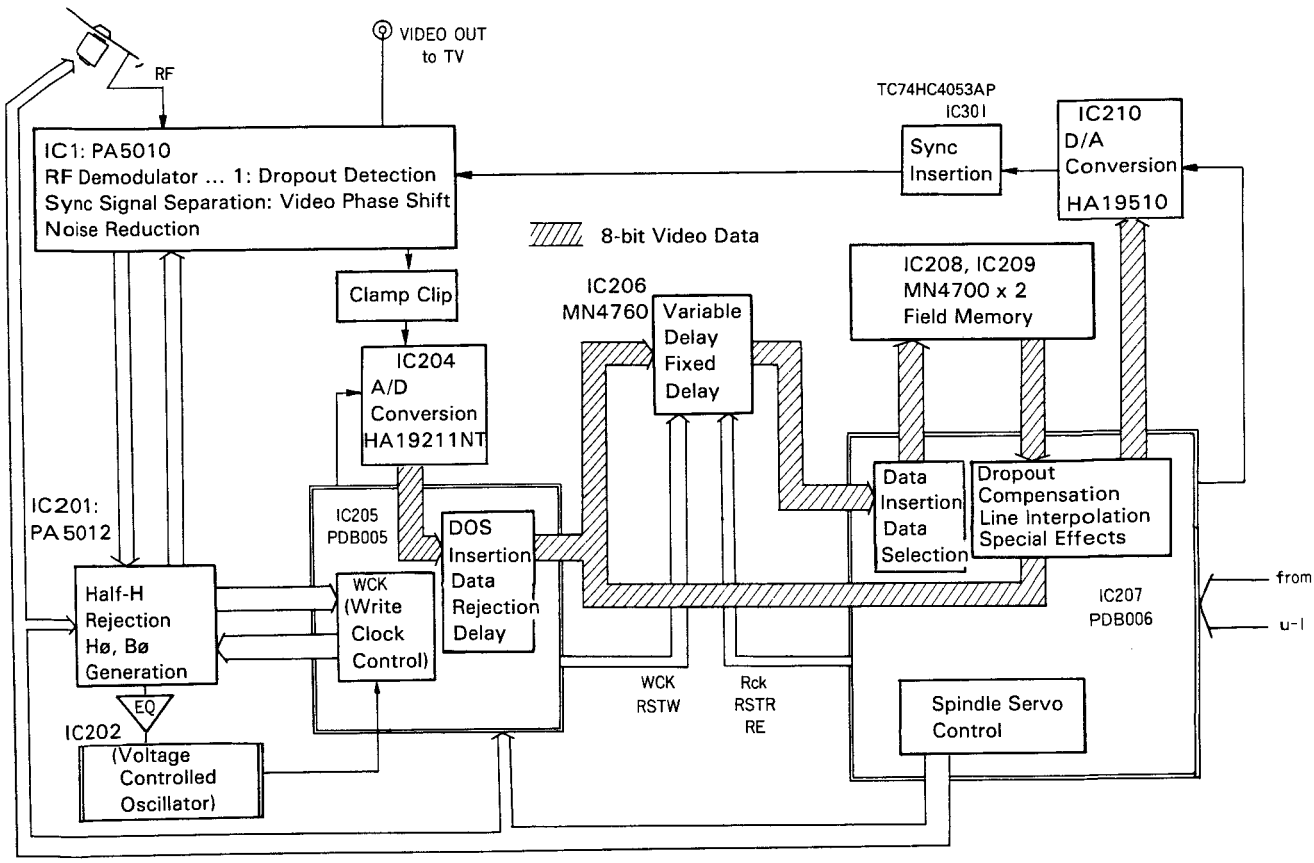


FIG. 15-3-1 Video Memory System Diagram (VSOP Assembly)

15-4. DESCRIPTION OF PDB005, PDB006

The basic specifications of PDB005 and PDB006 are shown in Fig. 15-4-1.

(1) PDB005 Functions

- Insertion of DOS (Dropout Sense Data)
- Write clock control
- Chroma judgement of playback video signal
- Field judgement of playback video signal
- Writing start control of line memory

Fig. 15-4-2 shows the internal block diagram of PDB005, while Fig. 15-4-3 shows its pin functions.

(2) Outline

PDB005 operates on the basis of the writing clock which follows the time base error of the demodulated video signal. The video signal demodulated by PA5010 is A/D converted into 8-bit video data, then quantized and applied to pin 47 (DI0) - pin 40 (DI7) so that it is delayed by 17 clock pulses, and output to pin 52 (DO0) - pin 64 (DO7). As dropout compensation (DOC) is performed during this time, the DOS (dropout sense) data is multiplexed. The DO (dropout) output is controlled by pin 6 (NTBH) and goes high-impedance in the line interpolation mode.

The 1/910 counter generates the reference signal (TSS) for the trapezoid signal which is generated at PA5012 by dividing the writing clock, and is also used as the reference signal to generate the RSTW signal which controls the write start point of the line memory and the "560 ns detection window" which is used to set the lock point timing of the VCO (Voltage Controlled Oscillator) loop.

For chroma judgement, the burst signal of the demodulated video signal is input and its polarity is detected in every 1H periods and output to pin 3 as the PCR signal. At the same time, the VSYNC (vertical sync) signal of the demodulated video signal is input to pin 35 (PV) to generate the WV signal latched by RSTW to be output to pin 5 and the field judgement (WF) signal to be output to pin 4.

Other than above, PDB005 generates the SHINH signal to be output to pin 22 which inhibits the sample & hold of the trapezoid signal at PA5012, and the DCREST signal to be output to pin 26 which resets the DC error of the burst signal.

Silicon CMOS 1.5 um two-layer aluminum wiring standard cell

	PDB005	PDB006
Package	64-pin plastic flat package	148-pin plastic flat package
No. of gates	Approx. 1,500 gates	Approx. 5,000 gates
Power voltage	+5V±10%	+5V±5%
Operating temperature	−40~+70°C	−40~+70°C
Current consumption	50mA	94mA

FIG. 15-4-1 Basic Specifications of PDB005, PDB006

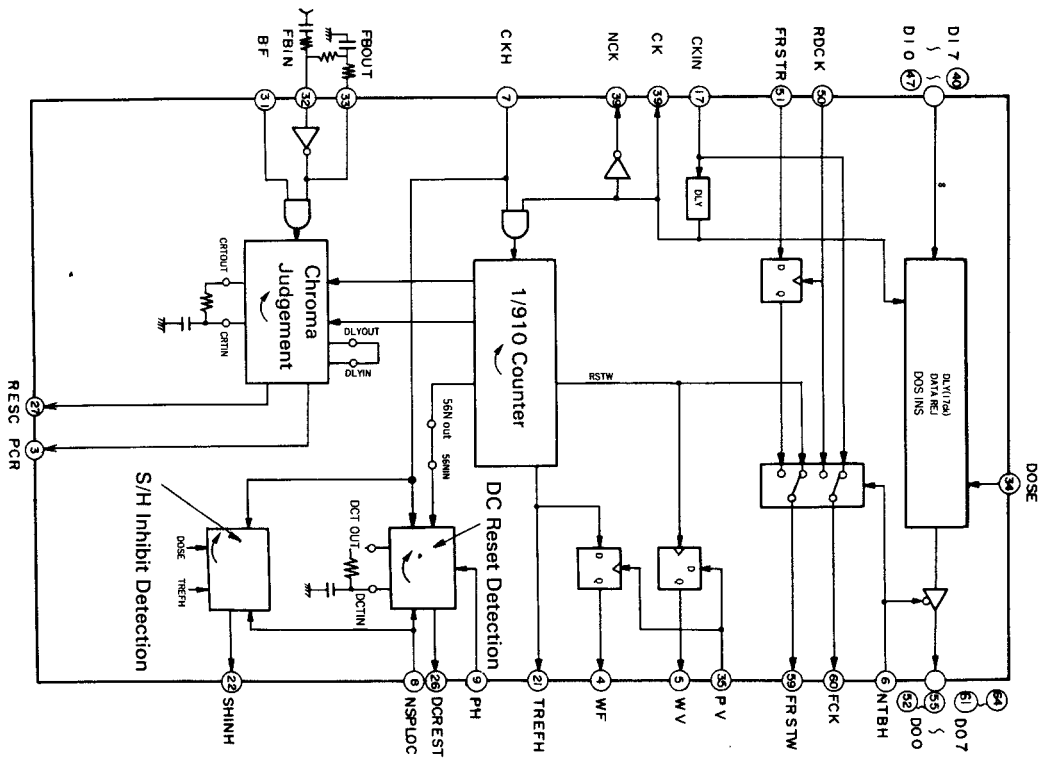


Fig. 5-4-2 PDB005 Internal Block Diagram

Pin No.	I/O	Pin Name	Function	
1	I	56NIN	560N window input	
2	O	56NOUT	560N window output	
3	O	PCR	Playback chroma judgement signal output	
4	O	WF	Playback field judgement signal output	Odd: High
5	O	WV	Playback vertical sync signal output	
6	I	NTBH	When line memory is in 1H fixed mode:	High input
7	I	CKH	Write counter hold signal input	Hold: High
8	I	NSPLOC	SPDL lock input	Lock: Low
9	I	PH	Playback horizontal sync signal input	
10	I	CKIN	Write clock input	
11	O	QOUT	D-latch output	
12	I	LAT	D-latch clock input	
13	I	DIN	D-latch data input	
14	I	SEL	Test input	
15	I	TESTIN	Test input	
16	I	DCTIN	Write position detection time constant input	
17	O	DCTOUT	Write position detection time constant output	
18	O	NOUT	NAND output	
19	I	NIN2	NAND input 2	
20	I	NIN1	NAND input 1	
21	O	TREFH	T.S.S. output (trapezoid signal starts at the falling edge)	
22	O	SHINH	Inhibits sampling of the H error signal	Inhibit: Low
23	I	RESET	Test input	
24		VSS	GND	
25		VDD	+ 5 V	
26	O	DCREST	Burst DC error reset	Reset: High
27	O	RESC	Reference SC output	
28	O	DLYOUT	Reference SC (time constant) output	
29	I	DLYIN	Reference SC (time constant) input	
30	O	REFMON	Reference SC monitor output	
31	I	BF	Burst flag input	
32	I	FBIN	Playback burst input	
33	O	FBOUT	Playback burst amp output	
34	I	DOSE	Dropout signal input	Dropout: High
35	I	PV	Playback vertical sync signal input	
36		VDD	+ 5 V	
37		VSS	GND	
38	O	NCK	Write clock invert output	
39	O	CK	Write clock output	
40	I	D17	Video data input from A/D converter (MSB)	
41	I	D16	Video data input from A/D converter	
42	I	D15	Video data input from A/D converter	
43	I	D14	Video data input from A/D converter	
44	I	D13	Video data input from A/D converter	
45	I	D12	Video data input from A/D converter	
46	I	D11	Video data input from A/D converter	
47	I	D10	Video data input from A/D converter (LSB)	
48	I	CRTIN	Chroma judgement time constant input	
49	O	CRTOUT	Chroma judgement time constant output	
50	I	RDCK	Read clock input	
51	I	FRSTR	Line memory read reset input	
52	O	DO0	Video data output to line memory	
53	O	DO1	Video data output to line memory	
54	O	DO2	Video data output to line memory	
55	O	DO3	Video data output to line memory	
56		VDD	+ 5 V	
57		VSS	GND	
58			–	
59	O	FRSTW	Line memory write reset output	
60	O	FCK	Write clock output to line memory	
61	O	DO4	Video data output to line memory	
62	O	DO5	Video data output to line memory	
63	O	DO6	Video data output to line memory	
64	O	DO7	Video data output to line memory (MSB)	

Fig. 5-4-3

(3) PDB006 Functions

- Color dropout compensation
- Line interpolation
- Special effects (multi-screen, art 1, 2, after-image screen (one-shot memory), dual screen, solarization)
- Field memory control
- Line memory read start control
- Spindle error generation
- Field control
- Digital 140 ns shift
- VCXO (voltage controlled crystal oscillator)

Fig. 15-4-5 shows the internal block diagram of PDB006 while Fig. 15-4-6 shows its pin functions.

(4) Outline

PDB006 incorporates a VCXO which locks to the external sync generator to control the crystal oscillator connected to pin 110 (CKIN) and pin 113 (CKOUT) by the PDO output (phase error) at pin 114.

The phase error signal at pin 114 (PDO) is generated by comparing the SGEH signal which is made by subtracting the equivalent pulse from the sync generator signal input to pin 99 (SGEC), with the HBL signal which is generated by the R-address counter determining the read address from the field memory and output at pin 95 then passed through DLCR of pin 109, in the PD section. PDB006 operates using the read clock as the above VCXO output as a reference signal.

PDB006 provides 5 lines of inputs and outputs for video data.

The video data, with its time base (axis) compensated by the line memory (MN4760), is input to pin 68 (FFD0) through pin 58 (FFD7), and the shift data which indicates the chroma judgment signal and that it has passed is inserted. After the shift data is inserted, the video data is output from pin 29 (TMD0) through pin 15 (TMD7), then written into the field memory (MN4760). The video data read from the field memory is input to pin 33 (FMD0) through pin 22 (FMD7), and the chroma judgement and shift data which has been inserted in the video data is detected. Also the processing required for line interpolation or various special effects are performed, and output to pin 90 (OD0) through pin 87 (OD7) then applied to digital/analog converter IC. The video data output from the D/A converter IC is divided into two; one part of the signal is delayed by 2 clock pulses (140 ns) at pin 103 (N14SH1) and other part of the signal is not delayed; the output video signal delayed by 140 ns is processed digitally.

Pin 72 (TFD0) through pin 51 (TFD7) are connected to the input of the line memory, and are at high impedance normally. But in line interpolation mode, the video data output DO0 - DO7 of PDB005 goes high impedance while TFD0 - TFD7 go active so that the video data read from the field memory can be output to the line memory. That is, the line memory is used as the variable delay line for the TBC and also as a 1H fixed delay line for line interpolation.

In the spindle control section, the spindle error and spindle lock signals are generated, and the CKH signal which performs the reference shift of the VCO loop and the DCHOLD signal which maintains the burst DC error at PA5012 are output.

In the 1/8-divider section, the WE (write enable), RS (read select)/WS (write select), CE (chip enable) signals are generated, and the H-address clock for write and read sides are also generated. Also, the memory is controlled so that writing the 14 MHz data to the field memory in which the addresses are separated for every 8 clock pulses is interrupted for 6 clock pulses every 1H period.

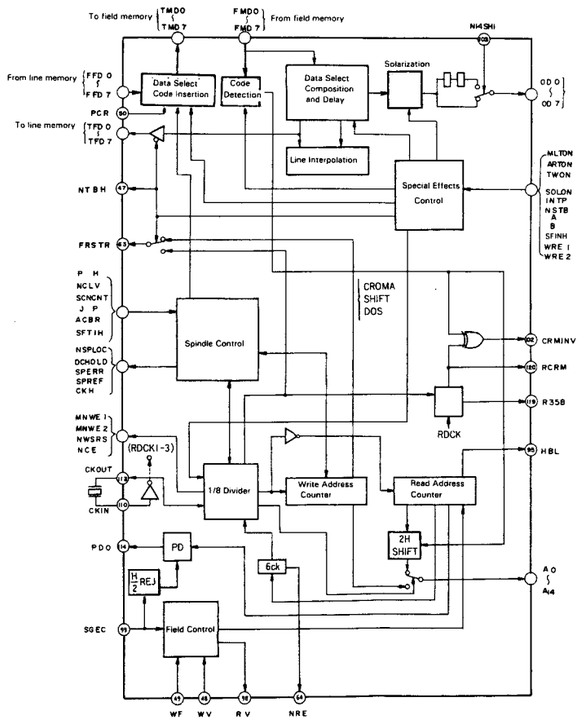


Fig. 15-4-5 PDB006 Internal block diagram

Pin No.	I/O	Pin Name	Function
1			NC (Not connected)
2		VSS	GND (Ground)
3	O	A7	Read/write V address time-division output
4	O	A6	Read/write H address time-division output
5	O	A5	Read/write H address time-division output
6	O	A4	Read/write H address time-division output
7	O	A3	Read/write H address time-division output
8	O	A2	Read/write H address time-division output
9	O	A1	Read/write H address time-division output
10	O	A0	Read/write H address time-division output
11	O	NCE	Field memory chip enable
12	O	MNWE2	Field memory 2 write enable (LSB)
13	O	MNWE1	Field memory 1 write enable (MSB)
14	O	NWSRS	Field memory read/write strobe
15	O	TMD7	Write video data to field memory (MSB
16	O	TMD6	Write video data to field memory
17	O	TMD5	Write video data to field memory
18		VDD	+ 5 V power supply
19	O	TMD4	Write video data to field memory
20		VSS	GND (Ground)
21	O	RDCK1	4Fsc output
22	I	FMD7	Video data read from field memory (MSB)
23	I	FMD6	Video data read from field memory
24	I	FMD5	Video data read from field memory
25	I	FMD4	Video data read from field memory
26	O	TMD3	Write video data to field memory
27	O	TMD2	Write video data to field memory
28	O	TMD1	Write video data to field memory
29	O	TMD0	Write video data to field memory (LSB)
30	I	FMD3	Video data read from field memory
31	I	FMD2	Video data read from field memory
32	I	FMD1	Video data read from field memory
33	I	FMD0	Video data read from field memory (LSB)
34	O	SPREF	Spindle reference output
35	I	SFTIH	Reference shift inhibit input — Inhibit: High
36	I	CRO	Spindle lock detection time constant input
37			NC (Not connected)
38			NC (Not connected)
39		VSS	GND (Ground)
40	O	CRI	Spindle lock detection time constant output
41	O	TMON3	Test output [SGEH: S.G 1/2H rejection output]
42	O	WVCLK	Write V address clock output
43	O	DCHOLOD	Burst DC error hold — Hold: High
44	I	PH	Playback horizontal sync signal input
45	O	NSPLOC	Spindle lock output — Lock: Low

Fig. 15-4-6 PDB006 Pin functions

Pin No.	I/O	Pin Name	Function
46	O	CKH	Write counter hold signal output Hold: High
47	O	NTBH	When line memory is 1H fix mode: High
48	I	WV	Playback vertical sync signal input (from PDB005)
49	I	WF	Playback field judgement signal input
50	I	PCR	Playback chroma judgement signal input
51	O	TFD7	Video data output to line memory (1H fix mode)
52	O	TFD6	Video data output to line memory (1H fix mode)
53	O	TFD5	Video data output to line memory (1H fix mode)
54	O	TFD4	Video data output to line memory (1H fix mode)
55		VSS	GND (Ground)
56	I	ART	Write area control input Write enable: High
57		VDD	+ 5 V power supply
58	I	FFD7	Video data output to line memory (MSB)
59	I	FFD6	Video data output to line memory
60	I	FFD5	Video data output to line memory
61	I	FFD4	Video data output to line memory
62	O	RDCK2	4Fsc output
63	O	FRSTR	Line memory read reset
64	O	NRE	Line memory read enable Enable: Low
65	I	FFD3	Video data output to line memory
66	I	FFD2	Video data output to line memory
67	I	FFD1	Video data output to line memory
68	I	FFD0	Video data output to line memory (LSB)
69	O	TFD3	Video data output to line memory (1H fix mode)
70	O	TFD2	Video data output to line memory (1H fix mode)
71	O	TFD1	Video data output to line memory (1H fix mode)
72	O	TFD0	Video data output to line memory (1H fix mode)
73		VDD	+ 5 V power supply
74			NC (Not connected)
75			NC (Not connected)
76		VSS	GND (Ground)
77	I/O	ODCR	DC hold signal detection time constant I/O
78	O	TMON1	Test output [WV2: write V address 2 output]
79	O	TMON2	Test output [RV2: read V address 2 output]
80	I	ACBR	Acceleration/deceleration signal input Acceleration/deceleration: High
81	O	SPERR	PWM spindle error output
82	O	DFH	1/128 Fsc input
83	O	OD7	Video data output (MSB)
84	O	OD6	Video data output
85	O	OD5	Video data output
86	O	OD4	Video data output
87	O	OD3	Video data output (MSB)
88	O	OD2	Video data output
89	O	OD1	Video data output
90	O	OD0	Video data output (LSB)

Pin No.	I/O	Pin Name	Function	
91	O	RDCK3	4Fsc output	
92		VSS	GND (Ground)	
93	I	CKINV	RDCK 3 output select control input	INV: High
94		VDD	+ 5 V power supply	
95	O	HBL	H-blanking output	
96	I	HBLRTN	H-blanking return input	
97	O	HBLS	140Nsec shift H-blanking output	
98	O	RV	Read field timing output	
99	I	SGEC	S.G C-sync input	
100	O	CSYNC	140Nsec shift S.G C-sync output	
101	O	CBL	H-V sync insert control output	
102	O	CRMINV	140Nsec shift control input	
103	I	N14SHI	Digital 140Nsec shift control input	2-clock delay: High
104	O	SGCSOT	S.G C-sync output	
105	I	SGCSIN	140Nsec delay S.G C-sync input	
106	I	CLR1	Test input	
107	I	CLR2	Test input	
108	I	HIZ	Test input	
109	I/O	DLCR	Read position adjustment time constant I/O	
110	I	CKIN	VCXO oscillator input	
111			NC (Not connected)	
112			NC (Not connected)	
113	O	CKOUT	VCXO oscillator output	
114	O	PDO	VCXO error output	
115	I	MD1	Test input	
116	I	MD2	Test input	
117	I	MD3	Test input	
118	I	NRVSIH	Address shift inhibit input	Inhibit: High
119	O	R358	Read side 3.58 MHz output	
120	O	RCRM	Read side chroma judgement signal output	
121	O	WFMON	Write side field judgement signal output	Odd: High
122	O	RFMON	Read side field judgement signal output	Odd: High
123	I	JP	Jump trigger input	
124	I	SCNCNT	Scan control input	
125	I	NCLV	CAV/CLV input	CLV: Low
126	I	WRE1	Field memory 1 write control input	Write enable: High
127	I	WRE2	Field memory 2 write control input	Write enable: High
128	I	A	Multi/Bit parameter input	
129		VDD	+ 5 V power supply	
130	I	SFINH	Art/Multi inhibit input	Inhibit: High
131		VSS	GND (Ground)	
132	I	B	Multi/Bit parameter input	
133	I	MLTON	Multi control input	Multi mode: High
134	I	ARTON	Art control input	Art mode: High
135	I	TWON	Dual-screen control input	Dual-screen mode: High

Pin No.	I/O	Pin Name	Function
136	I	ZNZON	After-image picture control input — After-image picture : High
137	I	SOLON	Solarization control input — Bit mode: High
138	I	INTP	Interpolation control input — Interpolation mode: High
139	I	NSTB	Special effects playback control signal strobe input
140	O	A14	Read/write V address time-division output
141	O	A13	Read/write V address time-division output
142	O	A12	Read/write V address time-division output
143	O	A11	Read/write V address time-division output
144	O	A10	Read/write V address time-division output
145	O	A9	Read/write V address time-division output
146	O	A8	Read/write V address time-division output
147		VDD	+ 5 V power supply
148			NC (Not connected)

15-5. DIGITAL TIME BASE CORRECTOR

15-5-1 Outline

The structure of the digital time base corrector is shown in Fig. 15-5-1, while its operation concept is shown in Fig. 15-5-2. For comparison, the operation concept of the conventional (analog) time base corrector is shown in FIg. 15-5-3.

In the analog TBC (time base corrector), the video signal containing time base errors (jitter) is transferred sequentially to the CCD delay device, while the clock rate is varied according to the time base error to change the transfer speed (rate) so that time base errors are absorbed.

In this way, the analog delay device absorbs time base errors by varying the delay time, however, since the frequency response of the video signal changes according to the clock frequency, it is inevitable that the video signal will be slightly degraded. With a video signal including a large amount of time base error, especially the color signal may be affected greatly, and the picture may flicker depending on the monitor TV used. For this reason, this unit employs a digital time base corrector which has advantages over an analog TBC in its absorption of time base errors.

The digital TBC section of this unit is shown in Fig. 15-5-5.

The 1H line memory for digital data is used as the delay device to absorb time base errors.

The digital data containing time base errors which has been converted from analog to digital is written into the 1H line memory with the write clock having the same time base error, and read from the 1H line memory using the stabilized clock with a fixed period to absorb time base errors.

In this way, when the digital data is used for the absorption of time base errors, there is no signal deterioration in the delay device stage while the video signal output is stabilized. In the analog system, as shown in Fig. 15-5-4, since the delay device is located within the TBC servo loop, the phase of the servo loop may tend to be delayed and only a small margin can be applied, so time base errors may not be compensated completely.

On the other hand, in the digital TBC, since the delay device is not provided within the TBC loop and a large amount of margin can be applied, a greater amount of residual jitter can be eliminated while a picture with less color shading is obtained.

PDB005 mainly controls the VCO (voltage controlled oscillator) used to generate the write clock. PDB006 controls the VCXO to generate the read clock used to read the video data from the field memory, and generates the spindle error.

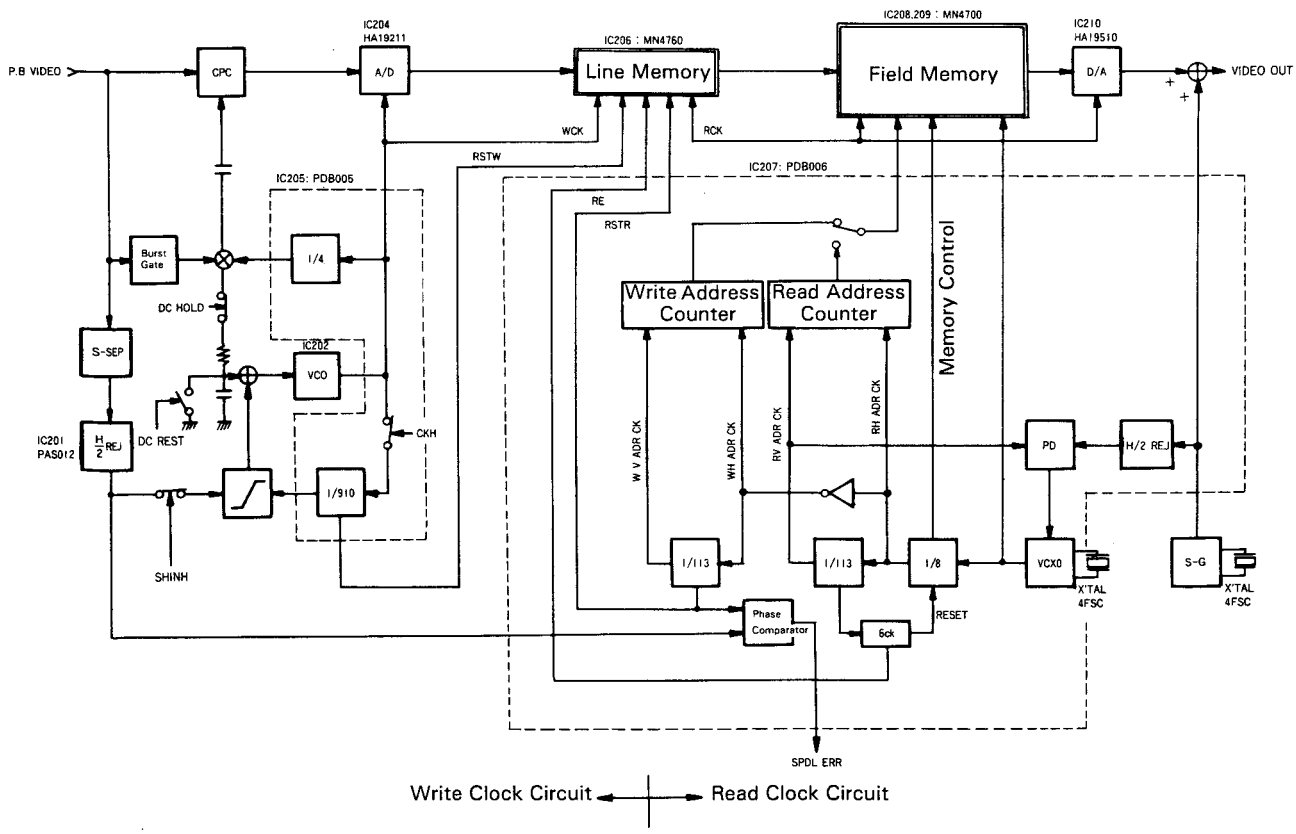


FIG. 15-5-1 Digital TBC Structure (VSOP Assembly 2/2)

PDB005 mainly controls the VCO (voltage controlled oscillator) used to generate the write clock. PDB006 controls the VCXO to generate the read clock used to read the video data from the field memory, and generates the spindle error.

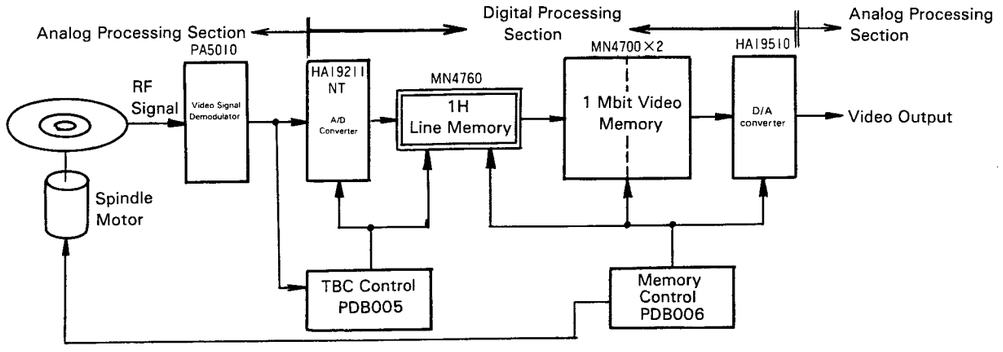


FIG. 15-5-2 Operation Concept Diagram of Digital TBC

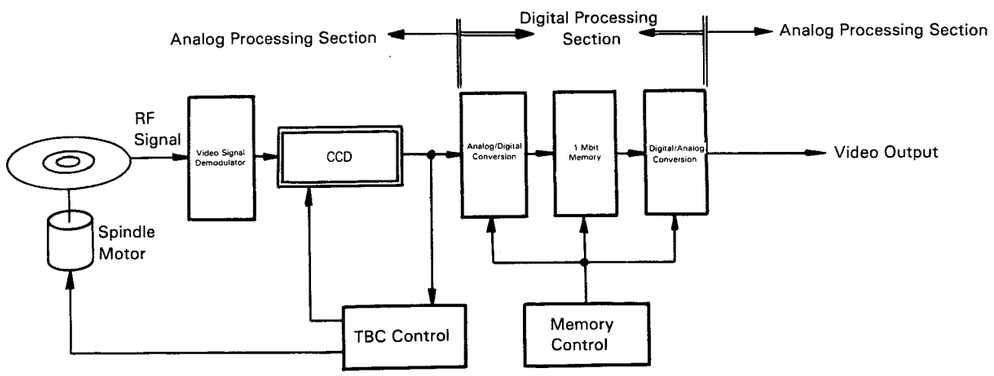


FIG. 15-5-3 Analog TBC (Conventional Type)

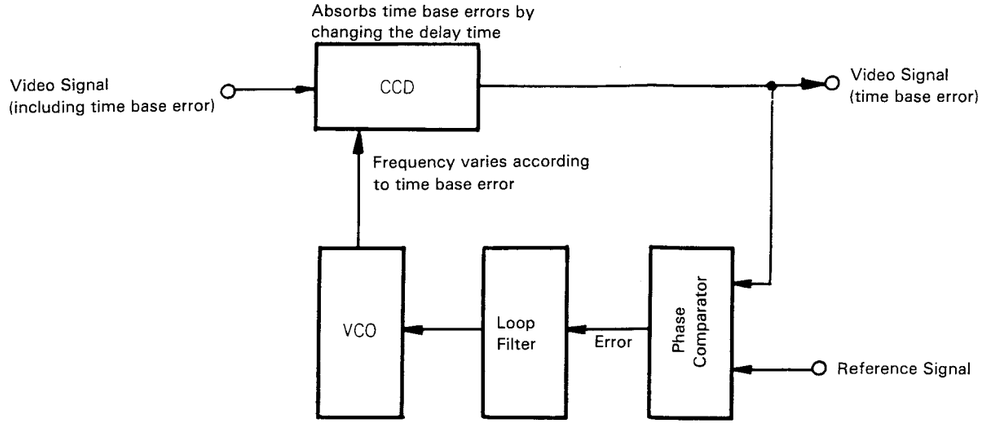


Fig. 15-5-4 Analog TBC Section (Conventional Type)

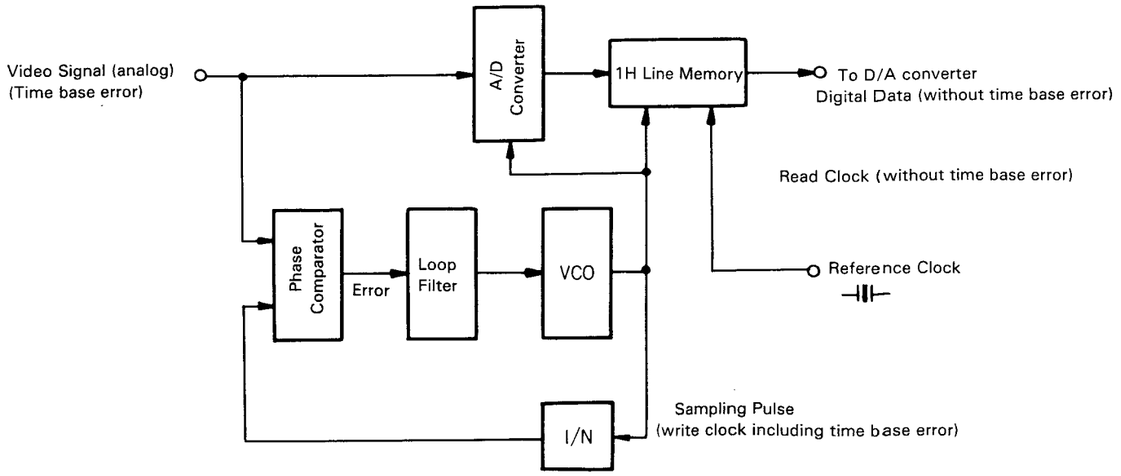


FIG. 15-5-5 Digital TBC Section

15-5-2. Write Clock Control

— CKH (PDB005, ⑦) —

This pin goes high receiving the PB-H (playback horizontal sync signal) when scanning or jumping with a CLV (Constant Linear Velocity) disc, and the signal is sent from PDB006 pin ㊻ to PDB005 pin ⑦. When the CKH pin is at high level, the write clock of the 1/910 counter is set to the hold status.

— SHINH (PDB005, ㉒) —

This signal inhibits the sample & hold operation of the trapezoid signal, and PDB005 pin ㉒ goes high in the following period, and supplied to PA5012 pin ⑥.

- Reference shift period (CKH (PDB005 pin ⑦) goes high)
- While the spindle signal is being unlocked (NSPLOC (PDB005 pin ⑧) goes high)
- When there is dropout and DOSE signal goes high before trapezoid waveform starts, the PB-H (playback horizontal sync signal) is sampled & held.

— DCREST (ODB005 pin ㉖) —

The write start point to the memory of each H sync should be the same, however, lock points of the VCO exist in every 140 ns period. To prevent the VCO lock point shifting too much because of this, an window with a width of 560 ns is provided in the 56NOUT signal at pin ② with the timing shown in Fig. 15-5-7 so that the falling edge of PB-H signal comes inside this window when locked.

In the following status, DCREST pin ㉖ goes high, controlling PA5012 pin ㉘ to reset the burst DC error of VCO so that the rising edge of PB-H signal is locked almost at the center of the 560 ns window. (*1)

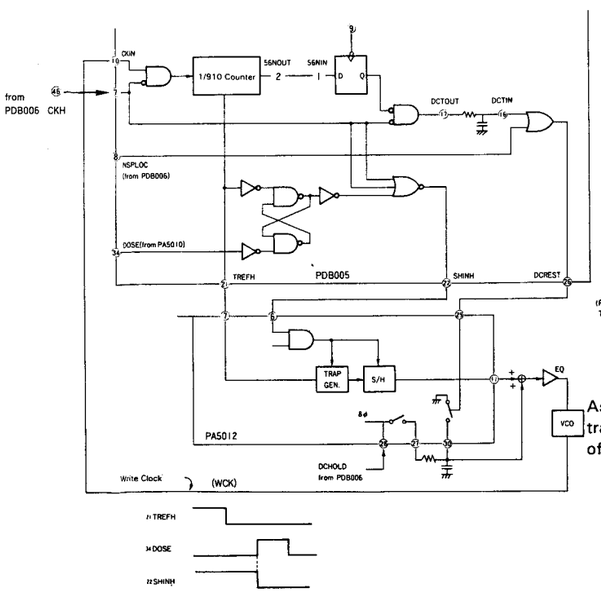
- When the spindle signal is unlocked (SNPLOC pin ⑧ is at high level)
- When the falling edge of PK pin ⑨ does not come within the 560 ns window when reference shift is not done (CKH pin ⑦ is at low level).

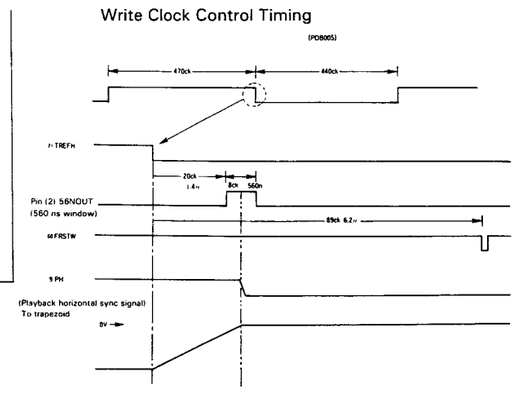
*1: With the DC error reset (PA5012 pin ㉘ at high level), adjust the inclination of the trapezoid signal, and adjust so that the falling edge of the signal output from PA5012 pin ⑤ comes at the center of the 560 ns window as the initial setup.

— DCHOLD (PDB005 pin ㊺) —

This outputs a high level signal to PA5012 pin ㉘ to hold the burst DC error so that there is no change after the VCO lock point, that is the start point of write to memory is locked once in the following status:

- When scanning or jumping (CKH pin is at high level) with CLV discs
- Passing-by happens frequently (sensitivity is adjusted by the time constant of ODCR pin ㊼).





As initial setup, with the burst DC error being reset, adjust the trapezoid signal so that the falling edge of PH comes to the center of the 560 ns window.

FIG. 15-5-7

FIG. 15-5-6

15-5-3 Spindle Control

(1) Spindle error:

The relationship of the start point of write to line memory (RSTW) and start point of read from line memory (RSTR) when the spindle servo is locked is shown in Fig. 15-5-12. And the operation to counter the eccentricity of the disc is shown in Fig. 15-5-13.

(2) Scanning with CLV discs:

When scanning with CLV discs, since the playback horizontal sync signal becomes non-continuous and also the eccentricity of the disc is not continuous, the following controls are performed.

- The SPERR output from PDB006 pin 81 is switched to a signal with a duty ratio of 1:1 (1/128 fsc).
- "56" is loaded as the H address counter for writing to the field memory to reset the spindle error while the writing to the field memory is inhibited by the WEINH signal.

(3) When jumping with CLV discs:

When jumping with a CLV disc, since the playback horizontal sync signal may be non-continuous in the same way as the scanning operation while the eccentricity of the disc is continuous, the following processing is performed.

- The H address counter for writing to the field memory is maintained while the writing into the field memory is inhibited by the WEINH signal.
- The SPERR output at PDB006 pin 81 is switched to asignal with a duty ratio of 1:1 (1/128 fsc).

If the spindle servo cannot follow due to excessive eccentricity or high-speed scanning, the RSTR signal is shifted to control the spindle servo.

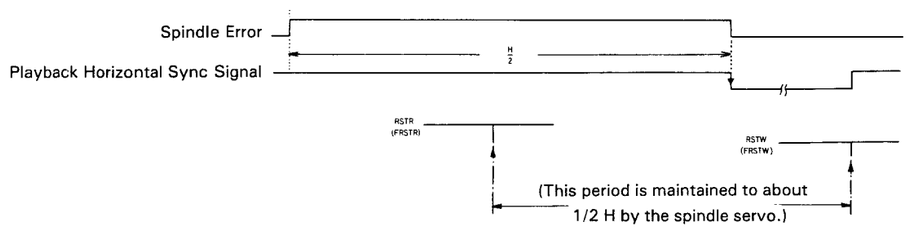


FIG. 15-5-12

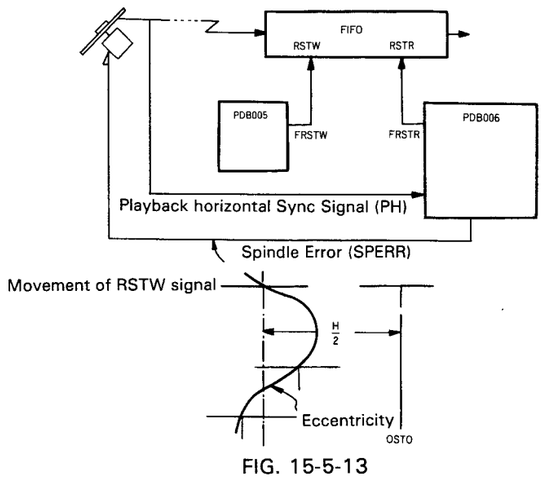


FIG. 15-5-13

15-6. SPECIAL EFFECTS (DIGITAL PICTURE EFFECTS)

Pins concerning special (digital) effects of PDB006 are described below:

- MLTON (pin 133):
  This controls so that the picture is output to the specified screen which is divided on the monitor.
- ARTON (pin 134):
  This controls to provide special effects by controlling the writing of data to memory every 8 clock pulses with the ART pin (156). For example, when the ARTON pin is controlled by the video signal passing through the comparator, only the brighter (or dark) portions of the picture are written into the memory and the movement of objects is traced on the screen.
- SOLON (pin 137):

When the MSB (most significant bit) of the video data which has been converted from analog to digital form is at high level (bright), the corresponding bit is dropped. (See Fig. 15-6-1.)

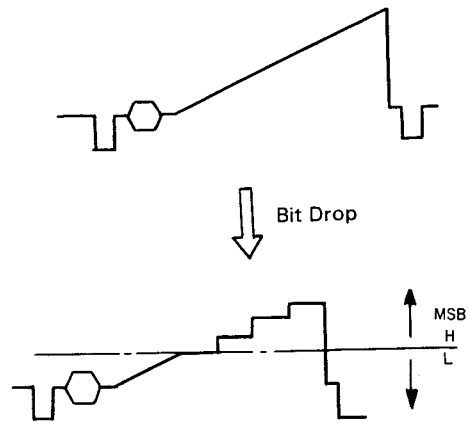


FIG. 15-6-1 Simplified Bit Drop Diagram by SOLON Signal

Special digital effects MLTON and ARTON are possible only every 4 fields because the same color field comes every 4 fields.
The various special digital effects controls are listed below:
These signal line is connected via the communication bus, and latched by PDB006 by the $\overline{\text{STB3}}$ (negative STB3) signal.

Note) 4N: Goes high once per 4N fields

	Pin Name / Function	WRE	WRE1	A	B	MILTON	ARTON	SOLON	INTP
8-Bit	NORMAL		H			L	L	L	L
	Multi	Toggle	4N	H/L	H/L	H	L	L	L
	Art		4N			L	H	L	L
	Solarization	H or L	H or L	H/L	H/L	H or L	H or L	H	H or L
	Interpolation	L	L						H

- Solarization can be controlled independently fromthe control of other modes.

Fig. 15-6-2 Special effects controls

ART ON	ART	
H	H	WENA
H	L	WINH
L	H	WENA
L	L	WENA

Multi

A	B	Height x Width
H	H	4 × 4
L	H	8 × 8
H	L	16 × 16
L	L	256 × 1

Solarization

A	B	
H	H	4bit
L	H	3bit
H	L	2bit
L	L	1bit

Fig. 15-6-3 A, B control signal

15-7. LINE INTERPOLATION WHEN SPECIAL EFFECTS ARE USED WITH CLV DISCS

When special effects using the digital memory are applied (still picture, one-shot memory, etc.), either of the 2 fields (1 frame) making up one picture is written into the digital memory (MN4700) and these two fields are combined then read out from the memory. With this, the following problems may happen in the playback picture:

- Vertical resolution is reduced by half (525/2)
- Two pictures are shifted slightly (flickering)
- Oblique lines on the screen are not straight

For this reason, in this unit, when reading the picture from the digital memory, the H lines before and after the read-out field are interpolated (the middle point value is inserted) to solve the above problem.
When playing back a CAV (Constant Angular Velocity) disc the video signal is passed through the digital memory IC in the same way as in special effects play with a CLV disc, however, since the still picture play is performed by writing data for two fields into the memory and reading from it continuously, the picture is not fixed on the screen as in special effects play with a CLV disc.

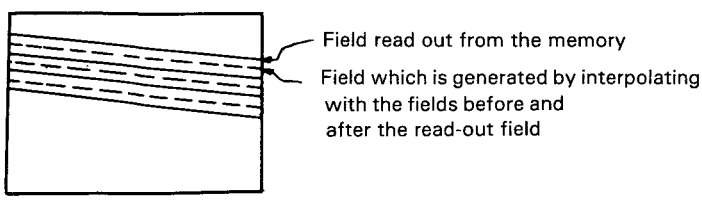


Fig. 15-7-1 Interpolation

15-8. CONTROL BY MN4700

The operation concept of MN4700 is shown below.
Since the minimum unit for random access play, writing to memory or reading from memory is 8 clock periods, the memory write controlled by the ART pin for special effects is performed every 8 clock periods.
Fig. 15-8-2 shows the timing chart for memory control.

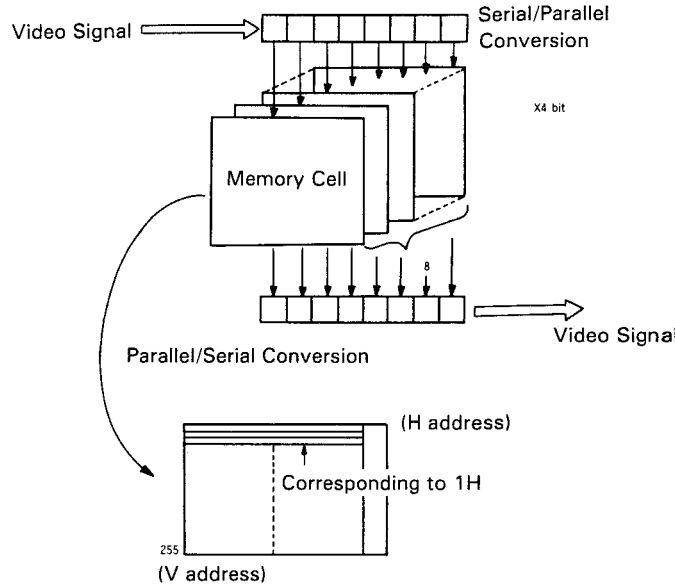


Fig. 15-8-1 Operation concept of MN4700

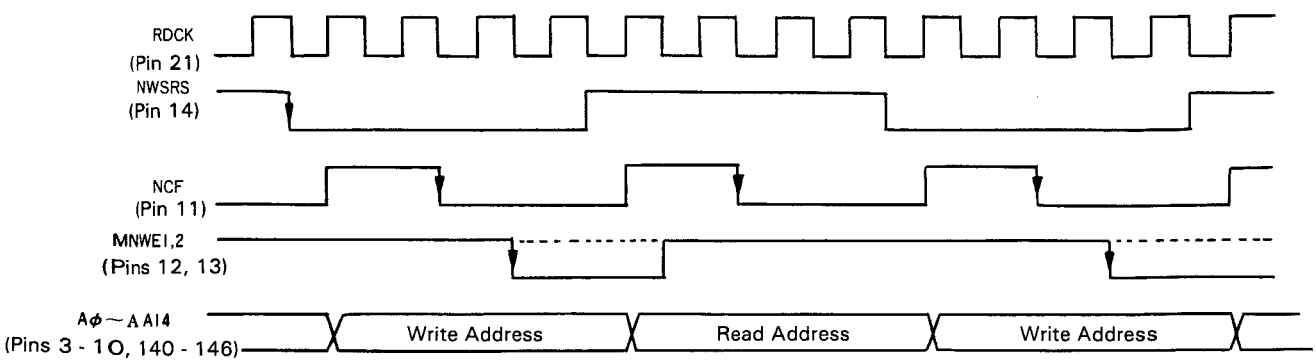


Fig. 15-8-2 Memory access timing chart (PDB006)

SERVICE GUIDE
16. FOCUS (FOCS), TRACKING (TRKG), SLIDER (SLDR) AND TILT SERVOS (DESCRIPTION OF THE HA11529).

16.1. SUMMARY

The HA11529 is an analog/digital hybrid bipolar IC which performs the following functions:

1. FOCS servo control (FOCS servo loop pull in control, FOCS servo loop gain control)
2. TRKG servo control (TRKG servo loop ON/OFF and brake control during track jump and SCAN operations)
3. SLDR servo control (SLDR servo loop ON/OFF, variable speed transport, motor PWM drive)
4. TILT servo control (TILT servo loop ON/OFF)
5. CD/LD FOCS and TRKG servo switch
6. All of the above functions are controlled by 8-bit serial data passed through a serial bus (DATA, CLK, LATCH).
   The 8-bit serial data commands are as shown below.

MODE	ADDRESS				DATA			
	D7	D6	D5	D4	D3	D2	D1	D0
SCAN MODE CONT	1	0	0	0	SCAN SPEED 1	SCAN SPEED 2	SCAN SPEED 3	1: SCAN ON 2: SCAN OFF
SERVO CONTROL 1	1	0	0	1	FOCS 1: ON 0: OFF	DIRECTION 1: FWD 0: RVS	TILT 1: ON 0: OFF	1: LD 0: CD
SERVO MODE CONTROL 2	1	0	1	0	TRKG Zero cross output 1: 1/256 0: Through	TRKG 1: OFF 0: ON	TEST 1: TEST 0: NORMAL	—

* It is possible to set SCAN SPEED at 7 stages using the 3 bits, D3/D2/D1.

16.2. HA11529 Pin Functions

Pin No.	Pin Function
1.	Vee: −5V
2.	FOCS ERROR signal input: OP AMP input to which a SW is connected for gain control during SCAN operation
3.	FOCS SUM input: For DISC detection. Comparator input threshold is +0.4V.
4.	Comparator input threshold for the FOCS S-curve detection is +0.3V.
5.	Comparator input threshold for MAIN BEAM ON/OFF track detection is +0.5V. FOCS SUM input.
6.	TRKG ERROR input: Comparator input threshold for TRKG ERROR zero cross detection is 0V.
7.	GND
8.	TRKG ERROR AMP for CD input
9.	TRKG ERROR AMP for LD input
10.	TRKG ERROR AMP output. TRKG servo phase compensation is connected between this pin and pins 8, 10.
11.	Output for switching the TRKG servo loop characteristics during track jump. (Open or Close)
12.	Outputs the actuator drive and brake pulse during track jump and the actuator brake pulse during SCAN.
13.	Window comparator input to detect the amount of movement in the TRKG actuator during SCAN. Threshold voltage is 0.2V. Actually, an FTS SCAN signal is being input.
14.	Current setting terminal for TRKG actuator brake.
15.	Current setting terminal for pins other than 14P
16.	TRKG RTN input: TRKG RTN input for SLDR servo.
17.	SLDR servo amp output: During play, the SLDR motor is PWM driven and at that time this pin becomes the window comparator input.
18.	SLDR drive signal output during play or when high speed slider is in operation.
19.	SLDR drive signal input when SLDR is operating at low or mid speeds.
20.	Capacitor connected pin for setting the slope of the reference triangular wave for the SLDR motor PWM drive during play.
21.	Resistor-connected pin to set comparator threshold for turning off the TILT servo drive.
22.	TILT ERROR input: op amp input.
23.	A VR is connected for setting the TILT servo gain with the output of the op amp from 22P.
24.	Output for TILT motor drive.
25.	T-CROSS output: TRKG ERROR zero cross count output. Depending on the serial data command, output may be divided by 256.
26.	F-LOCK: L when FOCS lock activated.
27.	J-TRIG input: triggered at startup. L under normal operating conditions.
28.	RESET input:
29.	LATCH input: serial interface bus to the system microprocessor CPU. (29, 30, 31P) Data is latched on the trailing edge.
30.	SDATA input: 8-bit serial command data input.
31.	SCLK input: clock for serial data transmission.
32.	500kHz input: internal logic clock input.
33.	TEST pin: normal state = L.
34.	Pin for setting the injection current used by internal I^2L logic.
35.	Capacitor connected pin for setting the lens UP/DOWN cycle when FOCS ON is activated.
36.	Drive voltage output for lens UP/DOWN.
37.	FOCS Error amp output: FOCS servo phase compensation is connected between 38, 39P.
38.	FOCS Error LD input.
39.	FOCS Error CD input.
40.	Pin with connected offset adjustment VR that uses the uninverted FOCS Error amp input
41.	Op amp output for FOCS gain control
42.	Vcc: +5V.

16.3. DESCRIPTION OF FUNCTIONS

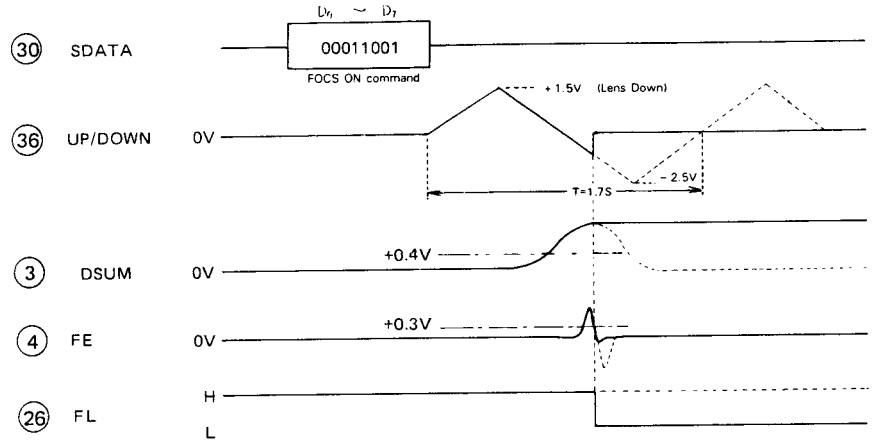
16.3.1. FOCS Assembly

1) FOCS pull in operation

The pull in operation of the FOCS servo raises the objective lens UP/DOWN and, when the input of DSUM (pin ③) and FE (pin ④) fulfill FOCS lock conditions, turns the FOCS servo loop ON. In the case of a defocus caused by damaged disc, the FOCS servo loop is turned OFF and, about 0.5 seconds later, a voltage of +0.6V is output at pin 36.

2) FOCS down and repeat pull in

When the input of DSUM (pin ③) falls below +0.4V as a result of a damaged disc or excessive external vibration, the unit detects an abnormal condition. When this occurs the FOCS servo loop is turned off and at the same time the objective lens is automatically moved UP/DOWN. When conditions as described in 1) have been fulfilled the FOCS servo loop turns to ON.



* The dotted line indicates the wave form when the FOCS servo loop is not ON.

Fig. 16-3-1 FOCS Servo pull in timing Chart

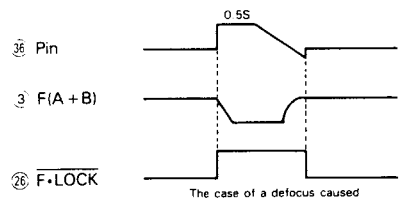


Fig. 16-3-2 Defocus Timing Chart

3) CD/LD switching

Depending on what type of disc is being played, compact disc or laser disc (CD or LD), a switch alters the loop gain and phase compensation of the FOCS servo for the particular disc type. The serial data bit for the CD/LD switch has the same address as the FOCS ON command bit and both can be set with a single transmission.

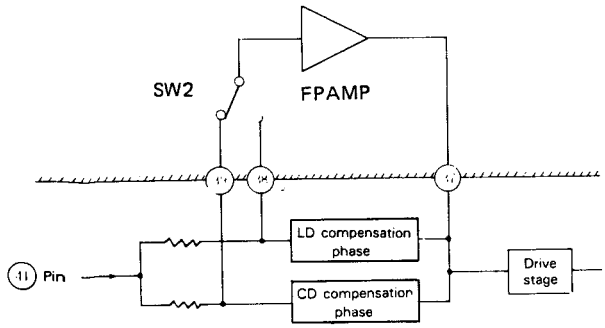
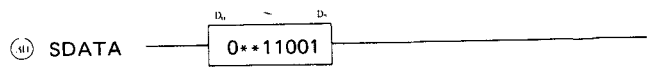
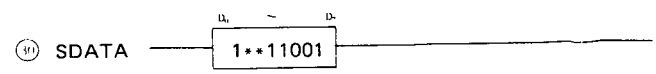


Fig. 16-3-3 CD/LD switching

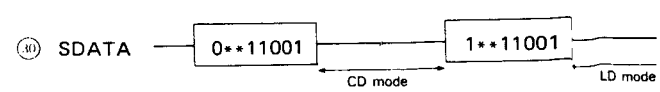
i) Focus ON command when the CD mode is set.



ii) FOCS ON command when the LD mode is set.



iii) When the CD/LD mode is switched in the middle of playback (CD mode → LD mode)



Note 1) The asterisks (*) represent bits which bear no relation to the operation under examination. (This convention will be used throughout the manual.)

16.3.2. TRKG Assembly

1) Track jump operation

Track jump commences when the jump trigger startup pulse is received from JUMP (pin ㉗). Acceleration and deceleration switching are performed by monitoring tracking error zero cross. During a jump operation, SW12 and SW24 are activated sequentially. SW12 is used to switch TRKG loop characteristics and SW24 for adjusting the position of TRKG error zero cross.

Switching between forward and reverse jump is performed by serial data transmission.

The jump trigger signal, controls so that the phase of the input signal to pin ⑥ can be pushed forward beyond its position during normal operation.

i) Forward jump

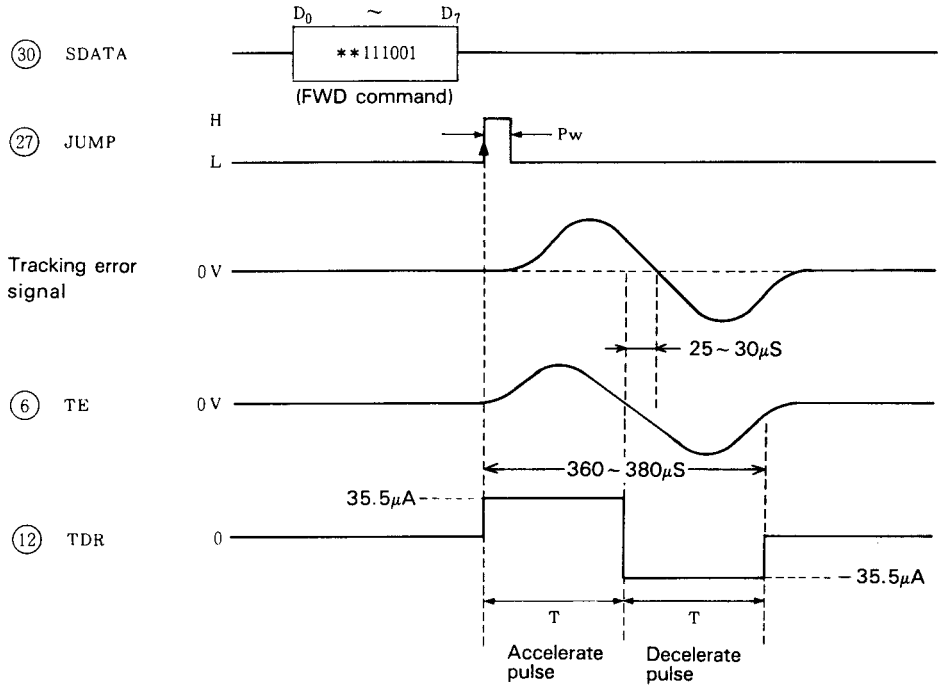
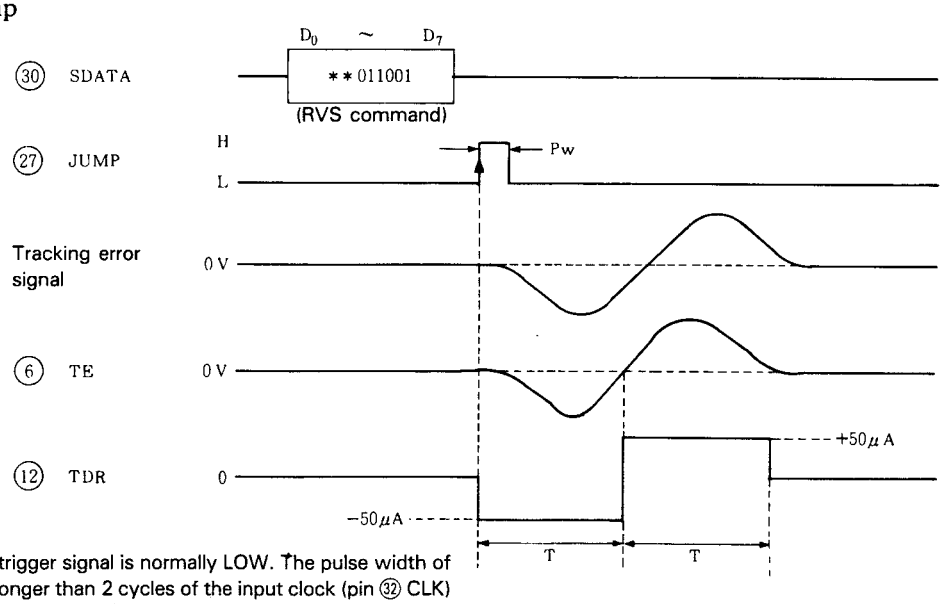


Fig. 16-3-4 FWD JUMP Timing Chart

ii) Reverse jump



Note 1) The jump trigger signal is normally LOW. The pulse width of Pw is set longer than 2 cycles of the input clock (pin ㉜ CLK) and the width acceleration pulse T is set at 9.6μS.

Fig. 16-3-5 Reverse jump Timing Chart

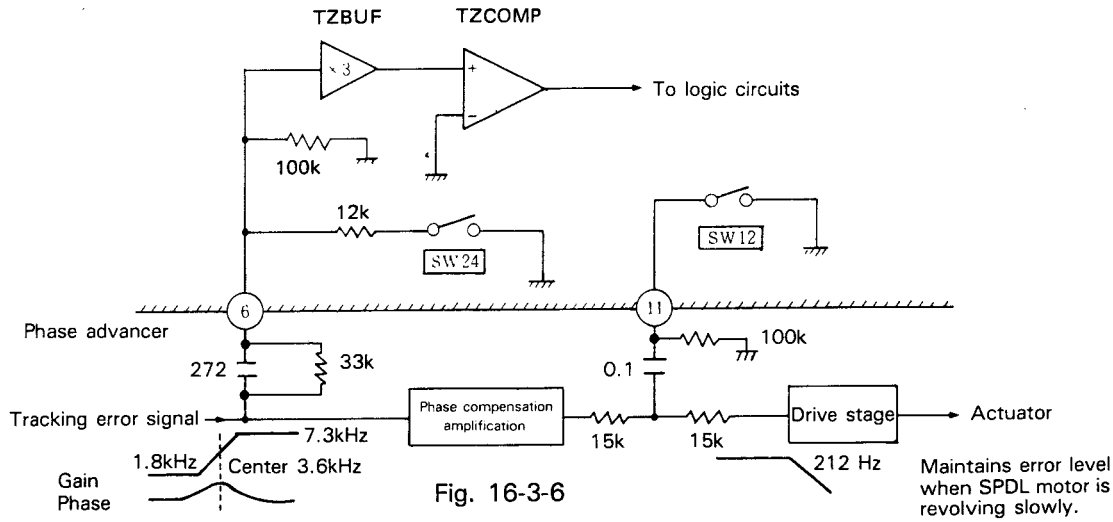


Fig. 16-3-6

2) Scan operation

During slow or medium scan the TRKG servo performs ON/OFF control of the TRKG loop. Input to ST (pin ⑬) signals displacement of the actuator position and the TRKG servo loop is turned OFF. When the error signal at TE (pin ⑥) drops below a set frequency, the TRKG servo loop is turned back ON.

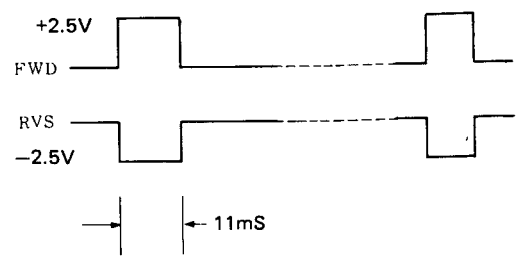
While the TRKG servo loop is OFF, a brake pulse is output by TDR (pin ⑫) according to the timing charts shown below. The polarity of the brake pulse is not a direction command sent via serial data but is determined by the polarity of the signal input to ST (pin ⑬). Corresponding to actuator speed as detected by TE (pin ⑥), brake pulse duty is automatically set to operate in 5 stages (50%-100%). Brake current IB can be adjusted at BSET (pin ⑭).

Because switch timing for the open/close operation of the TRKG servo loop during SCAN is determined by the system microprocessor, an FTS signal like that shown below is actually input to pin ⑬.

This signal also flows into pin ⑫, but the polarity of the brake pulse is opposite to it, which acts to improve convergence during braking.

The cycle of the FTS SCAN signal varies depending on the absence or presence of video memory.

After a jump, the TRKG servo loop closes and if one field worth of data has been properly written to memory, the following FTS scan signal is output. To account for possible mistakes in writing to memory, the period for this operation is not fixed.



i) Forward scan

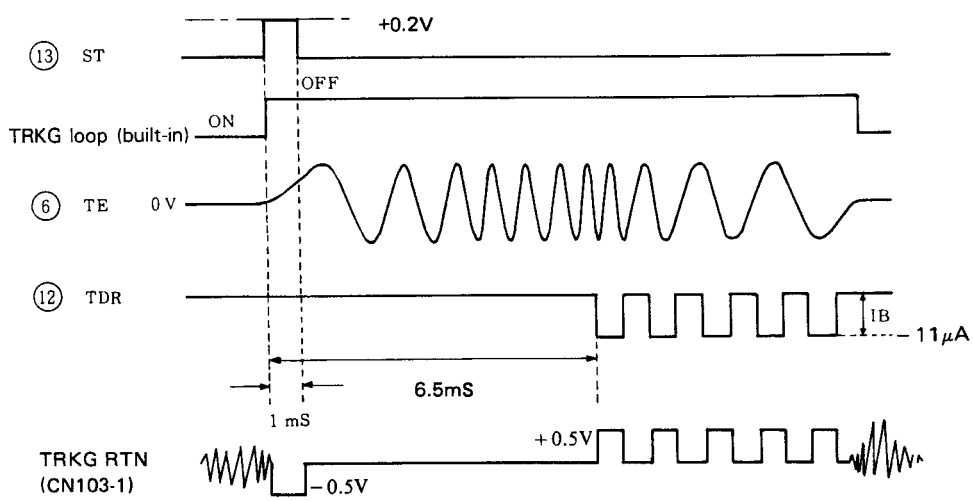


Fig. 16-3-7 Timing chart of forward scan

ii) Reverse scan

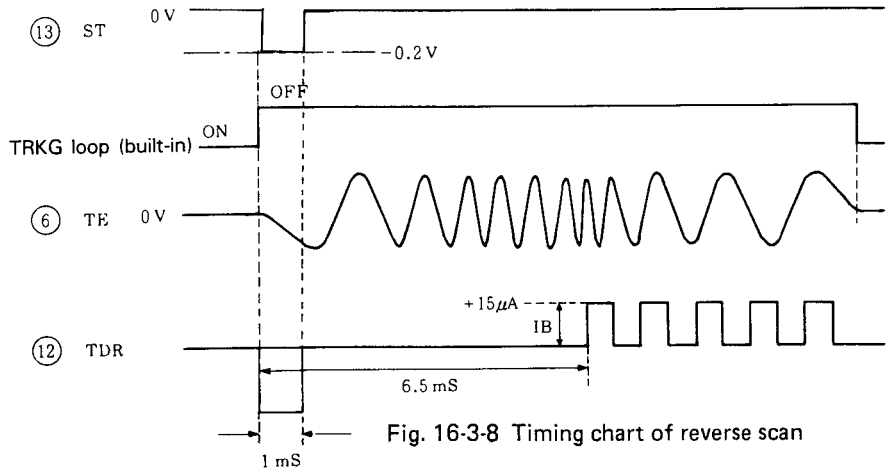


Fig. 16-3-8 Timing chart of reverse scan

3) CD/LD switching

Switching between CD and LD is performed in exactly the same way as CD/LD switching for the FOCS servo.

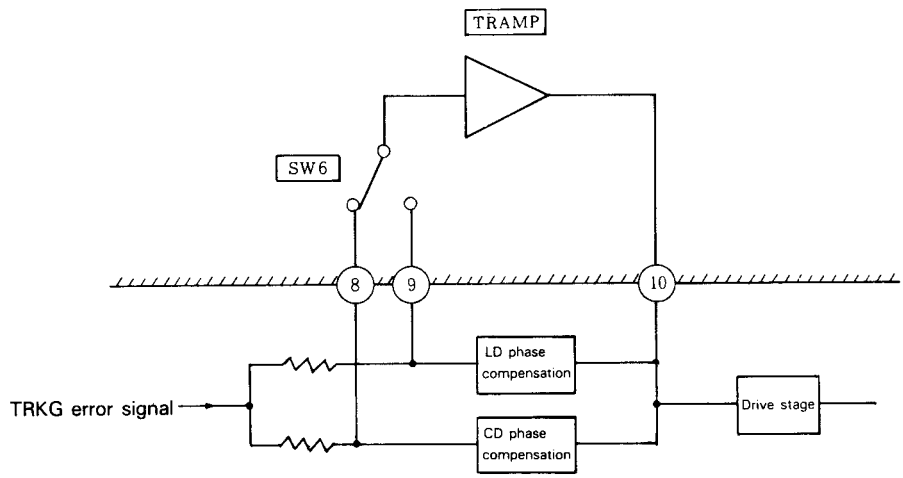


Fig. 16-3-9 CD/LD switching

4) TRKG servo loop ON/OFF control

Switching the TRKG servo loop ON/OFF is done by means of serial data transmission.

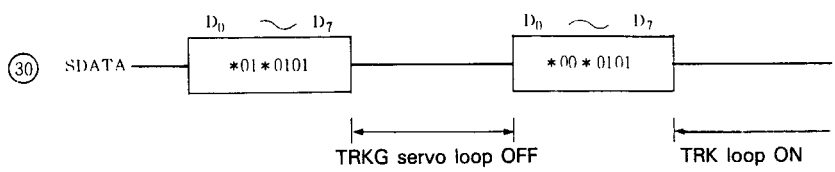


Fig. 16-3-10 TRKG servo loop ON/OFF

5) TRKG count

The number of tracks crossed during high speed scan is counted and then, according to the serial data transmission, a choice is made to either divide (1/256) the output TCNT (pin ㉕) pulse or output it as is.

When a misclamp is detected at the beginning of play, the pulse is divided (1/256) and when tracks are counted during CD search the pulse is output as is.

Once play has begun and the TRKG servo loop is open, track crossing is normal if the number of tracks crossed per disc rotation (6 FG pulses = 1 rotation) is under 1,280 tracks (TRKG count, 5 times: 1mm of eccentricity). If this number is exceeded, however, a misclamp is detected and the disc is ejected from the unit.

16.3.3. Slider Servo Operation

1) Operation in the normal play mode

During normal play DC components in the drive current of the TRKG actuator are PWM modulated at SCOMP1 and SCOMP2. This PWM pulse turns SW7 and SW17 ON and activates the output of the drive signal. The slope of the reference triangular wave can be altered by means of the capacitor connected to SLP (pin ⑳).

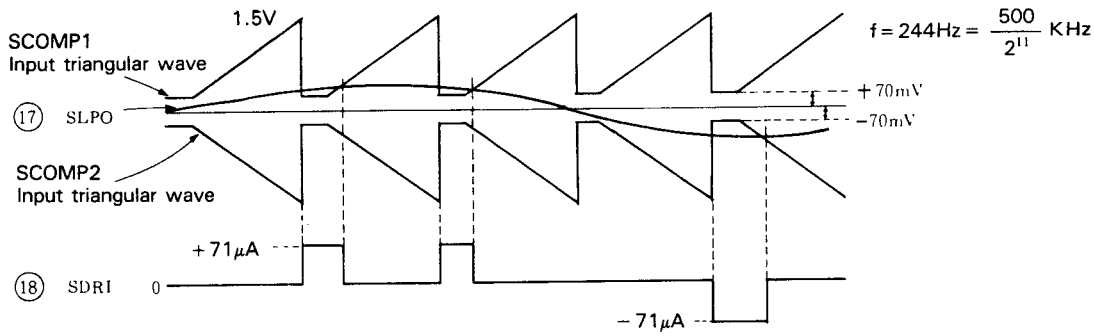


Fig. 16-3-11 SLDR Servo Operation

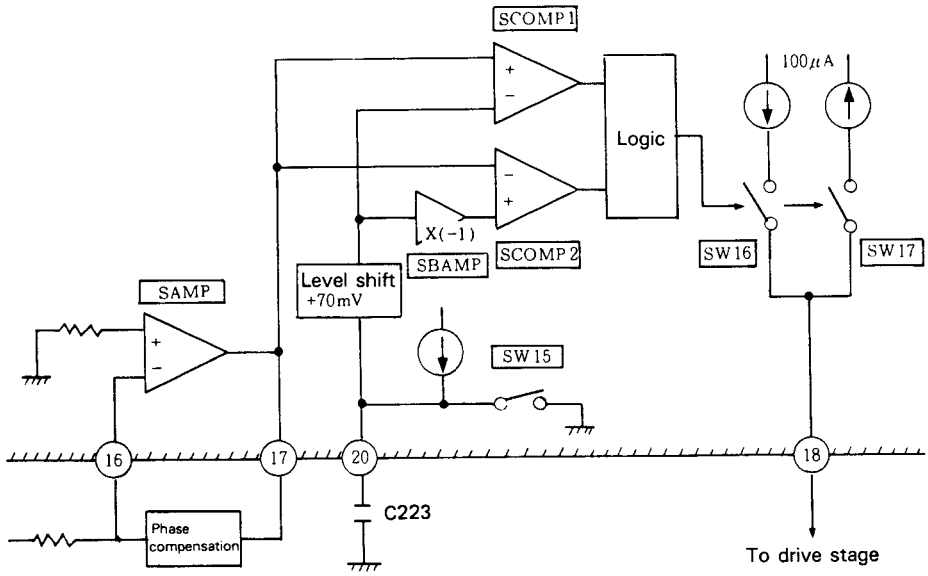


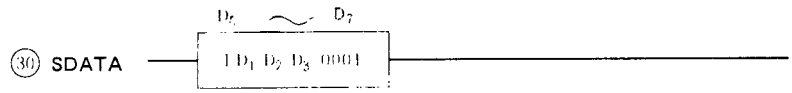
Fig. 16-3-12 SLDR Servo Port (HA11529)

2) Operation in the scan mode

During a scan operation, the SLDR servo loop is OFF and a signal that agrees with the set speed as given by serial data transmission is output either from SDR2 (pin ⑲) or SDR1 (pin ⑱).

i) Low and mid speed scan

SW18, SW20 and SW22 (when set in the FWD direction) or SW19, SW21 and SW23 (when set in the RVS direction) correspond to the serial data, D3, D2 and D1. When the bit is "0", it is OFF, and when the bit is "1", it is ON. Furthermore, on the basis of these three bit combinations a current of 10μA — 110μA (FWD) or −10μA — −110μA (RVS) is output as a duty 50% pulse from SDR2 (pin ⑲). Actually, however, when the unit is used as a CD player, only ±110μA is used.



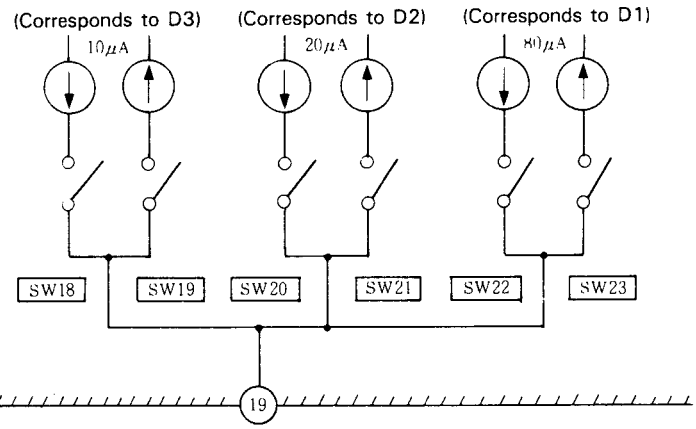
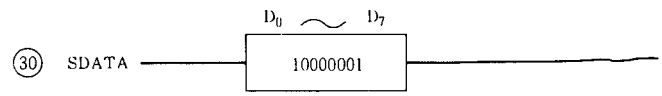


Fig. 16-3-13

ii) High speed scan

By means of the serial data transmission shown at the right, SW16 or SW17 can be turned ON and a ±100μA drive signal output from SDR1 (pin ⑱). The direction is as given in the serial data transmission.

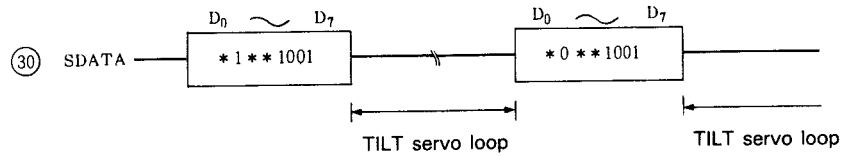


When the unit is used as an LD, the SCAN SPEED control function discussed above is not employed. A combination of the two commands, 10000001 for high speed SCAN and 10001110 that turns the SLDR servo loop OFF are used to control SLDR drive voltage and set SCAN SPEED.

16-3-4 TILT Assembly

1) Loop ON/OFF switch

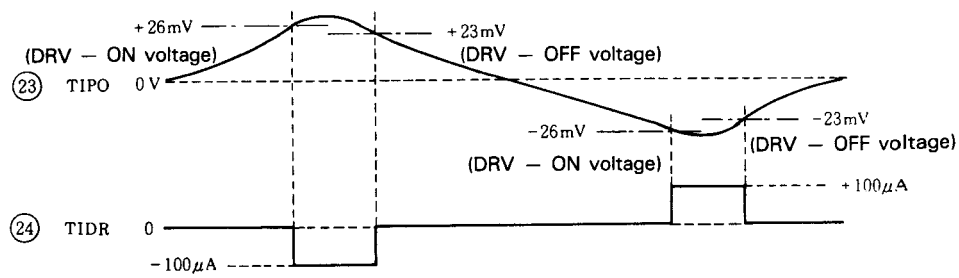
The ON/OFF control of the TILT servo loop is performed by means of serial data transmission.



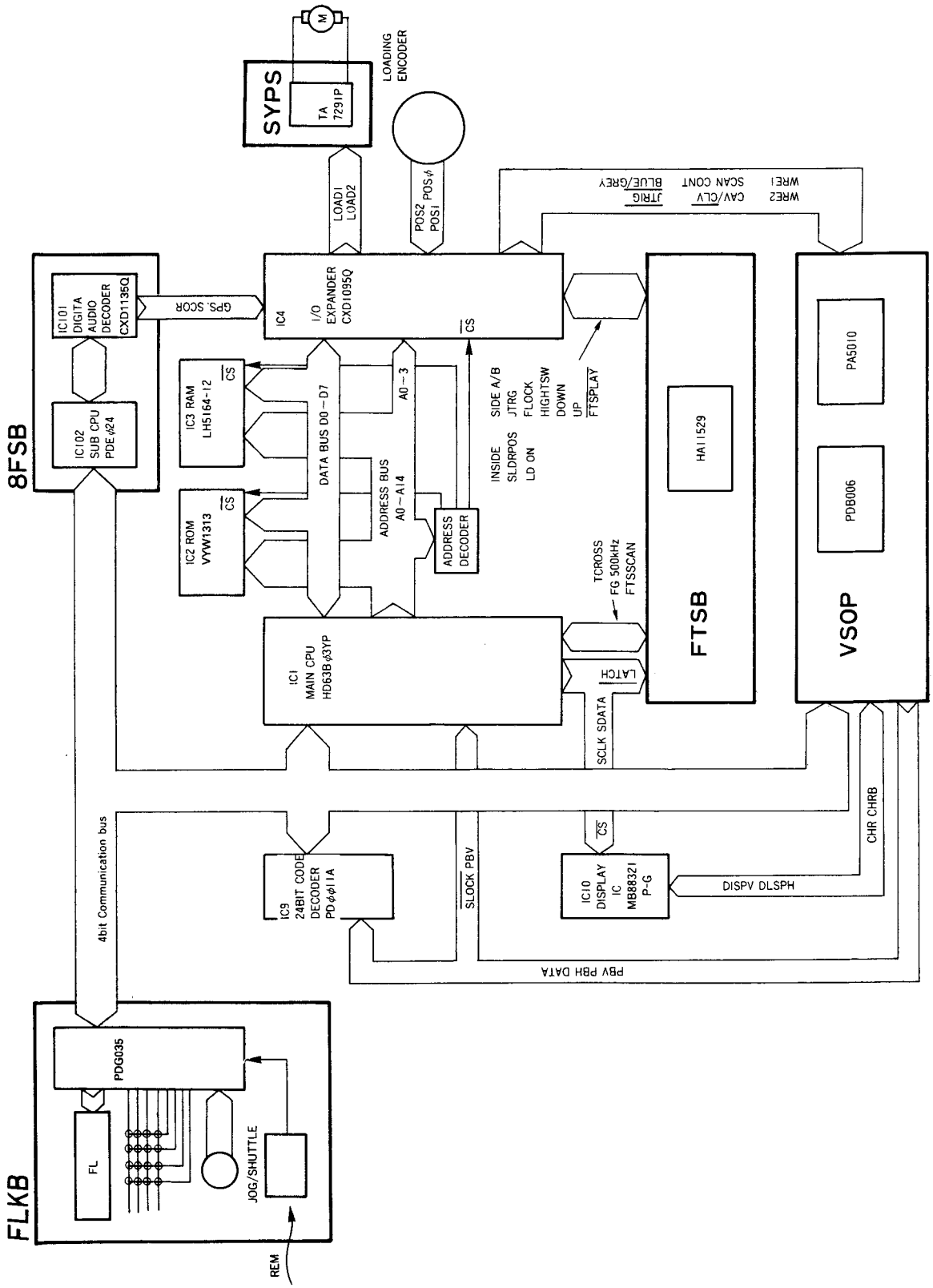
2) TILT servo operation

The TILT error signal is input to the window comparators TCOMP1 and TCOMP2. The drive voltage which is output at TSEF (pin ㉑) operates on an ON/OFF basis. If input is higher than the TCOMP2 reference voltage (DRV — ON voltage), then ON; if input is lower than the TCOMP1 reference voltage (DRV — OFF voltage), then OFF.

DRV — OFF voltage can be adjusted at TSEF (pin ㉑).



17. EXPLANATION OF SOFTWARE USED IN THE SYSTEM MICROPROCESSOR



17-2 DESCRIPTION OF OPERATIONS

Note 1: The LD, CDV and CD inside position signals are related to each other as shown in Fig. 17-2-1, and each position is indicated by the ON/OFF status of the position detect switches (SW) provided for each.

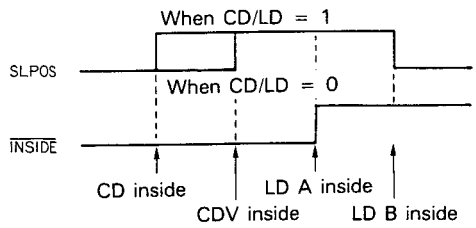


Fig. 17-2-1 Relationship of inside positions of CD, CDV and LD discs

Note 2: The movement of the pickup from side A to side B or vice versa is performed in the directions shown in Fig. 17-2-2.

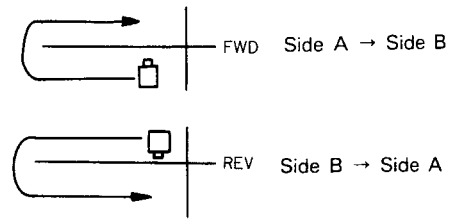


Fig. 17-2-2

(1) When the disc is loaded:

① The disc is loaded until the side A clamp position is reached. (Pulse drive)

② The slider is moved until the position where the LD inside SW is turned ON.

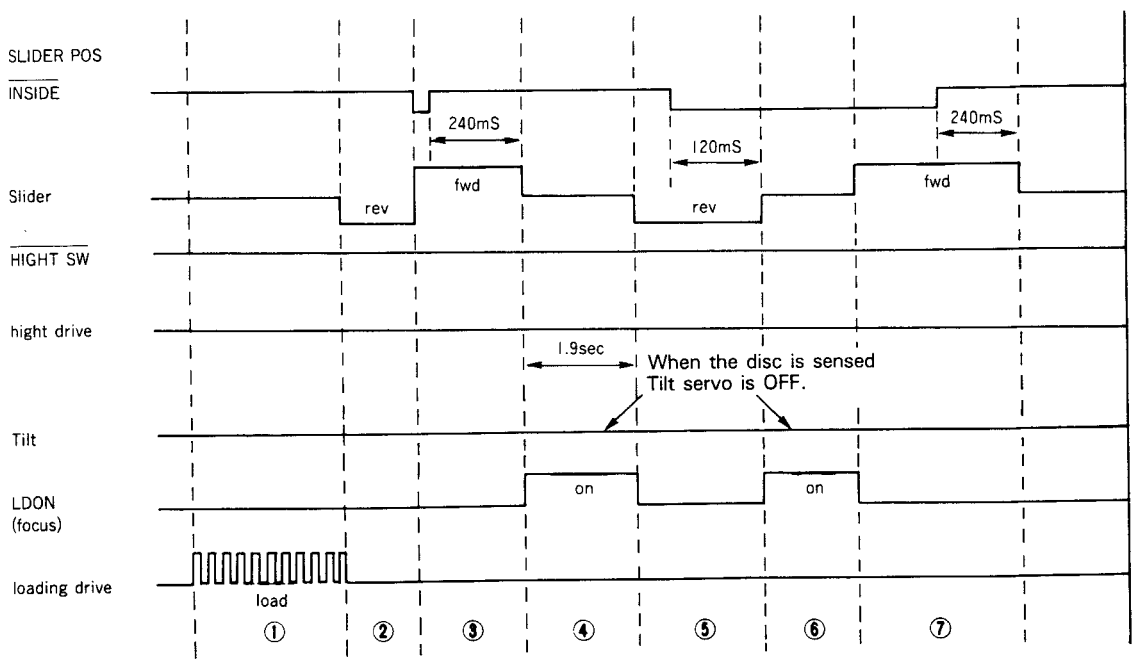
③ After the LD inside SW is turned OFF, the slider is fed again outward by 240 ms (to the LD disc sense position).

④ FOCS servo is turned ON to check whether LD disc is loaded or not. (1.9 sec.)

⑤ After the LD inside SW is turned ON, the slider is fed inward by 120 ms (to the CD disc sense position).

⑥ FOCS servo is turned ON to check whether CD disc is loaded or not. (1.9 sec.)

⑦ If there is no disc, the slider is fed to the transportation position (same as the LD disc sense position).



(2) Switching from side A play status to side B play status:

①The height motor is rotated in the direction in which the pickup is lowered.

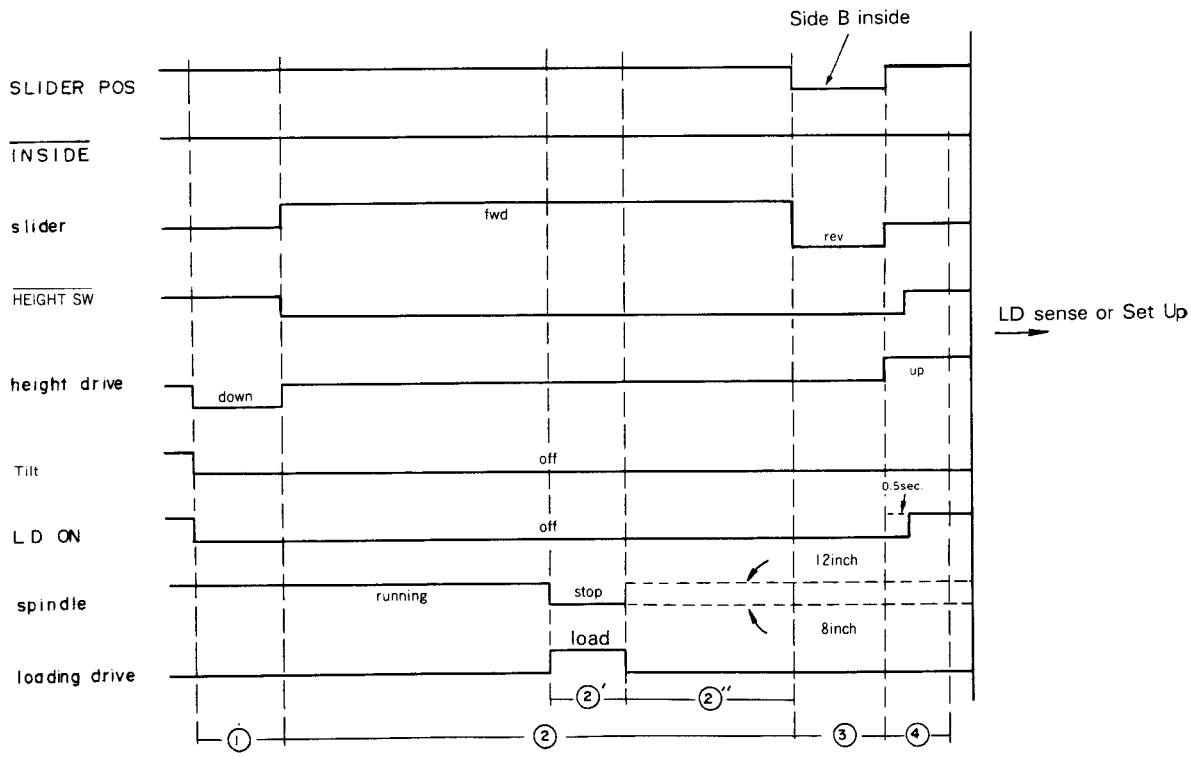
②While the slider is moved to the side B inside position, the status is monitored to see whether the spindle motor has stopped rotating or not.

②′ When the spindle motor stops rotating, side B of the disc is clamped.

②″ When a 12-inch disc is loaded, the spindle motor starts rotating.

③When the side B inside SW is turned ON, the slider is moved to the position where the side B inside SW is turned OFF.

④At the side B inside position, the height motor is rotated in the direction in which the pickup is moved toward the disc. Then, after 0.5 sec. has elapsed after rotation has started, LD ON signal is turned to H.



(3) Switching from side B play status to side A play status:

①The height motor is rotated in the direction in which the pickup is lowered.

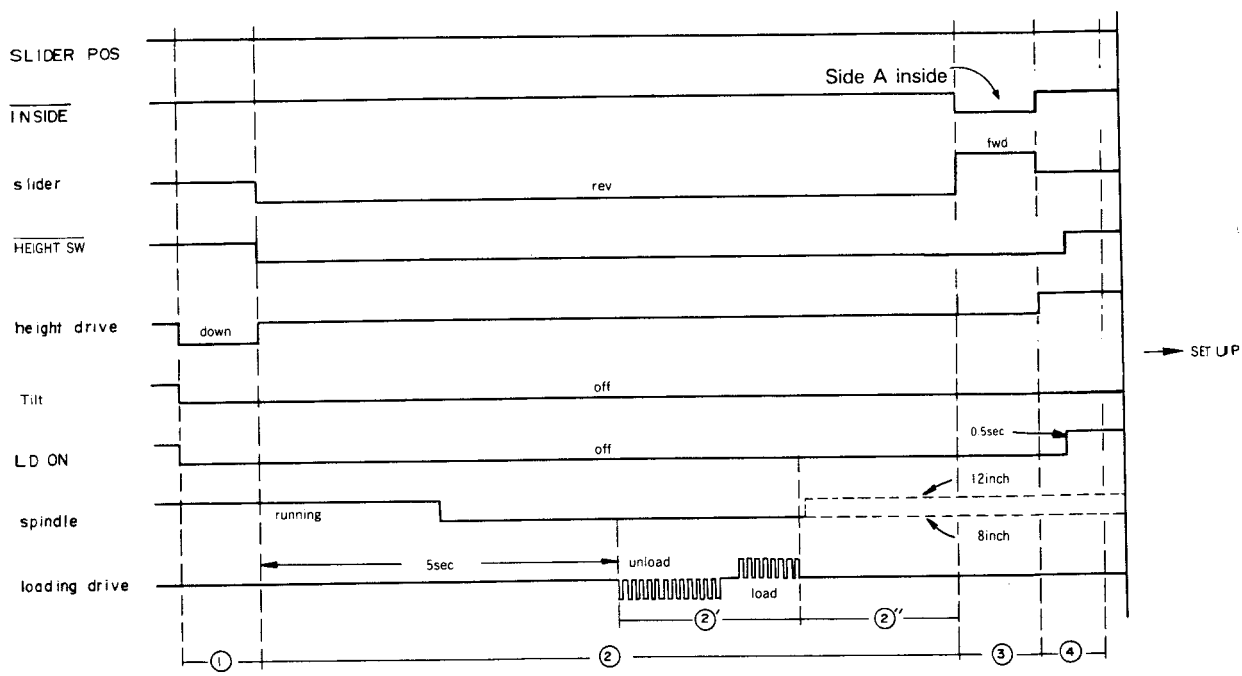
②While the slider is moved to the side A inside position, the status is monitored to see whether the spindle motor has stopped rotating or not. (Monitoring continues for 5 seconds even when rotation has stopped.)

②′When the spindle motor has stopped rotating and 5 sec. has elapsed after the slider begins moving in the reverse direction, side A of the disc is clamped.

②″ When a 12-inch disc is loaded, the spindle motor starts rotating.

③When the side A inside SW is turned ON, the slider is moved to the position where the side A inside SW is turned OFF.

④At the side A inside position, the height motor is rotated in the direction in which the pickup is raised. Then, after 0.5 sec. has elapsed after rotation has started, LD is turned ON.



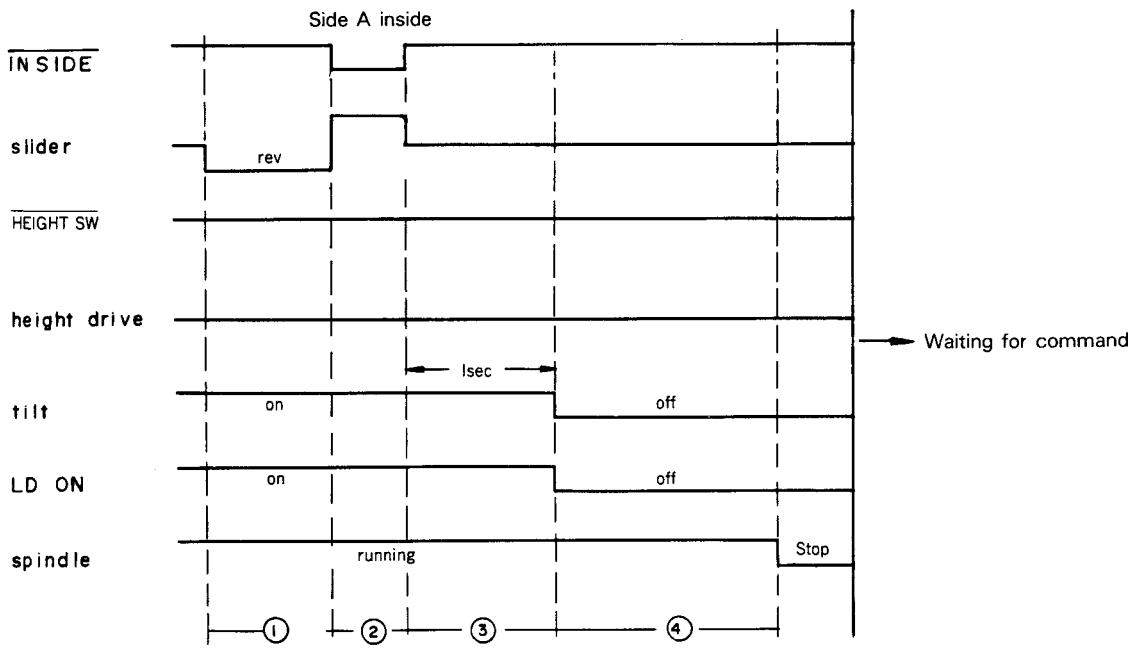
(4) Operation from the side A play status to the stop mode:

① While the LD tilt servo is operating, the slider is moved to the side A inside position.

② When the side A inside SW is turned ON, the slider is moved to the position where the side A inside SW is turned OFF.

③ 1 sec. later, the operation of the LD tilt servo stops.

④ No operation will be performed until the spindle motor stops rotating.



(5) Operation from the side B play status to the stop mode:

①The height motor is rotated in the direction in which the pickup is lowered.

②When the slider has moved to the side A inside position, the status is monitored to see whether the spindle motor has stopped rotating or not.

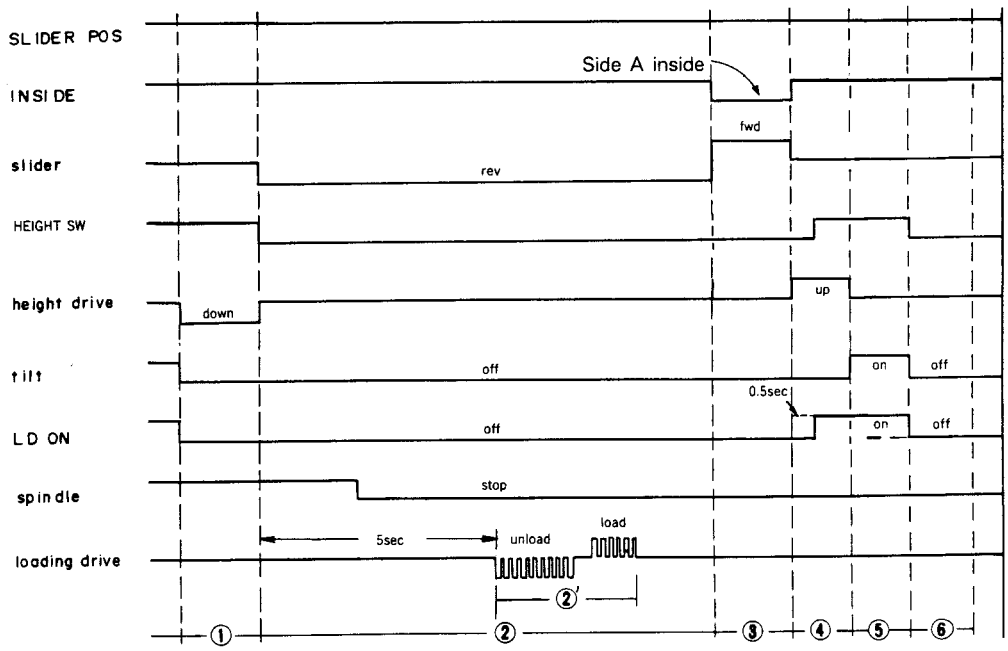
②'When the spindle motor stops rotating and 5 sec. has elapsed after the slider begins moving toward the reverse direction, side A of the disc is clamped.

③When the side A inside SW is turned ON, the slider is moved to the position where the side A inside SW is turned OFF.

④At the side A inside position, the height motor is rotated in the direction in which the pickup is raised.

⑤The LD tilt servo is turned ON and tilt adjustment is performed for side A (for 3 sec.).

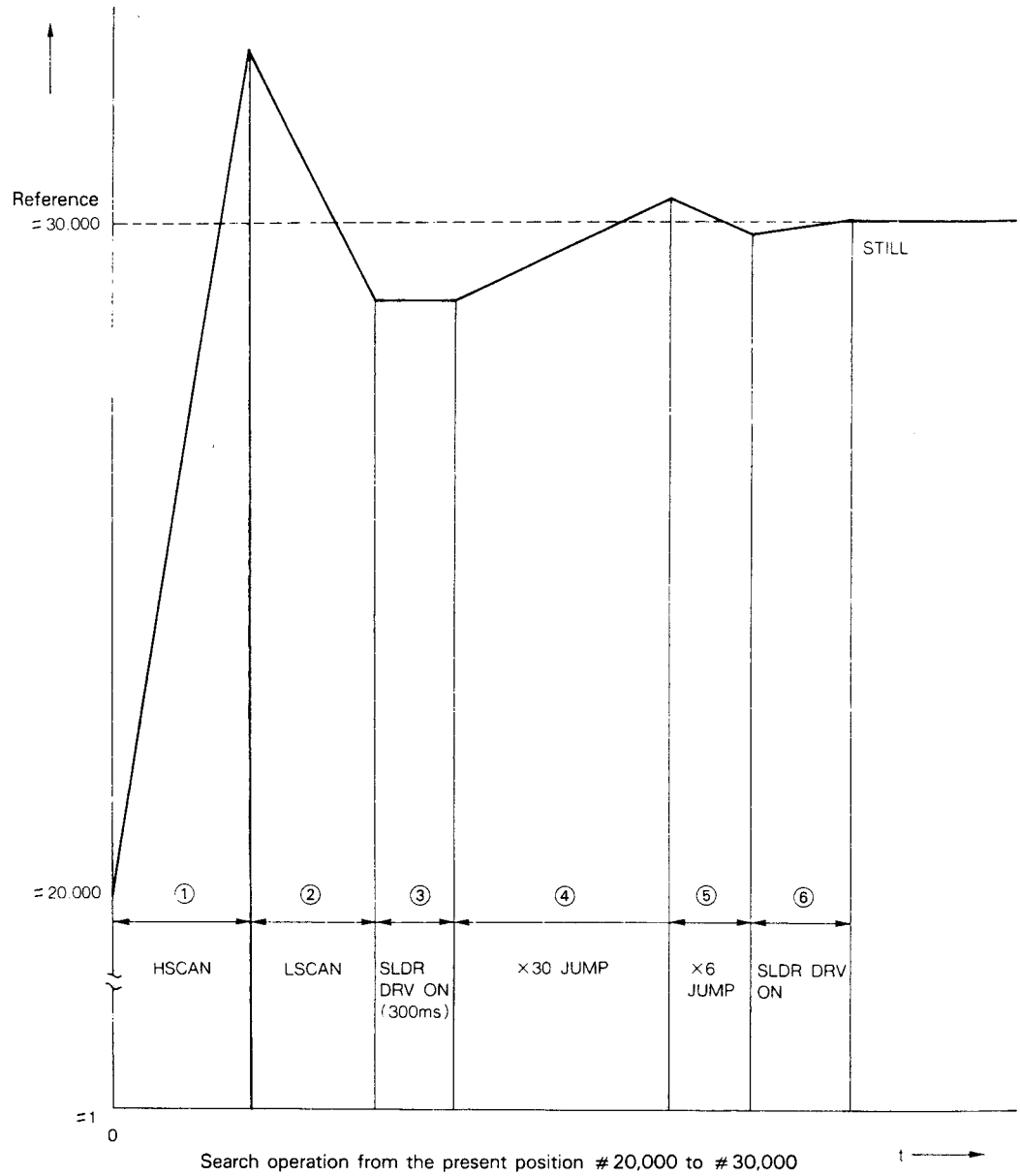
⑥The LD and the tilt servo are turned ON.



(6) When the power is turned ON:

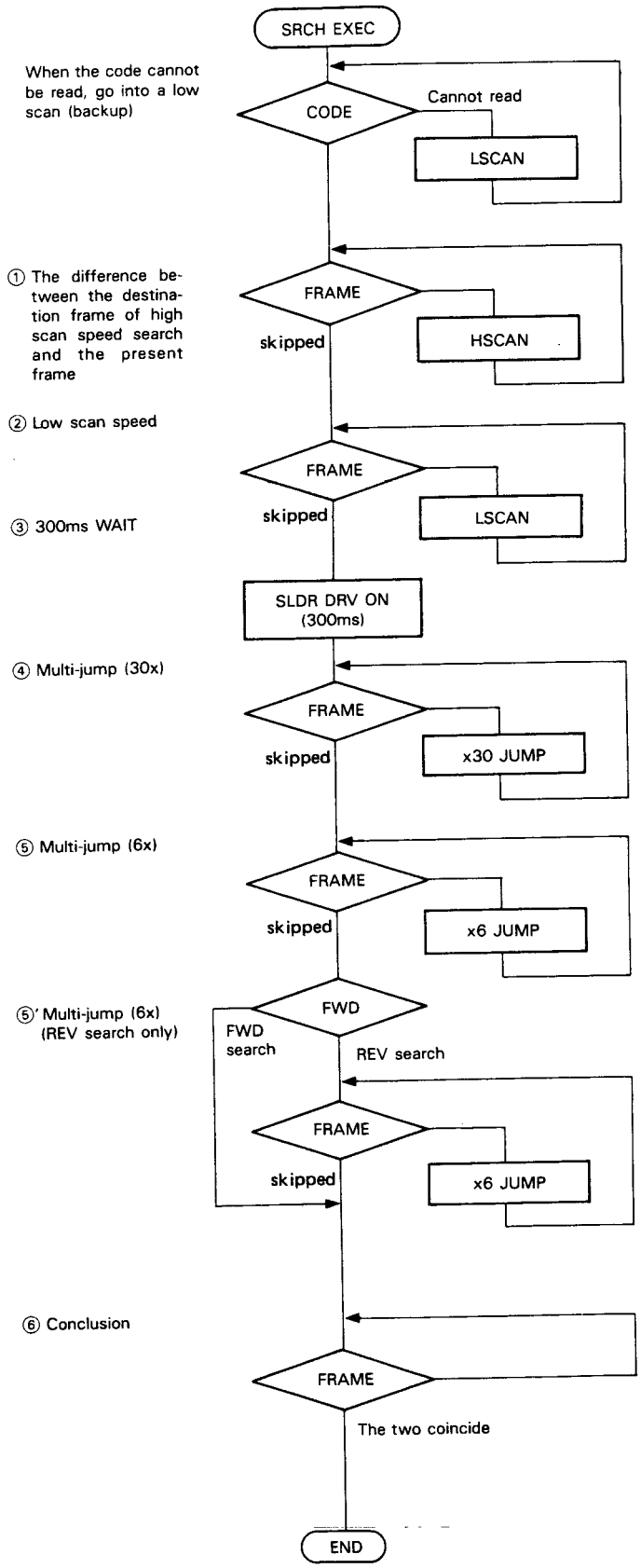
1) The height motor is rotated in the direction in which the pickup is lowered.
2) The height motor is rotated in the direction in which the pickup is raised for 1.4 sec.
3) As the presence of a disc or the type of disc, etc. before the power is turned OFF are stored in memory, after this, operation is performed according to the mode. That is, if an LD is loaded, the slider is stopped at the position where the LD inside SW is turned ON/OFF. If a CD is loaded, the TOC (table of contents) is read. If there is no disc, the slider is moved to the transportation position.

(7) Flame search operation

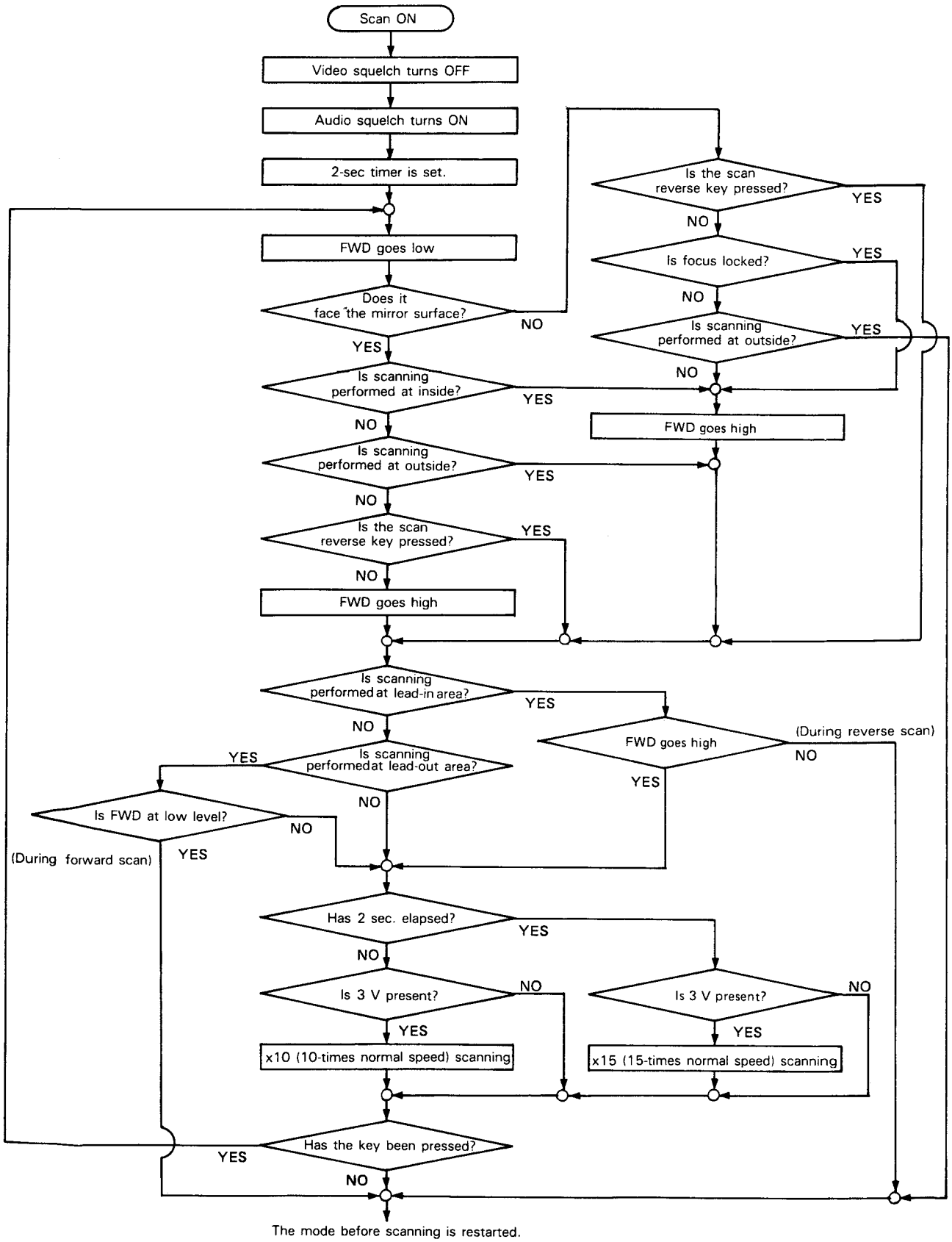


Flame search operation

Flow chart of frame search

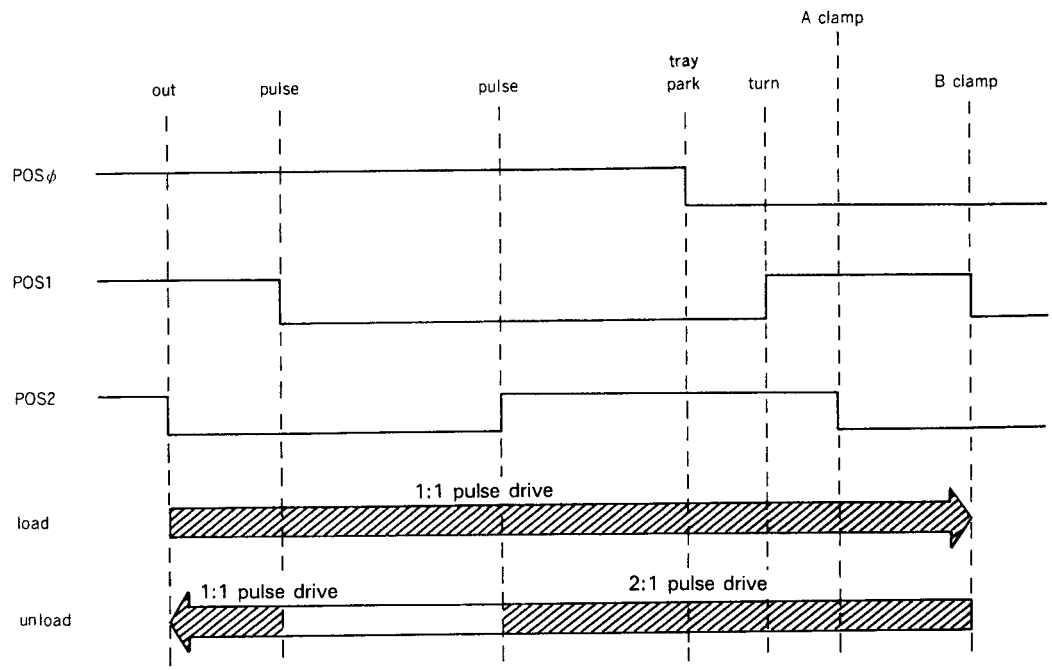


(8) Flow chart of scanning operation



(9) Loading operation:

To recognize the loading position, a rotary encoder is provided which outputs a signal using 3 bits to designate eight positions. The loading operation is performed by pulse drive according to the position detected by the above method.

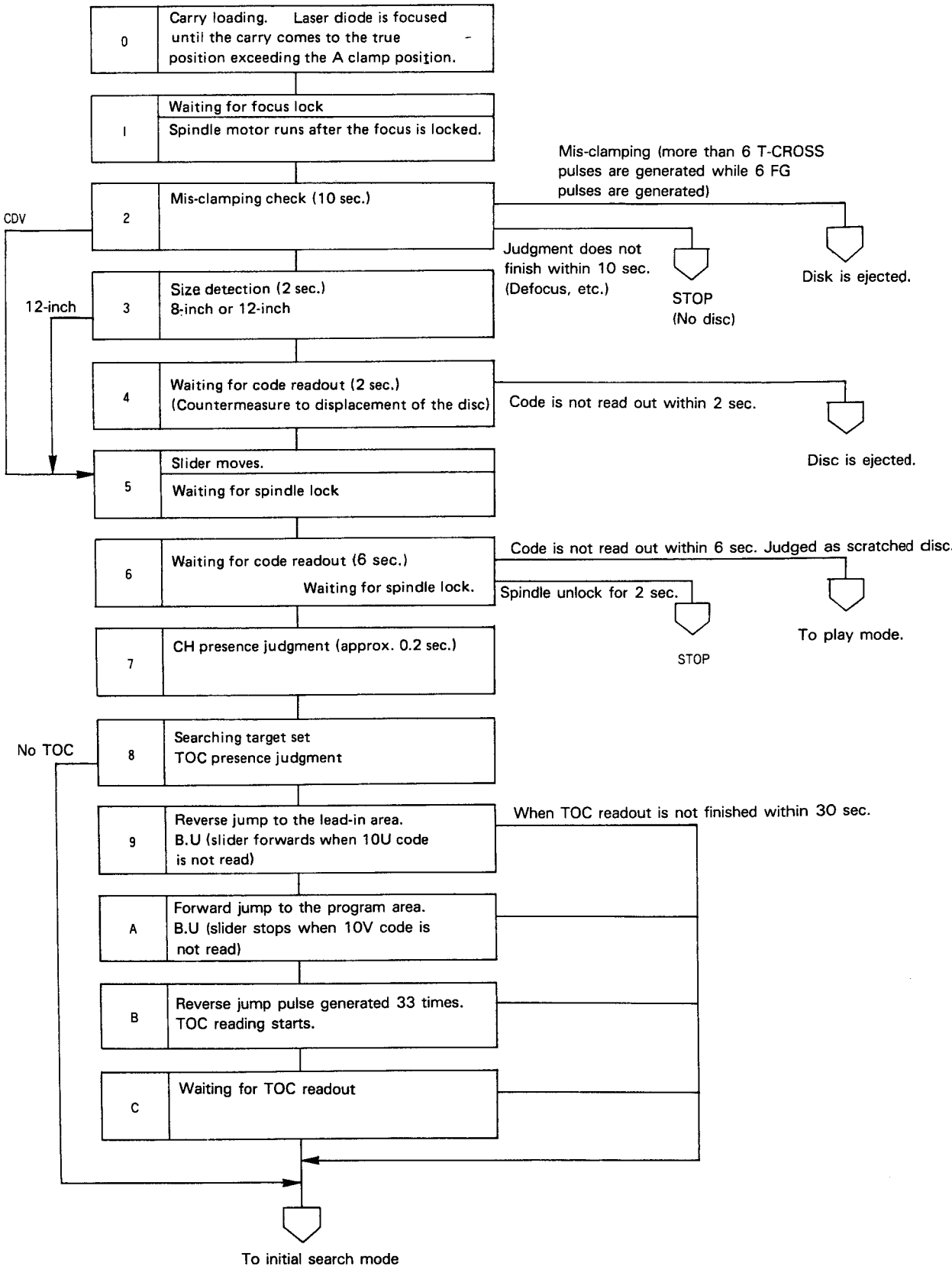


(10) Height servo:

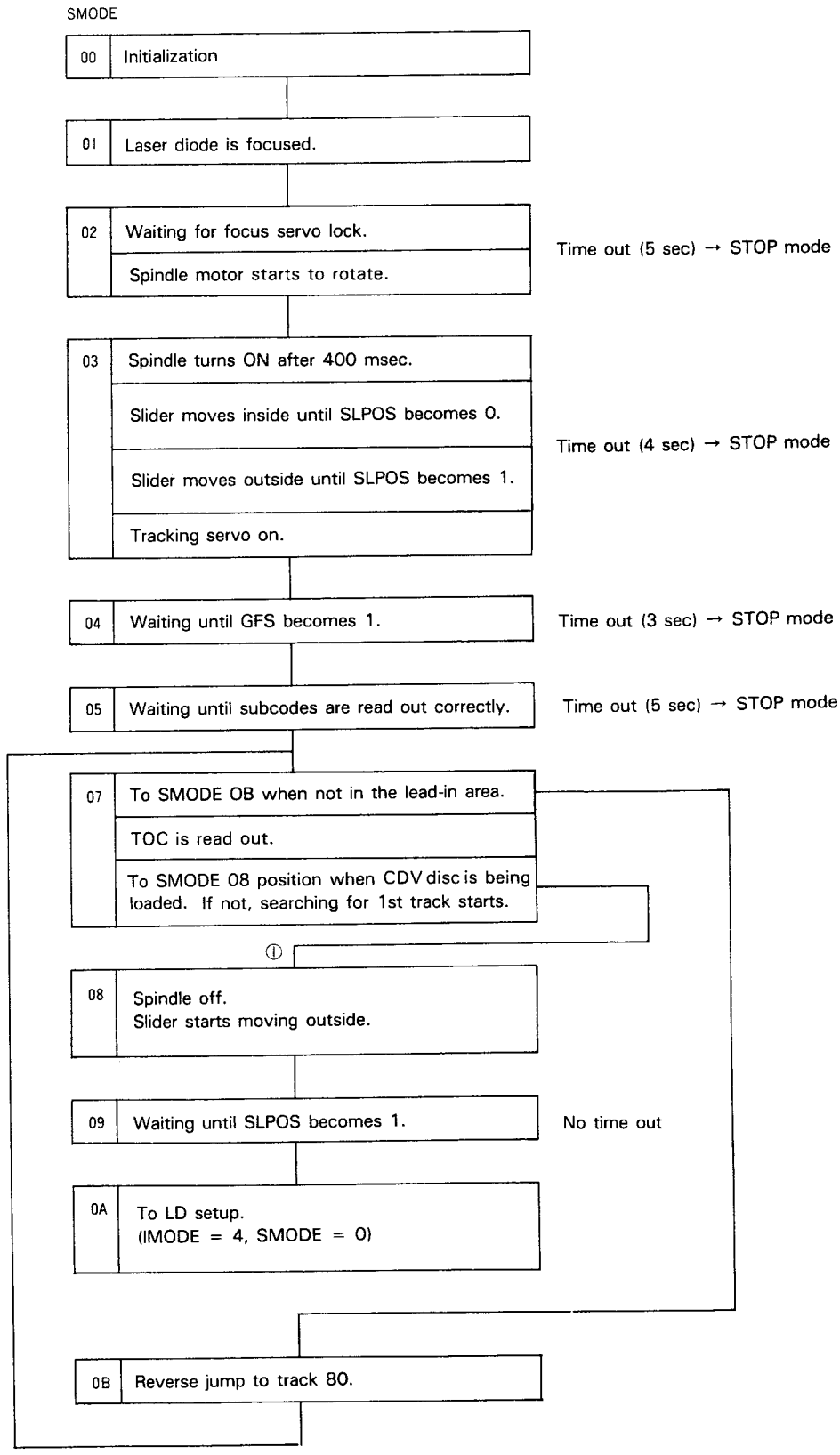
The height servo is used to obtain the sufficient focus stroke for any position on the disc. When LD (focus) is turned ON, it is controlled by the DC component of the focus servo signal. When LD is turned OFF, the height motor can be moved up/down under the control of the microcomputer.

The height servo is normally maintained in the condition of the disc which was played last. However, when the power is turned ON or when playback of the side B of the disc is finished, the height motor is lowered until the $\overline{\text{HIGHT SW}}$ signal is turned ON under the control of the microcomputer, then the height motor is raised (height neutral) after approx. 1.4 sec. has elapsed.

(11) LD setup (contents of SMODE display when IMODE = 4):



(12) CD setup:


SMODE
00
Initialization
01
Laser diode is focused.
02
Waiting for focus servo lock.
Spindle motor starts to rotate.
Time out (5 sec) → STOP mode
03
Spindle turns ON after 400 msec.
Slider moves inside until SLPOS becomes 0.
Slider moves outside until SLPOS becomes 1.
Tracking servo on.
Time out (4 sec) → STOP mode
04
Waiting until GFS becomes 1.
Time out (3 sec) → STOP mode
05
Waiting until subcodes are read out correctly.
Time out (5 sec) → STOP mode
07
To SMODE 0B when not in the lead-in area.
TOC is read out.
To SMODE 08 position when CDV disc is being loaded. If not, searching for 1st track starts.
①
08
Spindle off.
Slider starts moving outside.
09
Waiting until SLPOS becomes 1.
No time out
0A
To LD setup.
(IMODE = 4, SMODE = 0)
0B
Reverse jump to track 80.