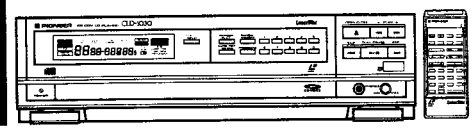
PIONEER®
The future of sound and vision.

Service Manual



ORDER NO.
ARP 1502

COMPACT DISC/LASERVISION PLAYER

CLD-1030

- This service manual is applicable to the KUC type.
- For the circuit description, refer to CLD-3030 Service Guide (ARP1560).

CONTENTS

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS SERVICE INC. P.O. Box 1760, Long Beach, California 90801 U.S.A.
PIONEER ELECTRONICS OF CANADA, INC. 505 Cochrane Drive, Markham, Ontario L3R 8E3 Canada
PIONEER ELECTRONIC [EUROPE] N.V. Keetberglaan 1, 2740 Beveren, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia TEL: [03] 580-9911

1. SAFETY INFORMATION

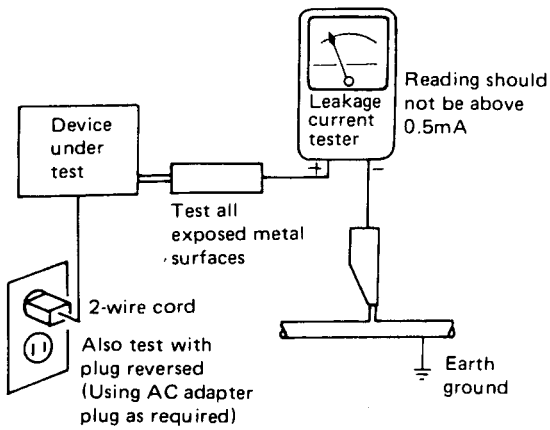
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

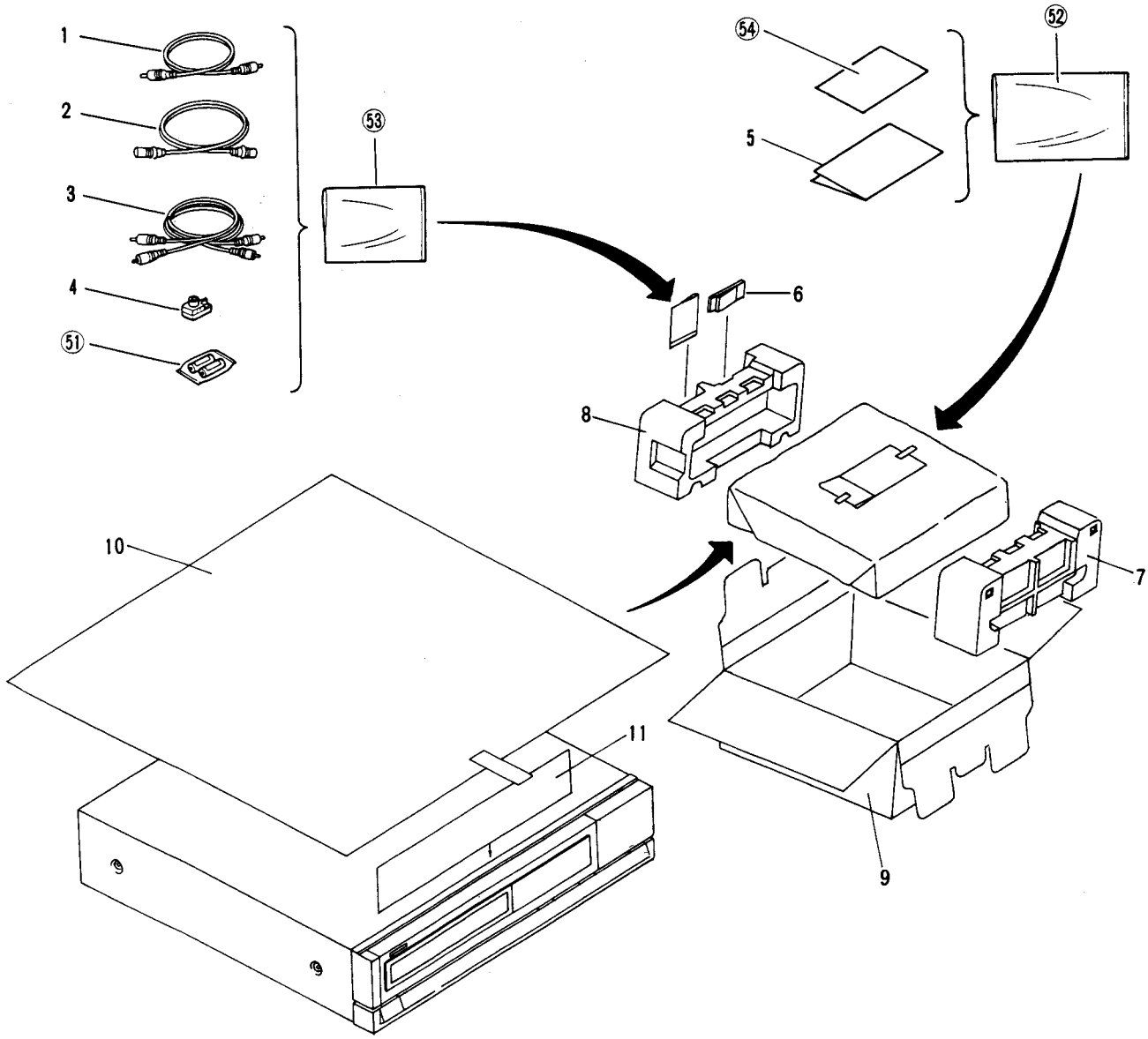
Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

2. PACKING



Parts List of Packing

Mark	No.	Part No.	Description
	1.	VDE-056 (VDE1004)	Video cable
	2.	VDE1001 (VDE-054)	RF antenna cable
	3.	VDE-055 (VDE1005)	Audio cable
	4.	VKX1001	Antenna adaptor
	5.	VRB1008	Operating instructions (English)
	6.	VXX1122	Remote control unit
	7.	VHA1027	Pad (F)
	8.	VHA1028	Pad (R)
	9.	VHG1026	Packing case
	10.	VHL1006	Packing sheet
	11.	VHL1008	Protection sheet
	51.		Battery UM-4
	52.		Polyethylene bag
	53.		Polyethylene bag
	54.		Caution card

3. EXPLODED VIEWS AND PARTS LIST

3.1 EXTERIOR AND FRONT VIEW

NOTES:

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *For your parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★ GENERALLY MOVES FASTER THAN ★
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

Parts List of Exterior and Front View

Mark	No.	Part No.	Description
	1.	VNK1090	Carry
	2.	VNL1061	Rack gear (R)
	3.	VNL1060	Rack gear (L)
	4.	VEC1130	Disc pad (Z)
	5.	VEC1115	Disc pad
	6.	VBH1047	Sub container spring
	7.	VXX1143	Container assembly-S
	8.	VNL1062	Stopper
	9.	VBH1021	Stopper spring
	10.	VEB1041	Rack Dump rubber
	11.	IBZ30P080FCU	Screw
	12.	VXX1125	Bonnet assembly-S
⚠	13.	VDG1012	AC Power cord
	14.	REC1005	Dumper assembly
	15.	PMZ20P040FCU	Screw
	16.	BBZ30P050FCC	Screw
	17.	APZ30P080FCU	Screw
	18.	VXA1094	Insulator assembly
	19.	BBT30P060FBR	Screw
	20.	BPZ40P100FBR	Screw
	21.	APZ30P140FCU	Screw
	22.	BPZ30P080FCU	Screw
	23.	VDA1051	Fuji card
	*24.	VXX1126 VXX1196	Front door assembly-S
	25.	VNK1125	FL panel (X)
	26.	VXX1124	Front panel assembly-S
	27.	VEB1033	Door dump rubber
	28.	VXX1081	Door cover assembly-S
	29.	VNL1042	Roller
	30.	VXA1166	Hinge assembly
	31.	VBH1048	Door spring (L)
	32.	VBH1049	Door spring (R)
	33.	VNK1105	Power button
	34.	VNK1106	Volume knob
	35.	VBH1019	Power spring
	36.	BPZ30P080FCU	Screw
◉	37.	VYG1017	FLKY assembly
	38.	VEC1059	Plastic rivet
	39.	VBK1009	Switch spring
	40.	VEB1045	Stop dump rubber
	41.	VNL1084	PSW cap
	42.	BPZ26P060FCU	Screw
	43.	CPZ26P100FZK	Screw
	44.	VBH1047	Sub container spring
	45.	WT16D060D025	Wsher
	46.	WA22N050W020	Nylon washer
	101.		Rack holder
	102.		Base assembly
	103.		Dumper holder plate
	104.		Insulator cushion
	105.		Bottom plate assembly
	106.		HEPB assembly
	107.		CNNB assembly
	108.		IRKB assembly
	109.		Stop plate
	110.		Cushion (A)
	111.		Insulator sheet
	112.		Spacer
	113.		Cushion (B)
	114.		Jack panel
	115.		Sub container assembly

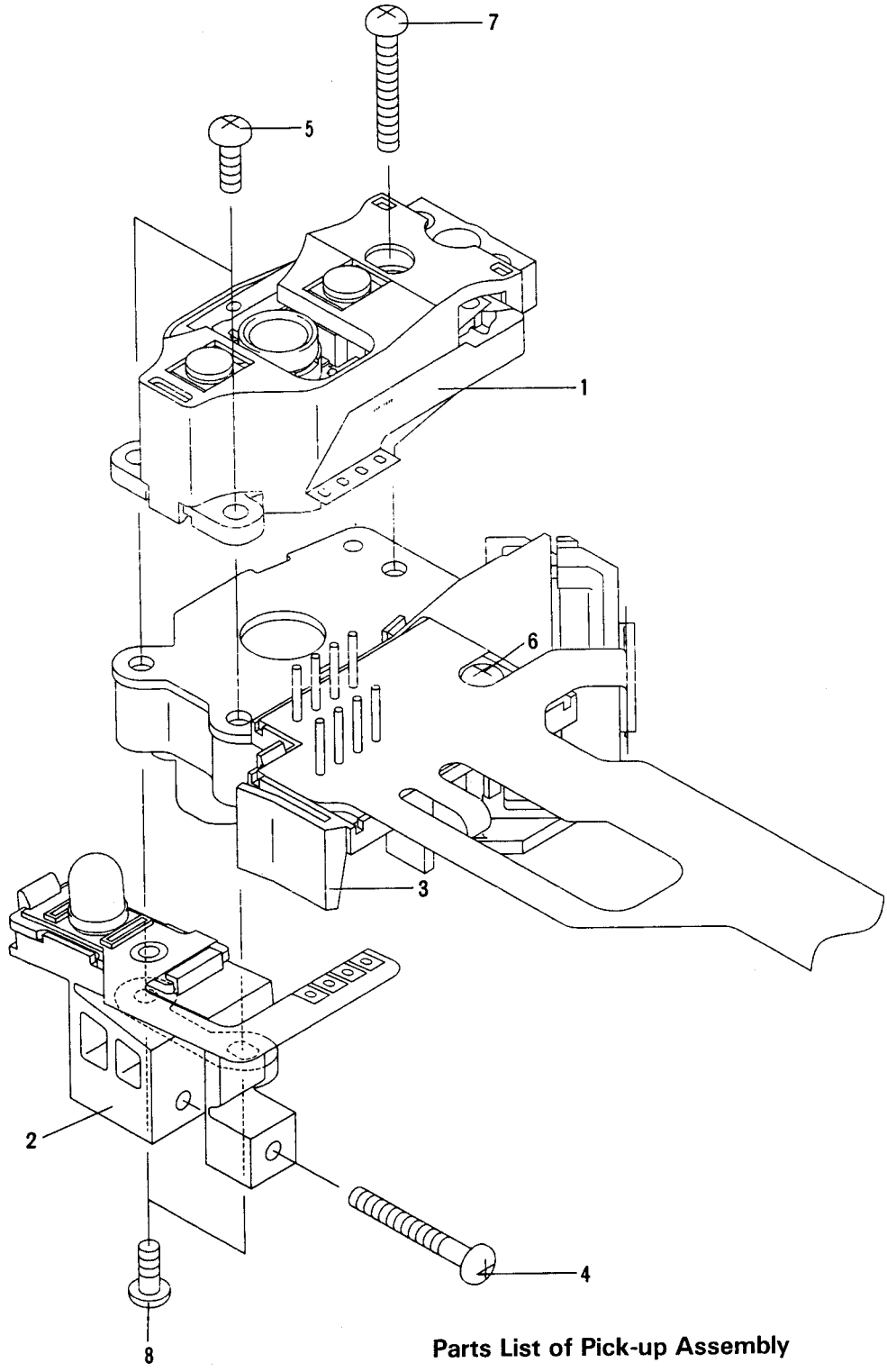
***NOTE:**

Front door assembly-S

Serial No.	Part No.
3903001 ～3903100	VXX1126
3903101 ～	VXX1196

The difference between VXX1126 and VXX1196 is the color of the FL filter.

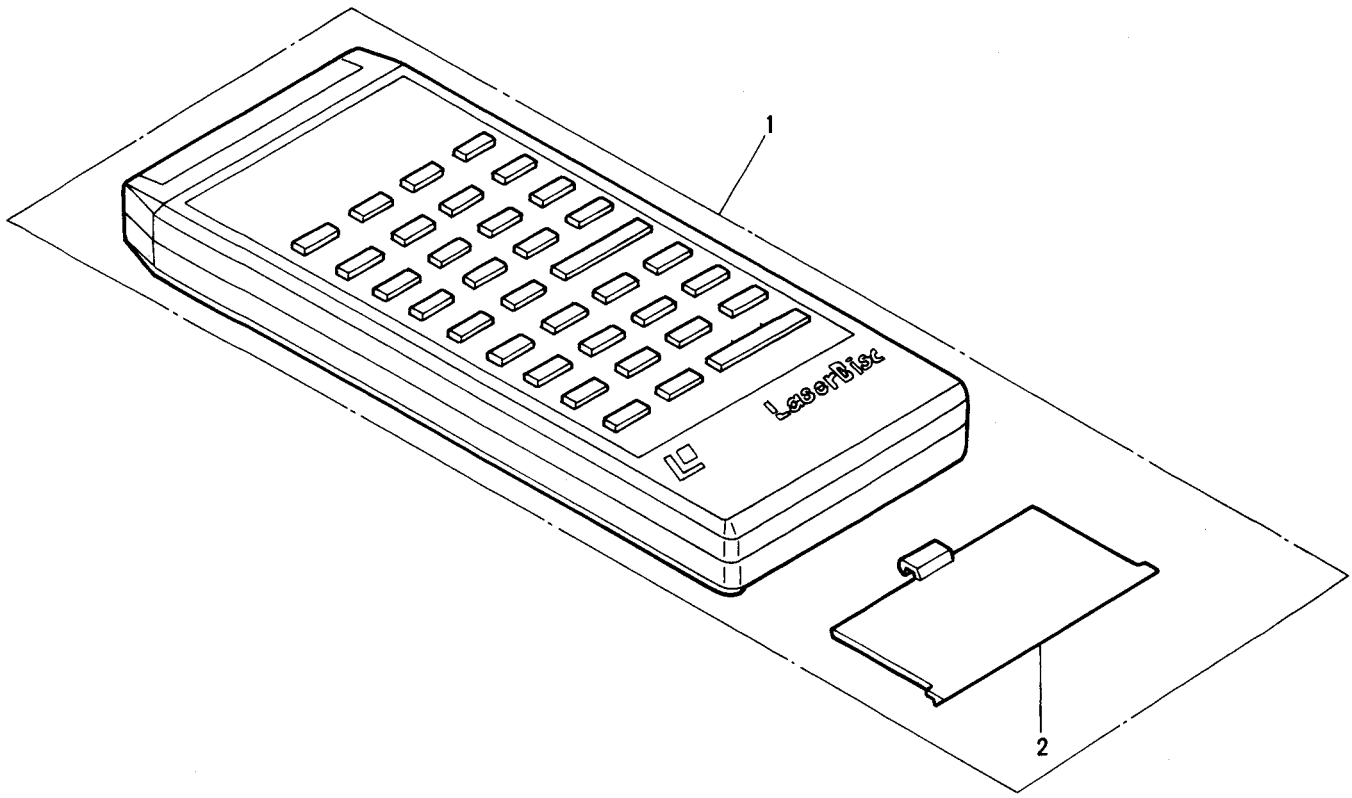
3.5 PICK-UP ASSEMBLY VIEW



Parts List of Pick-up Assembly

Mark	No.	Part No.	Description
	1.	VXX1056	Actuator assembly
	2.	VXX1094	Sensor assembly-S
	3.	VXX1095	Pre pick-up assembly
	4.	PBZ20P160FMC	Screw
	5.	PMA20P060FMC	Screw
	6.	PMA20P080FMC	Screw
	7.	PMA20P140FMC	Screw
	8.	PMB20P050FMC	Screw

3.6 REMOTE CONTROL UNIT



Parts List of Remote control unit

Mark	No.	Part No.	Description
	1.	VXX1122	Remote control unit
	2.	PNW1153	Battely cover

Mark	Symbol & Description	Part No.
	C139, C181, C344, C352, C412, C420	CFTXA104J50
	C19, C361, C466, C495, C509, C521, C526, C611, C657, C665, C669	CGCYX473M25
	C332, C333	CKCYB472K50
	C8, C21, C24, C123, C401, C404, C409, C410, C414—C416, C423—C426, C431, C436, C438, C439, C441, C442, C464, C477, C485, C487, C489, C491, C492, C502, C504, C506, C510, C512, C517, C524, C601—C604, C652—C654	CKCYF103Z50
	C615	CKPUYB101K50
	C127, C326, C327	CKPUYB102K50
	C130	CKPUYB681K50
	C605	CKPUYF103Z25
	C28, C118, C120, C132, C134, C153, C156, C159, C160, C162, C172—C176, C178, C182, C303—C308, C359, C606, C607	CKPUYF223Z25
	C104, C105, C117	CQMA102J50
	C419, C113, C116, C608	CQMA103J50
	C131	CQMA122J50
	C329, C331	CQMA152J50
	C101	CQMA182J50
	C137, C664	CQMA183J50
	C418	CQMA272J50
	C339, C340	CQMA393J50
	C102, C144	CQMA472J50
	C167	CQMA563J50
	C122	CQMA682J50
	C468	CQMA683J50
	C341, C342	CQMA822J50
	C121	CQSA181J50
	C484	CQSA471J50
	C479	CQSA821J50
	VC1 Ceramic trimmer	VCM-003

RESISTORS

Mark	Symbol & Description		Part No.
★	VR401	Semi-fixed (1kΩ)	VRTB6VS102
★	VR405	Semi-fixed (220Ω)	VRTB6VS221
★	VR403	Semi-fixed (470Ω)	VRTB6VS471
★	VR103, VR402	Semi-fixed (4.7 kΩ)	VRTB6VS472
★	VR101, VR105	Semi-fixed (47 kΩ)	VRTB6VS473
★	VR406	Semi-fixed (4.7 kΩ)	VRTG6VS472
	R25	Resistor array (10kΩx5)	RA5S103J
	R408		RD1/2PM221J
	R41, R42, R44—R48, R225—R229		RD1/4PM□□□J
	R205—R207, R333, R334, R338, R339		RD1/4VM□□□J
	R161—R164, R401, R402, R405, R406, R409, R410, R413, R414, R426, R471, R479, R611		RN1/6PQ□□□□F
		Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
★	X1	Ceramic resonator	KBR-4.0MS
★	X2	Crystal resonator	VSS1005
		RFMD	VWL1008
		Pin jack (VIDEO)	VKB-014
		IC socket (28 Pin)	VKH1001
		Mini pin jack (2P)	VKN1034

2FSB Assembly (VWV1040)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC202, IC203	BU4053B
★★	IC104	CXD1135Q
★★	IC105	CXK5816M-12L (CXK5816M-15L)
★★	IC1	M5F78M12L
★★	IC2	M5F79M12L
★★	IC204, IC205	M5238PF
★★	IC102, IC103	NJM082D
★★	IC301	NJM4558D
★★	IC3	NJM78L06A
★★	IC4	NJM79L06A
★★	IC501	NJU4053BD
★★	IC201	PCM56P-J
★★	IC106	PDE024
★★	IC101	TC40H004P
★★	IC206	TC74HC74P
★★	Q201	RN2203
★★	Q303, Q601	2SA933S
★★	Q304, Q305	2SB808
★★	Q202, Q203	2SD1302
★	D106	FC54M
★	D101	KV1226YBR
★	D1—D4	1SR35—100AVL
★	D5—D8, D107, D108, D301, D302, D304	1SS254

RELAY

Mark	Symbol & Description		Part No.
★★	RY301	Relay	VSR-005

COILS

Mark	Symbol & Description		Part No.
	VL101	Variable coil	VTL-275 (VTL1005)
	L101	Coil (4.7μH)	VTL1003
	L102		VTH-008

CAPACITORS

Mark	Symbol & Description	Part No.
	C201, C203	CCCCH220J50
	C118	CCCCH560J50
	C310, C311, C312	CCCSL101J50
	C226, C227	CCCSL121J50
	C212, C213	CCCSL221J50

Mark	Symbol & Description	Part No.
	C107, C214, C215	CCCSL331J50
	C119	CCCSL391J50
	C104, C120	CCCUJ221J50
	C103, C202	CCCUJ330J50
	C113	CEANP2R2M50
	C228, C229	CEANP220M10
	C110, C230	CEAS010M50
	C108, C109, C116, C117, C122	CEAS100M50
	C121, C123, C125, C206—C211	CEAS101M10
	C5, C6	CEAS221M10
	C3, C4	CEAS221M25
	C1, C2	CEAS222M25
	C105	CEAS470M25
	C112, C204, C205, C222—C225, C306, C307	CFTXA104J50
	C115	CFTXA474J50
	C216, C217	CFTXA683J50
	C101, C126, C127, C314	CGCYX473M25
	C313	CKCYB102K50
	C102, C503, C504	CKCYF103Z50
	C501, C502	CQMA102J50
	C111, C218, C219	CQMA103J50
	C220, C221	CQMA182J50
	C106	CQMA223J50
	C114	CQMA822J50

RESISTORS

Mark	Symbol & Description	Part No.
★	VR102, VR501 Semi-fixed (22kΩ)	VRTB6VS223
	R114, R115, R118, R120, R127, R128, R138	RN1/6PQ□□□□F
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
★	X101	Crystal resonator (16MHz)	VSS1004
		Pin jack (2P)	VKB-027

TNTR Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	Q201, Q202	RPI-38

RESISTORS

Mark	Symbol & Description	Part No.
	R201, R202	RD1/6PM472J

BLDB Assembly

SEMICONDUCTORS

Mark	Symbol & Description		Part No.
★★	IC301		TA8413P
★★	Q301	Transistor array	STA302A
★★	Q302	Transistor array	STA303A
★★	Q303—Q305		2SA1048
★	D301—D303		S2V10-4001

CAPACITORS

Mark	Symbol & Description	Part No.
	C301—C303 (33μF/50V)	VCH1034
	C304	CEAS4R7M50
	C305	CKCYF103Z50

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

FTSB Assembly (VYS1004)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC2, IC3	BA15218N
★★	IC1	HA11529
★★	IC6	IR3C02A
★★	IC4	NJM4556DE
★★	IC5	NJM4556S
★★	Q1, Q3	DTC363ES
★★	Q2	UN4112
★★	Q16	2SA933S
★★	Q5, Q8, Q10	2SB1185
★★	Q12	2SB1238X
★★	Q13, Q14	2SC1740S
★★	Q4, Q7, Q9	2SD1762
★★	Q11	2SD1859X
★★	Q6, Q17	2SK184
★	D1—D5	1SS254

CAPACITORS

Mark	Symbol & Description	Part No.
	C2	CCPUSL680J50
	C38	CEAL010M50
	C52, C53	CEAL220M6R3
	C24, C25	CEAL330M25
	C9, C37	CEANPR47M50
	C3, C56	CEJANP010M50
	C4, C18	CEJANP100M10
	C11	CEJANP220M10
	C28	CEJA010M50
	C48, C50	CEJA220M6R3
	C31, C32	CEJA330M25
	C54	CFTXA103J50
	C5, C17, C19, C33, C35	CFTXA104J50
	C15, C16	CFTXA184J50
	C21	CFTXA223J50

Mark	Symbol & Description		Part No.
	C7		CFTXA333J50
	C8, C14		CFTXA473J50
	C10, C13		CFTXA683J50
	C26		CKCYF103Z50
	C30		CKPUYB101K50
	C20, C23, C27, C34		CKPUYB102K50
	C1, C29		CKPUYB331K50
	C36, C39—C41, C45—C47, C49, C51		CKPUYF103Z25
	C12		CQMA272J50
	C55		CQMA472J50
	C44		CSZA220M10

RESISTORS

Mark	Symbol & Description		Part No.
★	VR1—VR3, VR6, VR7, VR11	Semi-fixed (4.7kΩ)	VRTB6VS472
★	VR10	Semi-fixed (2.2kΩ)	VRTB6VS222
	R128		RN1/6PQ5602F
	R82, R86, R93, R98		RD1/2PMF□□□J
		Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
	CN10	Side connector (23P)	VKN1013

FLKY Assembly (VYG1017)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC1	PDG012
★★	Q1, Q2	2SC2458
★	D1—D6	1SS254

SWITCHES

Mark	Symbol & Description		Part No.
★★	S1—S15	Tact switch (SEARCH/MEMORY, RANDOM PLAY, TIME DISPLAY, PROGRAM, AUTO PGM EDITING, 10 KEY)	VSC-012

CAPACITORS

Mark	Symbol & Description	Part No.
	C1	CEJA100M50
	C2	CEJA101M6R3
	C3	CKPUYF103Z25

RESISTORS

Mark	Symbol & Description		Part No.
	R1	Resistors array (10kΩx4)	RA4S103J
	R2, R3		RD1/6PM154J

OTHERS

Mark	Symbol & Description		Part No.
★	X1	Ceramic resonator	RSS1006
★	V1	Fluorescent tube	VAW1005
	CN57	Connector (20P)	VKN1017

CNNB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★	D101	1SS254

CAPACITORS

Mark	Symbol & Description	Part No.
	C105	CEJA470M6R3
	C104	CKPUYF103Z25

RESISTORS

Mark	Symbol & Description	Part No.
	R101	RD1/6PM103J
	R102—R104	RD1/4PM221J

OTHERS

Mark	Symbol & Description		Part No.
	CN56	Connector (20P)	VKN1020

IRKB Assembly

SWITCHES

Mark	Symbol & Description	Part No.
★★	S301—S306 Tact switch (OPEN/CLOSE, PLAY/PAUSE, SCAN, SKIP)	VSC-012

OTHERS

Mark	Symbol & Description		Part No.
		IR sensor unit	GP1U50V

HEPB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC201	NJM4556S

CAPACITORS

Mark	Symbol & Description	Part No.
	C201—C203	CGCYX473M25

RESISTORS

Mark	Symbol & Description		Part No.
★	VR201	Variable resistor (2P)	VCS1009
		Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
	JA201	Headphone jack	VKN1018

LFSB Assembly

SWITCH

Mark	Symbol & Description		Part No.
⚠ ★★	S1	Power switch	VSA-010

COIL

Mark	Symbol & Description		Part No.
⚠	L101	Line filter	VTL-157 (VTL-004)

CAPACITORS

Mark	Symbol & Description		Part No.
⚠	C101-C103	Ceramic capacitor (0.01/AC125V)	RCG-009

RESISTORS

Mark	Symbol & Description	Part No.
⚠	R101	RD1/2PM225J

SYPS Assembly (VYR1055)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC1	NJM4558S
★★	Q12, Q14, Q15	UN4212
★★	Q2, Q6, Q8	2SA933S
★★	Q5	2SB1052
★★	Q17	2SB1238X
★★	Q10	2SC1627
★★	Q1, Q7, Q9, Q13	2SC1740S
★★	Q16	2SC1847
★★	Q3, Q4, Q11	2SD1267
★	D8, D9	HZS5.6EB2
★	D10	HZS8.2EB2
★	D15	MTZ36C (MTZ36D)
★	D16	MTZ5.1B
★	D1, D2	RB-152LF
★	D11	S2K20
★	D12–D14	1SR35–100AVL
★	D3–D7	1SS254

COIL

Mark	Symbol & Description		Part No.
	L1	Coil	VTT-070

CAPACITORS

Mark	Symbol & Description		Part No.
	C18		CCCSL331J50
	C22		CCCSL471J50
	C9, C10, C13, C17, C29		CEAS100M50
	C16, C27, C28		CEAS101M50
	C23		CEAS3R3M50
	C7, C8		CEAS470M25
	C14, C15		CEAS470M50
	C21		CKCYB102K50
	C1, C2, C11, C12, C30, C31		CKCYF103Z50
	C19		CQMA183J50
	C26		CQMA472J50
	C3, C4	(2200μF/25V)	PHC1027
	C6	(4700μF/10V)	VCH1003
	C5	(6800μF/10V)	VCH1046

RESISTORS

Mark	Symbol & Description	Part No.
	R27	RS1PMFR51J
	R26	RS1PMF2R7J
	R39	RS1PMF3R3J
	R42, R43	RD1/2PMF3R3J
	R1, R2	RD1/2PM471J
	R28–R31	RN1/6PQ□□□□F
	Other resistors	RD1/6PM□□□J

LMCB Assembly

SEMICONDUCTORS

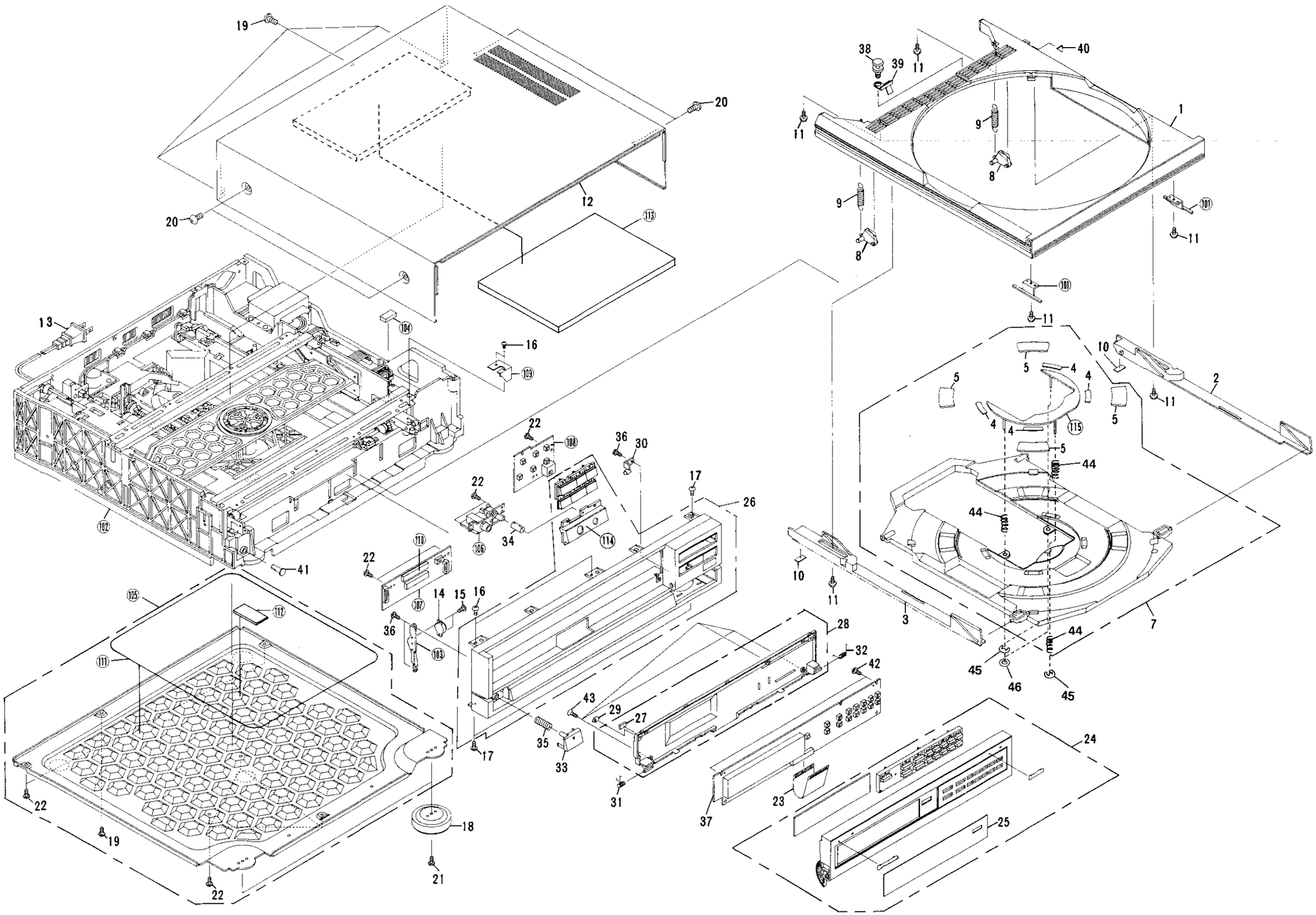
Mark	Symbol & Description	Part No.
★★	IC1	TA7291P
★	D1	HZS9B3

CAPACITORS

Mark	Symbol & Description	Part No.
	C1	CGDYX473M25
	C3	CEAS100M50

RESISTORS

Mark	Symbol & Description	Part No.
	R1	RD1/4VM222J
	R2	RD1/4VM220J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111
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101
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101
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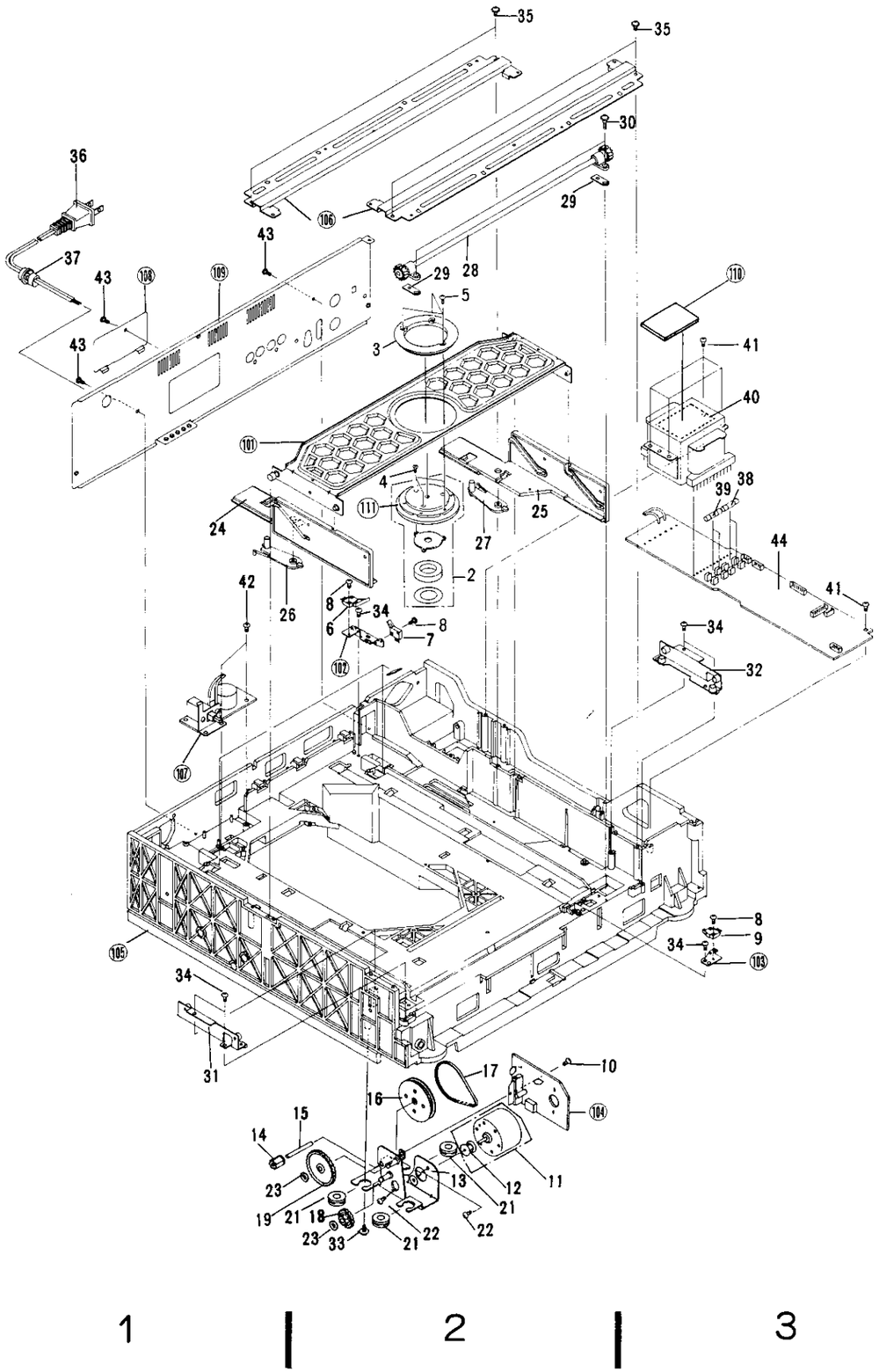
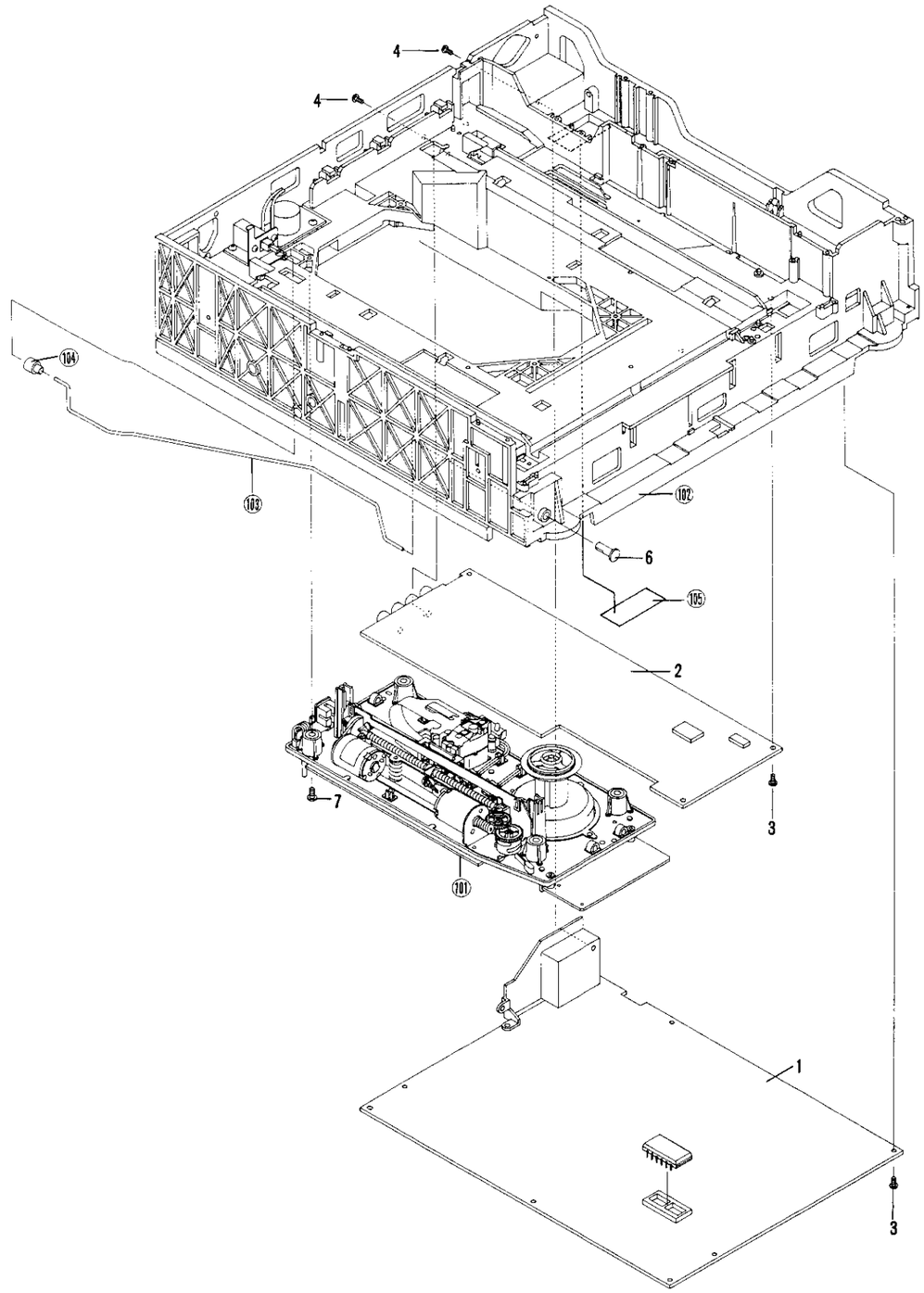
3.2 TOP VIEW



Parts List of Top View

Mark	No.	Part No.	Description	Mark	No.	Part No.	Description
	1.	. . .	. . .		101.		Clamper holder assembly
	2.	VXX1156	Disc clamper assembly-S		102.		Switch holder (A)
	3.	VNL1130	Clamper head		103.		Switch holder (B)
	4.	CMZ20P050FCU	Screw		104.		LMCB assembly
	5.	BPZ26P060FCU	Screw		105.		Base
★★	6.	VSK-010	Slide switch (S2) (TABLE/IN)		106.		Reinforcement bridge
★★	7.	VSK1003	Slide switch (S1) (TABLE/PARK)		107.		LFSB assembly
	8.	BMZ20P080FCU	Screw		108.		Rear cover
★★	9.	VSK-012	Slide switch (S3) (TABLE/OUT)		109.		Rear panel
	10.	VEC-143	Plastic rivet		110.		Transformer cushion
					111.		Disc clamper assembly
★★	11.	VXX1084	Loading motor assembly-S				
	12.	VNL1051	Motor pulley				
	13.	VXA1088	Motor base assembly				
	14.	VNL1020	Gear (A)				
	15.	VLL1037	Gear shaft				
	16.	VXA-477	Pulley (L) assembly				
	17.	VEB-125	Synchronized belt L				
	18.	VNL1010	Gear (C)				
	19.	VNL1064	Gear (B)				
	20.	. . .	. . .				
	21.	VEB1025	Rubber bushing				
	22.	PMA26P040FCU	Screw				
	23.	WT32D060D050	Washer				
	24.	VNL1068	Clamper cam (L)				
	25.	VNL1069	Clamper cam (R)				
	26.	VNL1070	Rock lever (L)				
	27.	VNL1071	Rock lever (R)				
	28.	VXA1163	Synchronized gear assembly				
	29.	VEB1026	Dumper sheet				
	30.	VBA1002	Screw				
	31.	VXA1161	Roller plate (L) assembly				
	32.	VXA1162	Roller plate (R) assembly				
	33.	VBA1003	Screw				
	34.	BPZ30P080FCU	Screw				
	35.	APZ30P080FCU	Screw				
⚠	36.	VDG1012	AC Power cord				
	37.	CM-22C	Strain relief				
⚠ ★★	38.	VEK-018	Fuse (3A) (FU1, FU2)				
⚠ ★★	39.	VEK-022	Fuse (2A) (FU3, FU4)				
⚠ ★	40.	VTT1026	Power transformer				
	41.	APZ30P080FCU	Screw				
	42.	BPZ30P080FCU	Screw				
	43.	BPZ30P080FBR	Screw				
	44.	VYR1055	SYPS assembly				

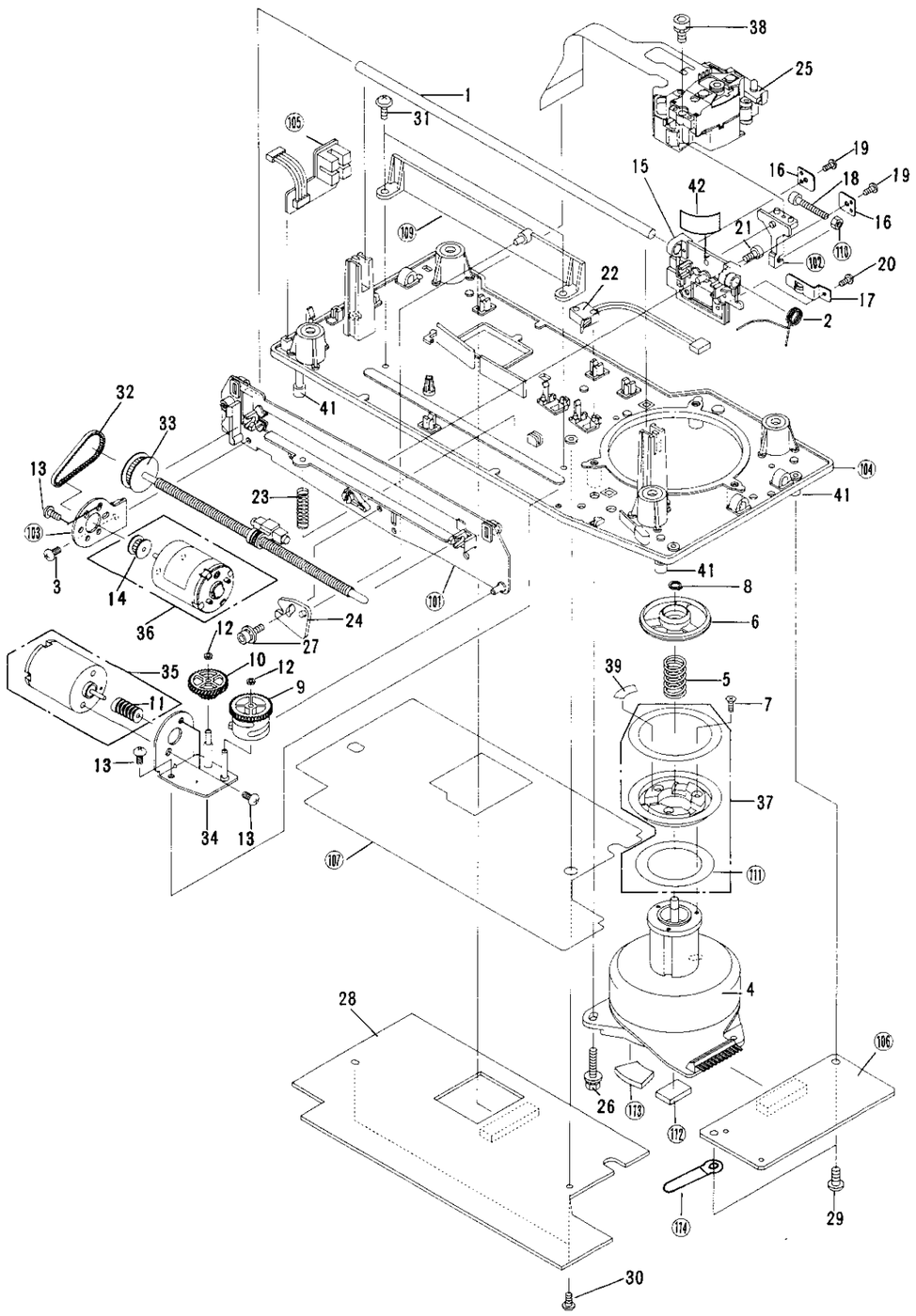
3.3 BOTTOM VIEW



Parts List of Bottom View

Mark	No.	Part No.	Description
◉	1.	VWS1025	VSOP assembly
◉	2.	VWV1040	2FSB assembly
	3.	BPZ30P080FCU	Screw
	4.	BPZ30P080FBR	Screw
	5.	. . .	. . .
	6.	VNL1084	PSW cap
	7.	VBA1004	Screw
	101.		Mechanism assembly
	102.		Base
	103.		PSW joint
	104.		Joint cap
	105.		Cover

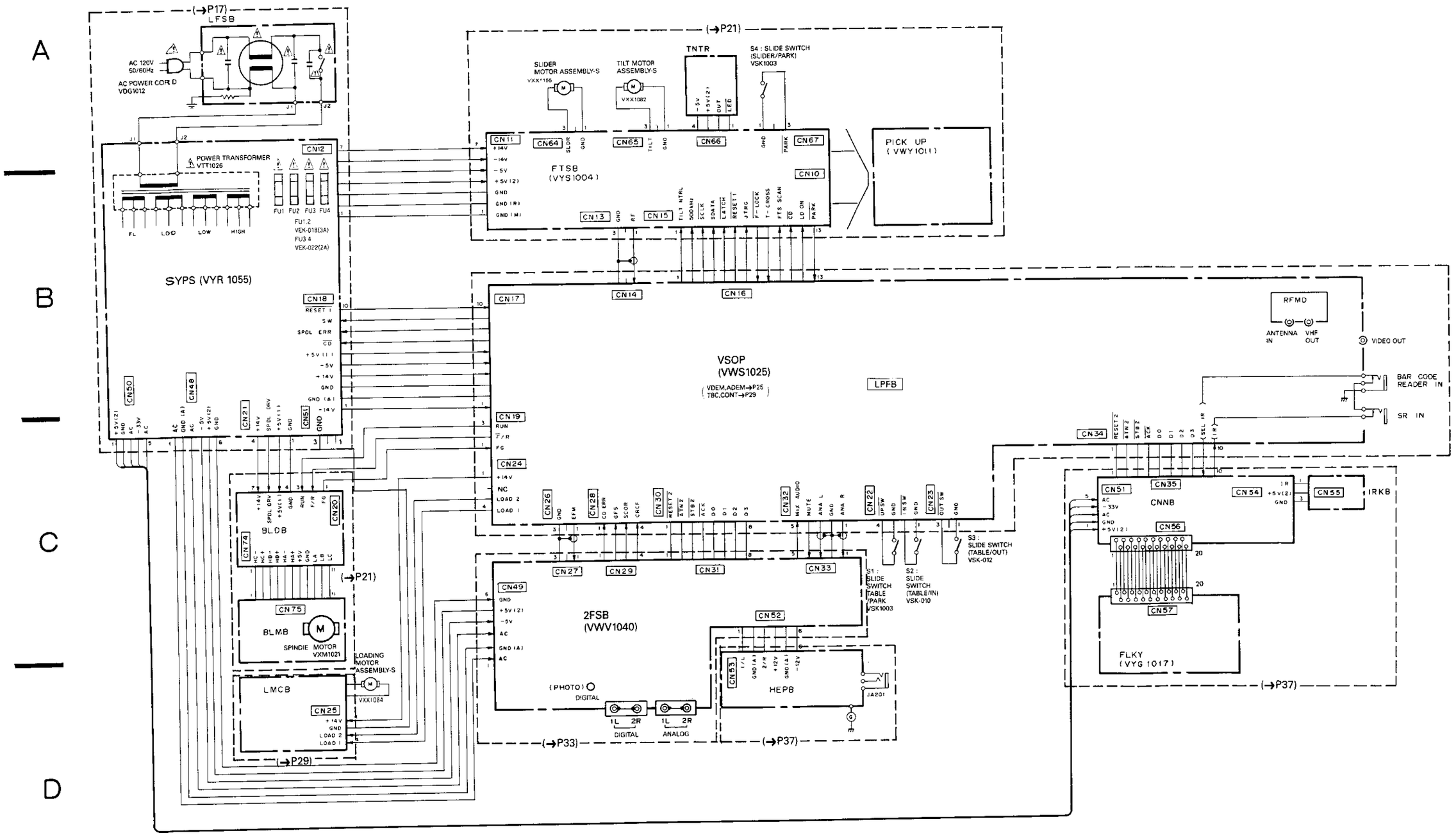
3.4 MECHANISM ASSEMBLY VIEW



Parts List of Mechanism Assembly

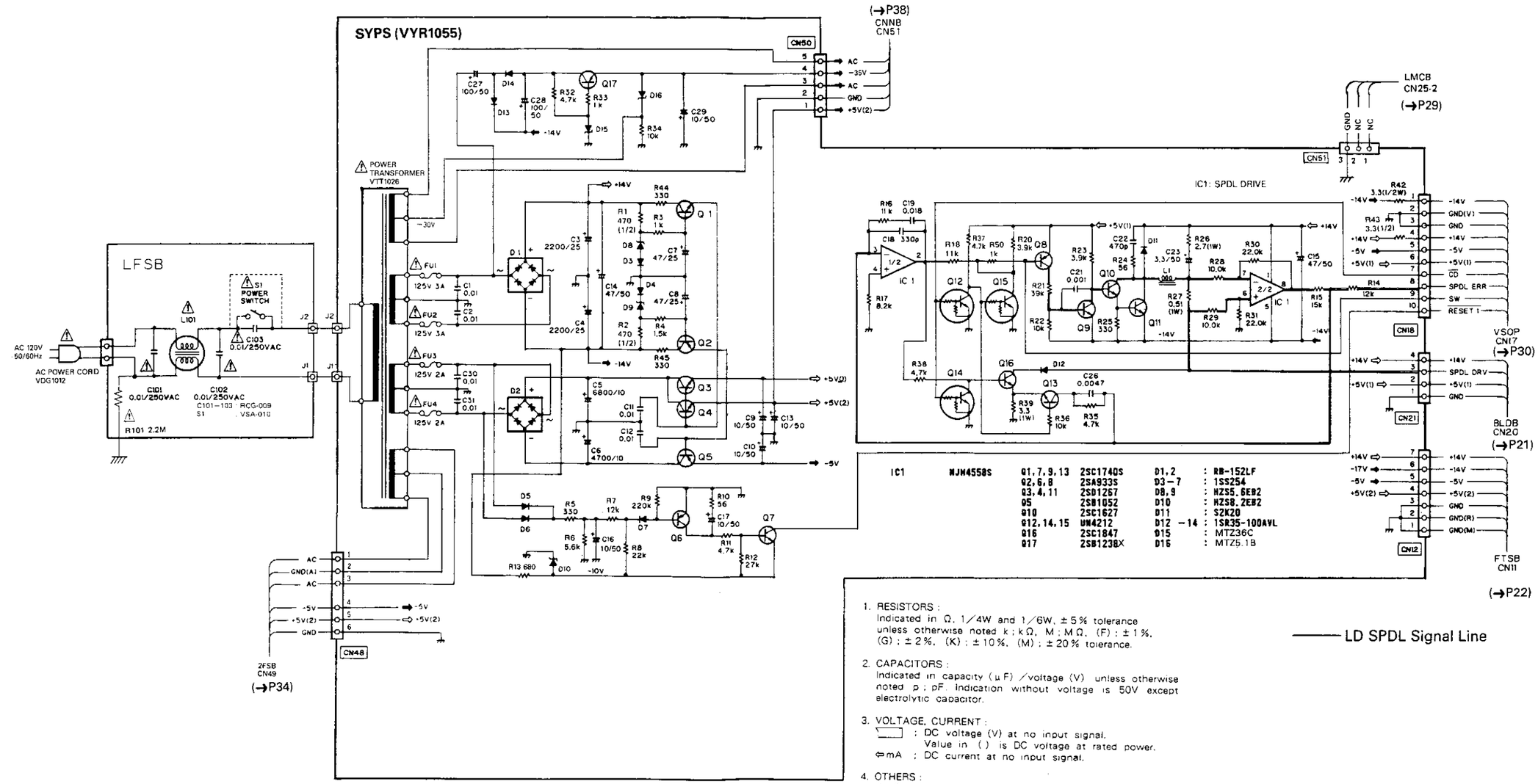
Mark	No.	Part No.	Description	Mark	No.	Part No.	Description
	1.	VLL1058	Carriage shaft		101.		Tilt base
	2.	VBH1040	Slider spring		102.		PU holder
	3.	PMA30P060FCU	Screw		103.		M holder
★★	4.	VXM1021	Spindle motor		104.		Mechanism base
	5.	VBH1024	Centering spring		105.		TNTR assembly
	6.	VNT1003	Centering hab		106.		BLDB assembly
	7.	CMZ20P080FCU	Screw		107.		FTS sheet
	8.	YC40FBT	Washer		108.		. . .
	9.	VNL1079	Cam gear		109.		Base plate
	10.	VNL1078	Gear		110.		Nut
	11.	VNL1085	Worm		111.		Insulator sheet
	12.	WT21D050D050	Washer		112.		Dump cushion
	13.	PMA30P040FCU	Screw		113.		Cushion E
	14.	VNL1051	Motor pulley		114.		Cord clamper
	15.	VNL1080	Slider				
	16.	VNE1100	Rock plate				
	17.	VXA1159	Roller assembly				
	18.	SMZ30H250FBT	Screw				
	19.	PPZ20P050FMC	Screw				
	20.	PMA20P040FCU	Screw				
	21.	SMZ30H080FBT	Screw				
★★	22.	VSK1003	Slide switch (SLIDER/PARK) (S4)				
	23.	VBH1022	Tilt spring				
	24.	VNL1077	Fulcrum cam				
	25.	VWY1011	Pick-up assembly				
	26.	VLL1065	Bolt 3 x 18				
	27.	VLL-378	Bolt 8				
◉	28.	VYS1004	FTSB assembly				
	29.	IPZ30P080FCU	Screw				
	30.	BPZ30P080FCU	Screw				
	31.	PMB30P060FCU	Screw				
	32.	VEB1029	Timing belt				
	33.	VXA1129	Screw nut assembly				
	34.	VXA1106	TL base assembly				
★★	35.	VXX1082	Tilt motor assembly-S				
★★	36.	VXX1155	Slider motor assembly-S				
	37.	VXX1071	Turntable assembly-S				
	38.	VLL1107	Bolt 2.6 x 6				
	39.	VEB1032	Sheet				
	40.	. . .	. . .				
	41.	VEB1017	Rubber tube				
	42.	VBK1010	SN spring				

4. CONNECTION DIAGRAM



5. SCHEMATIC DIAGRAM AND P.C. BOARD PATTERNS

5.1 LFSB AND SYPS ASSEMBLY



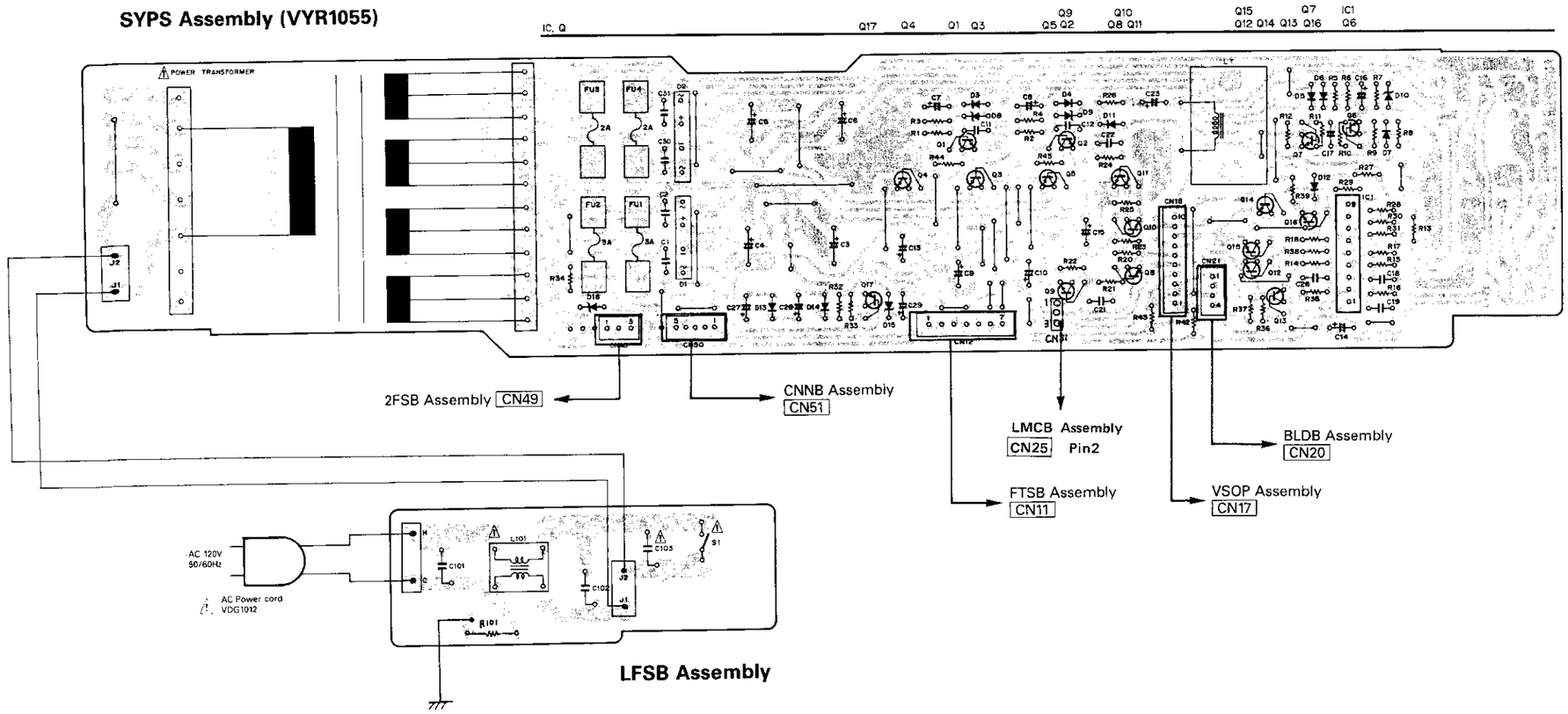
IC1	MJM4558S	Q1, 7, 9, 13	2SC1740S	D1, 2	: RB-152LF
		Q2, 6, 8	2SA933S	D3–7	: 1SS254
		Q3, 4, 11	2SD1267	D8, 9	: HZS5.6EB2
		Q5	2SB1052	D10	: HZS8.2EB2
		Q10	2SC1627	D11	: S2K20
		Q12, 14, 15	UN4212	D12 –14	: 1SR35-100AVL
		Q16	2SC1847	D15	: MTZ36C
		Q17	2SB1238X	D16	: MTZ5.1B

1. RESISTORS :
   Indicated in Ω, 1/4W and 1/6W, ±5% tolerance unless otherwise noted k : kΩ, M : MΩ, (F) : ±1%, (G) : ±2%, (K) : ±10%, (M) : ±20% tolerance.
2. CAPACITORS :
   Indicated in capacity (μF) /voltage (V) unless otherwise noted p : pF. Indication without voltage is 50V except electrolytic capacitor.
3. VOLTAGE, CURRENT :
   ▭ : DC voltage (V) at no input signal.
   Value in ( ) is DC voltage at rated power.
   ⇦mA : DC current at no input signal.
4. OTHERS :
   ➡ : Signal route.
   ⊘ : Adjusting point.
   The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
   ※ marked capacitors and resistors have parts numbers.

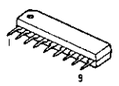
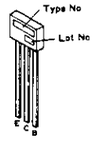
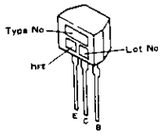
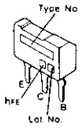
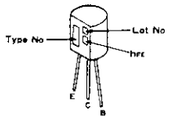
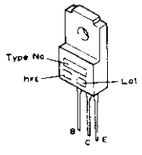
   This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

——— LD SPDL Signal Line

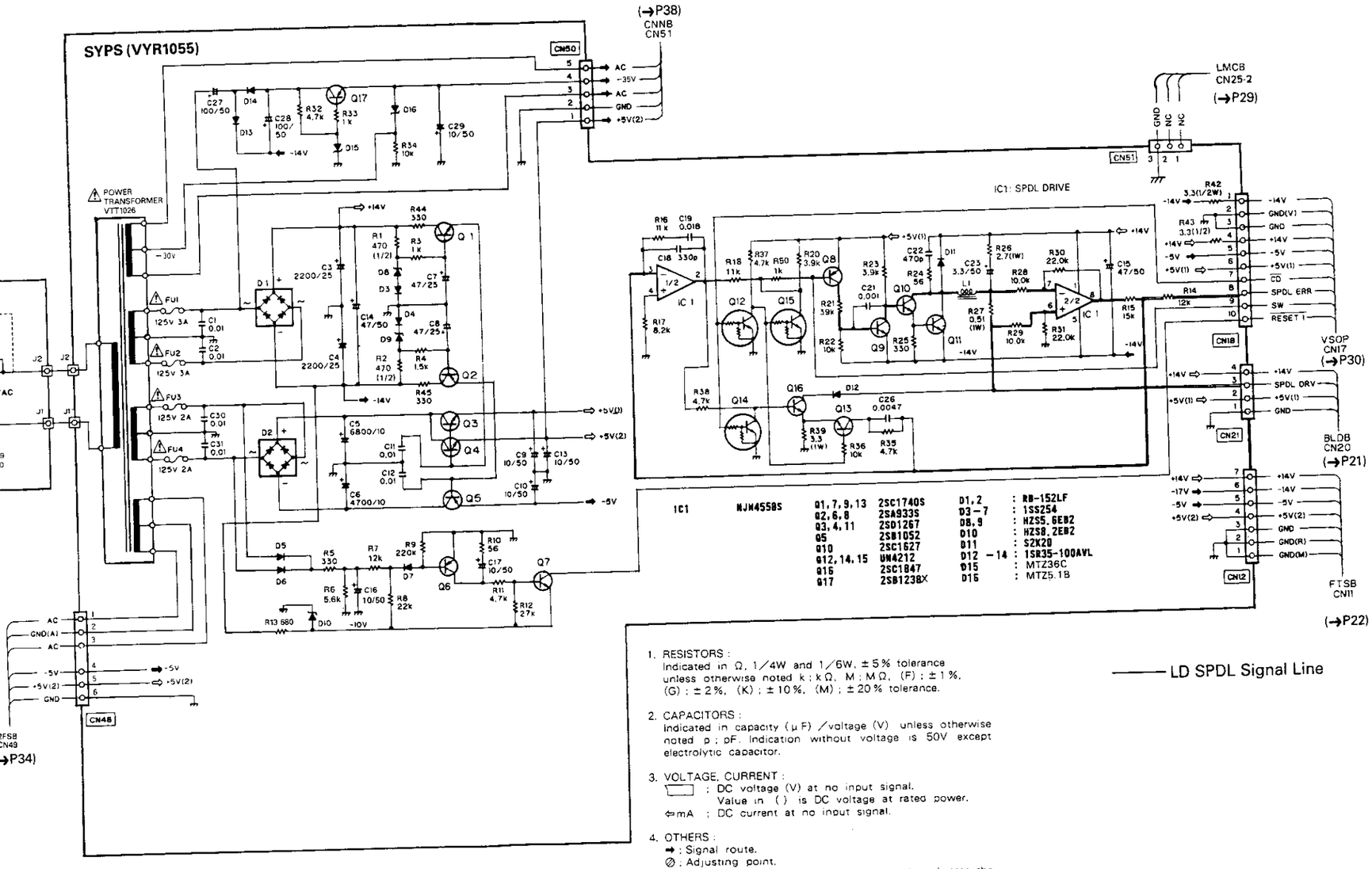
SYPS Assembly (VYR1055)



LFSB Assembly

NJM4458S	UN4212	2SA993S 2SC1740S	2SC1847	2SB1238X	2SC1627	2SB1052 2SD1267
						

M AND P.C. BOARD PATTERNS



IC1	NJM4558S	Q1, 7, 9, 13	2SC1740S	D1, 2	: RB-152LF
		Q2, 6, 8	2SA933S	D3 – 7	: 1SS254
		Q3, 4, 11	2SD1267	D8, 9	: HZS5.6EB2
		Q5	2SB1052	D10	: HZS8.2EB2
		Q10	2SC1627	D11	: S2K20
		Q12, 14, 15	UN4212	D12 – 14	: 1SR35-100AVL
		Q16	2SC1847	D15	: MTZ36C
		Q17	2SB123BX	D16	: MTZ5.1B

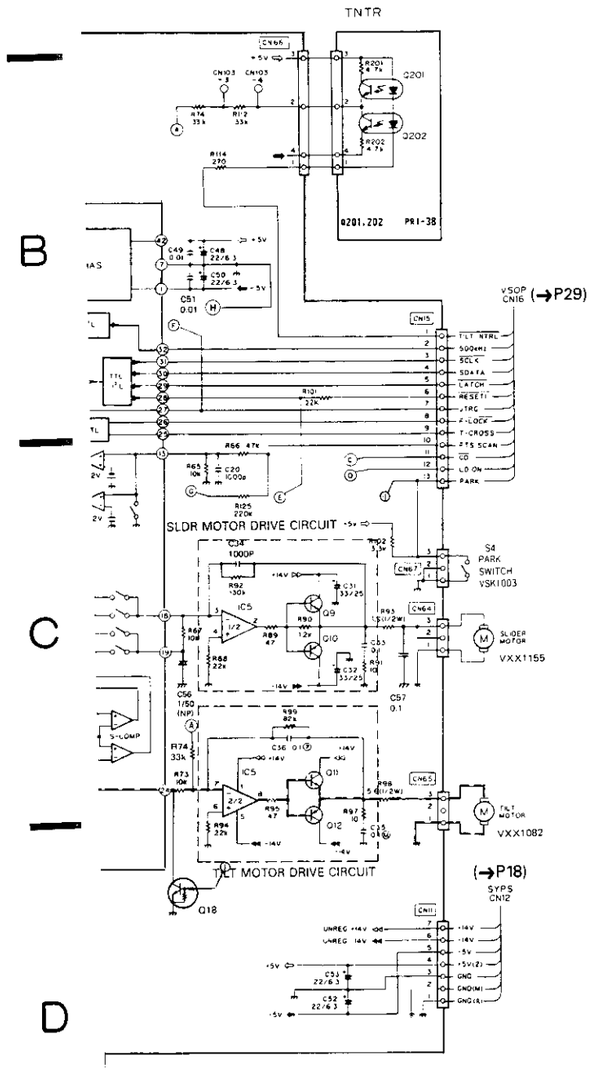
1. RESISTORS :
   Indicated in Ω, 1/4W and 1/6W, ±5% tolerance unless otherwise noted k : kΩ, M : MΩ, (F) : ±1%, (G) : ±2%, (K) : ±10%, (M) : ±20% tolerance.

2. CAPACITORS :
   Indicated in capacity (μF) /voltage (V) unless otherwise noted p : pF. Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE, CURRENT :
   ▭ : DC voltage (V) at no input signal.
   Value in ( ) is DC voltage at rated power.
   ⇦mA : DC current at no input signal.

4. OTHERS :
   ➡ : Signal route.
   ⊘ : Adjusting point.
   The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
   ※ marked capacitors and resistors have parts numbers.

   This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.



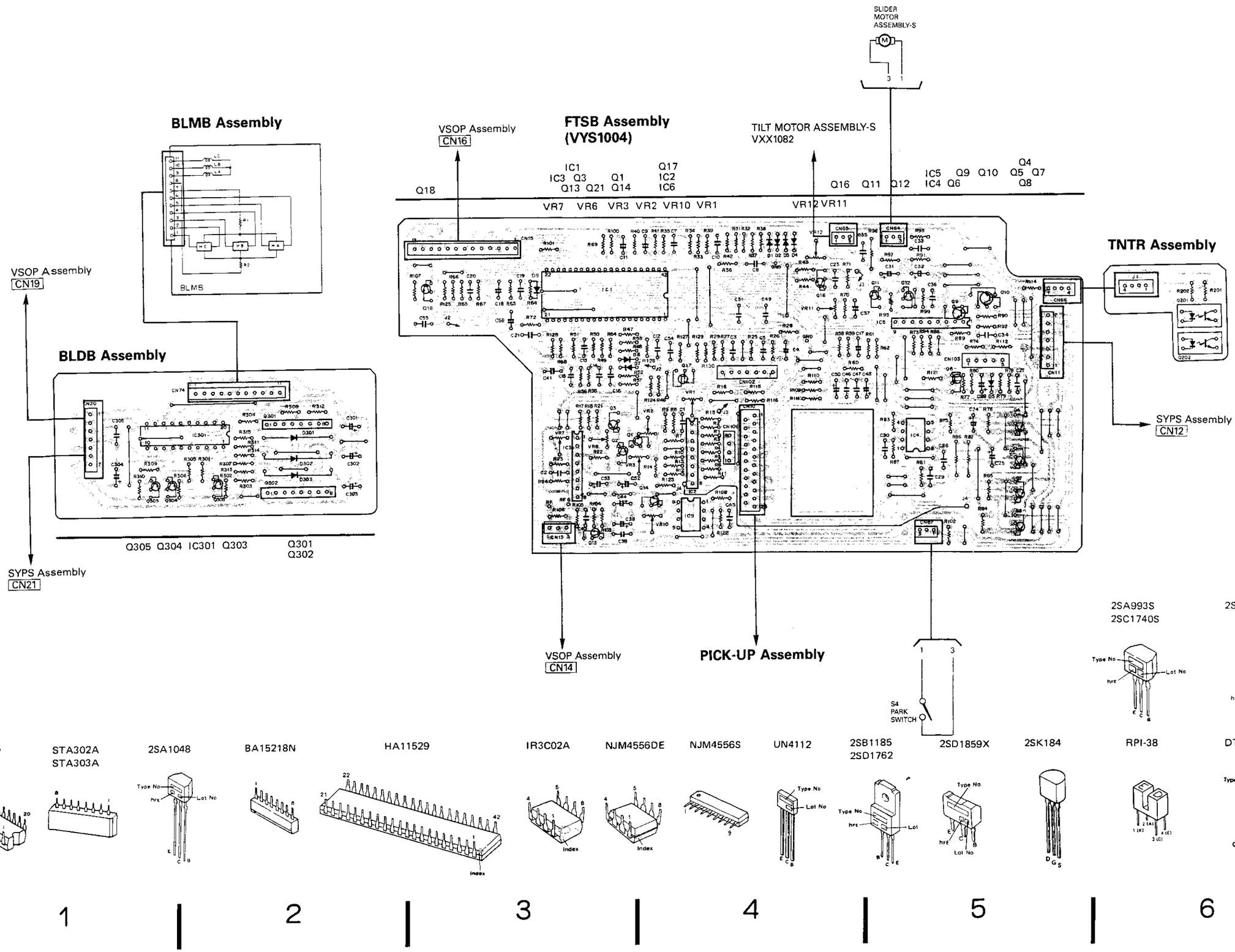
——— LD SPDL Signal Line

——— FOCS SERVO Signal Line

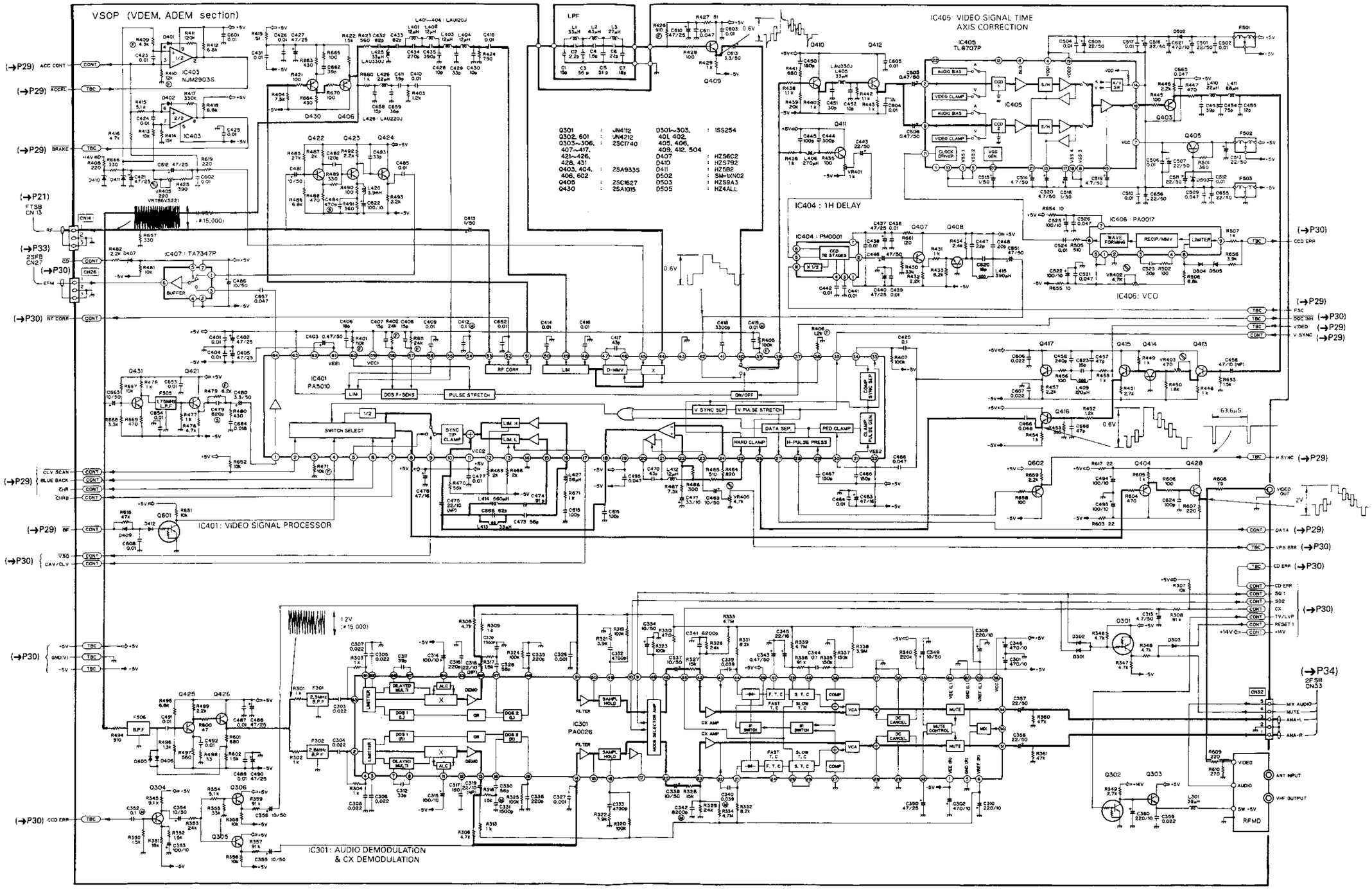
- - - - - - - TILT SERVO Signal Line

——— SPDL SERVO Signal Line

- - - - - - - RF Signal Line


BLMB Assembly
BLMS
VSOP Assembly
CN19
BLDB Assembly
Q305 Q304 IC301 Q303
Q301
Q302
SYPS Assembly
CN21
FTSB Assembly
(VYS1004)
VSOP Assembly
CN16
Q18
IC1
IC3 Q3
Q13 Q21 Q14
Q1
Q17
IC2
IC6
VR7 VR6 VR3 VR2 VR10 VR1
VR12 VR11
Q16 Q11 Q12
IC5 Q9 Q10
IC4 Q6
Q4
Q5 Q7
Q8
SLIDER
MOTOR
ASSEMBLY-S
TILT MOTOR ASSEMBLY-S
VXX1082
TNTR Assembly
SYPS Assembly
CN12
VSOP Assembly
CN14
PICK-UP Assembly
S4
PARK
SWITCH
2SA993S
2SC1740S
2SB1238X
TA8413P
STA302A
STA303A
2SA1048
BA15218N
HA11529
IR3C02A
NJM4556DE
NJM4556S
UN4112
2SB1185
2SD1762
2SD1859X
2SK184
RPI-38
DTC363ES

5.3 VSOP (VDEM, ADEM) AND LPFB ASSEMBLY (VWS1025)



1 2 3 4 5 6

A B C D

VSOP Assembly (VWS1025)

LMCB Assembly
CN25

FTSB Assembly
CN15

S2 : INP SWITCH
S1 : UP SWITCH
S3 : OUT SWITCH

LPFB Assembly

2FSB Assembly
CN29

SYPS Assembly
CN18

CNNB Assembly
CN35

2FSB Assembly
CN31

2FSB Assembly
CN27

FTSB Assembly
CN13

BLDB Assembly
CN20

2FSB Assembly
CN33

CLD-1030

PA0026

PA5010

NJM2903S
PA0017

PM0001

TL8707P

TA7347P

UN4112
UN4212

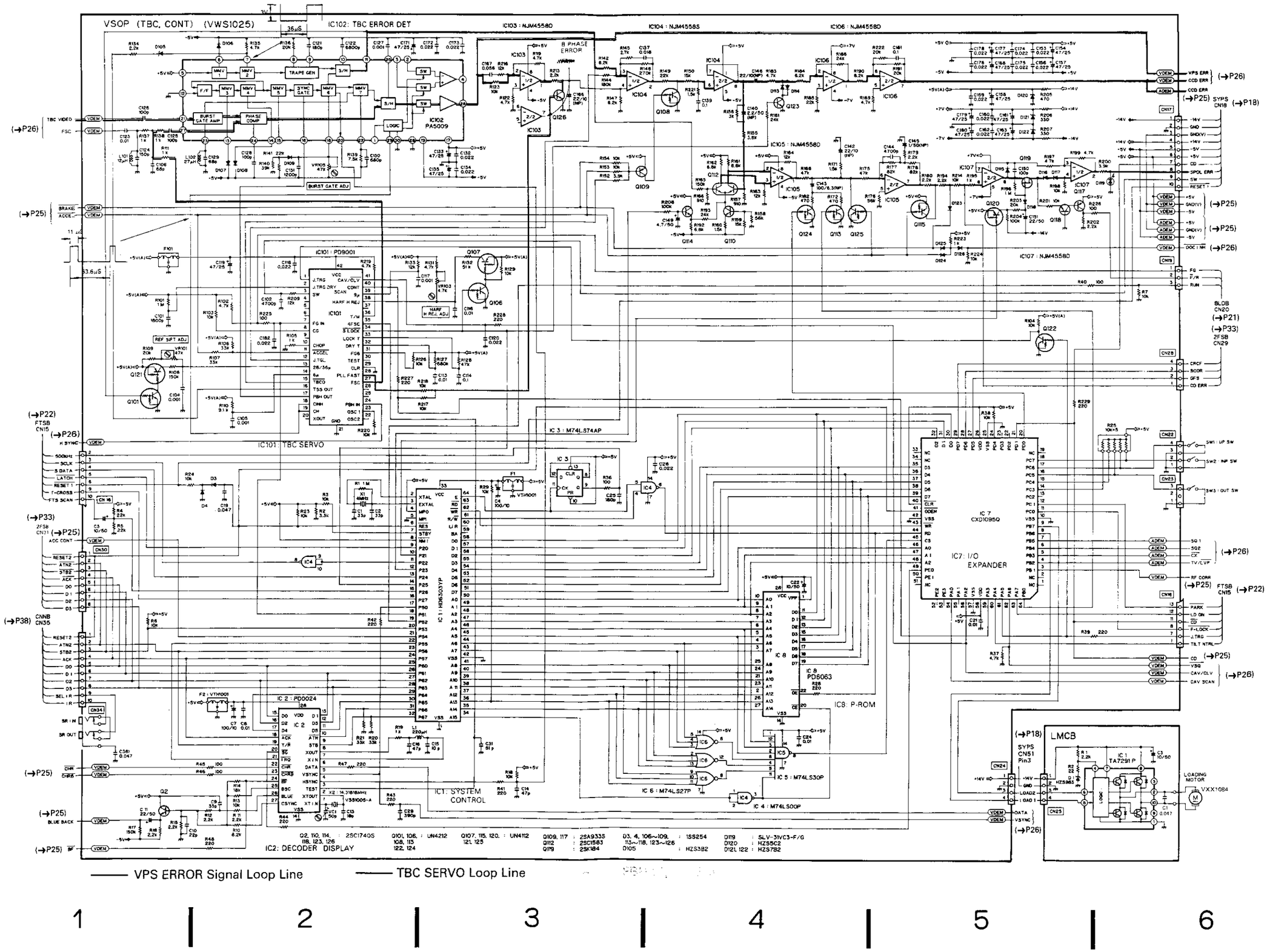
2SA1015
2SC1627

2SA933S
2SC1740S

2SC1583

2SA1015

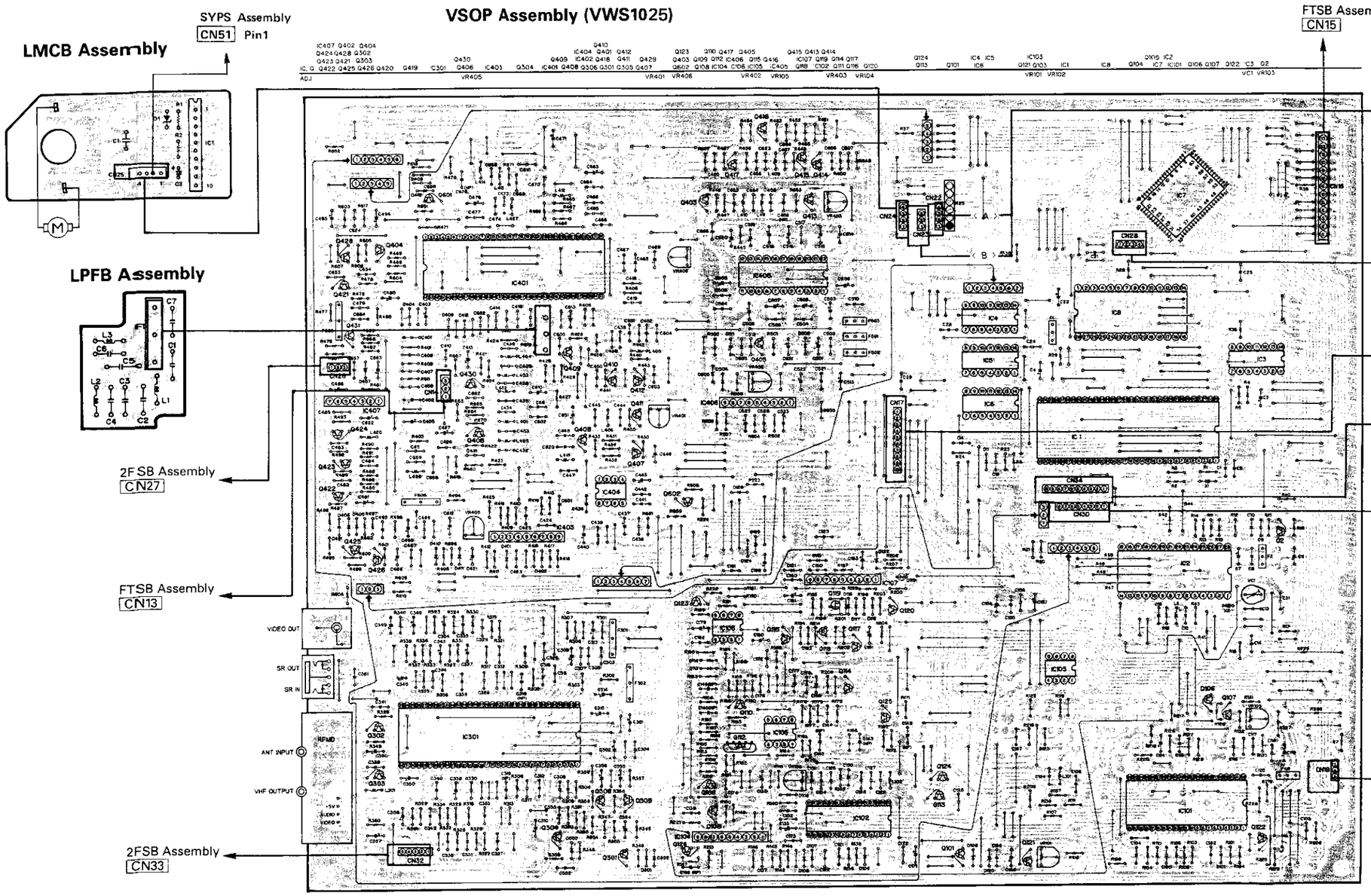
5.4 VSOP (TBC, CONT) AND LMCB ASSEMBLY (VWS1025)



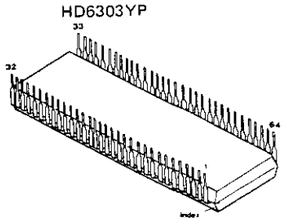
1 2 3 4 5 6

A B C D

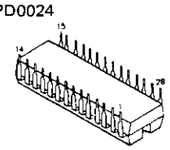
VSOP Assembly (VWS1025)



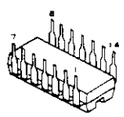
HD6303YP



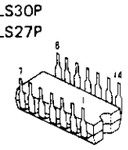
PD6063
PD0024



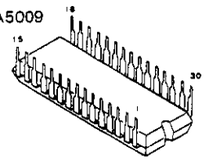
M74LS74AP



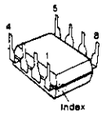
M74LS00P
M74LS30P
M74LS27P



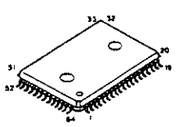
PA5009



NJM4558D

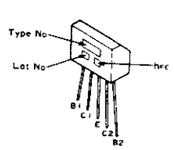


CXD1095Q

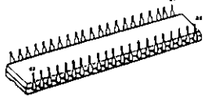


2SK184

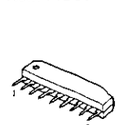
2SC1583



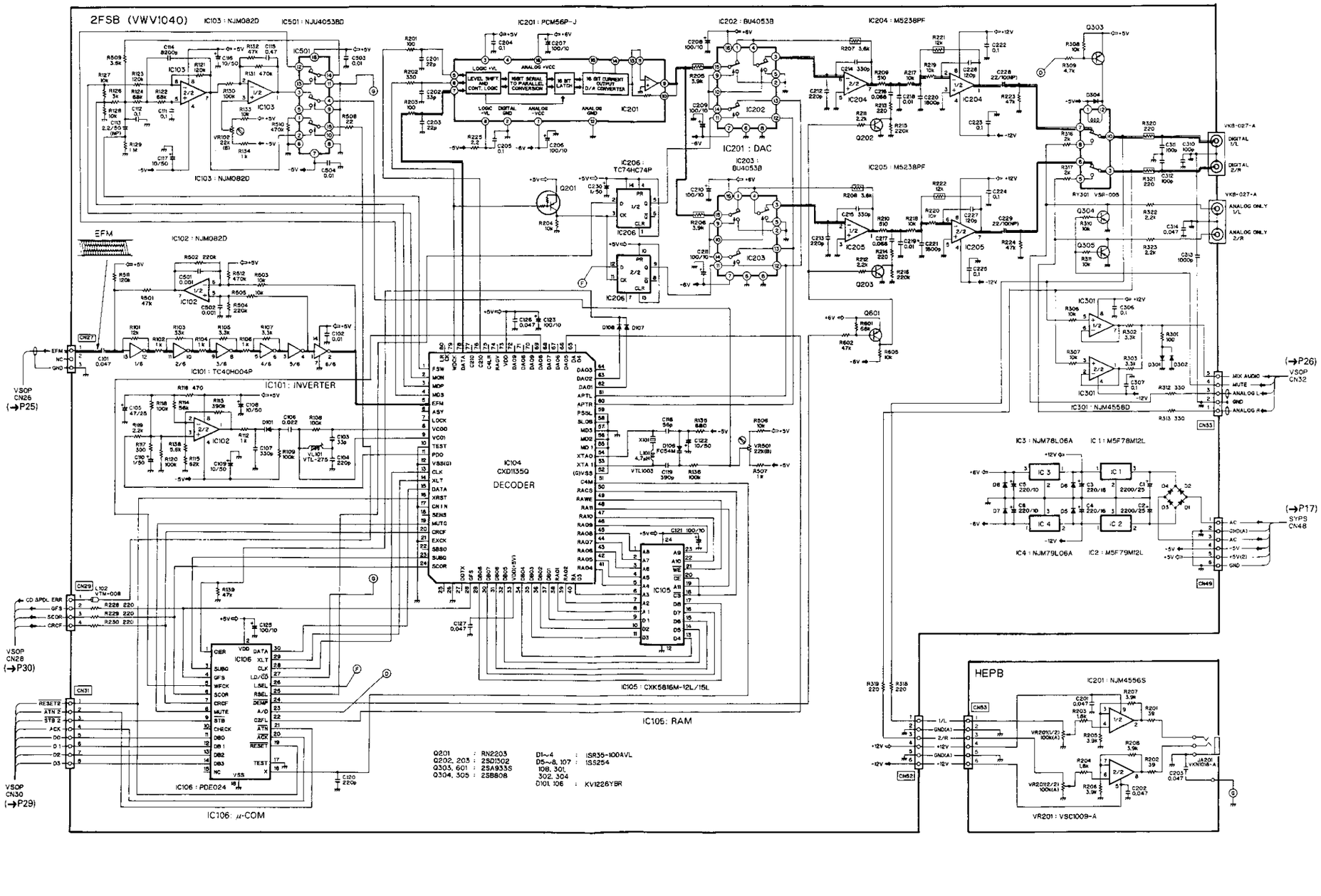
PD9001



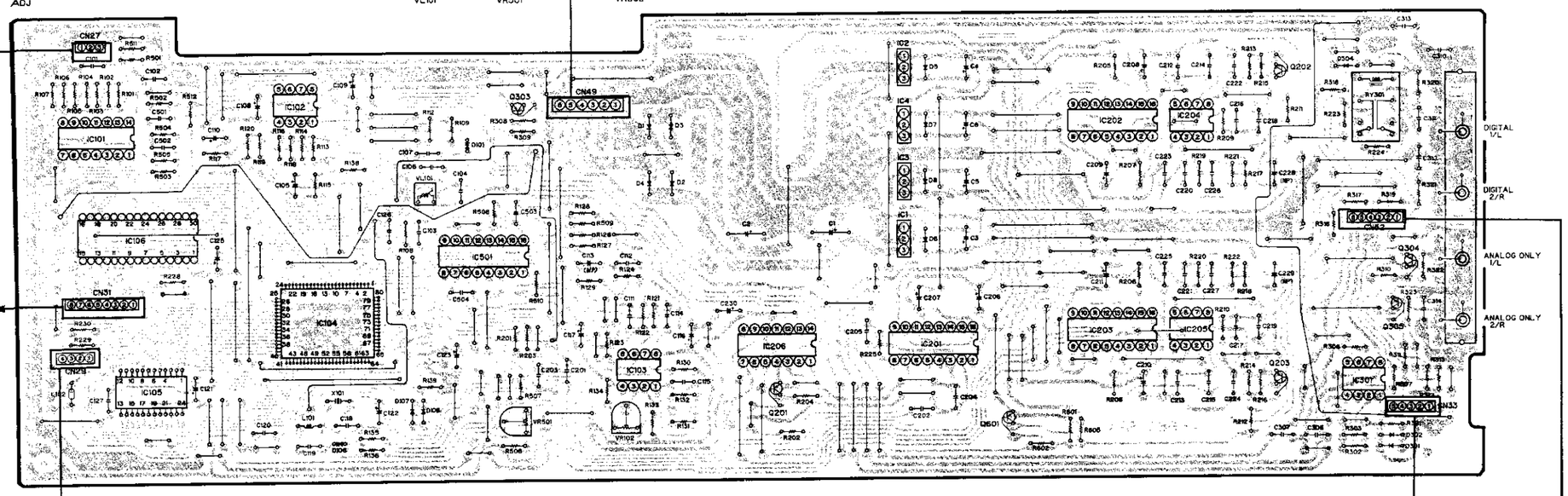
NJM4458S



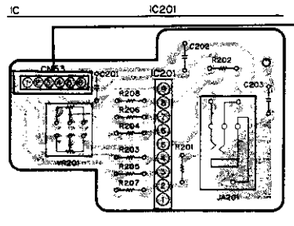
5.5 2FSB ASSEMBLY



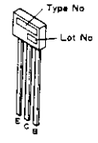
2FSB Assembly (VWV1040)



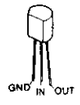
HEPB Assembly



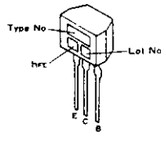
RN2203



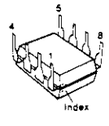
NJM79L06A



2SA933S

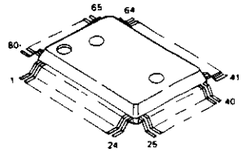


NJM4558D

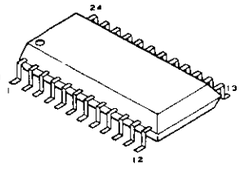


2SB808

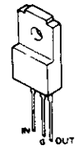
CXD1135Q



CXK5816M-12L
CXK5816M-15L



M5F78M12L



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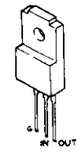
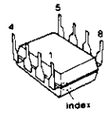
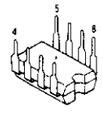


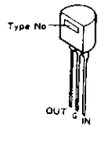
NJM082D



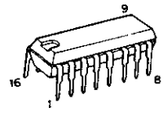
M5238PF



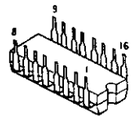
NJM78L06A



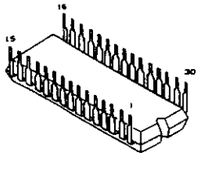
NJU4053BD



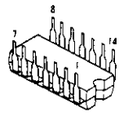
PCM56P
BU4053B
TC40H004P



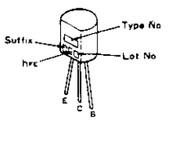
PDE024



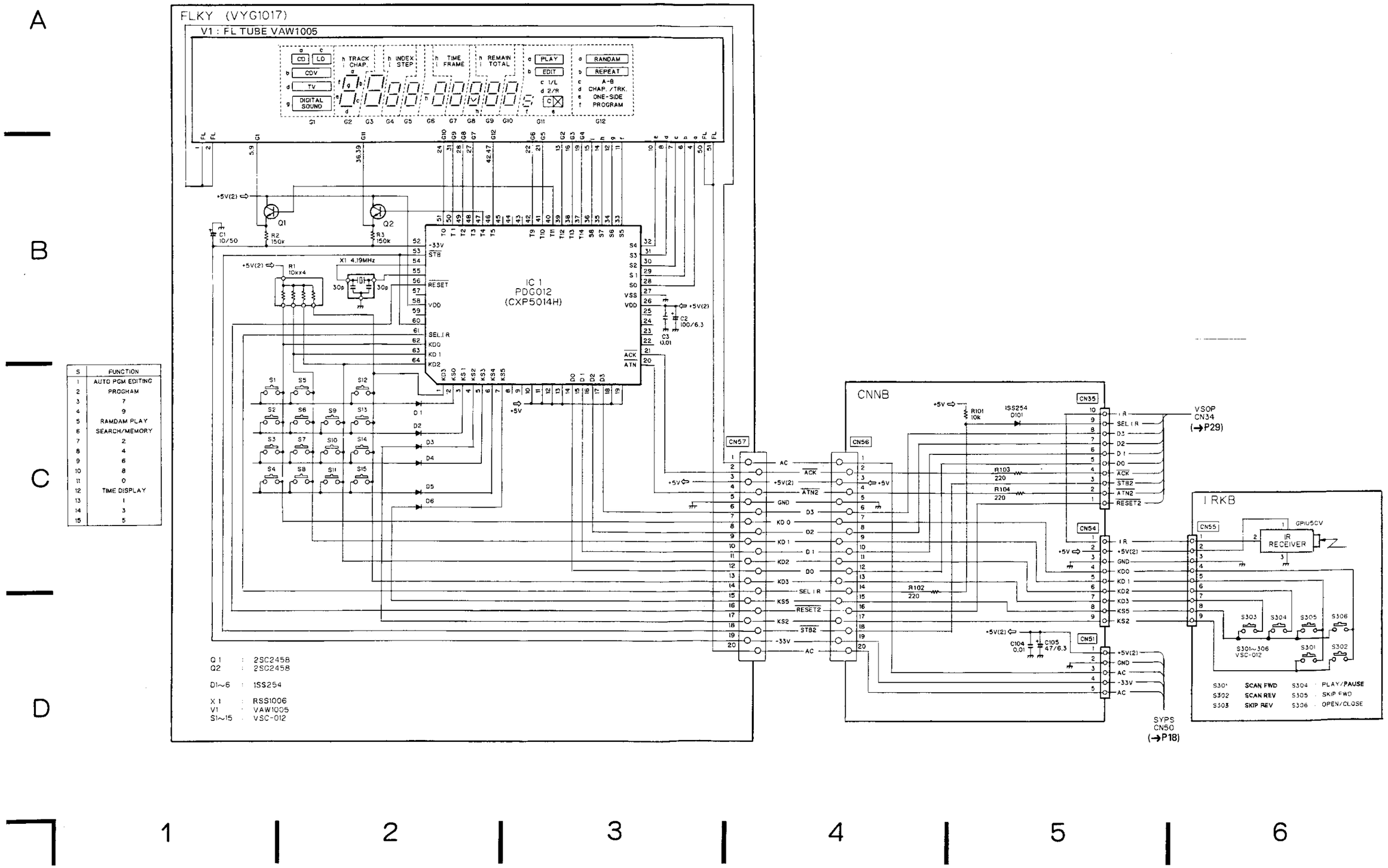
TC74HC74P



2SD1302

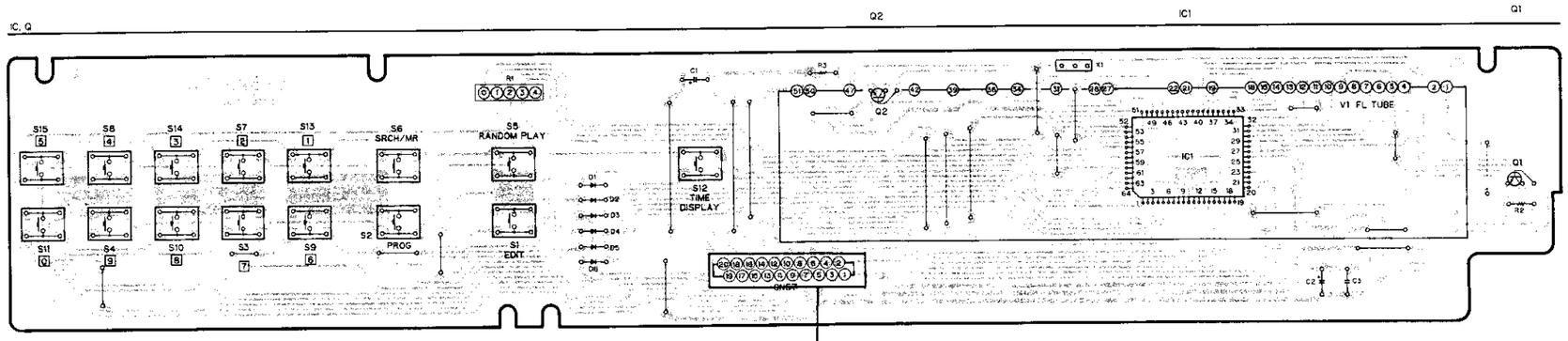


5.6 HEPB, FLKY, IRKB AND CNNB ASSEMBLY



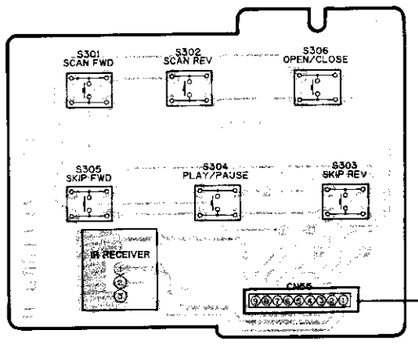
S	FUNCTION
1	AUTO PGM EDITING
2	PROGRAM
3	7
4	9
5	RAMDAM PLAY
6	SEARCH/MEMORY
7	2
8	4
9	6
10	8
11	0
12	TIME DISPLAY
13	1
14	3
15	5

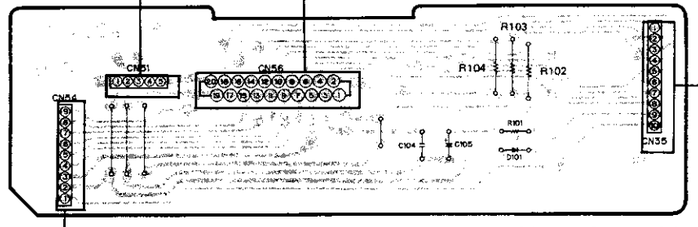
FLKY Assembly (VYG1017)



SYPS Assembly
CN50

IRKB Assembly

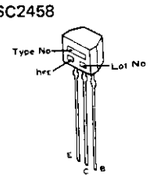




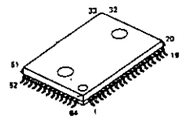
VSOP Assembly
CN34

CNNB Assembly

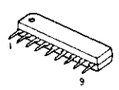
2SC2458



PDG012



NJM4556S



6. ELECTRICAL PARTS LIST

NOTES:

- *Parts without part number cannot be supplied.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *For your parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★ GENERALLY MOVES FASTER THAN ★
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560Ω	*56 × 10¹*	*561*	*RD1/4PS 5 6 1 J*
47kΩ	*47 × 10³*	*473*	*RD1/4PS 4 7 3 J*
0.5Ω	*0R5*		*RN2H 0 R 5 K*
1Ω	*010*		*RS1P 0 1 0 K*

Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62kΩ	*562 × 10¹*	*5621*	*RN1/4SR 5 6 2 1 F*

Miscellaneous Parts

P.C. BOARD ASSEMBLIES

Mark	Symbol & Description	Part No.
	LPFB assembly	
	VSOP assembly	VWS1025
	2FSB assembly	VWV1040
	TNTR assembly	
	BLDB assembly	
	FTSB assembly	VYS1004
	FLKY assembly	VYG1017
	CNNB assembly	
	IRKB assebmly	
	HEPB assembly	
	LFSB assembly	
	SYPS assembly	VYR1055
	LMCB assembly	
	BLMB assembly	

OTHERS

Mark		Symbol & Description		Part No.
			Fuji card	VDA1051
⚠			AC Power cord	VDG1012
			Strain relief	CM-22C
⚠	★★	FU1, FU2	Fuse (3A)	VEK-018
⚠	★★	FU3, FU4	Fuse (2A)	VEK-022
	★★	S1	Slide switch (TABLE/PARK)	VSK1003
	★★	S2	Slide switch (TABLE/IN)	VSK-010
	★★	S3	Slide switch (TABLE/OUT)	VSK-012
	★★	S4	Slide switch (SLIDER/PARK)	VSK1003
	★★		Loading motor assembly-S	VXX1084
	★★		Spindle motor	VXM1021
			Pick-up assembly	VWY1011
	★★		Tilt motor assembly-S	VXX1082
	★★		Slider motor assembly-S	VXX1155
⚠	★		Power transformer	VTT1026

LPFB Assembly

COILS

Mark	Symbol & Description		Part No.
	L1	Axial inductor	LAU330J
	L2	Axial inductor	LAU430J
	L3	Axial inductor	LAU270J

CAPACITORS

Mark	Symbol & Description	Part No.
	C1	CCPUCH150J50
	C2	CCPUCH2R2K50
	C3	CCDCH560J50
	C4	CCPUCH1R5M50
	C5	CCDCH510J50
	C6	CCDCH220J50
	C7	CCPUCH180J50

VSOP Assembly (VWS1025)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC7	CXD1095Q
★★	IC1	HD6303YP (HD63A03YP)
★★	IC4	M74LS00P
★★	IC6	M74LS27P
★★	IC8	PD6063
★★	IC5	M74LS30P
★★	IC3	M74LS74AP
★★	IC403	NJM2903S
★★	IC103, IC105, IC106	NJM4558D
★★	IC104, IC107	NJM4558S
★★	IC406	PA0017
★★	IC301	PA0026
★★	IC102	PA5009
★★	IC401	PA5010
★★	IC2	PD0024
★★	IC101	PD9001
★★	IC404	PM0001
★★	IC407	TA7347P
★★	IC405	TL8707P
★★	Q107, Q115, Q120, Q121, Q125, Q301	UN4112
★★	Q101, Q106, Q108, Q113, Q122, Q124, Q302, Q601	UN4212
★★	Q430	2SA1015
★★	Q117, Q109, Q403, Q404, Q406, Q602	2SA933S
★★	Q112	2SC1583
★★	Q405	2SC1627
★★	Q2, Q110, Q114, Q118, Q123, Q126, Q303–Q306, Q407–Q417, Q421–Q426, Q428, Q431	2SC1740S
★★	Q119	2SK184
★	D105	HZS3B2
★	D120	HZS5C2
★	D407	HZS6C2
★	D121, D122, D410	HZS7B2
★	D503	HZS9A3
★	D505	HZ4ALL
★	D411	HZ5B2
★	D119	SLV31VC3
★	D3, D4, D106–D109, D113–D118, D123–D126, D301–D303, D401, D402, D405, D406, D409, D412, D504	1SS254
★	D502	SM-IXN02

COILS AND FILTERS

Mark	Symbol & Description	Part No.
	L101, L401–L404, L412 Axial inductor	LAU120J
	L409 Axial inductor	LAU121J
	L410, L426 Axial inductor	LAU220J
	L1 Axial inductor	LAU221J
	L102 Axial inductor	LAU270J
	L405, L413, L425 Axial inductor	LAU330J
	L427 Axial inductor	LAU560J
	L411 Axial inductor	LAU680J
	L406 Coil	LRA271K
	L301 Coil	LRA390K
	L415 Coil	LRA391K
	L414 Coil	LRA561K
	L420 Coil (3.9MHz)	VTL-170
	F301 B.P.F. (2.3MHz)	VTF1002 (VTF1026)
	F302 B.P.F (2.8 MHz)	VTF1003 (VTF1027)
	F505 L.P.F (1.75MHz)	VTF1021 (VTF1024)
	F506 Audio B.P.F	VTF1022 (VTF1025)
	F1, F2, F101, F501–F503 3 terminal filter	VTH1001

CAPACITORS

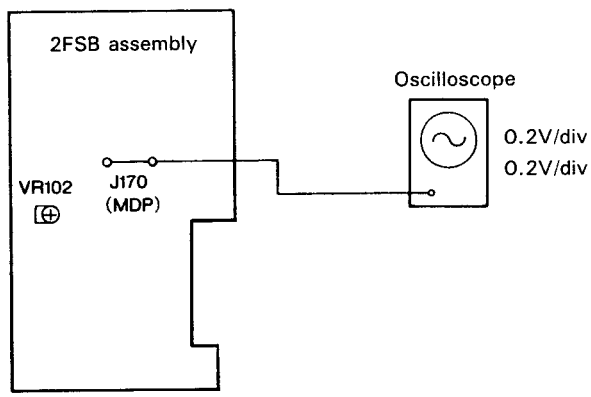
Mark	Symbol & Description	Part No.
	C125, C126, C128, C150, C445, C624	CCCCH101J50
	C448, C482	CCCCH121J50
	C124, C465, C467	CCCCH151J50
	C451, C523, C659	CCCCH300J50
	C312, C429, C483	CCCCH330J50
	C311, C453, C662	CCCCH390J50
	C417, C470	CCCCH430J50
	C457, C666	CCCCH470J50
	C31, C411	CCCCH510J50
	C328, C330, C473	CCCCH560J50
	C106, C129	CCCCH680J50
	C454	CCCCH750J50
	C432, C433	CCCCH820J50
	C317, C450, C25	CCCSL181J50
	C316, C335, C336	CCCSL221J50
	C458	CCCSL241J50
	C434	CCCSL271J50
	C444	CCCSL301J50
	C1, C2, C9	CCCSL330J50
	C435	CCCSL391J50
	C447	CCDCH220J50
	C668	CCDCH620J50
	C474	CCDCH910J50
	C29	CCDSL391J50
	C15, C428, C430, C452	CCPUCH100J50
	C455	CCPUCH120J50
	C407, C408, C623, C658	CCPUCH150J50
	C13, C406, C620	CCPUCH180J50
	C10	CCPUSL220J50
	C14, C16	CCPUSL470J50
	C475	CEALNP220M16
	C343	CEANLR47K50
	C345	CEANL220K16
	C145	CEANP010M50
	C143	CEANP101M6R3
	C140	CEANP2R2M50
	C166, C142, C146, C318, C319	CEANP220M10
	C403, C503, C508	CEASR47M50
	C114, C413, C515, C518	CEAS010M50
	C3, C22, C334, C337, C338, C349, C354–C356, C469, C481, C663	CEAS100M50
	C4, C7, C314, C315, C353, C493, C494, C522, C525, C622,	CEAS101M10
	C11, C151, C357, C358, C443, C501, C505, C507, C511, C513, C516, C655, C656	CEAS220M50
	C309, C310, C360	CEAS221M10
	C480, C613	CEAS3R3M50
	C149, C313, C514, C519, C520	CEAS4R7M50
	C119, C133, C135, C154, C157, C158, C161,C163, C168, C171, C177, C179, C180, C350, C402, C405, C421, C427, C437, C440, C446, C488, C490, C610, C612, C651	CEAS470M25
	C301, C302, C346, C621	CEAS471M10
	C456	CEJANP470M10
	C486	CEJA100M16
	C471	CEJA330M10
	C463, C476	CEJA470M16

3. VCXO OFFSET ADJUSTMENT

- Purpose: Minimize the VCXO PLL phase error offset voltage
- Symptoms indicating need for adjustment: Intermittent output of digital sound during LDD playback (output of synchronous noise)

• Measuring instruments and jigs:	• Oscilloscope
• Measuring position	• 2FSB assembly J170 (MDP)
• Test disc and player mode	• LDD disc — play any frame
• Adjustment position	• 2FSB assembly VR102

Connection diagrams



Adjustment procedure

1. Play any frame of the LDD disc.
2. Connect the oscilloscope to jumper lead J170 (MDP) on the 2FSB assembly and observe the VCXO PLL phase error output signal.
3. Adjust VR102 on the 2FSB assembly to minimize the pulse width on the positive or negative side and obtain a continuous waveform. (Center waveform in Photo 23.)

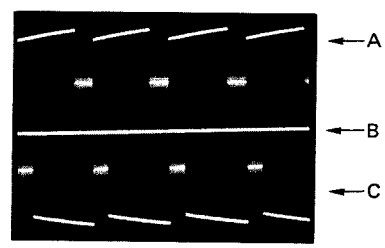


Photo 23

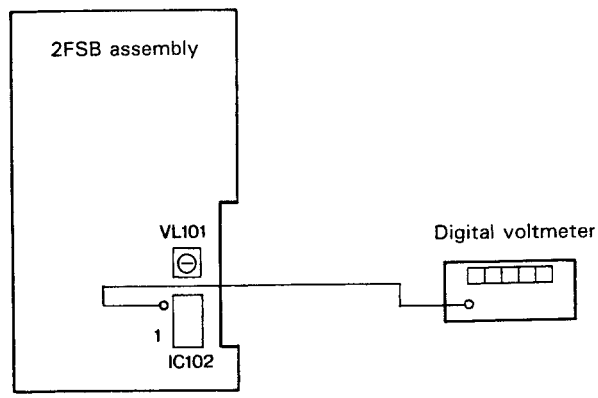
A Waveform obtained when VR102 is turned clockwise from the position of optimum adjustment.
B Optimum adjustment
C Waveform obtained when VR102 is turned counter clockwise from the position of optimum adjustment.

2. PLL FREE-RUN FREQUENCY ADJUSTMENT

- Purpose: Adjustment of the free-run frequency of the PLL VCO used in the EFM decoder to the optimum value
- Symptoms indicating need for adjustment: No digital sound, or intermittent digital sound

• Measuring instruments and jigs:	• Digital voltmeter
• Measuring position	• 2FSB assembly IC102 (NJM082D) pin 1
• Test disc and player mode	• LaserVision disc with digital sound (LDD) disc hereafter — play any frame
• Adjustment position	• 2FSB assembly VL101

Connection diagrams



Adjustment procedure

1. Play any frame of the LDD disc.
2. Connect the digital voltmeter to pin 1 of IC102 on the 2FSB assembly and measure the DC voltage of the VCO control signal.
3. Set the DC voltage of the VCO controller signal to 150mV ± 100mV by adjusting VL101 on the 2FSB assembly.

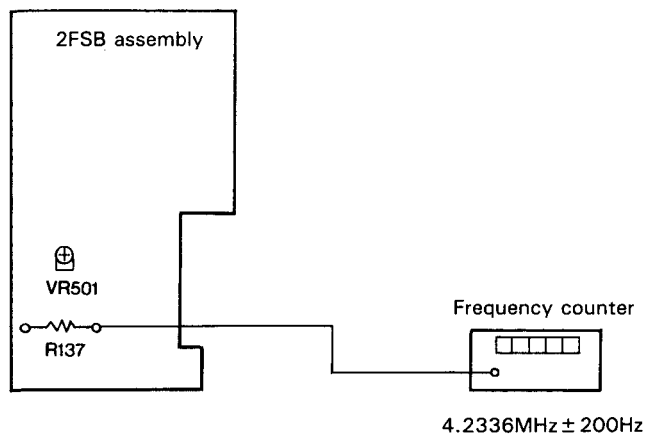
8.6 2FSB ASSEMBLY ADJUSTMENTS

1. VCXO FREE-RUN FREQUENCY ADJUSTMENT

- Purpose: Adjustment of the frequency of the crystal generator used in the EFM decoder to the optimum value

• Measuring instruments and jigs:	• Frequency counter
• Measuring position	• 2FSB assembly R137 lead wire
• Test disc and player mode	• CD test disc — play any track
• Adjustment position	• 2FSB assembly VR501

Connection diagrams



Adjustment procedure

1. Play any track of the CD test disc.
2. Connect the frequency counter to the lead wire of R137 on the 2FSB assembly and observe the VCXO free-run frequency.
3. Set the frequency to 4.2336MHz ±200Hz by adjusting VR501 on the 2FSB assembly.

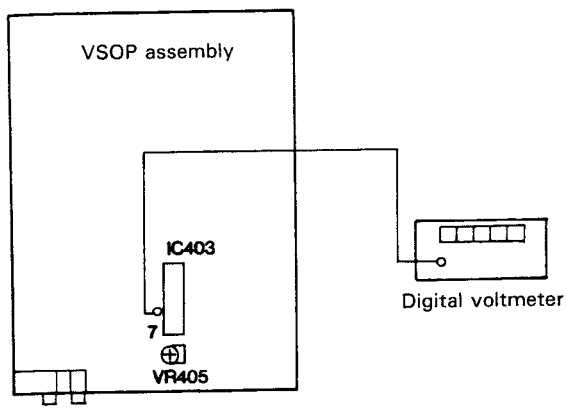
9. DETECTOR LEVEL ADJUSTMENT

8.5 VSOP (VDEM, ADEM) Assembly Adjustments

- Purpose: Optimization of the input voltage applied to the spindle motor speed detector comparator.
- Symptoms indicating need for adjustment: Spindle servo lock failure. Picture aberration.

• Measuring instruments and jigs	• Digital voltmeter
• Measuring position	• VSOP assembly IC403 (NJM2903S) pins 6 and 7
• Test disc and player mode	• Test disc #4,801 (#5,401)
• Adjustment position	• VSOP assembly (VDEM, ADEM) VR405

Connection diagrams



Adjustment Procedure

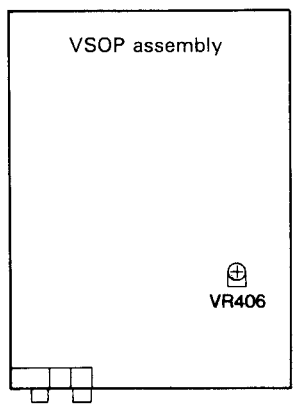
1. Play an LD test disc and search to frame #4,801 (#5,401).
2. Connect the digital voltmeter to pin 7 of IC403 (NJM2903S) on the VSOP assembly. Measure and record the reference voltage of the spindle motor speed detector comparator.
3. Also connect the digital voltmeter to pin 6 of the same IC and measure the speed detector output voltage. Adjust VR405 on the VSOP assembly to obtain a voltage +330mV higher at pin 6 than at pin 7.

8.COLOR PHASE ERROR SIGNAL LEVEL ADJUSTMENT 8.5 VSOP (VDEM, ADEM) Assembly Adjustments

- Purpose: Optimization of the amount of color phase error signal to be applied to the color phase compensation stage.
- Symptoms indicating need for adjustment: Conspicuous color irregularities

• Measuring instruments and jigs	• TV monitor
• Measuring position	• Adjust while watching the monitor screen.
• Test disc and player mode	• LD test disc #7,201 (#26,101)
• Adjustment position	• VSOP assembly VR406

Connection diagrams



Adjustment Procedure

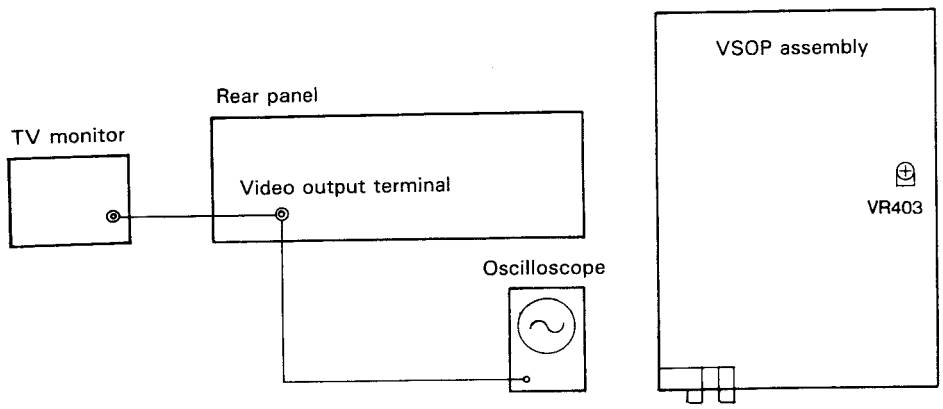
1. Play an LD test disc and search to frame #7,201 (#26,101)
2. Adjust VR402 on the VSOP assembly to minimize magenta screen color irregularities.

7. OUTPUT VIDEO LEVEL ADJUSTMENT

- Purpose: Adjustment of the amplitude of the output video signal (pedestal ↔ 100% white) to 0.71Vp-p.
- Symptoms indicating need for adjustment: Replay started from intermediate position due to misreading data. Screen too bright or too dark.

• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• Video output terminals
• Test disc and player mode	• LD test disc #19,801 (#19,801)
• Adjustment position	• VSOP assembly VR403

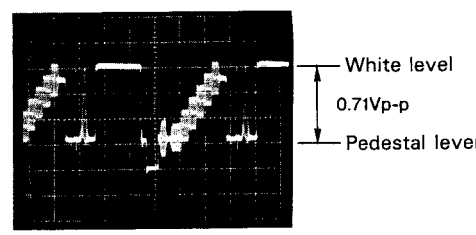
Connection diagrams



Adjustment Procedure

Note: Connect the player video output terminal to a video monitor, and terminate the monitor internally with 75 ohms. If using a TV set with no video input terminal, terminate the player video output terminal with 75 ohms.

1. Play an LD test disc and search to frame #19,801 (#19,801)
2. Connect the oscilloscope to the player video output terminal, and observe the playback video signal waveform.
3. Adjust VR403 on the VSOP assembly until the amplitude from the pedestal level to the white level of the playback video signal waveform reaches 0.71V ±5%. (Photo 20.)

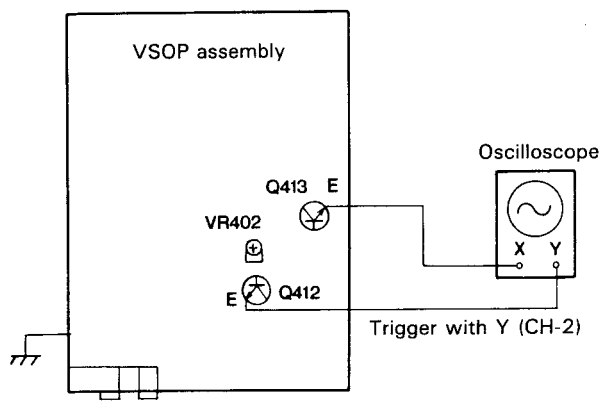


6. VCO CENTER FREQUENCY ADJUSTMENT

- Purpose: Optimization of the CCD delay time for time base error compensation purposes.
- Symptoms indicating need for adjustment: Color lock failure. Slow color lock after a search.

• Measuring instruments and jigs	• Dual-trace oscilloscope
• Measuring position	• VSOP assembly Q412 emitter and Q413 emitter
• Test disc and player mode	• LD test disc #19,801 (#19,801)
• Adjustment position	• VSOP assembly VR402

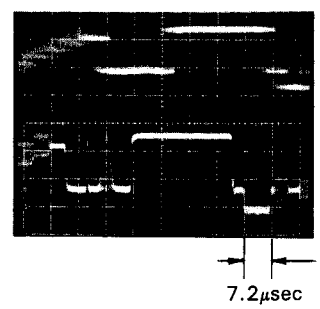
Connection diagrams



X: 20mV/div, AC input,
Y: 20mV/div, AC input,
5 μsec/div

Adjustment Procedure

1. Play an LD test disc, and search to frame #19,801 (#19,801).
2. Connect the oscilloscope X input (CH-1) to the emitter of Q413 on the VSOP assembly, and the Y input (CH-2) to the emitter of Q412. Trigger with CH-2, and observe the video signal waveforms before and after time base error compensation simultaneously.
3. The video signal of following time base error compensation in CH-1 contains jitter. Adjust VR402 on the VSOP assembly to delay the center of that jitter by 70.7 μsec (1H + 7.2 μsec) from the trailing edge of the horizontal synchronizing signal (H-sync) in the video signal prior to time base error compensation at CH-2. (Photo 19.)



CH-1
Video signal after compensation

CH-2
Video signal before compensation

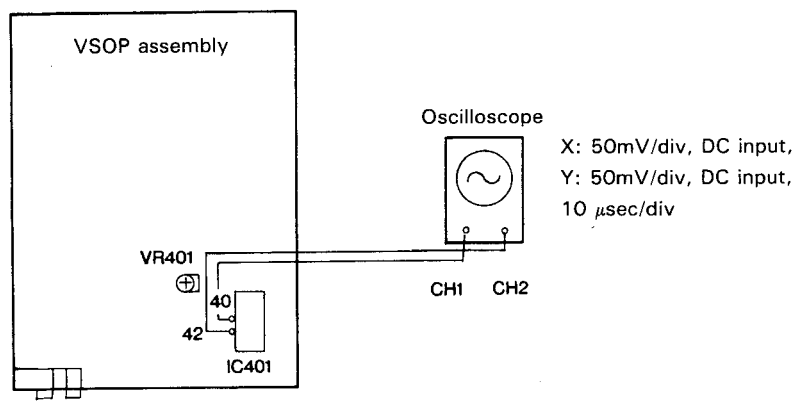
Photo 19

5. 1H DELAYED VIDEO LEVEL ADJUSTMENT

- Purpose: Adjustment of the amplitude of the 1H delayed video signal to the same amplitude as the main video signal.
- Symptoms indicating need for adjustment: Considerable white drop-out and H displacement (horizontal lines on the screen) when 1H level is large, and considerable black drop-out when 1H level is small.

• Measuring instruments and jigs	• Dual-trace oscilloscope
• Measuring position	• VSOP assembly • IC401 (PA5010) pin 42 and pin 40
• Test disc and player mode	• LD test disc #19,801 (#19,801)
• Adjustment position	• VSOP assembly VR401

Connection diagrams



Adjustment Procedure

1. Play an LD test disc, and search to frame #19,801 (#19,801).
2. Connect the oscilloscope X input (CH-1) to pin 40 of IC401 (PA5010) on the VSOP assembly, and the Y input (CH-2) to pin 42. Observe the main video signal and the 1H delayed video signal waveforms simultaneously.
3. Adjust VR401 on the VSOP assembly until the amplitude from the synk tip to the white level in the 1H delayed video signal (CH-2) is the same as the amplitude of the main video signal (CH-1). (Photo 18.)

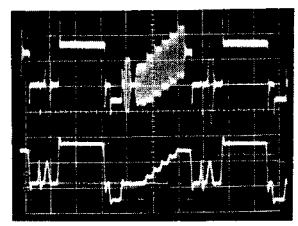


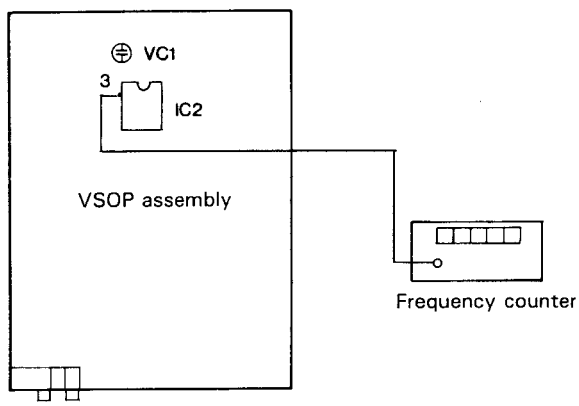
Photo 18

4. 14.31818MHz ADJUSTMENT

- Purpose: Reference clock frequency adjustment
- Symptoms indicating need for adjustment: Color aberration, spindle servo lock failure

• Measuring instruments and jigs	• Frequency counter
• Measuring position	• VSOP assembly IC2 (PD0024) pin 3
• Test disc and player mode	• Switch power on without playing disc.
• Adjustment position	• VSOP assembly VC1

Connection diagrams



Adjustment Procedure

1. Switch the power on, and connect the frequency counter to pin 3 of IC2 (PD0024) on the VSOP assembly.
2. Adjust VC1 on the VSOP assembly until the reference clock frequency reads 14.31818MHz.

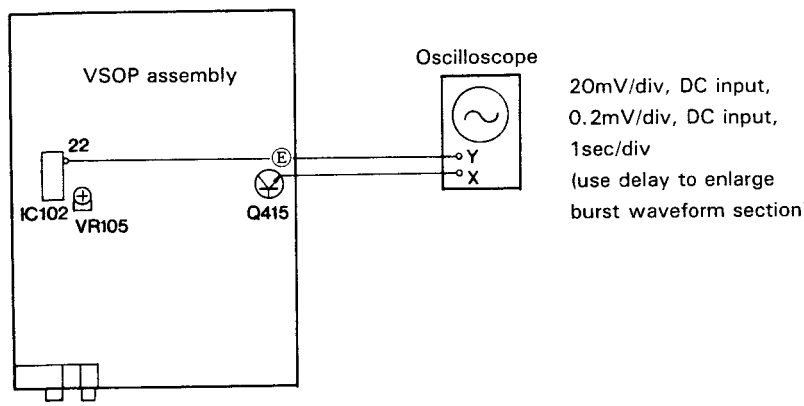
Note: If this frequency is difficult to adjust, play an LD test disc, and adjust the VSOP assembly VC1 to obtain a frequency of 15.734265MHz at pin 25 of IC101 (PD9001) during playback.

3. BURST GATE POSITION ADJUSTMENT

- Purpose: Adjustment of the burst gate position.
- Symptoms indicating need for adjustment: Playback commenced from intermediate position (not from start of disc), missing or irregular color, fine stripes

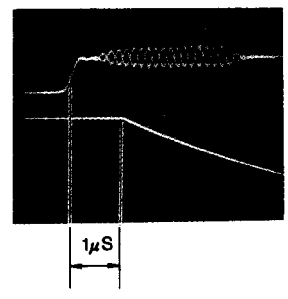
• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• VSOP assembly Q415 (emitter), IC102 (PA5009) pin 22
• Test disc and player mode	• LD test disc
• Adjustment position	• VSOP assembly VR105

Connection diagrams



Adjustment Procedure

1. Play an LD test disc.
2. Connect the oscilloscope X input (CH-1) to the emitter of Q415 on the VSOP assembly, and the Y input (CH-2) to pin 22 of IC102 (PA5009).
3. Adjust VR105 on the VSOP assembly until the trailing edge of the MMV output is delayed by about 1μsec in respect to the leading edge of the video signal. (Photo 17.)
   MMV: Monostable Multi-Vibrator



Top: Q415 emitter
(TBC VIDEO)
Bottom: IC102 pin 22

Photo 17

2. HALF H REJECTION

- Purpose: Adjustment of MMV (Monostable Multi-Vibrator) pulse width for half H rejection.
- Symptoms indicating need for adjustment: Picture aberration (spindle lock failure)

• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• VSOP assembly IC101 (PD9001) pin 17
• Test disc and player mode	• LD test disc
• Adjustment position	• VSOP assembly VR103

Connection diagrams

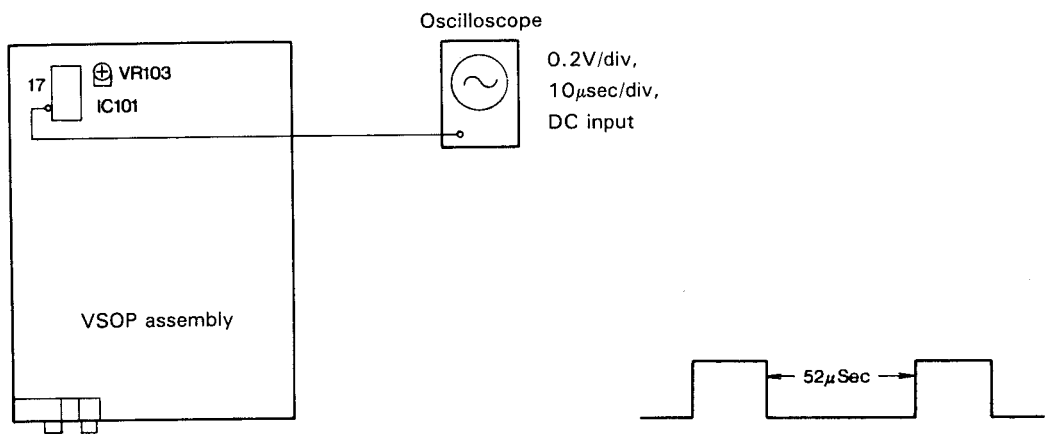


Fig. 1

Adjustment Procedure

1. Play an LD test disc.
2. Connect the oscilloscope to pin 17 of IC101 (PD9001) on the VSOP assembly.
3. Adjust VR103 on the VSOP assembly until the width of the LOW interval of the pulse waveform is 52 μsec.

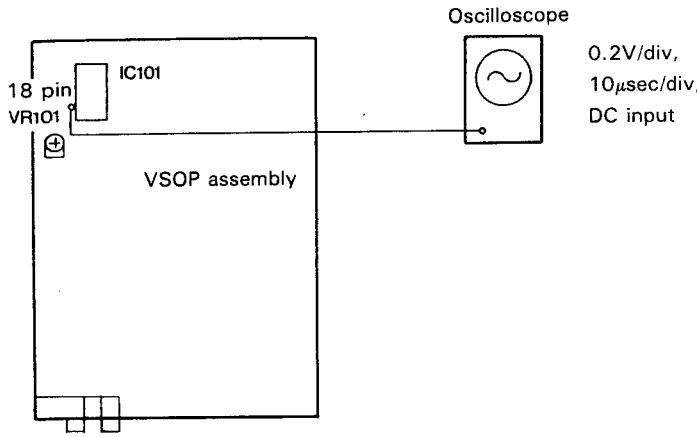
8.5 VSOP ASSEMBLY ADJUSTMENTS

1. REFERENCE SHIFT ADJUSTMENT

- Purpose: Adjustment of the amount of REFERENCE shift required for detecting spindle servo frequency error.
- Symptoms indicating need for adjustment: Spindle servo locking failure

• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• VSOP (TBC, CONT) assembly IC101 (PD9001) pin 18
• Test disc and player mode	• Power switch on
• Adjustment position	• VSOP assembly VR101

Connection diagrams



Adjustment Procedure

1. As simply switch the player power on, connect the oscilloscope to pin 18 of IC101 (PD9001) on the VSOP assembly.
2. Adjust the oscilloscope trigger knob to stabilize the pulse waveform as shown in Photo 15.
3. Adjust VR101 on the VSOP assembly until the width of the HIGH interval up to the start of the LOW interval in the pulse waveform is 28 μsec.

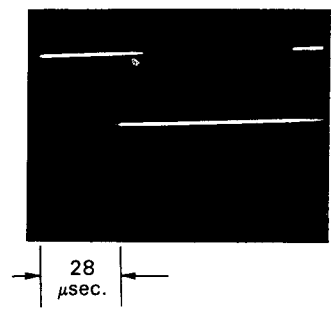


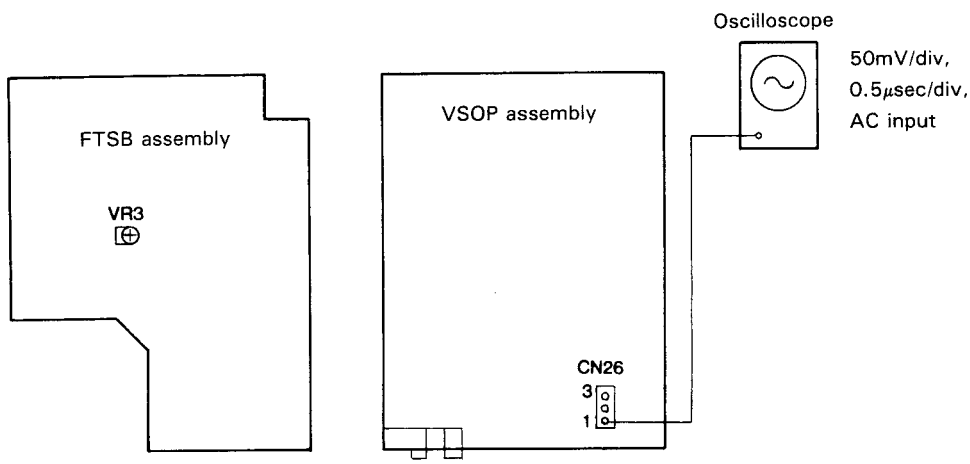
Photo 15.

4. CD FOCS ERROR BALANCE ADJUSTMENT

- Purpose: To ensure that the FOCS maintains the objective lens at the optimum distance from the disc during CD playback.
- Symptoms indicating need for adjustment: Noise in CD playback sound

• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• VSOP assembly CN26-1 (EFM OUT)
• Test disc and player mode	• CD test disc (YEDS-7)
• Adjustment position	• FTSB assembly VR3

Connection diagrams



Adjustment Procedure

1. Play a CD test disc.
2. Connect the oscilloscope to CN26-1 (EFM OUT) on the VSOP assembly, and observe the EFM signal (eye pattern).
3. Adjust VR3 on the FTSB assembly until the EFM signal reaches maximum amplitude. (Photo 14.)

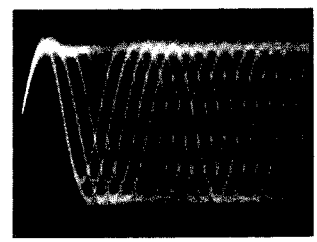


Photo 14. EFM signal

3. FOCS SERVO LOOP GAIN ADJUSTMENT

- Purpose: Adjustment of FOCS servo loop gain to the optimum value.
- Symptoms indicating need for adjustment: Poor blayback performance
  Improper focusing. (No initial focusing, intermittent play etc)

• Measuring instruments and jigs	• Oscilloscope • Resistor (100kΩ) • AF generator
• Measuring position	• FTSB assembly CN102-5 (FOCS error), CN102-4 (FOCS gain)
• Test disc and player mode	• Suspend FOCS motor protector circuit function. • LD test disc #16,000 (#15,000)
• Adjustment position	• FTSB assembly VR1

Connection diagrams

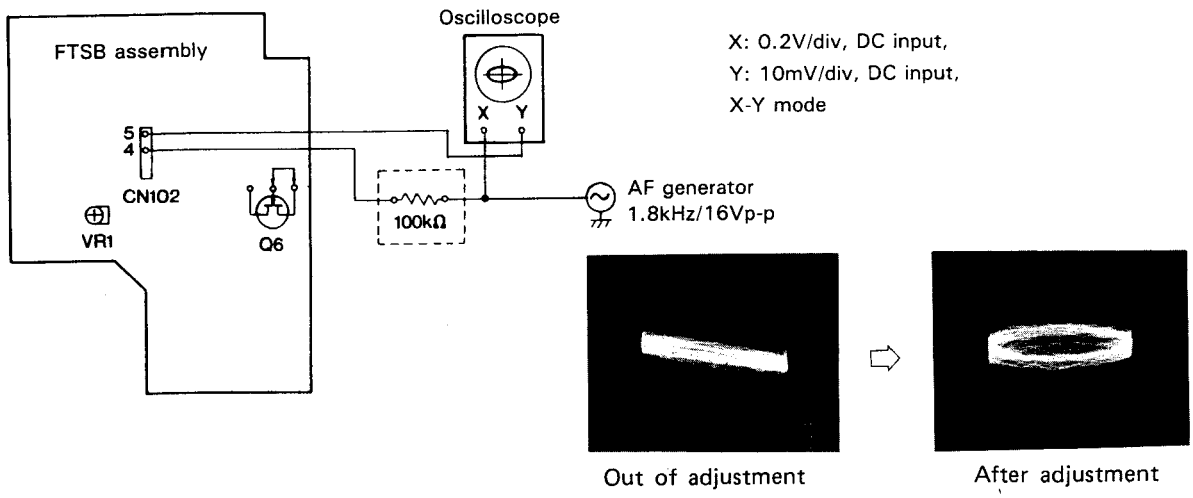


Photo 13

Adjustment procedure

1. Connect the gate of FTSB assembly Q6 (2SK184) to ground to suspend the focus motor protector circuit function.
2. Connect the resistor, AF generator, and oscilloscope to CN102 on the FTSB assembly as shown in the diagram.
3. Set the AF generator output to 1.8kHz/16Vp-p.
4. Put the oscilloscope into X-Y mode, and observe the Lissajous figures.
5. Adjust VR1 on the FTSB assembly until the Lissajous figures become symmetrical along the respective X and Y axes of the oscilloscope. (Photo 13.)
6. Disconnect the gate of FTSB assembly Q6 from ground.

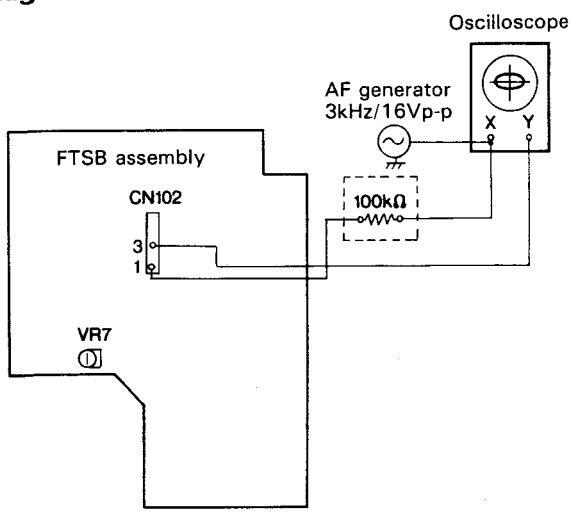
   Note: If the AF generator output does not exceed 16Vp-p, decrease the value of the above resistor (100kΩ) until the Lissajous figures become easy to observe. (33kΩ limit.)

2. TRKG SERVO LOOP GAIN ADJUSTMENT

- Purpose: Adjustment of TRKG servo loop gain to the optimum value.
- Symptoms indicating need for adjustment: Improper tracking (Skip, Jump, etc)

• Measuring instruments and jigs	• Oscilloscope • Resistor (100kΩ) • AF generator
• Measuring position	• FTSB assembly CN102-1 (TRKG error), CN102-3 (TRKG gain)
• Test disc and player mode	• LD test disc #16,000 (#15,000) (TRKG servo: close)
• Adjustment position	• FTSB assembly VR7

Connection diagrams

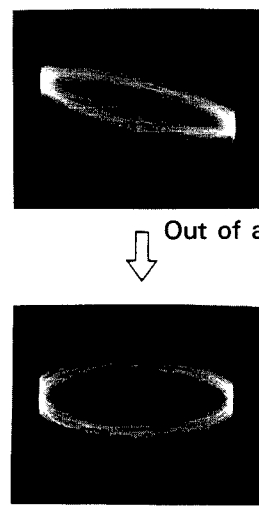


X: 0.2V/div, DC input,
Y: 10mV/div, DC input,
X-Y mode

Adjustment procedure

1. Play an LD test disc and search to frame #16,000 (#15,000).
2. Connect the resistor, AF generator, and oscilloscope to CN102 on the FTSB assembly as shown in the diagram.
3. Set the AF generator output to 3kHz/16Vp-p.
4. Put the oscilloscope into X-Y mode, and observe the Lissajous figures.
5. Adjust VR7 on the FTSB assembly until the Lissajous figures become symmetrical along the respective X and Y axes of the oscilloscope. (Photo 12.)

Note: If the AF generator output does not exceed 16Vp-p, decrease the value of the above resistor (100kΩ) until the Lissajous figures become easy to observe. (33kΩ limit.)



Out of adjustment

After adjustment Photo 12

Photo 12

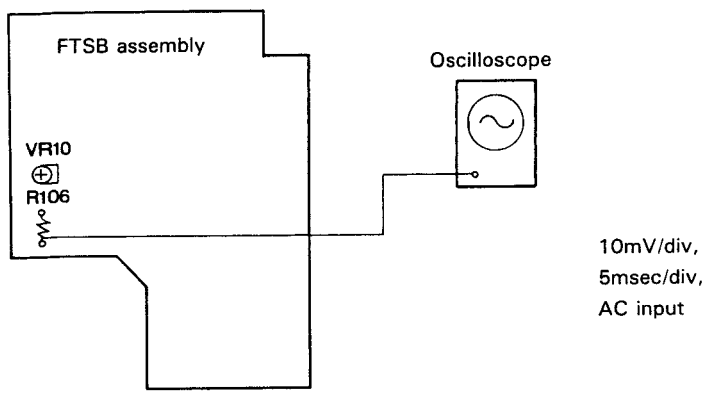
8.4 FTSB ASSEMBLY ADJUSTMENTS

1. RF GAIN ADJUSTMENT

- Purpose: Adjustment of RF signal amplitude to the optimum value.
- Symptoms indicating need for adjustment: Frequent drop-out

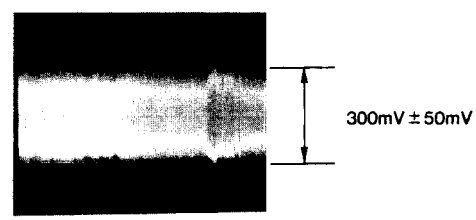
• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• Lead of R106 on FTSB assembly (RF signal)
• Test disc and player mode	• LD test disc #16,000 (#15,000) (TRKG servo: closed)
• Adjustment position	• FTSB assembly VR10 (RF gain)

Connection diagrams



Adjustment procedure

1. Play an LD test disc and search to frame #16,000 (#15,000).
2. Connect the oscilloscope to the lead of R106 on the FTSB assembly and observe the RF signal.
3. Adjust VR10 on the FTSB assembly to obtain an RF signal amplitude of 300mV ±50mV. (Photo 11.)



RF signal

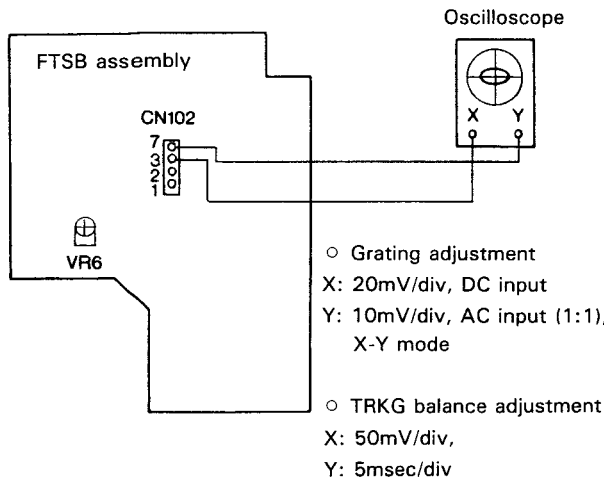
Photo 11

8. FINE GRATING ADJUSTMENT AND TRKG BALANCE ADJUSTMENT CHECK

- Purpose: • Fine adjustment of the grating to ensure that the two beams for TRKG servo are directed to the optimum positions in the disc track.
  • Adjustment of TRKG servo loop offset voltage to 0V.
- Symptoms indicating need for adjustment: Improper Tracking (Skip. Jump etc)

• Measuring instruments and jigs	• Oscilloscope • Screwdriver
• Measuring position	• FTSB assembly CN102-3 (TRKG error), CN102-7 (TRKG sum)
• Test disc and player mode	• LD test disc #16,000 (#15,000) • Test mode (TRKG servo: open)
• Adjustment position	• Grating • FTSB assembly VR6

Connection diagrams



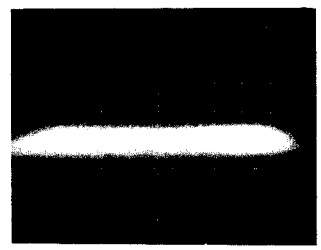


Photo 9.
Fine grating adjustment

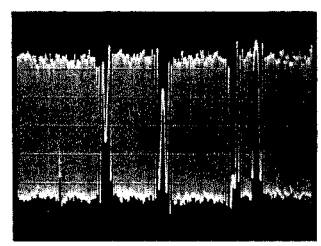


Photo 10.
TRKG balance adjustment

Adjustment procedure

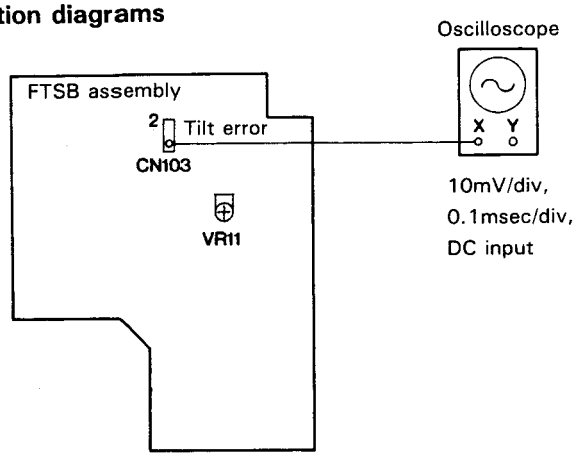
1. Play an LD test disc, search to frame #16,000 (#15,000), and open the TRKG servo.
2. Connect the oscilloscope X input (CH-1) to CN102-3 of the FTSB assembly, and the Y input (CH-2) to CN102-7.
   Switch the oscilloscope to X-Y mode, and observe the Lissajous figures for the TRKG error and TRKG sum signals.
3. Insert a small screwdriver into the grating adjustment hole (see p.51), and fine adjust the grating until the amplitude of the Lissajous figures along the Y axis reaches a minimum. (Photo 9.)
   If the grating is turned too far and the optimum position can no longer be found, repeat the "Rough Grating Adjustment".
4. Using the X input (CH-1) of the oscilloscope, check that the positive and negative amplitudes of the TRKG error signal are equal. (Photo 10.) If they are not equal, repeat the "Tracking Balance Adjustment".
5. Close the TRKG servo, and check that a normal picture is shown on the TV screen.

7. TILT SENSOR INCLINATION ADJUSTMENT

- Purpose: Adjustment of the tilt servo offset voltage to 0V by adjustment of tilt sensorinclination.
- Symptoms indicating need for adjustment: Crosstalk

• Measuring instruments and jigs	• Oscilloscope • Philips head screwdriver
• Measuring position	• FTSB assembly CN103-2 (tilt error)
• Test disc and player mode	• LD test disc #4,760 (#4,760) (TRKG servo: closed)
• Adjustment position	• Tilt sensor inclination adjustment screw • FTSB assembly VR11 (tilt gain)

Connection diagrams



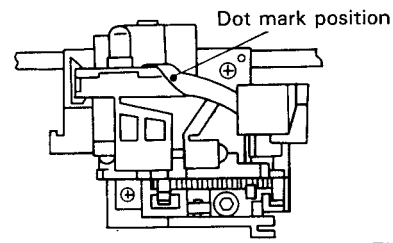
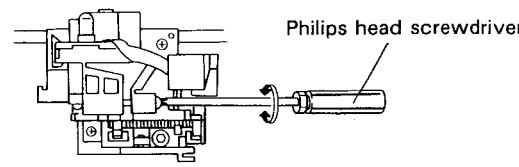


Fig.1



Tilt sensor inclination adjustment

Fig.2

Adjustment Procedure

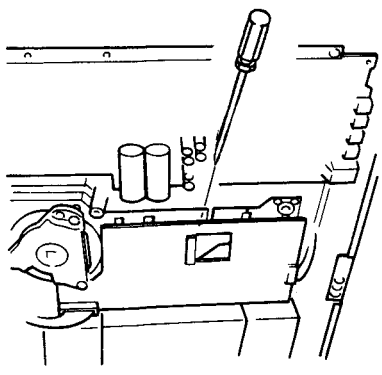
1. Check the color of the dot marked on the flexible cable next to the tilt sensor. (Fig.1)
   There are three types of dots. Adjust VR11 on the FTSB assembly accordingly.
   Red dot ... Turn VR11 fully clockwise.
   Blue dot ... Turn VR11 fully counter clockwise.
   No dot (no mark) ... Adjust VR11 to center position.
2. Play an LD test disc, and search to frame #4,760.
3. Connect the oscilloscope to CN103-2 of the FTSB assembly, and observe the tilt error DC voltage.
4. Insert a Philips head screwdriver with a long shaft through the rear panel and adjust the tilt sensor inclination adjustment screw until the tilt error DC voltage reads 0V. (See Fig.2.)
   During this step, it does not matter if the pick-up is displaced a little from the designated frame by the screwdriver.
5. Connect the tilt motor connector CN65 disconnected during the "Pick-up Tracking Direction Inclination Adjustment".
6. Search to frame #115 (#104) and check that crosstalk on the left and right hand sides of the TV screen has been minimized, and that it is about equal on both sides.

6. PICK-UP TANGENTIAL DIRECTION ANGLE ADJUSTMENT

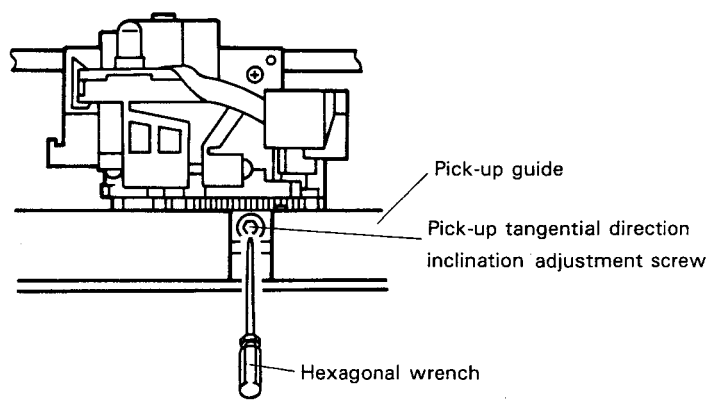
- Purpose: Adjustment of pick-up tangential direction inclination to minimize crosstalk.
- Symptoms indicating need for adjustment: Conspicuous crosstalk

• Measuring instruments and jigs	• TV monitor
• Measuring position	• Crosstalk on the screen • FTSB assembly CN102-3 (TRKG error)
• Test disc and player mode	• LD test disc #28,600 (#27,000), #115 (#104) • Test mode (TRKG servo: open/close)
• Adjustment position	• Pick-up tangential direction inclination adjustment screw

Connection diagrams (For the connection diagrams, refer to page 52.)



Pick-up tangential direction inclination adjustment



Adjustment Procedure

Note: This adjustment is necessary only if crosstalk remains conspicuous after completing the "Pick-up Tracking Direction Inclination Adjustment" and "LD FOCS Error Balance Adjustment" procedures.

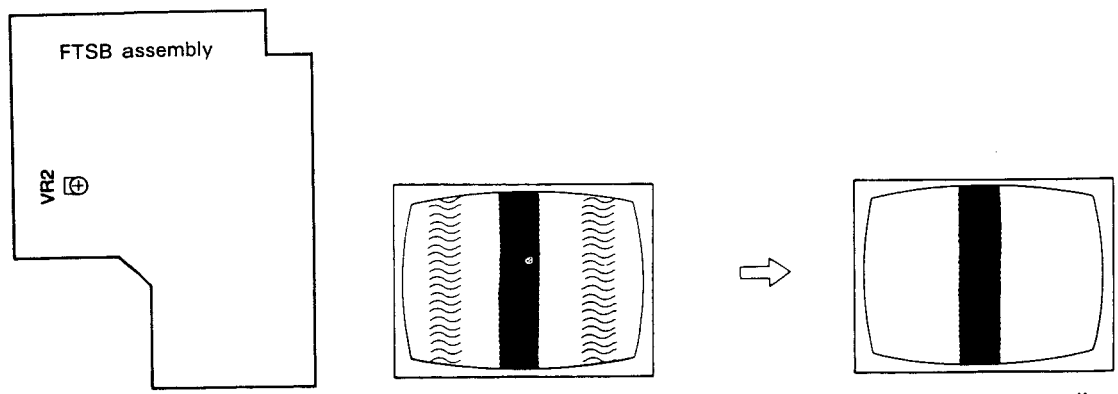
1. Play an LD test disc, search to frame #28,600 (#27,000), and open the TRKG servo.
2. Connect the oscilloscope to CN102-3 of the FTSB assembly and observe the TRKG error waveform.
3. Insert the hexagonal wrench through the gap between the 2FSB assembly and mechanical assembly to the pick-up tangential direction inclination adjustment screw.
4. Adjust this screw until the TRKG error waveform reaches maximum amplitude.
5. Remove the hexagonal wrench, then search to frame #115 (#104) and check that crosstalk on the left and right hand sides of the TV screen has been minimized, and that it is about equal on both sides. Repeat steps 4 and 5 if considered necessary.

5. LD FOCS ERROR BALANCE ADJUSTMENT

- Purpose: To ensure that the FOCS servo maintains the objective lens at the optimum distance from disc during LD playback.
- Symptoms indicating need for adjustment: Crosstalk

• Measuring instruments and jigs	• TV monitor
• Measuring position	• Player video output terminals
• Test disc and player mode	• LD test disc #115 (#104)
• Adjustment position	• FTSB assembly VR2

Connection diagrams



Screen showing generation of crosstalk

Minimum crosstalk

Adjustment Procedure

1. Play an LD test disc, and search to frame #115 (#104).
2. Adjust VR2 on the FTSB assembly to minimize crosstalk in the left and right hand sides of the TV screen. If this adjustment fails to reduce crosstalk down to the allowable level, go to the "Pick-up Tangential Direction Angle Adjustment" procedure.

4. PICK-UP TRACKING DIRECTION INCLINATION ADJUSTMENT

- Purpose: Adjustment of slider shaft inclination to ensure that the pick-up assembly moves parallel to the disc surface, and adjustment of the pick-up assembly tracking direction angle to ensure that the laser beam is beamed perpendicularly at the disc.
- Symptoms indicating need for adjustment: Crosstalk

• Measuring instruments and jigs	• Oscilloscope • Battery with lead wires • Low-pass filter • 2.5mm hexagonal wrench
• Measuring position	• FTSB assembly CN103-5 (FOCS drive)
• Test disc and player mode	• LD test disc #4760 (#4760), #46,135 (#42,314), #115 (#104)
• Adjustment position	• Pick-up tracking direction angle adjustment screw • Adjust slider shaft angle with tilt motor

Connection diagrams

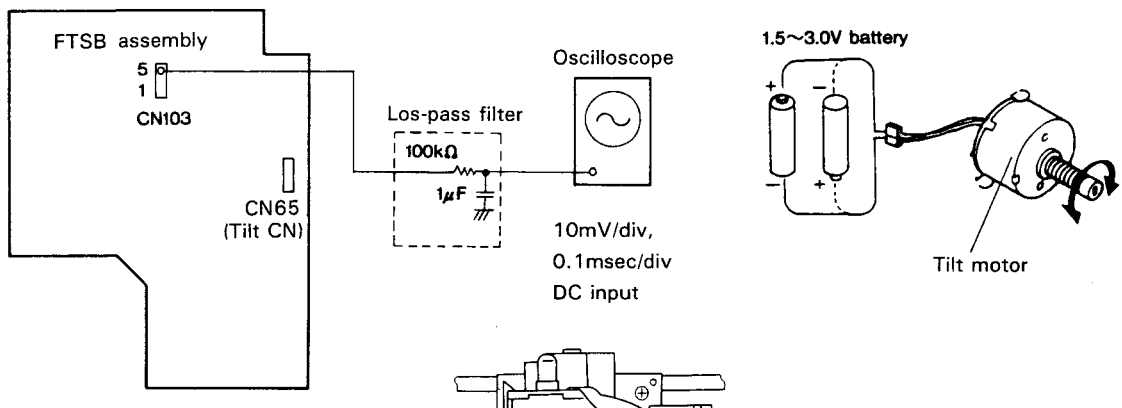


Fig.1

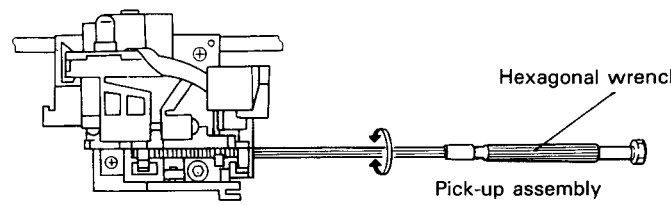


Fig.2

Adjustment Procedure

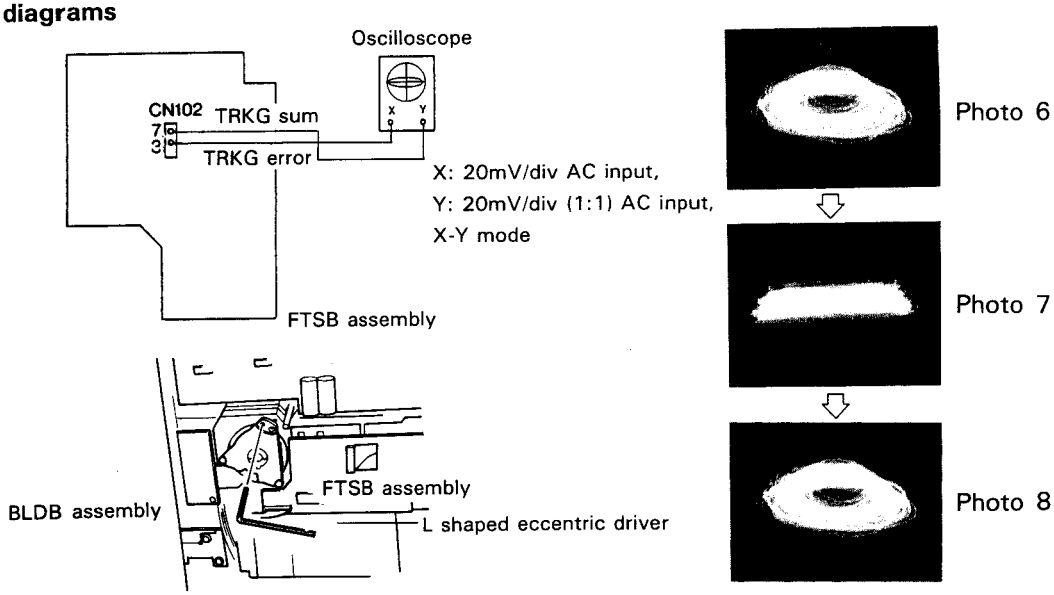
1. Disconnect the FTSB assembly CN65 (tilt motor) connector, and do not connect it again until the "Tilt Sensor Angle Adjustment" has been completed.
2. Play an LD test disc, and search to frame #4,760 (#4,760) where the tilt fulcrum is located.
3. Connect the oscilloscope to CN103-5 of the FTSB assembly via a low-pass filter, and observe the focus drive voltage. The oscilloscope GND level does not have to be aligned in the center of the screen at this stage.
4. Adjust the Y axis position adjustment knob on the oscilloscope to position the focus drive voltage waveform in the center of the oscilloscope screen.
5. If the focus drive voltage measured when searching for frame #46,135 (#42,314) differs from that obtained in step 4 above, connect a battery (1.5 to 3V) to the tilt motor connector, and turn the motor until the focus drive voltage is within ±50mV of the step 4 voltage.
6. Insert the hexagonal wrench into the adjustment hole in the rear panel, and adjust the pick-up tracking direction inclination adjustment screw to minimize the crosstalk on the left and right hand sides of the TV screen.
7. Search to frame #115 (#104) and check that crosstalk on the left and right hand sides of the TV screen has been minimized, and that it is about equal on both sides. If the level of crosstalk on the TV screen is still too high, repeat steps 6 and 7.

3. SPINDLE MOTOR CENTERING ADJUSTMENT

- Purpose: Position the spindle motor center on the production of laser beam locus.
- Symptoms indicating need for adjustment: Track jumping. Long search times.

• Measuring instruments and jigs	• L-shaped eccentric driver (GGV-129) • 2.5mm hexagonal wrench
• Measuring position	• Oscilloscope
• Test disc and player mode	• FTSB assembly CN102-3 (TRKG error) and CN102-7 (TRKG sum)
• Adjustment position	• CD test disc • Test mode (TRKG servo: open/close)
	• Spindle motor centering adjustment hole • Grating

Connection diagrams



Adjustment Procedure

Note: This adjustment is necessary only when indicated by the Spindle Motor Centering Check.

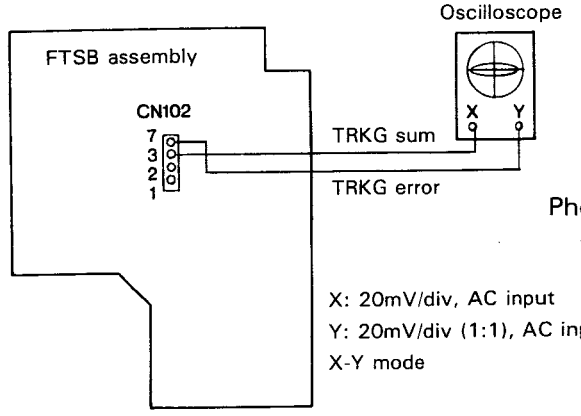
1. Loosen the three spindle motor setscrews by turning each about half a turn.
2. Connect the oscilloscope X input (CH-1) to CN102-3 of the FTSB assembly, and the Y input (CH-2) to CN102-7.
3. Play a CD test disc, and move the pick-up to the outer tracks of the disc by scanning or searching.
4. Open the TRKG servo, and observe the Lissajous figures of the TRKG error and TRKG sum signals.
5. Fine adjust the grating until the amplitude of the Lissajous figures along the Y axis reaches a minimum. (See Photo 7.)
6. Close the TRKG servo, and move the pick-up to the inner tracks of the disc by scanning or searching.
7. Open the TRKG servo again and observe the Lissajous figures. Record the amplitude on the Y axis.
8. Insert the L-shaped eccentric screwdriver into the adjustment hole, and slowly turn in the direction which reduces the Lissajous figures amplitude on the Y axis. After reaching the minimum amplitude, continue turning the eccentric driver to the same direcction until the same amplitude as that recorded in step 7 is reached. (See Photos 6 thru 8.)
9. Close the TRKG servo, and move the pick-up back to the outer tracks of the disc by scanning or searching.
10. Repeat steps 4, 5, and 6.
11. Open the TRKG servo again and observe the Lissajous figures. Check that the amplitude along the Y axis has reached a minimum. If the Lissajous figures are still inflated in the Y axis direction, repeat steps 8 thru 11.

2. SPINDLE MOTOR CENTERING CHECK

- Purpose: Check that the spindle motor is centered on the locus traced by the laser beam.

• Measuring instruments and jigs	• Oscilloscope
• Measuring position	• FTSB assembly CN102-3 (TRKG error) and CN102-7 (TRKG sum)
• Test disc and player mode	• CD test disc • Test mode (TRKG servo: open)
• Adjustment position	• Lissajous figure check

Connection diagrams



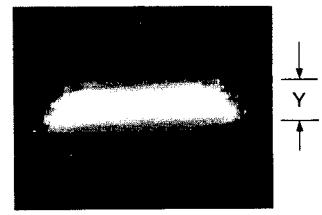


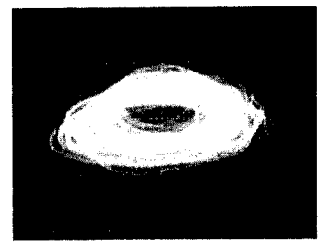
Photo 3 Lissajous figure at inner track of CD disc

Photo 4 Lissajous figure at outer track of CD disc

Check Procedure

1. Play a CD test disc.
2. Move the pick-up to the inner tracks of the disc by scanning or searching, and then open the TRKG servo.
3. Connect the oscilloscope X input (CH-1) to CN102-3 of the FTSB assembly, and the Y input (CH-2) to CN102-7. Switch the oscilloscope to X-Y mode and observe the Lissajous figures of the TRKG error and TRKG sum signals.
4. Record the amplitude of the Lissajous figures along the Y axis.
5. Close the TRKG servo, and move the pick-up to the outer tracks of the disc by scanning or searching. Open the TRKG servo again and observe the Lissajous figure.
   Check that the amplitude of the Lissajous figures along the Y axis is the same as that recorded in step 4 above.

If it is not the same, proceed to the "Spindle Motor Centering Adjustment" procedure.



Lissajous figure indicating need for adjustment

Photo 5.

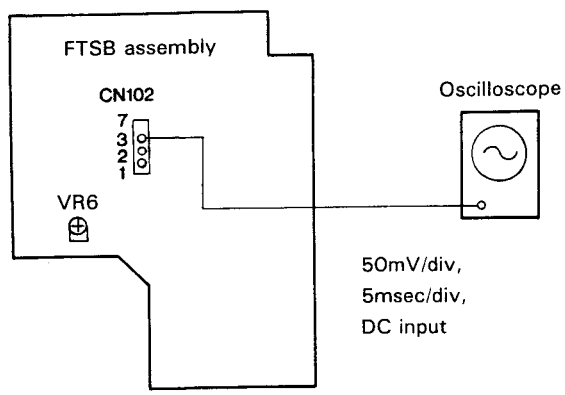
8.3 MECHANICAL ADJUSTMENTS

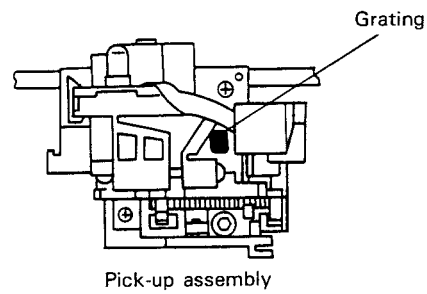
1. ROUGH GRATING AND TRACKING (TRKG) BALANCE ADJUSTMENTS 8.3 Mechanical Adjustments

- Purpose: Adjust the laser beam (divided into 3 beams by grating) to the optimum position on the playback tracks. Adjust TRKG servo offset voltage to 0V.
- Symptoms indicating need for adjustment: Improper tracking (Jumping, Skipping etc.)

• Measuring instruments and jigs	• Small screwdriver • Oscilloscope
• Measuring position	• FTSB assembly CN102-3 (TRKG error)
• Test disc and player mode	• LD test disc #16,000 (#15,000) • Test mode (TRKG servo open)
• Adjustment position	• Grating • FTSB assembly VR6 (TRKG balance)

Connection diagrams





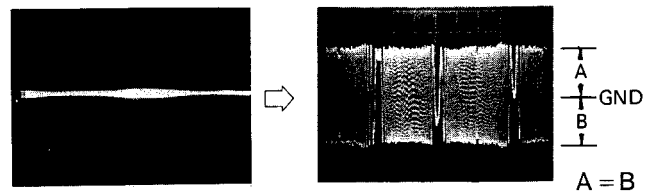


Photo 1. On-track position

Photo 2. Maximum amplitude

Adjustment Procedure

<Rough Grating Adjustment>

1. Play an LD test disc.
2. Press the DISPLAY key to display the frame # on the TV screen.
3. Move the pick-up to frame #16,000 (#15,000) by scanning or searching.
4. Open the TRKG servo. (See p.50.)
5. Connect the oscilloscope to CN102-3 of the FTSB assembly and observe the waveform.
6. Insert a small screwdriver into the grating adjustment hole (see p.51) and turn the grating so that the omplitude of the TRKG error signal varies large and small alternately. Find the position where the waveform amplitude reaches a minimum with a smooth waveform envelope. (See Photo 1.) (This condition indicates that the 3-way split laser beam is directed onto a single track. This is called the "on-track" position.)
7. Slowly turn the grating counterclockwise from the on-track position until the gradually increasing TRKG error waveform amplitude reaches a maximum. (See Photo 2.)
8. Close the TRKG servo and check that a normal picture is displayed on the TV screen.

<TRKG Balance Adjustment>

1. Align the oscilloscope GND with the center of the oscilloscope screen.
2. Adjust VR6 in the FTSB assembly to a position where the positive and negative halves of the TRKG error waveform are equal. (See Photo 2.)

4. Grating adjustment

Grating can be adjusted in two different ways.

– Adjusting with player standing on its side –

Stand the player on its side as shown in Fig.3. The grating can be adjusted by inserting a small screwdriver through the gap between the mechanical assembly and the 2FSB assembly. (Figs.9 and 10)

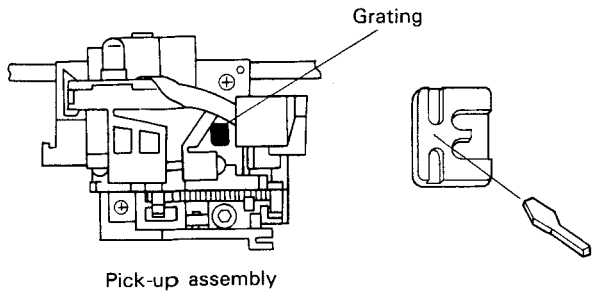


Fig.9

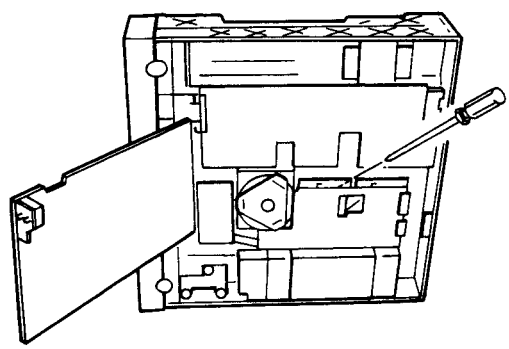


Fig.10

– Adjusting with player lying flat –

Approaching from the direction shown in Fig.11, insert a small screwdriver along the edges of the two guides in the pick-up assembly as shown in Fig.12 and into the grating adjustment hole.

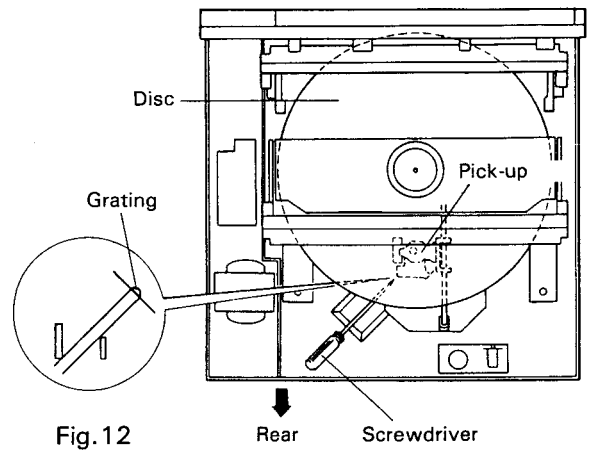


Fig.12

Fig.11

5. Test discs

The LD test discs used in these adjustments may be either N series or F series. The frame numbers given in the text are N series numbers while those enclosed in parentheses are F series numbers.

6. Unless specified otherwise, all oscilloscope settings shown in the connection diagrams are values obtained by using a 10:1 probe.

8. ADJUSTMENTS

8.1 JIGS AND INSTRUMENTS REQUIRED FOR ADJUSTMENTS

- Small screwdriver (about 7cm long axis)
- Small Philips head screwdriver (at least 15cm long axis)
- Hexagonal wrench (2.00mm and 2.5mm)
- L-shaped eccentric driver (GGV-129)
- 1.5V battery with lead wires
- Low-pass filter (100k Ω + 1μF)
- Dual-trace oscilloscope (with delay)
- AF generator
- Frequency counter
- LD test disc (N or F series)
- LDD disc (local purchase)
- CD test disc (YEDS-7)
- Shorting clips
- Digital voltmeter

8.2 ADJUSTMENT PREPARATIONS AND PRECAUTIONS

1. Player settings

For most adjustment procedures, the player should be stood on its side with the power transformer at the top and the VSOP assembly open. The 2FSB assembly CN33 connector may also be disconnected at this stage.

2. Prevention of double clamping

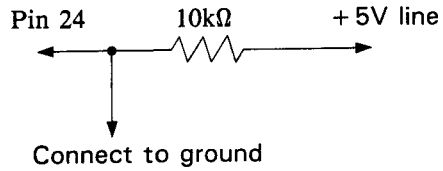
When the disc tray is in position and a disc is clamped, the clamping action is actually performed twice. This is called "double clamping".
If double clamping is performed while the player is stood on its side for adjustment purposes, however, the disc will fall off the turntable. Therefore, short circuit pin 3 (white lead) to pin 4 (white lead) of CN22 in the VSOP assembly to prevent double clamping.

3. Opening the tracking servo

The tracking servo can be opened and closed during test mode controlled by microcomputer.

— Switching to test mode —

1) Switch the power off.
2) See the patterned side of the VSOP assembly and find the 10kΩ resistor connecting pin 24 of IC7 (CXD1095) and +5V line. Connect the IC side of the resistor lead ground.



3) Switch the power on and check that the entire fluorescent tube display on the front panel comes on.

Note 1. The player can still be used in the normal way during test mode.
2. After switching to test mode, the ground connection described above in 2) can be disconnected without effecting test mode.
3. The disc is only stopped, not ejected, when the EJECT key is pressed in test mode.
4. Normal fluorescent tube display operation can be restored by pressing [CX] + [0] once. Pressing a second time turns the entire display back on.

— Opening and closing the tracking servo —

The tracking servo is opened by pressing [CX] + [3] on the remote control unit continuously. The servo is closed by pressing [CX] + [3] again. (The tracking servo is subsequently opened and closed alternately each time [CX] + [3] is pressed.)

— Cancellation of test mode —

Test mode can be canceled by switching the power off, or by pressing [CX] + [9] on the remote control unit.

7.2 DISC TRAY REMOVAL

7.2.1 Disc Tray Removal Procedure

1. Remove the bonnet. (Fig.1)
2. Switch the power on and press the OPEN/CLOSE key to eject the disc tray. Then switch the power off and push the disc tray in by about 5cm.
3. Extract the rivet by pulling upwards, and remove the switch spring. (Fig.5)

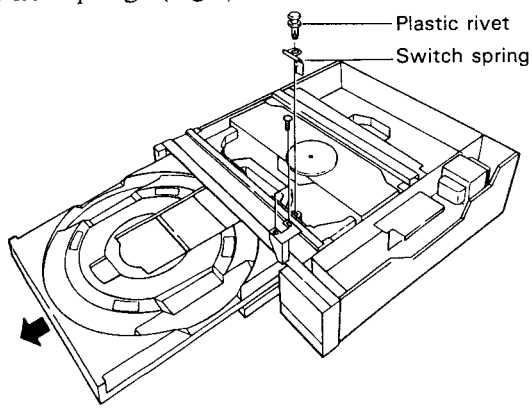


Fig.5

4. Undo a screw to remove the stopper plate. (Fig.5)
5. Remove the disc tray by gently pulling forward.

7.2.2 Method for Clamping Disc when Disc Tray is Removed

1. Insert disc from the rear and place it on the turntable.

Note: Take care not to let grease from the rails get on the disc surface.

2. Pull the lock levers (L) and (R) toward the rear while being pushed outwards, the clamper is lowered to clamp the disc. Check that the disc has been properly clamped by turning the clamper by hand. (Fig.6)

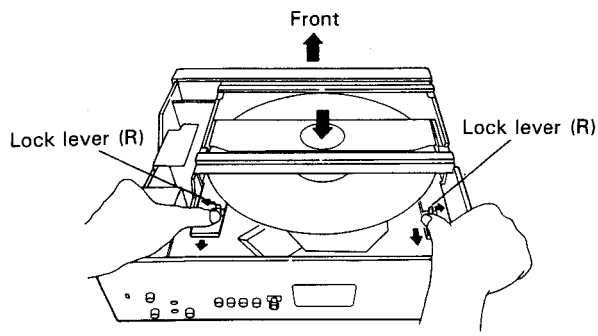


Fig.6

7.2.3 Play Procedure while Disc Tray is Removed

1. Switch the power on while pressing the slide switch, and then immediately press the play key. Release the slide switch after the disc starts to turn. (Fig.7)

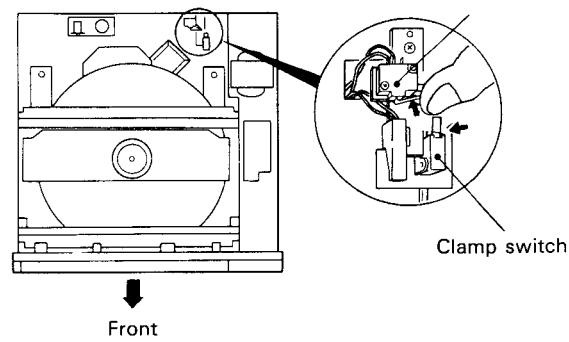


Fig.7

7.2.4 Disc Tray Insertion and Ejection

1. Insert the tray after aligning the disc tray tooth with the missing tooth section of the gear. (Fig.8)
2. Insert the rivet, switch spring, and stopper plate removed in steps 3 and 4 in procedure 7.2.1.

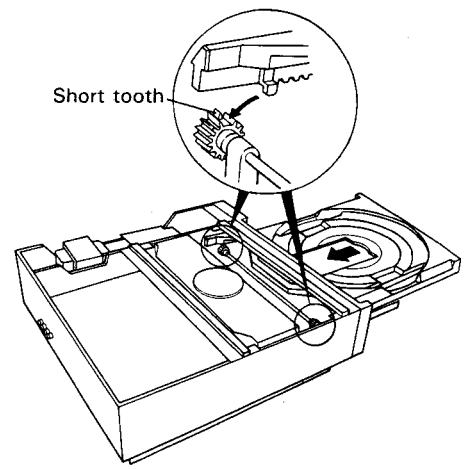


Fig.8

7. PICK-UP ASSEMBLY REPLACEMENT PROCEDURES

7.1 PICK-UP ASSEMBLY REPLACEMENT

1. Remove the bonnet and the bottom plate. (Fig.1)

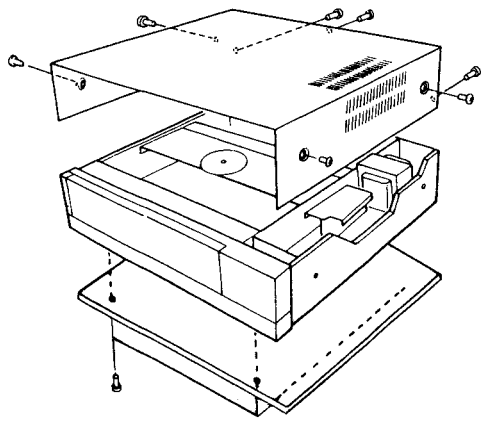


Fig.1

2. Switch the power on and press the OPEN/CLOSE key to eject the disc tray. Then switch the power off.
3. Shift the pick-up assembly to the position shown in Fig.2.

Note: Rather than turning the slider motor by hand, the pick-up assembly can be readily moved by connecting a 1.5V battery across the slider motor terminals.

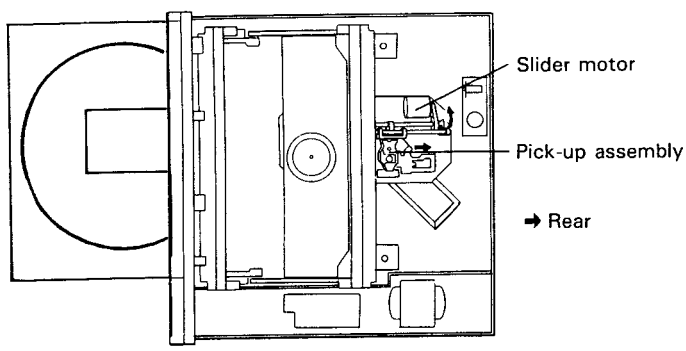


Fig.2

4. Stand the unit on its side with the power transformer at the bottom. Undo the four VSOP assembly screws and the two rear panel screws.
   Open the VSOP assembly and disconnect CN33 from the 2FSB assembly. (Fig.3)

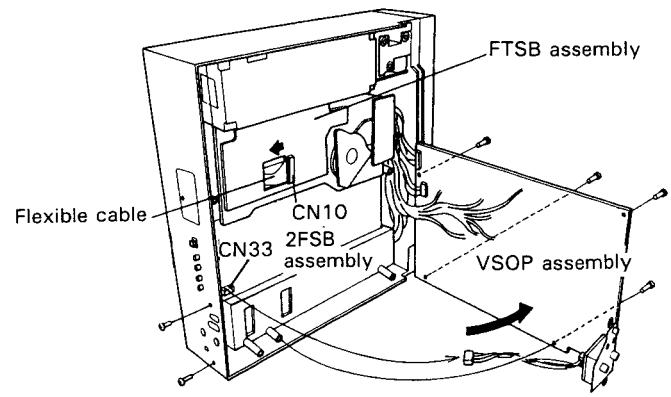


Fig.3

5. Disengage the CN10 lock in the FTSB assembly and carefully remove the flexible cable. In addition to protecting the cable from damage, also guard against electrostatic damage to the laser diode. For maximum protection, do not touch the conductor section of the cable under any circumstances.
6. Undo the pick-up securing screw from the top of the unit, and carefully remove the pick-up assembly. (Fig.4)

Note: Do not touch soldered sections on the pick-up assembly.

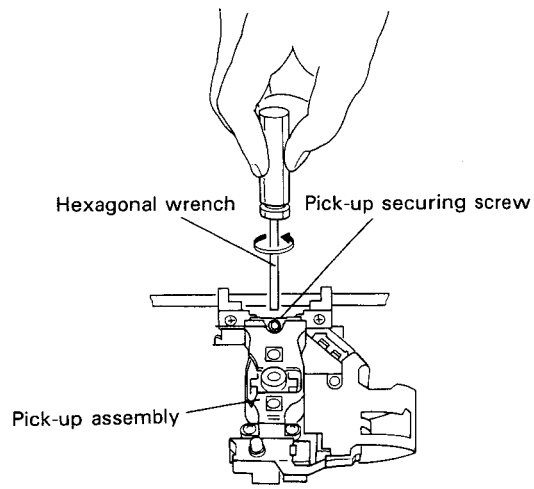


Fig.4

7. Mount a new pick-up assembly, tighten the securing screw, and carefully reconnect and lock the flexible cable to CN10 in the FTSB assembly. This completes replacement of the pick-up assembly.

Note: After replacing the pick-up assembly, check the spindle motor centering. (Refer to Page 53)

3306

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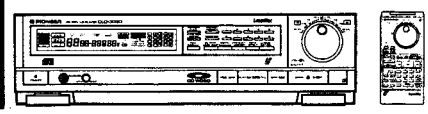
Service Manual



SERVICE GUIDE
ORDER NO.
ARP 1560

CD CDV LD PLAYER

CLD-3030

CONTENTS

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS SERVICE INC. P.O. Box 1760, Long Beach, California 90801 U.S.A.
PIONEER ELECTRONICS OF CANADA, INC. 505 Cochrane Drive, Markham, Ontario L3R 8E3 Canada
PIONEER ELECTRONIC [EUROPE] N.V. Keetberglaan 1, 2740 Beveren, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia TEL: [03] 580-9911

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3306

1. FOCUS (FOCS), TRACKING (TRKG), SLIDER (SLDR) AND TILT SERVOS (DESCRIPTION OF THE HA11529).

1.1. SUMMARY

The HA11529 is an analog/digital hybrid bipolar IC which performs the following functions:

1. FOCS servo control (FOCS servo loop pull in control, FOCS servo loop gain control)
2. TRKG servo control (TRKG servo loop ON/OFF and brake control during track jump and SCAN operations)
3. SLDR servo control (SLDR servo loop ON/OFF, variable speed transport, motor PWM drive)
4. TILT servo control (TILT servo loop ON/OFF)
5. CD/LD FOCS and TRKG servo switch
6. All of the above functions are controlled by 8-bit serial data passed through a serial bus (DATA, CLK, LATCH).
   The 8-bit serial data commands are as shown below.

MODE	ADDRESS DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
SCAN MODE CONT	1	0	0	0	SCAN SPEED 1	SCAN SPEED 2	SCAN SPEED 3	1: SCAN ON 2: SCAN OFF
SERVO CONTROL 1	1	0	0	1	FOCS 1: ON 0: OFF	DIRECTION 1: FWD 0: RVS	TILT 1: ON 0: OFF	1: LD 0: CD
SERVO MODE CONTROL 2	1	0	1	0	TRKG Zero cross output 1: 1/256 0: Through	TRKG 1: OFF 0: ON	TEST 1: TEST 0: NORMAL	—

* It is possible to set SCAN SPEED at 7 stages using the 3 bits, D3/D2/D1.

1.2. HA11529 Pin Functions

Pin No.	Pin Function
1.	Vee: −5V
2.	FOCS ERROR signal input: OP AMP input to which a SW is connected for gain control during SCAN
3.	FOCS SUM input: For DISC detection. Comparator input threshold is +0.4V.
4.	Comparator input threshold for the FOCS S-curve detection is +0.3V.
5.	Comparator input threshold for MAIN BEAM ON/OFF track detection is +0.5V. FOCS SUM input.
6.	TRKG ERROR input: Comparator input threshold for TRKG ERROR zero cross detection is 0V.
7.	GND
8.	TRKG ERROR AMP for CD input
9.	TRKG ERROR AMP for LD input
10.	TRKG ERROR AMP output. TRKG servo phase compensation is connected between this pin and pins 8, 9.
11.	Output for switching the TRKG servo loop characteristics during track jump.
12.	Outputs the actuator drive and brake pulse during track jump and the actuator brake pulse during SCAN.
13.	Window comparator input to detect the amount of movement in the TRKG actuator during SCAN. Threshold voltage is 0.2V. Actually, an FTS SCAN signal is being input.
14.	Current setting terminal for TRKG actuator brake.
15.	Current setting terminal for pins other than 14P
16.	TRKG RTN input: TRKG RTN input for SLDR servo.
17.	SLDR servo amp output: During play, the SLDR motor is PWM driven and at that time this pin becomes the window comparator input.
18.	SLDR drive signal output during play or when high speed slider is in operation.
19.	SLDR drive signal input when SLDR is operating at low or mid speeds.
20.	Capacitor connected pin for setting the slope of the reference triangular wave for the SLDR motor PWM drive during play.
21.	Resistor-connected pin to set comparator threshold for turning off the TILT servo drive.
22.	TILT ERROR input: op amp input.
23.	A VR is connected for setting the TILT servo gain with the output of the op amp from 22P.
24.	Output for TILT motor drive.
25.	T-CROSS output: TRKG ERROR zero cross count output. Depending on the serial data command, output may be divided by 256.
26.	F-LOCK: L when FOCS lock activated.
27.	J-TRIG input: triggered at startup. L under normal operating conditions.
28.	RESET input:
29.	LATCH input: serial interface bus to the system microprocessor CPU. (29, 30, 31P) Data is latched on the trailing edge.
30.	SDATA input: 8-bit serial command data input.
31.	SCLK input: clock for serial data transmission.
32.	500kHz input: internal logic clock input.
33.	TEST pin: normal state = L.
34.	Pin for setting the injection current used by internal I2L logic.
35.	Capacitor connected pin for setting the lens UP/DOWN cycle when FOCS ON is activated.
36.	Drive voltage output for lens UP/DOWN.
37.	FOCS Error amp output: FOCS servo phase compensation is connected between 38, 39P.
38.	FOCS Error LD input.
39.	FOCS Error CD input.
40.	Pin with connected offset adjustment VR that uses the uninverted FOCS Error amp input
41.	Op amp output for FOCS gain control
42.	Vcc: +5V.

1.3. DESCRIPTION OF FUNCTIONS

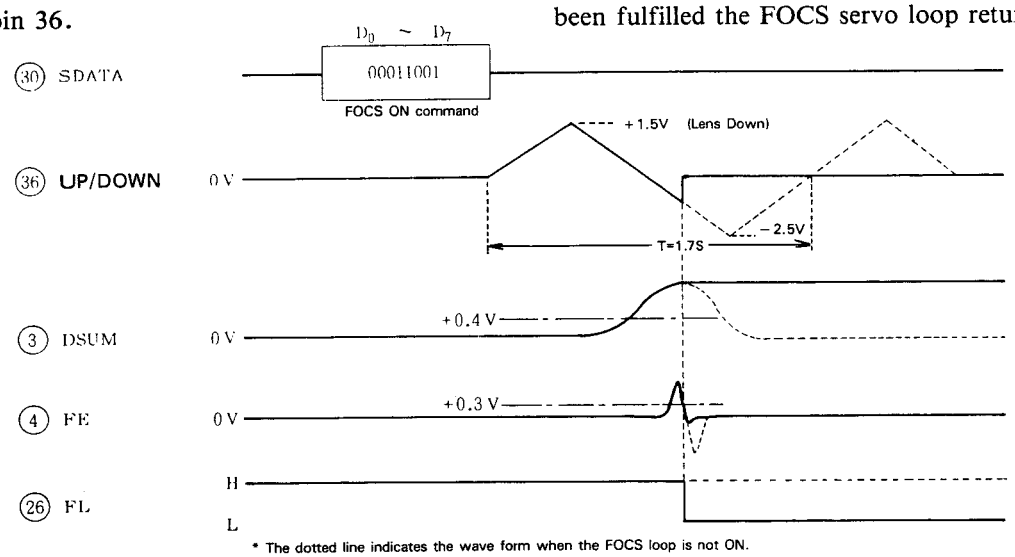
1.3.1. FOCS Assembly

1) FOCS pull in operation

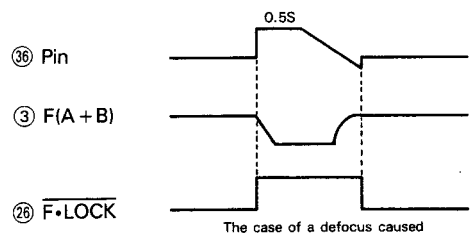
The pull in operation of the FOCS servo raises the objective lens UP/DOWN and, when the input of DSUM (pin ③) and FE (pin ④) fulfill FOCS lock conditions, turns the FOCS servo loop ON. In the case of a defocus caused by damaged disc, the FOCS servo loop is turned OFF and, about 0.5 seconds later, a voltage of +0.6V is output at pin 36.

2) FOCS down and repeat pull in

When the input of DSUM (pin ③) falls below +0.4V as a result of a damaged disc or excessive external vibration, the unit detects an abnormal condition. When this occurs the FOCS servo loop is turned off and at the same time the objective lens is automatically moved UP/DOWN. When conditions as described in 1) have been fulfilled the FOCS servo loop returns to ON.



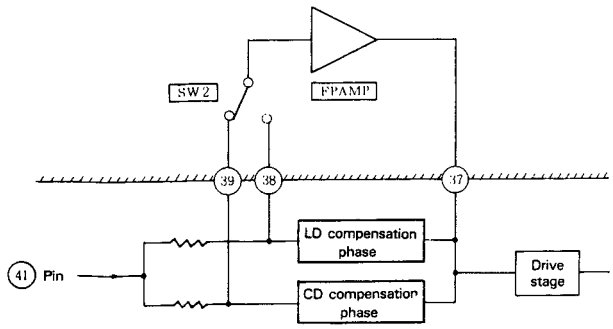
* The dotted line indicates the wave form when the FOCS loop is not ON.



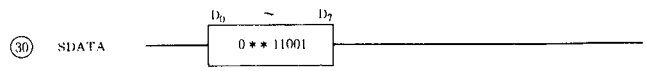
The case of a defocus caused

3) CD/LD switching

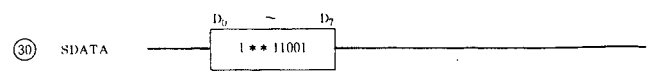
Depending on what type of disc is being played, compact disc or laser disc (CD or LD), a switch alters the loop gain and phase compensation of the FOCS servo for the particular disc type. The serial data bit for the CD/LD switch has the same address as the FOCS ON command bit and both can be set with a single transmission.



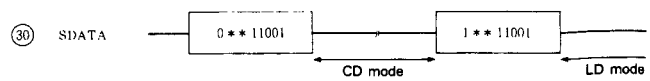
i) Focus ON command when the CD mode is set.



ii) FOCS ON command when the LD mode is set.



iii) When the CD/LD mode is switched in the middle of playback (CD mode → LD mode)



Note 1) The asterisks (*) represent bits which bear no relation to the operation under examination. (This convention will be used throughout the manual.)

1.3.2. TRKG Assembly

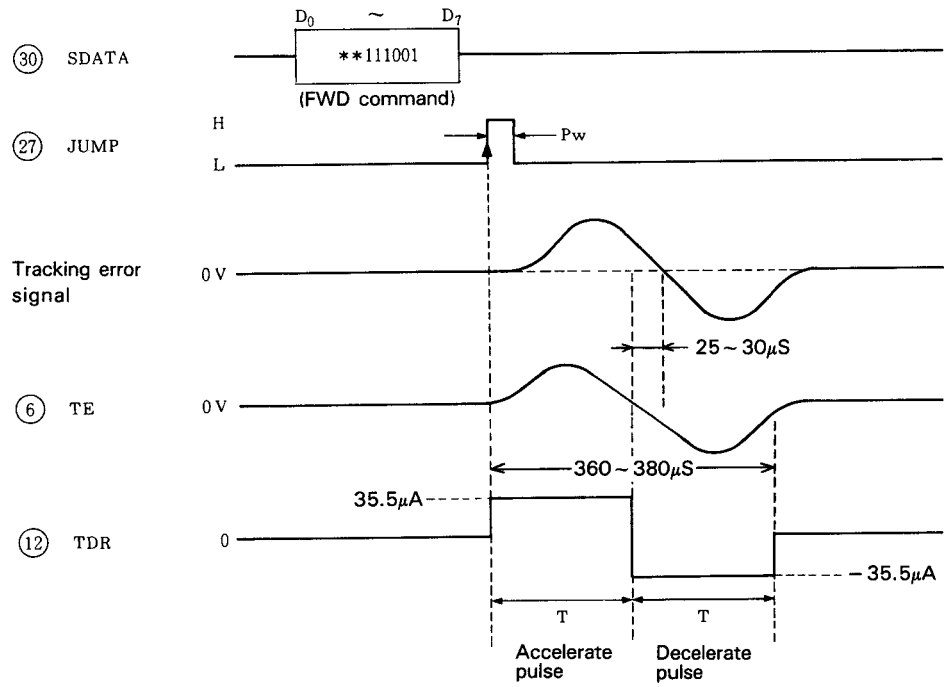
1) Track jump operation

Track jump commences when the jump trigger start-up pulse is received from JUMP (pin ㉗). Acceleration and deceleration switching are performed by monitoring tracking error zero cross. During a jump operation, SW12 and SW24 are activated sequentially. SW12 is used to switch TRKG loop characteristics and SW24 for adjusting the position of TRKG error zero cross.

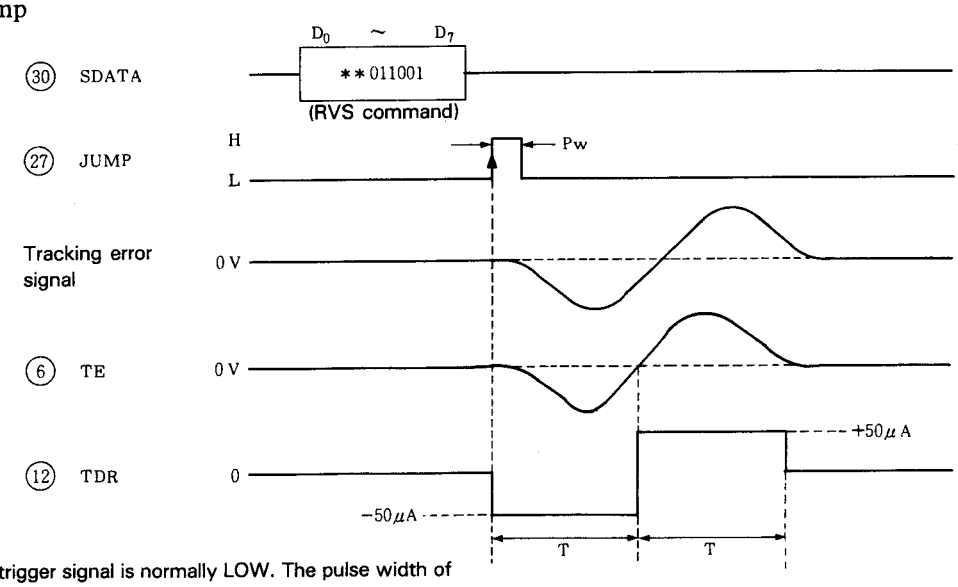
Switching between forward and reverse jump is performed by serial data transmission.

The jump trigger signal, by turning Q17 OFF only during a jump, cuts off C54 to which 6P is connected so that the phase of the input signal to 6P can be pushed forward beyond its position during normal operation.

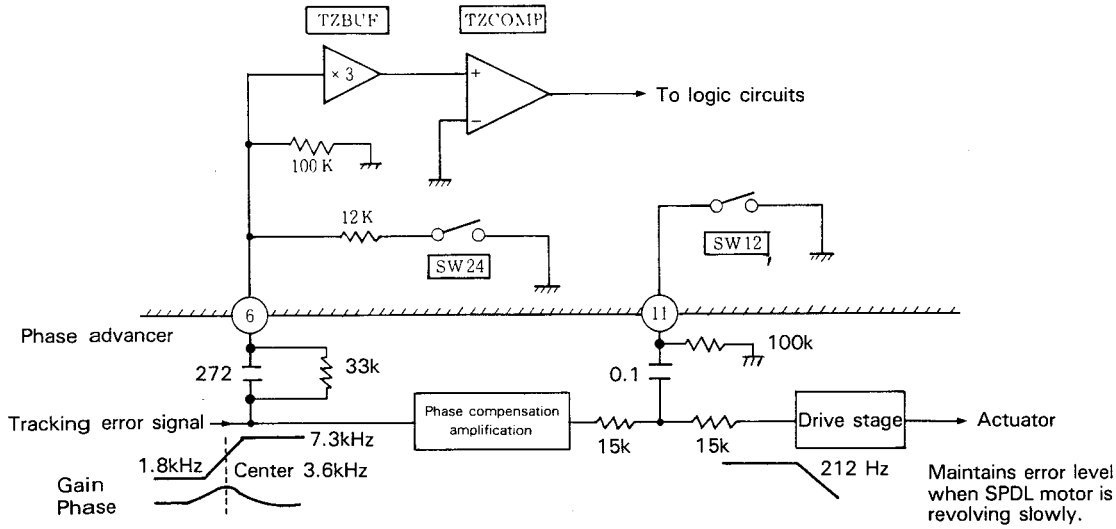
i) Forward jump



ii) Reverse jump



Note 1) The jump trigger signal is normally LOW. The pulse width of Pw is set at 9.6μS.



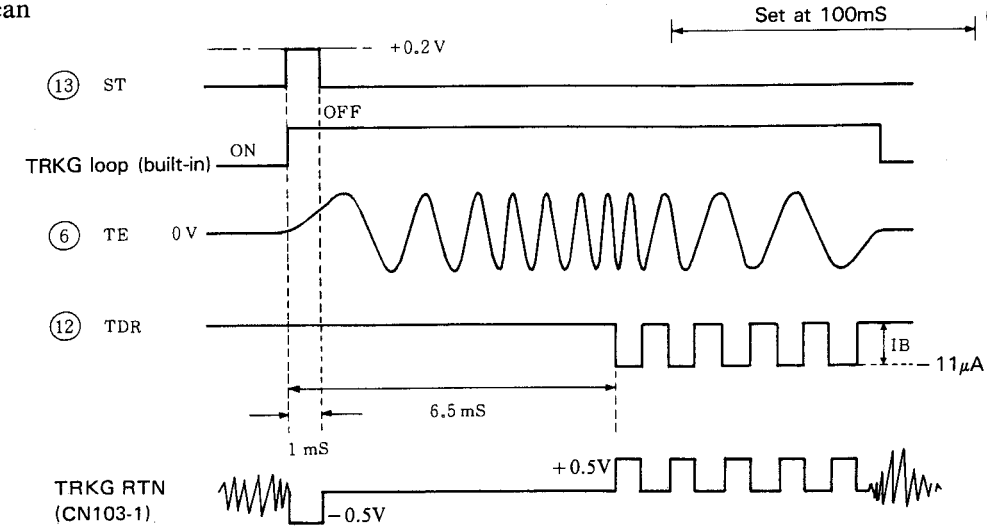
2) Scan operation

During slow or medium scan the TRKG servo performs ON/OFF control of the TRKG loop. Input to ST (pin ⑬) signals displacement of the actuator position and the TRKG loop is turned OFF. When the error signal at TE (pin ⑥) drops below a set frequency, the TRKG loop is turned back ON.

While the TRKG loop is OFF, a brake pulse is output by TDR (pin ⑫) according to the timing charts shown below. The polarity of the brake pulse is not a direction command sent via serial data but is determined by the polarity of the signal input to ST (pin ⑬). Corresponding to actuator speed as detected by TE (pin ⑥), brake pulse duty is automatically set to operate in 5 stages (50%-100%). Brake current IB can be adjusted at BSET (pin ⑭).

Because switch timing for the open/close operation of the TRKG servo loop during SCAN is determined by the system microprocessor, an FTS signal like that shown below is actually input to pin ⑬.

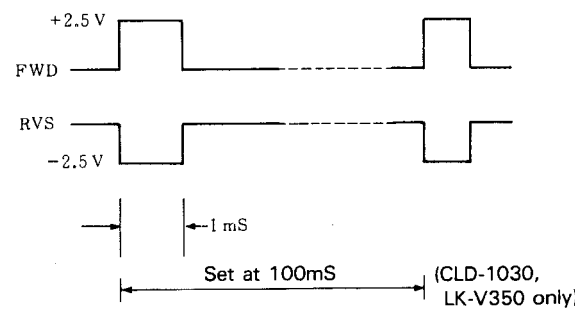
i) Forward scan



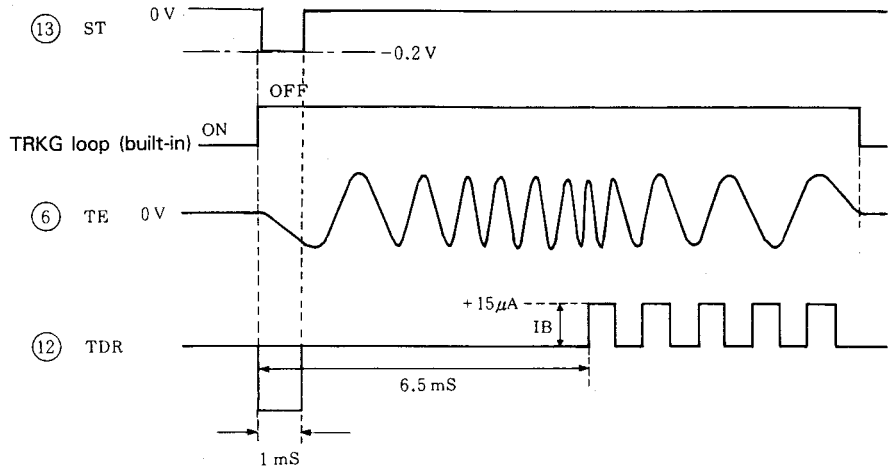
This signal also flows into pin ⑫, but the polarity of the brake pulse is opposite to it, which acts to improve convergence during braking.

The cycle of the FTS SCAN signal varies depending on the absence or presence of video memory.

1) The CLD-3030 (with video memory)
   After a jump, the TRKG servo loop closes and if one field worth of data has been properly written to memory, the following FTS scan signal is output. To account for possible mistakes in writing to memory, the period for this operation is not fixed.
2) CLD-1030, LK-V350
   The period is set at 100mS.

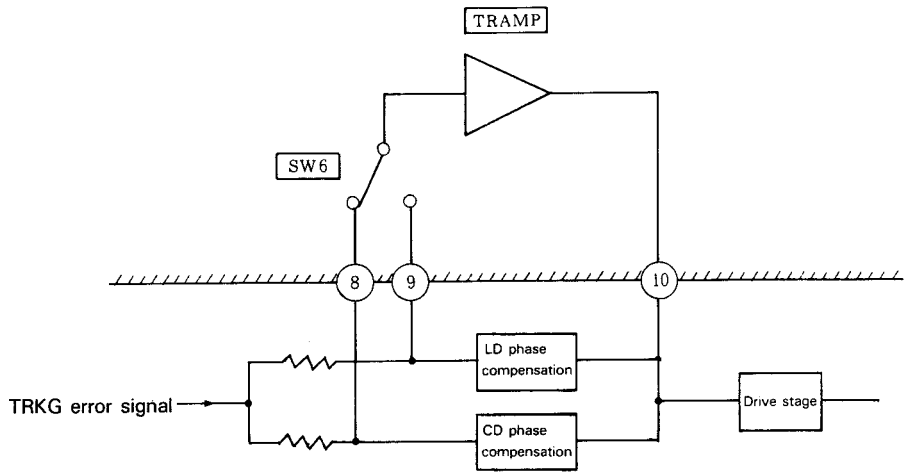


ii) Reverse scan



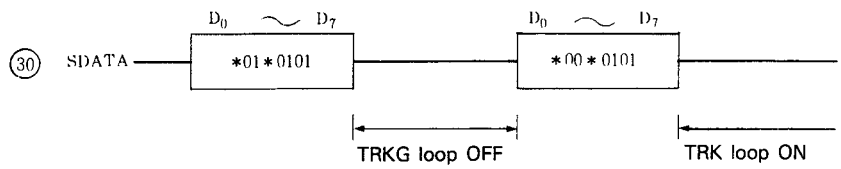
3) CD/LD switching

Switching between CD and LD is performed in exactly the same way as CD/LD switching for the FOCS servo.



4) TRKG loop ON/OFF control

Switching the TRKG loop ON/OFF is done by means of serial data transmission.



5) TRKG count

The number of tracks crossed during high speed scan is counted and then, according to the serial data transmission, a choice is made to either divide (1/256) the output TCNT (pin ㉕) pulse or output it as is.

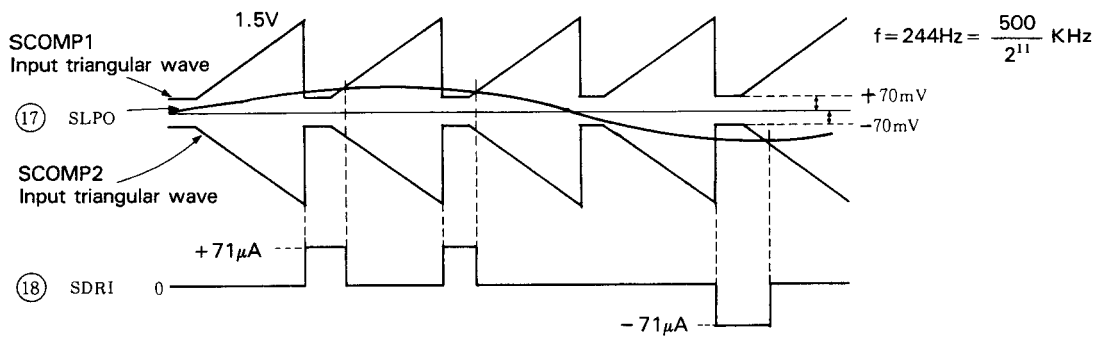
When a misclamp is detected at the beginning of play, the pulse is divided (1/256) and when tracks are counted during CD search the pulse is output as is.

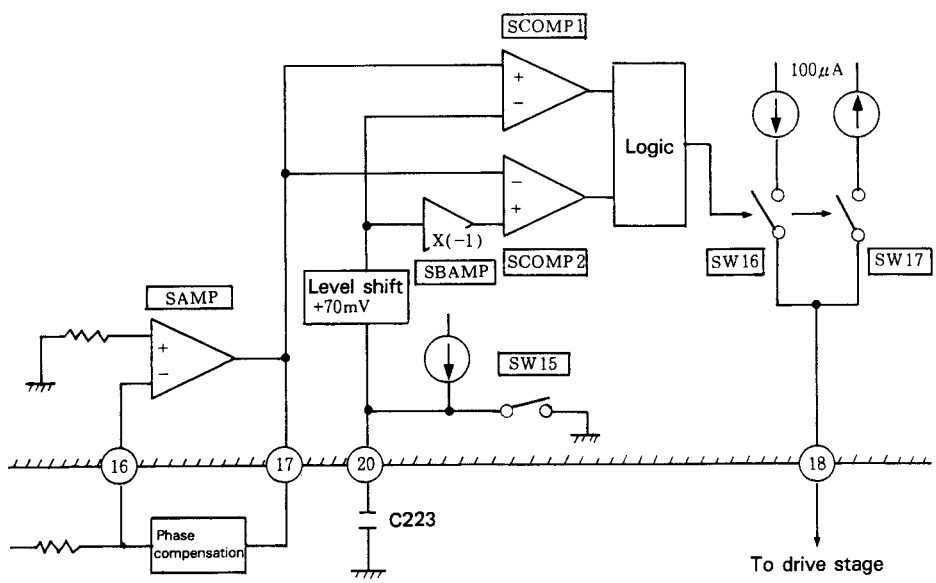
Once play has begun and the TRKG servo loop is open, track crossing is normal if the number of tracks crossed per disc rotation (6 FG pulses = 1 rotation) is under 1,280 tracks (TRKG count, 5 times: 1mm of eccentricity). If this number is exceeded, however, a misclamp is detected and the disc is ejected from the unit.

1.3.3. Slider Assembly

1) Operation in the normal play mode

During normal play DC components in the drive current of the TRKG actuator are PWM modulated at SCOMP1 and SCOMP2. This PWM pulse turns SW16 and SW17 ON and activates the output of the drive signal. The slope of the reference triangular wave can be altered by means of the capacitor connected to SLP (pin ⑳).



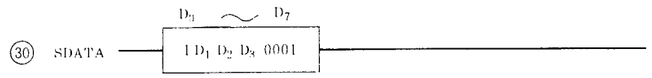


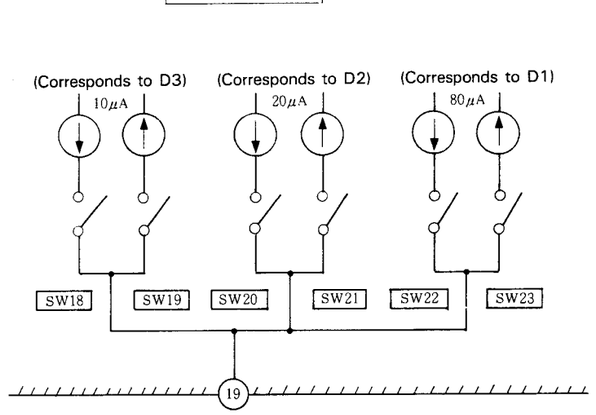
2) Operation in the scan mode

During a scan operation, the SLDR servo loop is OFF and a signal that agrees with the set speed as given by serial data transmission is output either from SDR2 (pin ⑲) or SDR1 (pin ⑱).

i) Low and mid speed scan

SW18, SW20 and SW22 (when set in the FWD direction) or SW19, SW21 and SW23 (when set in the RVS direction) correspond to the serial data, D3, D2 and D1. When the bit is "0", it is OFF, and when the bit is "1", it is ON. Furthermore, on the basis of these three bit combinations a current of 10μA — 110μA (FWD) or −10μA — −110μA (RVS) is output as a duty 50% pulse from SDR2 (pin ⑲). Actually, however, when the unit is used as a CD player, only ±110μA is used.

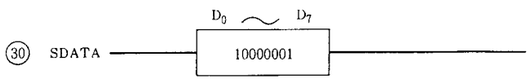




ii) High speed scan

By means of the serial data transmission shown at the right, SW16 or SW17 can be turned ON and a ±110μA drive signal output from SDR1 (pin ⑱). The direction is as given in the serial data transmission.

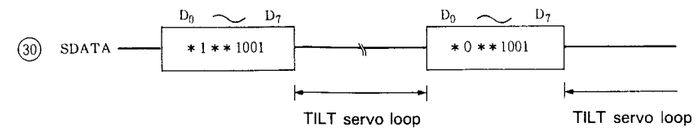
When the unit is used as an LD, the SCAN SPEED control function discussed above is not employed. A combination of the two commands, 10000001 for high speed SCAN and 10001110 that turns the SLDR servo loop OFF are used to control SLDR drive voltage and set SCAN SPEED.



1.3.4. TILT Assembly

1) Loop ON/OFF switch

The ON/OFF control of the TILT servo loop is performed by means of serial data transmission.

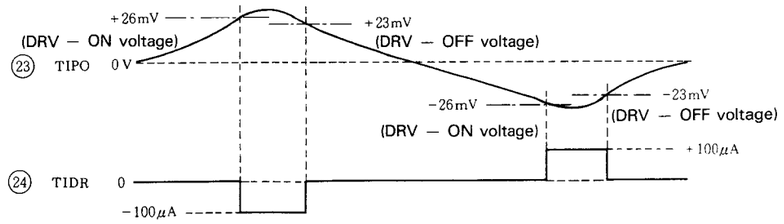


2) TILT servo operation

The TILT error signal is input to the window comparators TCOMP1 and TCOMP2. The drive voltage which is output at TSEF (pin ㉑) operates on an ON/OFF basis.

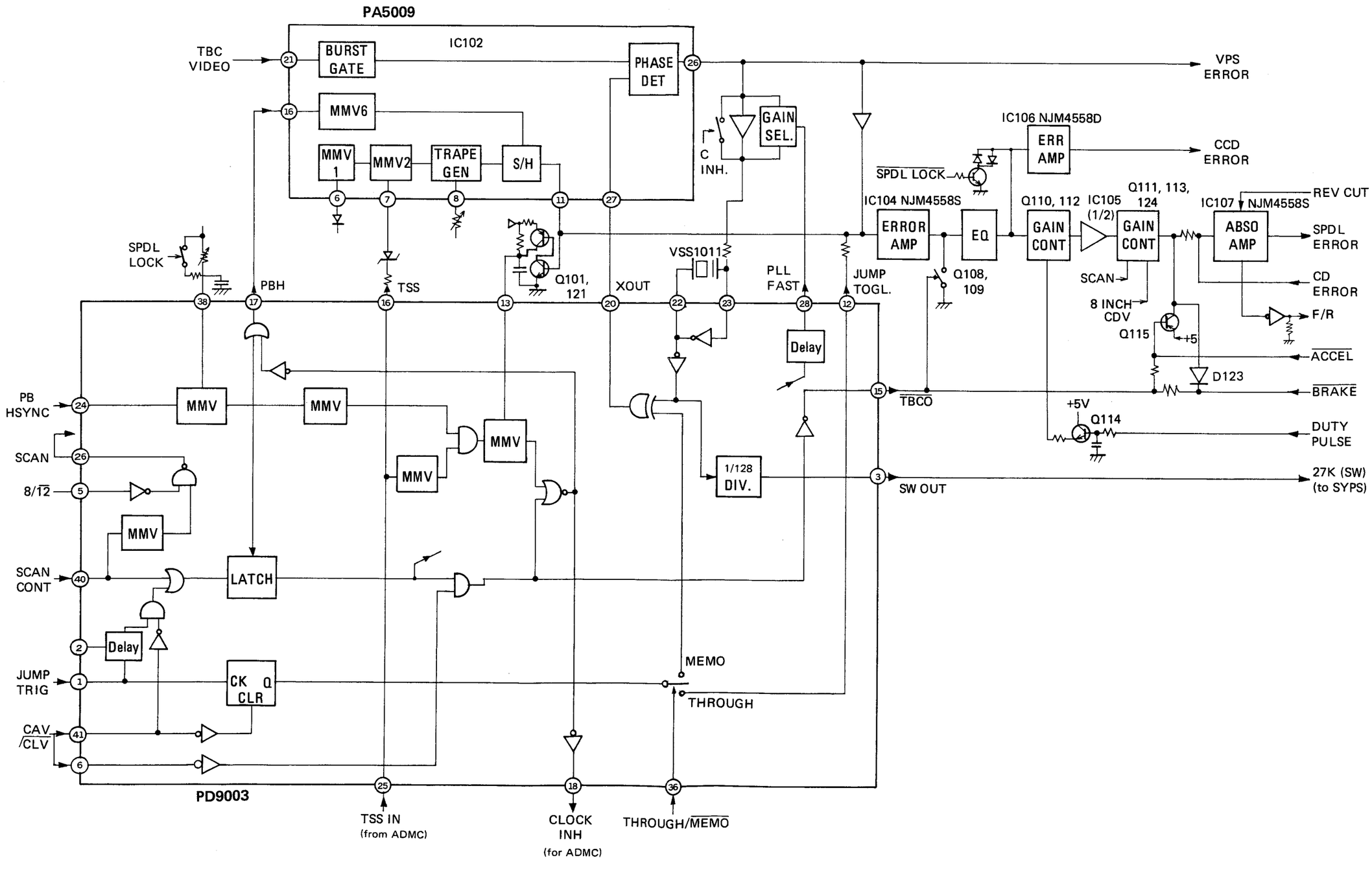
If input is higher than the TCOMP2 reference voltage (DRV — ON voltage), then ON; if input is lower than the TCOMP1 reference voltage (DRV — OFF voltage), then OFF.

DRV — OFF voltage can be adjusted at TSEF (pin ㉑).

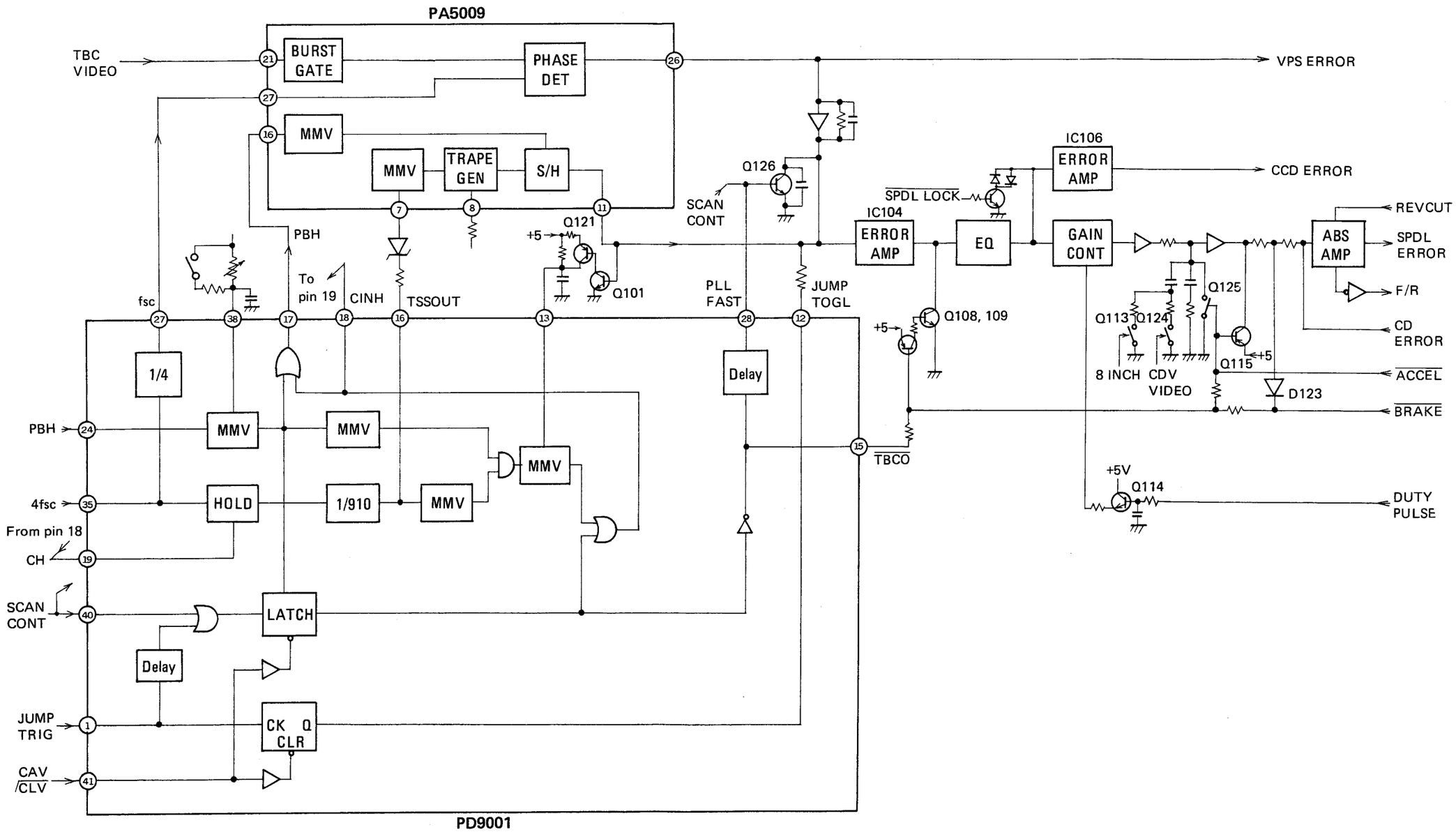


2. SPDL SERVO AND TBC (TIME BASE CORRECTOR)

2.1. VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-3030)



2.2. VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-1030, LK-V350)



2.3. DESCRIPTION OF VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-3030)

Comparison error between the trapezoid derived from the TSS signal (576fH/576) and PB-H (Playback H-synch) is output by IC102-11P (PA5009) and amplified by error amp IC104 (NJM4558S).

IC106 is the CCD error amp. After the SPDL servo lock is ON, Q123 becomes an error limiter. Q110 and 112 are variable gain amps and, as the collector voltage to Q110 rises, GAIN is lowered.

During CLV disc play, Q114 smooths out the duty pulse which is output by the system microprocessor CPU for SPDL servo loop gain control.

Q111 and 116 are GAIN switches during scan. Q113 and 124 are gain switches for 8INCH disc play and CDV disc play, respectively.

- **VPS (Video Phase Shift)**

VPS error is derived by phase shift comparison between PB-B (Playback-Burst) at IC102 and the output of 3.58M VCXO near 23 Pin, IC101 — 22 Pin.

Error output from IC102 - 26 Pin is input to the error amp of IC103 (1/2).

Gain switches Q104 and 105 have been added to IC103. When Q104 is OFF, error detection loop gain increases and activates the FAST mode.

When Q104 is ON, gain is lowered and because the detection loop trails only the low frequency components, high frequency error components remain in the error output of 26 Pin. These are output as VPS error to the VSOP Assembly (VDEM section).

The switch into the FAST mode is performed by means of the PLL FAST signal from 28P which delays TBCO output from IC101 - 15P.

- **CD/CDV play**

The operation of CDV video play sections is exactly the same as for LD video play.

During the audio play sections of CD or CDV, CD SPDL error is input to the absolute value amp IC107 by board 4FSB (digital decoder) and the SPDL motor driven.

2.4. SUMMARY OF SPDL & TBC

	CLD-3030
SPDL error detection CCD/CPC error detection	} PD9003 + PA5009
SPDL REF-H	T.S.S. (regardless of memory ON/OFF)

Frequency phase errors and CCD errors are detected by using the trapezoid generated from REF-H (Reference-H-synch) and PB-H (Playback-H synch), as well as the method of reference shift which delays REF-H by either 28μsec or 36μsec when necessary. Furthermore, spindle and CCD servos are always operating at the same time.

During SCAN and other operations, when the TRKG servo loop is open, REF-H is being held. And when the servo loop is closed, REF-H is activated in phase with PB-H. The fact that SPDL and CCD servos are turned on at the same time after a jump, with the CCD servo operating until the SPDL motor has been able to absorb frequency component errors, allows the color lock to be activated immediately after a jump.

Consequently, in the CLD-3030, since the TSS signal, which is the 576fH, A/D, D/A conversion clock of the video memory section, undergoes frequency division by 576 at PDJ002, is being employed, memory ON/OFF no longer has any bearing on the status of REF-H. In the CLD-3030, the ICs employed for SPDL servo detection and for CCD and CPC error detection are PD9003 and PA5009. The CLD-1030 and LK-V350 employ PD9001 and PA5009.

<Deleted features>

1. 910 dividing circuit and REF-H switch
2. 8/12 INCH recognition

<Added features>

1. 3.58MHz VCXO output is divided and a 27kHz signal generated for the SPDL motor PWM (formerly 2fH).
2. SPDL GAIN switch timing is derived from the SCAN CONT signal.

SPDL/CCD error detection, 3.58MHz VCXO, and JUMP TRIG signal processing sections are the same as the PD9001 and pin numbers and names for these sections have remained the same as well.

Because in the CLD-1030 and LK-V350, which have no video memory, there is no TSS signal either, it is necessary to frequency divide 4fsc by 910 for REF-H.

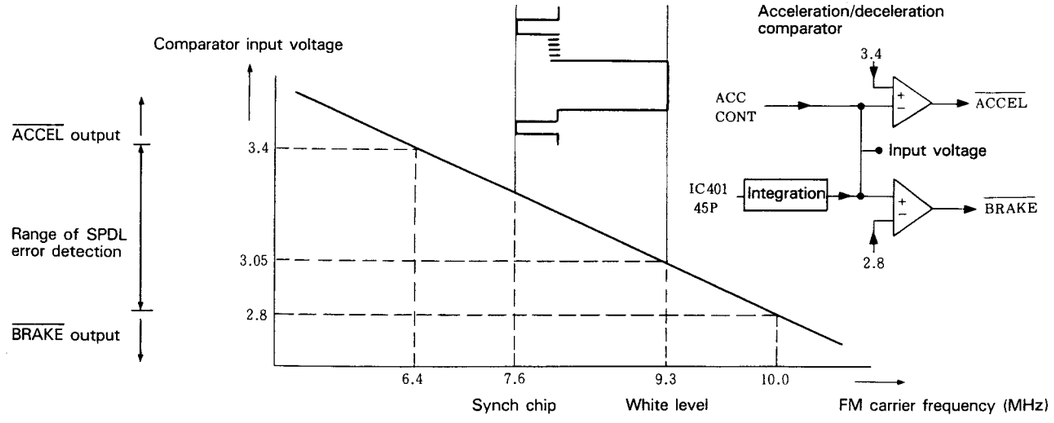
2.5 DETECTION AND CONTROL OF RUNAWAY SPDL MOTOR

In cases where the SPDL motor runs out of control, i.e., if the SPDL motor rpms for whatever reason get out of the servo's tracking range, speed can be controlled by using either acceleration (ACCEL) or deceleration (BRAKE) signals.

In this manual, voltage inversely proportional to the video FM carrier frequency in the RF signal from the screen image demodulation section is extracted and input to the acceleration/deceleration signal detection comparator.

The output of IC401 (PA5010) — 45P of the VSOP Assembly (VDEM, ADEM) is integrated and input to the comparator of IC403 (NJM2903). The input voltage to the comparator is as shown in the figure below.

When the FM carrier frequency is at the 100% white level, equivalent to 9.3M, the comparator input voltage is at 3.05V. The upper and lower threshold voltage levels are then set at the detection limits of the SPDL servo frequency error. The ACCEL signal is over 3.4V and the BRAKE signal is under 2.8V. Both are labeled L.



Detection works on the basis of DC voltage when the SPDL servo LOCK goes out of order and rotational speed is thrown off. ACCEL or BRAKE signals are output when disc speed goes beyond the tracking range of the servo. These oblige the spindle motor to accelerate or decelerate until rotational speed again falls within the range of servo control.

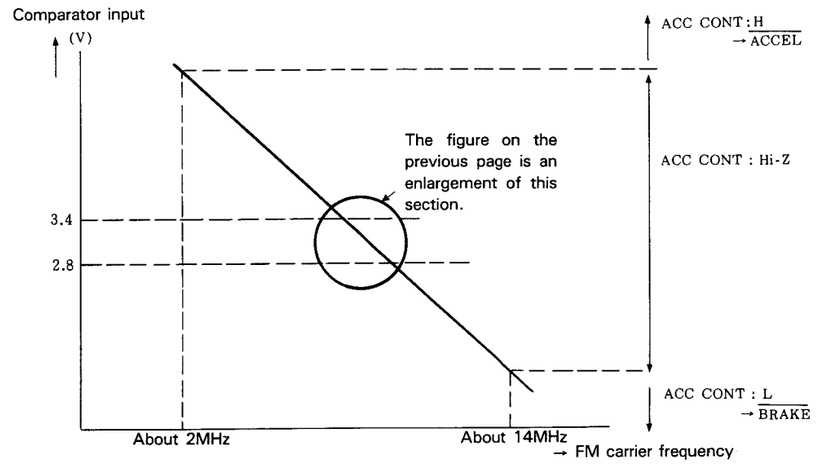
When the outer tracks of a CLV disc are being played and the SPDL motor is rotating relatively slowly, it may be possible, if the SPDL servo is locked, to detect acceleration or deceleration signals being used to maintain the FM carrier frequency within the range shown in the figure above.

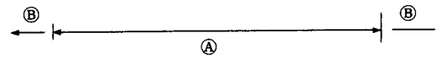
However, if the LOCK goes out of order and SPDL motor rotation is radically disrupted, the relation between frequency and DC voltage becomes non-linear and detection is no longer possible.

For this reason, the FG output cycle of the SPDL motor is measured by the system microprocessor CPU. If it falls into the areas marked B in the figure below, i.e., beyond 80% of reference speed, ACC CONT (ACCEL CONTROL) which is input to the acceleration/deceleration comparator registers either H or L and SPDL motor speed control is performed by the CPU.

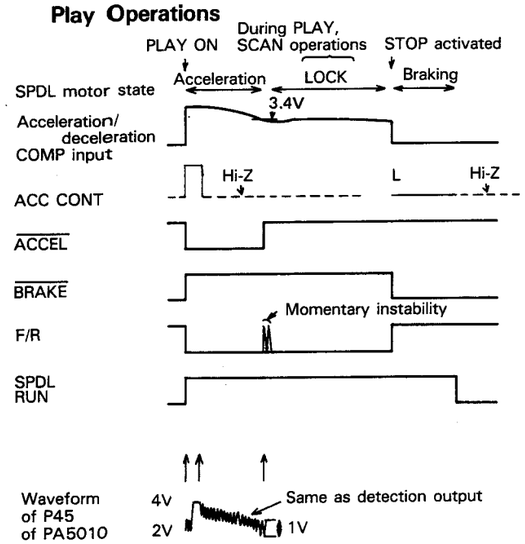
In addition, the system microprocessor CPU also performs SPDL motor stop detection at the conclusion of play based on the FG output cycle.

When rotational speed is within 80% of reference speed (the area marked off as A in the figure below), the ACC CONT signal is in a Hi-Z state and speed control is not performed by the CPU.





2.6 CLD-3030 SPDL Servo Timing Chart during LD Play Operations



Control Signals for SPDL Servo Timing

$\overline{\text{ACCEL}}$, $\overline{\text{BRAKE}}$: Output of the acceleration/deceleration comparator. The (3-state) ACC CONT signal from the system microprocessor CPU and the signal from 45P of PA5010 are integrate and input in the acceleration/deceleration comparator. The COMP input voltage in the Figure is derived from the sum of these two inputs.

$\overline{\text{F}}$/R : The signal at Q117, 118 which detects the polarity of the voltage going to the SPDL error absolute value amp in the SPDL servo circuit. This is input to the motor control IC on the BLDB board.

SPDL RUN : This is input to the motor control IC from the system microprocessor CPU. At SPDL start up, this becomes H along with ACC CONT. Later, this returns to L when the brake is released. (During rotation it is always H.)

< SPDL Start up Operation >

After FOCUS is locked, the system microprocessor CPU switches ACC CONT and SPDL RUN to H. When ACC CONT is H and $\overline{\text{ACCEL}}$ is L, Q115 is ON. This applies a positive voltage to the absolute value AMP (IC107) and about −1.5V is input as SPDL error to the SPDL drive circuit of SYPS assembly. At the same time, with Q117, 118 OFF, the $\overline{\text{F}}$/R signal shifts to L.

At this point, the configuration, SPDL RUN → L, $\overline{\text{F}}$/R → L, SPDL error → about −1.5V, triggers acceleration of the SPDL motor.

The system microprocessor CPU switches ACC CONT to Hi-Z when it detects that SPDL speed is within 80% of the reference value from the SPDL motor FG cycle.

Furthermore, the acceleration/deceleration comparator input is integrated at 45P of PA5010. At this point, with $\overline{\text{ACCEL}}$ at L and the application of DC 4V, acceleration of the SPDL motor continues.

As the SPDL motor accelerates, the acceleration/deceleration comparator input voltage drops. If it falls below the ACCEL threshold voltage, ACCEL switches to H and the SPDL/TBC servo loop closes.

When the loop closes, the SPDL servo performs reference shift and promptly locks.

<SPDL Brake Operation>

When the STOP or OPEN buttons are pressed, ACC CONT and $\overline{\text{BRAKE}}$ switch to L. Voltage is applied through D123 to the absolute value AMP (IC107), Q117, 118 shift to ON and $\overline{\text{F}}$/R shifts to H.

At this point, the configuration, SPDL RUN → H, $\overline{\text{F}}$/R → H and SPDL error → about −1.5V triggers application of the brake to the SPDL motor.

The system microprocessor CPU detects brake release timing from the FG cycle and shifts SPDL RUN to L and ACC CONT to Hi-Z to release the brake.

When FG is not input to the system microprocessor CPU, SPDL will continue accelerating from the onset as long as ACC CONT is maintained at H. Care should be taken at this point, because, if the OPEN button is pressed, the system microprocessor will judge that the SPDL has stopped, and regardless of whether it is rotating or not, will open the tray. Furthermore, when RF is not being input to PA5010, acceleration will stop at onset if ACC CONT shifts to Hi-Z and $\overline{\text{ACCEL}}$ to H. In this state, ACC CONT repeats H and Hi-Z and the SPDL continues rotating at low speed. (In one minute this state will be rejected.)

2.7. SPDL SERVO LOOP GAIN CONTROL DURING CLV DISC PLAY

A duty pulse with a duty ratio that is variable according to the disc time code is generated in the CPU, smoothed, and utilized for SPDL servo loop gain control.

The duty pulse has a 1V cycle with a sixteen stage variable duty ratio. The signal registers L at the innermost track and H at the outermost track. Providing the signal is smoothed, voltage will continue to rise as the pickup moves toward the outer tracks. This method derives a signal identical to that of obtained by slider resistor voltage and can perform the task of SPDL servo loop gain control during CLV disc play.

2.8. DIFFERENCES IN SPDL/TBC OPERATION DURING CAV AND CLV PLAYBACK

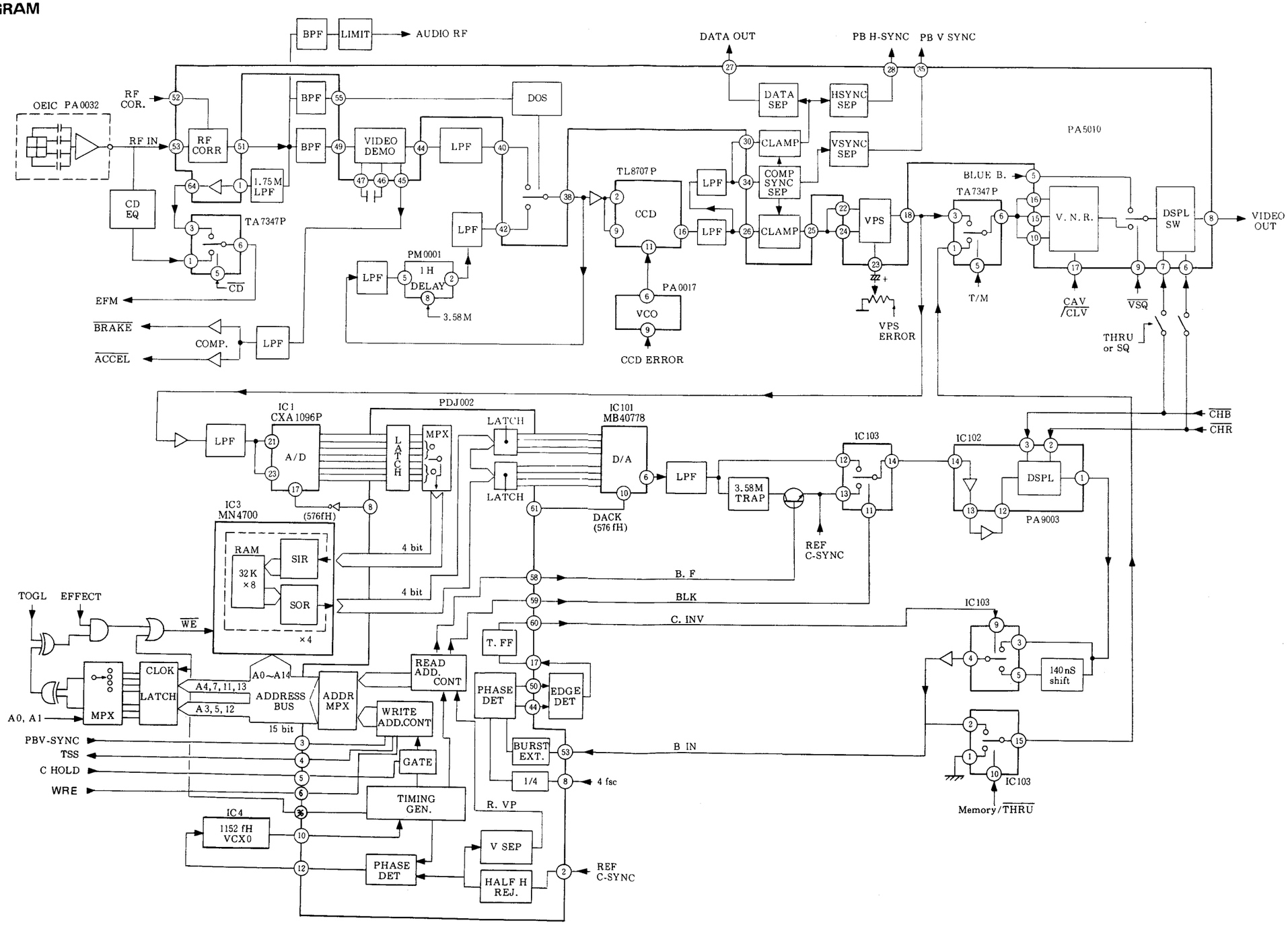
(○ : being output, X : not being output)

	< CAV >	< CLV >
During SCAN		
CLOCK INH	X	○
PLL FAST	○	○
TBCO	X	○
STILL, SLOW etc. (during track jump)		
CLOCK INH	X	○
PLL FAST	○	○
TBCO	X	○
JUMP TOGL	○ (memory-through only)	X

During CAV playback, even if the TRKG servo is open during SCAN, STILL and other operations, since CLOCK INH is not being input to the video memory section, reference shift is not being performed.

3. VIDEO SIGNAL PROCESSING SYSTEM (CLD-3030)

3.1. BLOCK DIAGRAM



3.2. SUMMARY OF VIDEO SIGNAL PROCESSING

The pickup of these models (1988 models) incorporates a unitized IC (PA0032) containing both photodetectors and head amp section. After gain adjustments have been made on the FTSB board, the output of PA0032 is input to the VDEM section of VSOP.

The flow of signals from the VDEM section and the operations of the various segments of the video signal processing circuitry are exactly the same as in the LD players. As can be seen from the block diagram, virtually all the indispensable circuitry is contained in the PA5010.

<PA5010 Functions>

- RF correction
- Video demodulation
- Dropout detection/Video correction SW
- EFM amp
- V-H synch and data separation
- VPS (Video Phase Shifter)
- VNR (Video Noise Reduction)
- Blue background SW and squelch
- Screen display
  (when video memory is OFF or when using blue background screen)

In other sections (for instance, CCD, CCD clock generating VCO IC, 1H delay IC), parts are identical to those used in the LD player.

The flow of signals in the video memory section is almost the same as in the LD-S1, although handling of the screen (character) display video in memory and through-video are two places where the '88 models operate differently.

With video that passes through memory, unless the characters are inserted before the 140nS shift circuit (equivalent to one half the cycle of the sub-carrier) that is used to maintain sub-carrier continuity between frames (every successive frame undergoes phase inversion), only the characters on screen will not be 140nS shifted.

3.3. SIGNAL PROCESSING IN THE VIDEO MEMORY SECTION

3.3.1. Signal Flow

The Video Memory Section is made up of two circuit boards: the ADMC and DAPS.

At the heart of the ADMC circuit board is the 1 M bit D-RAM and RAM control IC. It also includes those circuitry sections before the D/A converter.

The time axis corrected video signal is input to ADMC from the VDEM section of the VSOP board.

The IC1 (CXA1096P) is a parallel comparator type A/D converter and the A/D conversion reference voltage has been set at 26P (VRB pin) and 18P (VRT pin). The video signal level is shifted to coincide with the reference voltage, passed through an LPF (low pass filter) and then input to 21P and 23P. Reference voltage is 0 and -2V, and signals within that range undergo 8-bits A/D conversion.

The A/D conversion clock signal, which is set at 576fH (=9.06M) is input to IC1 — 17P from IC2 (PDJ002) — 80P.

The 8-bits data is divided at IC2 into an upper and lower 4-bits and transmitted in 4-bits form into memory. 1152fH VCXO is comprised of Q9, Q10 and IC4 (TC74HCU-04P) and is controlled at IC2 on the basis of error (output from IC2 — 12P) derived by phase comparison of REF-C-SYNC and memory READ address clock (READ REF-H). If the two signals are not phase locked, REF-C-SYNC insertion position and the D/A converted video signal will not coincide.

Writing to memory is indicated by a WE (WRITE ENABLE) signal from the system control.

A fixed time difference is maintained between write timing and memory readout timing, and the latter is always performed synchronously with REF-C-SYNC. Furthermore, unless a new frame is written to memory, the previous frame will continue to be output.

The DAPS circuit board contains the circuitry that follows D/A conversion. 8-bits data and the 576fH clock signal from IC2 are input to IC101 (MB40778) of DAPS.

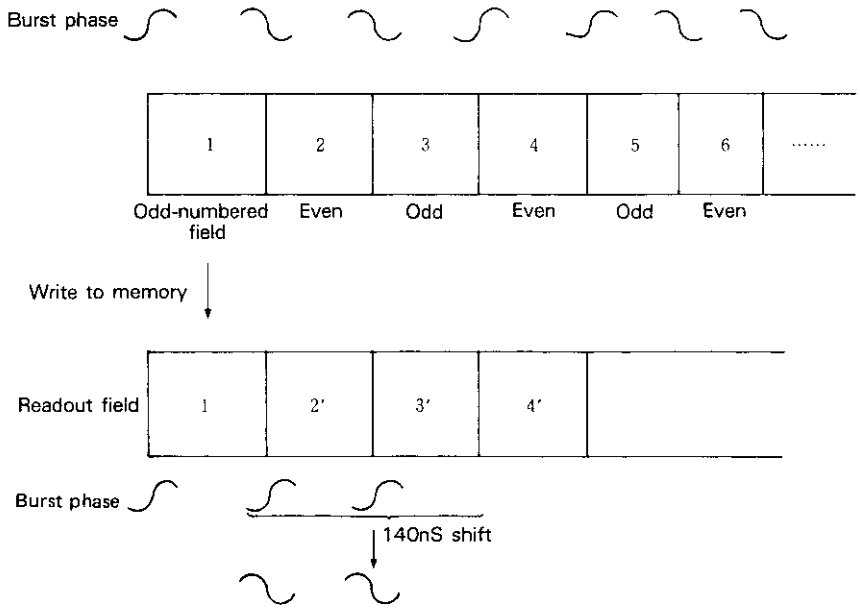
The IC101 D/A converter was also employed in the LD-S1, and the SYNC insertion, DSPL insertion and 140nS shift circuit occurring further downstream in the signal path are virtually identical to those found in the LD-S1 as well.

Insertion of the DSPL signal at DAPS is performed only for memory video. In the memory-through mode DSPL signal insertion is performed at PA5010 in the VDEM section of VSOP.

If DSPL signal insertion is performed in the VDEM section when memory is ON, dislocation occurs between the DSPL display and 140nS due to the fact that the memory video has been passed through the 140nS shift circuit. For this reason DSPL insertion must be performed before 140nS shift.

3.3.2. Necessity of the 140nS Shift

As the figure below shows, the burst phase of the NTSC video signal is reversed for each frame.



If by a still operation as shown above, field No. 1 is written to memory and then continuously read out, the burst phase for every field will become the same. In order to normalize the burst phase, the timing of fields 2' and 3' must be delayed for a period of time equal to one half the periodicity of the burst signal, or 140nS.

By delaying the video signal it is possible to perform an equivalent reversal of burst phase and thereby activate the color lock.

Detection of the discontinuous burst phase is done by comparing the 3.58MHz signal derived by frequency division of the reference clock 4fsc signal input from VSOP at IC2 (PDJ002) of ADMC, with the play burst signal, and then performing edge detection at IC5 and 6. The output of edge detection is the C-TRIG signal. This is input to IC2 — 17P and triggers FF in IC2 to output the C-INC signal from 60P which acts as the 140nS shift circuit control signal.

The C-INV signal is then input to IC103 — 9P of DAPS where switching to activate and deactivate 140nS delay is performed.

3.3.3. RAM Control IC (PDJ002)

The CLD-3030 incorporates the PDJ002 as its RAM control IC. This IC differs from the PD3080 employed in the LD-S1 in the following ways.

< Additional functions not performed by the PD3080 (in VMRB of LD-S1)>

1. V-SYNC separation for REF-C-SYNC, MMV for half H rejection
2. Phase comparator for 1152fH VCXO drive
3. Burst extraction for D/A converted video signal

<Other functions>

1. Control signal generation (WRS, CE, RE) for D-RAM (MN4700)
   Address signal generation (A0 — A14) for D-RAM (MN4700)
2. Clock for D-RAM, A/D converter, D/A converter (SCK, LTCK, DACK)
3. Phase comparator to check burst continuity in the D/A converted video signal
   Two 3.58M signals are derived by frequency dividing the 4fsc signal by 4 and then shifting signal phase by 90°. These signals are then compared with the burst signal and output as P-DET1, 2.

The video memory section is composed of the two circuit boards, ADMC and DAPS.

3.3.4 Writing Data to RAM

Sampling of the video signal is done at 576fH (=9.06M) just as in the LD-S1 with 8-bit quantization. Data recorded in RAM has 512 samples on the H axis and 256 on the V axis which means that RAM capacity required is the same as for the LD-S1, namely:

$8 \times 256 \times 512 = 1048576$ (bits).

In the CLD-3030, one chip of RAM (MN4700) has the capacity to handle this volume of data.

First of all, the 8-bit parallel data from the A/D converter is divided into an upper and lower 4-bits. Because the D-RAM (MN4700) employed in the CLD-3030 has been specifically designed for video memory applications, it has separate 4-bit data buses for write and readout.

As the figures to the right show, data is sent in 4-bit increments, the upper 4-bits first and then the lower 4-bits, to RAM.

Furthermore, the MN4700 is equipped with an 8-bit serial shift register that can realize 8-bits of information for each bit input to the 4-bit data bus.

The 8-bit register is transmitted in sequence and when all 8-bits are assembled they are sent to the memory cell to complete recording to memory.

Because 8-bit serial data processing is being employed, one line of the 4-bit data bus, in fact, yields a total of 32-bits. In other words, one block of data handled by the system is equivalent to 4 samples.

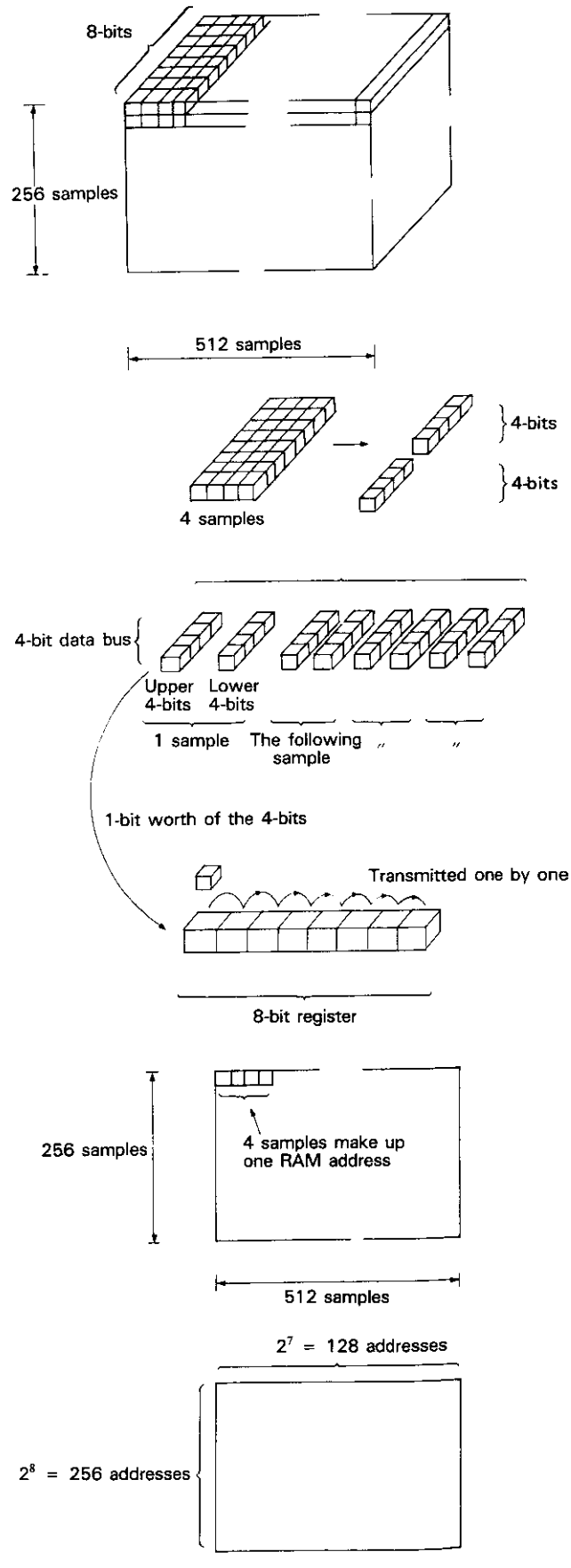
In order to arrange and process 4 samples worth of data (=32 bits) in RAM, one RAM address corresponds to 4 samples worth of data. Consequently, the number of RAM addresses required is:

H axis: $512/4 = 128 = 2^7 = 7$-bits

V axis: $256 = 2^8 = 8$-bits

Total bits required = 15-bits.

Because the MN4700 does not employ the address multiplexing normally found in D-RAM which allows switching between row and column addresses, it inputs the addresses as 15bit data.



<Data Processing in RAM>

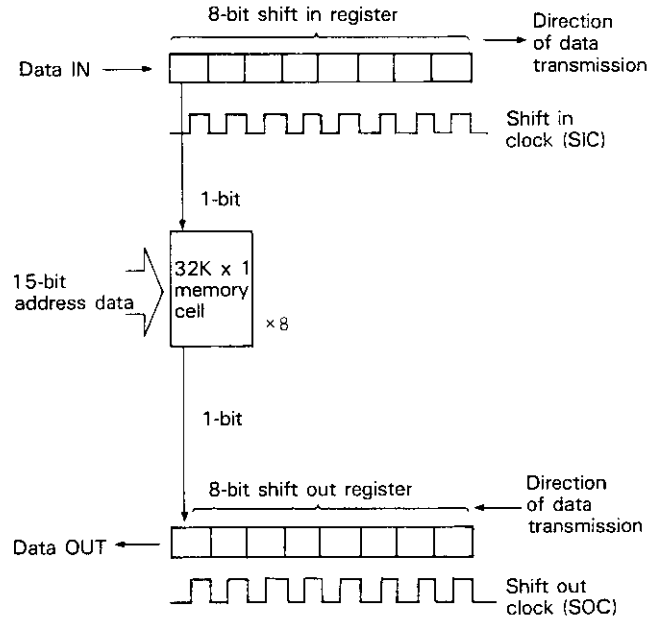
The figure to the right shows one bit worth of data from a 4-bit data bus. Each 8-bit register is connected to a 32K-bit memory cell and in RAM there are a total of 8 × 4 = 32 of these 32K-bit memory cells yielding a memory storage capacity of

32,768 × 32 = 1,048,576.

Because of the need to process the 8-bit data sampled at 576fH in 4-bit units, the frequency of the shift-in, shift-out clock has been set at

576 × 2 = 1152fH (=18.12M).

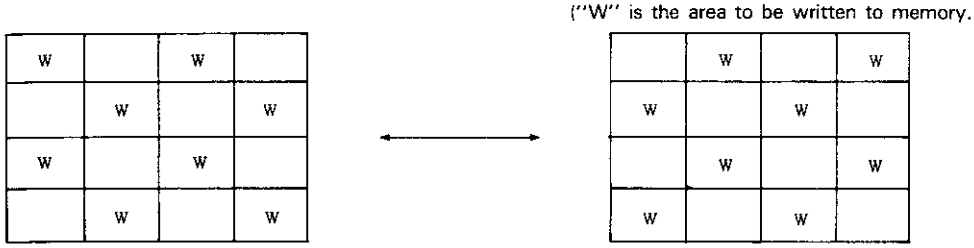
The necessary clock and timing signals needed for the operation of MN4700, as well as data I/O are all input from the RAM control IC, PDJ002.



3.3.5. How Digital Effects Work

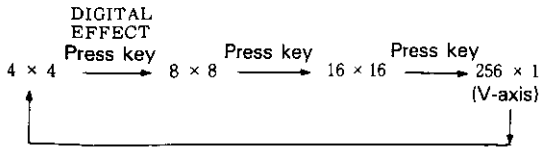
During strobe play, the unit goes into a partitioned screen mode. When the key is pressed once, the following operation occurs "W" is the area to be written to memory).

("W" is the area to be written to memory.)



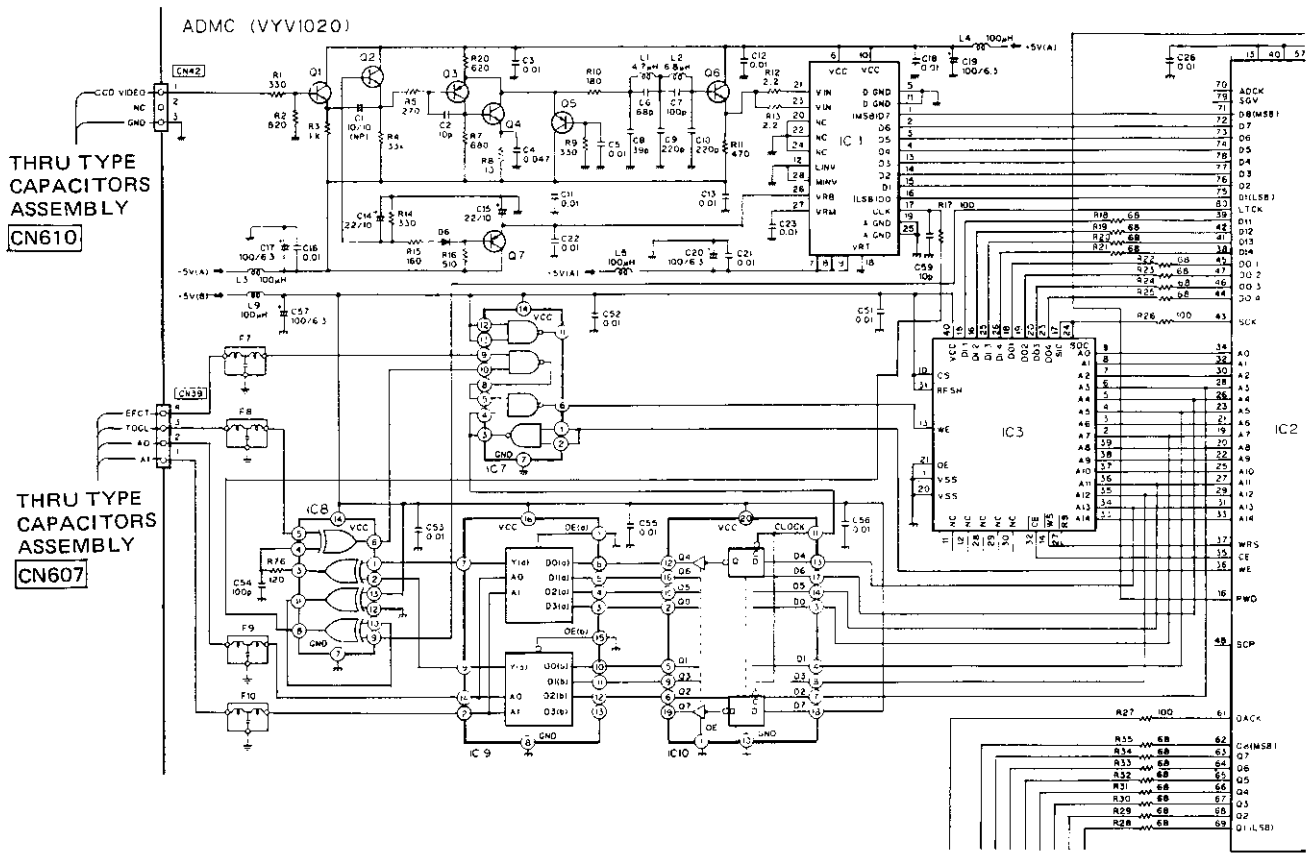
The screen is partitioned into a 4 × 4 Pattern with 16 boxes as shown above. 8 boxes at a time are alternately written to memory. Write speed at this time is the same as for normal strobe play, i.e. set to 1/4 at power ON, and variable with the remote control +, − speed KEY from 1/2 to STEP 3 (from every 2 frames to every 3 seconds).

The result is the special effect achieved on screen by shifting the write speed timing for the neighboring areas. Continuing to press the DIGITAL EFFECT key one or more times, alters the screen by increasing the number of partitions as shown in the figure below.



During these operations, the chroma signal and color burst phase for the neighboring areas must coincide. Since the phase of the burst signal is reversed for each frame, the phase for every other frame will be the same. That's why the DIGITAL EFFECT write speed is limited to integral multiples of 2 and can only be performed during strobe play.

3.3.6. Operation of the DIGITAL EFFECT INTERFACE



IC10 latches WRITE ADDRESS DATA.
When the WE signal of IC3 — 13P is L, the RAM WRITE/READ switch is on WRITE. From IC2 — 36P, the WE signal passes through two NAND gates in IC7 and is input to IC3 (RAM) — 13P and the WE signal which has been inverted once is input to IC10 — 11P (CLOCK pin).

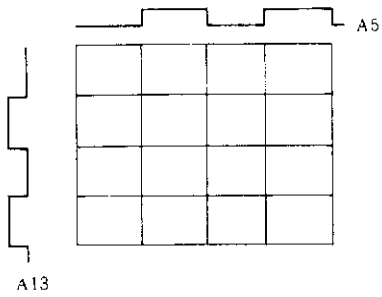
Since IC10 latches input data on the leading edge of the CLOCK pulse and sets the L to H, i.e., READ to WRITE, timing, it can latch WRITE ADDRESS.

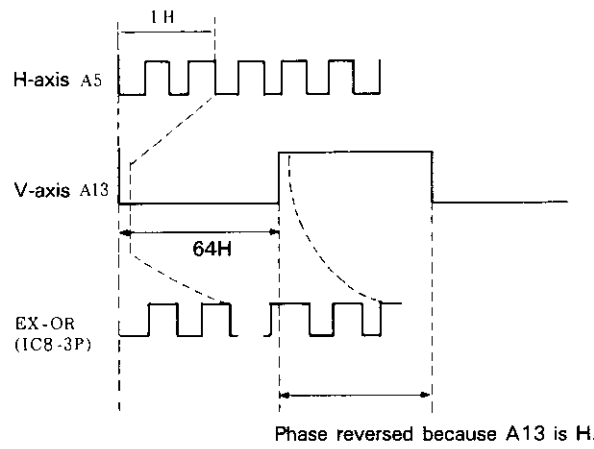
IC9 acts as an address selector for setting the number of screen partitions during DIGITAL EFFECT. Of the four possible choices, the number of screen partitions selected is determined by the A0 and A1 signals generated by the system microprocessor CPU as follows.

A0	A1	Selected address	Number of screen partitions
L	L	A5 A13	4 x 4
H	L	A4 A12	8 x 8
L	H	A3 A11	16 x 16
H	H	A7	256 x 1

Next, two addresses are input to EX-OR. This takes the data from the partitioned screen and writes it in alternating form to memory and, depending on whether the V axis address data is L or H, reverses the H axis address data. The next EX-OR has a switching function. On the basis of the TOGL signal generated by the system microprocessor CPU, it does or does not perform inversion one more time.

The 4 x Partitioned screen is taken as an example here.





Phase reversed because A13 is H.

Then the output of IC8 — 3P is input again to EX-OR.

When the TOGL signal generated by the system microprocessor CPU and input to the second EX-OR is L, polarity remains unchanged and the video signal is output from 6P as is. On the other hand, if TOGL is H, the signal is inverted and then output from 6P.

If IC7 — 9P is H when DIGITAL EFFECT is ON, the output of IC8 — 6P is inverted before being input to the NAND gate.

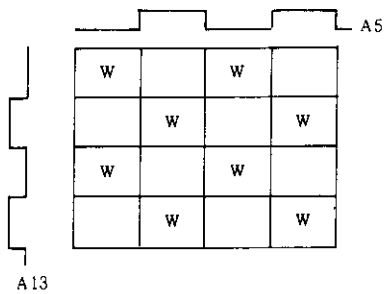
Another input to the NAND gate is the inverted WE signal from the RAM control IC (IC2). This allows WE to be controlled by the output of IC8 — 6P. In other words:

When IC8 — 6P is L: The WE signal from IC2 is input to IC3 (D-RAM) — 13p, WE pin.
WRITE to memory is performed.

When IC8 — 6P is H: The WE signal from IC2 is not input to IC3 - 13P and because it is H, nothing will be written to memory.

Furthermore, as the figure below shows, the L or H of TOGL indicates which areas (shown by W) of the screen are to be written to memory.

TOGL:L



W		W	
	W		W
W		W	
	W		W

TOGL:H

	W		W
W		W	
	W		W
W		W	

4. DIGITAL AUDIO CIRCUITRY

4.1 SUMMARY

The 4FSB circuit board receives the EFM signal from the VDEM section of the VSOP Assembly and performs the necessary signal processing. The principle IC for this purpose is the CXD1135Q, which has the following functions:

1. Generation of the bit clock (PLCK: 4.3218M) by EFM-PLL
2. EFM signal demodulation, correction and interpolation
3. Frame synch signal detection, protection and interpolation
4. Subcode signal demodulation and error detection
5. SPDL servo (obligatory deceleration/acceleration, brake, speed servo, phase servo)
6. Zero cross counter for 8-bit tracking error (not found in these models)
7. Double oversampling digital filter (35-stages)
8. Digital audio interphase output

The functions listed in 1 — 6 are essentially those handled by the CX23035 found in previous models. Both the CXD1135Q and the CX23035 receive commands from the system microprocessor in the form of 8-bit serial command data and, in terms of the CX23035 commands, the CXD1135Q is upward compatible.

4.2 CXD1135Q COMMAND CODE

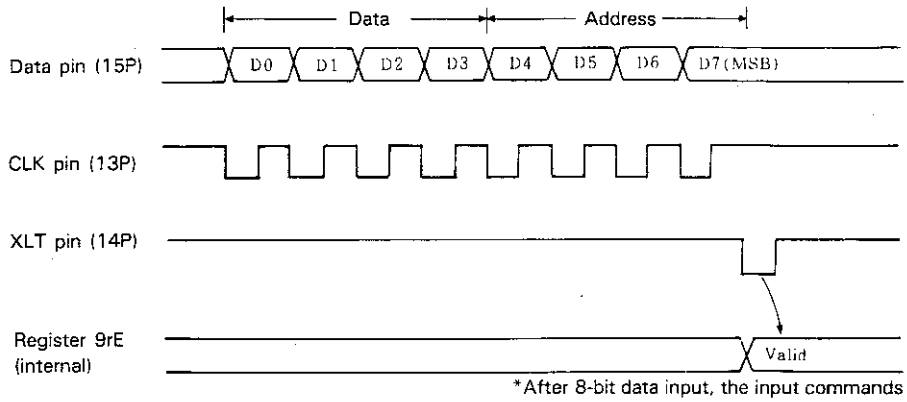
As the table below shows, CXD1135Q has a 4-bit register containing addresses 9 through E. Player operations can be performed by sending 8-bit data (command code) containing address and data (totalling 8-bits) to these addresses.

<Register Chart>

Register Name	Command	Addresses D7 – D4	Data				SENS pin (18P)
			D3	D2	D1	D0	
9	Control of new functions	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A	Synch protection, attenuation control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Lower 4-bits	1011	Tc3	Tc2	Tc1	Tc0	COMPLETE
C	Counter set, Upper 4-bits	1100	Tc7	Tc6	Tc5	Tc4	COUNT
D	CLV control	1101	DIV	Tz	Tp	GAIN	Z
E	CLV mode	1100		CLV mode			Pw≧64

* The B.C register is for tracking error zero cross count and is not employed in the 1988 models.

<Data Input Timing Chart>



*After 8-bit data input, the input commands are executed during the time period when XLT is L. Data input timing is the same as in the CXA1082A.

«Information about the Registers»

• Register 9

Register 9 handles the commands for new functions not found in the previously employed CX23035. Registers A through E, however, are essentially the same as in the CX23035.

		Dn = 0	Dn = 1
ZCMT	D3	Zero cross MUTE OFF	Zero cross MUTE ON
HZPD	D2	The PDO pin is always active	The PDO pin is Z at the trailing edge of GFS
NCLV	D1	CLV-P servo supported by frame synch signal	CLV-P servo supported by base count
CRCQ	D0	CRCF is not superimposed on SUBQ	At the leading edge of SCOR, SUBQ = CRCF
		(Functions identical to those of the CX23035)	(New functions)

ZCMT: Turns zero cross MUTE ON/OFF.

HZPD: Switches PD output to Hi-Z (ON/OFF) from the trailing edge of the GFS pulse (GFS is H when SPDL LOCK is activated) to a maximum of 0.55nS. (PLCK and play EFM undergo phase comparison, and the PD output controls the VCO.)

NCLV: Switches the SPDL phase servo error detection method when PLL is locked.

CRCQ: Switches the output of CRCF data from the subcode data Qoutput pin, SUBQ, ON/OFF.

If the content of Register 9 is cancelled out by activating POWER ON RESET and none of its commands are active, the IC will function exactly like the CX23035.

• Register A

Controls the 4 signals: GSEM, GSEL, WSEL, ATTM.

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

When frame synch detection is not working properly, a dummy frame synch is interpolated, but the number of frames for which interpolation will be performed is fixed: during LD play, 8 frames; during CD play (CLD-3030, CLD-1030) 8 frames; and during SCAN, 13 frames.

WSEL	Clock
0	± 3
1	± 7

To prevent errors during frame synch detection, a detection window of a certain width is set and synch patterns which fall outside the detection window are ignored. The width of the detection window is set as follows: (set at ± 7 clock)

ATTM	MUTG pin	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

In combination with the MUTG pin (19P), MUTE ON/OFF and the application of -12dB attenuation can be controlled.

In terms of actual command code, $AA is being input. Since A = 1010 and GSEL = 1, GSEL = 0, there are 8 interpolation frames with detection width parameter set at 7 clock.

• **Register D**

DIV	D3	0	RFCK/4 and WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 and WFCK/8	
TB	D2	0	RFCK/32	Bottom hold cycles in CLV-S, CLV-H modes
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold cycle in CLV-S mode
		0	RFCK/2	
GAIN	D0	0	− 12dB	MDP pin gain in CLV-S, CLV-H modes
		1	0dB	

RFCK: Read Frame Clock (frequency divided from X'TAL, 7.35k)

WFCK: Write Frame Clock (Frame synch during play EFM)

CLV-P mode: Phase servo which operates when the PLL loop is locked

CLV-S mode: Speed servo which operates when the PLL loop is not locked

CLV-H mode: Speed servo during search (when pickup is moving)

In terms of actual command code, $D4 is being input. Since 4 = 0100, RFCK, WFCK are frequency divided by 4 for phase error, RFCK is frequency divided by 16 for bottom hold in the CLV-S mode, RFCK is frequency divided by 4 for peak hold and MDP pin gain is − 12dB.

• **Register E**

		(3P)	(4P)	(1P)	(2P)
Mode	**D3−D0**	**MDP pin**	**MDS pin**	**FSW pin**	**MON pin**
STOP	1000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	Z	L	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H
CLV-A'	0101	CLV-S' or CLV-P	Z or CLV-P	L or Z	H

This register sets the operating mode for the SPDL servo. In this mode, the SENS pin, 19P, registers L when the frame sync pulse amplitude detected at CLV-S is over 64T. This output, however, is not utilized.

From commands 0000 to 0110, the system is identical to that of the CX23035.

After the focus servo lock check, actual SPDL start is performed by $E8, i.e., command code 1000 puts the unit into KICK mode which force starts the SPDL. Next, $E6 puts the unit into CLV-A mode which closes the SPDL servo and PLL loop. The lock can be checked by verifying that GFS registers an H.

When stopping, $EA, command code 1010, applies the brake, and after SPDL stop detection at FG, $EO puts the unit into stop mode. Because the CD-3030 has a 4-times oversampling digital filter IC (SM5807B), the digital filter in the CXD1135Q is not utilized.

As a digital OUT terminal, the toss link for optical fiber transmission (identical to that of the D-1000) is passed through a buffer and connected to 27P. However, since the function assigned to MODE 0 of the digital OUT IC, CX23033, employed in the D-1000 is built into the CXD1135Q, 27P is no longer needed for this purpose. Instead, modulated output for the digital audio interface format is obtained from 27P.

ON/OFF for digital filter and OUT functions can be fixed according to the H and L signals from MD1, 2 and 3 of 55, 56 and 57P. On the CD-3030 these are set at L, L, H corresponding to digital, OFF and digital OUT, ON.

4.3. SIGNAL PROCESSING AND CXD1135Q PERIPHERAL CIRCUITRY

The EFM signal from the VDEM section of the VSOP Assembly passes through the ATC circuit made up of IC101 (TC40H004P) and IC102 (1/2) (NJM082D) and is input to IC104 — 5P (CXD1135Q). The result of phase comparison between EFM and the VCO output of IC102 (2/2) is output from IC104 — 11P. A PLL loop is used to control a VCO.

IC104 performs SPDL servo error detection from EFM and the output of 1 through 4P is utilized for the SPDL servo. The function of the pins is as follows:

FSW (1P): When the PLL loop is locked, it is Hi-Z. At other times it is L.
IC103 (2/2) (NJM082S) is the phase and speed error mix filter, and is used to switch the cut-off frequency. (Hi-Z, 500Hz, L: 20Hz).

MON (2P): When the motor is stopped: L, when rotating: H.

MDP (3P): SPDL phase error when PLL is locked and otherwise, speed error

MDS (4P): Speed error when PLL is locked and, otherwise, Hi-Z

Internal detection of whether PLL is locked or not, is performed at the GFS pin, 28P, which registers H when PLL is locked.

During CD play or the audio section of a CDV, the error signal of IC103 — 8P is input as CD ERR to the absolute value amp for the SPDL servo section from IC501 — 15P (NJU4053BD) and drives the SPDL motor.

During LDD play or the video section of a CDV, a 384fs (=16.9344M) VCXO is input IC501 — 4P to control VCXO. As a clock signal, VCXO is input to IC104 and IC201 (SM5807B). At IC104 the demodulated digital audio data is input as serial data to IC201 along with LRCK (44.1k) and C210 (2.1168M).

IC201 is a 61-stage + 13-stage 4-times oversampling digital filter.

The CLD-3030 utilizes a sub-CPU, IC106 (PDE0234), to handle the transmission of 8-bit serial command data to IC104 (CXD1135Q) and the reception of sub-code data from IC104.

IC106 is connected to the main CPU by the 4-bit data bus and by the signal lines ATN, STB and ACK. PD0031 and PDG012 are also connected to the data bus.

The CLD-1010 does not use a CPU. Instead the decoder ICs (CX23035, CXD1135Q) are controlled directly from the main CPU and data I/O is performed.

In previous models, the only operation using sub-code data during LDD play was the Emphasis ON/OFF check. This helped keep processing time short and allowed the main CPU to directly read data.

However, with the introduction of TOC (ADR = 4) in LDD discs, the reading of the TOC renders processing time too long and it is no longer practical for the main CPU to directly read the data.

For this reason, sub-code data from CXD1135Q is placed in a buffer at IC106 (PDE024) and, in response to a command from the main CPU, is transmitted by 4-bit bus. In addition, command code destined for CXD1135Q is input through IC106.

On the basis of data received from CXD1135Q and the main CPU, IC106 performs digital/analog switching, LD/CD switching and Emphasis ON/OFF.

Another function of IC106 is to output LSEL and RSEL signals used for switching left/right channels during LDD play:

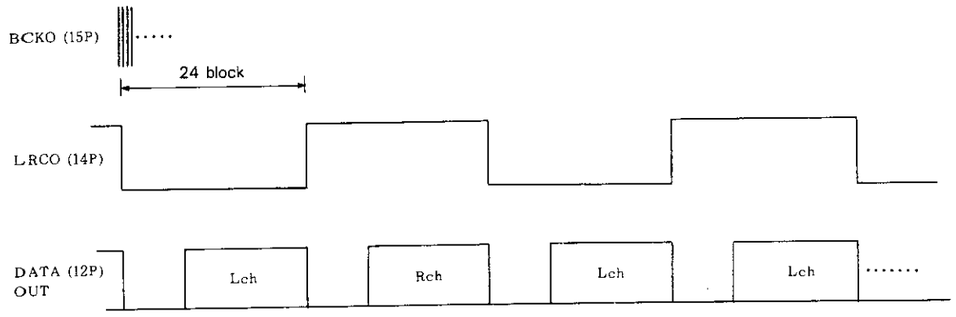
	Both CH	RCH only	LCH only
LSEL	L	L	H
RSEL	L	H	L

As the figure on the facing pages shows, Lch, Rch data is output in alternating form from IC201 (SM5807B). L/R switching during LDD play and L-R, same phase D/A conversion during normal play are performed at IC202, 203 and 204. (L.R. same phase conversion is performed at PD-7070.)

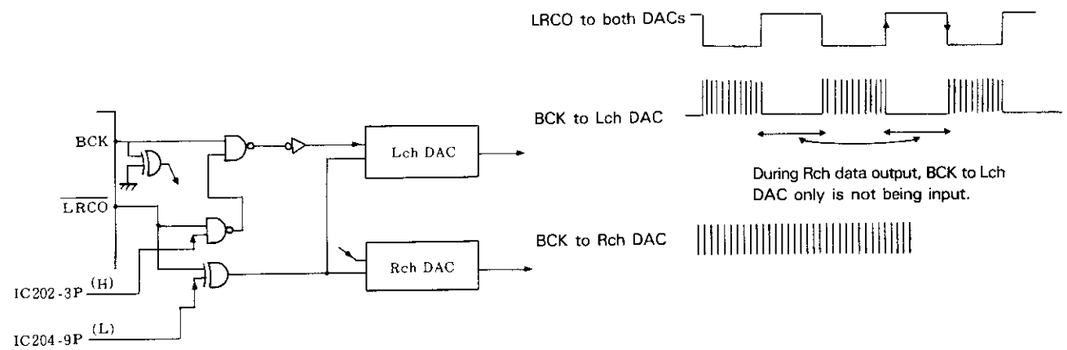
Next, the timing for L/R switching is shown.

4.4. THE L/R SWITCHING SYSTEM FOR DIGITAL AUDIO

IC201 (SM5807) Output



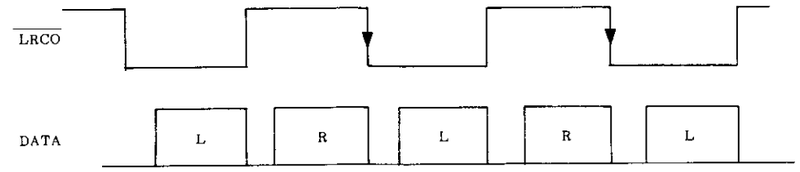
① When both L,R are output (LSEL = L, RSEL = L)



In this mode, LRCO is H for the Lch DAC and DATA BCK, which means that input to DAC is halted while Rch data is being output. Since both DACs are latching and outputting data on the trailing edge of LRCO, L and R are being output simultaneously on the trailing edge of LRCO.

② Rch only output (RSEL only = H)

When RSEL is H, IC204 — 5P also outputs an H. Since IC204 — 9P is L, IC203 — 11P becomes H and IC202 — 3P becomes L. As a result, IC202 — 11P becomes H and BCK to the Lch DAC is not gated to LRCO but continues being input.

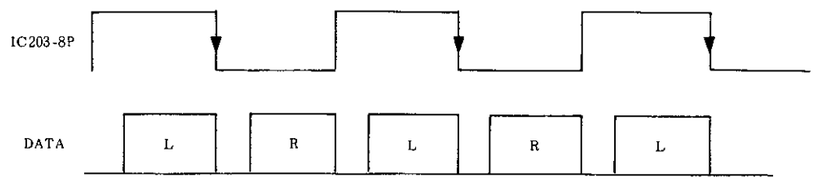


Because IC204 — 9P is L, LRCO is input to both DACs without undergoing phase reversal.

Consequently, since both DACs are latching data on the trailing edge of LRCO, only Rch data is being output by the DACs.

③ Lch only output (LSEL only = H)

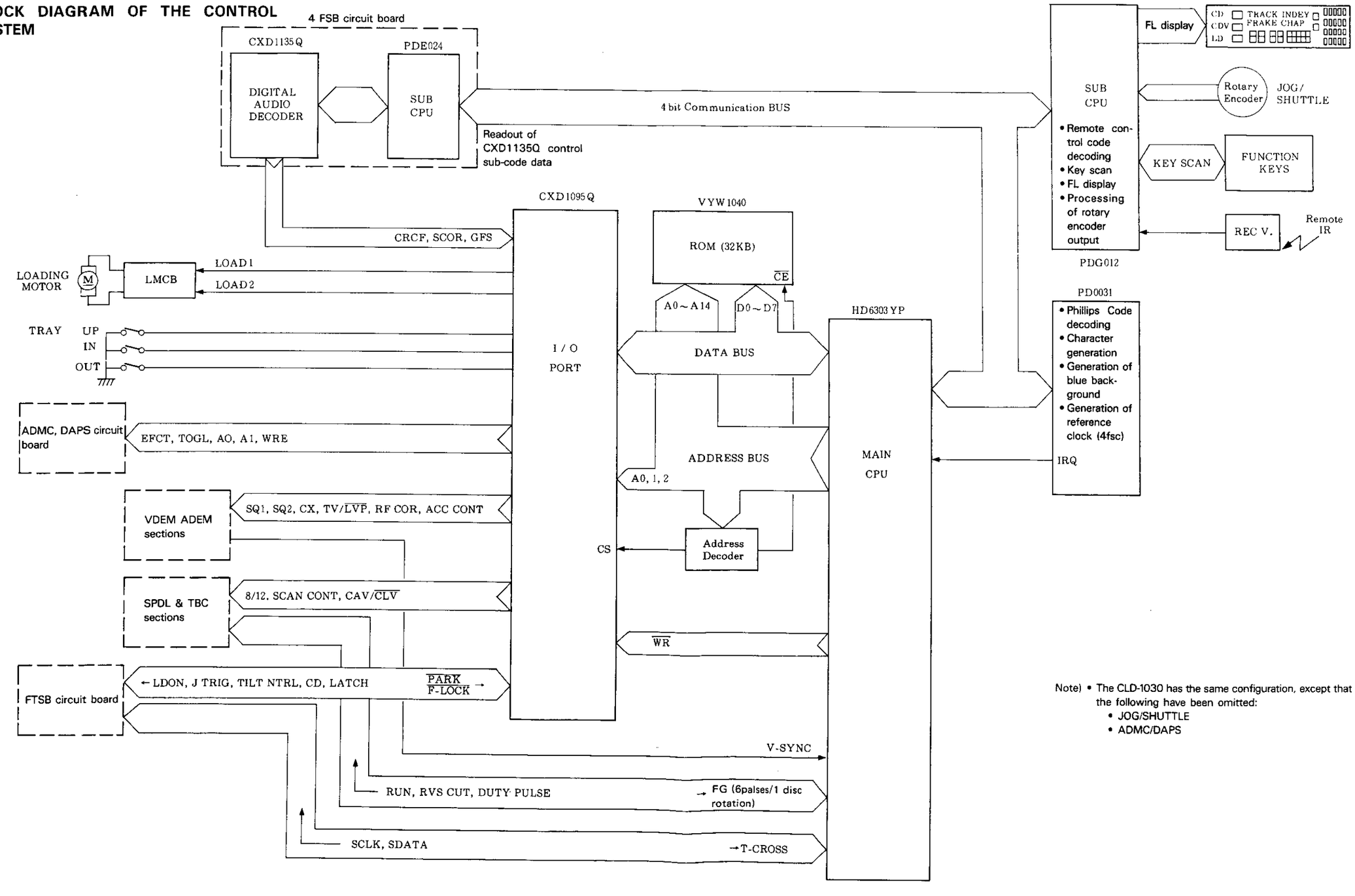
When LSEL is H, IC204 — 9P also outputs an H which inverts the LRCO for both DACs. Since IC204 — 5P is L, IC202 — 11P becomes H and the BCK to the Lch DAC is not gated.



Consequently, since both DACs are simultaneously latching Lch data, Lch audio is output from both DACs. DAC output then passes through the 3-stage LPFs, IC207, 208.

5. EXPLANATION OF SOFTWARE USED IN THE SYSTEM MICROPROCESSOR

5.1. BLOCK DIAGRAM OF THE CONTROL SYSTEM



Note) • The CLD-1030 has the same configuration, except that the following have been omitted:
- JOG/SHUTTLE
- ADMC/DAPS

5.2. THE ICS IN THE CONTROL SYSTEM

HD6303Y: is an externally connected ROM-type 8-bit CPU and operates on the basis of the program written to the externally connected ROM.

PDG012: is a 4-bit CPU which performs JOG/SHUTTLE decoding, main unit key decoding, remote control key decoding and maintains FL, LED displays on the main unit.

PDE024: is a 4-bit CPU which performs LDD control. It performs sub-code decoding and controls CXD1135Q.

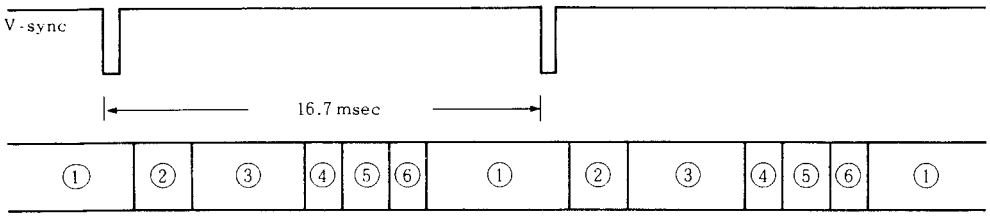
CXD1095Q: is an enlarged I/O port IC connected to HD6303Y of the main CPU.

MBM27C256: ROM (32k) contains the program for HD6303Y.

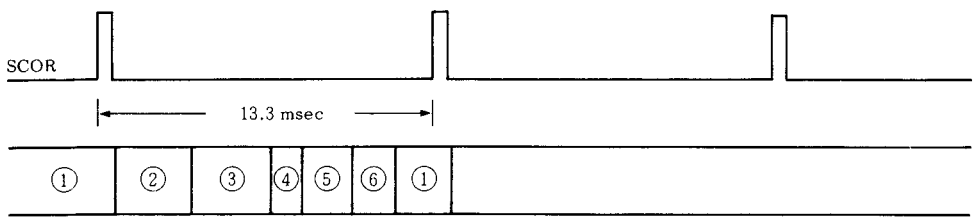
5.3 SUMMARY

The main CPU, HD6303Y, reads code, handles displays and key information and performs all control functions, including servo control, loading, etc. The processing routine is arranged in a loop with time division for processing handled by an internal timer and play synch signal. When the unit is in the LD mode, the internal timer is set to 20msec and, if the play V-synch signal doesn't intervene, the signal covers the loop in a period of 20msec. When time division is applied from the play V-synch signal, the internal timer is reset and the period for covering the loop is equal to the V-synch period of 16.7msec.

When the unit is in the CD mode, the internal timer is set to 20msec and, if sub-code data doesn't intervene, the signal covers the loop in a period of 20msec. If subcode data is applied, timing is reset and the period for covering the loop is equal to the SCOR period of 13.3msec.

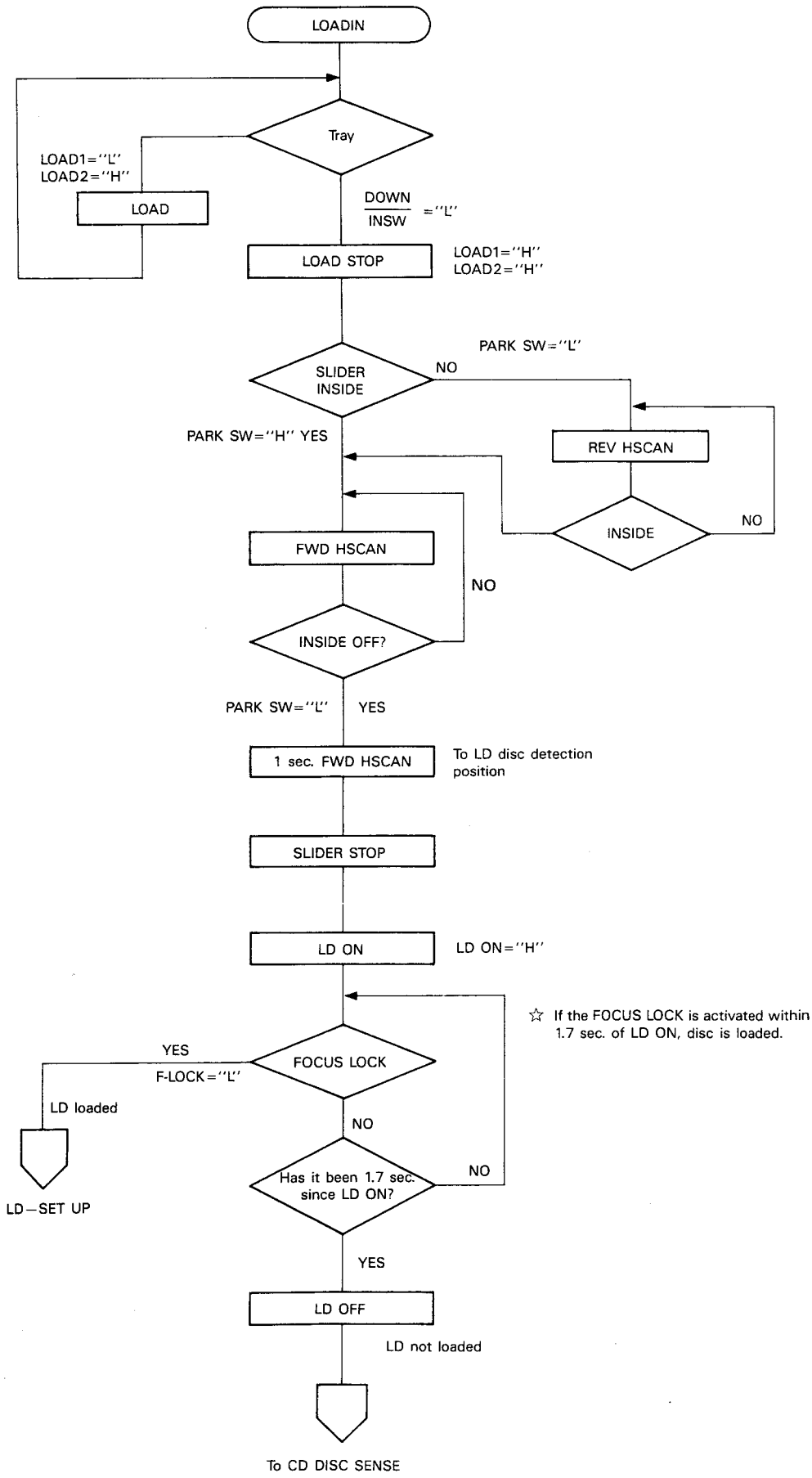


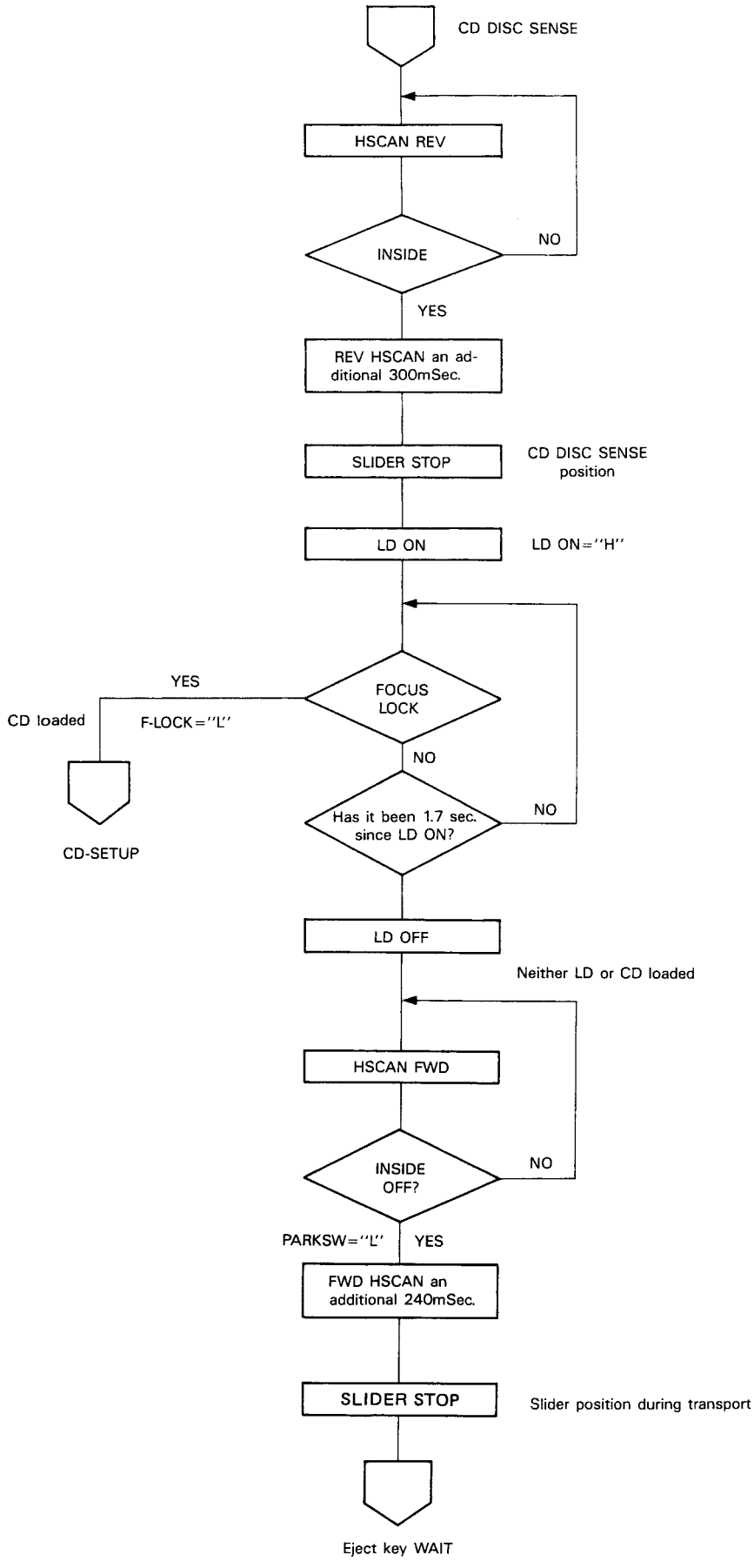
① V-sync WAIT and jump control
② Code readout
③ Display control
④ Key readout and processing
⑤ Servo and mechanical control
⑥ Backup, audio control

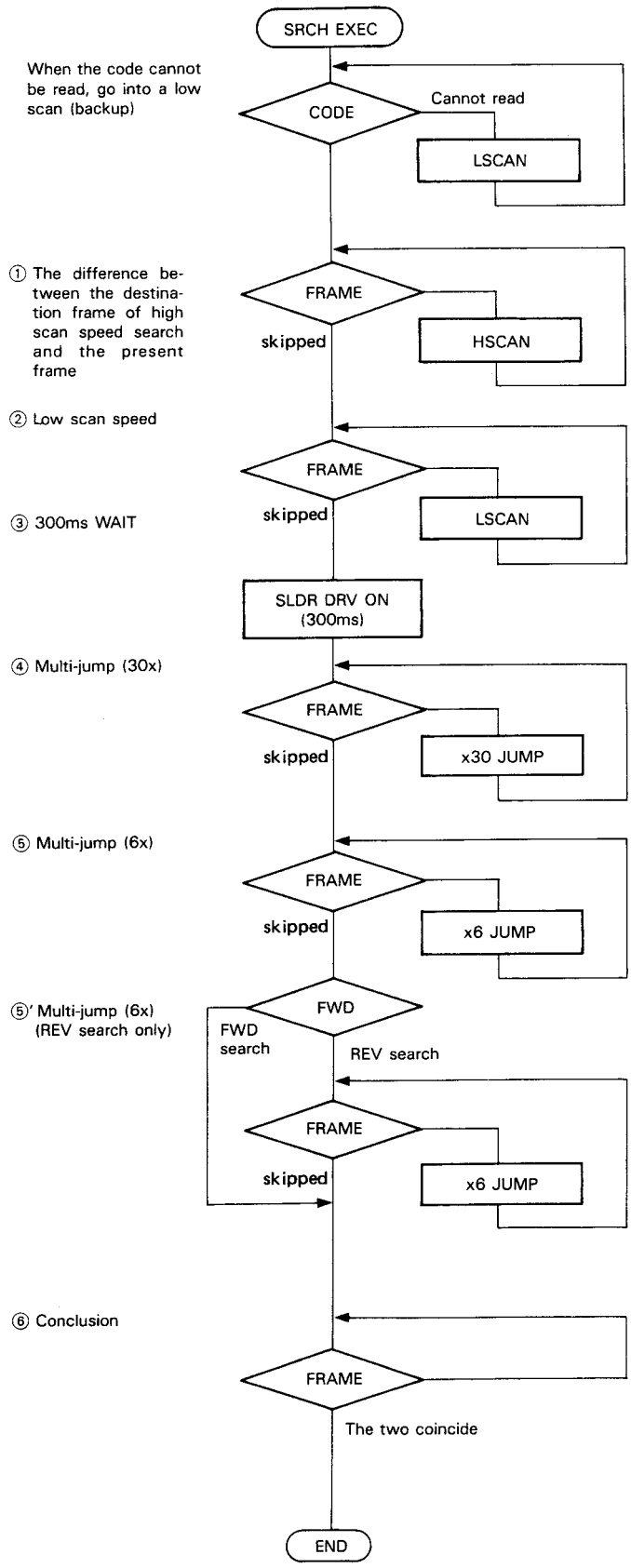


① Sync WAIT
② Subcode readout
③ Display control
④ Key readout and processing
⑤ Servo and mechanical control
⑥ Backup

Fig. 5-3-1. Control Summary Timing Chart


LOADIN
Tray
LOAD1="L"
LOAD2="H"
LOAD
DOWN / INSW ="L"
LOAD STOP
LOAD1="H"
LOAD2="H"
PARK SW="L"
SLIDER INSIDE
NO
PARK SW="H" YES
REV HSCAN
INSIDE
NO
FWD HSCAN
NO
INSIDE OFF?
PARK SW="L"
YES
1 sec. FWD HSCAN
To LD disc detection position
SLIDER STOP
LD ON
LD ON="H"
☆ If the FOCUS LOCK is activated within 1.7 sec. of LD ON, disc is loaded.
YES
F-LOCK="L"
FOCUS LOCK
LD loaded
NO
Has it been 1.7 sec. since LD ON?
NO
LD—SET UP
YES
LD OFF
LD not loaded
To CD DISC SENSE


CD DISC SENSE
HSCAN REV
INSIDE
NO
YES
REV HSCAN an additional 300mSec.
SLIDER STOP
CD DISC SENSE position
LD ON
LD ON="H"
YES
CD loaded
F-LOCK="L"
FOCUS LOCK
NO
Has it been 1.7 sec. since LD ON?
NO
CD-SETUP
LD OFF
Neither LD or CD loaded
HSCAN FWD
INSIDE OFF?
NO
PARKSW="L"
YES
FWD HSCAN an additional 240mSec.
SLIDER STOP
Slider position during transport
Eject key WAIT


SRCH EXEC
When the code cannot be read, go into a low scan (backup)
CODE
Cannot read
LSCAN
① The difference between the destination frame of high scan speed search and the present frame
FRAME
skipped
HSCAN
② Low scan speed
FRAME
③ 300ms WAIT
skipped
LSCAN
SLDR DRV ON (300ms)
④ Multi-jump (30x)
FRAME
skipped
x30 JUMP
⑤ Multi-jump (6x)
FRAME
skipped
x6 JUMP
⑤' Multi-jump (6x) (REV search only)
FWD
FWD search
REV search
FRAME
skipped
x6 JUMP
⑥ Conclusion
FRAME
The two coincide
END

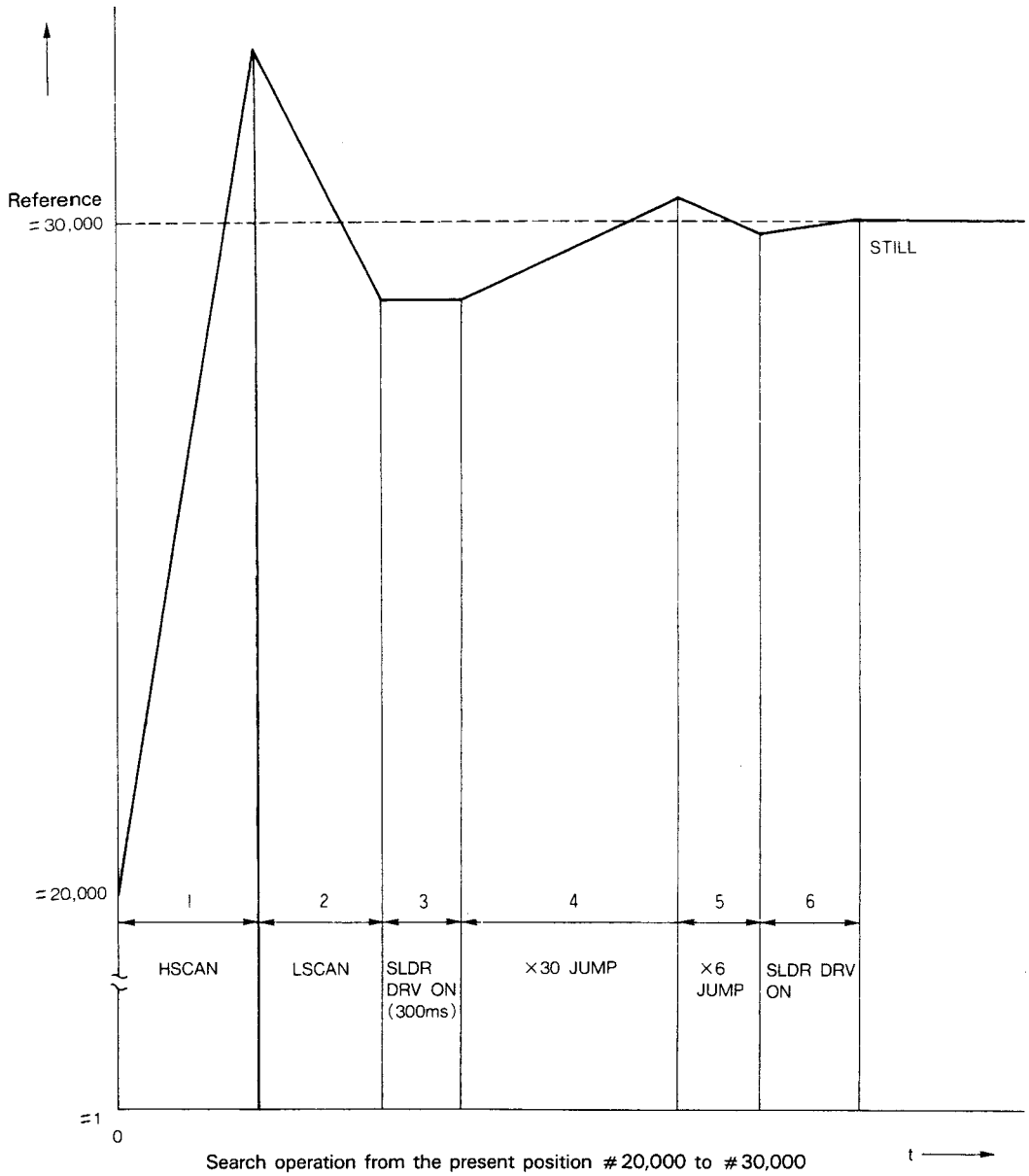


Fig. 5-3. Frame Search Operation

5.4. THE CONDEPT BEHIND SPECIAL PLAY OPERATIONS

An explanation of the basic concepts behind the special play operations incorporated in the CLV disc.

5.4.1. STILL Operation

When the STILL key is pressed, the disc rotates twice and the operation is complete.

Based on the spindle motor derived FG signal which registers disc rotations, the CPU counts Pulses of the FG signal (1 rotation = Pulses) to determine that the disc has made a half rotation, and then the CPU converts the signal to the ROTATION (ROT) signal.

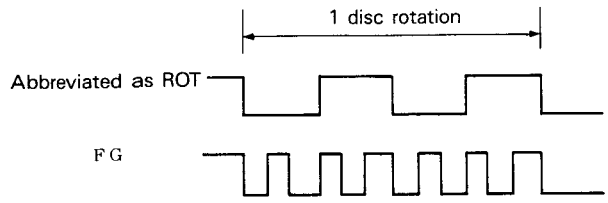


Fig. 5-4-1.

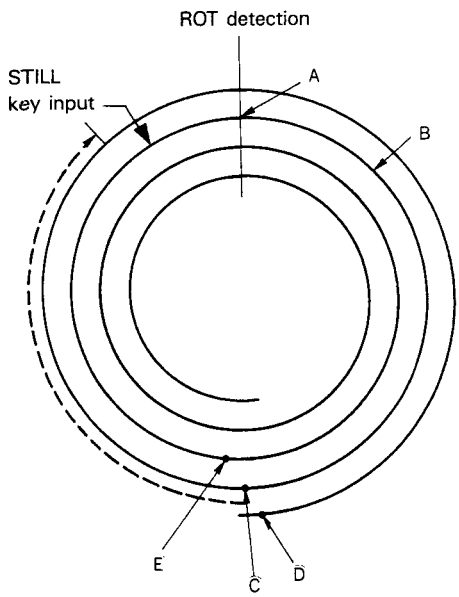


Fig. 5-4-2.

1. The STILL key is pressed.
2. When the ROT signal is detected at point A , the CPU puts V-SYNCH on INPUT WAIT.
3. At point B V-SYNCH is detected but the CPU is still waiting with the next V-SYNCH input.
4. When V-SYNCH is input at point C , the CPU immediately outputs a WRITE ENABLE signal to video memory and from point C one frame worth of signal is input to memory (indicated by the dotted line that begins at point C).
5. The disc then makes a single rotation and after V-SYNCH detection at point D and readout of Philips code are performed, a two track reverse jump is made (interval of 1msec) to point E .
6. Return to Step 2 above and repeat the operation.

This explains, then, in brief, how the STILL operation is completed in the interval of two disc rotations.

5.4.2. STEP Operation

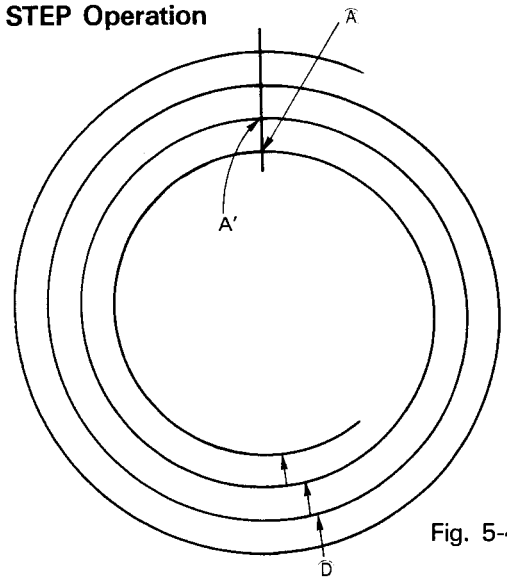


Fig. 5-4-3.

As Fig. 5-4-3 shows, in the STILL mode described above, the two track reverse jump from point D and the return to point A are repeated. At that point however, if a one track reverse jump only is performed from point D , the pickup is one track later or further out from point A on the ROT detection spot at a point we call A '.

If a normal STILL operation is then performed from point A ', the field that is written to memory will be slightly different from the first field. This maneuver is what makes the STEP FWD operation possible.

Conversely, if a three track reverse jump is made from point D this will put the pickup one track earlier than the first field written to memory and during playback there will be a STEP REV effect.