DEPARTMENT OF THE ARMY TECHNICAL MANUAL — TM 11-6625-218-35

DEPARTMENT OF THE AIR FORCE TECHNICAL ORDER — TO 33A1-5-73-2

FIELD AND DEPOT MAINTENANCE

FREQUENCY METER AN/TSM-16

DEPARTMENTS OF THE ARMY AND THE AIR FORCE

JANUARY 1960

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on the 220-volt plate and power supply circuits, or on the 115/230-volt ac line connections. Serious injury or death may result from contact with these points.

DON'T TAKE CHANCES!

TECHNICAL MANUAL No. 11-6625-218-35
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DEPARTMENTS OF THE ARMY AND THE AIR FORCE
WASHINGTON 25, D. C., *8 January 1960*

FREQUENCY METER AN/TSM-16

CHAPTER 1

THEORY

Section I. BLOCK DIAGRAM

1. Scope

a. This manual covers field and depot maintenance for Frequency Meter AN/TSM–16. It includes instructions appropriate to fourth and fifth echelons for troubleshooting, testing, and repairing the equipment, and for replacing maintenance parts. It also lists tools, materials, and test equipment for fourth and fifth echelon maintenance. Detailed functions of the equipment are covered in the theory section.

b. The complete technical manual for this equipment includes one other publication, TM 11–6625–218–12.

c. Forward comments concerning this manual to the Commanding Officer, U. S. Army Signal Publications Agency, Fort Monmouth, N. J.

d. For applicable forms and records, see paragraph 2, TM 11–6625–218–12.

2. Basic Signal Path, Block Diagram (fig. 1)

Frequency Meter AN/TSM–16 is a high-speed electronic counter used to test and measure the generated frequency of carrier telephone, telegraph, teletypewriter, and similar equipment. It will automatically count and display, in numerical form, any number of events (from 20 to 1,000,000 per second) which can be coupled to it as voltage changes. The equipment can also be used to measure the time interval which has elapsed between the time of application of two distinct externally applied *start* and *stop* pulses. Basic signal paths for counter operation are shown in the simplified signal path block diagram (fig. 1). The frequency meter consists of seven basic functional sections, as described below.

a. Input Trigger Channel. When the equipment is used to count the frequency of externally applied signals, the input trigger channel receives the applied signal and modifies its waveform into a series of positive and negative output pulses, corresponding in frequency to that of the applied signal.

b. Clock Pulse Generator.

(1) The clock pulse generator provides timing pulses at intervals of 0.0001, 0.001, 0.01, 0.1, 1, or 10 seconds. These timing intervals control the opening and closing of the gate, and permit incoming signals to be counted for accurate intervals of time.

(2) In addition, when the equipment is set up for self-checking or for making time-interval measurements, the externally applied signal is disconnected from the input trigger channel. The output of the clock pulse generator, operating at its fundamental frequency of 100 kilocycles (kc), is coupled to the input trigger channel. With front panel controls properly set, the numerical readout will show a count of 100,000 cycles in 1 second, indicating proper operation of the equipment. See paragraph 4 for theory of time-interval measurements.

c. Gate Circuit. Another output of the input trigger channel is coupled to the gate circuit. The gate circuit also receives the start and stop pulses from the clock pulse generator. In the absence of a starting pulse, the gate stage within the gate circuit is blocked, and no input pulses are coupled to the remainder of the circuitry. When a starting pulse is applied, the gate circuit is opened for a period of time determined by the setting of a front panel switch, and the gate circuit passes the input pulses to the counters and numerical indicator tubes.

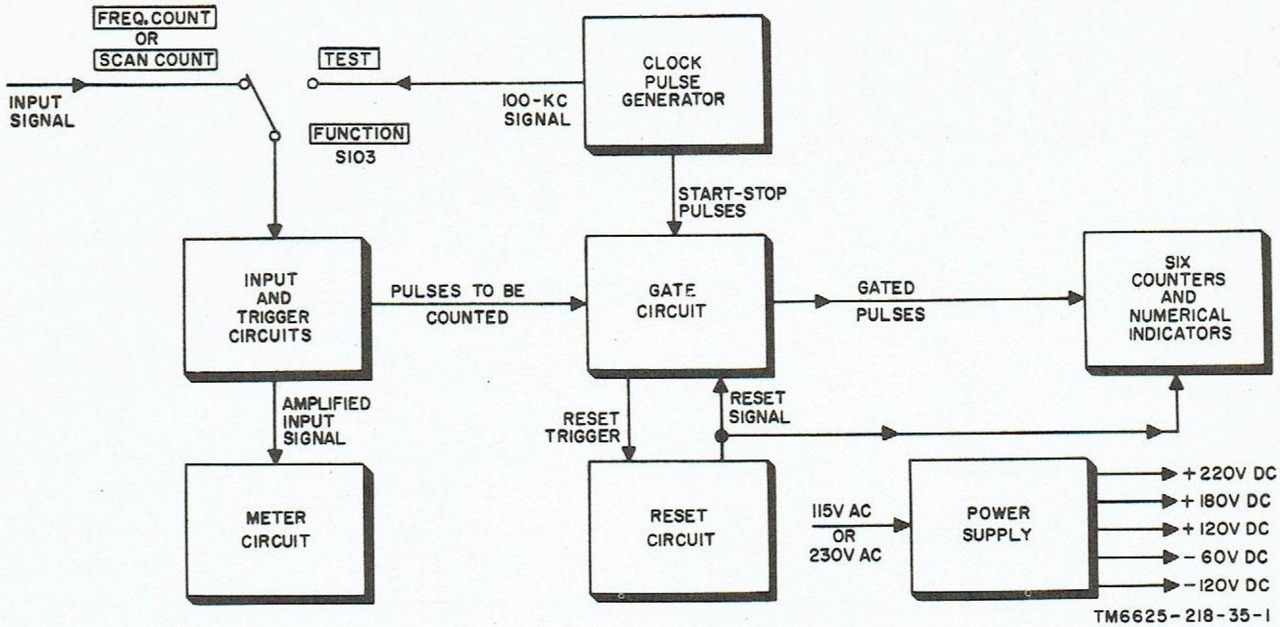

Figure 1. Simplified signal path, block diagram.

d. Meter Circuit. The output of the input trigger channel is coupled to the meter circuit to obtain an indication of signal level. This indication assists the operator in the proper setting of the front panel SENSITIVITY control.

e. Reset Circuit. When the equipment is set up for automatic display, it is necessary to reset the counting circuit to zero electronically after each count. This is accomplished by the reset circuit, which receives the reset trigger pulse from the gate. Reset voltages are generated at the end of each display period and are coupled to the gate circuit and to the counters, thereby enabling them to recycle for the reception of succeeding input signals. In the manual mode of operation, the numerical indicators retain the readout for an indefinite period. Resetting is accomplished manually by pressing and releasing the front panel RESET switch. This produces the identical reset voltage as is used in automatic display operation.

f. Counters and Numerical Indicators. The gated pulses from the gate circuit are applied to the six counters and numerical indicators. The counters are connected in cascade. The *units* Nixie indicator registers incoming counts, with the 10th count also being automatically coupled to the succeeding *tens* counter. Likewise, the second through the fifth counters automatically count and couple each 10th output to the hundreds, thousands, ten-thousands, and hundred-thousands counters, respectively.

g. Power Supply. The internal power supply operates on input power of either 115 volts alternating current (ac) or 230 volts ac, 50 to 1,000 cycles per second (cps). A toggle switch on the rear panel selects the appropriate input power available. An electronically regulated supply produces positive 120-volt and negative 60-volt direct current (dc). Unregulated potentials of positive 220 volts, 180 volts, and negative 120 volts are also produced for use by less critical circuits.

3. Detailed Signal Path Block Diagram, Frequency Count Operation
(fig. 2)

Figure 2 is a block diagram which shows detailed operation of the equipment when used as a frequency counter. The block diagram shows five basic sections. (The reset and power supply circuits are omitted from the discussion.) A separate block diagram (fig. 18) is provided for analysis of the resetting function.

a. Clock Pulse Generator. The clock pulse generator consists of 10 stages, with the last stage consisting of a complete plug-in assembly, clock counter A 301. The clock pulse generator starts with a 100-kç signal developed by crystal

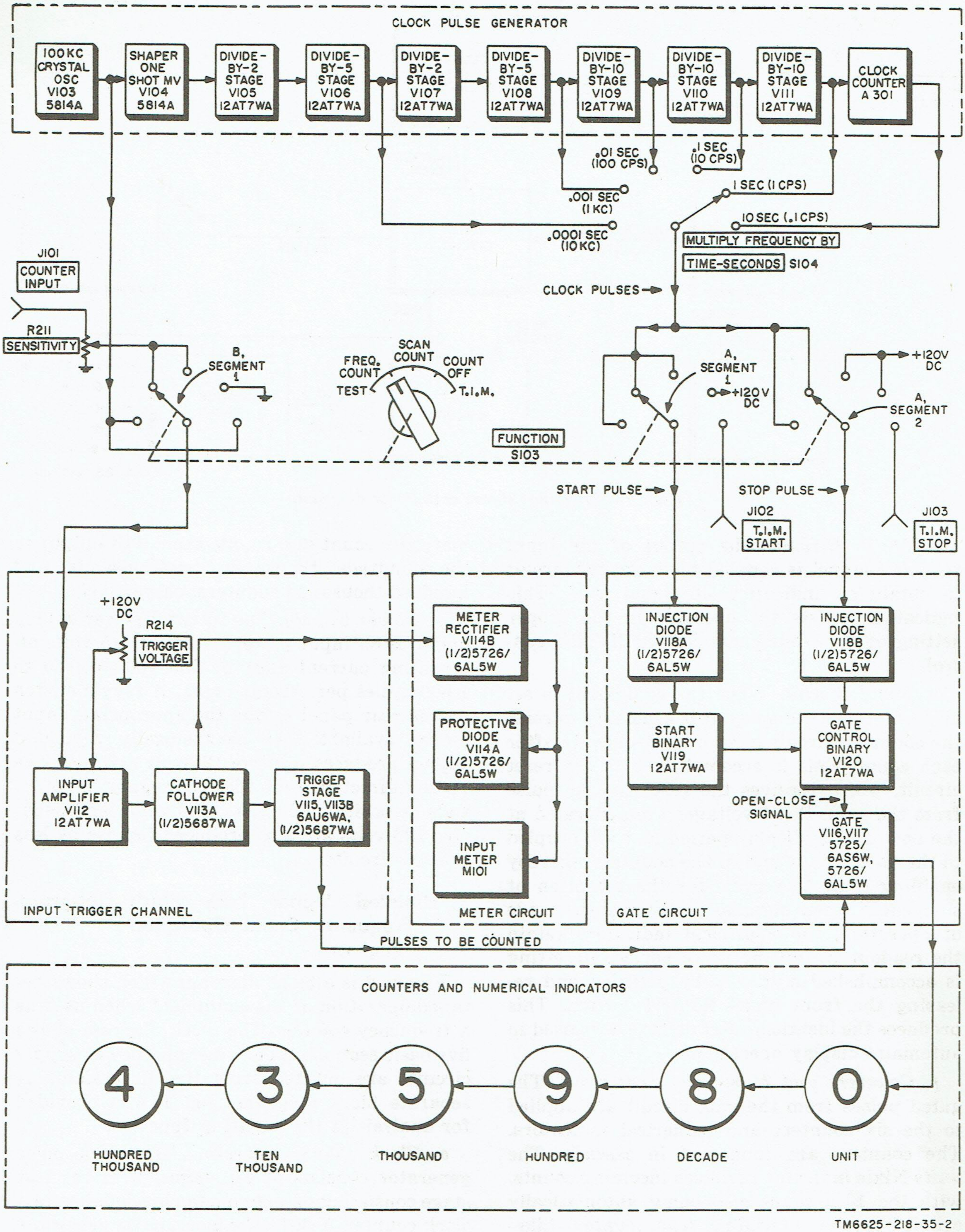

Figure 2. Detailed signal path for frequency counting, block diagram.

oscillator V103 and divides this fundamental frequency by decades into lower frequency signals of 10 kc, 1 kc, 100 cps, 10 cps, and 0.1 cps. The purpose of this division is to permit the selection of the reciprocal of any one of the six divided frequencies as the counting interval. For example: the 0.1-cps signal is selected by rotating the MULTIPLY FREQUENCY BY/TIME-SECONDS switch (hereafter abbreviated to TIME-SECONDS switch) to the 10-second position. Under this condition, the gate circuit will permit the applied input signal to be coupled to the counters for repetitive intervals of 10 seconds each. In addition to 100-kc crystal oscillator V103, the clock pulse generator includes the following stages:

(1) A shaper one-shot multivibrator, V104, which produces modified output pulses of constant amplitude.

(2) A divide-by-2 stage, V105, and a divide-by-5 stage, V106, divide the 100-kc input signal by 10. The resulting 10-kc signal is coupled to the next division stage and to the 0.0001-second interval position of S104.

(3) Another divide-by-2 stage, V107, and another divide-by-5 stage, V108, divide the 10-kc signal from V106 by 10. This 1-kc signal is coupled to the next division stage and to the 0.001-second-interval position of S104.

(4) Three individual divide-by-10 stages, V109, V110, and V111 couple 100-cps, 10-cps, and 1-cps signals, respectively, to both the succeeding stage and to the 0.01-, and 0.1-, and 1-second-interval positions of S104.

(5) Because of the slow time interval of the input signal (1 cps), a special type of binary circuit, with feedback, is required in clock counter A 301 to produce the 0.1-cps (equivalent to a counting time of 10 seconds) output. Clock counter A 301 is a four-stage, plug-in, divide-by-10 circuit.

b. Input Trigger Channel. With FUNCTION switch S103 in the TEST or T.I.M. position, the 100-kc signal from crystal oscillator V103 is coupled into the input trigger channel. With switch S103 set in the FREQ. COUNT or SCAN COUNT position, the 100-kc crystal oscillator signal is disconnected from the channel and an external signal applied to COUNTER INPUT jack J101 is coupled to the input trigger channel. The amplitude of the externally applied signal is adjusted by SENSITIVITY control R211. The input signal is then coupled to the following circuitry:

(1) Input amplifier V112, which amplifies the signal and provides an adjustable dc level set by TRIGGER VOLTAGE control R214.

(2) Cathode follower V113A, which accepts the incoming signal and drives both the meter circuit and the trigger stage.

(3) Trigger stage V115-V113B, a voltage discriminator circuit, modifies the input and develops a series of positive and negative pulses (at the same frequency as the input signal). These pulses are coupled to the gate circuit.

c. Meter Circuit. The meter circuit receives the output of cathode follower V113A. The incoming signal is rectified, and is applied as a dc potential to INPUT LEVEL meter M101. A protective diode is connected in shunt with the meter to protect the meter from damage by strong input signals.

d. Gate Circuit. The gate circuit consists of five stages. Its input signal depends on the position of FUNCTION switch S103.

(1) When the FUNCTION switch is in the TEST or FREQ. COUNT position, injection diodes V118A and V118B receive their inputs from one of the division stages in the clock pulse generator. In figure 2, TIME-SECONDS switch S104 is set at 1. This connects the output of divide-by-10 stage V111 (a frequency of 1 cps or a period of 1 second) to the two injection diodes. The five other positions of S104 are used to pick up the output of the five other division stages in the clock pulse generator, as determined by the operator. The output of diode V118A is coupled to start binary V119, resulting in a flip-flop action in V119. The output pulse from V119 is coupled by gate control binary V120 to gate stage V116-V117. This action opens the gate

and enables the externally applied signal from trigger stage V115-V113B (*b*(3) above) to pass through the gate stage and into the counters. Injection diode V118B, however, also affects gate control binary V120. The output from diode V118B restores V120 to its original condition (an action which occurs at the end of the timing interval) and effectively closes the gate.

(2) When the FUNCTION switch is in the SCAN COUNT position, operation is similar to that described in (1) above, except that no stop pulse is coupled to injection diode V118B. Cumulative counting will continue as long as the FUNCTION switch remains in the SCAN COUNT position. To stop the cumulative count, the FUNCTION switch can be rotated to COUNT OFF, which disconnects the input signal from the input to the gate circuit. Another method of stopping a cumulative count is to rotate the FUNCTION switch to the FREQ. COUNT position; in this position, the next clock pulse will stop the count.

(3) When the equipment is used for time-interval measurements (T.I.M. position of S103), the input to injection diode V118A consists of the signal coupled to T.I.M. START jack J102, and the input to diode V118B consists of the signal coupled to T.I.M. STOP jack J103. The gate circuit will be open for the duration of time between the start and stop pulses.

e. Counters and Numerical Indicators. The counters and numerical indicators receive the pulses that have been passed through the gate circuit. The number of pulses received during the time that the gate is open is registered in one 1-megacycle (mc) counter (the unit counter), and in as many as five 100-kc counters (the tens, hundreds, thousands, ten-thousands, and hundred-thousands counters), depending on the frequency of the input signal. Each counter registers its output on a numerical (Nixie) indicator tube, with its 10th output also coupled to a succeeding counter. The output of each counter energizes electrodes in its Nixie tube, and causes appropriate metallic numerals, within the Nixie tube envelope, to be illuminated. The display persists on the Nixie tubes from the end of the counting interval until the reset signal (par. 2*e*) returns the display to zero.

4. Time Interval Measurement Operation

a. Starting Signal Path. The start signal is coupled from T.I.M. START jack J102 through S103A, segment 1, and V118A into start binary V119, causing this flip-flop stage to change its condition of operation. As a result, the output is coupled to gate control binary V120 which opens the gate stage and permits signals to pass through the gate.

b. Timing Signal Path. In this type of operation, the 100-kc output from crystal oscillator V103 is coupled through input and trigger circuits V112, V113, and V115. Gate stage V116-V117 passes the 100-kc signal to the counters and numerical indicators as long as the gate is open. The period of each cycle of this 100-kc signal is 10 microseconds; each cycle registers one count on the display. Therefore, the time interval between the start and stop pulses is measured in units of 10 microseconds.

c. Stopping Signal Path. When the T.I.M. stop signal is coupled to injection diode V118B, the output pulse closes the gate stage and prevents the passing of any further timing signals through the gate. Therefore, the numerical indicators will show the number of units of time (in 10-microsecond periods) which have elapsed between the application of the start and the stop signals. For example, if there is a readout of 800,000 after the stop signal, multiplying 800,000 by 10 microseconds gives a result of 8 seconds; this indicates that there was an 8-second time interval between the application of the start and the stop signals.

5. Introduction to Stage Analysis

The general signal flow and functioning of the basic sections of Frequency Meter FR-114/U are discussed in this section. The following sections cover a detailed analysis of each stage in the frequency meter. Paragraphs 6 through 15 follow the signal path through the input trigger channel, the meter circuit, the gate stage, and the counters with their numerical indicators. Paragraphs 16 through 25 describe the generation and switching of the control pulses through the clock pulse generator. Paragraphs 26 through 36 describe the gate control circuit and the reset circuit. Paragraph 37 describes the development and distribution of power.

Section II. INPUT TRIGGER CHANNEL AND COUNTER CIRCUITS

6. Input Trigger Channel and Meter Circuit

(figs. 3 and 4)

a. *Input Amplifier.* Input amplifier V112 amplifies the incoming signal and establishes a threshold voltage determined by the operator. There are two possible inputs to the grid, pin 7, of V112. The position of FUNCTION switch S103B determines whether the input comes from COUNTER INPUT jack J101 or from 100-kc oscillator V103.

(1) When S103 is in the FREQ. COUNT or SCAN COUNT position, the input to V112 comes from COUNTER INPUT jack J101 through blocking capacitor C175 and SENSITIVITY control R211. The magnitude of this sig-

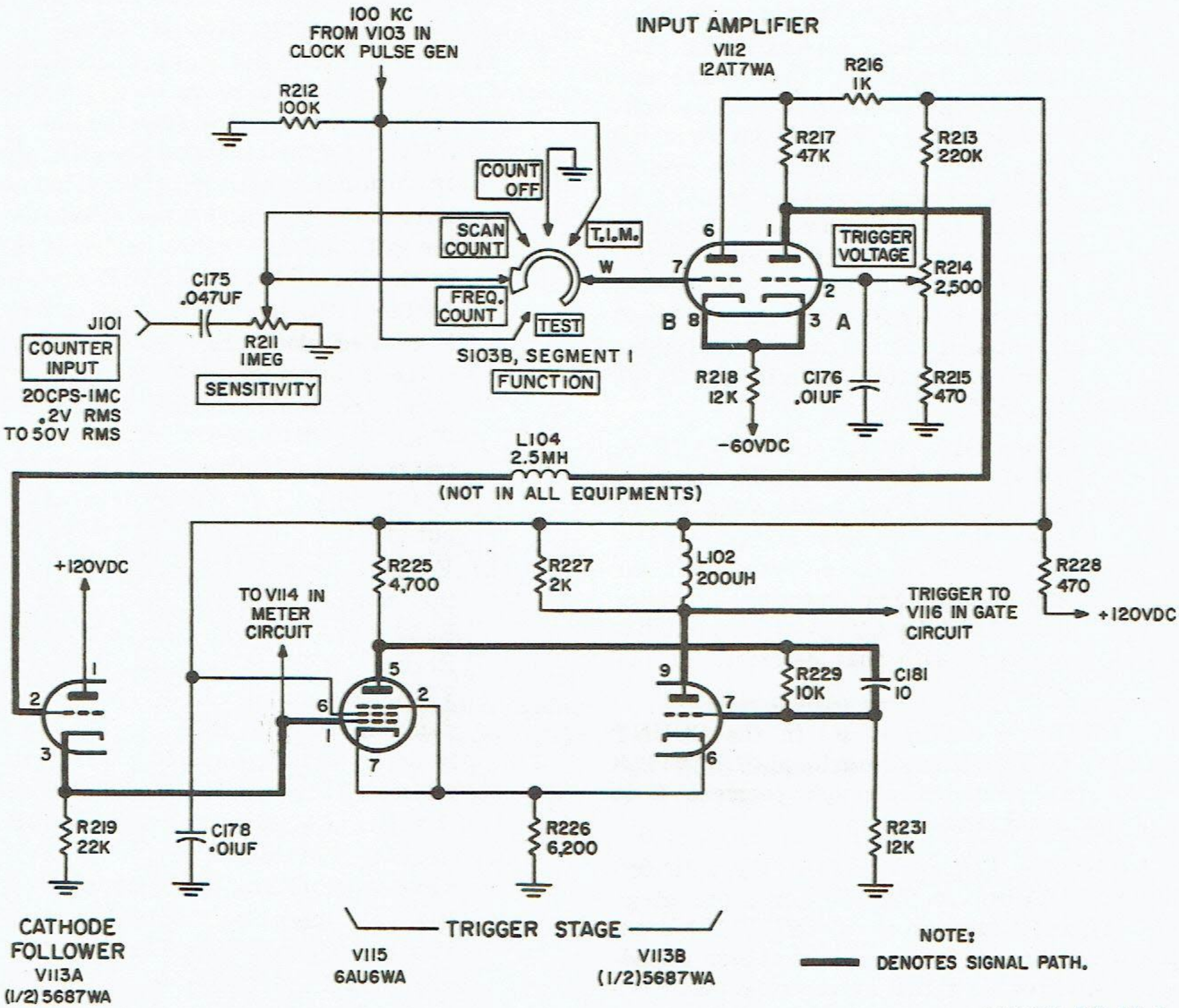

Figure 3. Input trigger channel, simplified schematic diagram.

nal is controlled by adjusting the setting of R211. Stage V112 is a cathode-coupled voltage amplifier with an adjustable dc level maintained across its output. Resistor R218 is the cathode resistor for the cathode follower portion of V112, and is connected to the minus 60-volt line. Resistor R217 is the output plate load resistor; R216 is the plate decoupling resistor. Capacitor C178 and resistor R228 make up a plate decoupling network to isolate the input trigger channel signals from the B+ line. Resistors R213, R214, and R215, in series with R228, form a voltage divider from B+ to ground. The setting of TRIGGER VOLTAGE control R214 determines the positive bias applied to the grid, pin 2, of amplifier V112A. Capacitor C176 bypasses transient pickup voltages to ground The output from the plate, pin 1, is coupled to the grid of V113A through peaking coil L104. Peaking Coil L104 prevents fall-off in response of the input amplifier at frequencies above 500-kc. In certain early-model frequency meters, this coil is not used. Serial numbers of these frequency meters are 1-37, 42, 43, 46, 48, 49, 53, 64, 65 and 77.

(2) When S103 is set in the TEST or T.I.M. position, the 100-kc signal is coupled from oscillator V103 to the grid, pin 7, of input amplifier V112. Resistor R212 is switched into the circuit as a grid impedance resistor for V112B. Operation of the circuit is identical with that described in (1) above.

(3) When S103B is set in the COUNT OFF position, the grid, pin 7, of V112B is grounded through segment 1 to avoid stray pickup.

b. Cathode Follower V113A. Cathode follower V113A isolates the following meter stage (V114) and trigger stage (V115–V113) from the input circuits by providing a high-impedance input for the signal developed across V112 plate load resistor R217, and a low-impedance output for the signal developed across cathode resistor R219. The output signal is dc coupled to V115, the first half of the trigger stage (*c* below). The signal is also coupled through blocking capacitor C117 (fig. 4) to the meter circuit (*d* below).

c. Trigger Stage V115–V113B (fig. 3). The purpose of the trigger stage is to modify the signal of the frequency being measured so that its output will be suitable for driving the six counters and their associated numerical indicators. This stage is a Schmitt trigger, with the circuit constants establishing the voltage required for triggering. When the input signal is of the proper amplitude, the trigger flips, resulting in a sharp output pulse with short rise and fall times. These characteristics are desirable for pulses that must drive high-speed binary counters. Detailed operation is as follows:

(1) The input to this circuit is an ac signal superimposed on a dc level. The ac signal is an amplified reproduction of the voltage variations on the grid, pin 7, of input amplifier V112. The dc level is determined by the voltage on the grid, pin 2, of V112, which is set by the TRIGGER VOLTAGE control. As the TRIGGER VOLTAGE control is rotated clockwise, the dc level is lowered and a higher level of input signal is required for triggering. When the TRIGGER VOLTAGE control is rotated counterclockwise, V115–V113B triggers at a lower level of input signal.

(2) Feedback from V113B occurs through the common cathode line. Resistor R226 is the common cathode resistor. Resistor R225 is the plate load for V115. Peaking coil L102, shunted by damping resistor R227, is the plate load for V113B. Capacitor C181 and resistor R229 couple the signal from the plate of V115 to the grid of V113B. Resistor R229 is also part of the voltage divider (R225, R229, R231) from B+ to ground that biases grid pin 7 at a positive potential. Resistor R231 is the grid load resistor, and forms part of the positive bias voltage divider.

(3) The loop gain is greater than one; the circuit is regenerative and tends to assume one of two stable stages, depending on the amplitude of the voltage applied to V115 grid, pin 1.

(*a*) When the voltage at V115 grid, pin 1, is low, tube V115 is cut off, and V113B, biased positive, conducts steadily.

(*b*) When the voltage at V115 grid, pin 1, rises to the point where V115 begins to conduct, the voltage drop across resistor R225 (additional to the drop caused by divider current flow) lowers the voltage on V113B grid, pin 7. The current through, and the voltage across, R226 decreases, thereby reducing the bias on V115. This regenerative action further increases current through V115 until V115 is fully conducting and V113B is cut off. When the voltage on the V115 grid drops slightly below the triggering value, the action is reversed and the circuit is rapidly restored to the condition described in (*a*) above.

(4) The difference between the level at which a positive-going voltage change triggers the circuit, and the lower level at which a negative-going voltage change causes the action to reverse, determines the input sensitivity. To trigger the circuit back and forth, the input signal must pass through both levels.

(5) Coil L102 differentiates the rapid current changes of V113B to produce a positive pulse at its plate, pin 9, when V115 is triggered by a positive-going voltage. A negative pulse is produced at the plate when V115 is triggered by a negative-going voltage. The output pulses are coupled through C179 (fig. 5) to the control grid of gate stage V116–V117.

d. Meter Circuit. The meter circuit (fig. 4) consists of driver cathode follower V113A and dual diode V114. The signal from V112 is coupled through L104 to the grid of V113A. The dual diode performs two separate functions. One half, V114B, rectifies signals fed to it from cathode load resistor R219 of V113A. The cathode, pin 5, of V114B, is connected to ground and conducts only on the positive half of each input cycle, effectively shorting series network R221, R222, and meter M101. The meter indicates the relative amplitude of the rectified signal. In the presence of strong input signals, protective diode V114A prevents meter burnout by voltage divider action at the junction of R221 and R222. The plate, pin 7, of V114A, is biased by —24 volts obtained from the junction of R223 and R224. When a negative input signal of greater potential than —24 volts is coupled to the cathode, pin 1, V114A conducts. As a result, diode plate current through R224 to ground is in parallel to R222 and M101, preventing excessive current flow through R222 to INPUT LEVEL meter M101.

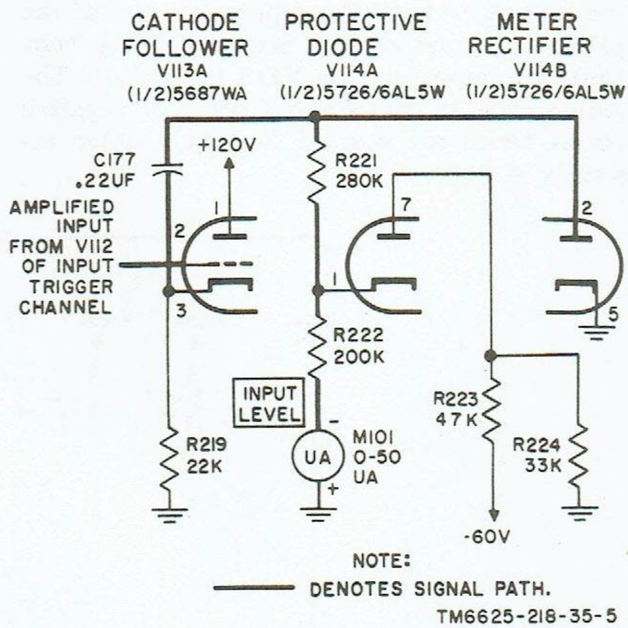

Figure 4. Meter circuit, schematic diagram.

7. Gate Stage, Detailed Analysis (fig. 5)

The gate stage consists of pentode V116, with duodiode V117 operating as a clamp on V116 suppressor grid, pin 7. Resistors R232 and R233 make up a voltage divider connected between —60 volts and ground, and from their junction a fixed negative bias is applied to the grid, pin 1, of V116. This bias potential results in near cutoff of V116. Resistor R234 is the screen dropping resistor and C182 is the screen bypass capacitor. Resistor R235, in series with peaking coil L103, is the plate load resistor. In the clamping stage, capacitor C183, shunted by dropping resistor R237, couples the gate voltage from V120 (in the gate control circuit) to the suppressor grid, pin 7, of V116.

a. While gate control binary V120 is in its reversed condition (B section cut off, par. 27*a* and *b*), the suppressor grid, pin 7, of V117 receives a voltage which is essentially at ground potential. Gate stage V116 conducts and amplifies the positive trigger pulses from V113B through coupling capacitor C179. In this state, the gate is *open*. Negative input pulses drive V116 further into cutoff, and have little effect on tube conduction. When the suppressor grid voltage is negative, V116 cannot conduct even though positive pulses appear on V116 control grid, pin 1. In this state, the gate is *closed*. Both the control grid and the suppressor grid of the gate stage must receive proper polarity voltages simultaneously for V116 to conduct. The output of V116 consists of a series of negative pulses which are coupled to 1-mc counter assembly A 501.

b. Diode V117 is a clamp for the suppressor grid of V116. Its plates, pins 2 and 7, are tied to the suppressor; its cathodes, pins 1 and 5, are connected to ground. The diode will conduct only when the gate control voltage from V120 rises above ground potential. When the diode conducts, the suppressor of V116 is held at ground potential and V117 can conduct.

8. Beam Switching Tube, Introduction
(figs. 6 and 7)

a. The heart of the plug-in counters is the beam switching tube, which is a 10-position, high-vacuum, constant current distributor. The beam switching tube consists of 10 identical arrays located radially about a central cathode (fig. 6). Each array is made up of a spade which automatically forms and locks the electron beam; an output target which makes the beam current available; and a high-impedance switching grid which serves to switch the beam from target to target. A small cylindrical magnet is permanently attached to the glass envelope to provide an axial magnetic field. A large cylindrical magnetic shield (fig. 33) surrounds the exterior of the assembly to prevent stray mag-

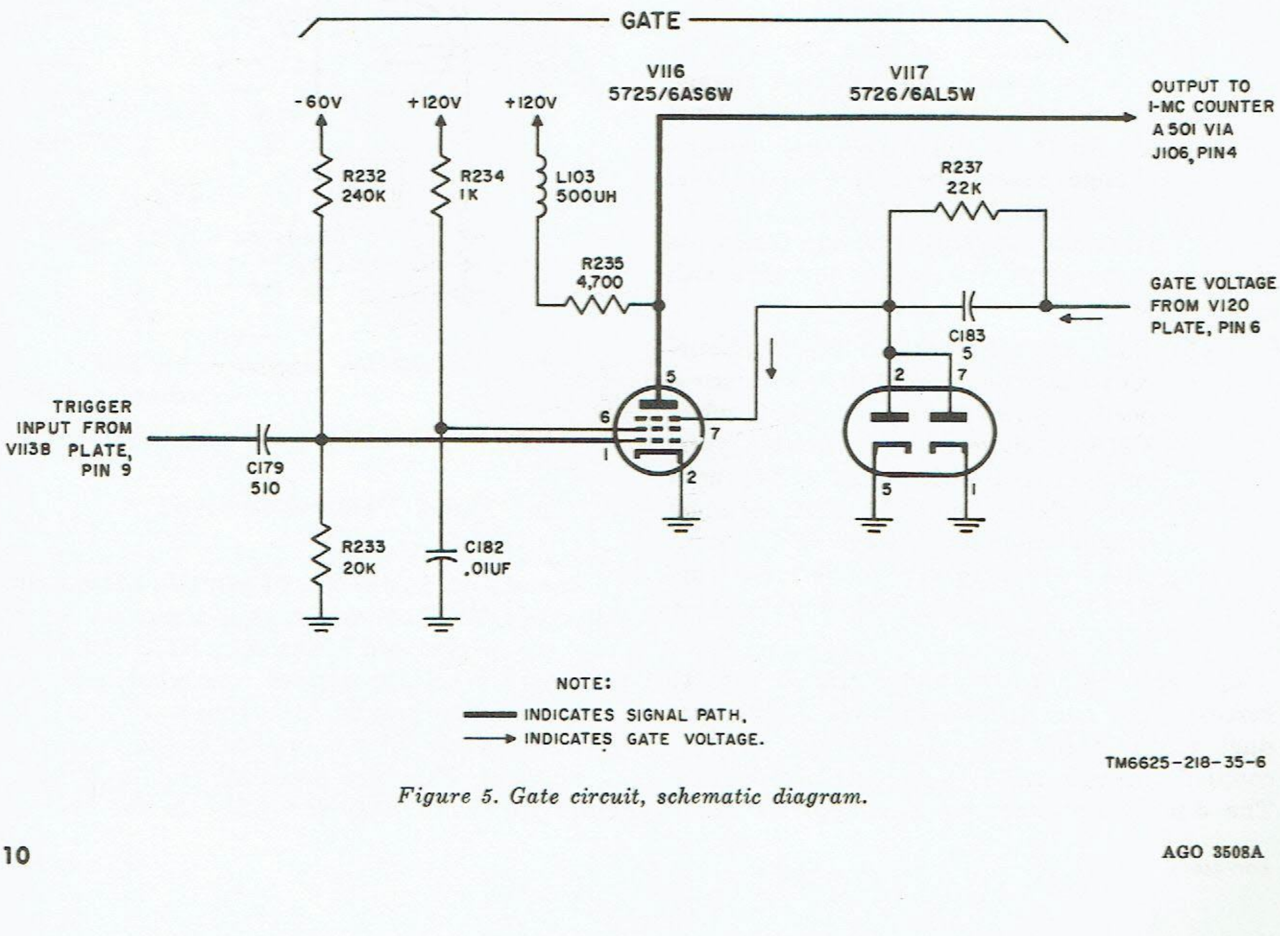

Figure 5. Gate circuit, schematic diagram.

netism from affecting tube operation. The shield is integral with the tube and cannot be removed from it.

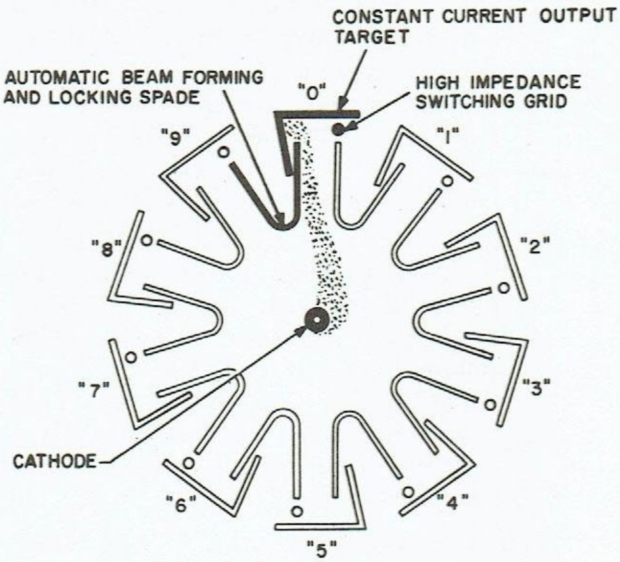

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Figure 6. Beam switching tube array.

b. The cylindrical cathode is in the center of the tube in the longitudinal axis. Around this are the 10 spades. Behind the gaps and between the spades are the targets; in the gaps are the grids. All electrodes run parallel to the axis and to the magnetic field, so that the electric field is at right angles to the magnetic field. The spades are at positive potential, except when current is drawn through them. Under this condition, the potential of the spade drops toward cathode potential. As the electrons move outward from the cathode, they are deflected by the magnetic field; therefore, they move in a spiral and tend to follow an equipotential path. As the electrons move to a zone of higher potential, they gain velocity. The force from the magnetic field becomes stronger and deflects the electrons toward the equipotential line. If the electrons move into a zone of lower potential, they lose velocity and the force of the magnetic field is weakened. The electric field can then deflect them back on course.

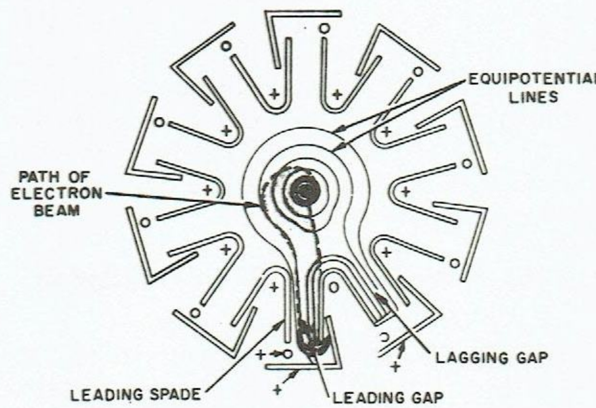
9. Beam Formation, Static Condition

The beam may be formed in any of its 10 *on* positions by sufficiently lowering the potential of the corresponding spade with either a dc voltage or a high-speed pulse. The one spade which forms and locks the beam is near cathode potential; the remaining ones are at B+. A detailed explanation of beam formation follows:

a. If one spade is close to cathode potential and the others are positive, the equipotential lines will run between the low potential spade and adjacent spades (fig. 7). The electrons following these equipotential lines will form a beam and will be guided into the leading gap.

b. Most of the electrons will then reach the target, but some will land on the spade. Under this condition, both the spade and the target will draw current.

c. The fact that a spade can draw current only when its potential is lowered gives it a negative resistance characteristic. Paragraph 10 explains how this characteristic is used in the beam switching action.



NOTE: STATIC-ONE SPADE AT CATHODE POTENTIAL

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Figure 7. Beam switching tube, formation of electron beam.

10. Beam Formation, Dynamic Condition

a. When a beam has been formed on a spade, it can remain there indefinitely, or it can be advanced. One method of advancing the beam is by lowering the switching grid voltage to a value where it will change the electric field in the area between spades. In this way, enough of the electron beam is diverted to the leading spade to cause that spade voltage to be lowered.

b. The grid is, therefore, the electrode used for sequential switching. It performs its function without drawing any appreciable current. Because of the grid shape and position, a negative voltage or pulse to the grid electrodes will effect very fast and uniform switching. The fixed polarity of the magnetic field determines the direction of sequential clockwise switching (fig. 6).

c. In each position, the beam is affected only by the individual grid with which it is associated. The grids are connected in two groups: the odd-numbered grids (1, 3, 5, 7, and 9) in one group, and the even-numbered (0, 2, 4, 6, and 8) in the other. (Odd and even numbers refer to the associated numerals on the Nixie indicator tube to which each array is connected.) Therefore, it is possible to use a dc input in push-pull or flip-flop fashion and still obtain single-position stepping. In Frequency Meter FR–114 U, a flip-flop stage, using high input impedance cathode followers with low-impedance outputs, drives the grids. Figures 8 and 9 show that the output of one cathode follower (V504A for the 1-mc counter, and V4A for the 100-kc counters) drives all the odd-numbered grids. The output of the second cathode follower (V504B for the 1-mc counter and V4B for the 100-kc counters) drives the even-numbered grids. Paragraphs 11 and 12 describe the plug-in counters in detail.

11. The 1-Mc Counter, Circuit Description
(fig. 8)

The 1-mc counter is a plug-in circuit consisting of binary V501, voltage dropping stages V502-V503, cathode follower V504, and beam switching tube V505.

a. Binary V501. Binary stage V501 (tube type 5670) is a flip-flop multivibrator. The circuits of the tube halves, V501A and V501B, are essentially symmetrical.

(1) The plates, pins 4 and 6, each have a plate load resistor (R518 and R516, respectively) connected to the +180-volt supply line through common decoupling resistor R501. The plates have similar crossover networks, with C503–R524 coupling an output from the plate, pin 4, to the grid (pin 7) of the opposite half of the tube. Network C502–R517 couples an output pulse from the plate, pin 6, to the opposite grid, pin 3.

(2) In the grid circuits, diodes CR501 and CR502 pass incoming negative pulses from gate stage V116 via coupling capacitor C506 to the grids, pins 7 and 3, respectively, of binary V501. One grid, pin 3, is tied to the —120-volt supply line through R525 and R526; the other grid, pin 7, is tied to the same voltage source through R519 and R521. Capacitor C505, at the junction of R519 and R521, couples a reset pulse to the grid of V501 (par. 12*b*).

(3) In the cathode circuits, R522 is the common cathode resistor for both halves of the tube; capacitor C504 is the bypass capacitor. Resistor R523 couples cathode voltage to diodes CR501–CR502. This biases the diodes to a level that must be exceeded by the incoming pulse before diode conduction can occur.

b. Voltage Dropping Stages. Voltage dropping stages V502 and V503 are neon lamps connected between the plates, pins 4 and 6 of V501, and the grids, pins 2 and 7, respectively, of cathode followers V504A and V504B. Neon lamps, when conducting, maintain a constant voltage drop over a range of current values. When the rising potential at the V501 plate reaches the striking voltage of the neon lamp, the remainder of the leading edge of the pulse and the pulse plateau are coupled through the low resistance of the neon lamp (reduced by a fixed dc potential). Because neon lamps cannot respond rapidly enough to pass high-frequency square waves, they are bypassed by capacitors C507 (for V502) and C508 (for V503). The capacitors couple the sharp leading edge of the input pulse and high-frequency signals. All incoming pulses must pass through the 1-mc counter and therefore the neon light-capacitor combination must be capable of passing this wide range of frequencies without appreciably changing the V501 plate waveshapes.

c. Cathode Follower V504. The plates, pins 1 and 6, of cathode follower V504 are directly connected to the 180-volt B+ line. The grids, pins 2 and 7, are connected to the —120-volt supply line through grid resistors R527 and R529, respectively. Cathode resistors R528 and R531 develop the signal voltage for V504A and V504B, respectively. These cathode load resistors are also connected to the —120-volt line.

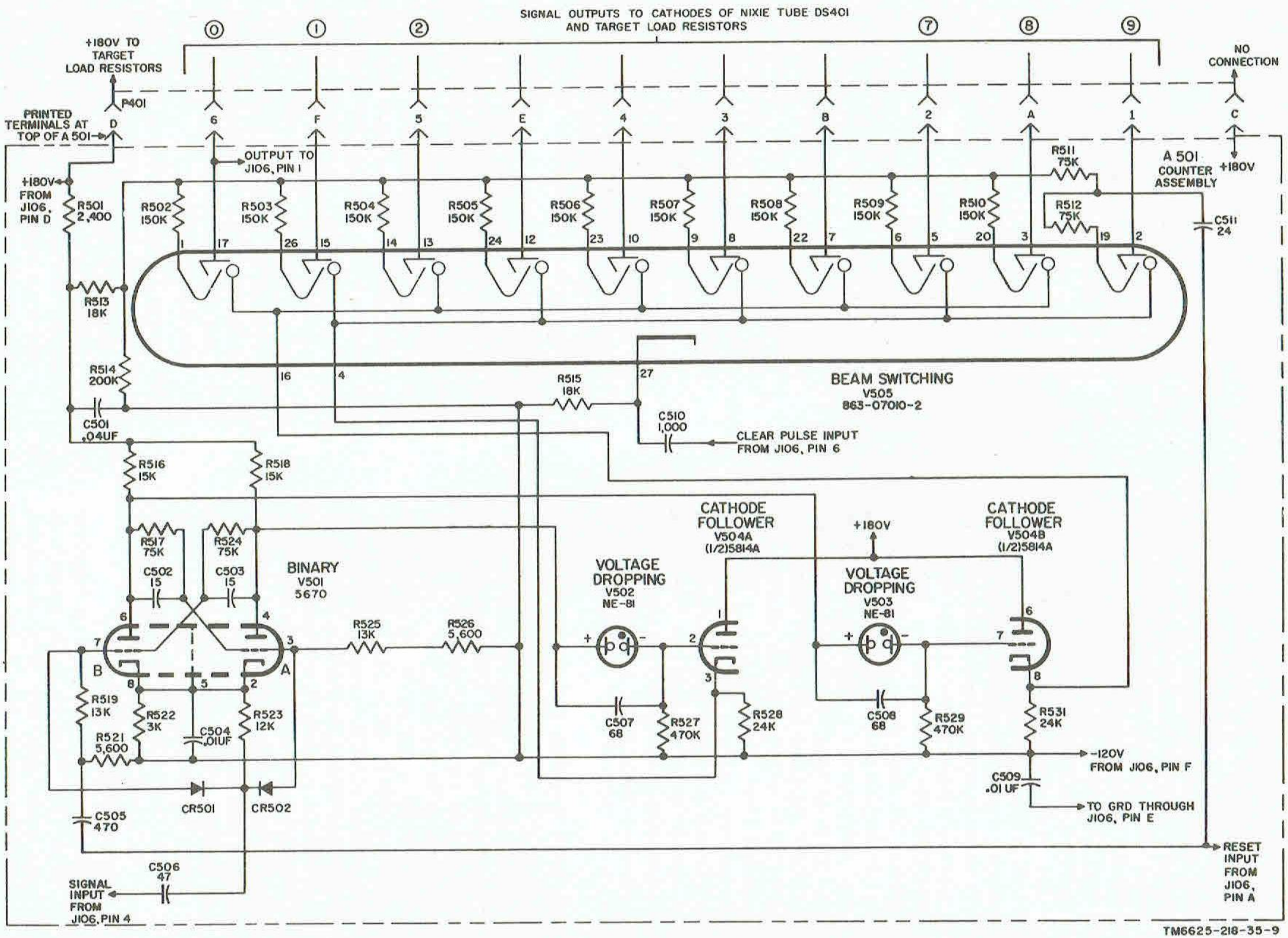


Figure 8. One-mc counter assembly A 501, schematic diagram.

d. Beam Switching Tube V505. The even-numbered grids (par. 10*c*) are connected to the cathode load resistor of V504B and the odd-numbered grids are connected to the cathode load resistor of V504A. Each spade has an identical value load resistor, consisting of R502 through R510 for spades 0 through 8. For spade 9, the load resistor is made up of two equal value resistors, R511 and R512. The reset pulse (par. 12*b*) is received through C511 at the junction of the two resistors. All load resistors are connected through dropping resistors R513 and R501 to the common +180-volt supply line. In the cathode circuit, R515 connects the cathode, pin 27, to the —120-volt line. Capacitor C510 couples the clear pulse (par. 36) to the beam switching tube to allow it to be cleared of all counts. The constant current output of each target is applied in order to numerals 0 through 9 in the Nixie indicator tube. Each 10th count is also coupled into the succeeding counter. The output signal from target 0 (V505, pin 17) couples driving voltage to the succeeding counter through terminal 1 (at the bottom of printed circuit board assembly A 501), and through terminal 1 of mating connector J106, to the input of first 100-kc counter assembly A 601.

12. The 1-Mc Counter, Circuit Operation

a. Beam Switching Action. Immediately after reset (*b*(2) below), V501B is cut off and V501A is conducting. With V501A conducting, the plate, pin 4, is lowered in potential. This output is dc coupled to the grid, pin 7, of V501B and holds V501B in its cutoff condition. The plate, pin 6, of V501B will be at a higher potential; this voltage, which is dc coupled to the grid of V501A, keeps V501A conducting. As long as the stage is not disturbed, it will hold itself in this state indefinitely. This condition will be referred to as the *even* state. A detailed step-by-step analysis follows:

(1) Because of the symmetry of the circuit, there is another possible stable state, with V501B conducting, and V501A cut off. This condition is referred to as the *odd* state.

(2) When a negative pulse is received from gate V116 while the stage is in the *even* state, this pulse is coupled to V501A grid, pin 3, by capacitor C506 and diode CR502. The pulse is amplified and inverted by V501A and coupled by capacitor C503 to V501B grid, pin 7.

(3) Under this condition, V501B will start to conduct and the potential at V501B plate, pin 6, drops. This change in potential is coupled to the V501A grid and cuts off V501A. The stage will then be in the *odd* state.

(4) The next pulse from gate stage V116 will, in a similar manner, be coupled to the V501B grid, via C506 and CR501, and cause the stage to return to the *even* state.

(5) The output voltages, at pins 6 and 4 of binary V501, are coupled by voltage dropping stages V503 and V502 to the grids of cathode followers V504B and V504A, respectively. The voltages at these grids will be the voltages at the plates of V501, reduced by a fixed dc potential. The cathodes, pins 3 and 8, of V504 follow the grid voltage changes, and couple output voltages to the odd-numbered and even-numbered grids, respectively, of beam switching tube V505. Detailed circuit action is then as described below:

(*a*) In the *even* state, the odd grids of V505 are negative and the even grids are positive. In the *odd* state, the even grids of V505 are negative and the odd grids are positive. Initially, with the zero grid positive, the beam is formed upon the zero spade and target and the beam remains there as long as the *even* state persists. When the first pulse is received, the transfer to the *odd* state takes place, as described above, and, with the zero grid becoming negative, the beam is forced to shift to the No. 1 position.

(*b*) In the *odd* state, the odd grids (including the No. 1 grid) are positive. Therefore, the beam will remain on the No. 1 target. When the second pulse is received, a transfer back to the even state will take place, and the beam will be forced ahead to the No. 2 position. In a similar fashion, each succeeding pulse causes a change of state and forces the beam ahead by one position. The overall action is like that of a stepping relay which switches ahead one contact for each input pulse. The outputs are the targets to which most of the electrons pass.

(*c*) When the grids of beam switching tube V505 are driven negative, the beam is deflected to the succeeding gap. Once in the gap, the target becomes activated and illuminates the corresponding numeral within the Nixie tube. When the grids of V505 are driven positive, the beam will remain on a particular target, and its associated numeral within the Nixie tube remains illuminated.

b. Resetting Action. To reset the 1-mc counter, the beam switching tube must be cleared of any existing count which it is registering. The tube can then be reset to accept the next series of input pulses to be counted. The following description covers the clearing and resetting actions:

(1) The electron beam is destroyed by applying a positive pulse of relatively large amplitude to the cathode. This prevents electrons from leaving the cathode surface. A positive-polarity clear pulse is developed within reset generator V123 (par. 36) and is coupled through capacitor C510 to the cathode of the beam switching tube. Because the clear pulse has a duration of less than 1 microsecond, the cathode of V505 can return to its normal emitting condition immediately after application of the clear pulse.

(2) Within 1 microsecond after the application of the clear pulse, a negative reset pulse (also produced by reset generator V123) is coupled through pin A of receptacle J106 (and the mating bottom terminal of printed circuit board assembly A 501) to the junction of capacitors C505 and C511. The negative pulse is coupled through C505 and grid resistor R519 to the grid, pin 7, of V501B, resetting this half of the binary to the *even* state. This action results in driving the even grids of V505 positive, and the odd grids of V505 negative.

(3) The negative reset pulse is also coupled through capacitor C511 to the junction of resistors R511 and R512, at the No. 9 spade (V505, pin 19). By this action, the beam starts to form in position nine. However, the No. 9 grid, along with all other odd grids, is now at a negative potential ((2) above), and the beam is instantly switched to the zero position. The beam remains in the zero position, because the No. 0 grid, along with all other even grids, is positive. The beam switching tube is now ready for the counting action to begin again when the next series of incoming pulses for the timing period selected by the TIME-SECONDS switch is applied.

13. Counter, 100-Kc, Circuit Description (fig. 9)

Five identical 100-kc plug-in counters are used in the display section. The stages in this counter are similar to those in the 1-mc counter (par. 11). Only the differences between the 1-mc counter and the 100-kc counter are described in this paragraph.

a. Binary V1. Binary V1 is a twin-triode stage, similar to binary V501, but a different tube type is used. Stage V1 uses a type 5814A tube with a split heater, and V501 is a type 5670 tube with a single heater. The two tubes are not interchangeable.

(1) Resistors R14 and R20 are the plate load resistors for V1A and V1B respectively. Resistor R13 is the voltage dropping resistor in the +180-volt line. Capacitor C1 couples the incoming signal from the preceding counter to the plate circuits and, thereby, to the grid of the opposite half of the tube. The crossover network, C3–R21, feeds signals from the B plate to the A grid; a corresponding crossover network, C2–R15, functions in a similar

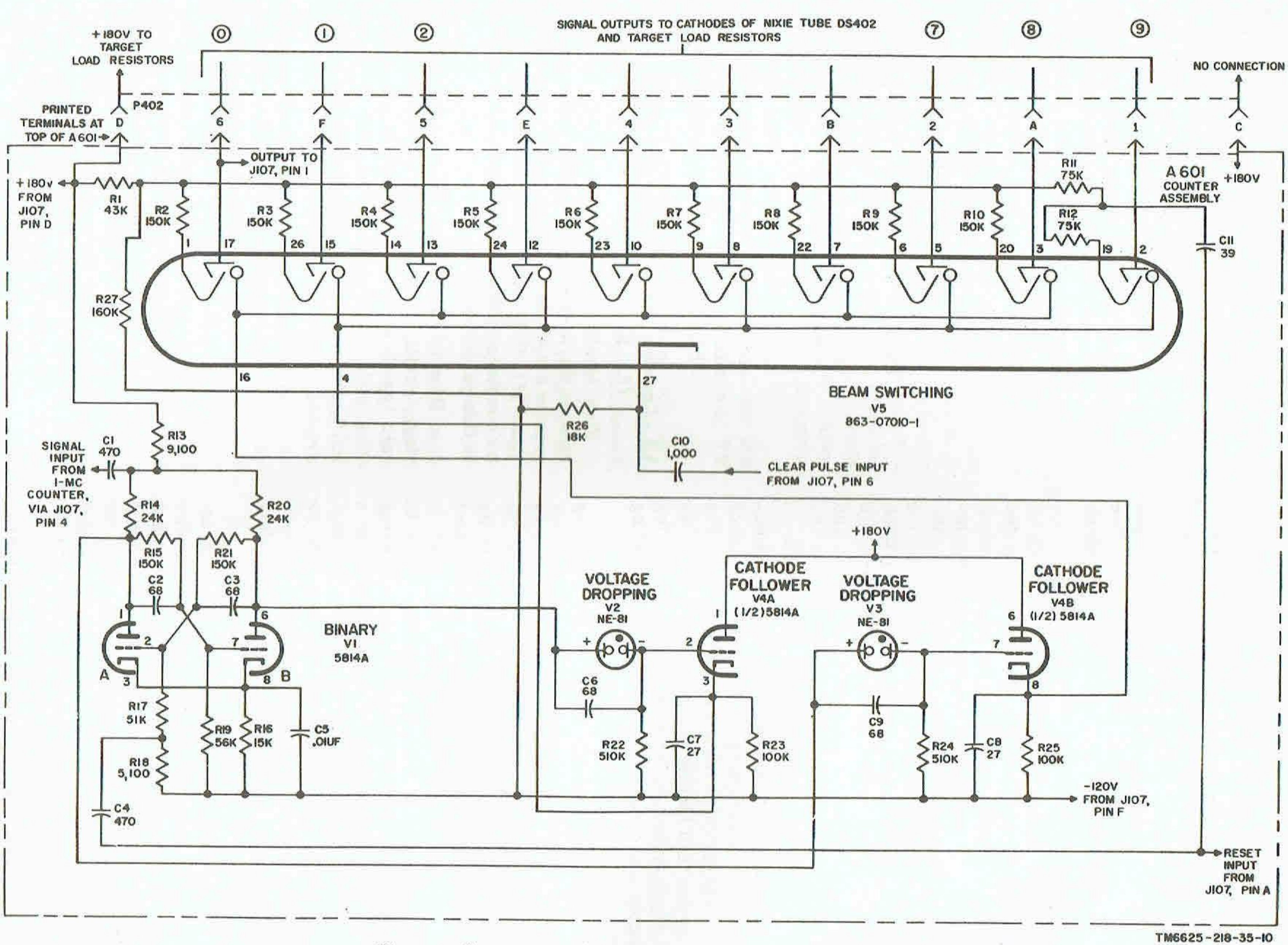


Figure 9. Counter assembly A 601, 100-kc, schematic diagram.

manner for the opposite half of the tube.

(2) Resistors R17 and R18 are the grid resistors for V1A, and R19 is the grid resistor for V1B. The method of coupling the reset voltage through capacitor C4 to the grid, pin 2, is similar to that used in the 1-mc counter, except that the circuit values and ratios of the voltage-divider network (R17–R18) are different.

(3) No crystal diodes are used in the V1 circuit because the method of coupling the incoming signal input pulses to the 100-kc counter is through the plate circuit instead of through the grid circuit as in the 1-mc counter.

b. Voltage Dropping Stages V2 and V3. These stages, working with capacitors C2 and C3, are identical to voltage dropping stages V502 and V503 in the 1-mc counter (par. 11*b*).

c. Cathode Follower V4. This stage is identical to cathode follower V504, in the 1-mc counter, except for changes in values of grid resistors R22 and R24 and cathode resistors R23 and R25. Because the 100-kc counters need not respond to as high a signal input frequency as the 1-mc counter, and to prevent too sharp a rise time of the final output pulse which is coupled to the beam switching tube grids, cathode resistor R23 is bypassed by C7 and cathode resistor R25 is bypassed by C8.

d. Beam Switching Tube V5. The circuitry of beam switching tube V5 is identical to that of beam switching tube V505 (par. 11*d*), except for the value of the spade dropping resistor network. In the 100-kc counter, the +180-volt line is dropped through 43K resistor R1. In the 1-mc counter, series resistors R501 and R513 make up a total voltage dropping resistance of 20.4K. Tubes V5 and V505 are not interchangeable.

14. Counter, 100-Kc, Circuit Operation

a. Beam Switching Action. Immediately after receiving the reset pulse, V1A is cut off and V1B is conducting. The binary tube is then in the *even* state. A negative transient from the zero target of V505 (pin 17, fig. 8) is coupled through connector J107, pin 4, to terminal 4 at the bottom of printed circuit board assembly A 501 and through capacitor C1 to the junction of resistors R13, R14, and R20. The negative transient has no effect on the cutoff half of the binary (V1A), but does affect the condition of the conducting half of V1B. The incoming signal is coupled through plate load resistor R14 and crossover network C2 and R15 to the grid, pin 7, of V1B. This action cuts off current in V1B, and develops a positive-going pulse at the plate, pin 6. The positive pulse output of V1B causes a flip-flop action in the binary because the pulse is coupled through C3 and R21 to the grid, pin 2, of nonconducting V1A. Tube V1 is then in the *odd* state. The resulting circuit action within each of the five 100-kc counters (A 601–A 605) is identical to that described in paragraph 12*a*. The outputs from the plates of V1 are coupled through the voltage dropping stages to the grids of cathode followers V4A and V4B. The cathodes, pins 3 and 8 of V4, couple output voltages to the odd-numbered and even-numbered grids, respectively, of beam switching tube V5. In the *even* state, the odd grids of V5 are negative and the even grids are positive. The reverse is true in the *odd* state.

b. Resetting Action. The resetting action of the 100-kc counters is identical to that described in paragraph 12*b*. Coupling capacitor C11 in the 100-kc counter is a different value from corresponding capacitor C511 in the 1-mc counter.

15. Nixie Circuit Board A 401
(fig. 44)

Nixie circuit board A 401 is the mounting board for the six numerical indicator tubes, DS401 through DS406, their tube sockets, and their associated resistor networks. Connections from the output of each target of the beam switching tubes are made to a corresponding metallic numeral within the Nixie tube.

a. The Nixie tube is a neon gas-filled cold-cathode tube. It contains 10 cathodes and 1 common anode. Each of the cathode elements is formed in the shape of a numeral (0–9). When the cathode voltage is lowered sufficiently, the specific cathode (numeral) is surrounded by the characteristic neon glow. Only this numeral is visible.

b. Because all six of the Nixie tubes have identical circuits, this paragraph discusses only one stage, DS401, the numerical indicator for the units readout. Resistor R471, the anode voltage dropping resistor, is connected to the 220-volt power supply. Each cathode (corresponding to numerals 0 through 9) has an identical value target load resistor in its circuit, designated R401 through R410. Common to all the target load resistors is cathode dropping resistor R461 which is connected to the 180-volt supply. With no current flow, the voltage from any cathode to the anode is 40 volts. This voltage is not sufficient to cause electron flow. When current from the beam switching tube is applied, the voltage at the cathode is lowered, and when a 170-volt difference is obtained, the tube fires from the appropriate cathode to the anode.

c. For the remaining Nixie tubes, the following chart lists those parts performing identical functions:

Nixie tube	Target load resistors	Common cathode resistor	Anode dropping resistor
DS402	R411 through R420	R462	R472
DS403	R421 through R430	R463	R473
DS404	R431 through R440	R464	R474
DS405	R441 through R450	R465	R475
DS406	R451 through R460	R466	R476

d. The load on the beam switching tube targets is made up of the target load resistor and the Nixie tube numeral. The target load resistors are necessary because the Nixie tube cannot carry the full target current of the beam switching tube. Each target resistor, besides drawing superfluous target current, stabilizes the action of the beam switching tube by providing a more constant load impedance.

Section III. CLOCK PULSE GENERATOR STAGES

16. General
(fig. 2)

The clock pulse generator, which consists of stages V103 through V111 and plug-in clock counter assembly A 301, provides two separate types of outputs depending on the setting of FUNCTION switch S103.

a. With FUNCTION switch S103 in the FREQ. COUNT, SCAN COUNT, or TEST position, the timing interval output of the clock pulse generator is used. Counting intervals of 0.0001, 0.001, 0.01, 0.1, 1, or 10 seconds can be selected by the setting of the TIME-SECONDS switch. The gate stage, V116, permits incoming signals to pass on to the counters and numerical indicators for the selected counting interval. (See figure 2, S103A, segment 1, for functional illustrations of this application of the clock pulse generator circuit.) In the TEST position, the 100-kc output of the clock pulse generator is also used.

b. With FUNCTION switch S103 in the T.I.M. position, only the 100-kc output is used. This 100-kc signal is either the output of self-contained crystal oscillator V103 (with INT.-EXT. switch S107 in the INT. position) or the amplified output of an externally applied 100-kc signal source (S107 in EXT. position). The external signal is coupled into the frequency meter through EXTERNAL 100 KC jack J112 on the rear panel.

17. Crystal Oscillator V103
(fig. 10)

Stage V103 is a crystal-frequency controlled oscillator used to produce a 100-kc signal when INT.-EXT. switch S107 is in the INT. position. When S107 is in the EXT. position, V103B amplifies an externally applied 100-kc signal.

a. Internal Oscillator Operation. The manner in which the 100-kc signal is generated is as follows:

(1) With INT.-EXT. switch S107 in the INT. position, V103 is a two-stage regenerative amplifier. It is basically a free-running multivibrator with frequency determined by a crystal instead of resistance-capacitance (RC) circuits. Oscillator sections V103A and V103B are cathode-biased by the voltage developed across their respective cathode resistors, R119 and R121, and are always conducting. Capacitors C115 and C116 are radiofrequency (rf) bypass capacitors. Resistor R134 and capacitor C113 provide plate decoupling.

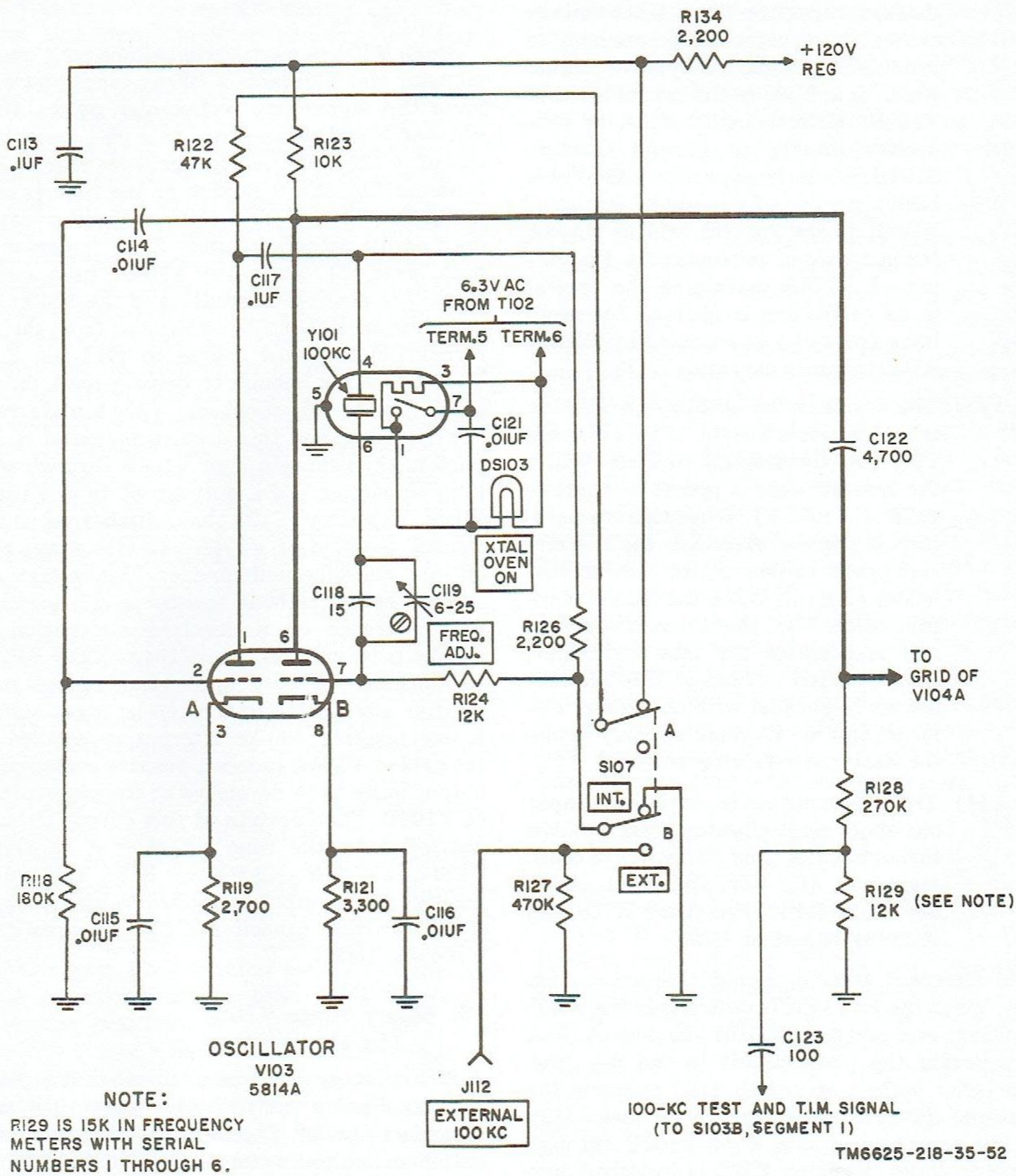


Figure 10. Crystal oscillator stage V103, schematic diagram.

(2) B+ voltage (120 volts, regulated) is applied to the plate of V103A through S107A. With V103A conducting, crystal Y101 obtains an exciting voltage through capacitor C117. This voltage causes the crystal to vibrate and to provide a 100-kc sine wave signal which is applied to the control grid of V103B. Grid resistor R124 is connected directly to ground through S107B. Coupling capacitor C114 feeds back a portion of the 100-kc output of V103B to the control grid of V103A for purposes of regeneration. The output of V103A maintains the crystal in an oscillating condition. The oscillator frequency is adjusted by FREQ. ADJ. trimmer capacitor C119.

(3) The crystal oven obtains 6.3 volts ac from terminals 5 and 6 of transformer T102. A thermostat, located within the crystal oven, is preset to regulate at 75° C (167° F). When this temperature is slightly exceeded, the thermostat opens to deenergize the internal heater element. When the temperature falls below 75°C the thermostat closes, and reenergizes the internal heater. XTAL OVEN ON lamp DS103 is connected in parallel with the heater element and is illuminated only when the heater is receiving power.

(4) The 100-kc output is coupled to shaper one-shot multivibrator stage V104 through C122, and to switch S103B, segment 1 (fig. 43), and input amplifier V112 through resistor R128 and coupling capacitor C123.

b. External 100-Kc Signal Operation (fig. 10). When the INT.-EXT. switch is in the EXT. position, one section of S107 disables V103A by opening the plate circuit to the B+ line. The other section of switch S107 connects the external 100-kc signal (obtained via jack J112) to the control grid, pin 7, of V103B through resistor R124. Resistor R127 is switched into the circuit to become the grid resistor for V103B. The amplified external 100-kc signal at the plate, pin 6, is then applied to V104 through C122 and to input amplifier V112 through S103B, segment 1 (*a*(4) above). The crystal circuit plays no part during external 100-kc signal operation.

18. Shaper One-shot Multivibrator V104 (fig. 11)

Stage V104 is a conventional one-shot multivibrator which obtains a 100-kc input and converts this signal into rectangular pulses. Grid pin 7 of V104B is returned to a positive potential of +120 volts through grid resistor R135; consequently, the B section of the tube is normally conducting. The voltage thereby developed across cathode resistor R131 (common to both sections) maintains V104A in a cutoff state. The positive alternation of the 100-kc input from crystal oscillator V103 or from the external 100-kc signal source to grid pin 2 of V104A is large enough to drive V104A out of cutoff. Under this condition, V104A plate voltage decreases and this drop in potential is applied to the grid, pin 7, of V104B through coupling capacitor C124, cutting off tube V104B. When capacitor C124 has discharged sufficiently, the grid of V104B will rise above cutoff, and the tube will conduct. The voltage developed across cathode resistor R131, together with presence of a negative alternation at V104A grid, cuts off tube V104A. Tube V104A remains cut off until application of the next positive alternation of the 100-kc input signal. Every positive 100-kc alternation applied to the grid of V104A causes a positive rectangular output pulse to be developed at the plate, pin 6, of V104B. The duration of this output pulse is controlled by the time constant of capacitor C124 and V104B grid resistor R135. The 100-kc positive pulse output is applied to binary stage V105 through capacitor C125 and resistors R136 and R137.

19. Binary Stage V105 (fig. 11)

Binary stage V105 is a conventional plate-coupled flip-flop multivibrator operating as a frequency divider. The 100-kc rectangular pulse output of multivibrator V104 is divided into a 50-kc square wave output.

a. There are two conditions of stable equilibrium. One condition is obtained when V105A is conducting and V105B is cut off. The other condition is obtained when V105B is conducting and V105A is cut off. One or the other of these conditions is maintained, with no variations in plate, grid, or cathode potentials (or in plate current), until some transient signal is introduced and the sections reverse their operation. The new condition remains unchanged until another signal is applied.

b. When positive plate potential (+120 volts dc) is simultaneously applied to both plates, pins 1 and 6, of V105 through respective plate load resistors R138 and R143, one section will conduct more current than the other. For purposes of circuit analysis, assume that V105A conducts more than V105B. This results in a voltage drop across plate load resistor R138 of greater amplitude than the drop across plate load resistor R143. The lowered voltage is reflected at the control grid, pin 7, of V105B through the direct-coupling network consisting of resistors R144 and R145. This decreases plate current through V105B and thereby increases the voltage at plate pin 6. This increased voltage, in turn, is applied to the control grid, pin 2, of V105A through a direct-coupling network consisting of resistors R139 and R141. The increased positive voltage applied to the control grid of V105A causes additional plate current flow through V105A, reducing the voltage at its plate. The same action continues until V105 is in a stable state, with V105A conducting at maximum and V105B cut off. The stage remains in this condition until a pulse from V104 is applied.

c. The positive square wave output from shaper one-shot multivibrator V104 is coupled through capacitor C125 to two resistor networks. One network consists of R137 in series with R143, and the other consists of R136 in series with R138. With C125, these networks differentiate the incoming pulses and the signals appearing at the tube grids appear as alternate positive and negative triggers. The positive triggers have no effect; the conducting half of the tube is already at saturation and the positive amplitude (approximately one-fifth of the original voltage due to voltage-divider action) is insufficient to allow the nonconducting half to come out of cutoff. The negative trigger, however, can affect the conducting tube section (assumed to be V105A). This negative pulse is amplified and inverted by V105A to produce a strong positive pulse at its plate. The positive pulse from the plate is coupled through the crossover network, consisting of C128 and R144, to the grid, pin 7, of V105B. Because of action similar to that in *b* above, V105B is now conducting and V105A is nonconducting. The negative output is coupled through capacitor C129 to the input of V106A, and through C132, R146, and C133, to the input of V106B. A portion of the negative output from V105B plate, pin 6, is fed back to the grid, pin 2, to reinforce cutoff of V105A.

d. The original state of binary V105 is restored by the succeeding differentiated negative incoming pulse. The signal path is through C125, R136, and C128 to the grid, pin 7, of V105B. The positive pulse has no effect on V105B, which is now conducting. The negative input pulse, however, causes a change in V105B by first reducing its conduction, and soon cutting the tube off completely. This negative pulse is amplified and inverted by V105B to produce a strong positive pulse across plate load resistor R143. The positive output is coupled through capacitor C126 to restore conduction in V105A. Since each negative input pulse to binary V105 causes each section of the binary to change state, two negative input pulses are required to produce 1 complete output cycle. The 100-kc signal from V104 is divided down to 50 kc, with each section of V105 conducting for 10 microseconds and cut off for 10 microseconds. The total elapsed time for 1 cycle is, therefore, 20 microseconds (the reciprocal of 50 kc).

20. Divide-by-5 Stage V106
(figs. 11 and 12)

a. This stage functions as a flip-flop frequency divider. It differs from the operation of V104 in that conduction of V106B is synchronized to the fifth submultiple of the applied 50-kc signal. With no input, the stage is stable. Tube V106B is conducting because its control grid is connected to the +120-volt supply through resistor R154 and .0001 TIME BASE ADJUSTMENTS potentiometer R155. Tube V106A is cut off by the voltage drop across common cathode resistor R151 (bypassed by capacitor C134). Resistor R149 is the grid resistor for the A section.

b. The square wave output of binary V105 is differentiated by the network consisting of capacitor C132 and resistors R146 and R147. The positive differentiated pulse has no effect on V106B, because this half of the tube is already conducting at saturation. The negative differentiated pulse, however, is coupled through capacitor C133 to the control grid, pin 7, of V106B. The output appears as an amplified positive pulse at the plate, pin 6, of V106B and is coupled to the control grid, pin 2, of V106A via capacitor C131. This positive pulse causes V106A to conduct, and provides a decreased value of plate voltage at pin 1. The decreased plate voltage is applied to the control grid of V106B as a negative-going voltage via coupling capacitor C133.

c. The regenerative action produces a quasi-stable state in which V106B is cut off, and V106A is conducting. Tube V106B will remain cut off as long as C133 holds sufficient charge to keep the V106B grid below cutoff. The capacitor C133 discharge path is through R154, R155, C144 and R165, ground, cathode resistor R151, and conducting section A of V106. Because of the long time constant, the voltage present on the *timing grid,* pin 7, rises relatively slowly. At the same time, negative input pulses from V105 (reaching the control grid, pin 2, of V106A via coupling capacitor C129) appear as amplified positive pulses at the plate, pin 1. These positive pulses are coupled to the timing grid, pin 7, through capacitor C133 and appear superimposed on the rising voltage curve (fig. 12).

d. Figure 12 shows the rise in voltage at grid pin 7. When the fifth pulse is applied, voltage is above cutoff and V106B conducts. Flip-flop action returns the stage to its original stable state. The frequency output at the plate, pin 6 of V106B, is one-fifth of the 50-kc trigger input, equivalent to 10 kc. The 10-kc pulses are coupled by capacitor C136 to the next binary, V107, and by capacitor C135 to the .0001 position of TIME-SECONDS switch S104.

e. Figure 12 shows that .0001 TIME BASE ADJUSTMENTS control R155 is adjusted to set the 10-kc output precisely. The setting of variable resistor R155 adjusts the slope of the charging curve for capacitor C133 by changing the V106B bias voltage. If the bias voltage for V106B grid, pin 7, is made more positive, more resistance will be inserted in the discarge line and capacitor C133 will discharge more slowly. This may result in division by the sixth trigger pulse. When the bias voltage for V106B is

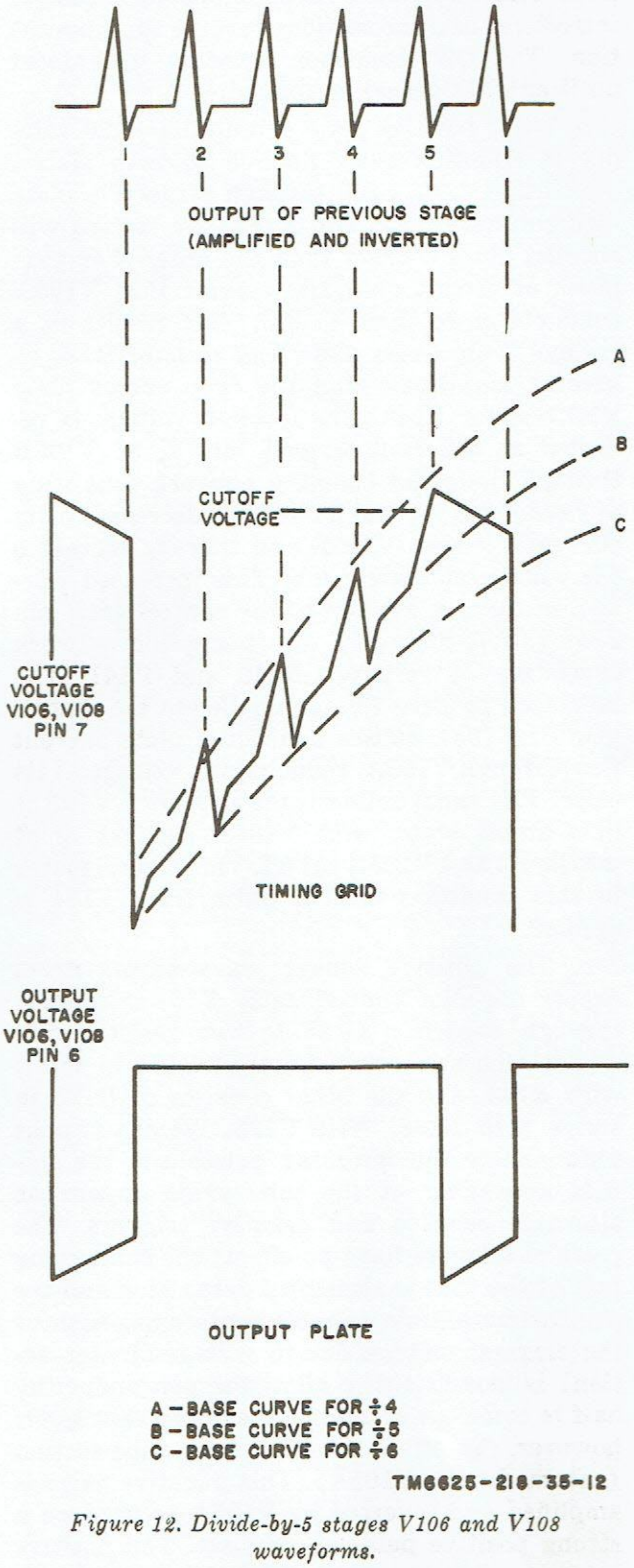


Figure 12. Divide-by-5 stages V106 and V108 waveforms.

Figure 11. Clock pulse generator stages V104 through V111, schematic diagram.

made less positive, less resistance is inserted in the discharge line, the capacitor will discharge faster, and division by the fourth trigger pulse may result. Resistor R165 is used as part of a voltage divider in the grid circuits of V106B and V108B and is also a factor in capacitor C133 and C146 discharge. Capacitor C144 also bypasses voltage variations to ground.

21. Binary Stage V107
(fig. 11)

Binary stage V107 operates in the same manner as binary stage V105, except that with an input of 10 kc, an output of 5 kc is developed. All circuit components have the same values as equivalent parts in stage V105 except for differentiating network resistors R156 and R157. These are 47K; corresponding resistors R136 and R137 in the V105 stage are 100K. The final 5-kc output signal from the V107B plate, pin 6, is coupled through capacitor C141 to V108A grid, pin 2, and through capacitor C143, in series with resistor R166 and capacitor C146, to V108B grid, pin 7.

22. Divide-by-5 Stage V108
(fig. 11)

Divide-by-5 stage V108 operates in the same manner as divide-by-5 stage V106, except that with an input to V108 of 5 kc, an output of 1 kc is developed. All circuit parts have the same values as equivalent parts in stage V106 except coupling and time-constant capacitor C146 and input differentiating resistor R166. Capacitor C146 is 470 micromicrofarads ($\mu\mu$f) and R166 is 100K; in the V106 stage, the corresponding components are 56 $\mu\mu$f and 150K, respectively. The .001 TIME BASE ADJUSTMENTS control, R174, functions in the same manner as .0001 TIME BASE ADJUSTMENTS control R155 (par. 20) to set the 1-kc output precisely. The 1-kc output signal is coupled through C149 and C148 to the next division stage, V109. In addition, the 1-kc output signal is available for selection as a 0.001-second timing interval at terminal 5 of TIME-SECONDS switch S104.

23. Divide-by-10 Stages V109, V110, and V111
(figs. 11 and 13)

Each of these divide-by-10 stages operates in the same manner as divide-by-5 stage V106, differing only with respect to input and output frequencies. In addition, the values of plate-to-grid coupling capacitors C153, C158, and C166 differ in each stage, because different frequencies are involved in each case. Because of their similarity, a detailed analysis of the frequency-divider waveforms (fig. 13) is given with respect to V109. The explanation is equally applicable to V110 and V111, except for changes in reference symbols.

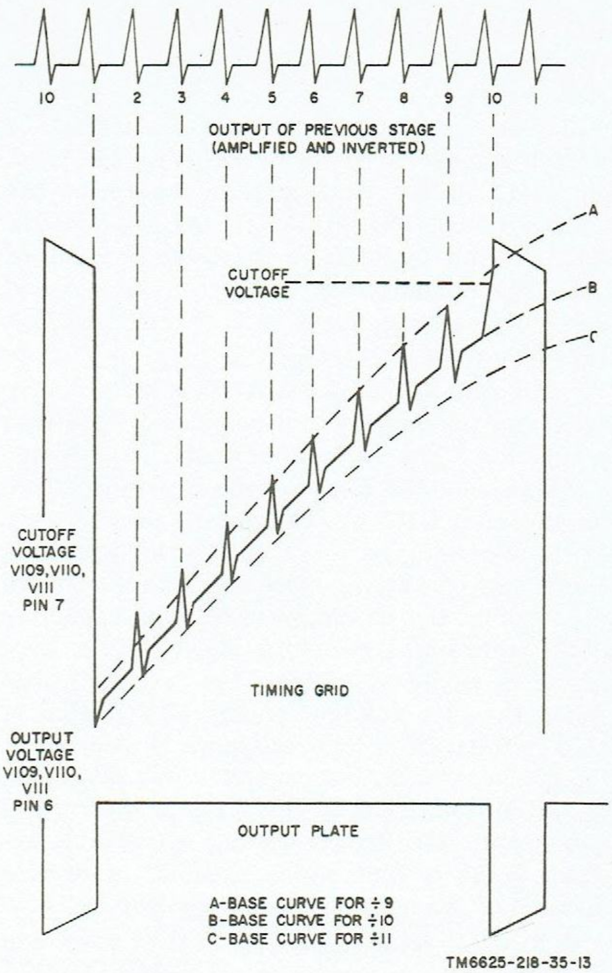


Figure 13. Divide-by-10 stages V109, V110, and V111 waveforms.

a. Figure 13 shows the differentiated input waveform, and how these pulses are superimposed on the recovery-time curve at the grid, pin 7, of V109B. While capacitor C153 discharges through resistors R183 and R185, the grid potential rises toward cutoff. The 10th trigger pulse from driver stage V108 drives the grid, pin 7, of V109B slightly above cutoff, causing V109B to begin drawing plate current. This action initiates a new output cycle at V109B plate, pin 6.

b. The sudden drop in plate potential of V109B is coupled through C151 to the grid, pin 2, of V109A, causing that portion of the tube to cut off. The .01 TIME BASE ADJUSTMENTS control, R185, in the discharge path of C153, may be adjusted to change the slope of the recovery-time curve and thereby set the 100-cps output precisely.

c. Figure 13 shows that R185 is set properly when the 10th trigger pulse drives V109B into conduction. The setting of variable resistor R185 adjusts the slope of the charging curve for capacitor C153 by changing its bias voltage. If the bias voltage for V109B grid, pin 7, is made more positive, more resistance will be inserted in the discharge line and capacitor C153 will discharge more slowly. This may result in division by the 11th trigger pulse. When the bias voltage for the V109B gird is made less positive, less resistance is inserted in the discharge line, the capacitor will discharge faster, and division by the nigth trigger pulse may result. The proper setting of variable resistor R185 is that which produces a precise division of the input trigger frequency by 10.

d. Resistor R190 is used as part of a voltage divider in the grid circuits of V109B, V110B, and V111B and is also a factor in capacitor C153, C158, and C166 discharge. Capacitor C164 bypasses voltage variations to ground.

e. By means of frequency-dividing action, the precise 10th output of each stage is coupled to the circuits shown in the chart below:

Stage	Output frequency (cps)	Output to next stage	Output to switch S104
V109	100	V110	Terminal 4 (.01 second position).
V110	10	V111	Terminal 3 (.1 second position).
V111	1	Clock counter A 301	Terminal 2 (1 second position).

24. Clock Counter Assembly A 301
(fig. 14)

a. Clock counter assembly A 301 is a four-stage cascade-connected binary counter, which forms a divide-by-10 configuration for incoming signals of 1 cps. This circuit produces a 0.1-cps output (having a period of 10 seconds) for each 1-cps input obtained from the preceding divide-by-10 stage, V111.

b. Binary stages V301 through V304 (fig. 14) operate in a similar manner to binary stage V105 (par. 19), except for the following differences:

(1) The plates, pins 1 and 6, are returned to +220 volts. Each tube has a voltage dropping resistor common to both plates. These are R307, R312, R319, and R336, respectively, for V301 through V304.

(2) The control grid, pin 2, of each A section is returned to a control voltage designated *reset to nine* (par. 25*f*). Grid return resistors R311, R321, R331, and R339 are tied between these grids and terminal 2 of plug P301. Paragraph 33 describes the generation of the reset voltage by reset amplifier V121. Paragraph 25 explains the effect of this reset control voltage on clock counter operation.

(3) The control grid, pin 7, of each B section is returned to —120 volts through terminal 6 of plug P301 and its mating connector J105.

(4) Cathode resistors R305, R316, R326, and R333 for each binary are connected to the —120-volt source through terminal 8 of plug P301 and its mating connector J105.

c. Four cascade-connected binaries would ordinarily function as a divide-by-16 frequency network. Clock counter A 301, however, functions as a divide-by-10 network, accepting a 1-cps input signal from V111, and producing a 0.1-cps output signal. A detailed analysis of the divide-by-10 scale is given in paragraph 25.

25. Clock Counter and Scale of 10
(figs. 14–16)

In clock counter A 301, four binaries are con-

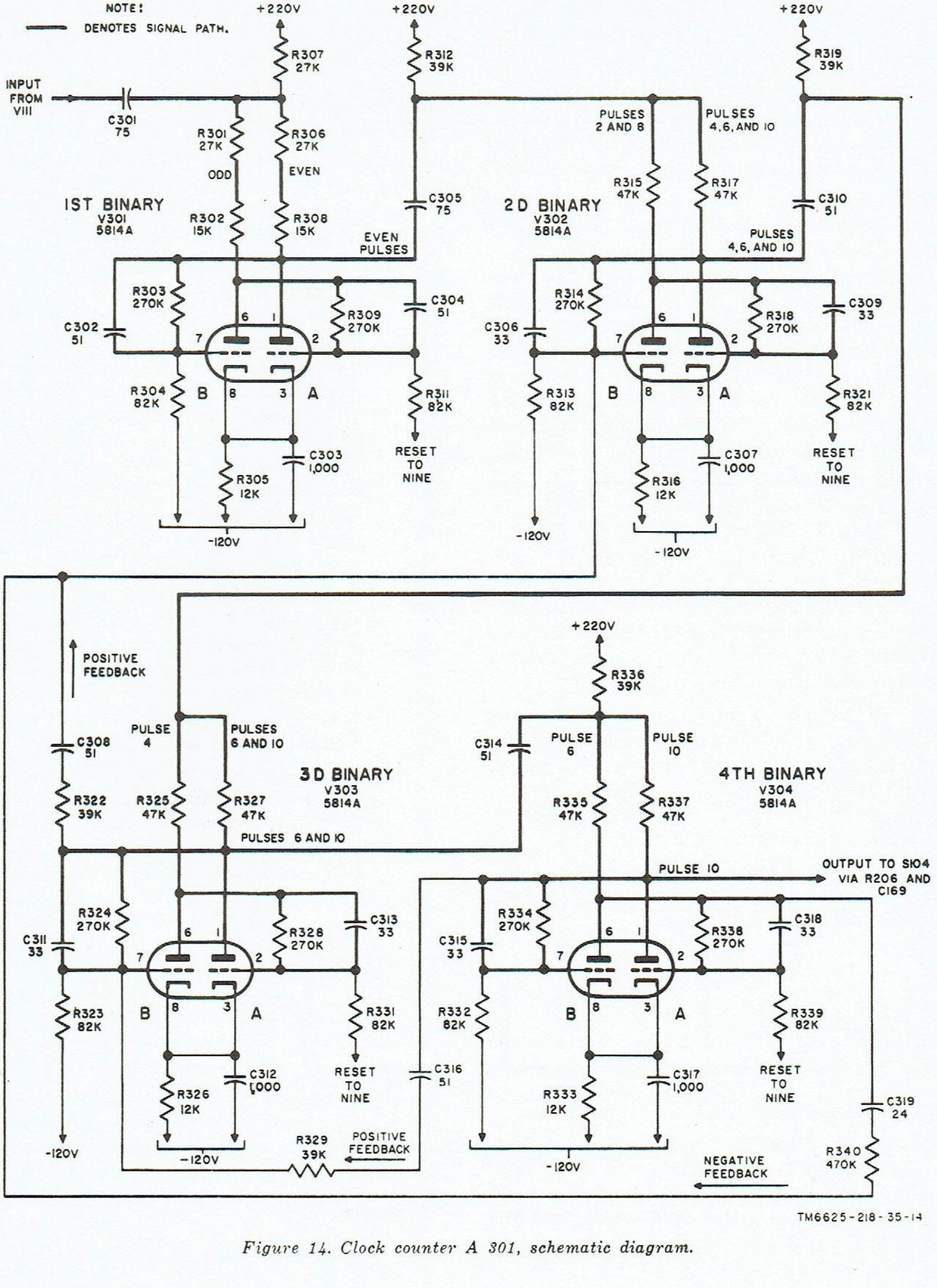


Figure 14. Clock counter A 301, schematic diagram.

nected in cascade to form a scale of 16, which is changed to a scale of 10 by 2 positive feedback paths, as shown in the simplified block diagram (fig. 15) and in the idealized waveforms (fig. 16).

a. For the first 3 negative input pulses (fig. 16) from the preceding divide-by-10 stage, V111, the circuit operates as a simple binary counter.

b. At the fourth input pulse, third binary V303 is triggered for the first time, sending a pulse through the first positive feedback path (R322 and C308, fig. 14) to trigger second binary V302 again. Because two input pulses are required to complete each binary cycle, this feedback is equivalent to adding two input pulses. Therefore the state of the clock counter circuit now corresponds to a binary count of six input pulses.

c. The sixth input pulse (equivalent to the eighth input in a simple binary chain) triggers fourth binary V304, which sends a pulse through the second positive feedback path (R329 and C316 to the grid, pin 7, of V303), triggering the third binary. This feedback action is equivalent to adding 4 more input pulses, so that the state of the clock counter circuit now corresponds to a binary count of 12.

d. For the next 4 input pulses (7–10), the circuit operates again as a simple binary chain, producing an output pulse at the 10th pulse. Adding the equivalent of 6 input pulses internally has, therefore, changed the binary chain from a scale of 16 to a scale of 10.

e. At the sixth input pulse, third binary V303 is triggered along with fourth binary V304 (fig. 16). This action sends a second pulse along the first positive feedback path (R322 and C308). This pulse could trigger binary V302 again, adding two extraneous counts. The prevent this, the pulse is mutually neutralized by a simultaneous pulse of opposite polarity from binary V304, through the feedback path consisting of C319 and R340 to the grid, pin 7, of V302.

f. After completion of the display interval, clock counter A 301 is reset to 9 to avoid delay of the next 10-second counting interval. The following is a description of the reset cycle:

(1) The reset-to-nine action, while not an essential requirement in design, saves time for the operator. If not reset to 9, the counter in going through the process described above, would produce 1 pulse every 10 seconds because a pulse is necessary to start the counting period as well as to end the count. There would be a minimum of 10 seconds between counts and the interval between counts would be some multiple of 10 seconds.

(2) By resetting the clock counter to 9 at the end of the display period (at the same time as the display is reset to zero), the next 1-second pulse functions as though it were a 10th pulse, and produces an output to start the next counting period. The next count begins within 1 second after reset.

(3) This reset-to-nine action is accomplished by feeding a negative pulse from reset amplifier V121 (par. 33*c*) through grid resistors R311, R321, R331, and R339 to the control grids, pin 2, of binaries V301 through V304, respectively. This negative polarity

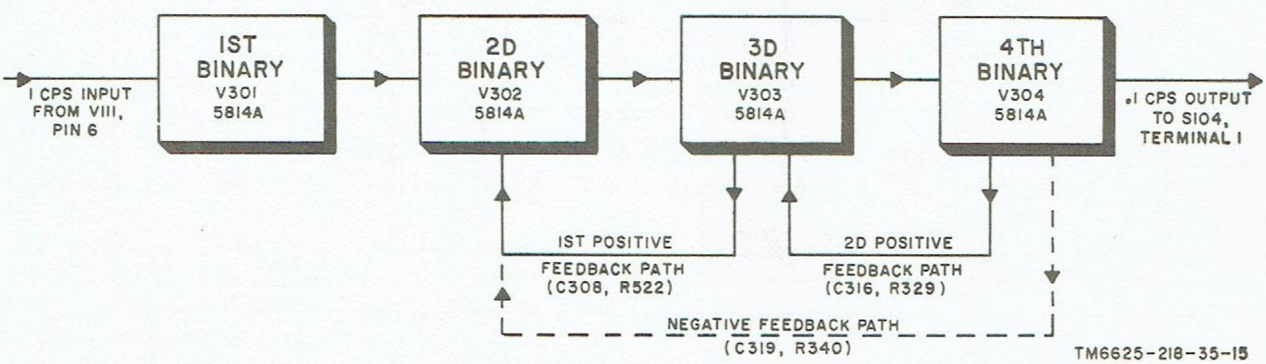


Figure 15. Clock counter A 301, simplified block diagram.

signal applied to the control grids, pin 2, restores the binaries in the clock counter to the condition existing for a count of nine. A detailed analysis of the generation of the reset circuit is given in paragraph 30.

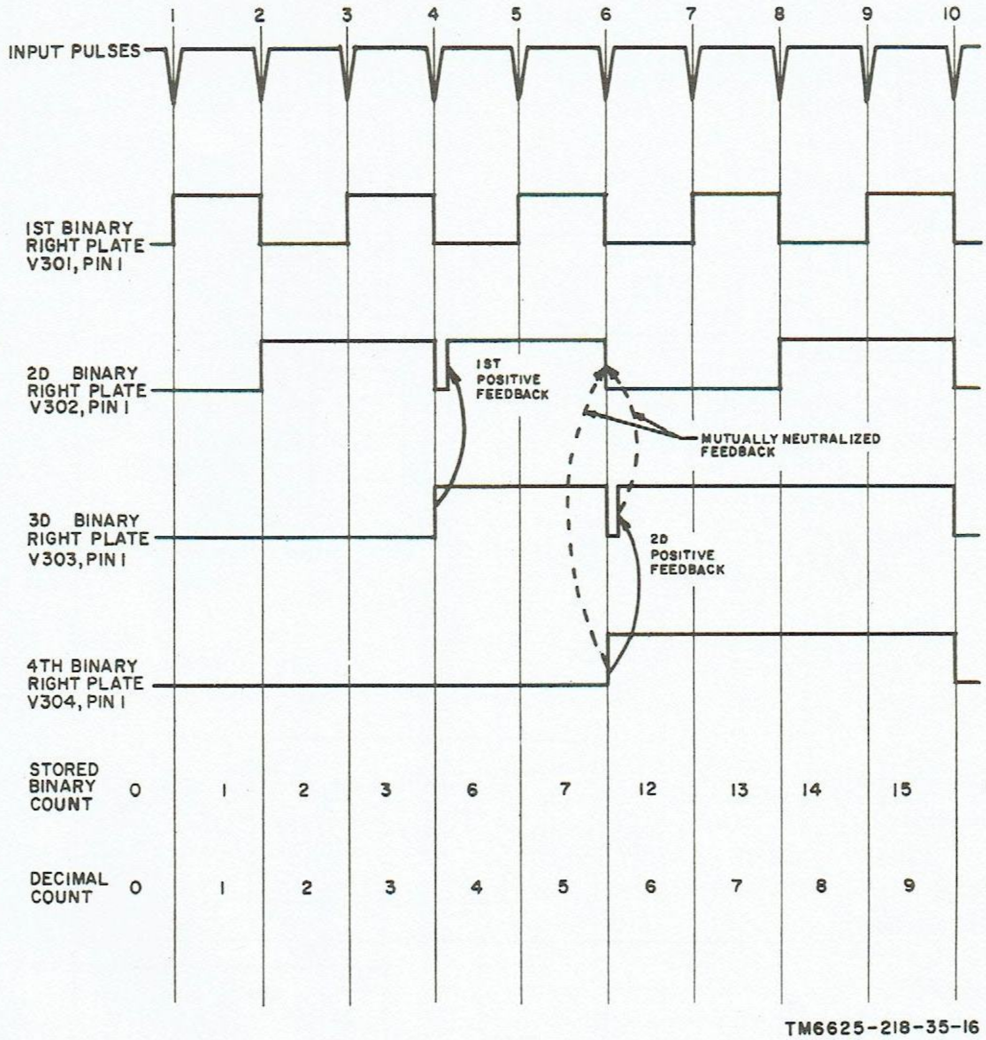


Figure 16. Clock counter A 301, idealized waveforms.

Section IV. GATE CONTROL, RESET, AND POWER SUPPLY CIRCUITS

26. Gate Control Circuitry, Introduction (fig. 17)

The gate control circuit consists of stages V118 through V120, with the final output driving the suppressor grid, pin 7, of gate stage V116 (par. 7) to ground potential. During the period that the suppressor of V116 is at ground potential, the gate stage amplifies and couples the input signal at its control grid, pin 1, to the six cascaded counted. In this state, the gate is *open*. When V116 suppressor grid is at a potential lower than ground, the gate is *closed*, and no signals can be coupled to the counter assemblies. Paragraphs 27 and 28 describe the generation of the *open-closed* voltages in the gate control circuitry. Paragraph 29 covers a brief description of a secondary output of the circuit, which is termed *readout control*.

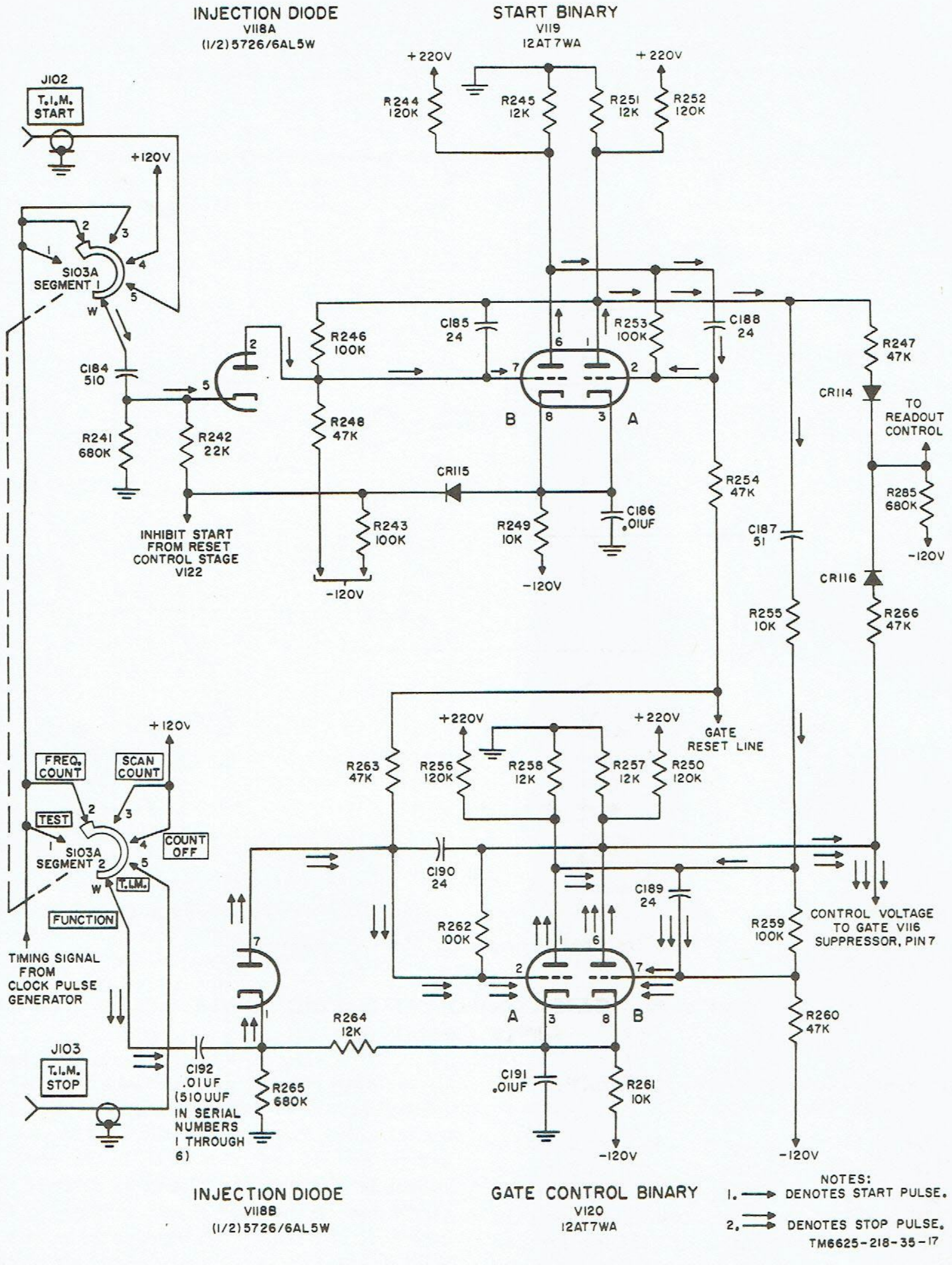


Figure 17. Gate control circuit, schematic diagram.

27. Gate Control Binary V120 and Injection Diode V118B

(fig. 17)

The *open-close* voltages which are applied to the suppressor grid, pin 7, of V116 are generated at the plate, pin 6, of gate control binary V120. This stage is a conventional flip-flop circuit, similar in basic operation to binary V105 in the clock pulse generator circuit (par. 19). The stage has two stable states, with either V120B conducting and V120A cut off or with V120A conducting and V120B cut off.

a. Input pulses or transients, applied at various points in the circuit, will trigger V120 back and forth between its two stable states. A negative start pulse transient from the plate, pin 1, of start binary V119, is coupled through capacitor C187 and resistor R255 and grid network C189 and R259 to the grid, pin 7, of V120B. This pulse triggers gate control binary V120 to cut off V120B and allow V120A to conduct.

b. In this state, the voltage at V120B plate, pin 6, rises above ground. This voltage, applied to gate stage V116 (fig. 5), allows the latter to conduct and pass incoming pulses into the counters, with the count registering on the Nixie indicators.

c. When a negative stop pulse from FUNCTION switch S103A, segment 2, reaches the grid, pin 2, of V120A through coupling capacitor C192 and injection diode V118B, the gate control binary is triggered back to the state where V120B is conducting; the negative plate potential holds gate stage V116 closed.

d. Cathode resistor R261, bypassed by capacitor C191, is common to both halves of the gate control binary stage. Resistors R261, R264, and R265 are part of a voltage divider from the —120-volt bus to chassis ground. The cathode, pin 1, of injection diode V118B is biased negatively, at approximately the same potential (only slightly less negative) as the cathodes of V120. Resistor R262, shunted by capacitor C190, serves as the crosswork network from the plate, pin 6, of V120B to the grid, pin 2, of V120A. Resistor R263 is the grid return for V120A grid, pin 2, and is connected to the gate reset line. Except during the gate reset pulse, the potential of the gate reset line is —120 volts. The plate of V118B is tied directly to this grid. At this time, the plate is more negative than the grid and the diode is cut off. The gate reset pulse is discussed in paragraph 30. In the plate circuits, resistor R250 is the plate load for V120B. Resistor R257 is connected from plate to ground and, with R250, forms a voltage divider to establish correct plate voltage. A similar divider circuit, R256 and R258, is used in the V120A plate circuit. Resistor R256 is the plate load resistor. In the grid circuits, resistor R259, shunted by C189, is the crossover network from the plate, pin 1, of V120A, to the grid, pin 7, of V120B. Resistor R260 is the grid return for V120B. Diode CR118 in the gate reset line circuit (fig. 20 and par. 33*b*) couples the negative 120-volt line to the grid of V120A through grid resistor R263. This keeps the potential of the gate reset line at —120 volts except during the gate reset pulse.

e. In the TEST and FREQ. COUNT positions of S103A, segment 2, the timing signal from the clock pulse generator (as selected by TIME-SECONDS switch S104) is coupled through capacitor C192 to the cathode, pin 1, of injection diode V118B. In the SCAN COUNT and COUNT OFF positions, capacitor C192 is connected to +120 volts. This is the same potential as that applied to other contacts of the switch segment through individual resistors and S104. This prevents false pulses to C192 due to switching operations between different dc potentials. In the T.I.M. position, pulses from T.I.M. STOP jack J103 are coupled to the cathode of V118B. Incoming negative pulses are coupled to V118B, driving the cathode strongly negative. The diode had previously been cut off because the plate was negative with respect to the cathode. With the cathode driven negative, the diode conducts and a negative pulse is applied from the V118B plate to the V120A cathode. This triggers V120 (*c* above).

28. Start Binary V119 and Injection Diode V118A

(fig. 17)

Start binary V119 is a conventional flip-flop circuit (par. 19) with two stable states, and is similar in circuit description to V120 (par. 27). Either V119B is conducting while V119A is cut off or V119A is conducting while V119B is cut off.

a. With V119B conducting, its plate, pin 6, is negative with respect to ground. In the TEST, FREQ. COUNT, and SCAN COUNT positions of S103A, segment 1, the negative timing signal from the clock pulse generator (as selected by TIME-SECONDS switch S104) is coupled through capacitor C184 to the cathode of injection diode V118A. In the COUNT OFF position, +120 volts is connected to C184. This serves no function directly but prevents development of false pulses during switching operations. Other contacts of S103A, segment 1, have +120 volts applied through individual resistors and TIME-SECONDS switch S104. The false pulses would be generated if different dc potential levels were applied to C184. In the T.I.M. position, pulses from T.I.M. START jack J102 are coupled to the V118A cathode.

b. From capacitor C184, the negative pulse is applied to the cathode of cut-off diode V118A (*e* below). The negative pulse to the cathode causes V118A to conduct, plate voltage is dropped and this negative pulse is directly coupled to the grid, pin 7, of the conducting half of the binary, and cuts off V119B. Further negative pulses coupled through injection diode V118A to V119B grid, pin 7, will have no effect until the binary flops again.

c. In this state, the voltage at V119B plate, pin 6, rises above ground potential. The positive output from V119B is coupled through crossover network C188 and R253 to the grid, pin 2, of V119A. This action triggers a change in the binary to its other stable state, producing a negative output transient at V119A plate, pin 1. Paragraph 27*a* describes the action that this negative output transient has on gate control binary stage V120. The net effect is to allow the gate (V116) to open and a count to register.

d. Cathode resistor R249, bypassed by capacitor C186, is common to both halves of the start binary stage and is connected to the —120-volt line. Injection diode V118A cathode, pin 5, is biased negatively through voltage-divider resistors R241, R242, and R243, which are connected between chassis ground and the —120-volt supply line. Diode CR115 prevents the positive-going inhibit start voltage (par. 31*b* (7)(*c*)) from affecting the required negative potential at the cathode circuit of start binary V119.

e. In the plate circuits, resistor R244 is the plate load for V119B and, with R245, forms a voltage divider to drop the 220-volt bus voltage to a suitable value for tube operation. A symmetrical circuit is used for V119A plate, pin 1, with R252 the plate load, and R251 connected from plate to ground to form another voltage divider from the 220-volt line to ground.

f. Resistors R252, R246, and R248 form a voltage divider between the +220-volt and the —120-volt supply lines. Grid voltage for pin 7 of V119B is taken from the junction of R248 and R246. This is directly connected to the plate, pin 2, of V118A. This voltage is more negative than the cathode and the diode is cut off. Pulses from S103A, segment 1, (*a* above) cause the diode to conduct. A symmetrical circuit is used for the V119A grid, pin 2, with resistors R244, R253, and R254 making up a voltage divider across the same potentials. Diode CR118, in the gate reset line circuit (fig. 20 and par. 33*b*), couples the —120-volt supply line to the grid, pin 2, of binary V119A through grid resistor R254.

29. Readout Control Diodes CR114 and CR116

(figs. 17 and 43)

The final output transients of binaries V119 and V120 are used for the opening and closing of gate stage V116, and for the development of a readout control voltage which is applied to the control grid, pin 2, of reset amplifier V121. Diodes CR114 and CR116 are connected so that the readout control line will be positive when *either* V119A plate, pin 1, *or* V120B plate, pin 6, is positive (the tube section is nonconducting). When neither plate is positive, the readout control line is biased negatively through R285 by the —120-volt supply line. A more detailed circuit analysis of the readout control line is given in paragraph 32*b*.

30. Reset Circuit Analysis, Introduction

a. Circuits Affected by Reset Action. Analysis of the reset circuit requires an understanding of a number of actions which must occur at the end of each counting interval. Paragraph 16 describes how the counting interval is determined by the setting of TIME-SECONDS switch S104. The following circuits are affected by reset voltages:

(1) The 1-mc and all five of the 100-kc counter assemblies must first receive a *clear* voltage, which destroys the electron beam in the beam switching tubes. An instant later, the beam must be switched to the zero position, so that the numeral zero will appear on each of the six Nixie indicator tubes before a new counting interval occurs.

(2) Binaries V119 and V120 in the gate control circuit must receive a negative polarity pulse on their control grids, pin 2, so that the initial stable state of each binary is restored. In this manner, section A of each binary is returned to its initial cutoff state.

(3) Injection diode V118A must be set into a state, immediately after a display period, in which it cannot couple timing signals into start binary V119

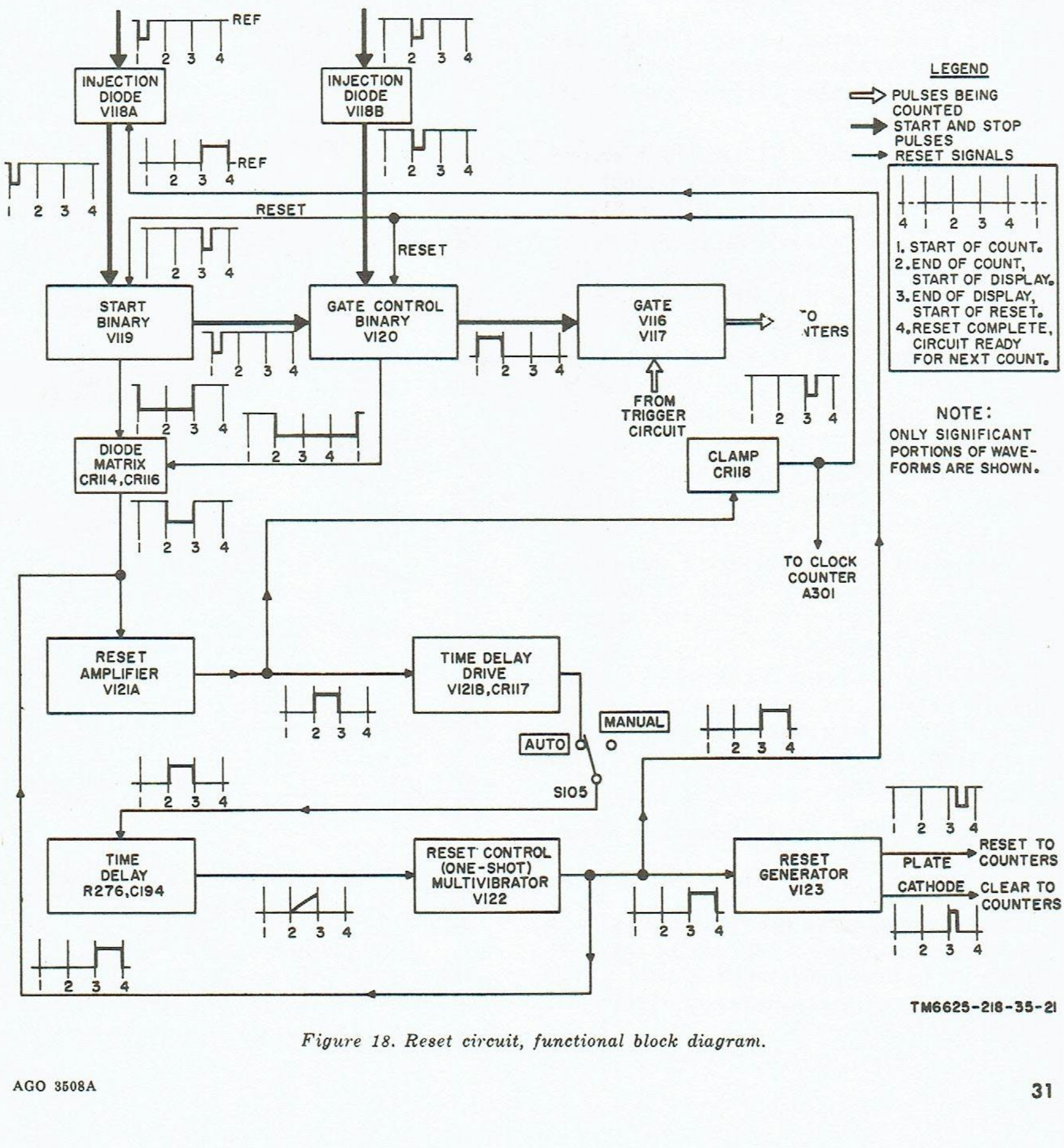


Figure 18. Reset circuit, functional block diagram.

and recycle the gate control circuit. This condition must persist only during the resetting cycle.

(4) Clock counter assembly A 301 is reset for the next counting interval. Unlike the 1-mc and 100-kc counters, however, the clock counter circuit is reset to a count of nine instead of to a count of zero (par. 25*f*).

b. Major Circuit Elements. The major circuit elements which make up the reset circuitry are illustrated in the functional block diagram (fig. 18), and consist of the following:

(1) Diode matrix network CR114 and CR116, which receives the final output of start binary V119 and gate control binary V120.

(2) Reset amplifier V121A, which receives two separate and distinct input signals at discrete intervals (par. 31).

(3) Cathode follower V121B and signal-passing diode CR117, which function together as a driving source for the time delay circuit.

(4) AUTO-MANUAL switch S105, which is assumed to be in the AUTO position throughout the discussion in paragraph 31.

(5) The time delay circuit, which is made up of DISPLAY TIME control R276 and charging capacitor C194.

(6) Reset control (one-shot) multivibrator stage V122, which develops an output pulse used in driving three elements in the reset circuit.

(7) Reset generator V123, which initially develops the clearing voltage and, an instant later, the zero resetting voltage for the 1-mc and 100-kc counter assemblies.

31. Reset Circuit, Block Diagram Signal Paths

(figs. 18 and 19)

The functional block diagram (fig. 18) and the idealized waveforms (fig. 19) of the reset circuit use a time scale which is vital to the understanding of the sequence of events discussed in this paragraph.

a. Time Scale. The time scale used is an arbitrary one, but is essential for purposes of discussion. It consists of four divisions, as follows:

(1) Time 1 represents the start of the counting interval.

(2) Time 2 represents the end of the counting interval and the beginning of the display period. This display period is variable, depending on the setting of the DISPLAY TIME control (R276, fig. 20). Limits of this control range from less than 1 second to more than 5 seconds. During this period, the Nixie indicators retain the count, with their metallic numerals glowing.

(3) Time 3 represents the end of the display period and the start of the reset

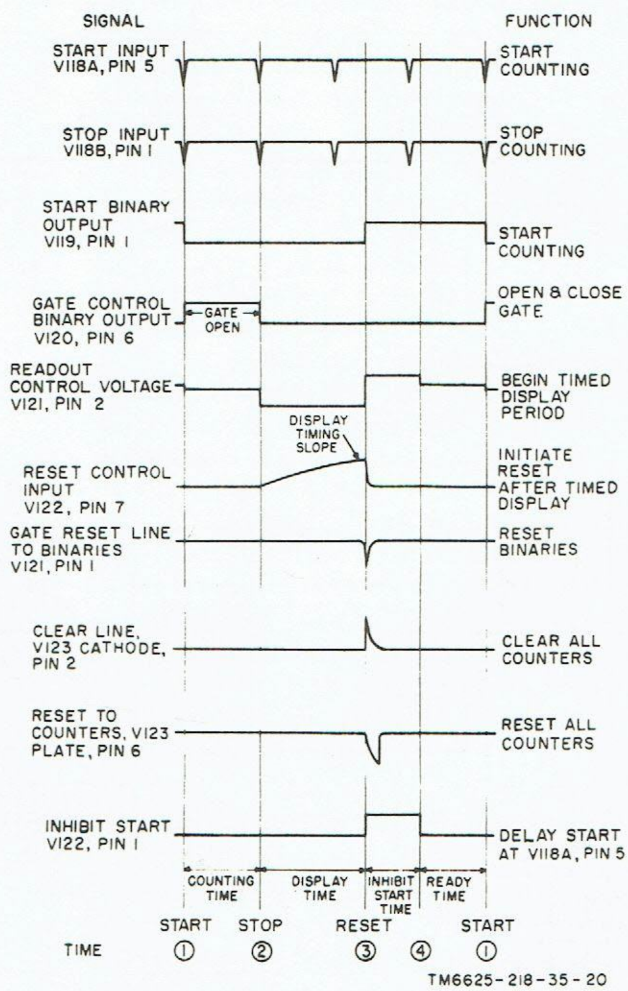


Figure 19. Reset control circuit, idealized waveforms.

cycle. The display is reset to zero during time 3 and 4.

(4) Time 4 represents the completion of the reset cycle. Circuits in the frequency counter are ready for the next counting period after time 4.

b. Signal Tracing. Based on the arbitrary time scale described in *a* above, the following actions occur. The waveforms shown in the block diagram (fig. 18) are superimposed on the arbitrary time scale; those shown in the idealized waveform chart (fig. 19) are more representative of the actual voltages existing at the designated circuit points.

(1) At time 1, the pulse from the selected timing circuit in the clock pulse generator (or from T.I.M. START jack in the T.I.M. position of S103), passes through injection diode V118A, and reverses the initial condition of start binary V119. As described in paragraph 28, the output transient of V119 causes a flip-flop action in gate control binary V120.

(2) At time 2, the stop timing pulse from the selected timing circuit in the clock pulse generator (or from T.I.M. STOP jack J103 in the T.I.M. position of S103) passes through injection diode V118B, and restores gate control binary V120 to its initial condition. During the time interval from 1 to 2 (figs. 18 and 19), the output voltage from V120 opens gate stage V116. This action permits signals from the trigger circuit (fig. 2) to pass through to the counters, with the count registering on the Nixie indicator tubes.

(3) A voltage obtained from the plate, pin 1, of start binary V119 is of negative polarity from time 1 until V119 is reset at time 3.

(4) A voltage obtained from the plate, pin 6, of gate control binary V120 is of negative polarity from time 2 (when the counting interval ends) until the next counting interval begins at time 1.

(5) A diode matrix (fig. 18), consisting of signal-passing diodes CR114 and CR116, provides a negative output voltage from time 2 until time 3. This interval is the period when the outputs of V119A and V120B are negative.

(6) The negative output of the diode matrix is amplified and inverted by reset amplifier V121A. The V121A positive output (from time 2 to 3) is coupled to the time delay drive circuit consisting of V121B (a cathode follower) and diode CR117. This positive output voltage is coupled through the AUTO contact of AUTO-MANUAL switch S105 to the time delay circuit of R276 and C194. Depending on the setting of DISPLAY TIME control R276, the voltage across charging capacitor C194 rises at a slow or fast rate.

(7) At the completion of the resistance-capacitance time-constant period (time 3), reset control stage V122 is triggered through S106A (fig. 20). This stage, a one-shot multivibrator, produces a positive output pulse which lasts from time 3 (the end of the display period) to time 4 (the completion of the reset cycle). This output pulse drives three circuits:

(*a*) The positive output of V122 triggers reset generators V123 (fig. 21) into conduction. This stage immediately develops one output of positive polarity (the clear pulse) at its cathode and, less than 1 microsecond later, a second output of negative polarity (the reset pulse) at its plate. The positive output clears the electron beam in the 1-mc and all five 100-kc counters. The negative output resets the electron beam in all of the counters to the zero position (par. 12*b*).

(*b*) The positive output of V122 is simultaneously applied to the input of reset amplifier V121A where the signal is amplified and inverted into a negative output. This negative output has no effect on negatively biased cathode follower V121B in the time delay drive circuit. However, the negative-going output voltage is applied as a reset signal to clock counter A 301 and to binaries V119 and V120 in the gate control circuit. Diode CR118 is a clamp that assures that only the negative output from reset amplifier V121A is coupled into the clock counter and binary circuits.

(c) The positive output of V122 is simultaneously applied to injection diode V118A. This diode is normally biased negatively and couples negative pulses to start binary V119 during a counting interval. However, for a period of approximately 10 milliseconds after time 3 (the end of the display period), diode V118A must be inhibited from passing timing signals to the gate control circuit. This is accomplished by driving the cathode of the diode highly positive (approximately 50 volts with respect to ground) to prevent the start of another counting period prematurely.

32. Reset Circuit, Stage-by-stage Analysis

a. Review of Binaries V119 and V120 (fig. 17). The input signal to the reset circuit is developed by the condition of start binary V119 and gate control binary V120. Three conditions of the binaries must be considered in this analysis, as follows:

(1) Binary V119 in its normal or precount state, with V120 also in its normal or precount state. This condition exists at the start of each counting interval.

(2) Binary V119 in its reversed state, with V120 also in its reversed state. This condition exists during a counting interval (par. 27).

(3) Binary V119 in its reversed state, with V120 restored to its normal or precount state. This condition exists after each counting interval, since the suppressor grid of gate stage V116 is driven negative to prevent the input signal from passing to the 1-mc and 100-kc counters.

b. Signal Passing Diodes CR114 and CR116. Diode CR114 (fig. 17) is connected from V119A plate, pin 1, to the readout control line. Diode CR116 is connected from V120B plate, pin 6, to the same readout control line. One diode (CR114) receives the output of binary V119A, which is in its *reversed* condition during a counting interval. The second diode (CR116) receives the output of V120B, which is in its *normal* condition at the end of a counting interval. Because of the circuit arrangement of the diodes, the following actions occur:

(1) In the normal or precount condition, the readout control line is maintained positive by start binary V119 and diode CR114.

(2) During the counting interval, the readout control line is maintained positive by gate control binary V120 and diode CR116.

(3) After the counting interval, however, neither diode is able to hold the readout control line positive. It is at this instant that the negative voltage from the —120-volt supply (connected through R285) causes the line to go negative. This instant marks the beginning of the readout period.

(4) The negative voltage from R285 exists on the readout control line until a positive output pulse from reset control stage V122 (fig. 18) overrides the negative potential. When this happens, the readout control line becomes positive again, and is maintained positive because start binary V119 is reset to its normal state by the time the V122 output has disappeared.

c. Detailed Analysis. On the basis of *a* and *b* above, the reset circuit can be analyzed with reference to the triggering of reset amplifier V121. This stage serves two separate and distinct functions during the reset cycle. Paragraph 33 gives a detailed analysis of V121.

33. Reset Amplifier V121
(fig. 20)

a. Amplifier Input Signal. Stage V121A amplifies and inverts the negative voltage which exists on the readout control line at the beginning of the readout period (par. 32*b*(3)). The negative signal is coupled through resistor R267 to the grid, pin 2, of V121A. The resulting positive signal (developed across plate load resistor R268) is dc coupled through resistor R269 to the grid, pin 7, of cathode follower V121B. Resistor R269 serves as the dc coupling path; R271 couples a fixed negative bias voltage to the grid.

b. Amplifier Output Signal. The positive signal produced across V121B cathode load resistor R274 is coupled through R273, CR117, AUTO-MANUAL switch S105 (AUTO position), and DISPLAY TIME control R276 to charging capacitor C194. Diode CR117 is part of a voltage-divider network, consisting of resistors R274, R273, and R275, which is connected between the —120-volt power supply and chassis ground. Diode CR118 prevents the positive signal at the plate of reset amplifier V121A from appearing on the gate reset line at this instant.

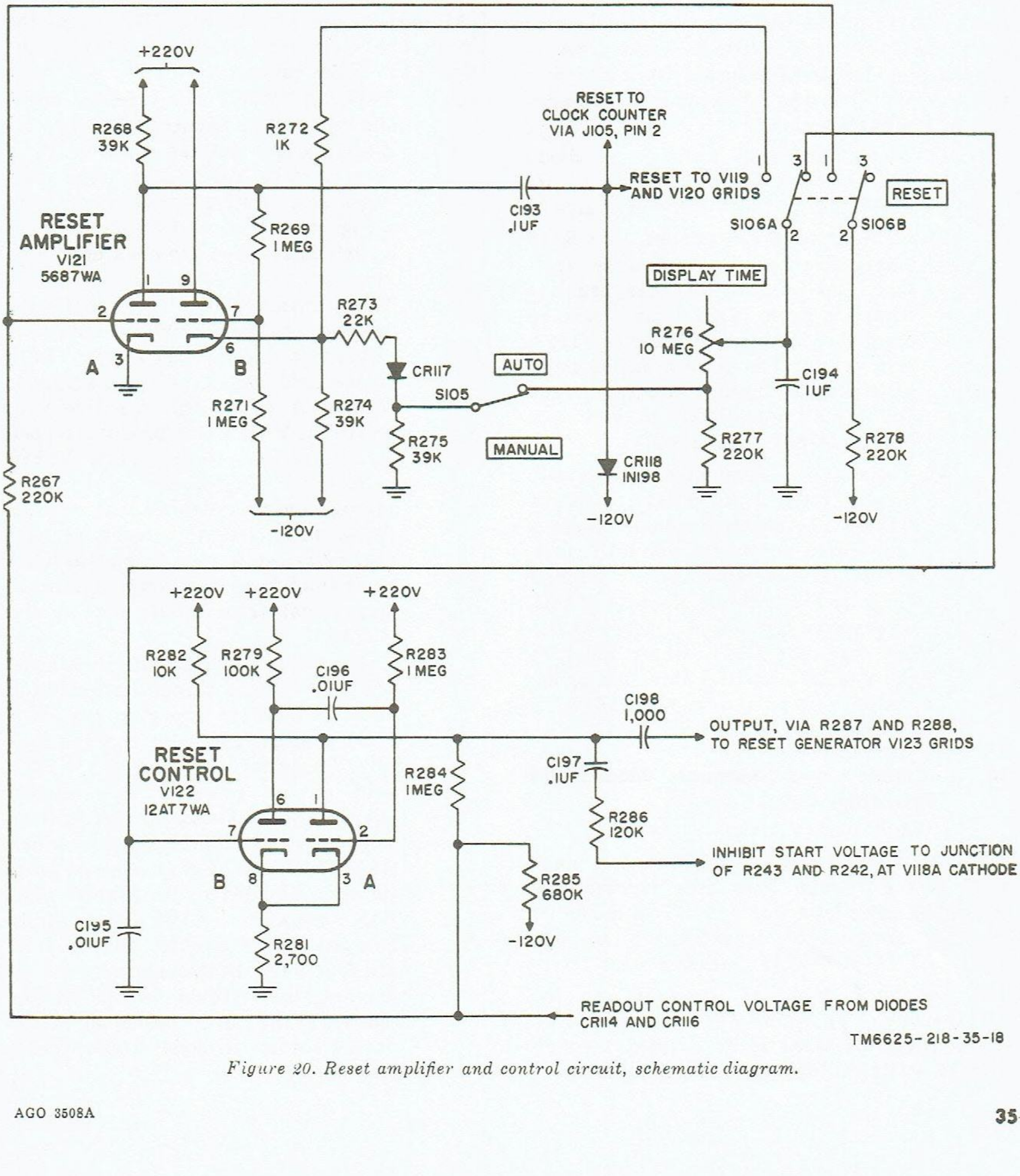


Figure 20. Reset amplifier and control circuit, schematic diagram.

Diode CR118 clamps the gate reset line to the —120-volt supply. The diode low forward resistance bypasses the positive output pulse from V121A, and the negative polarity of the gate reset line is not disturbed.

c. Gate Reset Line. At the instant the negative voltage on the readout control line ends (par. 32*b*(4)), a negative transient appears at the plate of V121A. This transient is coupled through capacitor C193 to the gate reset line. Diode CR118 allows this negative transient to be coupled to the desired circuits, while preventing the previous positive output from affecting the gate reset line. The following is an explanation of the diode action:

(1) Under quiescent conditions, diode CR118 is conducting because of its connection to the —120-volt source.

(2) A negative pulse applied to CR118 biases this diode in the reverse direction, and assures that the negative transient from V121A plate will be coupled to the grids of binaries V119A and V120A. The same negative pulse is dc coupled through connector J105 and its mating plug P301 to reset clock counter A 301 (par. 25*f*(3)).

(3) The negative transient at V121A plate is also coupled to cathode follower V121B. The negative signal voltage is reproduced across cathode load resistor R274, but also biases coupling diode CR117 to cutoff. Because of this, no negative signal ever reaches charging capacitor C194, which must be charged in a positive direction to accomplish its purpose in the DISPLAY TIME circuit.

34. Automatic and Manual Modes of Operation

(fig. 20)

The signal that triggers reset control stage V122 is the voltage that rises expotentially across charging capacitor C194. Two modes of operation are possible, depending on the position of AUTO-MANUAL switch S105.

a. Automatic Mode of Operation. In the AUTO mode of operation, the voltage built up across capacitor C194 is dc coupled through RESET switch C106A to the grid, pin 7, of V122. RESET switch S106 is a spring-loaded type, and is shown in its normal position. Under this condition, V122B is triggered when the voltage across capacitor C194 reaches a predetermined level. The time required to charge C194 to this level is determined by the setting of DISPLAY TIME control R276. Paragraph 35 describes the circuit action after V122 is triggered.

b. Manual Mode of Operation. In the MANUAL mode of operation, switch S105 opens the circuit line from reset amplifier V121 to the DISPLAY TIME control.

(1) Pressing RESET switch S106A opens the circuit line between charging capacitor C194 and the input to reset control stage V122. This action prevents reset control stage V122 from being triggered until the RESET switch is released from its depressed position.

(2) When switch S106 is held in its depressed position, S106B couples the —120-volt line through resistor R278 to the grid, pin 2, of reset amplifier V121A. Applying this negative voltage to the V121A grid produces a positive pulse that is coupled to V121B grid, pin 7. The positive pulse is reproduced across cathode load resistor R274. (The action is identical with that described in paragraph 33*b* when reset amplifier V121A receives a negative signal from diodes CR114 and CR116.)

(3) The positive pulse at V121B cathode, pin 6, is coupled through attenuating resistor R272 to charging capacitor C194, and the capacitor charges rapidly. Capacitor C195, in the V122B grid circuit prevents any sudden changes, due to switching action, from triggering V122 prematurely. When RESET switch S106 is released from its spring-loaded to its normal position, capacitor C194, now fully charged, is reconnected to the grid, pin 7, of V122. In this manner the conduction that would ordinarily be reached at the end of the display period during automatic mode of operation is duplicated.

(4) Manual resetting of the equipment is possible during the automatic mode of operation. This is true because of the connection of the grid, pin 2, of gate control binary V120A to the gate reset line. A manually initiated reset produces exactly the same conditions that normally exist at time 3 (fig. 18) in the automatic mode. This change in the condition of gate control binary V120A can be obtained at any instant of the automatic cycle.

35. Reset Control Stage V122, Circuit Analysis

Reset control stage V122 is a monostable multivibrator. In its stable state, the A section is conducting, and the B section is cut off. This is determined by the connection of +220 volts dc to the grid of the A section, pin 2, through resistor R283. Plate load resistors for the B and A sections, respectively, are R279 and R282. The two sections have a common cathode resistor, R281.

a. Feedback Loop. As the voltage developed across capacitor C194 rises, the potential at the grid of V122B, pin 7, begins to rise. When the grid voltage rises sufficiently to cause conduction of this section, the voltage at the plate, pin 6, drops. This negative voltage change is coupled through capacitor C196 to the grid of V122A, pin 2. The resulting decrease in plate current through V122A is reflected in a drop in the voltage developed across R281. This change in voltage is equivalent to a voltage rise at the grid of V122B and positive feedback action is achieved through the common cathode resistor.

b. V122B Conducting, V122A Cut Off. The regenerative process proceeds rapidly until V122A is completely cut off and V122B is conducting fully. The entire process of reversing the condition of this circuit takes place very rapidly, with the result that a positive pulse is developed at the plate of V122A, pin 1. This pulse, approximately 50 volts in amplitude, is used to drive three circuits in the reset cycle.

(1) The positive pulse passes through dc coupling resistor R284 to drive reset amplifier V121A. The resulting negative output of V121A plate, pin 1, causes the resetting of clock counter A 301 and gate control binaries V119 and V120 (par. 33*c*(2)).

(2) The positive pulse is also fed through coupling capacitor C197 and signal dropping resistor R286 to the junction of resistors R241 and R242, at injection diode V118A cathode (fig. 17). Here the positive voltage pulse prevents another counting interval from starting until reset control stage V122 has returned to its initial condition. Injection diode V118A cannot pass timing signals from the clock pulse generator as long as its cathode is positive. Because of this inhibit start pulse, all of the reset transients are given time to decay completely before a new counting interval begins.

(3) A third path for the positive output pulse of V122A is through coupling capacitor C198 to grid resistors R287 and R288, in reset generator V123. This signal path is described in detail in paragraph 36.

c. Return to Stable State, V122A Conducting and V122B Cut Off. The discharge path for coupling capacitor C196 is through grid return resistor R283 to the +220-volt supply line. When C196 discharges sufficiently, the A section of reset control stage V122 begins to con-

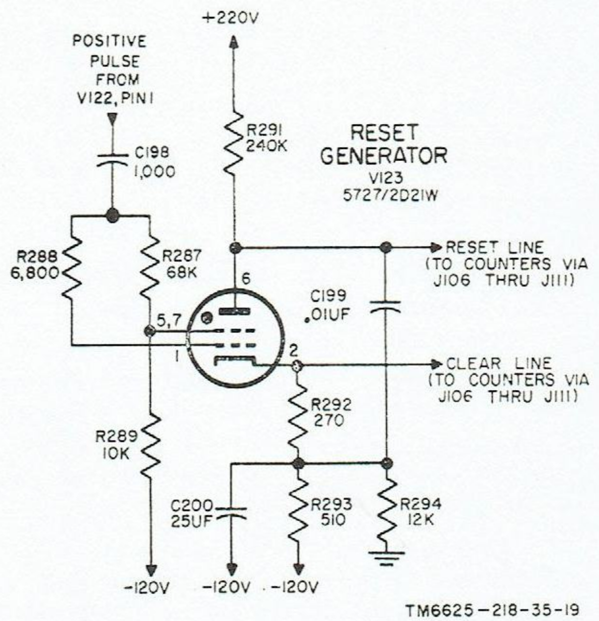


Figure 21. Reset generator V123, schematic diagram.

duct again, with a corresponding increase in the voltage drop across common cathode resistor R281. Stage V122B is soon restored to cutoff (while stage V122A is conducting fully) until the next charging voltage from delay time capacitor C194 starts the cycle again.

36. Reset Generator V123

(fig. 21)

Reset generator V123 is a gas-filled thyratron which is normally cut off by the negative 120-volt supply voltage applied through resistor R289 to the screen grid, pins 5 and 7, and through resistors R287 and R288 to the control grid, pin 1. The cathode, pin 2, is tied (through R292) to the junction of voltage-divider resistors R293 and R294. The cathode potential is less negative than the grid potential. Capacitor C200 bypasses low-frequency variations to ground. The series combination of resistors R292 and R294 make up the cathode resistor. Resistor R291 is the plate load resistor. Capacitor C199, connected between the plate and cathode, is the charging capacitor for the output signal developed at the plate, pin 6.

a. At the start of the reset cycle, a positive pulse of approximately 50-volt amplitude is coupled from the plate, pin 1, of reset control stage V122 through capacitor C198 and resistors R287 and R288 to the grids of reset generator V123. This incoming pulse is sufficient in amplitude to overcome the grid-to-cathode bias of V123 and the thyratron fires. With a heavy flow of current through V123, the potential at V123 cathode, pin 2, increases to a large positive value. This positive spike is applied to the 1-mc and all five of the 100-kc counters as a clearing voltage. It effectively destroys the electron beam within each of the beam switching tubes (par. 12*b*).

b. As capacitor C199 discharges through resistor R292, the spike at the cathode, pin 2, rapidly disappears. Simultaneously, the potential at V123 plate drops rapidly and produces a negative pulse on the reset line to the counter assemblies. This action resets the counters, and their associated Nixie indicators, to zero (par. 12*b*(2)).

c. When capacitor C199 has discharged sufficiently, the current through reset generator V123 becomes too small to maintain ionization, and V123 ceases to conduct. Capacitor C199 then recharges to the B+ potential through plate resistor R291.

37. Power Supply

(fig. 22)

a. General. The power supply provides dc outputs of +220, +180, +120, —60, and —120 volts. Three ac outputs of 6.3 volts are produced by the secondary windings of transformers T101 and T102.

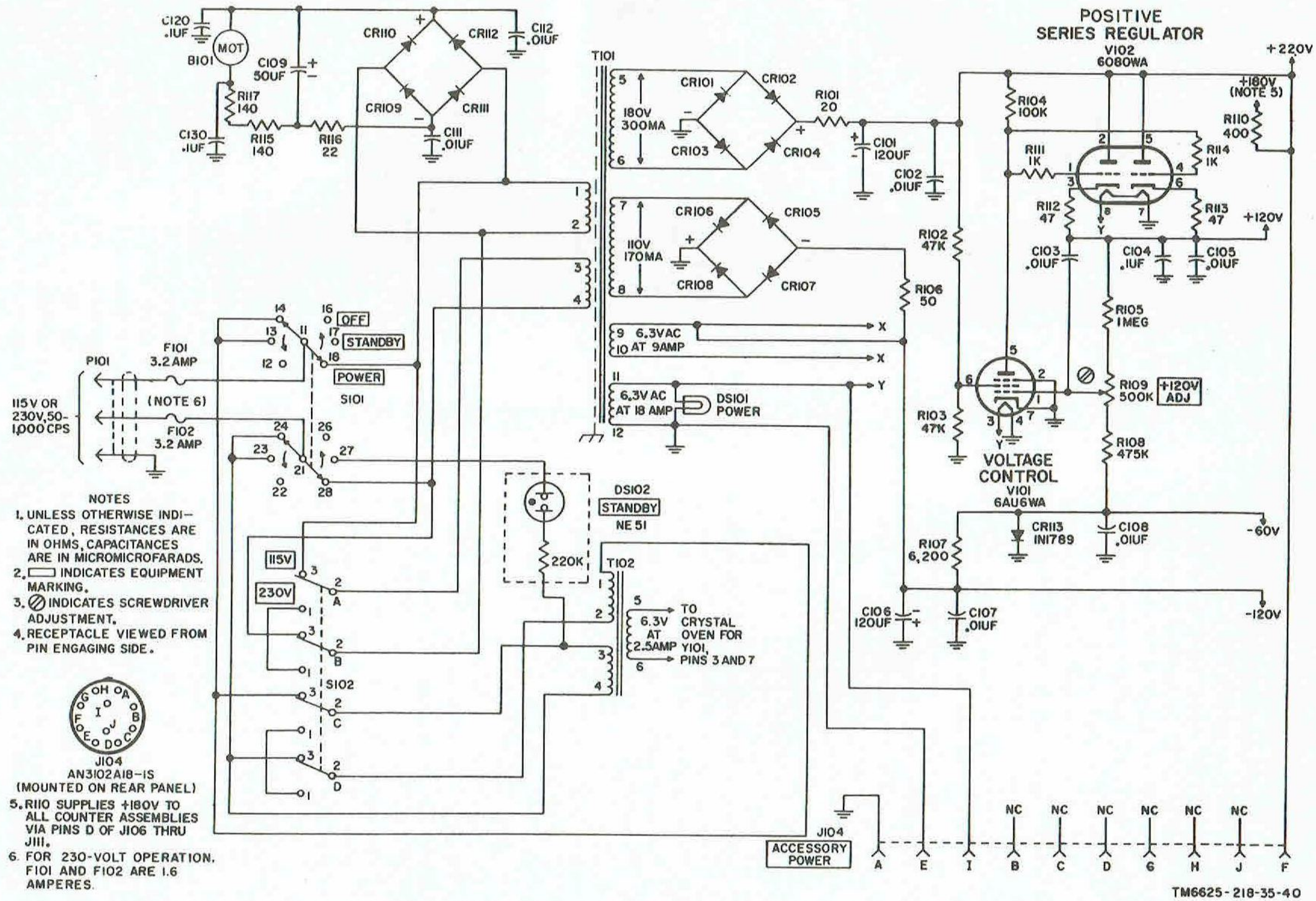
b. 115-volt or 230-volt Operation. Either 115-volt or 230-volt source power can be used by the frequency meter, depending on the position of 115V–230V switch S102 on the rear panel. When S102 is in the 115V position, source power is applied to both primaries of T101 in parallel, and to both primaries of T102 in parallel. When S102 is in the 230V position, source power is applied to both primaries of T101 in series, and to both primaries of T102 in series. In 115-volt operation, 3.2-ampere fuses are used; in 230-volt operation, 1.6-ampere fuses are used.

c. Standby Condition. When switch S101 is in the STANDBY position, source power is supplied to the primary windings of transformer T102 (*b* above) and 115 volts ac is applied to the STANDBY indicator lamp. The secondary of T102 supplies 6.3 volts ac to the crystal oven and XTAL OVEN ON lamp (par. 17*a*).

d. Power Condition. When switch S101 is in the POWER position, source power is supplied to the primaries of both T101 and T102, and to the blower motor circuit. Source power is removed from the STANDBY indicator lamp.

e. Circuit Description. The detailed circuit analysis below describes the circuit with POWER-STANDBY-OFF switch S101 in the POWER position.

(1) *Blower motor circuit.* With 115V-230V switch S102 in its 115V position, the 115-volt ac power connected to terminals 1 and 2 of transformer T101 is also applied to the full-wave bridge consisting of rectifiers CR109 through CR112. With the 115V-230V switch in the 230V position, the primary windings of T101 (terminals 1–2 and terminals 3–4) of T101 are in



NOTES

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROMICROFARADS.
2. ▭ INDICATES EQUIPMENT MARKING.
3. ⊘ INDICATES SCREWDRIVER ADJUSTMENT.
4. RECEPTACLE VIEWED FROM PIN ENGAGING SIDE.
5. R110 SUPPLIES +180V TO ALL COUNTER ASSEMBLIES VIA PINS D OF J106 THRU J111.
6. FOR 230-VOLT OPERATION, F101 AND F102 ARE 1.6 AMPERES.

Figure 22. Power supply, schematic diagram.

series. The primaries then function as an autotransformer to provide 115-volt input across terminals 1 and 2 to the bridge rectifier. The rectified dc voltage, filtered by capacitor C109 and resistor R116, is used to drive blower motor B101. Resistors R115 and R117 are voltage-limiting resistors. Capacitors C111, C112, C120, and C130, are radio-interference filters. The voltage across the motor terminals is approximately 110 volts dc.

(2) *Positive output circuit.* The ac voltage developed across terminals 5 and 6 of T101 is applied to the full-wave bridge consisting of rectifiers CR101 through CR104. The negative side of the bridge is grounded; the positive output of the bridge is applied through protective resistor R101 to filter capacitor C101. Capacitor C102 is a high-frequency bypass. The +220-volt line is applied to the plates of the Nixie tubes, clock counter tubes V301 through V304, and to V119 through V123 in the gate control and reset circuits. Resistor R110 drops the line voltage to provide a +180-volt potential to the 1-mc and the five 100-kc counter assemblies. The +180 volts is also applied to the cathodes of the Nixie tubes. Stages V101 and V102 provide a regulated +120-volt potential for the clock pulse generator (V103-V111) and the input trigger channel circuits (V112, V113, V114, and V116). Voltage control V101 is a dc voltage amplifier whose output is dc coupled to positive series regulator tube V102. Tube V102 is connected in series between the +220-volt line and the +120-volt output line. The effective change in resistance of V102 keeps the 120-volt line voltage constant. The regulated —60-volt output is used as a reference voltage. Resistors R105, R109, and R108 from a voltage divider between the +120-volt output line and the —60-volt output line. Regulating action is as follows:

(*a*) The voltage at the grid, pin 1, of V101, depending on the setting of R109, is slightly negative. If the +120-volt output line varies, approximately one-third of this change in potential is applied to the grid of V101. This error voltage is amplified and inverted by V101, and applied to grids, pins 1 and 4, of V102. This action changes the current flow through V102 to oppose the original voltage error, and restores the plus 120-volt output to the correct value.

(*b*) Resistors R111 and R114 prevent parasitic oscillations in V102. Cathode resistors R112 and R113 help keep the current balanced between the two sections of dual-triode V102. If either half of the tube begins to draw more than half the current, the additional current through R112 or R113 increases the negative bias of that section. This circuit arrangement increases the current in the half of the tube that has too little current and decreases the current in the half of the tube that has too much current. The final result is that the currents in each half are essentially balanced.

(*c*) Capacitor C103 couples any sudden variations in the +120-volt line to the V101 grid. These sudden variations in the feedback loop are nearly three times greater than the dc error voltage available at the arm of R109 and are therefore effective in reducing ripple on the +120-volt line.

(3) *Negative 120-volt output circuit.* The ac voltage developed across terminals 7 and 8 of T101 is applied to a full-wave bridge consisting of rectifiers CR105 through CR108. The positive side of the bridge is grounded and the negative output of the bridge is connected through protective resistor R106 to the —120-volt unregulated dc line. Capacitor C106 filters this output voltage; C107 is a high-frequency ac bypass. The output of the unregulated —120-volt supply is ap-

plied to the gate reset and readout control lines, the cathodes of V118A and V118B, the grids and cathodes of V119, V120, V121, and V123, the cathodes and grids of clock counter stages V301 through V304, and the cathodes of all tubes (including beam switching tubes) on the counter assemblies.

(4) *Negative 60-volt output circuit.* Resistor R107 drops the —120-volt output at the junction of resistor R106 and filter capacitor C106 to —60 volts. Zener diode CR113 is a regulator similar in operation to a gaseous voltage regulator tube. The Zener diode has a critical voltage below which negligible current is drawn by the diode. At this critical point, the diode begins to draw current. The amount of current drawn increases rapidly with very small increases in applied voltage. As an example, if the output of the —120-volt line should change due to variations in ac line voltage or in the load by 10 percent, or 12 volts, the current through resistor R107 will change by approximately 2 milliamperes. The voltage across Zener diode CR113 will change by approximately .2 volt to adjust the current drawn by CR113 by 2 milliamperes. In this way, the output across Zener diode CR113 is held relatively constant despite large variations in the unregulated —120-volt line. Because of the fast response time of the Zener diode, the regulating action eliminates ripple, and no filter capacitor is needed. Capacitor C108 is an ac bypass for exceptionally sharp transients. The output of the regulated negative 60-volt supply is applied to the grid of gate V116, the cathode of input amplifier stage V112, and to a voltage divider in the plate circuit of V114.

(5) *X-x heater circuit.* Terminals 9 and 10 of transformer T101 provide 6.3 volts ac heater power for all tubes on the 1-mc and 100-kc counter assemblies, as well as for reset generator V123. This filament voltage is superimposed on the —120-volt supply to eliminate the danger of arc-over from adjacent cathodes operating near the —120-volt level.

(6) *Y-to-ground heater circuit.* Terminals 11 and 12 of transformer T101 provide 6.3 volts ac heater power for the heaters of all other tubes in the equipment, as well as for POWER indicator lamp DS101.

(7) *Accessory power circuit.* A parallel output of T101, terminals 11 and 12, at 6.3 volts ac, and a parallel output of the +220-volt line are connected to ACCESSORY POWER jack J104, at the rear panel. The jack is a convenient means of connecting operating power to any accessory equipments which may need these ac and dc potentials.

CHAPTER 2

TROUBLESHOOTING

***Warning:* When servicing the frequency meter, be careful not to contact the B+ voltages (from —120 volts to +220 volts dc). Even with ac power removed, high dc potentials may still be retained as charges on capacitors. Before touching exposed parts, short them to ground. Be especially careful when checking the ac input circuits at fuseholders XF101 and XF102, at terminals board TB104, and at the terminals of POWER-STANDBY-OFF switch S101.**

38. General Instructions

Troubleshooting at field and depot maintenance level includes all the techniques outlined for organizational maintenance and any special or additional techniques required to isolate defective parts. The field and depot maintenance procedures are not complete in themselves but supplement the procedures described in TM 11–6625–218–12. The systematic troubleshooting procedure, which begins with the operational and sectionalization checks that can be performed at an organizational level, must be completed by means of sectionalizing, localizing, and isolating techniques.

39. Troubleshooting Procedures

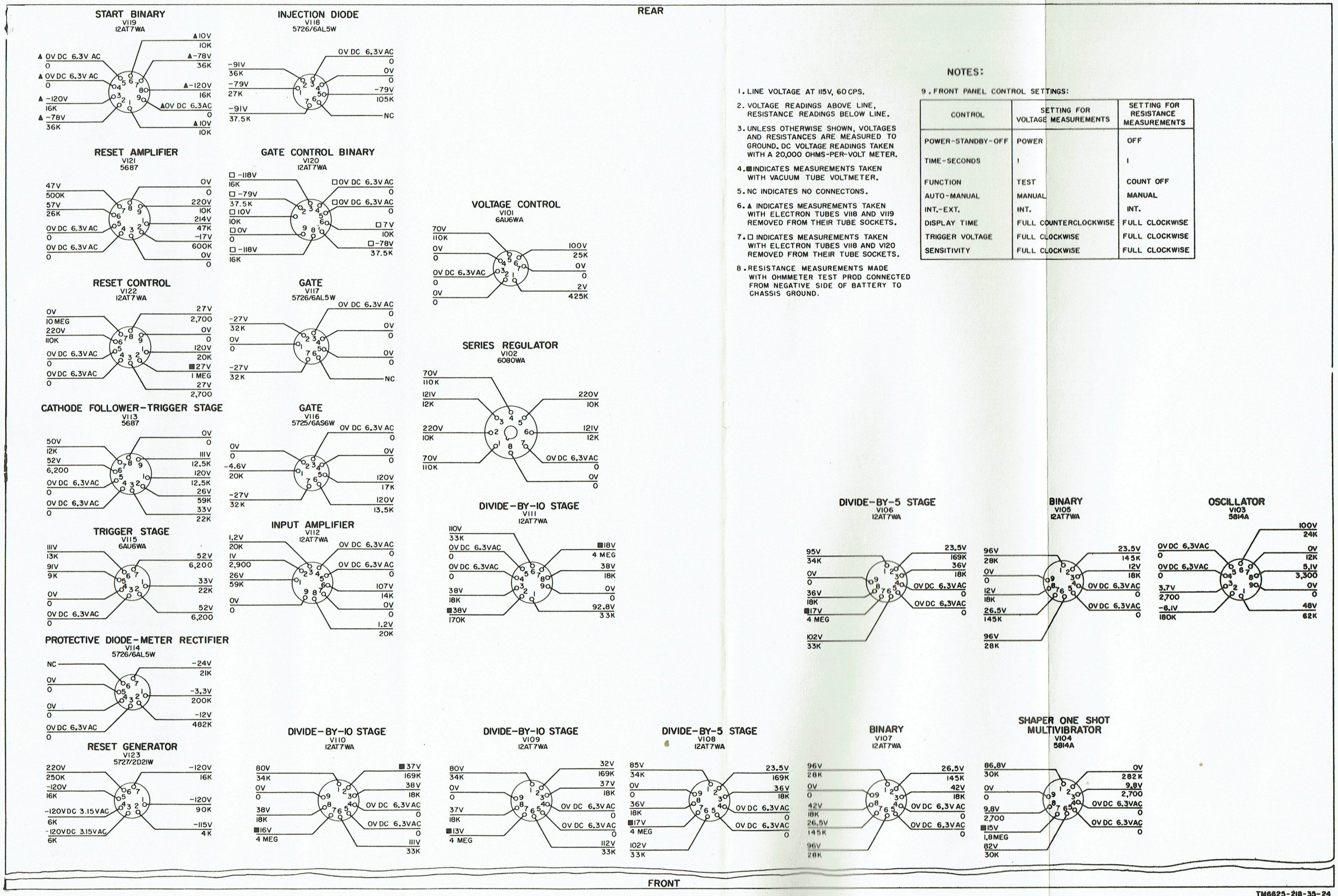
a. General. The first step in servicing a defective frequency meter is to sectionalize the fault. Sectionalization means tracing the fault to the major assembly or circuit responsible for the abnormal operation. The second step is to localize the fault. Localization means tracing the fault to a defective part responsible for the abnormal condition. Some faults, such as burned-out resistors or rectifiers, arcing, shorted transformers, etc., often can be located by sight, smell, and hearing. The majority of faults, however, must be localized by signal substitution and by checking voltages and resistances.

b. Sectionalization and Localization. The tests listed below aid in isolating the source of trouble. To be effective, the procedures should be followed in the order given. First localize the trouble to a single stage or circuit. Then isolate the trouble within that stage or circuit by appropriate voltage, resistance, and continuity measurements. The service procedure is summarized as follows:

(1) *Visual inspection.* Visual inspection enables the repairman to locate faults without testing or measuring circuits. This inspection is valuable in avoiding additional damage to the frequency meter which might occur through improper servicing methods, and also in forestalling future failures. Power-off visual inspection checks are given in paragraph 27 of TM 11–6625–218–12. With power-on, visual inspection often enables the repairman to locate tubes with open filaments and gassy tubes which give off a bluish-purple glow.

(2) *Resistance measurements.* The use of resistance measurements to locate trouble will prevent further damage to the equipment if possible short circuits are present. To assist in the localization of such faults, troubleshooting data include the normal resistance values as measured at the tube sockets and at key terminal points. The normal resistance values at any point can be determined by referring to the resistance values shown in diagrams (fig. 23-26) or by the resistor color code (fig. 40). Before making any resistance measurements, turn off the power.

(3) *Voltage measurements.* Most troubles either result from abnormal voltage or produce abnormal voltages. Normal voltages at tube sockets and key ter-

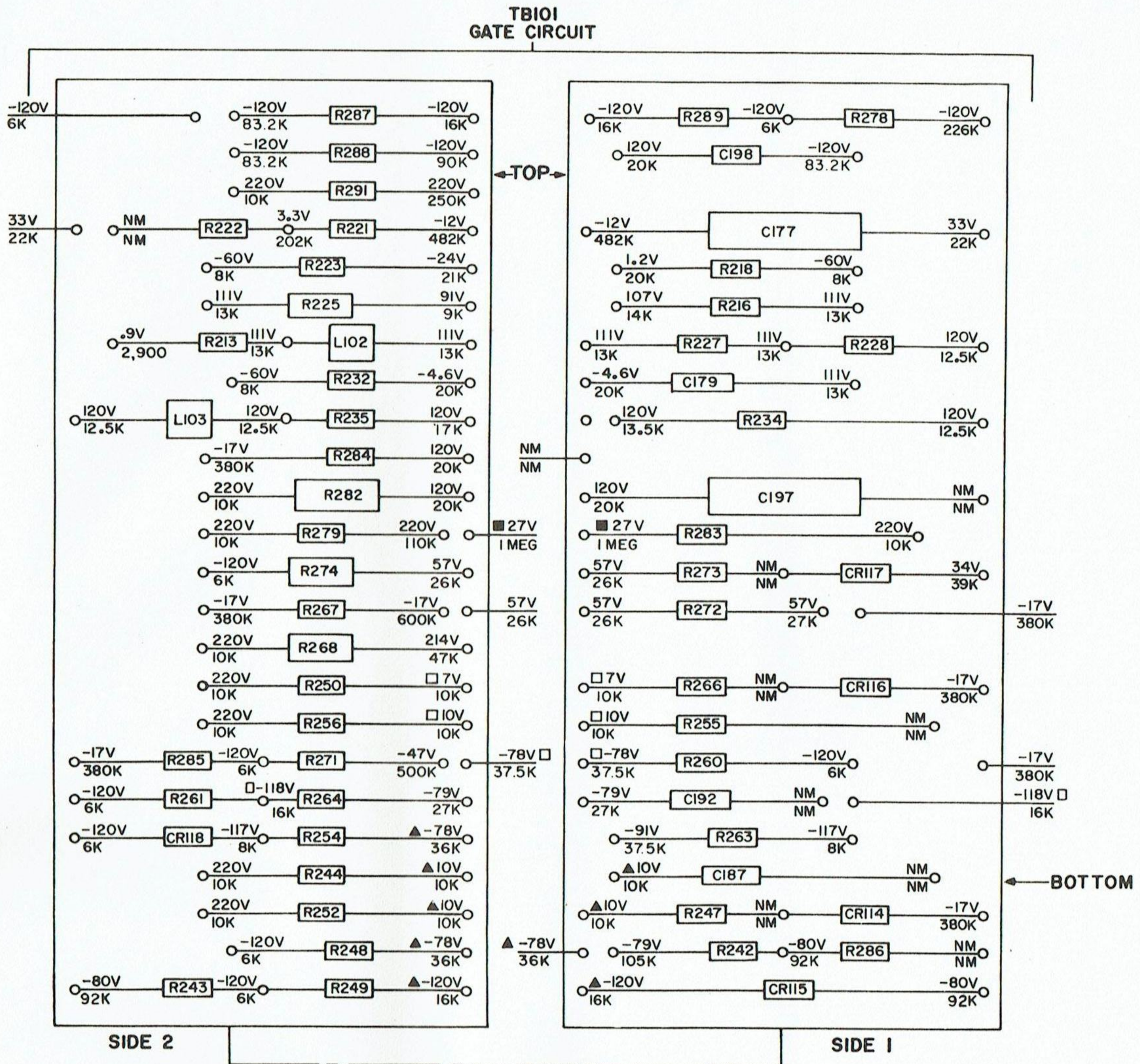


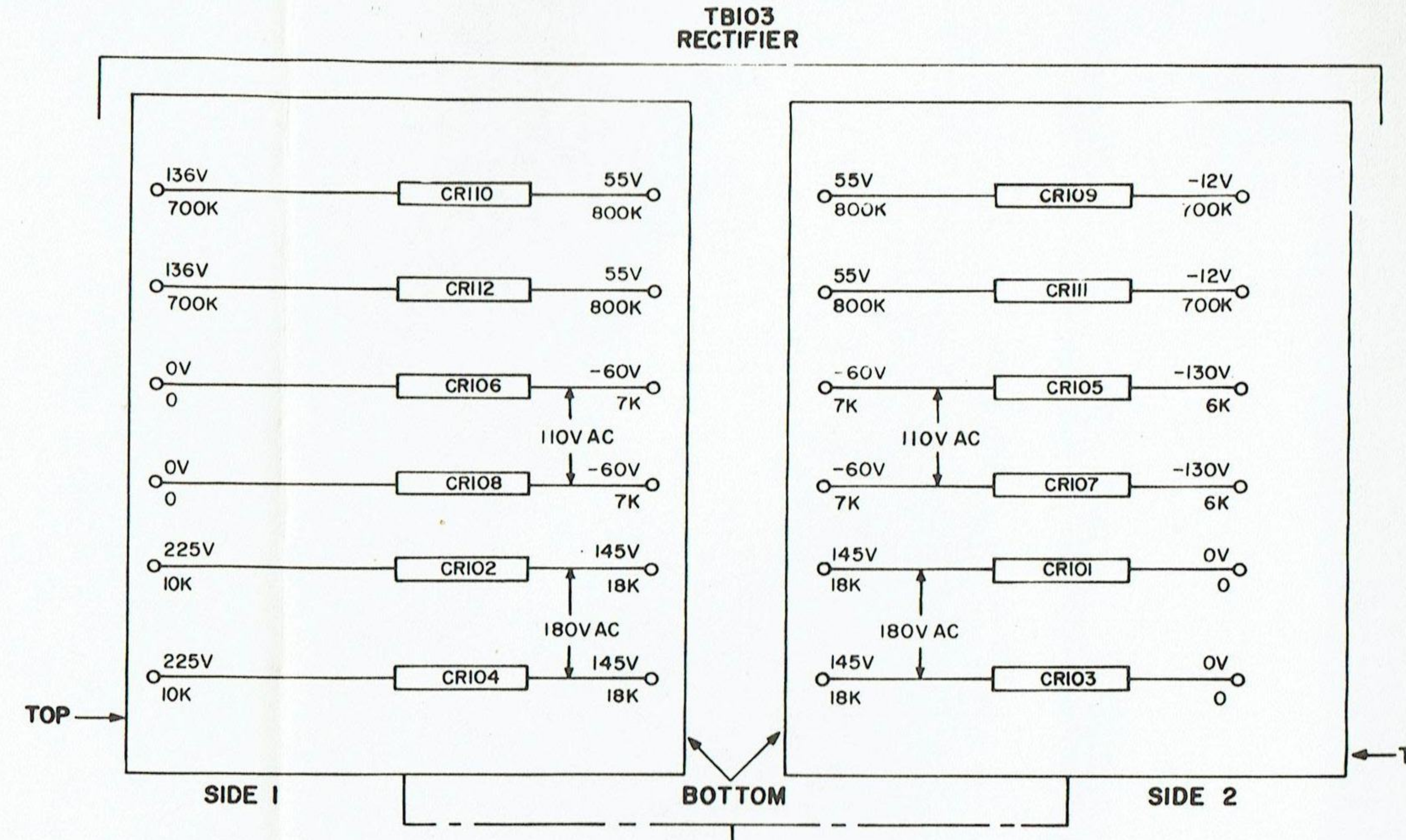
NOTES:

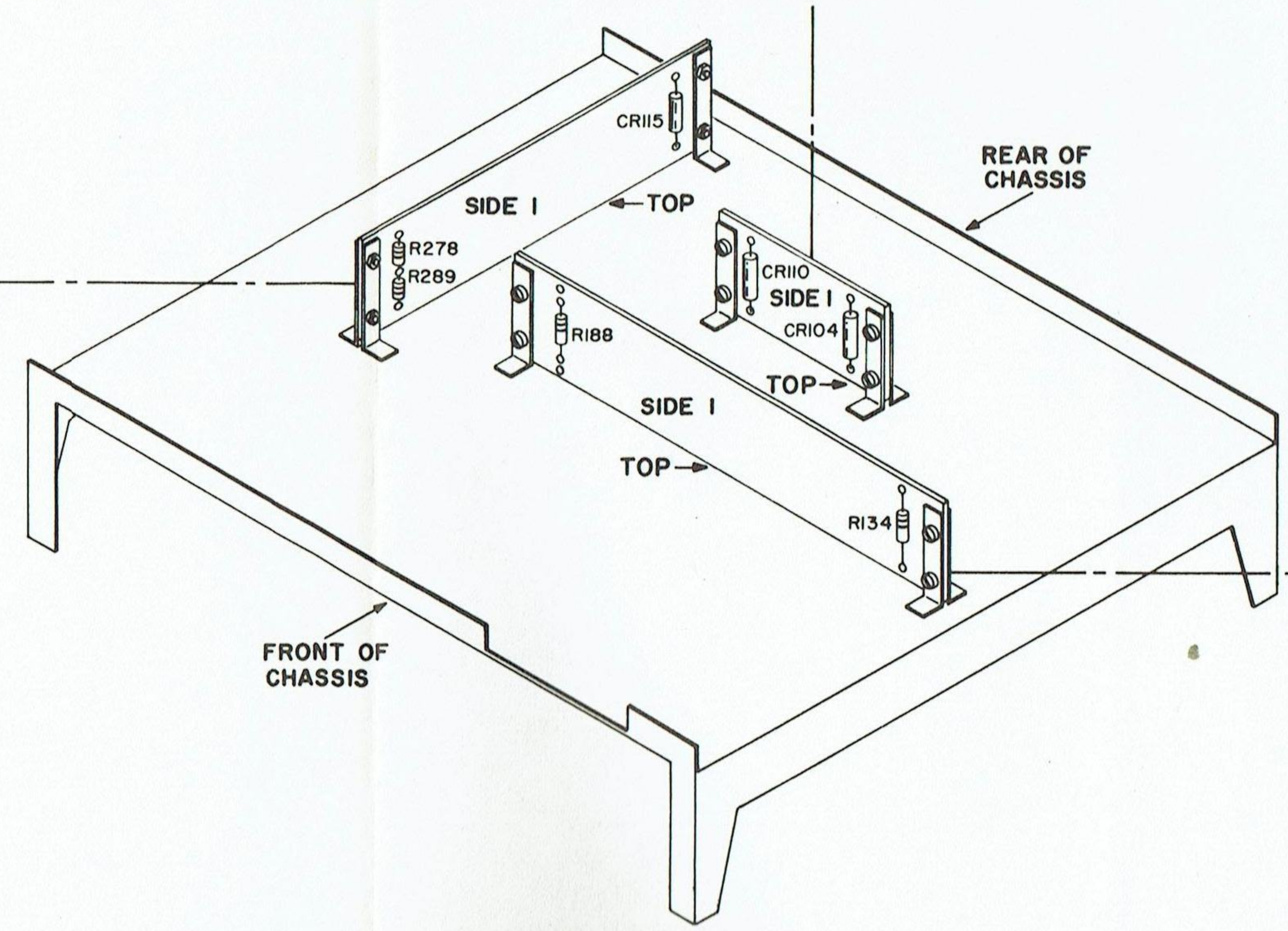
1. LINE VOLTAGE AT 115V, 60 CPS.
2. VOLTAGE READINGS ABOVE LINE, RESISTANCE READINGS BELOW LINE.
3. UNLESS OTHERWISE SHOWN, VOLTAGES AND RESISTANCES ARE MEASURED TO GROUND. DC VOLTAGE READINGS TAKEN WITH A 20,000 OHMS-PER-VOLT METER.
4. ■ INDICATES MEASUREMENTS TAKEN WITH VACUUM TUBE VOLTMETER.
5. NC INDICATES NO CONNECTONS.
6. ▲ INDICATES MEASUREMENTS TAKEN WITH ELECTRON TUBES V118 AND V119 REMOVED FROM THEIR TUBE SOCKETS.
7. □ INDICATES MEASUREMENTS TAKEN WITH ELECTRON TUBES V118 AND V120 REMOVED FROM THEIR TUBE SOCKETS.
8. RESISTANCE MEASUREMENTS MADE WITH OHMMETER TEST PROD CONNECTED FROM NEGATIVE SIDE OF BATTERY TO CHASSIS GROUND.
9. FRONT PANEL CONTROL SETTINGS:

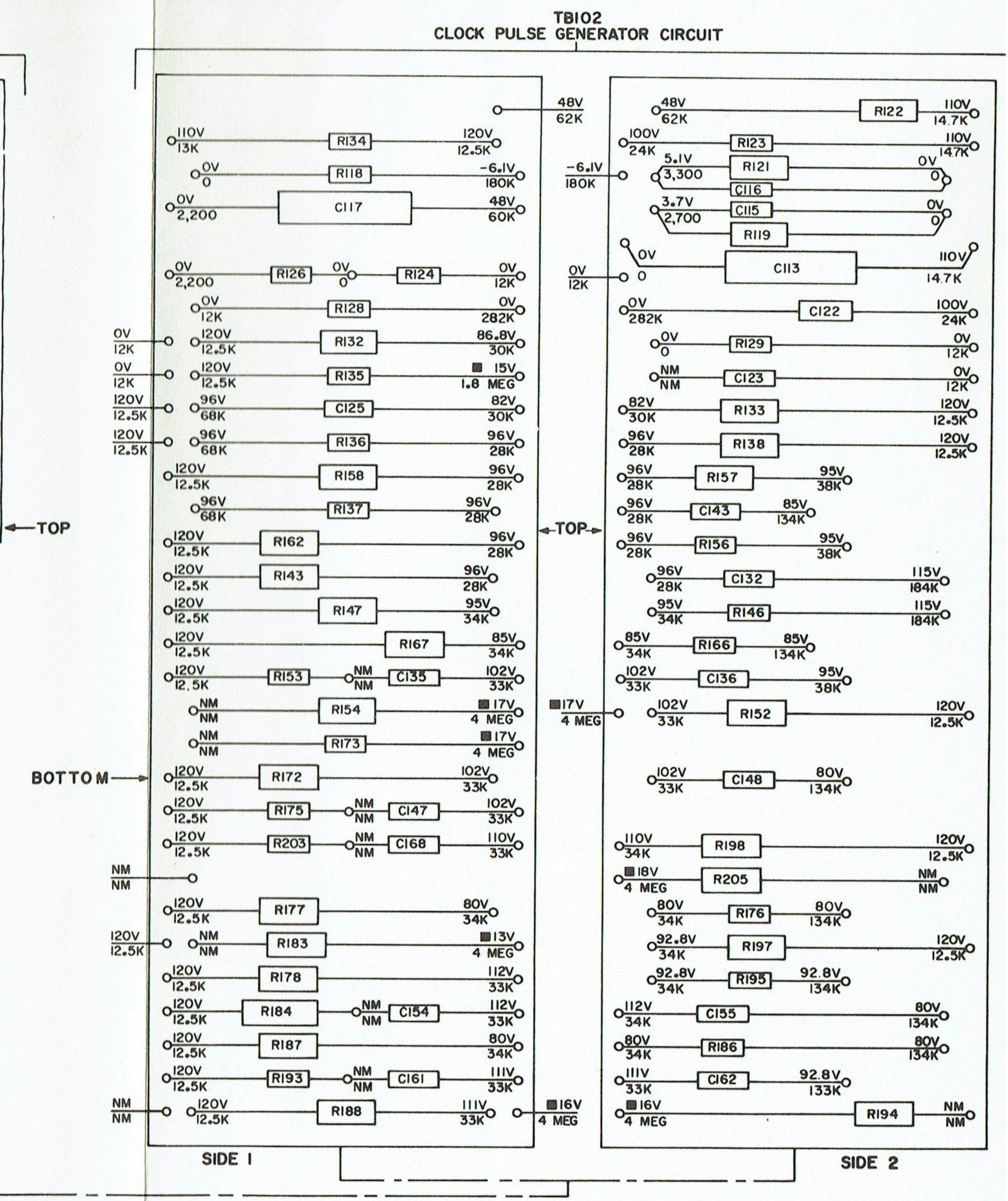
CONTROL	SETTING FOR VOLTAGE MEASUREMENTS	SETTING FOR RESISTANCE MEASUREMENTS
POWER-STANDBY-OFF	POWER	OFF
TIME-SECONDS	1	1
FUNCTION	TEST	COUNT OFF
AUTO-MANUAL	MANUAL	MANUAL
INT.-EXT.	INT.	INT.
DISPLAY TIME	FULL COUNTERCLOCKWISE	FULL CLOCKWISE
TRIGGER VOLTAGE	FULL CLOCKWISE	FULL CLOCKWISE
SENSITIVITY	FULL CLOCKWISE	FULL CLOCKWISE

Figure 23. Tube socket voltage and resistance diagram, main chassis, bottom view.









NOTES

1. LINE VOLTAGE AT 115V, 60 CPS.
2. VOLTAGE READINGS ABOVE LINE, RESISTANCE READINGS BELOW LINE.
3. UNLESS OTHERWISE SHOWN, VOLTAGES AND RESISTANCES ARE MEASURED TO GROUND. DC VOLTAGE READINGS TAKEN WITH A 20,000 OHMS-PER-VOLT METER.
4. NM INDICATES NOT MEASURED (READINGS HAVE NO SIGNIFICANCE).
5. ▲ INDICATES MEASUREMENTS TAKEN WITH ELECTRON TUBES V118 AND V119 REMOVED FROM THEIR TUBE SOCKETS.
6. □ INDICATES MEASUREMENTS TAKEN WITH ELECTRON TUBES V118 AND V120 REMOVED FROM THEIR TUBE SOCKETS.
7. ■ INDICATES MEASUREMENTS TAKEN WITH VACUUM TUBE VOLTMETER.
8. ALL RESISTANCE MEASUREMENTS TAKEN WITH OHMMETER TEST PROD CONNECTED FROM NEGATIVE SIDE OF BATTERY TO CHASSIS GROUND.
9. TOP SIDES OF TERMINAL BOARDS ARE CLOSEST TO CHASSIS; BOTTOM SIDES CLOSEST TO VIEWER, WITH EQUIPMENT AS ILLUSTRATED.
10. FRONT PANEL CONTROL SETTINGS.

CONTROL	SETTINGS FOR VOLTAGE MEASUREMENTS	SETTINGS FOR RESISTANCE MEASUREMENTS
POWER-STANDBY-OFF	POWER	OFF
TIME-SECONDS	1	1
FUNCTION	TEST	COUNT OFF
AUTO-MANUAL	MANUAL	MANUAL
INT.-EXT.	INT.	INT.
DISPLAY TIME	FULL COUNTER-CLOCKWISE	FULL CLOCKWISE
TRIGGER VOLTAGE	FULL CLOCKWISE	FULL CLOCKWISE
SENSITIVITY	FULL CLOCKWISE	FULL CLOCKWISE

Figure 24. Voltage and resistance diagram, terminal boards TB101 through TB103.

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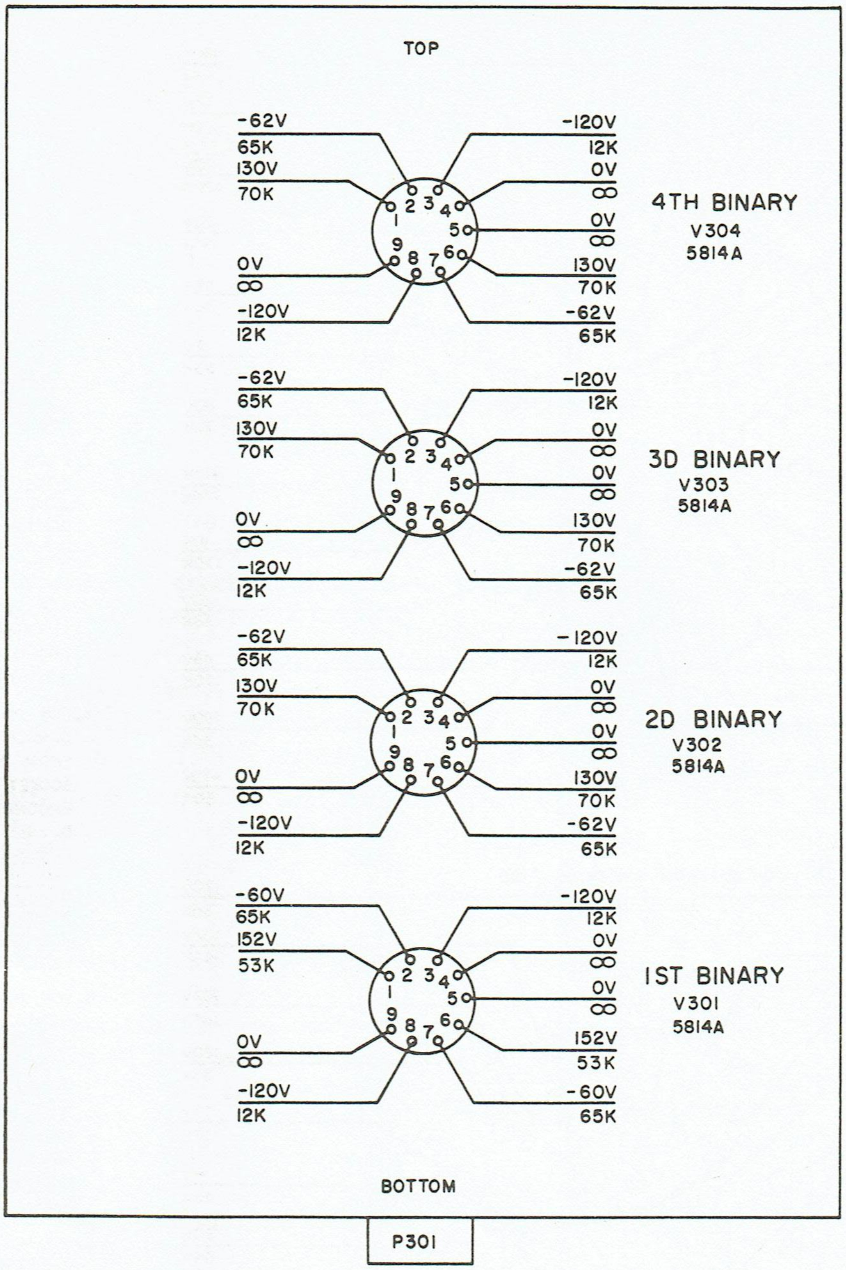

NOTES:

1. LINE VOLTAGE AT 115V, 60 CPS.
2. RESISTANCE READINGS BELOW LINE, VOLTAGE READINGS ABOVE LINE.
3. VOLTAGES ARE MEASURED AS FOLLOWS:
   A. CLOCK COUNTER ASSEMBLY A 301 IS AS PLUGGED INTO MATING JACK J105, ON MAIN CHASSIS.
   B. TUBES V301 THROUGH V304 ARE REMOVED FROM TUBE SOCKETS. VOLTAGES ARE TAKEN FROM TOP OF TUBE SOCKETS TO CHASSIS GROUND.
   C. [POWER]-[STANDBY]-[OFF] SWITCH IS IN [POWER] POSITION.
   D. [INT.]-[EXT.] SWITCH IS IN [INT.] POSITION.
4. RESISTANCES ARE MEASURED BY REMOVING CLOCK COUNTER ASSEMBLY A 301 FROM MAIN CHASSIS. ALL MEASUREMENTS ARE FROM INDICATED POINTS TO SHORTED PINS 2,4,6, AND 8 OF CONNECTOR P301.

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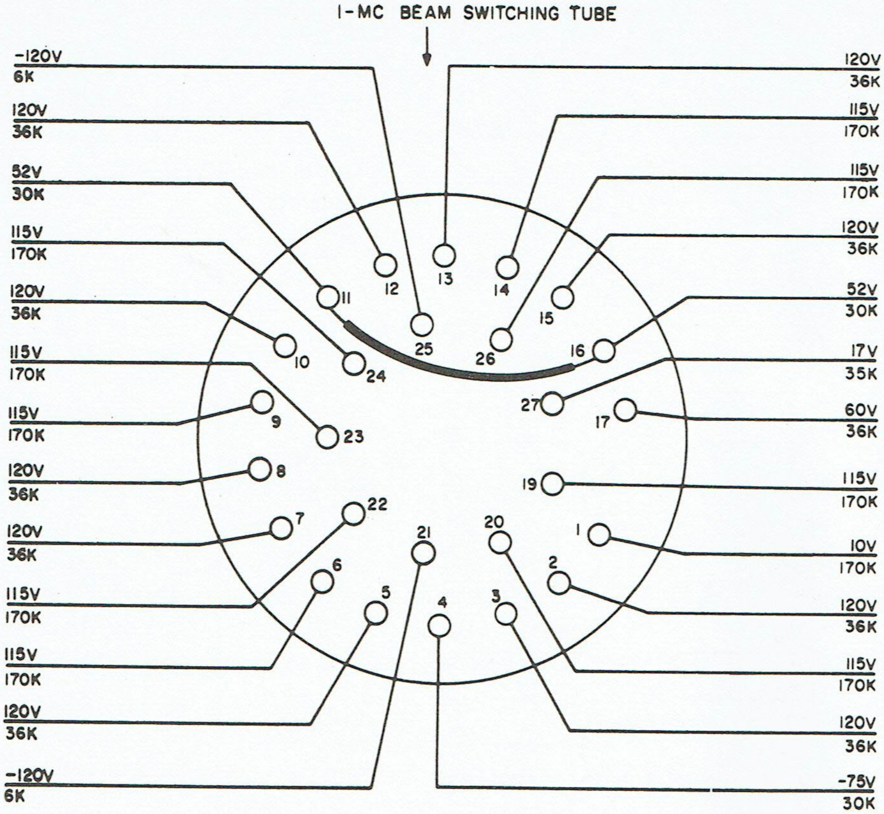
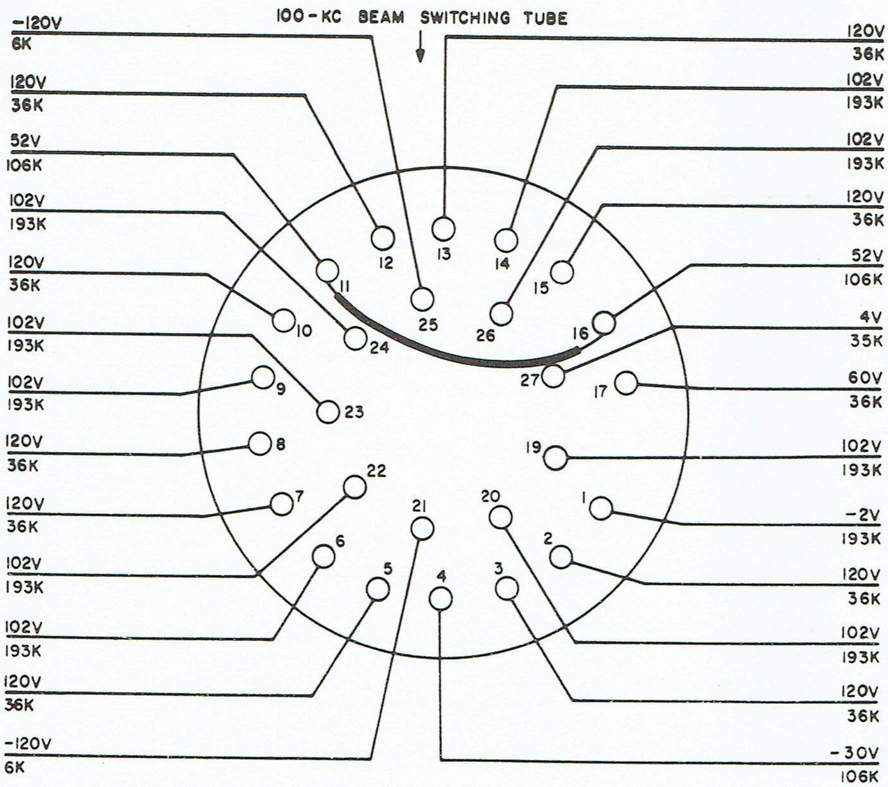
Figure 25. Voltage and resistance diagram, clock counter assembly A 301.





NOTES:

1. VOLTAGE READINGS ABOVE LINE; RESISTANCE READINGS BELOW LINE.
2. EACH COUNTER IS PLUGGED INTO ITS MATING RECEPTACLE J106 THROUGH J111, AT BOTTOM OF MAIN CHASSIS.
3. NIXIE TERMINAL BOARD CONNECTORS P401 THROUGH P406 ARE PLUGGED INTO PRINTED TERMINALS AT TOPS OF PRINTED CIRCUIT BOARDS A501, A601 THROUGH A605.
4. FOR VOLTAGE MEASUREMENTS:
   A. VOLTAGE IS MEASURED FROM INDICATED TUBE SOCKET PIN TO CHASSIS GROUND.
   B. LINE VOLTAGE IS 115V, 60CPS.
   C. POWER-STANDBY-OFF SWITCH IN POWER POSITION.
   D. INT.-EXT. SWITCH IS IN INT. POSITION.
   E. 20,000 OHMS-PER-VOLT METER USED.
5. FOR RESISTANCE MEASUREMENTS:
   A. RESISTANCE IS MEASURED FROM INDICATED TUBE SOCKET PIN TO THE COMMON +180-VOLT LINE, AVAILABLE AT UNUSED PIN C ON EACH CONNECTOR P401 THROUGH P406.
   B. POWER-STANDBY-OFF SWITCH IN OFF POSITION.
6. ALL VOLTAGE MEASUREMENTS TAKEN WITH "O" NUMERAL ON NIXIE INDICATOR TUBE LIT.
   A. SAME READINGS WILL BE OBTAINED AT CORRESPONDING SPADES AND TARGETS IF ANY OTHER NUMERAL ON NIXIE INDICATOR IS ILLUMINATED.
   B. READINGS AT GRID TERMINALS 4 AND 16 WILL BE REVERSED WHEN AN ODD NUMERAL ON THE NIXIE INDICATOR IS LIT.
7. PIN NO. 18 DOES NOT EXIST ON TUBE BASE.

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Figure 26. Voltage and resistance diagram, beam switching tubes.

minal points are shown on figures 23 through 26. Compare readings taken with normal readings shown.

(4) *Operational tests.* Operational tests frequently indicate the general location of trouble. In many instances, the results of the tests will determine the exact nature of the fault. The equipment performance checklist in paragraph 28 in TM 11–6625–218–12 is a good operational test.

(5) *Troubleshooting chart.* The trouble symptoms listed in this chart (par. 42) will aid in localizing trouble.

(6) *Intermittent troubles.* In all these tests, the possibility of intermittent troubles should not be overlooked. If present, this type of trouble often can be made to appear by tapping or jarring the equipment. Gently move the wiring to check for loose connections, and tap the components with an insulated tool such as a fiber rod. It is possible that the trouble is not in the frequently meter itself, but in the installation (mounting, loose or damaged cables, the equipment under test, etc.). Always be sure the installation is satisfactory before troubleshooting the frequency meter.

(7) *Signal substitution.* The principal advantage of the signal substitution method (par. 43) is that it usually enables the repairman to localize a trouble accurately and quickly to a particular stage when the preceding tests have not been successful. An audio oscillator, a multimeter, and an oscilloscope are items of test equipment that can be used in the signal substitution procedures applicable to this equipment.

40. Test Equipment Required

The following chart lists the test equipment required for troubleshooting the frequency meter. Associated technical manuals and assigned common names are also listed.

Test equipment	Technical manual	Common name
Audio Oscillator TS–382A/U	TM 11–2684A	Audio oscillator
Oscilloscope OS–8A/U	TM 11–1214	Oscilloscope
Test Set, Electron Tube TV–7/U	TM 11–5083	Tube tester
Electronic Multimeter TS–505A/U	TM 11–5511	Vtvm
Multimeter AN/URM–105	TM 11–6625–203–12	Multimeter

41. Checking B+ and B— Circuits for Shorts

a. When to Check. When any of the following conditions exist, check for short circuits and clear the troubles before applying power:

(1) When the nature of the trouble symptom is not known.

(2) When abnormal symptoms reported from operational tests indicate possible power-supply troubles.

(3) When the plastic insulation on filament wiring on the underside of the chassis shows evidence of melting or charring. This condition usually indicates a short circuit in filament wiring or an internal short in the heaters of electron tubes.

b. Conditions for Tests. To prepare for the short-circuit tests, proceed as follows:

(1) Remove the top and bottom cover plates from the frequency meter (par. 27*b*, TM 11–6625–218–12).

(2) Do not plug in the power cord while taking short-circuit measurements.

(3) Remove electron tubes V101 and V102 from their sockets.

c. Measurements. Make the resistance measurements indicated in the chart below. More than 20 percent difference from readings in the chart should be considered abnormal. If abnormal readings are obtained, perform the additional isolating procedures listed in the chart. When the faulty part is found, repair the trouble before applying power to the unit. When replacing faulty rectifiers or tubes in the power supply, always check for shorted filter capacitors. Frequently a faulty filter capacitor will cause the rectifier to go bad. In such cases, replace the faulty capacitor before installing the new rectifier.

Note. Be sure to connect the negative test prod of the multimeter to chassis ground for checking the positive power supplies. Reverse the test prods for checking the negative power supplies.

Point of measurement (to ground)	Normal indication	Isolating procedure
Pin 6 of V101	25K	Check R102, R103.
Pin 5 of V101	110K	Check R104.
Pin 1 of V101	425K	Check C103, R105, R109, and R108.
Pin 2 or pin 5 of V102	10K	If resistance is high, check R110 for open circuit. If resistance is low, check CR101 through CR104. If resistance is zero, check C101 and C102 for shorts.
Pin 1 or pin 4 of V102	110K	Check R111 or R114, respectively, if pin 5 or V101 checked out satisfactorily.
Pin 3 or pin 6 of V102	12.5K	Check R112 or R113, respectively. If resistance is very low, check C104 and C105 for shorts. Check decoupling capacitor C178.
Negative terminal of capacitor C108	8K	If resistance is very low, diode CR113 may be defective. Check C108 for short. If resistance is approximately 5,000 ohms, check R107 for short. If resistance is very high, check R107 for open circuit.
Negative terminal of capacitor C106	6K	If resistance is very low, check C106 and/or C107 for short. Check CR105 through CR108. If resistance is over 10K, check R107 for open circuit.

42. Troubleshooting Chart

The troubleshooting chart is designed to supplement the operational checks in TM 11–6625–218–12. Proceed with the steps of the checklist until a symptom of trouble appears.

***Caution:* If operational symptoms indicate the possibility of short circuits within the frequency meter, make the short-circuit tests in paragraph 41*c* before applying power to the unit.**

Symptom	Probable trouble	Correction
1. With POWER-STANDBY-OFF switch in STANDBY, STANDBY and XTAL OVEN ON lamps do not light.	No ac power is applied to the frequency meter.	Check for input voltage. Check line cord.
	Fuse F101 or F102 is open	Replace fuse. If the replacement fuse blows, check for short circuit at S101 or in T102. *Note.* Check to see that fuses of correct rating for the source voltage are in use and that the 115V-230V switch is in correct position.
2. STANDBY and XTAL OVEN ON lamps light, but XTAL OVEN ON lamp does not cycle off and on after suitable warmup.	Crystal oven or DS103 lamp defective; T102 defective.	Replace defective part.

Symptom	Probable trouble	Correction
3. With POWER-STANDBY-OFF switch in POWER position, POWER lamp does not light. Blower motor operates.	POWER lamp defective	Replace POWER indicator lamp.
	T101 secondary defective	Replace T101.
4. Same as above but blower motor is inoperative.	F101 or F102 open	If replacement fuse blows, check V101, V102, T101, C109, C112, and C120. Make short-circuit tests listed (par. 41*c*).
	T101 defective	Replace T101.
5. POWER indicator lamp lights, but blower motor fails to operate.	Blower motor B101 defective	Replace defective part.
	Resistor R115, R116, or R117 open. Diodes CR109 through CR112 defective.	
6. POWER indicator lamp and blower motor operate, but numerical indicators do not light or are erratic.	If all numerical indicators are out, check R110 and +220-volt output of power supply.	Replace R110.
		Check 220-volt output from power supply to Nixie tube board assembly (fig. 29).
		Check tubes V101 and V102.
	If one or more numerical indicators light, trouble is in unlighted numerical indicators, in an associated resistor on the Nixie tube board assembly, or in the associated counter assembly.	Replace unlighted numerical indicators.
		Check associated resistors on the Nixie tube board assembly (par. 44).
		Replace associated counter assembly.
		Check wiring and connections.
7. Lighted numerical indicators cannot be reset to zero by RESET switch.	Reset generator stage inoperative	Check tube V123. Replace defective part in reset generator stage.
8. When RESET switch is operated, all numerical indicators register zero but no further action takes place.	Clock pulse generator or gate control circuitry defective.	Check that AUTO-MANUAL switch is in AUTO position.
		Check that INT.-EXT. switch is in INT. position.
		Check tubes and associated parts in clock pulse generator and in gate control binary V120.
9. Numerical indicators do not cycle in either position of AUTO-MANUAL switch.	TRIGGER VOLTAGE control R214 incorrectly set or defective.	Adjust or replace R124.
10. Same as symptom 9 and FUNCTION switch in TEST position, INPUT LEVEL meter does not deflect to green area (near center) of scale.	Oscillator, input amplifier, or cathode follower stage V113A defective.	Check V103, Y101, C119 and associated components.
		Check V112 and V113 stages and associated components.
11. Same as symptom 9 but INPUT LEVEL meter does deflect to green area of scale.	Defect in clock pulse generator stages V104 through V111, gate control stage V120, or trigger stage V115 or V113B.	Replace defective tube or associated part.

Symptom	Probable trouble	Correction
12. Oscillator fails to tune to 100 kc	Crystal Y101 defective	Replace Y101 (par. 32, TM 11-6625-218-12).
	C114 has changed value	Replace C114.
	FREQ. ADJ. C119 misalined or defective.	Adjust C119 (par. 55); replace if necessary.
13. Numerical indicators do not count correctly in TEST position of FUNCTION switch.	One or more TIME BASE ADJUSTMENTS incorrectly set.	Adjust TIME BASE ADJUSTMENTS (par. 17*e*, TM 11-6625-218-12).
14. Resetting of all TIME BASE ADJUSTMENTS does not produce correct indications in TEST position of FUNCTION switch.	+120V ADJ R109 incorrectly adjusted.	Adjust R109 for +120 volts output (par. 54).
	V101, V102, or associated part defective.	Replace defective tube or part.
	Divide-by-5 stage V106 defective	Replace V106 or defective associated part.
	Potentiometer R155, R174, R185, R196, or R204 defective.	Replace defective potentiometer.
	Dropping resistor R165 or R190 defective.	Replace defective part.
	Defective tube in clock pulse generator (V103 through V111).	Replace defective tube.
	Defective FUNCTION switch S103	Replace S103.
15. Count is correct for shorter counting intervals but incorrect for longer counting intervals. (FUNCTION switch in TEST position.)	Stage producing shortest *incorrect* counting interval is defective.	Replace defective tube or part in faulty stage.
16. Count is wrong in all positions of TIME-SECONDS switch. (FUNCTION switch in TEST position.)	TRIGGER VOLTAGE control R214 improperly adjusted or defective.	Adjust or replace R214.
17. All counts high and cannot be corrected by readjusting TIME BASE ADJUSTMENTS. (FUNCTION switch in TEST position.)	One or more counter assemblies may be skipping certain digits.	Check counter assemblies by substitution.
18. Counts are double the correct amount. (FUNCTION switch in TEST position.)	Gate stage V116 defective	Check for correct bias at pin 1 or V116. Replace defective part in grid circuit.
19. One numerical indicator and those to the left of it (as viewed from front panel) remain at zero and do not count.	Defective counter assembly associated with first (right-hand) malfunctioning numerical indicator.	Check connections at top and bottom of suspected counter assembly. Replace counter assembly, if necessary.
20. One numerical indicator remains dark while all others function normally.	Defective numerical indicator	Replace numerical indicator.
	Open anode dropping resistor on Nixie tube board assembly.	Replace defective resistor.

Symptom	Probable trouble	Correction
21. Numerical indicators function properly in AUTO position of AUTO-MANUAL switch, but cannot be reset by RESET switch in MANUAL position.	RESET switch S106 defective	Replace S106.
	Dc coupling resistor R278 or R272 defective.	Replace defective resistor.
22. INPUT LEVEL meter does not function although equipment operates normally.	Meter M101 defective	Replace meter.
	Diode V114 defective	Replace V114.
	C177, R221, R222, R223, or R224 defective.	Replace defective part.
23. With an input signal applied, numerical indicators count continuously in all positions (except COUNT OFF) of FUNCTION switch.	Gate control binary stage V120 defective.	Replace V120 or defective associated part.
24. Numerical indicator skips two consecutive digits.	Poor connection to associated counter assembly.	Check connectors P401 through P406 at tops of printed circuit boards for good contact.
	Defective spade resistor on beam switching tube socket.	Check spade resistor for first of digits skipped. Replace if necessary.
	Defective target load resistor on Nixie tube board assembly.	Check target load resistor for first digits skipped. Replace if necessary.
25. One number on numerical indicator fails to light, but equipment operates normally otherwise.	Defective numerical indicator	Replace numerical indicator.
26. Two or more numbers on any numerical indicator light simultaneously (numbers may also be skipped).	Short between target connections on Nixie tube board assembly.	Eliminate short.
	Defective target load resistor on Nixie tube board assembly.	Replace defective resistor.
27. Equipment operates properly in TEST position of FUNCTION switch, but not in FREQ. COUNT position.	Input signal level too low, or improperly connected to COUNTER INPUT jack J101.	Check connections. Rotate SENSITIVITY control R211 clockwise to increase frequency meter sensitivity. Increase signal input level.
	J101, C175, R211, or S103 defective	Repair or replace defective part.
28. Equipment operates properly in INT. operation but not in EXT. operation.	External 100-kc source signal level too low or improperly connected to EXTERNAL 100 KC jack.	Check connections. Increase signal input level.
	INT.-EXT. switch S107 or R127 defective.	Repair or replace defective part.

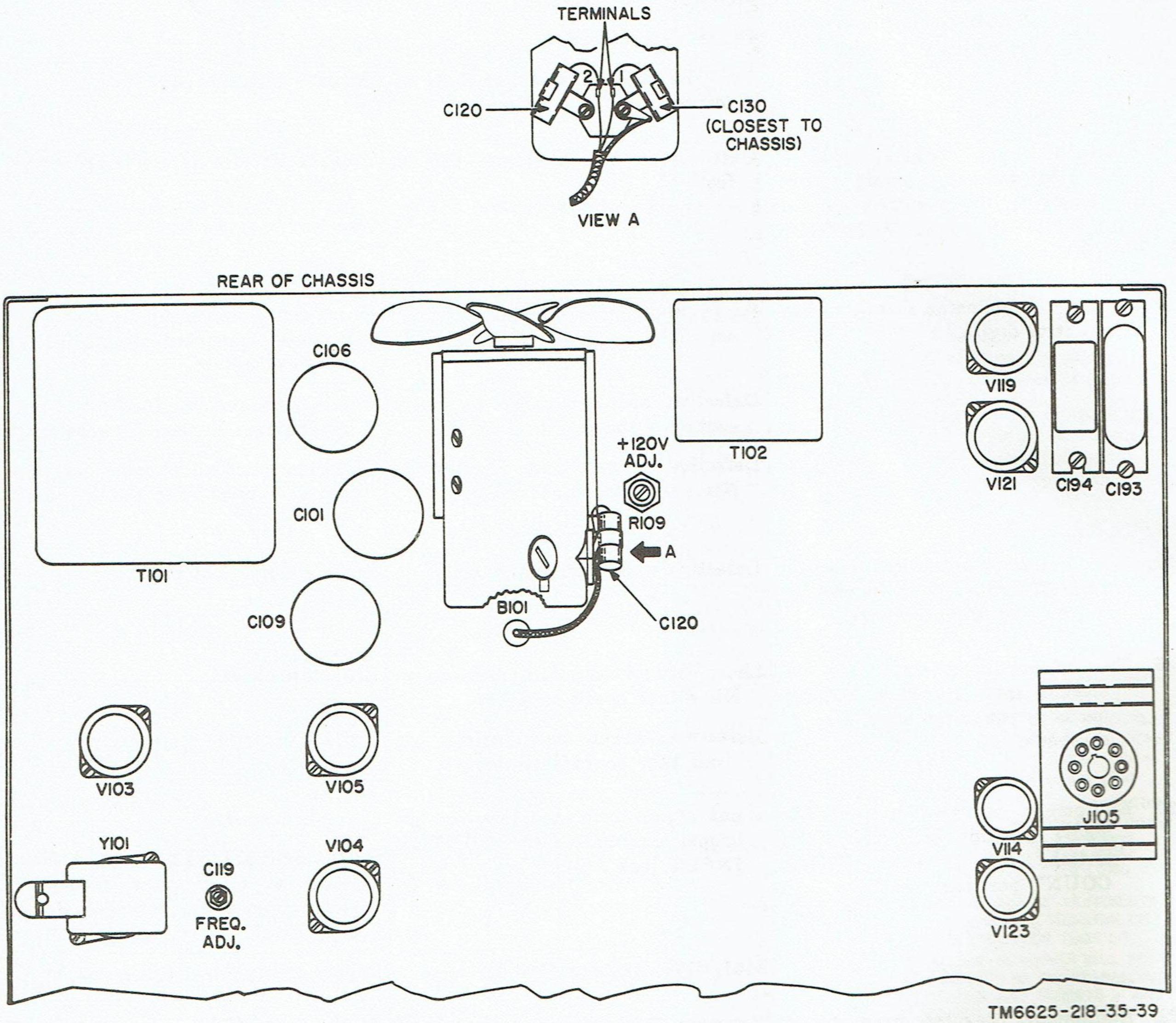
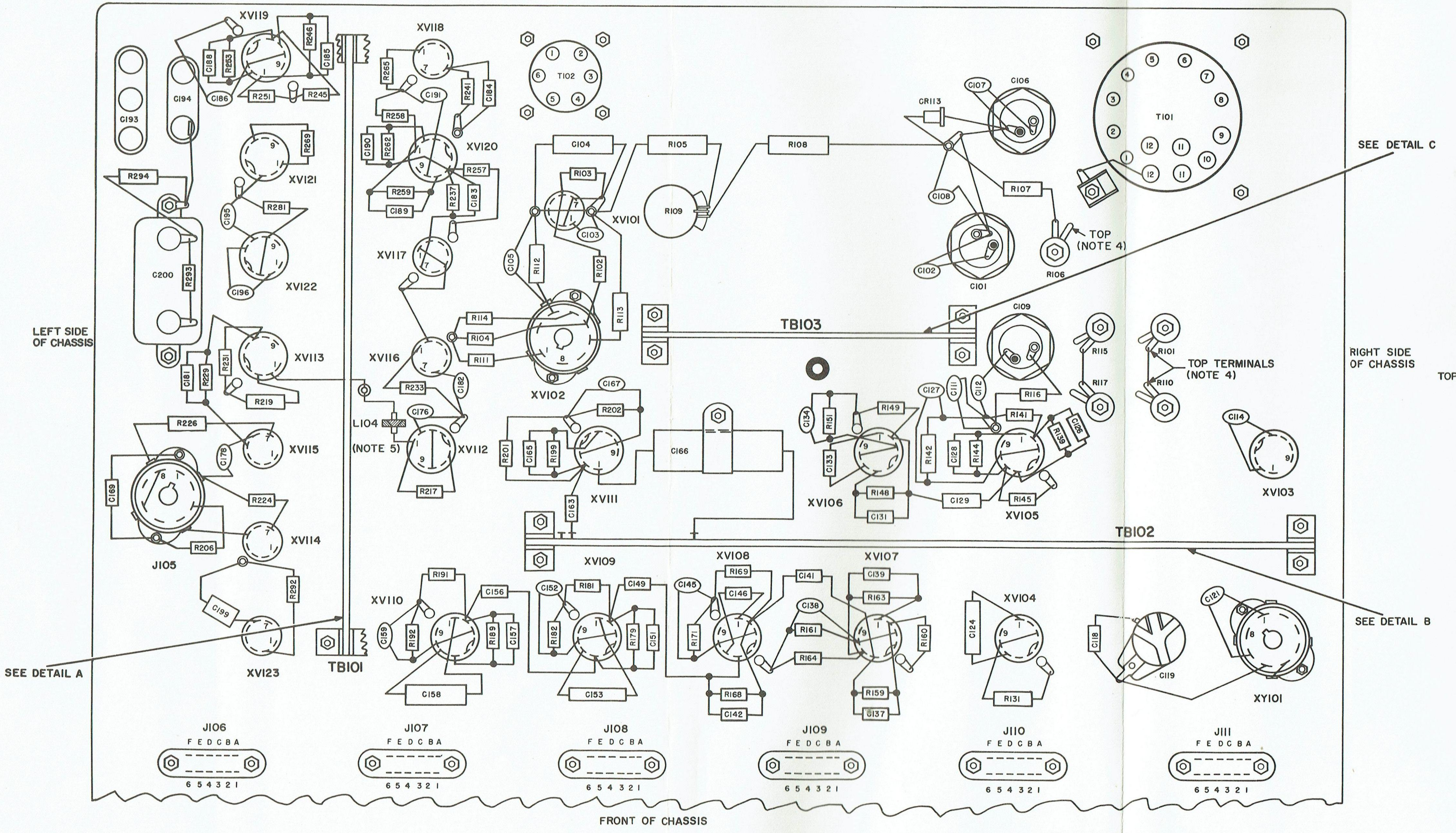
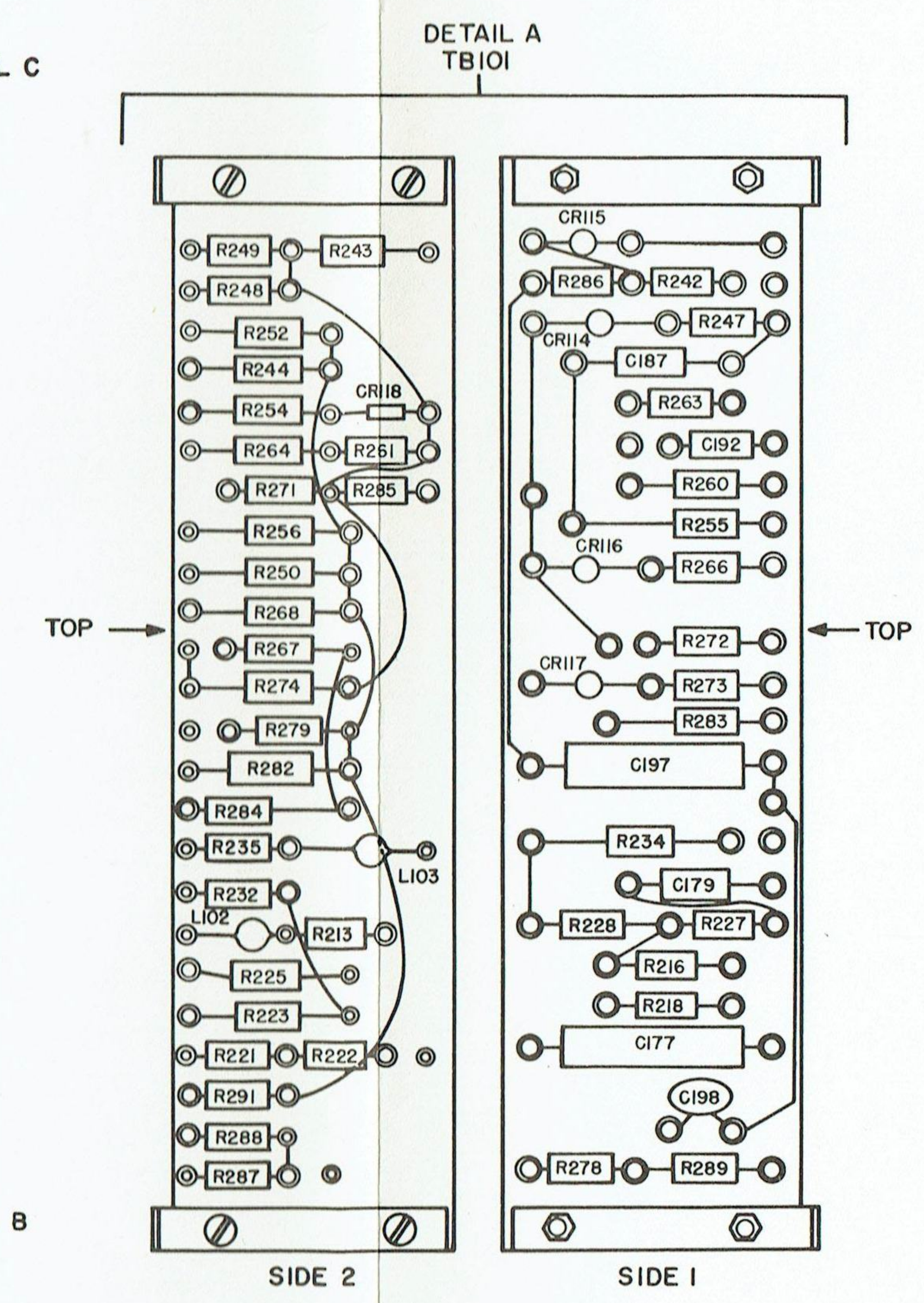
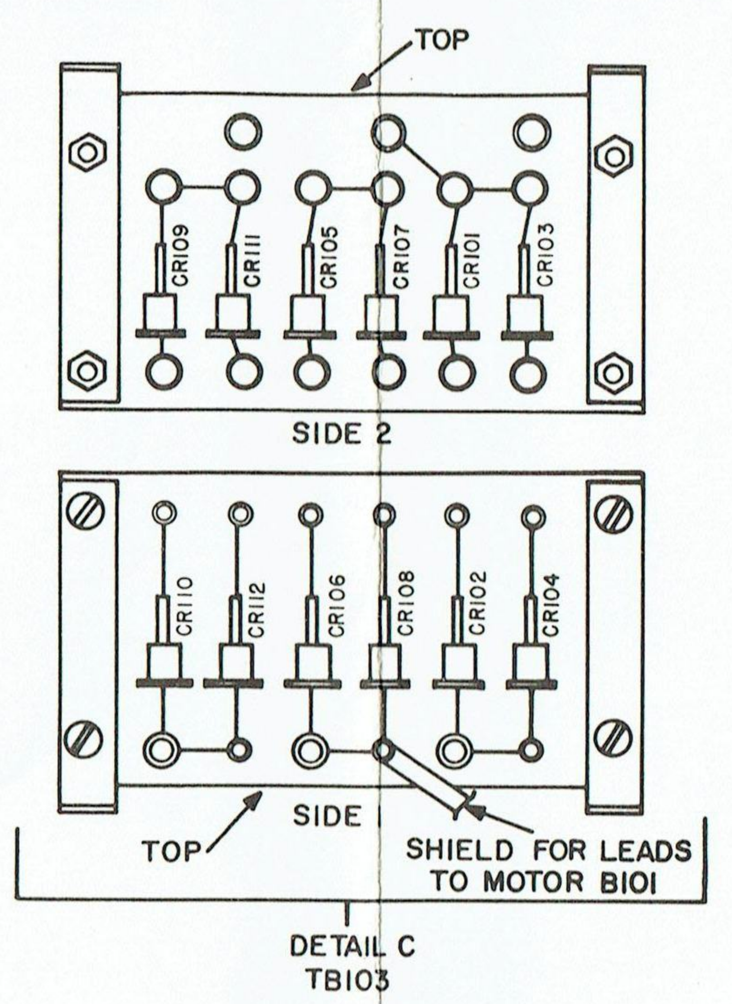
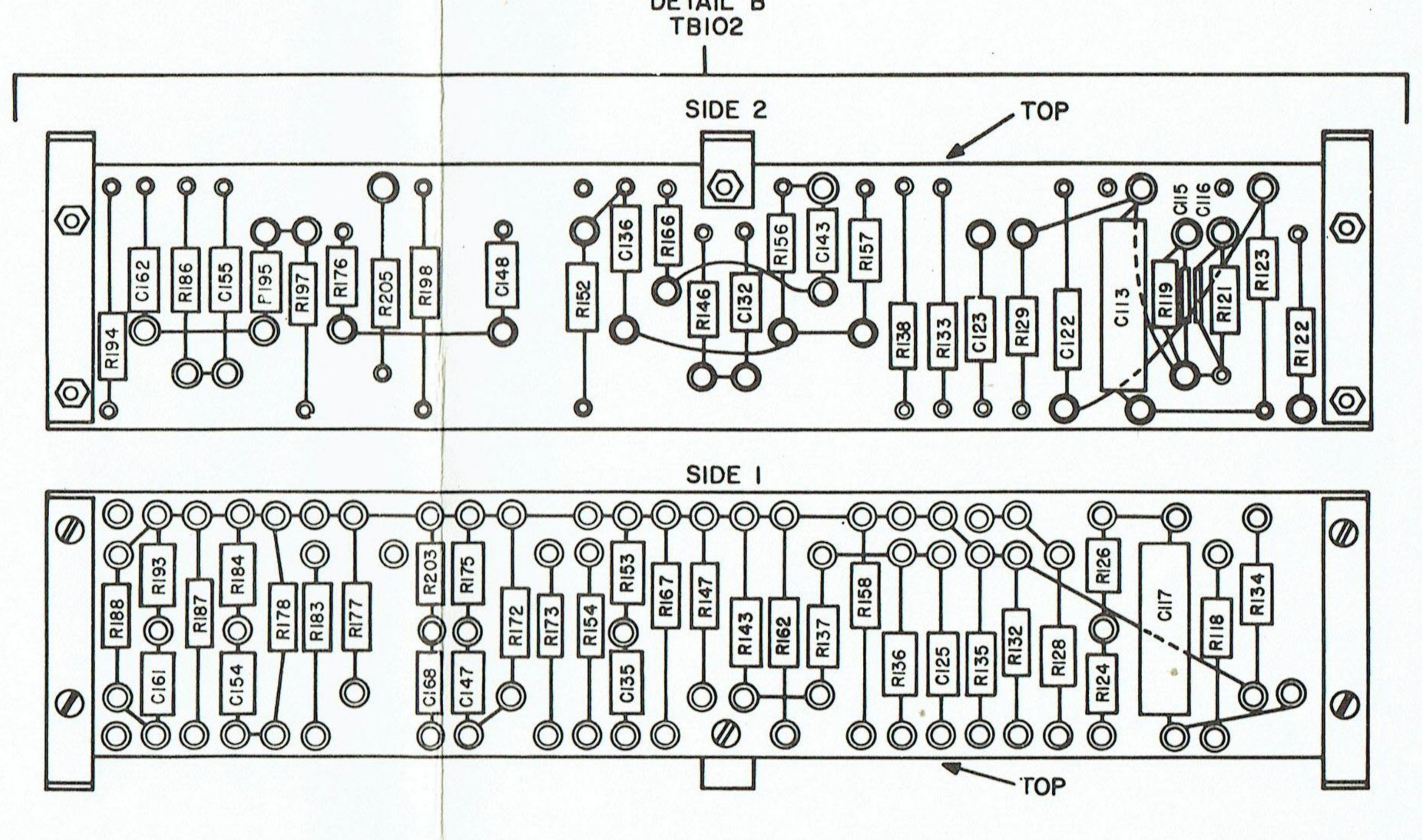


Figure 27. Top of main chassis, location of adjustment controls.









NOTES:

1. SIDE 1 OF TB101 FACES RIGHT SIDE OF CHASSIS. SIDE 2 FACES LEFT SIDE OF CHASSIS.
2. SIDES 1 OF TB102 AND TB103 FACE FRONT OF CHASSIS. SIDES 2 FACE REAR OF CHASSIS.
3. TOP SIDES OF TERMINAL BOARDS ARE CLOSEST TO CHASSIS; BOTTOM SIDES CLOSEST TO VIEWER, WITH EQUIPMENT AS ILLUSTRATED.
4. TOP TERMINALS OF R101, R110, R115, AND R117 ARE CLOSEST TO CHASSIS.
5. L104 NOT FOUND IN ALL EQUIPMENTS.

Figure 28. Bottom of main chassis, parts location diagram.

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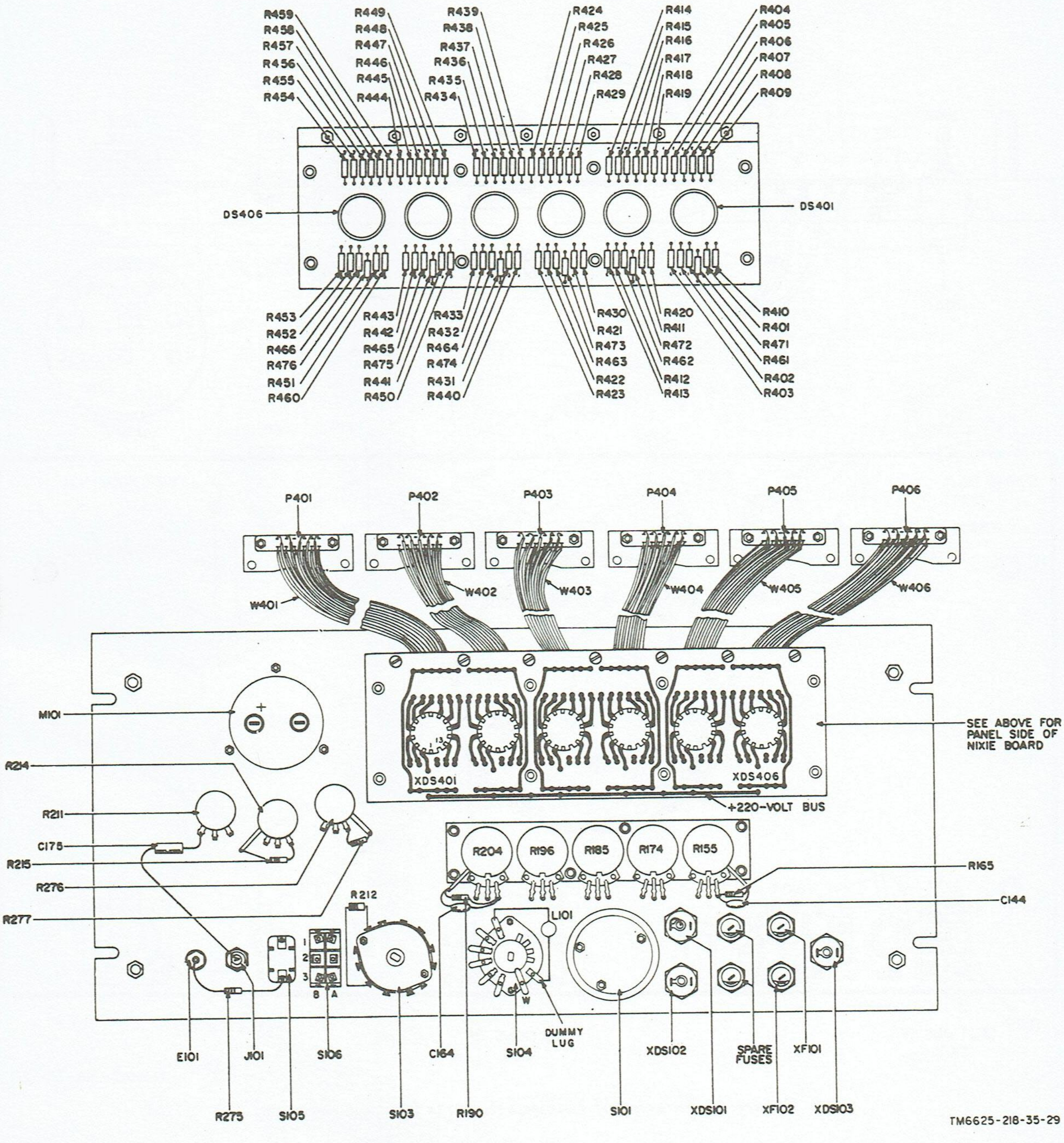


Figure 29. Rear of front panel, parts location diagram.

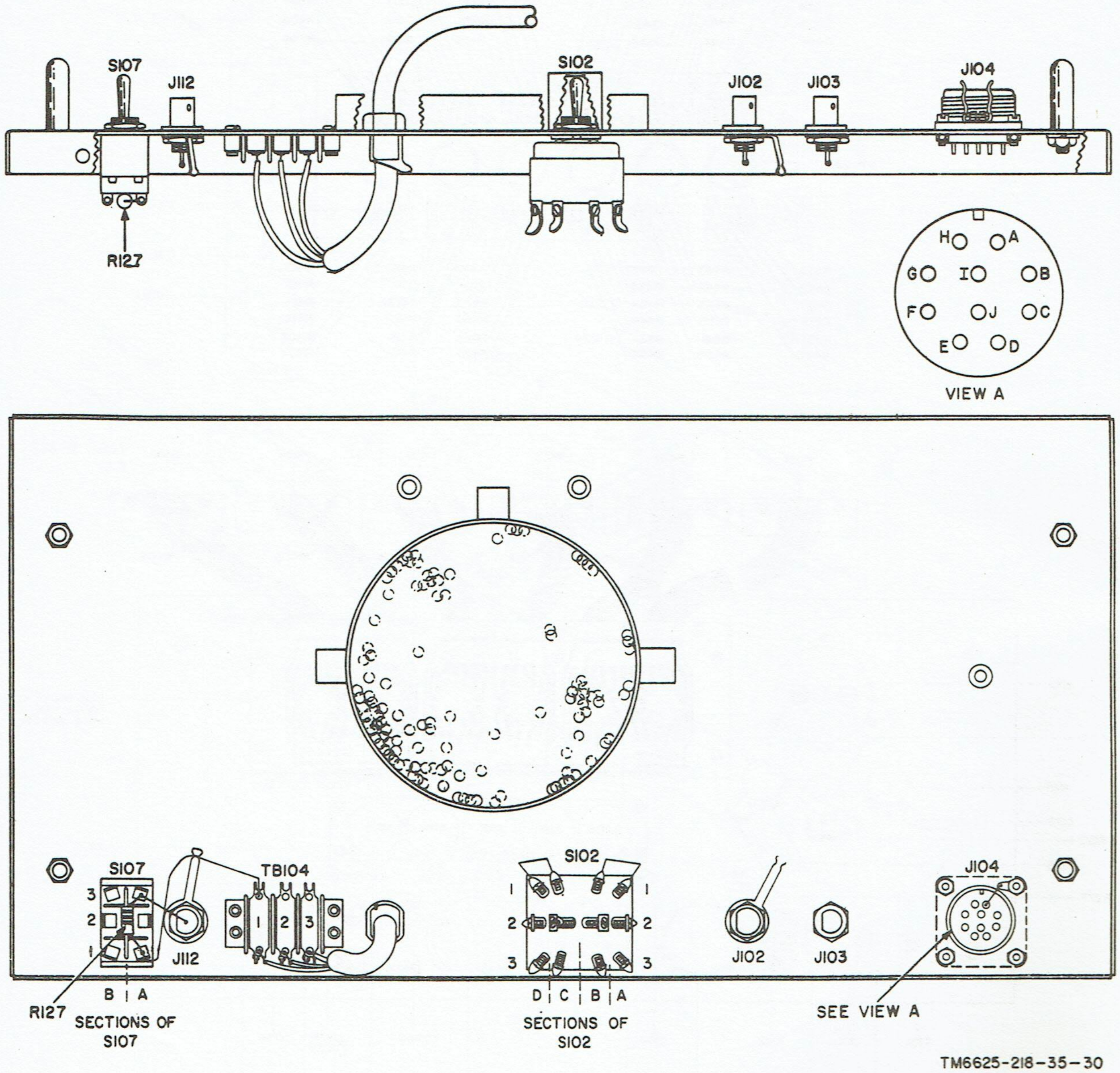


Figure 30. Interior of rear panel, parts location diagram.

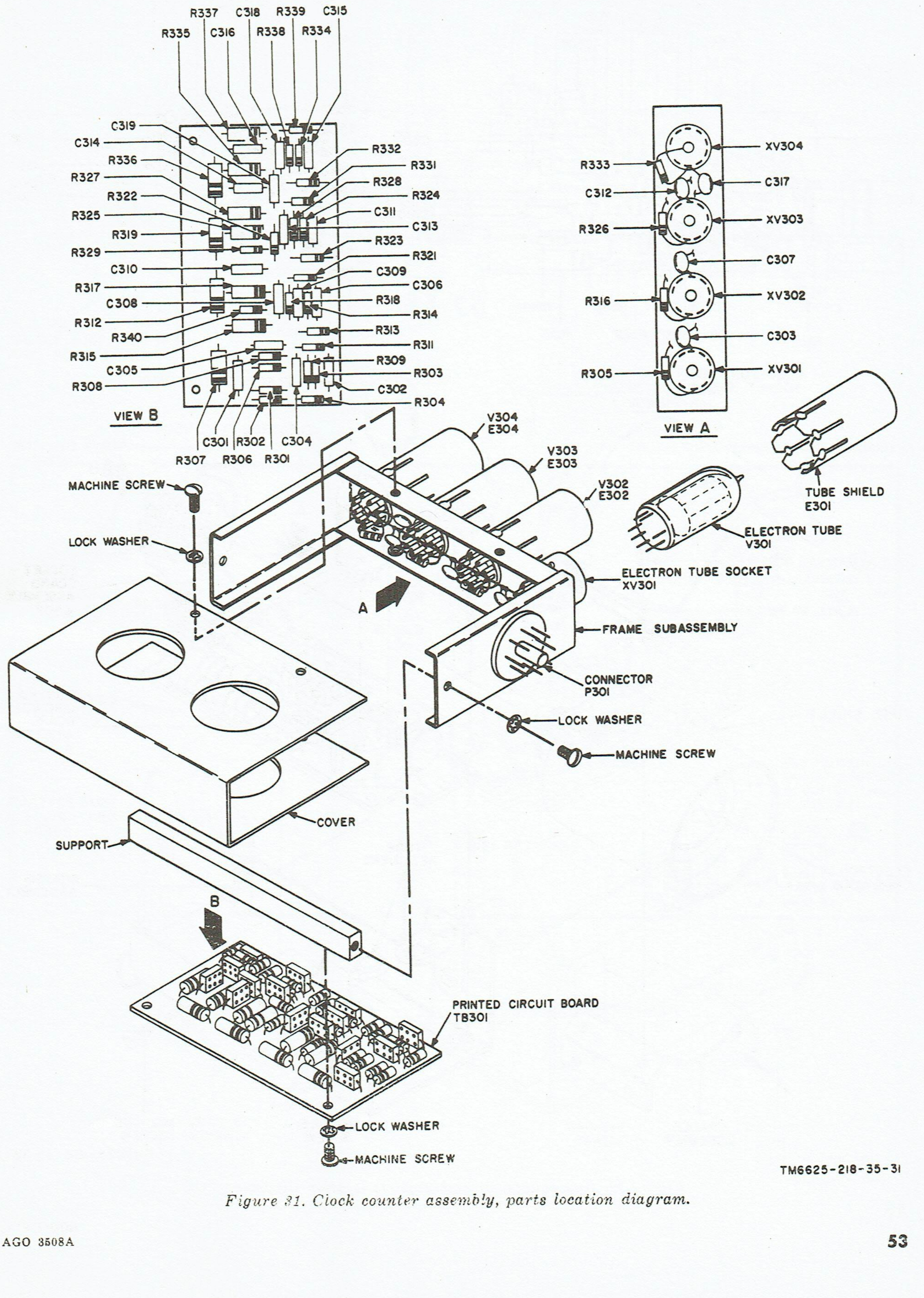


Figure 31. Clock counter assembly, parts location diagram.

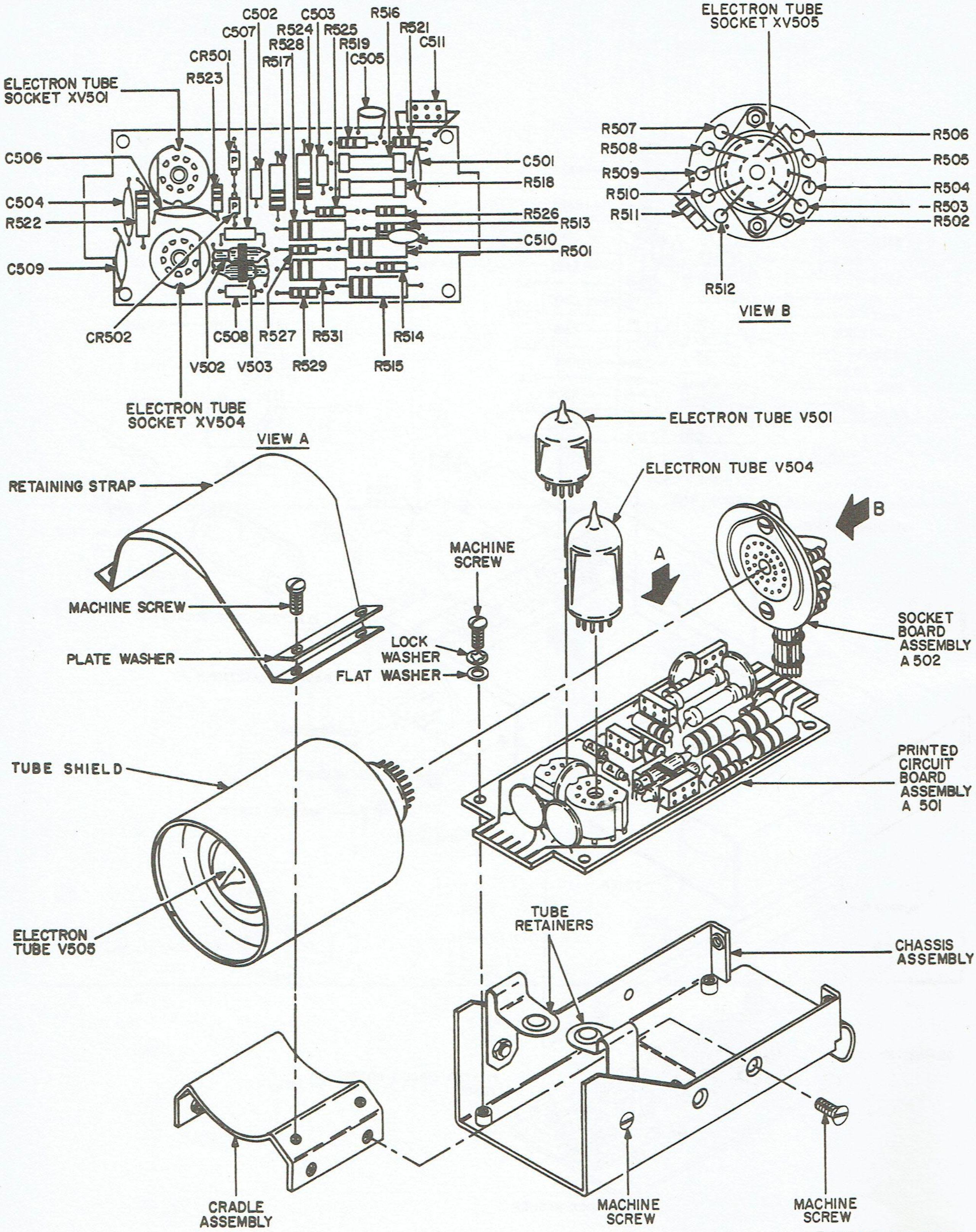


Figure 32. 1-mc counter assembly, parts location diagram.

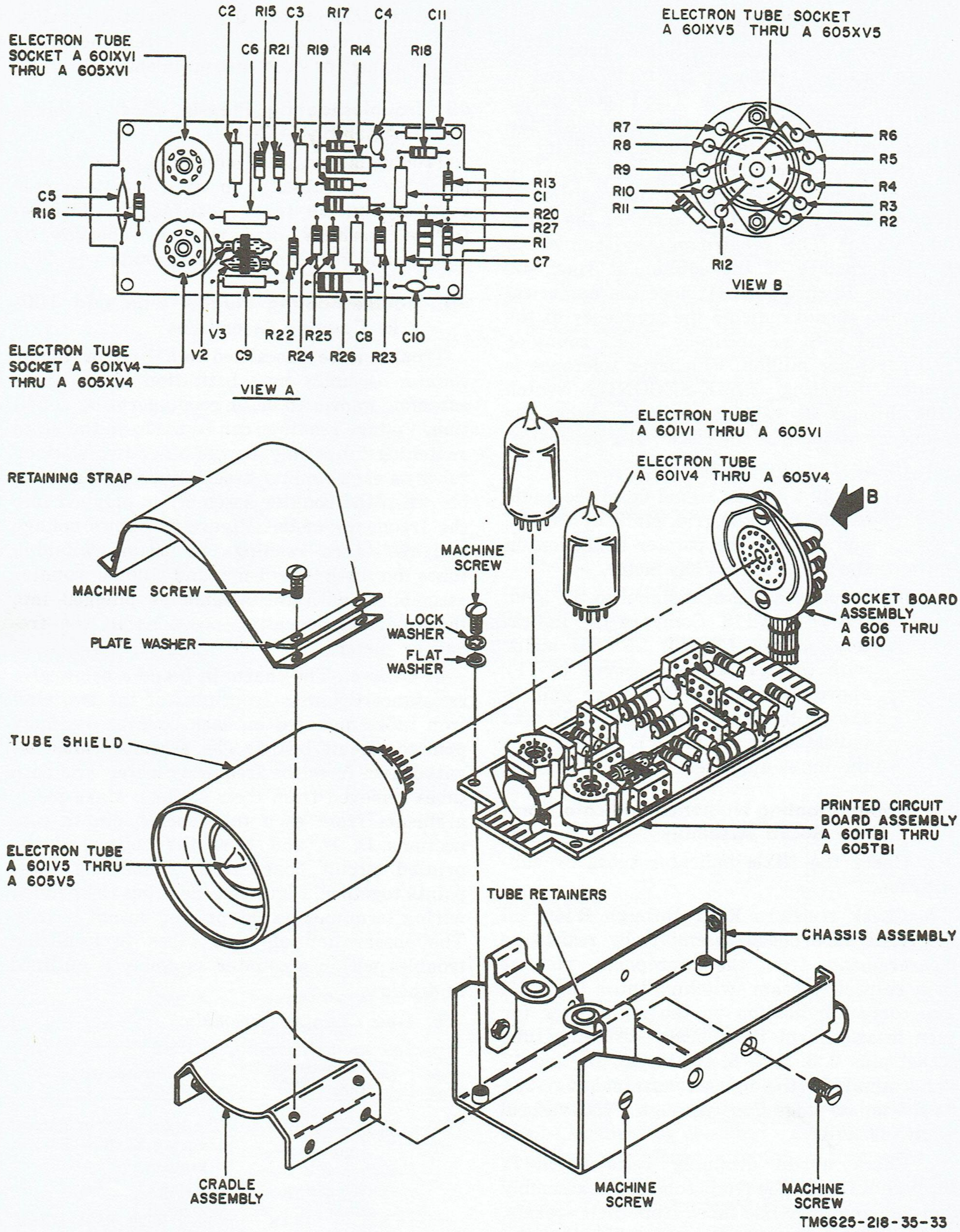


Figure 33. 100-kc counter assembly, parts location diagram.

43. Signal Substitution

a. General. Signal substitution procedures help to localize troubles to the input stages in the frequency meter. The TEST position of FUNCTION switch S103 enables the technician to apply either the internal 100-kc oscillator or an externally generated 100-kc test signal to the equipment (depending on the position of INT.-EXT. switch S107) in place of the usual input signal. The repairman can then check the performance of the equipment (par. 42, symptoms 13 through 18) since the numerical indicators should indicate the frequency of the test signal with an accuracy of ±1 count or ±10 parts per million, whichever tolerance is greater. Rotating TIME-SECONDS switch S104 through its various positions checks the frequency dividers of the clock pulse generator.

b. Input Amplifier V112.

(1) Apply a 100-kc signal from the audio oscillator to the grid, pin 2, of V113A, and observe the pointer deflection on the INPUT LEVEL meter.

(2) Apply the identical signal to the grid, pin 7, of V112. Compare the indication on the INPUT LEVEL meter with the indication observed in (1) above. If little or no voltage gain is shown by input amplifier V112 (as indicated on the meter), troubleshoot the input amplifier stage.

44. Troubleshooting Numerical Indicators and Nixie Board Assembly

a. Check the Nixie indicator tubes by substitution.

b. Check resistors R401 through R466, on the Nixie tube board assembly, by resistance measurements from the appropriate pins of their respective beam switching tubes (fig. 26). The correct indication on the multimeter for each measurement from beam switching tube socket pins 2, 3, 5, 7, 8, 10, 12, 13, 15, and 17 to terminal C (the unused terminal, fig. 29) on the top of plugs P401 through P406, respectively, is 36K.

c. Check anode dropping resistors R471 through R476, on the Nixie tube board assembly by removing the Nixie tubes from their sockets. Connect the ohmmeter successively between pin F of ACCESSORY POWER jack J104 and pin 2 of each numerical indicator tube socket. The indication on the multimeter should be 12,000 ohms for each measurement.

45. Troubleshooting Plug-in Clock Counter Assembly A 301

Trouble is best localized to the clock counter assembly by substitution of a clock counter assembly known to be satisfactory. The defective assembly may then be checked by voltage and resistance measurements (fig. 25).

46. Troubleshooting Plug-in 1-mc and 100-kc Counter Assemblies

Trouble is best localized to a 1-mc or 100-kc counter assembly by substitution of a counter assembly known to be in good operating condition. Voltage readings can be made on the beam switching tubes only, as the other two electron tubes on each counter assembly are not accessible when the counter assembly is plugged into the frequency meter. Figure 26 shows voltage and resistance readings of beam switching tubes on both the 1-mc and 100-kc counter assemblies, with the assemblies plugged into their normal operating positions in the frequency meter.

a. General. The charts in *b* and *c* below give resistance readings from pins of the two electron tubes mounted on each counter assembly printed circuit board. The assembly must be withdrawn from the frequency meter, and both tubes removed from their sockets. Make measurements from each tube socket pin to connections D, E, and F at the bottom of the printed circuit board after connecting these points together. Figure 34 identifies the printed wiring terminals on the printed circuit boards. The observation of neon tubes in localizing troubles within a counter assembly is outlined in *d* below.

b. 1-mc Counter Assembly.

Tube	Pin	Normal indication (ohms)	If abnormal
V501	1	Infinite	Check for short in filament wiring to B+, B−, or ground.
	2	3K	Check R522, C504.
	3	15.4K	Check R526, R525, CR502, R523, R517, C502, R516, R501.

Tube	Pin	Normal indication (ohms)	If abnormal
V501	4	14.7K	Check R518, C501, R501, R524, C503, R519, R521, C507.
	5	3K	Same checks as pin 2.
	6	14.7K	Check R516, C501, C502, C508, R501, R517, R525, R526.
	7	15.4K	Check R519, R521, CR501, R524, R523, C505, C503, R518, R501.
	8	3K	Same checks as pin 2.
	9	Infinite	Same checks as pin 1.
V504	1	0	Check wiring.
	2	470K	Check R527 and C507.
	3	24K	Check R528.
	4	Infinite	Check for short in filament wiring.
	5	Infinite	Same checks as pin 4.
	6	0	Check wiring.
	7	470K	Check R529 and C508.
	8	24K	Check R531.
	9	Infinite	Same checks as pin 4.

c. 100-kc Counter Assembly.

Tube	Pin	Normal indication (ohms)	If abnormal
V1	1	28.6K	Check R14, R13, R15, C2, C9.
	2	43K	Check R17, R18, R21, C3, C4, R20, R13.
	3	15K	Check R16, C5.
	4	Infinite	Check for short in filament wiring.
	5	Infinite	Same checks as pin 4.
	6	28.6K	Check R13, R20, R21, C3, C6.
	7	43K	Check R19, R15, C2, R14, R13.
	8	15K	Same checks as pin 3.
	9	Infinite	Same checks as pin 4.
V4	1	0	Check wiring.
	2	510K	Check R22 and C6.
	3	100K	Check R23, C7, C6.
	4	Infinite	Check for short in filament wiring.
	5	Infinite	Same checks as pin 4.
	6	0	Check wiring.
	7	510K	Check R24 and C9.
	8	100K	Check R25, C8, C9.
	9	Infinite	Same checks as pin 4.

d. Observation of Voltage-dropping Tubes. Observation of the two neon voltage-dropping tubes, V502 and V503 (for the 1-mc counter), or V2 and V3 (for the 100-kc counter) is useful in localizing trouble within a defective counter assembly. Plug the defective counter assembly into the frequency meter, apply power, and observe the neon tubes.

(1) If both neon tubes are dark, either no B+ voltage is reaching the counter assembly or the common voltage-dropping resistor in the path is open.

(2) If only one neon tube glows, check for trouble in the multivibrator plate resistor or cathode follower grid resistor of the unlighted tube.

(3) If the neon tubes are lighted (or flicker with a low-frequency input signal such as 30 cps), the trouble is in the cathode follower or beam switching tube circuits.

47. Dc Resistances of Transformers and Coils

The dc resistances of the transformer windings and the coils in the frequency meter are as follows:

Transformer or coil	Terminals	Ohms
T101	1–2	2.4
	3–4	2.4
	5–6	13.6
	7–8	10.5
	9–10	Less than 1
	11–12	Less than 1
T102	1–2	88
	3–4	88
	5–6	Less than 1
L101	1–2	11
L102	1–2	7.2
L103	1–2	11

48. Checking Waveforms (fig. 35)

Certain troubles that do not permit rapid localization to a stage through operational tests can be localized by checking waveforms. Figure 35 shows significant waveforms that exist at tube sockets or at the wiring side of multipin connectors J106 through J111 (fig. 28). Use the oscilloscope and compare the waveforms at

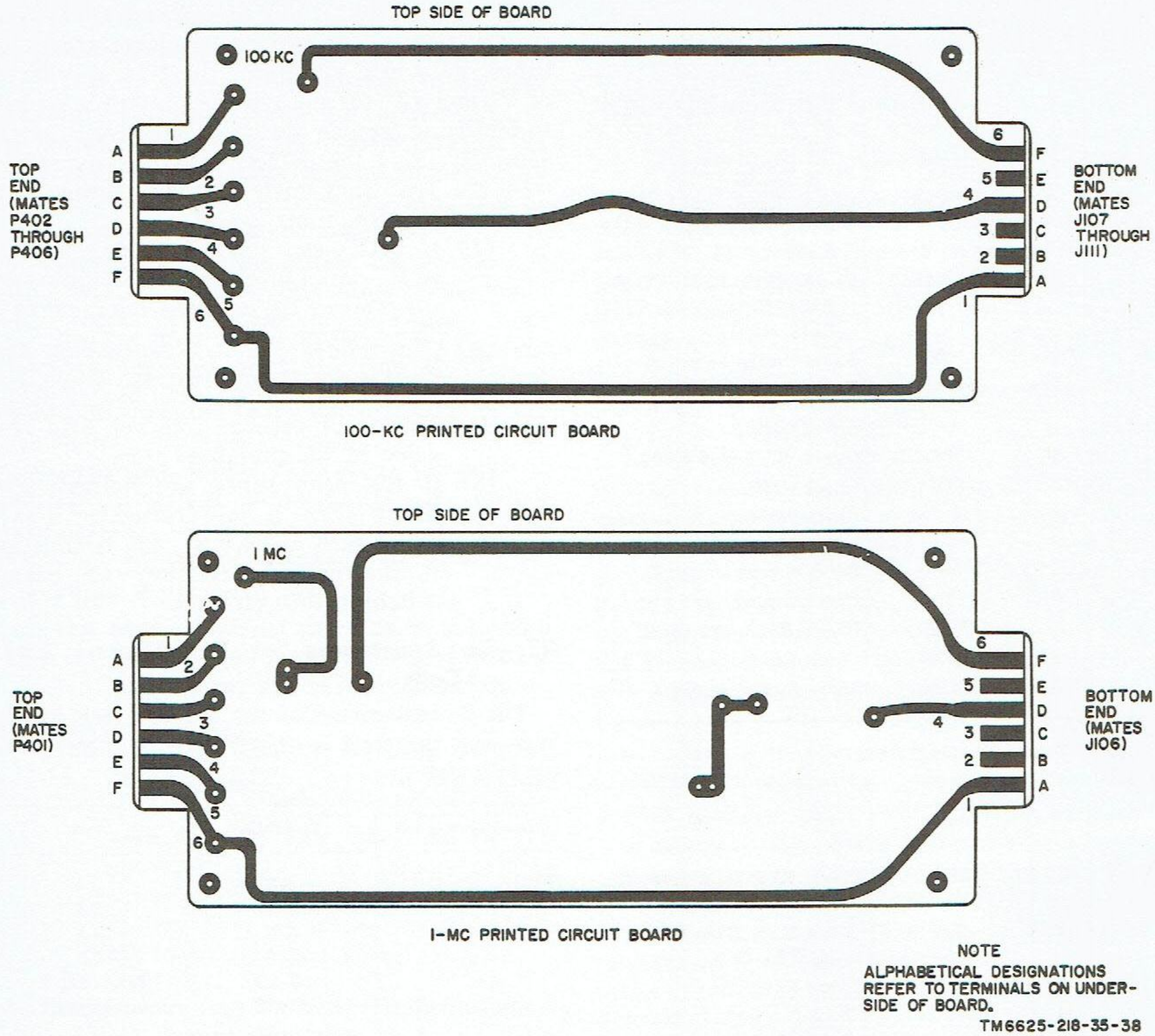


Figure 34. Counter assembly printed circuit boards, terminal identification.

the test points listed in figure 35 against the typical waveforms illustrated. Note that the waveform deteriorates in appearance as higher input frequencies are applied to the instrument. For example, in A, 10 clearly defined pips that represent the switching of the electron beam in beam switching tube V505, with a relatively low frequency of 100 kc under measurement, are shown. The waveform in B is different in appearance. Both the leading and trailing edges of the first switching count are rounded off because the relatively high frequency of 1 mc is under measurement. This phenomenom indicates normal functioning of the equipment and is not to be misinterpreted as an indication of malfunction. Special note should be made of the use of waveform A. This waveform will appear at pin 10 of counter A 501 and at pin 10 of counters A 601 through A 605. Trouble within the equipment can be localized by observing waveforms as follows:

a. If the waveforms shown in A and B are correct, proper operation of the 1-mc counter assembly and all preceding circuits (including the clock pulse generator, input and trigger circuits, gate stage V116, and gate control stages) is indicated. By placing the oscilloscope probe successively on pin 10 of each of the five

100-kc counter assembly beam switching tube sockets, waveforms similar to A and B should appear. The time base must be multiplied by a factor of 10 each time the probe is shifted leftward (as viewed from the equipment front panel) to the next counter assembly in the chain. If the waveform disappears or if there are missing pips the indication is that the respective counter assembly circuit is defective.

b. If the waveforms shown in A and B are incorrect or missing, check for the waveforms shown at the input to the 1-mc counter (C and D).

c. If the waveforms shown in A and B are incorrect, but those shown in C and D are satisfactory, trouble is then definitely localized to the 1-mc counter assembly (V501 through V505 circuits).

d. If the waveforms shown in C and D are incorrect or missing, check for the waveforms from trigger stage V113B (E and F).

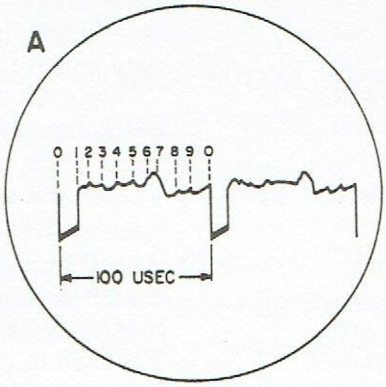
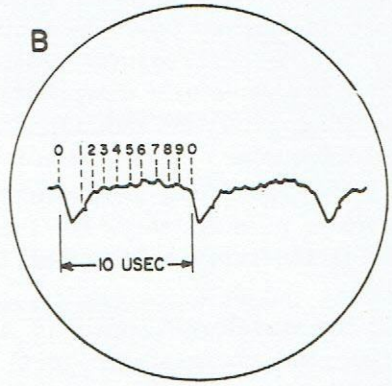
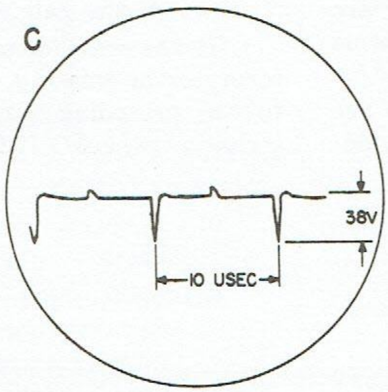
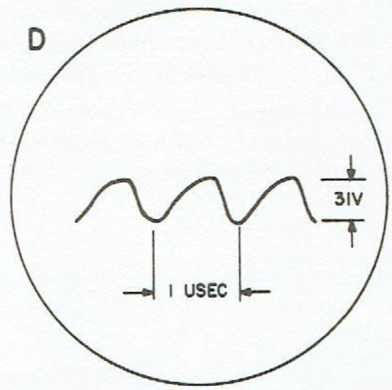
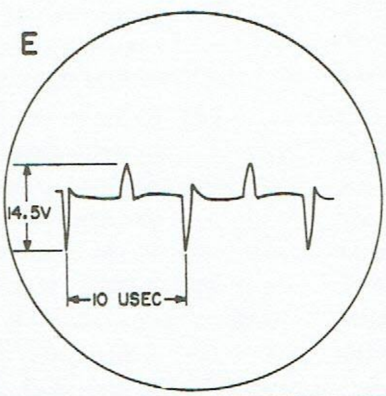
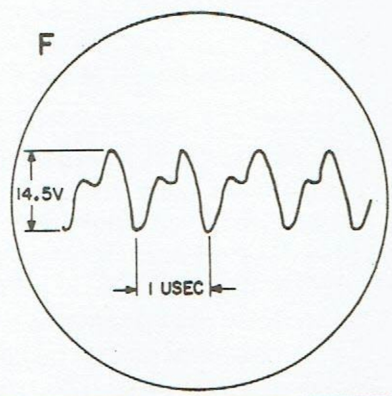
e. If the waveforms shown in C and D are incorrect, but those shown in E and F are satisfactory, trouble is then localized to the gate stage, the gate control circuit, or to the clock pulse generator, as follows:

(1) Gate stage V116 functions properly only when it receives the output of gate control binary V120 at the start and end of the counting interval. An open line or defective part in the signal path from the plate, pin 6, of V120 to the suppressor, pin 7, of V116, may be the source of trouble.

(2) Any failure in the gate control circuit may be responsible for the lack of a control voltage at gate control binary V120 plate, pin 6.

(3) A failure in the clock pulse generator, for the timing period in use, may be responsible for the lack of triggering of the gate control circuit.

f. If the waveforms shown in E and F are incorrect or missing, trouble is then localized to the preceding input and trigger circuits, including stages V112 through V114.

TEST POINT	100-KC INPUT SIGNAL UNDER MEASUREMENT	1-MC INPUT SIGNAL UNDER MEASUREMENT
OUTPUT OF 1-MC COUNTER AT BEAM SWITCHING TUBE SOCKET, PIN 10		
INPUT TO 1-MC COUNTER AT J106, PIN 4		
OUTPUT OF TRIGGER STAGE V113B, PIN 9		

NOTE:

SWITCH	POSITION
FUNCTION	SCAN COUNT
AUTO-MANUAL	AUTO
TIME-SECONDS	10 (FOR 1-MC INPUT) 1 (FOR 100-KC INPUT)

TM6625-218-35-45

Figure 35. Typical waveforms used to help localize troubles in counter assemblies and gate stages.

CHAPTER 3

REPAIRS AND ADJUSTMENTS

Section I. REPAIRS

49. General Parts Replacement Techniques

Most of the parts in the frequency meter can be reached and replaced easily without special procedures. Before a part is unsoldered, note the position of its leads. Wire the replacement part in the same position as that occupied by the old part. A part that has the same electrical value but different physical size may cause trouble in high-frequency circuits. Give particular attention to proper grounding. Use the same ground as in the original wiring. Failure to observe these precautions may decrease the accuracy of the frequency meter.

50. Removal of Parts

a. Instructions for removal of the top and bottom cover plates are contained in paragraph 27*b*, TM 11-6625-218-12.

b. Instructions for removal of crystal Y101 from the oven assembly are contained in paragraph 32, TM 11-6625-218-12.

c. Instructions for removal of counter assemblies and Nixie numerical indicators are contained in paragraph 30*a*, TM 11-6625-218-12.

d. To remove the beam switching tube (fig. 32 and 33) from a counter assembly, proceed as follows:

(1) Remove the counter assembly from the frequency meter as instructed in paragraph 31*b*, TM 11-6625-218-12.

(2) Carefully disengage the socket board assembly from the beam switching tube.

(3) Free the beam switching tube by removing four machine screws from the retaining strap and removing the strap.

Caution: **Hold the strap firmly while removing the screws to prevent the strap from springing away and throwing the screws and plate washers.**

(4) Lift the beam switching tube from its cradle.

(5) Orient the new tube so that the pins line up correctly with the tube socket. Replace the socket board.

(6) Secure the retaining strap with the four machine screws and two plate washers.

e. To remove the printed circuit board assembly from a counter assembly (fig. 32 and 33), proceed as follows:

(1) Perform the steps in *d*(1) and (2) above.

(2) Shift the tube retainers of the two electron tubes aside, and remove both tubes from their sockets on the printed circuit board assembly.

(3) Remove the cradle assembly (containing the beam switching tube) from the counter chassis assembly by removing the four screws at the sides of the chassis assembly.

(4) Remove the printed circuit board assembly from the counter chassis assembly by removing the four screws and eight washers at the four corners of the printed circuit board.

f. To remove the blower motor from the chassis, proceed as follows:

(1) Remove the air filter clamp at the rear of the frequency meter by removing the two screws that secure the clamp to the rear panel. The filter clamp is located directly above the air filter (fig. 5, TM 11-6625-218-12).

(2) Slide the air filter straight up and out of its retaining bracket.

(3) Remove the fan blade from the motor shaft by loosening the two retaining setscrews. Pull the fan blade out through the opening in the rear panel.

(4) With the air filter removed, the three screws that secure the blower motor to the blower motor bracket are accessible from the rear of the instrument. Remove these three screws while holding the motor. (Do not allow it to fall into the chassis after all screws have been removed.)

(5) There is sufficient slack in the wiring to capacitors C120 and C130, which are mounted on the motor frame (fig. 27), to permit turning the motor so that the brush retaining caps are accessible. Using a screwdriver, loosen each of the two brush retaining caps. Expected brush life is a minimum of 1,000 hours of operation.

(6) Withdraw the defective motor brush and spring. Insert a replacement brush and spring.

(7) Reassemble the motor, fan, and air filter by following the instructions above in reverse order.

51. Repairing Printed Wiring Assemblies

a. General. Repairing printed circuit wiring assemblies is more difficult and requires more skill than repairing conventional equipment. Printed wiring can be damaged easily by heat; be careful when soldering. Prolonged heat will destroy the adhesive qualities of the agent that bonds the copper foil to the base material.

b. Special Tools and Materials Required.

(1) *Special tools.* Special tools, some of them small in size, are required for repairing printed circuit assemblies.

(*a*) Pencil-type soldering iron, 25 watts.

(*b*) Small twist drills, No. 30 through No. 60

(*c*) Pin vise

(*d*) Small metal pick

(*e*) ½-inch brush

(2) *Materials.* A list of materials needed, in addition to those used in troubleshooting conventional assemblies, follows:

(*a*) Rosin-alcohol solder flux, spec MIL–14256 (Sig C)

(*b*) Varnish (MIL–V–173A)

(*c*) Alcohol

c. Removing Part.

(1) *Removing protective coating.* The protective coating on the printed circuit board must be removed before starting repairs. Carefully scrape or chip the coating away with a metal pick, knife, or other suitable instrument. If scraping or chipping is not successful, apply a hot soldering iron to the coating to soften it. Never use a solvent to remove the coating. Solvents are difficult to control and may loosen the copper foil from the printed circuit board.

(2) *Removing defective part.* Cut the leads of the defective part as close as possible to the body of the defective part. Unsolder each lead individually as follows:

(*a*) Working from the foil side of the board, use the tip of the soldering iron to melt the solder at the foil connection.

(*b*) Gently work the lead outward on the foil side just far enough to cut off the flattened portion of the lead.

(*c*) While the solder is still molten, carefully pull the lead out from the *component* side of the board, to avoid the risk of tearing the foil.

d. Clearing Lead Hole.

(1) Molten solder will sometimes flow into the lead holes while the part is being removed. Avoid using a soldering iron to remove the solder because the amount of heat required may loosen the foil. Do not clean the hole by heating the solder when inserting the new part; the lead may catch the edge of the foil and tear it away from the board.

(2) On the beam switching tube socket boards, some of the leads are passed through metal eyelets. The solder often will flow into the eyelet where it cannot be brushed away. Tap the

board sharply while the solder is still molten, and force it to flow out. If the solder cannot be removed this way, chuck a twist drill of suitable size in a pin vise and carefully drill the solder out from the foil side of the board. This will form a hole large enough to insert the new part lead. Drilling from the component side of the board can loosen the foil as the drill passes through it.

e. Installing New Part.

(1) Scrape the leads clean with a knife. Bend the leads carefully until the distance between them is such that they will fit into the holes from which the defective part was removed. Mount the part and clinch or swage the leads close to the foil. This will form a strong mechanical joint.

(2) Apply a small amount of noncorrosive, nonconductive rosin-alcohol-mixture flux to the joint. Touch the soldering iron tip to the part lead and apply a small amount of solder (fluxless 60/40 solder) to the junction of the lead and the foil. Remove the iron as soon as the solder flows into the joint. Hold the lead firmly until the solder sets. Remove any excess flux with a small amount of alcohol.

f. Recoating Joint. After the solder cools, inspect the joint to see that it is clean and that solder has not flowed or dropped where it can cause short circuits. Newly soldered joints will become corroded if left uncoated, especially in damp climates. Apply a coating of varnish (MIL–V–173A) to the bare areas. Cover the area completely and overlap the surrounding coating areas.

g. Repairing Printed Conductor on the Printed Circuit Board. The printed conductor, which is a thin copper foil, can become damaged and cause an open circuit. Generally, when the foil is damaged in one place, it probably is damaged at other points also. Therefore, the entire board should be replaced. A defect in more than one place on a board crowded with many components means that it must be discarded because the space in particular areas is too small for repairs. When repairs must be made and the space is adequate, follow the procedure below.

(1) Remove the loose or charred portions of the conductor. Bend a piece of tinned copper wire, about No. 20. gage, into the shape of a staple. The staple must be long enough to span the defective portion of the conductor and be clinched about 1/4 inch from the end, after being inserted through the assembly board.

(2) Drill two holes of proper size to receive the staple ends. The holes must not be drilled through the foil, but near the foil so that the staple will be parallel to the foil. Insert the staple from the component side of the board, and bend the ends diagonally across the printed conductor. There is greater contact with the conductor when it is bent diagonally rather than at right angles to the foil. If possible, the staple should make contact for about 1/4 inch. Apply flux and use the soldering iron to solder the staple to the foil. Do not leave the soldering iron on the joint any longer than necessary.

52. RF Cabling and Connector Service

The signal cord, CG–409E/U, uses type RG–58/U coaxial cable. To repair or replace RF connectors, follow the procedures in figure 36.

53. Wiring Legend

(figs. 27-30)

a. General. The wiring legend, shown in the chart in *b* below, lists wiring used to interconnect parts mounted on the top of the chassis (fig. 27), on the bottom of the chassis (fig. 28), on the rear of the front panel (fig. 29), and on the interior of the rear panel (fig. 30). Jumper wires are shown on figures 28 through 30. The information listed in the wiring legend is helpful to the technician in repairing or replacing defective parts. Because frequent reference to the overall schematic diagrams for checking wiring connections are necessary, certain arbitrary numbers have been assigned to the terminals on TB104 (fig. 30), and to the terminals of toggle switches S102, S106, and

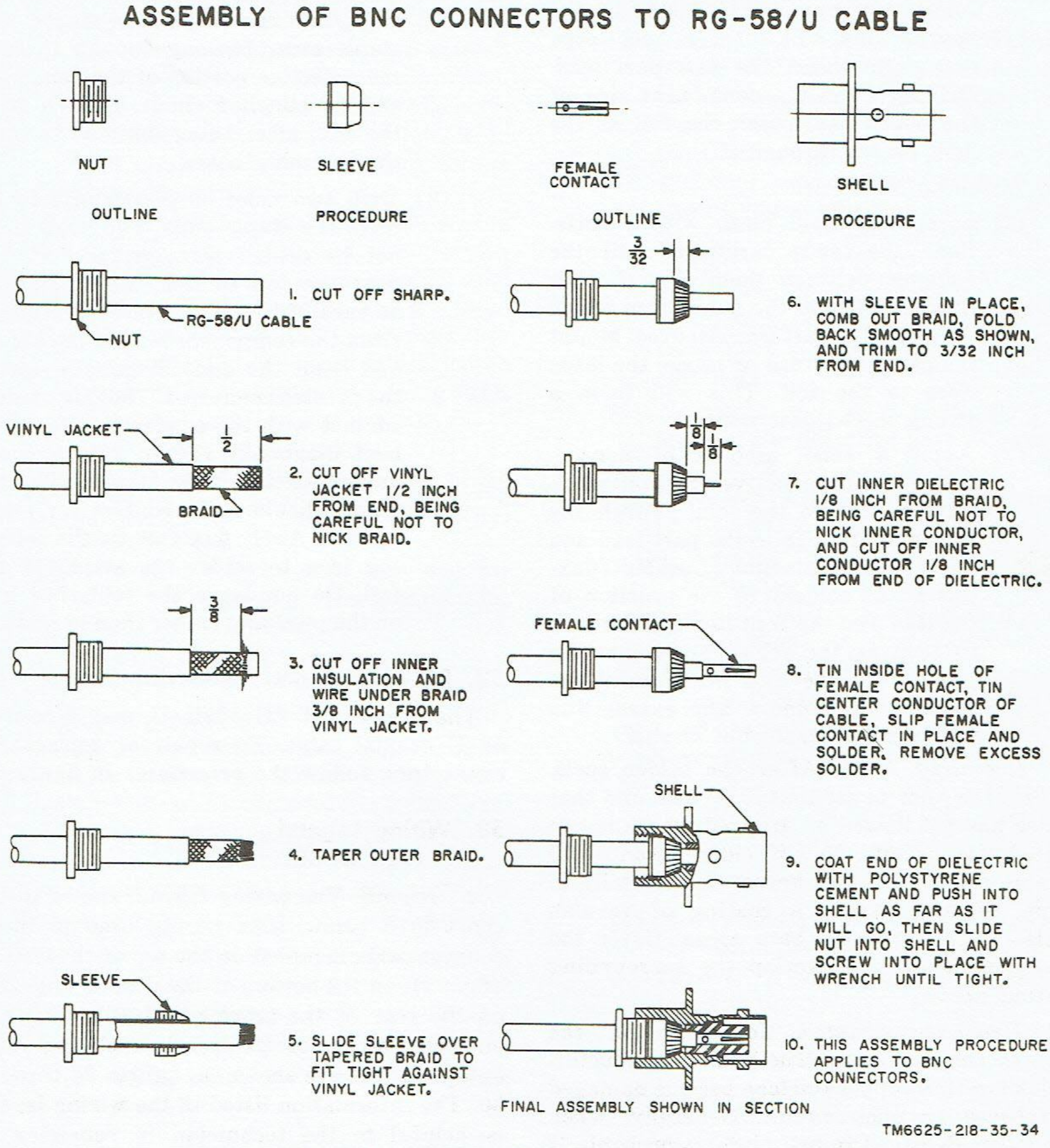


Figure 36. Assembly of rf cable and connectors.

S107 (fig. 29 and 30). These arbitrary numbers help locate wiring connections.

***Caution:* To prevent incorrect wiring of replacement parts, be sure to be guided by the notes on each parts location diagram (fig. 28–30) which define *top, bottom, front,* and *rear. Left* and *right* directions are as shown on the parts location diagrams.**

b. Legend.

Notes.

1. All parts are located on the bottom of the chassis, unless otherwise indicated.
2. When parts on the main chassis are referenced, *top* designates that connection which is closer to the chassis. *Bottom* designates that connection which is closer to the viewer, with the wiring side of the chassis facing the viewer.
3. *Front* designates that connection which is closer to the front of the chassis. *Rear* designates that connection which is closer to the rear of the chassis.

From	To
B101–1; on top of chassis	R117, top terminal.
B101–2; on top of chassis	C109, positive terminal.
C101, negative terminal	CR101, CR103; on TB103.
C101, negative terminal	CR113, ground lug.
C101, positive terminal	J104F; on interior of rear panel.
C101, positive terminal	R101, bottom terminal.
C101, positive terminal	XV102–5.
C104, R112	R113, R105.
C106, negative terminal	J111F.
C106, negative terminal	R106, bottom terminal.
C106, negative terminal	T101–9.
C106, positive terminal	CR113, ground lug.
C109, negative terminal	R115, bottom terminal.
C109, positive terminal	CR110, CR112; on TB103.
C111, R116	CR109, CR111; on TB103.
C115, top; on TB102	XV103–3.
C117, top; on TB102	XY101–4.
C119, front terminal	XY101–6.
C119, rear terminal	R124, top; on TB102.
C123, top; on TB102	S103B–1, terminal 5; on rear of front panel.
C125, top; on TB102	XV104–6.
C132, top; on TB102	XV105–6.
C135, R153; on TB102	E104–6; on rear of front panel.
C136, top; on TB102	XV106–6.
C147, R175; on TB102	S104–5; on rear of front panel.
C154, R184; on TB102	S104–4; on rear of front panel.
C161, R193; on TB102	S104–3; on rear of front panel.
C168, R203; on TB102	S104–2; on rear of front panel.
C169, rear terminal	S104–1; on rear of front panel.
C177, thru lug, bottom; on TB101.	XV113–3.
C179, top; on TB101	XV116–1.
C184, standoff	S103A–1, terminal W; on rear of front panel.
C192, bottom; on TB101.	S103A–2, terminal W; on rear of front panel.
C192, top; on TB101	XV118–1.
C193, front terminal	CR118, R254; on TB101.
C193, front terminal	J105–2.
C193, rear terminal	XV121–1.
C194, front terminal	C200, ground lug.
C194, rear terminal	S106A, terminal 2; on rear of front panel.
C199, R292	R294, C200.
C200, front terminal	R274, bottom; on TM101.
CR101, CR102; on TB103	T101–5.
CR102, CR104; on TB103	R101, bottom terminal.
CR103, CR104; on TB103	T101–6.
CR105, CR106; on TB103	T101–7.
CR105, CR107; on TB103	R106, top terminal.
CR107, CR108; on TB103	T101–8.
CR109, CR110; on TB103	T101–2.
CR111, CR112; on TB103	T101–1.
CR113, R108	R218, bottom; on TB101.
CR117, bottom; on TB101	S105, bottom terminal; on rear of front panel.
J102, conductor; on interior of rear panel.	S103A–1, terminal 5; on rear of front panel.
J102, ground lug; on interior of rear panel.	J102, shield; on interior of rear panel.
J102, ground lug; on interior of rear panel.	J103, shield; on interior of rear panel.
J103, conductor; on interior of rear panel.	S103A–2, terminal 5; on rear of front panel.
J104, ground lug; on interior of rear panel.	J104A; on interior of rear panel.
J104, ground lug; on interior of rear panel.	XV119, ground lug.
J104E; on interior of rear panel.	T101–12.
J104I; on interior of rear panel.	T101–11.
J105, ground	XV114–5.
J105–1	T101–11.
J105–1	XV114–3.
J105–4	R291, bottom; on TB101.
J105–5	XV111–6.
J105–7	T101–12.
J105–7	XV114–4.
J105–8	R278, R289, thru lug; on TB101.
J106A	J107A.
J106A	XV123–6.
J106B	J107B.
J106B	XV123–3.
J106C	J107C.
J106C	XV123–4.
J106D	J107D.
J106E	J107E.

From	To
J106F	J107F.
J106–1	J107–4.
J106–4	R235, top; on TB101.
J106–6	J107–6.
J106–6	XV123–2.
J107A	J108A.
J107B	J108B.
J107C	J108C.
J107D	J108D.
J107E	J108E.
J107F	J108F.
J107–1	J108–4.
J107–6	J108–6.
J108A	J109A.
J108B	T101–9.
J108C	T101–10.
J108D	J109D.
J108E	J109E.
J108F	J109F.
J108–1	J109–4.
J108–6	J109–6.
J109A	J110A.
J109B	J110B.
J109C	J110C.
J109D	J110D.
J109E	J110E.
J109F	J110F.
J109–1	J110–4.
J109–6	J110–6.
J110A	J111A.
J110B	J111B.
J110C	J111C.
J110D	J111D.
J110E	J111E.
J110F	J111F.
J110–1	J111–4.
J110–6	J111–6.
J111B	T101–9.
J111C	T101–10.
J111D	R110, bottom terminal.
J111E	XY101, ground.
J112; on interior of rear panel.	S107A, terminal 1; on interior of rear panel.
J112, ground lug; on interior of rear panel.	S107A, terminal 3; on interior of rear panel.
L102, top; on TB101	XV113–9.
L103, bottom; on TB101	XV113–1.
M101, negative terminal; on rear of front panel.	R222, bottom; on TB101.
M101, positive terminal; on rear of front panel.	R215, ground; on rear of front panel.
R101, top terminal	R110, top terminal.
R104, R114 standoff	XV101–5.
R106, bottom terminal	R260, bottom; on TB101.
R109, arm	XV101–1.
R118, bottom; on TB102	XY101, ground.
R118, top; on TB102	XV103–2.
R121, top; on TB102	XV103–8.
R122, bottom; on TB102	S107B, terminal 2; on interior of rear panel.
R122, top; on TB102	XV103–1.
R123, bottom; on TB102	S107B, terminal 1; on interior of rear panel.
R123, top; on TB102	XV103–6.
R124, top; on TB102	XV103–7.
R124, R126; on TB102	S107A, terminal 2; on interior of rear panel.
R128, top; on TB102	XV104–2.
R132, top; on TB102	XV104–1.
R135, top; on TB102	XV104–7.
R138, top; on TB102	XV105–1.
R146, top; on TB102	XV106–1.
R154, bottom; on TB102	R155, arm; on rear of front panel.
R154, top; on TB102	XV106–7.
R158, top; on TB102	XV107–1.
R162, top; on TB102	XV107–6.
R167, top; on TB102	XV108–1.
R172, top; on TB102	XV108–6.
R173, bottom; on TB102	R174, arm; on rear of front panel.
R173, top; on TB102	XV108–7.
R174, left terminal; rear of front panel.	R155, left terminal; rear of front panel.
R174, right terminal; rear of front panel.	R155, right terminal; rear of front panel.
R177, top; on TB102	XV109–1.
R178, top; on TB102	XV109–6.
R183, bottom; on TB102	R185, arm; on rear of front panel.
R183, top; on TB102	XV109–7.
R185, left terminal; on rear of front panel.	R174, left terminal; on rear of front panel.
R187, top; on TB102	XV110–1.
R188, top; on TB102	XV110–6.
R193, bottom; on TB102	R204, left terminal; on rear of front panel.
R194, bottom; on TB102	R196, arm; on rear of front panel.
R194, top; on TB102	XV110–7.
R195, top; on TB102	XV111–1.
R196, left terminal; on rear of front panel.	R185, left terminal; on rear of front panel.
R196, right terminal; on rear of front panel.	R185, right terminal; on rear of front panel.
R197, bottom; on TB102	R228, bottom; on TB101.
R198, top; on TB102	XV111–6.
R204, left terminal; on rear of front panel.	R196, left terminal; on rear of front panel.
R204, arm; on rear of front panel.	R205, bottom; on TB102.
R204, right terminal	R196, left terminal; on rear of front panel.
R205, top; on TB102	XV111–7.
R211, arm; on rear of front panel.	S103B–1, terminal 3; on rear of front panel.
R211, right terminal; on rear of front panel.	R214, ground lug; on rear of front panel.
R213, bottom; on TB101	R214, left terminal; on rear of front panel.

From	To
R214, arm; on rear of front panel.	XV112-2.
R216, top; on TB101	XV112-6.
R218, top; on TB101	XV112-3.
R221, bottom; on TB101	XV114-2.
R221, R222; on TB101	XV114-1.
R223, top; on TB101	XV114-7.
R225, bottom; on TB101	XV115-6.
R225, top; on TB101	XV115-5.
R234, bottom; on TB101	S103A-1, terminal 4; on rear of front panel.
R234, bottom; on TB101	XV101, standoff.
R234, top; on TB101	XV116-6.
R235, top; on TB101	XV116-5.
R242, top; on TB101	XV118-5.
R244, bottom; on TB101	XV121-9.
R224, top; on TB101	XV119-6.
R248, top; on TB101	XV118-2.
R248, top; on TB101	XV119-7.
R249, top; on TB101	XV119-8.
R252, top; on TB101	XV119-1.
R254, top; on TB101	XV119-2.
R255, top; on TB101	XV120-1.
R260, top; on TB101	XV120-7.
R261, R264; on TB101	XV120-8.
R263, top; on TB101	XV120-2.
R266, top; on TB101	XV120-6.
R267, top; on TB101	XV121-2.
R268, top; on TB101	XV121-1.
R271, top; on TB101	XV121-7.
R272, bottom; on TB101	S106A, terminal 1; on rear of front panel.
R274, bottom; on TB101	R278, R289, thru lug; on TB101.
R274, top; on TB101	XV121-6.
R276, arm; on rear of front panel.	S106A, terminal 2; on rear of front panel.
R276, right terminal; on rear of front panel.	S105, top terminal; on rear of front panel.
R278, bottom; on TB101	S106B, terminal 2; on rear of front panel.
R279, top; on TB101	XV122-6.
R282, top; on TB101	XV122-1.
R283, bottom; on TB101	XV102-2.
R283, top, thru lug; on TB101	XV122-2.
R287, top; on TB101	XV123-5, 7.
R288, top; on TB101	XV123-1.
R291, bottom; on TB101	Plus 220-volt bus on Nixie board.
R291, top; on TB101	XV123-6.
S101-11; on rear of front panel.	XF101, center terminal; on rear of front panel.
S101-14; on rear of front panel.	T102-1.
S101-18; on rear of front panel.	T101-1.
S101-21; on rear of front panel.	XF102, center terminal; on rear of front panel.
S101-24; on rear of front panel.	T102-4.
S101-27; on rear of front panel.	XDS102, center terminal; on rear of front panel.
S101-28; on rear of front panel.	T101-4.
S102A, terminal 1; on interior of rear panel.	S102B, terminal 1; on interior of rear panel.
S102A, terminal 2; on interior of rear panel.	T101-3.
S102A, terminal 3; on interior of rear panel.	T101-1.
S102B, terminal 2; on interior of rear panel.	T101-2.
S102B, terminal 3; on interior of rear panel.	T101-4.
S102C, terminal 1; on interior of rear panel.	S102D, terminal 1; on interior of rear panel.
S102C, terminal 2; on interior of rear panel.	T102-3.
S102C, terminal 3; on interior of rear panel.	T102-1.
S102D, terminal 2; on interior of rear panel.	T102-2.
S102D, terminal 3; on interior of rear panel.	T102-4.
S103A-1, terminal 1; on rear of front panel.	S103A-1, terminal 2; on rear of front panel.
S103A-1, terminal 1; on rear of front panel.	S103A-2 terminal 2; on rear of front panel.
S103A-1, terminal 2; on rear of front panel.	S103A-1, terminal 3; on rear of front panel.
S103A-1, terminal 3; on rear of front panel.	S104, terminal W; on rear of front panel.
S103A-1, terminal 4; on rear of front panel.	S103A-2, terminal 3; on rear of front panel.
S103A-1, terminal 4; on rear of front panel.	L101, connected to S104 dummy lug; on rear of front panel.
S103A-2, terminal 1; on rear of front panel.	S103A-2, terminal 2; on rear of front panel.
S103A-2, terminal 3; on rear of front panel.	S103A-2, terminal 4; on rear of front panel.
S103B-1, terminal W; on rear of front panel.	XV112-7.
S103B-1, terminal 1; on rear of front panel.	S103B-1, terminal 5; on rear of front panel.
S103B-1, terminal 2; on rear of front panel .	S103B-1, terminal 3; on rear of front panel.
S103B-1, terminal 4; on rear of front panel.	S103, ground lug; on rear of front panel.
S106A, terminal 3; on rear of front panel.	XV122-7.
S106B, terminal 1; on rear of front panel.	XV121-2.
T101-11	XDS101, side terminal; on rear of front panel.
T101-11	XV102-8.
T101-11	XV104-4.
T101-11	XV105-4.

From	To
T101-12	XV102-7.
T101-12	XV104-9.
T101-12	XV105-9.
T102-3	XDS102, side terminal; on rear of front panel.
T102-5	XY101-7.
T102-6	XY101-3.
TB104, terminal 2; on interior of rear panel.	XF101; on rear of front panel.
TM104, terminal 3; on interior of rear panel.	XF102; on rear of front panel.
XDS103, center terminal; on rear of front panel.	XY101-1.
XDS103, side terminal; on rear of front panel.	XY101-3.
XV101-3	XV102-8.
XV101-3	XV120-5.
XV101-4	XV102-7.
XV101-4	XV120-9.
XV103-5	XV105-4.
XV103-9	XV105-9.
XV104-5	XV107-4.
XV104-9	XV107-9.
XV105-5	XV106-4.
XV105-9	XV106-9.
XV106-5	XV111-4.
XV106-9	XV111-9.
XV107-5	XV108-4.
XV107-9	XV108-9.

From	To
XV108-5	XV109-4.
XV108-9	XV109-9.
XV109-5	XV110-4.
XV109-9	XV110-9.
XV112-1	XV113-2.
XV112-4	XV116-3.
XV112-9	XV116-4.
XV113-3	XV115-1.
XV113-4	XV115-3.
XV113-5	XV122-4.
XV113-6	XV115-7.
XV113-8	XV115-4.
XV113-8	XV122-9.
XV114-3	XV115-3.
XV114-4	XV115-4.
XV116-3	XV117-3.
XV116-4	XV117-4.
XV116-7	XV117-2.
XV117-3	XV120-4.
XV117-4	XV120-9.
XV118-3	XV120-5.
XV118-4	XV120-9.
XV118-7	XV120-2.
XV119-4	XV121-5.
XV119-9	XV121-8.
XV121-4	XV122-4.
XV121-8	XV122-9.

Section II. ADJUSTMENTS

Note. Adjustment of the five TIME BASE ADJUSTMENTS potentiometers is described in paragraph 17, TM 11-6625-218-12.

54. Adjustment of +120-volt Regulated Supply

a. Remove tube V113 from its socket on top of the frequency-meter chassis, permitting access to a convenient +120-volt circuit point.

b. Connect the positive lead of the multimeter, set on its appropriate dc scale, to pin 1 of the tube socket. Connect the negative lead to ground. Apply power to the equipment and wait 1 minute for warmup.

c. Adjust the +120V ADJ. control R109 (fig. 27), for an indication of +120 volts on the multimeter.

d. Remove power, disconnect the multimeter, and replace V113 in its socket.

55. Setting FREQ. ADJ. Capacitor C119

Whenever crystal Y101 or oscillator tube V103 is replaced, the following procedure will ensure a precise 100-kc frequency output from the oscillator stage:

a. Connect a suitably accurate 100-kc signal source (maximum error 1 cycle in 100,000) to the horizontal plates of the oscilloscope. Frequency Calibrator AN/URM-18 can be used, if available. Connect the vertical plates of the oscilloscope across pin 6 of tube V104 and ground to isolate the oscillator stage from the measuring circuits.

b. Adjust the screw of FREQ. ADJ. capacitor C119 (fig. 27) until the Lissajous figure on the oscilloscope indicates that the frequencies are identical. Remove the screwdriver, and recheck the pattern on the oscilloscope. Readjust C119, if necessary, to obtain the proper one-to-one ratio Lissajous figure.

CHAPTER 4

FINAL TESTING

56. Purpose of Final Testing

The tests outlined in this section are designed to measure the performance capability of a repaired frequency meter. Equipment that meets the minimum standards stated in the tests will furnish satisfactory operation, equivalent to that of new equipment.

57. Test Equipment Required for Final Testing

In addition to the test equipment listed in paragraph 40, the following items are required for final testing:

a. A receiver capable of receiving station WWV 10-mc signals.

b. Frequency Calibrator AN/URM–18, or equivalent 1-mc signal source, such as a crystal-controlled, adjustable 1-mc oscillator.

c. Transformer, Variable CN–16/U or equivalent.

d. Pulse Generator AN/UPM–15, or equivalent.

e. A mechanical stopwatch.

f. A spare Frequency Meter AN/TSM–16, known to be operating satisfactorily, or any other source of accurate 1-second timing interval pulses is satisfactory.

g. A three-position rotary switch, two 470-ohm resistors, and one 47-ohm resistor. (These are shown in figure 38 as S1, R2, R3, and R1, respectively.)

58. Frequency Range, Sensitivity, and Accuracy Tests

a. Connect the frequency meter under test and items of test equipment as shown in figure 37.

b. Calibrate the 1-mc output of the frequency calibrator or signal source against the WWV 10-mc signal.

Note. A one-cycle per second beat between the two signals represents an error of 1/10 part per million. This accuracy is acceptable for testing the frequency meter.

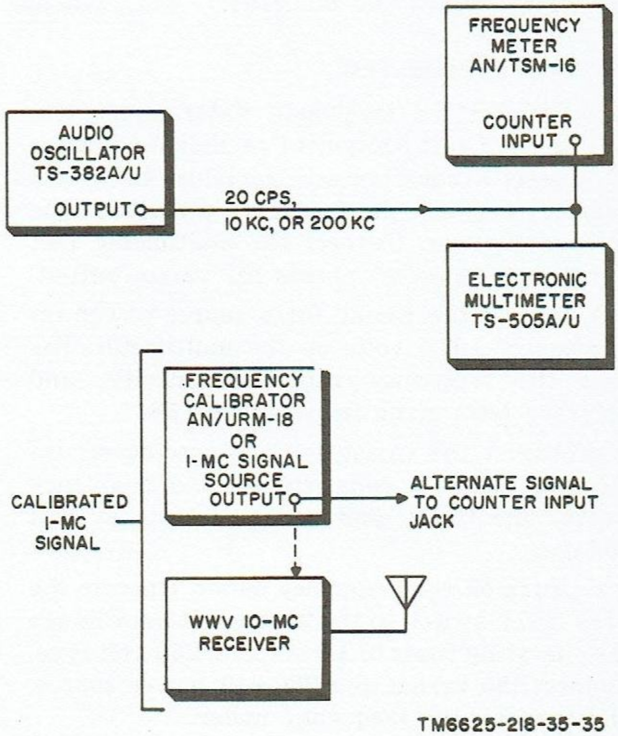


Figure 37. Test setup for frequency range, sensitivity, and accuracy tests.

c. Set the audio oscillator successively to 20 cps, 10 kc, and 200 kc. Adjust the audio oscillator for 0.2-volt output at each frequency, as indicated on the vtvm. The INPUT LEVEL meter pointer should deflect within the green area of the scale by a slight amount at each of the three check frequencies. It may be necessary to reset the TRIGGER VOLTAGE control at the different check frequencies.

d. Repeat *c* above with the audio oscillator adjusted for maximum output (approximately 10 volts) at each frequency. The INPUT LEVEL meter pointer should deflect into the red area of the scale, and counterclockwise rotation of the SENSITIVITY control should reduce the amount of pointer deflection.

e. Disconnect the output cable of the audio oscillator. Connect the signal-source output to the frequency meter. Adjust the output of the signal source to exactly 1 megacycle.

Note. Since the 1-megacycle frequency imposes the severest requirements on the frequency meter, accuracy measurement at this frequency only is sufficient.

f. Rotate the TIME-SECONDS switch to the 1 position. The reading on the numerical indicators should be within .001% of 1 million (between 999,990 and 000,010).

59. Line Voltage Test

a. Connect the frequency meter under test and items of test equipment as shown in figure 37. Insert Transformer, Variable CN–16/U (variac) between the frequency meter and the ac source power. Connect the multimeter (set to measure ac volts) across the variac output.

b. Adjust the variac for a source-power indication of 103.5 volts on the multimeter. Repeat the frequency range, sensitivity, and accuracy tests given in paragraph 58.

c. Adjust the variac for a source-power indication of 126.5 volts. Repeat the frequency range, sensitivity, and accuracy tests at this voltage.

d. Turn off the frequency meter. Operate the 115V-230V switch to the 230V position. Change the operating fuses to 1.6 ampere, 250-volt type. Connect the variac to a 230-volt power source, and turn on the frequency meter.

e. Adjust the variac for a source-power indication of 20 volts on the multimeter. Repeat the frequency range, sensitivity, and accuracy tests at this voltage.

f. Adjust the variac for a source-power indication of 253 volts on the multimeter. Repeat the frequency range, sensitivity, and accuracy tests at this voltage.

g. Turn off the frequency meter. Operate the 115V-230V switch to the 115V position. Change the operating fuses to 3.2 ampere, 125-volt type, and reconnect the frequency meter to the 115-volt power source.

60. Display Time Test

a. Turn on the frequency meter under test and set the FUNCTION switch to the TEST position.

b. Rotate the DISPLAY TIME control fully counterclockwise; use the stop watch and check to see that the numerical indicators have a display time shorter than 1 second.

c. Rotate the DISPLAY TIME control fully clockwise, and check to see that a display time longer than 5 seconds is obtained.

61. Time Interval Test

a. Connect the frequency meter under test and items of test equipment as shown in figure 38.

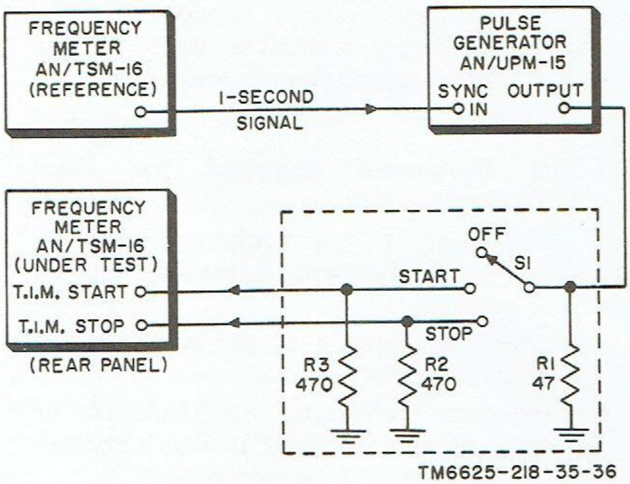


Figure 38. Test setup for time interval test.

b. Rotate the TIME-SECONDS switch on the *reference* frequency meter to the 1 position. Connect the cable from the SYNC IN receptacle on Pulse Generator AN/UPM–15 to terminal 2 (the 1 position) of TIME-SECONDS switch S104 on the *reference* frequency meter.

c. Adjust the pulse generator for 3 volts negative output, and adjust its pulse width to 0.2 microsecond.

d. Reset the frequency meter under test. Rotate switch S1 (fig. 38) from OFF to START and then to STOP within 1 second. The frequency meter under test should indicate 100,000 (±1 count).

e. Repeat the procedures given in *c* and *d* above; use 3 volts negative output and a pulse width of 10 microseconds from the pulse generator.

f. Repeat the procedures given in *c* and *d* above; use 8 volts negative output and a pulse width of 0.2 microsecond from the pulse generator.

g. Repeat the procedures given in *c* and *d* above; use 8 volts negative output and a pulse width of 10 microseconds from the pulse generator.

62. External 100-kc Input Test

a. Connect the frequency meter under test and items of test equipment as shown in figure 39.

b. Set the audio oscillator to exactly 100 kc (calibrated) and adjust its output to 2 volts as indicated on the vtvm.

c. Operate the INT.-EXT. switch, on the rear panel of the frequency meter, to the EXT. position. Rotate the FUNCTION switch to the TEST position. The numerical indicators should indicate 100,000 (±1 count).

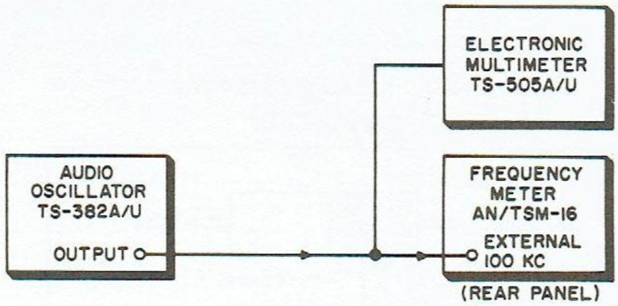
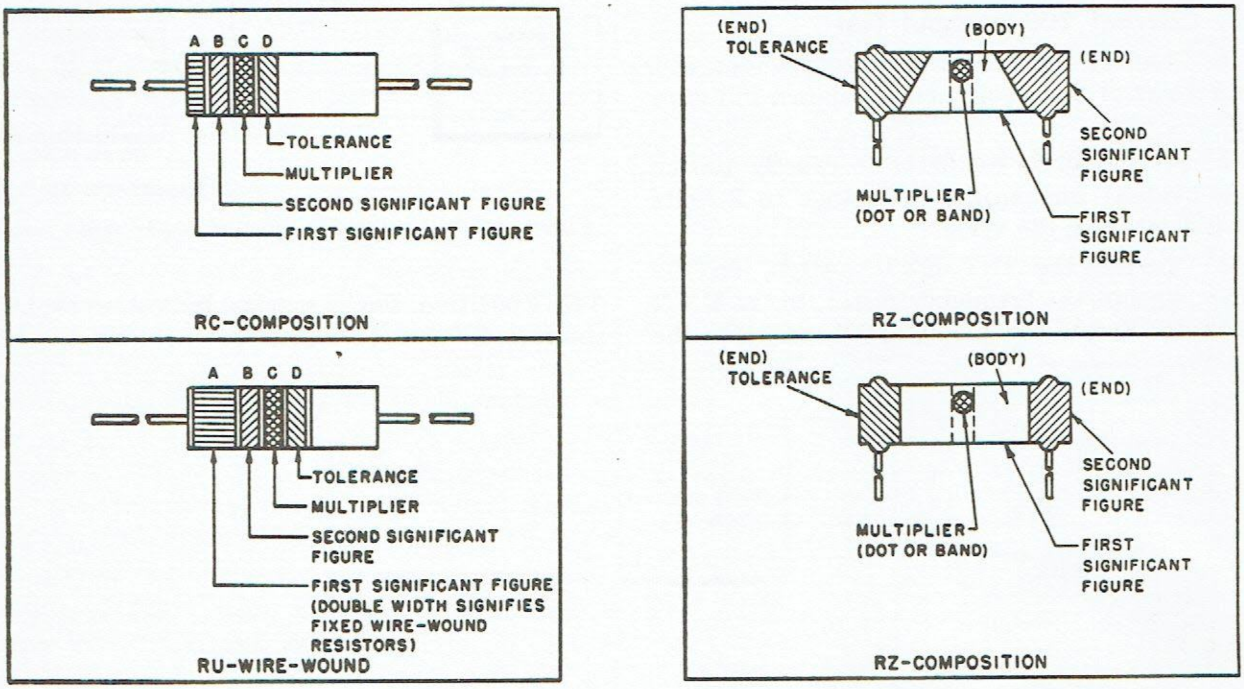


Figure 39. Test setup for external 100-kc input test.

RESISTOR COLOR CODE MARKING
(MIL-STD RESISTORS)

AXIAL-LEAD RESISTORS (INSULATED) | RADIAL-LEAD RESISTORS (UNINSULATED)



RESISTOR COLOR CODE

BAND A OR BODY*		BAND B OR END*		BAND C OR DOT OR BAND*		BAND D OR END*	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
BLACK	0	BLACK	0	BLACK	1	BODY	± 20
BROWN	1	BROWN	1	BROWN	10	SILVER	± 10
RED	2	RED	2	RED	100	GOLD	± 5
ORANGE	3	ORANGE	3	ORANGE	1,000		
YELLOW	4	YELLOW	4	YELLOW	10,000		
GREEN	5	GREEN	5	GREEN	100,000		
BLUE	6	BLUE	6	BLUE	1,000,000		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7				
GRAY	8	GRAY	8	GOLD	0.1		
WHITE	9	WHITE	9	SILVER	0.01		

*FOR WIRE-WOUND-TYPE RESISTORS, BAND A SHALL BE DOUBLE-WIDTH. WHEN BODY COLOR IS THE SAME AS THE DOT (OR BAND) OR END COLOR, THE COLORS ARE DIFFERENTIATED BY SHADE, GLOSS, OR OTHER MEANS.

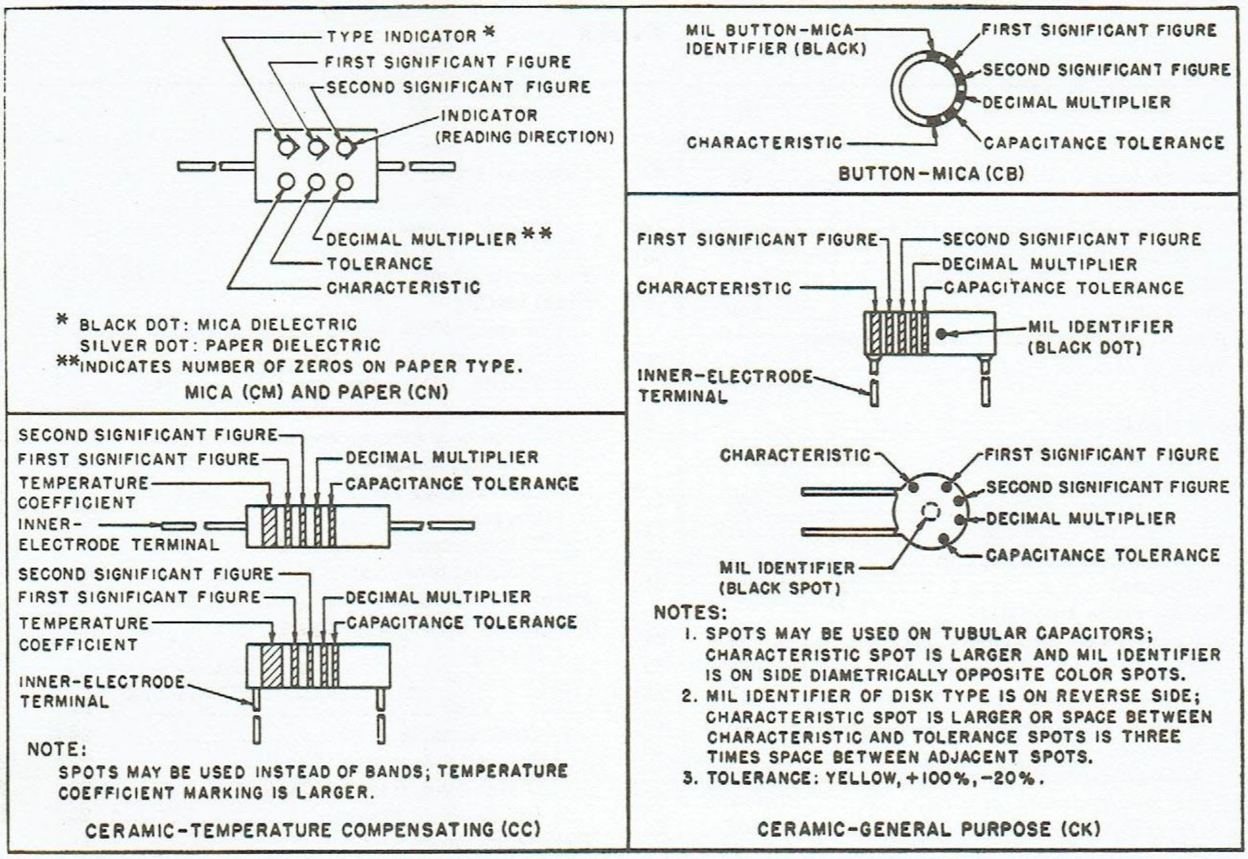
EXAMPLES (BAND MARKING):
10 OHMS ±20 PERCENT: BROWN BAND A; BLACK BAND B; BLACK BAND C; NO BAND D.
4.7 OHMS ±5 PERCENT: YELLOW BAND A; PURPLE BAND B; GOLD BAND C; GOLD BAND D.

EXAMPLES (BODY MARKING):
10 OHMS ±20 PERCENT: BROWN BODY; BLACK END; BLACK DOT OR BAND; BODY COLOR ON TOLERANCE END.
3,000 OHMS ±10 PERCENT: ORANGE BODY; BLACK END; RED DOT OR BAND; SILVER END.

STD-R1

Figure 40. MIL–STD resistor color-code markings.

CAPACITOR COLOR CODE MARKING
(MIL-STD CAPACITORS)



CAPACITOR COLOR CODE

COLOR	SIG FIG.	MULTIPLIER		CHARACTERISTIC[1]				TOLERANCE [2]					TEMPERATURE COEFFICIENT (UUF/UF/°C)
		DECIMAL	NUMBER OF ZEROS	CM	CN	CB	CK	CM	CN	CB	CC OVER 10UUF	CC 10UUF OR LESS	CC
BLACK	0	1	NONE		A			20	20	20	20	2	ZERO
BROWN	1	10	1	B	E	B	W				1		-30
RED	2	100	2	C	H		X	2		2	2		-80
ORANGE	3	1,000	3	D	J	D			30				-150
YELLOW	4	10,000	4	E	P								-220
GREEN	5		5	F	R						5	0.5	-330
BLUE	6		6		S								-470
PURPLE (VIOLET)	7		7		T	W							-750
GRAY	8		8			X						0.25	+30
WHITE	9		9								10	1	-330(±500) [3]
GOLD		0.1						5		5			+100
SILVER		0.01						10	10	10			

1. LETTERS ARE IN TYPE DESIGNATIONS GIVEN IN MIL-C SPECIFICATIONS.
2. IN PERCENT, EXCEPT IN UUF FOR CC-TYPE CAPACITORS OF 10 UUF OR LESS.
3. INTENDED FOR USE IN CIRCUITS NOT REQUIRING COMPENSATION.

STD-C1

Figure 41. MIL-STD capacitor color-code markings.

INDEX

Figure 42. Clock pulse generator and clock counter, schematic diagram.

TM6625-218-35-41

Figure 43. Input, gate, and reset circuits, schematic diagram.

Figure 44. 1-mc counter, 100-kc counter, and numerical indicator circuits, schematic diagram.

[AG 413.6 (15 Dec 59)]

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OS Sup Agcy (1)
Yuma Test Sta (2)
USA Elct PG (1)
Sig Lab (5)
Sig Fld Maint Shops (3)
USA Corps (Res) (1)
JBUSMC (2)
Units org under fol TOE:

11–5 (2)
11–6 (2)
11–7 (2)
11–16 (2)
11–55 (2)
11–56 (2)
11–57 (2)
11–97 (2)
11–98 (2)
11–117 (2)
11–155 (2)
11–500 (AA–AE) (2)
11–557 (2)
11–587 (2)
11–592 (2)
11–597 (2)

NG: State AG (3)

USAR: None

For explanation of abbreviations used, see AR 320–50.

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