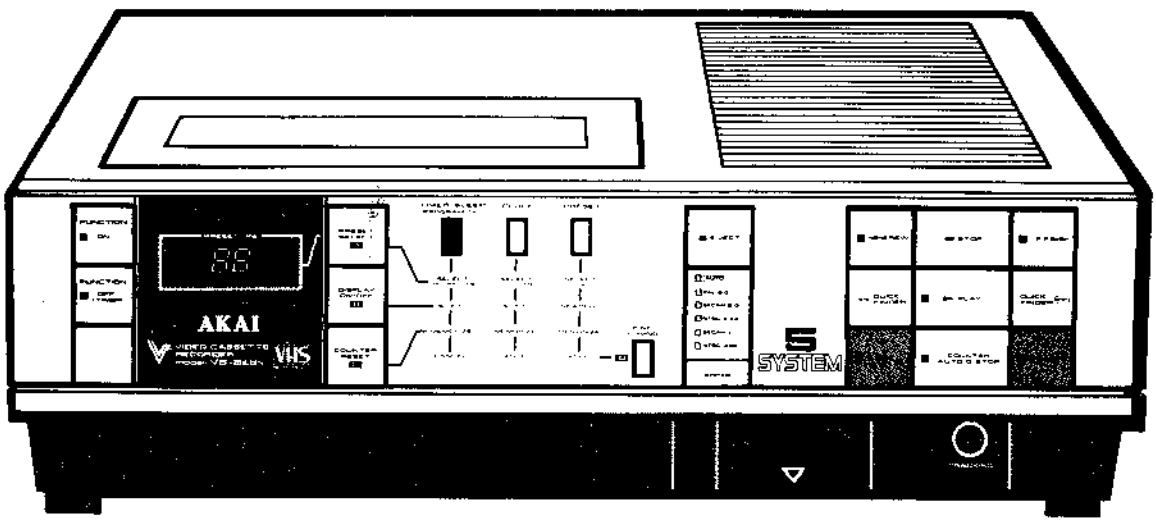
AKAI SERVICE MANUAL

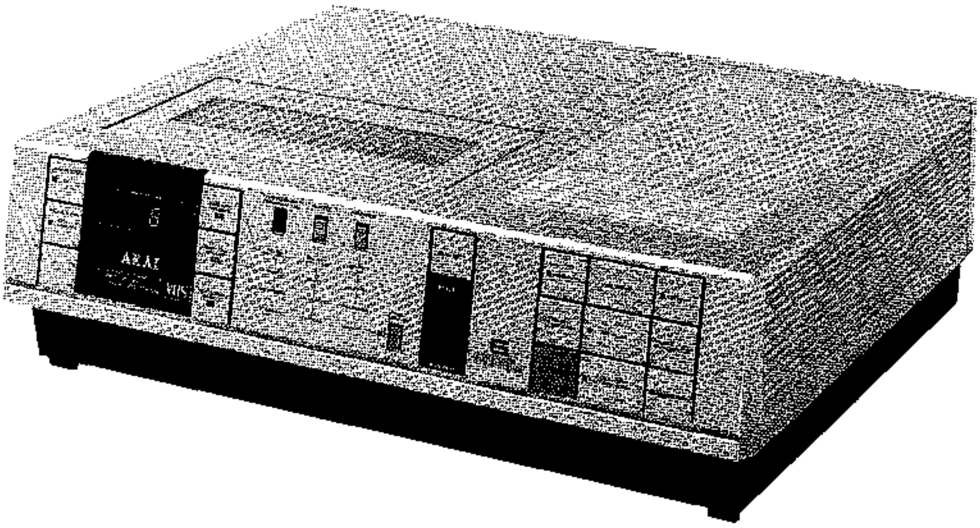
VS-2EGN



VIDEO CASSETTE RECORDER

MODEL **VS-2EGN** (5 System)

pers. Eigentum
von R2 D2
Juana-Massah-Sir



VIDEO CASSETTE RECORDER

MODEL VS-2EGN(5 System)

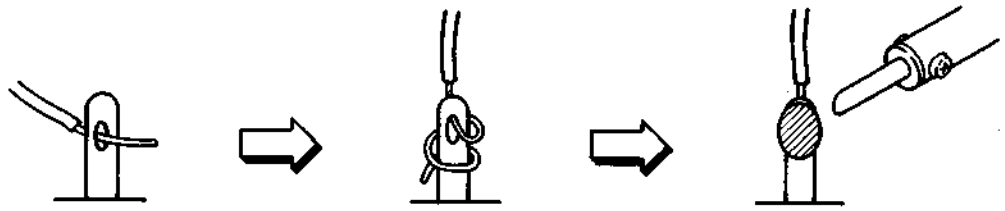
SAFETY INSTRUCTIONS

SAFETY CHECK AFTER SERVICING

Confirm the specified insulation resistance between power cord plug prongs and externally exposed parts of the set is greater than 10 Mohms, but for equipment with external antenna terminals (tuner, receiver, etc.) and is intended for [C] or [A], specified insulation resistance should be more than 2.2 Mohms (ground terminals, microphone jacks, headphone jacks. line-in-out jacks etc.)

PRECAUTIONS DURING SERVICING

1. Parts identified by the ⚠ symbol parts are critical for safety.
   Replace only with parts number specified.
2. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
   Examples: RF converters, tuner units, antenna selector switches, RF cables, noise blocking capacitors, noise blocking filters, etc.
3. Use specified internal wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
4. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulation Tape
   2) PVC tubing
   3) Spacers (Insulating Barriers)
   4) Insulation sheets for transistors
   5) Plastic screws for fixing microswitch (especially in turntable)
5. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



6. Observe that wires do not contact heat producing parts (heatsinks, oxide metal film resistors, fusible resistors, etc.).
7. Check that replaced wires do not contact sharp edged or pointed parts.
8. Also check areas surrounding repaired locations.
9. Use care that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

SECTION 1

SERVICE MANUAL

TABLE OF CONTENTS

For basic adjustments, measuring methods, and operating principles, refer to GENERAL TECHNICAL MANUAL.

I . SPECIFICATIONS

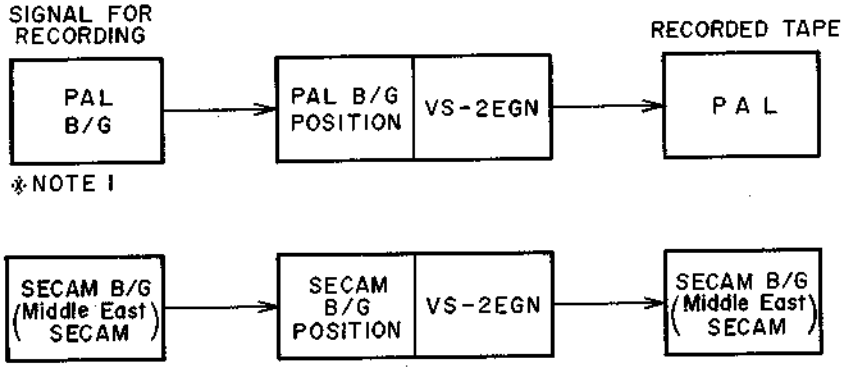
FORMAT	VHS Standard
VIDEO RECORDING SYSTEM	Rotary, slant azimuth two-head helical scan system
RF INPUT	System B, G (PAL, SECAM) VHF Ch 2 to 12 UHF Ch 21 to 69
RF OUTPUT	System G type modulation UHF Ch 30 to 39 adjustable (preset to Ch 36)
RECORDING (LINE INPUT)	PAL, System B, G, I SECAM, System B, G NTSC, 4.43 MHz NTSC, 3.58 MHz
PLAYBACK (LINE OUTPUT)	PAL, System B, G, I SECAM, System B, G SECAM, System L NTSC, 4.43 MHz NTSC, 3.58 MHz
VIDEO	
LINE INPUT LEVEL	0.5 to 2.0 Vp-p/75 ohms unbalanced
LINE OUTPUT LEVEL	1.0 Vp-p/75 ohms unbalanced
S/N	More than 43 dB
HORIZONTAL RESOLUTION	More than 250 lines (PAL) More than 220 lines (SECAM) More than 220 lines (NTSC)
AUDIO	
LINE INPUT LEVEL	–20 dBs/50 kohms unbalanced
LINE OUTPUT LEVEL	–6 dBs/1 kohm unbalanced
S/N	More than 40 dB
FREQUENCY RESPONSE	70 Hz to 8 kHz
RECORDING OR PLAYBACK TIME	240 min. with E-240 cassette (PAL, SECAM) 168 min. with E-240 cassette (NTSC) 160 min. with T-160 cassette (NTSC)
TAPE SPEED	23.39 mm/sec. (PAL, SECAM) 33.35 mm/sec. (NTSC, "standard play" mode only)
QUICK FINDER	
PAL/SECAM	Approx. 7 times the normal speed (noise bars fixed)
NTSC	Approx. 5 times the normal speed (noise bars fixed)
FF., RWD TIME	4 min. with E-240 cassette
TIMER	
PROGRAMS	Nine 4-week-one time memory programs and one shut-off program
CLOCK REFERENCE	Locked to power line frequency (50/60 Hz)
DISPLAY	TV screen (Tape counter, Timer, Clock and Calendar)
POWER REQUIREMENTS	110 (100–120)/220 (200–240)V, 50/60 Hz
POWER CONSUMPTION	45 watts
OPERATING TEMPERATURE	5°C to 40°C
DIMENSIONS	440(W) x 133(H) x 360(D) mm
WEIGHT	10.5 kg

* For improvement purposes, design and specifications are subject to change without notice.

II. OPERATING PROCEDURE

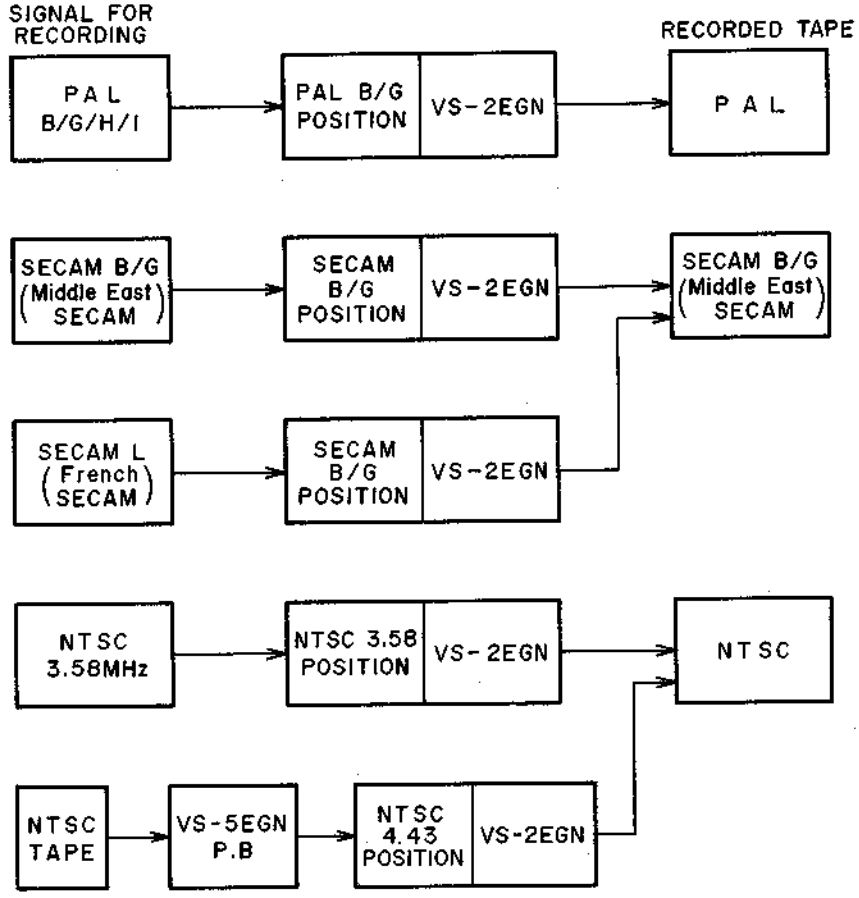
1. RECORDING

1) From built-in Tuner (To record TV programs)



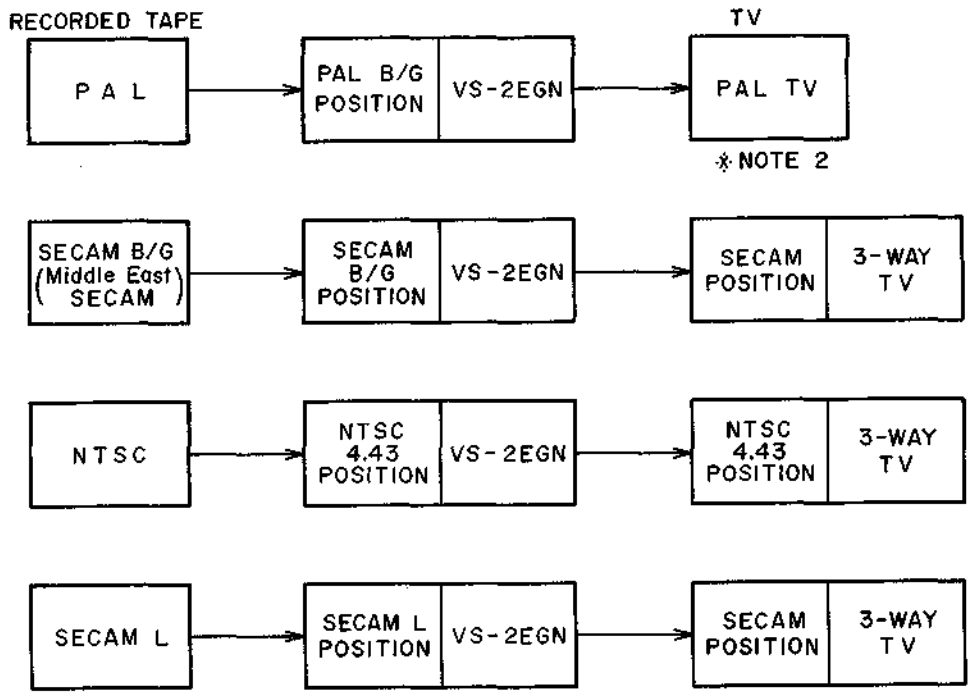
※NOTE I : The PAL I color system which is used in U.K and Hong Kong cannot be recorded through the built-in tuner.

2) From source connected to VIDEO IN jack



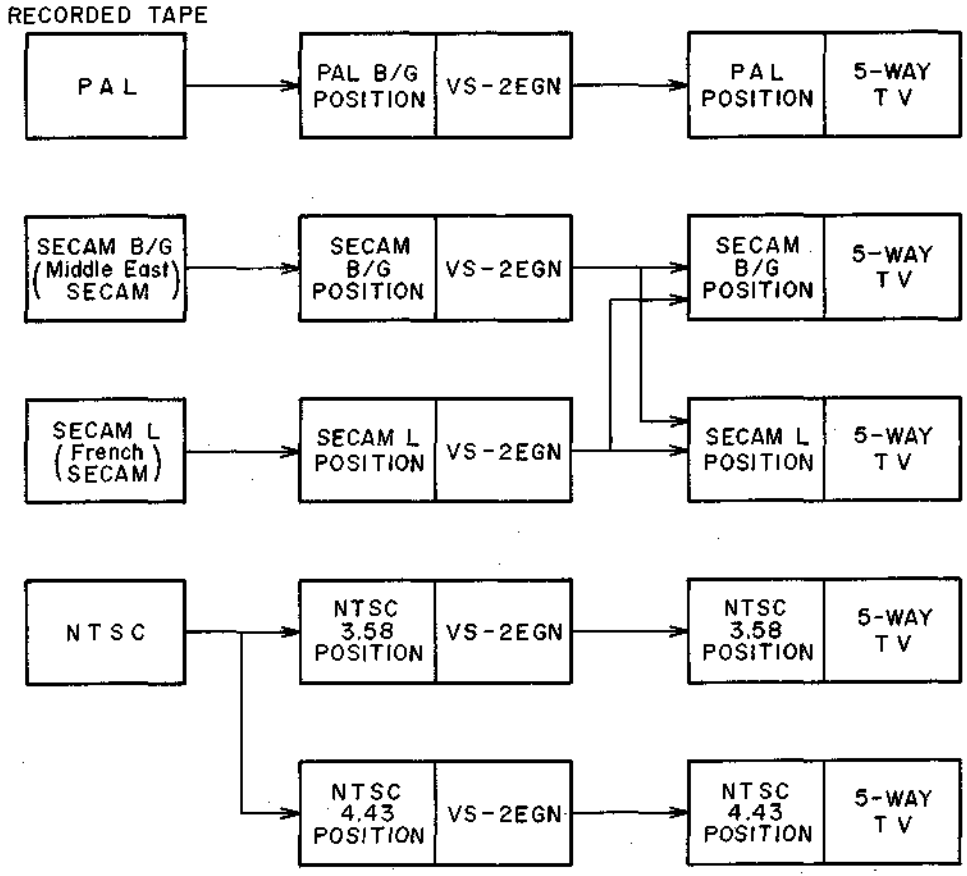
2. PLAYBACK

1) On TV connected to RF OUT jack



※NOTE 2 : Use a TV which can receive the PAL B/G color system. If a TV which can receive the PAL I color system in used no sound will be heard.

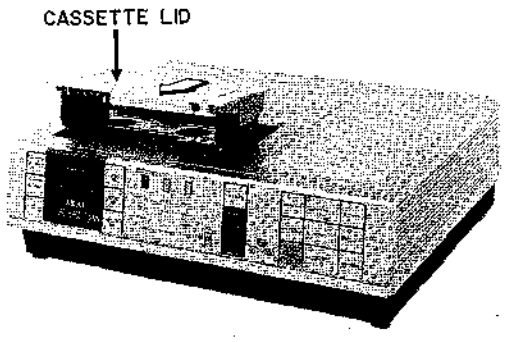
2) On TV connected to VIDEO OUT jack



III. DISMANTLING OF UNIT

In case of trouble, etc. necessitating dismantling, please dismantle in the order shown in the photographs. Reassemble in reverse order.

1



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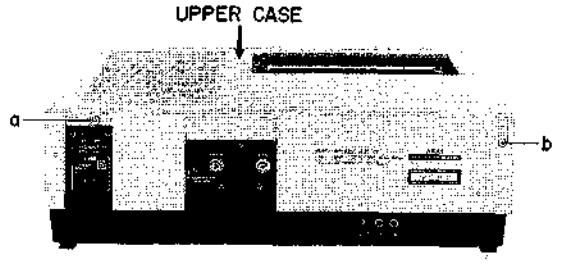
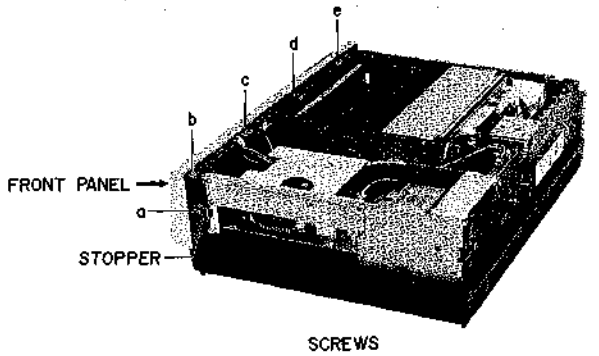
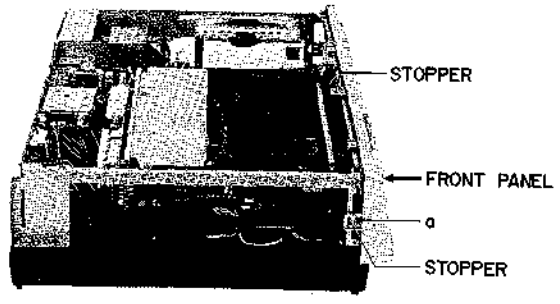


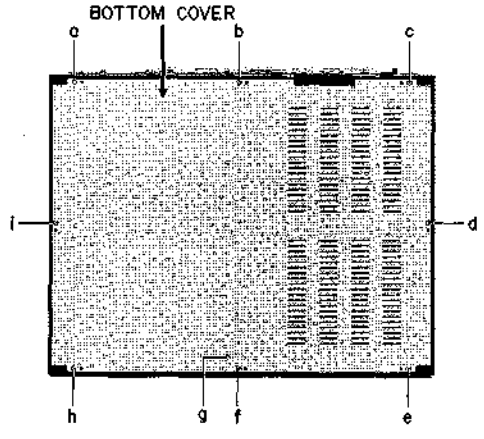
3



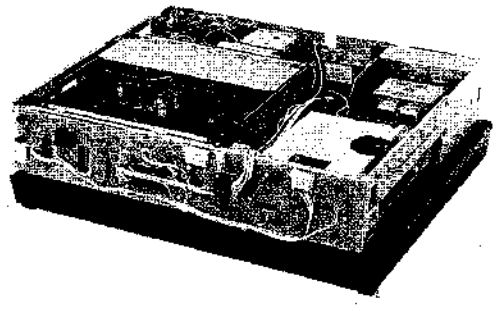
4



5



6



IV. CONTROLS

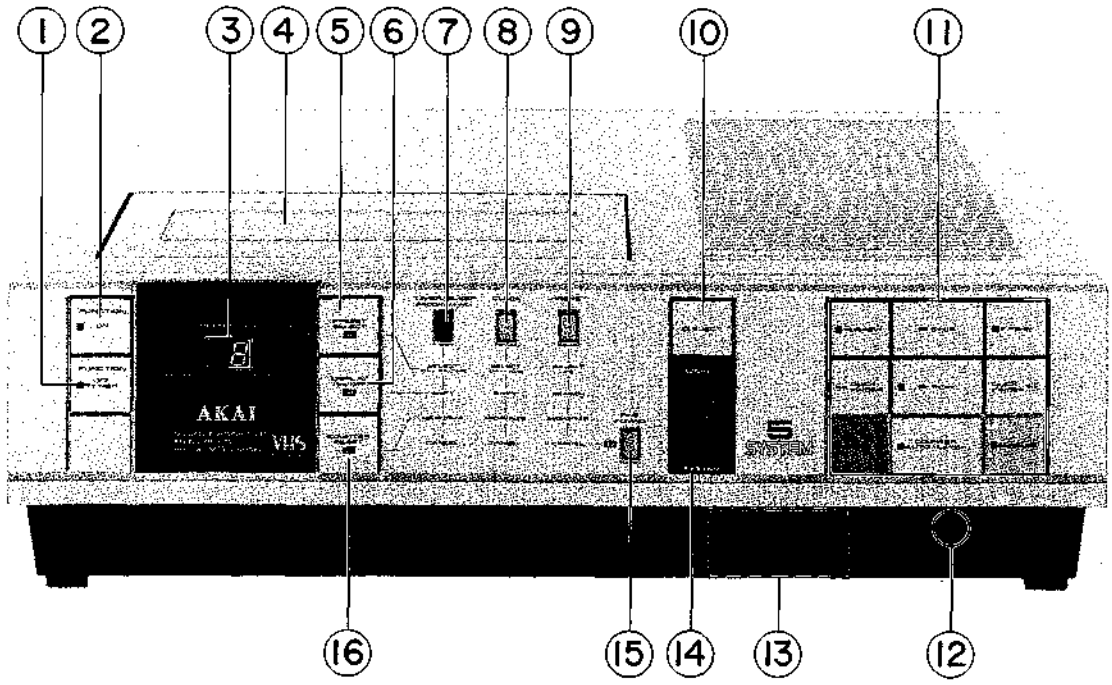


Fig. 4-1 Controls (Front View)

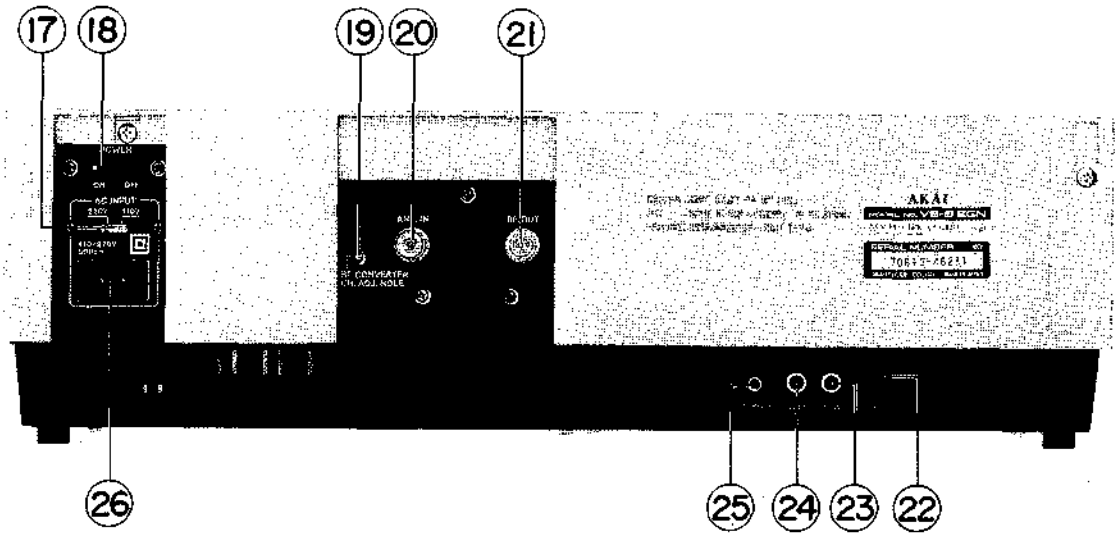


Fig. 4-2 Controls (Rear View)

1. FUNCTION "OFF/TIMER" BUTTON
2. FUNCTION "ON" BUTTON
3. PRESET (PS) STATION DISPLAY
4. CASSETTE HOLDER
5. PRESET SELECT (A) BUTTON
6. DISPLAY ON/OFF (B) BUTTON
7. TIMER/SLEEP PROGRAM NO. BUTTON
8. CLOCK BUTTON
9. PRESET BUTTON
10. EJECT BUTTON
11. TAPE TRANSPORTING BUTTON
    REWIND (◀◀ REW), STOP (■ STOP),
    FAST FORWARD (F.F ▶▶),
    QUICKFINDER REVERSE (◀◀ QUICK FINDER),
    PLAY (▶ PLAY),
    QUICKFINDER FORWARD (QUICK FINDER ▶▶),
    RECORDING (● REC),
    COUNTER "0" STOP, PAUSE (▮▮ PAUSE)
12. TRACKING CONTROL
13. COMPARTMENT FOR THE OPTIONAL REMOTE CONTROL UNIT RC-V202
14. COLOR SYSTEM SELECTOR
15. FINE TUNING (D) BUTTON
16. COUNTER RESET (C) BUTTON
17. AC INPUT SELECTOR
18. POWER ON/OFF SWITCH
19. RF CONVERTER CHANNEL (CH.) ADJUSTMENT (ADJ.) HOLE
20. ANTENNA (ANT.) IN JACK
21. RF OUT JACK
22. AUDIO JACK
23. VIDEO IN JACK
24. VIDEO OUT JACK
25. REMOTE PAUSE JACK
26. AC INLET
27. TV/VIDEO BUTTON (EA MODEL ONLY)

V. PRINCIPAL PARTS LOCATION

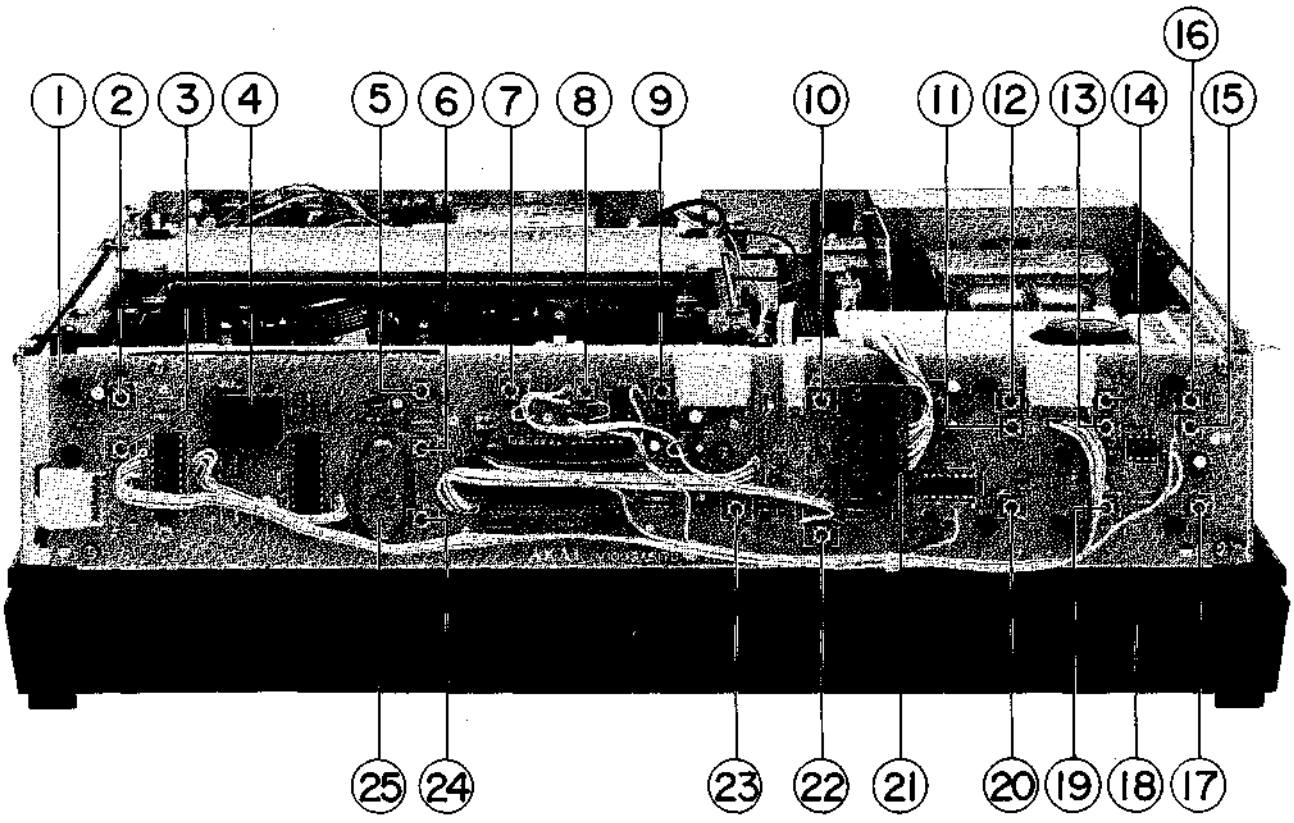


Fig. 5-1 Parts Location (Front View)

1. OPERATION P.C BOARD V1009A5170
2. FUNCTION ON SWITCH
3. FUNCTION OFF/TIMER SWITCH
4. DIGITAL DISPLAY
5. PRESET SELECTOR (A) SWITCH
6. DISPLAY ON/OFF (B) SWITCH
7. TIMER/SLEEP/PROGRAM NO. SWITCH
8. CLOCK SWITCH
9. PRESET SWITCH
10. EJECT SWITCH
11. QUICK FINDER REVERSE SWITCH
12. REWIND SWITCH
13. PLAY SWITCH
14. STOP SWITCH
15. QUICK FINDER FORWARD SWITCH
16. FAST FORWARD SWITCH
17. PAUSE SWITCH
18. TRACKING VOLUME
19. COUNTER AUTO "0" STOP SWITCH
20. REC SWITCH
21. LED P.C BOARD V1009D5320
22. SYSTEM SWITCH
23. FINE TUNING (D) SWITCH
24. COUNTER RESET (C) SWITCH
25. BACK UP BATTERY

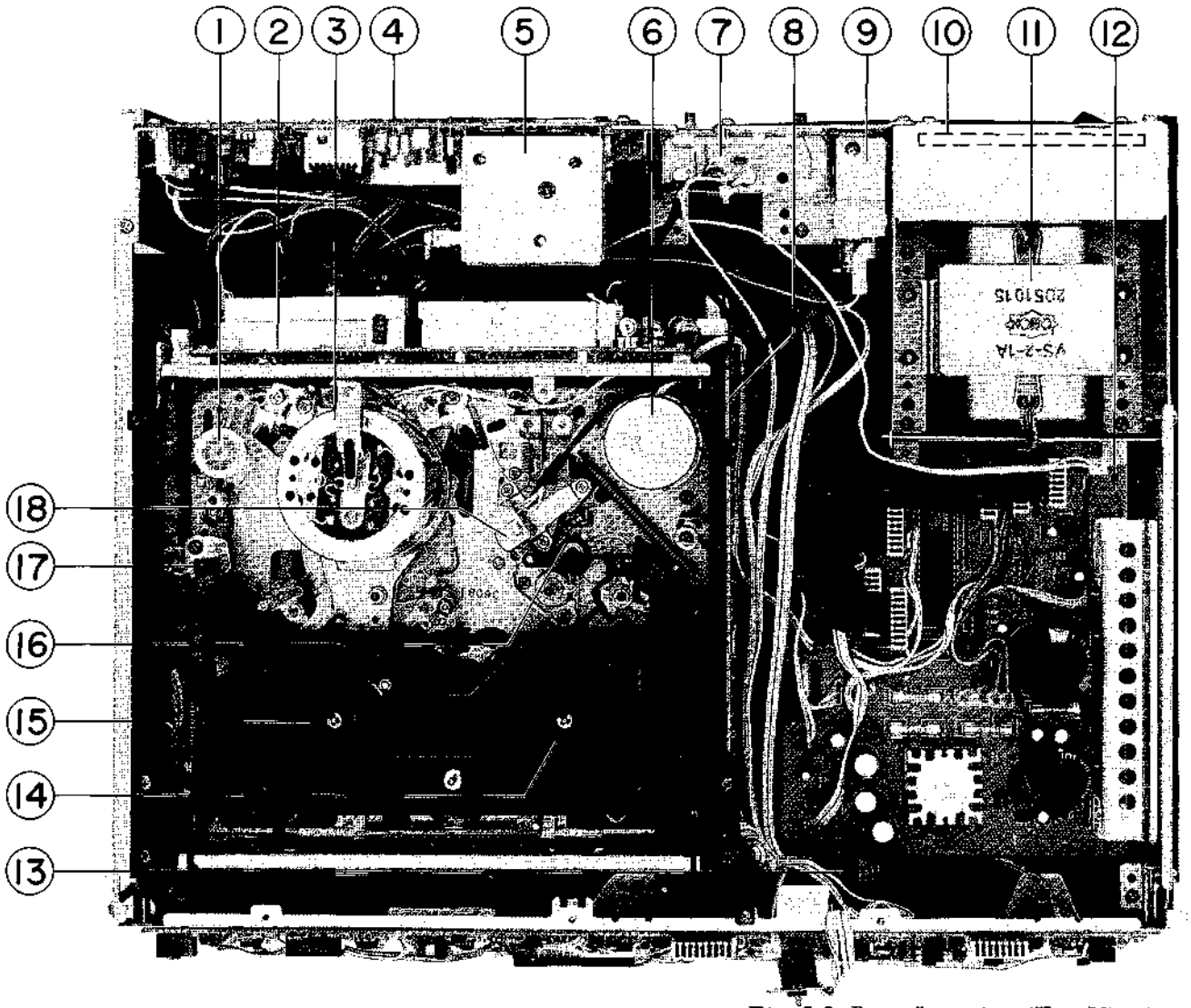


Fig. 5-2 Parts Location (Top View)

1. S. IMPEDANCE ROLLER
2. AUDIO/PRE P.C BOARD V1009A5180
3. DRUM HEAD BLOCK
4. DEMODULATOR P.C BOARD
5. TV TUNER UNIT
6. CAPSTAN MOTOR
7. ANTENNA BOOSTER
8. MECH DRIVE P.C BOARD V1009A519B
9. RF CONVERTER
10. POWER FILTER P.C BOARD V1009D5210
11. POWER TRANSFORMER
12. POWER & SYSCON P.C BOARD V1009A519A
13. SOCKET FOR THE OPTIONAL REMOTE CONTROL UNIT RC-V202
14. TAKE UP REEL
15. SUPPLY REEL
16. PINCHROLLER
17. FULL ERASE HEAD
18. AUDIO/CONTROL HEAD

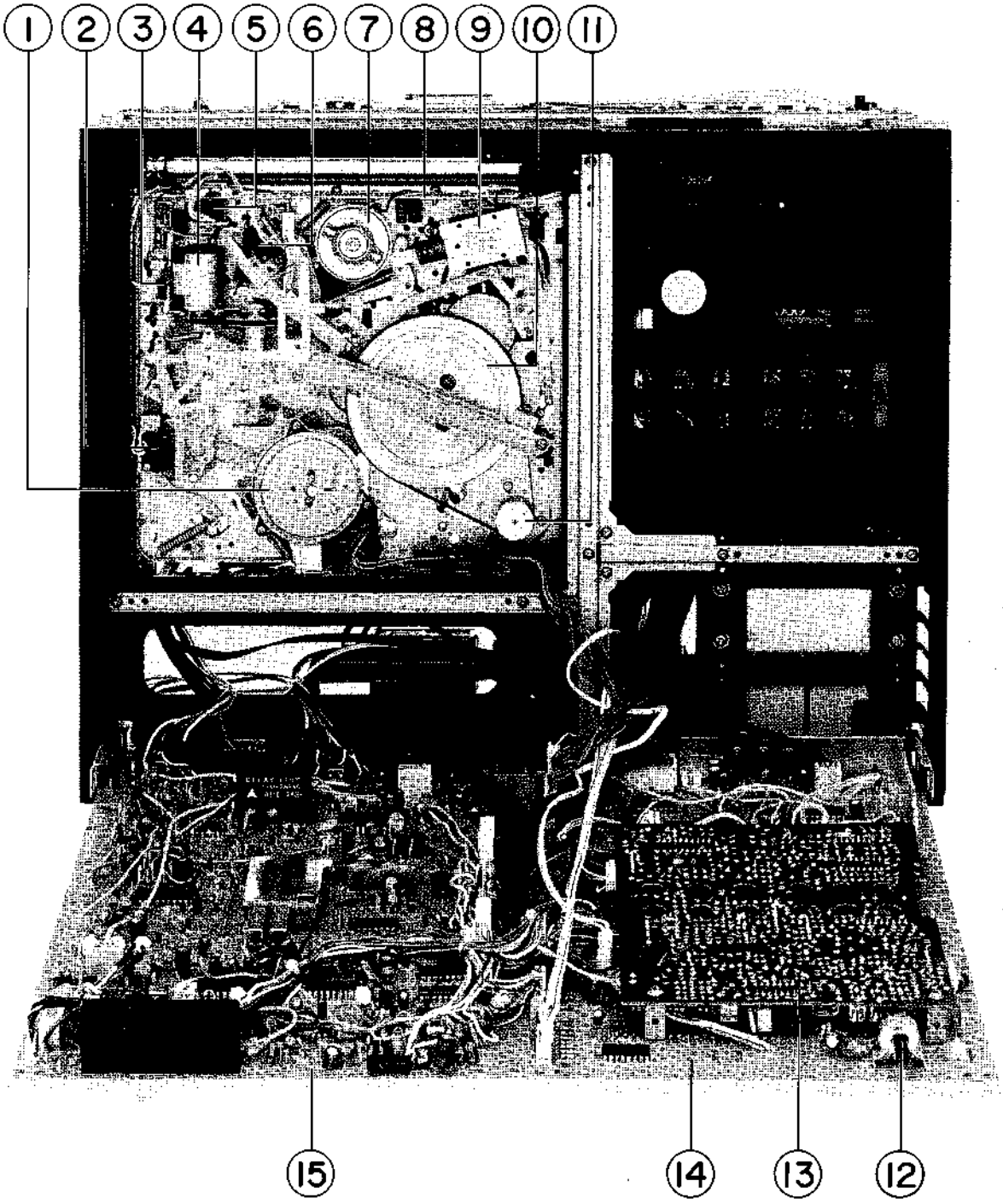


Fig. 5-3 Parts Location

1. DRUM MOTOR
2. LOADING SWITCH A
3. EJECT SWITCH
4. LOADING MOTOR
5. REC. SAFETY SWITCH
6. LOADING SWITCH B
7. REEL MOTOR
8. INTERMEDIATE P.C BOARD V1009A519C
9. PLUNGER
10. CAPSTAN FLYWHEEL
11. CAPSTAN MOTOR
12. TRACKING VOLUME
13. EGN P.C BOARD
14. SERVO (EGN) P.C BOARD
15. VIDEO (EGN) P.C BOARD

VI. VOLTAGE CONVERSION

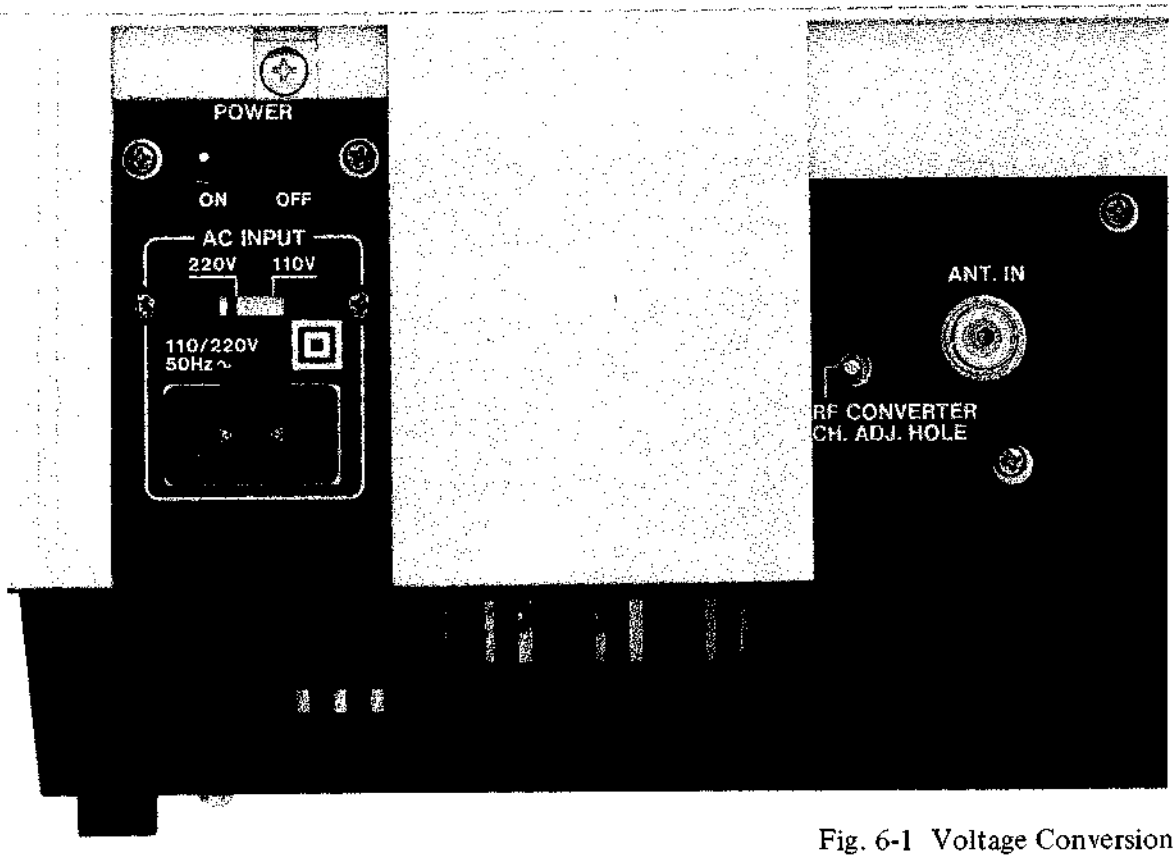


Fig. 6-1 Voltage Conversion

Power requirements for electrical equipment differ from area to area. The operating voltage of VS-2EGN is preset to 220V. Before connecting, check that the AC INPUT selector on the rear panel is set to the voltage for your area:
110V, 50 Hz for other countries. If the AC INPUT is not set for your area:

1. Confirm that the POWER Switch on the rear panel is set to OFF.
2. Confirm that the POWER Cord is disconnected.
3. Move the AC INPUT selector with a screwdriver so that the marker is above the voltage for your area.

VII. CIRCUIT DESCRIPTION

TV system	Scanning lines/ field frequency (With respect to B-Y)	Line Frequency fH (Hz)	TV-CH frequency spectrum	Sound Modulation	Video Modulation	Colour System	Subcarrier frequency (MHz)	Modulation system	Phase of Burst With respect to B-Y
B (VHF)	625/50	15,625	fp Picture carrier, fs Sound carrier; 0.75, 0, 5.5 MHz	FM	NEGATIVE	PAL	4.433619	Carrier suppression quadrature 2-phase modulation	Even line: −135°; Odd line: +135°; Field 1st: +135°, 2nd: +135°, 3rd: −135°, 4th: −135°
G (UHF)									
H (UHF)			1.25, 0, 5.5 MHz						
I			1.25, 0, 6.0 MHz						
D (VHF)									
K (UHF)			0.75, 0, 6.5 MHz						
L			1.25, 0, 6.5 MHz	AM	POSITIVE	SECAM	f_{OR}: 4.40625 f_{OB}: 4.25	FM	No burst
M	525/60	15,750 (B/W) 15.734264 (Colour)	0.75, 0, 4.5 MHz	FM	NEGATIVE	NTSC	3.579545	Same as PAL	−180°

Fig. 7-1 World TV Systems and Colour Systems

1. GENERAL

The VS-2EGN is capable of recording and playback of television signals shown below, and is a high grade multi-function model.

ⓐ Recording/playback of PAL BG
ⓑ Recording/playback of SECAM BG
ⓒ Recording/playback of NTSC 4.43 (line video recording only)
ⓓ Recording/playback of NTSC 3.58 (line video recording only)
ⓔ Playback of SECAM L

At present, there are various television systems in the world. Television signals which can be recorded or reproduced by the VS-2EGN and television systems in the world are described below.

1-1 WORLD TELEVISION AND COLOUR SYSTEMS

Refer to Fig. 7-1.
For example, in the case of SECAM B/G which is called Middle East SECAM, monochromatic signals follow the CCIR system, while colour signals are of the SECAM system.

1-2 RADIO FREQUENCY HEAD OF VS-2

VS-2 DEMODULATOR								
Model	Receivable broad cast system	VIDEO IF (MHz) / SOUND IF (MHz)	Receivable Broadcast channels			Demodulated signal		Country
			VHF-L	VHF-H	UHF	Video	Sound	
EG EGN	B/G PAL B/G SECAM	38.9 / 33.4	2~4	5~12	21~69	B/G PAL SECAM	AM	Germany, Singapore Middle East Country
EK	I PAL (UHF only)	39.5 / 33.5	–	–	21~69	I PAL		U.K. Hong Kong
EO	B/G PAL B/G SECAM (CATV)	38.9 / 33.4	2~4 S1~S3	M1~M10 5~12 U1~U10	21~69	B/G PAL B/G SECAM		Belgium Switzerland
EA	B/G PAL B/G SECAM	36.875 / 31.375	0~5	5A~11	21~69	B/G PAL B/G SECAM		Australia Newzealand
ES	I PAL (UHF & VHF-H)	38.9 / 32.9	–	4~13	21~69	I PAL		South-Africa
S	L SECAM	32.7 / 39.2	A~C	1~6	21~69	L SECAM Wide video bandwidth compared to B/G		France

Fig. 7-2 VS-2 Demodulator

VS-2 R.F Convertor				
Model	Television system	Frequency Spectrum	Output channel	Video modulation polarity
EA	B	S, VHF, 0, +5.5	CH3 CH4 switching	NEGATIVE
EG EO EGN	G	S, UHF, 0, +5.5	CH30 ~39 variable	
EK ES	I	S, UHF, 0, +5.996	CH30 ~39 variable	POSITIVE
S	L	S, UHF, 0, +6.5	CH30 ~39 variable	

Fig. 7-4 RF Converter Types for VS-2

As might be known from Fig. 7-1, the frequency spectrum, etc. of the television channel vary from TV system to TV system. Accordingly, the tuner unit of the video cassette recorder (VCR) which receives TV broadcasts is classified as shown in Fig. 7-2 according to the model code letters.

VS-2EGN has a built-in tuner for Model EG.

Fig. 7-3 shows the types of AKAI VTR available and the transmission channels used in major countries.

The types of RF converter are classified as shown in Fig. 7-4, which shows that the RF converter for the G system is used for the VS-2EGN. This type of RF converter is also used for models EG and EO.

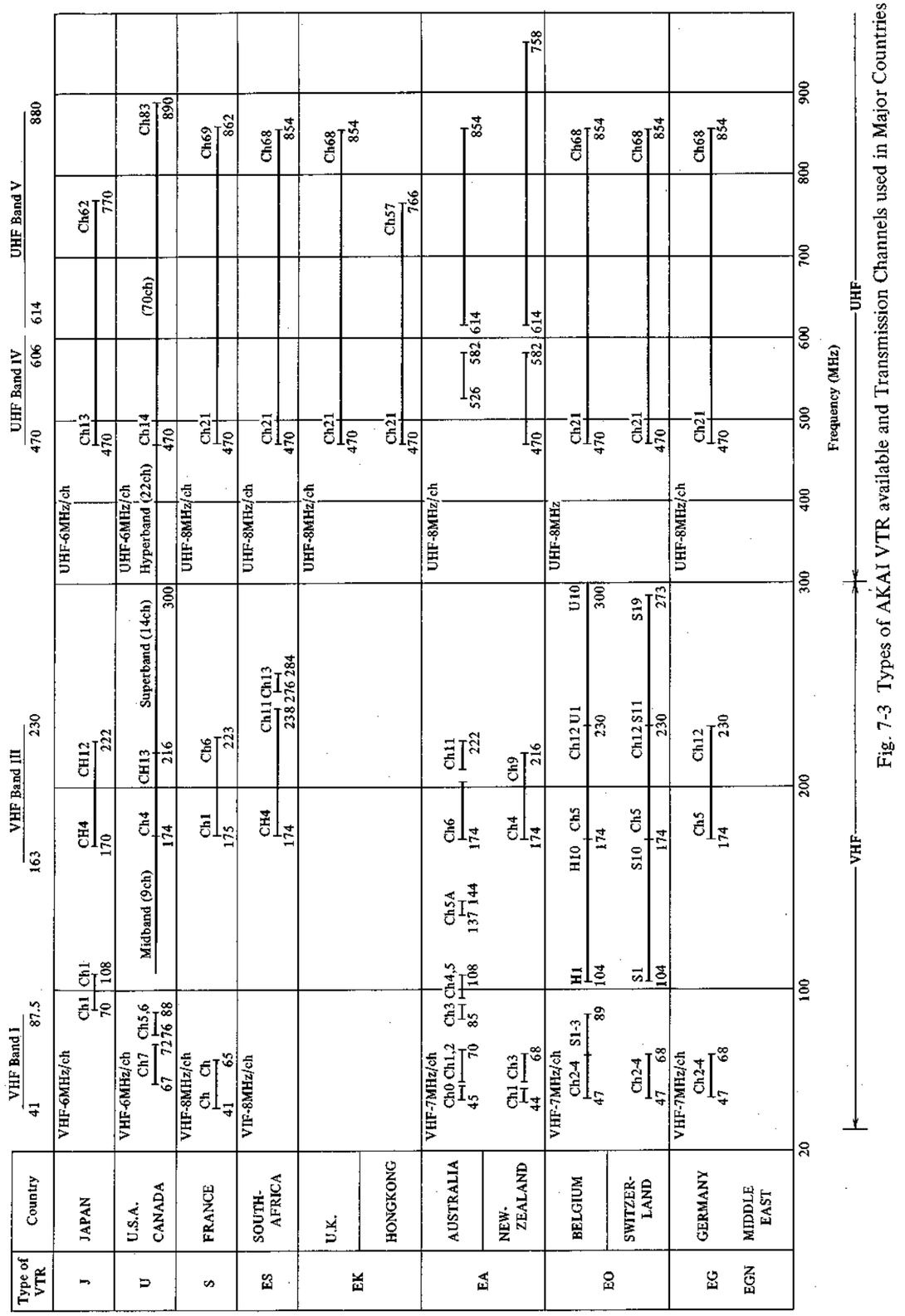
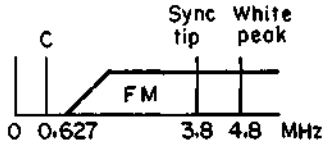
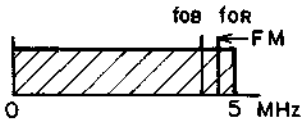
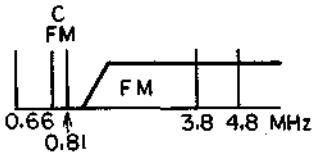
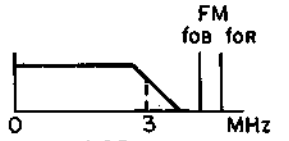


Fig. 7-3 Types of AKAI VTR available and Transmission Channels used in Major Countries

1-3 RECORDING/PLAYBACK FUNCTION OF VS-2EGN

Recordable Video Signal (With built-in tuner)		Signal Recorded on tape		Playback Video Signal
		Frequency spectrum on tape	Colour signal processing	
PAL B/G			CH-1 no change CH-2 extra 90° lag every 1H	
SECAM B/G			CH-1 CH-2 Both no change	

(Through Line input)

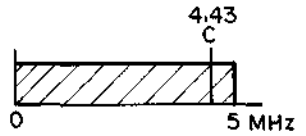
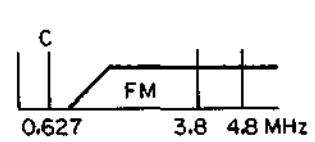
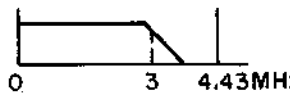
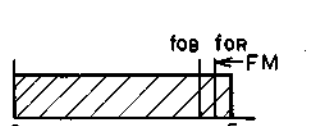
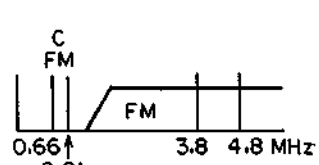
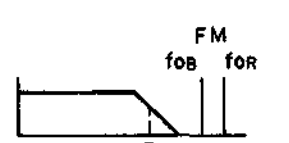
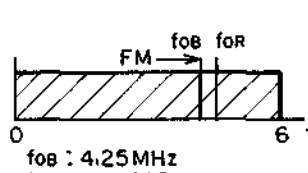
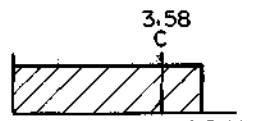
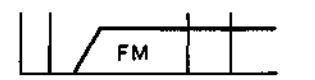
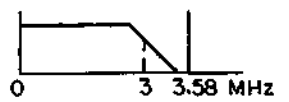
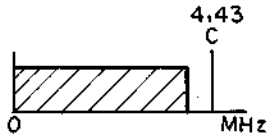
PAL B/G H/I			CH-1 no change CH-2 extra 90° lag every 1H	
SECAM B/G			CH-1 CH-2 Both no change	
SECAM L				
NTSC			CH-1 extra 90° advance every 1 H 3.58CH-2 extra 90° lag every 1H	
NTSC 4.43				

Fig. 7-5 Recording/Playback Function of VS-2 EGN

Refer to Fig. 7-5 Recording/Playback Function of VS-2

Recordable TV signals from built-in tuner
PAL B/G
SECAM B/G
Recordable TV signals from line input
PAL B/G/H/I
SECAM B/G (Middle East SECAM)
SECAM L (French SECAM)
NTSC 3.58 (standard NTSC)
NTSC 4.43 (modified NTSC)

The SECAM L signal from the line input is recorded as a SECAM B/G signal on the tape (system employing count down of the SECAM colour signal similar to the PAL system operation).
NTSC 4.43 signal is recorded on the tape as an NTSC 3.58 signal.

Playback signals vary from each other, and a 3-system or a 5-system television is required. The television should be set so that the system display at the front of VS-2 EGN becomes the same mode as the displayed signal.
For details, refer to II. Operating Procedure.

1-4 SELECTION OF SIGNAL SYSTEM

As shown in Fig. 7-6, the operation panel of Model VS-2EGN has an LED display unit (AUTO: green, the rest: red), the there is a SYSTEM selector switch below it. The SYSTEM switch permits manual system selection.
Normally, reset is effected at Function-ON, and the system selects the AUTO mode, which is detected by a microcomputer and displayed. Accordingly, the SYSTEM switch is not used.

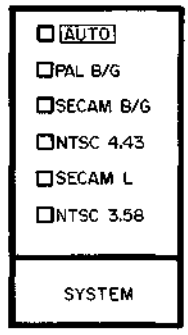


Fig. 7-6 System Display Unit

1-4-1 SYSTEM DISPLAY IN AUTO MODE
(Recording Electronic-to-Electronic (EE) Mode)

INPUT VIDEO / LED	PAL	SECAM B/G	NTSC 4.43	SECAM L	NTSC 3.58
AUTO	●	●	●	●	●
PAL B/G	●				
SECAM B/G		●		●	
NTSC 4.43			●		
SECAM L	–	–	–	– NOTE 1	–
NTSC 3.58					●

NOTES: 1. Since the SECAM L signal is recorded on the tape as a SECAM B/G signal, SECAM B/G indicator lights in the LED display unit.
2. When there is no input video signal, the AUTO indicator alone lights.

(Playback Mode)

TAPE / LED	PAL	SECAM B/G	NTSC	SECAM L
AUTO	●	●	●	●
PAL B/G	●			
SECAM B/G		●		
NTSC 4.43	–	–	– NOTE 1	–
SECAM L				●
NTSC 3.58			●	

NOTE: 1. When it is desired that signals are reproduced in NTSC 4.43, use the manual operation procedure.

1-4-2 SYSTEM DISPLAY IN MANUAL MODE

For selecting the system manually, press the SYSTEM switch the appropriate number of times until the desired system is selected.
(Recording EE Mode)

No. of times / LED	Function ON	1st time	2nd time	3rd time	4th time	5th time	6th time
AUTO	●						● NOTE 3
PAL B/G		●					
SECAM B/G			●			NOTE 2	
NTSC 4.43				●			
SECAM L	NOTE 1	–	–	–	–	–	
NTSC 3.58					●		

NOTES: 1. SECAM L cannot be selected in the Recording EE mode.
2. When all LEDs are OFF, the mode is 625 lines/50 Hz monochromatic mode.
3. At the 6th time, the LED display returns to AUTO. However, when there is no video input to the VCR, 'AUTO' does not light. The LED display lights a colour video signal is connected.

(Playback Mode)

No. of times / LED	Function ON	1st time	2nd time	3rd time	4th time	5th time	6th time	7th time
AUTO	●							● NOTE 2
PAL B/G		●						
SECAM B/G			●				NOTE 1	
NTSC 4.43				●				
SECAM L					●			
NTSC 3.58						●		

NOTES: 1. When all LEDs are OFF, the mode is 625 lines/50 Hz monochromatic mode.
2. At the 7th time, the LED display returns to AUTO. Since a video signal is always present at the video judge (VJ) output during playback, the LED display does not go off.

1-5 VIDEO PRESENT/ABSENT JUDGEMENT

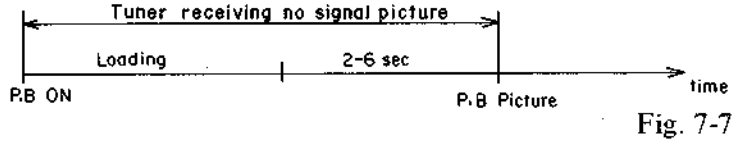


Fig. 7-7

In VS-2 EG/EO/EX/ES/EA/S, it is so controlled that even when no wanted video signal is present, a video signal is made to be present in the CUE/REVIEW mode of playback only. Accordingly, at the time of CUE/REVIEW playback of unrecorded tape, etc., a noise picture appears. On the other hand, no noise picture appears during normal playback or in the recording E-E mode, since switching to the internal oscillator takes place when no video signal is present.
In VS-2EGN, no video judgement is performed in any of the playback modes including CUE/REVIEW. That is, control is exercised to ensure an always video signal present condition. For this reason, the following special picture changes occur.

In the cases of tuner reception (when the converter is not connected to the VIDEO LINE IN) and no signal.
1) With no signal, the E-E picture is a gray picture from the internal oscillator.
2) When the PB button is depressed, a tuner reception signal appears regardless of whether or not a picture is received. *1
3) The condition of 2) continues until the end of loading and in addition for about 2.6 seconds, and then the TV display is changed to the playback signal picture.

*1: In the models other than VS-2EGN, 1) continues to the part of 2), but in Model EGN, the PB 12V control line is used to control all playback modes. Since the PB 12V is output concurrently with the depression of the PB button, the condition 2) appears.

2. VS2-EGN VIDEO CIRCUIT OPERATION

VS-2EGN can perform the recording and playback of the following signals.
1) Recording and playback of PAL B/G (from Built-in Tuner to RF OUT)
2) Recording and playback of SECAM B/G (from Built-in Tuner to RF OUT)
3) Recording and playback of NTSC 3.58M (from Line in to Line Out)
4) Recording and playback of NTSC 4.43M (from Line in to Line Out)
5) Playback of SECAM L (to LINE OUT)
Operation of the above five systems will now be described. Since the systems differ in the filter characteristics, PAL is mainly described, for the luminance system section, and for other sections only points differing from PAL are described.
The chrominance (CHROMA) circuit is described by dividing it into the following four sections according to the nature of its signals.
1) PAL B/G and NTSC 4.43 recording and playback
2) SECAM B/G recording and playback
3) NTSC 3.58
4) SECAM L playback

2-1 LUMINANCE (Y) RECORDING AND PLAYBACK

2-1-1 E-E SYSTEM (PLEASE REFER TO THE VIDEO SCHEMATIC)

A PAL B/G or SECAM B/G signal from the tuner (demodulator) or alternatively a video signal from LINE IN is terminated at R1 (75Ω), fed to VR-11 (E-E level) for E-E level adjustment and fed to VIDEO AMP IC6 (HA11703) pin ⑰, and output from pin ⑯. Quasi V pulse (VP) is added by TR32 only while in the trick-play, i.e., CUE, REVIEW, and PB/PAUSE. Then, the signal enters pin ⑱ and is amplified. Next, the signal is output from pin ⑳, and enters IC5 (HD14053BP) pin ③. Since the video signal is present and 12 VJ line of the video judge (VJ) circuit in the servo circuit is 'H', the signal is output to pin ④, and then the character signal is added at TR8 by the output Video on Word (VOW) from the mi-com of the operation PC board. Now, the video signal is output to LINE VIDEO OUT via TR2, and it is fed to the RF converter from the VID terminal through RL2 (LCB-56) and TR6. In summary, this signal flow represents the E-E system.

2-1-2 RECORDING SYSTEM

In accordance with the description of the E-E system in Section 2-1-1, the video signal is applied to IC5 (HD 14053BP) pin ①, and the character-added video is applied to pin ②. The signal from pin ① is output through IC5 output pin ⑮ at the normal time, i.e., when pin ⑩ is 'H', and this output signal is fed to the video head.
However, during the period when INS LINE is kept 'H' by the mi-com of the operation PC board, pin ⑩ is kept at 'L' via the converter TR29, and the input from pin ② is output to pin ⑮. That is, the character-added video signal is supplied to the video head. IC5 pin ⑮ output is branched to the LPF consisting of FL3, and the LPF consisting of FL5. The −3 dB point of FL3 is 3.0 MHz, and is 3.3 MHz for FL5.
In the state where a PAL (B/G) or SECAM (B/G) signal is being recorded, IC5 pin ⑪ is at 'H' level. Since pin ⑪ is connected to NT-L, only the luminance component of the video signal which has passed through the LPF is output to pin ⑭.
The output of pin ⑭ is supplied to IC1 (AN6310) pin ①, and is output to pin ㉒. During that time, the signal is subjected to AGC (automatic gain control), and the deviation (1.0 MHz) of the frequency modulation circuit in the next-stage is determined by VR8 located between pins ㉒ and ⑲.
The output of the VIDEO AMP circuit (pin ⑱ – pin ⑲) passes through the non-linear emphasis circuit. The amount of emphasis is determined by TR12 and TR16 when there is an NTSC signal. Then, the signal enters pin ⑯, and is subjected to frequency modulation. Since TR13 connected to pins ⑬ / ⑭ becomes ON in the modes other than NTSC, the FM carrier frequency is changed.
Dark Clip VR7 is connected to pin ⑫, while White Clip VR5 is connected to pin ⑩. The frequencies of White Clip, Dark Clip, and Deviation are as follows:

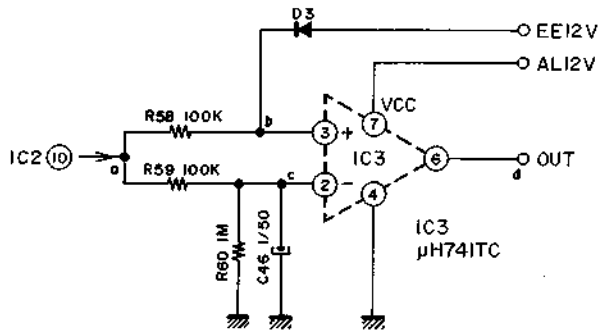
Mode	PAL B/G, SECAM B/G	4.43, 3.58 NTSC
WHITE CLIP	5.4 MHz	5.0 MHz
PEAK WHITE	4.8 MHz	4.4 MHz
SYNC TIP	3.8 MHz	3.4 MHz
DARK CLIP	3.4 MHz	3.0 MHz

The frequency-modulated Y signal (FMY) from IC1 pin ⑨ is directed to pass through the HPF consisting of FL1 (1.4 MHz at −3 dB point) so as to prevent interference with the low frequency converted CHROMA (mentioned later). Thereafter, the signal is controlled at VR4 (Y REC LEVEL), mixed with the low frequency converted CHROMA, passed through the REC Signal Inter-Board Connection to the Audio/Pre P.C Board, fed to the PRE AMP circuit, and supplied to the video head through the emitter follower (TR10) and the constant current buffer (TR8/9).
Since TR5 and TR6 are grounded by REC 12V during recording, a closed circuit of REC current is formed via R43, and VIDEO data is recorded on the tape.

2-1-3 PB SYSTEM

Since TR4 of the pre-amp circuit goes ON during playback, the PB VIDEO signals (FMY + Low Frequency Converted Chroma) from the video heads 1 and 2 are supplied to IC2 (AN6320N) pins ③ and ⑤. After going through pins ③ /⑤, PB VIDEO signals of CH-1 and CH-2 are selected by the Amplifier Switching Pulse which connects them to pins ⑬ and ⑨, after the overlap portions have been cut off. The outputs from pins ⑬ and ⑨ are mixed on the way to pin ⑪, and the mixture flows to pin ⑩ after going through the MIX AMP, and then to the video PC board as a PB PRE OUT through the emitter follower (TR7). On the video board, the PB signal from the pre-amp is directed through the HPF (1.4 MHz at −3 dB point) consisting of C1, 5, 6, R10, 11, and L1. Only FMY is extracted there, fed to the 5.8 MHz peaking circuit composed of L35, C203, and TR3, subjected to the phase correction at C15, 16 and L6, fed to pin ⑭ of IC2 (HA11718) subjected to AGC; and then output from pin ⑫ of IC2. When there is a drop-out, the signal 1H earlier is output from pin ⑪ and supplied to pin ⑫ by DL1 (64 μs delay).

1) DROP OUT Pulse Generator (Refer to Fig. 7-8)



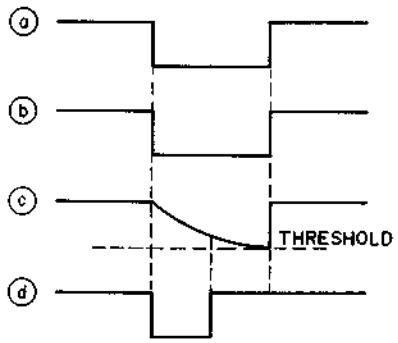


Fig. 7-8 DROP OUT Pulse Generator

At the time of a drop-out occurs, IC2 pin ⑩ becomes 'L', causing IC3 (μH741TC) pin ③ to become 'L'. Since C46 (1μF/50V) has only just started to discharge pin ② does not become 'L'. That is, the output is 'L'. D3 is for operation stop in the E-E mode.

The output of IC2 pin ⑫ is fed to the double limiter circuit in which the signal is divided into two.
First it is directed to the HPF composed of C48, R62, and C47, amplified at TR7, phase corrected at C39 and R37, amplified at TR15, and fed to IC4 (TA7060AP) pin ①. The signal is amplitude-limited at the 1st limiter between pin ① and pin ④, and then applied to the emitter of TR18.
Secondly, the output of IC2 pin ⑫ is directed to the LPF (4 MHz at −3 dB point) composed of R80 and C57, and applied to the base of TR18. At the collector, this signal appears, mixed with the first signal which is applied to the emitter.
After being phase-corrected at TR9, L10, and R47, the signal is fed to IC6 (HA11703) pin ④ via the emitter follower of TR39. After being amplitude-limited and FM-demodulated on the way from pin ④ to pin ⑨, the signal is directed through the respective filters of FL8 (PAL), FL6, 7 (NTSC), and FL9, 10 (SECAM), and fed to IC7 (HD14066BP) pins ①, ⑨, ④. Now, if both control signal lines 3N-H and 3L-H from the servo circuit are 'L' (PAL mode), the signal passes from IC7 pin ① to pin ②, is directed to the non-linear de-emphasis circuit composed of TR34, L20, C91, D8, and D9, phase corrected at L11 and C102, then fed to IC6 pins ⑪ and ⑫, and output from pin ⑯.
PB CHROMA is supplied to pin ⑮ and mixed there. The output of pin ⑯ passes through VP ADD of TR32.

During CUE/REVIEW and PB/PAUSE, the V pulse generated by the switching pulse is injected into the servo circuit to prevent shaking in the Vertical direction on the TV screen due to omission of V SYNC component.
Subsequent signal flow is omitted since it is the same as the E-E system.

2-2 CHROMINANCE (CHROMA) RECORDING AND PLAYBACK SYSTEM

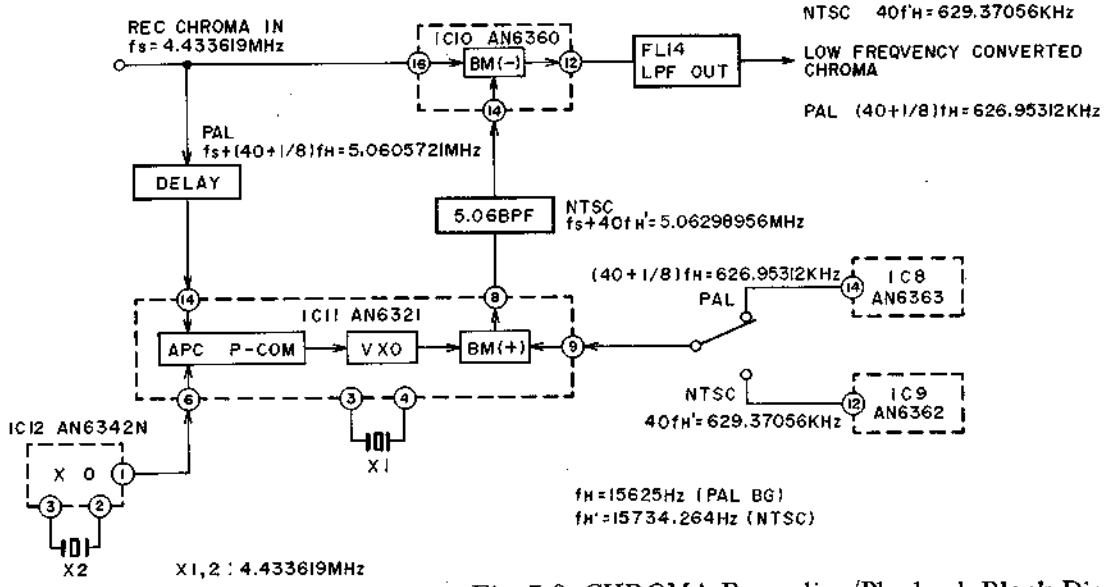


Fig. 7-9 CHROMA Recording/Playback Block Diagram

2-2-1 RECORDING OF PAL B/G AND NTSC 4.43

The input video signal already described in the section devoted to the luminance E-E system separates into a Y signal path through FL3–5, and a path for the CHROMA signal having the frequency band 4.43 MHz± 500 kHz. It alone passes through FL16 (LCB-57) and BPF (3.68 MHz–5.18 MHz at –3 dB point). (The Bandwidth and center frequency of PAL B/G CHROMA signals are the same as those of NTSC 4.43 CHROMA signals). The CHROMA signal is fed to IC10 (AN6360) pin ①. Since the internal switch is in the recording mode, the signal is output from pin ⑰, and reinput from pin ⑯. During the PAL mode, 5.0605721 MHz enters pin ⑭. The output of pin ⑫ becomes a 626.9 kHz low frequency CHROMA signal as it passes through FL14. During the NTSC 4.43 mode, 5.0629895 MHz enters pin ⑭, and the output from pin ⑫ passes through FL14, and is output as a 629.3 kHz low frequency CHROMA signal.
At this time, the APC system is actuated to lock the phase burst of low frequency converted CHROMA to that of input CHROMA signal.

During the NTSC 4.43 mode, 4N-H becomes 'H', actuating TR47 through D20. 40 fH from IC9 (AN6362) pin ⑫ is selected, which causes IC10 (AN6360) pin ⑤ to become 'L' via the inverter (TR52). Only the burst component is amplified by 6 dB after the balanced modulator.
(In the case of the PAL mode, the burst is not amplified due to IC10 pin ⑤ being 'H'.)

1) NTSC phase shift
IC9 pin ⑪ is driven by the switching pulse from the servo circuit, and +90° phase shift is effected at every horizontal period when this is 'H'. That is, the switching pulse gives +90° phase shift during CH-1 period if 'H' time is CH-1. Since pin ⑪ is 'L' in every CH-2 period, –90° phase shift is effected.
2) PAL phase shift
IC8 (AN6363) pin ⑬ is a control input pin to cause that CH-1 ('H' period) does not have any phase shift irrespective of the horizontal period while CH-2 ('L' period) makes –90° phase shift at every horizontal period. It carries out the above operation by using the switching pulse as the input.
3) Mixing of FMY signal
Low frequency converted CHROMA signal from IC10 pin ⑫ passes through FL14 (1.5 MHz at –3 dB point), enters pin ⑧, is amplified, switched to the recording side by the REC/PB switch, is output from pin ⑦, passed through the 4.47 MHz trap composed of L4 and C10, level-adjusted at VR2, mixed with the FMY signal, and supplied to the pre-amp through the emitter follower.
(Subsequent signal flow is omitted since it is described in the section devoted to the Y recording system.)

2-2-2 PLAYBACK OF PAL B/G AND NTSC 4.43 (CHROMA) SIGNALS

The PB video signal (low frequency converted CHROMA + FMY) from the Pre-amp Board passes through PRE OUT Inter-Board Connection to the Video Board and then to the LPF of FL12 (1.5 MHz at −3 dB), and is fed to IC10 pin (18) having only the CHROMA component remaining. This signal passes through the ACC (Auto Colour Control) in IC10 at the time of PB mode, is re-input from pin (17) to pin (16) , and converted to the original CHROMA signal at the balanced modulator by means of the 5.06 MHz carrier supplied to pin (14). The output from pin (12) , passes through the BPF FL13 (±500 kHz of 4.43 MHz at −3 dB), enters pin (10) as 4.43 MHz CHROMA signal, and is output from pin (9) via the amplifier.

1) Operation during the PAL mode

Regarding the CHROMA signal from IC10 pin (9), since the DIRECT PASS component and the 2H DELAY component are mixed in DL2 (PAL 2H delay line), the crosstalk component is cancelled. The cancelled crosstalk component passes through TR55 (due to NT-H line being 'L'), enters IC10 pin (6), goes out from pin (7) through internal switch, level-adjusted at VR13, and enters IC6 pin (15).

2) Operation during the NTSC 4.43 mode

Since the 4N-H line is 'H', D31 becomes ON, TR54 becomes ON, the emitter of TR55 is reverse-biased, the stroke component is cancelled at DL3 (NTSC 1H delay line), and the output from IC10 pin (9) enters IC10 pin (6). During recording, the BURST signal amplified by 6 dB is now attenuated by 6 dB during playback. The CHROMA signal fed to IC6 (HA11703) pin (15) is mixed with PBY, and the combined output passes to VIDEO OUT along the same route as the aforementioned E-E system.

3) PB APC system

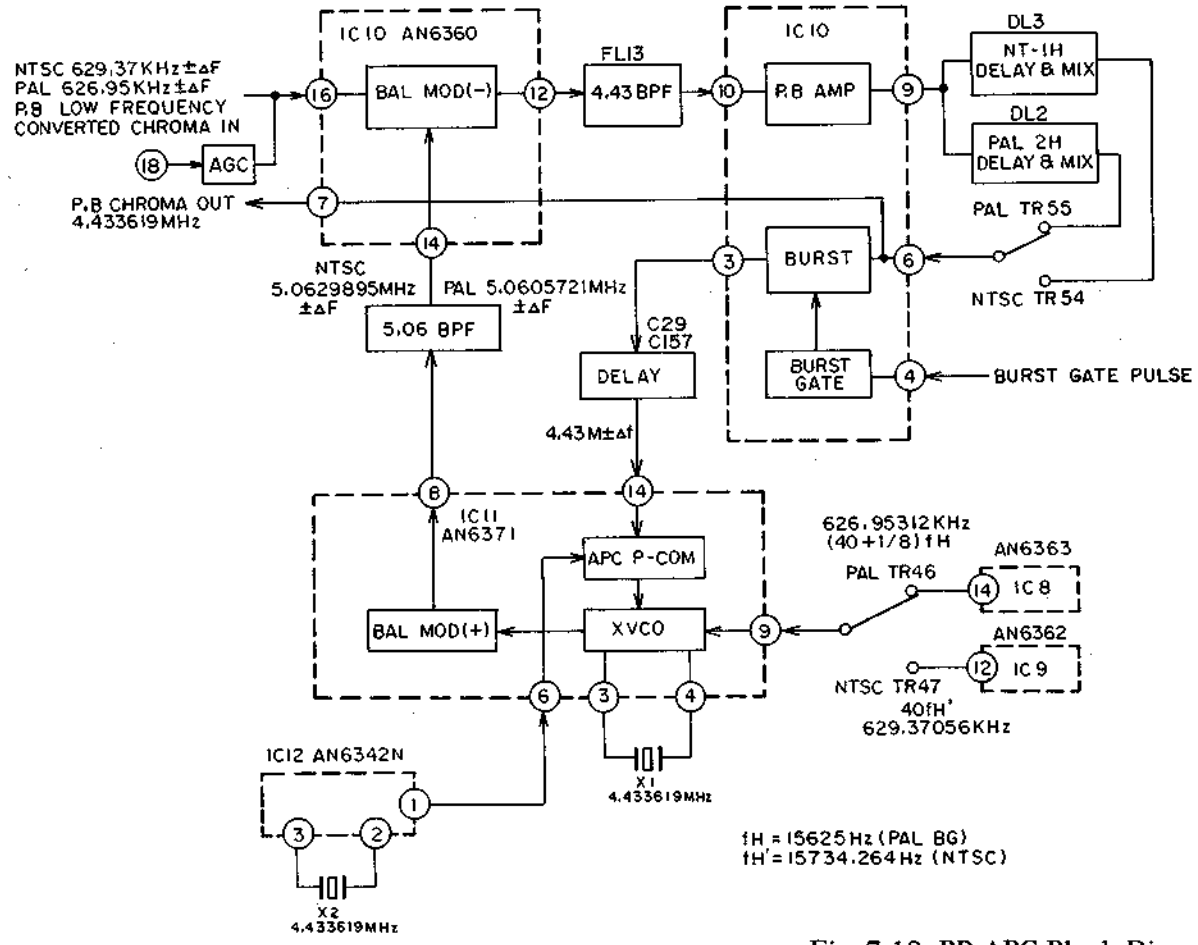


Fig. 7-10 PB APC Block Diagram

The 5.06 MHz signal to be supplied to IC10 pin (14). The PB low frequency CHROMA signal supplied to pin (18) is amplitude/frequency modulated due to uneven rotation of the tape driving system and uneven rotation of the mechanism system. When this modulated CHROMA signal is directly transformed to a normal CHROMA signal which is then fed to the TV set, hue changes and a picture with changing degrees of saturation will result. Accordingly, the amplitude modulated component is removed by passing the CHROMA signal through the ACC circuit, and the frequency modulated component is removed at the APC circuit.

The PB low frequency converted CHROMA signal is fed to IC10 pin (16). The lower and upper side bands of 4.43 MHz and 5.686 MHz (PAL) or 5.689 MHz (NTSC) are output to pin (12) from the balanced modulator, and only the lower side band is selected as it passes through the 4.43 BPF. This PB frequency-converted CHROMA signal has the jitter component IΔF. Since the output of IC11 (AN6371) pin (8) also has a jitter component IΔF, this IΔF is similarly fed to IC10 pin (14). Since the response of the APC system is very fast, if the time delay between the IΔF fed to pin (16) and the IΔF fed to pin (14) is zero, they are mutually cancelled completely, and the jitter component can be removed.

4) PAL PB AFC system

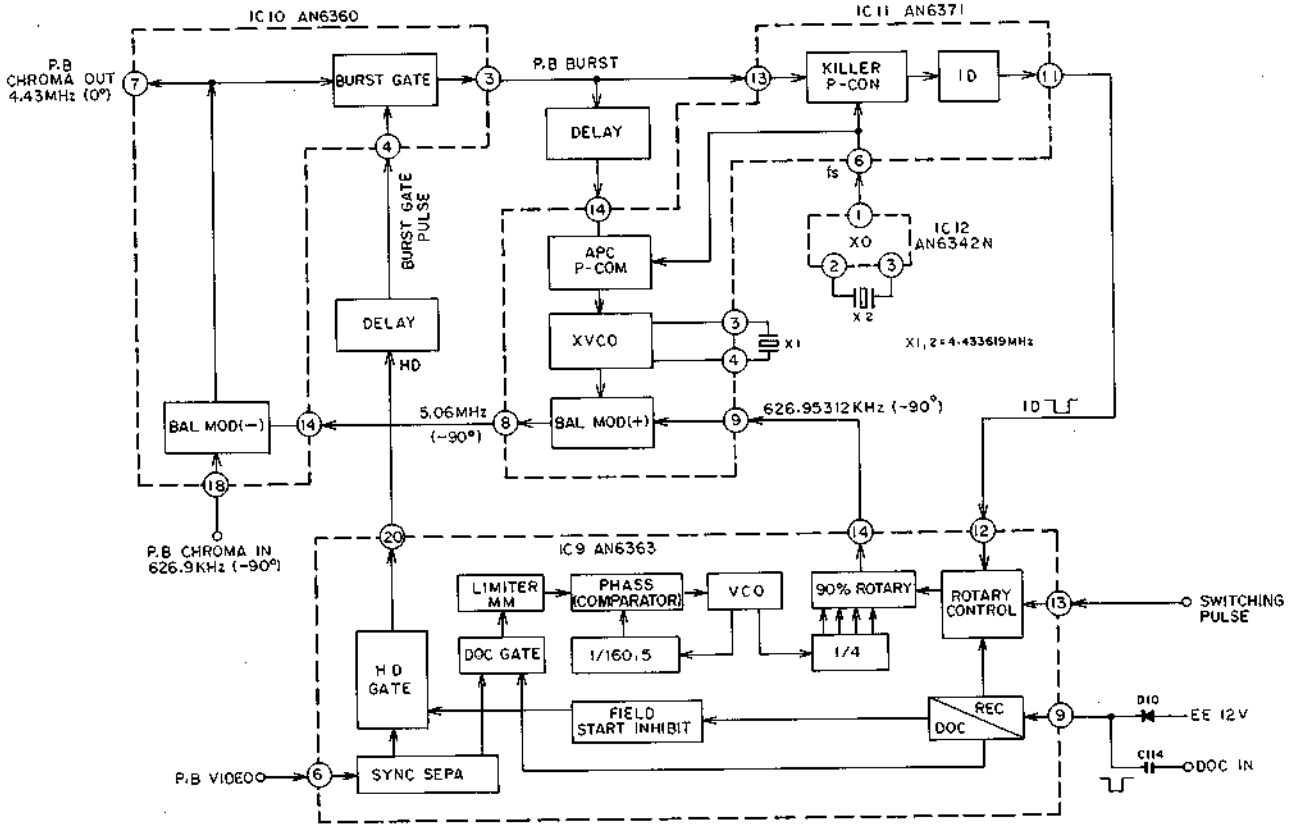


Fig. 7-11 PAL PB AFC Block Diagram

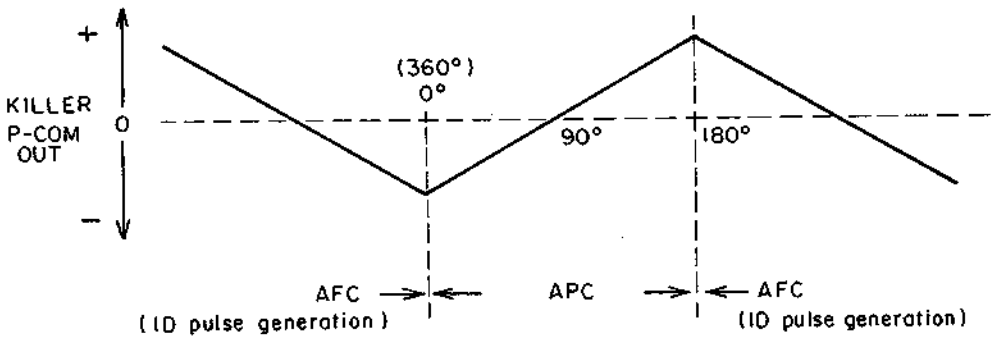


Fig. 7-12 ID Pulse System

The PB low frequency converted CHROMA signal fed to IC10 pin (18) is converted to 4.43 MHz CHROMA by the balanced modulator, and output from pin (7) as a PB CHROMA signal. A PB BURST signal output from IC10 pin (3), is obtained from sampling by the time delayed burst gate pulse connected to pin (4). This PB BURST signal is fed to IC11 pin (13), and phase detected by the 4.43 MHz XO connected to pin (6). If the phase difference is between 180° and 360°, an ID pulse is generated from pin (11). As the ID pulse enters IC9 (AN6362) pin (12), the rotary control circuit starts from the phase to which its 90° rotary circuit made a −90° shift. Accordingly, the phase of the output from pin (14) changes by −90°, reducing the phase difference between the PB BURST and the XO so it comes within the range allowing the APC system to lock.

Upon swing pulse input from IC9 pin (11), –90° phase-shift is effected every 1H at CH-2, and CH-1 does not make phase rotation. This method is totally identical with that of recording. However, since the difference component of the two inputs is extracted at the balanced modulator of IC10, the 90° shift is cancelled.

IC10 pin (18) signal phase . . –90° ——→ BAL MOD → 0°
IC10 pin (14) signal phase . . –90° ——→ BAL MOD → 0°

5) PAL DOC

When the PB output becomes very small due a cause such as tape damage, during playback, or when there is no output, a PB signal of 1H length only is used as compensation. This is obtained by using a 1H delay line. In the CHROMA system, as a drop-out occurs, IC9 pin (9) becomes 'L', HD output from pin (20) stops, PB Burst is no longer output from IC10 pin (3), and Colour Killer output CK-1 from IC11 pin (10) becomes 'L'. The output of IC8 (AN6363) pin (11) becomes 'H', TR57 is actuated via D14, the delay line of DL2 is put into the PASS condition. Though the output frequency of the XVCO becomes unstable, since the phase rotation stops, the CHROMA phase remains locked.

Since D10 makes pin (9) 'H' during recording, the DOC circuit does not operate.

6) NTSC 4.43 PB AFC

This is basically the same as PAL, and AFC operation is performed at IC9 (AN6362).

It differs from PAL in that 40 fH=629.37056 kHz is selected by the switching circuit composed of TR46 and TR47 and is fed to IC11 pin (9). The APC system is the same as the PAL APC system.

When phase differences occur between the PB Burst and the XO which cannot be followed by the APC system, an ID pulse is generated from IC11 pin (11). This ID pulse enters IC9 pin (10), causes the control circuit to effect –90° shift of the 90° rotation selector circuit, and changes the phase of the 40 fH being output from pin (12). This shifts the phase into the range that can be followed sufficiently well by the APC system.

2-2-3 RECORDING AND PLAYBACK OF SECAM B/G

1) SECAM B/G recording

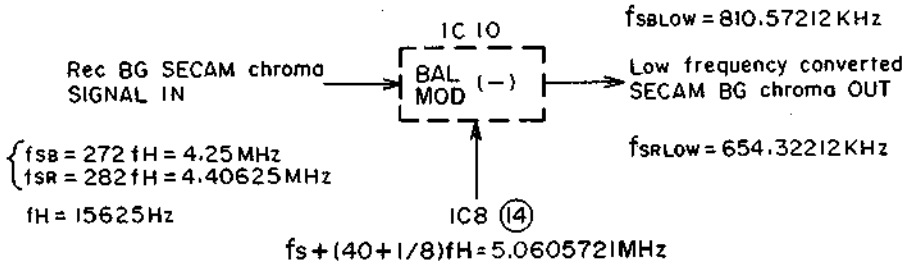


Fig. 7-13 SECAM B/G Recording—Frequency Conversion

SECAM B/G (Middle East SECAM): CHROMA recording

(a) Low frequency converted CHROMA signal is generated by the down system.

(b) Neither CH1 nor CH2 are subjected to phase rotation.

A SECAM B/G signal which has been fed to IC10 pin (1) through FL16 (4.43 MHz BPF) emerges from pin (12) by passing through the balanced modulator circuit with the 6 dB UP/DOWN unaffected.

Afterwards, the signal is fed to pin (8) through FL14 (1.5 MHz BPF) without being affected by D30 since D30 is cutoff because the PAL/SECAM/4N-H line is 'H'. It emerges from pin (7).

This low frequency converted SECAM CHROMA signal passes through the trap circuit (L4 and C10) without being affected by it, is level-adjusted at VR2, mixed with FMY, sent to the pre-amp, and to the video head record circuit.

Since the SD-H line is 'H' as this is the due to SECAM mode D16 conducts. As a result, the phase rotation control circuit of IC8 (AN6363) stops the phase rotation of the CHROMA signal.

At this time, the ACC circuit located between pin (1) and pin (17) controls the burst level by sampling the line burst signal by means of the BURST GATE pulse generated at HD.

The BURST signal from IC10 pin (3) becomes high via D22, since the emitter potential of TR58 is SB-H ('H' during SECAM B/G) mode. As TR58 becomes cutoff, the BURST signal is no longer fed to IC11 pin (14), and the APC loop is not formed for either recording or playback.

2) SECAM B/G playback

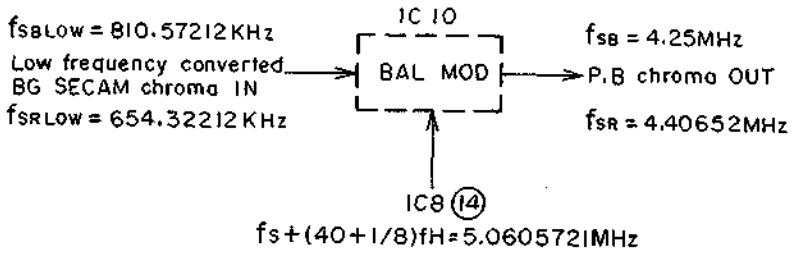


Fig. 7-14 SECAM B/G Playback–Frequency Conversion

The low frequency converted SECAM B/G CHROMA signal flows along the same route used for PAL B/G, and is output to VIDEO OUT. During recording, since IC8 pin (13) is 'H', no phase rotation is performed.

Since D17 conducts, TR57 conducts, and the signal passes through DL2 (PAL 2H delay). As a result, the signal is output directly to VIDEO OUT without being delayed.

2-2-4 RECORDING AND PLAYBACK OF NTSC 3.58 MHz (EGN P.C BOARD)

1) Recording

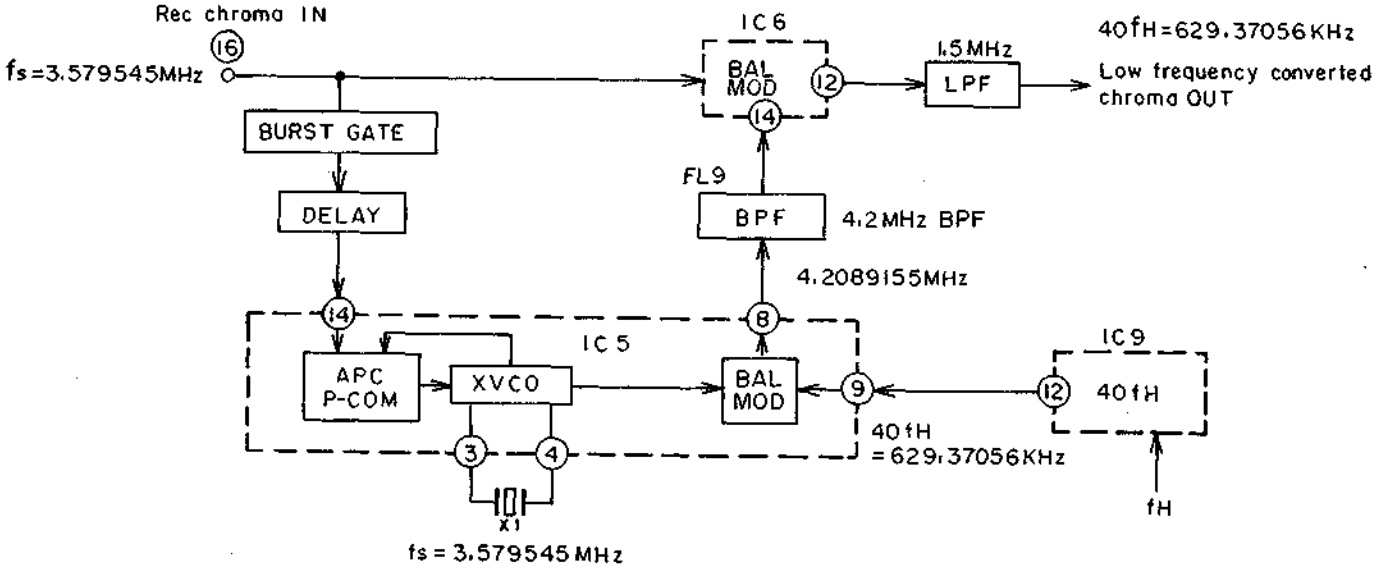


Fig. 7-15 Block Diagram of NTSC 3.58 Recording

The REC CHROMA signal is fed to IC6 (AN6360) pin (1) through the 3.58 MHz±500 kHz BPF FL8, and fed to pin (16) again through the ACC circuit before it is output to pin (17). Before being connected to pin (12), the signal passes through a balanced modulator to which fs + 40 fH (629,37056 kHz) is connected through pin (14) and recording signal fs, and only the BURST signal is amplified by 6 dB at the output.

The signal from pin (12) is directed through the low pass filter LPF (–3 dB at 1.5 MHz), fed to pin (8) without being affected by D6 (since D6 is cutoff because 3.58 NT-H line is 'H'), output from pin (7), passed through the 3.7 MHz trap composed of L5 and C11, level adjusted by VR3, and then fed to the pre-amplifier.

2) Playback

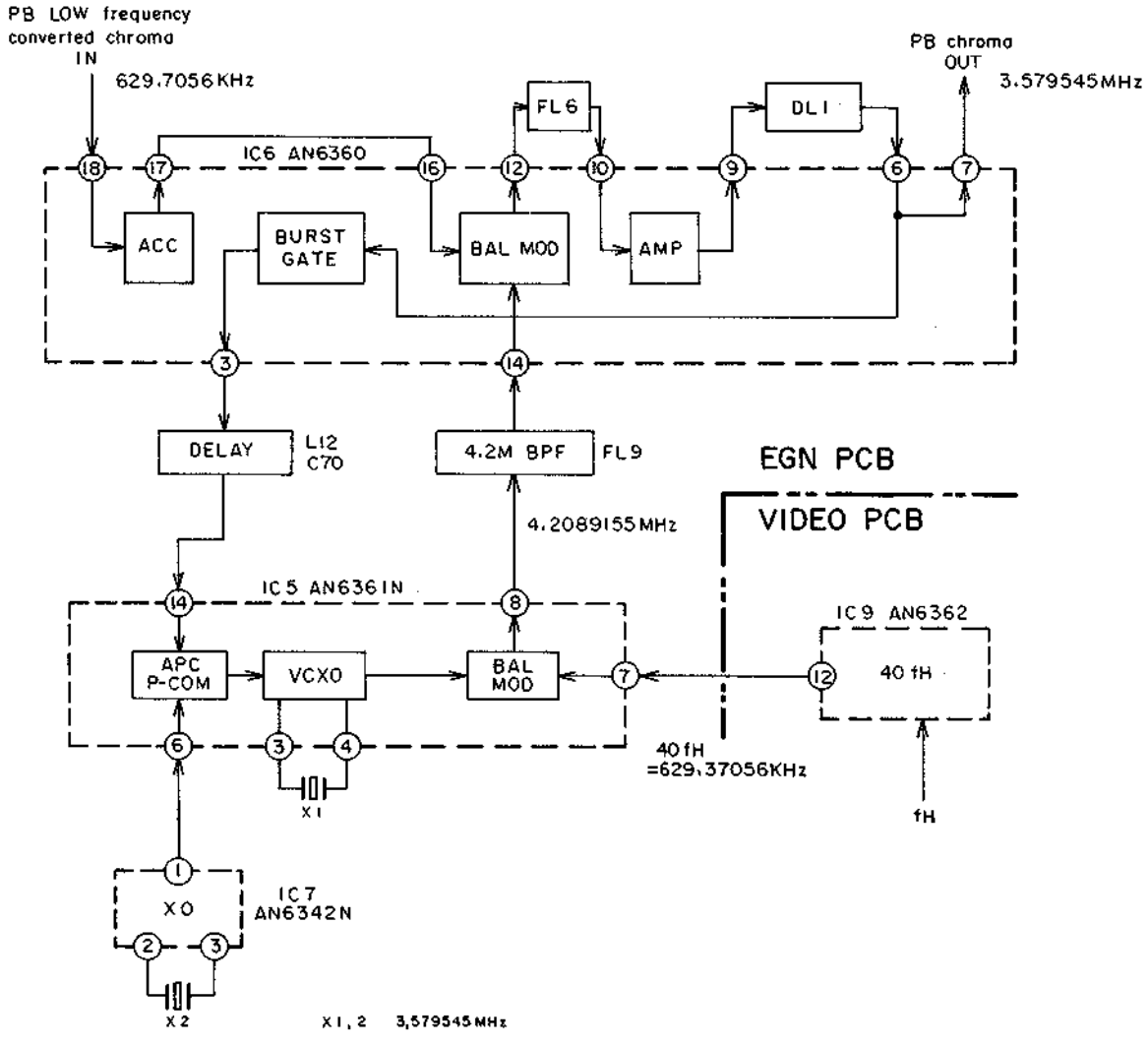


Fig. 7-16 Block Diagram of NTSC 3.58 Playback

Low frequency converted PB CHROMA supplied to IC6 pin (18) passes through the balance modulator within IC6, is converted to a 3.58 CHROMA signal, passes through FL6 (3.58 MHz±500 kHz), is amplified between pin (10) and pin (9), passes through DL1 (3.58 M 1H delay) is fed to pin (6), output from pin (7), level adjusted by VR14, and output to VIDEO OUT.

2-2-5 SECAM L PLAYBACK CIRCUIT

The PB signal fed from the pre-amplifier, is connected to the LPF FL-12 (LCB-59), TR43, and TR45, which select only the CHROMA signal components below 1.5 MHz. The luminance PB FM signal is attenuated. The signal is now passed from the Video Board to the EGN P.C Board via Inter-Board connection PBC. Then, the signal is directed to pass through the 1.07 MHz bell filter composed of TR2, VL1, etc., whose characteristic corrects for the 1.07 inverse bell filter used during recording. Since the gain of the following stage limiter amplifier, is high compared with that during playback, the optimum limiter input level should be adjusted.

The signal fed to IC1 (μPC1004C EGN PCB) pin (1) is subjected to a limiter operation. There the AM component of the PB 1/4 fc CHROMA signal, which was added during the process of electromagnetic conversion is removed, and waveform shaping is performed in readiness for the next stage double multiplying circuit. In order to return to the original CHROMA signal, quadruple multiplication is required. In IC1, double multiplication first of all is performed by the combination of the quadrature detector and filter FL8.

The output is output from pin (8), directed to pass through EF TR3, and then through the 2.2 MHz BPF (FL2 and FL3) to attenuate noise, etc. other than fundamental signal after the frequency doubling operation. Then, the signal is caused to pass through another frequency doubling circuit composed of TR4, D1, and D2, which restores the 1/4 count down signal to the original condition during recording.

The next filter, FL4, is a 4.43 MHz BPF, which removes noise, etc. other than the fundamental signal which has been multiplied by 4. The CHROMA signal amplified by TR5 and noise gated (at Rec Mode) by TR6 is directed to pass through EF TR7, and further through the 4.29 MHz bell filter composed of VL2. The characteristic corrected by the bell filter during the time of recording process is returned to the original condition so as to provide the BELL characteristic similar to the time it is transmitted as a TV signal.

The final output is directed to pass through EF TR8. It then passes to the Video Board via Inter-Board connection SL OUT on which the level is adjusted at C PB LEVEL VR15, fed to IC6 pin (15) via TR38, and mixed with the PB-Y signal.

1) IC1 (μPC1004C) function (EGN P.C Board)

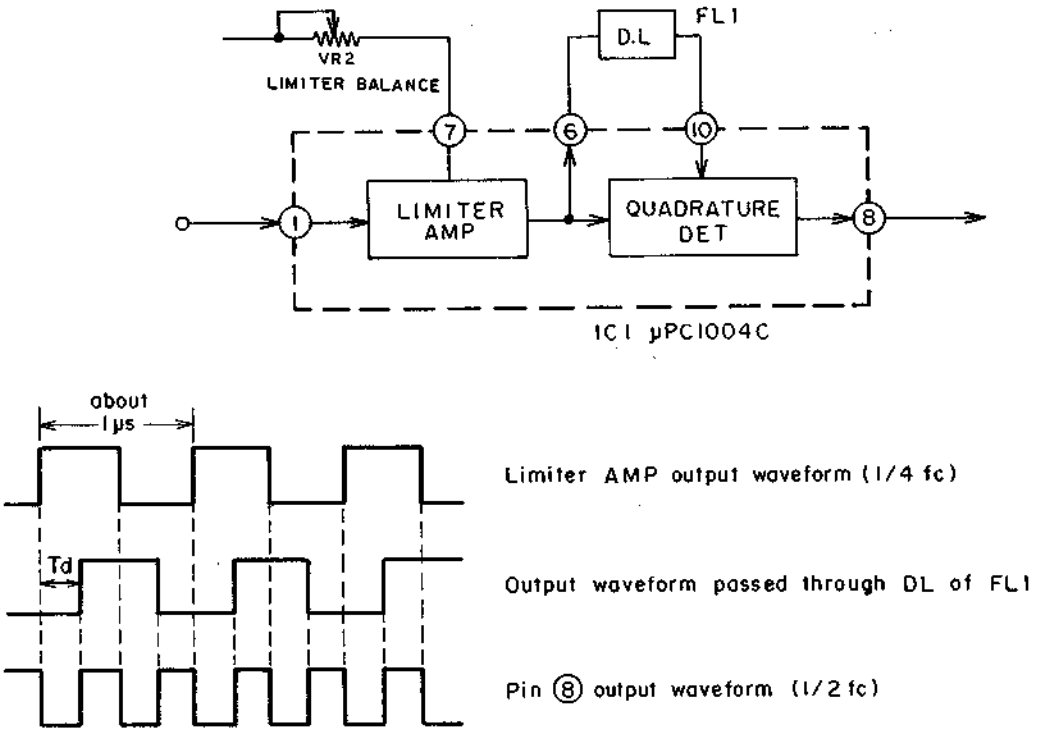
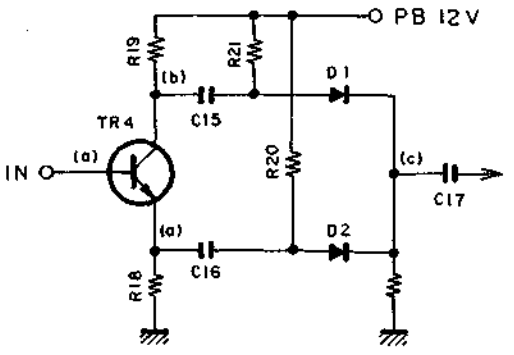


Fig. 7-17 Double Multiplying Circuit Block Diagram

This IC has a limiter amplifier and a frequency doubling circuit. The frequency doubling circuit consists of a quadrature detector and delay line (0.24 μs) FL1.

The signal passed through FL1 and the signal directly entering the quadrature detector, are detected which results in a doubled frequency component at the output.

2) Frequency doubling circuit



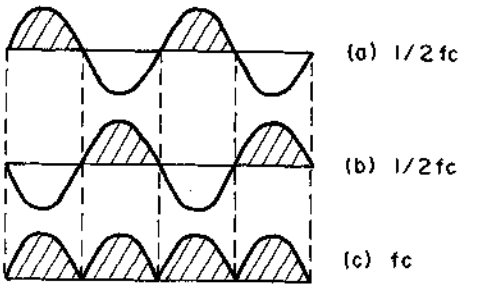


Fig. 7-18 Frequency doubling circuit

The signal at the emitter of TR55 is in phase with the input signal but a 180° reversed signal appears at the collector. Twice the original frequency is obtained by half-wave rectifying and mixing the signals at D23 and D24 respectively. (Refer to Fig. 7-18)

3) 1.07 MHz Bell Filter

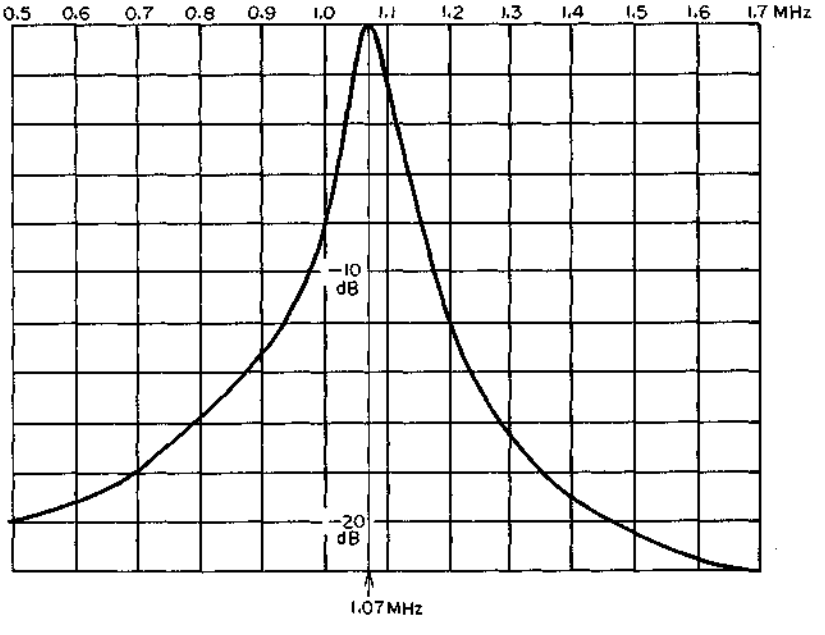


Fig. 7-19 1.07 MHz Bell Filter

Since the signal was subjected to the anti-bell filter operation during recording, it will be directed to pass through the bell filter with the complementary characteristic during the playback. That is, this is DE-EMPHASIS to PRE-EMPHASIS in recording. Its characteristic is shown in Fig. 7-19. Here, the amplitude of frequencies that had been emphasized are restored to the original condition and the response becomes uniform relative to the center frequency.

4) Limiter

The signal equalized by the PB EQ has become uneven in its amplitude due to noise, drop-out, uneven recording/playback, etc., i.e., it is amplitude modulated. In order to keep the amplitude constant, amplitude limiting is performed by the limiter. Then, the signal is directed to the next MPX.

5) BPF

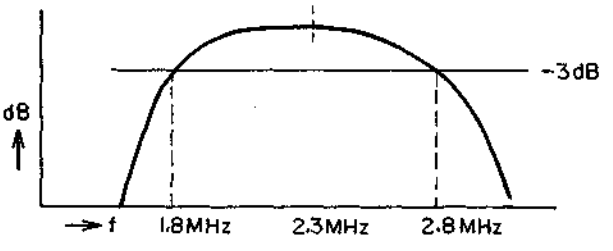


Fig. 7-20 Characteristics of Band Pass Filter

The frequency of the 1.07 MHz CHROMA signal is doubled (2.14 MHz) by the first doubling circuit. Unwanted signals are removed by the 2.14 MHz BPF.

6) NOISE GATE pulse

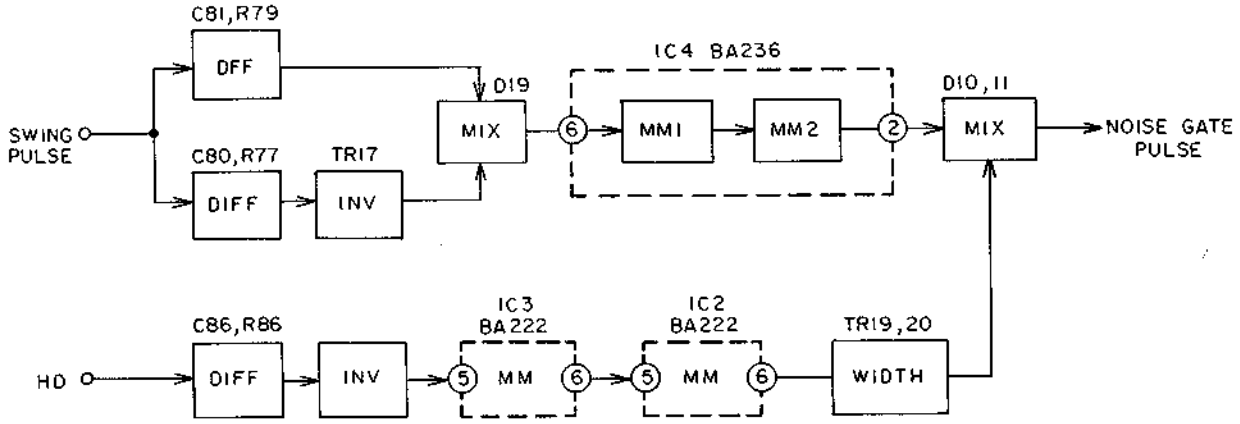


Fig. 7-21 Noise Gate Pulse Generation Block Diagram

The Noise Gate pulse circuit has the configuration as shown in Fig. 7-21 to eliminate noise generated as the SECAM L CHROMA signal is played back. (As CHROMA signal is passed through the limiter, noise occurs in the non-FM modulated SYNC/BLANKING period due to the absence of a CHROMA component on that period.) The horizontal noise gate pulse obtained from the HD signal which has its phase and width synchronized with that HD signal and the vertical noise gate pulse obtained from the switching pulse are mixed together at D10 and D11. The signal resulting from the mixing is fed to the PB SECAM-L signal circuit, and noise during part of the horizontal/vertical SYNC/BLANKING period is eliminated.

7) Band Pass Filter (BPF)

The 4.28 MHz converted CHROMA signal is routed through the BPF shown in Fig. 7-22, which eliminates unwanted signals.

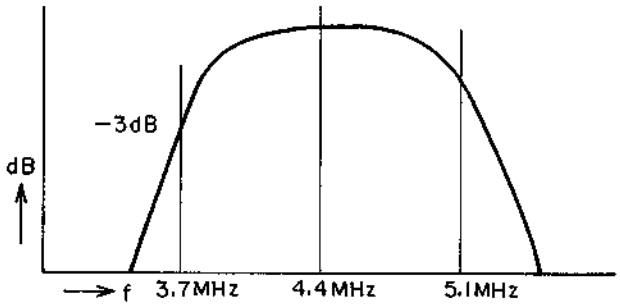


Fig. 7-22 Characteristics of BPF

8) Anti Bell Filter

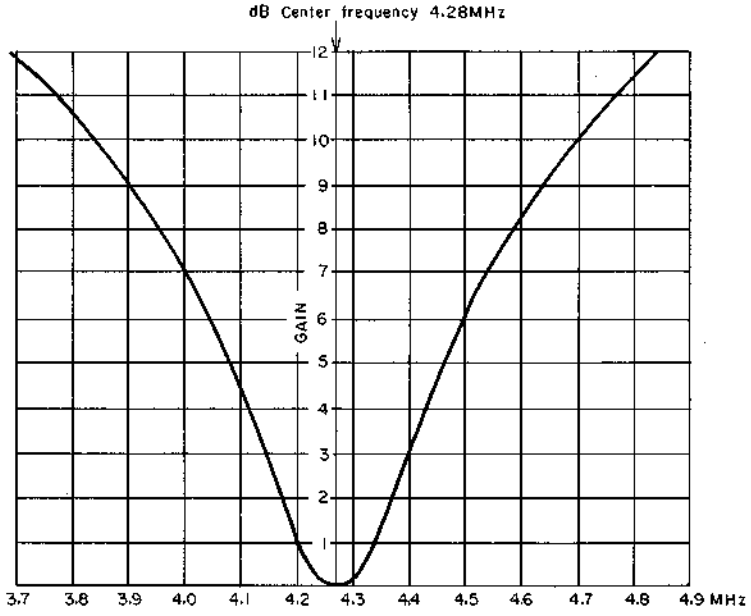


Fig. 7-23 Characteristic of Anti Bell Filter

The chroma signal is ultimately routed to the Anti Bell Filter shown in Fig. 7-23, for suppression of the CHROMA FM signal. The output is the PB CHROMA signal.

2-3 SECAM DETECTOR

1) SD-1 (on Video PC Board)
The BURST signal from IC10 (AN6360) pin (3) is connected to FL17 which is a 4.5 MHz SAW (Surface Acoustic Wave) filter. Accordingly, when there is a SECAM signal, BURST signal is obtained, the amplitude of which varies form 1H to the next. This is amplified by TR60–62, and routed to through the 8 kHz BPF composed of VL1, C186, L30, and C187, to the peak detection circuit of D28, D29, and C160.
As ta result, the base of TR51 becomes 'H', and SD-1 the line connected to the collector becomes 'L'. This is used for the identification of SECAM B, G signals.

2) SD-2 (on EGN PC Board)
The HD (Horizontal Drive) pulse from IC9 pin (18) on the Video Board enters the emitter follower of TR10 on the EGN PC board. The delay value and the width are determined by L4, C27, and R40, and the pulse becomes a BURST GATE pulse. Only the BURST signal of the PB SECAM-L signal is sampled. Subsequent operation is the same as the SD-1 operation. That is, SD-2 becomes 'L' during the time of SECAM-L signal playback.

2-4 VIDEO JUDGE (ON SERVO PC BOARD)

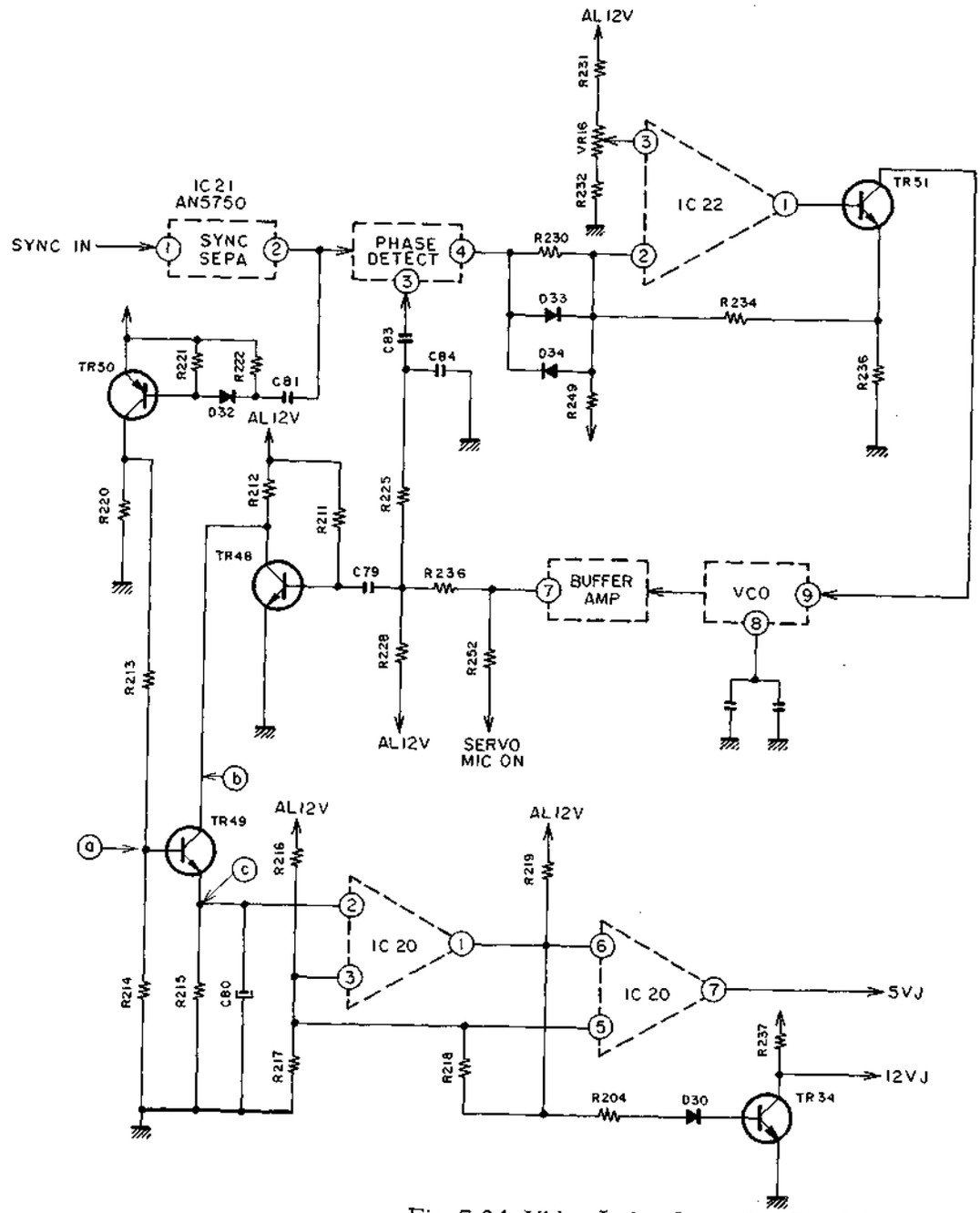


Fig. 7-24 Video Judge Operation Block Diagram

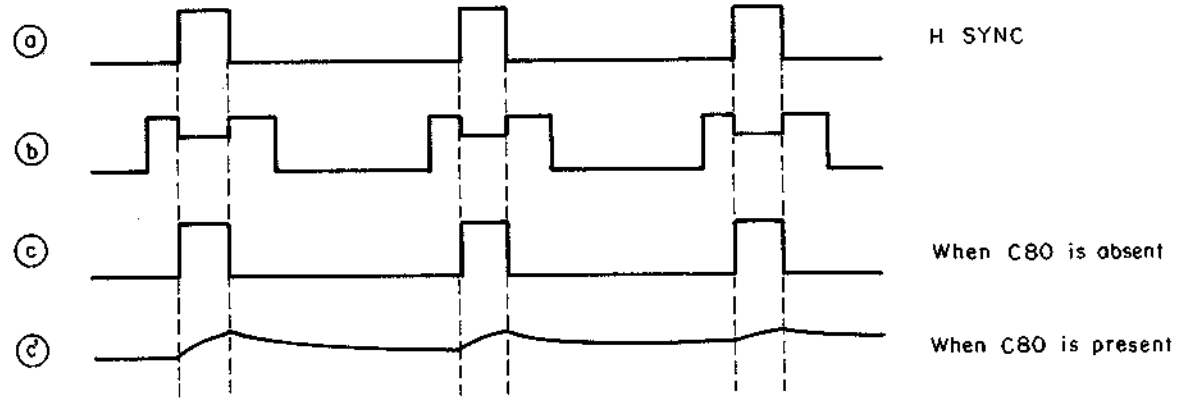


Fig. 7-25 Video Judge System

The Video Judge (video signal presence/absence) detects whether or not H SYNC is present, and acts on this information. IC22 is used for the extension of the lock range of the AFC system.

The SYNC input from IC21 (AN5750) pin ① is subjected to SYNC separation to isolate H SYNC, which is amplified by TR50, and fed to the base of TR49. On th other hand H SYNC resulting from SYNC separation is a DC voltage used in the phase detector, and controls the internal VCO.

That is, the ouput frequency and the phase of the VCO are locked to the input H SYNC.

Since the waveform (C) is the output from TR49, when this voltage becomes higher than the set potential (about switches 2.5 V) of IC20 (AN6914) pin ③, output pin ① becomes 'L', and TR34 becomes OFF, i.e., 12VJ becomes 'H'.

Since pin ⑥ is 'L', 5VJ becomes 'H', (5V).

When there is no H SYNC, i.e., there is no video signal, both 12VJ and 5VJ become 'L'. (See Fig. 7-25)

2-5 REFERENCE SIGNALS IN EACH MODE (ON VIDEO PC BOARD)

	VIDEO absent			VIDEO present		
	EE	P.B	C/R	EE	P.B	C/R
REF V	PAL: 50 Hz NT: 60 Hz	PAL: 50 Hz NT: 60 Hz	VP	INPUT V	PAL: 50 Hz NT: 60 Hz	VP
V SYNC	PAL: 50 Hz NT: 60 Hz	PAL: 50 Hz NT: 60 Hz	VP	INPUT V	INPUT V	INPUT V
H SYNC	HP	HP	HP	SFP	SFP	SFP
VIDEO OUT	HP + PAL 50 Hz NT 60 Hz	HP + PAL 50 Hz NT 60 Hz	HP + VP	INPUT VIDEO	INPUT VIDEO	INPUT VIDEO + VP

Fig. 7-26 Reference Signals in Each Mode

3. SERVO CIRCUIT OPERATION

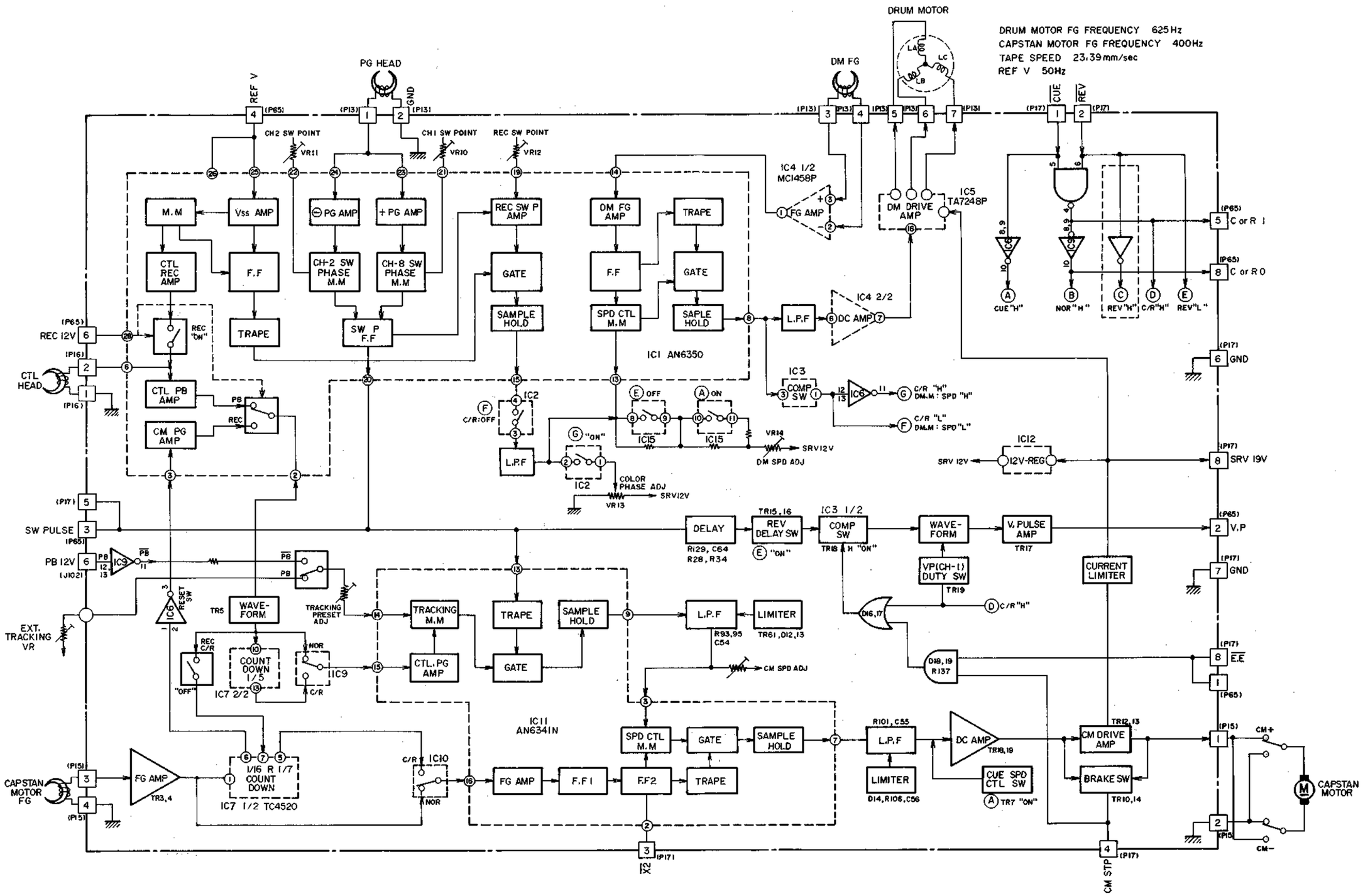


Fig. 7-27 Block Diagram (PAL/SECAM)

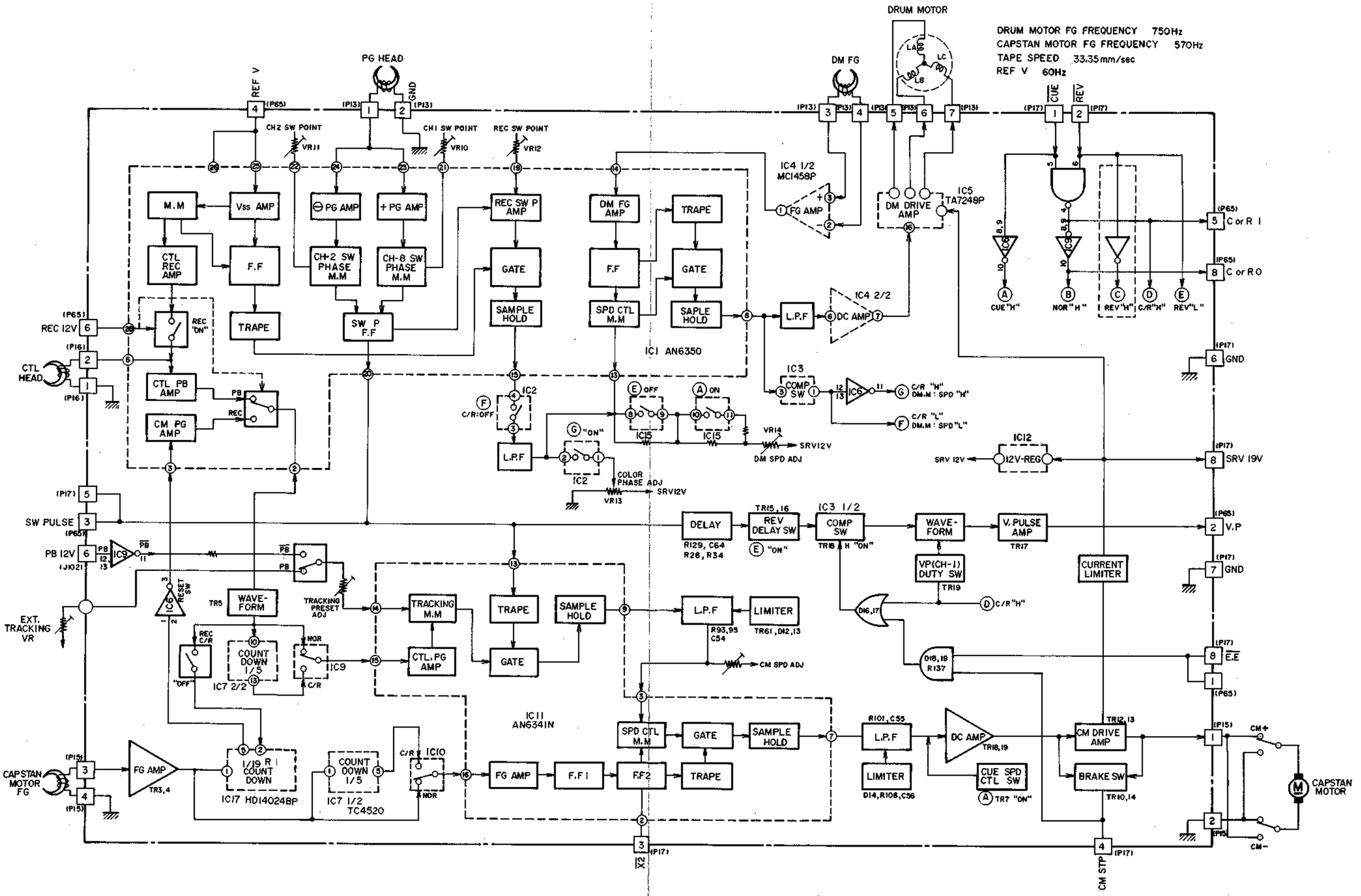


Fig. 7-28 Block Diagram (NTSC)

3-1 GENERAL

VS-2 EGN includes PAL (SECAM) and NTSC servo circuits. The PAL (SECAM) servo circuit is mainly described herein, and the description of the NTSC servo circuit is limited to parts differring from the PAL (SECAM) servo circuit.
In addition to the normal speed recording and playback servo circuits, the VS-2 EGN servo circuit icnludes the simplified still playback circuit for playback.
For PAL (SECAM), there are CUE (forward directin) and REVIEW (reverse direction) servo circuits of about 7 times the normal speed.
Servo circuits are largely classified as follows:

1) Drum motor servo circuit
   ⓐ Drum motor phase control circuit
   ⓑ Drum motor speed control circuit
   ⓒ Drum motor drive circuit
2) Capstan motor servo circuit
   ⓐ Capstan motor phase control circuit
   ⓑ Capstan motor speed control circuit
   ⓒ Capstan motor drive circuit &
   Capstan motor starting current limiting circuit
3) Automatic editing control servo circuit
4) Quasi-vertical synchronization pulse generator circuit
5) PAL (SECAM)/NTSC switching circuit
6) Automatic discriminator circuit

The drum motor servo circuit and the capstan motor servo circuit include the recording servo circuit, normal playback servo circuit, about 7 times faster (about 5 times in PAL and NTSC modes) servo circuit, and electronic editing servo circuit.
AKAI call the 7 times faster mode (NTSC 5 times) QUICK FINDER, the forward direction is called CUE, and the reverse direction is called REVIEW (or REV).

3-2 CAPSTAN SERVO CIRCUIT

The capstan servo circuit runs the magnetic tape at a constant speed of 23.39 mm/sec (33.35 mm/sec in the case of NTSC system), and it also controls the video head so it runs accurately aligned with the recorded video track during the playback.
In addition, when either a tape recorded by an other maker's VHS standard VTR or a pre-recorded tape is reproduced, the video head path can be adjusted by the TRACKING knbo on the front panel so that the video head runs accurately over the video track.
Since the capstan motor is a DC motor, the servo requires a phase control circuit and a speed control circuit.
For this reason, IC AN6341 which has a built-in phase control circuit and a speed control circuit is used.

3-2-1 PHASE CONTROL

The Switching pulse (25 Hz for PAL/SECAM system, 30 Hz for NTSC system) form the drum motor servo circuit (IC1 pin ⑳) is supplied to IC11 (AN6341N) pin ⑬ as a reference signal A . Comparison signal is supplied to IC11 pin ⑮. The comparison signal at used during the time of recording differs from that at the time of during playback. The comparison signal used during the CUE mode differs from that during REVIEW.
Fig. 7-29 shows the reference signal and comprison signal of the capstan motor phase control circuit.

Mode	REFERENCE SIGNAL	COMPARISON SIGNAL
RECORDING	SWITCHING PULSE	$\frac{\text{CAPSTAN MOTOR FG}}{16}$ = 25 Hz
PLAYBACK	SWITCHING PULSE	CTL PULSE
CUE or REVIEW	SWITCHING PULSE	$\frac{\text{CTL PULSE}}{7}$

Fig. 7-29 Reference signal and comparison signal of various modes

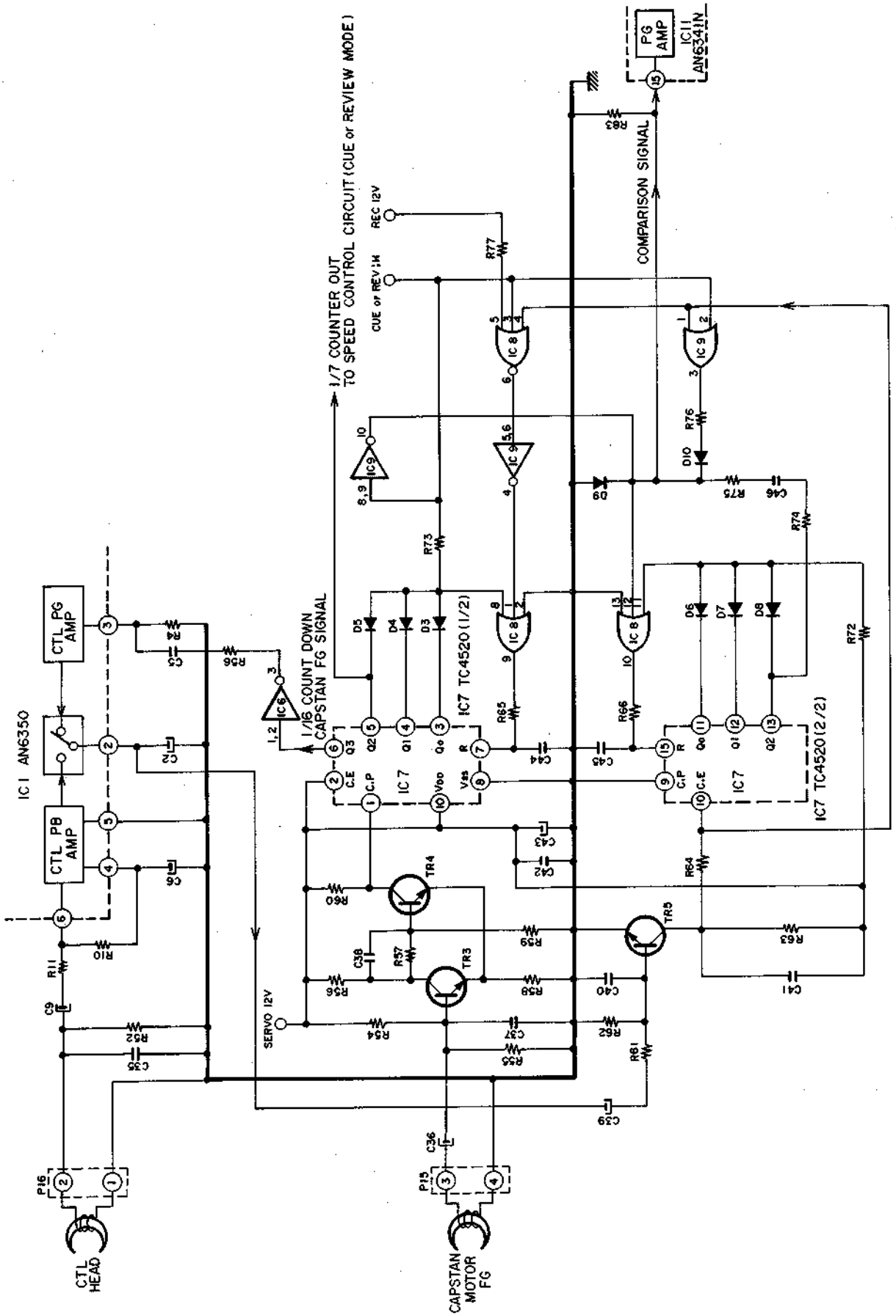


Fig. 7-30 Comparison signal

The capstan motor FG frequency is 400 Hz. The capstan motor FG signal is shaped to a square waveform by the FG AMP (Schmitt cirucit) of TR3/4, and is fed to IC7 (TC4520BP) pin ①. IC7 1/2 is the 1/7 and 1/16 counter circuit. Only the 1/16 counter circuit is described here, since the 1/7 counter circuit is described in the part dealing with the speed control circuit.

1) 1/16 counter circuit (Refer to Fig. 7-30)

The condition of the RESET terminal (IC7 pin ⑦) of the 1/16 counter circuit is as follows:

ⓐ During recording

Since REC 12V is fed to IC8 pin⑤ IC8 (HD14075BP) pin ⑥ becomes high level. Since IC9 (HD14001BP) is an inverter, the output thereof (IC9 pin ④) becomes low level. Accordingly, IC8 pins⑧,①, and② become low level, IC8 pin ⑨ becomes low level, and therefore the RESET terminal (pin ⑦) becomes low level. Accordingly, the 1/16 counter is not reset. The capstan motor FG pulses are frequency divided by 16 down to 25 Hz and output on IC7 pin⑦.

ⓑ During playback

During playback, the CTL pulse reproduced at the CTL head passes through the CTL PB AMP of IC1, is inverted amplified at TR5, shaped, and fed to IC8 pin ④. At this time, since IC8 pins ⑤ and ③ are low level, the CTL pulse is output to IC8 pin⑥.

This pulse is inverted at the inverter IC9, and is fed to the RESET terminal (pin⑦) via the next IC8.

Accordingly, the 1/16 capstan motor FG pulse (25 Hz) which is reset by the CTL pulse is output from pin ⑥

During playback, the 1/16 counter is reset by the CTL pulse to prevent picture deformation during the switching from the electronic editing playback mode to the electronic editing recording mode.

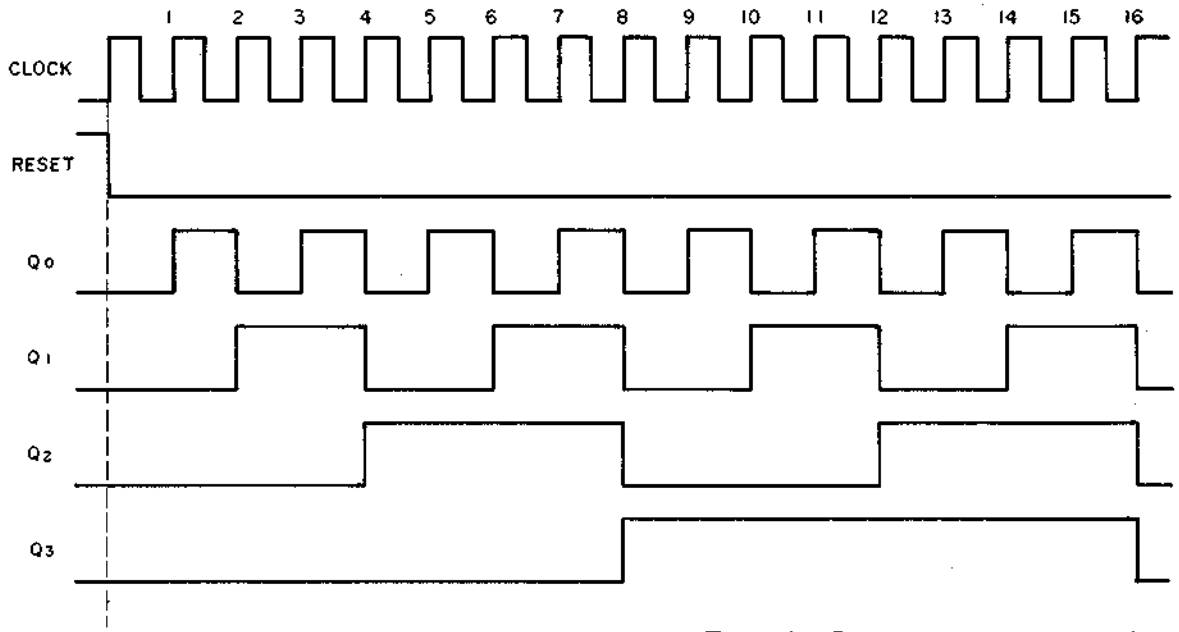


Fig. 7-31 Binary counter timing chart

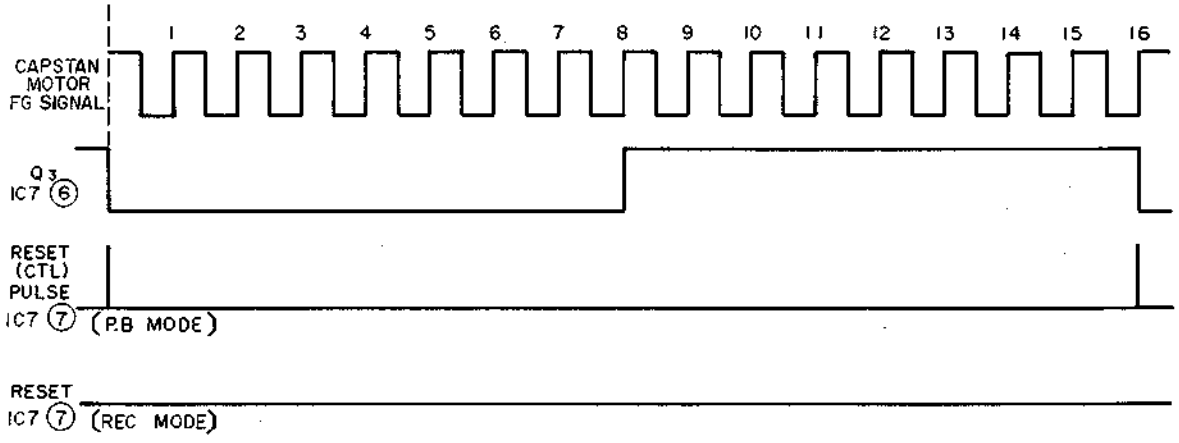


Fig. 7-32 1/16 counter timing chart

The capstan motor FG pulses whose frequency is divided by 16 is inverted at the inverter, and fed to IC1 pin ③. This signal is routed through the CTL PG AMP and the REC/PB switch, output from pin ②, and fed to TR5.
This signal is subjected to inversion, amplification, shaping by TR5, and is then fed to IC7 pin ⑩.

2) 1/7 counter (Refer to Fig. 7-30)
IC7 2/2 is a 1/7 counter circuit.

ⓐ During recording
The 1/16 capstan motor FG pulses shaped by TR5 are fed to IC9 pin ①.
Since IC9 pin ② is at the low level in the recording mode, the iverted waveform of pin ① is output to IC9 pin ③. This output is fed to IC11 pin ⑮ as a comparison signal through R76, D10 and TR22.

ⓑ During playback
The CTL pulse reproduced at the CTL head is fed from IC1 pin ⑥, output from pin ② through the CTL PB AMP and REC/PB switch, and fed to TR5.
This CTL pulse is shaped at TR5, and fed to IC9 pin ①. Afterwards in a similar way to the recording mode of operation, the signal is fed to IC11 pin ⑮ as a comparison signal.

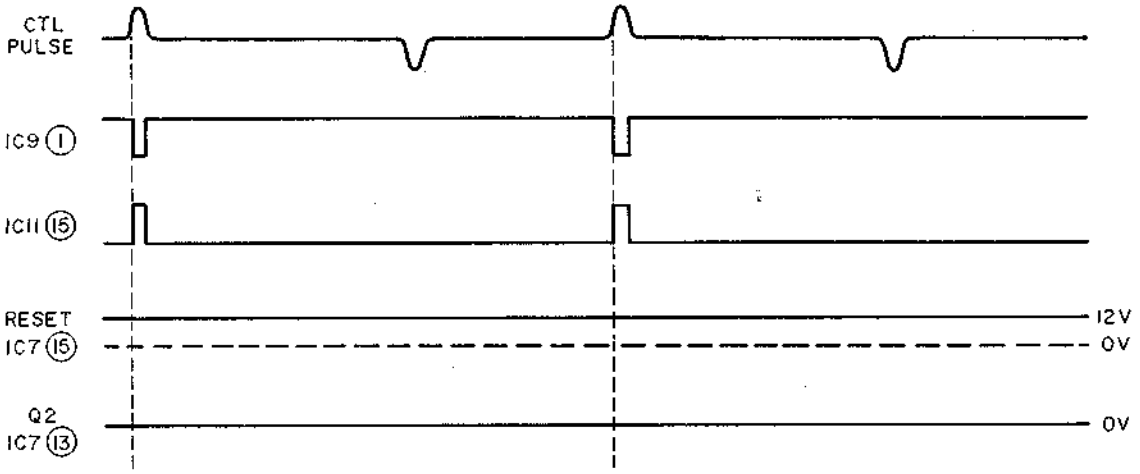


Fig. 7-33 REC/PB mode timing chart

ⓒ CUE or REVIEW mode (refer to Fig. 7-30)
Since CUE or REVIEW (hgih level) is applied to IC9 pin ②, IC9 pin ② is at the high level. Accordingly, IC 9 pin ③ becomes low level, and D10 is cut off.
On the other hand, IC8 pin ⑫ is at the low level, as known from the examination of the state of the RESET terminal (pin ⑮) of IC7 2/2.
That is, CUE or REVIEW ('H') is fed to IC9 pins ⑧ and ⑨, inverted and supplied from IC9 pin ⑩.
Since the AND circuit composed of D6, and 8 and R72 is connected to IC8 pin ⑪, the RESET pulse is output to IC7 pin ⑮. The 7 times rate CTL signal reproduced at the CTL head is inverted at TR5, fed to IC7 pin ⑩, counted down to 1/7, and output from pin ⑬. This pulse is differentiated at R74, C46, R75, D9, and R83, and fed to IC11 pin ⑮ as a comparison signal.

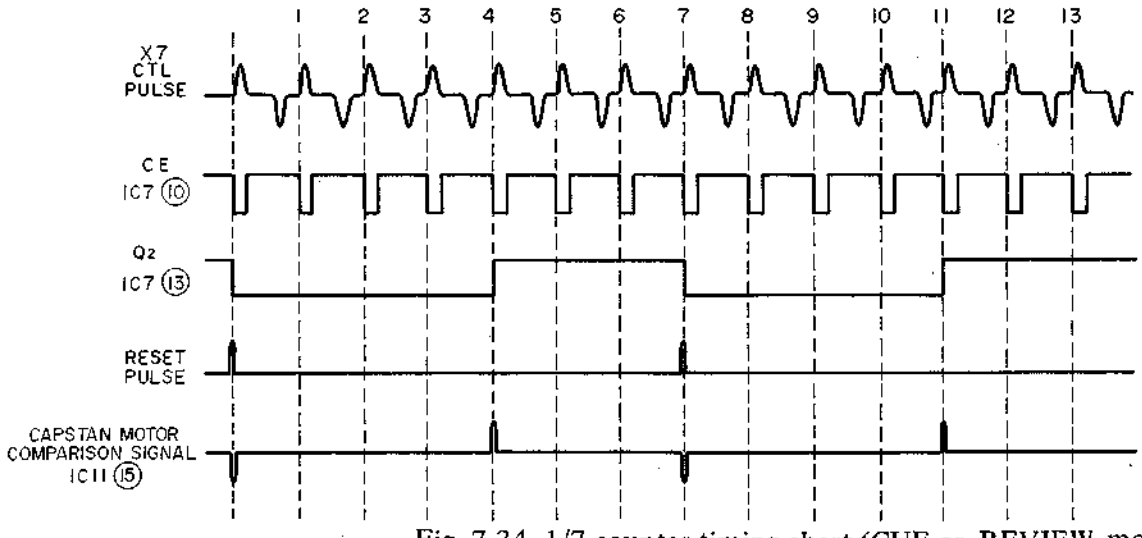


Fig. 7-34 1/7 counter timing chart (CUE or REVIEW mode)

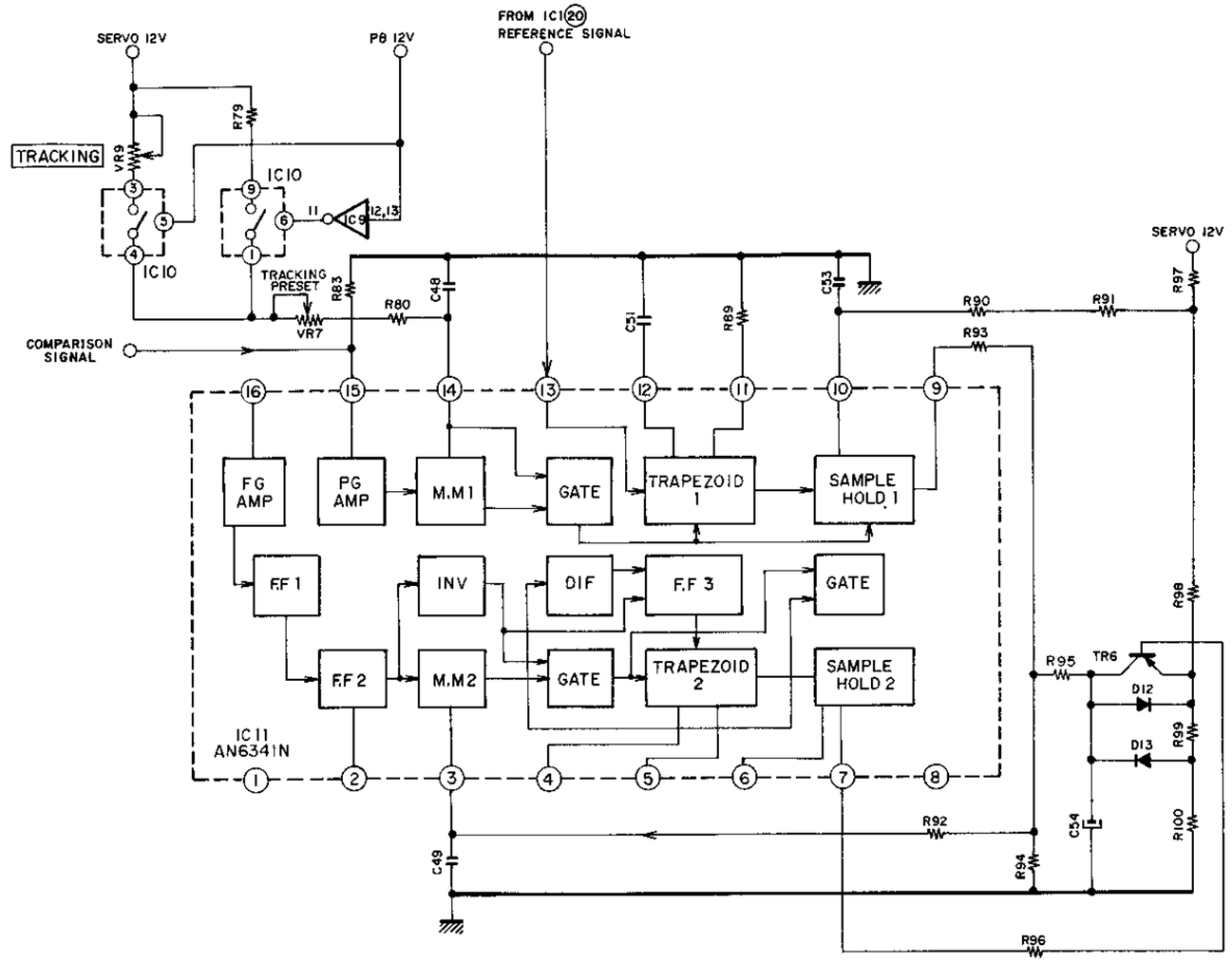


Fig. 7-35 shows the main elements of the capstan motor phase control circuit.

The comparison signal having entered IC11 pin (15) is amplified by the PB AMP, and fed to the Mono-Multi 1. Mono-Multi 1 is triggered at the leading edge of the comparison signal. The delay time of this Mono-Multi is determined by the time constant connected to pin (14).

(d) During recording

During recording, PB 12V ('L') is inverted at IC9, and a high level PB signal is fed to IC10 pin (6), so pins (8) and (9) conduct. As a result, SERVO 12V is fed to IC11 pin (14) through R79, VR7, and R80, which determine the time constant of the Mono-Multi along with C48.

(e) During playback

PB 12V is fed to IC10 pin (5), and pin (4) and (3) conduct. As a result, SERVO 12V is fed to IC11 pin (14), through VR9, VR7, and R80, which determine the time constant of the Mono-Multi along with C48.

Tracking is adjusted by varying the time constant of the Mono-Multi by the Tracking Control Volume VR9.

Discharge current of C48 limits the internal resistance of the Mono-Multi, and delays the trailing edge of the control terminal pulse. This control terminals pulse and the output pulse from Mono-Multi 1 are fed to the next Gate 1. The sampling pulse is generated by means of the delay of the trailing edge of the CONTROL terminal pulse (pin (14)). This sampling pulse is fed to TRAPEZOID 1 and to the Sampling & Hold (S & H) Circuit. A reference signal (switching pulse) is supplied from IC1 pin (20) to IC11 pin (13). TRAPEZOID 1 is triggered at the traling edge of this reference signal. The trapezoidal wave is formed at the TRAPEZOID 1. The leading edge of the trapezoidal wave is determined by C51 connected to pin (12) and internal resistance, while the height of the trapezoidal wave is determined by R89 connected to pin (11).

The trapezoidal wave and the sampling pulse are fed to the S & H 1 circuit. The phase of the former is compared with that of the latter, and C53 is charged with that pulse voltage.

The output voltage of the S & H 1 circuit is output to pin (9). Hunting is prevented at the LPF (R93, R95, C54), and the output voltage is limited within a fixed range by the limiter circuit (TR6, D12, D13) so as to prevent abnormal rotation of the motor.

The output voltage thus obtained is fed to pin (3) of the speed control servo for the phase control of the capstan motor.

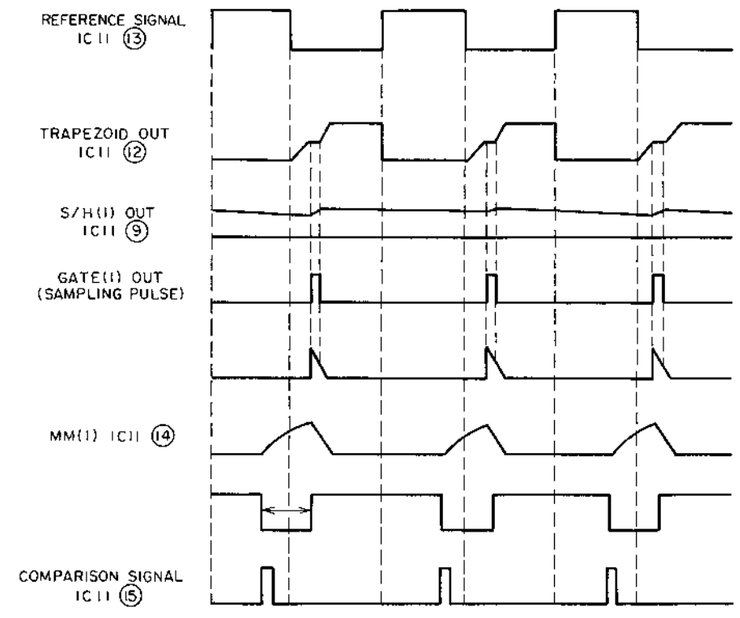


Fig. 7-36 Timing chart of capstan phase-control system in recording mode

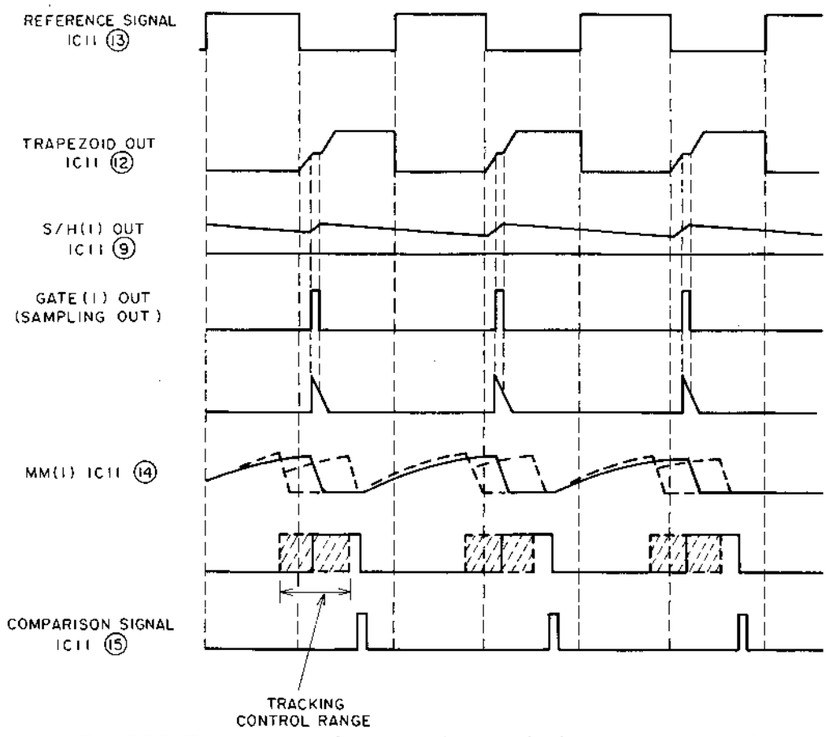


Fig. 7-37 Timing chart of capstan phase-control system in playback mode

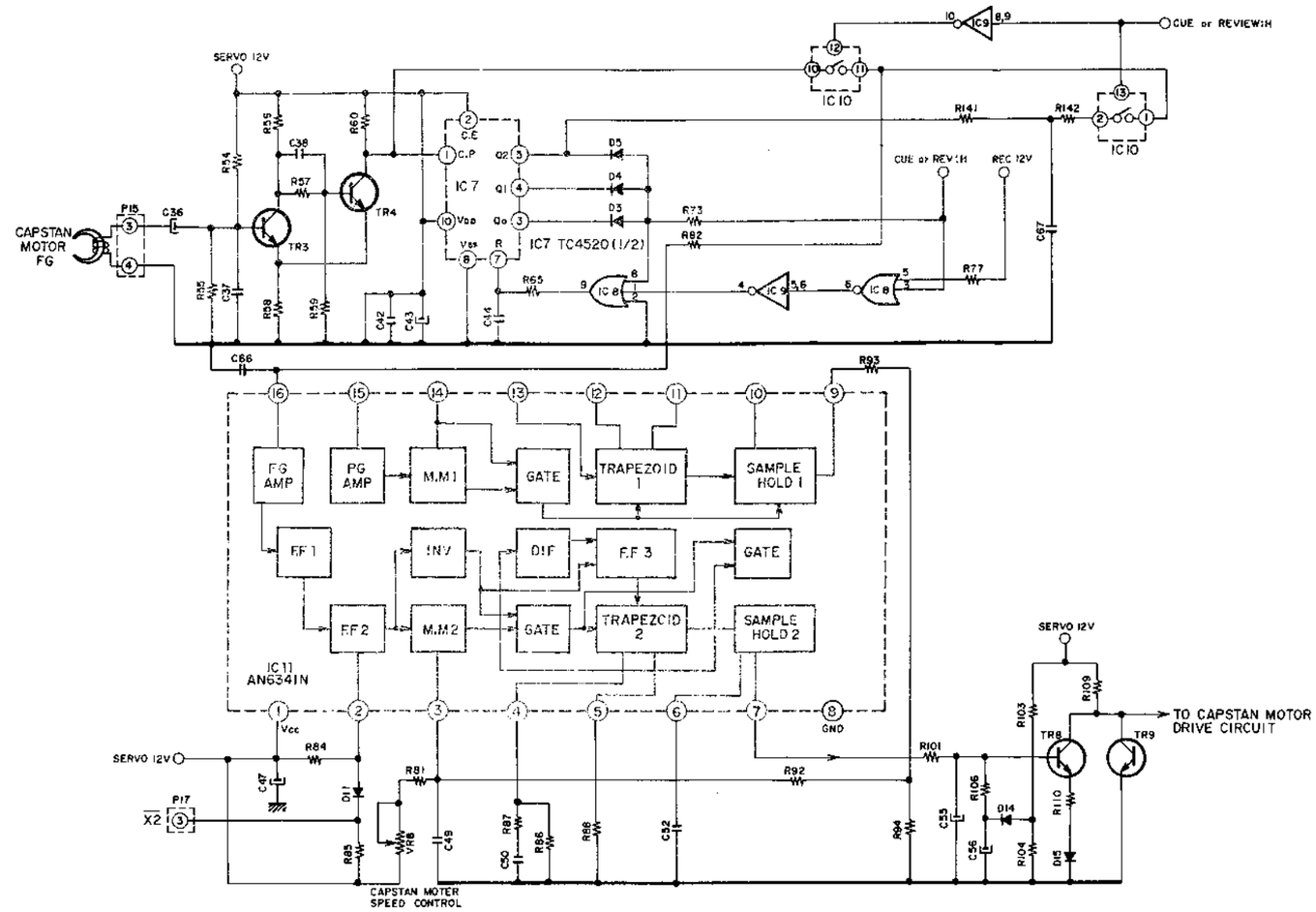


Fig. 7-38 Capstan motor speed control circuit

1) Recording and playback modes

The capstan motor FG frequency is 400 Hz (570 Hz in NTSC system). The capstan motor FG signal is shaped to a square wave at the FG AMP (Schmitt circuit) of TR3 and TR4.

The 400 Hz (570 Hz for NTSC system) pulse shaped at FG AMP is fed to the analog switch IC10 pin ⑩.

Since 12V is supplied to the analog switch control terminal IC10 pin 12 in REC and PB modes, this analog switch is ON. Accordingly, the signal fed to IC10 pin ⑩ is supplied to IC11 pin ⑯ via IC10 pin ⑪.

The FG signal fed to IC11 pin ⑯ is amplified at FG AMP, and its frequency is divided by 2 at flip-flop 1 making it 200 Hz (285 Hz in NTSC system).

Since IC11 pin ② is at the high level except in the electronic editing mode, flip flop 2 does not operate, and 200 Hz is fed to Mono-Multi 2..

Mono-Multi 2 is triggered at the leading edge of this pulse, and the delay time is determined by the time constant of C49, R81, and VR8 connected to the control terminal pin ③ and by the output voltage of the phase control circuit.

If the output voltage of the phase control circuit is constant, the delay time of Mono-Multi will be constant.

The output of this Mono-Multi 2 and the inverted output of flip-flop 2 are fed to GATE. Since the delay time of this Mono-Multi 2 is constant, a signal (GATE output) whose pulse width corresponds to the speed error, is output. The GATE output pulse fed to TRAPEZOID controls the rise time of the trapezoidal wave. That is, the peak value of the trapezoidal wave varies according to the pulse width of the GATE output, and the wider the pulse width, the longer the charge time becomes. This raises the peak value of the trapezoidal wave. Conversely, as the pulse width becomes narrower, the peak value of the trapezoidal wave becomes lower.

Charge time constant of the trapezoidal wave is determined by R86, R87, and C50 connected to pin ④.

TRAPEZOID 2 is triggered at the trailing edge of the output of flip-flop 3.

The output of TRAPEZOID 2 is supplied to S & H 2.

During the period while the sampling pulse is 'H', i.e., throughout the top part of the trapezoidal wave, the pulse is sampled, and an error voltage is produced.

In contrast to the method when the sampling pulse is generated using a capacitor, in a differential circuit, for example the width of the sampling pulse does not change.

Let's assume the case when the rotation of the capstan motor has become fast. As the speed of the capstan motor increases, the frequency of the capstan motor FG becomes high, the frequency divided at flip-flop 1 becomes high, and the period of the output pulse becomes short.

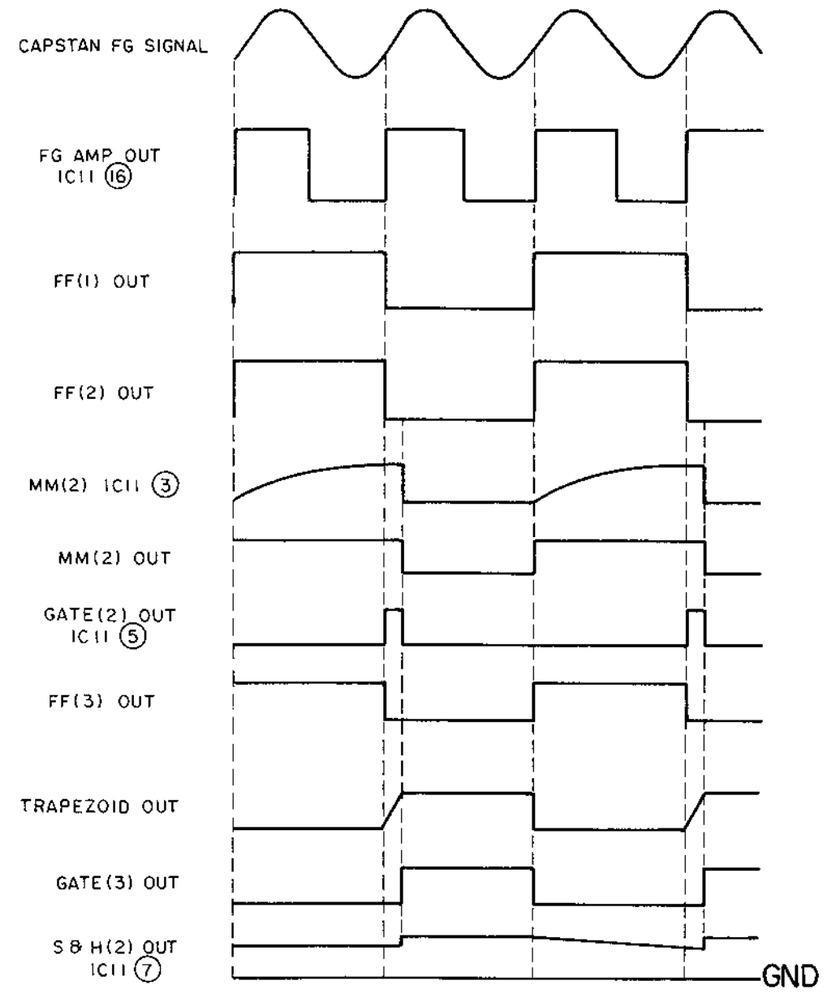


Fig. 7-39 Timing chart of capstan speed control system

If the output voltage of the phase control circuit is constant, the output of Mono-Multi 2 has a constant time period. Accordingly, the GATE output pulse width becomes wide, and the charge time of TRAPEZOID 2 becomes long. As a result the peak value of the trapezoidal wave becomes high, and the output voltage of the Sampling & Hold circuit becomes high.
This output voltage is inverted and amplified by the DC AMP (TR8 and TR9), and fed to the next capstan motor drive circuit. It lowers the voltage to be applied to the capstan motor, causes the capstan motor speed to fall, and returns the speed (rpm) to the original.
Conversely, when the capstna motor speed falls, the speed control circuit operates to increase the speed so as to return the speed to the original value.

2) CUE or REVIEW mode

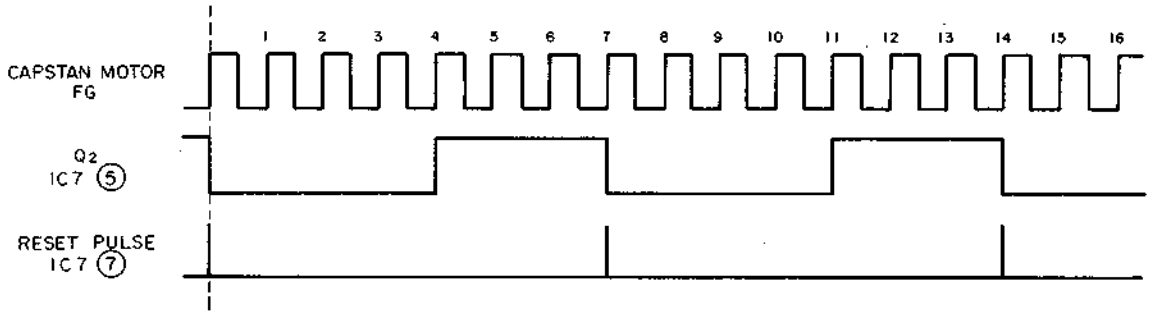


Fig. 7-40 Timing chart of 1/7 counter (CUE or REVIEW mode)

With CUE or REVIEW: H set to "H", the Ⓐ portion goes to "H" while the Ⓑ portion goes to "L". To implement the function of a 1/7 frequency divider, the counter must be started and then reset instantaneously upon reception of the 7th input pulse. From the binary counter timing chart, it can be seen that resetting upon 7th input pulse can be done when IC7 (pin ③ TR0, pin ④ TR1 and pin ⑤TR2) are at "H", and thus TR0, TR1 and TR2 are AND (D3, D4, D5, R73) so as for resetting.

Operation as the result of this frequency division is shown in the timing chart, Fig. 7-40 C44 and R65 make up an integration circuit which ensures a delay necessary to attain the proper reset pulse width so as to avoid malfunction of the counter.

3-2-3 NTSC MODE

The reference signal of the capstan servo phase control is the 30 Hz switching pulse available from IC1 pin ⑳. The comparison signal is a 30 Hz signal which is obtained by dividing the frequency of the capstan motor FG signal (570 Hz) by 19.

Since CUE or REVIEW in the NTSC system is 5 times faster, than the PLAY mode, the comparation signal in CUE or REVIEW mode is a CTL signal obtained by dividing the frequency by five.

The 1/19 counter circuit, CTL pulse 1/5 counter circuit, CTL pulse 1/5 counter circuit, capstan motor FG signal 1/5 counter circuit used in the NTSC mode alone are described in the following sections.

1) 1/19 counter

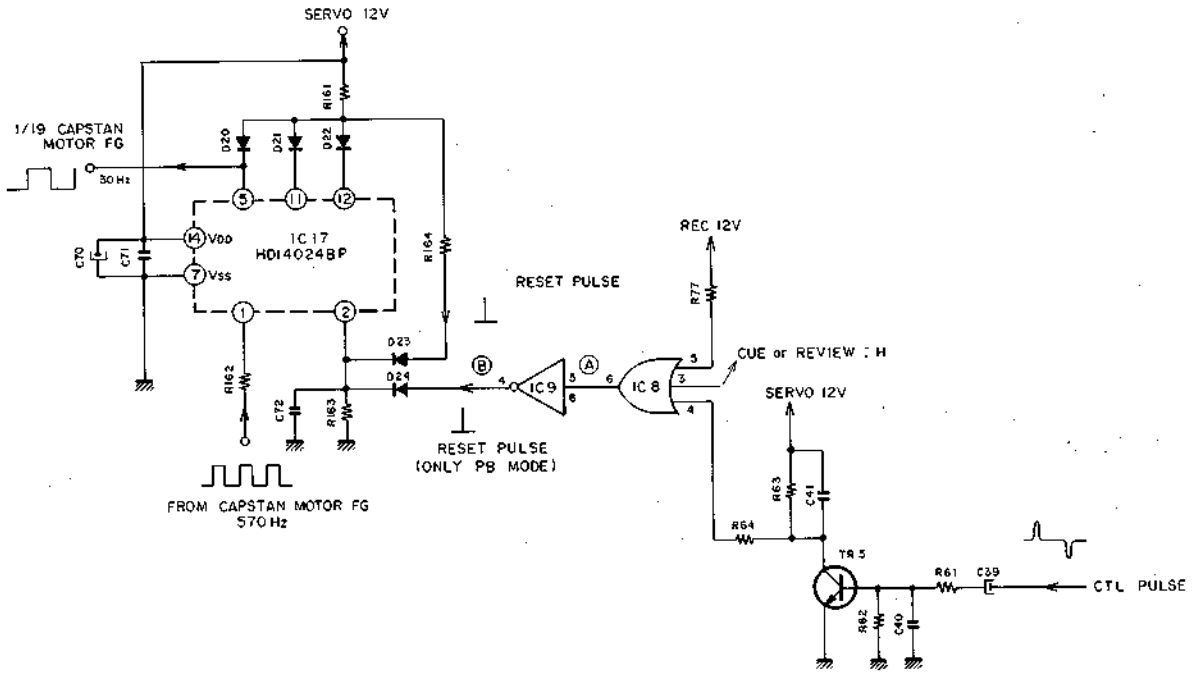


Fig. 7-41 1/19 counter circuit

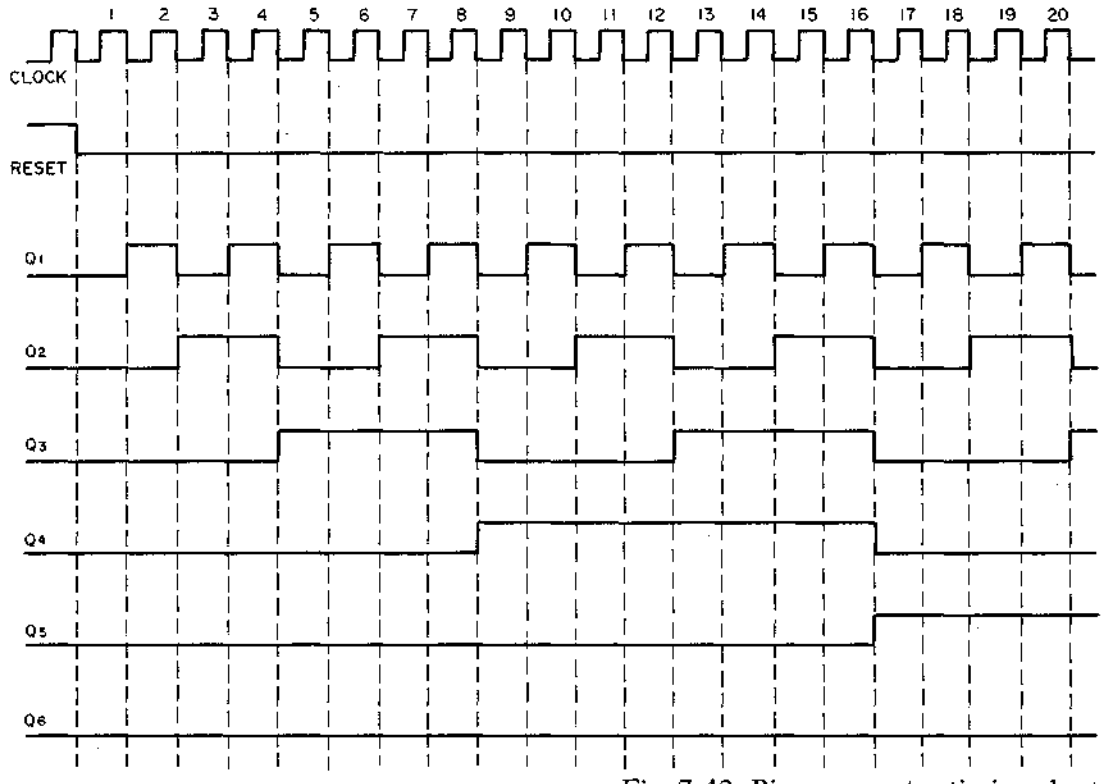


Fig. 7-42 Binary counter timing chart

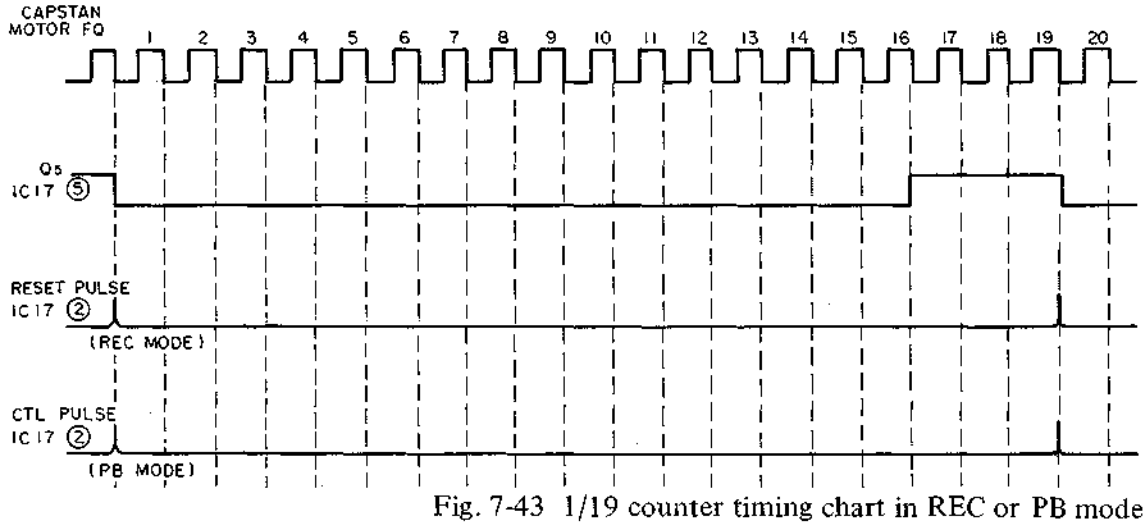


Fig. 7-43 1/19 counter timing chart in REC or PB mode

ⓐ Recording mode

In the recording mode, since REC 12V becomes 'H', A becomes 'H', and B becomes 'L', so the control pulse cannot reset. When TR1=H, TR2=H, and TR5=H, the 3 diodes D22, D21, and D20 cease to conduct, SERVO 12V is applied to IC17 pin ②, and reset is applied at the 19th period. (Refer to Binary Counter Timing Chart).

The capstan motor FG pulse whose frequency is divided by 19 is output to IC17 pin ⑤.

ⓑ Playback mode

In the playback mode, reset is always applied by the control pulse. Operation is the same as that of the 1/16 counter.

2) Control pulse 1/5 counter

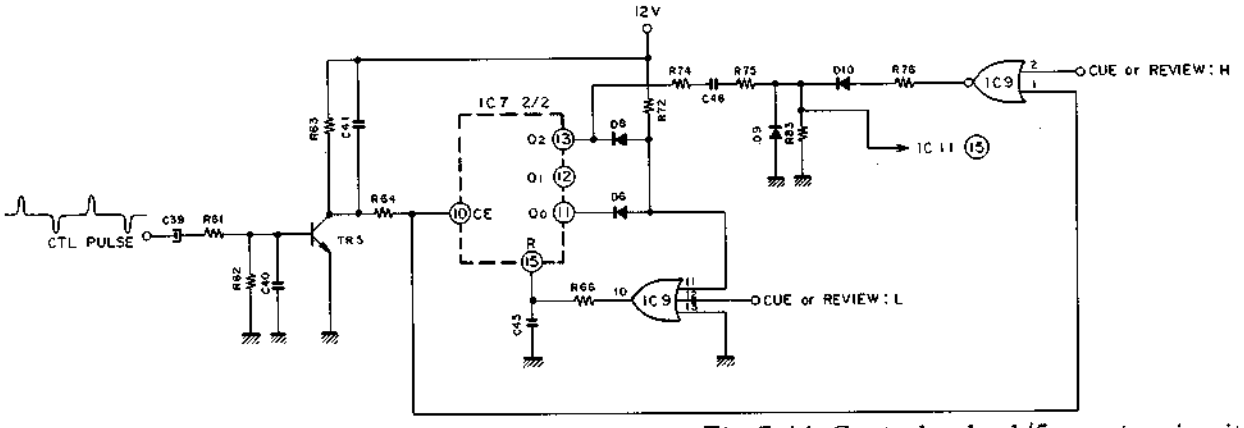


Fig. 7-44 Control pulse 1/5 counter circuit

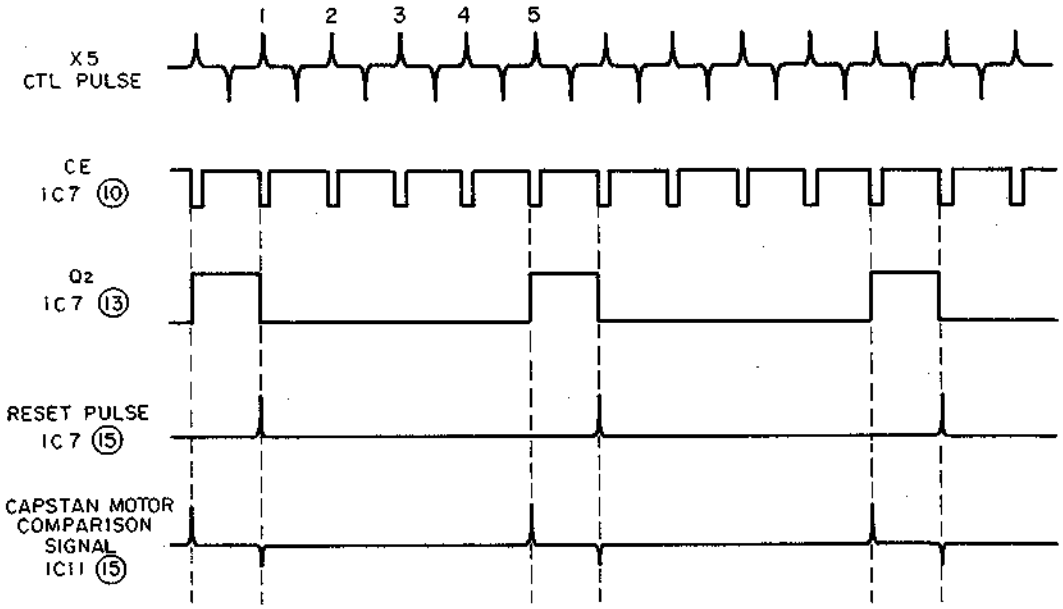


Fig. 7-45(A) Control pulse 1/5 counter timing chart in CUE or REVIEW mode

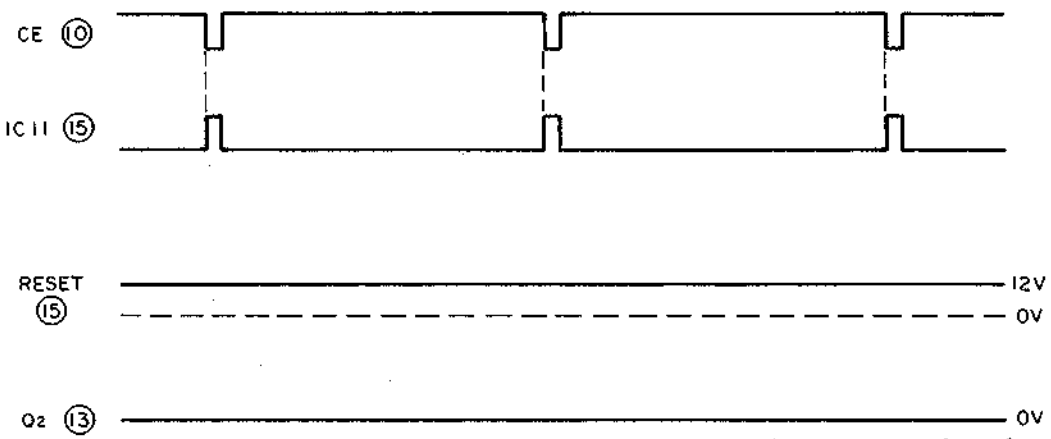


Fig. 7-45 (B) Control pulse 1/5 counter timing chart in normal mode

ⓐ CUE or REVIEW mode
The operation is the same as that of the control pulse 1/7 counter circuit of PAL (SECAM). To switch from the 1/7 counter to the 1/5 counter, TR1 is open circuited.
Fig. 7-45 (A) shows the timing chart.

ⓑ Normal mode (recording or normal playback mode)
The operation is the same as that of PAL (SECAM) mode.
Fig. 7-45 (B) shows the timing chart.

3) Capstan motor FG 1/5 counter

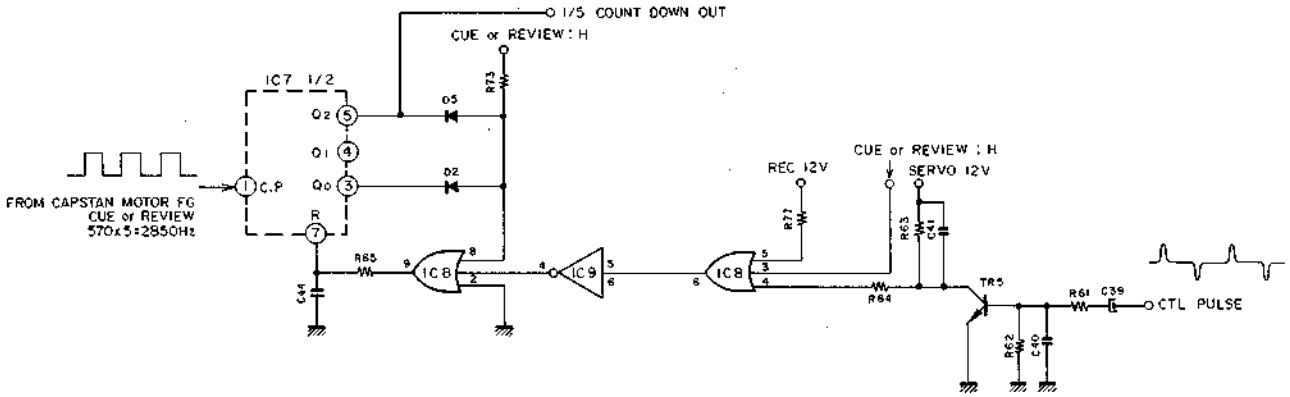


Fig. 7-46 Capstan motor FG 1/5 counter circuit

The operation is the same as that of the capstan motor FG 1/7 counter circuit.

To switch from the 1/7 counter to the 1/5 counter, TR1 is open circuited.

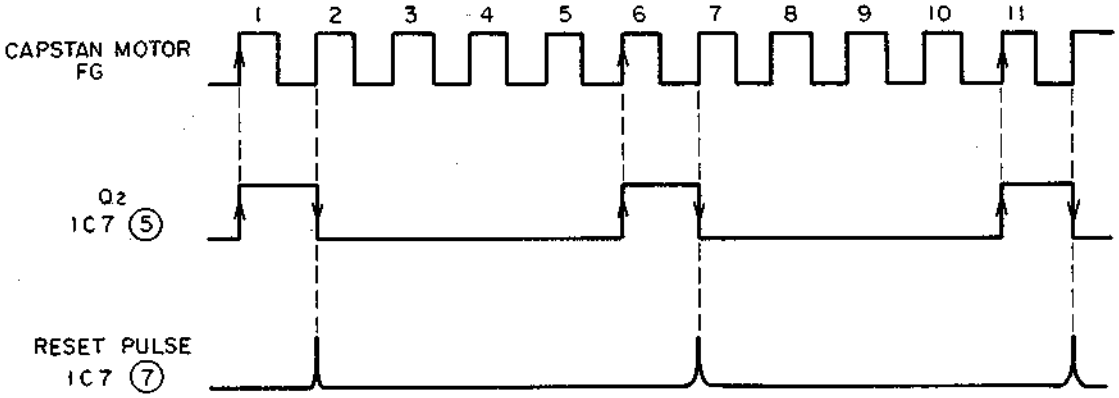


Fig. 7-47 Capstan motor FG 1/5 counter timing chart

3-3 DRUM SERVO CIRCUIT

The drum servo circuit sets the drum speed at 25 rpm/sec (30 rpm/sec in the case of NTSC system) in the recording mode taking the vertical SYNC signal as reference.

Servo is applied so that the vertical SYNC signal is positioned to the bottom of the video track to be recorded on the tape, and so that the picture switching point during playback occupies a fixed position at the bottom of TV screen.

In the playback mode, the drum speed is set at 25 rpm/sec for PAL/SECAM and 30 rpm/sec in the case of NTSC. The drive signal is obtained by dividing 4.43 MHz (PAL/SECAM) (or 3.58 MHz in the case of NTSC system) using the local oscillator circuit of the APC circuit as a reference.

Since a DC motor is used for the drum motor, the servo circuit requires a phase control circuit and a speed control circuit. Accordingly, IC AN6350 provided with built-in phase control and speed control circuits is employed.

3-3-1 PHASE CONTROL CIRCUIT

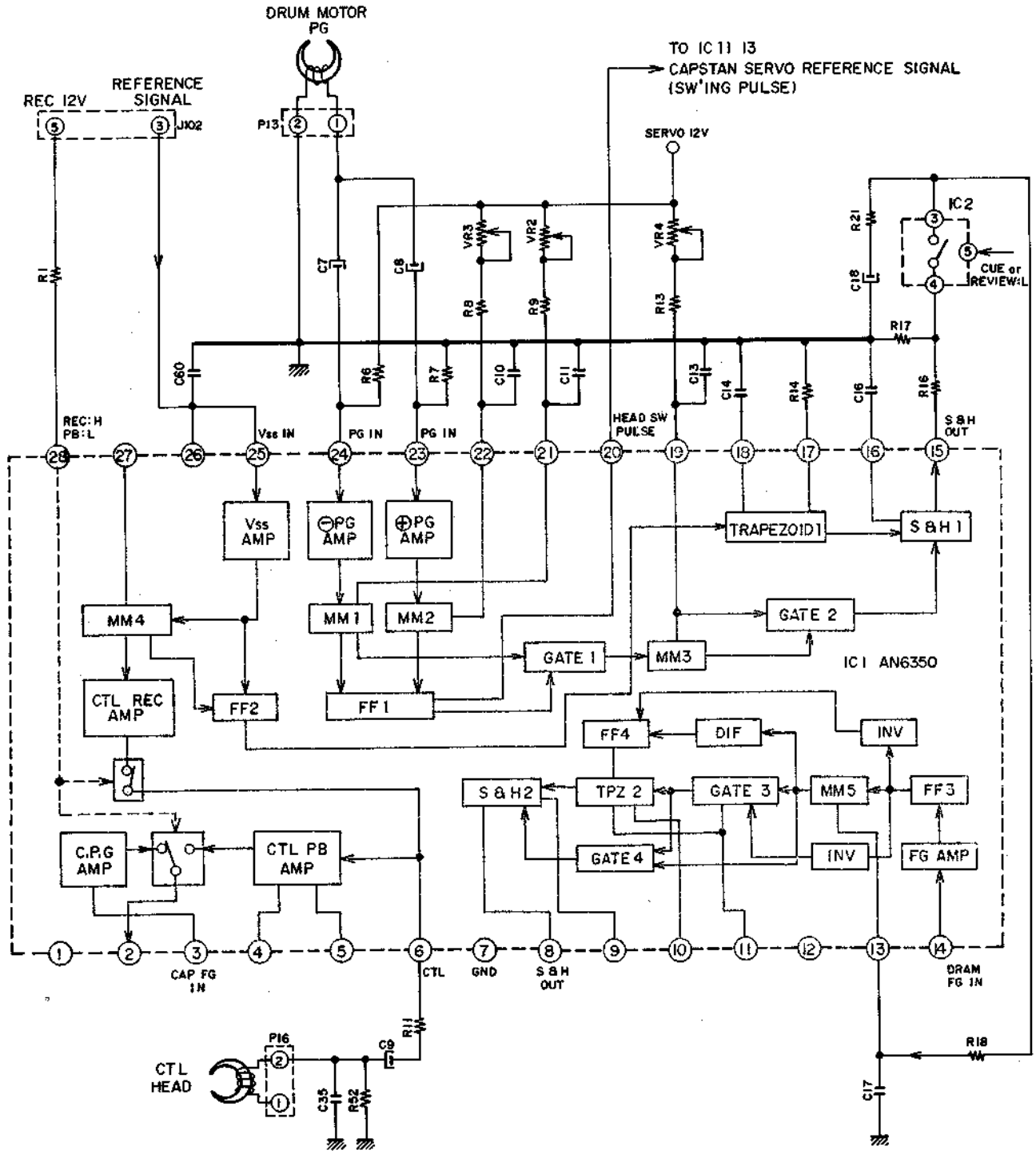


Fig. 7-48 Drum servo phase control circuit

In the recording mode, the reference signal used for the servo differs according to whether or not an input video signal is present.
When the input video signal is present, the vertical SYNC signal resulting from SYNC separation of the input video signal by the SYNC separation circuit (SYNC SEP), becomes the servo reference signal.
When the input video signal is not present, 50.0002 Hz (PAL/SECAM) or 59.9468 Hz (NTSC) is used as the reference signal.
50.0002 Hz is obtained by dividing down the 4.433618 MHz oscillation of the APC local oscillator circuit by a factor of 88672.
59.9468 Hz is obtained by dividing down the 3.57954 MHz oscillation by a factor of 59712 in the case of NTSC.
The reference signal fed to IC1 (AN6350) pins ㉕ and ㉖ is amplified by the VSS (Vertical SYNC signal) AMP, and is then fed to Mono-Multi 4 and flip-flop 2. The delay time of Mono-Multi 4 is determined by C3 and R2 connected to the control terminal (pin ㉗).
The output of this Mono-Multi 4 is amplified by the CTL REC AMP. The amplified CTL signal is output to pin ⑥ through the control REC/PB switch, and supplied to the CTL head.
The control REC/PB switch is transferred by REC 12V to be supplied to pin ㉘.
On the other hand, the reference signal fed to flip-flop 2 is divided by 2 by flip-flop 2 (25 Hz for PAL/SECAM system, 30 Hz for NTSC system), and fed to TRAPEZOID, where it triggers the TRAPEZOID at the leading edge. A trapezoidal wave is formed at TRAPEZOID. The slope time of the trapezoidal wave is determined by C14 connected to pin ⑱, while the height of the trapezoidal wave is determined by R14 connected to pin ⑰.
This trapezoidal wave is supplied to the S & H 1 circuit as a reference signal.

Now, the comparison signal circuit will be described.
The PG pulse from the drum pick-up head is amplified at each amplifier + PG AMP and –PG AMP, which have positive and negative clamp effects respectively, and is picked up as alternating pulse trains of positive direction negative direction pulses. The alternating pulse trains are fed to the trigger Schmitt circuit, which separates the positive and negative alternating pulses. The separated pulse signals is fed to the switching point adjustment Mono-Multi circuit (MM1, MM2), which delays each signal.
The delay time of this Mono-Multi is determined by the capacitor and resistor (including the switching point volume control) connected to control terminal pins ㉑ and ㉒.
MM1 and MM2 are designed so as to discharge at constant current. Each signal delayed by MM1 (MM2) triggers flip-flop 1 (FF1), and generates the switching pulse. The MM1 output pulse is fed to the GATE 1 circuit, and the trigger pulse is generated.
This pulse is fed to MM3 which follows. The delay time of MM3 is determined by VR4, R13, and C13 connected to the control terminal (pin ⑲). MM3 output and the pulse of control terminal (pin ⑲) are fed to GATE 2, and the sampling pulse is generated.
S & H 1 circuit is ON during the positive period of this pulse, and C16 is charged with the voltage of trapezoidal wave during this time. The S & H output voltage connected output to IC1 pin ⑮ is fed to the speed control circuit via the analog switch (IC2). The drum motor is phase-controlled by this voltage.

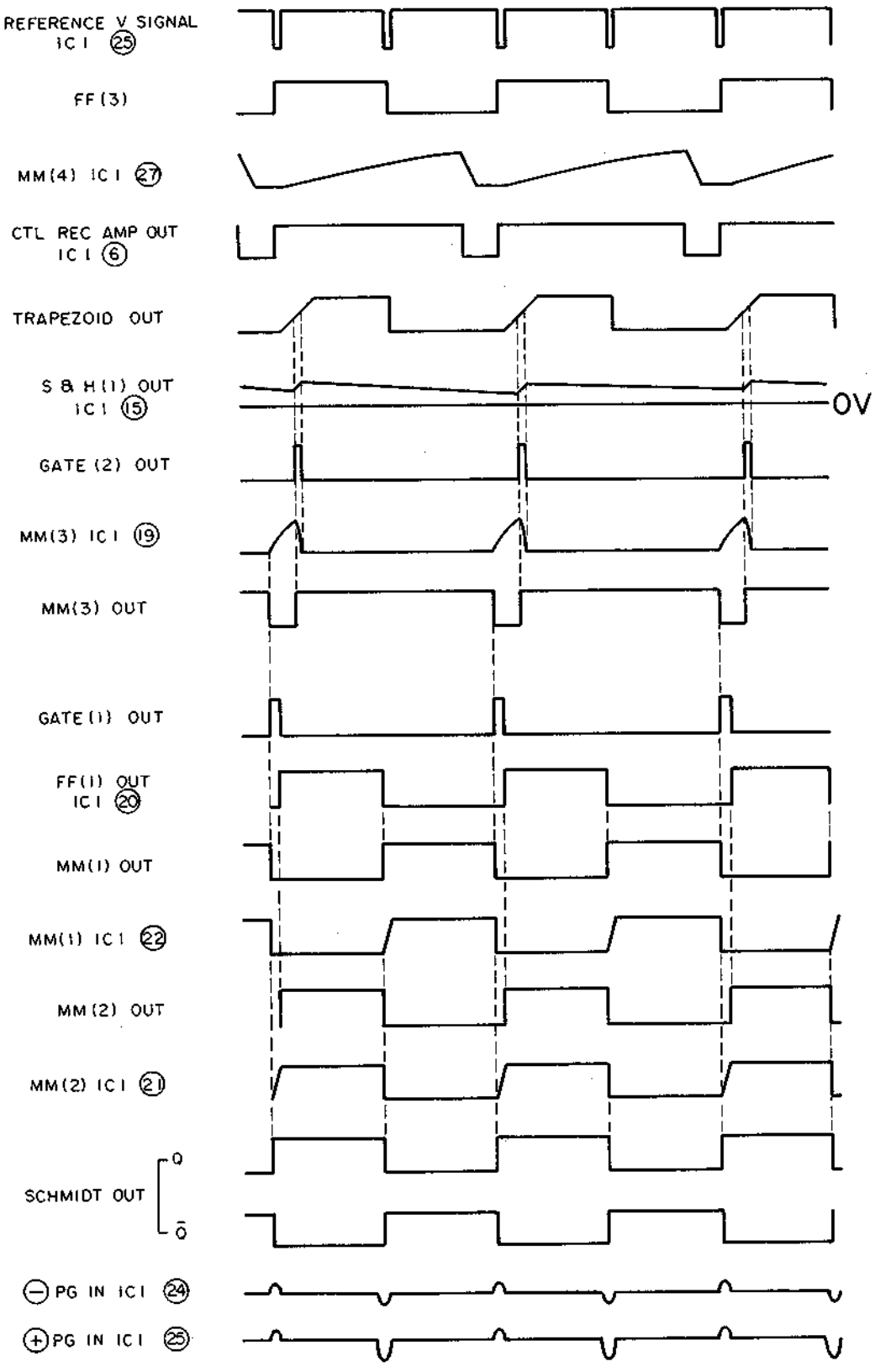


Fig. 7-49 Timing chart of drum phase control system

3-3-2 SPEED CONTROL

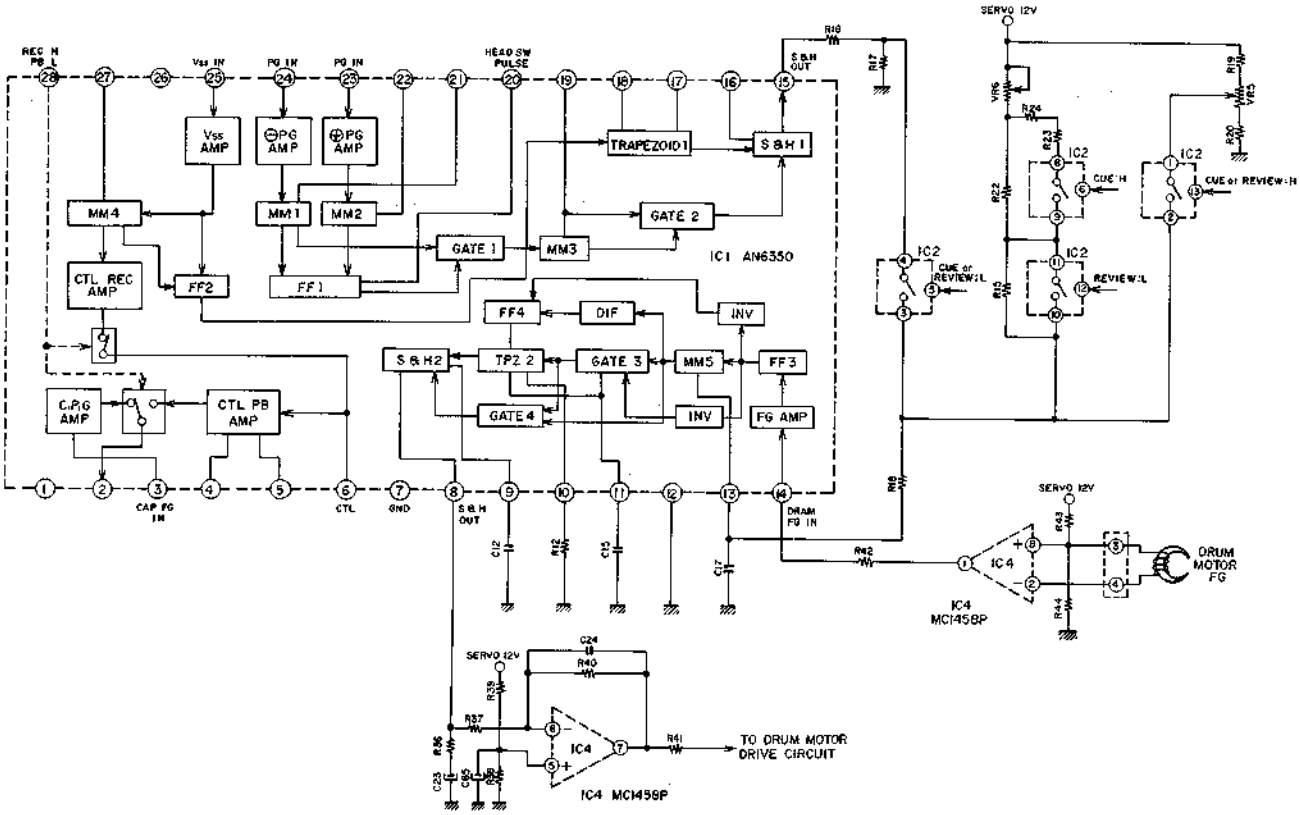


Fig. 7-50 Drum Motor Speed Control Circuit

The drum motor FG frequency is 625 Hz (NTSC: 750 Hz). The drum motor FG signal is shaped by the FG AMP (IC4 1/2), and is fed to IC1 pin (14).

The FG signal fed to IC1 pin (14) is amplified by the FG AMP, and divided by 2 at the next flip-flop, XFF3.

Mono-Multi 5 is triggered at the trailing edge of the FF3 output pulse, and the delay time is determined by C17 and R22 connected to the control terminal pin (13) and by the output voltage from the phase control circuit.

If the output voltage of the phase control circuit is constant, the delay time of MM5 is constant.

The output of this MM5 and the output of FF3 inverted at the inverter, and fed to GATE 3. Since the delay time of MM5 is constant, the output signal of GATE 3 has a pulse width corresponding to the speed error. GATE 3 output pulse is fed to TRAPEZOID 2, and the rise time of the trapezoidal wave is controlled there. That is, the peak value of the trapezoidal wave changes according to the GATE 3 output pulse width.

The wider the pulse width, the longer the charging time becomes, and as a result the peak value of the trapezoidal wave becomes high. Conversely, the narrower the pulse width, the lower the peak value of the trapezoidal wave becomes.

TRAPEZOID 2 is triggered at the trailing edge of FF4 output pulse.

The output of TRAPEZOID 2 is fed to S & H 2.

The sampling pulse is an output pulse of GATE 4 which is generated from the MM5 output pulse and the GATE 3 output pulse.

The output of S & H 2 is inverted at DC AMP (IC4), and fed to the next drum motor drive circuit.

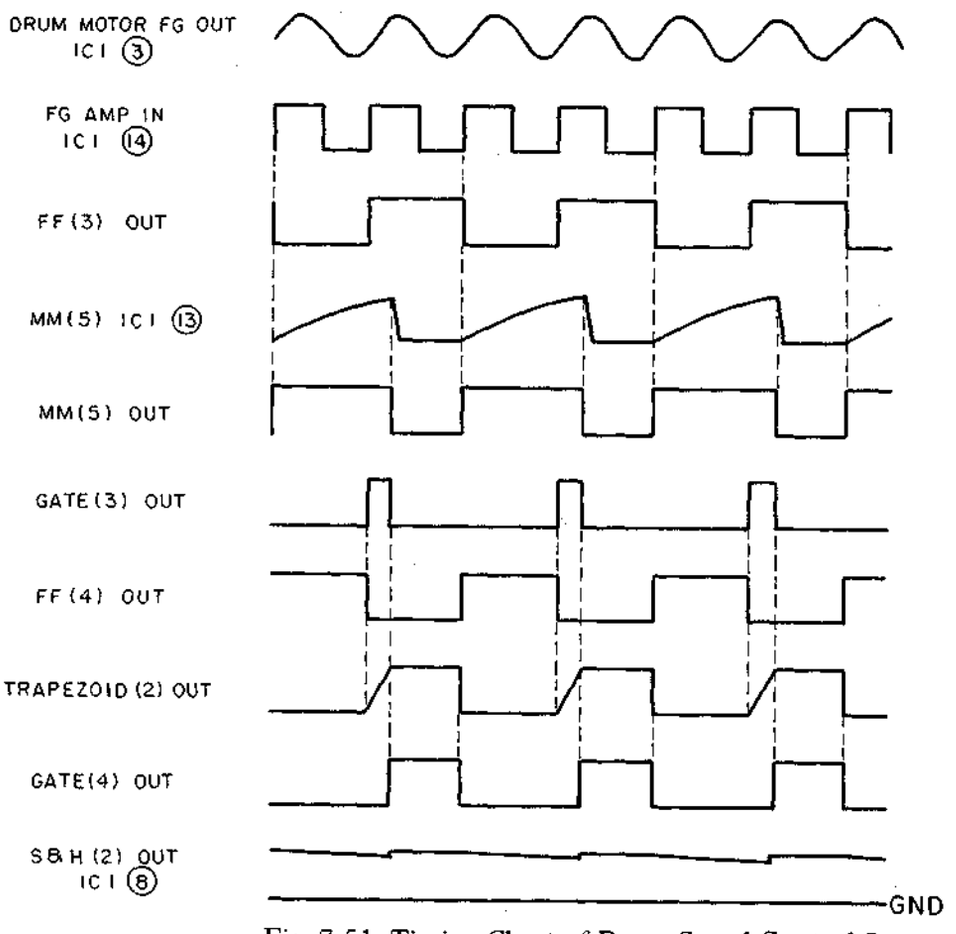


Fig. 7-51 Timing Chart of Drum Speed Control System

3-3-3 DRUM MOTOR SPEED ADJUSTMENT CIRCUIT

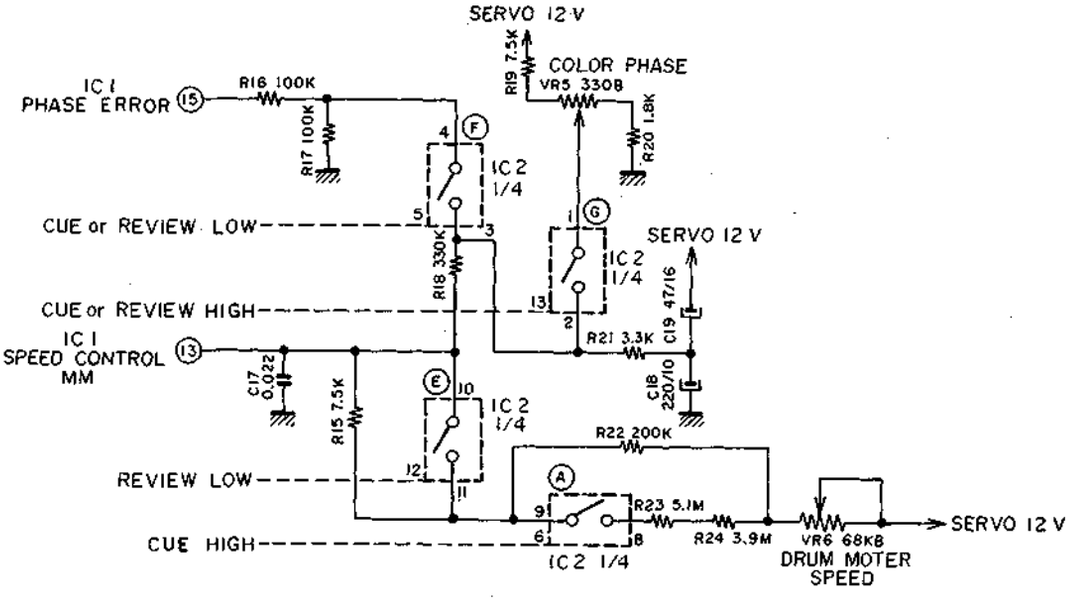


Fig. 7-52 Drum Motor Speed Adjustment Circuit (PAL/SECAM MODE)

During CUE or REVIEW modes, the tape is driven or reversed at a high speed. At this time, the relative speed between the video head and the tape changes, and the PB video signal horizontal frequency changes,which means that the TV horizontal synchronization becomes abnormal. Therefore the drum speed is changed to compensate for this.

1) PAL (SECAM) mode (Refer to Fig. 7-52)

ⓐ Normal mode

In normal mode, the analog switches F and E becomes ON, and the time constant of MM5 becomes C17 (0.022 μF) and R22 (200 kohms) + VR6 (68 kohms) = 268 kohms. This determines the speed control performance. The phase Error signal is connected via the analog switch F, and the speed control is performed by varying the time constant of MM5, which is the basis of the speed control.

ⓑ CUE mode

In the CUE mode, analog switches G, E and A are ON, and F is OFF.

The time constant of MM5, which is the basis of the speed control, is C17 (0.022 μF) and

$$\frac{R22\times(R23+R24)}{R22+(R23+R24)} + VR6$$

$$= \frac{200\ \text{kohms} \times 9\ \text{Mohms}}{200\ \text{kohms} + 9\ \text{Mohms}} = 195.65\ \text{kohms}$$

This is 2.17% smaller than that during the Normal mode. That is, in the CUE mode, the drum motor speed is increased by 2.17% compared with the Normal mode, thus equating the horizontal frequency of PB video signal to the stnadard horizontal frequency.

When the drum motor speed varies due to, say, tolerances of components, a TV picture colour offset phenomenon occurs. VR5 is a colour phase adjustment control potentiometer.

ⓒ REVIEW mode

In the REVIEW mode, the analog switch G is ON. The time constant of MM5 providing the basis for the speed control is C17 (0.0022 μF) and R15 (7.5 kohms) + R22 (200 kohms) + VR6 (68 kohms) = 275.5 kohms. This is 3.75% larger than in the normal mode. That is, in the REVIEW mode, the drum motor speed is reduced by 3.75% compared with the normal mode, thereby making the horizontal frequency of PB video signal equal to the reference horizontal frequency.

2) NTSC mode

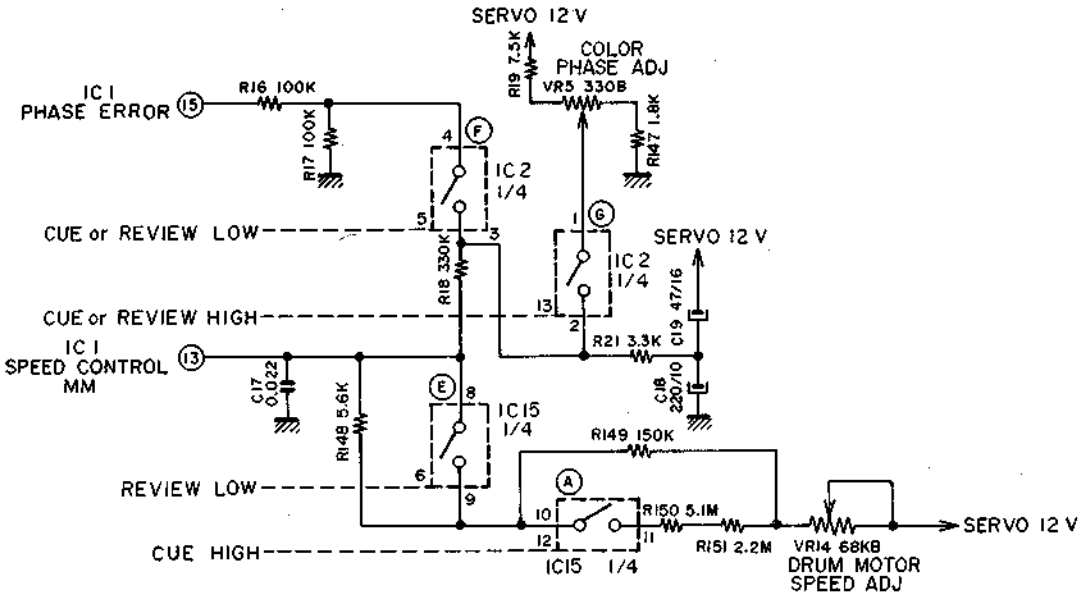


Fig. 7-53 Drum Motor Speed Adjustment Circuit (NTSC mode)

ⓐ Normal mode

In the Normal mode, analog switches F and E are ON. The time constant of MM5 providing basis for the speed control is C17 (0.002 μF) and R149 (150 kohms) + VR 14 (68 kohms) = 218 kohms.

The phase error signal is connected via the analog switch F, and the speed control is performed by varying the MM5 time constant which is the basis of the speed control.

ⓑ CUE mode

In the CUE mode, analog switches G, E , and A are ON. The MM5 time constant providing the basis for the speed control is C17 (0.002 μF) and

$$\frac{R149 \times (R150 + R151)}{R149 + (R150 + R151)} + VR14$$

$$= \frac{150 \text{ kohms} \times 7.7 \text{ Mohms}}{150 \text{ kohms} + 7.7 \text{ Mohms}} + 68 \text{ kohms} = 215 \text{ kohms}$$

In the CUE mode, therefore the drum motor speed is increased by 2.013% compared with the normal mode so as to make the horizontal frequency of the PB video signal equal to the reference horizontal frequency.

ⓒ REVIEW mode

In the REVIEW mode, analog switch G is ON. The MM5 time constant providing the basis for the speed control is

R148 (5.6 kohms) + R149 (150 kohms) + VR14 (68 kohms) = 223.6 kohms

In the REVIEW mode, therefore the drum motor speed is reduced by 3.733% compared with the normal mode, thus making the horizontal frequency of the PB video signal equal to the reference horizontal frequency.

3-3-4 DRUM MOTOR PHASE, SERVO CANCELLATION CIRCUIT

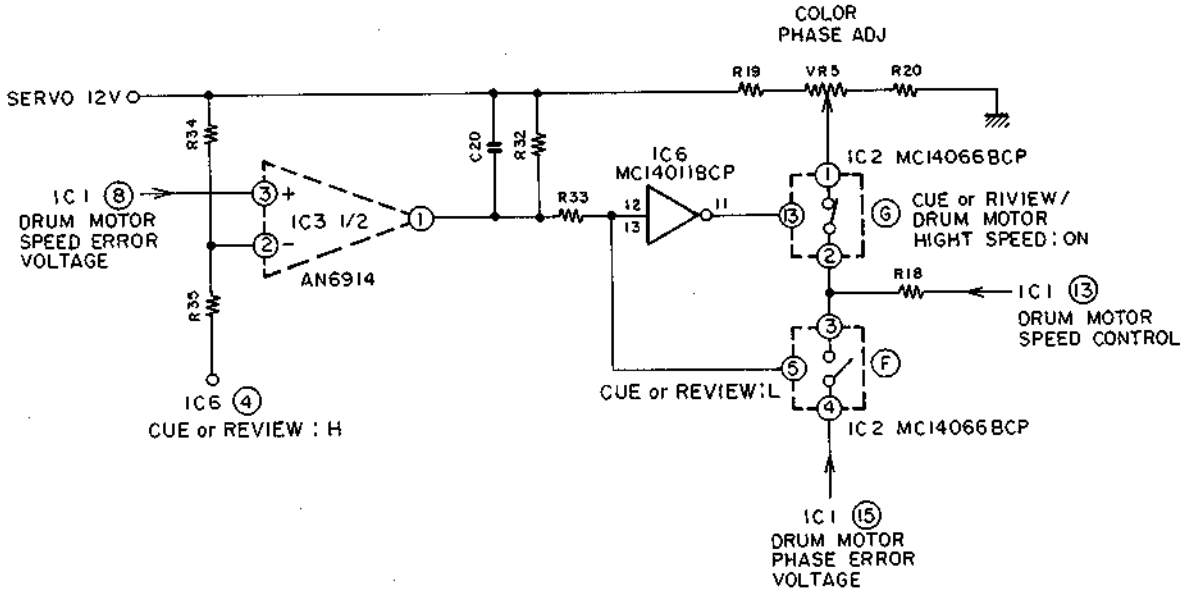


Fig. 7-54 Drum motor phase, servo cancellation circuit

1) CUE or REVIEW mode

On VS-2, the Drum Motor phase servo is cancelled at CUE or REVIEW MODE; i.e., only the Drum Motor speed servo is in use. Thus, by turning off IC2 (MC 14066BCP) Analog Switch Ⓕ , or the point where the phase and speed systems are connected, it is possible to prevent an error voltage in the phase system interfering with the speed system. Also, the Analog Switch Ⓖ circuit is incorporated in the form of color phase adjustment to compensate for a speed error at Quick Finder Mode.

2) Drum motor at abnormally high speed

In addition, the phase control system may also be cancelled when the drum motor rotates at an abnormally high speed. This is done by means of a comparator (IC3, AN6914). That is, the comparator output (IC3 pin ①) goes to "L" at CUE/REVIEW MODE, and 4.8 V appears at the inverse input terminal (IC3 pin ②) at "Normal" mode. When the motor revolution becomes so high that the S/H OUT of IC1 (AN6350 pin ⑧) falls below 4.8 V, the comparator goes to "L", and the phase system is cancelled, thereby eliminating interference to the phase system and preventing "hunting" of the drum motor.

Note: Normal Mode ~ Recording Mode or Normal Playback Mode.

3-4 QUASI-VERTICAL SYNCHRONIZATION PULSE GENERATOR CIRCUIT

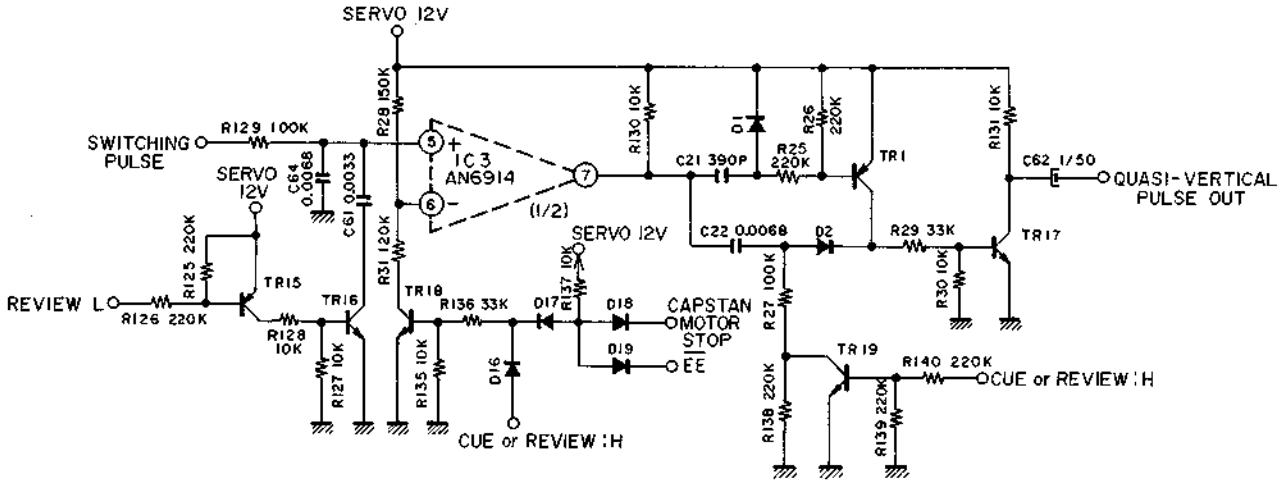


Fig. 7-55 Quasi-Vertical Synchronization Pulse Generator Circuit

During the trick-play of CUE, REVIEW, PLAY, PAUSE, etc. it sometimes occurs that a noise bar occurs during the vertical blanking period, or that the TV picture sways vertically or rolls.

To prevent such trouble, a quasi-vertical synchronization pulse is generated during trick-play modes, and it is added to the PB signal (squelch circuit of video circuit) to achieve TV synchronization.

3-4-1 CUE MODE

When CUE mode CUE/REVIEW (H) terminal goes to HIGH, TR18 and TR19 are turned on while R31 and R27 are grounded.

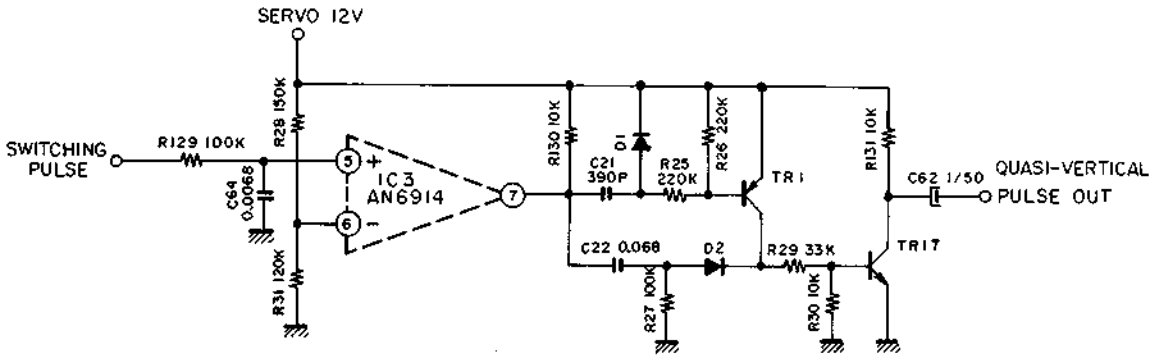


Fig. 7-56 Quasi-Vertical Synchronization Pulse Generator Circuit (CUE mode)

The quasi V-pulse is delayed 480 μs from Switching Pulse CH-1 and CH-2 with the pulse width being 300 μsec.

ⓐ The delay is determined by the time constant of R129 and C64 and the reference potential which is determined by the comparator's inverse inputs R28 and R31. (See Fig. 7-57 ②.)

ⓑ The pulse width is determined by the threshold potential, as determined by R29 and R30, and by the time constant (CH-2, C21, R25 and R26 or CH-1, C22 and R27) that differentiates delayed Switching Pulse. (See Fig. 7-57 ④, ⑥.)

ⓒ C62 (1/50) is employed to prevent disturbance of the picture caused by the video power source taken into the servo due to timing lag between servo power source (SERVO 12 V) OFF and video power source AL 12 V.

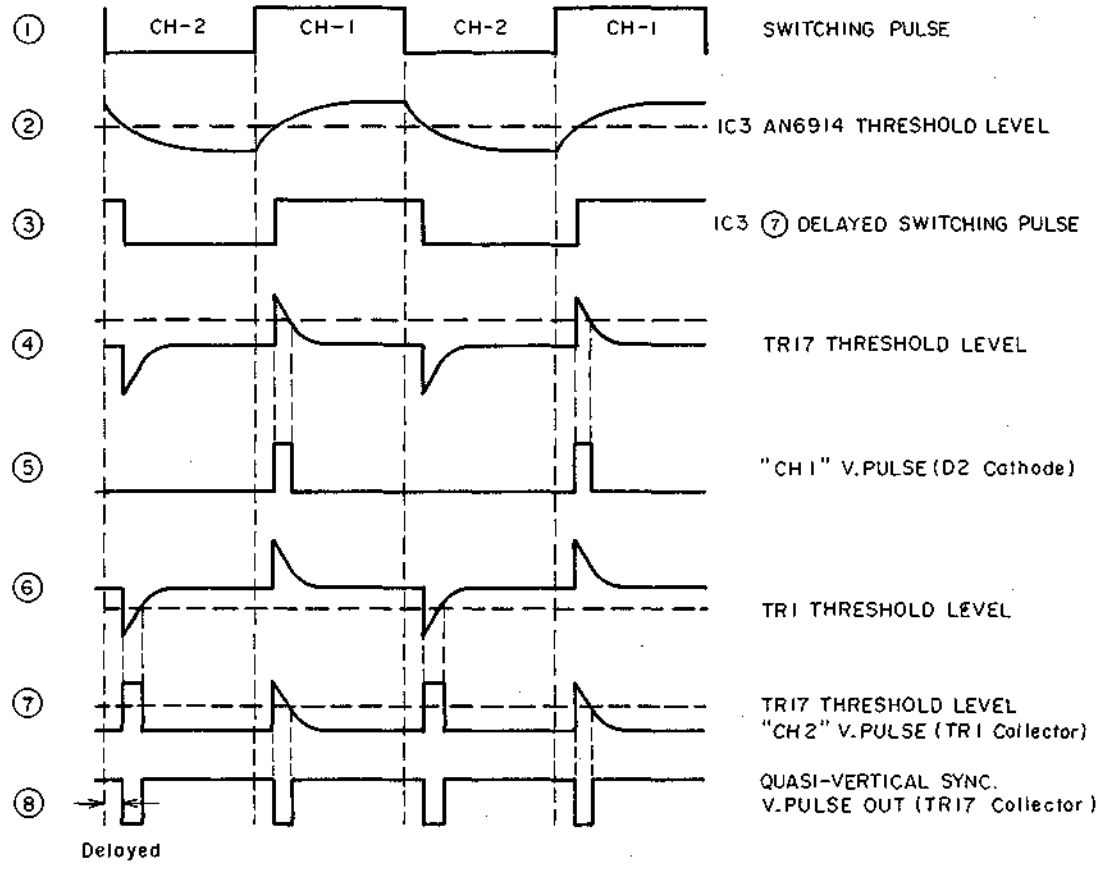


Fig. 7-57 Waveform at Each Point

3-4-2 REVIEW MODE

With the REVIEW mode, when TR16 is turned on, C61 is grounded (See Fig. 7-55).

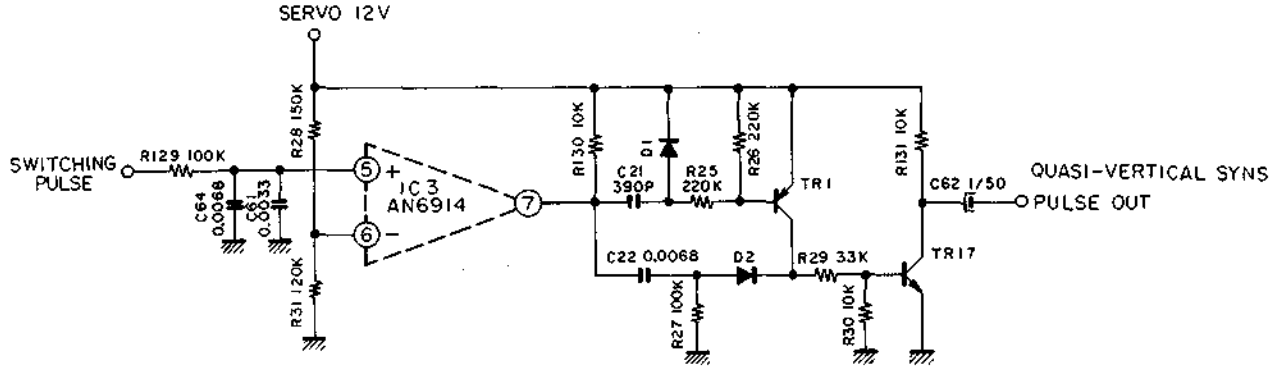


Fig. 7-58 Quasi-Vertical Synchronization Pulse Generator

As a result, the Switching Pulse delay is increased to 720 μs.

3-4-3 PLAYBACK PAUSE (SIMPLIFIED STILL) MODE

D18, D19 and R137 form an AND circuit. When Capstan Motor Stop and $\overline{EE}$ go to "high", TR18 is turned on and R31 grounded. Further when CUE/REVIEW goes to "low", TR19 is turned off and R27 + R138 grounded. (See Fig. 7-55).

Thus, the time constant of C22 and R27 + R138 causes the width of Quasi-Vertical Synchronization Pulse on Switching Pulse CH-1 to become 400 μs. (The pulse width on CH-2 remains unchanged, 300 μs).

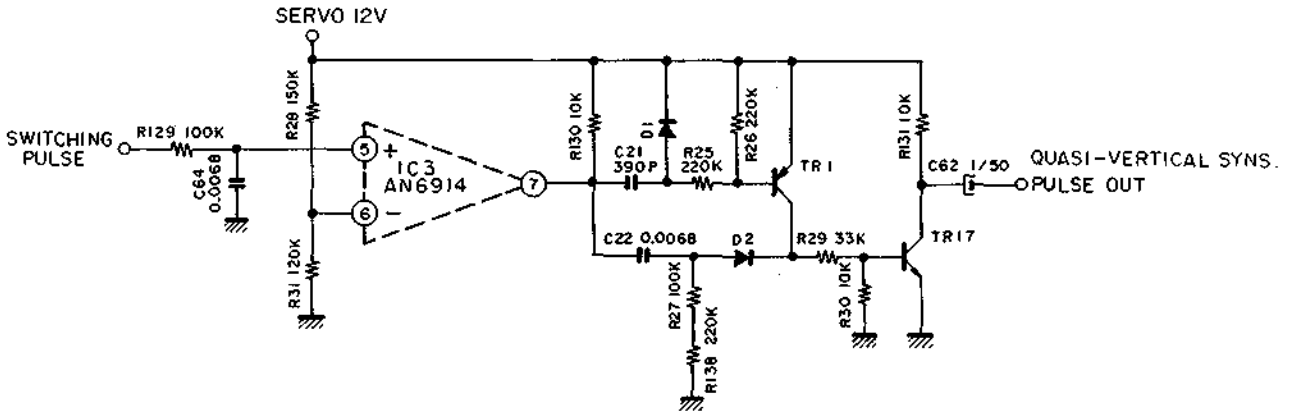


Fig. 7-59 Quasi-Vertical Synchronization Pulse Generator Circuit (PB PAUSE mode)

In each mode, the Quasi-Vertical Synchronization Pulse should appear as shown in Fig. 7-60.

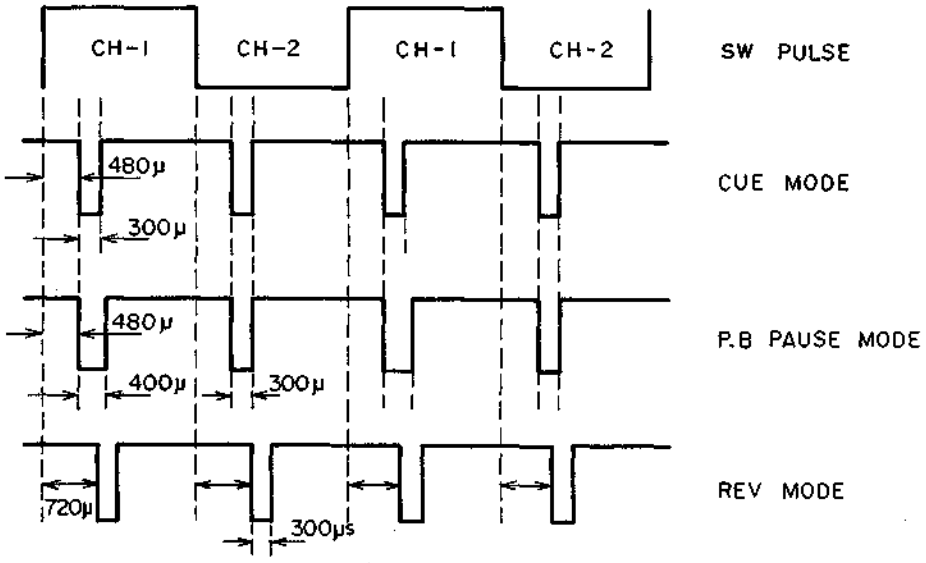


Fig. 7-60 Quasi-Vertical Synchronization Pulse each mode

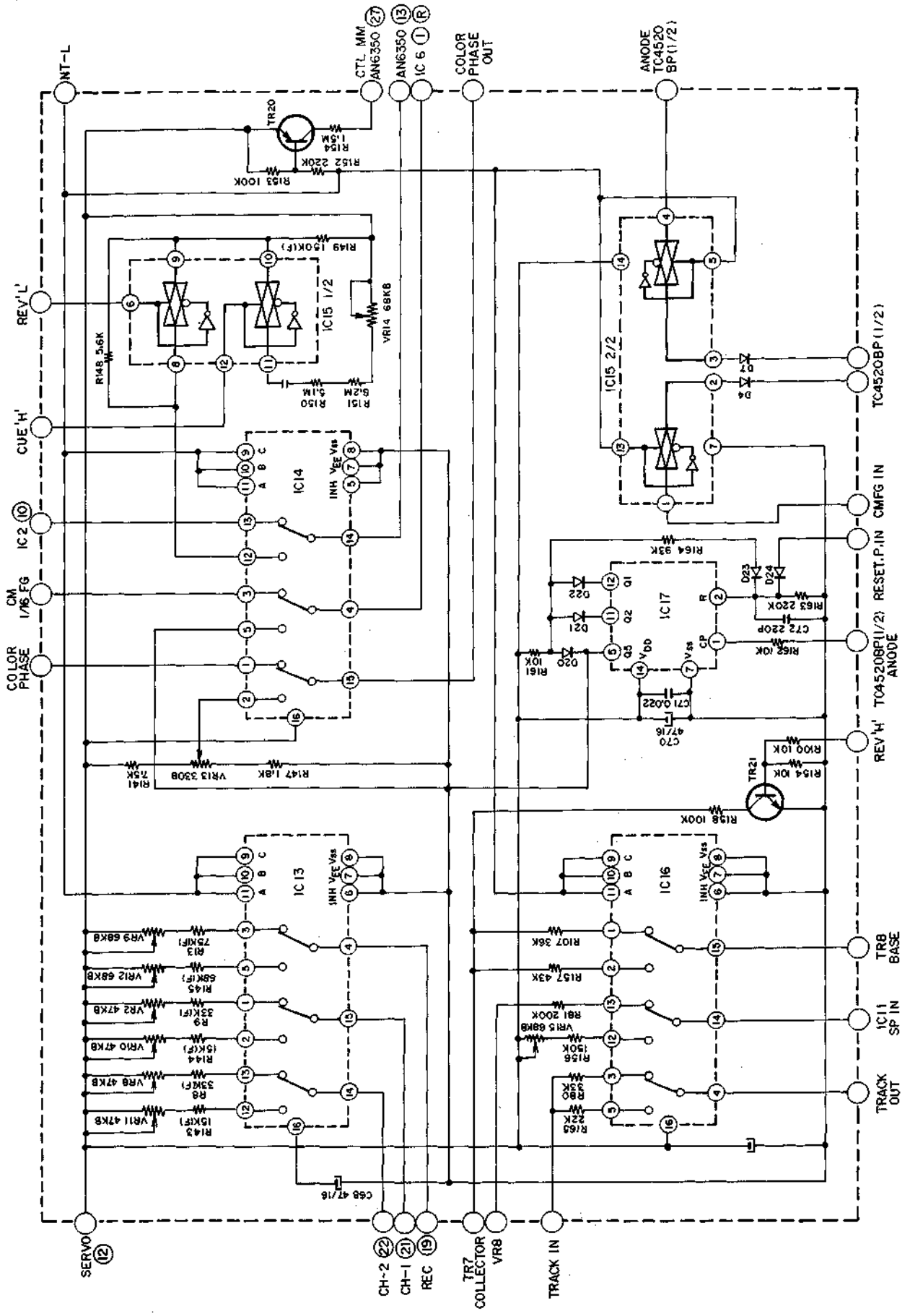


Fig. 7-61 PAL (SECAM)/NTSC Switching Circuit

3-6 AUTO DISCRIMINATOR CIRCUIT

3-6-1 MICROCOMPUTER CONFIGURATION

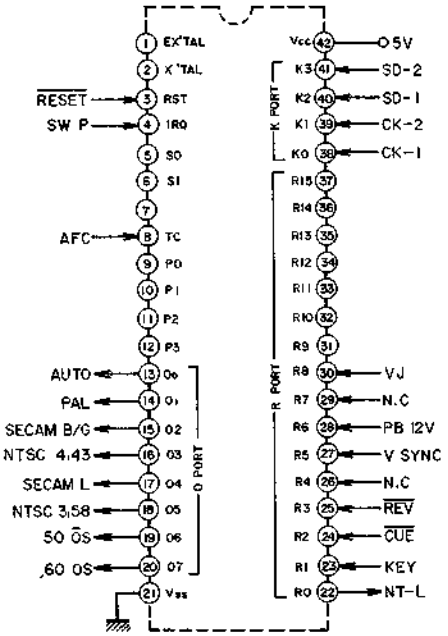


Fig. 7-62 MB8841-1041J

PORT	PIN No.	I/O	ACTIVE	PORT NAME	COMMENT
O_0	13	OUT	L	AUTO	AUTO LED ON
O_1	14	OUT	L	PAL	PAL LED ON, control signal to video circuit
O_2	15	OUT	L	SECAM B/G	SECAM B/G LED ON, control signal to video circuit
O_3	16	OUT	L	NTSC 4.43	NTSC 4.43 LED ON, control signal to video circuit
O_4	17	OUT	L	SECAM L	SECAM L LED ON, control signal to video circuit
O_5	18	OUT	L	NTSC 3.58	NTSC 3.58 LED ON, control signal to video circuit
O_6	19	OUT	L	50 OS	50 Hz control
O_7	20	OUT	L	60 OS	60 Hz control
R_0	22	OUT	L/H	NT-L	Control signal to servo circuit
R_1	23	IN	L/H	KEY	Signal supplied by manual operation of touch buttons
R_2	24	IN		$\overline{\text{CUE}}$	"L": CUE
R_3	25	IN		$\overline{\text{REV}}$	"L": REVIEW
R_4	26	IN		N·C	NOTE 1
R_5	27	IN		V SYNC	V. SYNC. SIGNAL
R_6	28	IN		PB 12V	H: PB MODE L: E-E MODE
R_7	29	IN		N·C	*1
R_8	30	IN		VJ	VIDEO SIGNAL
TC	8	IN		AFC	AFC (H. SYNC.) PULSE
IRQ	4	IN		SW P	Detection of Switching Pulse trailing edge
K_0	38	IN		CK-1	COLOR KILLER-1 H: PAL or NTSC 4.43MHz
K_1	39	IN		CK-2	COLOR KILLER-2 H: NTSC 3.58 MHz
K_2	40	IN		SD-1	SECAM DETECTOR-1 H: SECAM B/G
K_3	41	IN		SD-2	SECAM DETECTOR-2 H: SECAM L

Fig. 7-63 Description of I/O Port

*1: The discrimination level in the CUE/REVIEW mode is changed by bringing this port to 'L' or 'H'.

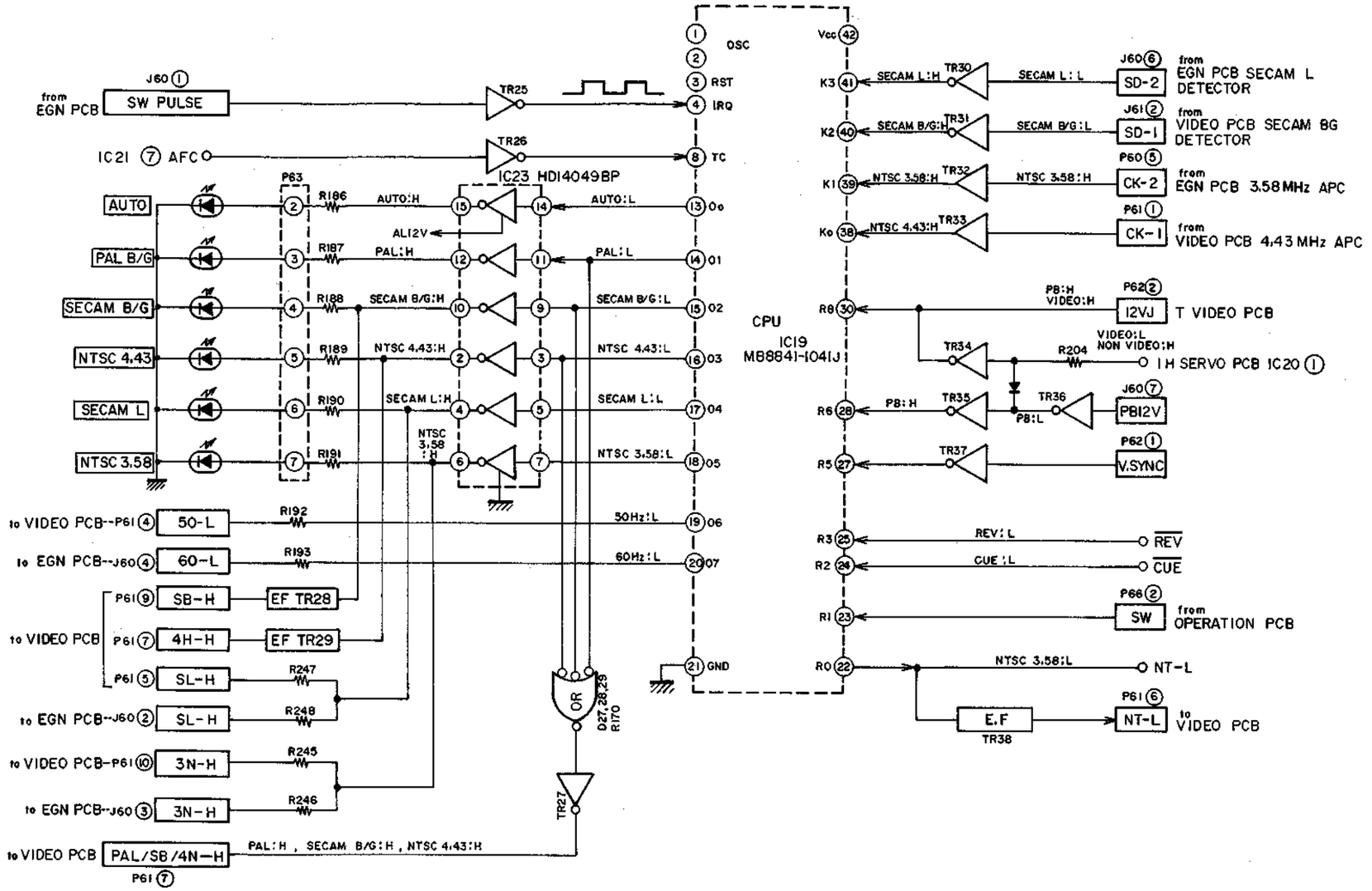


Fig. 7-64 Auto Discriminator Block Diagram

1) Outline

When FUNCTION ON is operated, power is supplied to the microcomputer, thereby causing the AUTO LED to light regardless of whether or not the video signal is present.

Then, the microcomputer judges by means of PB 12V that the mode is PB when the level is high, and EE when the level is low. In the PB mode, detection of 50 Hz or 60 Hz is made automatically by counting AFC (H SYNC) pulses occuring between one trailing edge and the next trailing edge of the Switching Pulse.

In the PB mode, fixed setting to that mode may be made by manual operation.

In the EE mode, detection of 50 Hz or 60 Hz is made automatically by counting AFC (H SYNC) pulses occuring between one leading edge and the next leading edge of V SYNC (R5 port).

In the EE mode, fixed setting to that mode may be made by manual operation.

2) Change from EE mode to PB mode

When changing from EE to PB mode, the loading time (2.6 seconds) is controlled by the internal timer via the microcomputer. This is the same as the loading time by the power SYS CON (System control).

3-6-3 AUTO DISCRIMINATION

The auto discrimination method in the EE mode differs from that in the PB mode.

1) EE mode

In the EE mode, AFC (H SYNC) pulses between the leading edge and the next leading edge of V SYNC are counted, and the mode is judged to be 50 Hz when the number of pulsis counted is more than the discrimination level of 288 and 60 Hz when the count is less than 288.

For the 50 Hz mode, 50 OS (06 port) is brought to LOW and 60 OS (07 port) to HIGH.

Then, NT-L (R0 port) is brought to HIGH, the discriminator acts on the input signal of K port (CK-1, SD-1, or SD-2), and the mode is determined .

For the 60 Hz mode, 50 OS (06 port) is brought to HIGH, and 60 OS (07 port) to LOW.

Then, NT-L (R0 port) is brought to LOW, the discriminator acts on the input signal (CK-1 or CK-2) of K port and the mode is determined.

	50 Hz Mode	60 Hz Mode
1	SECAM B/G	NTSC 4.43
2	SECAM L	NTSC 3.58
3	PAL B/G	60 Hz B/W
4	50 Hz B/W	

Fig. 7-65 Discrimination priority

When two or more signal enter K port, the one of highest priority is favoured.

50-L	60-L	NT-L	SD-1	SD-2	CK-1
L	H	H	H	L	L
L	H	H	L	H	L
L	H	H	L	L	H
L	H	H	L	L	L

SB-H	4N-H	3N-H	SL-H	PAL/SB/4N-H	MODE
H	L	L	L	L	SECAM B/G
L	L	L	H	L	SECAM L
L	L	L	L	H	PAL B/G
L	L	L	L	L	50 Hz B/W

Fig. 7-66 Mode discrimination in 50 Hz mode

50-L	60-L	NT-L	CK-1	CK-2
H	L	L	H	L
H	L	L	L	H
H	L	L	L	L

SB-H	4N-H	3N-H	SL-H	PAL/SB/4N-H	MODE
L	H	L	L	H	NTSC 4.43
L	L	H	L	L	NTSC 3.58
L	L	L	L	L	60 Hz B/W

Fig. 7-67 Mode discrimination in 60 Hz mode

2) Playback mode

In the playback mode, the AFC (H SYNC) pulses occuring during the period of the Switching pulse from one trailing edge to the next trailing edge), are counted. When the number of pulses is equal to or more than the discrimination level of 576, the mode is judged to be 50 Hz. When the number of pulses is less than 576, the mode is judged to be 60 Hz. The rest is the same as the EE mode.

3) CUE or REVIEW mode

CUE or REVIEW mode is the same as the PB mode except that the discrimination levels are different.

4. MECHANISM DRIVE OPERATION

4-1 MECHANISM DRIVE OPERATION

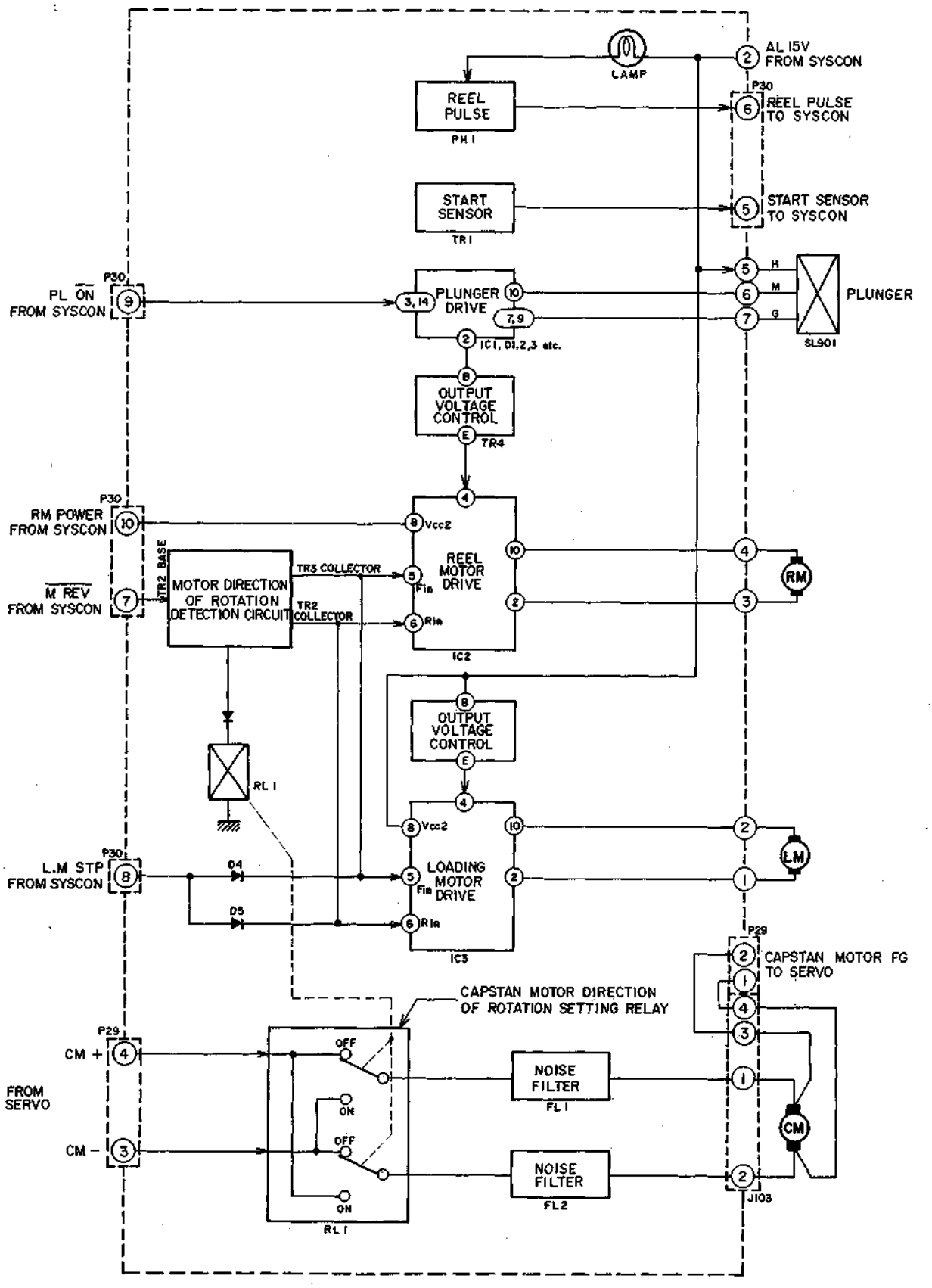


Fig. 7-68 Block Diagram of Mechanism Drive Circuit

4-1-1 GENERAL

Fig. 7-68 is a block diagram of the mechanism drive circuit

1) Reel pulse is generated at PH-1 (GP411), and sent to the SYS CON (System control PCB).

2) TR-1 (PN2025) is a start sensor, the output of which is sent to SYS CON.

3) The plunger drive circuit consists of IC-1 (M54532P), D1, D2, and D3, and the plunger is driven by PL $\overline{ON}$ which is an input to IC-1.

4) TR2 and TR3 are transistors for determining the direction of motor rotation. These transistors determine the direction of rotation (normal or reverse) of the reel motor, loading motor, and capstan motor.

5) The reel motor drive circuit consists of IC3 (BA6109) and TR4. IC2 receives RM POWER and $\overline{MRVS}$ inputs and drives the reel motor.

6) The loading motor drive circuit consists of IC3 (BA 6109) and TR5. IC3 drives the loading motor under the control of LM STP, MRVS, and AL-15V inputs.

7) CM (+) and CM(–) from the servo circuit pass through the relay contacts of RL1, and to the noise filters (FL1, FL2) on the MECHA Drive P.C Board and drive the capstan motor. In the REVIEW mode, RL is switched ON, and the capstan motor runs in the reverse direction.

4-1-2 REEL PULSE GENERATOR CIRCUIT

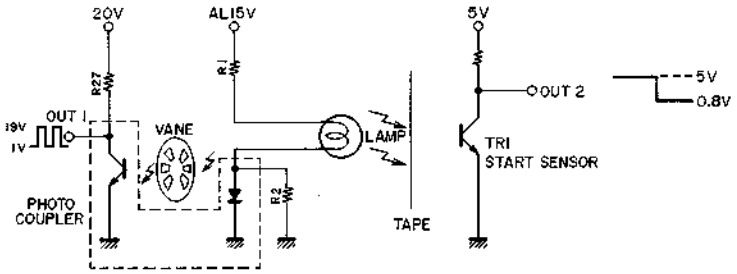


Fig. 7-69 Reel Pulse Generator and Start Sensor

As shown in Fig. 7-69, vanes in the center are driven by the take-up reel base. When light passes through the vane, the impedance of the photo transistor falls. When the light is cut off by through the vane, the impedance of the photo transistor rises. When the take-up reel base is turning, the output waveform as shown in the figure is detected at the OUT1 terminal, and is fed to the system control PCB.

4-1-3 START SENSOR

As shown in Fig. 7-69, the tape stops the lamp light, and the impedance of the start sensor becomes high. As the tape reaches the leader section, the lamplight is transmitted through the tape, the start sensor impedance becomes low, and a low voltage is detected at OUT 2 (Fig. 7-69), and this signal is fed to the system control PCB.

4-1-4 PLUNGER DRIVE CIRCUIT

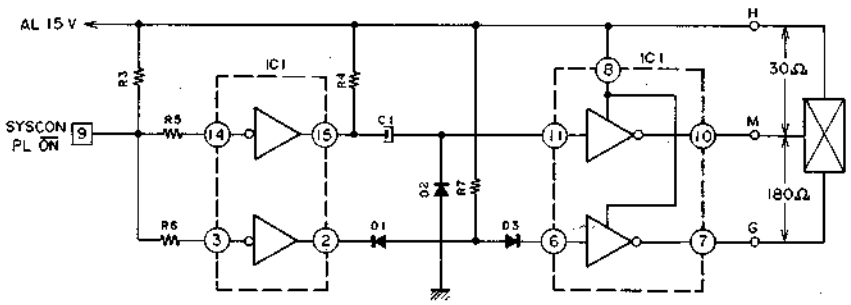


Fig. 7-70 Plunger Drive Circuit

Fig. 7-70 shows the plunger drive circuit.

When the level on the PL $\overline{ON}$ terminal is made LOW, IC1 pin ⑮ becomes HIGH, and IC1 pin ⑩ stays LOW during the time determined by the time constant of R4 and C1 . This causes a current (approx. 500 mA) to flow between H and M, and the plunger is pulled in. When C1 is fully charged, IC1 pin ⑪ becomes LOW, and IC1 pin ⑩ becomes HIGH. As the PL $\overline{ON}$ terminal becomes LOW, IC1 pin ② also becomes HIGH, making IC1 pin ⑥ HIGH and G terminal LOW. Accordingly, when PL $\overline{ON}$ becomes LOW, a current flows between H and M until C1 is charged, and the plunger is pulled in. When C1 is charged, a current (approx.72 mA) keeps flowing, to hold the plunger.

As PL $\overline{ON}$ becomes HIGH, IC1 pins ⑮ and ② become LOW. C1 is rapidly discharged through D2, and pin ⑮. Both M and G terminals become HIGH, and the plunger is released. The counter electromotive force from the relay is absorbed by the diode incorporated in IC1 (M54532P).

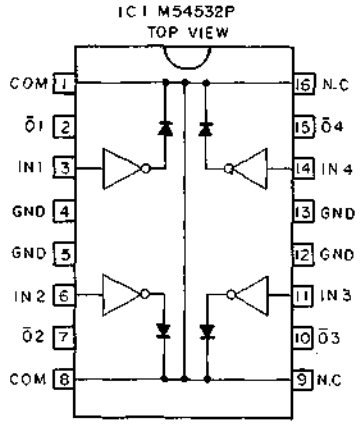


Fig. 7-71 IC1 Block Diagram

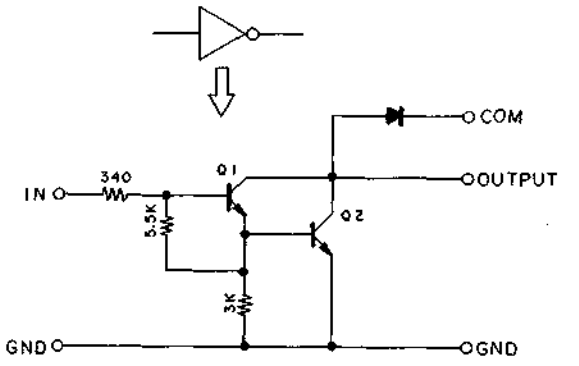


Fig. 7-72 Equivalent Circuit of Inverter

4-1-5 REEL MOTOR/LOADING MOTOR DRIVE IC (BA6109)

Fin	Rin	Vout 1	Vout 2
H	H	L	L
L	H	L	H
H	L	H	L
L	L	OPEN	OPEN

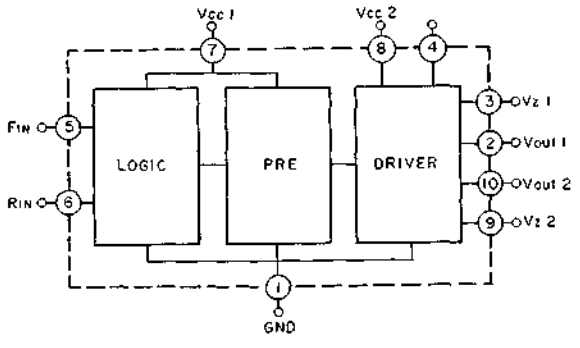


Fig. 7-73 IC BA6109 Block Diagram and Truth Table

BA6109 has three output modes of NORMAL, REVERSE, and STOP corresponding to two input logics (Fin, Rin), and it determines the direction of motor rotation. The use of a relay has become unnecessary thanks to the use of this IC.

CAUTION

When a short-circuit occurs between POWER (pin ⑦, pin ⑧) or GND (pin ①) and an output terminal (pin ②, pin ⑩), or between the output terminals (pin ②, pin ⑩), the load of the output transistor becomes almost zero ohm, and a large current above 1A will flow through the IC, destroying the IC.

4-1-6 REEL MOTOR DRIVE CIRCUIT

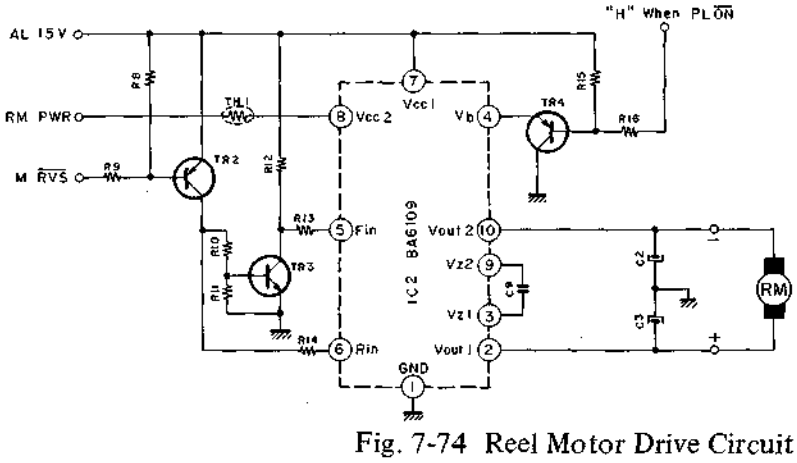


Fig. 7-74 Reel Motor Drive Circuit

Fig. 7-74 shows the reel motor drive circuit. When RM PWR is fed from the SYS-CON, NORMAL/REVERSE is determined by Fin and Rin at that time, and a current is fed to the reel motor (RM). Fin and Rin are generated by TR2 and TR3 from the M $\overline{RVS}$ information from the SYS-CON. In the mode where the reel motor does not turn rotate, the signal may be Fin or Rin.

TR4 is for controlling the output voltage of BA6109, and limits the output voltage during the period of 0.3 second from the reel motor rotation start to the time that the plunger draws about 3V. As the plunger is operated, TR4 is switched OFF, and the output is determined by RM PWR

4-1-7 LOADING MOTOR DRIVE CIRCUIT

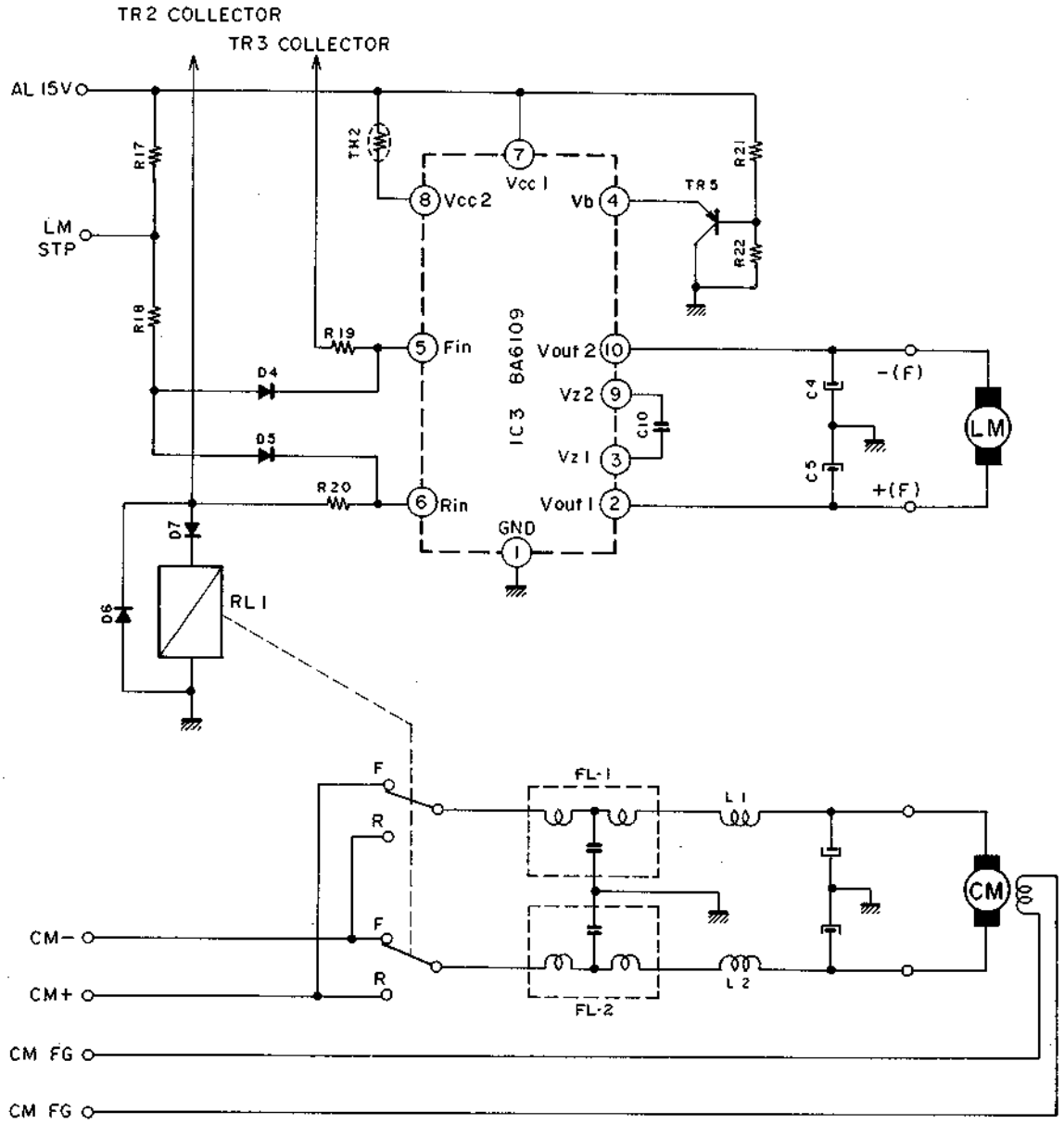


Fig. 7-75 Loading Motor Drive Circuit and Capstan Motor Control Circuit

The upper half of Fig. 7-75 is the loading motor drive circuit. The power supply is obtained from AL 15V. When LM STP from the SYS-CON is HIGH, D4 and D5 conduct, and outputs Vout 1 and Vout 2 become LOW regardless of M $\overline{\text{RVS}}$, causing the loading motor to stop rotating. When LM STP becomes LOW, D4 and D5 cease conducting, HIGH/LOW of Fin and Rin is determined by M $\overline{\text{RVS}}$, so that NORMAL/REVERSE is controlled. TR5 is for determining the output voltage, so that about 10.5V is applied to the motor.

TH1 and TH2 are posisters (Positive temperature coefficient thermistors) for preventing abnormal heating of IC, transistors, resistors, etc. in the event of a short circuit, by means of limiting the current.

4-1-8 CAPSTAN MOTOR CIRCUIT

The lower half of Fig. 7-75 is the capstan motor circuit. CM+ and CM– are supplied from the servo circuit, and connected to the capstan motor after passing through the respective relay and filter.

In the REVIEW mode, relay RL1 is ON, so that the CM+ and CM– connections are reversed, and hence the capstan motor runs in the reverse direction.

5. OPERATION CIRCUIT

5-1 OPERATION CIRCUIT COMPOSITION

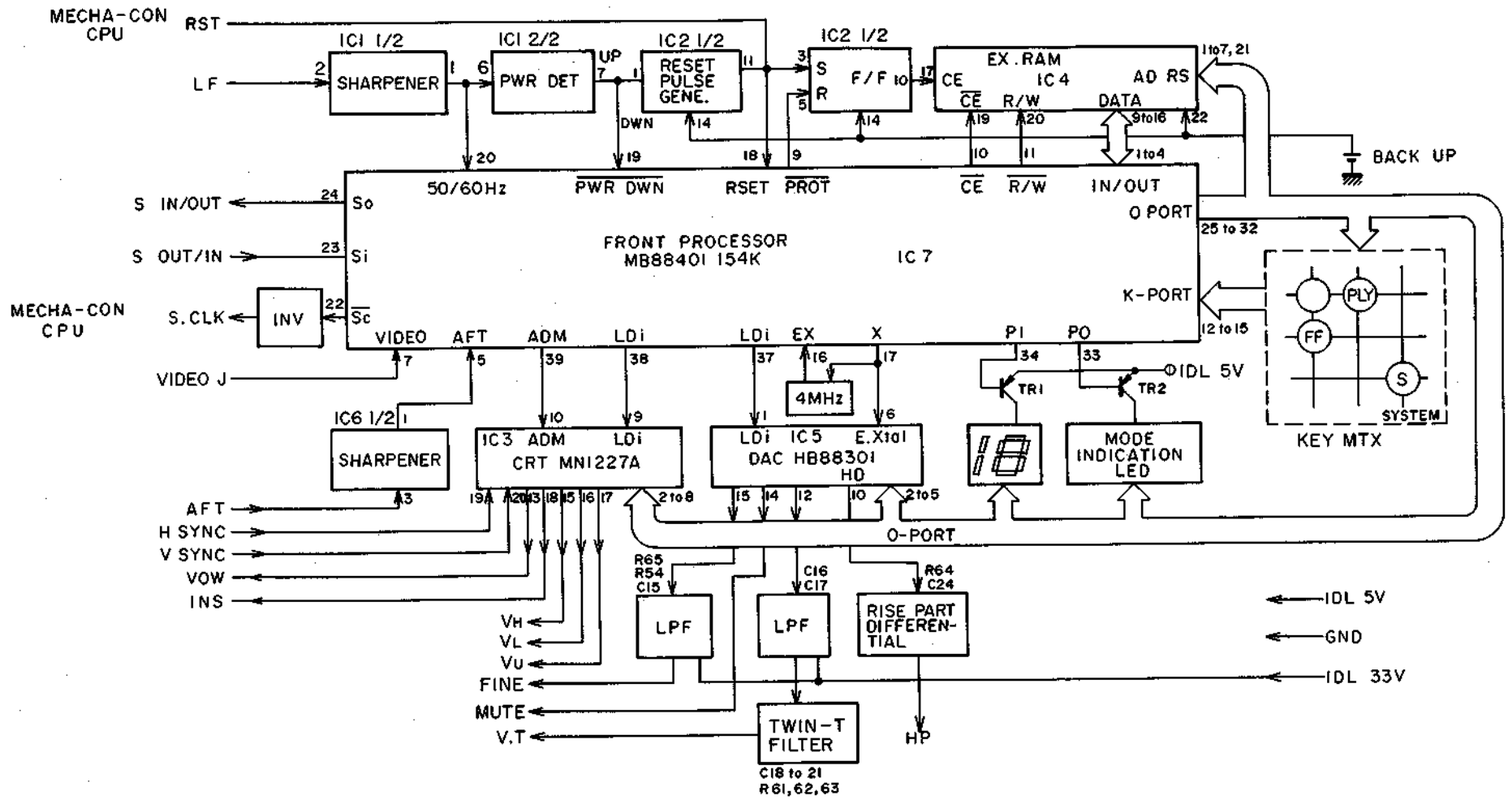


Fig. 7-76 Block Diagram of Operation Circuit

Fig. 7-76 shows the block diagram of the operation circuit. Peripheral circuits, such as EXT RAM (IC4: program content holding), D/A converter (IC5: tuning voltage), CRT interface (IC3), key matrix, power UP/DOWN (IC1), Reset Pulse generator (IC2), channel/LED display circuit, and LPF, are arranged around the front processor (IC7).

When the power is switched on, the 50/60 Hz signal enters LF (Line Frequency), the power detector circuit detects power UP, it is fed to IC2 1/2, and a RESET pulse is generated there. This RESET pulse resets the microcomputers of the front and SYS-CON, and data are exchanged using Sin/out, Sout/in, and S. CLK. When the FUNCTION ON button is pressed, FUNCTION ON data is fed to the K-port of the front processor from the key matrix. As a result, the mode becomes the FUNCTION ON mode. Concurrently, the output signal from the O-port is fed to each circuit for control.

ⓐ Function-ON LED of the mode indication LED lights.

ⓑ Channel display LED displays the last channel.

ⓒ D/A converter outputs data corresponding to that channel, and supplies the tuning voltage to the tuner after it is converted to DC by the LPF.

ⓓ A specified character pattern is written in to the CRT interface (IC3) to correct the clock, and the signal for TV superposition is output to VOW(Video On Word), synchronized with H. SYNC and V. SYNC. As a result, the clock correction character pattern is displayed in the top left part of the TV screen.

As described above, it is so designed as to control peripheral circuits by the front processor.

5-2 RESET RELATED CIRCUITS

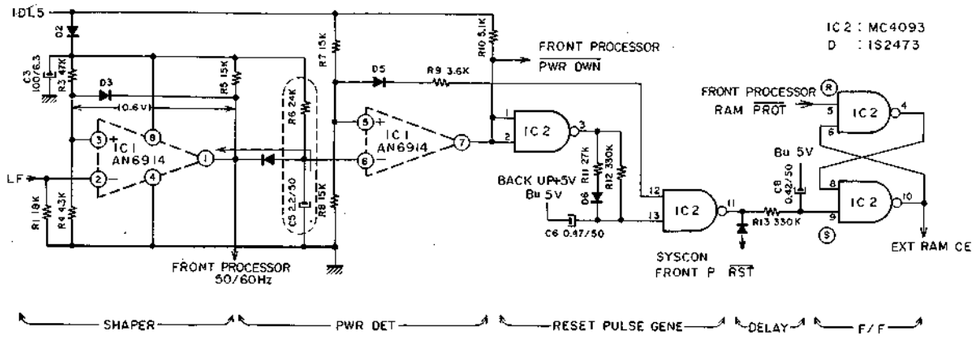


Fig. 7-77 Reset Related Circuits

Fig. 7-77 is the wiring diagram of reset related circuits. LF (Line Frequency) is a signal as shown in Fig. 7-78. The IC1 comparator output (pin ①) becomes LOW when LF exceeds 2.1V (determined by R3 and R4), and becomes HIGH when LF falls below 0.6V (forward voltage of D3). Since LF is supplied from the power line, when it becomes LOW or nonexistent due to power failure or else, IC1 pin ② immediately becomes 0V via R1, and the output (IC1 pin ①) becomes HIGH.

When IDL 5V exceeds the threshold voltage of IC2, a series of changes as follows take place.

IC2 pin ①/②– 'H' – IC2 pin ③– 'L' – C6 charge (C6× R12) – IC2 pin ⑬– 'H' / IC2 pin ⑫– 'H' > IC2 pin ⑪ – 'L'

However, when charging of C6 is completed at a time determined by C6 and R12.

IC2 pin ⑬ – 'L' / IC2 pin ⑫ – 'H' > IC2 pin ⑪ – 'H'

When the power is switched on, a negative pulse (⎍) can be supplied to IC2 pin ⑪. RESET pulse is sent to the microcomputer (IC7) of the Operation Board and the microcomputer of the system control for effecting reset. When the RESET pulse is output from IC2 pin ⑪, the potential of IC2 pin ⑨ becomes LOW only after about 60 ms which is determined by the time constant of R13 and C8. As a result, IC2 pin ⑩ (EXT RAM CE) becomes HIGH , and EXT RAM can be accessed.
Fig. 7-78 shows the waveform at each part at the power input sequence.

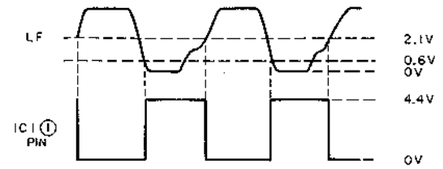


Fig. 7-78 Line Frequency (LF)

Fig. 7-80 shows the signal waveform at power down time.

In Fig. 7-77, at power down, first LF becomes nonexistent, then the voltage at IC1 pin ⑥ starts rising under the control of the time constant determined by R6 and C5, IC1 pin ⑦ becomes LOW when this voltage exceeds 2.5V, As a result POWER DOWN is output, and it is sent to the front processor pin ⑲. According to this data, the front processor saves all required data by storing it in the external RAM in about 8 ms, brings PROT to LOW level to prevent the content of the external RAM from changing, and sends this information to IC2 pin ⑤. Flip-flop (IC2) is reset thereby, IC2 pin ⑩ (EXT RAM CE) becomes LOW, and EXT RAM can no longer be accessed, so that the contents are protected.

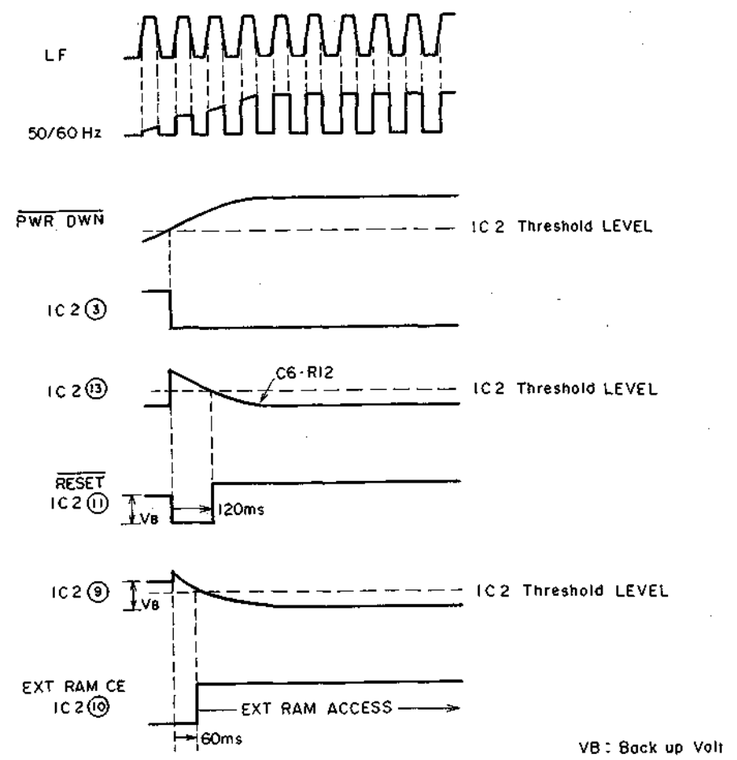


Fig. 7-79 Signal Waveform at Power ON time

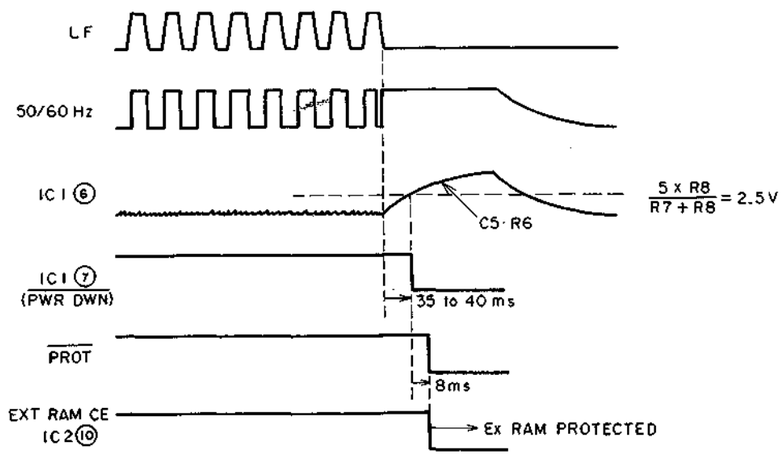


Fig. 7-80 Signal Waveform at Power Down

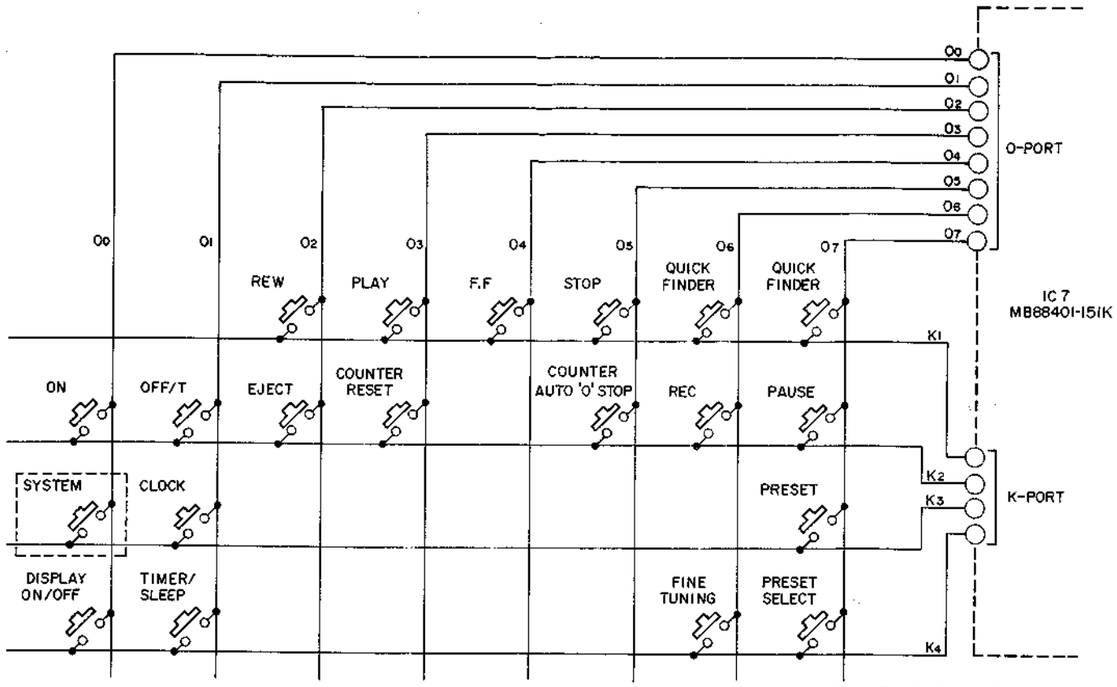


Fig. 7-81 Key Scanning

Of eight O-port outputs (pin (25) – pin (32)) of the front processor, each output is brought to LOW level sequentially. K input (K-port: pin (12) – pin (15)) is read. If it is LOW, the microcomputer identifies which key is depressed based on the data about which pin No. of O-port has been made LOW and data about the pin No. of K-port which is at LOW level. 32 ms is required for a single scan. The microcomputer judges that the key has been depressed properly, if the key has been depressed for two scans. (Chattering can be prevented) Only when the REC key is depressed from the STOP state, REC is not accepted even at the 9th scan unless the REC key has been continuously depressed during that time, thus preventing one touch record by accident.
Each time the SYSTEM key (newly provided in VS-2 EGN) is pressed, an "H"→ "L" or "L"→"H" signal is sent out to the system switching microcomputer in the servo PCB, through the connector P-34 from the front processor R3 (pin (40)).
Fig. 7-81 key scanning.

Key Depressed / Mode	CODE	FF	REW	STOP	REC	PLAY	CUE	REVIEW	F-ON	F-OFF	EJECT	PAUSE	COUNTER RESET	MEMORY
		01	02	03	05	06	07	08	0C	0D	00	19	0A	04
FUNCTION OFF									STOP					
STD-BY	0									○	○		○	○
FF	1		○	○		○	○	○		○	○		○	○
REWIND	2	○		○		○	○	○		○	○		○	○
STOP	3	○	○		○ *2	○	○	○		○	○	STOP PAUSE	○	○
REC	5	○	○	○						○		REC PAUSE	○	○
PLAY	6	○	○	○			○	○		○	○	PLAY PAUSE	○	○
STOP PAUSE	9	○	○	○	REC *2 PAUSE	PLAY PAUSE	○	○		○	○		○	○
REC PAUSE	B	○	○	○	○					○	○		○	○
CUE	7	○	○	○		○		○		○	○	PLAY PAUSE	○	○
REVIEW	8	○	○	○		○	○			○	○	PLAY PAUSE	○	○
PLAY PAUSE	C	○	○	○		○	○	○		○	○		○	○

Fig. 7-82 Key Acceptance Judgement Table

CUE/REVIEW : In VS-5, acceptance only from PLAY.
In VS-2, acceptance even from FF and RWD.

◯ : Acceptable.
Character display: Corresponds to that mode.
Blank: Unacceptable.

*1 : Eject state or cassette-nonexistent state.
*2 : Acceptable only when cassette tab is unbroken.

5-4 CRT CONTROL (IC3: MN-1227A)

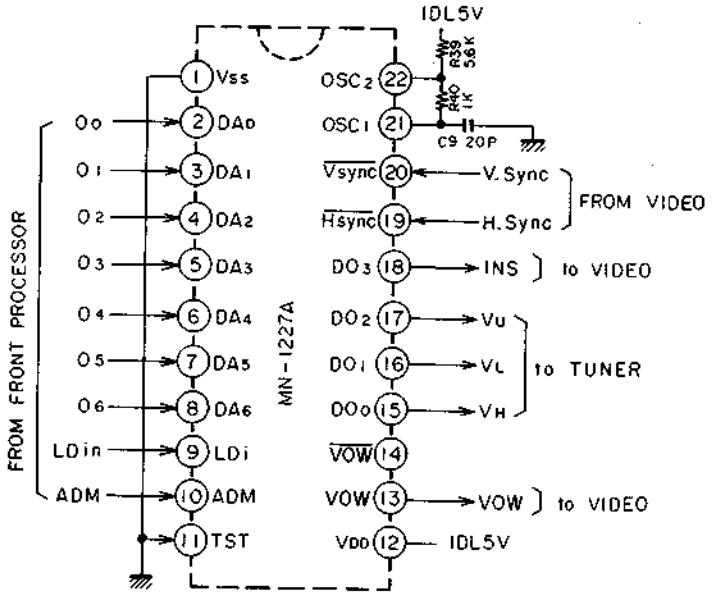


Fig. 7-83 CRT Interface

1) Operational outline

MN-1227A has a built-in character pattern generator. Data about "the display position" (60 points) and "characters to be displayed" (44 kinds) are read at the leading edge and the trailing edge of LDi from the front processor into 0_0–0_6, and the superposing signal is output from VOW, synchronized with the leading edge of V SYNC and H SYNC.

R39, R40, and C9 control an oscillator at about 6 MHz, and this determines the character size.

INS is controlled by the front processor so that when a character is to be recorded, it becomes 'H', and it is fed to the video PCB.

VU, VL and VH are tuner band switching signals. When any one becomes 'H', that band alone is selected.

2) Data loading

Data are loaded into the MN1227A data memory in any of the following two modes.

ⓐ Direct address mode (ADM='L')

When ADM is at 'L' level (Refer to Fig. 7-84), DA_0–DA_6 7-bit data is latched at the memory address register at the time when the signal fed to LDi terminal changes from 'L' to 'H', and DA_0–DA_5 6-bit data is loaded into the memory address appointed by the memory address register at the time when the signal at the LDi terminal changes from 'H' to 'L'.

ⓑ Address increment mode (ADM='H')

In the case when ADM is at the 'H' level (refer to Fig. 7-85), the data already latched at the memory address register is incremented when the signal fed to LDi terminal changes from 'L' to 'H', and DA_0–DA_5 6-bit data is loaded the memory address specified by the memory address register after the increment mode is complete, as the signal at the LDi terminal changes from 'H' to 'L'.

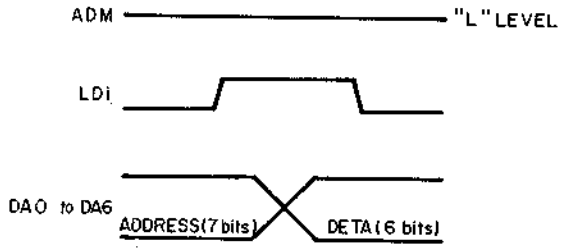


Fig. 7-84 In the case of ADM='L'

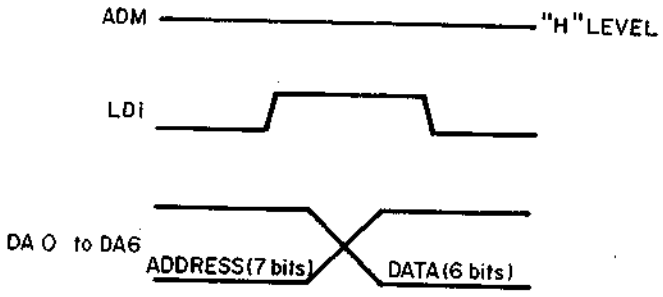


Fig. 7-85 In the case of ADM='H'

5-5 EXT RAM: IC4

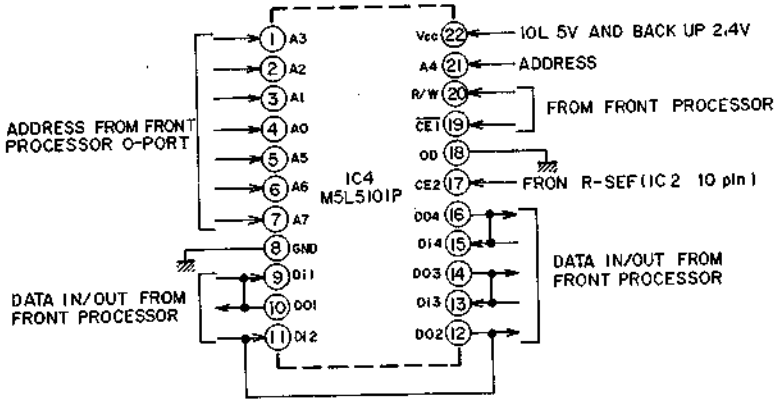


Fig. 7-86 IC4: EXT RAM

Pin functions are as follows:

1) Pin (1) thru pin (7) and pin (21) : address designation
2) Pin (9) thru pin (16) : data in/out. Data exchange with front processor.
3) Pin (17): R.S FF output. When this is connected with pin (10) , and is at HIGH level, RAM operation becomes possible.
4) Pin (19): When this terminal is connected with $\overline{CE}$ terminal of the front processor and is at LOW level, RAM is disabled.
5) Pin (20) : W/R terminal. This is connected with WR terminal of the front processor. Data is read when this is HIGH, while data is written when this is LOW.
6) Pin (22) : Vcc. Normally IDL 5V is impressed. B1 (battery) backup (2.4V) in case of power OFF.

5-6 LED SCAN

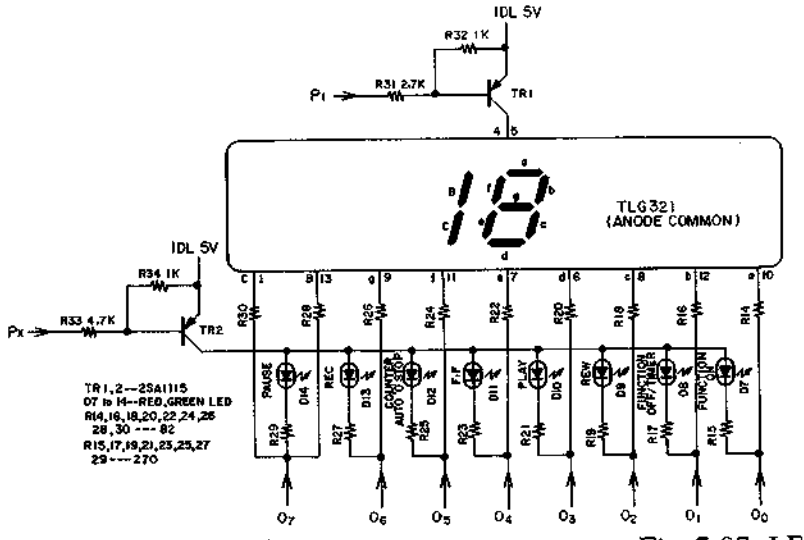


Fig. 7-87 LED Control Circuit

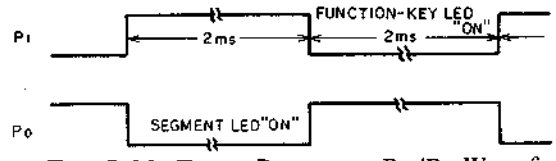


Fig. 7-88 Front Processor P_0/P_1 Waveform

Fig. 7-87 shows the LED scan circuit. Channel display segment LEDs and function mode display LEDs are switched every 2 ms, and dynamic LED ON operation is performed. This is because the contents of both LED displays are controlled by the data of the same O-port. In this way, the number of output pins of the microcomputer is kept to a minimum. As shown in Fig. 7-88, TR1 and TR2 are alternately switched ON and OFF by P0 and P1 from the microcomputer, and the output of the O-port of the microcomputer alternately changes between the channel display data and function mode display data. Since the switching time is as fast as 2 ms, both appear to be ON at the same time. However, since ON time of each LED is half that of the static ON condition, the values of series resistors (R14–R30) are set at small values. Before access is made to EXT RAM, D/A converter, CRT controller, etc., all LEDs are turned OFF. Accordingly, it may sometimes occur at such time that the LEDs flicker.

5-7 D/A CONVERTER PERIPHERAL CIRCUITS

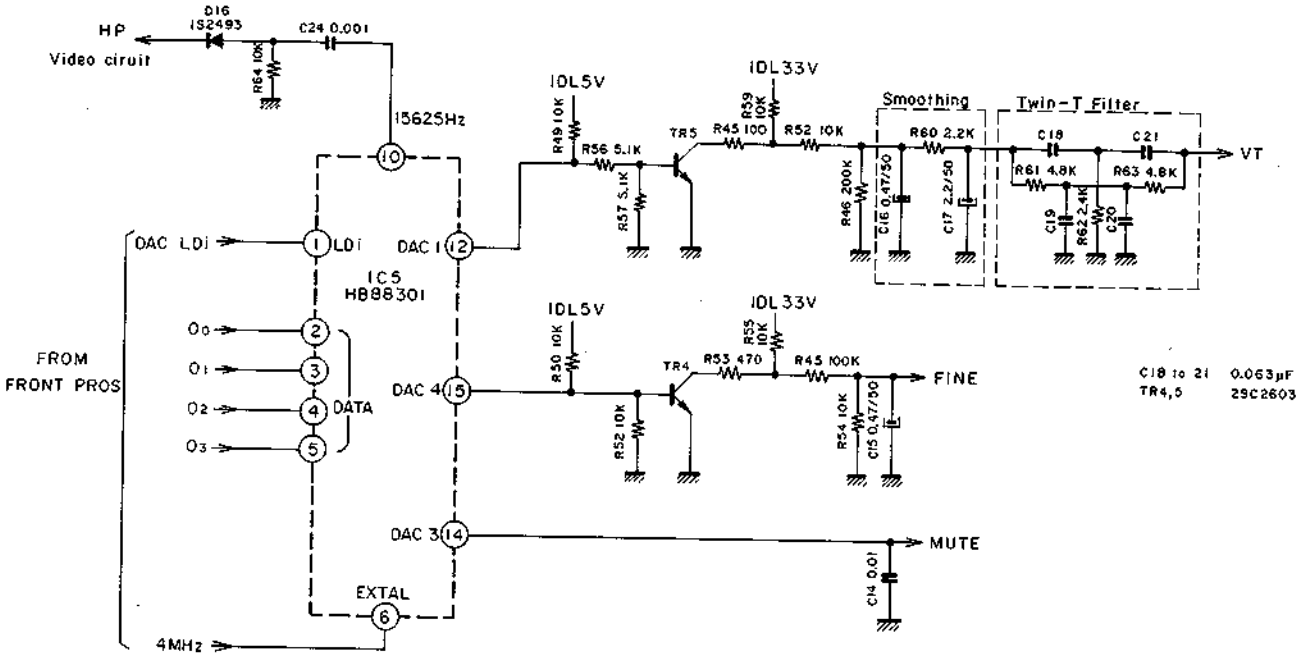


Fig. 7-89 D/A Converter Peripheral Circuits

1) Fig. 7-89 shows D/A converter peripheral circuits.
VS-2 employs a D/A converter (IC5) using the pulse width modulation system. IC5 consists of four D/A converters, three of which are used.

DAC-1 is a VT 13-bit signal, DAC-3 is a mute control 6-bit signal, and DAC-4 is a fine data 6-bit signal.

DAC-1 output passes through the smoothing circuit (R60, C16, C17), and then the main component of 2 ms, which is the repetition period of the DAC output, is removed by the Twin-T type filter.

This has a long repetition period compared to Fine (DAC 4), and the number of bits is large. Therefore, unless DC conversion is performed thoroughly, the use of 13 bits is wasted, while if the time constant is set at a large value, an unduly long time would be required until VT becomes stable. The above is required for the effective solution of the problem.

The range of VT change is from 0.31±0.02V to 3 ±1.8V. It is designed so that the VT change/bit is small when the VT potential is low, and that the VT change increases as the VT potential rises, by using a variable time constant during charge/discharge. (Refer to Fig. 7-90). A tuning oscillator variable capacitor diode exhibits the characteristic where VT changes more when its potential is low than when it is high. The above action is taken, which more or less compensates for it.

DAC-3 output is used as a mute signal. Since a 1-bit spike of noise is output once in 32 μs when Mute is switched off, it is removed by C14 and a resistor on the tuner side.

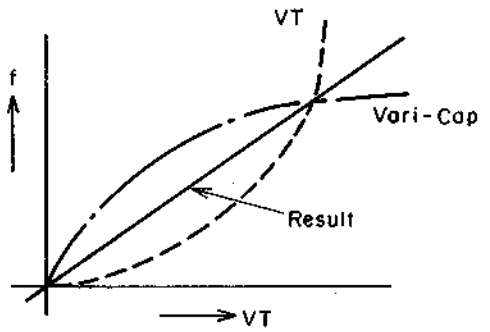


Fig. 7-90 VT change

There is a clock divide output in IC5 (MB88301). The 4 MHz clock is subjected to division by 256 down to 15625 Hz. The resultant signal is picked up at pin (10) and differentiated by C24 and R64. Only the leading edge is sent to the video circuit by D16. This is used as a trigger for the horizontal frequency to make the character appear at the left top part of the screen even when there is no video signal.

2) Pulse width modulation type D/A converter

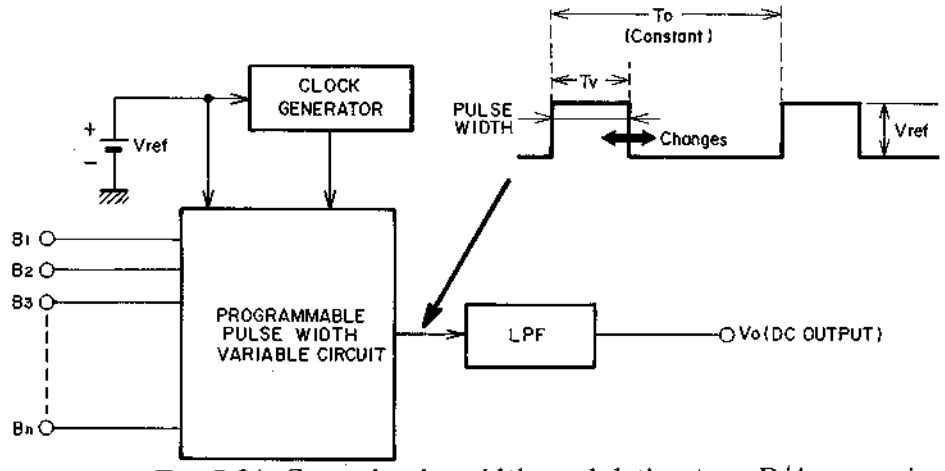


Fig. 7-91 General pulse width modulation type D/A converter

$$\begin{cases} V_O = \dfrac{T_V}{T_O} \times V_{ref} \\ T_V = T_O\,(B_1/2 + B_2/2^2 \ldots\ldots + B_{n-1}/2^{n-1} + B_n/2^n) \end{cases}$$

In the pulse train of a constant period at a constant voltage, duty cycle matching with the set digital input is generated. Smoothing by the LPF is used to obtain a D/A converted output.

Features

(a) Accuracy is not affected by the variation of clock frequency.

(b) Low cost and high precision compared with other D/A converters.

High-speed operation cannot be achieved since a LPF is used.

5-8 SEARCH OPERATION AND AFT

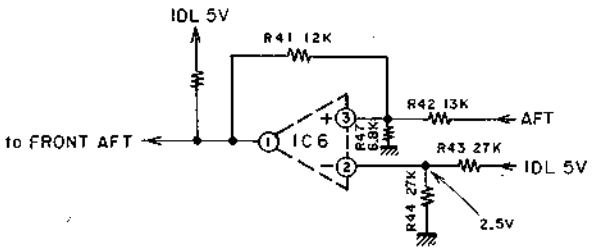


Fig. 7-92 AFT Comparator

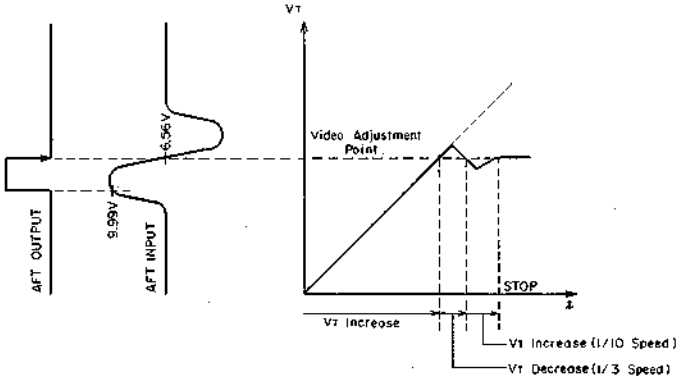


Fig. 7-93 AFT Comparator input/output and VT

Fig. 7-92 shows the AFT comparator.

When PRESET selector button is pressed and then button-B is pressed, the TV search mode is initiated, and the front processor gradually raises the tuning voltage (VT) via the D/A converter (*1). Since the AFT input from the tuner changes as shown in Fig. 7-93 if there is a TV signal, present the front processor starts reducing the value of VT at only one third of the speed curing the time that AFT falls after the original steady increase. (*2)

However, since the VT change lags in time after the microcomputer passes its output to DAC as a result because that VT passe suffers delay through LPF, VT continues rising for a while after the TV signal has been recognized, and turns to falls a little later.

When the AFT output becomes HIGH, VT is again increased but at a speed 1/10th the initial speed (*3). The time lag of VT presents no problem at this speed. Then, VT is stopped when the AFT output has become LOW.

Now, there would be no significant overshoot, and the VT potential would come within the trailing edge of AFT input. Then, AFT is turned ON (Mute off). Video judgement is performed after 0.2 second. If VID. J='H', "FOUND . . . " is displayed. When button -C is pressed, an instruction is given to memorize the data. Then, the data being output to DAC is stored in EXT RAM as VT data of that channel.

As a result, a channel stored previously may be called by specifying the VT data to the DAC correspoinding to TV data to be read from EXT RAM each time a channel is selected.

In order to make the AFT input resistant to noise, positive feedback is effected by R41, and hysteresis is provided.

*1 1 bit change in 3 ms

*2 1 bit change in 9 ms

*3 1 bit change in 30 ms

5-9 AFT CONTROL

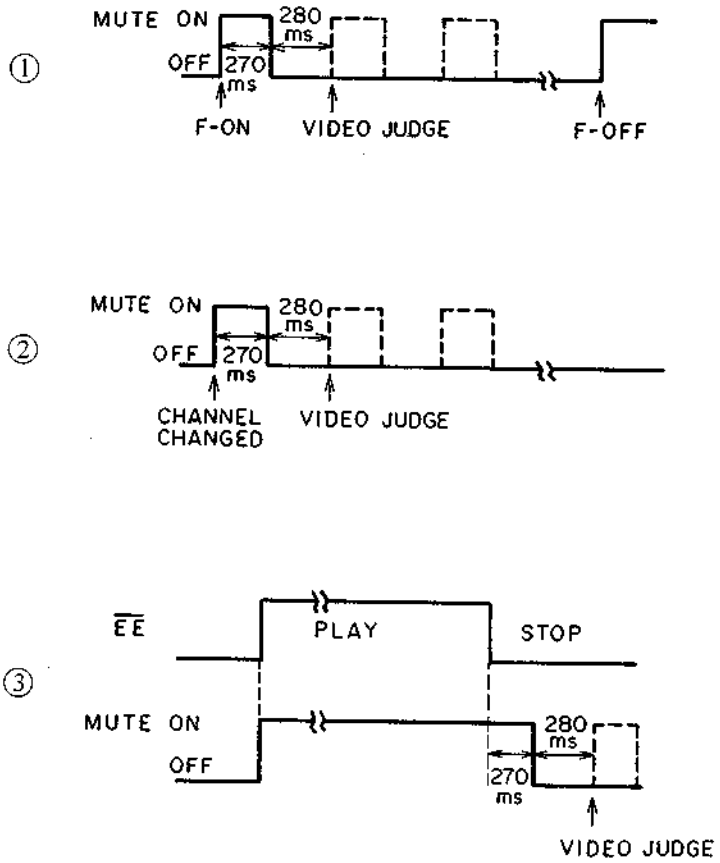


Fig. 7-94 AFT control

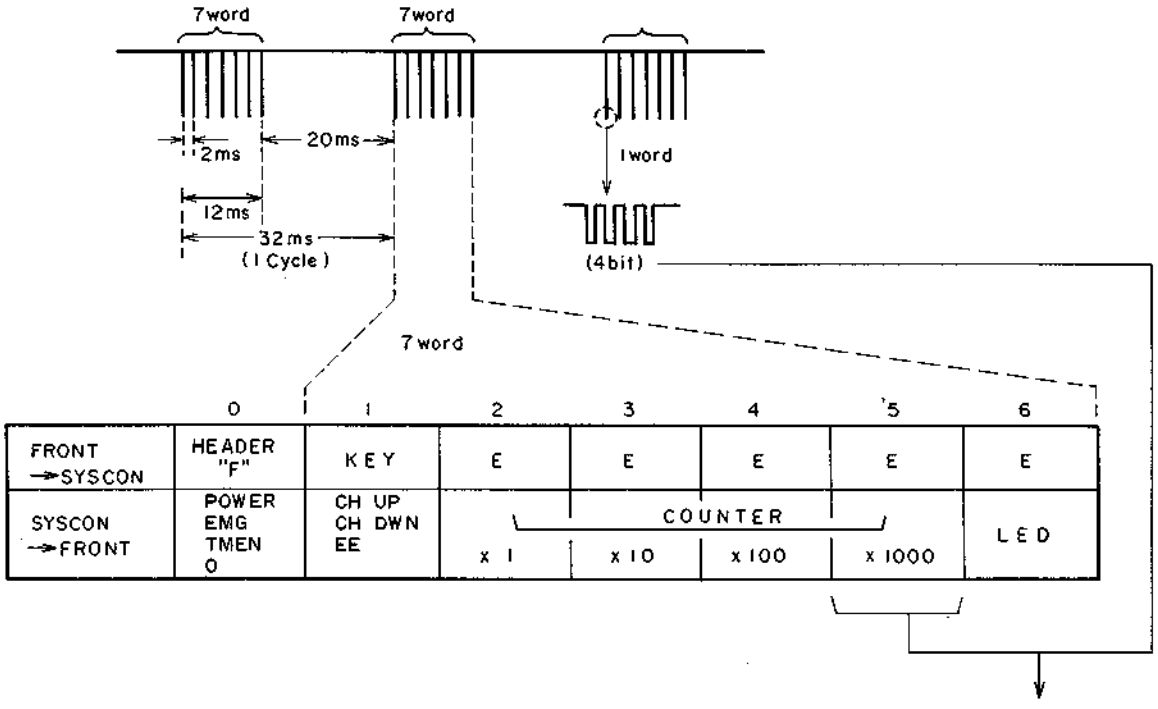
In the case of EE signal changes and changes made on the function buttons of ON/OFF, PRESET SELECT, and PLAY/STOP, the front processor switches the Mute output to the tuner ON/OFF. This Mute output is at once an AFT control output for VT, and it is designed so that Mute ON effects AFT OFF, and Mute OFF effects AFT ON.

1) Function key ON/OFF (Fig. 7-94 ①)
When the function-ON key is depressed, the last channel data is output to the DAC, Mute is switched ON in 270 ms, and video judgement is performed 280 ms after AFT ON occurs. When non-video signal judgement is made, this operation is repeated over and over again. (cycle time: 550 ms) Reason: When broadcast of a preset channel has completed, if AFT is left ON, . . . is drawn in a strange place due to noise, getting away from this may not be possible even when a broadcast begins. (Same as VS-5)

2) PRESET SELECT (Fig. 7-94 ②)
Similar to 1). Mute is switched ON for a period of 270 ms, AFT is turned on, and then video judgement is made after in 280 ms. The rest is the same as 1).

3) EE signal change (Fig. 7-94 ③)
When the mode ceases to be EE due to, say, PLAY, Mute is applied to the tuner so as not affect the playback system. Mute is kept ON for a period of 270 ms after the mode is returned from PLAY to EE, AFT is switched ON, and video judgement is performed after 280 ms. The rest is the same as 1).

270 ms and 280 ms are longer than the times required for VT to gain the corresponding potentials after VT data is sent to DAC, and also longer than the time during which the VIDEO DETECT signal is established after AFT ON occurs. (Though both are set at the same time during the programming, 'H' time is shorter than 'L' time due to the effect of C14.)



Command / Code	KEY	LED
0	EJECT	STD-BY
1	FF	FF
2	REW	REW
3	STOP	STOP
4	–	REC-PAUSE
5	REC	REC
6	PLAY	PLAY
7	CUE	CUE
8	REVIEW	REVIEW
9	PAUSE	STOPPAUSE
A	C-RESET	PLAYPAUSE
B	MEMORY	–
C	F-ON	DISP
D	F-OFF	TMSTDBY
E	–	–
F	–	–

POWER ; F-ON
EMG ; Emergency
TMEN ; Timer Enable
CH UP ; Channel Up
CH DWN ; Channel Down

F-ON: Function SW ON

Fig. 7-95 Data Transfer Format

VS-2EGN outputs transfer clock from $\overline{SC}$ (pin (22)) of the front processor. Data is output to So at the trailing edge of this $\overline{SC}$, and Si data is read at the leading edge. Conversely, the SYSCON reads data at the trailing edge of $\overline{SC}$, and outputs the next data at the same time. Accordingly, direct connection of SC of both microcomputers will result in erroneous data reading. Therefore, $\overline{SC}$ is inverted at TR3, and is sent to SYSCON as an S. CLK instruction.

1) Transfer format

Data transfer between the front microcomputer and the system microcomputer is performed according to the transfer clock of the front microcomputer.

One cycle transfer is completed with seven 4-bit words. Fig. 7-95 shows the transfer format.

2) Transfer clock (Fig. 7-96)
One transfer cycle time is about 32 ms. Actual transfer is performed in the first 12 ms (2ms x 6), and no transfer clock is sent for the remaining 20 ms. Due to serial transfer, this is for the bit matching at the SYSCON.

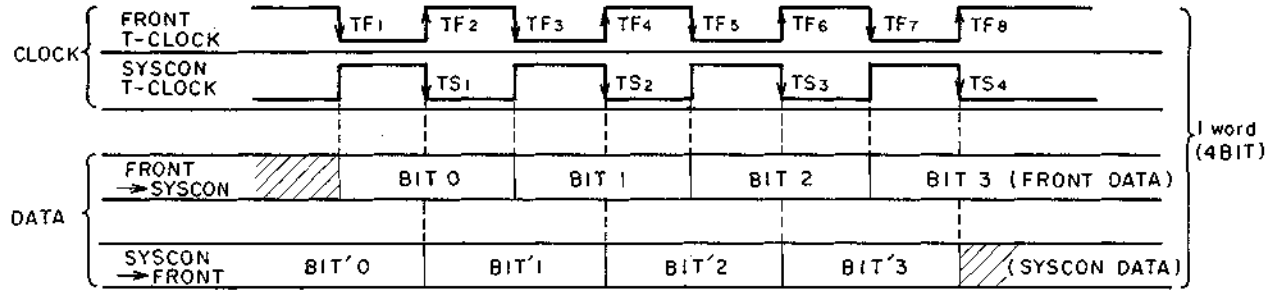


Fig. 7-96 Relation between transfer clock and data

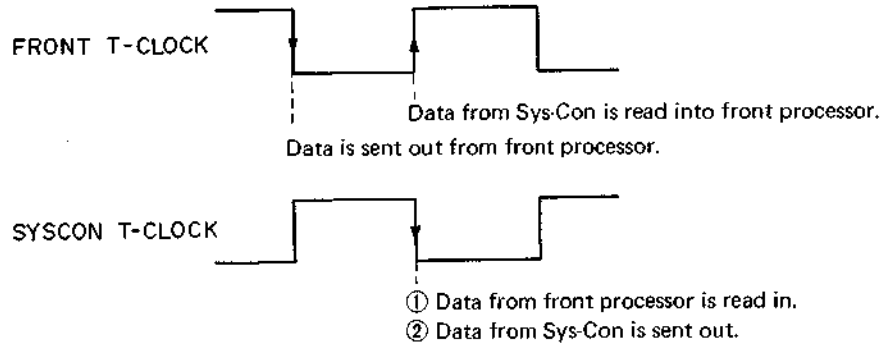


Fig. 7-97 Transfer clock

Fig. 7-97 shows the relationship between the transfer clock and data.
SYSCON data Bit 0 appears at the output terminal concurrent with SYSCON microcomputer (ACC) accumulator output reaching the output buffer. Accordingly, SYSCON data appears independent of SYSCON T-Clock.
Though Bit 0 of input data is output following Bit 3 according to System T-Clock "TS4", this data is invalid since it is spaced 20 ms to the next data.

3) Tape status check
The SYSCON microcomputer checks the tape status first by the SENS input, and then accepts the next key-in.
Necessary inputs for SENS inputs are as follows:

ⓐ EJECT SW (Eject or not)
ⓑ START SENSOR
ⓒ END SENSOR
ⓓ REC SAFETY SW (No Safety Tab)

4) Infrared remote-control decoding
Signals sent from the remote-control unit are amplified/shaped at the receiving circuit, and the codes are decoded. The codes are the same as those of VS-5 except that the display (character display on the TV screen) is added and Sound-Dub is removed.

CODE	COMMAND	CODE	COMMAND
00		10	
01	FF	11	
02	REW	12	
03	STOP	13	
04		14	
05	REC	15	
06	PLAY	16	
07	CUE	17	
08	REVIEW	18	
09	PAUSE	19	
0A	COUNT-Reset	1A	CH-DOWN
0B	DISPLAY	1B	CH-UP
0C	F-ON	1C	
0D	F-OFF	1D	
0E		1E	
0F		1F	

Fig. 7-98 Remote-control Code Scheme

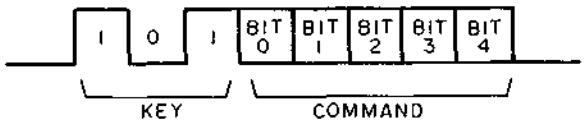


Fig. 7-99 Remote-control Code Content

6. THE POWER /SYSCON CIRCUIT

6-1 INTRODUCTION

The power & syscon circuit consists of a power supply circuit, and a microprocessor (syscon) and associated circuits. (Note that the tuner and timer control section are not included.)
For the power supply section, the timer data count, time, etc. are displayed on the TV screen rather than using FLD, thereby eliminating the need for a transformer for FLD. In addition, all ICs in use operate on ⊕ power, eliminating the need for ⊖ power.

6-2 POWER SUPPLY SECTION

The power supply circuit consists of unregulated 9V and 19V circuits. The action of each of the circuits is as follows:

6-2-1 UNREGULATED 9V CIRCUIT

1) IDL 5V
5V is generated from UNREG9V by a 3-terminal regulator (TA78L005AP). IDL5V is used both in POWER SYSCON and on OPERATION PCB.

2) Line Frequency (LF)

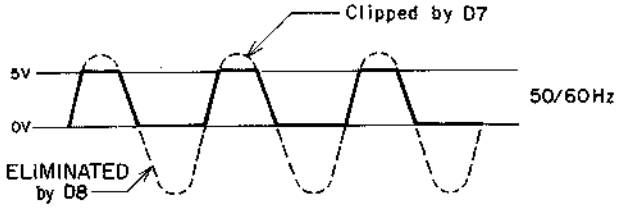


Fig. 7-100 Waveform of Line Frequency (LF)

Line frequency (LF), on which micro-computer power failure detection and timing are based, is produced from AC9V and supplied to OPERATION PCB.

6-2-2 UNREGULATED 19V CIRCUIT

1) SERVO 19V and drum heater 19V
The power is supplied to SERVO PCB as drum heater 19V and SERVO 19V. It is regulated in the servo circuit. To reduce power consumption, the power to the drum heater is turned off/on as the servo power is turned on/off, and heater current is also reduced as much as possible.
Thus, while the servo is operating, the drum heater is turned off, or vice versa, so as to balance the power supply.
SERVO 19V is controlled by $\overline{\text{SERVO}}$. The purpose is to achieve power saving and simplicity in circuit design by turning on/off the power to the servo system as the drum motor is turned on/off.

2) IDL 12V
IDL 12V, which is used as the power to the booster and remote control receiving section, is produced from UNREG 19V by a 3-terminal regulator IC1 (TA781012AP).

3) EE 15V
By making EE voltage available at 15V, it becomes possible to incorporate a 3-terminal regulator within the video PCB. This eliminates the need for re-adjustment after assembly of VRs already adjusted on the PCB prior to assembly. (This applies only to circuitry associated with EE12, however.)

4) AL12V and AL15V
AL15V is used for the mechanism (reel motor, loading motor and plunger) as well as for EE 15V. AL12V is produced from AL15V.
On VS-2, PB12V and REC12V are produced from AL 12V.
AL15V and AL12V are produced in IC2 (STK-5315). STK-5315 is a hybrid IC incorporating 15V and 12V regulators. (See Fig. 7-101.)
Semi-regulated AL15V (15 ± 0.3V) is used as the voltage for the drive circuit for each of the following mechanism driving components:
ⓐ Plunger
ⓑ Loading motor
ⓒ Reel motor
ⓓ Lamps
The use of the semi-regulated voltage ensures that even with AC input voltage fluctuation of 10%, stabilized mechanism driving can be achieved if 15V REG is kept stable, and that the proper plunger current can be obtained without being affected by AC input fluctuations. All this has resulted in reduced current for each of the mechanism components (e.g., plunger take-in current..... 0.5A with VS-2 against 2A with VS-5)

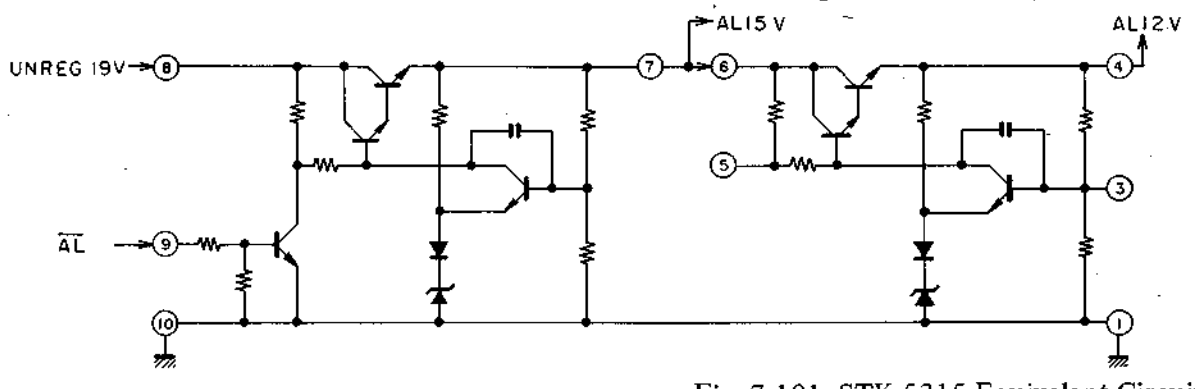


Fig. 7-101 STK-5315 Equivalent Circuit

5) Regulated 5V

The power supply for the micro-computer uses a different winding (secondary side) from the one used with the VTR drive system. This arrangement helps to minimize the effect of possible trouble in the mechanical section on the micro-computer system. (Micro-computer-independent PWR SUPPLY)

6) IDL 33V

This is the supply which provides the basis for the tuning voltage to be generated at the operation PCB. AC19V is doulbe-voltage rectified at D9, D3, C9 and C26, and smoothed at D4 and C10. With DC45V thus obtained, 33V regulated at IC4 (μPC574J) is generated.

6-3 CONTROL SYSTEM

Each VTR mode is controlled by a micro-computer, but the most of the circuitry is controlled through the or via the power supply. With VS-2, the micro-computer and power supply section are installed on the same PCB, and the power supply and control line to each block are provided on a per-connector basis.

6-4 POWER SUPPLY CIRCUIT

Fig. 7-102 is the block diagram of the power supply circuit with each power output given in detail.

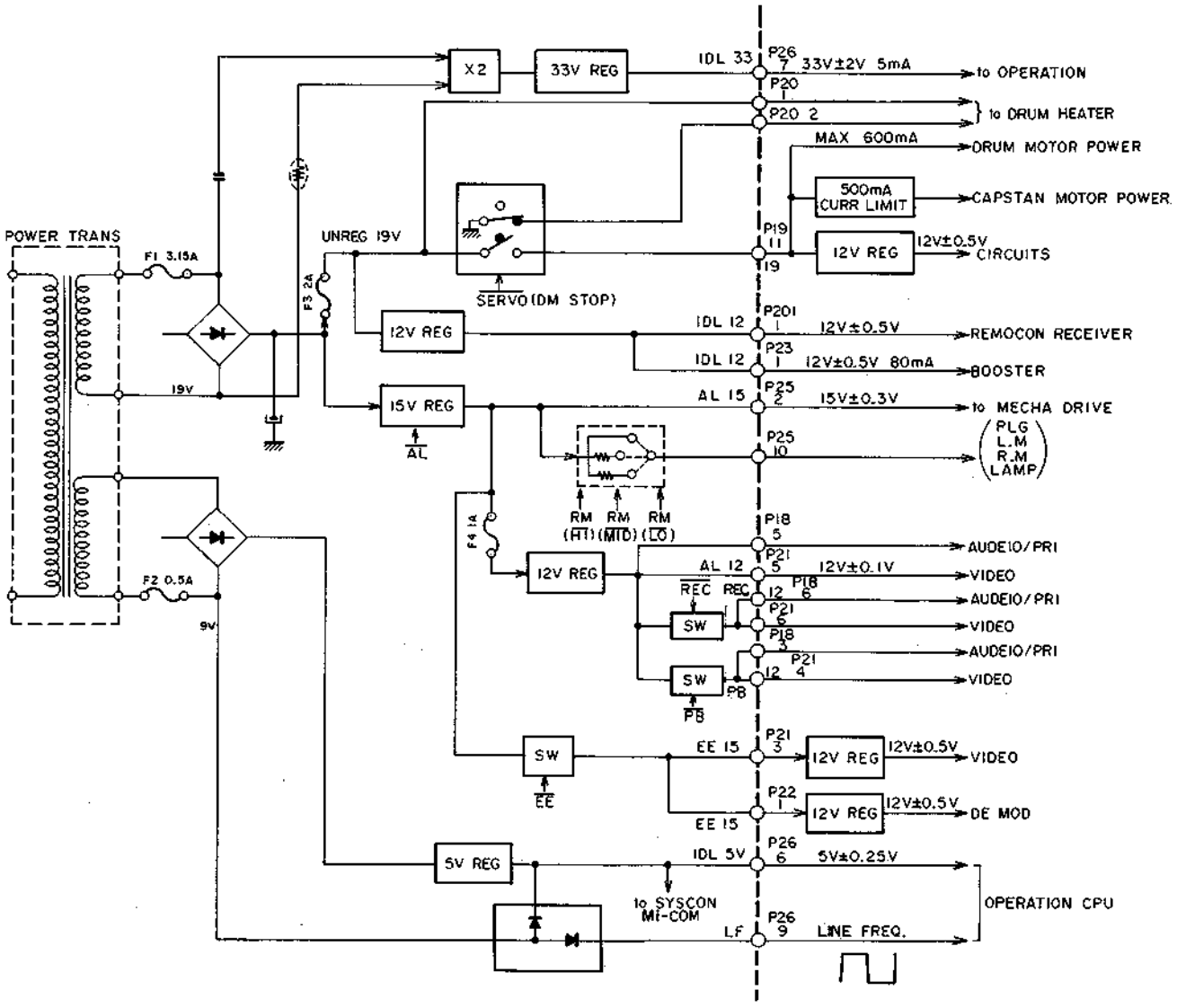


Fig. 7-102 Block Diagram of Power Supply Circuit

6-5 SYSCON SECTION

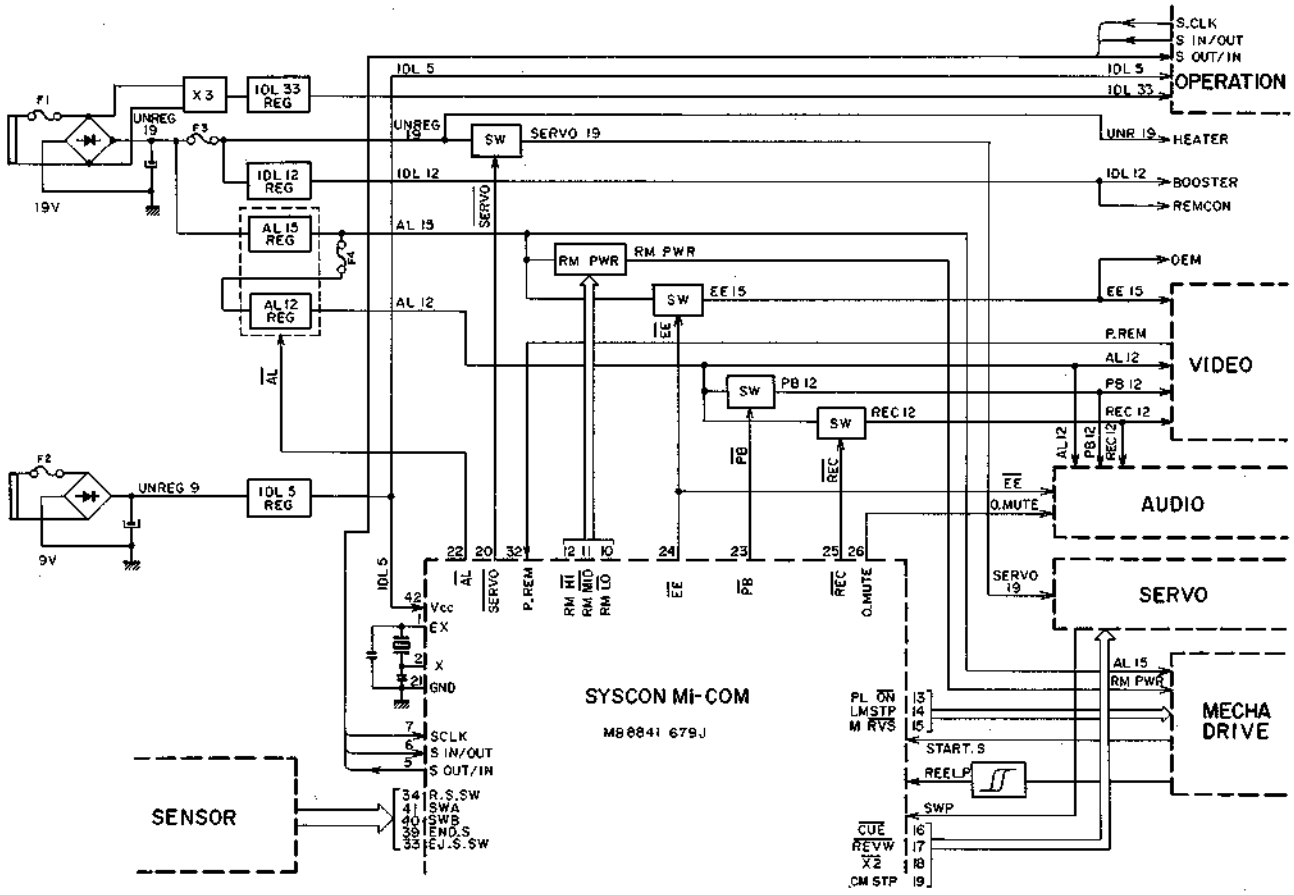


Fig. 7-103 Block Diagram of Power/Syscon Circuit

6-5-1 KEY ACCEPTANCE TESTING

The mech-control key data taken in by the front processor (or FRONT) is tested according to the "Key Acceptance Table" (Fig. 7-82), so as to provide mech-control.

6-5-2 TAPE CONDITION CHECKING

By checking on EJ. S. SW (whether ejected or not), STRT. S (start sensor), END. S (end sensor) and R.S. SW (claw folded), the FF, AUTO REW and KEY acceptance are tested.

6-5-3 INFRA-RED REY (IFR) REMOTE CONTROL DECODING

The signal from the remote controller is amplified and corrected for decoding. The codes in use are almost identical to those used with VS-5 except that S-DUB has been deleted and DISP (character, counter, time, and/or day of week ON/OFF on TV screen) added. The Fig. 7-104 summarizes the remote control codes in use.

Code	Command	Code	Command
00		10	
01	FF	11	
02	REW	12	
03	STOP	13	
04		14	
05	REC	15	
06	PLAY	16	
07	CUE	17	
08	REVIEW	18	
09	PAUSE	19	
0A	C-RESET	1A	CH-DOWN
0B	DISP	1B	CH-UP
0C	F-ON	1C	
0D	F-OFF	1D	
0E		1E	
0F		1F	

Fig. 7-104 Remote Control Codes

6-5-4 PAUSE REMOTE CONTROL

The PAUSE remote control provides control over REC↔R. PAUSE and PLAY↔P. PAUSE through switching between HIGH and LOW.

- The rising edge converts REC mode to REC pause or PB mode to PB pause.
- The falling edge converts REC pause to REC mode or PB pause to PB mode.

With HIGH (PAUSE) selected, depressing the key REC/PLAY on VTR results in R. PAUSE/P. PAUSE. With LOW (REC/PLAY) selected, the key on VTR itself is accepted just as when the PAUSE remote control terminal is disconnected.

6-5-5 POWER SUPPLY CONTROL

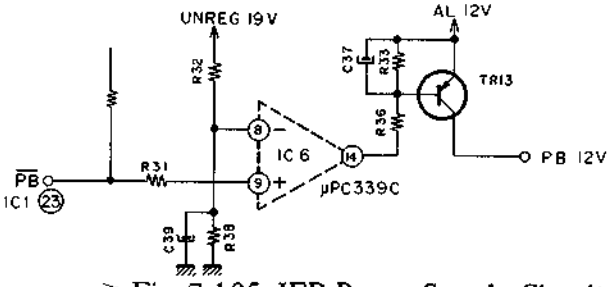


Fig. 7-105 IFR Power Supply Circuit

The key depressed on the front panel or remote control command entered is tested to turn on/off power supplies (AL12V, AL15V, PB12V, EE15V and REC 12V).

When the mode in which PB12 is to be sent out is established, $\overline{PB}$ goes to "LOW" and pin (14) of IC6 also goes to "LOW" which in turn activates TR13, causing PB12V to be supplied. The purpose of C37 is to prevent PB12V from being turned on/off abruptly.

Further, the purpose of R32, R38 and C39 is to set pin (14) of IC6 forcedly to "HIGH" for a period of time as determined by the time constant of R32 and C39, so as to prevent PB12V from being sent out until $\overline{RESET}$ is applied to the microcomputer after MAIN POWER on the rear is turned on.

Note that EE15V and REC12V are also controlled using the same circuit configuration.

6-5-6 REEL MOTOR POWER SUPPLY CONTROL

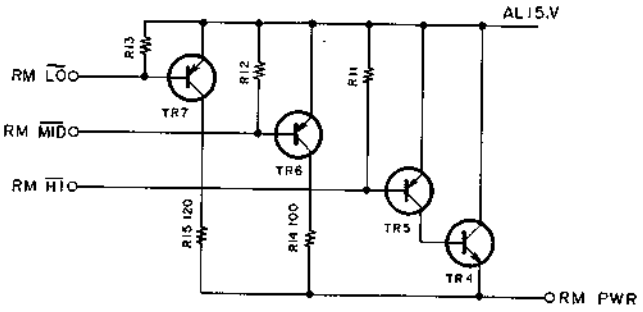


Fig. 7-106 Reel Motor Power Supply Circuit

As with VS-5, the reel motor is controlled through torque switching by means of three control lines RM-$\overline{Hi}$, RM-$\overline{Mid}$ and RM-$\overline{Lo}$. The torque varies depending on whether the motor is driven directly, via a 100 ohms resistance (R14), or via a 120 ohms resistnace (R15).

1) At FF/REW time . . . . . RM-$\overline{Hi}$ (Low)
   ; to be driven directly with TR5 and TR4.
2) At Review/AEC rewinding/Memory-stop rewinding time . . . . RM-$\overline{Mid}$ + RM-$\overline{Lo}$ (Both are Low)
   ; to be driven via R14//R15
3) At Unload time . . . . . RM-$\overline{Lo}$ (Low)
   ; to be driven via R15.

6-5-7 SERVO POWER SUPPLY AND DRUM HEATER CONTROL

If the $\overline{SERVO}$ terminal is at "HIGH", TR9 and TR8 are kept OFF, resulting in no power being supplied to the servo PCB, whereas TR10 and TR11 are activated, causing the drum heater to be energized. When the $\overline{SERVO}$ terminal goes to "LOW", TR9 and TR8 are activated, causing SRV19V to be supplied to the servo PCB, whereas TR10 and TR11 are deactivated, resulting in the drum heater being turned off. In other words, the power is supplied to the servo PCB only in the mode where the drum motor rotates, while the power supply is cut off in the mode where the motor does not rotate (in this case, the drum heater is turned on).

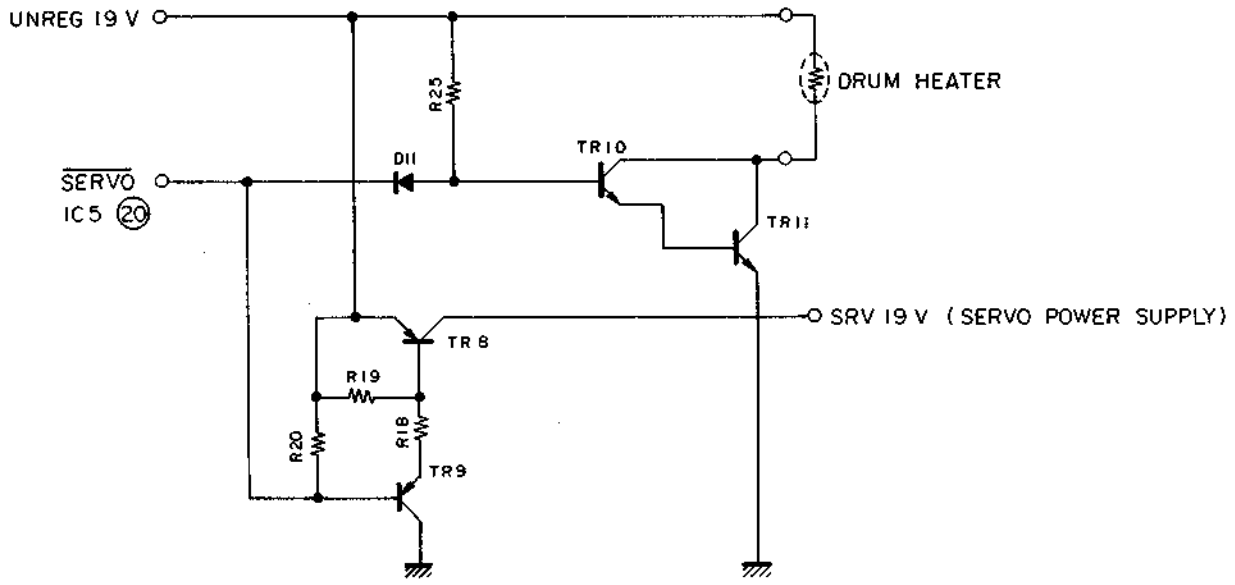


Fig. 7-107 Servo Power Supply and Drum Heater Circuit

SERVO	Servo Power Supply	Drum Heater
H	OFF	ON
L	ON	OFF

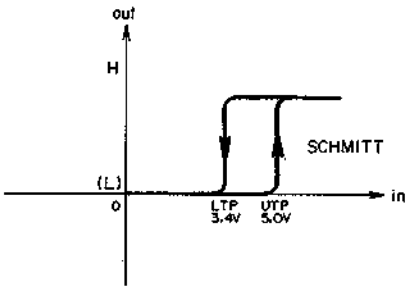
NOTE: 12V is produced from SRV19V (19V) in the servo PCB.

6-5-8 REEL PULSE, START SENSOR AND END SENSOR DETECTION

When AL15V is supplied with the FUNCTION "ON", the lamp comes on, allowing detection of the start/end sensor. In addition, the LED of the photo-interrupter PH1 also comes on, allowing detection of the reel pulse. For detection of the reel pulse, pulses generated by the photo-interrupter are given a hysteresis in the comparator for conversion to High (5V) and Low (0V). (Upper Trip Point (UTP): 5V) (Lower Trip Point (LTP): 3.4 V)

The reel pulse is used as the standard pulse for the reel stop detection (See 6-6 "Syscon Error Detection") and tape counter.

Where the reel pulse is used as the tape counter, the count is incremented or decremented by "±1" each time the rising edge of the pulse is encountered twice. As the detection wheel makes a complete revolution, 6 pulses are generated and therefore the count is incremented or decremented by "±3".



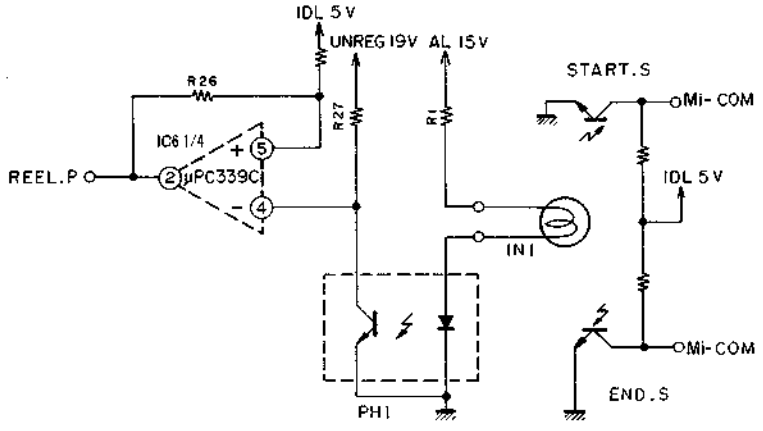


Fig. 7-108 Reel pulse, Start Sensor and End Sensor Circuit

6-6 VS-2 SYSCON ERROR DETECTION

The VS-2 Syscon (micro-computer) provides error detection to ensure safe operation.

6-6-1 BREAKDOWN

In a mode where the loading motor runs, if either the SW "A" or SW "B" state does not change within a certain period of time, the motor is assumed not rotating; all outputs are turned off and a key is no more accepted. (This applies also to VS-5.) To recover from breakdown, first remove the cause of the loading error (for Example, (a) improper cam position, (b) disconnected belt, (c) mech-drive circuit error, etc.) and then turn on MAIN POWER at the rear.

6-6-2 REEL STOP

In a mode where the reel rotates (i.e., FF, REW, PLAY, REC, CUE or REVIEW), if the rising edge of the reel pulse is not encountered within a certain period of time, the reel is assumed not rotating and the operation proceeds to the STOP mode.

The rising edge must be encountered at least once in:
- 0.1 s . . . . . FF/REW
- 0.3 s . . . . . CUE/REVW
- 1.3 s . . . . . PLAY/REC

The revolution of the take-up reel is transmitted via the belt and the pulse is generated by means of a photo-interrupter.

Note that this applies only to the take-up reel; that is the "supply" reel is not monitored.

6-6-3 DRUM STOP

In a mode in which the drum motor rotates (PAUSE to PLAY), if the rising edge of SWP (switching pulse) is not encountered at least once in 0.5 s, the drum is assumed not rotating, and the operation proceeds to the STOP mode.

This also applies where SWP is not at the specified level (H . . . . . 2.0V or more; L . . . . . 0.8V or less) even though the drum is revolving.

6-6-4 DETECTION OF LAMP FAILURE (ITS OMISSION)

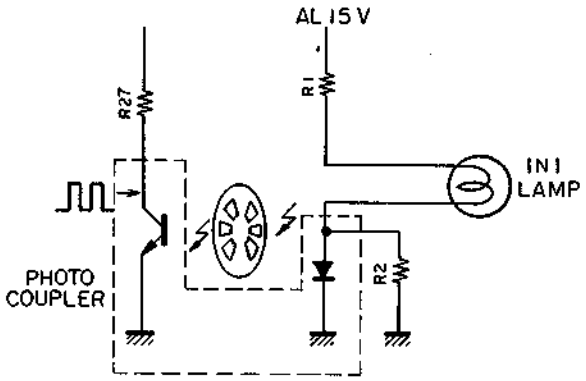


Fig. 7-109 Reel pulse Generation Circuit

Lamp failure needs to be detected when the tape is running, during which time the reel pulse is always detected.

Lamp failure brings a problem only when the tape is pulled excessively near its end or when it broken while it is running.

Detection of the reel pulse involves a delay in each mode. Therefore, in the event of lamp failure, this delay causes the tape to be pulled near its end. This pull is about 500g (based on calculation), while the tape is designed to withstand a pull of 3 kg. This, together with the fact that lamp failure rarely occurs, makes it possible to omit the operation that is concerned with detection of lamp failure.

As shown in Fig. 7-109, the lamp is connected in series with LED used for reel pulse detection, and thus the reel pulse is cut off in the event of lamp failure.

7. AUDIO/VIDEO PRE-AMP CIRCUIT

7-1 AUDIO CIRCUIT

7-1-1 RECORDING SYSTEM

Audio signals from the built-in tuner or from the line input are supplied to the connector P5 pin (2). When a DIN connecter is connected, the line takes preference. The input level of the audio input signal is adjusted at the Automatic Level Control (ALC), the DC component is removed by C1, and the rest is fed to IC1 (BA 5102) pin (18). The signal is amplified at the AMP by about 37 dB, output to pin (4) via the electronic switch SW1, enters pin (9), passes through electronic switch SW2, is amplified by about 30 dB at the line amplifier, and output to pin (10).

The output at pin (10) is divided as follows:

1) The output is subjected to negative feedback to the line amp from pin (7) via C3.

2) The signal has its component removed by C20, is rectified by D1, smoothed by C24 and fed to ALC between pin (16) and pin (17) to provide level control.

3) The signal is fed to AUDIO OUT of connector P5 pin (4) as an EE output via C18.

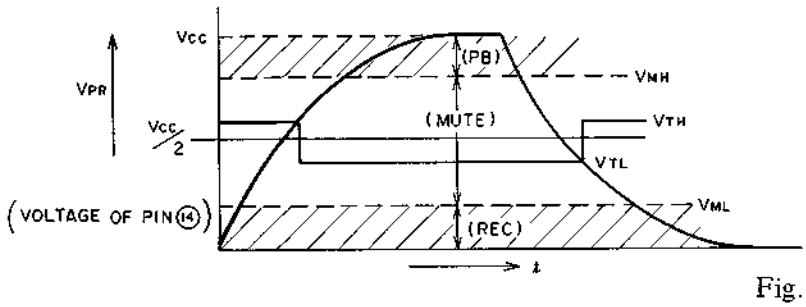
4) In parallel with this, the signal is subjected to the level adjustment at VR3 (REC LEVEL), fed to IC1 pin (12), and supplied to the REC AMP.

The REC AMP perfoms peaking by means of R16, L3, and C17, to compensate for the loss of high frequency components during recording/and playback of magnetic tape, so as to supply constant recording current to the head regardless of the signal frequency, and the bias current is supplied to the head. The DC component is removed by C22.

7-1-2 PLAYBACK SYSTEM

The signal reproduced from the tape by the audio head is fed to connector P3 pin (3), fed to IC1 pin (2), passes through EQ AMP, and SW1, and is output to pin (4). This signal is subjected to level adjustment at VR2 (PB LEVEL), fed to pin (8), passes through SW2 and LINE AMP, is output to pin (10), and passes through C18. One output is supplied to LINE OUT as AUDIO OUT, and the other is fed to the RF converter.

7-1-3 LOGIC CONTROL



$V_{P/R}$	MUTE	P.B/REC
$V_{CC} \sim V_{MH}$	OFF	P.B
$V_{MH} \sim V_{TH}$	ON	P.B
$V_{TH} \sim V_{TL}$	ON	P.B REC
$V_{TL} \sim V_{ML}$	ON	REC
$V_{ML} \sim 0$	OFF	REC

Fig. 7-110 Operation of Logic Control

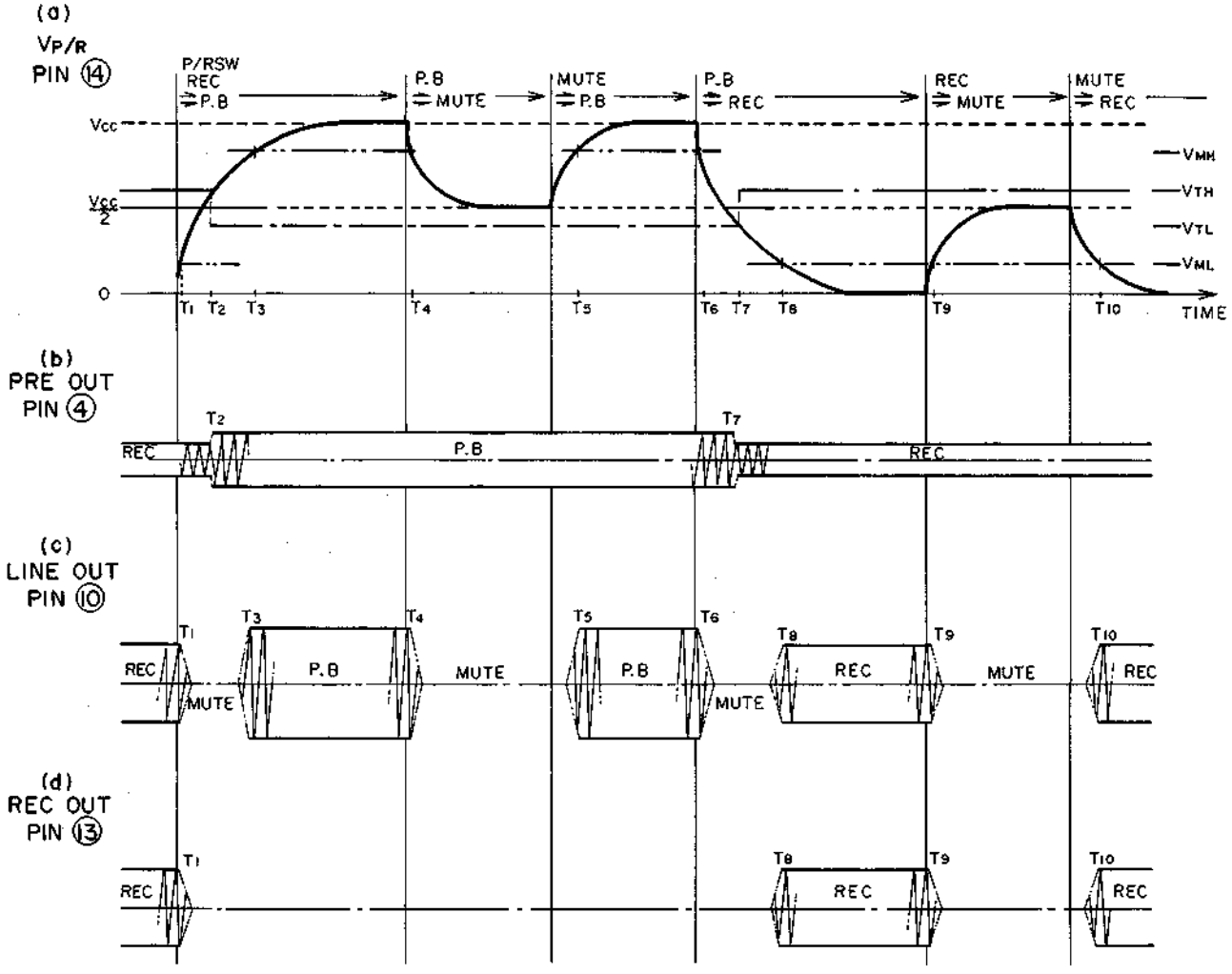


Fig. 7-111 Operation of Muting Control

IC1 (BA5102) used in this circuit employs an Electronic Switch (E. SW) so that the same circuits may be used for the Record and Playback circuitry.

The switching terminal is controlled by a voltage applied to pin ⑭. Switching to REC mode is made on LOW voltage input, switching to PB mode is made on HIGH voltage input, and switching to PB MUTE mode is made on MIDDLE voltage input.

Fig. 7-111 shows the timing chart during transfers between REC and PB modes. As seen from (a) pin ⑭ and (c) LINE OUT, when REC is switched to PB, the condition at time T3 is HIGH voltage, so that the PB audio signal is connected to the output. Then, as PB is switched to MUTE, MUTE is applied at time position T4. Though switching from normal PB to Muting is instantly accomplished, when returning from MUTE (STILL or QUICK FINDER mode) to normal PB, the audio signal is connected to the output after the tape run becomes stable, with the time constant arranged slightly longer than this to ensure reliable operation.

7-2 VIDEO PRE-AMP CIRCUIT

7-2-1 RECORDING SYSTEM

The recording signal consisting of a mixture of the FM signal from video PCB and the low band converted colour signal, is fed to connector P1 pin (5). This recording signal passes through the emitter follower (EF) of TR10, and is fed to REC AMP (TR8, TR9) (Audio/Pre PC Board) . This REC AMP operates to optimize the recording current for all signal frequencies.
The recording signal is fed to the video heads 1 and 2, and recorded on the tape.

7-2-2 PLAYBACK SYSTEM

PB signals from the video heads 1 and 2 are fed to IC2 (AN6320N) pins (3) and (5) respectively on the Audio/Pre PC Board, and then amplified at the 1st AMP.
Signals at the video heads 1 and 2 are extracted by the Switching Pulse supplied to pin (12), and output from pins (13) and (9) repsectively.
Then, the signals are fed to pin (11), made into a continuous signal by the MIX AMP, and output to pin (10).
Then, the signal is passes through the EF TR7, and supplied to the video PCB through connector P1 pin (3) (PRE-OUT).

1) Switching operation

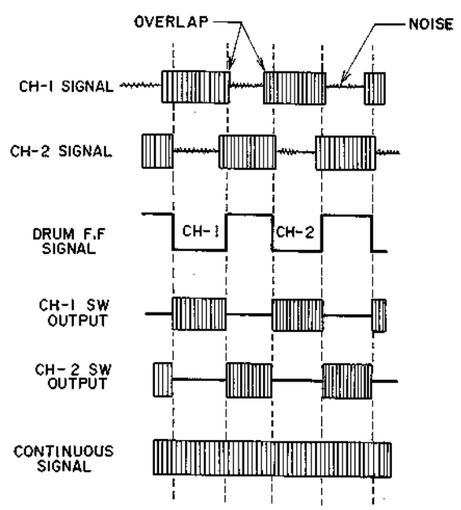
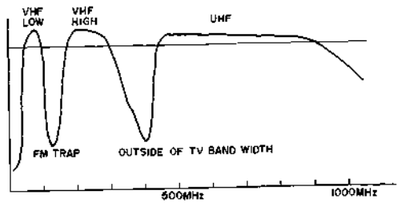


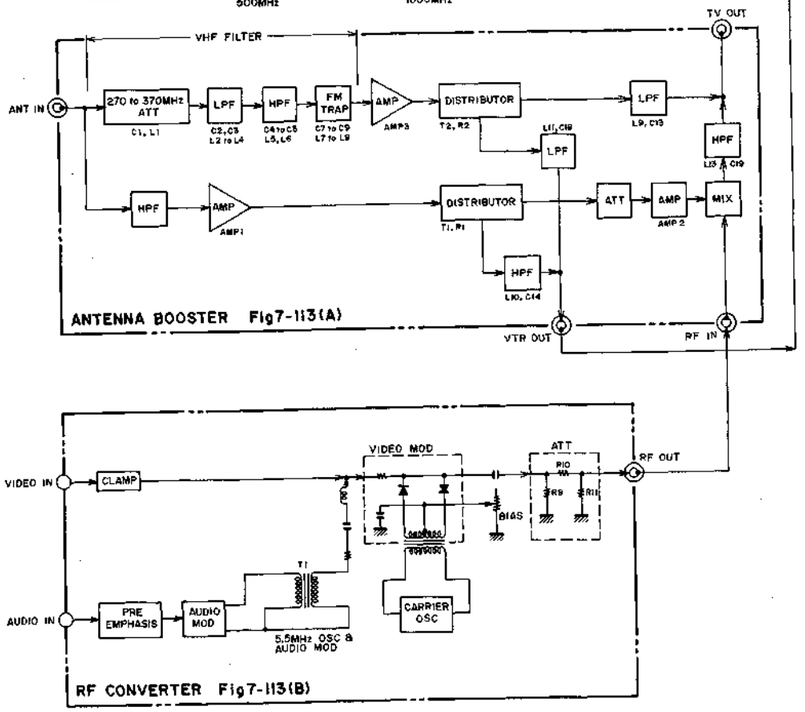
Fig. 7-112 Switching Operation

PB signals from the video heads 1 and 2 alternate every 180° of the 25 Hz switching pulse.
The times during which there is no PB signal contain noise, and so the channels are overlapped to avoid gaps in picture reproduction. Accordingly, Video heads 1 and 2 cannot be mixed simply. For this reason, the PB signals are switched by the 25 Hz drum flip-flop to form a continuous PB signal. Refer to Fig. 7-112.

8. BOOSTER CIRCUIT

Fig7-114 Filter Characteristics





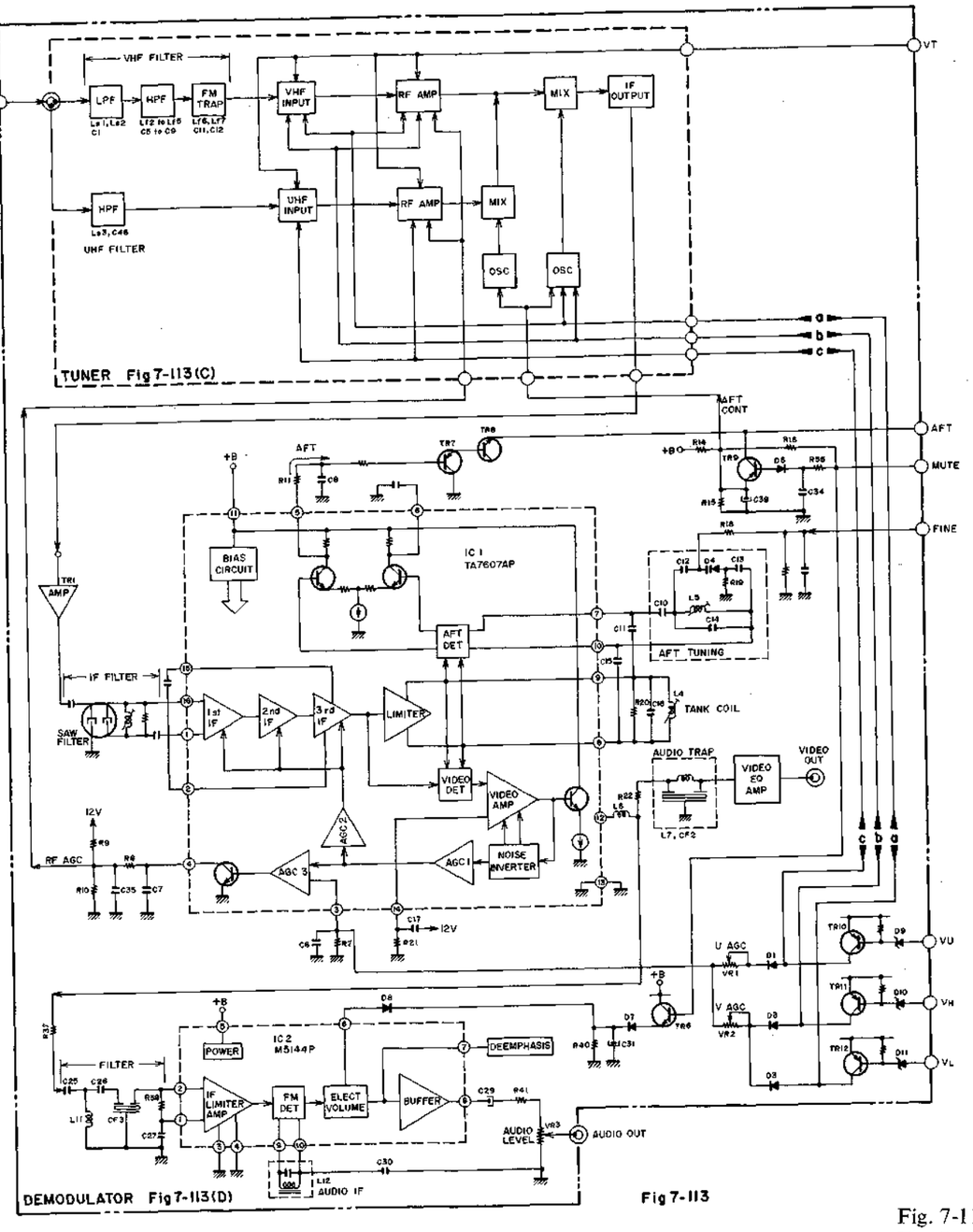


Fig7-113

Fig. 7-113
Fig. 7-114

The signal flow in the booster circuit is as shown in Fig. 7-113 (A). The composite TV signals having entered ANT IN, are separated into different bands by the UHF and VHF filters. The signals thus separated are distributed to VTR OUT and TV OUT passing through the respective special AMPs. The signal from the RF converter is fed to RF IN, combined with the UHF signal, and output to TV OUT. Adequate reverse isolation is provided by the attenuator and amplifier so that the converter output does not leak back into the ANT input side.

Now, the circuit will be described with reference to the block diagram.

The VHF and UHF filters are as shown in Fig. 7-113 (A), and the overall characteristics thereof are as shown in Fig. 7-114.

8-1 DISTRIBUTING/COMBINING

The distributor/combiner circuit is as shown in Fig. 7-115.
When a 75 Ω load is applied to outputs 1 and 2, the impedance viewed from the input side becomes 75Ω, and the signal can be distributed without any matching loss. Combining is just the reverse, and impedance viewed from each of the output terminals 1 and 2 is designed to be 75Ω, without any transmission between them.

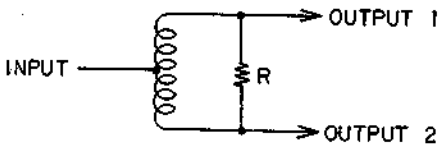


Fig. 7-115 Distributor/Combiner Circuit

8-2 LPF AND HPF

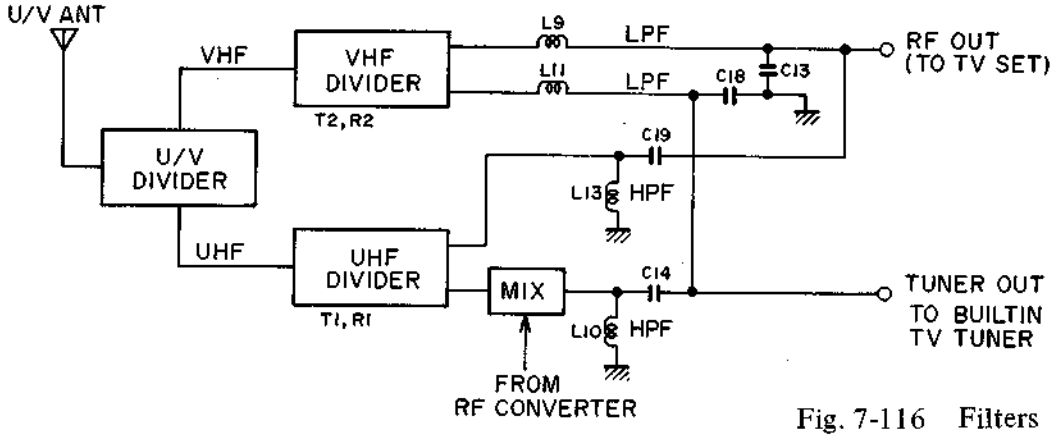


Fig. 7-116 Filters

The distributor/combiner circuit is shown in Fig. 7-Tuner) terminals are provided with a LPF (VHF) and a HPF (UHF) respectively to prevent VHF output and UHF output from being affected by presence of the UHF amp and VHF amp respectively. Refer to Fig. 7-116.

9. RF CONVERTER FUNCTIONS AND CIRCUITS

The RF converter is for modulating video and audio signals to obtain an RF signal within the TV UHF Band between channels 30 and 39, in the case of PAL SECAM.

The circuit will be described with reference to Fig. 7-113 (B). The actual RF converter circuit is an IC except for the carrier oscillator and the balanced modulator. The operation in the IC is described in the section dealing with the discrete circuit.

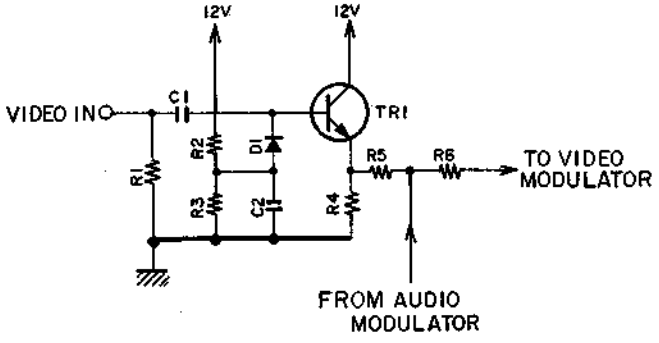


Fig. 7-117 Clamp Circuit

9-1 CLAMP CIRCUIT

The clamp circuit is for regulating the leading edge of the SYNC signal which is the reference level of modulation to be used as a fixed level before the input video signal is modulated. By applying the voltage split provided by R2 and R3 to the base of transistor TR1 via D1, the leading edge of the SYNC signal is clamped to this voltage. TR1 is the emitter follower. The level of video/audio signal to be fed to the modulator is adjusted by R5 and R6.

9-2 VIDEO MODULATOR

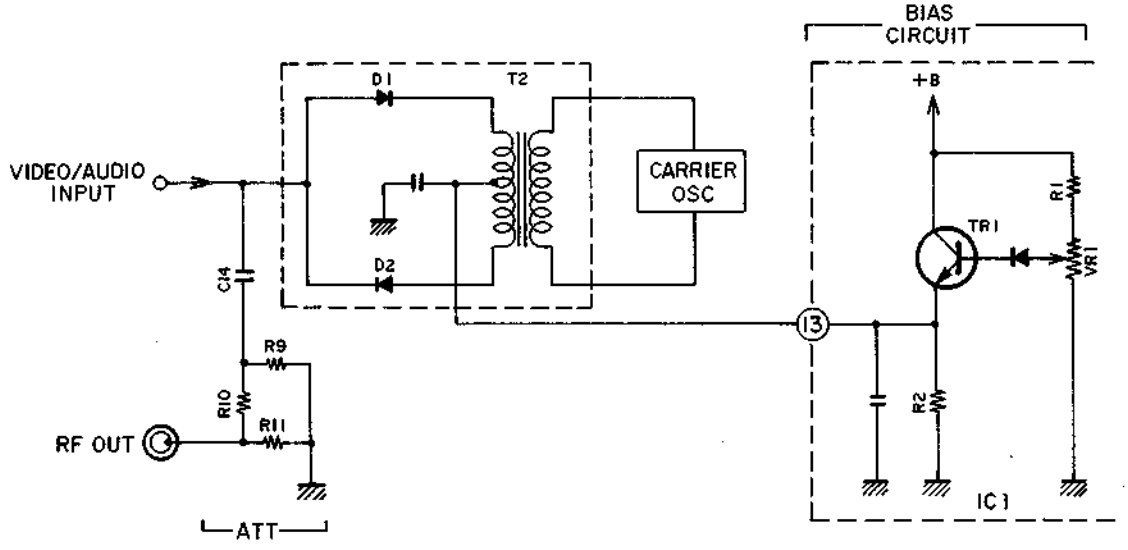


Fig. 7-118 Video Modulator

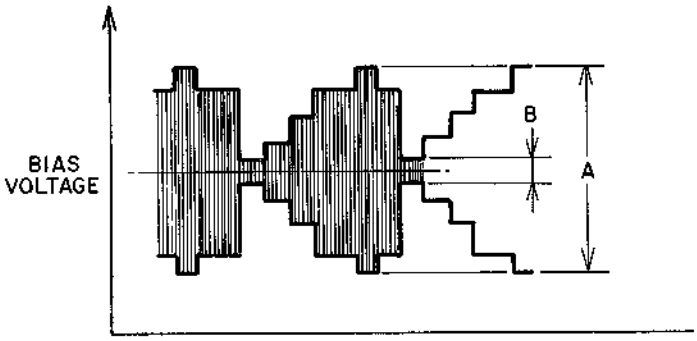


Fig. 7-119

In Fig. 7-118 the modulating circuit is enclosed in a broken line. This circuit is a balanced modulator. If the voltage applied from the bias circuit and the video input signal voltage are at the same level, the RF carrier output becomes zero. If they differ, the carrier output is proportional to the level difference.

In Fig. 7-119, the degree of modulation (M) is $M=\frac{A-B}{A+B}$.

As the bias voltage changes, the degree of modulation changes. (The degree of modulation can be changed by changing VR1).

In Fig. 7-118, C14 is for matching the impedance viewed from the input side. The pi (π) type attenuator (R9-11) is for adjusting the RF output level, and serves as a buffer for the modulator.

9-3 CARRIER OSCILLATOR

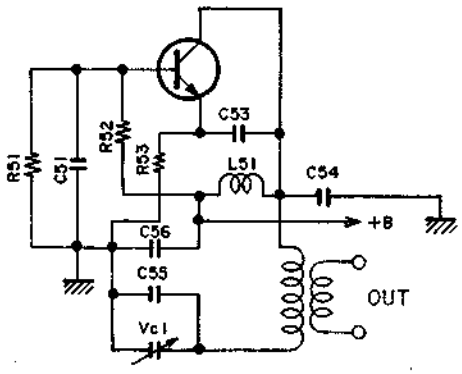


Fig. 7-120 Carrier Oscillator circuit

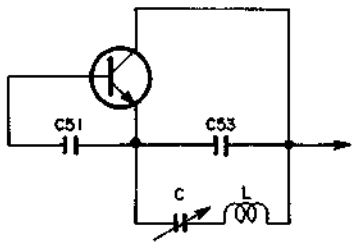


Fig. 7-121 Carrier OSC equivalent circuit

Fig. 7-120 shows the carrier OSC circuit. Fig. 7-121 is the equivalent circuit. Fig. 7-121 shows a collector tuning type OSC circuit. Oscillation frequency (fc) is $fc=\frac{1}{2\pi\sqrt{LC}}$. C represents a variable capacitor, and it can change the channel by changing its position in the frequency spectrum.

9-4 AUDIO MODULATOR CIRCUIT

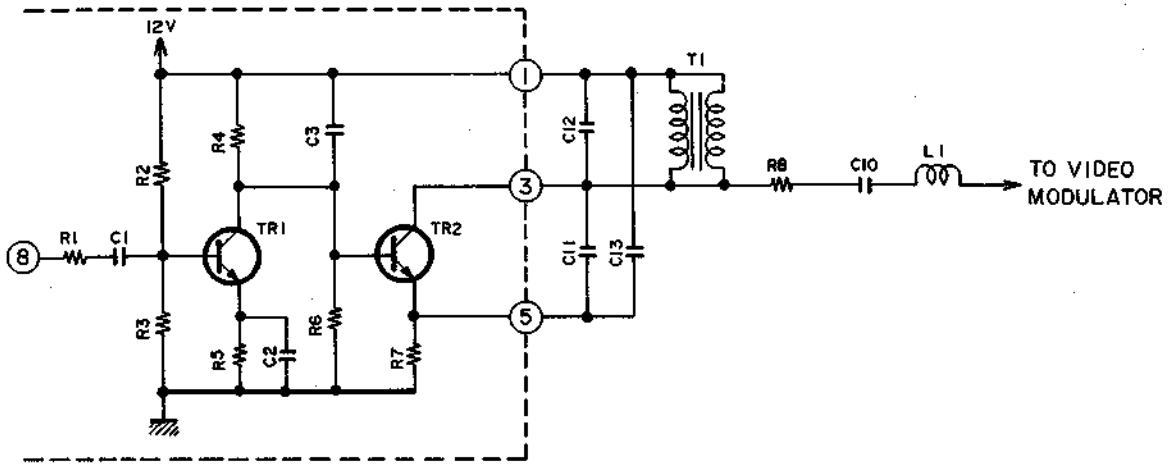


Fig. 7-122 Audio Modulator

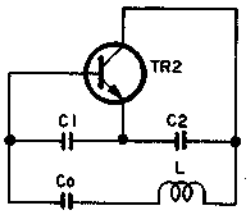
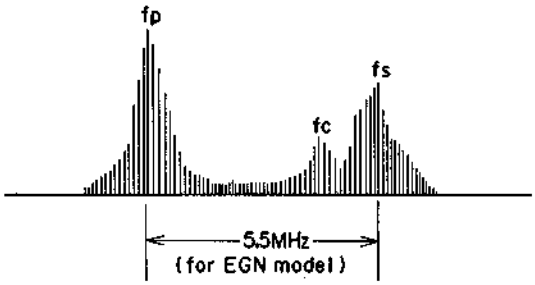


Fig. 7-123 Clapp OSC



fp = VIDEO CARRIER
fc = COLOR CARRIER
fs = AUDIO CARRIER

Fig. 7-124 RF output frequency spectrum

1) In Fig. 7-122, TR1 is AUDIO AMP, and 50 μs pre-emphasis is provided by R5 and C2.

2) TR2 is an oscillator transistor. Fig. 7-123 shows the equivalent circuit. This is a Clapp OSC. T1 of Fig. 7-122 corresponds to L of Fig. 7-123, and the sub-carrier frequency is adjusted by this component.

3) A sufficiently large audio signal is applied to the base of TR2 (base bias voltage). The base input capacity changes in proportion to the change in this voltage. As a result, the oscillation frequency of this circuit changes. Audio frequency modulation is performed based thereon. The center oscillation frequency is 5.5 MHz (in the case of EG and EGN models). Frequency is adjusted by T1 of Fig. 7-122.

4) The sub-carrier signal subjected to frequency modulation enters the video modulator, modulates the carrier together with the video signal, and becomes the RF output. Fig. 7-124 shows its frequency specturm.

10. TV TUNER (FRONT END) FUNCTIONS AND CIRCUITS

10-1 TUNER FUNCTIONS

1) The signal from the antenna is received with minimum loss.
2) Only required signals are selected and unwanted signals are removed.
3) The receiving channel is selected, and its band alone is amplified. This is called RF amplification.
4) The frequency band is converted to an easy-to-handle low frequency band. This low frequency (band) is called an intermediate frequency (band). (IF). A fixed frequency is defined in each country.

The above are the main functions of the tuner.
Sub-functions are as follows:

ⓐ The Automatic Gain Control (AGC) is provided to control the RF amplifier gain to keep the IF output level constant.

ⓑ The Automatic Fine Tuning (AFT) circuit is provided to keep constant the local oscillation frequency for IF frequency conversion.

10-2 CIRCUIT DESCRIPTION

The circuit will be described with reference to Fig. 7-113 (C). The VHF circuit will be mainly described, since the VHF and UHF circuits are basically the same. The VHF and UHF circuits differ greatly in that the VHF filter uses a discrete component configuration, while the UHF filter uses distributed component circuitry because of the high frequencies at which it operates.

10-2-1 FILTER CIRCUIT

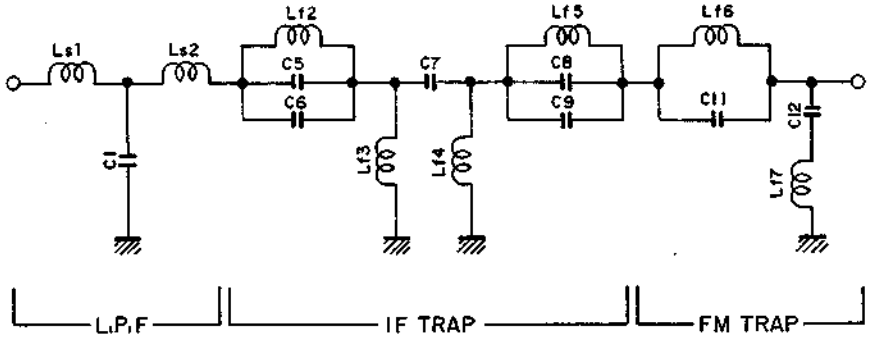


Fig. 7-125 VHF band filter circuit

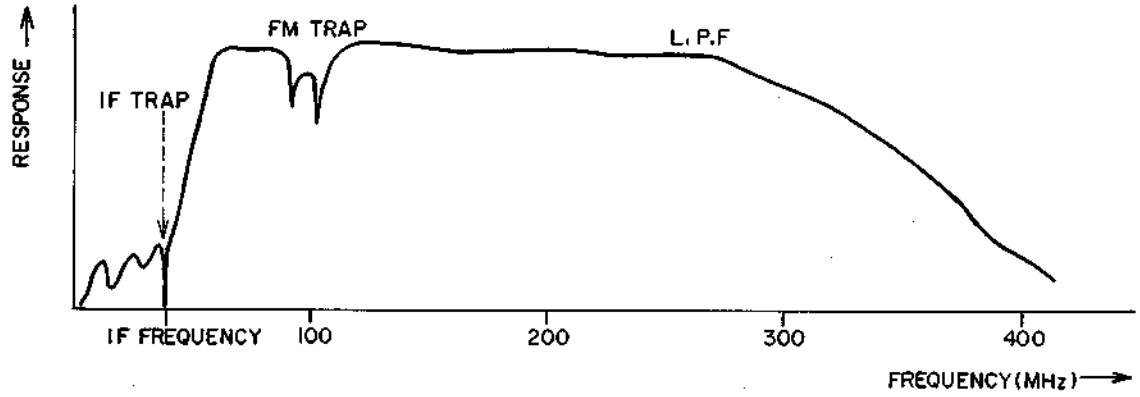


Fig. 7-126 VHF band filter characteristics

In Fig. 7-125, LS1, LS2, and C1 constitute the LPF for the UHF band. (In the UHF circuit, there is only an HPF for the VHF band, with no LPF and no trap circuit.)

Lf2–5 and C5–9 constitute an HPF for cutting off frequencies below the IF, and a trap is inserted at the IF frequency.
Lf6–7 and C11–12 constitute an FM trap. Refer to Fig. 7-126.

10-2-2 INPUT CIRCUIT

The input circuit consists of a single tuned circuit, and is provided to give good matching with the antenna as well as selectivity.
The following symptons indicate poor matching.

1) Ghose on the screen
If matching is poor, signal reflections occur at the antenna cable, which cuase delayed signals to enter the filter, causing ghosting. The delay depends on antenna cable length. VSWR (voltage standing wave ratio) is used for indicating the matching degree matching.
VSWR is expressed using the characteristic impedance of a line (Zo: which for a tuner is normally 75Ω) and the network input impedance (ZR) as follows:

$$VSWR = \frac{1 + \left(\frac{ZR - Zo}{ZR + Zo}\right)}{1 - \left(\frac{ZR - Zo}{ZR + Zo}\right)}$$

Matched condition: VSWR = 1 when ZR=Zo

2) When VSWR becomes poor, matching loss increases, and S/N performance on the screen becomes worse.

3) The VS-2EGN tuner input circuit is as shown in Fig. 7-127.

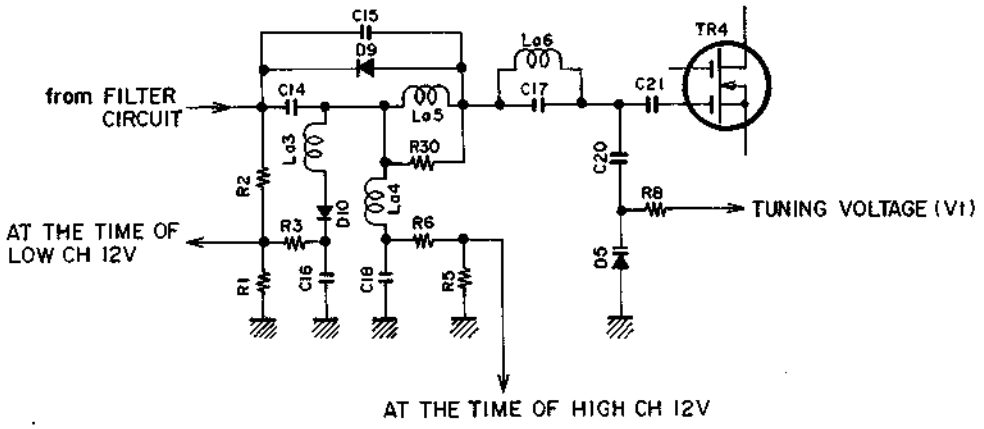


Fig. 7-127 Tuner input circuit

D9, D10 . . . . Switching diode
D5 . . . . . Vari-cap diode

ⓐ Fig. 7-128 shows those parts of the circuit related to HF signals, rewritten from Fig. 7-127.

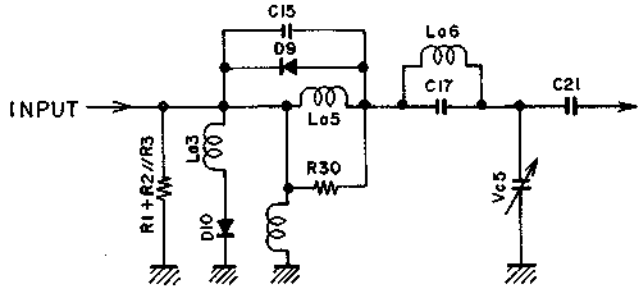


Fig. 7-128 HF signal related circuits

ⓑ Figs. 7-129 and 7-130 show the circuits effective during LOW-CH reception and HIGH-CH reception respectively.

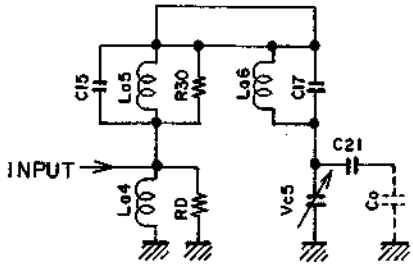


Fig. 7-129 Circuit during LOW-CH reception

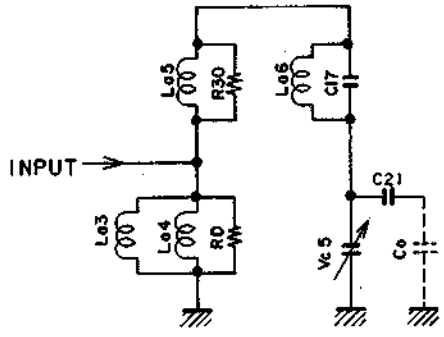


Fig. 7-130 Circuit HIGH-CH

RD: Damping resistor
Co: FET (TR4) input capacitance
*Channel is changed at Vc5.

© Fig. 7-131 shows the principle of the input circuit.

The tuned circuit has a tapped inductor and a tapped capacitor in order to obtain a high 'TR' and also to conveniently match the impedance of input and output.

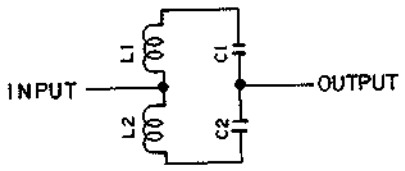


Fig. 7-131 Principle of input circuit

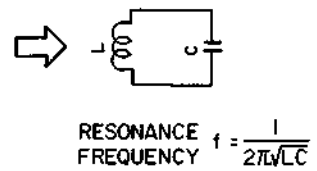


Fig. 7-132 Resonant circuit

Fig. 7-133 Frequency response

ⓓ The LOW-CH and HIGH-CH circuit configurations which are produced by the action of the switching diode are as shown in Figs. 7-129 and 7-130. During HIGH-CH reception, La4 is inserted in parallel with La3, to reduce the inductance and C15 is eliminated, so the capacitance is made smaller and a higher resonant frequency is achieved. Resistors R30 and RD inserted in parallel with La3 and La5 respectively are damping resistors for controlled damping of the circuit TR. When the TR is too high, variation of the frequency response characteristic between the channels becomes too large, and adjustment becomes difficult.

Circuit load TR can be expressed as follows:

$TR = \omega L/R$

where L=total inductance of the tuned circuit.

Response when there is no damping resistor.

Response when there is damping resistor.

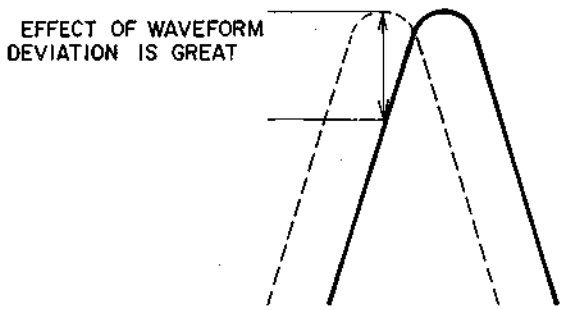


Fig. 7-134 High TR

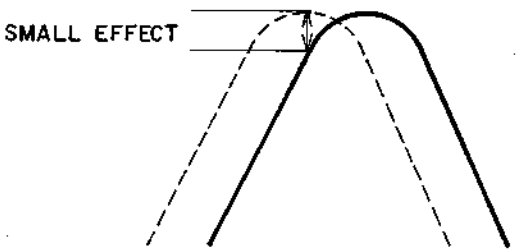


Fig. 7-135 Low TR

ⓔ Fig. 7-136 shows the IF trap characteristic (See Fig. 7-128).

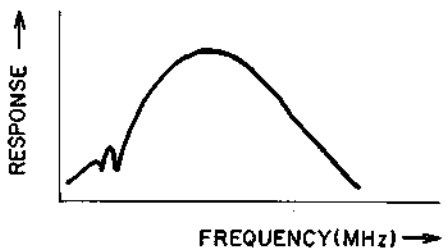


Fig. 7-136 IF trap characteristic

10-2-3 RF TUNING AMPLIFIER

The RF amplifier is a tuned amplifier having a double tuned circuit in its output stage. The frequency characteristic, gain, noise factor, and cross modulation of the tuner are almost completely determined here. Important points to note are as follows:

1) Cross modulation distortion
The received signal is modulated by other distortion components. This is called cross modulation distortion. This is generated from third order distortion components occurring in the RF transistor. This can be improved by using an FET with the optimum bias.

2) Noise figure (NF)
NF is indicative of the noise level generated by a transistor. The smaller the NF, the better the S/N ratio on the transistor output side. Since the NF is almost completely determined by the RF stage, it is necessary to use a transistor with a better NF and to obtain a sufficient gain at the same time.

3) Frequency response of tuned circuit.
Since the frequency characteristic of the tuner is almost completely determined by this circuit, sufficient bandwidth and flatness between fp (video carrier) and fs (audio carrier) are essential. When the response of this circuit is poor, the frequency response after video detection becomes worse, picture quality is affected, and the selectivity falls.

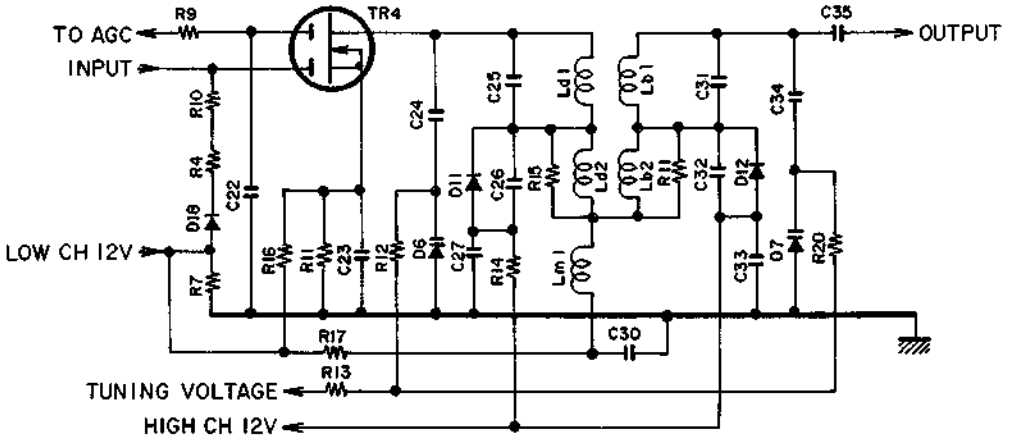


Fig. 7-137 RF tuned amplifier

4) Fig. 7-137 shows the RF tuned amplifier.
ⓐ Referring to Fig. 7-137, TR4 is an RF FET amplifier with a grounded input on the first gate.
An AGC voltage is applied to the second gate. By changing the bias, the gain is changed. Amplification the highest when the output circuit is tuned, and only a specified frequency band is amplified, which depends on the characteristic of the tuned circuit.

ⓑ HF related components in the tuned circuit.
Fig. 7-138 shows mutual inductance coupled double tuned circuit. The primary and the secondary tuned circuits are coupled by mutual inductance. The two tuned circuits are symmetrical. When receiving a HIGH-CH signal, D11 and D12 conduct so that C26, R15, Ld2, Lm1, Lb2, R18 and C32 are shorted, and both the tuning capacitance and inductance become smaller. R15 and R18 are damping resistors which are only connected when LOW-CH signals are being received.

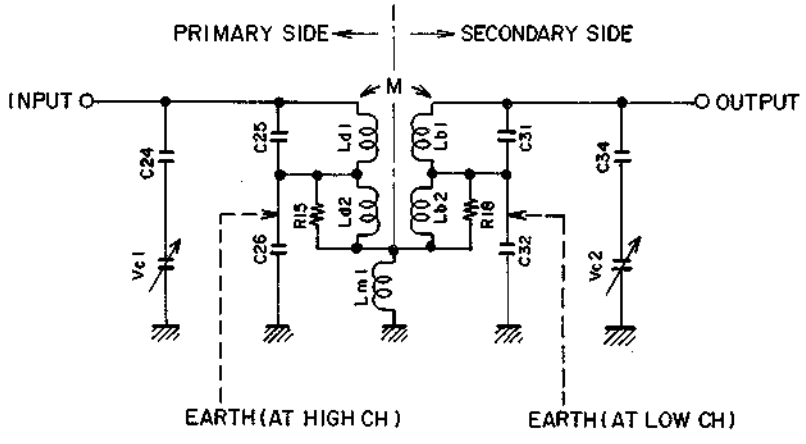


Fig. 7-138 HF related components in the tuned circuit

© Figs. 7-139 and 7-140 respectively, show the components connected into circuit during reception of LOW-CH and HIGH-CH signals.

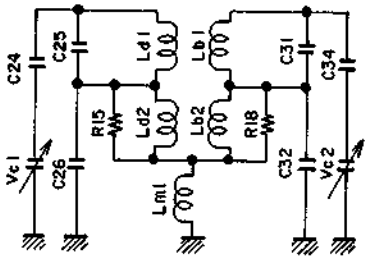


Fig. 7-139 Circuit configuration during LOW-CH reception

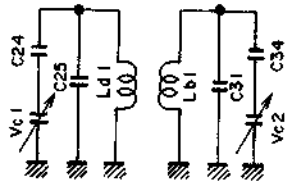


Fig. 7-140 Circuit configuration during HIGH-CH reception

ⓓ Both circuits of Figs. 7-139 and 7-140 can be represented by the equivalent circuit of Fig. 7-141.

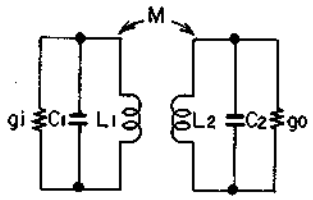


Fig. 7-141 Equivalent circuit of tuning circuit

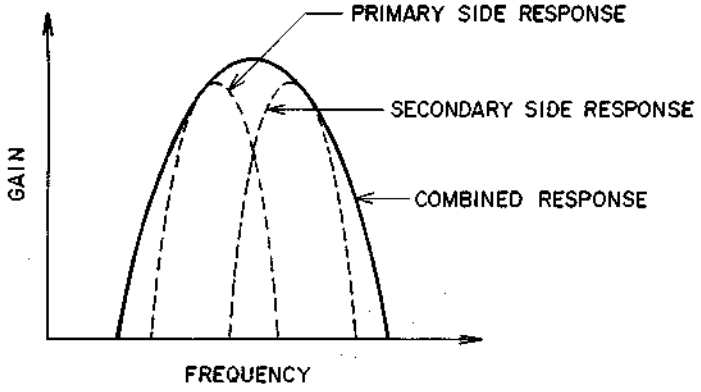


Fig. 7-142 Frequency response of double tuned circuit

gi = Primary side conductance including output conductance of RF transistor

go = Secondary side conductance including input conductance or mixer transistor

The circuit shown in Fig. 7-141 is a stagger tuned circuit. A double tuned circuit consists of primary and secondary resonant circuits with staggered resonant frequencies, which are coupled by mutual inductance. The frequency response is as shown in Fig. 7-142.

ⓔ For the adjustment of this response, mutual inductance and inductance are adjusted using Ld2 and Lb2 for LOW-CH, and Ld1 and Lb1 for HIGH-CH. The double tuned circuit is better than a single tuned circuit because the selectivity is good and flatness in the frequency band can be obtained.

10-2-4 LOCAL OSCILLATOR

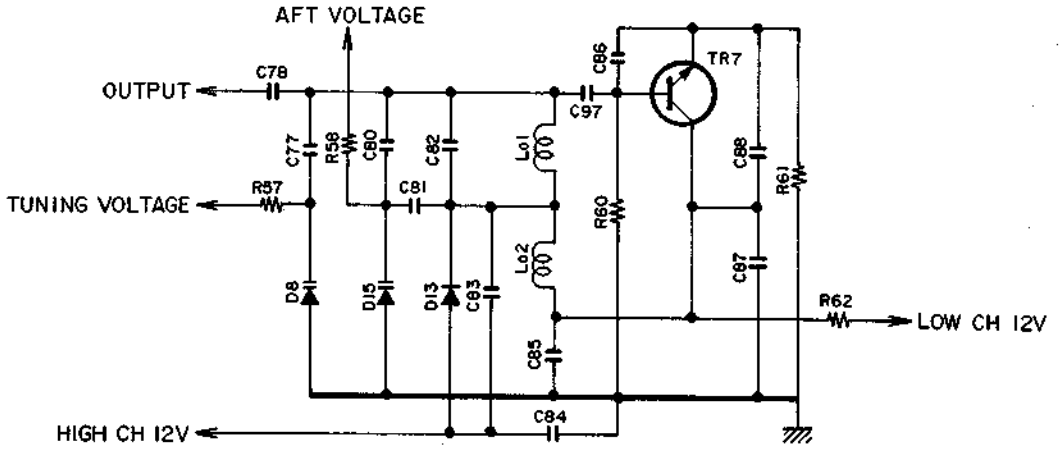


Fig. 7-143 Tuner oscillator

1) The local oscillator oscillates at a frequency is higher than the received signal frequency by an amount equal to the IF frequency. This system is called the upper supertheterodyne system, and the following relation exists.

$fo = fp + f_{IF}$

where fo = local oscillator frequency
fp = video frequency of received channel
f_{IF} = video IF frequency (5.5 MHz)

2) Important requirements of the tuner local oscillator are as follows:

ⓐ Oscillation frequency is stable. It should not deviate beyond the AFT locking range.

ⓑ Oscillator output is sufficient without affecting the oscillator frequency stability.

3) Fig. 7-143 shows the oscillator.
D13 is a switching diode, which conducts when HIGH-CH signals are selected C83, L02, and C85 are then shorted to earth. As a result, both inductance and capacitance are decreased, which raises the tuned frequency to a higher value.

4) Fig. 7-144 shows the tuner oscillator excluding the bias circuit and switching circuit of Fig. 7-143, during LOW-CH reception.
Fig. 7-145 shows the circuit during HIGH-CH reception.

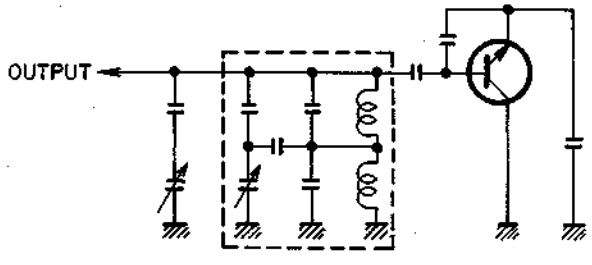


Fig. 7-144 The circuit components specific to the LOW-CH are enclosed in a broken line

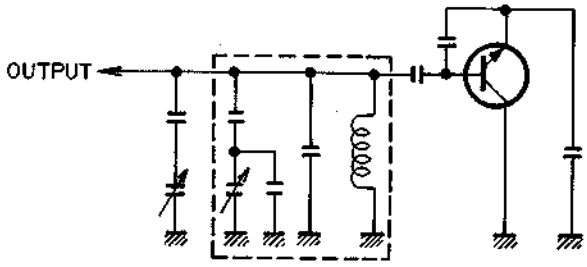


Fig. 7-145 The circuit components specific to the HIGH-CH are enclosed in a broken line

5) Fig. 7-144 can be redrawn in a simplified from as Fig. 7-146.

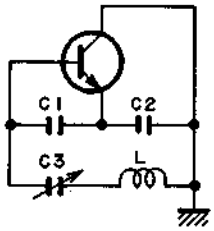


Fig. 7-146 Clapp Oscillator

Fig. 7-146 shows a Clapp oscillator. Its oscillation frequency is highly stable. The oscillator frequency is adjusted by the variable capacitance diode D8 of Fig. 7-143. D15 is a variable capacitance diode for AFT. This corresponds to varying C3 of Fig. 7-146. The oscillation frequency of this circuit is $fo = \frac{1}{2\pi\sqrt{LC_3}}$

The capacitance of C3 is the total capacitance of C77, C80, C81–83, D8, and D15. At the time of manufacture, the frequency is adjusted using Lo1 and Lo2.

10-2-5 MIXER CIRCUIT

1) The mixer circuit is for obtaining sum and difference components by applying the received channel signal and the local oscillator frequency to the semiconductor which is a non-linear element.

2) Key requirements of the mixer circuit
The voltage to be supplied from the local oscillator shall be sufficiently large compared to the receiving signal voltage. When it is insufficient, the oscillation frequency may vary when there is a large signal input.

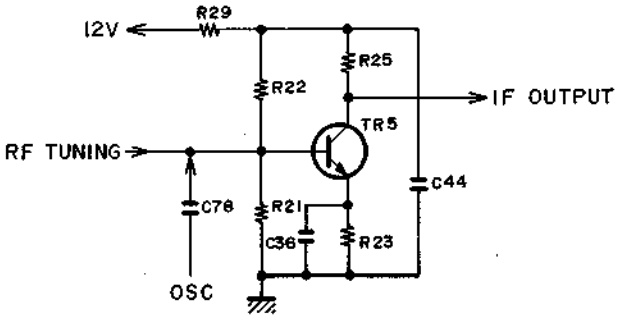


Fig. 7-147 Mixer circuit

In Fig. 7-147, when a voltage of a large amplitude is fed to the base of the transistor TR5 from the local oscillator through the injection capacitor C78, the transistor operation is non-linear. When the received signal applied to the mixer is very small, sum and difference components are generated, amplified, and picked up as the collector output. The desired frequency band only emerges from the subsequent IF tuned circuit.

10-2-6 IF OUTPUT CIRCUIT

1) The IF output circuit is a single tuned circuit for selecting f_{IF}=fo–fp from fo±fp generated by the mixer circuit.

2) Fig. 7-148 shows the IF output circuit (mixer transistor is included).
In Fig. 7-148, TR5 and TR6 are cascade-connected to avoid a low impedance as viewed from the mixer input at the base of TR5. The output side of TR6 has a single tuned circuit, and the output impedance is 75Ω.

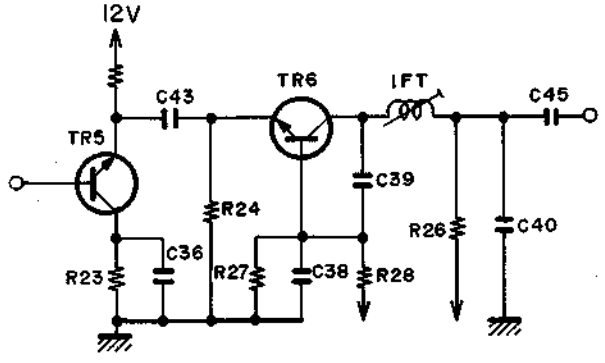


Fig. 7-148 IF output circuit

3) Fig. 7-149 shows the equivalent circuit of the IF output circuit. Fig. 7-150 shows IF response.

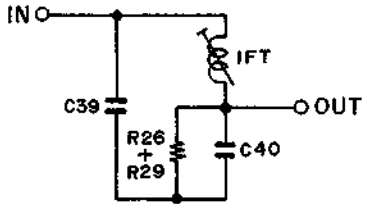


Fig. 7-149

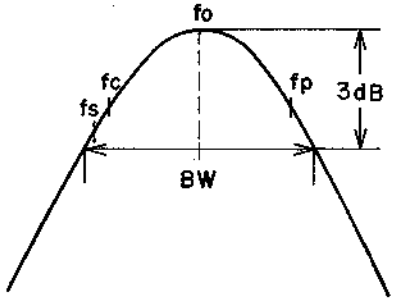


Fig. 7-150

Resonance frequency $fo = \frac{1}{2\pi\sqrt{L_{IFT}(C39 + C40)}}$

–3 dB band width is as follows:

$BW = \frac{fo}{TR}$ $\qquad TR = \frac{\omega L_{IFT}}{R}$

where $\omega = 2\pi fo$

R=value when damping resistor is made by (R26+ R29)

This IF response becomes the overall response of the tuner.

4) Fig. 7-151 shows an example of the standard quality of IF response.

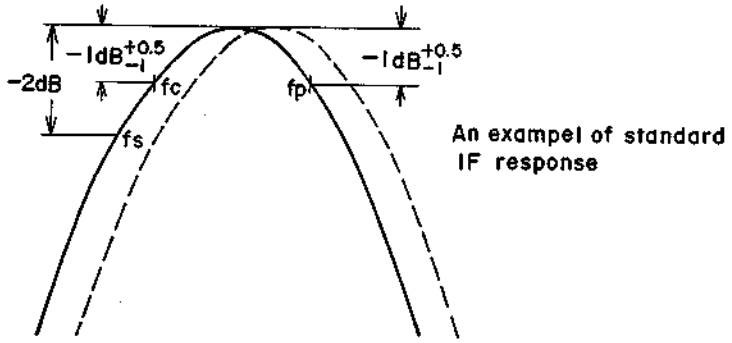


Fig. 7-151 An example of the standard quality of IF response

IF response is defined by the level differences from the peak output of waveform. During the assembly with the IF PCB, the response waveform can be adjusted to some degree by the core of the IFT. (The center of the waveform becomes incorrect.)

10-2-7 UHF CIRCUIT

The UHF circuit is basically the same as the VHF circuit except that the former employs a distributed component circuit because of the high frequency.

1) Distributed component circuit
In case of these high frequencies, the coil for the tuned circuit cannot be made as a discrete component. Therefore, a transmission line resonant circuit is used.

ⓐ Symbols in circuit diagram

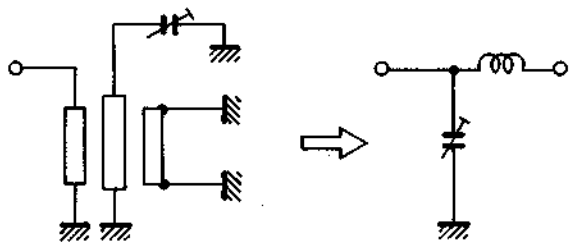


Fig. 7-152 Distributed component circuit

ⓑ In the construction as shown in Fig. 7-153, when the length ℓ is a quarter of the signal wavelength, impedance Zo becomes inductive, and line performs the same operation as a coil.

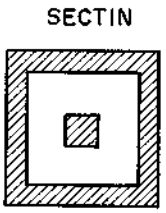


Fig. 7-153

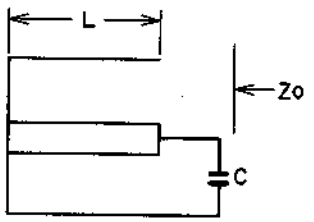


Fig. 7-154

2) Fig. 7-155 shows the equivalent circuit of the UHF tuner.

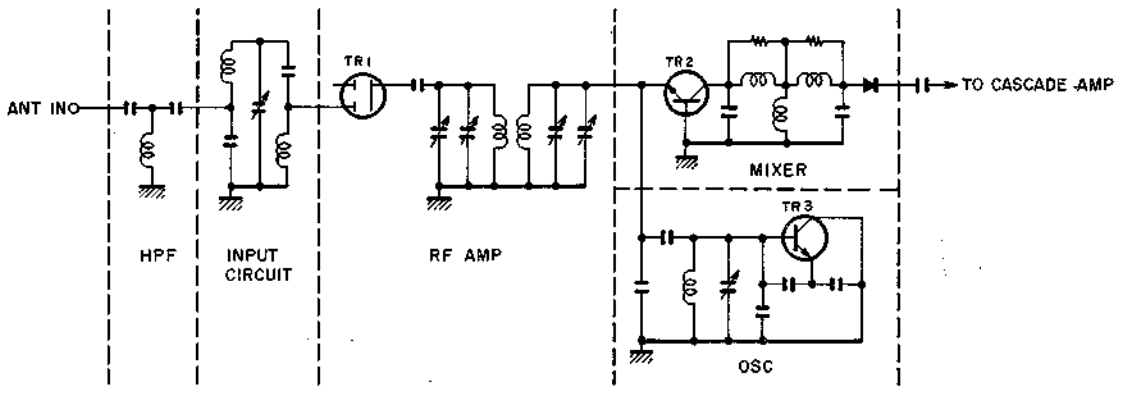


Fig. 7-155 UHF tuner equivalent circuit

11. DEMODULATOR FUNCTIONS AND CIRCUITS

11-1 DEMODULATOR FUNCTION

The demodulator described here is a front end tuner, and it amplifies the IF signal, and detects the video and audio signals separately.

11-2 DEMODULATOR CONFIGURATION

The demodulator consists of the following:
1) Filter circuit for determining the band width of the IF characteristic.
2) IF amplifier
3) Video signal detector
4) Audio signal detector
5) RF AGC voltage generator
6) AFT control voltage generator
7) Tuner band switching circuit

11-3 CIRCUITS

Circuits will be described with reference to Fig. 7-113.

11-3-1 IF FILTER CIRCUIT

Fig. 7-156 shows the IF filter circuit.

1) In Fig. 7-156, L1 and R44 form the input impedance for the tuner. L1 and R44 are in parallel as the load, together with some parasitic capacitance, and the impedance is about 70Ω. Coil L1 is inserted, because the IF output characteristic is affected when the load impedance for the tuner becomes capacitive.

2) C2 is a dc block and HPF, and C2 is HF FPF. TR1

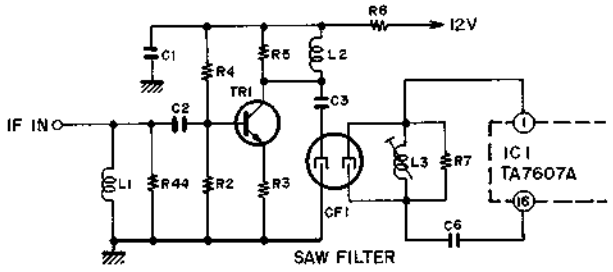


Fig. 7-156 IF filter circuit

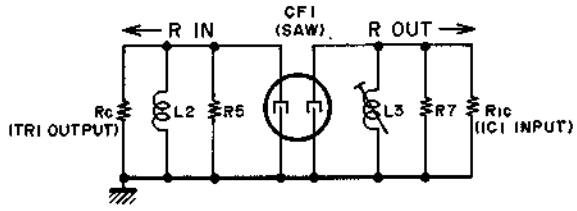


Fig. 7-157 Equivalent circuit of SAW filter

is an amplifier for compensating for the loss of the SAW (Surface Acoustic Wave) filter. Its gain is about 25 dB.

3) The SAW filter is a solid state element providing the desired frequency characteristic, and it requires no adjustment.

Fig. 7-156 shows the equivalent circuit relating to the SAW filter.

In Fig. 7-157, L2 is a coil for cancelling the SAW input capacitance while L3 is a coil for cancelling the output capacitance. Thus the internal capacitance of the SAW filter is cancelled, and impedance is made a pure resistance.

Input and output impedances viewed from the SAW filter are determined by R5 and R7, and mismatching loss is determined thereby. (Insertion loss is 22–23 dB)

4) Fig. 7-158 shows the frequency characteristic of the SAW filter.

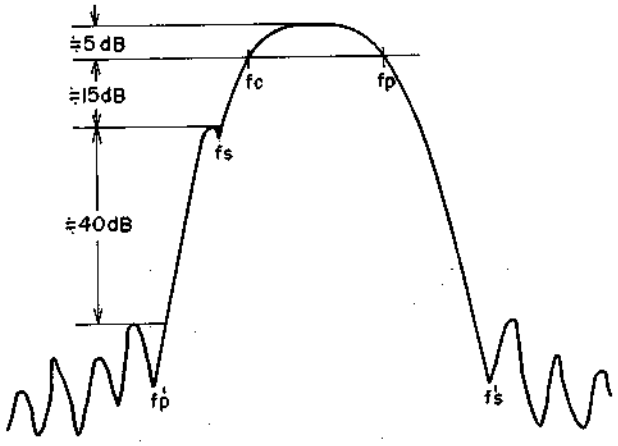


Fig. 7-158 SAW filter frequency characteristic

It is desired that the response between fp and fc is flat, but there is normally about 5 dB level difference between fp/fc and the peak. In addition, there is an audio trap, where the attenuation is about 15 dB.

fp' and fs' are video and audio traps of adjoining channels, where the attenuation is 40 dB or more.

11-3-2 VIDEO IF (VIF) IC AND PERIPHERAL CIRCUITS

IF signals having their characteristic determined by the SAW filter, enter VIF IC1 pins ① and ⑯, pass through the 3-stage VIF amp, are detected at the video detector, then are amplified, and output to pin ⑫ via the emitter follower. This IC has an AGC circuit for the gain control, and an AFT voltage generator for the control of the tuner local oscillator frequency.

1) Detector circuit

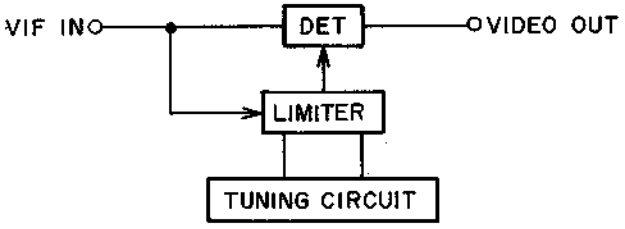


Fig. 7-159 LLD circuit composition

An LLD (Low Level Detector) is employed as the detector circuit (normally IC). Its feature is that a large video detection output can be obtained from a low level video IF input.

As shown in Fig. 7-159, the LLD consists of a limiter, a double balanced detector, and a tuned circuit.

2) Fig. 7-160 shows the limiter circuit, the IC part shows its equivalent circuit.

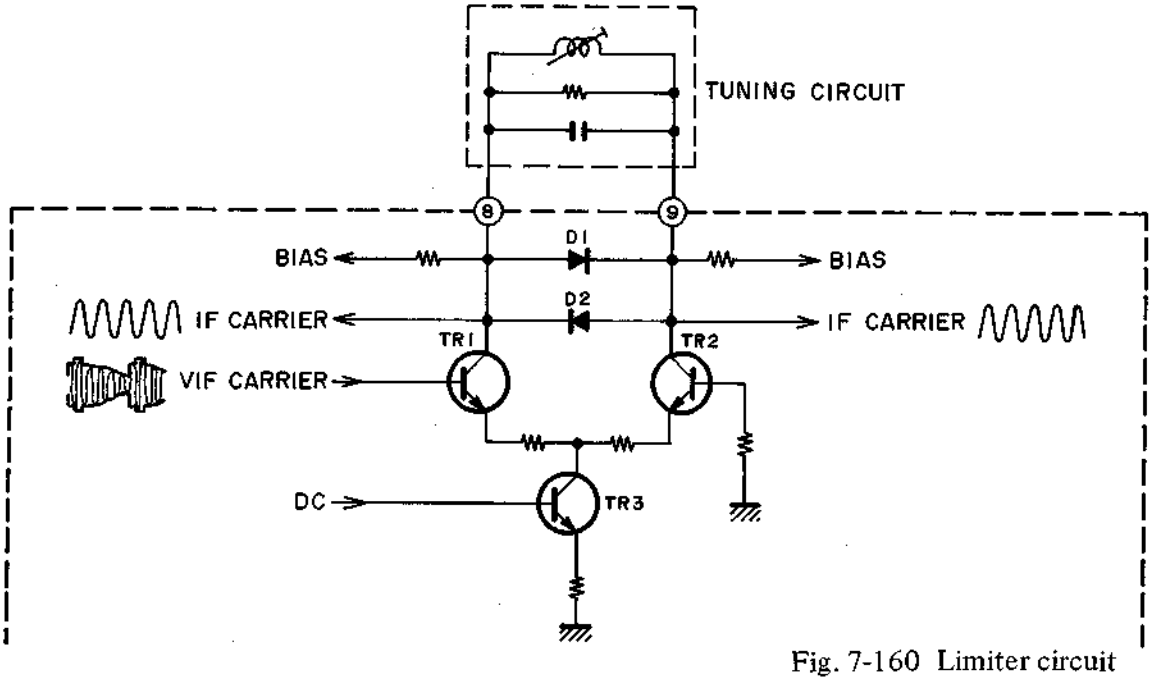


Fig. 7-160 Limiter circuit

Amplitude variations of the VIF are sliced off by the differential amplifier (TR1, TR2), and only the carrier is fed to the LC tuned circuit. The square wave is generated by clipping this carrier by D1 and D2.

The limiter circuit is made up of C16, L4, and R20 connected to IC1 pins ⑧ and ⑨ (Fig. 7-113(D)). Adjustment to the VIF frequency is made by adjusting L4. R20 is a damping resistor, and it is for reducing the TR of the tuned circuit. When the TR is too high, adjustment becomes difficult, and a slight deviation of VIF results in a large change in the detector output. A temperature compensating capacitor is used for C16.

3) Fig. 7-181 shows the double balanced detector.
(This is the basic circuit within the IC)

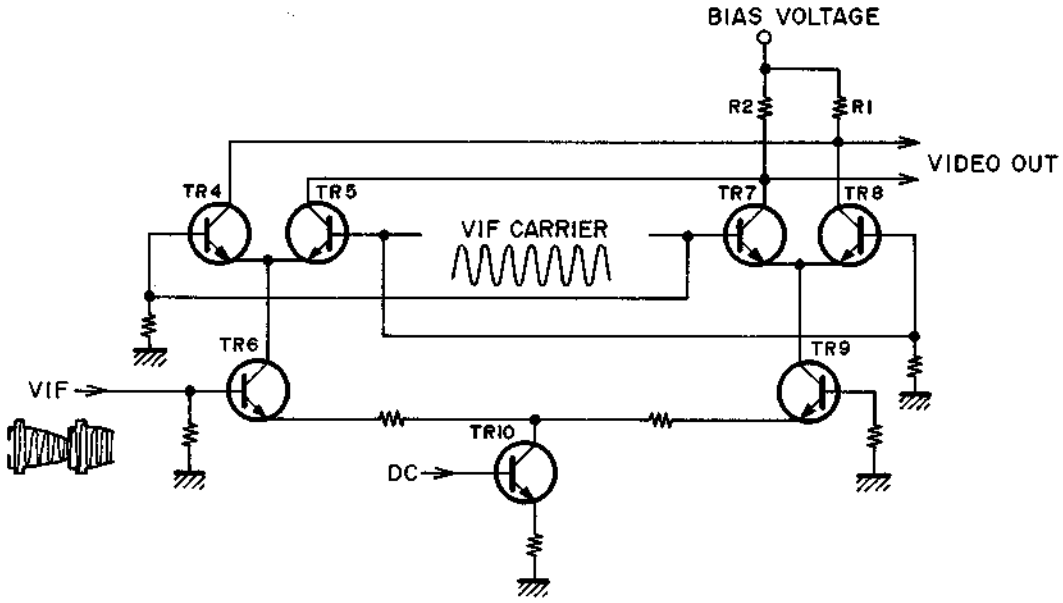


Fig. 7-161 Double balanced detector

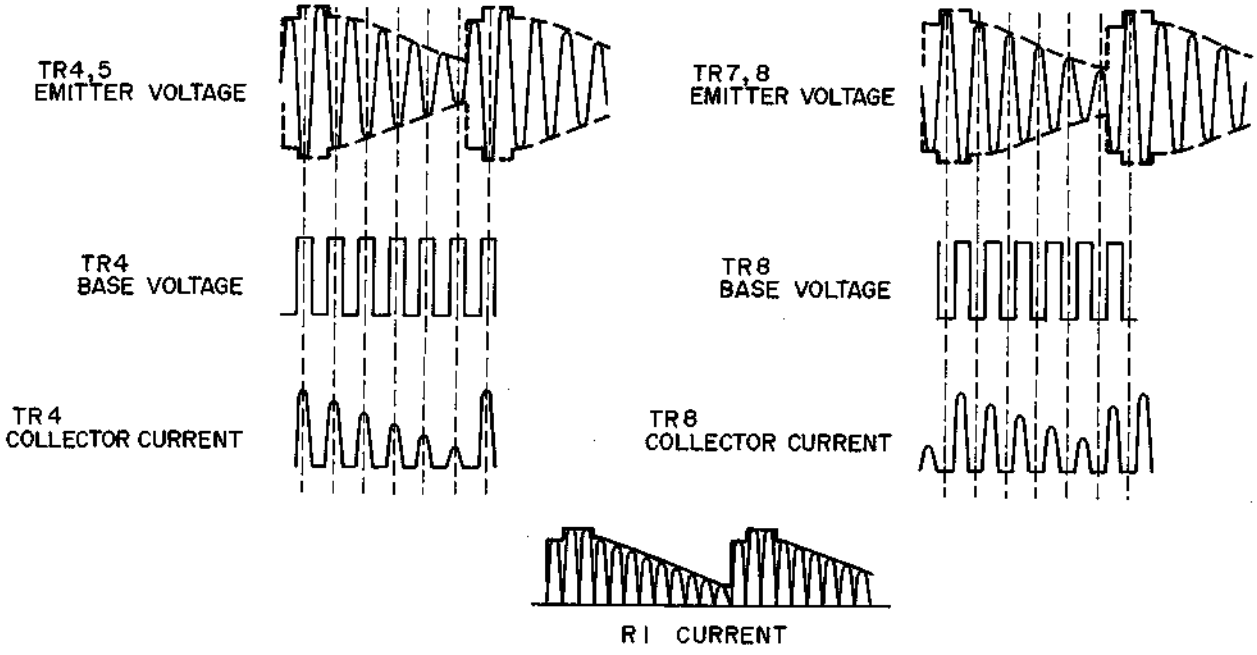


Fig. 7-162 VIF signal switching

When the carrier is fed to the bases of TR4 and TR8, switched VIF signals appear at the respective collectors (Fig. 7-162).
A VIF signal of positive only polarity, which is switched by TR4 and TR8 appears, and detected output is obtained at R1. (Detected output of negative polarity is obtained at R2). Since two pairs of transistors, TR6/TR9 and TR4/TR8 are employed for amplification, a large video detector output can be obtained for only a small VIF signal input.

11-3-3 AGC CIRCUIT

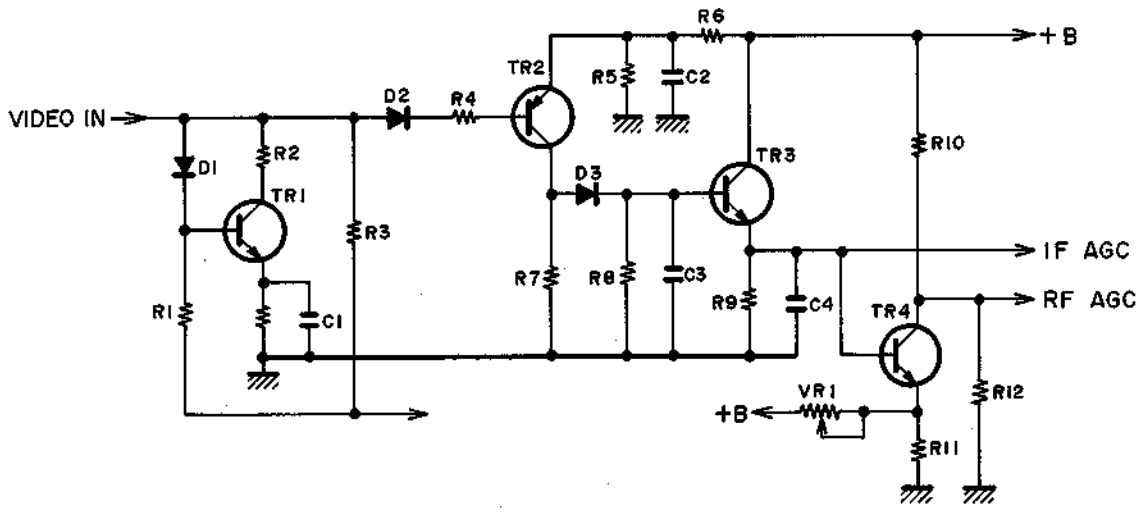


Fig. 7-163 An example of AGC circuit

1) Two AGCs are provided: one is for controlling RF amplifier gain of the tuner and the other is for controlling VIF amplifier gain. The former is RF AGC, and the latter is IF AGC.
This IC (TA7607AP) uses a peak value AGC circuit.
2) In the peak value AGC, gain is controlled by voltage proportional to the peak value of SYNC signal.
3).Fig. 7-113(D) shows the block diagram of the AGC circuit. (Bold line)
VIF gain is changed by controlling the collector current of the VIF transistor by the IF AGC voltage, and RF gain is changed by controlling the second gate of the tuner RF amp FET by the RF AGC voltage. The RF AGC is a delay type AGC designed so that it does not operate when the input is below a certain level.
4) The basic operation of the peak value AGC circuit will be described with reference to Fig. 7-163. (This AGC is within the IC.)
Since the peak value AGC is easily affected by noise, a noise canceller TR1 is provided. A video signal is fed to the base of TR1. When noise of a large negative amplitude is present here, the forward bias of TR1 is greatly reduced, and a noise of a large positive amplitude appears at the collector. Since this is superimposed on the video signal via R2, the noise is below the SYNC signal level. (Fig. 7-164)
5) Noise cancelled video signal of negative polarity is fed to the base of TR2, and a sync signal of positive polarity is picked up at the collector. The signal is detected at D3, passes through the integrating circuit (R8, C3), and is averaged. Then, an AGC control voltage is obtained via TR3.
In Fig. 7-113(D), this integrating circuit is represented by R1 and C17 (IF AGC filter).

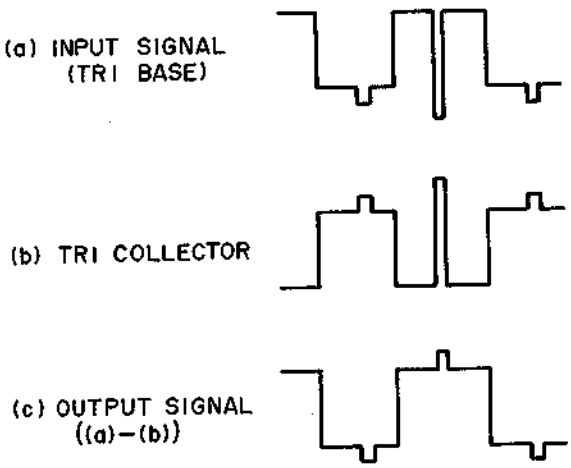


Fig. 7-164 Noise canceller I/O waveform

6) TR4 is a delay type RF AGC circuit. When the IF AGC voltage is lower than the emitter voltage, the transistor does not operate. The voltage is divided by R10 and R12, and the RF AGC voltage becomes constant. When the IF AGC voltage becomes higher than the emitter voltage as the input level rises, a collector current flows, the RF AGC voltage falls, and the RF amp gain is lowered accordingly.
7) R9 and R10 of Fig. 7-113(D) correspond to R10 and R12 of Fig. 7-172. There is shown in Fig. 7-113(D) a filter (C7, C35), which removes the ripple from the AGC voltage. (RF AGC filter)
The reason why VR4 and VR5 are adjusted for each channel band in Fig. 7-113(D) is that the tuner RF amplifier differs from VHF to UHF.

11-3-4 AFT CIRCUIT

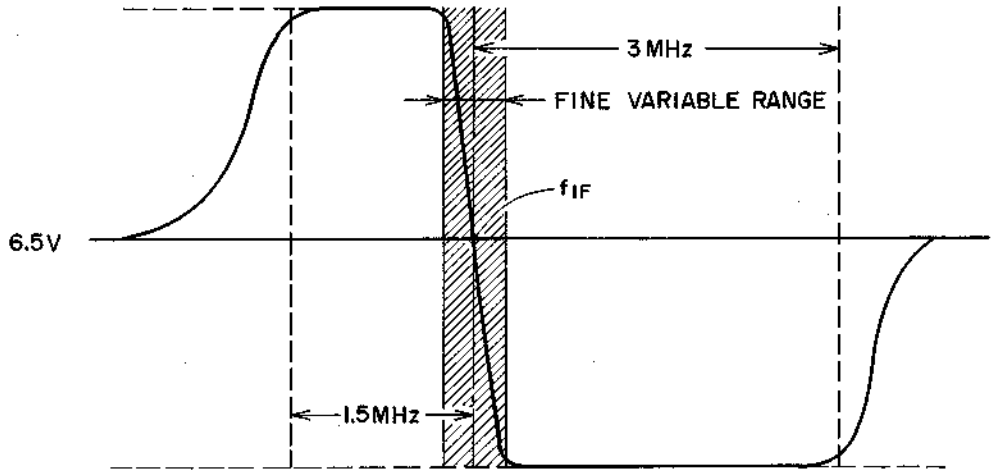


Fig. 7-165 AFT characteristic

The AFT (Automatic Fine Tuning) circuit is a circuit for the automatic control of local oscillator frequency by converting the frequency changes of the IF signal to DC voltage changes through FM detection and applying them to the variable capacitance diode of the tuner local oscillator.

1) Fig. 7-113(D) shows the AFT circuit configuration. The VIF carrier having passed through the limiter, enters the FM detector, which subjects it to frequency deviation detection, amplifies its DC output, and makes it an AFT control value on demand.

2) Carrier is fed to the AFT tuning circuit via C11 and C15, and then fed to the detector (IC).

3) The AFT tuning circuit consists of L5, C14, C10, and variable capacitance diode D4. Fine tuning in the AFT lead-in condition can be made by varying the capacitance of D4. The variable range is ±500 kHz with bias voltage at 6±3V.

Fig. 7-165 shows the AFT characteristic.

11-3-5 VIDEO EQUALIZER AND OUTPUT CIRCUIT

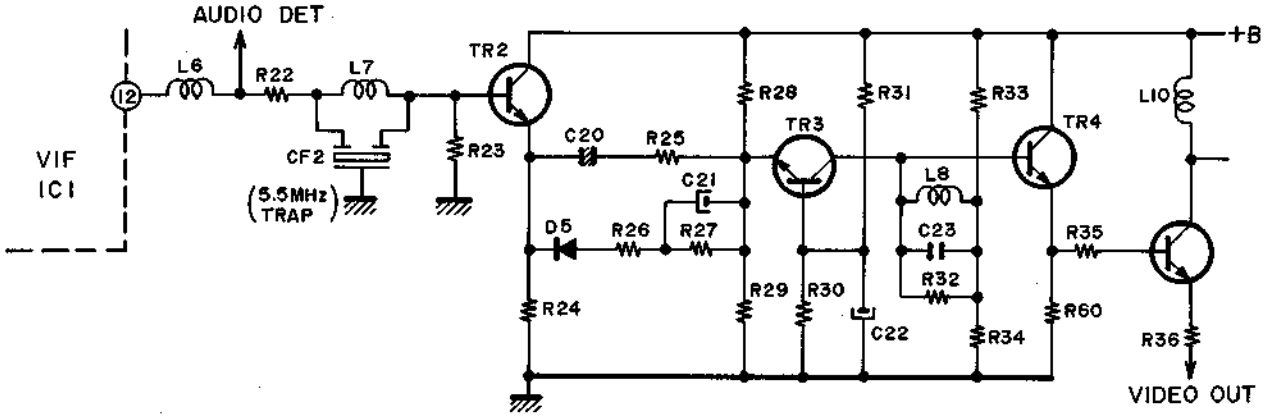


Fig. 7-166 Video equalizer and output circuit

1) L7 and CF2 (ceramic filter) forms a trap for the audio sub-carrier frequency, and the audio signal contained in the video signal is separated here, TR2 is an Emitter follower, and D5 is a diode for clamping the leading edge of the SYNC signal.

2) TR2 and TR3 are cascade-connected, to lower the AC load impedance, and improve the high band frequency characteristic.

3) Since the level around the CHROMA signal falls due to the audio trap, the high band is compensated for by the equalizer amp (TR3, R32, C23, L8). The resonant frequency of L8 and C23 is about 5.2 MHz, and the gain characteristic of the equalizer amplifier is as shown in Fig. 7-167.

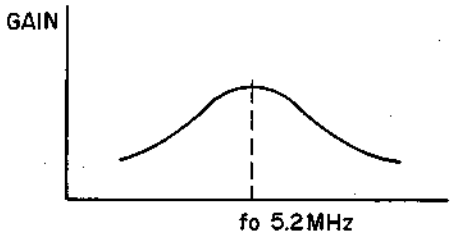


Fig. 7-167 Equalizer characteristic

11-3-6 AUDIO CIRCUIT

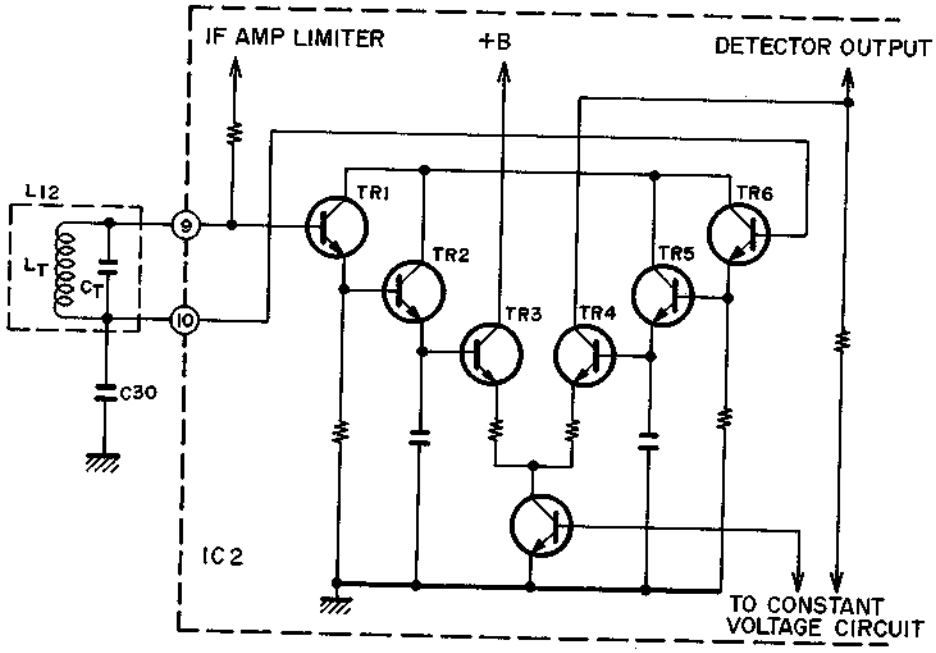


Fig. 7-168 FM detector

1) In Fig. 7-113 (D) a beat component at 5.5 MHz corresponding to the frequency difference between the video and audio carriers, is picked up by C25, C26, L11, and CF3 (ceramic filter), and is fed to IC2 terminals 1 and 2, and is further detected.
R38 (1 kohm) is a terminating resistor.
2) The audio signal fed to IC2 has its amplitude made constant, and fed to the FM detector, and fed to the FM detector. After detection, the low frequency signal passes through the electronic volume control buffer, is level adjusted at VR3, and becomes an audio output.
3) FM detector
The detector used here is called the peak differential detecting circuit. Its features are that a single tuned circuit suffices and that a large output is available.
Fig. 7-168 shows the FM detector, and the part within IC2 is its equivalent circuit. The tuning circuit (LT, CT, C30) resonates at f2 (Fig. 7-169) between terminal 9 and earth, and to f1 between terminal 10 and earth. Signals at terminals 9 and 10 are fed to the bases of TR1 and TR6 respectively, and fed to TR2 and TR5 via the emitter follower for peak value detection. This detection output is fed to the differential amplifier (TR3, TR4), and the differential output is picked up from the collector of TR4. Thus, the output of excellent linearity may be obtained.
4) Electronic volume
The level is varied by controlling the base bias current of the transistor. Normally IC2 pin (6) is locked to constant bias by D8 and R40. In Fig. 7-113(D) during the

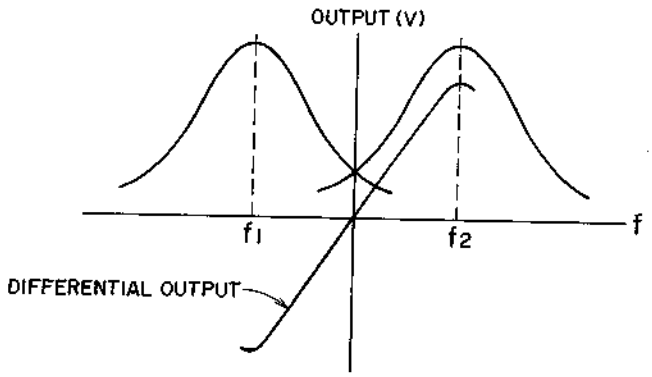


Fig. 7-169 FM detector output characteristic

Mute mode, Mute terminal becomes HIGH level, TR6 conducts, and the audio signal is cut off. Mute is effected during channel switching and search. Since the AFT operation cannot be made during the Mute mode, TR9 is turned OFF, AFT line is isolated, and the voltage is locked to the center AFT voltage 6.5V, determined by R14 and R15.

11-3-7 BAND SWITCHING CIRCUIT
In Fig. 7-113(D), the band switching circuit is composed of D9, D10, D11, TR10, TR11, TR12, etc. Any of the channels (VU, VH, and VL) specified by the operation PCB becomes LOW, the transistor (any of TR10–12) of that specified channel conducts, power is fed to the tuner and the demodulator AGC circuit, and the band is switched selected.

11-3-6 AUDIO CIRCUIT

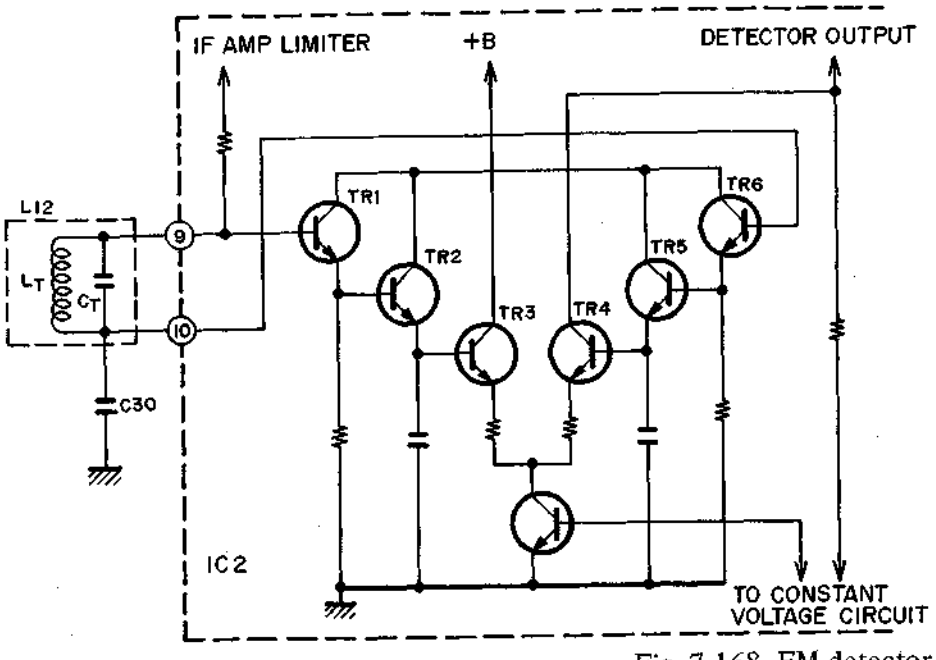


Fig. 7-168 FM detector

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The level is varied by controlling the base bias current of the transistor. Normally IC2 pin ⑥ is locked to constant bias by D8 and R40. In Fig. 7-113(D) during the

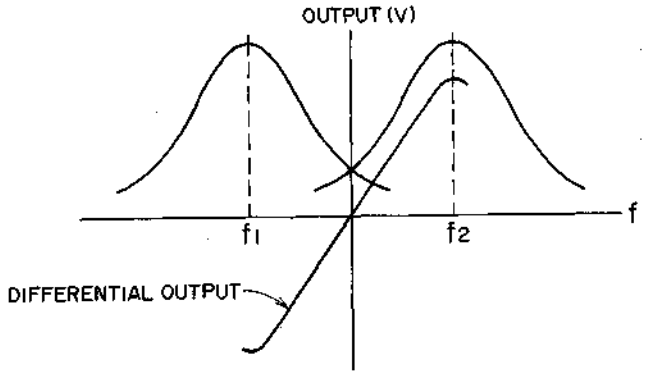


Fig. 7-169 FM detector output characteristic

Mute mode, Mute terminal becomes HIGH level, TR6 conducts, and the audio signal is cut off. Mute is effected during channel switching and search. Since the AFT operation cannot be made during the Mute mode, TR9 is turned OFF, AFT line is isolated, and the voltage is locked to the center AFT voltage 6.5V, determined by R14 and R15.

11-3-7 BAND SWITCHING CIRCUIT
In Fig. 7-113(D), the band switching circuit is composed of D9, D10, D11, TR10, TR11, TR12, etc. Any of the channels (VU, VH, and VL) specified by the operation PCB becomes LOW, the transistor (any of TR10–12) of that specified channel conducts, power is fed to the tuner and the demodulator AGC circuit, and the band is switched selected.

VIII. MECHANICAL ADJUSTMENTS

1. TENSION LEVER POSITION ADJUSTMENT

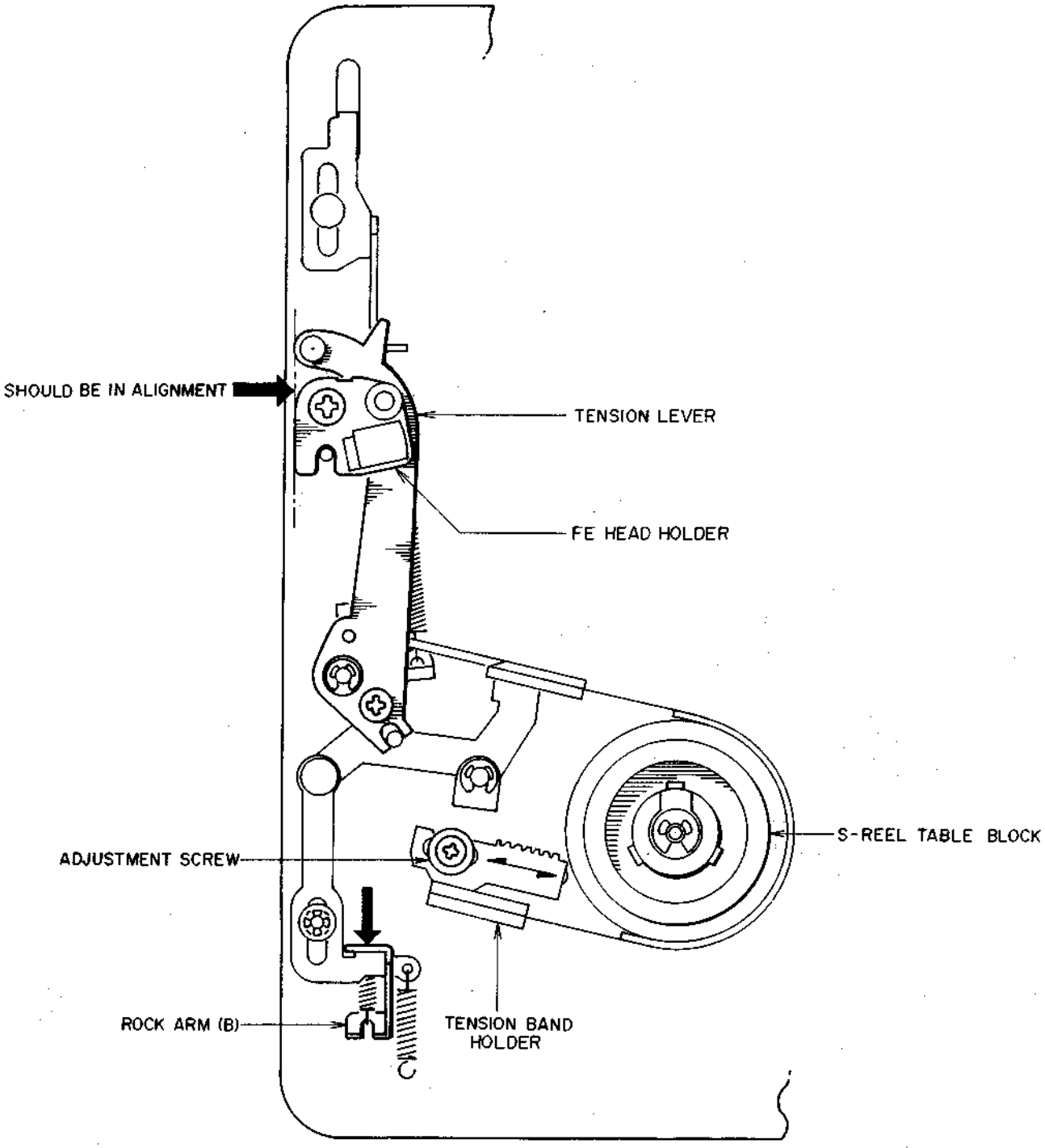


Fig. 8-1

1) Place the cassette holder in EJECT position.
2) Cover the detector lamp with a tape, etc. so that no light will leak.
3) Press the rock arm (B) in the arrow direction, and achieve PLAY mode.
4) Switch OFF the power switch on the rear panel and maintain the loading position.
5) Loosen the adjustment screw and adjust the tension band holder so that the tension lever and FE head holder are in alignment as shown in Fig. 8-1, and tighten the adjustment screw.
6) After adjustment, paint-lock the adjustment screw.

2. BACK TENSION ADJUSTMENT

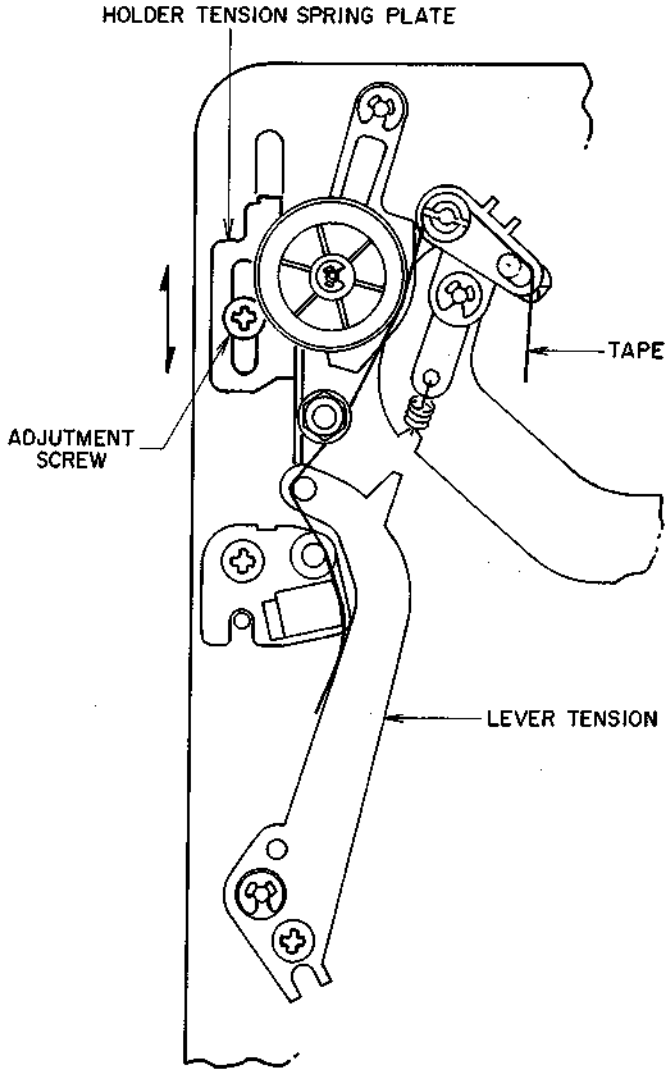


Fig. 8-2

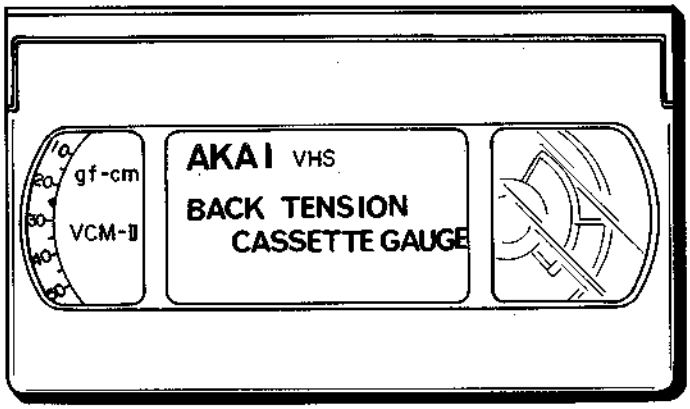


Fig. 8-3

1) Set the back tension adj. jig (AJ-751181) shown in Fig. 8-3 and achieve PLAY mode.
2) Loosen the adjustment screw shown in Fig. 8-2 adjust the holder tension spring plate so that back tension will be 20 gf-cm, and tighten the adjustment screw.
3) After adjustment, paint-lock the adjustment screw.

3. CHECK THE VARIOUS TORQUES

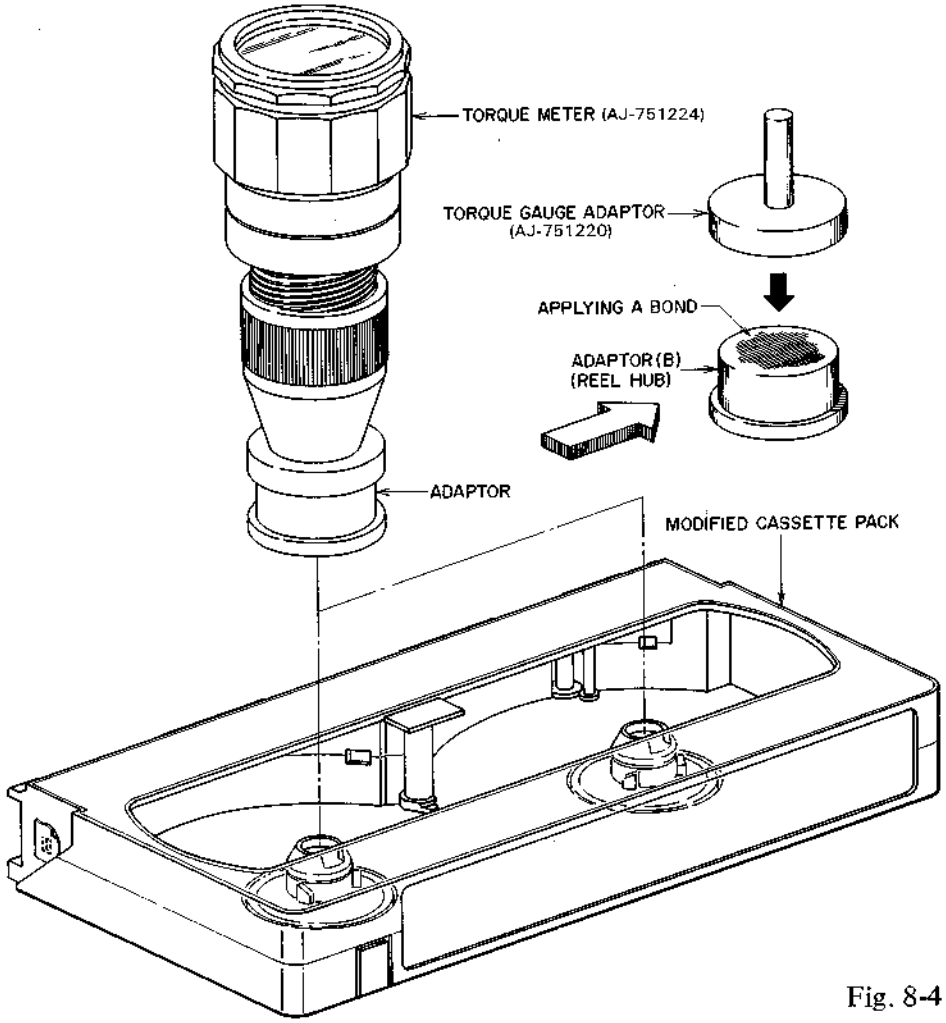


Fig. 8-4

MEASURING ITEM	MODE	MEASURING POINT	RESULT
PLAY Torque	PB	Take-up Reel	120^{+60}_{-40} g.cm
FF Torque	FF	Take-up Reel	More than 400 g.cm
REW Torque	REW	Supply Reel	More than 400 g.cm
Cue Torque	Cue	Take-up Reel	120^{+60}_{-40} g.cm
Review Torque	Review	Supply Reel	200^{+50}_{-40} g.cm
Unloading Torque	PB → STOP	Supply Reel	120^{+60}_{-40} g.cm

Fig. 8-5

NOTES: 1. The unloading torque operation is in three stages so finally, check that during unloading, the tape is winding into the cassette pack correctly.

2. A modified cassette pack is shown in Fig. 8-4. The upper side of the cassette pack has been cut away and the tape taken out.
There is black tape inside the pack to block the light from the start and end sensor.
This modified pack is very useful in checking in each mode so we recommend you make your own from a defective cassette pack.
This modified cassette pack is not available from Akai.

3. (How to make a Torque Gauge Adapter)
Adapter (B) is not supplied by Akai so make one by removing the reel hub of a VHS cassette tape E-120.
Use after fixing the adapter (B) to the Torque gauge adapter (AJ-751220)

IX. REPLACEMENT OF VIDEO HEAD ASSEMBLY

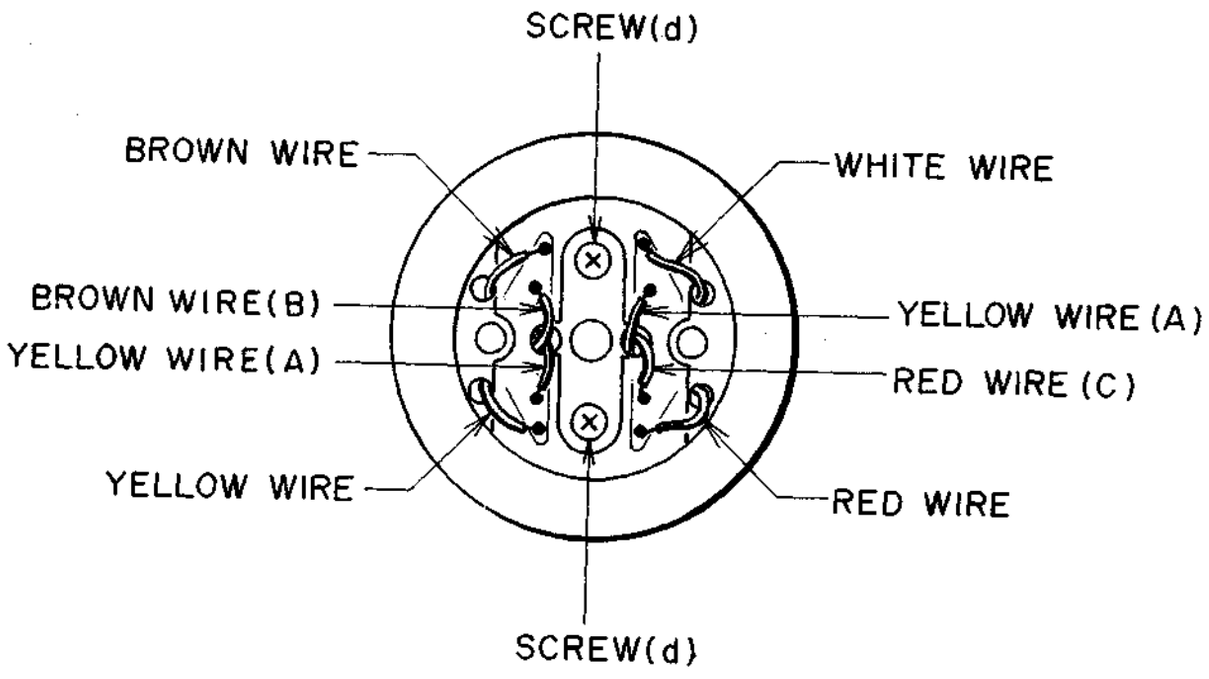


Fig. 9-1

1. UNSOLDER THE WIRE (A), THEN UNSOLDER THE BROWN WIRE (B) AND RED WIRE (C).
2. REMOVE THE TWO SCREWS (d), THEN PULL UP THE UPPER DRUM ASSEMBLY.
3. INSTALL THE NEW HEAD ASSEMBLY AND SOLDER THE WIRES AS SHOWN IN FIG. 9-1.
4. FASTEN TWO SCREWS (d).
5. AFTER REPLACEMENT, THE FOLLOWING ADJUSTMENTS ARE NECESSARY.
   1) PB Tracking Adjustment (Servo P.C Board Step 5 – PAL Mode)
   2) PB Switching Point Adjustment (Servo P.C Board Step 6 – PAL Mode)
   3) REC Switching Point Adjustment (Servo P.C Board Step 7 – PAL Mode)
   4) Video Head Q (Quality factor) and resonance Adjustment (Video P.C Board Step 12)
   5) PB Y Level Adjustment (Video P.C Board Step 13)
   6) PB Chroma Level Adjustment (Video P.C Board Step 16, 17, 18)

X. TAPE TRANSPORT ADJUSTMENT

1. TAPE GUIDE HEIGHT ADJUSTMENT

1) Set the cassette tape and achieve PLAY mode.
2) Make adjustment with the supply guide height adjustment nut, so that the lower part of the tape will pass the lower part of the guide pole without curling as shown in Fig. 10-1.
3) Make the same adjustment as that in 2) with the take-up guide height adjustment nut.

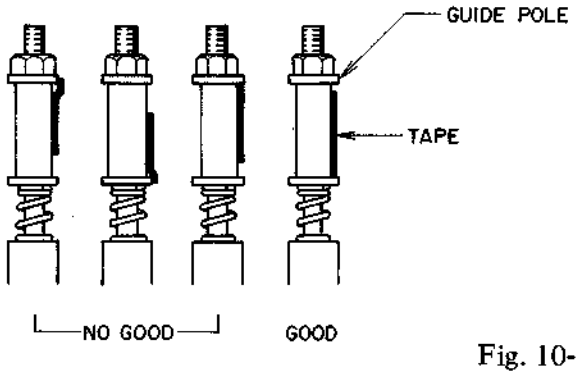


Fig. 10-1

2. GUIDE ROLLER HEIGHT ADJUSTMENT

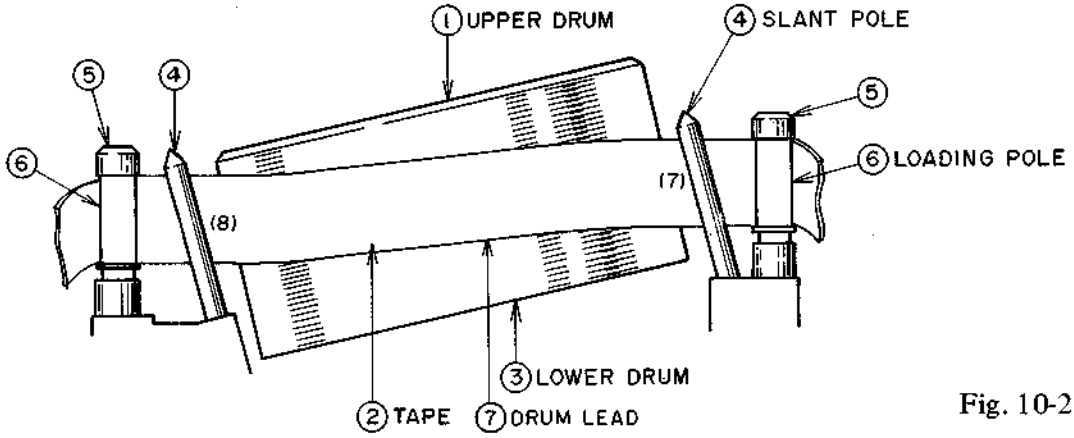


Fig. 10-2

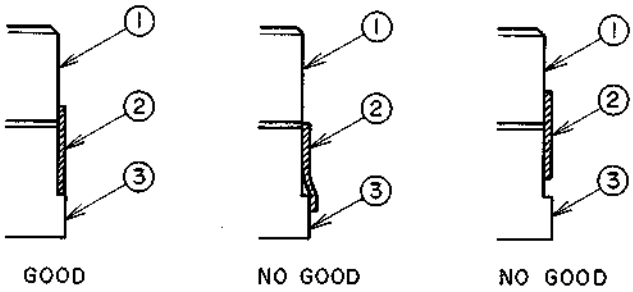


Fig. 10-3

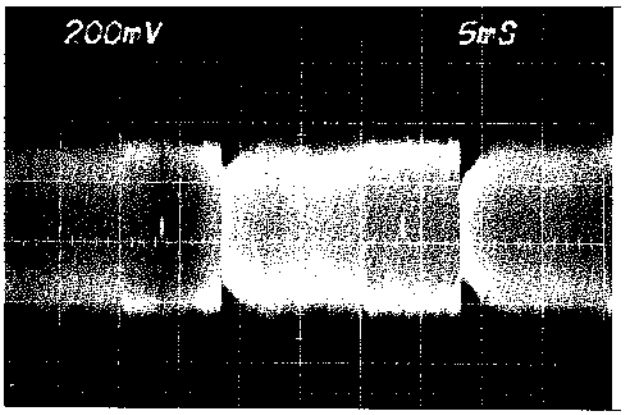


Fig. 10-5

1) Slightly loosen the set screw at the lower part of the guide roller so that the guide roller can be adjusted with reasonable tightness (See Fig. 10-4).
2) Connect an oscilloscope to P202 ③ (FM envelope out) of the Audio/pre P.C Board.

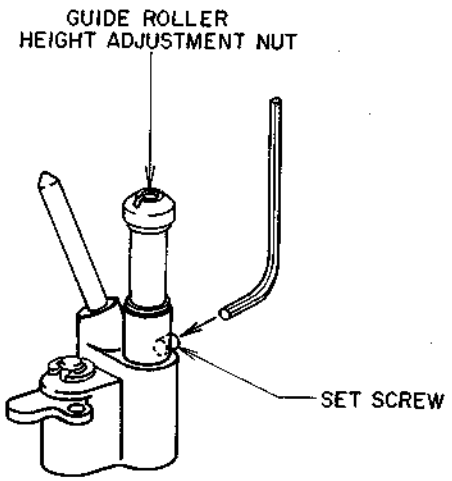


Fig. 10-4

3) Set the reference tape AT-750795 and achieve PLAY mode.
4) Ensuring it that the oscilloscope shows such a waveform as shown in Fig. 10-5 and also watching the point (7) of Fig. 10-2, adjust the height of the guide roller (R) so that the tape runs without curling as shown in Fig. 10-3(a).
5) Similarly, adjust the height of the guide roller (L) watching the waveform on the oscilloscope and the point (8) of Fig. 10-2.
6) Make sure that there is no shaking in the picture of the monitor TV.
7) Fix the guide roller with the set screw.

3. AUDIO/CONTROL HEAD HEIGHT, TILT AND AZIMUTH ADJUSTMENT

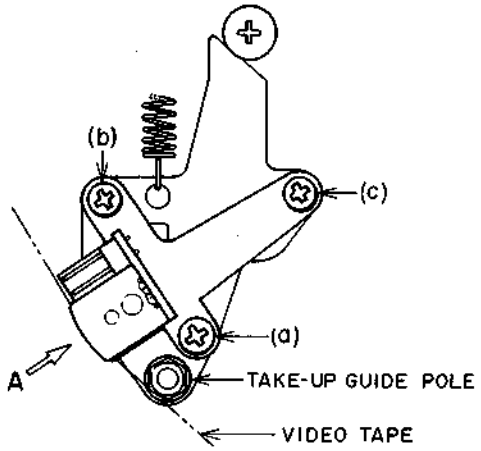


Fig. 10-6

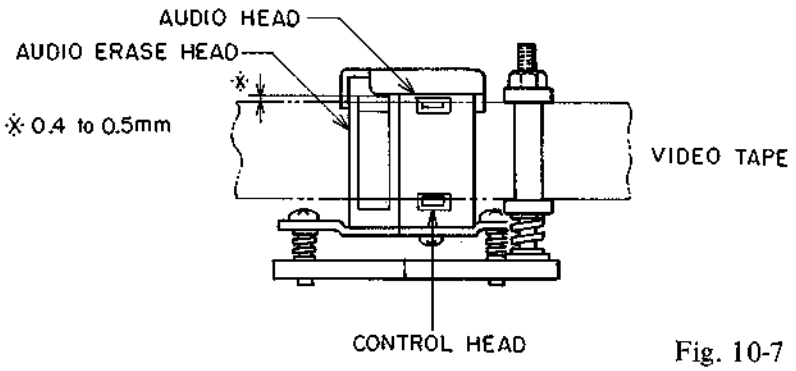


Fig. 10-7

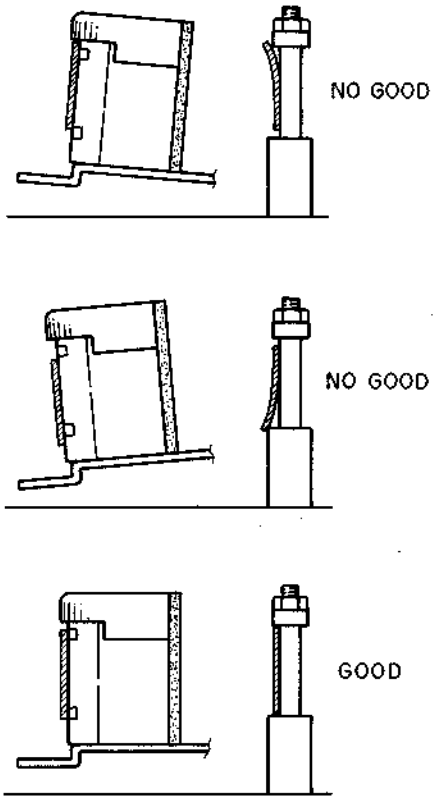


Fig. 10-8

1) Connect an AC Volt Meter to Audio Out.
2) Playback the reference tape AT-750795.
3) Turn screw (a), (b) and (c) in order slightly but by exactly the same amount. Adjust the audio output level to its maximum. Take screw (a) as your standard and use screw (b) for azimuth adjustment. Adjust screw (c) until there is no tape wrinkle in the guide pole section, the audio output level is at maximum and there is the minimum possible level fluctuation.
   Then raise and lower screw (a) very slightly and adjust (b) and (c), and set to the point for maximum output.

NOTE: Repeat the adjustment of tape guide height, guide roller height and audio/CTL several times in order to achieve the perfect tape running.

4. CONTROL HEAD POSITION ADJUSTMENT

1) Connect an oscilloscope to P202 ③ (FM envelope out) of the Audio/pre P.C Board.
2) Set the reference tape AT-750795 and initiate the PLAY mode.
3) While watching the waveform on the oscilloscope, turn the tracking volume on the front panel and confirm in which direction from the click position the maximum point of the waveform is located.
4) Turn back the tracking volume to the click position and carry out the following ⓐ or ⓑ adjustment.
   ⓐ If the maximum point of the waveform is reached by turning the tracking volume clockwise, turn the adjusting driver clockwise and make adjustment to the maximum point.
   ⓑ If the maximum point of the waveform is reached by turning the tracking volume counterclockwise, turn the adjusting driver counterclockwise to make adjustment to the maximum point.

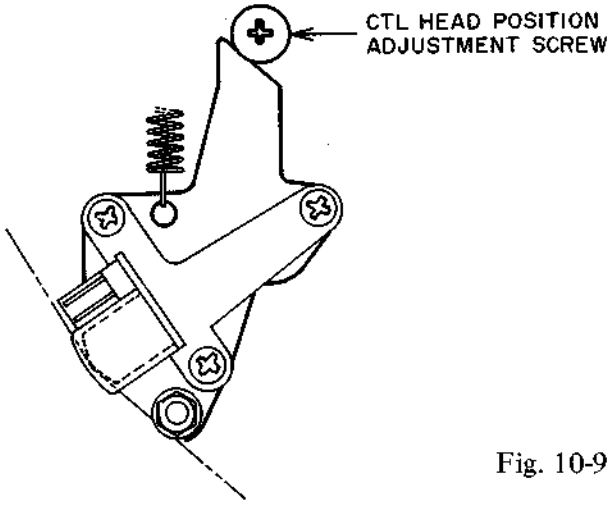


Fig. 10-9

NOTE: Make these adjustments only after the tape running is completely adjusted.

5. ADJUSTMENT OF QUICK FINDER (REVIEW) RUN

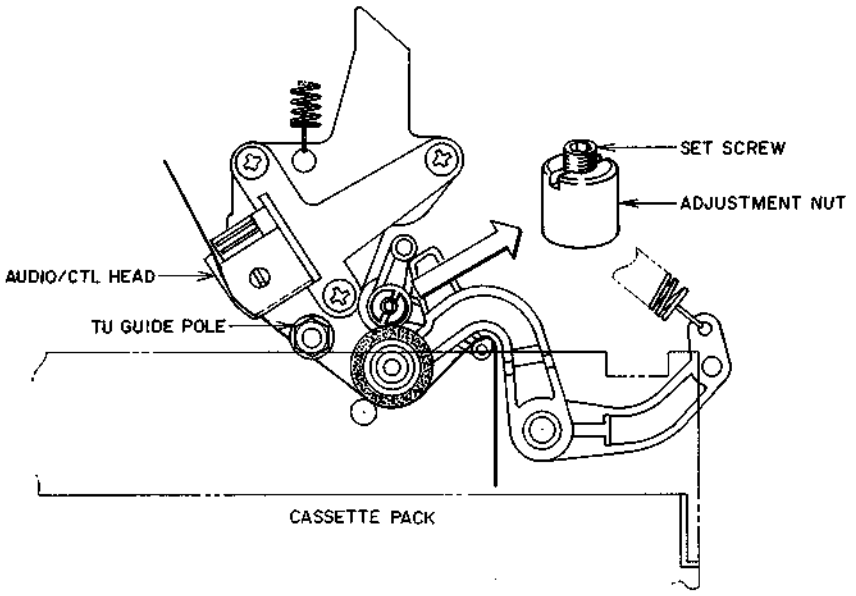


Fig. 10-10

1) Set the recording and playback tape E-240 and wind it up.
2) Press the REVIEW button to initiate the REVIEW mode.
3) Loosen the set screw in Fig. 10-10 so that the adjustment nut can be turned.
4) While watching the tape running on the take-up guide pole, turn the adjustment screw slowly so as to eliminate the curling of the tape (Fig. 10-11 (c)).
5) Tighten the set screw and fix the adjustment screw.
6) After the completion of adjustment, press the stop button once, and after unloading the tape, recheck the review run.

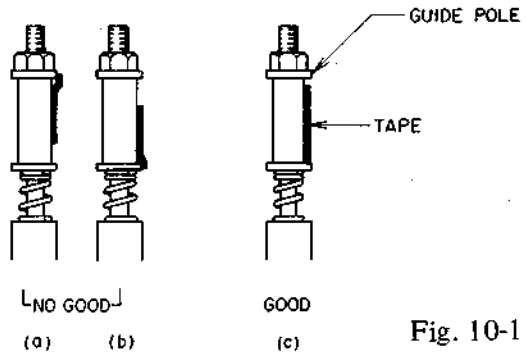


Fig. 10-11

NOTE: If the adjustment nut is turned too fast, some deviation may be found after adjustment because the tape running does not follow such a fast pace.

XI. ELECTRICAL ADJUSTMENT

1. SERVO P.C BOARD ADJUSTMENT

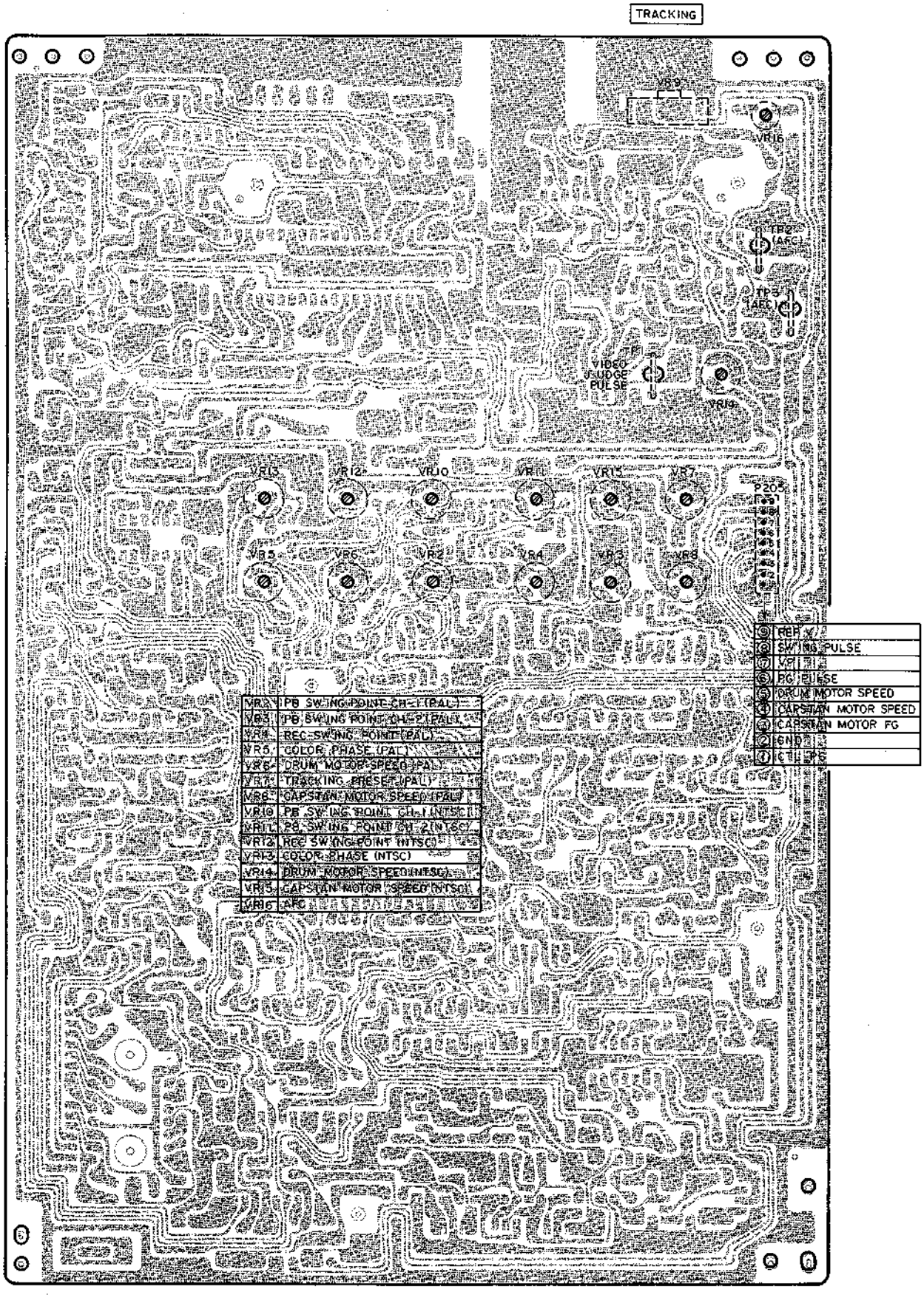
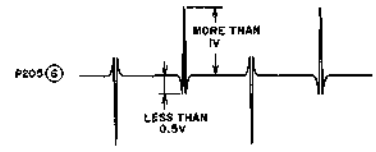
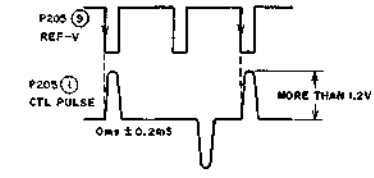
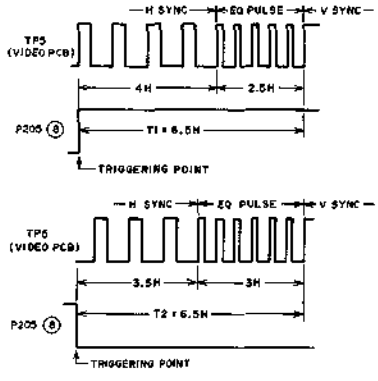
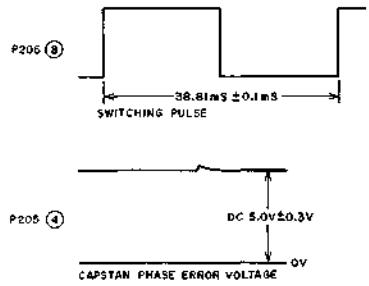
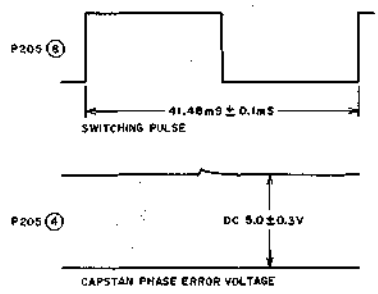


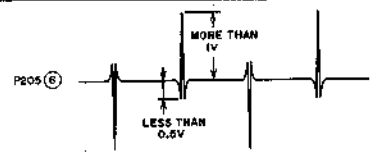
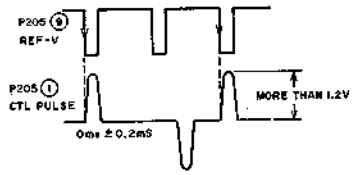
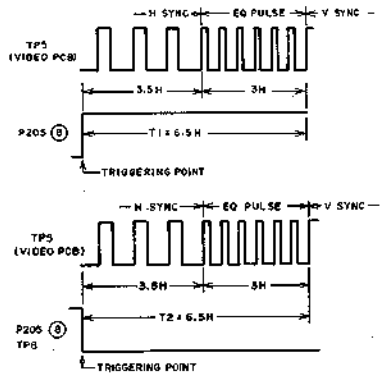
Fig. 11-1 Servo P.C Board V1009A5270 (Pattern Side View)

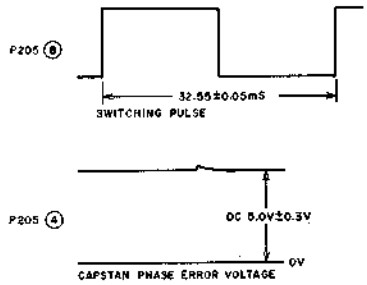
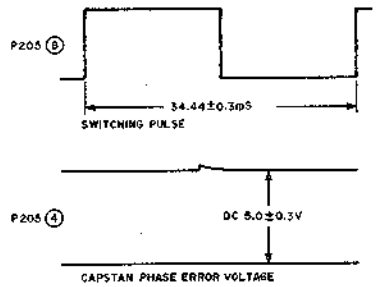
1-1 PAL MODE

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
1	AFC	Color Bar from Color Bar Generator	REC	TP2 TP3	VR16	Adjust VR16 so that the voltage of TP2 and TP3 are within DC 2.4V ±0.1V.
2	PG Pulse	Test Tape (AT-750795)	PB	P205 ⑥	Confirmation	 Confirm the PG waveform is within the level shown above.
3	Drum Motor Normal Speed	Test Tape (AT-750795)	PB	P205 ⑤	VR6	 Adjust so that the Drum Servo phase error voltage is within DC5.0V±0.1V.
4	Capstan Motor Normal Speed	Test Tape (AT-750795)	PB	P205 ⑤	VR8	 Adjust so that the capstan servo phase error voltage is within DC5.0V±0.2V.
5	Tracking Preset (EXT-Tracking volume is set to OFF position)	Test Tape (AT-750795)	PB	P205 ⑨ (REF-V) P205 ① (CTL pulse)	VR7	 1. Adjust so that the start-down waveform portion of REF-V (Servo standard signal) is brought in line with the phase of CTL pulse. 2. At this time, confirm the CTL pulse level is more than 1.2V.
6	PB Switching Point	Test Tape (AT-750795)	PB	TP5 (Video PCB) P205 ⑧	VR2 (CH1) VR3 (CH2)	 Adjust T1 with VR2 to 6.5H and T2 to 6.5H with VR3. The difference between T1 and T2 should be within 0.3H.

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
7	REC Switching Point	Color Bar from Color Bar Generator	REC	TP5 (Video PCB) P205 ⑧	VR4	Adjust T1 and T2 waveforms in step 6 to 6.5H±0.3H.
8	Color Phase	Test Tape (AT-750795)	PB Cue (Quick Finder)	P205 ⑧ P205 ④	VR5	 1. Adjust VR5 so that the switching pulse waveform is shown above. 2. Readjust VR5 when no color convergence is caused on the TV screen in cue mode. 3. Confirm that the capstan servo phase error voltage is within DC 5.0V±0.3V.
			PB Review (Quick Finder)	P205 ⑧ P205 ④	Confirmation	 1.Confirm the switching pulse waveform is shown above. 2. Confirm that color convergence and also confirm that the capstan servo error voltage is within DC 5.0V±0.3V.
9	Tape Speed	Test Tape (AT-750795)	PB	Capstan FG output	Confirmation	Confirm the Frequency of the capstan motor FG output is within 400 Hz±2Hz.
10	Wow & Flutter	Test Tape (AT-750800) 3,000 Hz	PB	Audio output	Confirmation	Confirm the Wow & Flutter is within 0.25% WRMS.

1-2 NTSC MODE

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
1	PG Pulse	Test Tape (AT-750796)	PB	P205 ⑥	Confirmation	 Confirm the PG waveform is within the level shown above.
2	Drum Motor Normal Speed	Test Tape (AT-750796)	PB	P205 ⑤	VR14	 Adjust so that the Drum Servo phase error voltage is within DC5.0V±0.1V.
3	Capstan Motor Normal Speed	Test Tape (AT-750796)	PB	P205 ④	VR15	 Adjust so that the capstan servo phase error voltage is within DC5.0V±0.2V.
4	Tracking Preset (EXT-Tracking volume is set to OFF position)	Test Tape (AT-750796)	PB	P205 ⑨ (REF-V) P205 ① (CTL pulse)	Confirmation	
5	PB Switching Point	Test Tape (AT-750796)	PB	TP5 (Video PCB) P205 ⑧	VR10 (CH1) VR11 (CH2)	 Adjust T1 with VR10 to 6.5H and T2 to 6.5H with VR11. The difference between T1 and T2 should be within 0.3H.

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
6	REC Switching Point	Color Bar from Color Bar Generator	REC	TP5 (Video PCB) P205 ⑧	VR12	Adjust T1 and T2 waveform in step 5 to 6.5H±0.3H.
7	Color Phase	Test Tape (AT-750796)	PB Cue (Quick Finder)	P205 ⑧ P205 ④	VR13	 1. Adjust VR13 so that the switching pulse waveform is shown above. 2. Readjust VR13 when no color convergence is caused on the TV screen in cue mode. 3. Confirm that the capstan servo phase error voltage is within DC 5.0V±0.3V.
			PB Review (Quick Finder)	P205 ⑧ P205 ④	Confirmation	 1. Confirm the switching pulse waveform is shown above. 2. Confirm that color convergence and also confirm that the capstan servo error voltage is within DC5.0V± 0.3V.
8	Tape Speed	Test Tape (AT-750796)	PB	Capstan FG output	Confirmation	Confirm the Frequency of the capstan motor FG output is within 570Hz±2H.
9	Wow & Flutter	Test Tape (AT-750801) 3,000 Hz	PB	Audio output	Confirmation	Confirm the Wow & Flutter is within 0.25% WRMS.

2. VIDEO (EGN) P.C BOARD ADJUSTMENT

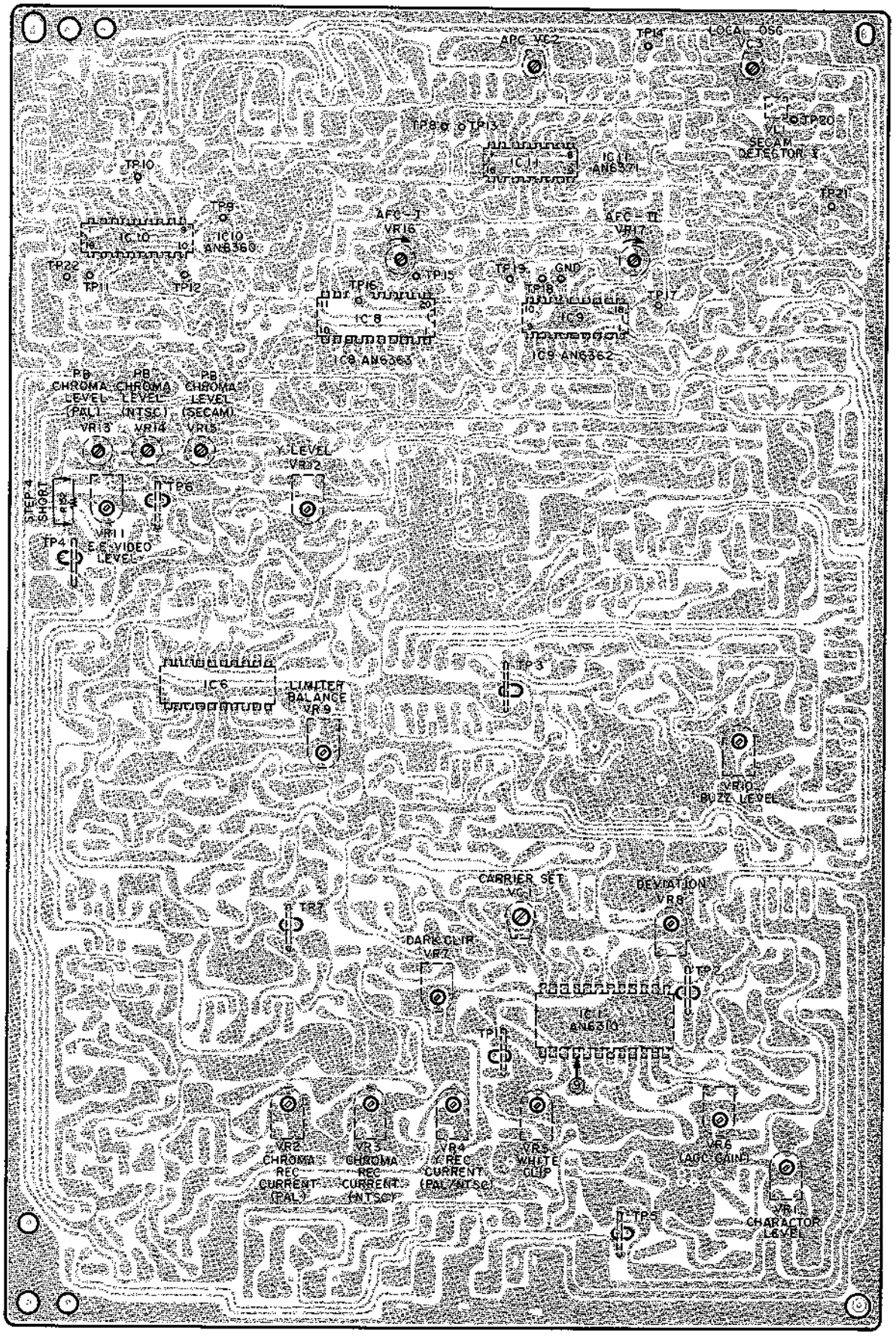
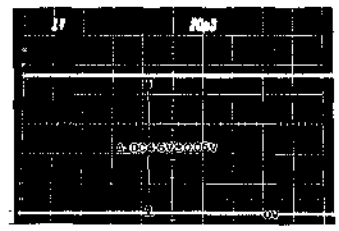
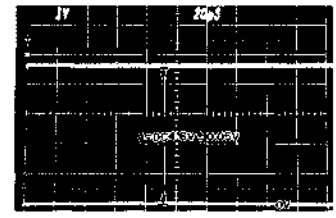
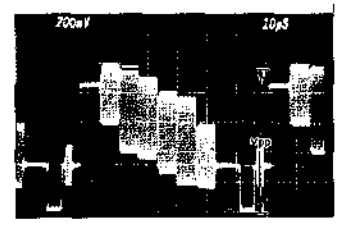
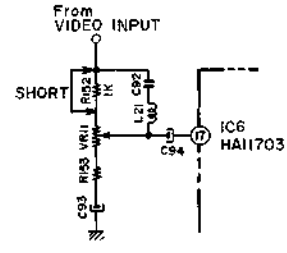
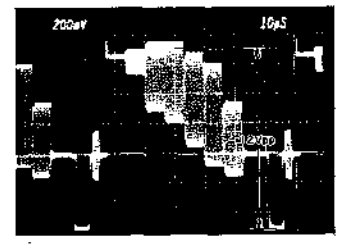
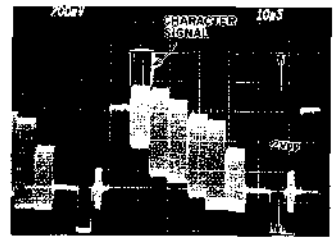
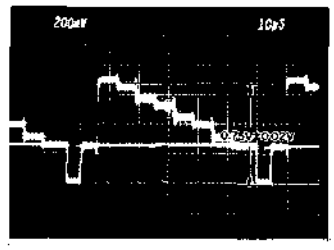
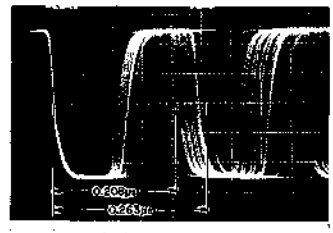
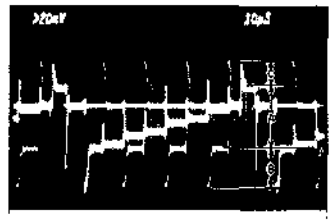
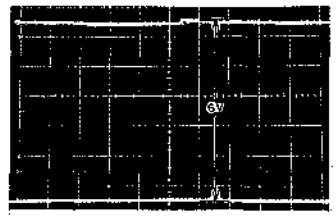
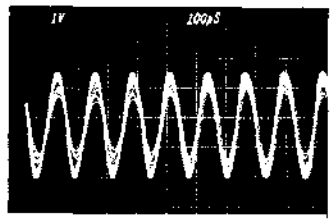
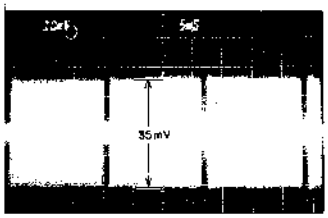
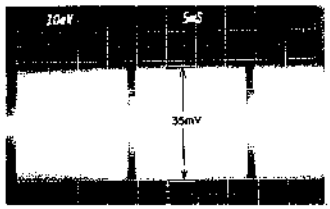
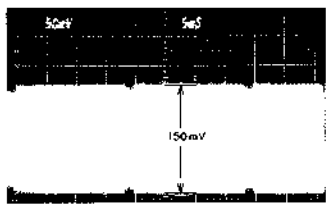
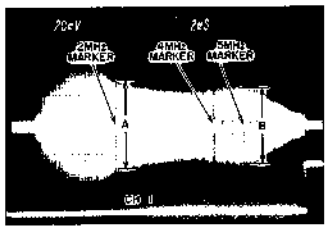
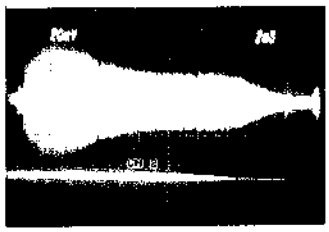
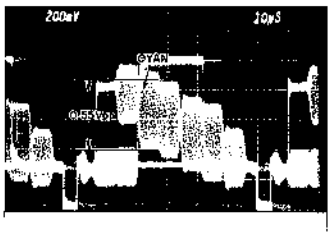
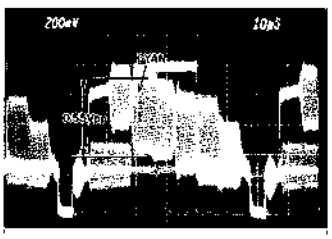
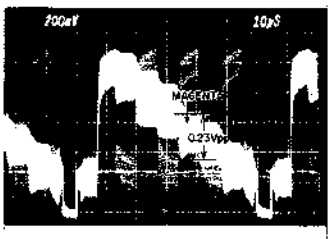


Fig. 11-2 Video (EGN) P.C Board V1009A5280 (Pattern Side View)

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
1	AFC-I	Color Bar from Color Bar Generator (PAL)	REC	TP15	VR16	 Adjust so that "A" is within DC 4.6V±0.05V.
2	AFC-II	Color Bar from Color Bar Generator (PAL)	REC	TP17	VR17	 Adjust so that "A" is within DC 4.6V±0.05V.
3	E-E Level	Color Bar from Color Bar Generator (PAL)	REC	TP5	VR11	 Adjust so that the video output is 1.00±0.02Vp-p.
4	Buzz Level	Color Bar from Color Bar Generator (PAL)	REC	TP5	VR10	  1. Short the R152 1 kohm as shown figure above. 2. Adjust VR10 so that the video signal cliped at 1.20±0.02Vp-p.

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
5	Character Level	Color Bar from Color Bar Generator (PAL) Display ON	REC	TP5	VR1	 1. Adjust VR1 so that the character level clipped at 1.20±0.02Vp-p.
6	AGC Gain	Color Bar from Color Bar Generator (PAL)	REC	TP2	VR6	
7	Carrier and Deviation	Color Bar from Color Bar Generator (PAL)	REC	IC 1 ⑨	VC1 (Carrier set) VR8 (Deviation)	 Carrier set = 0.263 μs Deviation = 0.208 μs
8	White Clip and Dark Clip	Color Bar from Color Bar Generator (PAL)	REC	TP1	VR 5 (White Clip) VR7 (Dark Clip)	 White Clip A:B=1:0.6 Dark Clip A:C=1:0.4
9	APC	Color Bar from Color Bar Generator (PAL)	REC	TP13	VC2	
10	SECAM Detector I	Color Bar from Color Bar Generator (SECAM)	REC	TP20	VL1	 Adjust VL1 to obtain maximum level.

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
11	Rec Current	Color Bar from Color Bar Generator (NTSC)	REC	P203 ①, ③ (Audio/Pre PCB)	VR4 (Y) VR3 (CHROMA)	 1) Fully turn the VR4 clockwise. 2) Adjust the chroma Rec Current so that P203 ①, ③ waveforms are set to 35mVp-p by the VR3.
		Color Bar from Color Bar Generator (PAL)	REC	P203 ①, ③ (Audio/Pre PCB)	VR2 (CHROMA) VR4 (Y)	  1) Adjust the Chroma Rec current so that P203 ①, ③ waveforms are set to 35mVp-p by the VR2. 2) Adjust the Y Rec current so that the P203 ①, ③ waveforms are set to 150mVp-p by the VR4.
12	Video Head Resonance and Q (quality factor)	Test Tape (AT-750802)	PB	P202 ③	VC2 VR6 (CH1) VC1 VR5 (CH2)	  *Refer to the Audio/pre P.C Board Adjustment point (Fig. 11-4) 1) Fully turn the VR6 clockwise and then adjust the VC2 so that the peak frequency is 5.0MHz. 2) Adjust the VR6 so that "Q" is set at a ratio of A:B=1:1.2 3) Connect the TP to the GND level and adjust the CH2 (VC1, VR5) in the same way as in the CH1.

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
13	PB Y Level	Test Tape (AT-750797)	PB	TP5	VR12	 Adjust so that the video output is 1.00±0.02Vp-p.
14	Limiter Balance	Test Tape (AT-750797)	PB	TP5	VR9	 Adjust VR9 so that the carrier leak is minimum at H. SYNC.
15	Local OSC	Test Tape (AT-750797)	PB	TP14	VC3	4.433619MHz±10Hz
16	PB Chroma Level (PAL)	Test Tape (AT-750797)	PB	TP5	VR13	 Adjust so that a cyan level is within 0.55±0.01Vp-p.
17	PB Chroma Level (NTSC)	Test Tape (AT-750798)	PB	TP5	VR14	 Adjust VR14 so that a cyan level is within 0.55±0.01Vp-p.
18	PB Chroma Level (SECAM)	Test Tape (AT-750799)	PB	TP5	VR15	 Adjust VR15 so that a magenta level is within 0.23±0.02Vp-p.

3. EGN P.C BOARD ADJUSTMENT

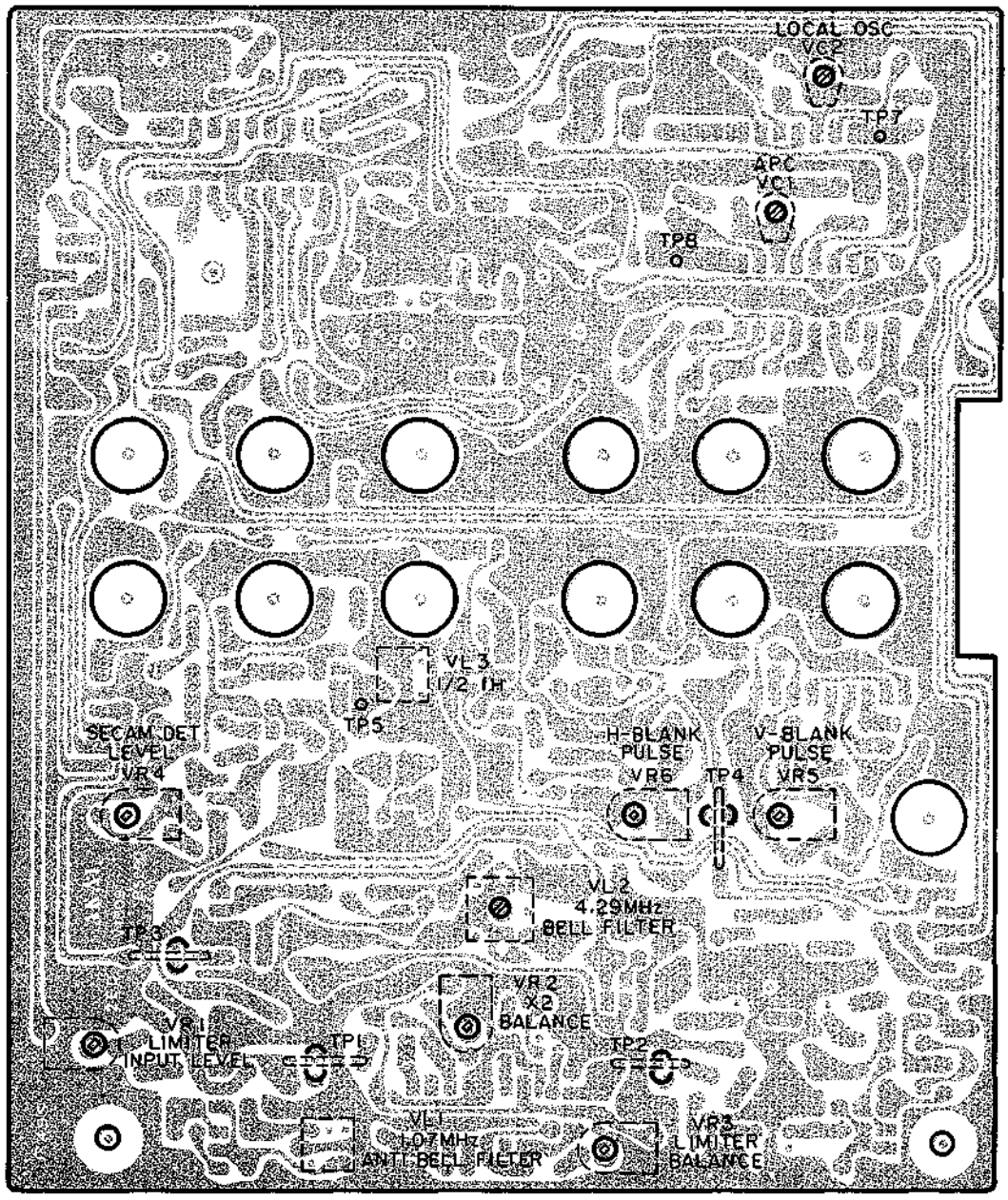
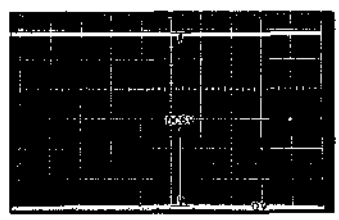
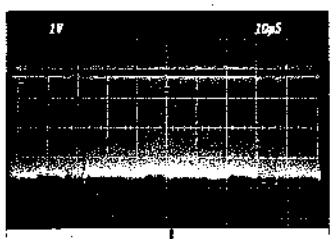
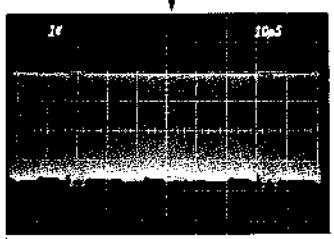
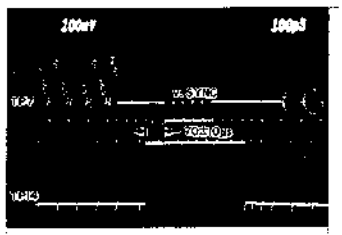
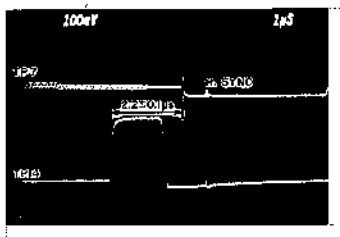


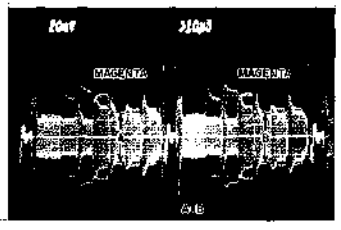
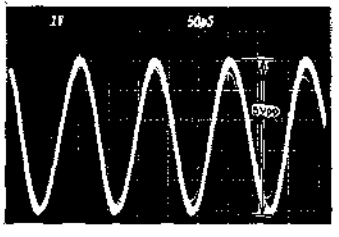
Fig. 11-3 EGN P.C Board V1009B5290 (Parts Side View)

3-1 NTSC 3.58 MHz MODE

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
1	APC	Color Bar from Color Bar Generator	REC	TP8	VC1	
2	Local Oscillator	Test Tape (AT-750798)	PB	TP7	VC2	3.579545MHz±10Hz

3-2 SECAM L MODE

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
1	1.07MHz Anti Bell Filter	Test Tape (AT-750799)	PB	TP1	VL1 VR1	  1) Adjust VL1 so that the waveform will be flattest. 2) Adjust VR1 so that the level will be 450±20mVp-p.
2	Limiter Balance x2 Balance	Test Tape (AT-750799)	PB	TP2	VR2 (x2 Balance) VR3 (Limiter Balance)	 
3	Noise Gate Pulse (H Blank Pulse V Blank Pulse)	Test Tape (AT-750799)	PB	TP5 (Video(EGN) PCB) TP4	VR5 (V-Blank Pulse) VR6 (H-Blank Pulse)	 

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
4	4.29 MHz Bell Filter	Test Tape (AT-750799)	PB	TP3	VL2	 Adjust so that the magenta level is equal at A and B.
5	SECAM Detector II	Test Tape (AT-750799)	PB	TP5	VL3 (½ f_H) VR4 (Level)	 1) Adjust VL3 to obtain maximum level. 2) Adjust VR4 so that level is within 5±0.5Vp-p.

4. AUDIO/PRE P.C BOARD ADJUSTMENT

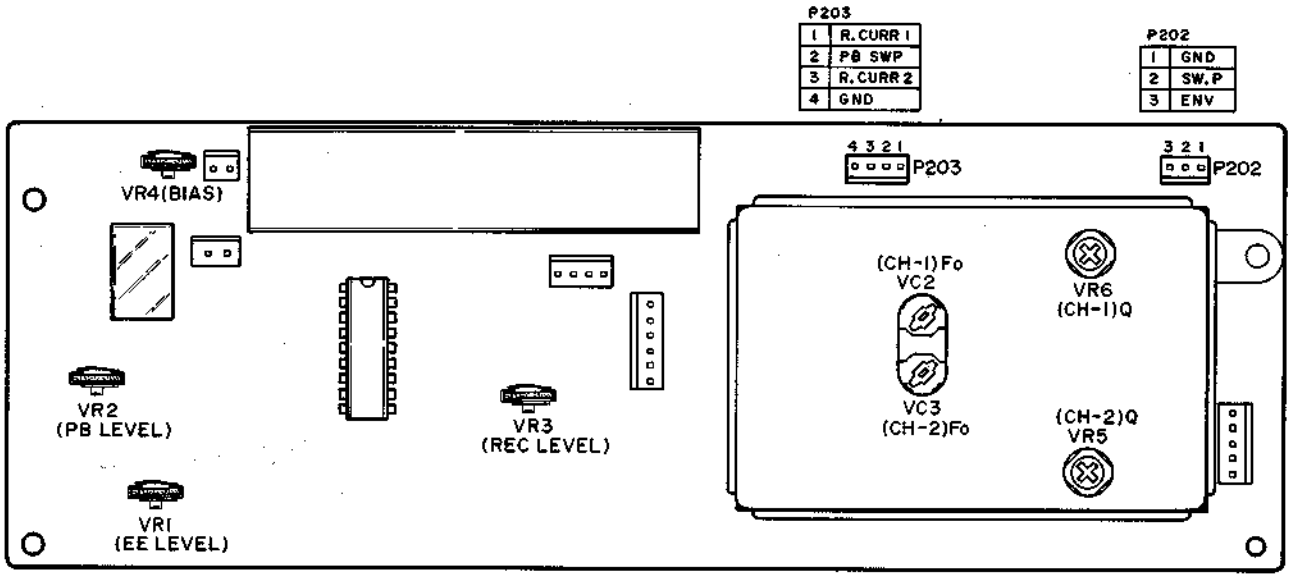


Fig. 11-4 Audio/pre P.C Board V1009A5180

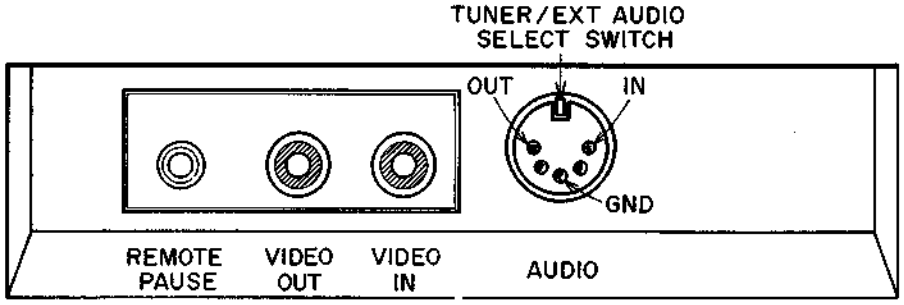


Fig. 11-5 Audio Jack

STEP	ADJUSTMENT ITEM	INPUT	MODE	TEST POINT	ADJUSTMENT PARTS	RESULT & REMARKS
1	E-E Level	Audio Input 1 kHz, –20dB	E-E	Audio Out	VR1	–6 dBm ± 0.5 dBm
2	PB Level	Test Tape AT-750800 (1,000 Hz)	PB	Audio Out	VR2	–6 dBm ± 0.5 dBm
3	Rec Level	Audio Input 1 kHz, –20dB	REC/PB	Audio Out	VR3	–6 dBm ± 0.5 dBm
4	Frequency Response	Audio Input 100Hz, –20dB 1 kHz, –20dB 7 kHz, –20dB	REC/PB	Audio Out	VR4	100 Hz: –6 dBm ± 1 dBm 1 kHz : –6 dBm ± 0.5 dBm 7 kHz : –6 dBm $^{+2}_{-3}$ dBm
5	Distortion Factor	Audio Input 1kHz, –20dB	REC/PB	Audio Out	Confirm	Less than 3%
6	Adjust by repeating steps 3, 4 and 5.					

5. DEMODULATOR P.C BOARD ADJUSTMENT

Since the adjustment of the Demodulator P.C Board requires a special jig, avoid touching the adjustment point. But should any adjustment become necessary, use the following adjustment method.

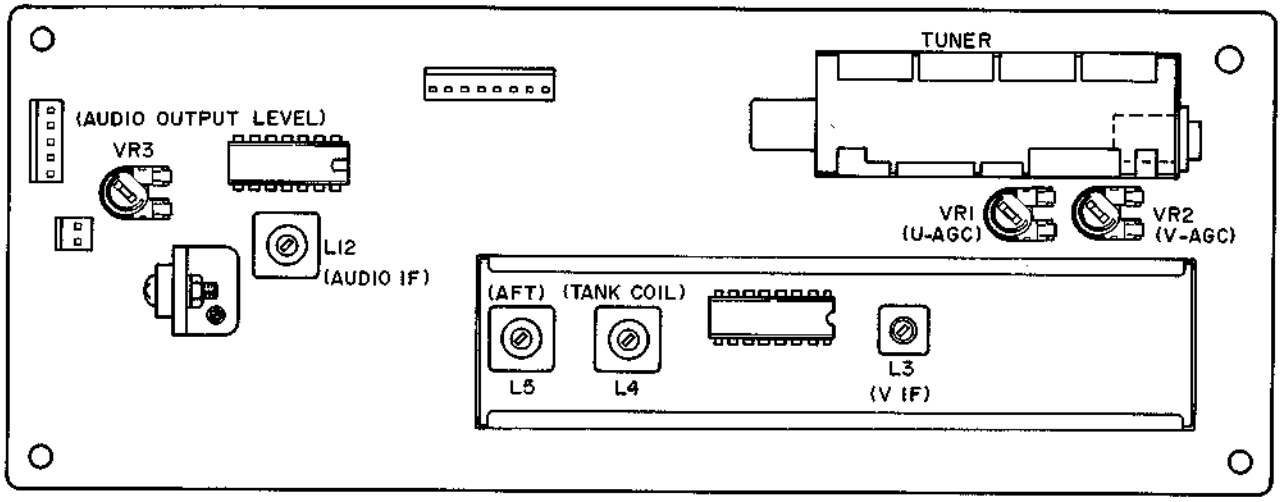


Fig. 11-6 Demodulator P.C Board

5-1 TANK COIL ADJUSTMENT

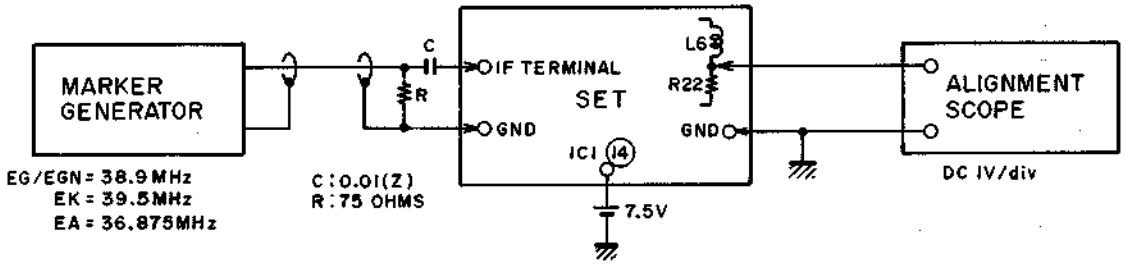


Fig. 11-7

1) Apply 50mVp-p in If frequency (EG/EGN=38.9 MHz) to IF terminal.
2) Connect the alignment scope to intersection between L6 and R22.
3) Apply DC 7.5V to Pin (14) of IC1.
4) Adjust L4 so that the DC voltage appearing on the alignment scope will be minimum.

5-2 AFT ADJUSTMENT

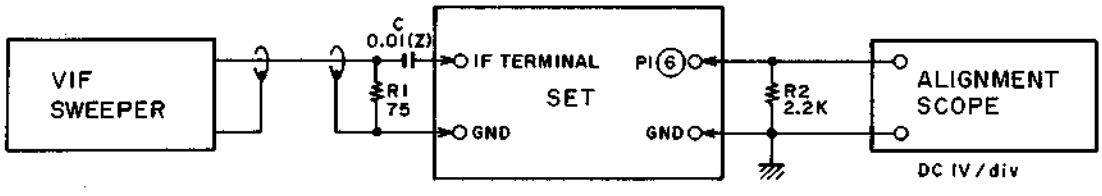


Fig. 11-8

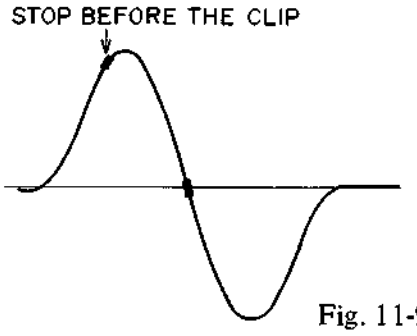


Fig. 11-9

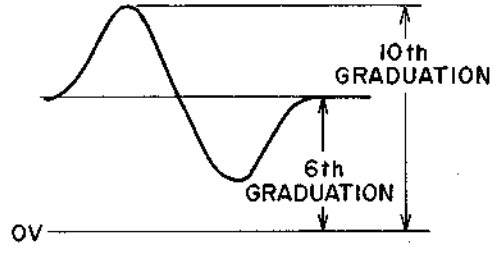


Fig. 11-10

1) Connect VIF sweeper output 70 dB to the IF terminal.
2) Connect the alignment scope to the AFT terminal (Pin ⑥ of P1).
3) Give an optional size to the waveform with the IF AGC volume, and make approximate adjustment with L5 so that the marker will be positioned at 6th graduation of the alignment scope.
4) Stop with IF AGC volume before the waveform is clipped (Fig. 11-9).
5) Adjust with L5 so that the marker (EG/EGN=38.9 MHz) will be at 6th graduation of the alignment scope (Fig. 11-10).

5-3 VIF ADJUSTMENT

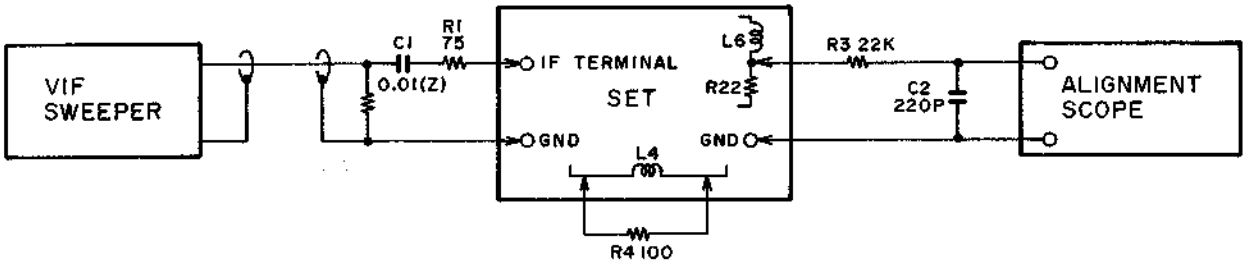


Fig. 11-11

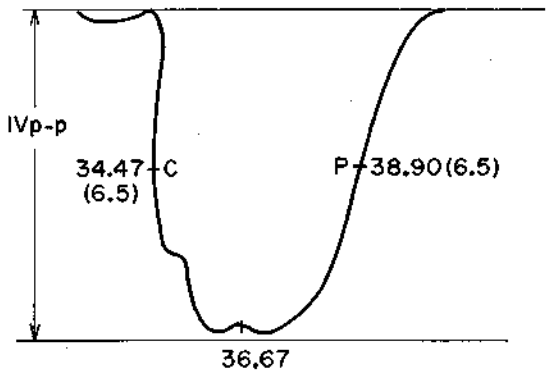


Fig. 11-12

1) Apply VIF sweeper output of 70 dB to IF terminal.
2) Connect the Alignment scope to the intersection between L6 and R22.
3) Connect dummy resistors of 100 ohms to both ends of the tank coil (L4).
4) Set the alignment scope to 10th graduation by means of the IF AGC volume and adjust the L3 so that the marker position is as shown in Fig. 11-12.
5) Adjust the Tuner IF coil so that the P and C level is as shown in Fig. 11-12.

5-4 RF AGC ADJUSTMENT

V-AGC

1) Receive VH channel and connect oscilloscope to the video out terminal (Pin ② of P2).
2) Adjust VR2, so that the Noise is disappears from the Noise condition and sync. signal becomes rather small.

U-AGC

1) Receive UHF channel, and connect oscilloscope to the video output terminal (Pin ② of P2).
2) Adjust VR1 in the same way as U-AGC Adjustment.

5-5 AUDIO OUTPUT ADJUSTMENT

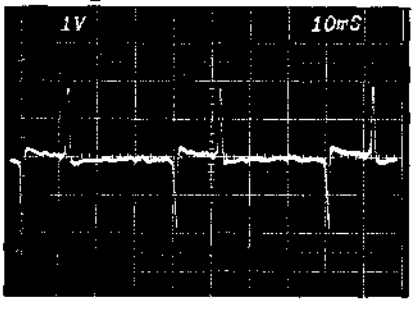
1) Apply DC 9.0V to Pin ② of P1.
2) Connect an AC voltmeter and a distortion meter to Pin ④ of P2.
3) Connect an oscilloscope to Pin ② of P2.
4) Add the following RF signals to ANT IN.
   EG/EGN model VHF 12CH (color bar)
   UHF 50CH (Philips)
   } 58dB
5) Turn VR3 fully anticlockwise, and adjust with L12 so that the reading of the AC voltmeter is a maximum and that distortion factor is a minimum.
6) Adjust with VR3 so that the reading of the AC voltmeter will be −17 dB.

XII. VARIOUS WAVEFORMS AT EACH TESTPOINT

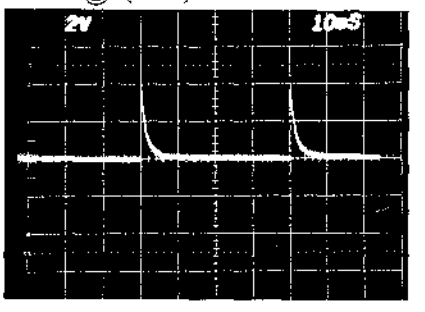
NOTES: 1. All the waveforms are measured using the VS-2EGN.
2. Use the Color Bar Tape(AT-750797) as the playback tape and the Color Bar Signal 1 Vp-p from SSG, as the input during recording.
3. If not specially instructed, take the waveform when the oscilloscope is in the AC Mode.
4. Shown are Volt/cm for left upper side figure and Time/cm for right upper side figure on the waveform photos.
(For example: making an observation at P205 ① under 1V/cm, 10mS/cm condition).

1. SERVO P.C BOARD

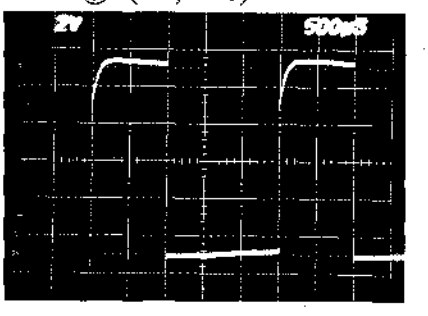
P205 ① (P.B)



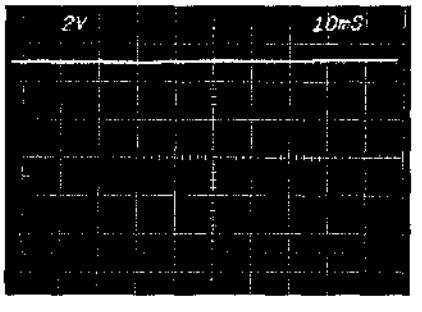
P205 ② (REC)



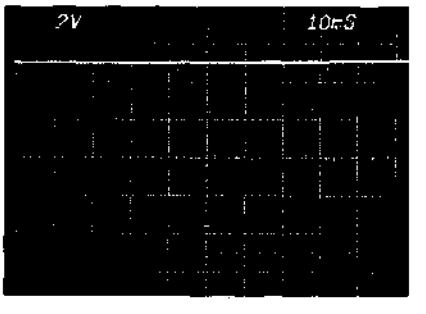
P205 ③ (P.B, REC)



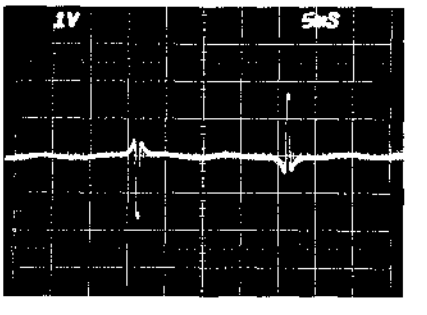
P205 ④ DC (P.B, REC)



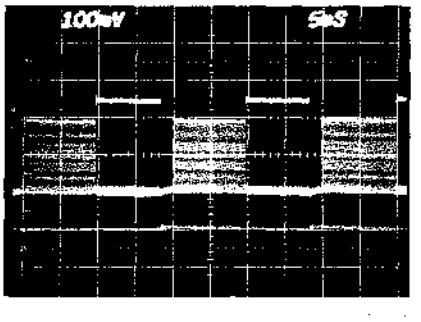
P205 ⑤ DC (P.B, REC)



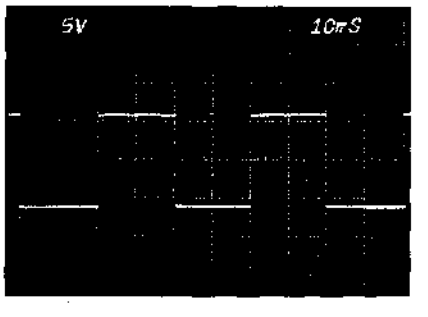
P205 ⑥ (P.B, REC)



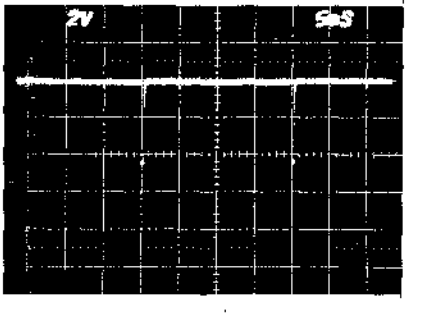
P205 ⑦ (P.B, REC)



P205 ⑧ (P.B, REC)



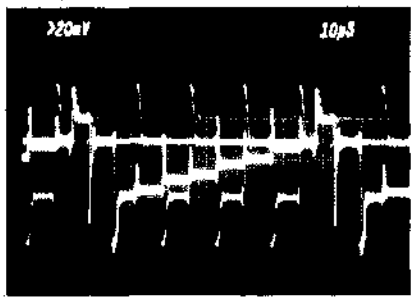
P205 ⑨ (P.B, REC)



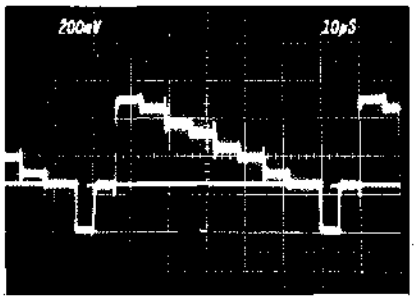
TP1

2. VIDEO P.C BOARD

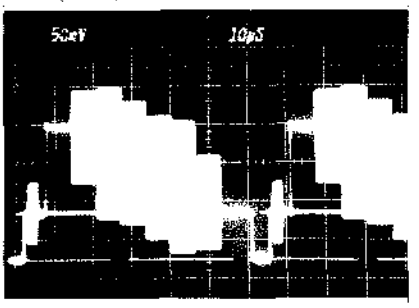
TP1 (REC) D-CLIP W-CLIP



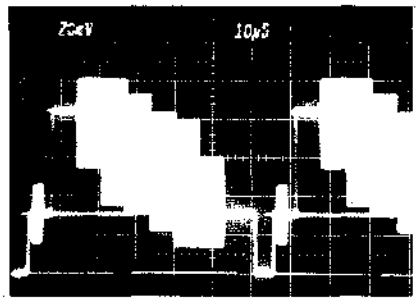
TP2 (REC) AGC



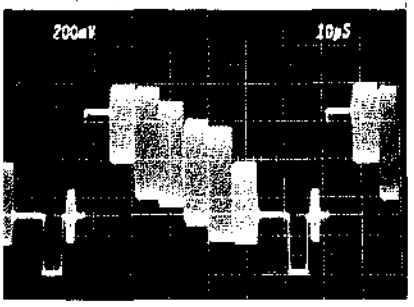
TP3 (REC)



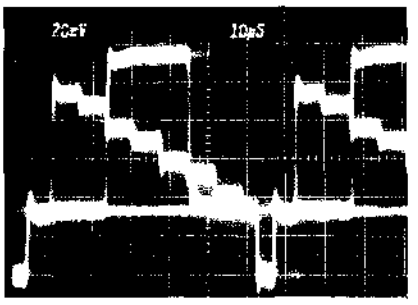
TP4 (REC)



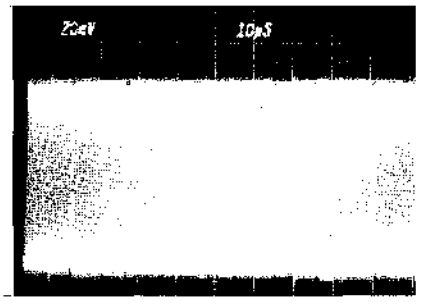
TP5 (REC) Video Out



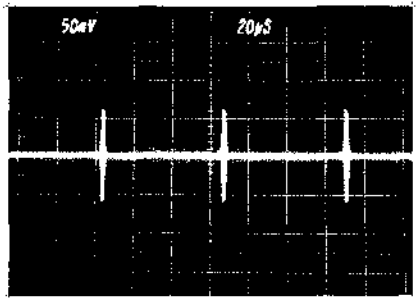
TP6 (PB) De-Emphasis



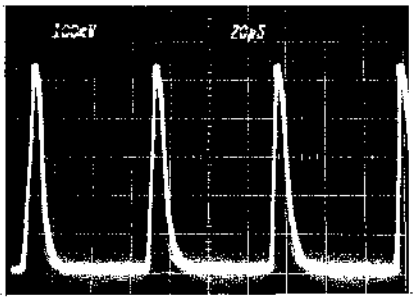
TP7 (P.B) D.O.C



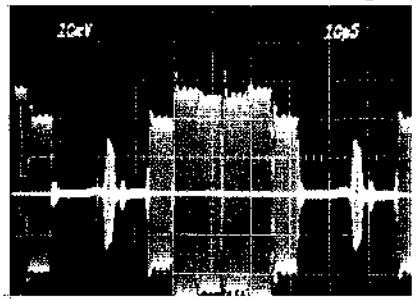
TP8 (REC) Gated Burst Signal



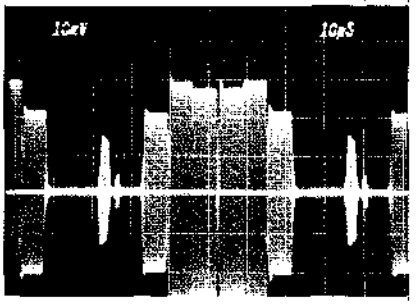
TP9 (REC)



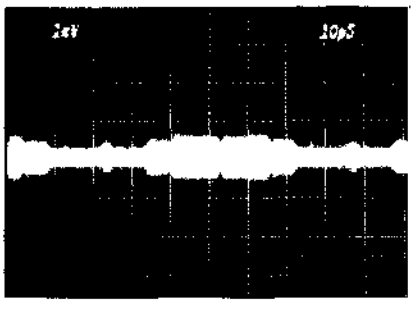
TP10 (REC) REC LOW CHROMA Signal



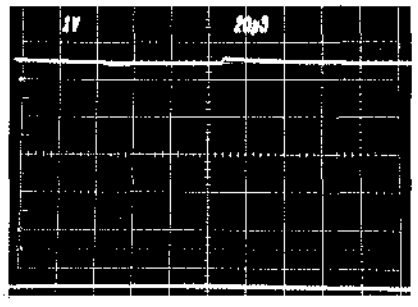
TP11 (REC) REC ACC



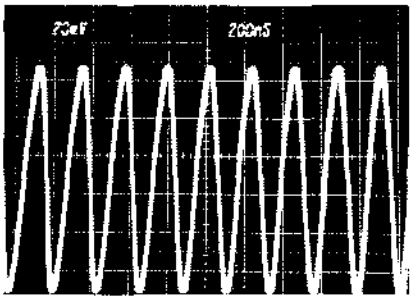
TP12 (REC)



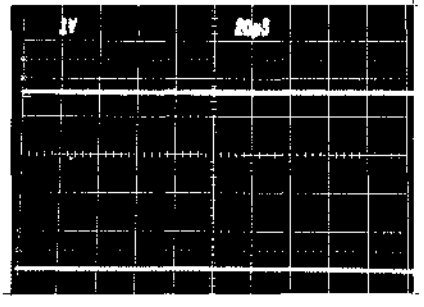
TP13 (REC) APC



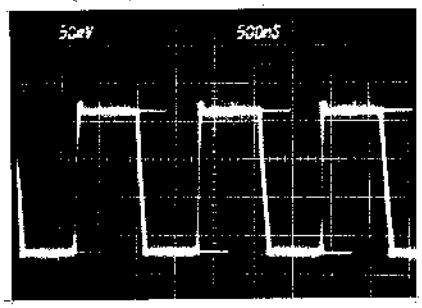
TP14 (PB) Local OSC



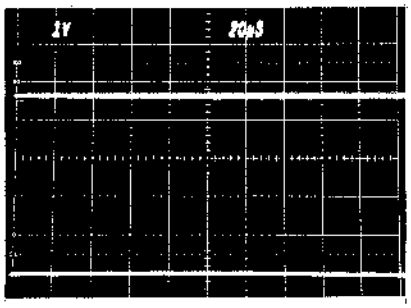
TP15 (REC) AFC-I



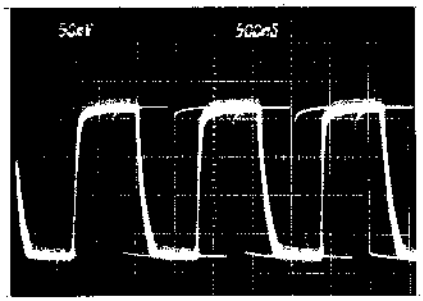
TP16 (REC)



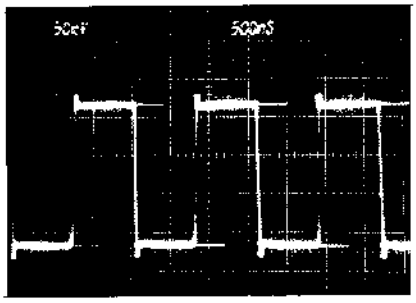
TP17 (REC) AFC-II



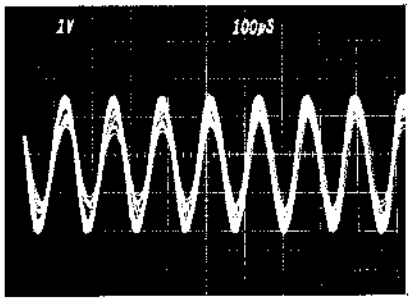
TP18 (REC) 40 fH



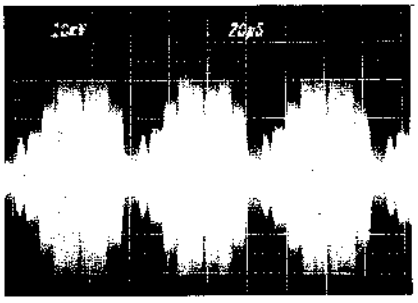
TP19 (REC)



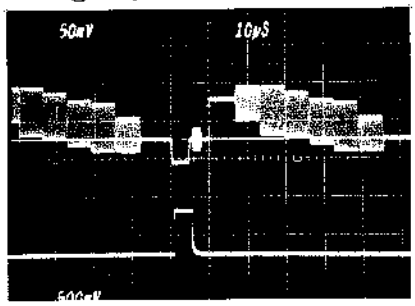
TP20 (REC) SECAM DETECTOR I



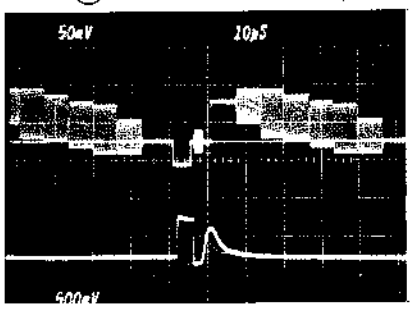
TP21 (P.B)



IC8 ③ Sync Pulse

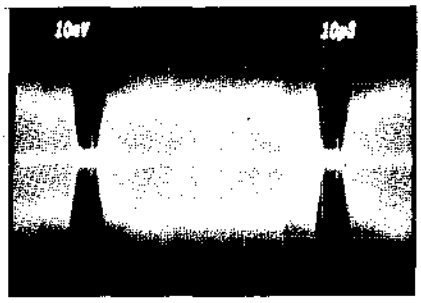


IC9 ⑱ HD Pulse

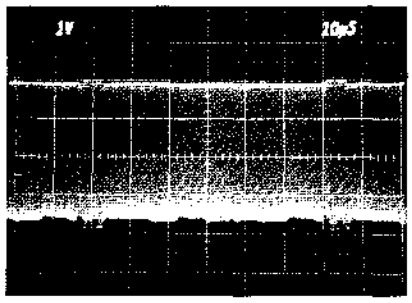


3. EGN P.C BOARD

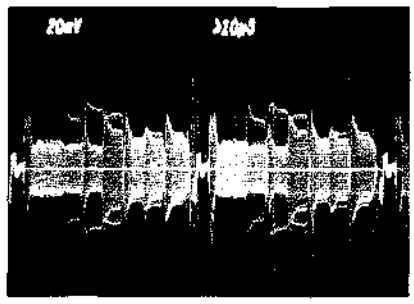
TP1 (PB)



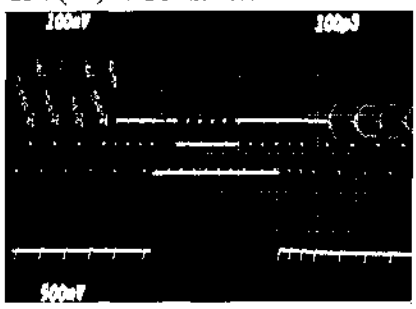
TP2 (PB)



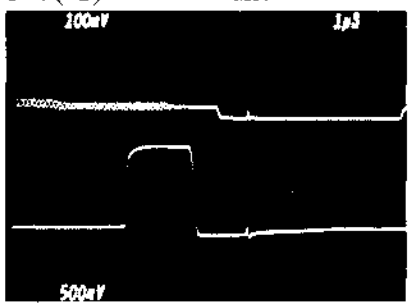
TP3 (PB)



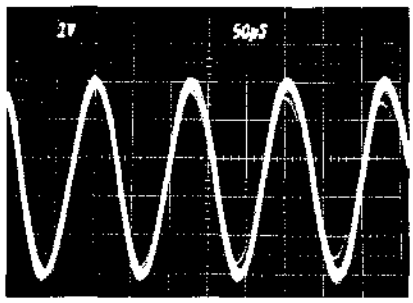
TP4 (PB) V-Blank Pulse



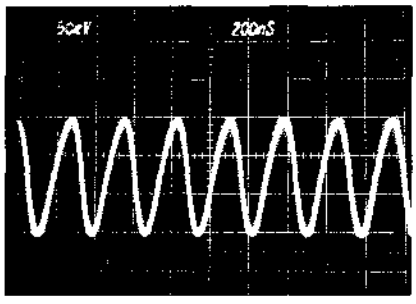
TP4 (PB) H-Blank Pulse



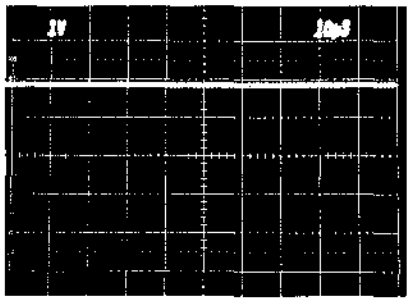
TP5 (PB) SECAM DETECTOR-II



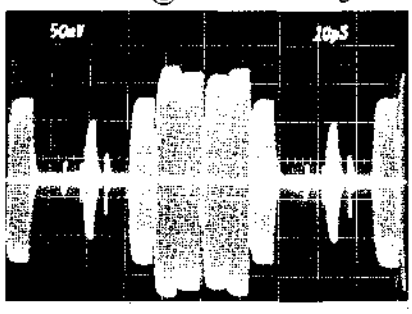
TP7 (PB) Local OSC



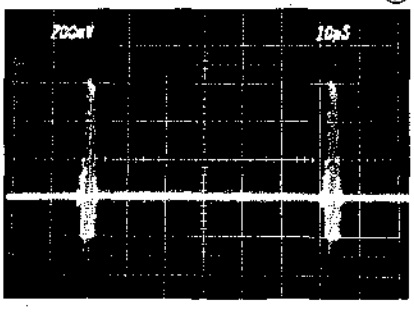
TP8 (PB) APC



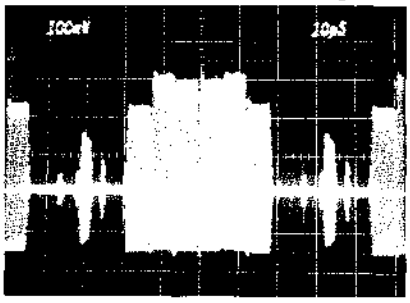
IC6 AN6360 ① EE Chroma Signal IN



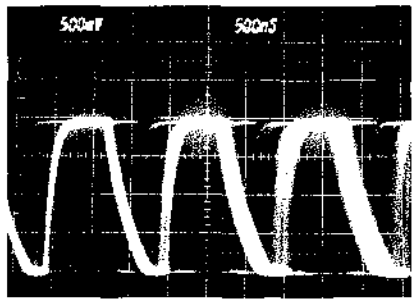
Gated Burst Pulse (REC)
IC6 AN6360 ③



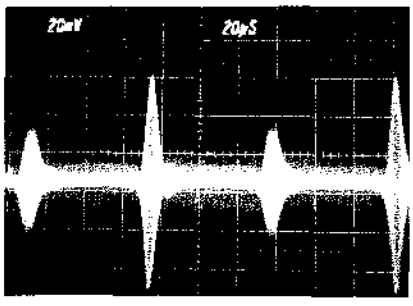
ACC (REC) IC6 AN6360 ⑰



40f_H (REC) P59 ⑧



Line Burst Signal TR12 Ⓑ



XIII. P.C BOARD TITLES AND IDENTIFICATION NUMBERS

P.C BOARD TITLE	P.C BOARD NUMBER
Video (EGN) P.C Board	V1009A5280
Audio/Pre P.C Board	V1009A5180
Servo (EGN) P.C Board	V1009A5270
Operation P.C Board	V1009A5170
Power & Sys. Con. P.C Board	V1009A519A
Mecha. Drive P.C Board	V1009A519B
Intermediate P.C Board	V1009A519C
EGN P.C Board	V1009B5290
Sensor (2) P.C Board	V1004C5540
R.S. SW P.C Board	V1004C5541
SW A P.C Board	V1004C5542
SW B P.C Board	V1004C5543
EJ. S. SW P.C Board	V1004C5544
Power Filter P.C Board	V1009D5210
LED (EGN) P.C Board	V1009D5320
Demodulator P.C Board	6C00033A1

XIV. COMPOSITION OF VARIOUS P.C BOARDS

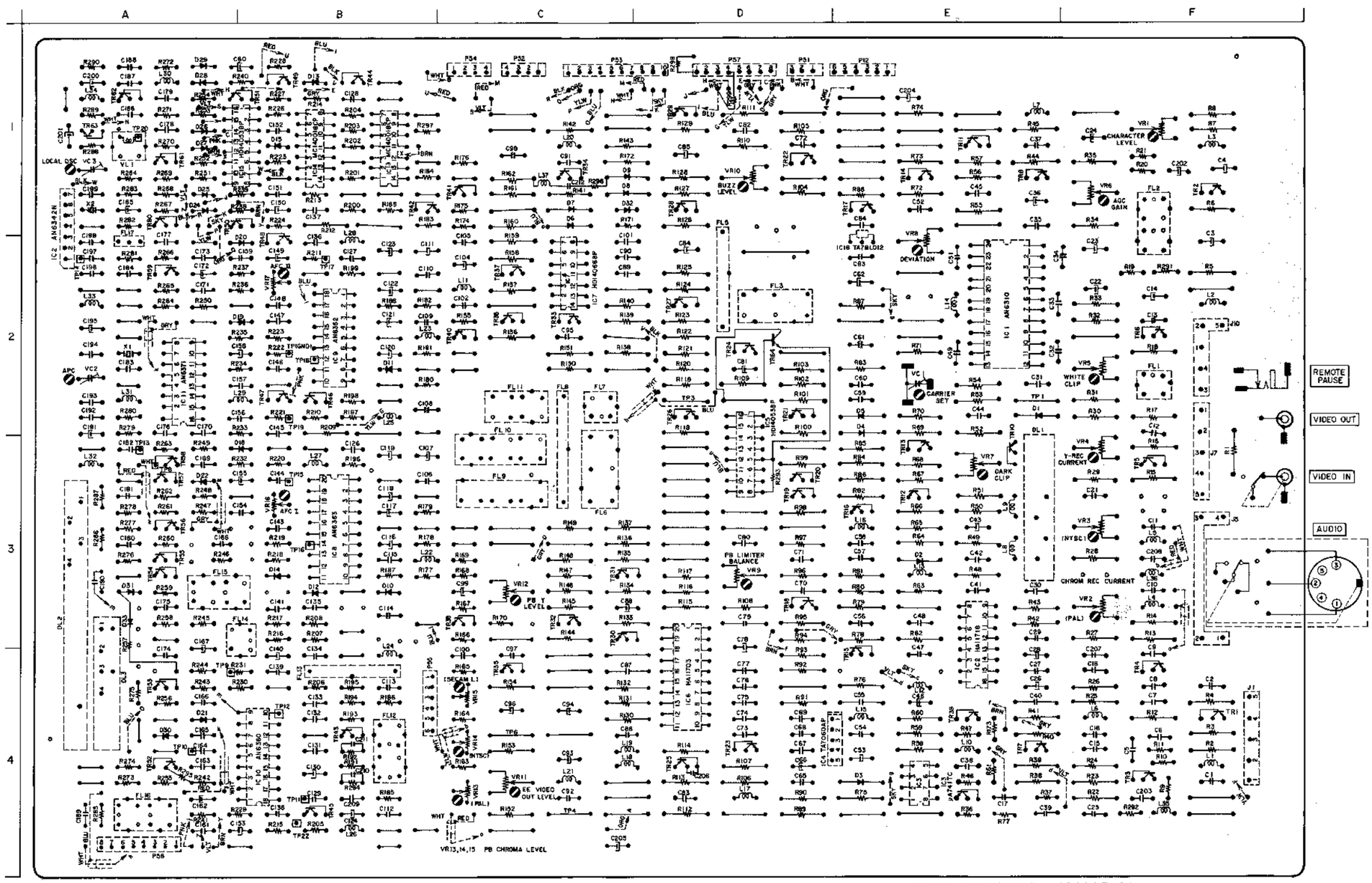
1. VIDEO (EGN) P.C BOARD V1009A5280

LOCATION OF COMPONENTS

IC
IC1 ..... E2
IC2 ..... E3
IC3,4 ..... E4
IC5 ..... D3
IC6 ..... D4
IC7 ..... C2
IC8 ..... B3
IC9 ..... B2
IC10 ..... B4
IC11 ..... A2
IC12 ..... A1
IC13,14,15 ..... B1
IC16 ..... E3

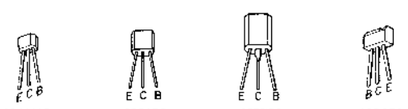
TR
TR1 ..... P4
TR2 ..... P1
TR3,4 ..... P4
TR5 ..... P3
TR6 ..... P2
TR7 ..... E4
TR8 ..... E1
TR9 ..... E4
TR10 ..... E3
TR11 ..... E1
TR12,13 ..... E3
TR14 ..... E1
TR15 ..... E4
TR16 ..... E3
TR17 ..... E1
TR18,19,20 ..... D3
TR21 ..... D2
TR22 ..... D1
TR23 ..... D4
TR24 ..... D2
TR25 ..... D4
TR26,27 ..... D2
TR28,29 ..... D1
TR03,31,32 ..... C3
TR33 ..... C2
TR34 ..... C1
TR35 ..... C4
TR36,37 ..... C2
TR38 ..... C3
TR39 ..... B4
TR40 ..... C2
TR41 ..... C1
TR42 ..... B1
TR43 ..... B4
TR44 ..... B1
TR45 ..... B4
TR46,47,48 ..... B2
TR49,50,51 ..... B1
TR52,53 ..... A4
TR54to58 ..... A3
TR59 ..... A2
TR60to63 ..... A1
TR64 ..... D2

TERMINAL
J1 ..... F4
J5,7 ..... F3
J10 ..... F2
P12 ..... E1
P52 ..... D1
P52,53,54 ..... C1
P55 ..... B4
P56 ..... A4
P57 ..... C4



VIDEO (EGN) PCB V1009A5280

TR1, 3 to 7, 9 to 15, 18, 27 to 33, 35 to 39, 41 to 44, 46, 47, 49 to 51, 53, 54, 56, 59 to 61 ---------- 2SC2603(D, E, F)
TR2 ---------- 2SC1213(C)
TR8, 16, 22, 25, 34, 40, 63 ---------- 2SA1115(D, E, F)
TR17 ---------- 2SB764(E, F)
TR19 to 21, 26 ---------- 2SD636(D, R, S)
TR23, 24, 45, 48, 52, 55, 58 ---------- 2SC458(C, D)
TR57 ---------- 2SC536K-NP(F)
TR64 ---------- 2SC536K-NP(E, F, G)



2SA1115
2SC2603

2SC458
2SC536K-NP
2SC1213

2SB764

2SD636

2. EGN P.C BOARD V1009B5290

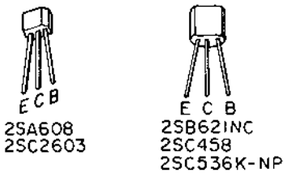
LOCATION OF COMPONENTS

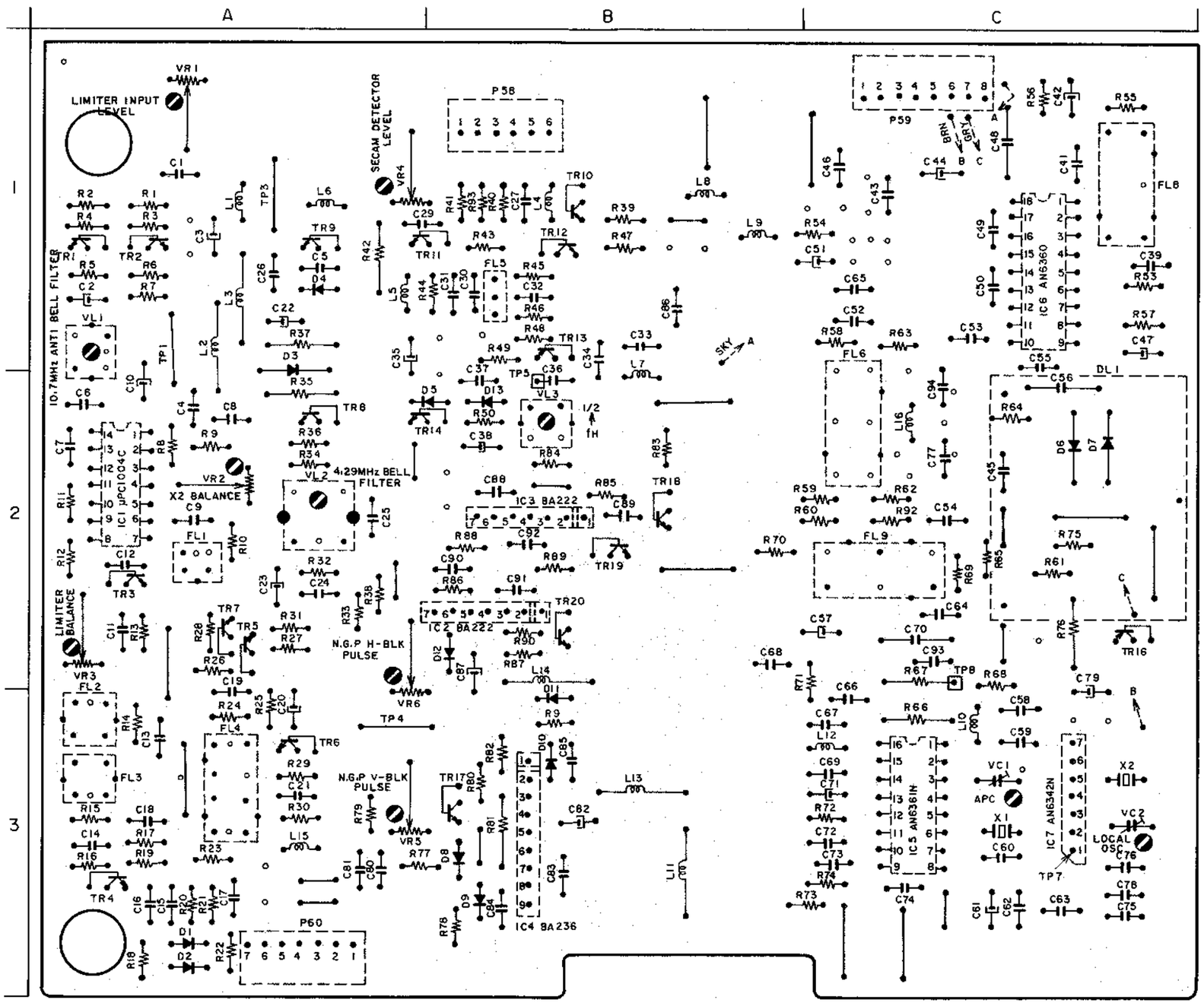
IC
IC1 ..... A2
IC2,3 ..... B3
IC4 ..... B3
IC5 ..... C3
IC6 ..... C1
IC7 ..... C3

TR
TR1,2 ..... A1
TR3 ..... A2
TR4 ..... A3
TR5 ..... A2
TR6 ..... A3
TR7,8 ..... A2
TR9 ..... A1
TR10to13 ..... B1
TR14 ..... B2
TR16 ..... C2
TR17 ..... B3
TR18to20 ..... B2

TERMINAL
P58 ..... B1
P59 ..... C1
P60 ..... A3

TR1,2,7,8,10,11
12,14,17,18,20---2SC536K-NP(E,F,G)
TR3,4,5,9-------2SC458(C,D)
TR6---------2SC2603(D,E,F)
TR13---------2SA608SP(E,F,G)
TR16---------2S862INC(Q,R,S)
TR19---------2SC536K-NP(F)





EGN PCB V100985290

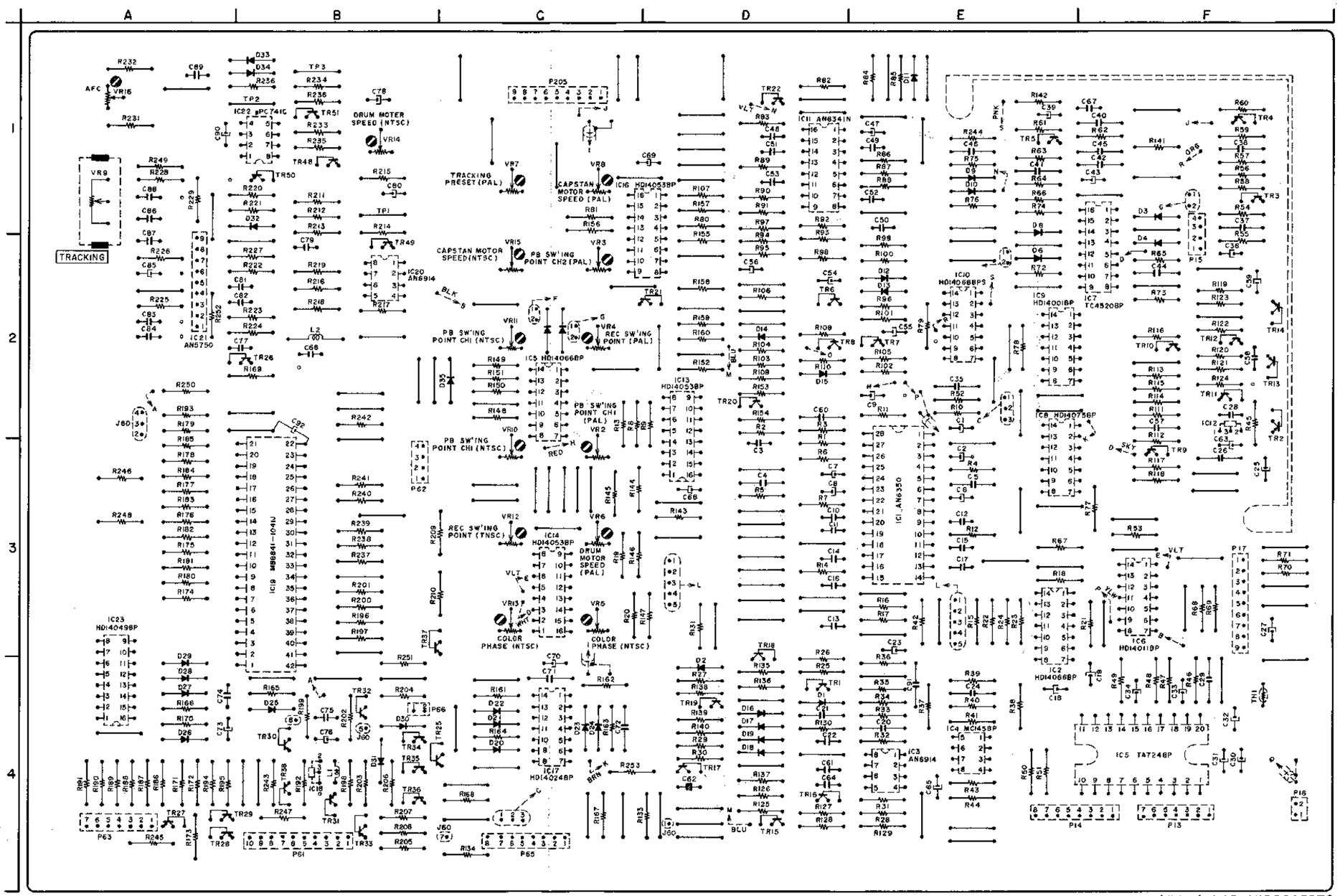
3. SERVO (EGN) P.C BOARD V1009A5270

LOCATION OF COMPONENTS

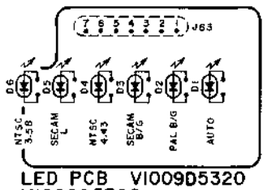
IC
IC1,2 ..... E3
IC3,4 ..... B4
IC5 ..... F4
IC6 ..... F3
IC7 ..... F2
IC8 ..... E3
IC9,10 ..... E2
IC11 ..... D1
IC12 ..... F2
IC13 ..... D2,3
IC14 ..... C3
IC15 ..... C2
IC16 ..... D1,2
IC17 ..... C4
IC18 ..... B4
IC19 ..... B4
IC20 ..... B2
IC21 ..... A2
IC22 ..... B1
IC23 ..... A4

TR
TR1 ..... D4
TR2 ..... F2
TR3,4 ..... F1
TR5 ..... E1
TR6 ..... D2
TR7 ..... E3
TR8 ..... D2
TR9 ..... F3
TR10to14 ..... F2
TR15to19 ..... D4
TR20,21 ..... D2
TR22 .. .. D1
TR25 ..... C4
TR26 ..... B2
TR27,28,29 ..... A4
TR30to36 ..... B4
TR37 ..... C3
TR38 ..... B4
TR48 ..... B1
TR49 ..... B2
TR50,51 ..... B1

TERMINAL
P13 ..... F4
P14 ..... E4
P15 ..... F1
P16 ..... F4
P17 ..... F3
P61 ..... B4
P62 ..... B3
P63 ..... A4
P65 ..... C4
P205 ..... C1
J60-1 ..... D4
J60-2,3,4 ... A4
J60-5,6 ..... B4
J66 ..... B4



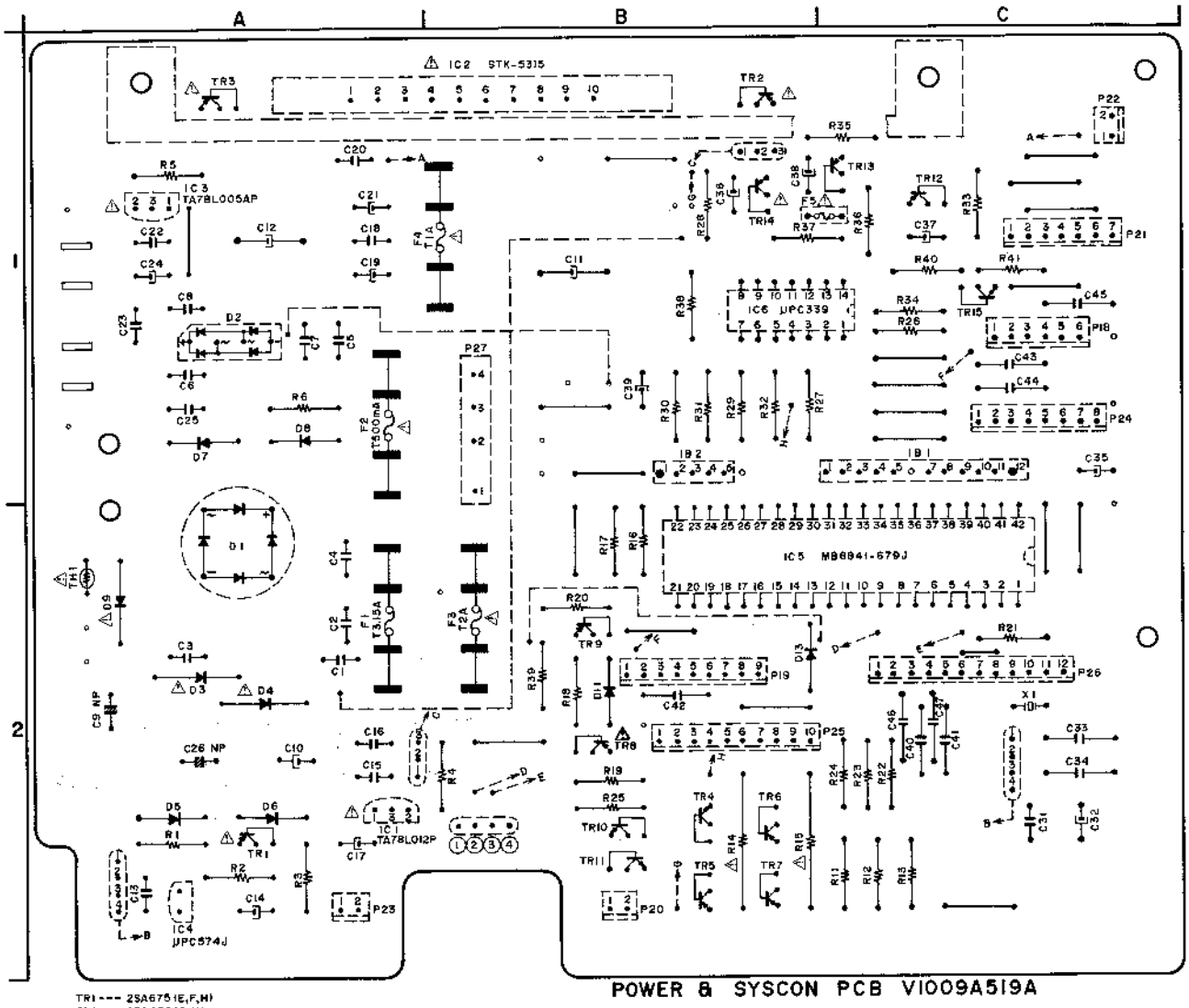
SERVO (EGN) PCB V1009A5270



LED PCB V1009D5320
V1009D5320

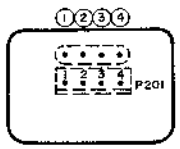
TR1,6,11,15,20,50 ---- 2SA1115(D,E,F)
TR3 to 5, 7 to 10, 16 to 19, 21, 22,
25 to 29, 30 to 36, 48, 51---2SC2603(D,E,F)
TR2 ----2SB632K(E,F)
TR12----2SD571(K,L,M)
TR13----2SB761(P)
TR14----2SC1983(R)
TR49 ---2SC536K-NP(F)

4. POWER & SYS. CON. P.C BOARD V1009A519A

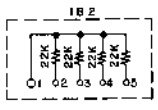


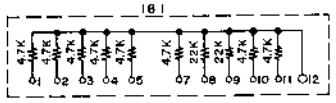
POWER & SYSCON PCB V1009A519A

TR1 --- 2SA675(E,F,H)
TR2 --- 2SA490(D,Y)
TR3 --- 2SB632K(D,E,F)
TR4 --- 2SD612K(D,E,F)
TR5,9 --- 2SA1115(D,E,F)
TR6 to 8,12 to 14 --- 2SB764(E,F)
TR10,15 --- 2SC2603(D,E,F)
TR11 --- 2SD863(E,F)

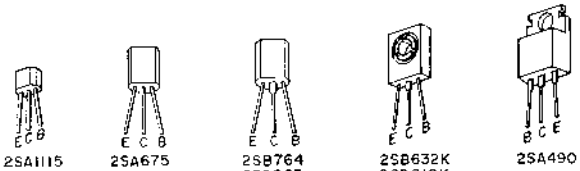


REMOCON TERMINAL
V1009A519D





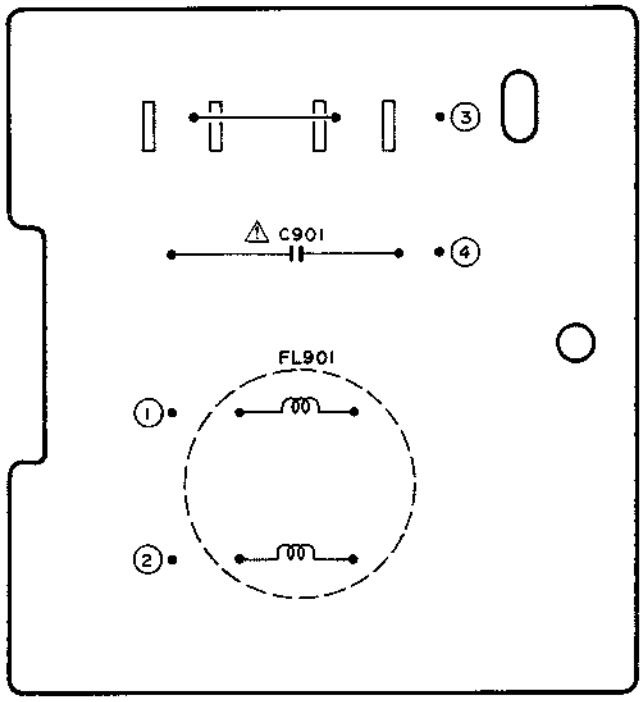
TR1	A-2	TR12	C-1
TR2	B-1	TR13	C-1
TR3	A-1	TR14	B-1
TR4	B-2	TR15	C-1
TR5	B-2	IC1	A-2
TR6	B-2	IC2	AB-1
TR7	B-2	IC3	A-1
TR8	B-2	IC4	A-2
TR9	B-2	IC4	B,C-2
TR10	B-2	IC6	B-1
TR11	B-2	IC5	



WARNING: ⚠INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS.

AVERTISSEMENT: ⚠IL INDIQUE LES COMPOSANTS CRITIQUES DE SÛRETÉ. POUR MAINTENIR LE DEGRÉ DE SÉCURITÉ DE L'APPAREIL NE REMPLACER LES COMPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SÉCURITÉ QUE PAR DES PIÈCES RECOMMANDÉES PAR LE FABRICANT.

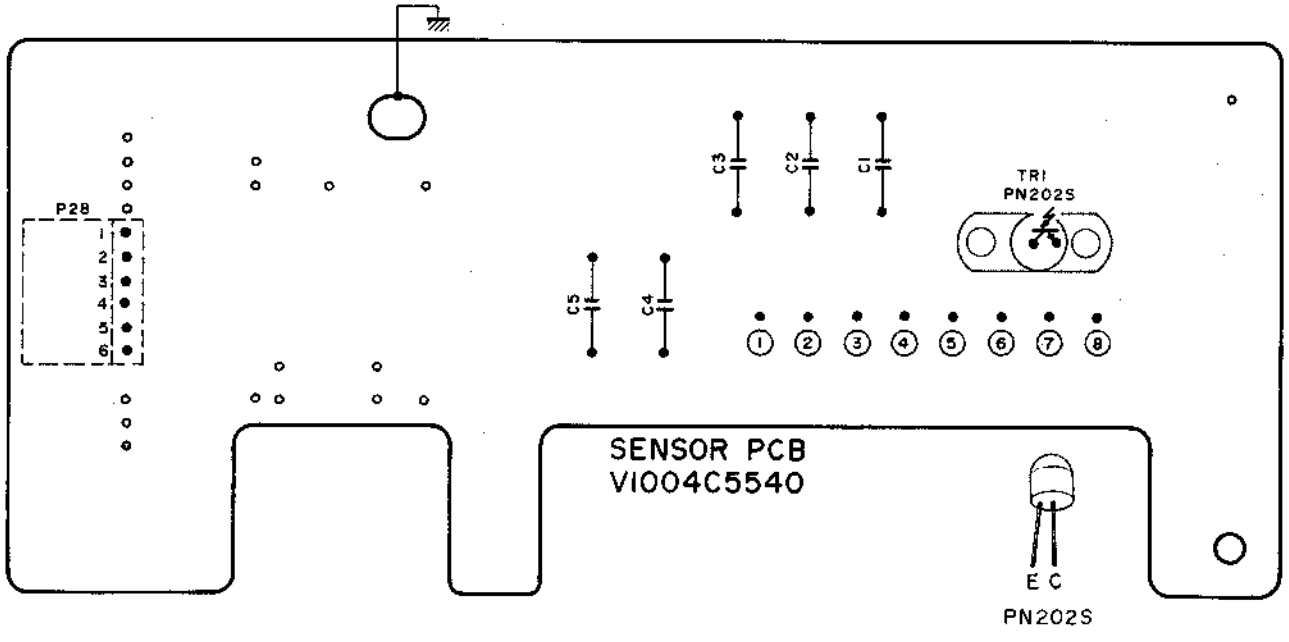
5. POWER FILTER P.C BOARD V1009D5200 (2ED)

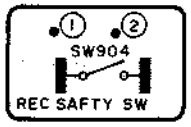


POWER FILTER PCB V1009D5200

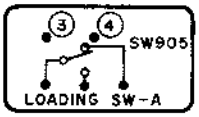
WARNING: ⚠INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS
AVERTISSEMENT: ⚠ IL INDIQU LES COMPOSANTS CRITIQUES DE SÛRETÉ. POUR MAINTENIR LE DEGRE DE SECURITE DE L'APPAREIL NE REMPLACER LES CONPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SECURITE QUE PAR DES PIECES RECOMMANDEES PAR LE FABRICANT

6. SENSOR P.C BOARD V1004C5540, R.S SW P.C BOARD V1004C5541, SW A P.C BOARD V1004C5542, SW B P.C BOARD V1004C5543 and EJ. S SW P.C BOARD V1004C5544

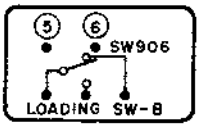




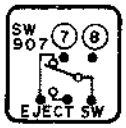
RS SW PCB
V1004C5541



SW-A PCB
V1004C5542

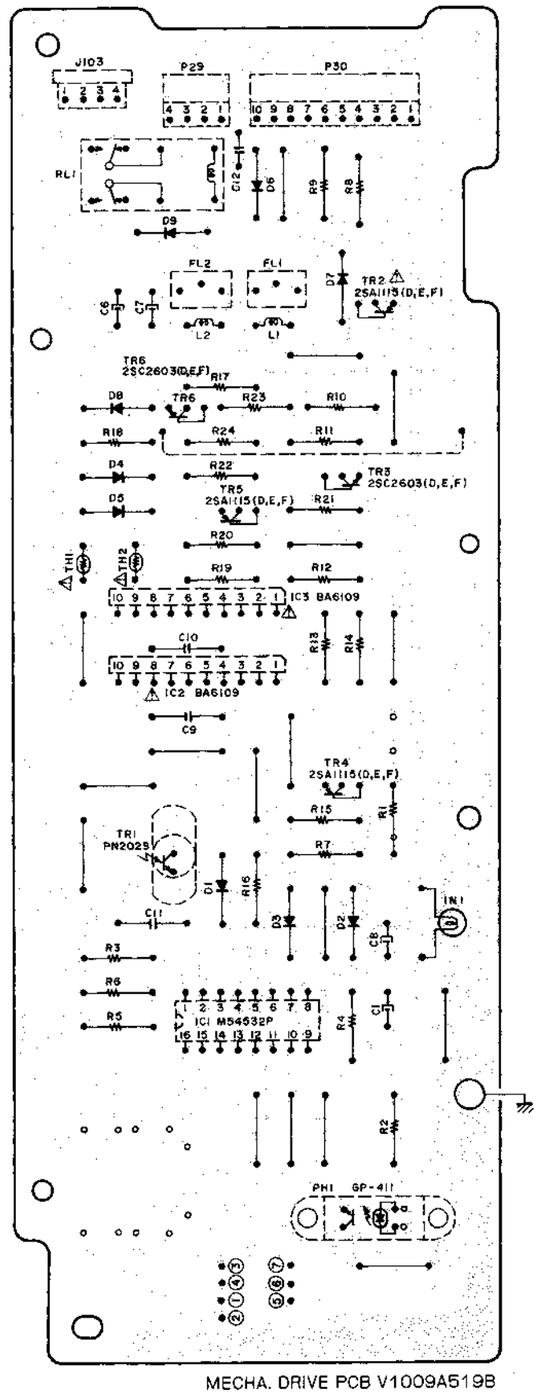


SW-B PCB
V1004C5543

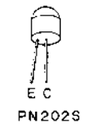


EJ S SW PCB
V1004C5544

7. MECHA. DRIVE P.C BOARD V1009A519B

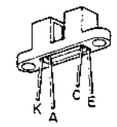


MECHA. DRIVE PCB V1009A519B



PN202S

2SA1115
2SC2603

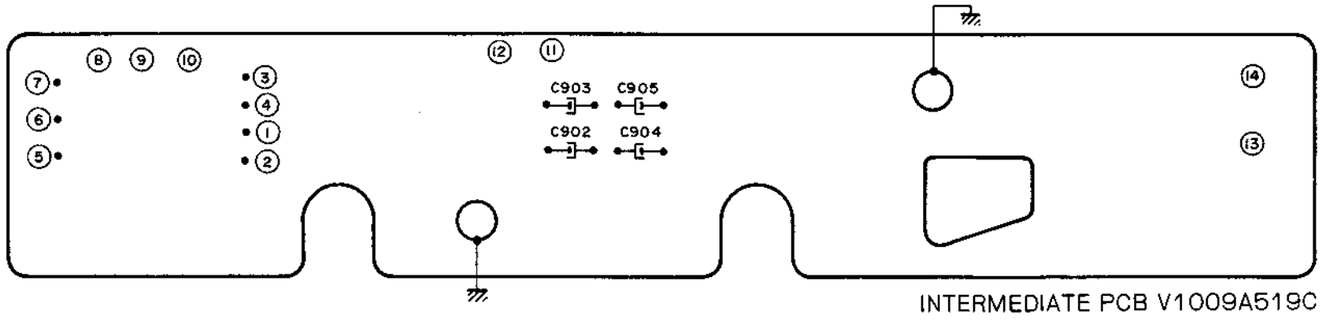


GP-411

WARNING: ⚠INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS

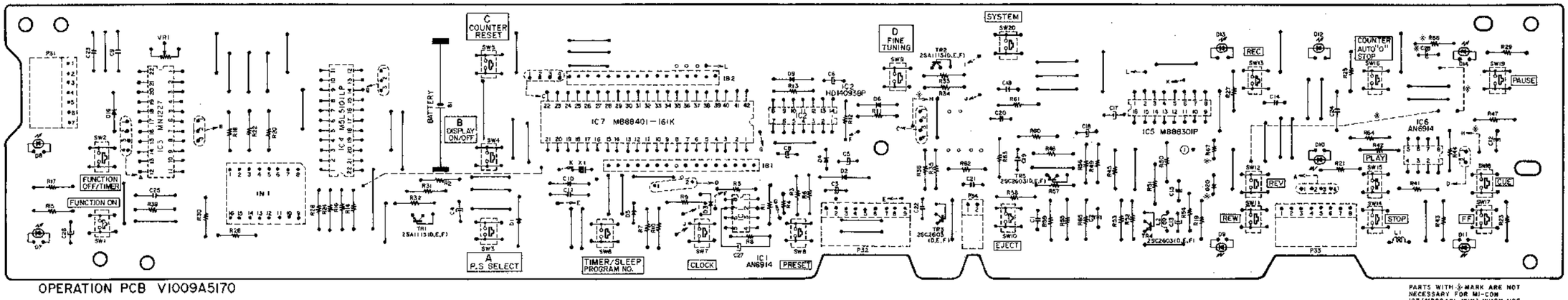
AVERTISSEMENT: ⚠IL INDIQU LES COMPOSANTS CRITIQUES DE SÛRETÉ. POUR MAINTENIR LE DEGRÉ DE SECURITE DE L'APPAREIL NE REMPLACER LES COMPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SECURITE QUE PAR DES PIECES RECOMMANDEES PAR LE FABRICANT

8. INTERMEDIATE P.C BOARD V1009A519C



INTERMEDIATE PCB V1009A519C

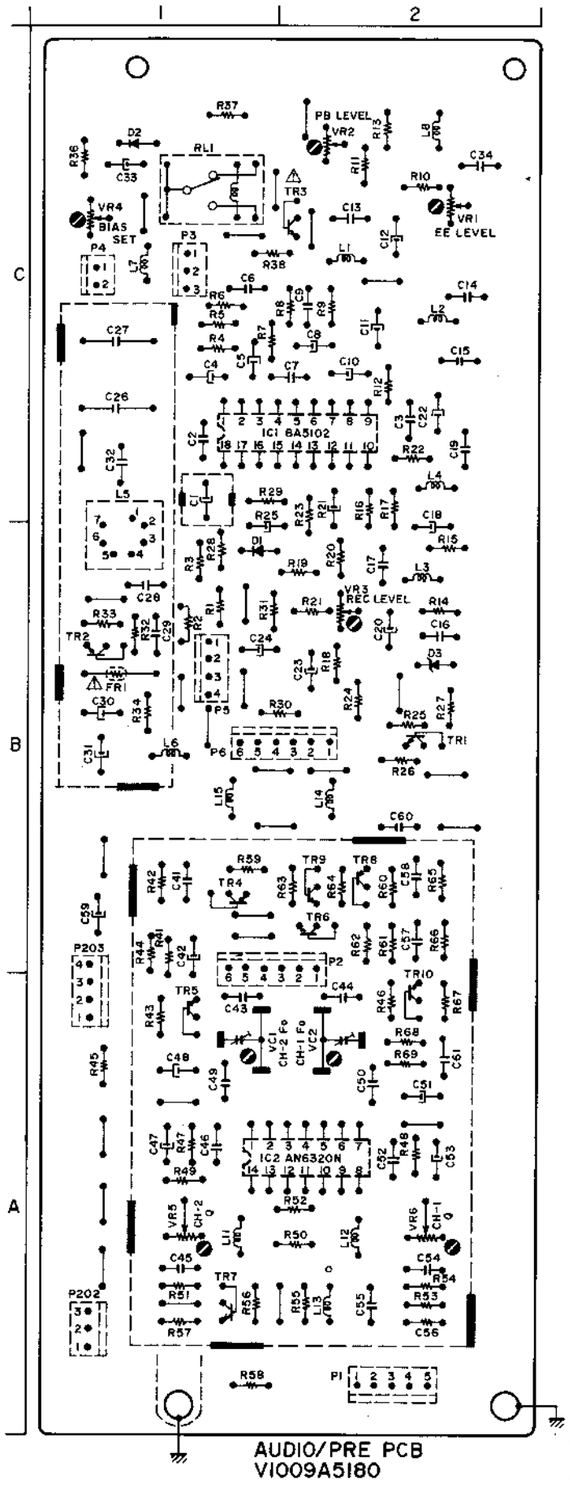
9. OPERATION P.C BOARD V1009A5170

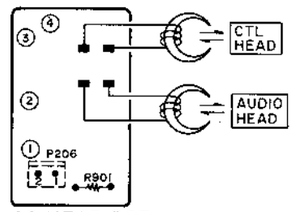


OPERATION PCB V1009A5170

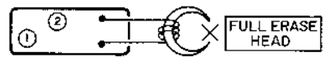
PARTS WITH ※ MARK ARE NOT NECESSARY FOR MI-CON IC TM88840I-151K) WHEN USE M88840I-161K PREASE REMOVE THEM

10. AUDIO/PRE P.C BOARD V1009A5180 and A/C HEAD P.C BOARD V1009D5230





AC HEAD PCB
V1009D5230



LOCATION

TR1 — B2
2 — B1
3 — C2
4 — B1
5 — A1
6 — B2
7 — A1
8 — B2
9 — B2
10 — A2

TR1, 3 to 6 — 2SC2603 (D,E,F)
TR2 ———— 2SC2001 (K,L,M)
TR7, 9, 10 — 2SC536K-NP (E,F,G)
TR8 ———— 2SA608 (E,F,G)

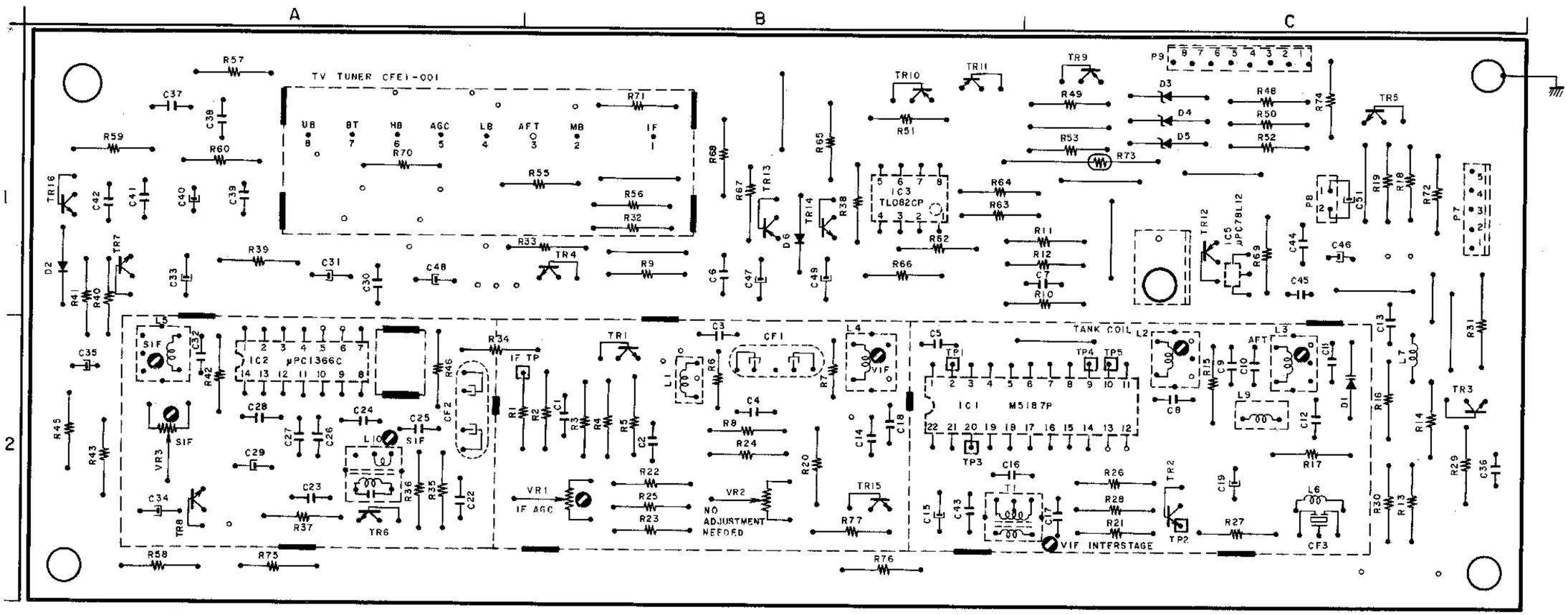
2SC2603

2SA608
2SC536K-NP
2SC2001

WARNING: △INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS

AVERTISSEMENT: △IL INDIQU LES COMPOSANTS CRITIQUES DE SÛRETÉ. POUR MAINTENIR LE DEGRÉ DE SECURITE DE L'APPAREIL NE REMPLACER LES CONPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SECURITE QUE PAR DES PIECES RECOMMANDÉES PAR LE FABRICANT

11. DEMODULATOR P.C BOARD 6C00034A1



LOCATION OF COMPONENTES

DEMODULATOR PCB 6C00034A1

IC

IC1 ------C2
IC2 ------A2
IC3 ------B1
IC5 ------C1

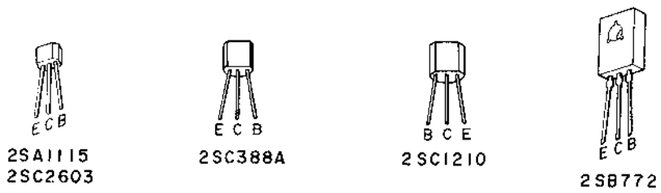
TR

TR1 ------B2
TR2,3 -----C1
TR4 ------B1
TR5 ------C1
TR6 ------A2
TR7 ------A1
TR8 ------A2
TR9 ------C1
TR10,11 ---B1
TR12 ------C1
TR15 ------B2
TR16 ------A1

TERMINAL

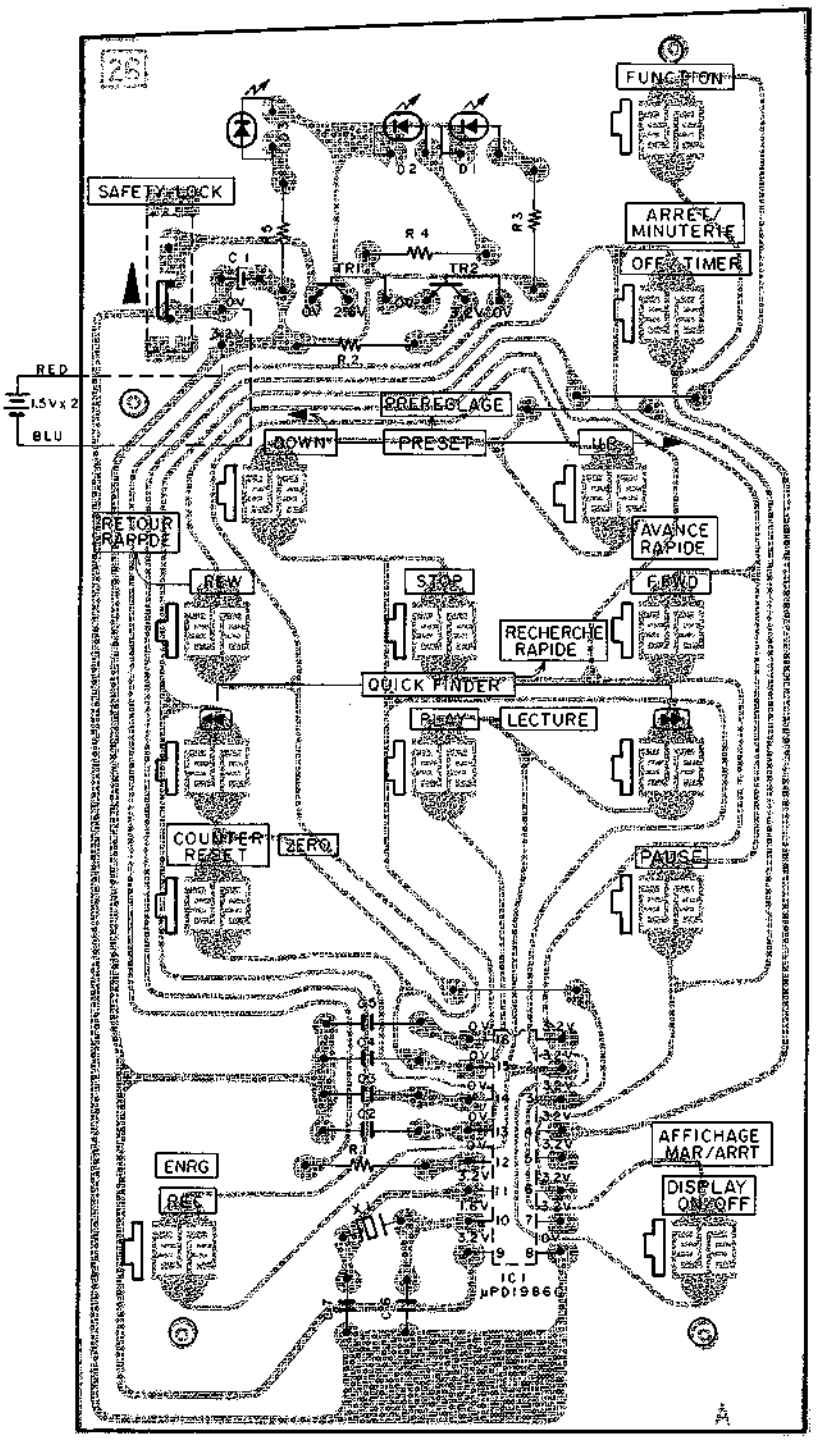
P7 to 9 ----C1

TR1,6 -------2SC388A
TR2,4,5,7,8 14to16--2SC2603(D,E)
TR3 --------2SC1210(D,E)
TR9 to 11 ------2SA1115(F)
TR12 -------2SB772(E,F)
TR13 -------2SA1115(D,E)



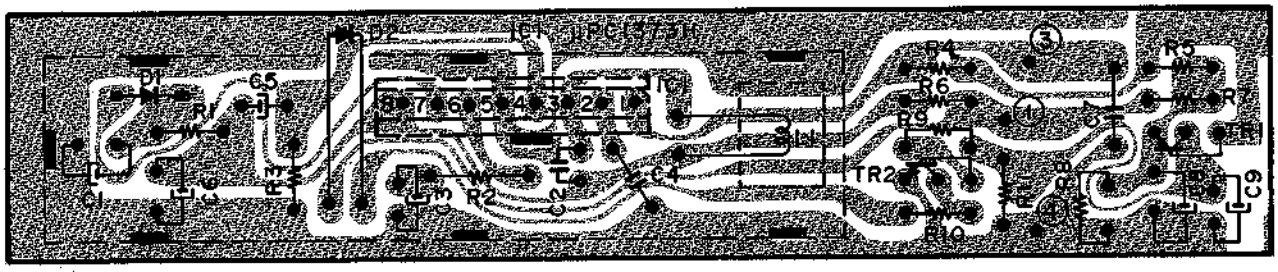
12. REMOTE CONTROL UNIT RC-V202

1) TRANSMITTER RC-T2



TR1--2SI115(D,E,F)
TR2--2SC2603(D,E,F)

2) RECEIVER RC-R2



SECTION 2

PARTS LIST

TABLE OF CONTENTS

ATTENTION

1. When placing an order for parts, be sure to list the parts no. model no., and description. There are instances in which if any of this information is omitted, parts cannot be shipped or the wrong parts will be delivered.
2. Please be careful not to make a mistake in the parts no. If the parts no. is in error, a part different from the one ordered may be delivered.
3. Because parts number and parts unit supply in the Preliminary Parts List may be partially changed, please use this parts list for all future reference.

HOW TO USE THIS PARTS LIST

1. This Parts List shows the parts that are considered necessary for repairs. Other parts, such as resistors and capacitors, are shown in the "Common List for Service Parts". Select and order such parts from the "Common List for Service Parts".
2. The Recommended Spare Parts shows those parts in the Parts List which are considered particularly important for service.
3. Parts not shown in the Parts List and "Common List for Service Parts" will not be supplied in principle.
4. How to read list

a) Mechanism Block

2. HEAD BASE BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
2-1x	BH-T2023A320A	HEAD BASE BLOCK GX-F66R
2-2	HP-H2206A010A	HEAD R/P PR4-8FU C
2-3	ZS-477876	PAN20×03STL CMT
2-4	ZS-536488	BID20×08STL CMT
2-5	ZG-402895	CS ANGLE ADJUST SPRING

- SP (Service Parts) Classification
- A small "x" indicates the inability to show that particular part in the Photo or Illustration.
- This number corresponds with the individual parts index number in that figure
- This number corresponds with the Figure Number

b) P.C Board Block

6. SYS. CON. P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
6-1	BA-T2034A070A	PC SYS CON BLK GX-F44R
6-IC1	EI-324536	IC HD14049BP
6-IC2	EI-336801	IC MB8841-564M
6-IC3	EI-331661	IC SN7405N
6-IC4	EI-336725	IC M54527P
6-TR1to4	ET-200985	TR 2SC2603 F,G
6-TR5to28	ET-554657	TR 2SA733A P,Q
6-D1	ED-318292	D SILICON H 1S2473T-77 T26
6-D2to4	ED-308952	D GERMA V 1K34A-LR F07
6-D5to10	ED-318292	D SILICON H 1S2473T-77 T26
6-X1	EI-318384	OSC X'TAL NC-18C 3.579545MHZ

- SP (Service Parts) Classification
- This reference numbers corresponds with symbol numbers of Schematic Diagrams.

5. Both the kind of part and installation position can be determined by the Parts Number. To determine where a parts number is listed, utilize Parts Index at end of Parts List. It is necessary first of all to find the Parts Number. This can be accomplished by using the Reference Number listed at right of parts number in the Parts Index.

WARNING

⚠ INDICATES SAFETY CRITICAL COMPONENTS FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS

AVERTISSEMENT

⚠ IL INDIQUE LES COMPOSANTS CRITIQUES DE SÉCURITÉ. POUR MAINTENIR LE DEGRÉ DE SÉCURITÉ DE L'APPAREIL, NE REMPLACER QUE DES PIÈCES RECOMMANDÉES PAR LE FABRICANT

I. MODEL VS-2EGN

RECOMMENDED SPARE PARTS

Because, if the parts listed below are on hand, almost any repair can be accomplished, we suggest that you stock these Recommended Spare Parts Items.

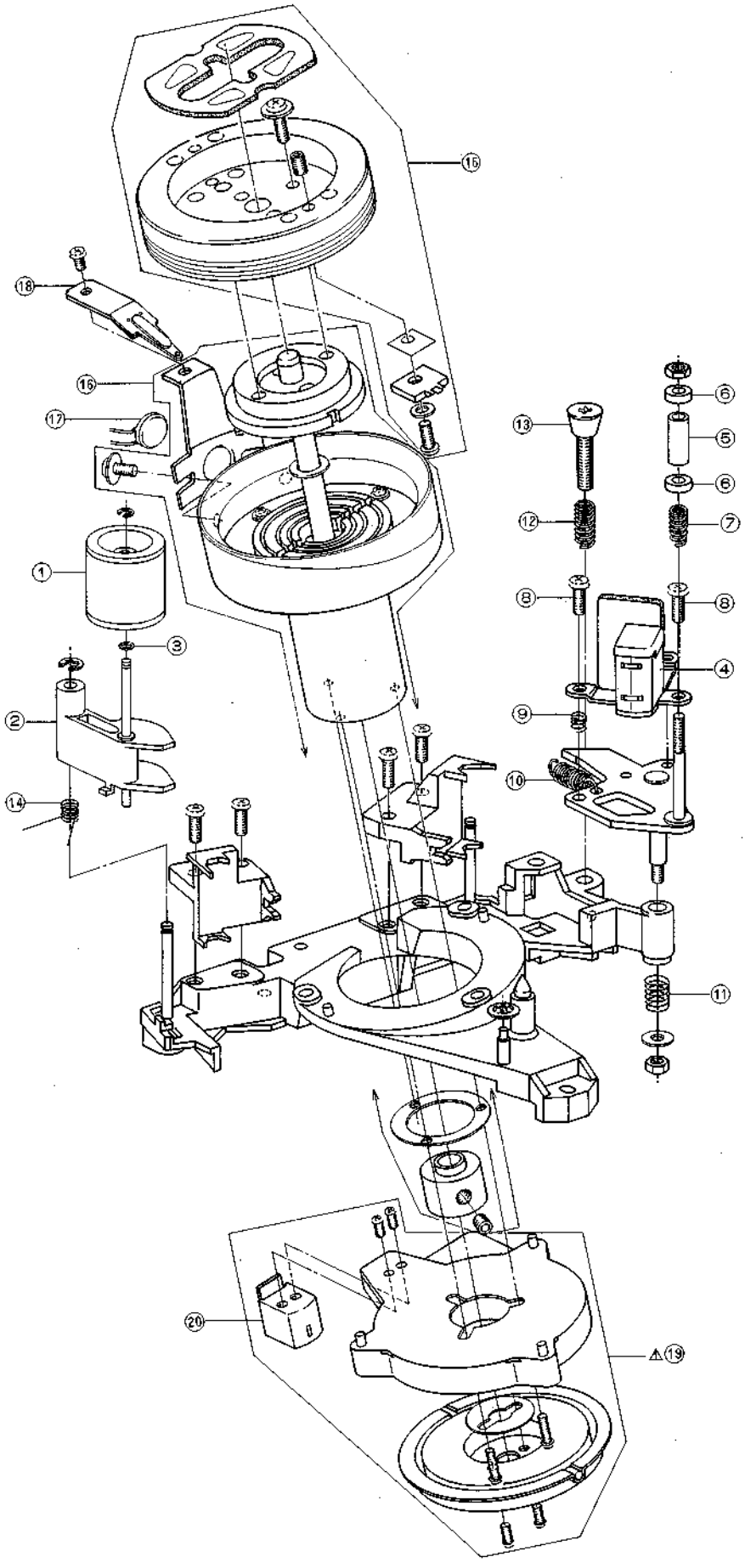
REF. NO.	PARTS NO.	DESCRIPTION
1	AX-337517	BATTERY 2/60DK
2	BH-VI009A180A	LOWER DRUM BLK VS-2EG
3	BH-VI004A280A	UPPER DRUM BLK VS-5EG
4	BM-337513	⚠ MOTOR DDV5-1E
5	BM-337512	⚠ MOTOR FG DMF-4917
6	BM-337510	⚠ MOTOR VY220B13
7	BM-780048	L MOTOR SUB ASSY (2)
8	BR-317908	SUPPLY REEL TABLE BLK
9	BR-327789	TU REEL TABLE ASSY
10	BT-344150	⚠ TRANS POWER VS-2-1A
11	BV-330111	⚠ ANT BOOSTER YBC1-001
12	BV-330109	⚠ RF CONVERTER MDK3-253
13	BV-VI004A160A	ROLLER PINCH BLK VS-5EG
14	BV-327815	TU IDLER ASSY
15	ED-332283	D LED SG205D GRN
16	ED-318988	D LED SR505D RED
17	ED-337587	D LED TLG321 GRN
18	ED-337617	D SILICON DBB50C-K8 200/5.0A
19	ED-337618	D SILICON DS135E-FB6 100/1.0A
20	ED-301911	D SILICON H DS448
21	ED-200469	D SILICON H DS448 FA5 F10
22	ED-337575	D SILICON H GMA-01-4-BT T26
23	ED-309437	D SILICON H 1S1926-M
24	ED-604541	D SILICON H 1S2076
25	ED-624903	D SILICON H 1S2473
26	ED-560913	D SILICON V 1S2473VE
27	ED-323979	D SILICON W03B F12 100/1.0A
28	ED-322238	D SILICON 1B4B41 100/1.0A
29	ED-705479	D SILICON 1SV70
30	ED-742650	D ZENER HZ9B3
31	ED-338553	D ZENER V HZ6B-1S1
32	ED-323892	PHOTO SENSOR GP-411P
33	EE-337170	TV TUNER CDE1-015
34	EF-593706	⚠ FUSE SEMKO T 250V 0.50A
35	EF-623103	⚠ FUSE SEMKO T 250V 1A
36	EF-601301	⚠ FUSE SEMKO T 250V 2A
37	EF-691007	⚠ FUSE SEMKO T 250V 3.15A
38	EI-322365	DL EFD-EN645A11E
39	EI-337468	DL EFD-JR124A13D
40	EI-337888	DL EFD-KR645B85C
41	EI-337940	DL EFD-WR645A12G
42	EI-201970	IC AN5750
43	EI-324204	IC AN6310
44	EI-321076	IC AN6320N
45	EI-321604	IC AN6341N
46	EI-324203	IC AN6342N
47	EI-326044	IC AN6350
48	EI-324151	IC AN6360
49	EI-337705	IC AN6361N
50	EI-324160	IC AN6362
51	EI-337717	IC AN6363
52	EI-324182	IC AN6371
53	EI-337469	IC AN6914
54	EI-337624	IC BA222
55	EI-337625	IC BA236
56	EI-332286	IC BA5102
57	EI-330352	IC BA6109
58	EI-322309	IC HA11703
59	EI-324107	IC HA11718
60	EI-324795	IC HD14001BP
61	EI-321350	IC HD14011BP
62	EI-325992	IC HD14024BP
63	EI-324536	IC HD14049BP
64	EI-328593	IC HD14053BP
65	EI-200497	IC HD14066BP
66	EI-324690	IC HD14075BP
67	EI-338346	IC HD14093BP
68	EI-337519	IC MB88301-P
69	EI-338537	IC MB88401-161K
70	EI-337531	IC MB8841-679J
71	EI-337687	IC MB8841-1041J
72	EI-310183	IC MC14001BCP
73	EI-330393	IC MC1458P
74	EI-337518	IC MN1227A
75	EI-330475	IC M5L510P
76	EI-704201	IC M5144P
77	EI-337528	IC STK-5315
78	EI-307574	IC TA7060AP
79	EI-337589	IC TA7248P
80	EI-705494	IC TA7607AP
81	EI-337529	IC TA78L005AP
82	EI-337470	IC TA78L012AP
83	EI-344166	IC TA78L012P
84	EI-300834	IC TC4520BP
85	EI-301744	IC μA741TC
86	EI-337549	IC μPC1004C
87	EI-318332	IC μPC339C
88	EI-337530	IC μPC574J
89	EI-301749	IC μPC741C
90	EI-318384	OSC X'TAL NC-18C 3.579545MHz
91	EI-309878	OSC X'TAL 4.433619MHz
92	EJ-301513	⚠ SOCKET INLET S-I6453 E 2P
93	EL-330446	PL SPL HOLDER LAMP
94	EO-322334	COIL TUN 1 T-1-B 4.29MHz
95	EO-324478	COIL TUN 1 T-7-A 1.07MHz
96	EO-325093	COIL VARI 1 T-6 8.2mH
97	EO-330256	OSC CE F85-006 4MHz
98	EP-337504	⚠ SOLENOID W/TAP 1240PLT
99	EP-200175	RELAY SIGNAL G2E 1TR 12V
100	EP-337416	RELAY SIGNAL G2V-282P-NL 2TR 12V
101	ER-318647	⚠ R FUSE ERD2FC S10 1/4W 4R7J
102	ER-705505	⚠ R FUSE W 1/4W 220J
103	ER-742639	⚠ R FUSE 1/4W 100J
104	ER-705499	FILTER CE SFE 5.5MHz
105	ER-328237	FILTER CE SFE4.5MB 4.5MHz
106	ER-705501	FILTER CE TPS 5.5MHz
107	ER-337715	FILTER LC AP GYV-565-1A
108	ER-322325	FILTER LC AP LCB-5-A
109	ER-324339	FILTER LC AP LCB-56
110	ER-337626	FILTER LC AP LCB-82
111	ER-337701	FILTER LC BP DXV-350-1B 3.58MHz
112	ER-337702	FILTER LC BP DXV-363-1A 3.58MHz
113	ER-337703	FILTER LC BP DXV-367-1A 4.21MHz
114	ER-324375	FILTER LC BP LCB-57 4.43MHz
115	ER-324470	FILTER LC BP LCB-60 4.43MHz
116	ER-325807	FILTER LC BP LCB-61 5.06MHz
117	ER-324471	FILTER LC BP LCB-74 4.43MHz
118	ER-324472	FILTER LC BP LCB-75 2.16MHz
119	ER-324473	FILTER LC BP LCB-76 2.32MHz
120	ER-330465	FILTER LC DST310-55B271M
121	ER-324305	FILTER LC HP LCB-53
122	ER-337711	FILTER LC LP DXV-265-1A
123	ER-337713	FILTER LC LP DXV-266-1A
124	ER-337706	FILTER LC LP LCB-83
125	ER-324398	FILTER LC LP LCB-58
126	ER-324469	FILTER LC LP LCB-59
127	ER-332221	FILTER LC LP LCB-78
128	ER-337472	FILTER LC LP LCB-81
129	ER-742662	FILTER SAW SAF38.9MZ51Z
130	ER-337939	R COMP FRE15-333M
131	ER-337515	R COMP 01-0419
132	ES-337509	⚠ SW SEESAW SDE3S-E 02-1 E
133	ES-309312	⚠ SW SLIDE 22293B 02-2
134	ES-318284	SW LEVER SCL101R23A 1-01-02N
135	ES-319124	SW LEVER SCL101S 1-01-02N
136	ES-319156	SW MICRO SS-1-E-4 UC
137	ES-337521	SW TACT KHH-10908
138	ET-318308	TR PHOTO PN202S
139	ET-307997	TR 2SA1115 D, E
140	ET-200479	TR 2SA1115 D, E, F
141	ET-742648	TR 2SA1115 F, G
142	ET-633677	TR 2SA490 O, Y
143	ET-322778	TR 2SA608K-NP E, F, G
144	ET-332402	TR 2SA608SP E, F, G
145	ET-337569	TR 2SA675 E, F, H
146	ET-330543	TR 2SB621NC Q, R, S

REF. NO.	PARTS NO.	DESCRIPTION
147	ET-330430	TR 2SB632K D, E, F
148	ET-322598	TR 2SB632K E, F
149	ET-337501	TR 2SB761 P
150	ET-318237	TR 2SB764 E, F
151	ET-330427	TR 2SB772 E, P
152	ET-522270	TR 2SC1210 D
153	ET-321644	TR 2SC1213 C
154	ET-325899	TR 2SC1983 R
155	ET-322412	TR 2SC2001 K, L, M
156	ET-330464	TR 2SC2603 D, E
157	ET-200480	TR 2SC2603 D, E, F
158	ET-200505	TR 2SC2603 E, F
159	ET-742646	TR 2SC388A
160	ET-309334	TR 2SC458 C, D
161	ET-322775	TR 2SC536K-NP E, F, G
162	ET-328272	TR 2SC536K-NP F
163	ET-246846	TR 2SC536NP E, F, G, H
164	ET-332313	TR 2SC536SP E, F, G
165	ET-200741	TR 2SD571 K, L, M
166	ET-307193	TR 2SD612K D, E, F
167	ET-200412	TR 2SD636 Q, R, S
168	ET-318239	TR 2SD863 E, F
169	EV-344479	C S-FIX H CTZ54C111 2.0-10
170	EV-648753	R S-FIX H CR19R 3P 0.50W 473
171	EV-341214	R S-FIX H CR19R 3P 0.50W 683
172	EV-307620	R S-FIX H H0651A 3P 0.05W 222
173	EV-336852	R S-FIX H KVSF807U 3P 102
174	EV-336853	R S-FIX H KVSF807U 3P 103
175	EV-336854	R S-FIX H KVSF807U 3P 104
176	EV-336850	R S-FIX H KVSF807U 3P 202
177	EV-336843	R S-FIX H KVSF807U 3P 303
178	EV-336847	R S-FIX H KVSF807U 3P 502
179	EV-341225	R S-FIX H KVSF807U 3P 503
180	EV-551643	R S-FIX H SR19R 3P 0.15W 331
181	EV-330863	R S-FIX H SR19R 3P 0.15W 333
182	EV-361800	R S-FIX H SR19R 3P 0.15W 471
183	EV-443733	R S-FIX H SR19R 3P 0.15W 683
184	EV-337957	R S-FIX H TM64K3 3P 0.30W 102
185	EV-337958	R S-FIX H TM64K3 3P 0.30W 202
186	EV-337948	R S-FIX H TM64K3 3P 0.30W 203
187	EV-702567	R S-FIX TT24R 202
188	EV-702568	R S-FIX TT24R 502
189	EV-475470	R S-FIX V V8K1-1 3P 103
190	EV-341256	R S-FIX V V8K1-1 3P 301
191	EV-341257	R S-FIX V V8K1-1 3P 302
192	EV-464264	R S-FIX V V8K1-1 3P 503
193	EV-337499	VR ROTARY 16P10x1L B104
194	HC-337506	HEAD CTL WY-3703HW
195	HE-337507	HEAD E WY-3603Z
196	MB-326474	BELT CAPSTAN
197	MB-322303	BELT DETECTION
198	MI-327773	IDLER ASSY
199	MI-326478	ROLLER IMPEDANCE

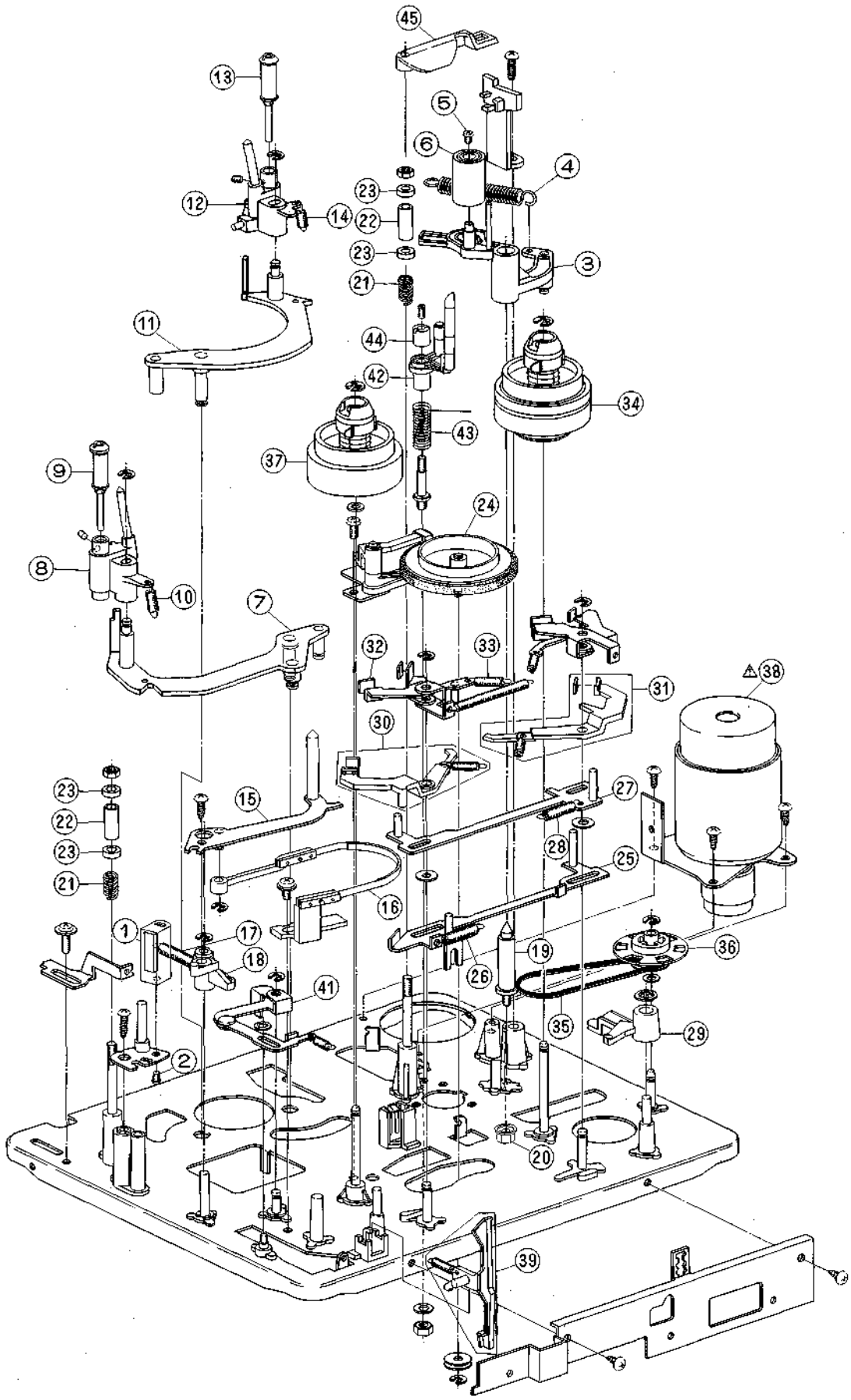
1. HEAD DRUM BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
		ROLLER IMPEDANCE BLOCK
1-1	MI-326478	ROLLER IMPEDANCE
1-2	BL-B327729	LEVER LZ PART
1-3	ZW-259334	PW 2.05x035x025PSL
		AC. H BLOCK
1-4	HC-337506	HEAD CTL WY-3703HW
1-5	HZ-343076	GUIDE TAPE (C)
1-6	HZ-342726	GUIDE TAPE (B)
1-7	ZG-328225	SP C-3.5/0.8-10.0G C-102G
1-8	ZS-380046	PAN30x10 STL CMT
1-9	ZG-327757	SP PULL ACH SET
1-10	ZG-313257	SP C-3.5/0.8-8.0 C-101
		DRUM BASE BLOCK
1-11	ZG-331178	SP PUSH PRESS ACH
1-12	ZG-332979	SP PUSH CTL(B)
1-13	ZS-332978	SCREW ADJUST
1-14	ZG-327740	SP TORSION LZ
		UPPER DRUM BLOCK
1-15	BH-V1004A280A	UPPER DRUM BLK VS-5EG
		LOWER DRUM BLOCK
1-16	BH-V1009A180A	LOWER DRUM BLK VS-2EG
		POSISTER BLOCK
1-17	ET-337508	POSISTER PTH499D19BG500QD30
		HEAD DRUM BLOCK
1-18	BV-342208	HOLDER EARTH ASSY
1-19	BM-337513	⚠ MOTOR DDV5-3E
1-20	VT-318213	HEAD PU SS-6EMC

HEAD DRUM BLOCK



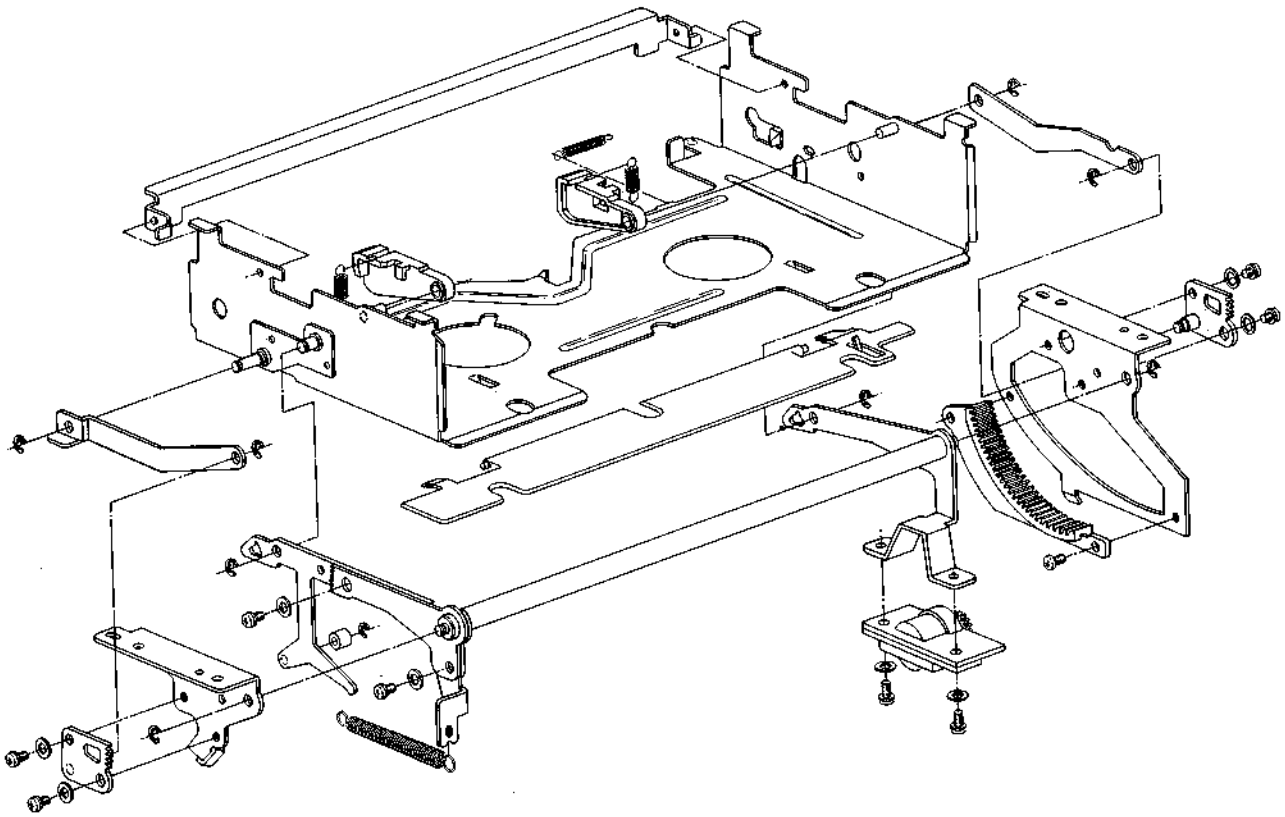
MECHA FRAME BLOCK (1)



2. MECHA FRAME BLOCK (1)

REF. NO.	PARTS NO.	DESCRIPTION
	HOLER ERASE HEAD BLOCK	
2-1	HE-337507	HEAD E WY-3603Z
2-2	ZS-477876	PAN20x03 STL CMT
	LEVER PINCH ROLLER BLOCK	
2-3	BL-B326296	LEVER PINCH ROLLER PART
2-4	ZG-330058	SP T2-6.3/0.8-45 T2-202
2-5	ZS-477876	PAN20x03 STL CMT
	ROLLER PINCH BLOCK	
2-6	BV-V1004A160A	ROLLER PINCH BLK VS-5EG
	LEVER LOADING (L) BLOCK	
2-7	BL-B326329	LEVER LOADING (L) PART
2-8	VT-B319445	LOADING LEADER (L) PART
2-9	VT-317947	VERTICAL POLE PART (P)
2-10	ZG-318043	SP LEADER
	LEVER LOADING (R) BLOCK	
2-11	BL-B326347	LEVER LOADING (R) PART
2-12	VT-B319446	LOADING LEADER (R) PART
2-13	VT-317947	VERTICAL POLE PART (P)
2-14	ZG-318043	SP LEADER
	TENSION ARM BLOCK	
2-15	BL-B326468	LEVER TENSION PART
2-16	VT-328134	TENSION BAND ASSY
2-17	ZG-331128	SP T2-4.0/0.4-45 T2-120
2-18	VT-326470	HOLDER TENSION LEVER
	MECHA FRAME BLOCK	
2-19	MH-321688	PROP 9 PINCH ROLLER LEVER
2-20	ZS-609434	N FRANGE 30STL CMT
2-21	ZG-328225	SP C-3.5/0.8-10.0G C-102G
2-22	HZ-343076	GUIDE TAPE (C)
2-23	HZ-342726	GUIDE TAPE (B)
2-24	MI-327773	IDLER ASSY
2-25	BL-B322090	LEVER BRAKE SLIDE (B) PART
2-26	ZG-313045	SP T1-5.0/0.55-25.0 T1-158
2-27	BL-B322027	LEVER BRAKE SLIDE (A) PART
2-28	ZG-332463	SP T2-3.2/0.29-20 T2-064
2-29	ML-330640	LEVER BRAKE RELEASER
2-30	BL-V1004A090A	LEVER FF BRAKE BLK VS-5EG
2-31	BL-V1004A100A	LEVER REW BRAKE BLK VS-5EG
2-32	VT-322159	SHEET BRAKE (A)
2-33	ZG-318204	SP T2-3.2/0.29-16 T2-062
2-34	BR-327789	TU REEL TABLE ASSY
2-35	MB-322303	BELT DETECTION
2-36	MI-322304	WHEEL DETECTION
2-37	BR-317908	SUPPLY REEL TABLE BLK
2-38	BM-337512	⚠ MOTOR FG DMF-4917
2-39	BL-V1004A170A	LEVER REC SAFETY BLK VS-5EG
	ASSEMBLY BLOCK	
2-40x	VT-342116	HOLDER REMOCON CONNECTOR
2-41	BL-B321741	LEVER RELEASE PART
2-42	BL-B326220	LEVER REVIEW PART
2-43	ZG-326247	SP TORSION REVIEW
2-44	ZS-326246	NUT ADJUST
2-45	VT-326477	GUIDE CAP

EJECTOR BLOCK



4. EJECTOR BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
4-1	BV-327845	EJECTOR ASSY

5. VIDEO (EGN) P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
5-1	BA-VI009A290A	PC VIDEO (EGN) BLK VS-2EGN
5-IC1	EI-324204	IC AN6310
5-IC2	EI-324107	IC HA11718
5-IC3	EI-301744	IC μA741TC
5-IC4	EI-307574	IC TA7060AP
5-IC5	EI-328593	IC HD14053BP
5-IC6	EI-322309	IC HA11703
5-IC7	EI-200497	IC HD14066BP
5-IC8	EI-337717	IC AN6363
5-IC9	EI-324160	IC AN6362
5-IC10	EI-324151	IC AN6360
5-IC11	EI-324182	IC AN6371
5-IC12	EI-324203	IC AN6342N
5-IC13	EI-310183	IC MC14001BCP
5-IC14	EI-310183	IC MC14001BCP
5-IC15	EI-328593	IC HD14053BP
5-IC16	EI-337470	IC TA78L012AP
5-TR1	ET-200480	TR 2SC2603 D, E, F
5-TR2	ET-321644	TR 2SC1213 C
5-TR3 to 7	ET-200480	TR 2SC2603 D, E, F
5-TR8	ET-200479	TR 2SA1115 D, E, F
5-TR9 to 15	ET-200480	TR 2SC2603 D, E, F
5-TR16	ET-200479	TR 2SA1115 D, E, F
5-TR17	ET-318237	TR 2SB764 E, F
5-TR18	ET-200480	TR 2SC2603 D, E, F
5-TR19to21	ET-200412	TR 2SD636 Q, R, S
5-TR22	ET-200479	TR 2SA1115 D, E, F
5-TR23,24	ET-309334	TR 2SC458 C, D
5-TR25	ET-200479	TR 2SA1115 D, E, F
5-TR26	ET-200412	TR 2SD636 Q, R, S
5-TR27to33	ET-200480	TR 2SC2603 D, E, F
5-TR34	ET-200479	TR 2SA1115 D, E, F
5-TR35to39	ET-200480	TR 2SC2603 D, E, F
5-TR40	ET-200479	TR 2SA1115 D, E, F
5-TR41to44	ET-200480	TR 2SC2603 D, E, F
5-TR45	ET-309334	TR 2SC458 C, D
5-TR46,47	ET-200480	TR 2SC2603 D, E, F
5-TR48	ET-309334	TR 2SC458 C, D
5-TR49to51	ET-200480	TR 2SC2603 D, E, F
5-TR52	ET-309334	TR 2SC458 C, D
5-TR53,54	ET-200480	TR 2SC2603 D, E, F
5-TR55	ET-309334	TR 2SC458 C, D
5-TR56	ET-200480	TR 2SC2603 D, E, F
5-TR57	ET-246846	TR 2SC536NP E, F, G, H
5-TR58	ET-309334	TR 2SC458 C,D
5-TR59	ET-200480	TR 2SC2603 D, E, F
5-TR60	ET-200505	TR 2SC2603 E, F
5-TR61	ET-200480	TR 2SC2603 D, E, F
5-TR62	ET-200505	TR 2SC2603 E, F
5-TR63	ET-200479	TR 2SA1115 D, E, F
5-TR64	ET-200412	TR 2SD636 Q, R, S
5-D1 to 3	ED-301911	D SILICON H DS448
5-D4, 5	ED-309437	D SILICON H 1S1926-M
5-D6, 7	ED-301911	D SILICON H DS448
5-D8, 9	ED-309437	D SILICON H 1S1926-M
5-D10 to 22	ED-337575	D SILICON H GMA-01-4-BT T26
5-D24 to 31	ED-337575	D SILICON H GMA-01-4-BT T26
5-D32	ED-309437	D SILICON H 1S1926-M
5-D33	ED-337575	D SILICON H GMA-01-4-BT T26
5-VR1 to 4	EV-336852	R S-FIX H KVSF807U 3P 102
5-VR5 to 8	EV-336847	R S-FIX H KVSF807U 3P 502
5-VR9	EV-336853	R S-FIX H KVSF807U 3P 103
5-VR10	EV-336847	R S-FIX H KVSF807U 3P 502
5-VR11	EV-336852	R S-FIX H KVSF807U 3P 102
5-VR12	EV-336850	R S-FIX H KVSF807U 3P 202
5-VR13to15	EV-337958	R S-FIX H TM64K3 3P 0.30W 202
5-VR16,17	EV-337957	R S-FIX H TM64K3 3P 0.30W 102
5-VL01	EO-325093	COIL VARI 1 T-6 8.2mH
5-L1	EO-330246	COIL FIX 1 EL0606SKI 56μH K
5-L2	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L3	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L4, 5	EO-330240	COIL FIX 1 EL0606SKI 47μH K
5-L6, 7	EO-330248	COIL FIX 1 EL0606SKI 33μH K
5-L8, 9	EO-330249	COIL FIX 1 EL0606SKI 8.2μH K
5-L10,11	EO-330250	COIL FIX 1 EL0606SKI 22μH K

REF. NO.	PARTS NO.	DESCRIPTION
5-L12	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L13	EO-330255	COIL FIX 1 EL0606SKI 18.00μH K
5-L14	EO-330241	COIL FIX 1 EL0606SKI 220μH K
5-L15	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L16	EO-330240	COIL FIX 1 EL0606SKI 47μH K
5-L17to19	EO-330241	COIL FIX 1 EL0606SKI 220μH K
5-L20	EO-330250	COIL FIX 1 EL0606SKI 22μH K
5-L21	EO-330249	COIL FIX 1 EL0606SKI 8.2μH K
5-L22,23	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L24	EO-330241	COIL FIX 1 EL0606SKI 220μH K
5-L25	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L26	EO-345893	COIL FIX 1 EL0606SKI 470μH J
5-L27	EO-321254	COIL FIX 1 FL07H 5.60mH J
5-L28	EO-330252	COIL FIX 1 EL0606SKI 100μH K
5-L29	EO-330240	COIL FIX 1 EL0606SKI 47μH K
5-L30	EO-346041	COIL FIX 1 EL0909SKI 8.2mH K
5-L31	EO-330246	COIL FIX 1 EL0606SKI 56μH K
5-L32to34	EO-330241	COIL FIX 1 EL0606SKI 220μH K
5-L35	EO-330247	COIL FIX 1 EL0606SKI 27μH K
5-L36	EO-330240	COIL FIX 1 EL0606SKI 47μH K
5-L37	EO-332352	COIL FIX 1 EL0606SKI 82.00μH K
5-FL1	ER-324305	FILTER LC HP LCB-53
5-FL2	ER-324339	FILTER LC AP LCB-56
5-FL3	ER-337711	FILTER LC LP DXV-265-1A
5-FL5	ER-337706	FILTER LC LP LCB-83
5-FL6	ER-337713	FILTER LC LP DXV-266-1A
5-FL7	ER-337715	FILTER LC AP GYV-565-1A
5-FL8	ER-337472	FILTER LC LP LCB-81
5-FL9	ER-332221	FILTER LC LP LCB-78
5-FL10	ER-322325	FILTER LC AP LCB-5-A
5-FL12	ER-324469	FILTER LC LP LCB-59
5-FL13	ER-324470	FILTER LC BP LCB-60 4.43MHz
5-FL14	ER-324398	FILTER LC LP LCB-58
5-FL15	ER-325807	FILTER LC BP LCB-61 5.06MHz
5-FL16	ER-324375	FILTER LC BP LCB-57 4.43MHz
5-FL17	ER-328237	FILTER CE SFE4.5MB 4.5MHz
5-X1,2	EI-309878	OSC X'TAL 4.433619MHz
5-DL1	EI-322365	DL EFD-EN645A11E
5-DL2	EI-337468	DL EFD-JR124A13D
5-DL3	EI-337940	DL EFD-WR645A12G
5-VC1	EC-257354	C S-FIX H ECV-1ZW20x44 2.5-20
5-VC2, 3	EV-344479	C S-FIX H CTZ54C111 2.0-10
5-C61	EC-332052	C EC V F05 NP SM 4R7M 35DC
5-C98	EC-332052	C EC V F05 NP SM 4R7M 35DC
5-C108	EC-200949	C EC V F05 NP SM 470M 10DC
5-C114	EC-200949	C EC V F05 NP SM 470M 10DC

6. SERVO (EGN) P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
6-1	BA-V1009A280A	PC SERVO (EGN) BLK VS-2EGN
6-IC1	EI-326044	IC AN6350
6-IC2	EI-200497	IC HD14066BP
6-IC3	EI-337469	IC AN6914
6-IC4	EI-330393	IC MC1458P
6-IC5	EI-337589	IC TA7248P
6-IC6	EI-321350	IC HD14011BP
6-IC7	EI-300834	IC TC4520BP
6-IC8	EI-324690	IC HD14075BP
6-IC9	EI-324795	IC HD14001BP
6-IC10	EI-200497	IC HD14066BP
6-IC11	EI-321604	IC AN6341N
6-IC12	EI-337470	IC TA78L012AP
6-IC13,14	EI-328593	IC HD14053BP
6-IC15	EI-200497	IC HD14066BP
6-IC16	EI-328593	IC HD14053BP
6-IC17	EI-325992	IC HD14024BP
6-IC18	EI-337529	IC TA78L005AP
6-IC19	EI-337687	IC MB8841-1041J
6-IC20	EI-337469	IC AN6914
6-IC21	EI-201970	IC AN5750
6-IC22	EI-301749	IC μPC741C
6-IC23	EI-324536	IC HD14049BP
6-TR1	ET-200479	TR 2SA1115 D, E, F
6-TR2	ET-322598	TR 2SB632K E, F
6-TR3 to 5	ET-200480	TR 2SC2603 D, E, F
6-TR6	ET-200479	TR 2SA1115 D, E, F
6-TR7 to 10	ET-200480	TR 2SC2603 D, E, F
6-TR11	ET-200479	TR 2SA1115 D, E, F
6-TR12	ET-200741	TR 2SD571 K, L, M
6-TR13	ET-337501	TR 2SB761 P
6-TR14	ET-325899	TR 2SC1983 R
6-TR15	ET-200479	TR 2SA1115 D, E, F
6-TR16to19	ET-200480	TR 2SC2603 D, E, F
6-TR20	ET-200479	TR 2SA1115 D, E, F
6-TR21, 22	ET-200480	TR 2SC2603 D, E, F
6-TR25to38	ET-200480	TR 2SC2603 D, E, F
6-TR48	ET-200480	TR 2SC2603 D, E, F
6-TR49	ET-246846	TR 2SC536NP E, F, G, H
6-TR50	ET-200479	TR 2SA1115 D, E, F
6-TR51	ET-200480	TR 2SC2603 D, E, F
6-D1 to 35	ED-301911	D SILICON H DS448
6-VR2, 3	EV-648753	R S-FIX H CR19R 3P 0.50W 473
6-VR4	EV-341214	R S-FIX H CR19R 3P 0.50W 683
6-VR5	EV-551643	R S-FIX H SR19R 3P 0.15W 331
6-VR6	EV-341214	R S-FIX H CR19R 3P 0.50W 683
6-VR7	EV-330863	R S-FIX H SR19R 3P 0.15W 333
6-VR8	EV-443733	R S-FIX H SR19R 3P 0.15W 683
6-VR9	EV-337499	VR ROTARY 16P10x1L B104
6-VR10,11	EV-648753	R S-FIX H CR19R 3P 0.50W 473
6-VR12	EV-341214	R S-FIX H CR19R 3P 0.50W 683
6-VR13	EV-551643	R S-FIX H SR19R 3P 0.15W 331
6-VR14	EV-341214	R S-FIX H CR19R 3P 0.50W 683
6-VR15	EV-443733	R S-FIX H SR19R 3P 0.15W 683
6-VR16	EV-337948	R S-FIX H TM64K3 3P 0.30W 203
6-L1	EO-330241	COIL FIX 1 EL0606SKI 220μH K
6-L2	EO-336963	COIL FIX 1 LAL03KB 220μH K
6-TH1	ET-330533	POSISTER PTH61G04BD3R3N
6-R8,9	ER-330272	R MF H F10 1/4W 3302F
6-R13	ER-318321	R MF H F10 1/4W 7502F
6-R143,144	ER-341399	R MF H 1/4W 1502F
6-R145	ER-314611	R MF H 1/4W 6802F
6-C62	EC-200948	C EC V F05 NP SM 1R0M 50 DC

7. AUDIO/PRE P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
7-1	BA-V1009A210A	PC AUDIO PRE BLK VS-2EG
7-IC1	EI-332286	IC BA5102
7-IC2	EI-321076	IC AN6320N
7-TR1	ET-200480	TR 2SC2603 D, E, F
7-TR2	ET-322412	TR 2SC2001 K, L, M
7-TR3	ET-200480	⚠ TR 2SC2603 D, E, F
7-TR4 to 6	ET-200480	TR 2SC2603 D, E, F
7-TR7	ET-322775	TR 2SC536K-NP E, F, G
7-TR8	ET-322778	TR 2SA608K-NP E, F, G
7-TR9,10	ET-322775	TR 2SC536K-NP E, F, G
7-D1, 2	ED-337575	D SILICON H GMA-01-4-BT T26
7-D3	ED-338553	D ZENER V HZ6B-1S1
7-VR1	EV-341256	R S-FIX V V8K1-1 3P 301
7-VR2	EV-475470	R S-FIX V V8K1-1 3P 103
7-VR3	EV-341257	R S-FIX V V8K1-1 3P 302
7-VR4	EV-464264	R S-FIX V V8K1-1 3P 503
7-VR5, 6	EV-361800	R S-FIX H SR19R 3P 0.15W 471
7-RL1	EP-200175	RELAY SIGNAL G2E 1TR 12V
7-L1	EO-337523	COIL FIX 1 L-8 22μH J
7-L3	EO-321254	COIL FIX 1 FL07H 5.60mH J
7-L4	EO-243966	COIL FIX 1 FL05H 820μH K
7-L5	EO-337524	COIL OSC 1 93-1006 70KHz
7-L6	EO-443722	COIL FIX 1 FL09H 1mH J
7-L7	EO-357287	COIL FIX 1 FL05H 100μH K
7-L8	EO-243966	COIL FIX 1 FL05H 820μH K
7-L11,12	EO-330244	COIL FIX 1 EL0606SKI 2.2μH K
7-L13	EO-330252	COIL FIX 1 EL0606SKI 100μH K
7-L14,15	EO-330241	COIL FIX 1 EL0606SKI 220μH K
7-VC1,2	EC-318315	C S-FIX H ECV-1ZW50×44 5.0-50
7-FR1	ER-318647	⚠ R FUSE ERD2FC S10 1/4W 4R7J
7-C26,27	EC-337561	C PP V F10 PFH 183J 400DC
7-C32	EC-328774	C STY V SNP CQFS 331J 250DC

8. DE-MODULATOR P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
8-1	BA-V1009A060A	PC DE-MODULATOR BLK VS-2EG
8-2	EE-337170	TV TUNER CDE1-015
8-IC1	EI-705494	IC TA7607AP
8-IC2	EI-704201	IC M5144P
8-IC3	EI-337470	IC TA78L012AP
8-TR1	ET-742646	TR 2SC388A
8-TR2 to 4	ET-330464	TR 2SC2603 D, E
8-TR5	ET-522270	TR 2SC1210 D
8-TR6	ET-330464	TR 2SC2603 D, E
8-TR7	ET-307997	TR 2SA1115 D, E
8-TR8	ET-330464	TR 2SC2603 D, E
8-TR9	ET-307997	TR 2SA1115 D, E
8-TR10to12	ET-742648	TR 2SA1115 F, G
8-TR13	ET-330427	TR 2SB772 E, P
8-D1 to 3	ED-604541	D SILICON H 1S2076
8-D4	ED-705479	D SILICON 1SV70
8-D5 to 8	ED-604541	D SILICON H 1S2076
8-D9 to 11	ED-742650	D ZENER HZ9B3
8-VR1, 2	EV-702568	R S-FIX TT24R 502
8-VR3	EV-702567	R S-FIX TT24R 202
8-L1	EV-707836	COIL FIX 1 144LZ 0.39μHK
8-L2	EO-742653	COIL RF 144LY 2.0μH K
8-L3	EO-742655	COIL RF 6F16001A1 7K
8-L4	EO-705490	COIL TKXNA S-27899RY
8-L5	EO-705491	COIL TKXN S-279789NK
8-L6	EO-742658	COIL FIX 1 EPL 4.7μH K
8-L7,8	EO-701411	COIL RF SPL 15μH
8-L9	EO-705485	COIL FIX 1 33μH K
8-L10	EO-705487	COIL FIX 1 100μH K
8-L11	EO-701266	COIL PEAKING SPL-120

REF. NO.	PARTS NO.	DESCRIPTION
8-L12	EO-705492	COIL TKACS-27617NK
8-CF1	ER-742662	FILTER SAW SAF38.9MZ51Z
8-CF2	ER-705501	FILTER CE TPS 5.5MHz
8-CF3	ER-705499	FILTER CE SFE 5.5MHz
8-R51	ER-705505	⚠ R FUSE W 1/4W 220J
8-R52,53	ER-742637	R OMF RNL 1/4W 4.75K
8-R54	ER-742638	R OMF RNL 1/4W 2.4K
8-R61	ER-742639	⚠ R FUSE 1/4W 100J
8-C17	EC-742640	C TT R47M 35DC
8-C28	EC-742641	C MY AMZ 822J 50V
8-C36to39	EC-742642	C MY AMZ 683J 50V
8-C40	EC-742643	C MY AMZ 273K 50V
8-C43	EC-742644	C MY AMZ 103K 50V

9. OPERATION P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
9-1	BA-V1009A070E	PC OPERATION BLK VS-2EGN
9-IC1	EI-337469	IC AN6914
9-IC2	EI-338346	IC HD14093BP
9-IC3	EI-337518	IC MN1227A
9-IC4	EI-330475	IC M5L510P
9-IC5	EI-337519	IC MB88301-P
9-IC6	EI-337469	IC AN6914
9-IC7	EI-338537	IC MB88401-161K
9-TR1,2	ET-200479	TR 2SA1115 D, E, F
9-TR3 to 5	ET-200480	TR 2SC2603 D, E, F
9-D1, 2	ED-323979	D SILICON W03B F12 100/1.0A
9-D3 to 6	ED-560913	D SILICON V 1S2473VE
9-D7	ED-318988	D LED SR505D RED
9-D8	ED-332283	D LED SG205D GRN
9-D9	ED-318988	D LED SR505D RED
9-D10	ED-332283	D LED SG205D GRN
9-D11 to 14	ED-318988	D LED SR505D RED
9-D16	ED-624903	D SILICON H 1S2473
9-D19	ED-624903	D SILICON H 1S2473
9-SW1 to 20	ES-337521	SW TACT KHH-10908
9-VR1	EV-307620	R S-FIX H H0651A 3P 0.05W 222
9-X1	EO-330256	OSC CE F85-006 4MHz
9-IB1	ER-337939	R COMP FRE15-333M
9-IB2	ER-337515	R COMP 01-0419
9-B1	AX-337517	BATTERY 2/60DK
9-IN1	ED-337587	D LED TLG321 GRN
9-L1, 2	EO-330252	COIL FIX 1 EL0606SKI 100μH K
9-R61	ER-337563	R MF H F10 1/4W 4751F
9-R62	ER-337564	R MF H F10 1/4W 2401F
9-R63	ER-337563	R MF H F10 1/4W 4751F

10. POWER SYS. CON. P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
10-1	BA-V1009A080B	PC POWER SYSCON BLK VS-2EGN
		POWER SYS. CON. P.C BOARD BLOCK
10-IC1	EI-344166	⚠ IC TA78L012P
10-IC2	EI-337528	⚠ IC STK-5315
10-IC3	EI-337529	⚠ IC TA78L005AP
10-IC4	EI-337530	IC μPC574J
10-IC5	EI-337531	IC MB8841-679J
10-IC6	EI-318332	IC μPC339C
10-TR1	ET-337569	⚠ TR 2SA675(A) E, F, H
10-TR2	ET-633677	⚠ TR 2SA490 O,Y
10-TR3	ET-330430	⚠ TR 2SB632K D, E, F
10-TR4	ET-307193	TR 2SD612K D, E, F
10-TR5	ET-200479	TR 2SA1115 D, E, F
10-TR6 to 8	ET-318237	TR 2SB764 E, F
10-TR9	ET-200479	TR 2SA1115 D, E, F
10-TR10	ET-200480	TR 2SC2603 D, E, F
10-TR11	ET-318239	TR 2SD863 E,F
10-TR12to14	ET-318237	TR 2SB764 E, F
10-TR15	ET-200480	TR 2SC2603 D, E, F
10-D1	ED-337617	⚠ D SILICON DBB50C-K8 200/5.0A
10-D2	ED-322238	⚠ D SILICON 1B4B41 100/1.0A
10-D3,4	ED-337618	⚠ D SILICON DS135E-FB6 100/1.0A
10-D5	ED-301911	D SILICON H DS448
10-D6,7	ED-200469	D SILICON H DS448 FA5 F10
10-D8	ED-301911	D SILICON H DS448
10-D9	ED-337618	⚠ D SILICON DS135E-FB6 100/1.0A
10-D11	ED-200469	D SILICON H DS448 FA5 F10
10-D13	ED-200469	D SILICON H DS448 FA5 F10
10-X1	EO-330256	OSC CE F85-006 4MHz
10-IB1	ER-337673	R COMP 01-0480
10-IB2	ER-337526	R COMP 01-0315
10-TH1	ET-337619	⚠ POSISTER PTH61G04BD101M
10-R14	ER-321192	⚠ R OMF H SNP FS 2W 101J
10-R15	ER-321290	⚠ R OMF H SNP FS 2W 121J
10-C9	EC-333977	C EC V CUT NP SM 101M 50DC
10-C26	EC-333977	C EC V CUT NP SM 101M 50DC
		MECHA DRIVE P.C BOARD BLOCK
10-IC1	EI-337503	IC M54532P
10-IC2,3	EI-330352	IC BA6109
10-TR1	ET-318308	TR PHOTO PN202S
10-TR2	ET-200479	⚠ TR 2SA1115 D, E, F
10-TR3	ET-200480	TR 2SC2603 D, E, F
10-TR4,5	ET-200479	TR 2SA1115 D, E, F
10-TR6	ET-200480	TR 2SC2603 D, E, F
10-D1 to 3	ED-301911	D SILICON H DS448
10-D4	ED-200469	D SILICON H DS448 FA5 F10
10-D5,6	ED-301911	D SILICON H DS448
10-D7	ED-200469	D SILICON H DS448 FA5 F10
10-D8,9	ED-301911	D SILICON H DS448
10-RL1	EP-337416	RELAY SIGNAL G2V-282P-NL 2TR 12V
10-L1,2	EO-669273	COIL FIX 2 FL5R200 18μH
10-FL1,2	ER-330465	FILTER LC DST310-55B271M
10-PH1	ED-323892	PHOTO SENSOR GP-411P
10-IN1	EL-330446	PL SPL HOLDER LAMP
10-TH1,2	ET-330533	⚠ POSISTER PTH61G04BD3R3N
10-2	VT-327360	CAP VS SENSOR
10-F1	EF-691007	⚠ FUSE SEMKO T 250V 3.15A
10-F2	EF-593706	⚠ FUSE SEMKO T 250V 0.50A
10-F3	EF-601301	⚠ FUSE SEMKO T 250V 2A
10-F4	EF-623103	⚠ FUSE SEMKO T 250V 1A
10-F5	EF-344106	⚠ FUSE ICP-N10 150V 0.4A

REF. NO.	PARTS NO.	DESCRIPTION
8-L12	EO-705492	COIL TKACS-27617NK
8-CF1	ER-742662	FILTER SAW SAF38.9MZ51Z
8-CF2	ER-705501	FILTER CE TPS 5.5MHz
8-CF3	ER-705499	FILTER CE SFE 5.5MHz
8-R51	ER-705505	⚠ R FUSE W 1/4W 220J
8-R52,53	ER-742637	R OMF RNL 1/4W 4.75K
8-R54	ER-742638	R OMF RNL 1/4W 2.4K
8-R61	ER-742639	⚠ R FUSE 1/4W 100J
8-C17	EC-742640	C TT R47M 35DC
8-C28	EC-742641	C MY AMZ 822J 50V
8-C36to39	EC-742642	C MY AMZ 683J 50V
8-C40	EC-742643	C MY AMZ 273K 50V
8-C43	EC-742644	C MY AMZ 103K 50V

9. OPERATION P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
9-1	BA-VI009A070E	PC OPERATION BLK VS-2EGN
9-IC1	EI-337469	IC AN6914
9-IC2	EI-338346	IC HD14093BP
9-IC3	EI-337518	IC MN1227A
9-IC4	EI-330475	IC M5L510P
9-IC5	EI-337519	IC MB88301-P
9-IC6	EI-337469	IC AN6914
9-IC7	EI-338537	IC MB88401-161K
9-TR1,2	ET-200479	TR 2SA1115 D, E, F
9-TR3 to 5	ET-200480	TR 2SC2603 D, E, F
9-D1, 2	ED-323979	D SILICON W03B F12 100/1.0A
9-D3 to 6	ED-560913	D SILICON V 1S2473VE
9-D7	ED-318988	D LED SR505D RED
9-D8	ED-332283	D LED SG205D GRN
9-D9	ED-318988	D LED SR505D RED
9-D10	ED-332283	D LED SG205D GRN
9-D11 to 14	ED-318988	D LED SR505D RED
9-D16	ED-624903	D SILICON H 1S2473
9-D19	ED-624903	D SILICON H 1S2473
9-SW1 to 20	ES-337521	SW TACT KHH-10908
9-VR1	EV-307620	R S-FIX H H0651A 3P 0.05W 222
9-X1	EO-330256	OSC CE F85-006 4MHz
9-IB1	ER-337939	R COMP FRE15-333M
9-IB2	ER-337515	R COMP 01-0419
9-B1	AX-337517	BATTERY 2/60DK
9-IN1	ED-337587	D LED TLG321 GRN
9-L1, 2	EO-330252	COIL FIX 1 EL0606SKI 100μH K
9-R61	ER-337563	R MF H F10 1/4W 4751F
9-R62	ER-337564	R MF H F10 1/4W 2401F
9-R63	ER-337563	R MF H F10 1/4W 4751F

10. POWER SYS. CON. P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
10-1	BA-VI009A080B	PC POWER SYSCON BLK VS-2EGN
		POWER SYS. CON. P.C BOARD BLOCK
10-IC1	EI-344166	⚠ IC TA78L012P
10-IC2	EI-337528	⚠ IC STK-5315
10-IC3	EI-337529	⚠ IC TA78L005AP
10-IC4	EI-337530	IC μPC574J
10-IC5	EI-337531	IC MB8841-679J
10-IC6	EI-318332	IC μPC339C
10-TR1	ET-337569	⚠ TR 2SA675(A) E, F, H
10-TR2	ET-633677	⚠ TR 2SA490 O,Y
10-TR3	ET-330430	⚠ TR 2SB632K D, E, F
10-TR4	ET-307193	TR 2SD612K D, E, F
10-TR5	ET-200479	TR 2SA1115 D, E, F
10-TR6 to 8	ET-318237	TR 2SB764 E, F
10-TR9	ET-200479	TR 2SA1115 D, E, F
10-TR10	ET-200480	TR 2SC2603 D, E, F
10-TR11	ET-318239	TR 2SD863 E,F
10-TR12 to 14	ET-318237	TR 2SB764 E, F
10-TR15	ET-200480	TR 2SC2603 D, E, F
10-D1	ED-337617	⚠ D SILICON DBB50C-K8 200/5.0A
10-D2	ED-322238	⚠ D SILICON 1B4B41 100/1.0A
10-D3,4	ED-337618	⚠ D SILICON DS135E-FB6 100/1.0A
10-D5	ED-301911	D SILICON H DS448
10-D6,7	ED-200469	D SILICON H DS448 FA5 F10
10-D8	ED-301911	D SILICON H DS448
10-D9	ED-337618	⚠ D SILICON DS135E-FB6 100/1.0A
10-D11	ED-200469	D SILICON H DS448 FA5 F10
10-D13	ED-200469	D SILICON H DS448 FA5 F10
10-X1	EO-330256	OSC CE F85-006 4MHz
10-IB1	ER-337673	R COMP 01-0480
10-IB2	ER-337526	R COMP 01-0315
10-TH1	ET-337619	⚠ POSISTER PTH61G04BD101M
10-R14	ER-321192	⚠ R OMF H SNP FS 2W 101J
10-R15	ER-321290	⚠ R OMF H SNP FS 2W 121J
10-C9	EC-333977	C EC V CUT NP SM 101M 50DC
10-C26	EC-333977	C EC V CUT NP SM 101M 50DC
		MECHA DRIVE P.C BOARD BLOCK
10-IC1	EI-337503	IC M54532P
10-IC2,3	EI-330352	IC BA6109
10-TR1	ET-318308	TR PHOTO PN202S
10-TR2	ET-200479	⚠ TR 2SA1115 D, E, F
10-TR3	ET-200480	TR 2SC2603 D, E, F
10-TR4,5	ET-200479	TR 2SA1115 D, E, F
10-TR6	ET-200480	TR 2SC2603 D, E, F
10-D1 to 3	ED-301911	D SILICON H DS448
10-D4	ED-200469	D SILICON H DS448 FA5 F10
10-D5,6	ED-301911	D SILICON H DS448
10-D7	ED-200469	D SILICON H DS448 FA5 F10
10-D8,9	ED-301911	D SILICON H DS448
10-RL1	EP-337416	RELAY SIGNAL G2V-282P-NL 2TR 12V
10-L1,2	EO-669273	COIL FIX 2 FL5R200 18μH
10-FL1,2	ER-330465	FILTER LC DST310-55B271M
10-PH1	ED-323892	PHOTO SENSOR GP-411P
10-IN1	EL-330446	PL SPL HOLDER LAMP
10-TH1,2	ET-330533	⚠ POSISTER PTH61G04BD3R3N
10-2	VT-327360	CAP VS SENSOR
10-F1	EF-691007	⚠ FUSE SEMKO T 250V 3.15A
10-F2	EF-593706	⚠ FUSE SEMKO T 250V 0.50A
10-F3	EF-601301	⚠ FUSE SEMKO T 250V 2A
10-F4	EF-623103	⚠ FUSE SEMKO T 250V 1A
10-F5	EF-344106	⚠ FUSE ICP-N10 150V 0.4A

11. EGN P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
11-1	BA-V1009A300A	PC EGN BLK VS-2EGN
11-IC1	EI-337549	IC μPC1004C
11-IC2,3	EI-337624	IC BA222
11-IC4	EI-337625	IC BA236
11-IC5	EI-337705	IC AN6361N
11-IC6	EI-324151	IC AN6360
11-IC7	EI-324203	IC AN6342N
11-TR1,2	ET-246846	TR 2SC536NP E, F, G, H
11-TR3 to 5	ET-309334	TR 2SC458 C, D
11-TR6	ET-200480	TR 2SC2603 D, E, F
11-TR7, 8	ET-246846	TR 2SC536NP E, F, G, H
11-TR9	ET-309334	TR 2SC458 C, D
11-TR10	ET-246846	TR 2SC536NP E, F, G, H
11-TR11	ET-332313	TR 2SC536SP E, F, G
11-TR12	ET-246846	TR 2SC536NP E, F, G, H
11-TR13	ET-332402	TR 2SA608SP E, F, G
11-TR14	ET-246846	TR 2SC536NP E, F, G, H
11-TR16	ET-330543	TR 2SB621NC Q, R, S
11-TR17,18	ET-246846	TR 2SC536NP E, F, G, H
11-TR19	ET-328272	TR 2SC536K-NP F
11-TR20	ET-246846	TR 2SC536NP E, F, G, H
11-D1, 2	ED-337575	D SILICON H GMA-01-4-BT T26
11-D3	ED-301911	D SILICON H DS448
11-D4, 5	ED-337575	D SILICON H GMA-01-4-BT T26
11-D6,7	ED-301911	D SILICON H DS448
11-D8 to 13	ED-337575	D SILICON H GMA-01-4-BT T26
11-VR1	EV-336850	R S-FIX H KVSF807U 3P 202
11-VR2,3	EV-336843	R S-FIX H KVSF807U 3P 303
11-VR4	EV-336853	R S-FIX H KVSF807U 3P 103
11-VR5	EV-336854	R S-FIX H KVSF807U 3P 104
11-VR6	EV-341225	R S-FIX H KVSF807U 3P 503
11-VL1	EO-324478	COIL TUN 1 T-7-A 1.07MHz
11-VL2	EO-322334	COIL TUN 1 T-1-B 4.29MHz
11-VL3	EO-325093	COIL VARI 1 T-6 8.2mH
11-L1	EO-330252	COIL FIX 1 EL0606SKI 100μH K
11-L2, 3	EO-318379	COIL FIX 1 LAL04 100μH K
11-L4	EO-379923	COIL FIX 1 FL07H 8.2mH J
11-L5	EO-345861	COIL FIX 1 EL0606SKI 3.30μH K
11-L6	EO-330252	COIL FIX 1 EL0606SKI 100μH K
11-L7	EO-379923	COIL FIX 1 FL07H 8.2mH J
11-L8	EO-321254	COIL FIX 1 FL07H 5.60mH J
11-L9	EO-330241	COIL FIX 1 EL0606SKI 220μH K
11-L10	EO-344167	COIL FIX 1 EL0606SKI 68.00μH K
11-L11	EO-318381	COIL FIX 1 LAL04 220μH K
11-L12	EO-345877	COIL FIX 1 EL0606SKI 56μH J
11-L13,14	EO-318379	COIL FIX 1 LAL04 100μH K
11-L15	EO-318383	COIL FIX 1 FL07H 6.8mH J
11-L16	EO-346500	COIL FIX 1 FL07H 220μH J
11-FL1	ER-337626	FILTER LC AP LCB-82
11-FL2	ER-324472	FILTER LC BP LCB-75 2.16MHz
11-FL3	ER-324473	FILTER LC BP LCB-76 2.32MHz
11-FL4	ER-324471	FILTER LC BP LCB-74 4.43MHz
11-FL5	ER-328237	FILTER CE SFE4.5MB 4.5MHz
11-FL6	ER-337702	FILTER LC BP DXV-363-1A 3.58MHz
11-FL8	ER-337701	FILTER LC BP DXV-350-1B 3.58MHz
11-FL9	ER-337703	FILTER LC BP DXV-367-1A 4.21MHz
11-X1,2	EI-318384	OSC X'TAL NC-18C 3.579545MHz
11-DL1	EI-337888	DL EFD-KR645B85C
11-VC1,2	EV-344479	C S-FIX H CTZ54C111 2.0-10

12. SENSOR P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
		SENSOR (2) P.C BOARD BLOCK
12-1	VT-327360	CAP VS SENSOR
12-TR1	ET-318308	TR PHOTO PN202S
		R.S. SW P.C BOARD BLOCK
12-SW904	ES-319156	SW MICRO SS-1-E-4 UC
		SW A P.C BOARD BLOCK
12-SW905	ES-318284	SW LEVER SCL101R23A 1-01-02N
		SW B P.C BOARD BLOCK
12-SW906	ES-318284	SW LEVER SCL 101R23A 1-01-02N
		EJ. S. SW P.C BOARD BLOCK
12-SW907	ES-319124	SW LEVER SCL101S 1-01-02N

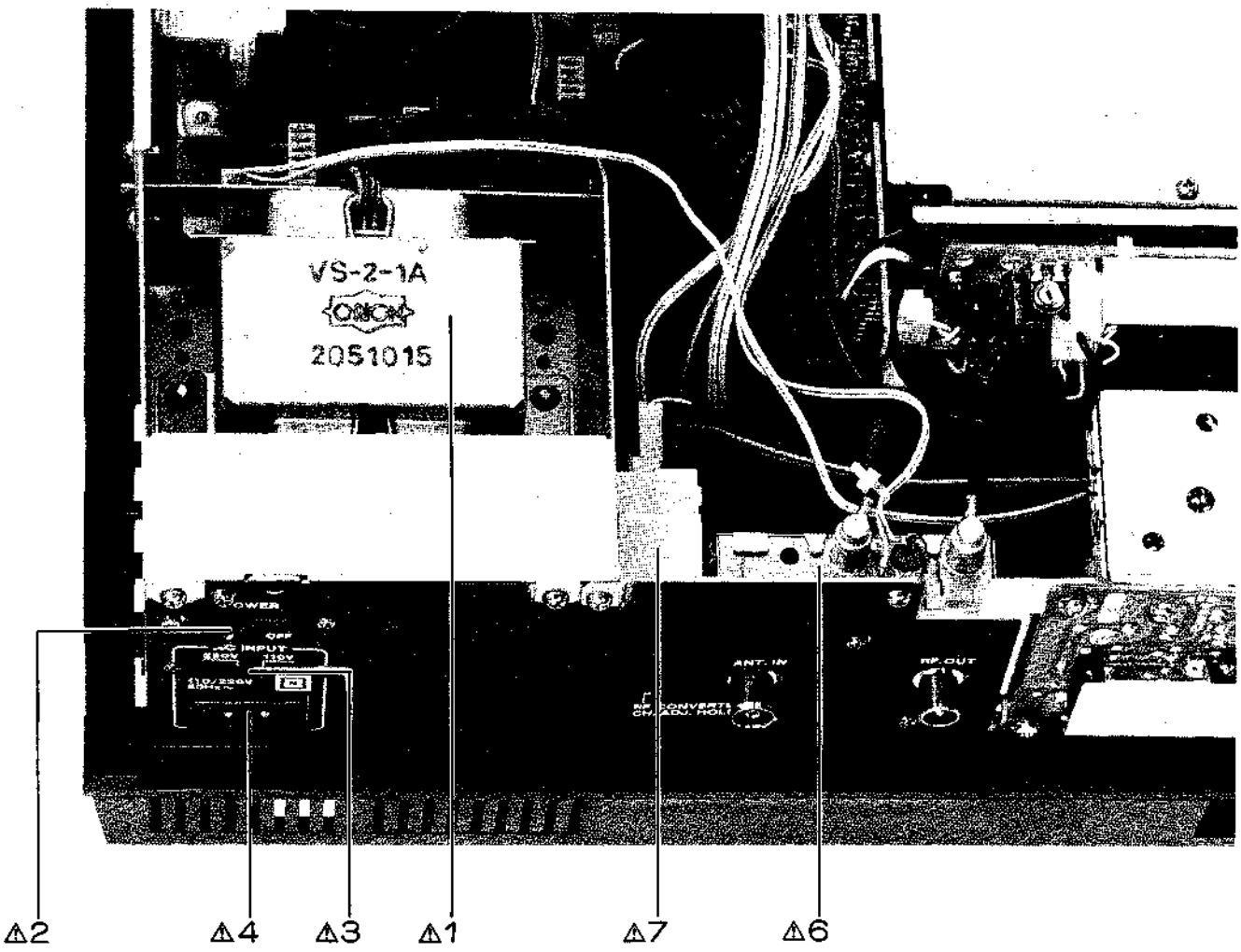
13. POWER FILTER P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
13-FL901	EO-339907	COIL LF FKOB160MH16 1000.0μH
13-C901	EC-325485	⚠ C MP V 473M 250AC

14. LED (EGN) P.C BOARD BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
14-D1	ED-332283	D LED SG205D GRN
14-D2 to 6	ED-318988	D LED SR505D RED

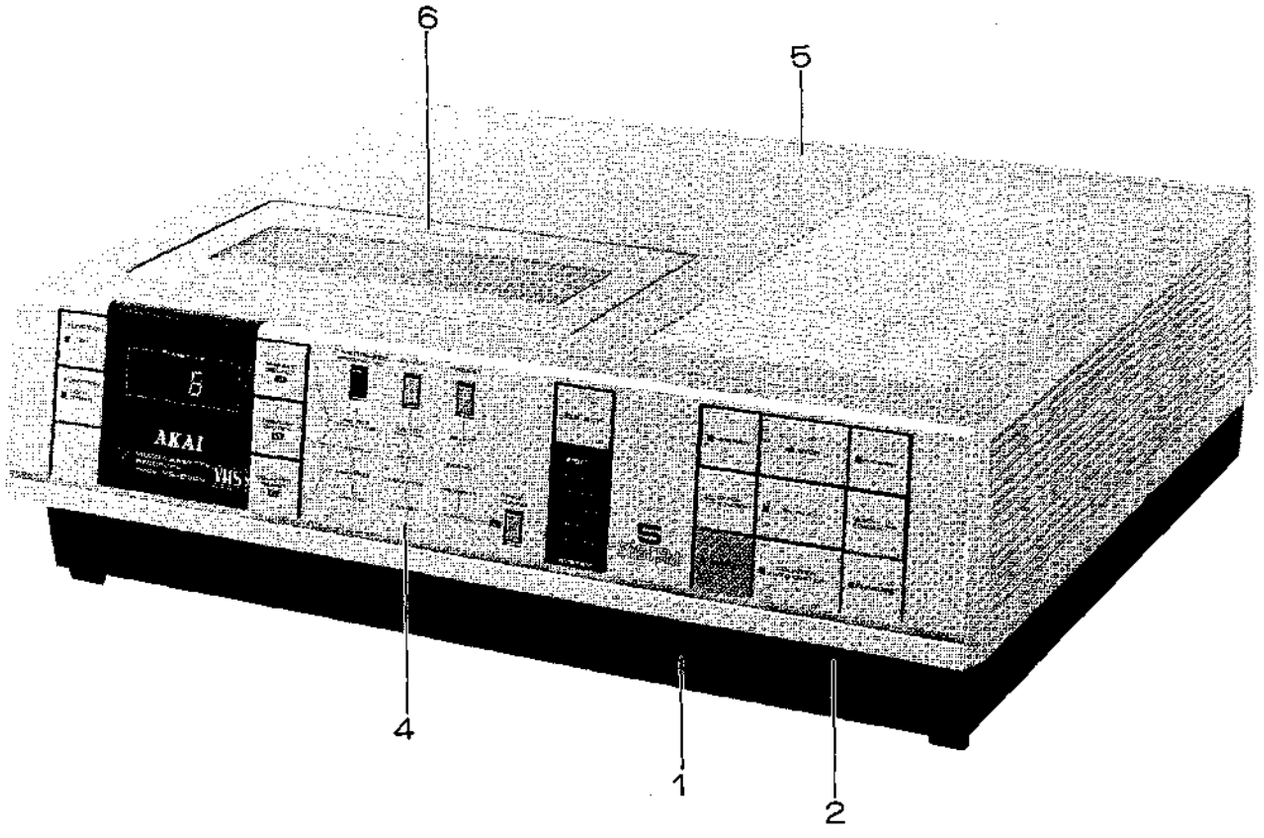
POWER & RF BLOCK



15. POWER & RF BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
	POWER BLOCK	
15-1	BT-344150	⚠ TRANS POWER VS-2-1A
15-2	ES-337509	⚠ SW SEESAW SDE3S-E 02-1 E
15-3	ES-309312	⚠ SW SLIDE 22293B 02-2
15-4	EJ-301513	⚠ SOCKET INLET S-I6453 E 2P
15-5x	EF-623103	⚠ FUSE SEMKO T 250V 1A
	RF BLOCK	
15-6	BV-330111	⚠ ANT BOOSTER YBC1-001
15-7	BV-330109	⚠ RF CONVERTER MDK3-253

FINAL ASSEMBLY BLOCK



16. FINAL ASSEMBLY BLOCK

REF. NO.	PARTS NO.	DESCRIPTION
16-1	BC-342143	COVER REMOCON HOLE
16-2	SK-342144	KNOB TRACKING
16-3x	SP-342155	COVER BOTTOM
16-4	BD-B604446	PANEL FRONT EGN PART
16-5	SP-342142	CASE UPPER
16-6	BD-327698A	LID CASSETTE (ENGLISH)
16-7x	EW-638144	AC CORD 2CORE VM0364/VM0305 E
16-8x	EW-321758	CORD VY-15 ANTENNA CABLE

II. REMOTE CONTROL UNIT RC-V202

1. TRANSMITTER RC-T2

REF. NO.	PARTS NO.	DESCRIPTION
1-IC1	EI-780020	IC μPD1986C
1-TR1	ET-318604	TR 2SD545NP E, F
1-TR2	ET-328553	TR 2SC945A K,P
1-D1, 2	ED-706226	D LED SE303A INFRARED
1-D3	ED-780019	D LED SEL1123W
1-SW1	ES-780015	SW SLIDE
1-X1	EC-780021	OSC CE

2. RECEIVER RC-R2

REF. NO.	PARTS NO.	DESCRIPTION
2-IC1	EI-330226	IC μPC1373H
2-TR1	ET-200479	TR 2SA1115 D, E, F
2-TR2	ET-200505	TR 2SC2603 E, F
2-D1	ED-330238	D PHOTO PH302
2-D2	ED-709904	D LED GL-9PG4
2-L1	EO-709902	COIL FS1012-562J

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1. MODEL VS-2EGN

PARTS NO.	REF. NO.	PARTS NO.	REF. NO.	PARTS NO.	REF. NO.	PARTS NO.	REF. NO.	PARTS NO.	REF. NO.
ET-322775	7-TR9,10	EV-336852	5-VR1to4	EW-321758	16-8x	VT-326476	3-4	ZG-780035	3-17
ET-322775	7-TR7	EV-336852	5-VR11	EW-638144	16-7x	VT-326477	2-45	ZG-780037	3-19
ET-322778	7-TR8	EV-336853	5-VR9	HC-337506	1-4	VT-327360	10-2	ZG-780038	3-20
ET-325899	6-TR14	EV-336853	11-VR4	HE-337507	2-1	VT-327360	12-1	ZG-780039	3-21
ET-328272	11-TR19	EV-336854	11-VR5	HZ-342726	1-6	VT-328134	2-16	ZG-780040	3-22
ET-330427	8-TR13	EV-337499	6-VR9	HZ-342726	2-23	VT-342116	2-40x	ZS-326246	2-44
ET-330430	10-TR3	EV-337948	6-VR16	HZ-343076	1-5	VT-780025	3-7	ZS-332978	1-13
ET-330464	8-TR8	EV-337957	5-VR16,17	HZ-343076	2-22	VT-780026	3-8	ZS-380046	1-8
ET-330464	8-TR2to4	EV-337958	5-VR13to15	MB-322303	2-35	VT-780027	3-9	ZS-477876	2-5
ET-330464	8-TR6	EV-341214	6-VR4	MB-326474	3-34	VT-780028	3-10	ZS-477876	2-2
ET-330533	6-TH1	EV-341214	6-VR12	MB-780029	3-11	ZG-313045	2-26	ZS-609434	2-20
ET-330533	10-TH1,2	EV-341214	6-VR6	MH-321688	2-19	ZG-313085	3-29	ZW-259334	1-3
ET-330543	11-TR16	EV-341214	6-VR14	MI-B328611	3-33	ZG-313257	1-10	ZW-698940	3-35x
ET-332313	11-TR11	EV-341225	11-VR6	MI-322304	2-36	ZG-318043	2-10		
ET-332402	11-TR13	EV-341256	7-VR1	MI-326478	1-1	ZG-318043	2-14		
ET-337501	6-TR13	EV-341257	7-VR3	MI-327773	2-24	ZG-318204	2-33		
ET-337508	1-17	EV-344479	5-VC2,3	ML-330640	2-29	ZG-321769	3-30		
ET-337569	10-TR1	EV-344479	11-VC1,2	ML-780036	3-18	ZG-326247	2-43		
ET-337619	10-TH1	EV-361800	7-VR5,6	MV-322302	3-24	ZG-327740	1-14		
ET-522270	8-TR5	EV-443733	6-VR8	MZ-B321701	3-23	ZG-327757	1-9		
ET-633677	10-TR2	EV-443733	6-VR15	SK-342144	16-2	ZG-328225	1-7		
ET-742646	8-TR1	EV-464264	7-VR4	SP-342142	16-5	ZG-328225	2-21		
ET-742648	8-TR10to12	EV-475470	7-VR2	SP-342155	16-3x	ZG-328610	3-27		
EV-307620	9-VR1	EV-551643	6-VR5	VT-B319445	2-8	ZG-328661	3-3		
EV-330863	6-VR7	EV-551643	6-VR13	VT-B319446	2-12	ZG-330058	2-4		
EV-336843	11-VR2,3	EV-648753	6-VR10,11	VT-317947	2-13	ZG-331128	2-17		
EV-336847	5-VR5to8	EV-648753	6-VR2,3	VT-317947	2-9	ZG-331178	1-11		
EV-336847	5-VR10	EV-702567	8-VR3	VT-318213	1-20	ZG-332463	2-28		
EV-336850	5-VR12	EV-702568	8-VR1,2	VT-322159	2-32	ZG-332979	1-12		
EV-336850	11-VR1	EV-707836	8-L1	VT-326470	2-18	ZG-780032	3-14		

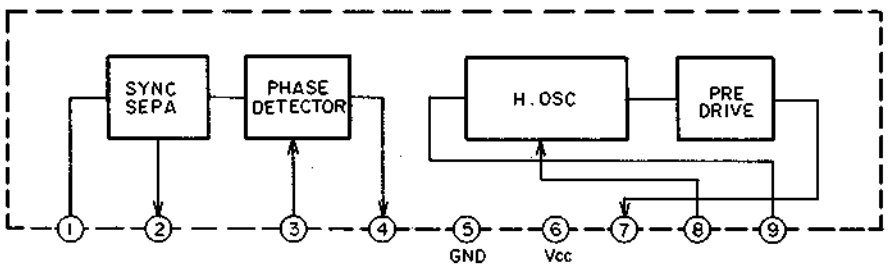
2. REMOTE CONTROL UNIT RC-V202

PARTS NO.	REF. NO.	PARTS NO.	REF. NO.	PARTS NO.	REF. NO.	PARTS NO.	REF. NO.	PARTS NO.	REF. NO.
EC-780021	1-X1								
ED-330238	2-D1								
ED-706226	1-D1,2								
ED-7809904	2-D2								
ED-780019	1-D3								
EI-330226	2-IC1								
EI-780020	1-IC1								
EO-709902	2-L1								
ES-780015	1-SW1								
ET-200479	2-TR1								
ET-200505	2-TR2								
ET-318604	1-TR1								
ET-328553	1-TR2								

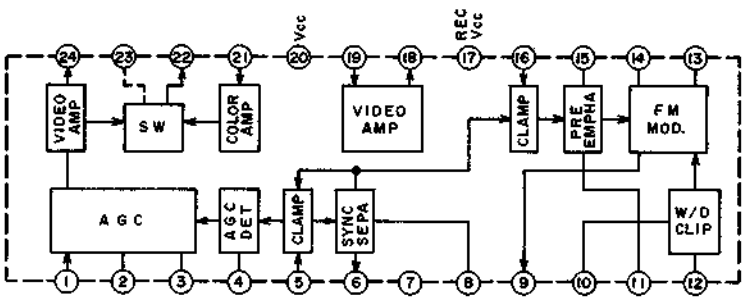
SECTION 3

SCHEMATIC DIAGRAM

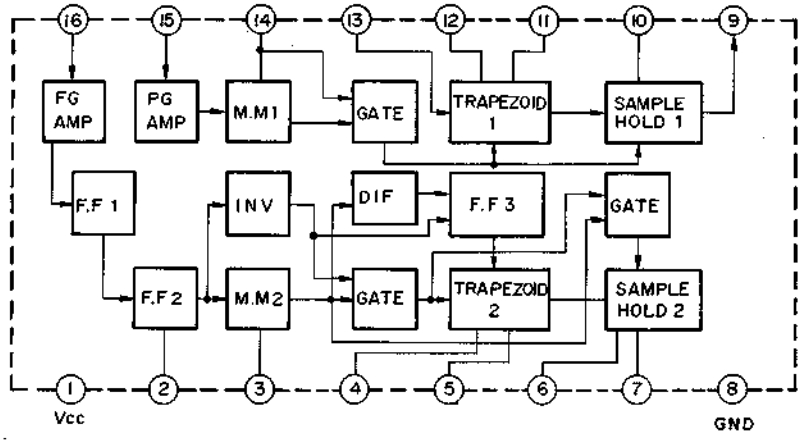
AN5750



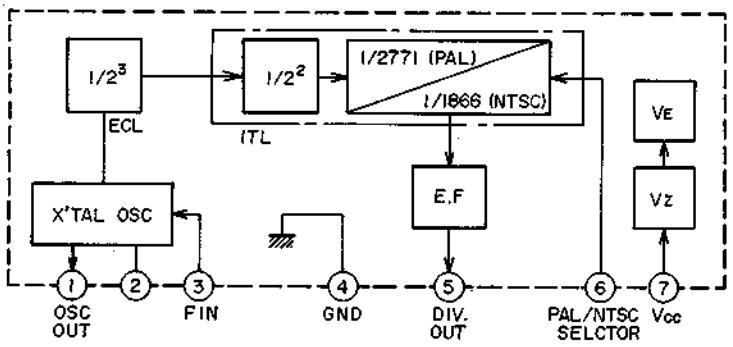
AN6310



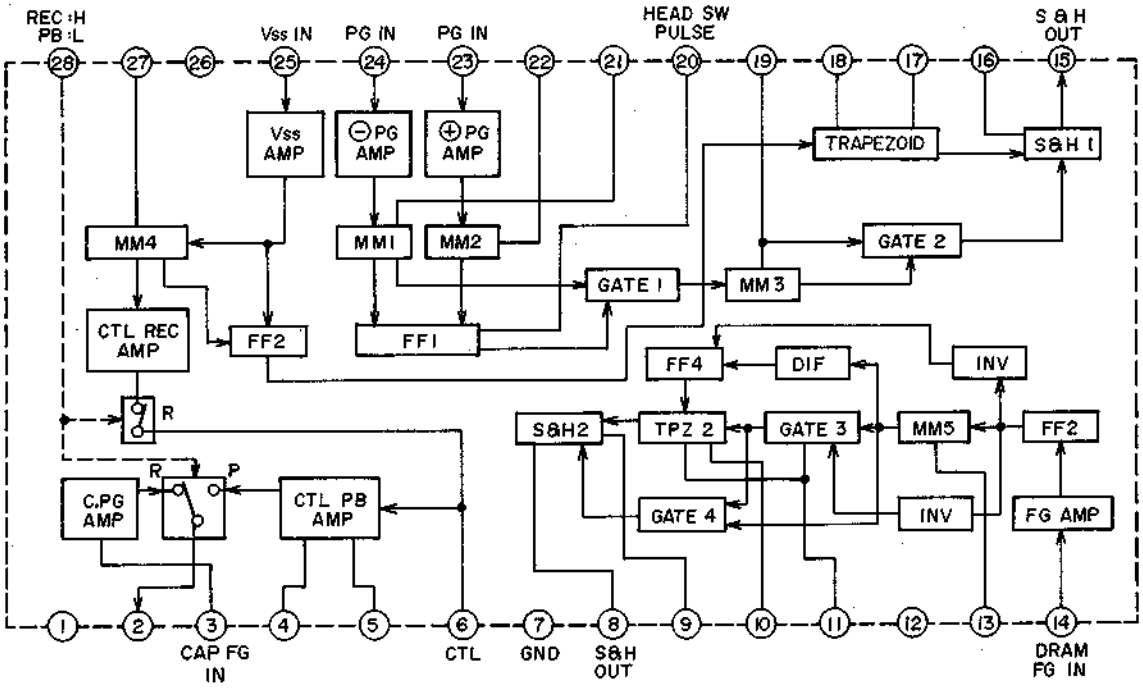
AN6341N



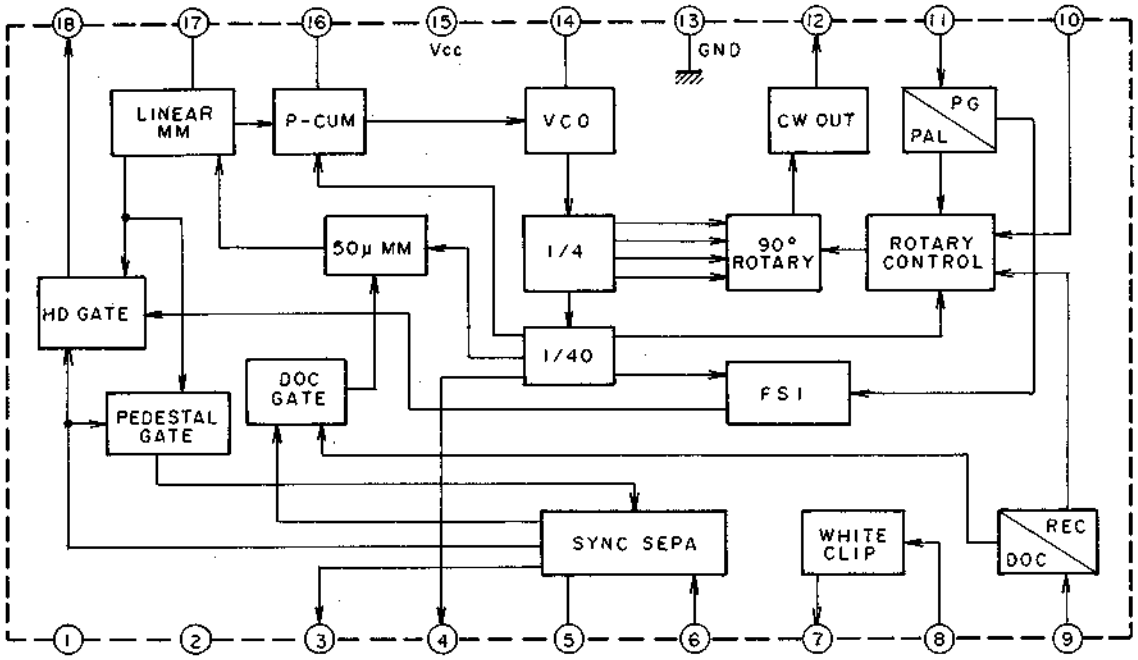
AN6342N



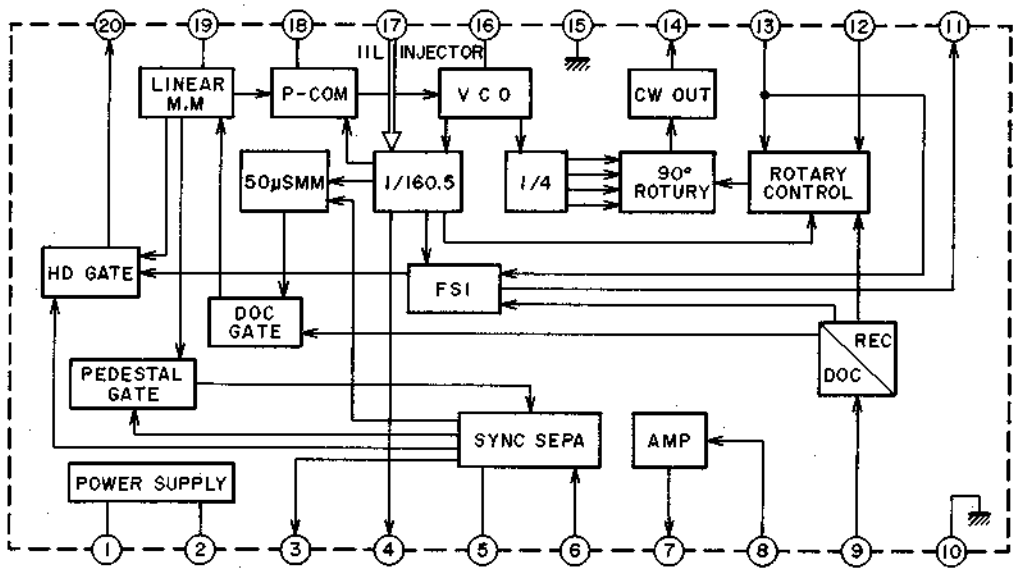
AN6350



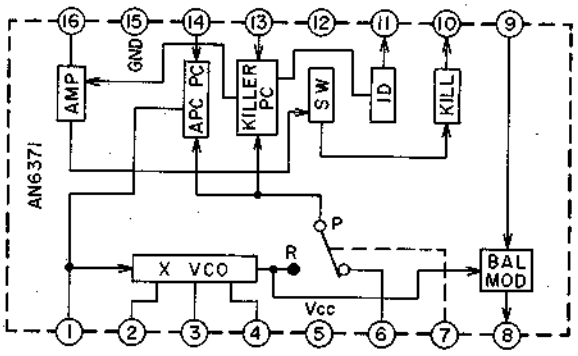
AN6362



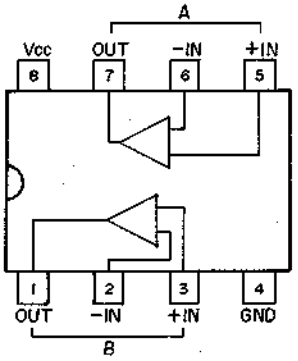
AN6363



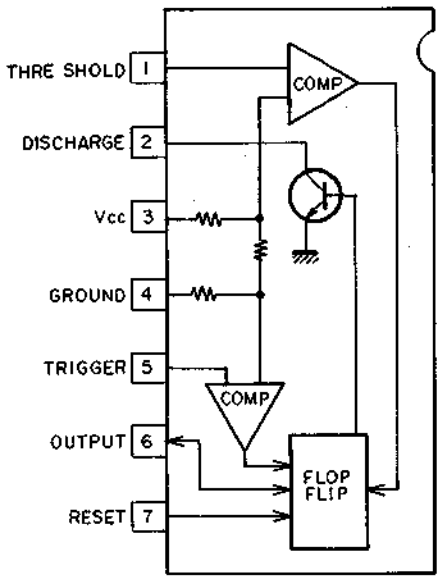
AN6371



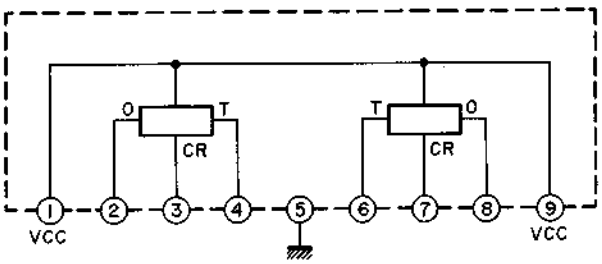
AN6914/MC1458P



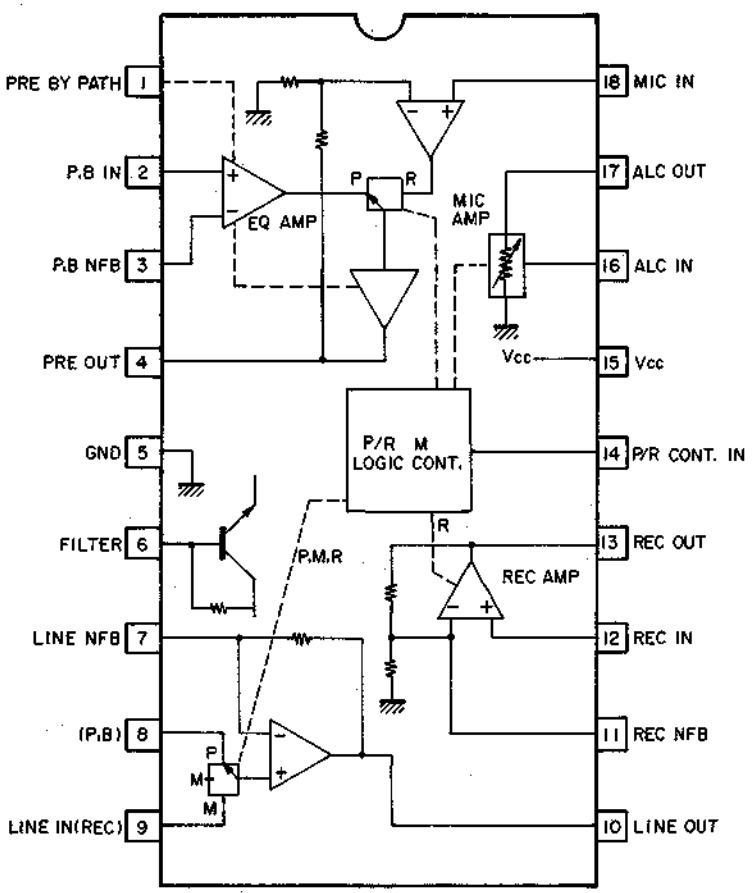
BA222



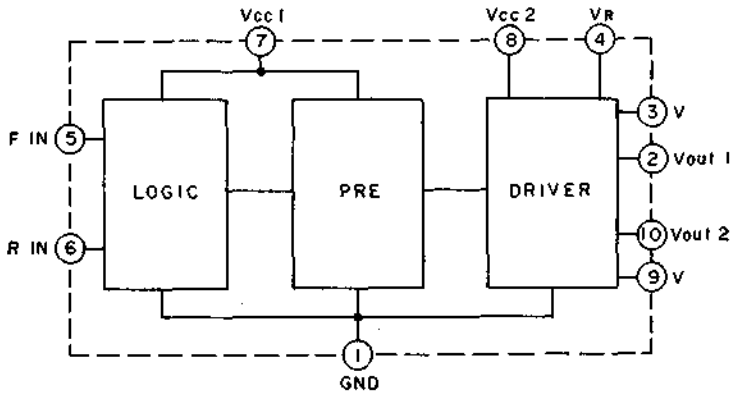
BA236



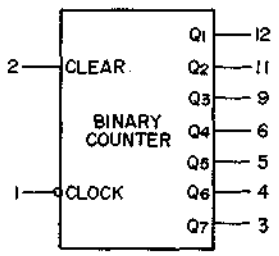
BA5102



BA6109



HD14024BP

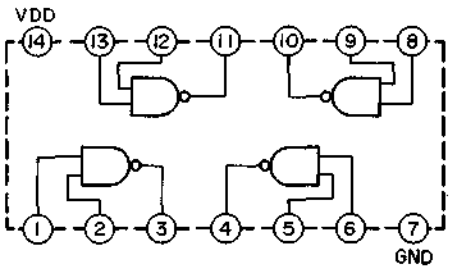


VDD : 14
Vss : 7
NC : 8,10,13

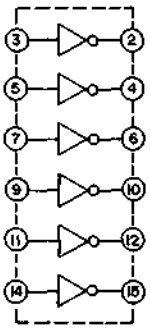
CLOCK Δ	CLEAR	OUTPUT STATE
※	H	ALL OUTPUTS="L"
↓	L	NO CHANGE
↓	L	ADVANCE TO NEXT STATE

Δ:LEVEL CHANGE, ※:DON'T CARE

HD14011B/BP

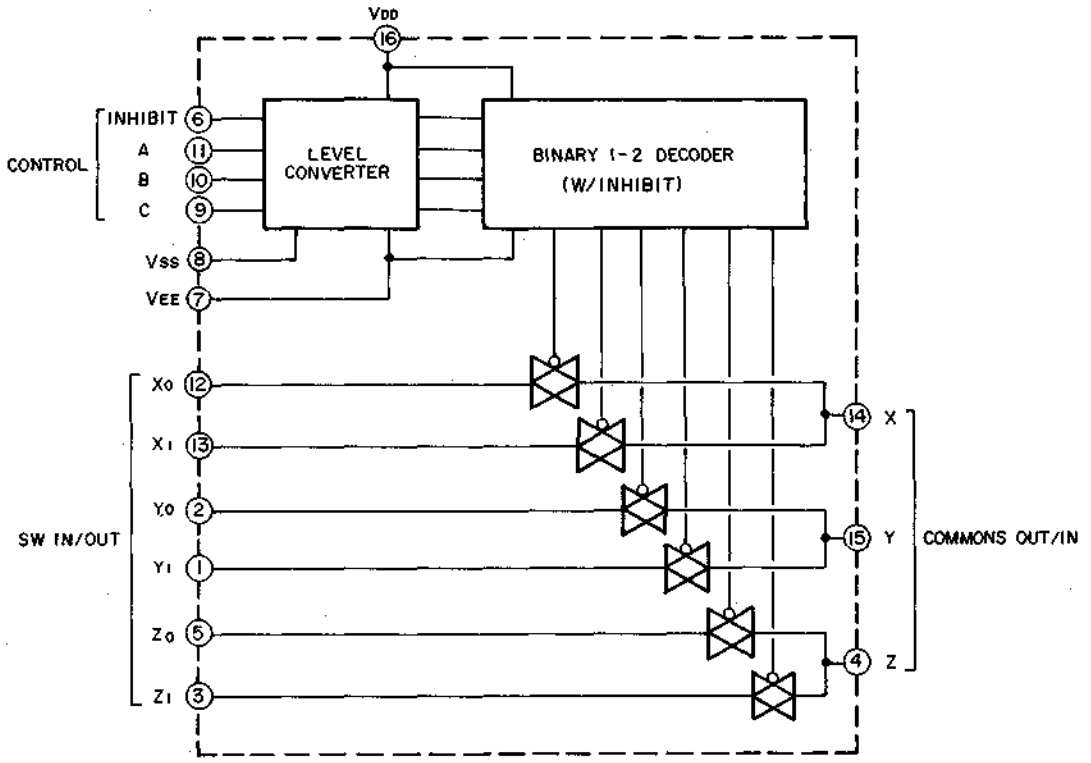


HD14049BP

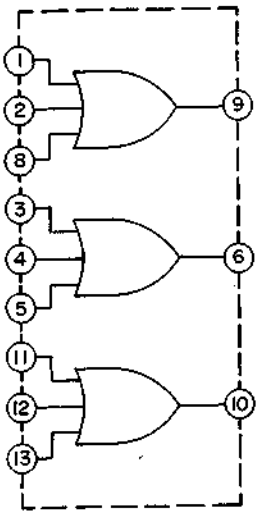


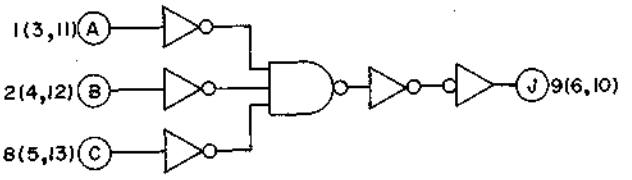
NC= Pin 13.16
VSS= Pin 8
VCC= Pin 1

HD14053BP

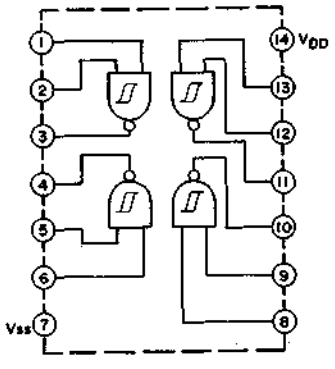


HD14075BP

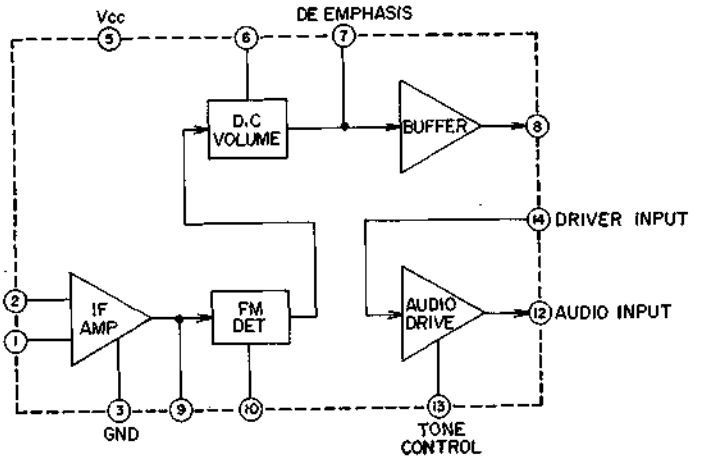




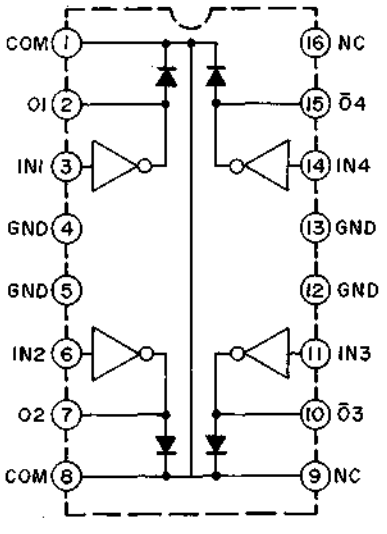
HD14093BP

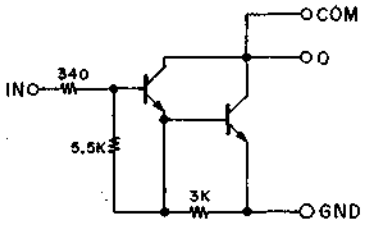


M5144P



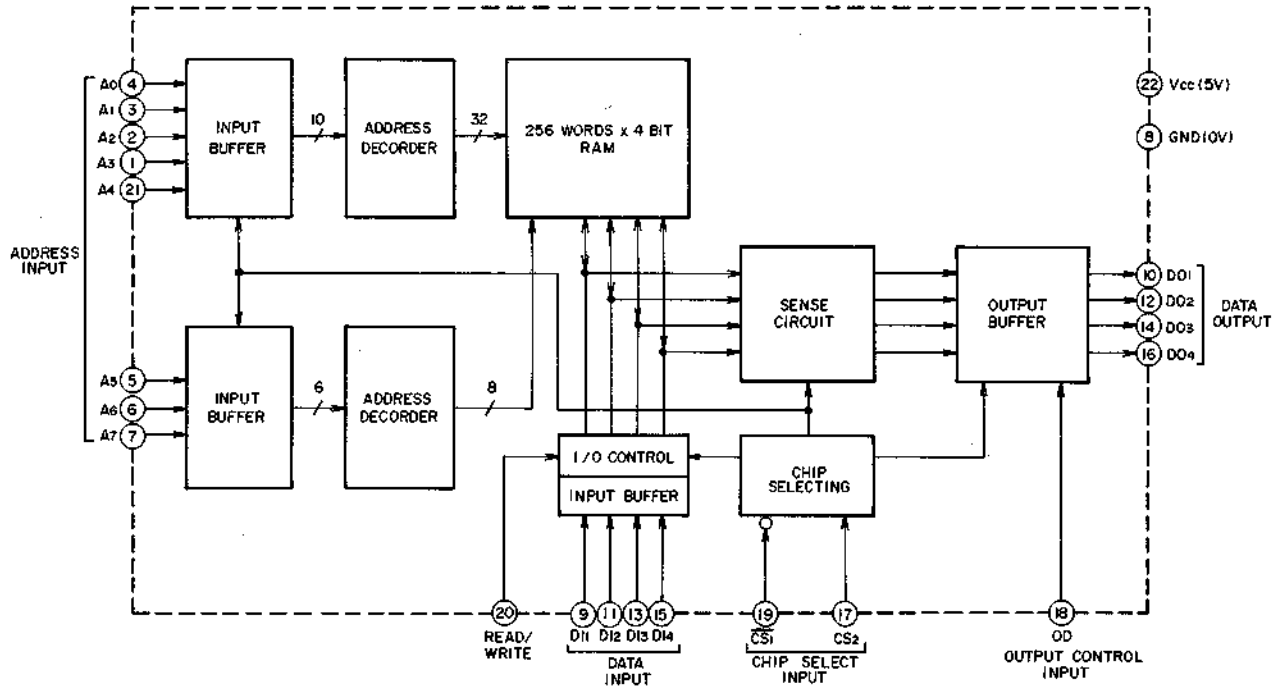
M5432P



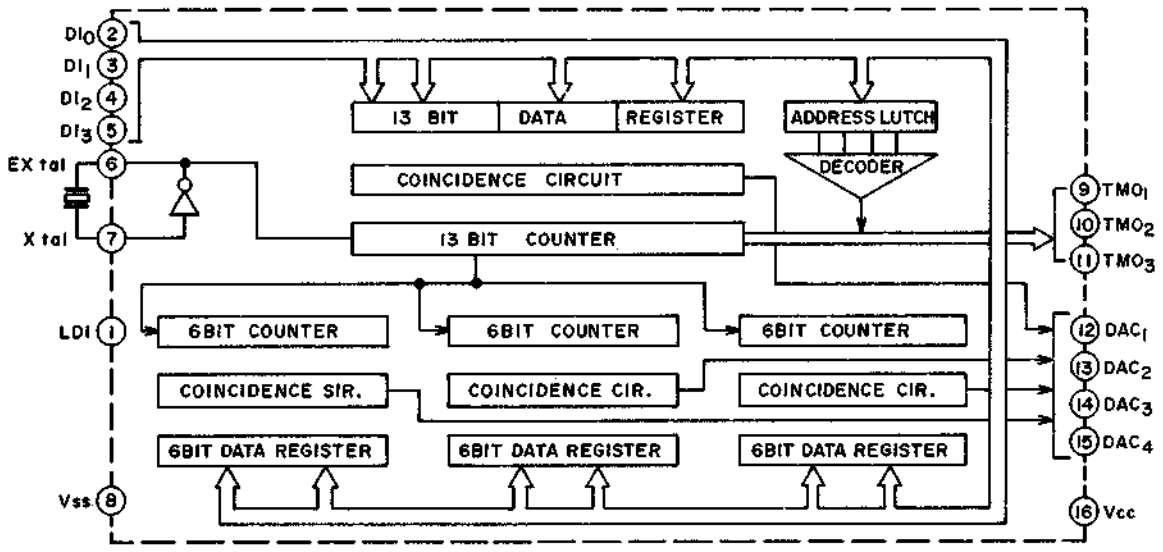


ALL GND CONECTED IN INSIDE

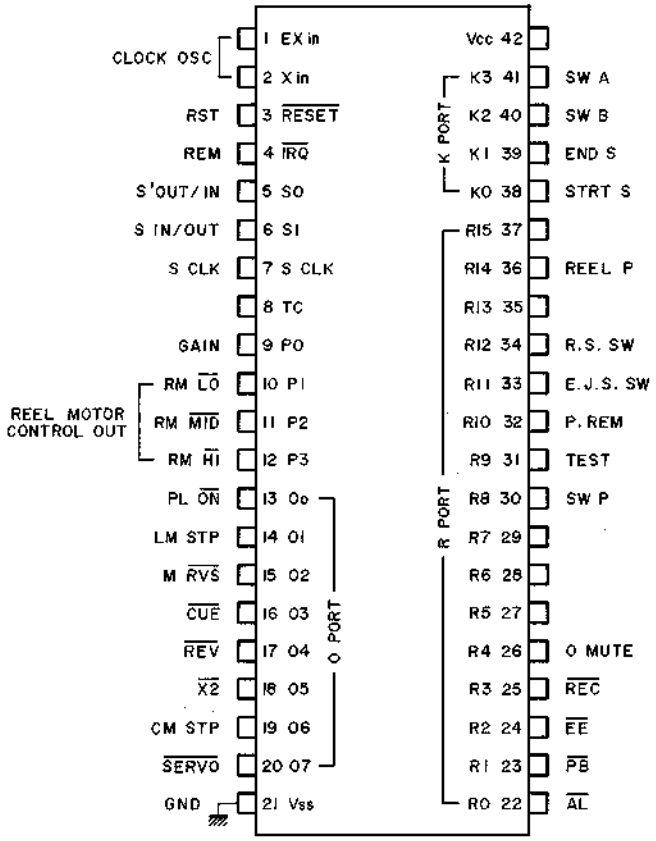
M5L510P

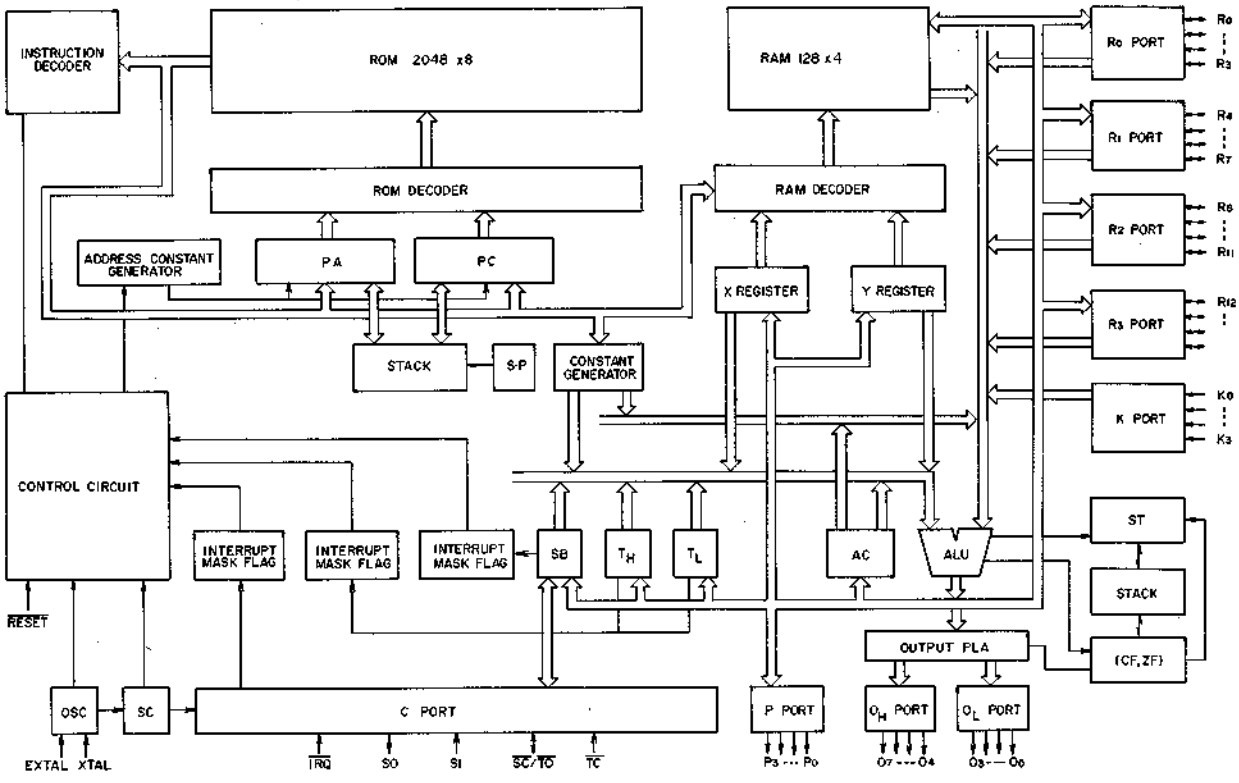


MB88301-P

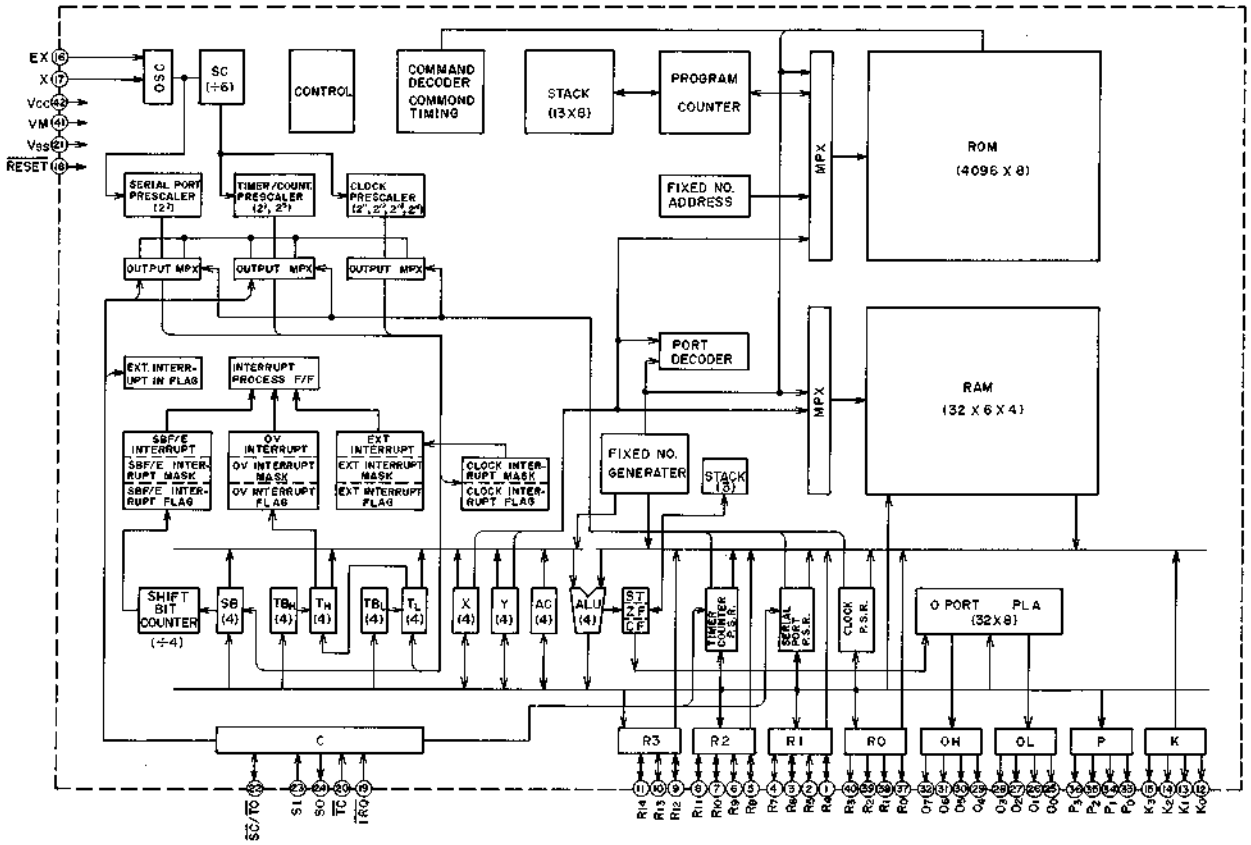


MB8841-679J

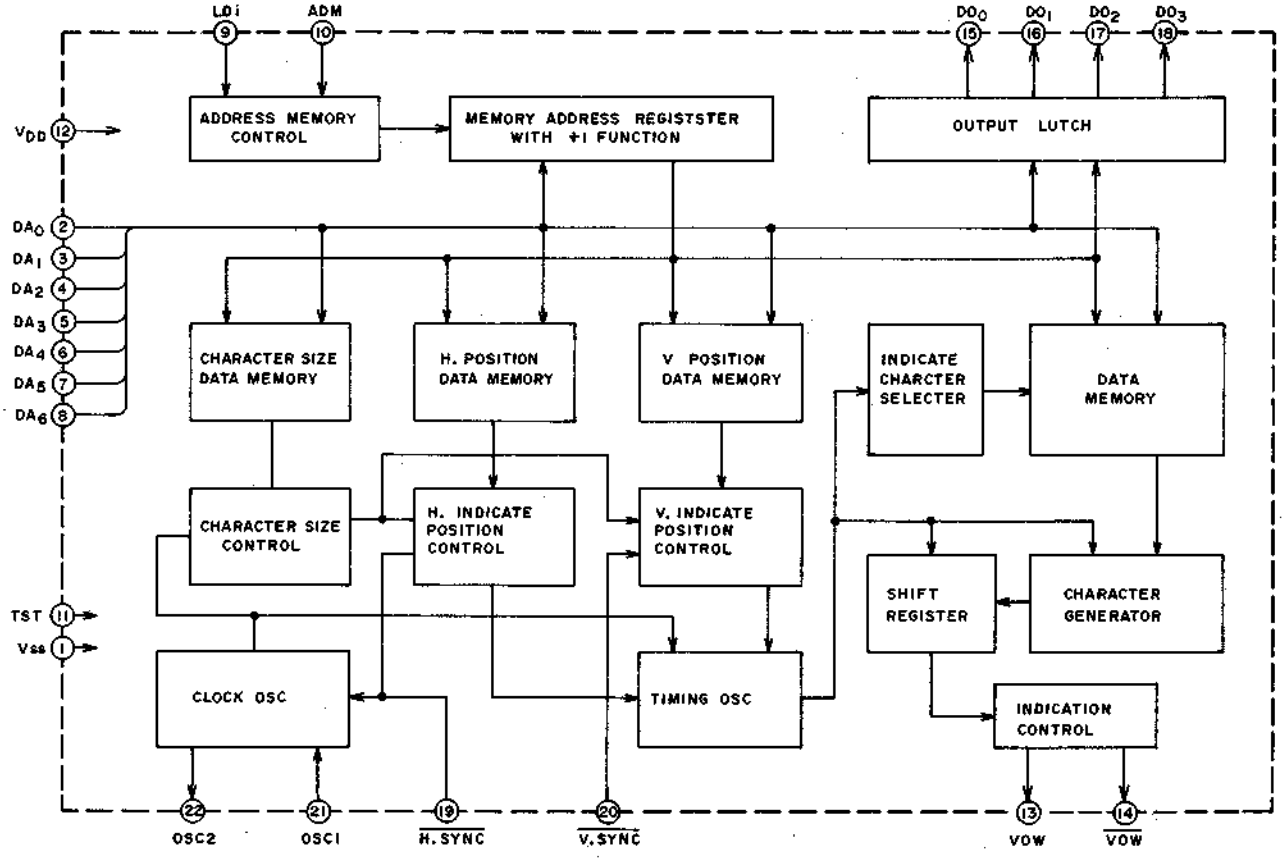

CLOCK OSC
1 EXin
2 Xin
RST
3 RESET
REM
4 IRQ
S'OUT/IN
5 SO
S IN/OUT
6 SI
S CLK
7 S CLK
8 TC
GAIN
9 PO
REEL MOTOR CONTROL OUT
RM LO
10 P1
RM MID
11 P2
RM HI
12 P3
PL ON
13 Oo
LM STP
14 O1
M RVS
15 O2
CUE
16 O3
REV
17 O4
X2
18 O5
CM STP
19 O6
SERVO
20 O7
O PORT
GND
21 Vss
Vcc 42
K PORT
K3 41
SW A
K2 40
SW B
K1 39
END S
KO 38
STRT S
R PORT
RI5 37
RI4 36
REEL P
RI3 35
RI2 34
R.S. SW
RI1 33
E.J.S. SW
RIO 32
P. REM
R9 31
TEST
R8 30
SW P
R7 29
R6 28
R5 27
R4 26
O MUTE
R3 25
REC
R2 24
EE
R1 23
PB
RO 22
AL


INSTRUCTION DECODER
ROM 2048 x8
RAM 128 x4
Ro PORT
R1 PORT
R2 PORT
R3 PORT
K PORT
ROM DECODER
RAM DECODER
ADDRESS CONSTANT GENERATOR
PA
PC
X REGISTER
Y REGISTER
STACK
S-P
CONSTANT GENERATOR
CONTROL CIRCUIT
INTERRUPT MASK FLAG
INTERRUPT MASK FLAG
INTERRUPT MASK FLAG
SB
TH
TL
AC
ALU
ST
STACK
(CF,ZF)
OUTPUT PLA
RESET
OSC
SC
C PORT
P PORT
OH PORT
OL PORT
EXTAL XTAL
IRQ
SO
SI
SC/TO
TC
P3 --- Po
O7 --- O4
O3 --- O0

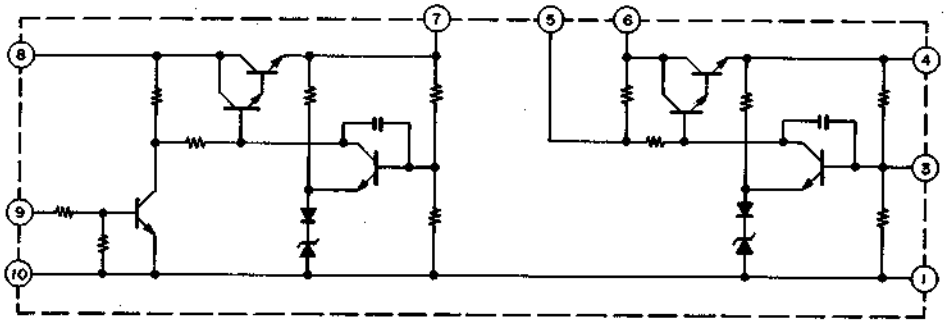
MB88401-151K/161K



MN1227P

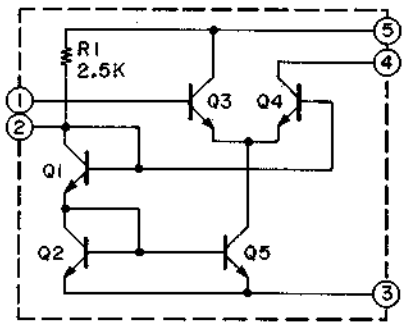


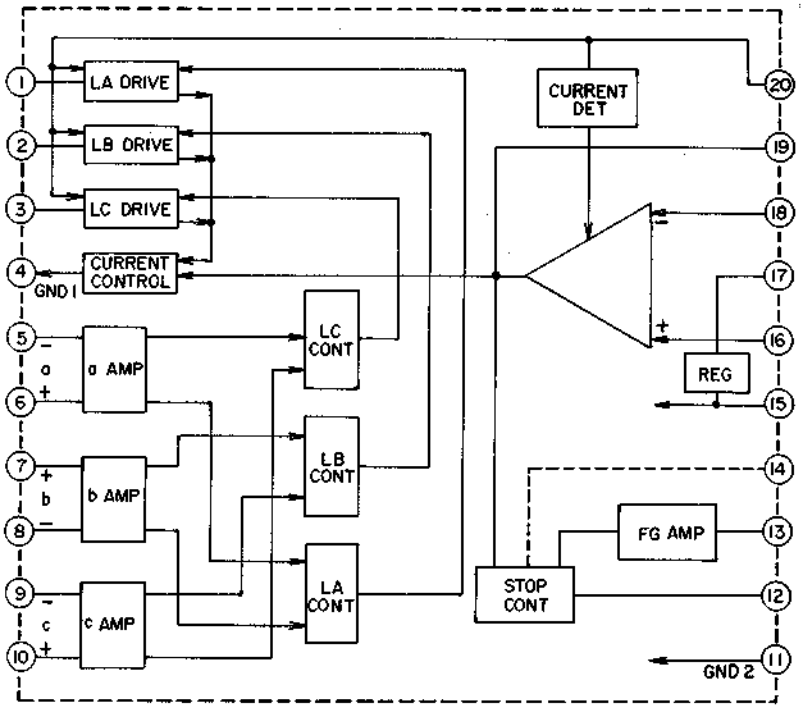
STK-5315



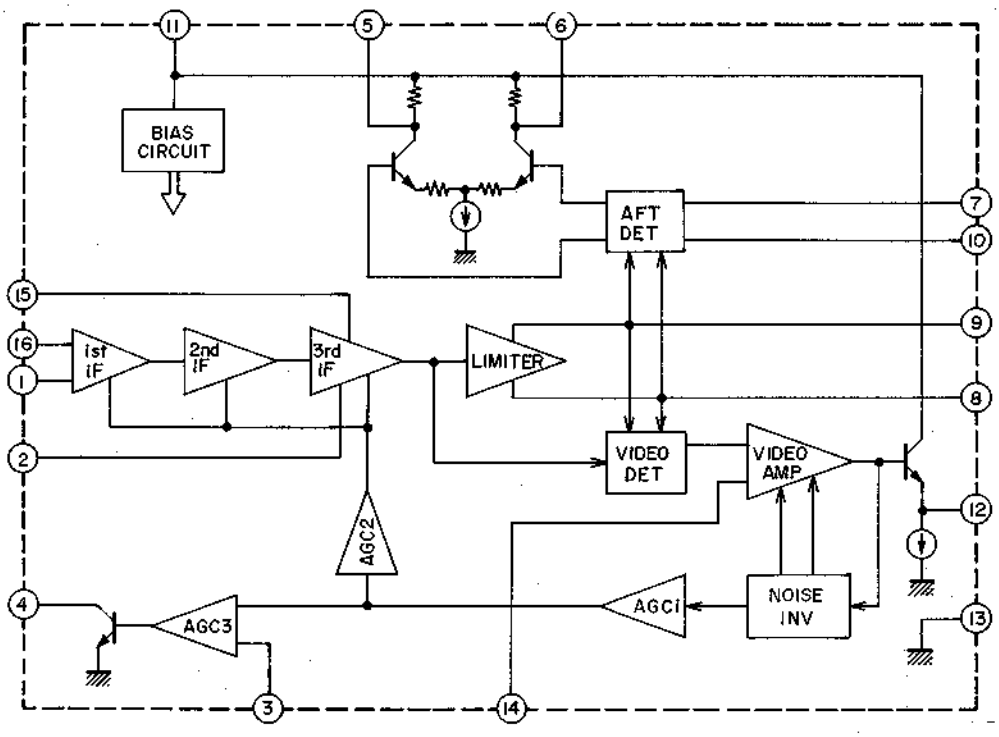
TA7248P

TA7060AP

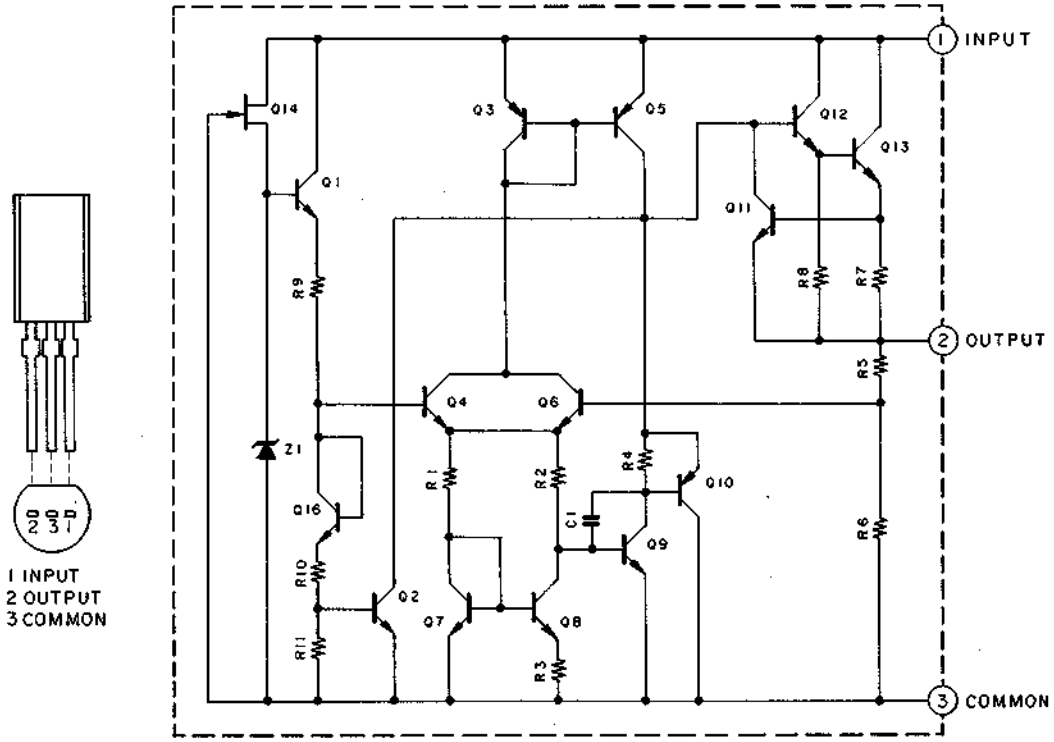




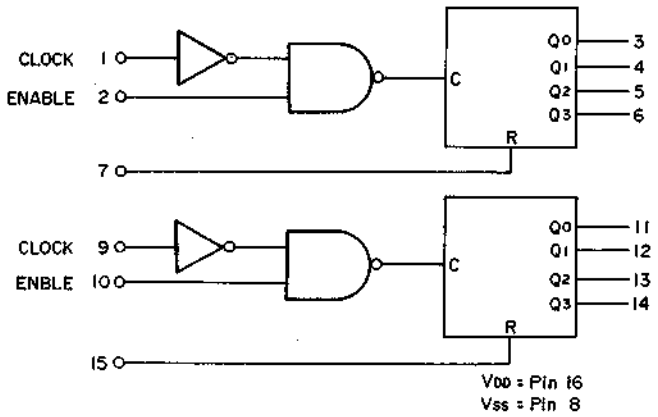
TA7607P



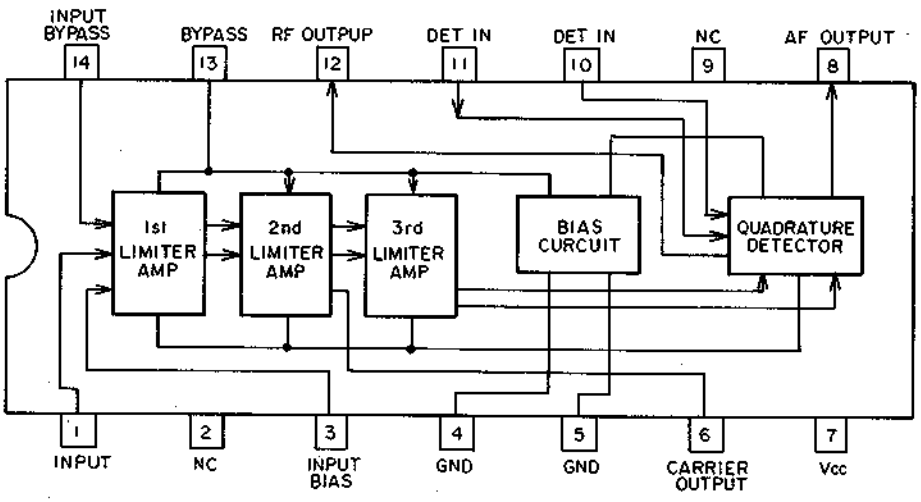
TA78L005AP/TA78L012AP



TC4520BP

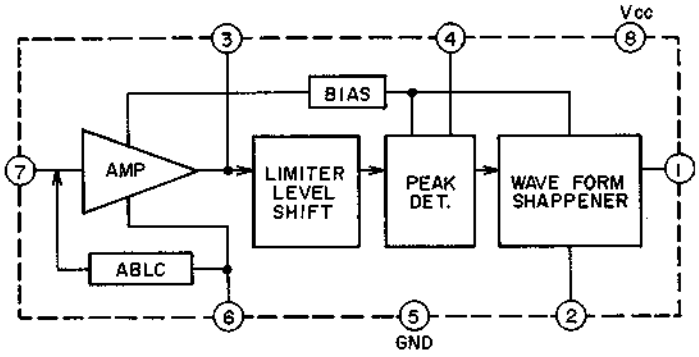


μPC1004C

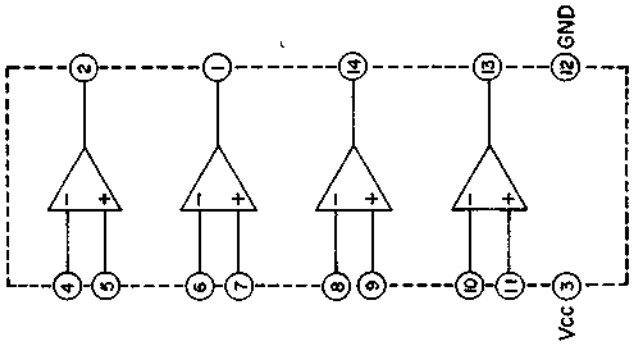


Schematic Diagram VS-2EGN

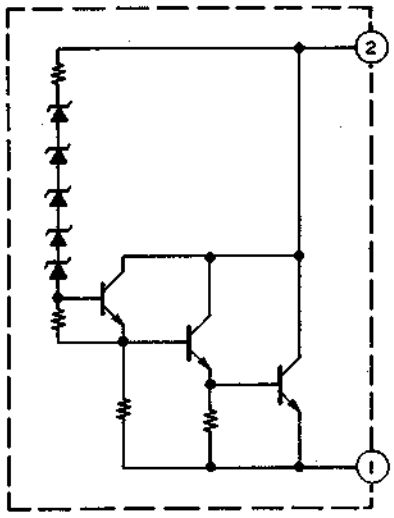
μPC1373H



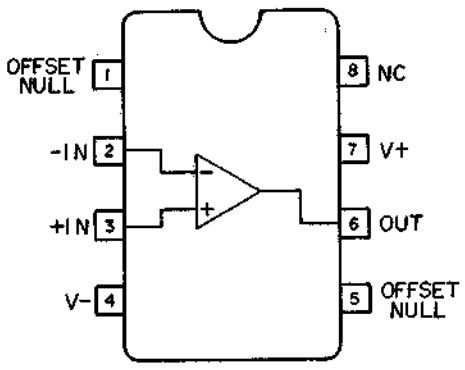
μPC339C

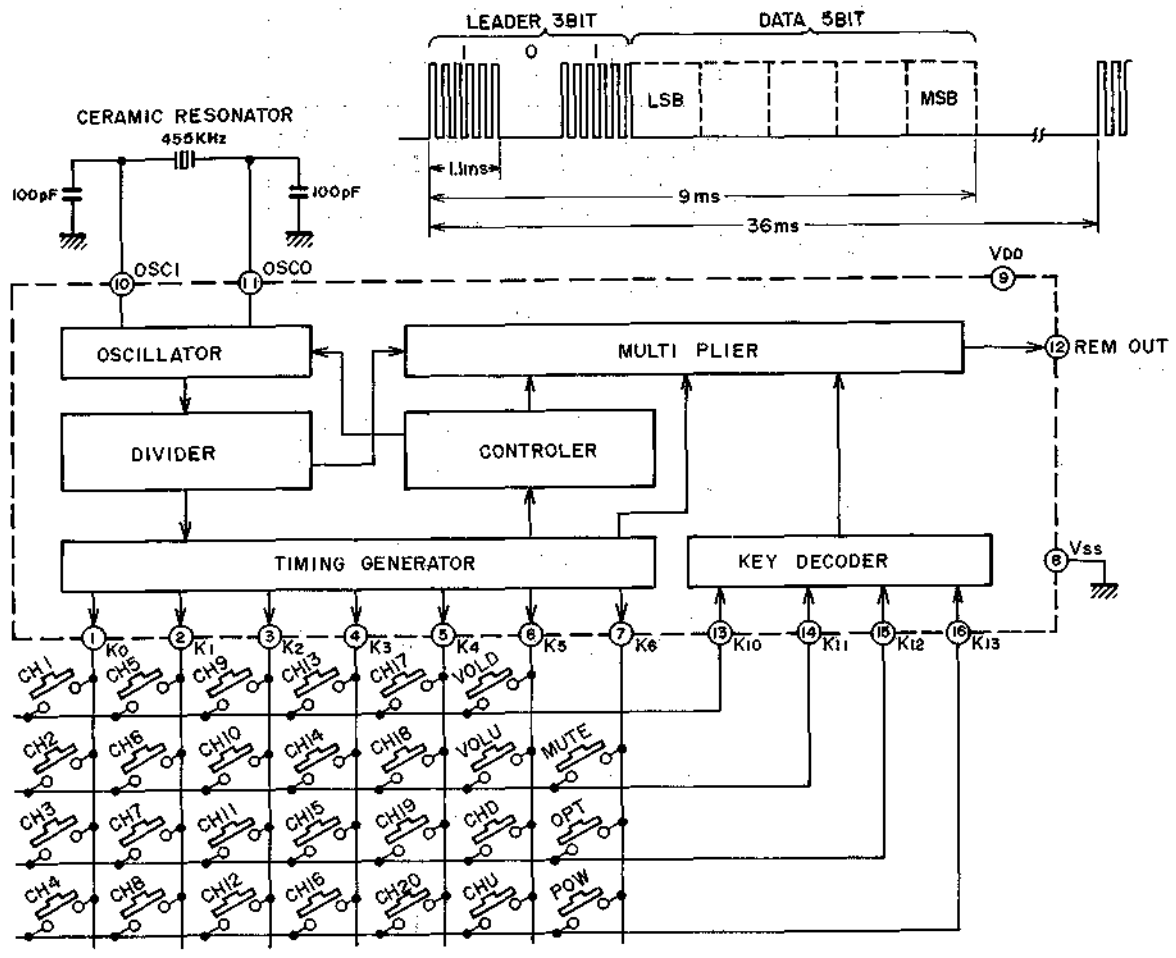


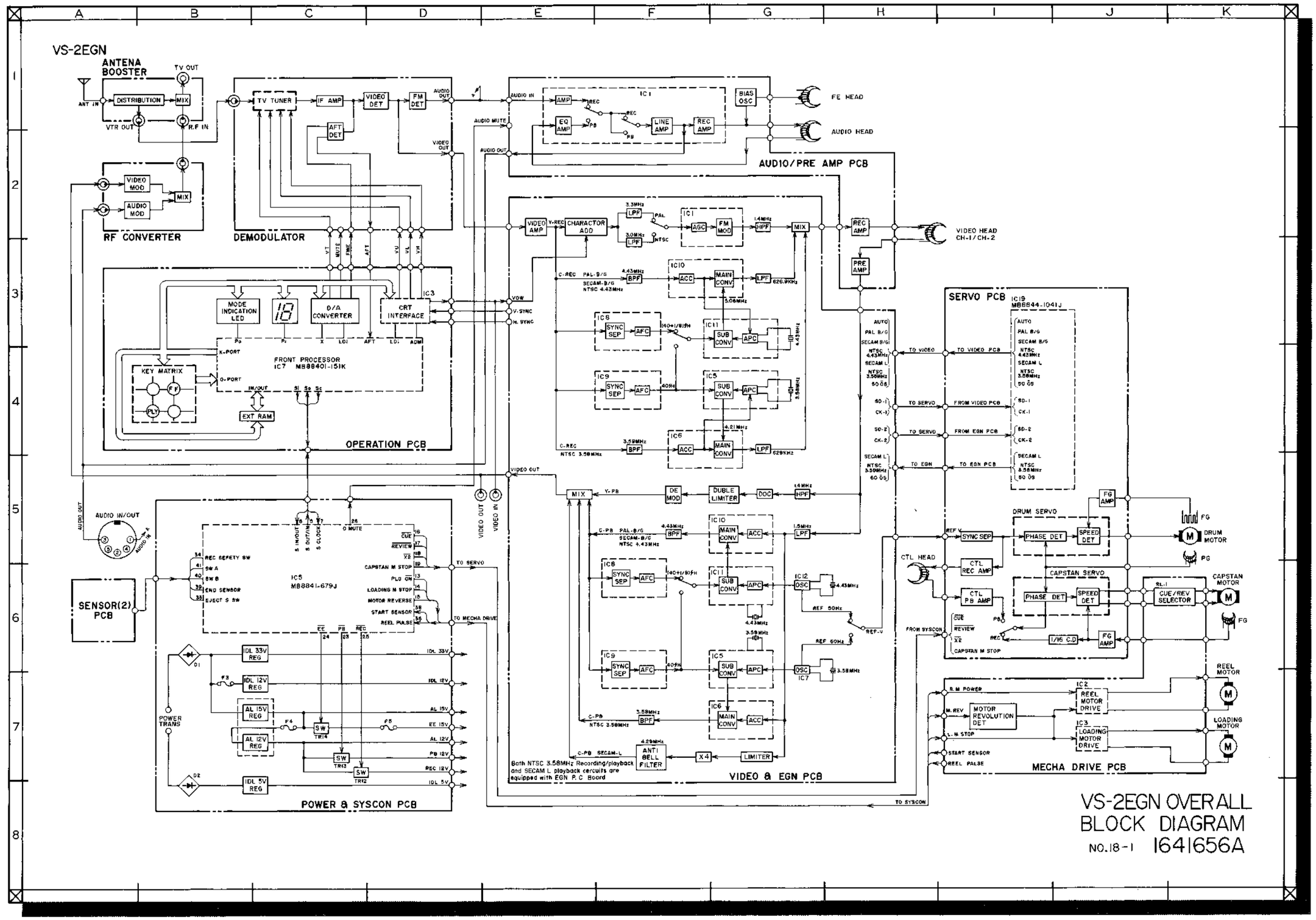
μPC574J



μPC741C/TC

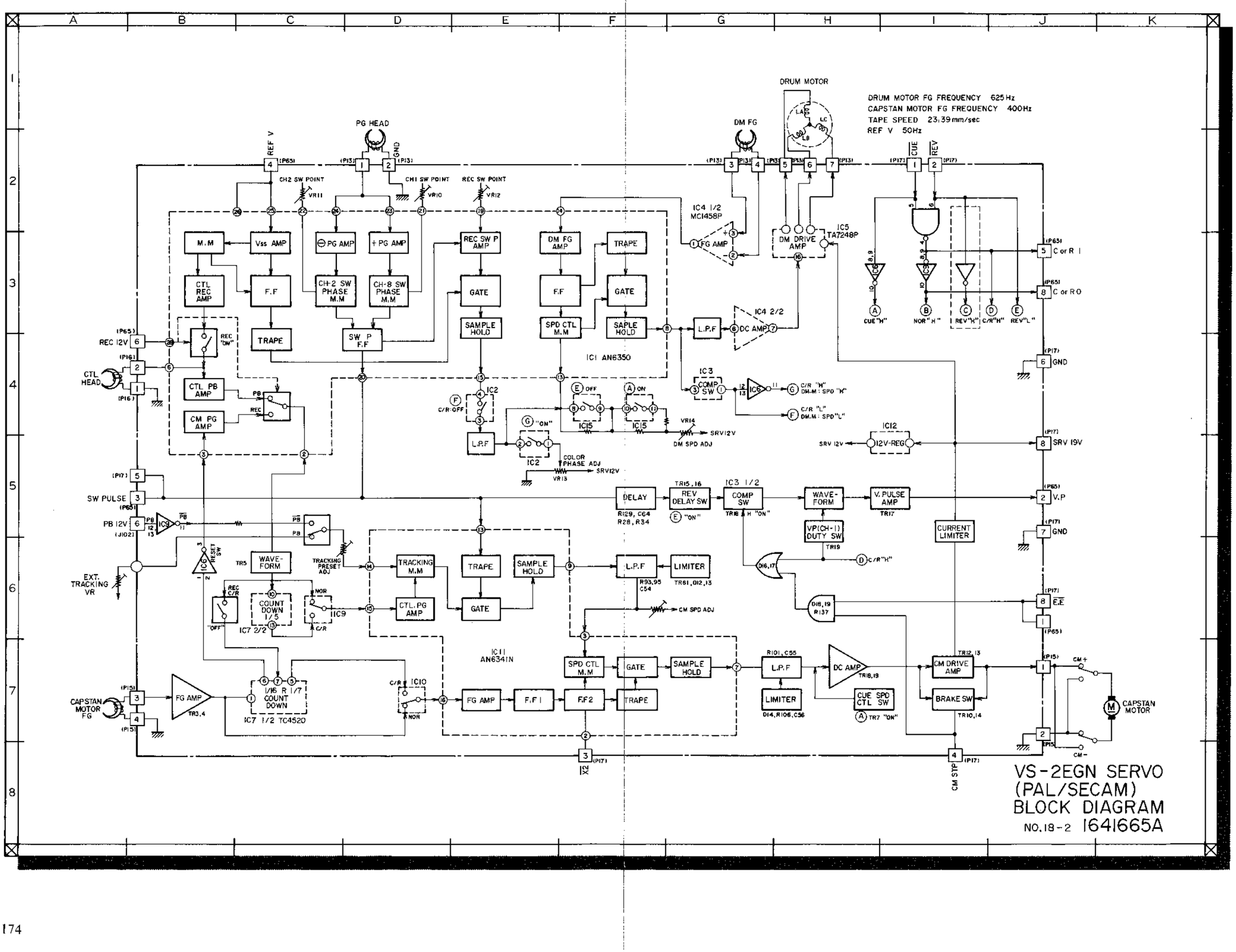



LEADER 3BIT
DATA 8BIT
1
0
1
LSB
MSB
1.1ms
9ms
36ms
CERAMIC RESONATOR
455KHz
100pF
100pF
OSCI
OSCO
VDD
OSCILLATOR
MULTI PLIER
REM OUT
DIVIDER
CONTROLER
TIMING GENERATOR
KEY DECODER
Vss
K0
K1
K2
K3
K4
K5
K6
K10
K11
K12
K13
CH1
CH5
CH9
CH13
CH17
VOLD
CH2
CH6
CH10
CH14
CH18
VOLU
MUTE
CH3
CH7
CH11
CH15
CH19
CHD
OPT
CH4
CH8
CH12
CH16
CH20
CHU
POW



VS-2EGN OVERALL BLOCK DIAGRAM

NO.18-1 1641656A


DRUM MOTOR
DRUM MOTOR FG FREQUENCY 625Hz
CAPSTAN MOTOR FG FREQUENCY 400Hz
TAPE SPEED 23.39mm/sec
REF V 50Hz
PG HEAD
REF V
GND
DM FG
CUE
REV
CH2 SW POINT
CH1 SW POINT
REC SW POINT
VR11
VR10
VR12
IC4 1/2 MC1458P
FG AMP
IC5 TA7248P
DM DRIVE AMP
M.M
Vss AMP
⊖ PG AMP
+ PG AMP
REC SW P AMP
DM FG AMP
TRAPE
CTL REC AMP
F.F
CH-2 SW PHASE M.M
CH-8 SW PHASE M.M
GATE
SAMPLE HOLD
SPD CTL M.M
SAPLE HOLD
L.P.F
DC AMP
IC4 2/2
REC 12V
REC "ON"
CTL HEAD
CTL PB AMP
CM PG AMP
SW P F.F
IC1 AN6350
IC3 COMP SW
C/R "H" DM.M : SPD "H"
C/R "L" DM.M : SPD "L"
IC2
C/R-OFF
"ON"
OFF
ON
IC15
VR14
SRV12V
DM SPD ADJ
IC12
12V-REG
SRV 12V
SRV 19V
COLOR PHASE ADJ
VR13
C or R I
C or R O
CUE "H"
NOR "H"
REV "H"
C/R "H"
REV "L"
GND
SW PULSE
PB 12V
DELAY
R129, C64
R28, R34
REV DELAY SW
"ON"
COMP SW
WAVE-FORM
V. PULSE AMP
TR17
V.P
VP(CH-1) DUTY SW
TR19
C/R "H"
CURRENT LIMITER
EXT. TRACKING VR
IC9
PRESET SW
TR5
WAVE-FORM
TRACKING PRESET ADJ
TRACKING M.M
TRAPE
SAMPLE HOLD
L.P.F
LIMITER
TR61, D12, 13
R93, 95
C54
CM SPD ADJ
D16, 17
D18, 19
R137
REC C/R
COUNT DOWN 1/5
IC7 2/2
"OFF"
NOR
C/R
CTL. PG AMP
GATE
IC11 AN6341N
SPD CTL M.M
GATE
SAMPLE HOLD
L.P.F
R101, C55
LIMITER
D14, R106, C56
DC AMP
TR18, 19
CUE SPD CTL SW
"ON"
CM DRIVE AMP
TR12, 13
BRAKE SW
TR10, 14
CM+
CM-
CAPSTAN MOTOR
CAPSTAN MOTOR FG
FG AMP
TR3, 4
1/16 R 1/7 COUNT DOWN
IC7 1/2 TC4520
C/R
IC10
NOR
FG AMP
F.F1
F.F2
TRAPE
CM STP
E/E
VS-2EGN SERVO (PAL/SECAM) BLOCK DIAGRAM
NO.18-2 1641665A

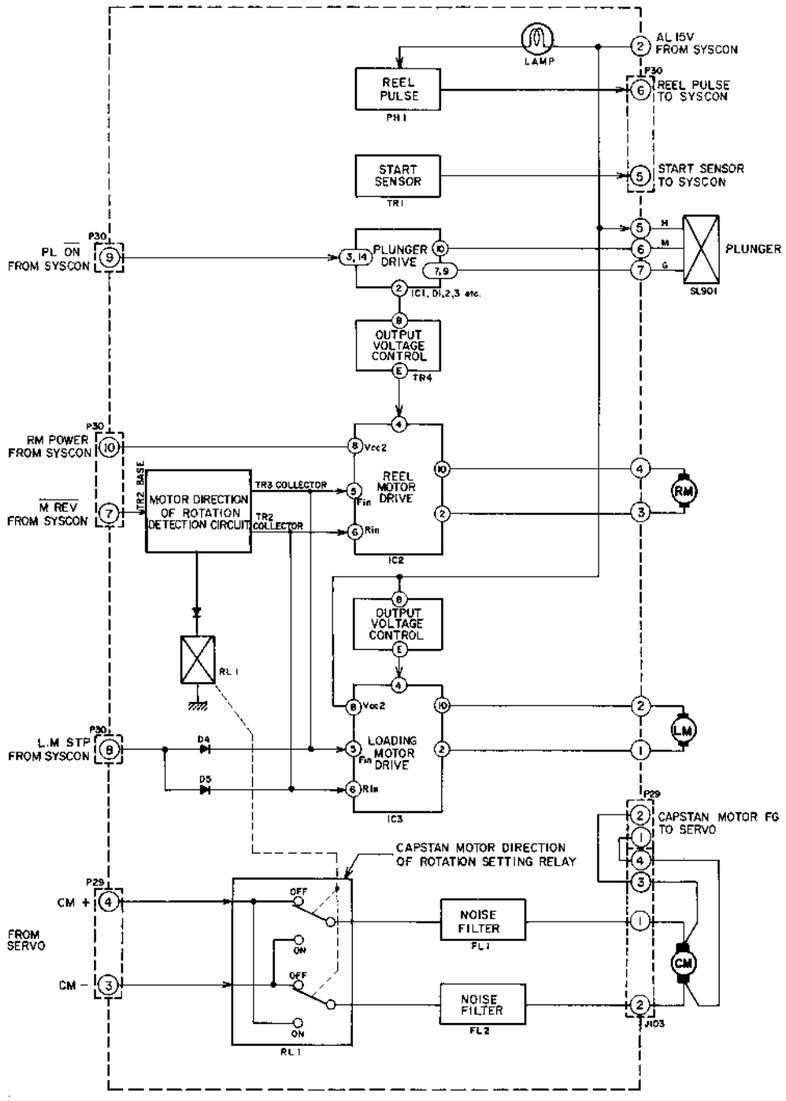
DRUM MOTOR FG FREQUENCY 750Hz
CAPSTAN MOTOR FG FREQUENCY 570Hz
TAPE SPEED 33.35mm/sec
REF V 60Hz

DRUM MOTOR
PG HEAD
DM FG
REF V
GND
CH2 SW POINT VR11
CH1 SW POINT VR10
REC SW POINT VR12
IC4 1/2 MC1458P
IC5 TA7248P
DM DRIVE AMP
FG AMP
M.M
Vss AMP
⊖PG AMP
+PG AMP
REC SW P AMP
DM FG AMP
TRAPE
CTL REC AMP
F.F
CH-2 SW PHASE M.M
CH-8 SW PHASE M.M
GATE
SAMPLE HOLD
SW P F.F
SPD CTL M.M
L.P.F
DC AMP
IC4 2/2
IC1 AN6350
REC 12V
REC "ON"
CTL HEAD
CTL PB AMP
CM PG AMP
PB
REC
IC2
C/R:OFF
"ON"
COLOR PHASE ADJ
VR13
SRV12V
IC15
VR14
DM SPD ADJ
IC3
COMP SW
C/R "H" DM.M : SPD "H"
C/R "L" DM.M : SPD "L"
IC12
12V-REG
SRV 12V
SRV 19V
CUE
REV
CUE"H"
NOR"H"
REV"H"
C/R"H"
REV"L"
C or R I
C or R O
GND
SW PULSE
PB 12V
DELAY
R129, C64
R26, R34
REV DELAY SW
TR15, 16
IC3 1/2
COMP SW
TR18
WAVE-FORM
V. PULSE AMP
TR17
VP(CH-1) DUTY SW
TR19
CURRENT LIMITER
V.P
GND
E.E
EXT. TRACKING VR
IC6
RESET SW
WAVE-FORM
TR5
TRACKING PRESET ADJ
TRACKING M.M
CTL. PG AMP
TRAPE
SAMPLE HOLD
L.P.F
LIMITER
TR61, 012, 13
D16, 17
D18, 19 R137
R93, 95 C54
CM SPD ADJ
REC C/R
"OFF"
COUNT DOWN 1/5
IC7 2/2
IC9
NOR
C/R
IC11 AN6341N
IC10
R101, C55
CM DRIVE AMP
TR12, 13
CM+
CM-
CAPSTAN MOTOR
CAPSTAN MOTOR FG
FG AMP
TR3, 4
1/19 R COUNT DOWN
IC17 HD14024BP
COUNT DOWN 1/5
IC7 1/2 TC4520
F.F1
F.F2
BRAKE SW
TR10, 14
CUE SPD CTL SW
TR7 "ON"
CM STP
IC2

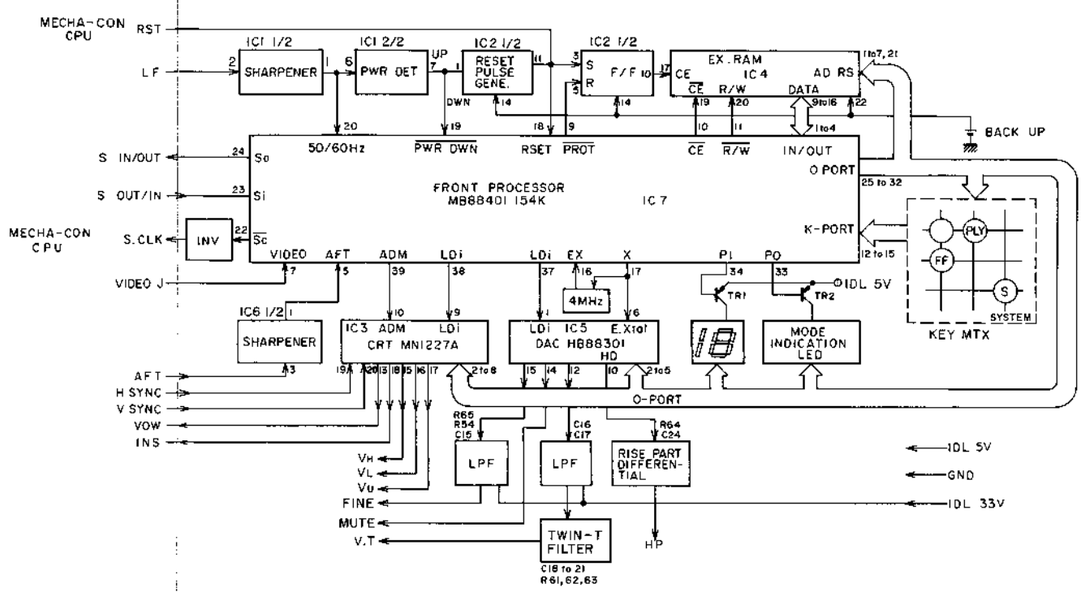
VS-2EGN SERVO (NTSC) BLOCK DIAGRAM

NO.18-3 1641666A

VS-2EGN



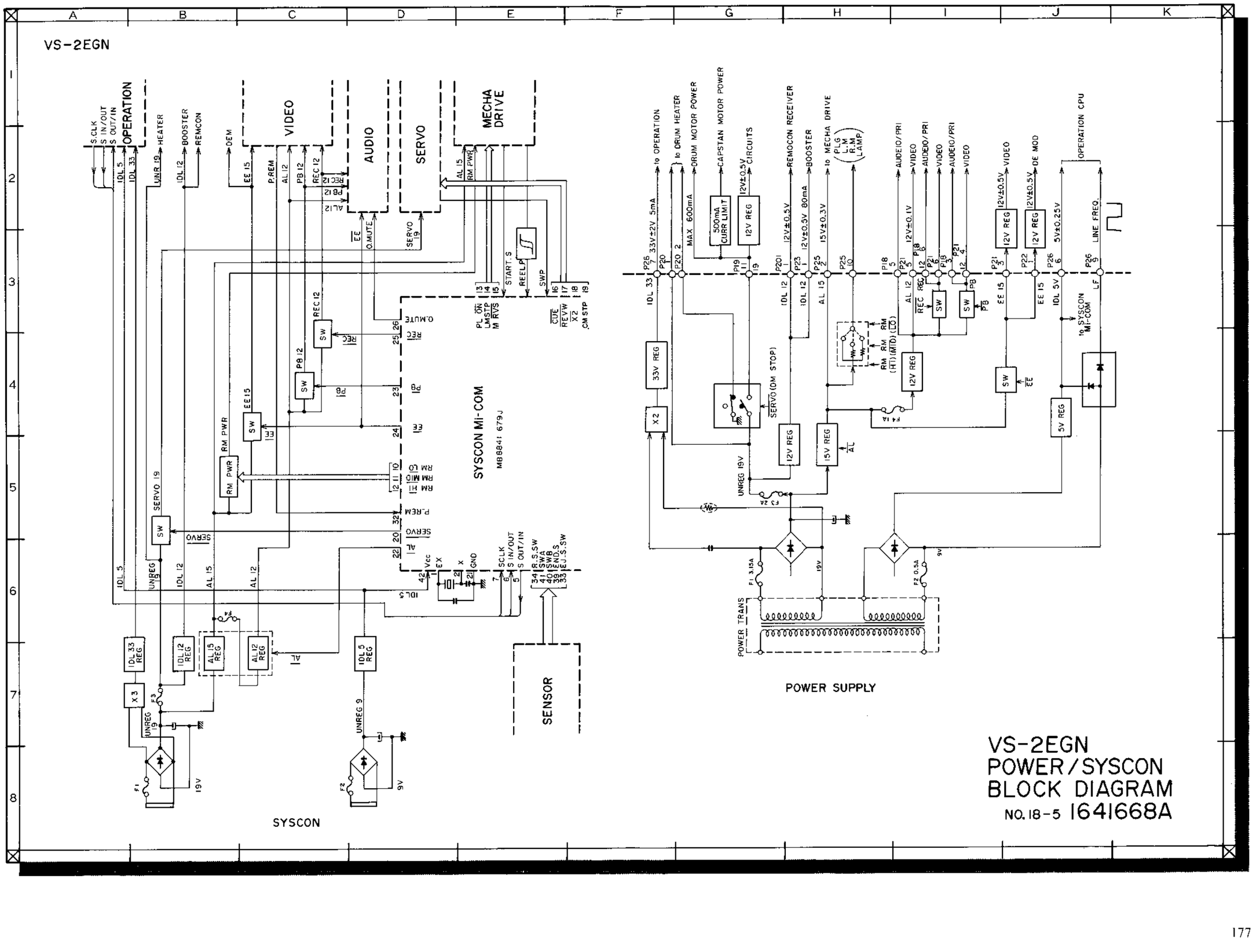
MECHANISM DRIVE



OPERATION

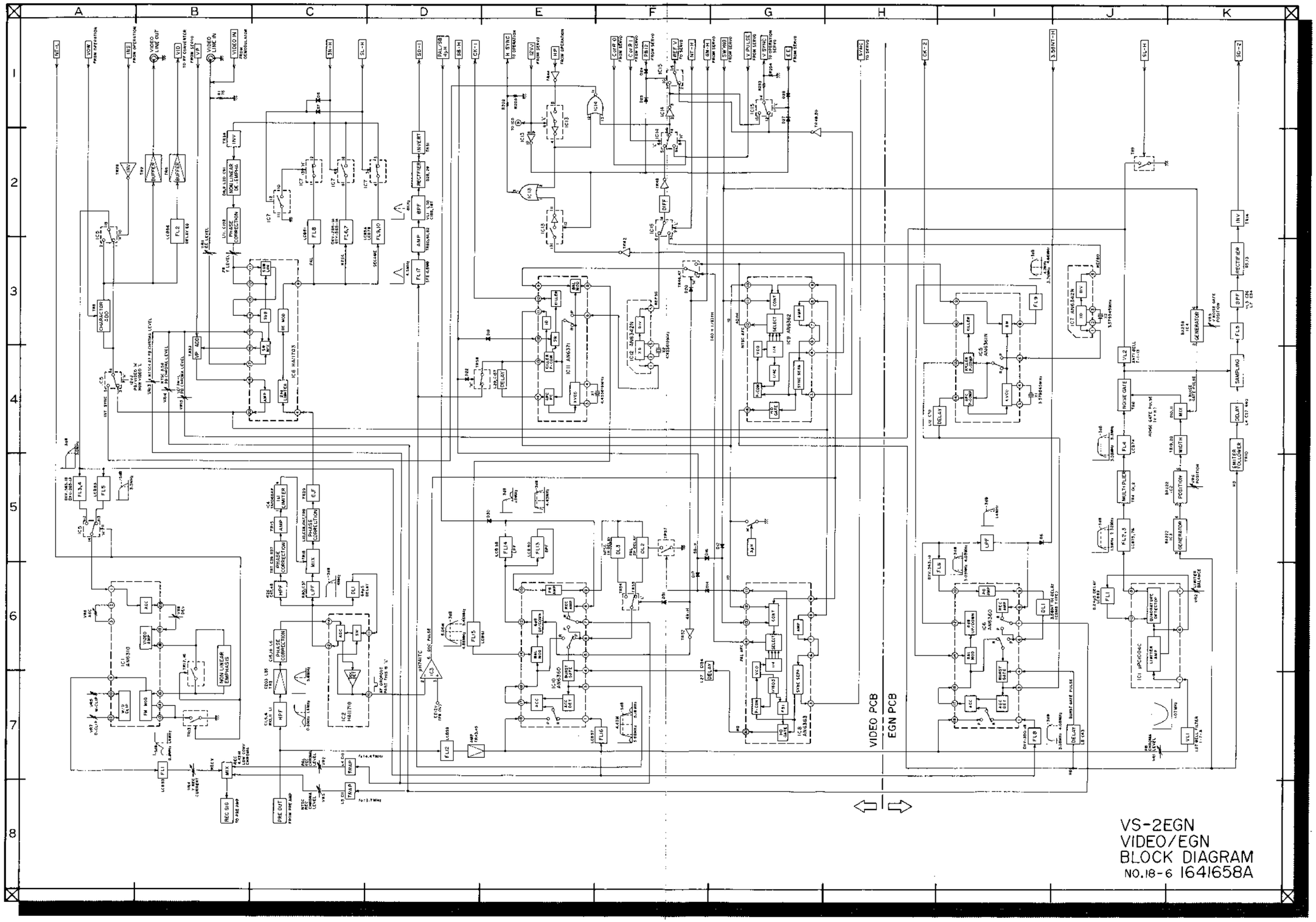
VS-2EGN
MECHA/OPERATION
BLOCK DIAGRAM
NO.18-4 1641667A

VS-2EGN



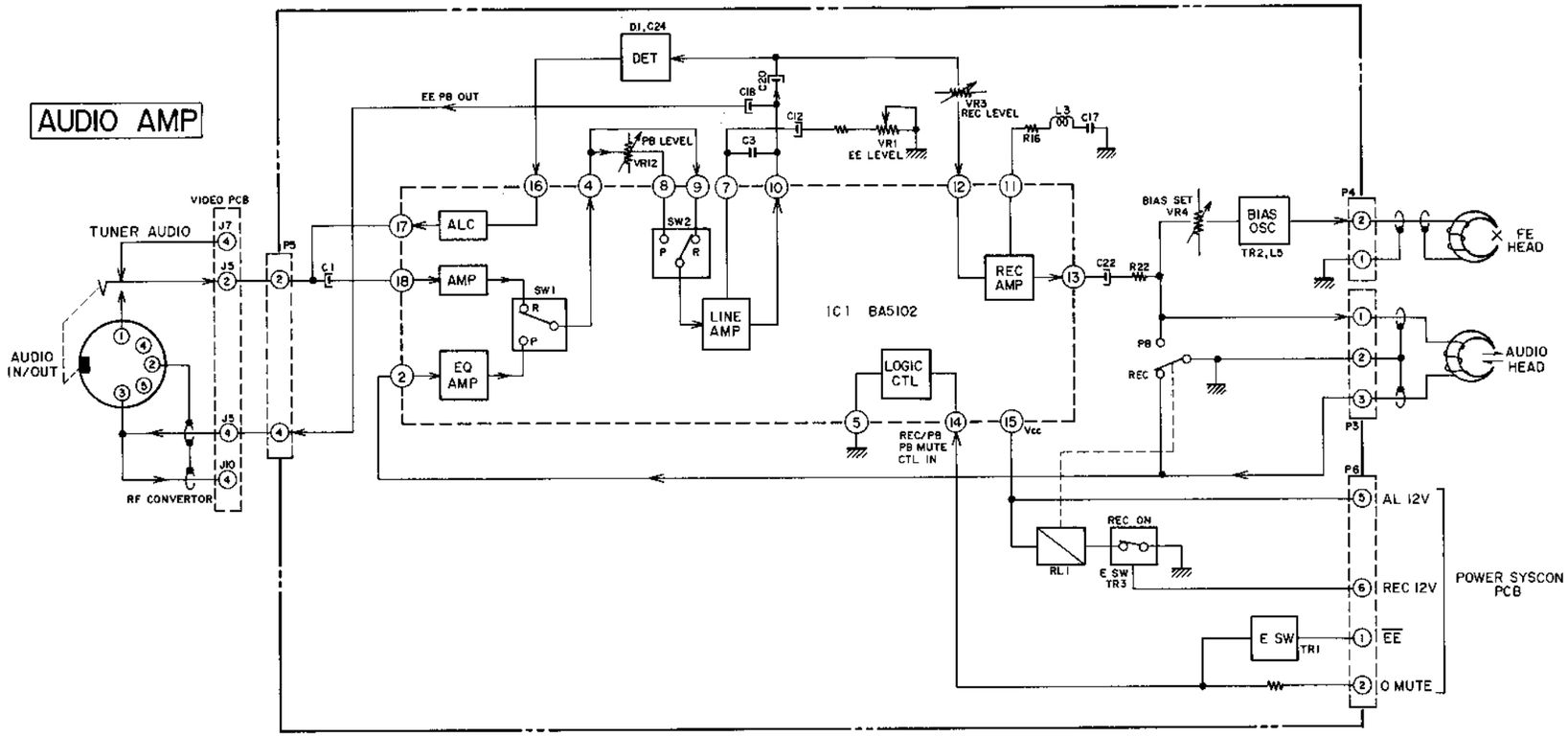
VS-2EGN POWER/SYSCON BLOCK DIAGRAM

NO. 18-5 1641668A

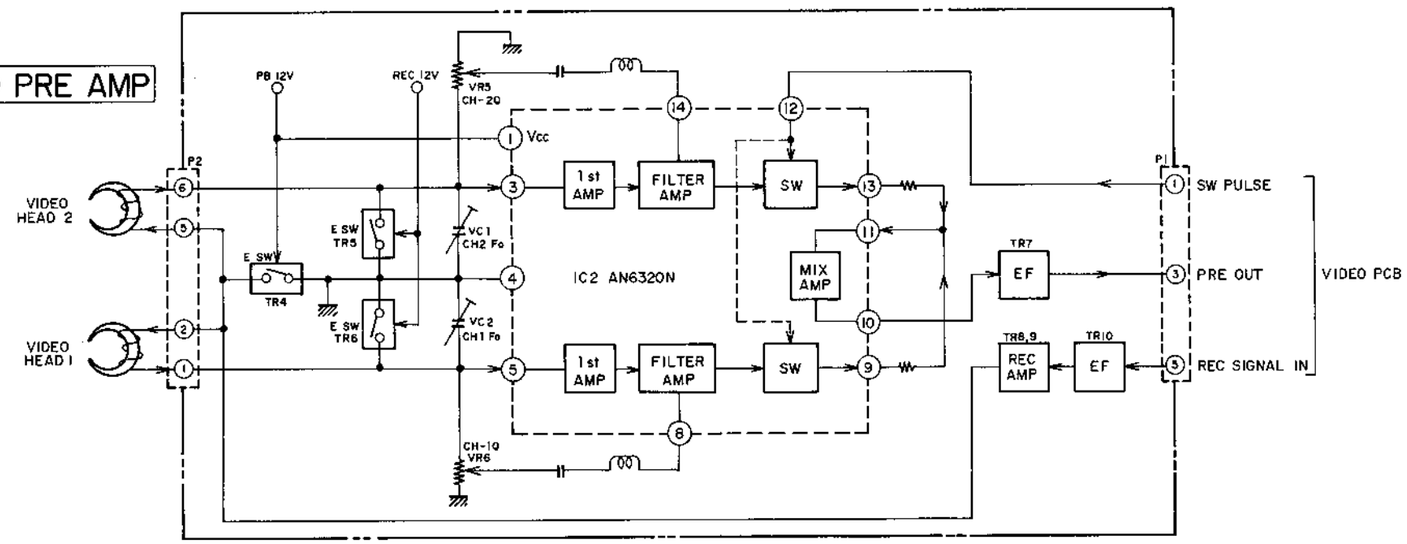

A
B
C
D
E
F
G
H
I
J
K
1
2
3
4
5
6
7
8
VIDEO PCB
EGN PCB
VS-2EGN
VIDEO/EGN
BLOCK DIAGRAM
NO.18-6 1641658A

VS-2EGN

AUDIO AMP



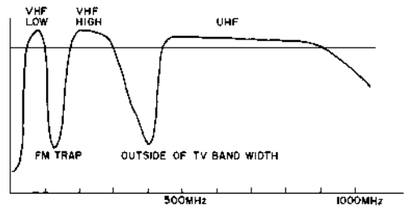
VIDEO PRE AMP

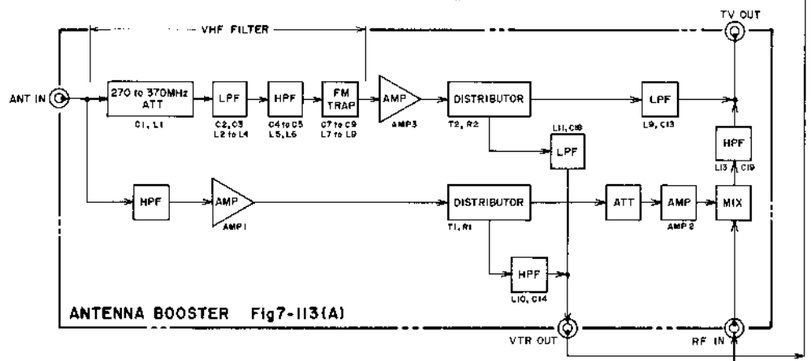


VS-2EGN
AUDIO/VIDEO PRE
BLOCK DIAGRAM
NO.18-7 1641658A

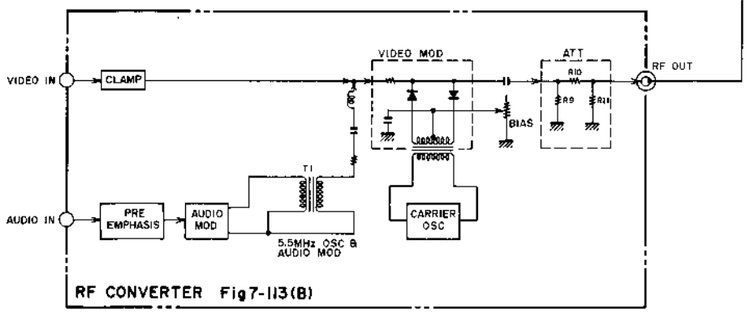
VS-2EGN

Fig7-114 Filter Characteristics

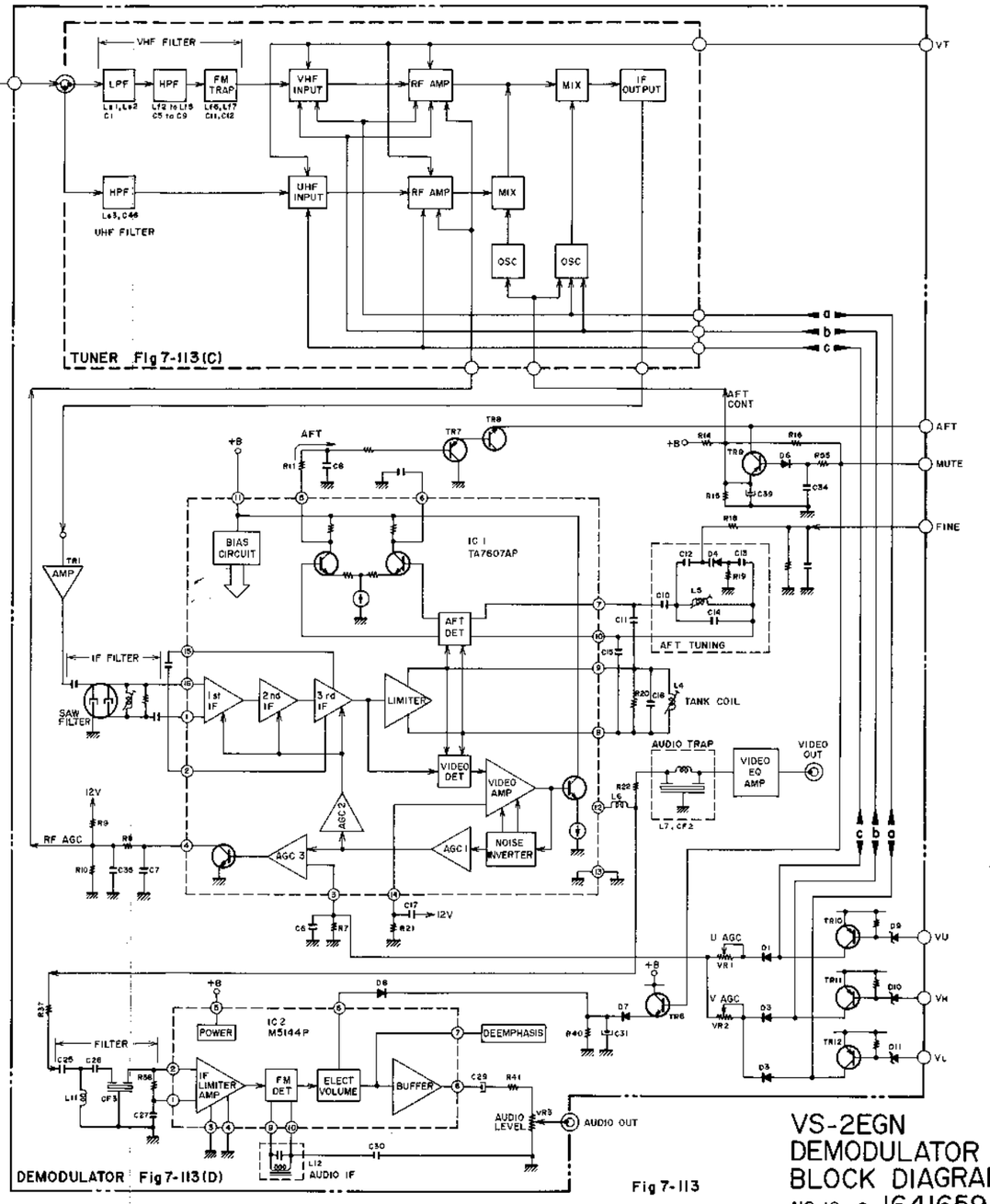




ANTENNA BOOSTER Fig7-113(A)



RF CONVERTER Fig7-113(B)



DEMODULATOR Fig7-113(D)

Fig 7-113

VS-2EGN
DEMODULATOR
BLOCK DIAGRAM
NO.18-8 1641659A

VS-2EGN

AUDIO/PRE PCB
V1009A5180

VIDEO(EGN) PCB
V1009A5280

LOWER DRUM
PCB VS-8068

UPPER DRUM
PCB VS-8012

EGN PCB V1009B5290

SERVO(EGN) PCB
V1009A5270

TUNER

DEMODULATOR PCB(TV TUNER
CDEI-015)

RF
CONVERTOR PCB
(MDK3-253)

BOOSTER PCB
(YBCI-001)

POWER & SYSCON PCB
V1009A519A

POWER FILTER PCB
V1009D5210

SENSOR(2) PCB V1004C5540

V1004C5544
Ej. S. SW

V1004C5543
SW B

V1004C5542
SW A

V1004C5541
R. S. SW

LED(EGN) PCB V1009D5320

MECHA DRIVE PCB
V1009A519B

INTERMEDIATE PCB V1009A519C

OPERATION PCB
V1009A5170

FUNCTION
ON

OFF/TIMER

PRESET A
SELECT

DISPLAY
ON/OFF B

COUNTER
RESET C

TIMER/SLEEP
PROGRAM RO

CLOCK

PRESET

CANCEL
FINE TUNING

EJECT

REW

STOP

FF

REV

PLAY

CUE

SYSTEM

REC

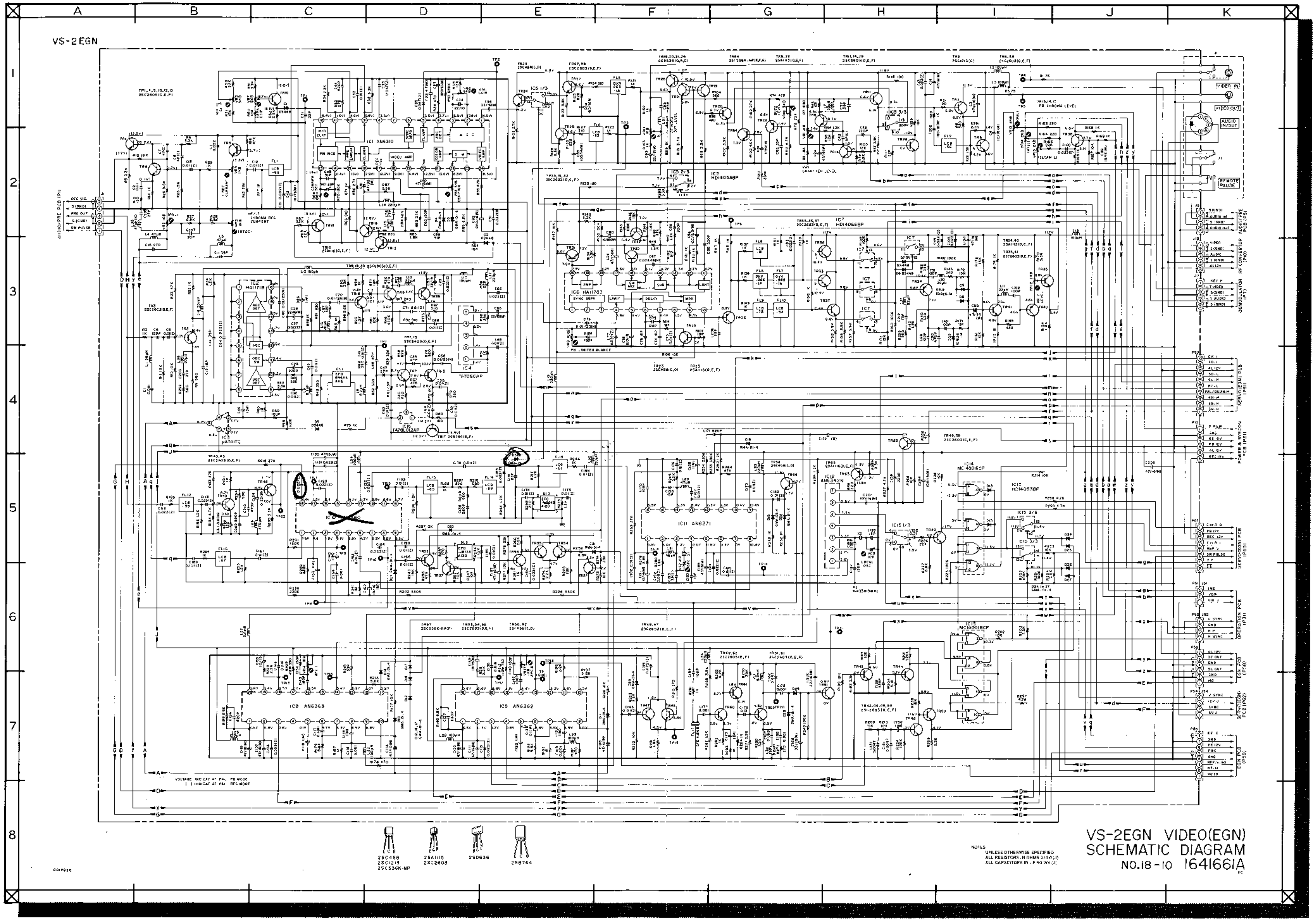
COUNTER
AUTO STOP

PAUSE

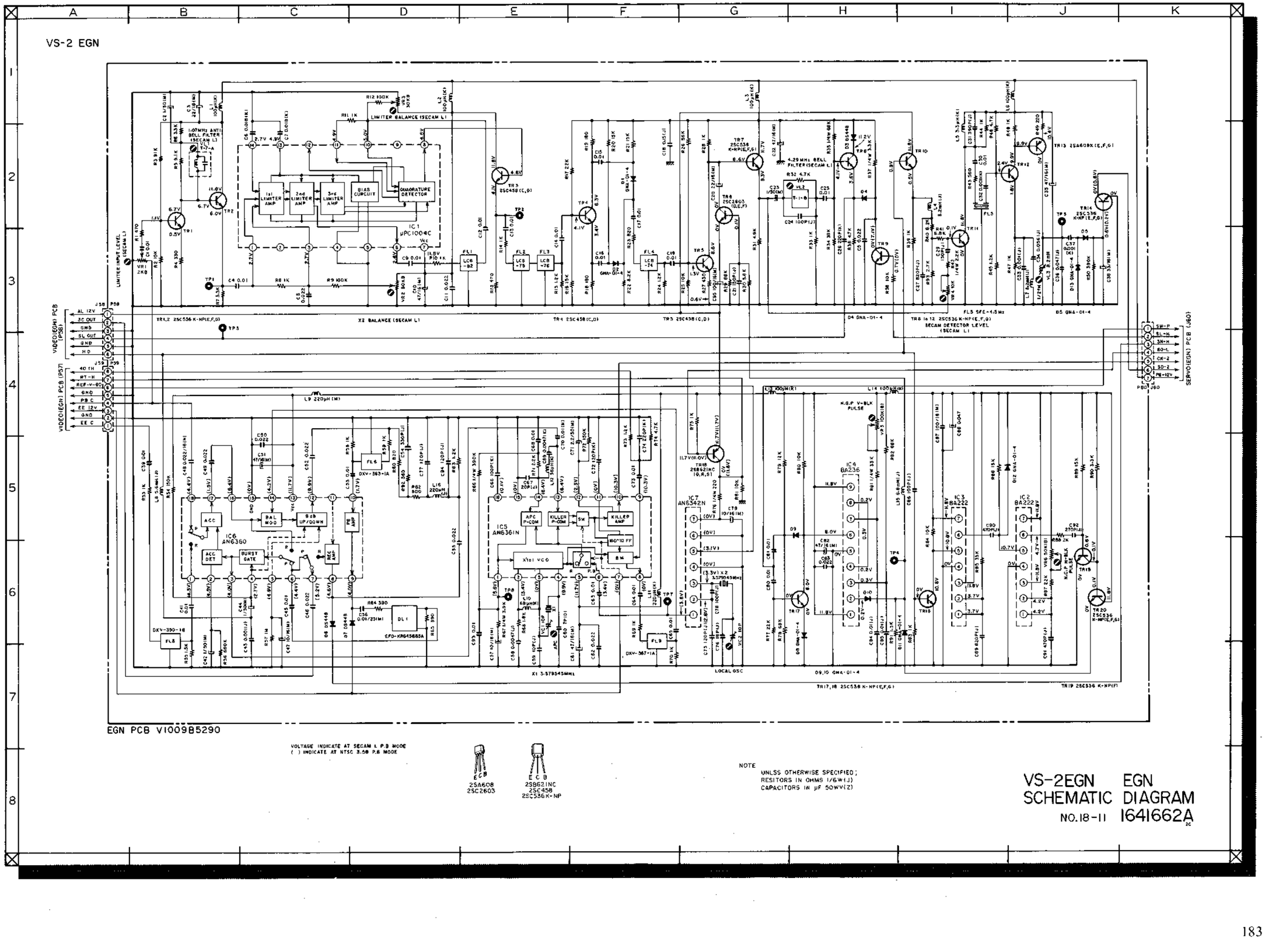
WARNING: ⚠INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY,
REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S
RECOMMENDED PARTS

AVERTISSEMENT: ⚠ INDIQUE LES COMPOSANTS CRITIQUES DE SÉCURITÉ
POUR MAINTENIR LE DEGRÉ DE SÉCURITÉ DE L'APPAREIL
NE REMPLACER QUE DES PIÈCES RECOMMANDÉES PAR LE FABRICANT

VS-2EGN
CONNECTION DIAGRAM
NO.18-9 1641660A


VS-2EGN
VS-2EGN VIDEO(EGN)
SCHEMATIC DIAGRAM
NO.18-10 164166IA

VS-2 EGN



VOLTAGE INDICATE AT SECAM L P.B MODE
( ) INDICATE AT NTSC 3.58 P.B MODE

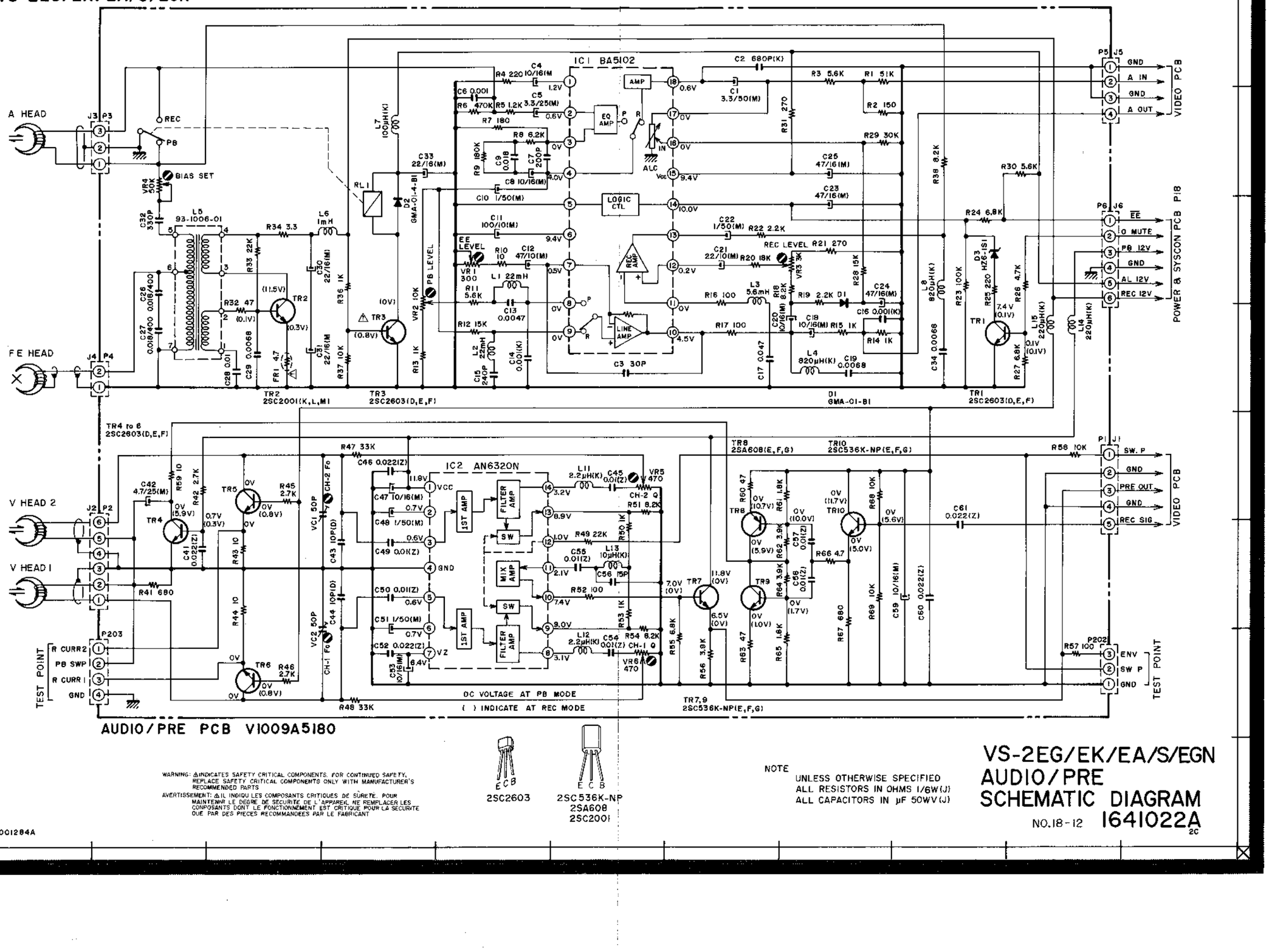
E C B
2SA608
2SC2603

E C B
2SB621NC
2SC458
2SC536K-NP

NOTE
UNLSS OTHERWISE SPECIFIED;
RESITORS IN OHMS 1/6W(J)
CAPACITORS IN μF 50WV(Z)

VS-2EGN EGN
SCHEMATIC DIAGRAM
NO.18-11 1641662A

VS-2EG/EK/EA/S/EGN



AUDIO/PRE PCB V1009A5180

WARNING: ⚠INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS

AVERTISSEMENT: ⚠ IL INDIQU LES COMPOSANTS CRITIQUES DE SÛRETÉ. POUR MAINTENIR LE DEGRÉ DE SECURITÉ DE L'APPAREIL NE REMPLACER LES COMPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SECURITÉ QUE PAR DES PIECES RECOMMANDEES PAR LE FABRICANT

001284A

E C B
2SC2603

E C B
2SC536K-NP
2SA608
2SC2001

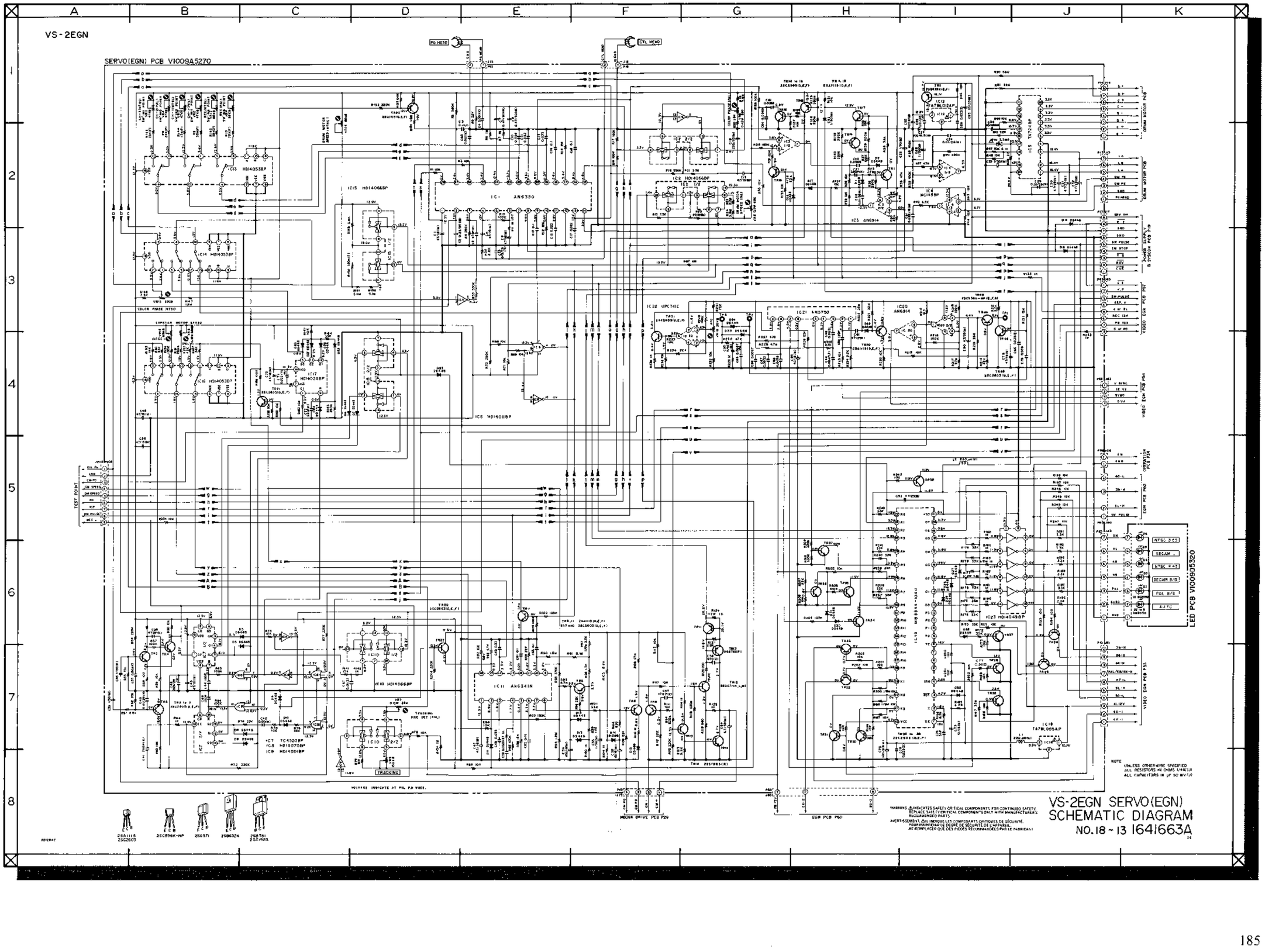
NOTE
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS IN OHMS 1/6W(J)
ALL CAPACITORS IN μF 50WV(J)

VS-2EG/EK/EA/S/EGN
AUDIO/PRE
SCHEMATIC DIAGRAM

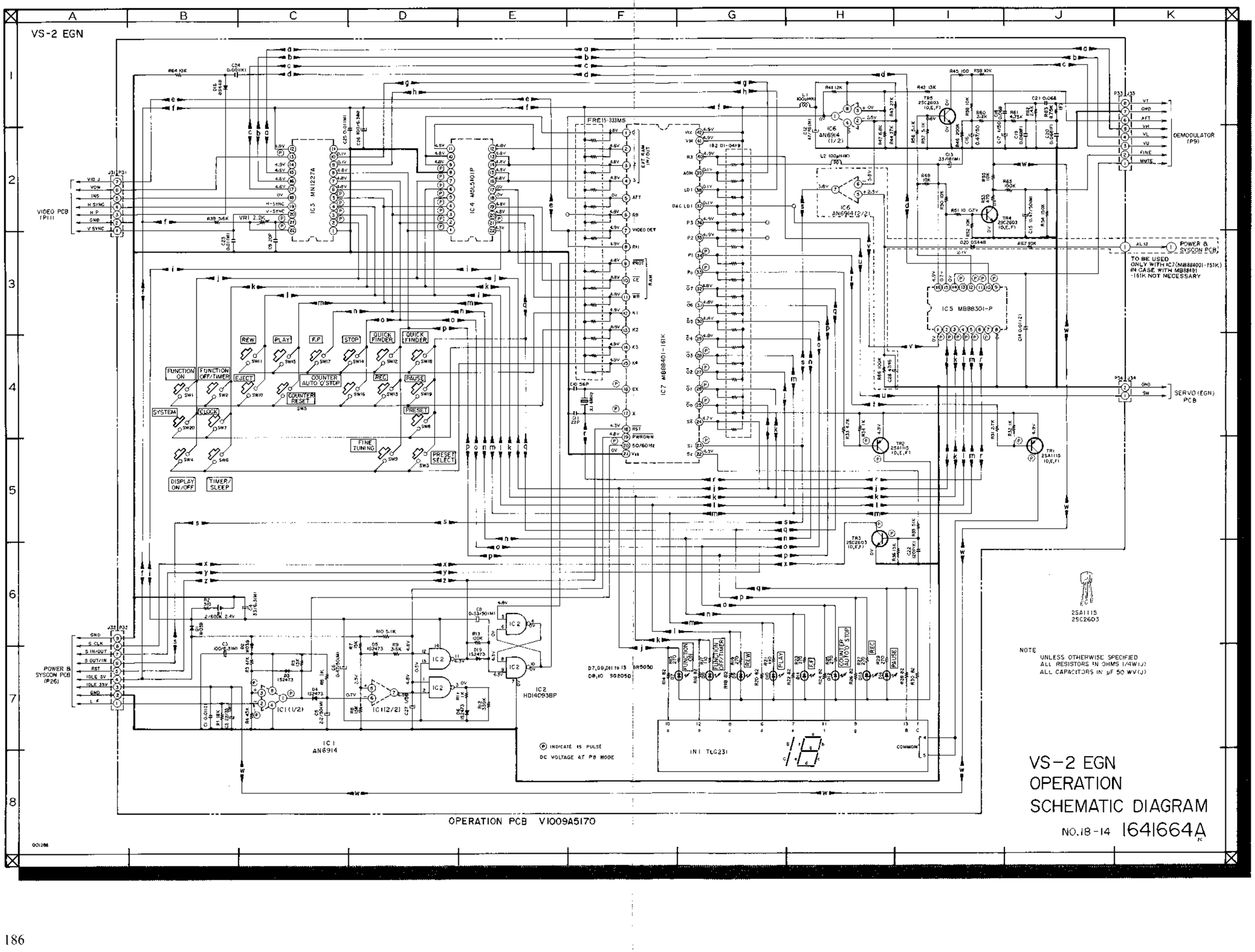
NO.18-12 1641022A 2C

VS-2EGN

SERVO(EGN) PCB V1009A5270



VS-2 EGN


VIDEO PCB (P11)
POWER & SYSCON PCB (P26)
DEMODULATOR (P9)
SERVO (EGN) PCB
TO BE USED ONLY WITH IC7(MB88401-151K) IN CASE WITH MB88481 -161K NOT NECESSARY
IC1 AN6914
IC2 HD14093BP
IC3 MN1227A
IC4 M5L5401P
IC5 MBB8301-P
IC6 AN6914 (1/2)
IC7 MBB8401-161K
IN1 TLG231
TR1 2SA1115 10,E,F1
TR2 2SA1115 10,E,F1
TR3 2SC2603 10,E,F)
TR4 2SC2603 (D,E,F1
TR5 2SC2603 10,E,F)
REW
PLAY
F.F
STOP
QUICK FINDER
QUICK FINDER
FUNCTION ON
FUNCTION OFF/TIMER
EJECT
COUNTER AUTO Q'STOP
COUNTER RESET
REC
PAUSE
SYSTEM
CLOCK
PRESET
FINE TUNING
PRESET SELECT
DISPLAY ON/OFF
TIMER/ SLEEP
INDICATE IS PULSE
DC VOLTAGE AT PB MODE
NOTE
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS IN OHMS 1/4W(J)
ALL CAPACITORS IN µF 50 WV(J)
2SA1115
2SC2603
OPERATION PCB V1009A5170
VS-2 EGN
OPERATION
SCHEMATIC DIAGRAM
NO.18-14 1641664A

VS-2EG/EK/EA/EGN

POWER & SYSCON PCB V1009A5190

REMOCON TERMINAL

SENSOR PCB

DEMODULATOR PCB

BOOSTER

OPERATION PCB

MECHA DRIVE PCB

SERVO PCB

DRUM HEATER (HTS01)

AUDIO/PRE PCB

OPERATION PCB

VIDEO PCB

TRANSFORMER

DC VOLTAGE AT PB MODE

2SA875 2SA490 2SB632 2SD612 2SA1115 2SB764 2SD863

WARNING: ⚠ INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS.

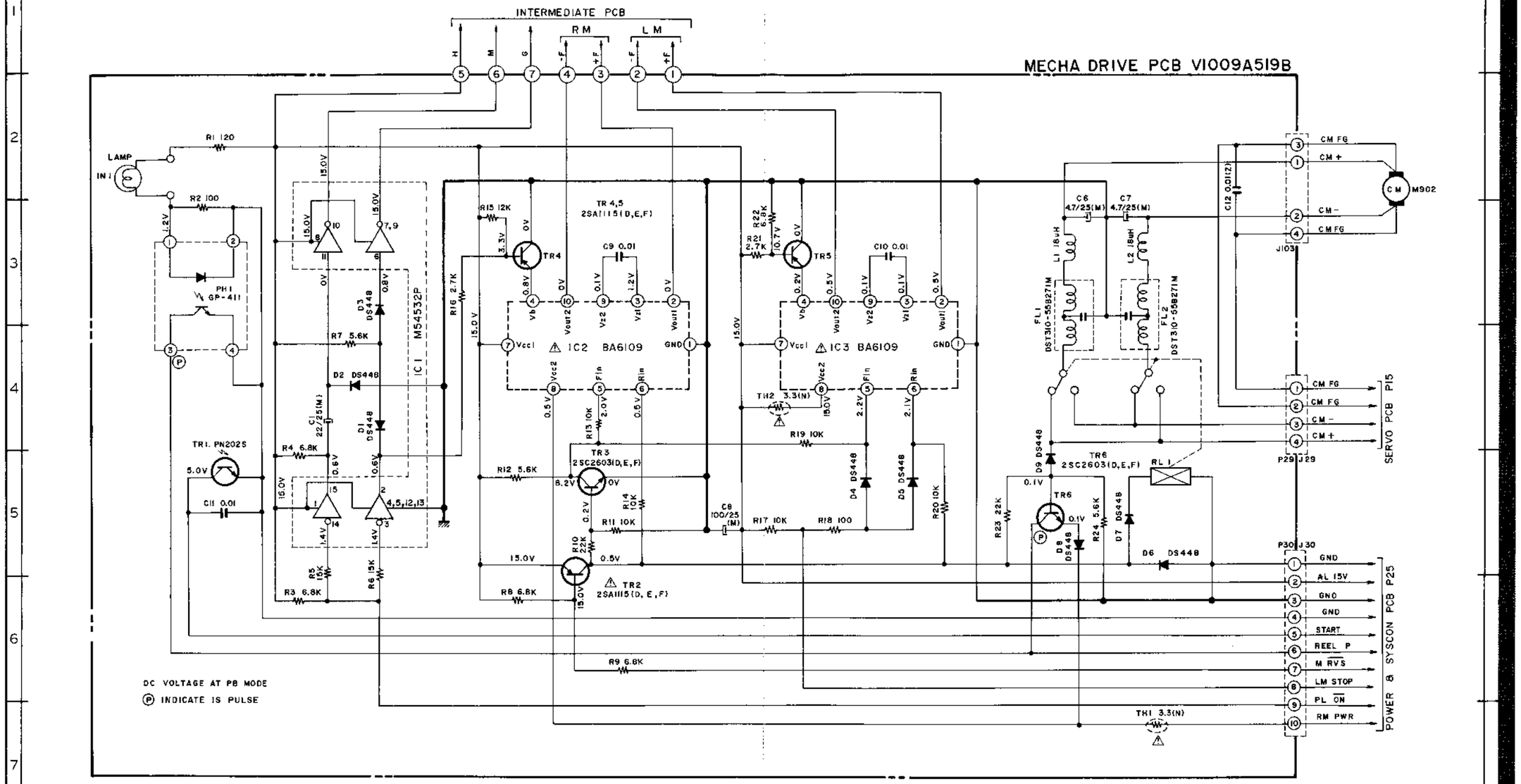
AVERTISSEMENT: ⚠ IL INDIQUE LES COMPOSANTS CRITIQUES DE SÉCURITÉ POUR MAINTENIR LE DEGRÉ DE SÉCURITÉ DE L'APPAREIL, NE REMPLACER QUE DES PIÈCES RECOMMANDÉES PAR LE FABRICANT

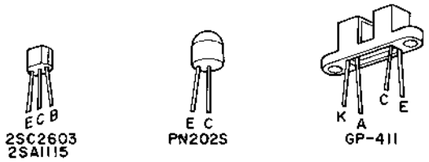
NOTE
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS IN OHMS 1/4W (J)
ALL CAPACITORS IN μF 50 WV (J)

VS-2SEG/EK/EA/EGN POWER & SYSCON SCHEMATIC DIAGRAM

NO.18-15 1641025B

VS-2 EG/EK/EA/S/EGN





WARNING: ⚠INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS.

AVERTISSEMENT: ⚠IL INDIQU LES COMPOSANTS CRITIQUES DE SÛRETÉ. POUR MAINTENIR LE DEGRÉ DE SECURITÉ DE L'APPAREIL NE REMPLACER LES COMPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SECURITÉ QUE PAR DES PIÈCES RECOMMANDEES PAR LE FABRICANT

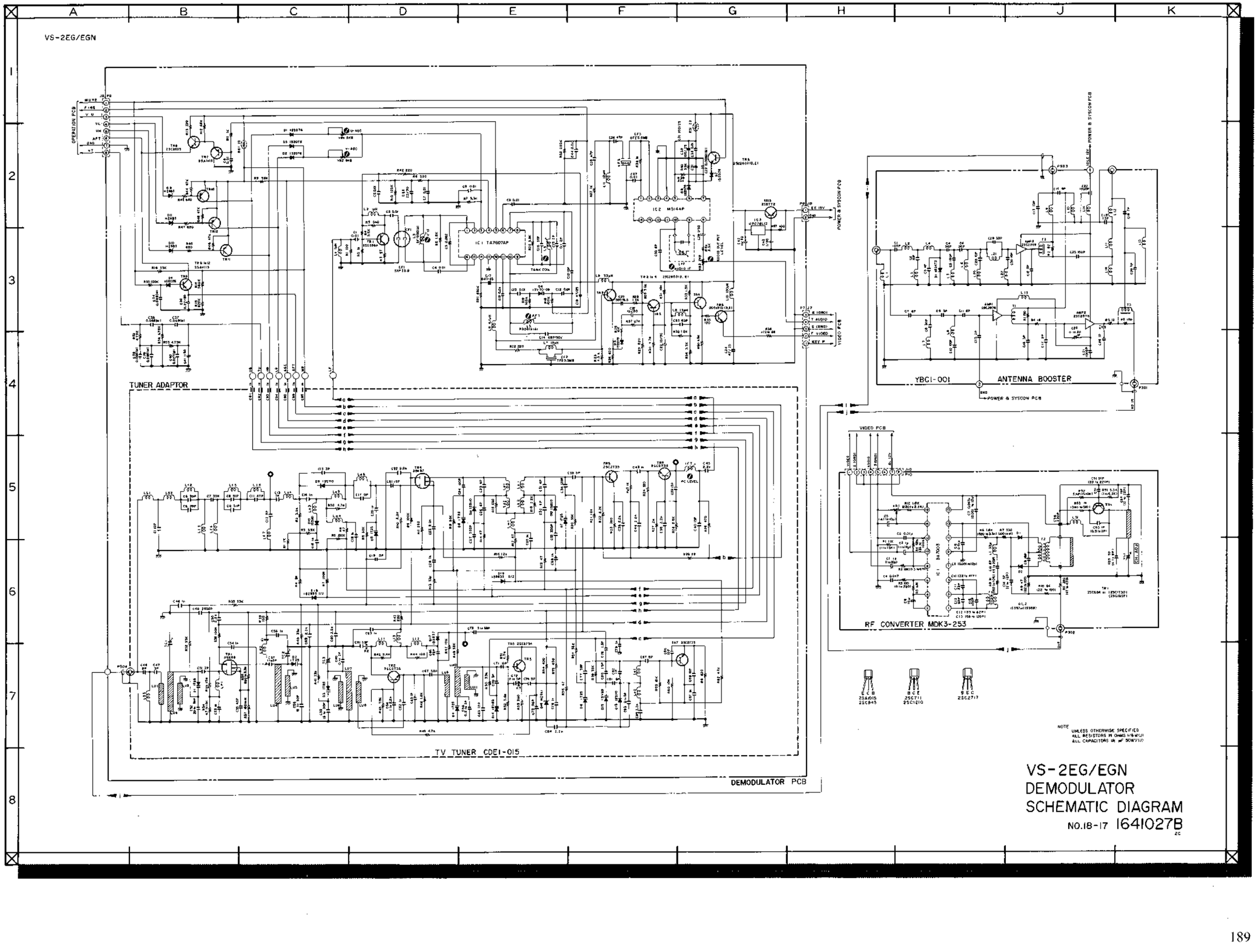
NOTE
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS IN OHMS 1/4W(J)
ALL CAPACITORS IN μF 25WV(J)

VS-2 EG/EK/EA/S/EGN MECHA. DRIVE SCHEMATIC DIAGRAM

NO.18-16 1641026B 2C

001288

VS-2EG/EGN



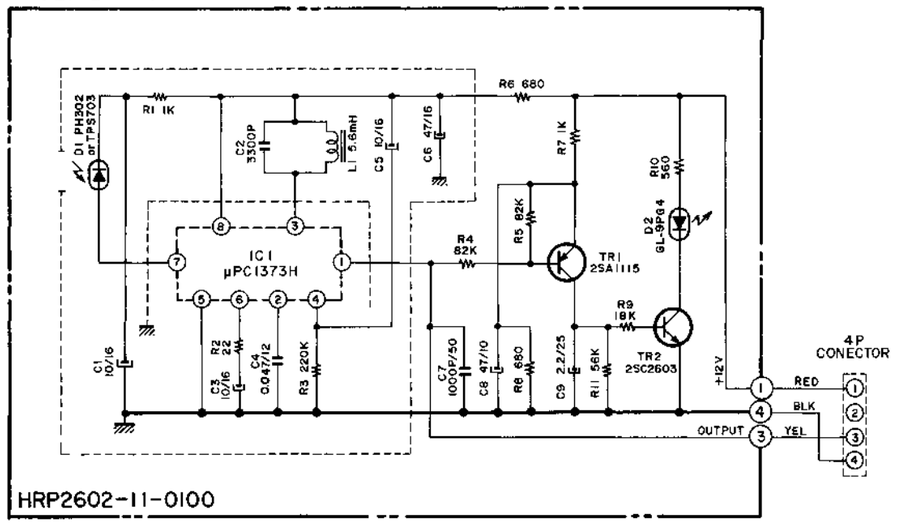
VS-2EG/EGN
DEMODULATOR
SCHEMATIC DIAGRAM

NO.18-17 1641027B
2C

RC-V202

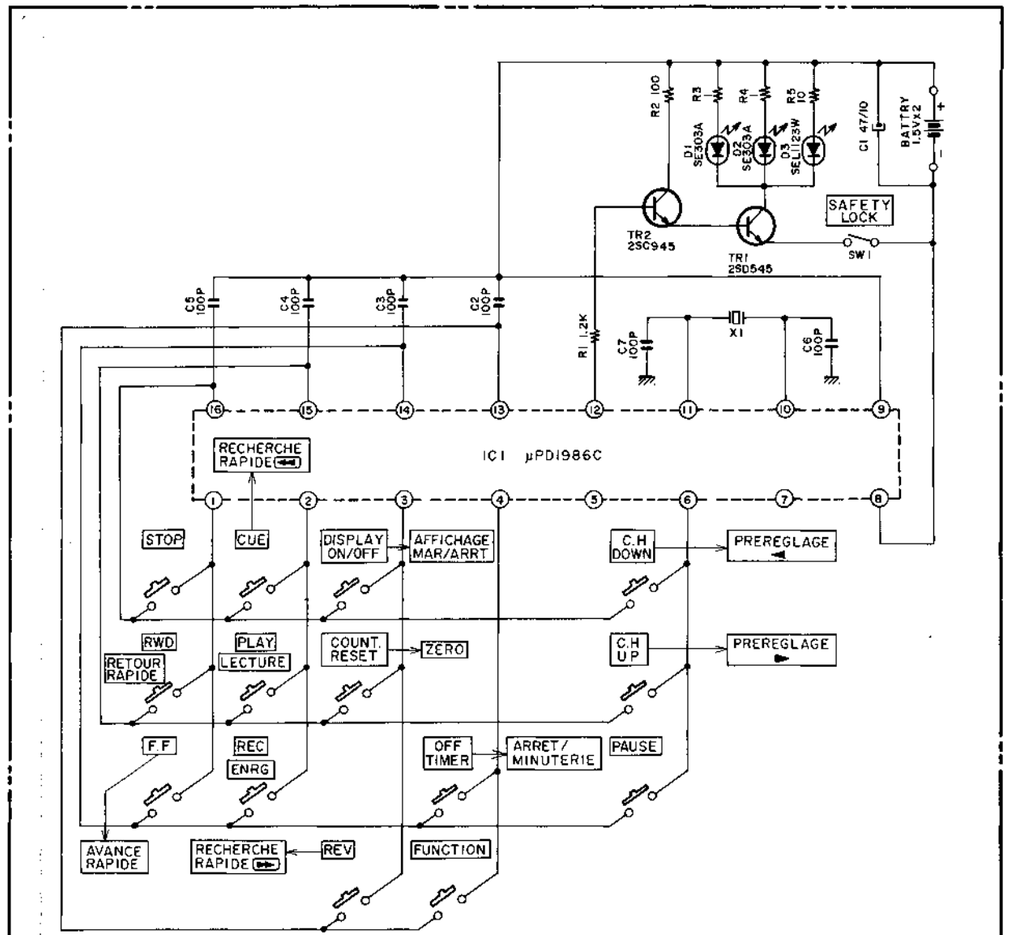
KONRAD VIETZKE
IN DER HALDE 7
1000 BERLIN 33
TELEFON 030/832 41 43

RECEIVER RC-R2

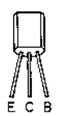


HRP2602-11-0100

TRANSMITTER RC-T2



2SA1115
2SC2603



2SD545
2SC945

RC-V202
REMOTE CONTROL UNIT
SCHEMATIC DIAGRAM

NO.18-18 1641030B